Characterization and modelling of GaAs MESFETs in the design of nonlinear circuits

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Abstract

The emergence of the MMIC as a cost effective, compact and enabling technology has increased the need for accurate CAD software. The performance of nonlinear MMICs must be evaluated during design using computer simulation, since they cannot be tuned after fabrication. Simulation relies upon accurate large-signal models for circuit components and this project involves the development of the GaAs MESFET large-signal model. In this work, the model is empirical and is derived entirely from characterizing S-parameter measurements over a range of bias levels and frequencies.

Small-signal equivalent circuits are calculated from each set of S-parameter measurements and the nonlinear model is constructed from the complete set of equivalent circuits. Frequency dispersion in the conductances of the MESFET creates differences in the device characteristics at low and high frequencies. Extra nonlinear elements have been therefore added to the nonlinear model, to account for these effects.

A series of MMIC circuits have been designed. Nonlinear measurements have been made and are compared with time domain simulations using the nonlinear model. Results indicate that this modelling approach is more accurate than one based on DC measurements, which does not account for the effects of frequency dispersion.

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List of Symbols

a_{ij}	Chebyshev polynomial coefficient
b_{ij}	Standard polynomial coefficient
C_{dc}	Dipole capacitance
C_{ds}	Drain-source capacitance
C_{dg}	Depletion region drain-gate capacitance
C_{gs}	Depletion region gate-source capacitance
C_o	Linear capacitance in definition of nonlinear capacitance
C_{open}	Capacitance of open circuit standard
C_i	Capacitance in region i of channel
C_x	Parallel capacitance for R_x
E	Total error in optimizing function
f	Frequency
g_m	Transconductance
g_o	Output conductance
I_{ch}	Current flowing through channel of MESFET
I_{ds}	Channel current
I_{dss}	Channel current at V_{gs}=0.0V
I_{subs}	Current flowing through substrate of MESFET
l	Length of transmission line
L	Degree of fit in V_{ds}
L_d	Drain inductance
L_g	Gate inductance
L_s	Source inductance
L_{short}	Inductance of short circuit standard
K	Degree of fit in V_{gs}
K_{eff}	Effective permittivity
P_{opt}	Optimum power point in load-pull curve

Q_{dg}	Drain-gate charge
Q_{gs}	Gate-source charge
R_d	Drain resistance
R_{dc}	Resistance at DC
R_{ds}	Output Resistance
$R_{ds'}$	Output resitance calculated from I_{ds}
R_g	Gate resistance
R_i	Intrinsic resistance
R_{rf}	Resistance at RF
R_s	Source resistance
R_x	Nonlinear output dispersive resistor
S	Normalized sensitivity
S_{ij}	2-port S-parameter
T_i	i'th order Chebyshev polynomial
τ	Time delay
V_{gs}	External gate-source voltage
$V_{gs'}$	Internal gate source voltage
V_{dg}	External drain-gate voltage
$V_{d'g}$	Internal drain-gate voltage
V_{ds}	External drain-source voltage
$V_{d's'}$	Internal drain-source voltage

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CHAPTER ONE - Introduction

1.1 Background

Microwave technology has developed continuously since its inception around 50 years ago. One of the most significant of these developments has been the emergence of solid state microwave components. Gunn and IMPATT diodes, which first appeared during the 1960's, resulted from the progress in semiconductor manufacturing and the production of new semiconductor materials.

Around the same time, low loss dielectric materials like Alumina and PTFE were developed, making possible the manufacture of compact microwave transmission media, such as microstrip and stripline. Solid state components mounted onto dielectric substrates formed hybrid microwave integrated circuits (HMICs). These were used to build low-noise amplifiers, power amplifiers, oscillators, mixers and phase shifters, all of which were considerably smaller than existing waveguide technology.

Solid state active devices which gave useful gain at microwave frequencies were slower to develop and it was not really until the gallium arsenide metal semiconductor field effect transistor (GaAs MESFET) was developed that useful gain could be obtained at more than a few GHz. The first FET was proposed in 1952 by Shockley [1] and was called the junction FET (JFET), but it was not a practical proposition until the early 1960's, due to problems associated with surface states. The silicon JFET was the first practicable field effect transistor to be produced and appeared on the market around the same time as the h.f. and u.h.f. bipolar transistor. The silicon metal oxide semiconductor FET (MOSFET) resulted from the developments in semiconductor manufacturing technology and the need for devices with lower energy consumption in highly integrated circuits.

As semiconductor technology matured in the early 1970s and progress was made with research on III-V compounds, gallium arsenide Schottky barrier FETs first appeared. These outperformed the existing silicon bipolar technology at higher frequencies with better noise figures. This new device was known as the metal semiconductor FET (MESFET). Compared with the well-established bipolar silicon technology, diodes and the travelling wave tube, the benefits of the MESFET were slow to reach the attention of the microwave market. This was partially due to material problems which prevented stable devices from being produced. Laboratories unfamiliar with GaAs technology also attempted, with mixed success, to build one-micron gate length devices which were at the limits of the existing photolithography.

Research work persisted, led by Hewlett-Packard [2], IBM and Plessey, and by 1976 the FET market had developed to a point where it could no longer be ignored. One of the first commercial MESFETs to become available was the NEC 244, launched in 1975 and offering a gain of 9.5dB at 10.0GHz. By 1987 monolithic amplifiers were being reported with gains in excess of 24.0dB across a bandwidth of 0.5-6.0 GHz [3]. GaAs MESFETs have now developed to the point that they are produced in large volumes for consumer products, such as satellite T.V. low-noise downconverters.

The first power FET was made by Fujitsu in the mid-seventies [4] and demonstrated 2.7W at 6GHz with a 6.0dB gain. By 1987 power FETs were reported with a gain of 4.3dB and an output power of 1.1W at 20.0GHz [5]. Research into the GaAs MESFET is still in progress and some laboratory results indicate its usefulness at 60GHz and beyond.

The concept of the monolithic microwave integrated circuit (MMIC) was first conceived in the mid-1960's and was seen as an obvious

development of the HMIC. The MMIC required the integration of active and passive components on the same substrate, offering reduced size and cost over HMICs. Attempts were made at building MMICs using silicon and silicon-on-sapphire bases but the problems of silicon's high resistivity, substrate losses and the silicon-sapphire interface restricted the effectiveness of these approaches.

By the early eighties, improvements in GaAs crystal growth techniques had finally made the commercialization of MMICs possible. The earliest successful MMICs [6,7] were narrowband amplifiers but applications quickly grew to cover almost all functions in microwave systems. There were a number of advantages of using the new MMIC technology in preference to the existing discrete microwave circuitry. MMICs were of greatly reduced size and weight and consumed less power. Once the design methods had been firmly established, unit costs could fall dramatically, allowing for the mass-production of many different types of circuit. Because all parts of a circuit could be integrated on the same substrate, the MMIC could give very reproducible performance as interconnect parasitics were reduced and a more broadband performance than HMICs was obtainable. By 1988, many MMIC designs had been published, including a K-band multistage power amplifier [8] with an output power of 1.33 W and a gain of 26.2 dB at 19.0 GHz.

The MMIC can be used in a wide variety of microwave circuit applications, replacing HMIC technology and acting as an enabling technology for designs which on HMICs would be too expensive, bulky and impractical to implement. An example of the enabling power of MMICs is the phased array radar. MMICs have so far been used to design small-signal, broadband, distributed and power amplifiers, although linear designs have been more successful.

MMICs have also been used to design switching and control circuitry. Tajima *et al* [9] have developed a voltage controlled attenuator with an operating frequency range of 2.0-18.0 GHz. MMIC switches have been designed for use in antenna transmit-receive modules, phase modulators and communications systems. Active and passive phase shifters have also been designed on MMIC [10]. The design of MMIC oscillators has been limited to date by the poor models for active devices in nonlinear CAD software which are available, whereas mixers have been successfully implemented [11,12].

Multifunction MMICs have also been produced, allowing for the integration of amplifiers, mixers, switches and phase shifters on the same chip. For example, a number of single chip Direct Broadcast Satellite (DBS) receivers have been realised on MMIC [13,14]. MMICs have also been designed for instrumentation, marine radars and land-mobile telephones [15].

Another trend over the past decade has been the increasing importance placed on CAD for microwave circuit design. Traditionally, HMICs were built using simple design procedures and were optimized by exercising the 'black-art' of tweaking. Post-fabrication 'tuning' was used, largely because the parasitics were not known or modelled effectively. Sometimes the circuits were designed with assistance from CAD programmes and as they could be tuned after fabrication, repeatable device models were often inaccurate and incomplete. Unlike the HMICs however, the MMIC could not be tuned after fabrication and require CAD with accurate models so that MMICs could be designed on a 'right-first-time' basis. Modelling of MMICs is made more complex because of their reduced physical size which creates field leakage and increases the coupling effects between different parts of the circuit [15].

A number of CAD programs became available during the early eighties [16,17]. Many were originally written for HMICs and were modified since the MMIC designs using older CAD systems tended to show poor yields. The modifications were made to satisfy the need for improved models of passive and especially active circuit components. Many programmes modelled passive components more successfully and contained accurate linear models for active devices. The major challenge lay in improving the nonlinear models needed for the CAD of power amplifier, mixer and oscillator designs.

1.2 The GaAs MESFET - Structure and Operation

Gallium arsenide is a group III-V compound offering several advantages over silicon for MESFET fabrication. High quality GaAs substrates offer better insulating properties than silicon, leading to lower parasitics and a resistivity in excess of $10^7\Omega$-cm. It also has a much higher electron mobility of 8900 $cm^2/V/s$ (at 300 K) compared with 1500 $cm^2/V/s$ for N-type silicon [18]. The saturation velocity for doped GaAs (10^7 cm/s) is similar to silicon but occurs at a lower field threshold (3500 V/cm compared with 10000 V/cm for Si). This gives rise to steeper current saturation characteristics for the GaAs MESFET than for the silicon JFET. Current-gain bandwidths are about two to three times higher and the maximum frequency of oscillation three times higher in GaAs as opposed to silicon.

The basic structure for the gallium arsenide MESFET is given in Figure 1.1. Basically, it consists of a semiconductor resistor, where the cross section of the channel is modulated by a Schottky barrier gate. The source and drain are ohmic contacts to the N-channel layer which is doped in the range of $10^{17}cm^{-3}$ to $10^{19}cm^{-3}$ [19] and the thickness of the N-channel layer

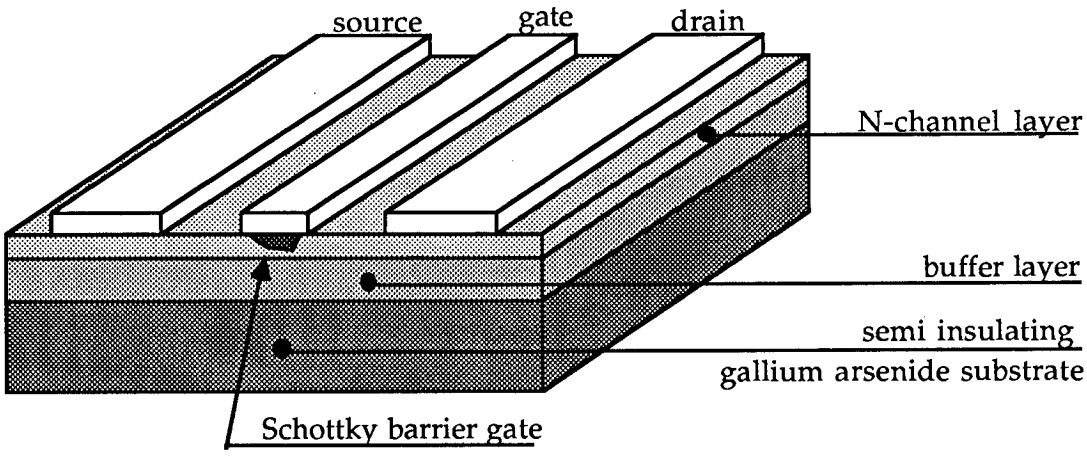


Figure 1.1: Structure of the GaAs MESFET

is around 0.1μm. As the device is used to switch or amplify signals in the microwave frequency range, the gate length has to be short.

When a voltage V_{ds} is applied between the source and drain such that the drain terminal is more positive than the source, an electric field is created, causing electrons to drift down the channel. As V_{ds} becomes more positive, the drift velocity of the electrons increase until the saturation drift velocity is reached. At this point the channel current begins to saturate, typically at V_{ds}=0.5V. Beyond this voltage, the current remains constant for an increase in V_{ds}.

The current is also affected by the gate voltage. A negative voltage applied to the gate terminal of the MESFET removes charge carriers under the gate area and this is known as the depletion region. The size of the depletion region can be increased by increasing the negative value of V_{gs}. Since this removes more charge carriers, the channel current will steadily drop until the pinchoff voltage is reached. Pinchoff voltage is defined as the gate voltage at which the depletion region has effectively blocked any current from flowing through the channel. The I/V curves for a typical FET are shown in Figure 1.2.

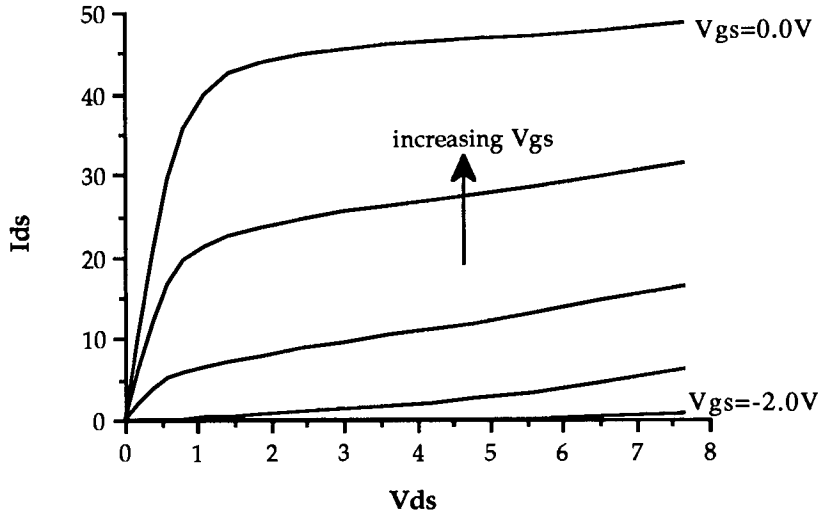


Figure 1.2: I/V characteristics for typical FET

1.3 Modelling MESFETs for CAD

The need for accurate CAD for MMIC design has already been discussed. In circuit simulation packages, active and passive components, losses in transmission lines, coupling effects and parasitics are represented by mathematical models. Although all circuit elements are ultimately nonlinear, most simulators assume that devices exhibit linear characteristics. In many cases, the linear assumption is quite valid, although not entirely correct. A resistor for example, can be modelled as a linear element in most applications. The resistor only appears to behave in a nonlinear manner when the current passing through it creates thermal effects, changing the value of the resistance. Additionally, GaAs MMIC resistors are nonlinear because charge velocity saturates with field strength. A nonlinear system is defined where the outputs vary with respect to the phase and amplitude of one or more vector input signals in a way which cannot be described by a simple linear expression.

Linear simulation programmes have been used for some time.

They are especially useful in the design of circuits such as small-signal amplifiers, which are weakly nonlinear and can be assumed to be linear. Other circuits however, such as mixers, rely on the nonlinearity of circuit components for their operation. The linear simulators are of little use in these cases, and nonlinear (or large-signal) simulators must be used instead.

There are a number of different types of nonlinear simulator most of which fall into one of four different categories [20], based on the way in which the circuit nonlinearities are calculated.

- Time domain simulators (for example SPICE) evaluate the transient and steady state responses of a circuit although they can be quite slow and may suffer from instability.

- Harmonic balance simulators use the time and frequency domains to solve nonlinear circuits. They only solve for the steady state response and are most useful when the excitation is only at one frequency.

- Some simulators use nonlinear transfer functions to analyse weakly nonlinear circuits, e.g. Volterra series.

- Describing-function methods use methods which change nonlinear systems to equivalent linear systems.

A more detailed discussion of large-signal simulators is given in Chapter Two.

1.4 The MESFET Equivalent Circuit

An equivalent circuit (or model) is used to describe the electrical characteristics of a MESFET. The model is found by making measurements of a device and proposing an equivalent circuit which, under simulation, produces similar results. A basic MESFET model is shown in Figure 1.3 comprising a total of ten elements; the model is also superimposed on the device structure [2] to illustrate the physical basis of the electrical model. C_{gs} and C_{dg} describe the charge stored in the depletion region between the gate and the channel. C_{dc} models the capacitance of the dipole layer. R_i and R_{ds} represent the effects of the channel resistance and R_s, R_d and R_g represent the bulk resistance of the N-layer and the contact resistance at the ohmic metallization in the source, drain and gate regions respectively. The current through the channel is modelled by a voltage controlled current source with a transconductance of g_m, where the control is the gate-source voltage.

The element values change with MESFET dimensions and doping concentrations, and some of these values also change with bias. Because the equivalent circuit is defined at a specified bias point, it can be considered to be a linear (or small-signal) model. The linear model is used in simulations when the signal voltages are small compared with the quiescent operating conditions.

Larger changes in the signal voltage alter the effective operating point of the device and hence the model element values. Under these conditions, the small-signal model becomes inadequate to describe the electrical behaviour of the MESFET and a nonlinear model must be used instead. As mentioned previously, there are a number of different methods of deriving nonlinear models but most are extensions of the basic

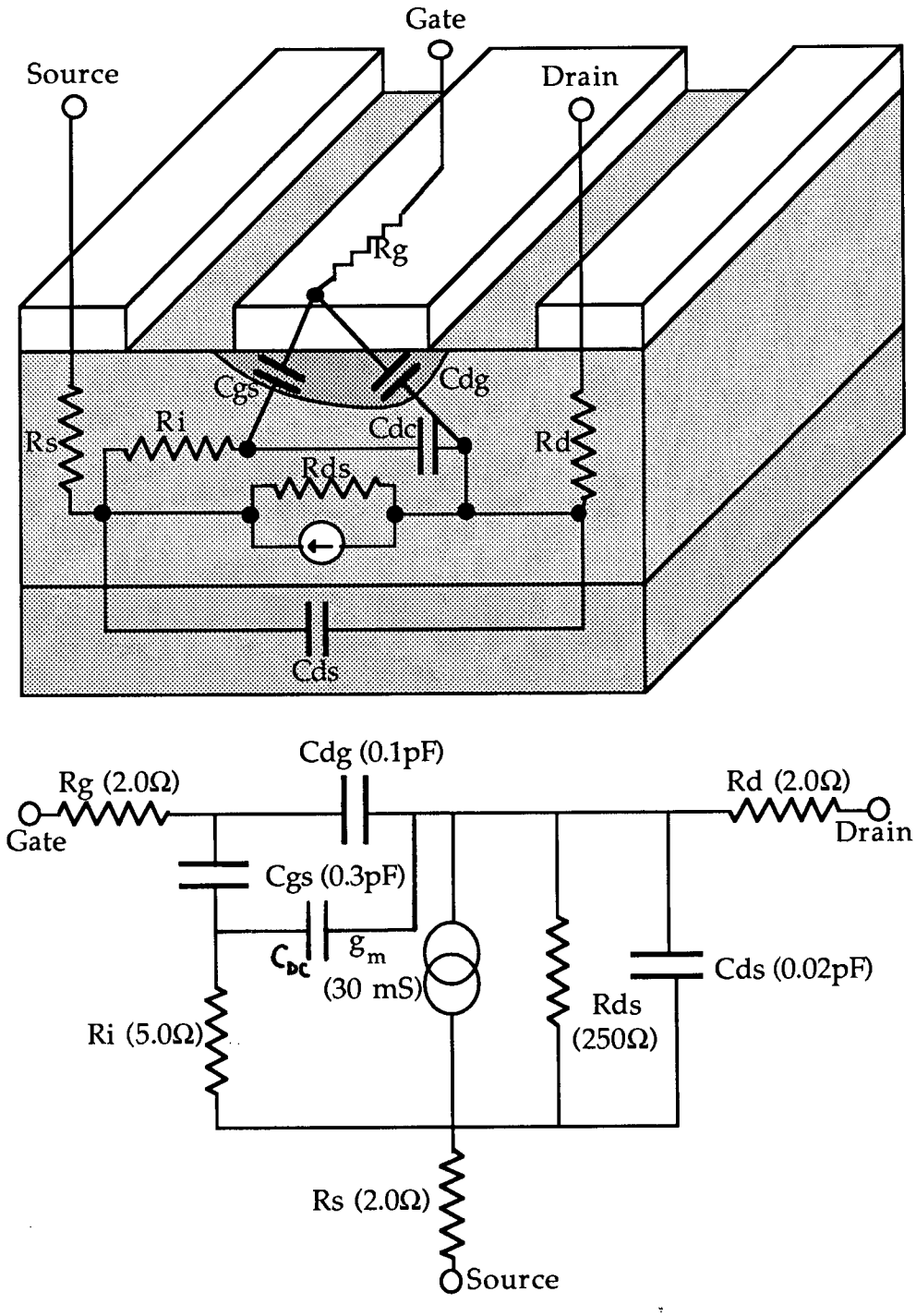


Figure 1.3: Basic FET equivalent circuit superimposed on device structure

small-signal model outlined in this section. A complete review of nonlinear models is given in Chapter Two.

In addition to predicting the electrical characteristics of MESFETs, equivalent circuits can also be used to establish the process parameters of fabrication, such as the doping profile and gate width. This is known as reverse modelling [21] and is particularly useful in diagnosing devices which have failed to meet specification. It is also used in process control monitoring and in the calculation of process yields.

1.5 S-parameters to Characterize the MESFET

Before a small-signal model is derived for the MESFET, it must be characterized. This is done by making a series of network measurements of the device, normally configured for common source operation and therefore modelled as a two-port device.

Impedance, admittance and hybrid parameters (Z,Y and h parameters) are often used by engineers to characterize devices at low frequencies. These parameters are expressed in terms of the input current and voltage I_1 and V_1 and the output current and voltage I_2 and V_2 (see Figure 1.4), where

Z-parameters;

$$V_1 = Z_{11} I_1 + Z_{12} I_2$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2$$

Y-parameters;

$$I_1 = Y_{11} V_1 + Y_{12} V_2$$

$$I_2 = Y_{21} V_1 + Y_{22} V_2$$

h-parameters;

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$V_2 = h_{21} I_1 + h_{22} V_2$$

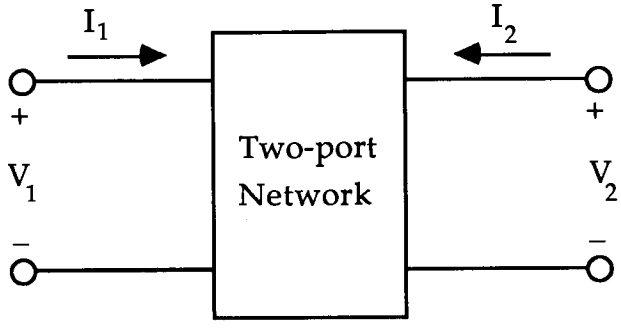


Figure 1.4: Two-port network for Z/Y/h parameters

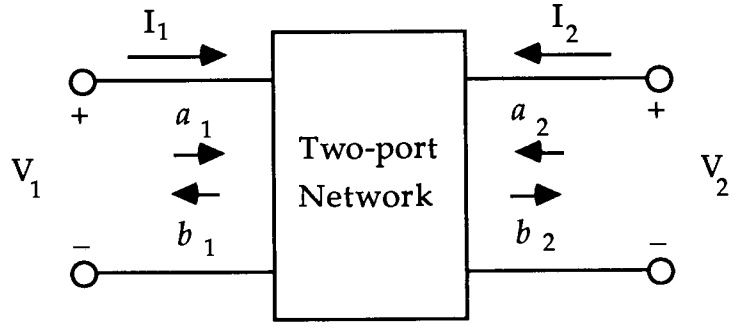


Figure 1.5: Two port network for S-parameters

For Z parameters, when the input parameter is being measured, the output circuit is open circuited. For example, $Z_{11} = V_1/I_1$ where $I_2=0$. Similarly for Y-parameters, a short circuit environment is required and for h parameters, both open and short environments are needed.

At high frequencies, the measurement of these parameters presents some problems. Broadband open circuits and short circuits are difficult to achieve at high frequencies because of the non-ideal nature of open and short connections. Active devices will often oscillate when connected to reactive loads such as open and short and direct measurement of voltage and current is very difficult at high frequencies. For these reasons, Z, Y and h parameters are not really suitable for characterizing microwave devices.

To overcome these problems, scattering parameters (S-parameters) are used to characterize high frequency networks. The voltage and current in a section of transmission line of length l are given as

$$V(x) = V^+ e^{-\gamma x} + V^- e^{+\gamma x}$$

$$I(x) = 1/Z_0 \{V^+ e^{-\gamma x} - V^- e^{+\gamma x}\}$$

where V^+ and I^+ are the incident voltage and current, and V^- and I^- are the reflected voltage and current. The equations are normalized by $\sqrt{Z_0}$ and the incident and reflected parameters a and b are defined by

$$a = V^+ e^{-\gamma l}/\sqrt{Z_0}$$

$$b = V^- e^{+\gamma l}/\sqrt{Z_0}$$

A two-port network is shown in Figure 1.5, where the S-parameters are defined by

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

where

$$S_{11} = b_1/a_2 \Big|_{a_{2=0}} \text{ (input reflection coefficient)}$$

$$S_{12} = b_1/a_2 \Big|_{a_{1=0}} \text{ (reverse transmission coefficient)}$$

$$S_{21} = b_2/a_1 \Big|_{a_{2=0}} \text{ (forward transmission coefficient)}$$

$$S_{22} = b_2/a_2 \Big|_{a_{1=0}} \text{ (output reflection coefficient)}$$

The S-parameters are found by making measurements on one port while the other port is terminated with a matched load. S-parameters can be converted to Z, Y, h or ABCD parameters using well-known equations [22]. The two-port S-parameters are conveniently measured on a network analyser and for accurate measurements the effects of connectors, lengths of transmission line, test jig and parasitics are removed using calibration techniques.

1.6 Outline of Project

In this chapter, the need to establish accurate nonlinear models for active devices has been noted, particularly as a result of the emerging MMIC technology. The following chapters of this thesis describe a new nonlinear model for GaAs MESFETs, which was developed so that power amplifier MMICs could be accurately modelled. A review of different nonlinear modelling techniques is presented in Chapter Two and from this review, a new nonlinear model is proposed, derived from sets of S-parameter measurements made at different bias points. The new model contains a novel aspect, in that importance is placed on the ability to model the changes in the characteristics of the MESFET with frequency. An

accurate nonlinear model can only be achieved with accurate measurements and Chapter Three describes methods used to make accurate S-parameters, including the need for good network analyser calibration. Once the S-parameter measurements have been made, a technique known as parameter extraction evaluates a small-signal equivalent circuit for each set of S-parameters and this is dealt with in Chapter Four. Chapter Five describes the way in which all of the information gathered in the previous chapter can be compressed into a nonlinear model. Finally, Chapters Six and Seven illustrate comparisons between simulations of the model and measurements of fabricated MMIC circuits. The results are discussed, further work is suggested and the final conclusions are drawn.

2.1 Introduction

In Chapter One, the need of accurate large-signal models of GaAs MESFETs for nonlinear circuit simulations was highlighted. The nonlinear model can be derived in a number of different ways and the purpose of this chapter is to review the merits of each different approach. It will be shown that the basic linear equivalent circuit can be expanded and adapted to model device nonlinearities.

Fundamentally, nonlinear modelling derives from one of two basic approaches. The model can be derived from theoretical considerations based on process parameters, such as device geometry and carrier concentrations. Another approach is to ignore the process information and instead derive the nonlinear model from a series of characterizing measurements. For this project, the latter of the two methods was chosen and the review therefore concentrates of this empirical type of modelling. The empirical model can be constructed without reference to process information and, for the fabrication process used in this project (at GEC Plessey Research (Caswell) Ltd.), no such information was readily available. An additional advantage of this method is that direct characterization of devices can lead to a more accurate model, since no assumptions need to be made about the physical operation of the device.

Following the review of nonlinear models, the effects of frequency dispersion are discussed. A difference between the performance of MESFETs at low and high frequencies has been widely observed [23-30] and the dispersive effects of the surface states on the FET are a major cause of this. Most commercially available nonlinear models do not specifically attempt to model these effects but the proposed model of this work is

designed to do this. The effects of frequency dispersion on the MESFET characteristics are discussed and techniques for modelling frequency dispersion are reviewed fully in Chapter Five.

The nonlinear model review illustrates that a number of different types of equivalent circuit have been used to model the MESFET. The final section in this chapter describes the topology of equivalent circuit that was chosen to represent the MESFET in this work. Also, in many of the existing models, some of the capacitive and resistive nonlinearities are omitted, or severely approximated. The proposed nonlinear model includes expressions for all of the major nonlinearities which are allowed for vary freely as functions of both the gate and drain biases.

2.2 Expanding the Linear Model to include Nonlinearities

The linear MESFET model can be used to accurately simulate device operation where the signal voltages are small compared with the static operating point. As the signal voltages rise, the linear assumption becomes increasingly less valid, because the signal voltages increasingly deviate from the static operating point, changing the characteristics of the device.

The values of some of the elements in the MESFET equivalent circuit (see Figure 1.3) do not change with bias and these are known as linear (or extrinsic) elements; the element values which change with bias are nonlinear (or intrinsic) elements. Generally, the elements g_m, R_{ds}, C_{gs}, C_{dg}, R_i and τ (time delay) are found to be intrinsic and functions which describe their behaviour with bias will be examined later in this chapter. The small-signal model linear transconductance (g_m) and the output conductance ($1/R_{ds}$) are the derivatives of the channel current with respect to the gate and drain voltages. In the large-signal model, these linear

elements must be replaced by an expression for the current, which varies with both gate and drain voltages. The bias dependence of the gate-source capacitance C_{gs}, the gate-drain capacitance C_{dg}, the intrinsic resistance R_i and the time delay τ are discussed in Chapter Four.

The large-signal model should include extra elements, not present in the linear model, to predict other nonlinear phenomena in the MESFET [30]. These are due to breakdown effects which occur at high voltage levels, or from forward biasing the gate-source Schottky diode. The gate-drain avalanche breakdown current occurs at high values of V_{dg} and the forward gate current occurs when a positive voltage is applied to the gate of the MESFET. Both of these currents substantially alter the characteristics of the device and will occur in many design applications, such as power amplifiers.

The existing model topologies have been derived by making certain assumptions. For simplicity all models have lumped elements where, in fact, distributed elements would be more appropriate. However, using distributed elements would increase the complexity of simulations and these are only needed to accurately predict model performance at very high frequencies. Many of the models also make the assumption that the characteristics of the device at a particular instant result from the voltage applied across the terminals at the same instant and this is known as the *quasi-static* assumption. However, the characteristics of the MESFET do not change immediately with voltage, which means that the quasi-static assumption degrades, to some extent, the accuracy of the large-signal model.

Ambient temperature and also thermal effects, caused by the drive levels in the device, will alter the characteristics of the device but no account is taken of temperature in either the small or large-signal models

and temperature effects will not be examined in this work.

2.3 Different Methods of Nonlinear Simulation

For any circuit, nonlinear behaviour can be defined where the output varies with the input and cannot be described by a linear expression. Linear circuits are generally solved in the frequency domain but this is not suitable for nonlinear characterization. In Chapter One, four different types of nonlinear analysis were listed: time domain, harmonic balance, Volterra series and describing functions. The following paragraphs describe the methods which are most often used to solve linear and nonlinear circuits.

A linear analysis of microwave circuits is most simply calculated in the frequency domain. Linear simulation techniques are well-established and have been implemented with great success on a number of simulation packages. Examples of such packages include SUPERCOMPACT [31], TOUCHSTONE [32] and MDS [33] which can all be run on personal computers, workstations and mainframes. In addition to circuit simulation, these packages have more recently offered optimization routines (which can be used to fit equivalent circuits to measurements), frequency sweeping, plotting algorithms and stability analysis. Many linear simulators can be linked to layout packages for MIC and MMIC mask design; for example, TOUCHSTONE can be used in conjunction with ACADEMY and linked to MICAD [34].

Time domain analysis is more suited to the solution of nonlinear circuits and involves solving a system of nonlinear equations with respect to time. The relationship between voltage and current in the time domain is specified for each circuit element which is solved using Kirchhoff's laws. Solutions are found over a transient period in steps of ∂t, where the size of

∂t is inversely proportional to the total solution time and the accuracy. The speed of solution is also affected by the complexity of the nonlinear circuit.

The disadvantage of time domain analysis is that all of the transients must be calculated to reach a solution, whereas in many cases only the steady-state solution is required. Often, the transient settling time (for example, of the bias circuit) can be many orders of magnitude greater than the basic RF period, leading to lengthy calculations. Another problem may occur where, for a given time step, a solution of Kirchhoff's law cannot be found and the solution fails to converge, usually caused by poorly defined nonlinear expressions. There are many time-domain simulators available including SPICE [35], ANAMIC [36], CIRCEC [37] and MICROWAVE SPICE [38].

Harmonic balance analysis is performed in both the time and frequency domains. The circuit is divided into linear and nonlinear sections: the linear section is solved most quickly in the frequency domain for each of N harmonics and the nonlinear section is solved separately in the time domain. Results are passed between the two sections by means of Fourier and inverse-Fourier transforms. Normally, simulation begins with an analysis of the linear system from the initial conditions. The solution of this analysis is used to perform an analysis of the nonlinear system and the results are passed back to the linear system once again. This iterative process continues until the error function between the two systems drops to an acceptably small level.

The speed efficiency of the harmonic balance method depends on the type of nonlinear circuit, the partitioning into linear and nonlinear blocks, the initial conditions and the number of harmonics which must be considered [39, 40]. It is usually quicker than time domain analysis but can become very complicated in applications where signals with more than

one frequency are considered. Several improvements to the harmonic balance method have been proposed [41, 39, 42] which have reduced the number of time domain calculations needed and increased the number of harmonics which can be considered. Harmonic balance simulators include LIBRA, MICROWAVE HARMONICA and MDS.

Nonlinear expressions can be described using Volterra series [43]. This is useful in systems which are only weakly nonlinear and where the input signal consists of a number of different frequencies. The Volterra series expansion has an advantage over the power series expansion, that nonlinear systems with memory can be analysed. It is particularly useful in circuits where higher harmonics can be ignored, although analysis becomes rather complicated in systems where this approximation cannot be made.

Describing functions are used to analyse systems where the level of nonlinearity is low. The nonlinear system is converted a number of linear systems (usually linear filters) which can be simply analysed in the frequency domain. The accuracy of the method is largely dependent on the error that exists between the nonlinear and equivalent linear systems. The main disadvantage of this method is that it can be difficult to transpose a nonlinear circuit into a number of linear circuits, especially when the nonlinearities are more pronounced.

2.4 Review of Large-Signal Modelling Techniques

2.4.1 Categorization

There are many ways to derive large-signal models for active devices, depending on the available data, the simulation software and the chosen theoretical approach. Four different categories are listed below, although a particular method may involve a combination of two or more

methods.

- Empirical models are derived from device measurements to produce a nonlinear model. The device is characterized using S-parameters, DC and pulsed I-V measurements, which are then interpreted to find the nonlinear components in the model.

- Semi-empirical models require some characterizing measurements and also some knowledge of the process parameters, like for example the MESFET gate dimensions and the channel doping concentration. These are the most commonly used commercial nonlinear models and are regarded as "industry standard".

- Analytical models are calculated from mathematical equations which describe the device physics, where certain assumptions have been made to simplify the calculations. Compared with empirical and semi-empirical models, the analytical models to date have been less accurate, mainly because the physical mechanisms controlling charge transport in the MESFET are not yet fully understood. The accuracy of the analytical model is also undermined by the assumptions and approximations which are made during derivation of the equations.

- The most complicated type of analysis is the numerical model. This type of modelling is computing intensive and requires detailed information about the material properties and device geometry. Because these equations require so much computer time to solve they are usually used by device physicists to understand device operation.

The following sections describe each of the above categories in more detail and illustrate each model with published examples. Some of the models are derived from pulsed I-V or DC measurements, zero-channel bias and low frequency S-parameter measurements. Many of the methods use parameter extraction techniques where the values of model elements are derived from S-parameter measurements. These topics are not included in this chapter but are discussed fully in Chapter Four. The techniques for the characterization and modelling of dual-gate FETs are similar to those used for single gate FETs and will not be covered in this work.

2.4.2 The Empirical Model

Empirical models are derived from device experimental measurements only, requiring no knowledge of any process parameters. The advantages of these models are that they are computer efficient and can be very accurate. The biggest disadvantage is that no correlation usually exists between the nonlinear model and physical parameters such as gate width, requiring new measurements to be made for each modelled device.

DC and pulsed I-V measurements can be used to characterize the channel current and breakdown effects in the MESFET. Alternatively, the current can be derived indirectly from S-parameter measurements. The remaining nonlinear parameters in the large-signal model can be established by characterizing the MESFET using S-parameter measurements, and extracting the linear and nonlinear parameters of the model from the measurements over a range of bias points [44].

One of the earliest large-signal modelling techniques was proposed

by Willing, Rauscher and de Santis [45] and is a purely empirical approach requiring no analytical or semi-analytical expressions. A device was characterized with S-parameter measurements over a range of bias points and parameter extraction (see Chapter Four) produced linear models for the MESFET at each bias point. Some of the element values in the model were found to vary with bias and were therefore nonlinear (or intrinsic). These were fitted to polynomial expressions where the nonlinearity was described as a function of the gate and drain voltages. The large-signal model shown in Figure 2.1 was verified using a time-domain analysis programme (SYSCAP) where the model was connected to purely resistive terminations. Under these conditions, the analysis was simplified and each of the nonlinear elements could be expressed as a function of only one control voltage.

In another paper [46], this technique was expanded. The instantaneous current through an element was defined as the product of the instantaneous element value and the instantaneous voltage. Nonlinear elements were expressed as either conductances (G) or capacitances (C), where the instantaneous current through them was defined as

$$i_G(t) = G\,[\,v_1(t)\,,\,v_2(t)\,]\,.\,v_G(t) \qquad (2.1)$$

$$i_C(t) = C\,[\,v_1(t)\,,\,v_2(t)\,]\,.\,\partial v_C(t)/\partial t \qquad (2.2)$$

Note that the time variable does not appear explicitly in the functions of G and C and any time dependence of these functions is due to the time dependence of v1 and v2 . Hence the nonlinear elements are functions of instantaneous voltages and this is known as the quasi-static assumption. If the currents and voltages are broken up into static and small-signal components

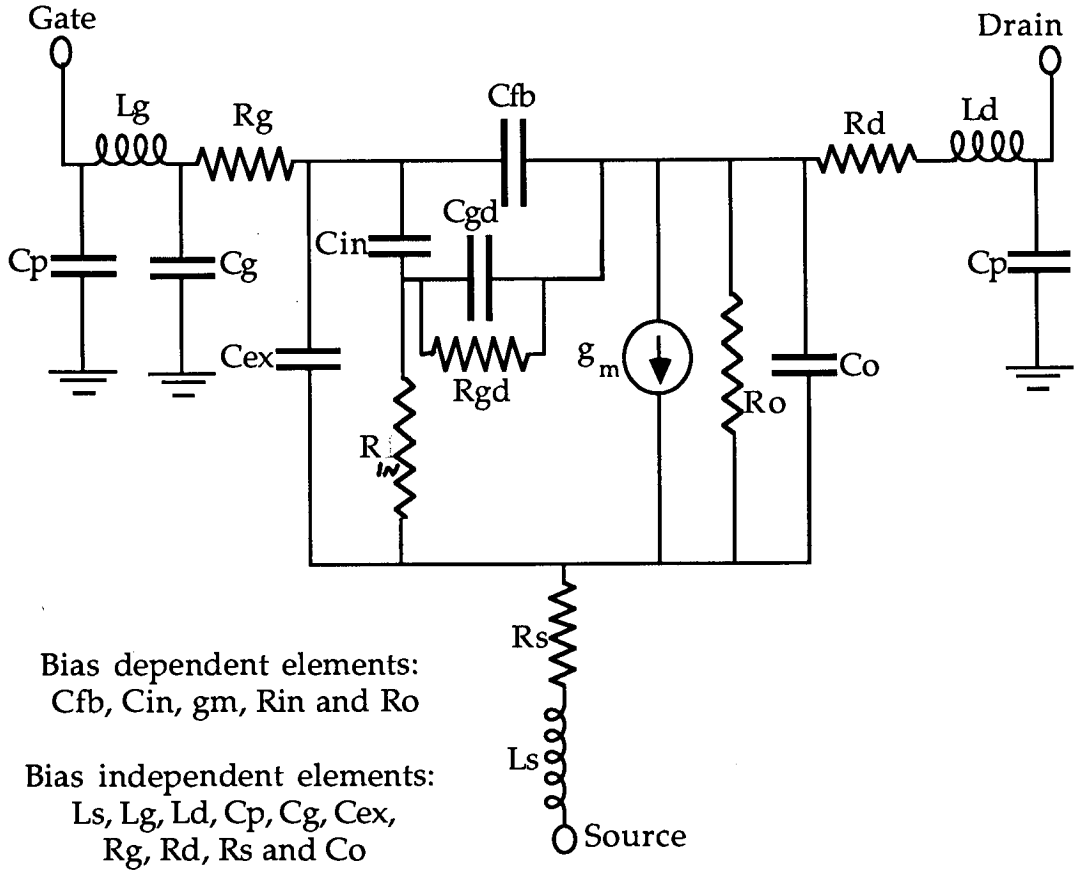


Figure 2.1: Empirical nonlinear model

$$i_G(t) = I_G + \underline{i}_G(t) \tag{2.3}$$

$$i_C(t) = I_C + \underline{i}_C(t) \tag{2.4}$$

$$v_G(t) = V_G + \underline{v}_G(t) \tag{2.5}$$

$$v_C(t) = V_C + \underline{v}_C(t) \tag{2.6}$$

I_G, I_C etc. represent static parameters whereas $\underline{i}_G$, $\underline{i}_C$ etc. represent small-signal dynamic quantities. It was suggested that

$$\underline{i}_G(t) = \underline{G}\,[\,V_1(t)\,,\,V_2(t)\,]\,.\,\underline{v}_G(t) \tag{2.7}$$

$$\underline{i}_C(t) = \underline{C}\,[\,V_1(t)\,,\,V_2(t)\,]\,.\,\partial\underline{v}_C(t)/\partial t \tag{2.8}$$

where $\underline{G}$ and $\underline{C}$ were the incremental values of conductance and capacitance and these parameters were found from small-signal S-parameter characterization. For all capacitances, $C = \underline{C}$. The transconductance and output conductance were assumed as partial derivatives of the current equation I_{ds} and the incremental conductances were simultaneously and partially integrated to produce two definitions of the current

$$I_{ds}(V_1,V_2) = I_0 + V_1.G_M(V_1,V_2) + V_2.G_O(0,V_2) \tag{2.9}$$

$$I_{ds}(V_1,V_2) = I_0 + V_1.G_M(V_1,0) + V_2.G_O(V_1,V_2) \tag{2.10}$$

where

$$G_M(V_1,V_2) = 1/V_1 \,.\int_0^{V1} \underline{G}_M(v,V_2)\partial v \tag{2.11}$$

$$G_O(V_1,V_2) = 1/V_2 \,.\int_0^{V2} \underline{G}_O(V1,v)\partial v \tag{2.12}$$

The current worked out from the two conductances was different and the final result was calculated as an average of the two.

A similar technique was used by Weiss and Pavlidis [47] to empirically characterize a MESFET and produce a large-signal model. The full model contained five nonlinearities: C_{gs}, R_{ds}, g_m, G_{gf} and G_{dg} (see Figure 2.2). The first three elements were found using parameter

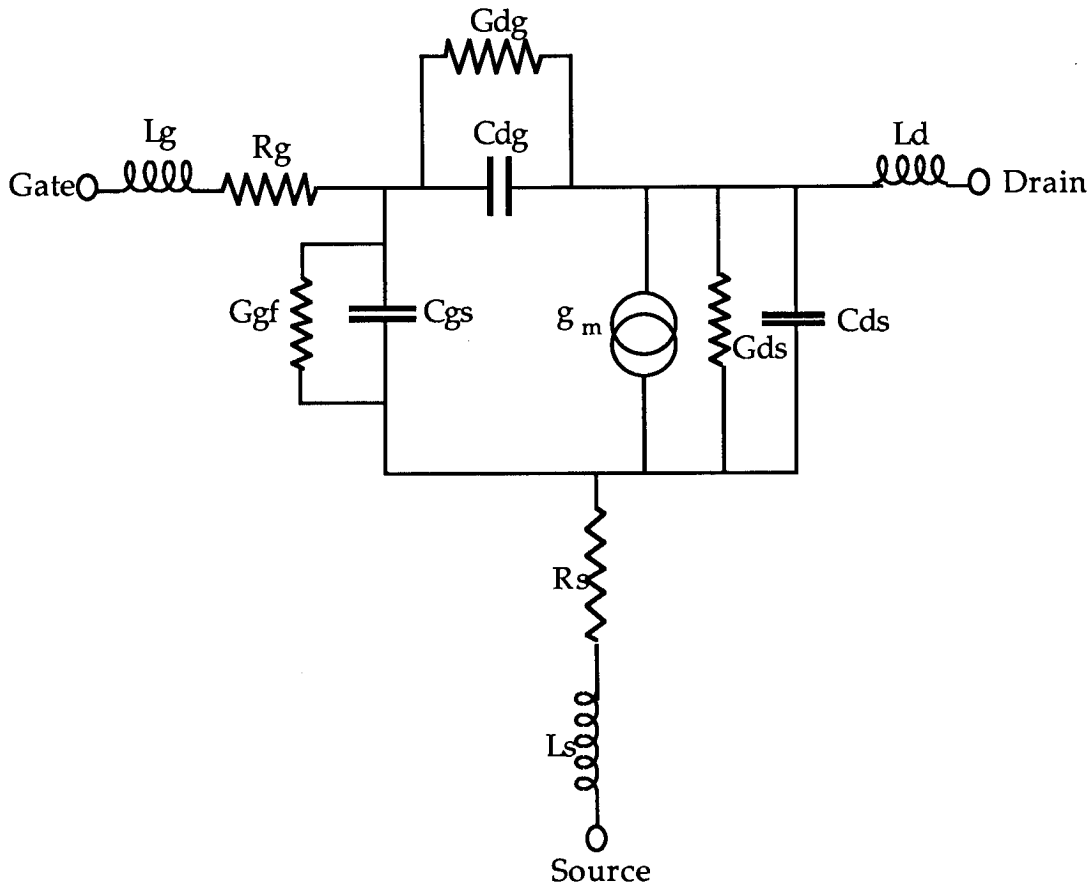


Figure 2.2: Large-signal model with five nonlinearities:
C_{gs}, R_{ds}, g_m, G_{gf} and G_{dg}

extraction from small-signal S-parameters. The other two elements described breakdown effects in the MESFET and were characterized with DC measurements.

The voltages in the circuit were expressed as combinations of static and dynamic components (2.5+2.6). The incremental conductances (G') and capacitances (C') related to their instantaneous counterparts by the equations

$$C = \int_0^{2\pi} \left[\int_0^{\omega t'} \left[-C' (V_{ds}, V_{gs}) \sin (\omega t + \phi) \right] \partial(\omega t') \right] . \cos (\omega t + \phi) \, \partial(\omega t) / \pi \quad (2.13)$$

$$G=\int_0^{2\pi} [\, G'(V_{ds}, V_{gs}) \cos(\omega t + \phi) \,] \cdot \partial(\omega t)/\pi \qquad (2.14)$$

An interesting aspect of the work was that the empirical model was compared with two other models, both of which are described later in this chapter. One of the models was semi-empirical and derived from Tajima's equations [48]. The other was analytical, combining Curtice's nonlinear current [49] with device physical equations. The empirical model was slightly more accurate than the semi-empirical model for predicting the power saturation curves of MESFET measurements and considerably more accurate than the analytical model.

Peterson *et al* [50] used an empirical technique to establish a large-signal model, illustrated in Figure 2.3 and showing the three main nonlinear currents of I_D, I_G and I_B. These were all assumed to be functions of the internal gate and drain voltages and were found using pulsed I-V measurements. The linear elements of R_G, R_D, R_S, L_G, L_D and L_S were found using DC characterization techniques. The capacitative elements and R_i were found from parameter extraction of small-signal S-parameters.

A series of complex simultaneous equations were derived using Kirchhoff's laws in the frequency domain. Expressing the nonlinearity of the currents in the frequency domain is very complex: time domain expressions for inductance and capacitance are also complex terms involving time integrals and differentials. Therefore the nonlinear currents were analysed in the time domain and the linear elements were analysed in the frequency domain using an iterative technique illustrated in Figure 2.4. This technique was also used to predict the large-signal behaviour of a MESFET modelled using the Curtice cubic current equation [51].

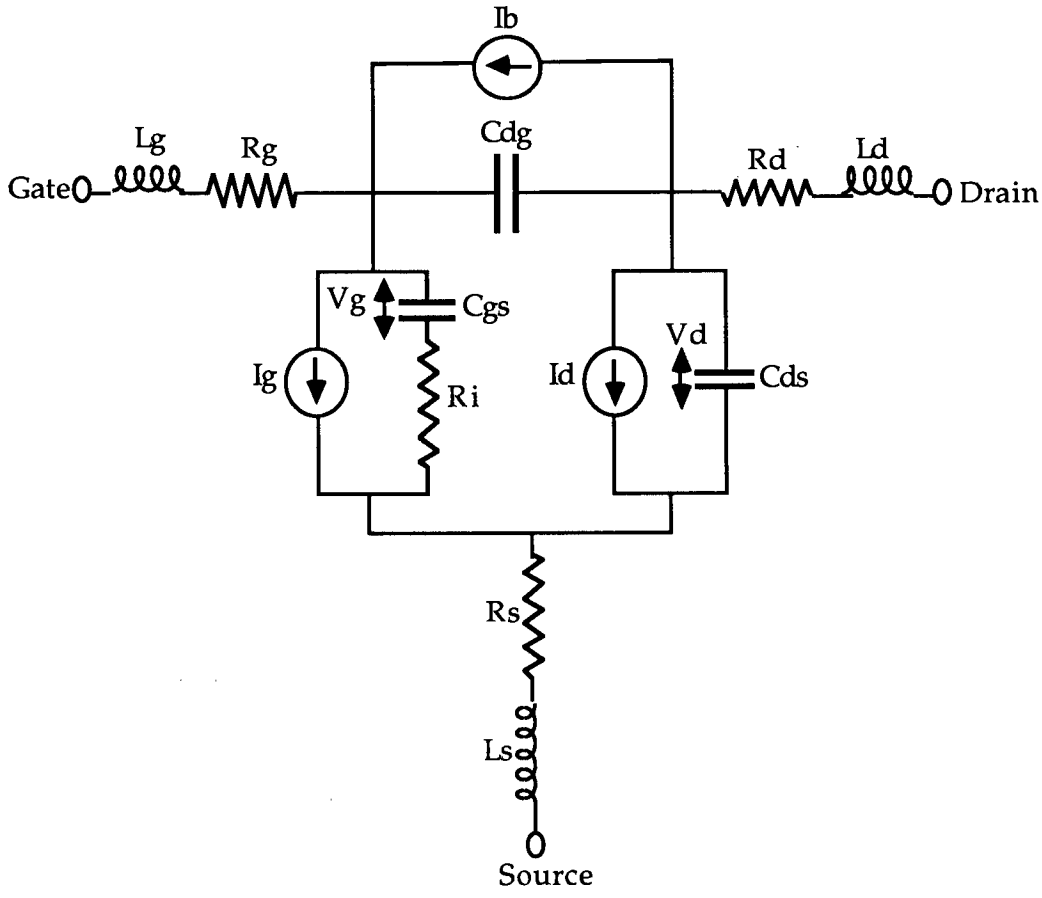


Figure 2.3: The Peterson nonlinear model

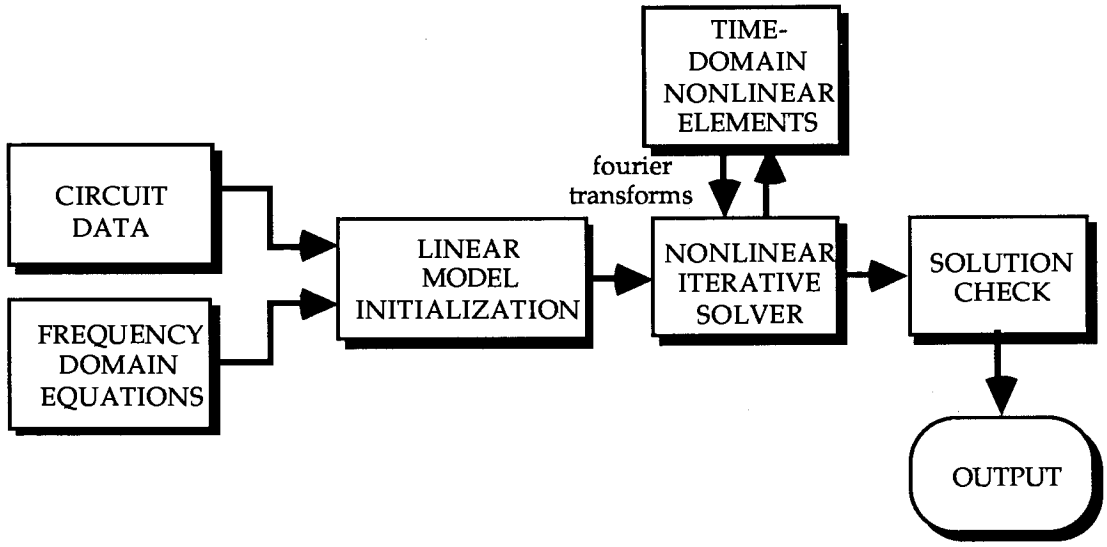


Figure 2.4: Iterative technique used to solve nonlinear model

Maas *et al* [52] described a method for measuring the channel current of the MESFET so that it could be fitted to a polynomial expression and included in a Volterra series analysis. The definition of the equation for I_{ds} was

$$I_{ds} = a_1 v_g + a_2 vg^2 + a_3 vg^3 + \ldots \quad (2.15)$$

The MESFET was supplied with low frequency signals and the current harmonics were observed on a spectrum analyser. The coefficient a_1 was calculated from DC measurements and the remaining coefficients were derived from expressions for the power in each of the harmonics.

Some empirical models [53, 54] have been developed, where the elements of the equivalent circuit were optimized so that the simulated output harmonics fitted measured high frequency power measurements. This technique greatly reduced the amount of data needed to produce a large-signal model. The principal problem of this approach is that the limited amount of data used to characterize the device would not necessary achieve an adequate physical representation of its nonlinear behaviour. Whilst the model may be accurate at bias points and power levels similar to the initial measurements, it may vary considerably at different biases and power levels.

Various approaches have been used to characterize the nonlinearity of MESFETs using large-signal S-parameters. None of these approaches are entirely accurate since the measured S-parameters depend not only on signal drive levels but on port terminations as well. The parameters are similar to the linear small-signal counterparts, except that the power of the applied test signals is large enough to measure the device under nonlinear conditions. One of the first large-signal S-parameter measurement techniques [55, 56] demonstrated the effects of drive levels on nonlinear behaviour in power transistors at given frequencies and operating points.

Difficulties were reported in measuring devices under certain bias conditions and an improved technique was proposed by Mazumder *et al* [57] where S-parameters were measured at ports one and two simultaneously.

Another technique was proposed [58] whereby large signal S-parameters could be made in place of load-pull measurements, to establish the optimum load for amplifier circuits. Load-pull measurements require time consuming variations to be made in the input and output loads at a single frequency. S-parameters are more convenient as they can be made with fixed 50Ω terminations over a swept frequency range. An expression was proposed whereby the optimum load was derived from large-signal measurements for S_{22} and the forward gain nonlinearity could be determined from large-signal measurements for S_{21}.

Umeda and Nakajima [59] also presented a method where the nonlinear output impedance of a device could be derived from large-signal S-parameter methods. Gain compression characteristics were also derived from the S-parameters and a good agreement with experimental data was observed.

The empirical models offer good potential for deriving an accurate nonlinear model from characterizing measurements. Some of the methods which are used to derive the nonlinear channel current are rather convoluted [46,47], whereas others rely on insufficient measurements [53,54] or are best suited to weak nonlinearities [52]. An empirical approach must be chosen to model devices for which no process information is available.

2.4.3 The Semi-empirical Model

Semi-empirical models result from a compromise between the

empirical and analytical approaches. These models are very popular with engineers because of their simplicity and computer efficiency. Most of the published semi-empirical models are based on fitting the DC I-V characteristics of the MESFET to equations which have been derived from analytical expressions. The equations may include process controlled parameters, such as the pinchoff voltage and the built-in voltage, but all of the equations contain arbitrary parameters (α, β, γ etc.) which are used to fit the equation to DC measurements.

The most important nonlinear element in the large-signal model is the current equation and many semi-empirical expressions have been proposed for it. The general shapes of these equations are similar, including a linear region rising to a "knee" point and a saturation region. The following section reviews the semi-empirical models which have been proposed for the other nonlinear elements in the large-signal model.

2.4.3.1 Models for the Drain Current I_{ds}

The Curtice quadratic model [49], illustrated in Figure 2.5, is one of the most widely used and referenced nonlinear models. The definition of the nonlinear current is simple and can provide a good fit to measured DC curves. The equation was derived from an analytical expression derived by Sze [60] for the saturation current in a symmetrical JFET and was defined as

$$I_{ds} = \beta (V_{gs} + V_T)^2 \qquad (2.16)$$

where $\beta = I_P/V_P^2$, I_P is the saturation current, V_P is the pinchoff voltage, V_T is the threshold voltage ($V_T=V_P + V_{BI}$) and V_{BI} is the built-in voltage. A hyperbolic tangent was added to the equation to improve its response at drain voltages below saturation and the full equation became

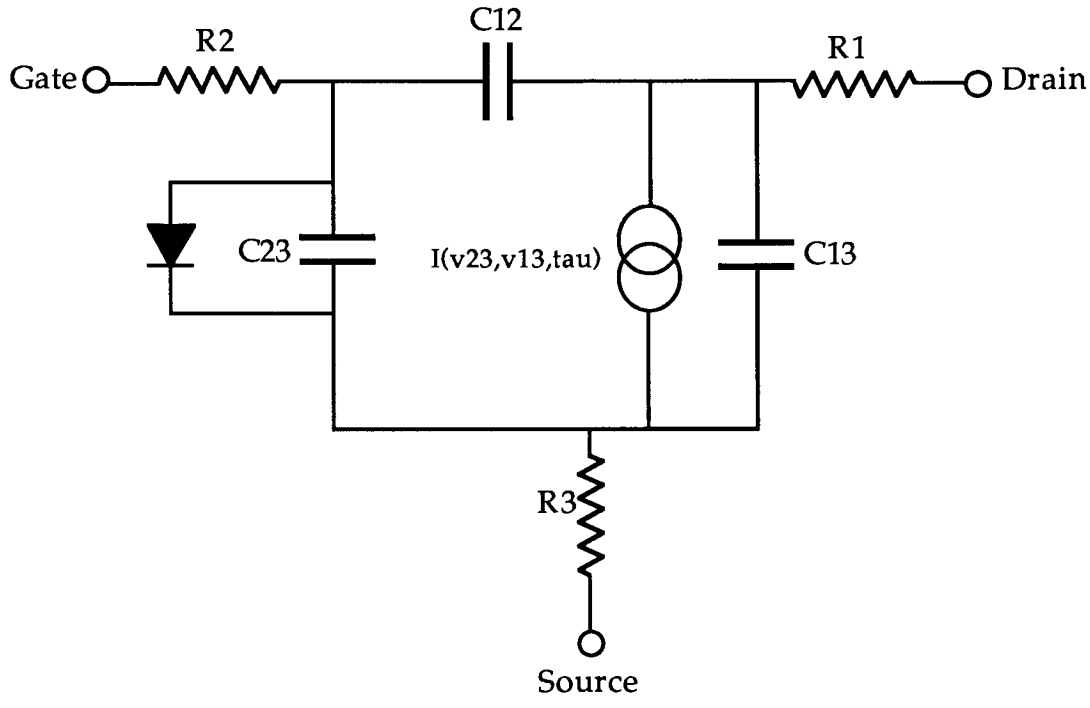


Figure 2.5: Curtice quadratic model

$$I_{ds} = \beta (V_{gs} + V_T)^2 (1 + \lambda V_{ds}) \tanh (\alpha V_{ds}) \qquad (2.17)$$

where α, β and λ are constants and are found by fitting the above equation to MESFET DC characteristics.

In later publications [51, 61], Curtice proposed a nonlinear cubic current equation. The cubic approximation was found to produce a better fit to the DC characteristics of the MESFET and was defined as

$$I_{ds} = (A_0 + A_1 V_{gs} + A_2 V_{gs}^2 + A_3 V_{gs}^3) \cdot \tanh(\alpha V_{ds}) \qquad (2.18)$$

where A_i were evaluated from DC channel current data in the saturation region. In simulation, the cubic model produced smaller errors than the quadratic expression, except at low drain-source voltages, where non-physical effects associated with calculation of V_p with respect to V_{ds} interfered with the optimization of the model [61].

The Curtice quadratic model was used to replace the JFET model of SPICE 2 in a number of applications and Sussman-Fort *et al* [62] published details of how this new expression could be implemented into the source code of the simulator.

Statz *et al* [63] proposed a modification of the Curtice quadratic model. They found that the current equation was poorly represented as a function of V_{gs} and suggested that, except for gate voltages near the pinchoff voltage, the current was proportional to the height of the undepleted channel. The saturated current was represented by the analytical expression

$$I_{ds} = Z\upsilon_{sat} \sqrt{(2\varepsilon q N_d)} ((\sqrt{(-V_T + V_{BI})} - \sqrt{(-V_{gs} + V_{BI})}) \qquad (2.19)$$

where Z is the channel width, υ_{sat} is the saturated electron velocity, ε is the dielectric constant, q is the electron charge and N_d is the donor density. For $|V_{gs} - V_T| \leq 0.3$, equation (2.19) was not valid since the approximation of constant channel height could not be made and equation (2.17) was used instead. An empirical expression was used to connect (2.17) and (2.19) over the whole range of gate voltages and this was

$$I_{ds} = \beta(V_{gs} - V_T)^2/(1 + b(V_{gs} - V_T) \qquad (2.20)$$

The tanh function in (2.18) was found to consume too much computer time and was replaced by a polynomial P, where

$$P = 1 - (1 - \alpha V_{ds}/n)^n \quad \text{for } n=2 \text{ or } 3 \qquad (2.21)$$

and the complete model was

$$I_{ds} = \beta(V_{gs} - V_T)^2/(1 + b(V_{gs} - V_T) \{1 - (1 - \alpha V_{ds}/n)^n \} (1 + \lambda V_{ds}) \qquad (2.22)$$

The current equation was implemented into SPICE and has also been used with success elsewhere [64, 65]. The Statz model [66] was found to give a poor fit for the current at values of V_{gs} close to pinchoff and the

output conductance was also poorly characterized. The poor fit for the current near pinchoff was improved by making V_T a function of the drain voltage, where

$$V_T = V_{T0} - \gamma V_{ds} \tag{2.23}$$

The fit of the output conductance was improved by modifying the Statz model so that

$$I_{ds} = I_{ds0}/(1 + \delta V_{ds} I_{ds0}) \tag{2.24}$$

and

$$I_{ds0} = \beta(V_{gs} - V_T)^Q \{1 - (1 - \alpha V_{ds}/n)^n\} \tag{2.25}$$

This resembles the original Statz equation with $b=\lambda=0$ and three new parameters δ, γ and Q.

Tajima [48] proposed a nonlinear model with a similar topology to the Curtice model. The transconductance and drain conductance were found to be nonlinear and so were R_i, C_{gs} and G_{gf} (the gate forward conductance, connected in parallel with C_{gs}). An expression for the nonlinear channel current I_{ds} was based purely on empirical measurements, describing the DC characteristics of the MESFET. The transconductance and output conductance were found by differentiating the current with respect to V_{gs} and V_{ds} respectively. The current I_{ds} was defined as

$$I_{ds}(V_{ds}, V_{gs}) = I_{d1} \times I_{d2} \tag{2.26}$$

where

$$I_{d1} = 1/k \left[1 + V_{gs'}/V_p - 1/m + (1/m) \times \exp\{-m(1 + V_{gs'}/V_p)\} \right]$$

$$I_{d2} = I_{dsp} \left[1 - \exp\{-V_{ds}/V_{dss} - a(V_{ds}/V_{dss})^2 - b(V_{ds}/V_{dss})^3\} \right]$$

$$k = 1 - 1/m\{1 - \exp(-m)\}$$

$$V_p = V_{p0} + pV_{ds} + V_{BI}$$

$$V_{gs'} = V_{gs} - V_{BI}$$

where V_{po} is the pinchoff voltage at V_{ds}=0V, V_{dss} is the drain current saturation voltage, I_{dsp} is the drain current for V_{gs}=V_{BI} and a,b,m, and p are constants, found by fitting the equation to the DC characteristics of the MESFET (similar to the Curtice α,β and λ terms). The model was later modified [48] to include the effects of gate-drain breakdown by adding a nonlinear resistance in parallel with the gate-drain capacitance C_{dg}. The current through the resistor was zero for V_{dg}<V_b and equalled $(1/R_b)$. $(V_{dg}-V_b)$ for $V_{dg} \geq V_b$, where

$$V_b = V_{b0} + R_1 I_{ds} \tag{2.27}$$

$$R_b = R_{b0} + R_2 \cdot (I_d/I_{dss}) \tag{2.28}$$

Large-signal models were simulated [67, 68], including nonlinear sources characterized by the Tajima equation. One of the models [67] was used to simulate power spectral characteristics and was compared to measurements made on commercial packaged transistors and the other was successfully used to design a power FET multiplier [68].

A nonlinear current equation was proposed by Taki [69] to model the JFET. An analytical derivation of the JFET current equation was considered, although this was abandoned in place of a simpler empirical equation. The current I_{ds} was defined as

$$I_{ds} = I_{dss} (1 - V_{gs}/V_p)^2 \cdot \tanh \alpha \ | V_{ds}/V_p - V_{gs} | \tag{2.29}$$

Comparisons were made [70] between the Taki and Tajima current equations and it was found that, although more complicated, the Tajima equation could be fitted to MESFET DC characteristics with greater accuracy.

Materka and Kacprzak [71] proposed a model, illustrated in Figure 2.6, which includes a current source $I_{ds}(V_{gs},V_{ds})$, a nonlinear capacitance

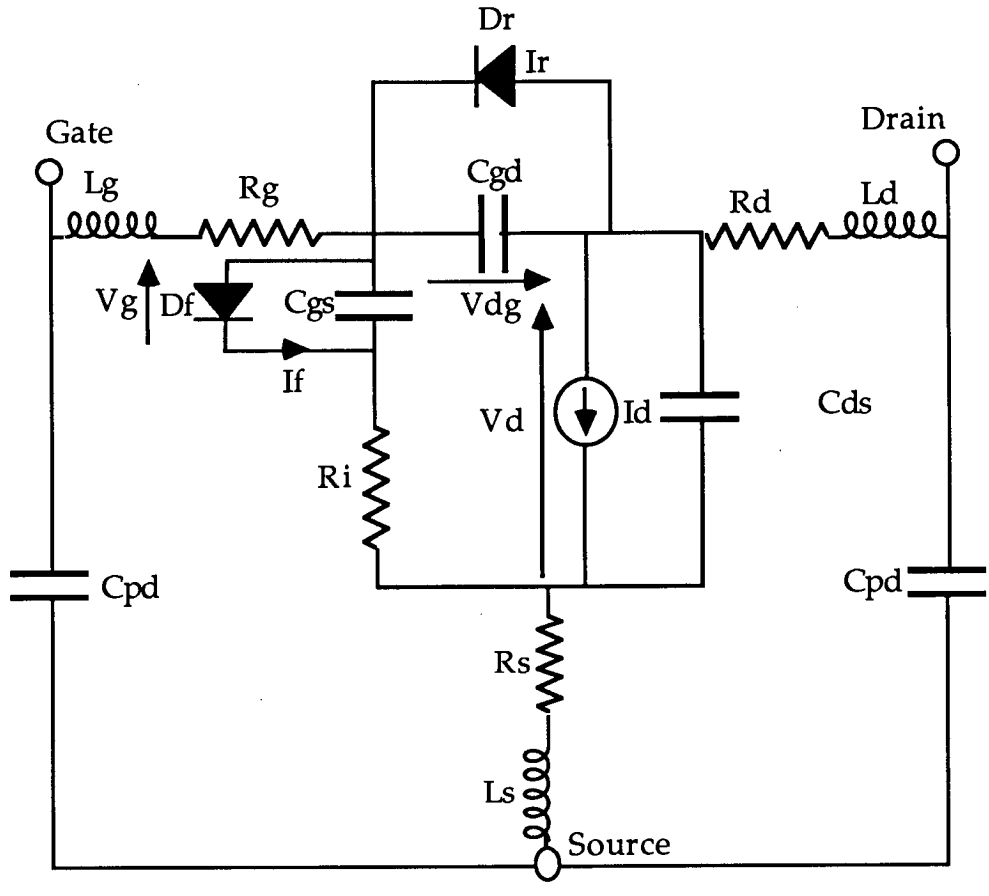


Figure 2.6: The Materka and Kacprzak nonlinear model

Cgs, a diode representing the gate channel current and another diode to represent gate-drain breakdown. The current equation was the same as the expression proposed by Taki [69]. The model was evaluated using the harmonic balance technique; power saturation results for an amplifier containing the model were simulated and found to compare well with experimental measurements.

The Materka current equation was modified by Hwang [72] in order to model the DC characteristics of a Hughes MESFET which exhibited a negative output conductance in the saturation region. The new equation became

$$I_{ds} = I_{dss}\,(1 - V_{gs}/V_p)^2 \,.\, \tanh\,[\, c\, V_{ds}/V_{gs} - V_p]$$

for $V_{ds} < V_{sat}$, and

$$I_{ds} = I_{dss}\,(1 - V_{gs}/V_p)^2 \,.\, \tanh\,[\, c\, V_{ds}/V_{gs} - V_p] - V_{ds}.g_0 / [V_s - V_{gs}]^q$$

for $V_{ds} \geq V_{sat}$ (2.30)

where $V_p = V_{p0} + r.V_{ds}$ and I_{dss}, c, g_0, V_{p0}, r, V_s and V_{sat} are optimized to fit the measured I-V curves.

Larson [73] examined the nonlinear current equation by Schichmann-Hodges for the JFET which is implemented in most SPICE simulators. The drawback of the latter expression is the assumed square-law relationship between V_{gs} and I_{ds} which is not always found to be the case for MESFETs. Also, because MESFETs possess a large negative threshold voltage, current saturation occurs at lower values of V_{ds} than can usually be predicted using the SPICE model and these observations were reported elsewhere [74]. Whilst the Curtice equation and others using the tanh function were found to provide a good fit to DC characteristics for devices with large negative threshold voltages, they were less suitable for devices with smaller thresholds.

Consequently, a new current equation was proposed, where

$$I_{ds} = \beta(1 + \lambda k V_{ds})kV_{ds}(1/q)^q\,[(1 + q)(V_{gs} - V_T) - kV_{ds}]^q$$

for $V_{gs} - V_T \geq kV_{ds}$

$$I_{ds} = \beta(1 + \lambda k V_{ds})(V_{gs} - V_T)^{1+q}$$

for $V_{gs} - V_T < kV_{ds}$ (2.31)

where the two new terms q and k were included to improve the modelling of I_{ds} with respect to V_{gs} and the onset of drain current saturation respectively.

A nonlinear current equation was also proposed by Jastrzebski [75]

and featured all of the important characteristics of the following models: Curtice, Tajima, Materka, Statz and Larson. It allowed for relationships between current and gate voltage other than square-law and for decreasing output conductance with increasing V_{gs}. The pinchoff voltage was defined as being dependent on V_{ds} and a negative slope for I_{ds} with respect to V_{ds} in the saturation region could be fitted. Also, the saturation voltage was defined as a function of V_{gs}. The models were compared with each other and with the new model and were all found to be deficient in at least one respect.

A series of comparisons were made [76] between the current models of Taki, Curtice, Materka, Statz and Tajima and a new model by Brazil. A DC curve fitting package called INTERSECT was used to fit the DC characteristics of an NE71000 chip device and a Plessey monolithic device to each of the equations and the results [76] are given below.

Model Name	No. Parameters	RMS Error	
		NE71000	Plessey
Taki	3	3.66	4.95
Curtice.Q	4	3.36	4.09
Materka	4	2.67	1.48
Statz	5	2.15	4.06
Brazil	6	1.51	1.13
Curtice.C	7	0.85	0.65
Tajima	9	1.03	0.84

Results of the work concluded that the Curtice cubic model was best equipped to model the DC current characteristics, whilst Materka's expression was simpler and still produced acceptable results. Another set of comparisons was made [65] between the Materka, Statz and cubic Curtice models and the results showed that the best fit was obtained from Materka's expression.

Other semi-empirical models for the MESFET exist. Some of them

have been developed for use in digital applications and have been implemented on SPICE, like the large-signal models proposed by Golio *et al* [77] and Goyal [78]. Whilst adequate for digital simulation, the current equation was often found lacking with respect to modelling the output conductance which made it unsuitable for analogue circuits.

All of the semi-empirical equations for the current are implemented in the nonlinear model by fitting the equation to characterizing measurements for the DC current of the MESFET. Therefore, a critical assumption is made, that the characteristics of the MESFET are the same at high frequencies, as they are at DC, unless the DC characterization has been made using pulsed I/V measurements (see Chapter Four). This assumption will be examined in greater detail in Section 2.5.

The semi-empirical models are also susceptible to errors arising from heating effects. The channel of the MESFET heats up the longer it is held at a particular bias setting, especially for high channel currents. The temperature change will affect the characteristics of the MESFET which will in turn affect the characterizing measurements at that bias point. If the bias setting has resulted from RF excitation, the temperature of the MESFET will be less than for the DC case.

2.4.3.2 Models for C_{gs}, C_{dg}, R_i and τ

The channel current is the most important nonlinearity in the MESFET model and this is confirmed by the MESFET model sensitivity analysis given in Chapter Four. The overall accuracy of the large-signal model depends on the other nonlinear elements which, listed in descending order of sensitivity, are: C_{gs}, C_{dg}, τ, and R_i (see Figure 2.3). Gate-drain breakdown and forward gate current effects should also be included

into the large-signal model by adding parallel, ideal, diode elements D_{dg} and D_{gs} to the existing elements C_{dg} and C_{gs} respectively, modelled on DC measurements

All of the published semi-empirical models include the non-linear element C_{gs}. Some of the models also include C_{dg} and/or D_{dg} and D_{gs}. Only a few of the models include nonlinear elements for R_i and τ. A summary of these nonlinear elements is given below.

In many of the large-signal models [35, 49, 79] and in commercial simulators such as SPICE and LIBRA, the gate-source capacitance is represented by an analytical expression for a reverse biased Schottky barrier capacitance. The equation is defined as

$$C_{gs} = C_{gs0}/(1 - V_{gs}/V_{BI})^{1/2} \tag{2.32}$$

where V_{BI} is the built-in voltage ($\approx$0.8V) and C_{gs0} is the zero bias gate capacitance. A similar equation is often used to model the gate-drain capacitance C_{dg}, where

$$C_{dg} = C_{dg0}/(1 - V_{dg}/V_{BI})^{1/2} \tag{2.33}$$

However, these expressions have a number of deficiencies. Firstly, when the source-drain voltage is zero and for a physically symmetrical MESFET, the values of C_{gs} and C_{dg} should be equal but the above equations may produce different values for both capacitances. The capacitive model also breaks down when the transistor is reverse biased and C_{gs} becomes C_{dg} and vice versa. The above equations also limit C_{gs} as varying with V_{gs} only and C_{dg} with V_{dg} only. In fact, the capacitances are functions of both voltages and this was recognised by Goyal [78] who modified (2.32) to

$$C_{gs} = C_{gs0}/(1 - V_{gs}/V_{BI})^{1/2} + C_0 V_{ds} \tag{2.34}$$

where the coefficient C_0 was added to account for the effect of V_{ds} on the gate capacitance. Statz [63] improved the equations for the gate-source and gate-drain capacitances by modelling the capacitances as derivatives of the

gate charge Q_g and not as unconnected elements. This removed many of the problems mentioned above and allowed the MESFET to be considered as a symmetrical device.

Larson [73] suggested that the capacitance in the channel could be divided into three regions: the source end of the depletion region, the drain end of the depletion region and the central region. The charge in the central region was derived from an analytical equation [80]. C_{gs} was defined as the derivative of the charge with respect to V_{gs} plus the capacitances of the two end regions. Similarly, C_{dg} was the derivative of the charge with respect to V_{dg} plus the end capacitances.

Jastrzebski [75] proposed a semi-empirical model for both capacitances, where

$$\begin{aligned} C(V) &= 0.5\, C_0/\sqrt{d}(3 - h/d) + C_{gf} && \text{for } V > V_{BI} - dV_{BI} \\ &= C_0/\sqrt{h} + C_{gf} && \text{for } V_{BI} - dV_{BI} > V > -V_{to} \\ &= C_0/(\sqrt{(1 + V_{t0}/V_{BI})}.(V + V_{to} + dV_{to})/dV_{to} + C_{gf} \\ & && \text{for } 0 > V + V_{to} > -dV_{to} \\ &= C_{gf} = \text{const} && \text{for } V < -V_{to} - dV_{to} \end{aligned} \tag{2.35}$$

where C_0 is the depletion capacitance at zero bias, C_{gf} is the gate fringing capacitance, h=1-V/VBI, V_{to} is the threshold voltage and d is a constant. V is either V_{gs} or V_{dg} depending on whether C_{gs} or C_{dg} is being specified.

The gate-drain capacitance has also been modelled by Hwang *et al* [72] with the equation

$$C_{dg} = C_{g0}/(1 - V_{gs}/V_{BI})^{1/2}.\,(1 - V_{ds}/V_{sat}) + C_{dp} \tag{2.36}$$

in recognition of the dependence of C_{dg} on both bias voltages.

Semi-empirical equations for the intrinsic resistance R_i and the time delay under the gate τ are quite scarce. In some models [79, 81] the intrinsic resistance was assumed to vary in such a way that the charging time constant did not change. Curtice [61], on the other hand, defined the

time delay as a linear function of only the drain voltage. Jastrzebski [75] proposed a nonlinear intrinsic resistance of the form

$$R_i(V_{gs}) = R_{i0} \times (1 - V_{gs}/V_r)^{\sigma} \qquad (2.37)$$

where R_{io} is the value of resistance at $V_{gs}=0$, V_r is the voltage at which R_i becomes zero and σ equals 1 or 2.

Less semi-empirical equations exist for the nonlinear elements C_{gs}, C_{dg}, R_i and τ than for the nonlinear current. It has been shown [78] that, for the gate-source capacitance C_{gs}, the existing equations, including the equation used in SPICE, are rather limited and can decrease the accuracy of the nonlinear model. Nonlinear expressions for the gate-drain capacitance are even less common and the intrinsic resistance R_i is most often represented as a linear resistor.

2.4.4 The Analytical Model

The analytical models result from the solution of the device equations (given below) with some simplifying assumptions. Therefore, the device can be investigated to some extent before it has been fabricated. The disadvantages of this approach are that analytical models are not usually as accurate as empirical and semi-empirical models and demand more computer power. Analysis of the MESFET channel can be either one-dimensional or two-dimensional. The one-dimensional approximation considers only a cross-section through the channel whereas the two-dimensional analysis involves solutions for the transport equations over a wider area. The four basic device equations [81], including Poisson's equation (2.38) and the current continuity equation (2.39) are

$$\nabla^2\psi = -q/\mathcal{E}\ (N_d - n) \qquad (2.38)$$

$$q\,\partial n/\partial t = \nabla . J \qquad (2.39)$$

$$J = -qn\upsilon + qD\nabla n \tag{2.40}$$

$$J_T = J + \partial E/\partial t \tag{2.41}$$

where $E = -\nabla\psi$

and N_d is the donor concentration, q is the electronic charge, ε is the dielectric permittivity, J is the conduction current density, E is the electric field, D is the diffusion coefficient and υ is the average carrier velocity. The unknown quantities are n (carrier distribution), ψ (electric potential) and J_T (the total current density).

A large number of analytical descriptions of the MESFET are to be found in a book by P. H. Ladbrooke [82]. The basic FET principles are described and many equations are derived for the nonlinear elements in the large-signal model. These are based on process parameters such as the doping density and thickness of the N-channel layer, the FET dimensions, the built-in potential, the density of traps, the ohmic resistance and the depletion region dimensions. Some aspects of this work are discussed in Chapter Four.

A model was proposed by Shur [83], where the current, current delay, gate-source capacitance and gate-drain capacitance were derived from a fundamental equation for field-effect transistors [84]. The assumptions made in this model were that there was a sharp boundary between the depletion region and the neutral channel, the electrical field distribution under the gate was one-dimensional and there was no diffusion under the gate. The capacitors were derived from an expression for the accumulated charge under the gate, where C_{gs} and C_{dg} were the partial derivatives of Q with respect to V_{gs} and V_{dg}.

Madjar [85, 86] proposed a nonlinear model based on analytical calculations for the channel current. The large-signal MESFET model is

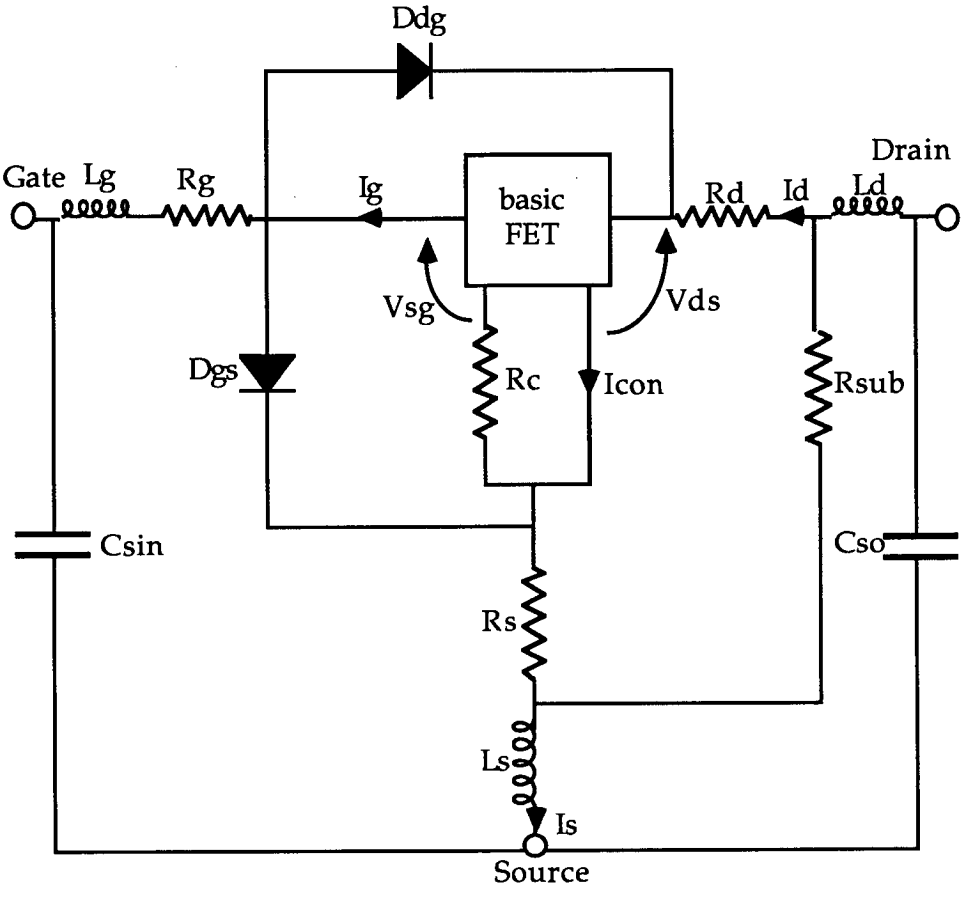


Figure 2.7: Madjar's nonlinear model

shown in Figure 2.7 where the passive components are derived either from device geometry by field models or by S-parameter characterization [61]. The active nonlinear part of the model is contained in the box labelled "basic FET". Here I_g and I_d are defined as

$$I_g = GVSG\ \partial V_{sg}/\partial t + GVDS\ \partial V_{ds}/\partial t \tag{2.42}$$

$$I_D = I_{CON} + DVSG\ \partial V_{sg}/\partial t + DVDS\ \partial V_{ds}/\partial t \tag{2.43}$$

$$I_S = I_{CON} + SVSG\ \partial V_{sg}/\partial t + SVDS\ \partial V_{ds}/\partial t \tag{2.44}$$

I_{CON} is the drain-source conduction current, V_{ds} and V_{sg} are the bias voltages and GVDG, GVDS, DVSG, etc. are capacitative coefficients representing the displacement current. I_{CON} is defined as

$$I_{CON} = I_S(1 + mV_{ds}) \tanh (V_{ds}/V_S) \tag{2.45}$$

where Is, m and Vs are all complex functions of V_{sg}. This equation resulted from an analytical derivation of the current in the MESFET channel. The MESFET consisted of an N-type layer on a semi-insulating substrate, where charge transport is governed by the well-known semiconductor equations for N-type JFETs (2.38-2.41). The analysis of this model includes an extension of the approach by Yamaguchi and Kodera [52] for deriving the drain conductance of a JFET in the hot electron range. In this analysis, the value of n is derived analytically, so that the electric field and the current density can also be obtained analytically.

Madjar's model was implemented on a two-dimensional simulator called BETTSI [87]. The model was compared with a set of experimental measurements [45] and a number of improvements to the model were suggested. The software was written to improve the link between physically based transistor simulation and circuit simulation packages.

Johnson and Johnson [88] proposed a combined DC and AC model, taking into account velocity saturation and the impurity profile. The physical derivation of the model assumed a gradual channel approximation, a standard function for the areal carrier concentration and allowed for greater flexibility in the relationship between V_{gs} and I_{ds} than the standard square law. It also assumed that the electron velocity saturated at the peak velocity under the drain edge of the gate.

An expression for the DC current was derived. An AC model was also derived, based on the same assumptions used for the DC equation. The charge in the depletion region was calculated analytically and the gate capacitance C_g was defined as the differential of that charge. C_g represented the combined capacitances of C_{gs} and C_{dg} or put another way, the total capacitance in the model with source and drain tied together. It was not possible to derive either C_{gs} or C_{dg} separately. The model was

implemented in SPICE and used to design a series of digital inverters.

Another analytical model by Khatibzadeh and Trew [89] has been derived from the device equations. The model takes into account the effects of arbitrary doping profiles and accumulation of charge in the channel. It is defined in terms of device geometry, material parameters, bias and RF operation conditions. Comparisons were made between the model and small and large-signal measurements of a Raytheon power FET and a good agreement between model and measurements was reported. The model was also used to study the effects of different MESFET doping profiles on RF performance [90].

Pantoja *et al* [91] proposed an analytical quasi-static model based on a one-dimensional analysis of the channel. Certain assumptions were made which considerably reduced the computing time during simulation. The current density was approximated as being one-dimensional and no current was assumed to flow through the depleted region. The model was compared with experimental measurements and good agreement was reported.

An analytical expression for the gate-source capacitance was implemented in SPICE [77] which was based on calculations by Ino *et al* [92]. The analytical expression includes five empirical terms which are used to fit the equation to measured data for the capacitance. A similar analytical expression was also proposed for the gate-drain capacitance.

Each of the analytical models have been derived to solve the device equations which govern the properties of charge conduction in the MESFET. Of these, the two-dimensional models are more accurate. The most satisfactory expressions for the depletion regions capacitances (C_{gs} and C_{dg}) have be derived from a consideration of the whole charge stored under the gate region.

2.4.5 The Numerical Model

Numerical models solve the nonlinear, coupled, partial differential equations for the MESFET device using finite-difference or finite-element numerical techniques. The models are useful for observing the physical operation of the MESFET but are computationally too inefficient to be used in applications such as RF simulation. The basic device equations are the same as the equations used for analytical models. Only a few assumptions are made since the objective is to achieve as much simulation accuracy as possible.

There have been a number of publications concerning numerical modelling [93-104] but these will not be discussed in this review, since numerical modelling requires a full knowledge of the physical dimensions and properties of the MESFET. Since this work is specifically concerned with modelling MESFETs on processes from which such information is not released to the designer, the numerical approach cannot be used.

2.5 Frequency Dispersion in the MESFET

Many existing nonlinear models, particularly the semi-empirical models, are based on the assumption that the DC and high frequency characteristics of the MESFET are the same. The result of this is that often, the DC current characteristics are used to describe the changes in the high frequency current with drive level. The output conductance (g_o) in the MESFET is represented in the basic model of Figure 2.8 by the combination of elements $1/(R_d + R_{ds} + R_s)$, where the model is derived from S-parameters at microwave frequencies. The value for the output conductance can also be found at DC from the I-V curves, where G_o is the gradient of the current with respect to the drain voltage. If the model

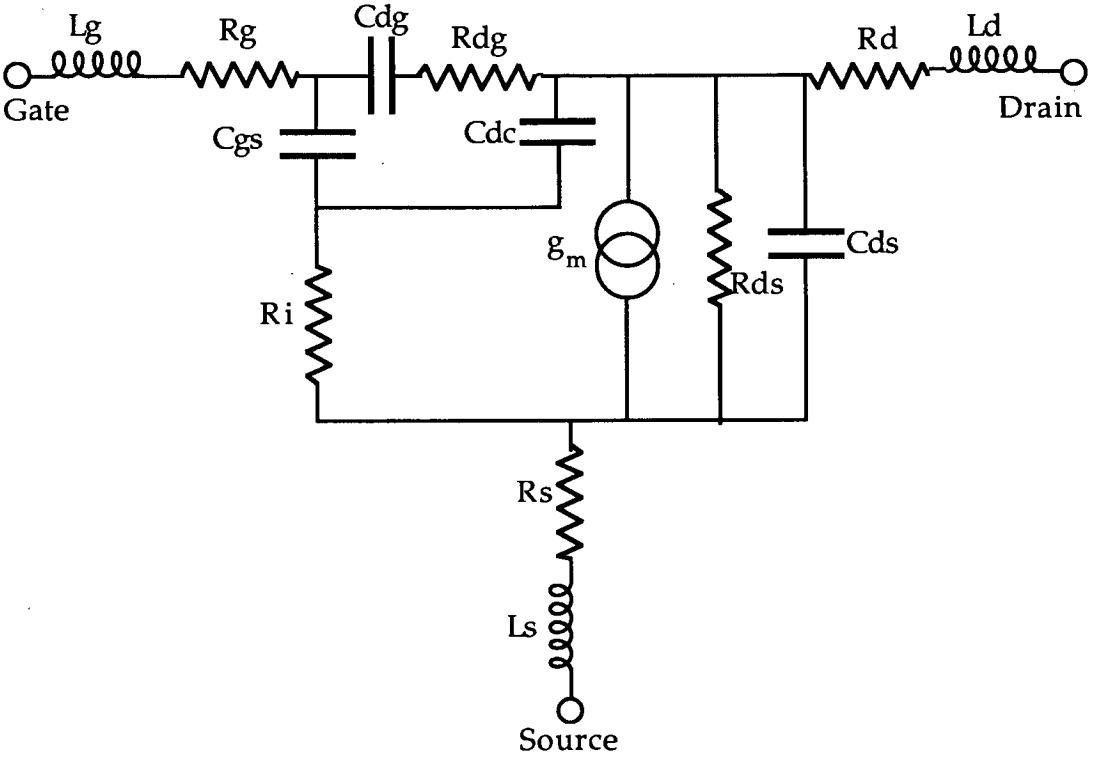


Figure 2.8: Leichti linear model

extracted from S-parameters is valid from high frequencies down to DC, then $g_o = G_o$. If this is not the case, then the model parameters are functions of frequency and dispersion of the output conductance is taking place.

A study was recently made [105] of 13 commercially available MESFETs. Some of the devices exhibited a small but significant dispersion: the rest of the devices exhibited a large amount of dispersion. In some cases, the value of the output resistance at high frequencies was down by a factor of three from that measured at DC. These results were not new, as similar findings had previously been reported [27, 28, 73].

The cause of dispersion in the output conductance is largely due to the change in the substrate current of the FET with frequency. At DC, the

substrate is full of generation-recombination (EL2) centres, otherwise known as traps, absorbing charge which would otherwise flow through the channel. At high frequencies, the effectiveness of the traps decreases and this has the effect of increasing the output conductance. The frequency at which dispersion takes place corresponds with the typical trapping time constant in GaAs structures.

Frequency dispersion is not only limited to the output conductance. It has also been reported in the transconductance and in the gate charge [25, 29], affecting both the gate-source and gate-drain capacitances, especially at low drain bias, where the current approaches pinchoff. In the case of the transconductance, the variation with frequency amounts to only a few percent in most cases.

Dispersion effects cause the high frequency model to be inaccurate at low frequencies - typically dispersion effects occur in the range of 1kHz to 100kHz. More significantly, these effects cast a shadow of doubt on the reliability of high frequency models derived from DC measurements. Whereas simulations of numerical and analytical models may be able to predict dispersion effects, the semi-empirical models rely heavily on characterizing the nonlinear channel current from DC current measurements.

A number of different models have been proposed, designed to include the effects of frequency dispersion in the output conductance. These models are summarized and discussed fully in Chapter Five.

2.6 Proposed Large-signal Model

All of the models described in this chapter fall into one of two categories: models which are based in part or wholly on experimental measurements and models which are derived from equations which

describe device physics. For the purposes of this work, it was decided to concentrate on the former approach. The justification of this is that no knowledge of fabrication procedures and process parameters is needed. Furthermore, such information was not readily available for the proprietary MESFET process on which the practical aspects of this work were based. A further point for consideration is that although making device measurements is time-consuming, a model based on measurements offers the possibility of greater accuracy, since the model can be tailored to the specific test device.

Measurement-based models, described earlier in the chapter, were either empirical or semi-empirical. The semi-empirical models derived in part from attempts to express the high frequency channel current as the same as, or a slightly modified version of, the DC current. However, the observed effects of frequency dispersion (mainly of the output conductance), as discussed in Section 2.5, have cast doubts over the wisdom of such an approach to produce an accurate model. Therefore it was decided to chose a completely empirical approach to non-linear modelling.

The proposed method for obtaining a nonlinear GaAs MESFET model was to make sets of S-parameter measurements at a series of different gate and drain bias points. In this way, the MESFET could be characterized using high frequency measurements and the model would therefore be able to predict the effects of frequency dispersion, which is often not possible in the commercial semi-empirical models. The equivalent circuits were extracted for each set of S-parameters, using a small-signal frequency domain simulator and the elements in the equivalent circuit whose values varied with bias identified the nonlinearity of the device. A nonlinear model was constructed where the

bias dependent elements in the equivalent circuit were defined as functions of the two external bias voltages V_{ds} and V_{gs}. The model was installed on a time-domain simulator to calculate the small and large-signal characteristics of different amplifier circuits, where the large signal characteristics included load-pull and power saturation simulations. To derive the model, the following hardware and software was needed:

- A set of test FETs. S-parameter measurements were made of single FETs different bias points

- An 8510B Network Analyser was used to make the S-parameter measurements. Two different types of calibration were used and these are described in Chapter Three

- MMIC amplifiers were designed and fabricated. They used the same FETs as the nonlinear model

- equipment for making load-pull and power saturation measurements. This included a microwave source, a microwave power meter, bias tees, a two-pole microwave switch, a device test jig and various connectors, attenuators etc.

- Small-signal frequency domain software for parameter extraction. Both SUPERCOMPACT [31] and TOUCHSTONE [32] were available

- Large-signal simulation software. ANAMIC [36] was used in the course of this work.

ANAMIC is a time domain microwave simulation package for nonlinear, active, lumped and distributed circuits. The software accepts many different types of linear and nonlinear elements and additional nonlinear functions can be added in user-defined Fortran libraries. Simulation time for ANAMIC is substantially smaller than for other time domain simulators since it uses state-space analysis. The state-space method ensures that the differential simultaneous expressions, derived from Kirchoff's voltage and current laws and the voltage-current relationship for each device in the model, are kept separate and this makes solutions for nonlinear circuits easier.

ANAMIC offers advantages over SPICE in that it has been written specifically for microwave applications and it is therefore easier to extract microwave parameters (such as S-parameters) during simulation. A particularly important advantage of ANAMIC for this work is that nonlinear elements can be defined by the user as Fortran subroutines. This kind of flexibility is rare on nonlinear simulators like SPICE where the source code would require to be extensively modified. The only alternative would be to limit the expression of nonlinearity as combinations of nonlinear current and voltage sources.

2.7 The MESFET Model Topology

During the discussion of large-signal modelling techniques, many different equivalent circuits were illustrated to describe the electrical properties of the GaAs MESFET. Most of the models are variations on a theme, where researchers have added or removed some of the elements to improve the simulation of particular characteristics. Sometimes the topology has been chosen simply to improve the overall fit with measured

data and this depends on the process on which the test device was fabricated. Topology selection depends on the required accuracy between the characterizing measurements and the model. Where large-signal models are made from extensions of linear models, the latter must consist of elements which represent the physical nature of the device. As measurements of the MESFET are taken at different bias points, the values of model elements can be seen to change in a predictable way which can be explained in terms of device physics.

A model, consisting of the minimum number of elements to describe the characteristics of the MESFET, is called "the minimal circuit" [106]. As the model is fitted to measured results, a perfect fit is impossible because of the inclusion of experimental errors. Where there are too many elements in the model, the number of possible model solutions is very large and the uncertainty associated with an individual element is very large. If there are too few elements in the model, then a satisfactory fit can never be reached and the elements begin to loose their physical significance. The best equivalent circuit contains enough elements to achieve a good match with the measurements and for which there are only a few solutions.

Some approaches determine the topology of the model while the equivalent circuit is fitted to measurements [107, 108]. The topology is chosen by trial and error and it quite often has no physical justification in which case it is unsuitable for this particular application. Distributed, rather than lumped, elements could be used in the MESFET model [109, 110] but this would greatly increase the complexity of nonlinear simulation and would only yield an increase in the accuracy at very high frequencies.

The small-signal model chosen for this work [111] is shown in

Figure 2.8. It is based on a compromise between the number of elements, problems with parameter extraction, physical reality and agreement with experimental data. This model is known as the Liechti equivalent circuit [2] and has the additional advantage of being widely used in the literature and by Plessey Research (Caswell) Ltd., who fabricated all of the test FETs used for this work on their commercial F20 GaAs MMIC process. The model is similar to the basic FET model given in Chapter One with the inclusion of gate, drain and source inductance and also a capacitance C_{dc}. At the centre of the model lies the voltage controlled current source (represented by g_m and R_{ds}) where the drain current is controlled by the voltage across the capacitor C_{gs}. The capacitances $C_{gs}+C_{dg}$ represent the total gate-to-channel capacitance and R_i is the intrinsic resistance of the channel. These five components are known as the intrinsic elements and vary with the DC bias while the remaining nine elements can be approximated as linear elements. A complete description of the elements and their physical function is given in Chapter Four.

CHAPTER THREE - Measurement Calibration

3.1 Introduction

In the previous chapter, an empirical nonlinear model was proposed, which derives from sets of S-parameters at different bias points. With this method, the model is only as accurate as the measured data and hence can be improved by reducing the experimental errors in the S-parameter measurements as much as possible. This chapter explores ways in which accurate S-parameters can be made and experimental errors reduced.

S-parameters are measured on a vector network analyser (in this project the Hewlett Packard 8510 vector network analyser (8510 VNA) was used), and their accuracy is largely determined by the quality of the network analyser calibration. This removes unwanted and repeatable information, such as the effects of non-ideal transmission lines, connectors and circuit parasitics. If all unwanted information has been removed, then the measurements represent the test device perfectly, but in practice this is not totally possible, and some small experimental errors will still remain.

For this work, measurements of test FETs and fabricated MMIC circuits were made, both to determine *and* to evaluate the accuracy of the nonlinear model. The model was determined from S-parameter measurements using the techniques described in Chapters Four and Five. The nonlinear model was used to simulate power measurements and these results are presented in Chapter Six. Since the experimental S-parameter measurements are an integral part in the development and testing of the nonlinear model, calibration techniques are vitally important and are discussed fully, including detailed descriptions of the

two calibration methods used for this work. Off-chip thru-reflect-line (TRL) calibration was used at Thorn-EMI for characterizing test transistors and on-chip short-open-line-thru (SOLT) calibration was used at Edinburgh University for load-pull and amplifier measurements. Some wafer-probed test FET S-parameter measurements were also made available by GEC Plessey Research (Caswell) Ltd. and these were also used in the development of the nonlinear model.

For the on-chip SOLT calibration, it was necessary to design and fabricate on-wafer calibration standards. This chapter includes details of how these standards were characterized to determine their actual physical structure and characteristics. A description is given of how the standards were used to perform two-port calibration and tested to verify their accuracy.

3.2 Calibration Techniques

Accurate device measurements are made when the effects of the device's environment are not included in the resultant S-parameters. This is done by calibrating the network analyser and device fixture and a number of methods, discussed below, can be used. The choice of calibration depends on the type of device fixture, the availability of accurate calibration standards and the degree of accuracy which is needed in the result.

The simplest way of calibrating a network analyser is to perform a standard two-port calibration, up to two known reference planes on the analyser, using accurate calibration standards. These standards can be a combination of short circuit, open circuit, ohmic and transmission line standards and are often provided commercially by network analyser vendors or test fixture manufacturers. The fixture containing the device

under test is inserted between the reference planes and the two-port measurements are made. The limitation of this procedure is that the physical characteristics of the fixture are included in the results and therefore true two-port measurements of the device are not readily available.

An improvement of this calibration is to extend the reference planes as near to the device under test as possible and remove the physical characteristics of the fixture. However, this presents some difficulties as devices are often mounted on microstrip for which no accurate calibration standards are available. Subsequently, it is usually necessary to fabricate and characterize custom calibration standards and, since MMICs are being tested, the standards should be realised on-chip. A method similar to the standard coaxial two-port calibration technique can be used, which requires short, open, load and through (SOLT) on-chip calibration standards.

In noncoaxial transmission media it may be difficult to realise three distinct impedance standards and an alternative approach to SOLT calibration can be used, which requires the use of through, reflect and line (TRL) on-chip standards. S-parameter measurements can also be made directly on semiconductor wafers, using an on-wafer measurement station (or wafer-probe).

The following subsections summarize the methods of standard coaxial, on-chip SOLT, on-chip TRL and wafer-probe calibration.

3.2.1 Standard Two-port SOLT Calibration

Standard two-port calibration for the 8510NA removes linear and repeatable errors, by combining two-port measurements with an imaginary two-port error adapter. In the resulting measurements, reflectometers and transmission lines up to the reference planes appear to

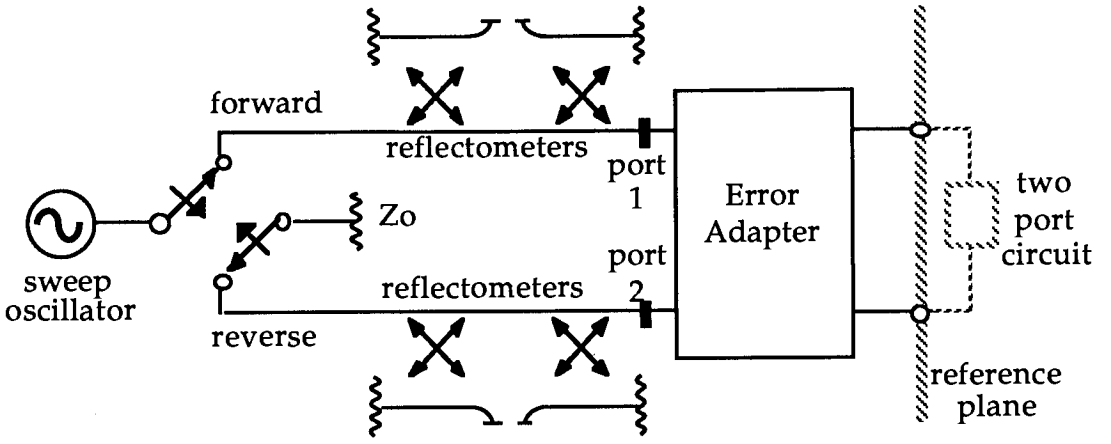


Figure 3.1: Two-port calibration system

be lossless and perfect, having zero phase shift over a range of frequencies.

A block diagram of a two-port calibration system [112] is given in Figure 3.1, where the error adapter algorithm consists of 16 error terms. In most situations, some of these errors are negligible and therefore the number of error terms can be reduced to 12. These are found by presenting different one and two-port impedance and transmission standards at the reference planes. The commonest technique, which offers a good compromise between accuracy and bandwidth uses load, short and open circuit standards for one-port terminations, where the standards must be well characterized, non-redundant and repeatable. Two-port measurements are made using a transmission standard with the reference planes connected together, after which the 12 frequency dependent error terms are calculated. Residual errors remaining after calibration can be attributed to imperfect standards, cables and non-repeatable errors caused by switching, connections and noise.

Following the standard two-port calibration, measurements are made on the device under test, which has been placed in a fixture and

inserted between the reference planes. Usually, calibration standards are not supplied with the test jig; the most accurate available standards are made for 3.5mm and 7.0mm coaxial connectors. Therefore, the effects of uncalibrated transmission line and parasitic circuit elements between the reference planes and the test jig must be accounted for and removed after the measurements have been made [113]. The uncalibrated line is represented by an equivalent circuit, and a small-signal simulation programme such as SUPERCOMPACT or TOUCHSTONE can remove the line effects from the measurements with a de-embedding simulation.

3.2.2 On-chip SOLT Calibration

The principal drawback of the calibration method described above, involves the characterization of the test jig. If the calibration reference planes are moved, so that they lie between the device under test and the jig, the characterization of the jig is unnecessary. Using this method for calibrating MMIC devices, the standards can be realised on-chip and designed in such a way that they can be mounted in the same type of package as the MMIC.

For SOLT calibration, four distinct standards must be available [114]; a short circuit, an open circuit, a matched load and a piece of transmission line. The short circuit should be as small as possible to eliminate coupling effects, unwanted capacitance and inductance. The open circuit should consist of an end piece of microstrip at the reference plane and it should be designed to minimise capacitive reactance and radiation. The accuracy of the matched load is important for establishing a good calibration and it should be as broadband as possible. An alternative to having one matched load, is to use a number of loads, each having a specific frequency band, together covering the whole frequency range.

3.2.3 TRL Calibration

TRL calibration is similar to the SOLT method, described in the previous section, in that the objective of calibration is to remove the effects of the transmission media in which the test device is placed. Three calibration standards are required, comprising a through line, a reflection standard and a delay line [115]. The length of the through line may be non-zero and the through and delay standards must be of different lengths. The advantage of this technique is that only transmission and reflection standards are needed to perform a two-port calibration and a matched load is not required: broadband matched loads are difficult to achieve accurately in many transmission media. The disadvantage is that leakage errors cannot be taken into account.

The calculation of the error terms using TRL is different to standard two-port calibration and a simplified matrix requires only eight error terms to be determined. Using the TRL standards, a total of ten measurements are made and since there are only eight terms in the error model, two additional parameters regarding the calibration pieces can be calculated, rather than having to be estimated. The calculated parameters are usually the complex reflection coefficient of the reflect standard and the propagation constant of the line [116]. Again this offers a direct advantage over standard two-port calibration where the reflection coefficient of the reflect standard must be precisely known and specified.

It is possible in some implementations of TRL to use through lines of either zero or non-zero length and also to use multiple delay lines, where a larger calibration frequency span is required. Any transmission line impedance reference may be used and any highly reflective termination may be used for the reflective standard.

TRL calibration for MMIC measurements employs the use of either on-chip or off-chip standards. On-chip standards have the advantage that once the calibration has been completed, no addition de-embedding of the results is required.

In practice, a matched load accurate over a wide band of frequencies is difficult to fabricate on a MMIC substrate, making SOLT on-chip calibration more difficult. Transmission lines, on the other hand, are amongst the easiest standards to design in microstrip, as the characteristic impedance of the lines is governed by the physical dimensions of the line and the substrate material. However, realising delay lines, especially for low frequency calibration, requires a large area of GaAs on a design mask ($\approx$ 4.0 mm^2) and such extravagance may not be possible, especially if the calibration will be used only a few times. In off-chip calibration, the standards are realised in the medium of the fixture and therefore the fixture is designed so that it can be mechanically split for the addition of the delay standards.

3.2.4 Wafer-probed Measurements

On-wafer measurement systems have been developed by the semiconductor industry to measure fabricated devices, removing the need for labour intensive wafer cutting or component repackaging. Since the mid-eighties, these systems have been modified to measure GaAs circuits at microwave frequencies [117] and some are now commercially available, such as the Cascade Microtech wafer-probe station.

Calibration pieces have been designed for wafer-probe equipment so that accurate measurements can be made. They are designed to be compatible with the shape of the probe tips used by the measurement system. Since the tips are coplanar, the devices and calibration standards

must be designed so that the ground plane is exposed on the top of the substrate.

3.3 TRL with the Thorn-EMI Fixture

3.3.1 Description

The Thorn-EMI fixture was used to perform off-chip two-port TRL calibrations on the network analyser. Shown in Figure 3.2, the reference planes are situated at both ends of the jig microstrip. The test fixture is placed in between the reference planes and is designed so that it can be split apart, where delay line measurements are needed. It consists of two brackets each holding an SMA launcher, screwed into a gold-plated brass block. The device under test is bonded onto a brass tray on top of the block. Separate brass trays are used for each of the TRL standards.

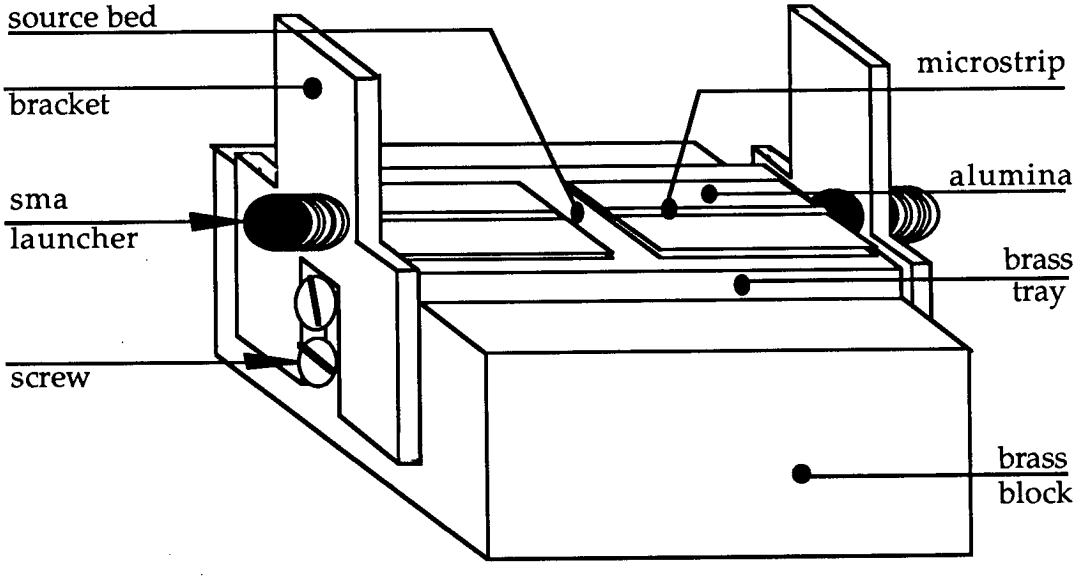


Figure 3.2: Thorn-EMI TRL jig

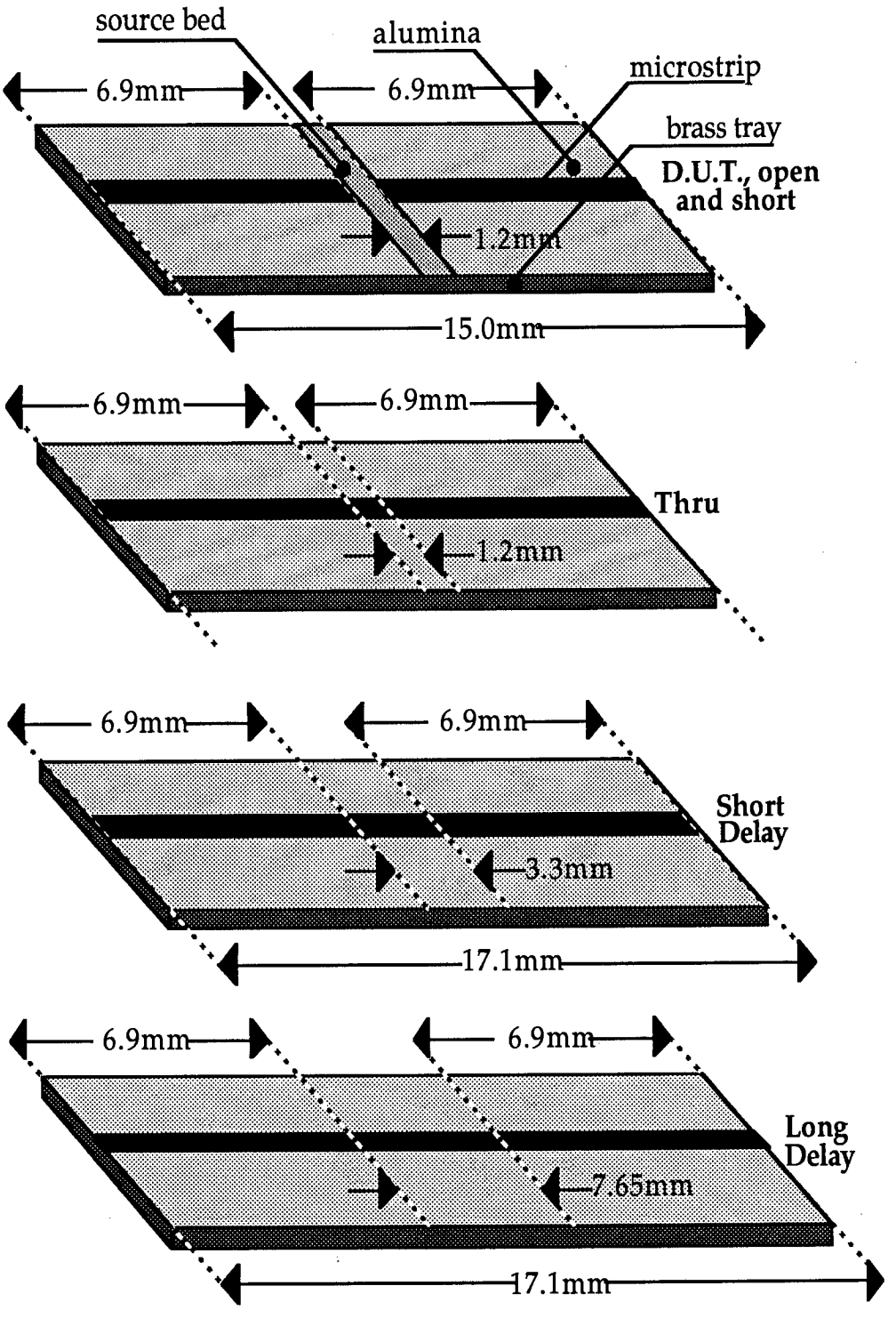


Figure 3.3: Brass trays used on Thorn-EMI jig

An illustration of all of the brass trays is given in Figure 3.3. For the device under test (D.U.T.), the brass tray consists of a centre strip (the source bed) and two rectangular sheets of alumina, with 50 Ω microstrip transmission lines running down the centre. The MMIC is glued with conductive epoxy to the source bed which is 1.2 mm wide and bonded to the two microstrip lines which are each 6.9mm long. The total length of the brass tray is 15.0mm. The open standard consists of an identical brass tray with an unconnected source bed. For the through line, the brass tray consists of a single piece of microstrip on alumina, which is also 15.0 mm long, so that it fits the same length of block as the test device. The reference planes are situated 6.9 mm from each end of the tray and the through line has a non-zero length of 1.2 mm (15.0 - 2 * 6.9). The delay lines have total lengths of 17.1 mm and 21.45 mm, corresponding to actual delay line lengths of 3.3 mm and 7.65 mm between the reference planes.

3.3.2 Calibration using 8510NA TRL Software

The through line has a non-zero physical length of 1.2 mm and the offset delay for the through is calculated as 10.02 pS. (offset delay = electrical length ÷ speed of light. The electrical length is equal to the physical length multiplied by $\sqrt{K_{eff}}$. The offset delays for the 17.1 mm and 21.45 mm lines are 28.2 pS and 64.7 pS respectively and the open and short standards have zero delay offsets.

For accurate TRL calibration [118], the delay lines must satisfy the equation:

$$\text{Phase(degrees)} = (360 \times f \times l) / c$$

where $20 \leq \text{Phase} \leq 160$, f is frequency, l is electrical length and c is the speed of light in air. Therefore the long delay line is valid from 0.86 GHz to 6.87 GHz and the short delay line from 1.97 GHz to 15.76 GHz. If a

calibration from 1.0 GHz to 15.0 GHz is required, both delay lines will be needed. A break frequency f_2 is set between the lower frequency f_1 and the upper frequency f_3 such that $f_2 = \sqrt{(f_1 \times f_3)}$ and $f_2 = 3.9$ GHz. The network analyser requires no further information to perform a two-port calibration. Figure 3.4 illustrates the non-zero length delay and isolation of the through and the non-zero length open and short standards, measured after TRL calibration.

3.3.3 De-embedding using an Equivalent Circuit

The previous subsection described the implementation of TRL on the Thorn fixture. The design of the fixture allows measurements to be de-embedded up to the bond wires which connect the device under test to the microstrip brass tray. For accurate measurements of MMIC components, the parasitic effects of the end of alumina microstrip, the bond wires and the bond pads must be removed and this is done after the two-port measurements have been made.

The end effects and bond pads can be represented by shunt capacitances of 0.02 pF and 0.06 pF respectively and the bond wires by series inductances of 0.9 nH per mm [121]. The de-embedding can be calculated using TOUCHSTONE, where the capacitances and circuit inductances are represented as a two-port NEG2 library function or as normal elements with negative values (see Figure 3.5).

3.4 On-wafer SOLT Calibration with the Tektronix Jig ETF-9000

3.4.1 Introduction

Another calibration procedure was developed as an alternative to the TRL method of the previous section. Whilst TRL measurements were made of test FETs at Thorn-EMI, two-port S-parameter and load impedance

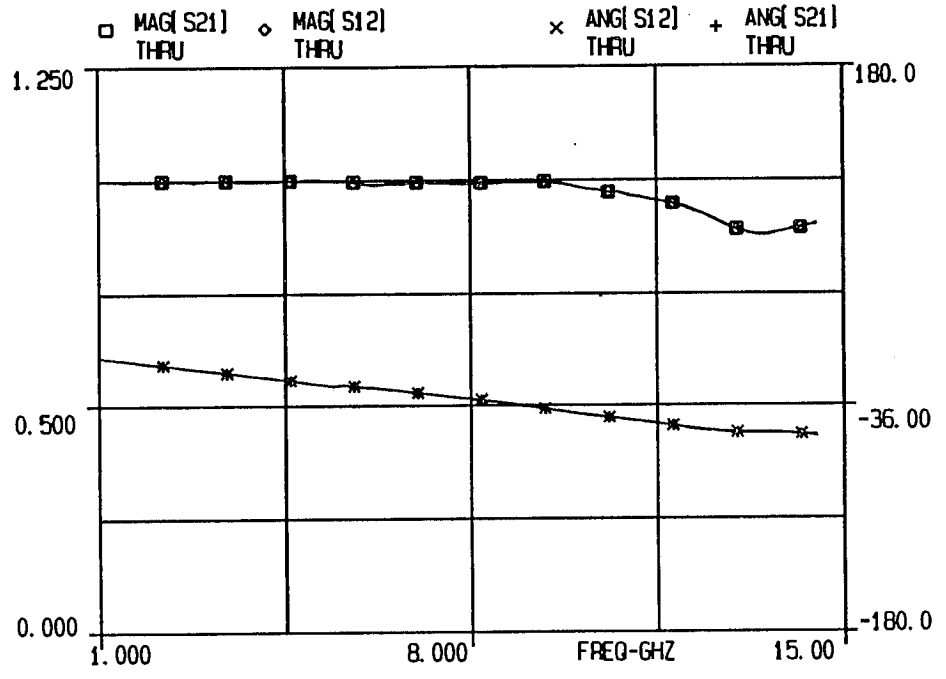


Figure 3.4a: Magnitude and phase response of transmission parameters for non-zero length through

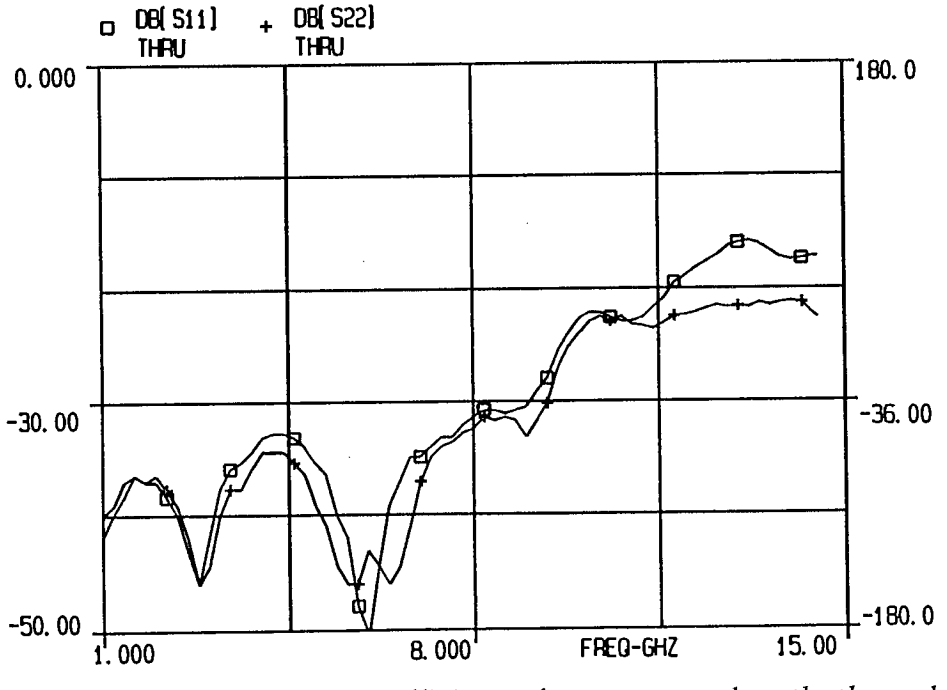


Figure 3.4b: Reflection coefficients for non-zero length through

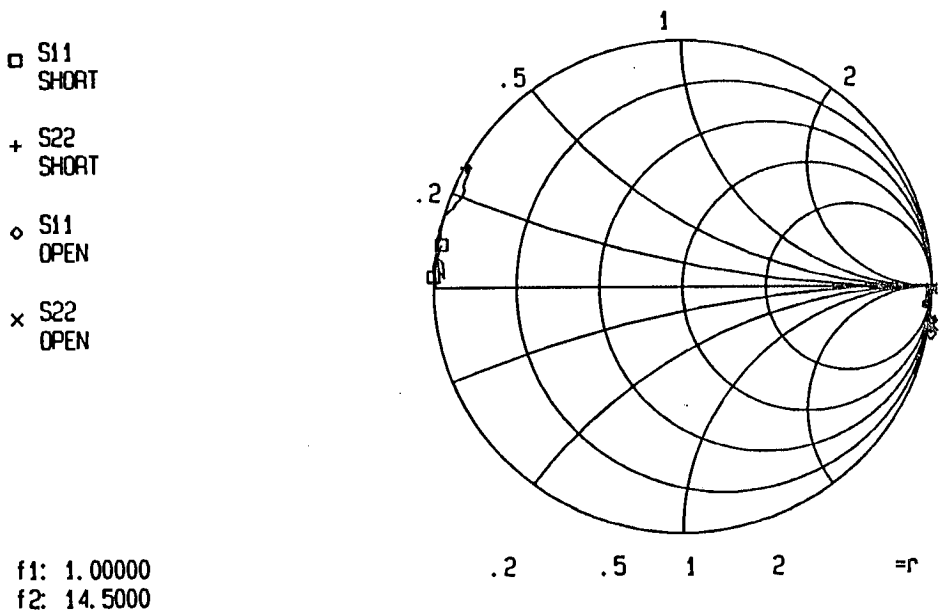


Figure 3.4c: Smith chart plots for non-zero length open and short

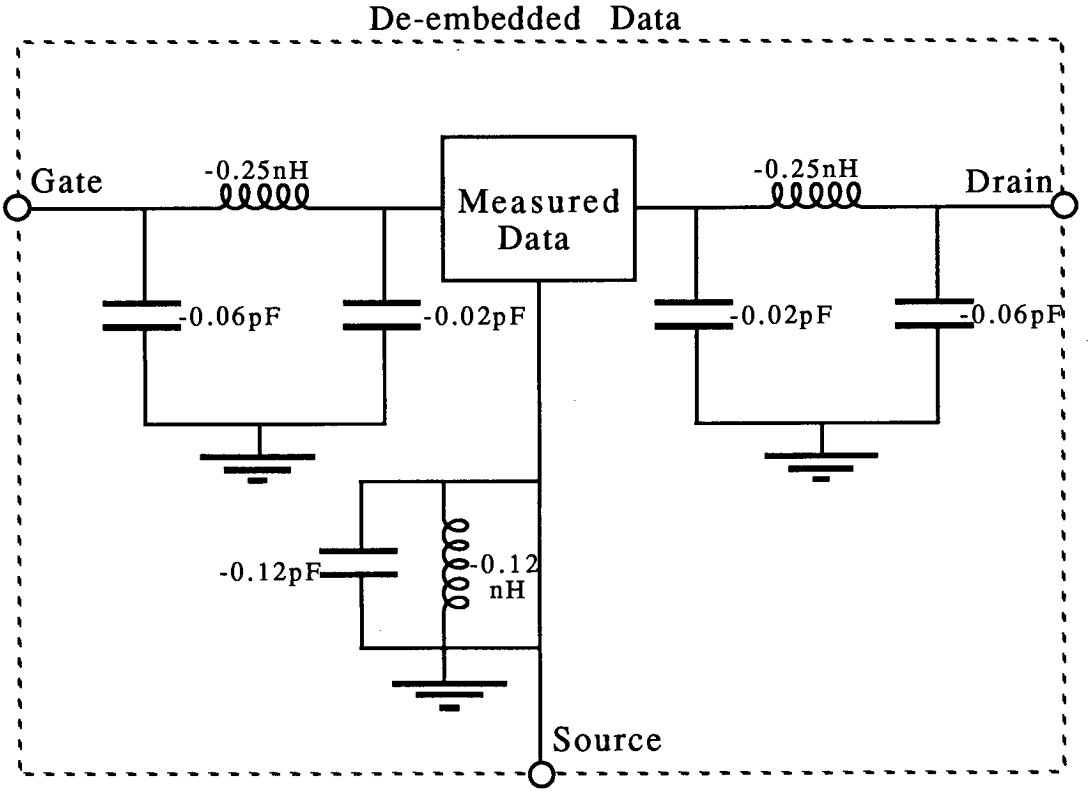


Figure 3.5: Deembedding circuit for TRL calibration

measurements had to be made on fabricated designs at Edinburgh. For these measurements, a Tektronix jig and some commercially available packages (Tektronix PK-MLC20/8) were obtained, into which the devices were epoxy mounted and bonded. The advantage of packaging the devices in this type of fixture was that custom alumina substrates and test jigs did not have to be fabricated for each design.

An illustration of the Tektronix jig ETF-9000 [119] is given in Figure 3.6, consisting of a metal housing containing the microstrip circuit board where the packaged device was placed. The fixture was supplied with 8 Micro-S package leads which had an insertion loss of less than 0.7 dB up to 18 GHz. Calibration standards were not supplied by the manufacturer for either the jig or the package and for accurate calibration, a set of on-chip standards were designed and fabricated, so that the de-embedded measurements could be made accurately. The on-chip calibration technique involved bonding the MMIC calibration standards to the same type of package on which the test devices were mounted. Since the reference planes for the standards were located on-chip, the calibration removed the errors caused by the following repeatable effects:

- non-ideality of 8510VNA directional couplers and connecting cables
- SMA connectors and transmission line losses up to and including the jig
- fringing capacitance at package/jig interface
- bond wire parasitics
- capacitance of on-chip bond pad on calibration standards

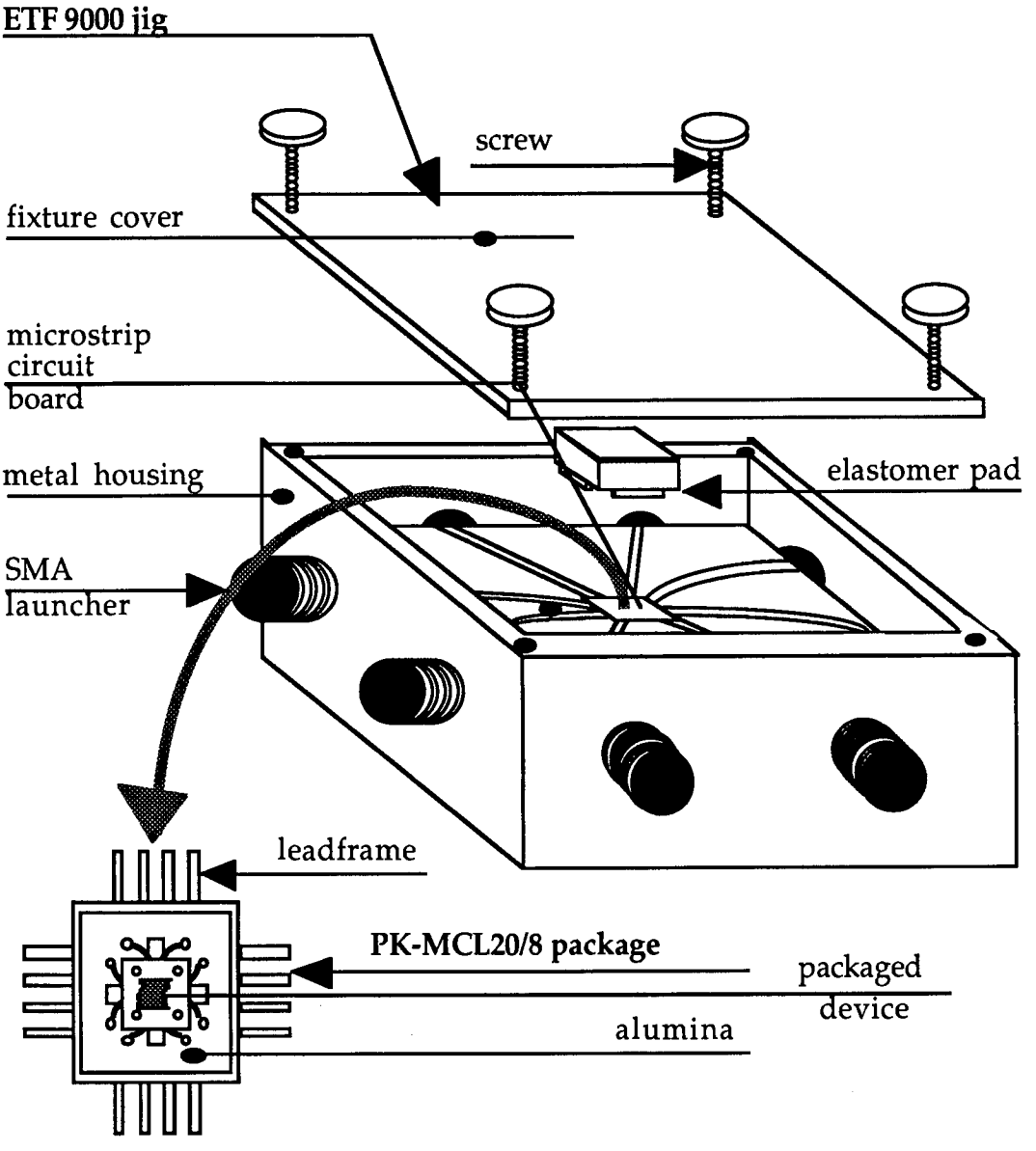


Figure 3.6: Tektronix jig and PK-MLC20/8 package

The package [120] used with the jig was the PK-MLC20/8 supplied by Tektronix and comprised a 54 * 54 mil die foot print on 10 mil alumina supported in a leadframe. It was designed for use with the ETF-9000 and had a useful frequency response up to 12 GHz. The fixture cover clamped the package into the well of the jig using elastomer pads, and the use of the cover ensured mode suppression and provided a greater than 25 dB isolation between any of the ports.

In all calibration and measurement procedures, unused launchers were terminated in 50Ω loads to prevent undesirable jig resonances. Without the terminations, these effects were found to be significant and affected the accuracy of the measurements especially at around 6.5 and 7.5 GHz, where the jig transmission lines had resonances.

It was found by measurement that the 8 ports of the jig had identical electrical lengths to within +/- 0.5°. Each of the 8 ports of the MMIC package also had repeatable electrical lengths and hence the orientation of the package in the jig well was unimportant.

3.4.2 Design of On-chip MMIC Calibration Standards

The accuracy of the 'on-chip' calibration relies on the ability to estimate the parasitics of the standards. In this section, the design of each calibration standard will be described in detail. The following sections describe the methods used to characterize the standards, where S-parameter measurements were taken and analyzed to determine the non-ideality of each standard. A verification of this calibration method is given in the final section where, by measuring an extra delay standard, the 'on-chip' standards can be shown to accurately calibrate the network analyser up to a reference plane lying on the MMIC substrate.

The on-wafer calibration pieces were included on the same design

mask as the test FETs and amplifier designs. Design masks and photographs for the four standards of through, load, short and open and a section of delay line are shown in Figure 3.7. Each standard contains two bond pads, separated by about 1.0 mm. All of the designs measured using this calibration procedure also contain input and output bond pads, separated by the same distance, ensuring that calibration can be made on the substrate beyond the pads.

The short standard comprises a bond pad connected to a via where the via and bond pad are as close together as the Plessey GaAs Foundry design rules [121] will allow. The open is similar to the short but without the via and the reference plane is defined at the end of the microstrip on the open. The through comprises two opens, again approximately 1.0 mm apart, connected by a piece of 50Ω transmission line and the length of this line is the non-zero length between the reference planes. The delay line consists of 2.32 mm of 50 Ω transmission line in an 'omega' shape with four mitred corners. It was used to verify that the calibration technique was accurate and will be discussed later.

The load comprises a bond pad connected to a via through an 'on-chip' 50 Ω resistor and the vias on the two loads are connected together to reduce the inductance of the standards. The impedance of the load is difficult to realise, since it changes with process variations and frequency. The Plessey design manual [121] gives some estimation of how the value of the resistance at high frequencies relates to the DC resistance, using the following equation:

$$R_{rf} = R_{dc} (1 + \beta f)$$

and when β=0.013 and the resistor is designed to be 50 Ω at 4.0 GHz then the design value of R_{dc} is 47.53 Ω. Using the foundry design rules, the length and width of the mesa were calculated.

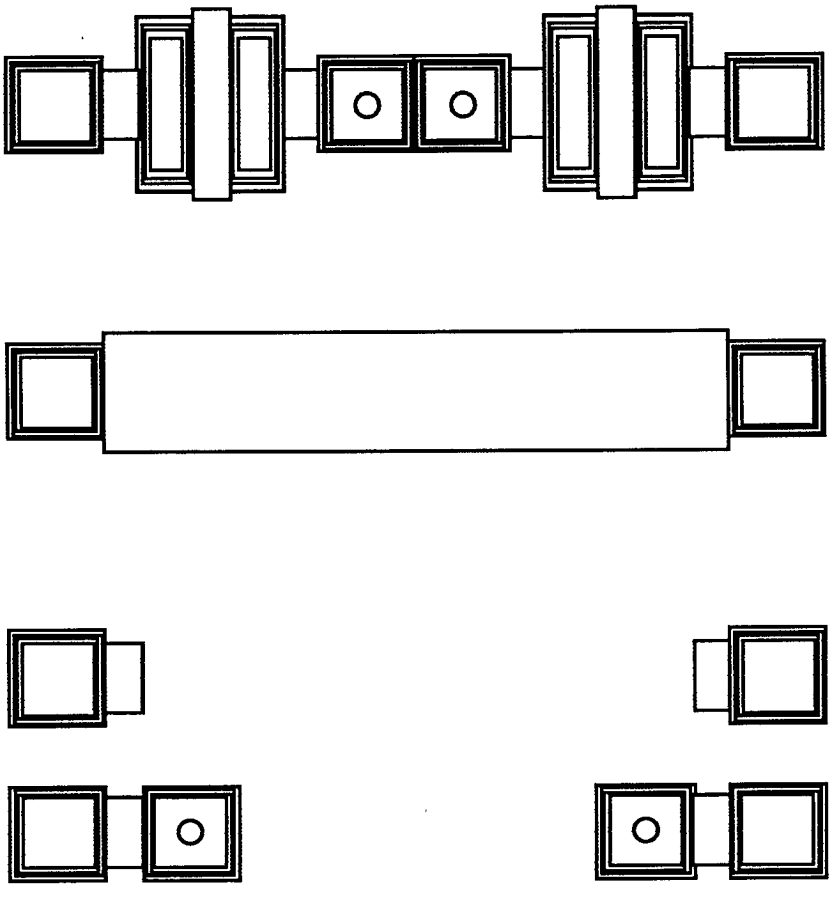


Figure 3.7a: Design masks for the calibration standards, from the top: load, through, open and short

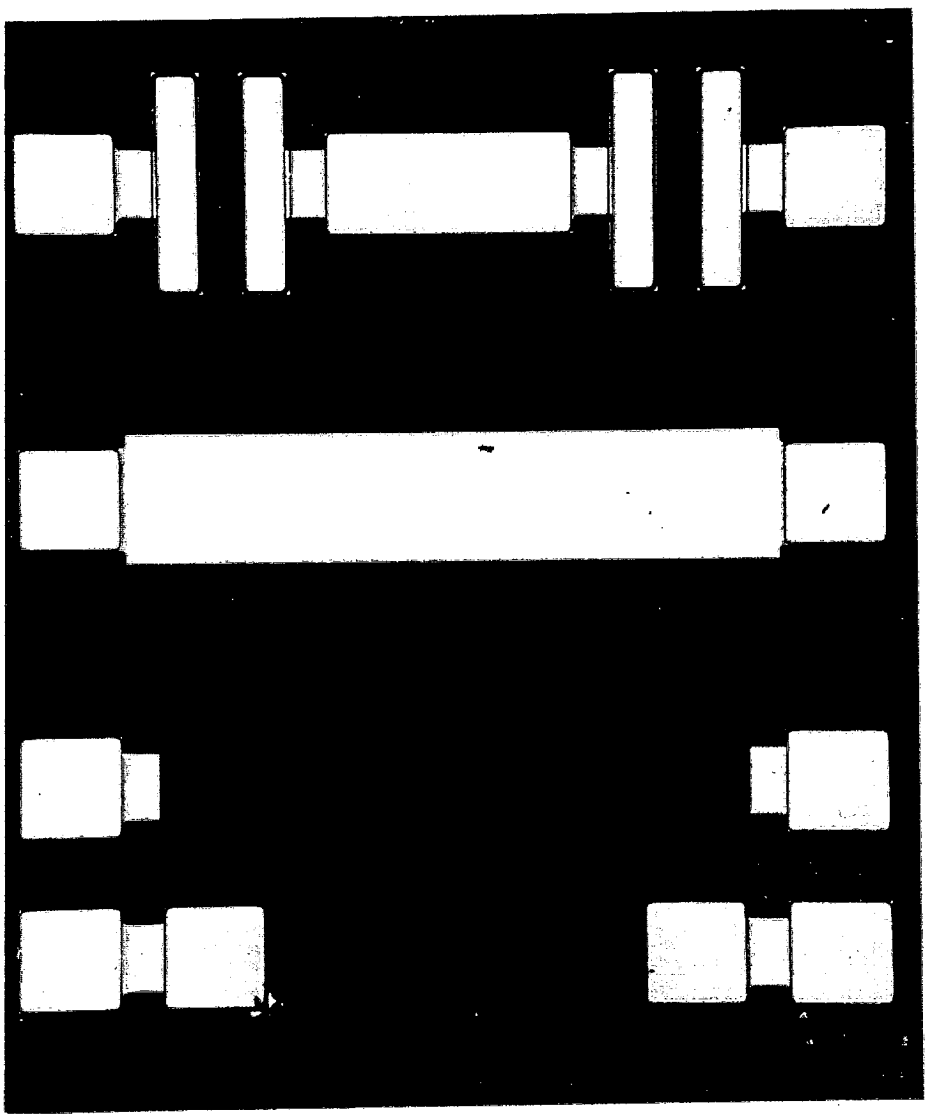


Figure 3.7b: Photographs of the calibration standards, from the top: load, through, open and short

3.4.3 Assessment of Calibration Standards to Evaluate Parasitics

The purpose of characterizing the calibration standards was to evaluate the size of the parasitics contributing to the non-ideal behaviour of each standard. The standards were characterized with S-parameter measurements and from these measurements an equivalent circuit model for the jig and package was proposed, which was the same for each standard. The only difference in the equivalent circuit for each standard, was the type of parasitic element used to express the non-ideality of the standard.

The parasitic information for each standard was specified in the vector network analyser software. For the open standard, the fringing capacitance was used to describe non-ideal behaviour. Similarly, the short standard parasitic was represented with an inductance and the load by an impedance. The actual electrical characteristics of each standard are more complicated, but these simplifications represent the parasitic effects well and are the only indication of non-ideal behaviour that can be specified in the network analyser software.

The fabricated calibration pieces were mounted onto the PK-MLC20/8 package. Four of each type of standard were measured and the phase of the S-parameters tallied to within +/- 4°; the magnitude was within 3%. The discrepancies can be explained by different packages, tolerances on chip fabrication and slightly different lengths of bond wire on each standard.

The first attempt to characterize the jig and package and hence discover the true electrical properties of the standards (as opposed to their idealised design properties) was made using one-port measurements on open, short and loads from 0.1 - 10.0 GHz. The measurements for each standard were compared with a circuit model, based on the physical

structure of the jig, package, connections and the standard characteristics.

The circuit model for each standard, illustrated in Figure 3.8, was the same, except for the standard parasitic (a resistance for the load, a capacitance for the open and an inductance for the short). From the jig, the SMA launcher and the RT-Duroid microstrip from SMA launchers to the package, were modelled using an LC pair and 50Ω transmission line respectively. The connection between the jig and the package was represented by another LC pair and the alumina microstrip in the package was another length of 50Ω transmission line. Capacitive end effects, bondwire inductance, bondpad capacitance and the short stub of transmission line to the reference plane were also included in the circuit model. The length of the transmission line was measured and the bondwire inductance was estimated to be 0.9nH per mm using the foundry design rules [121]. The complete circuit model comprised a total of 10 elements and was a compromise between too few elements which would decrease accuracy and too many elements which would make the solution non-physical.

First of all, the open standard was considered and the physical lengths, capacitances and inductances in the model were optimized between upper and lower limits until the model and measurements agreed well and a value for the open circuit fringing capacitance had been established. The open capacitance was replaced by an inductance (representing the short standard) and a good fit between model and short standard measurements was expected. This however, was not the case and can be explained by the fact that one-port measurements alone are not enough to establish such a large number of elements uniquely and the result arrived at did not adequately represent the physical circuit.

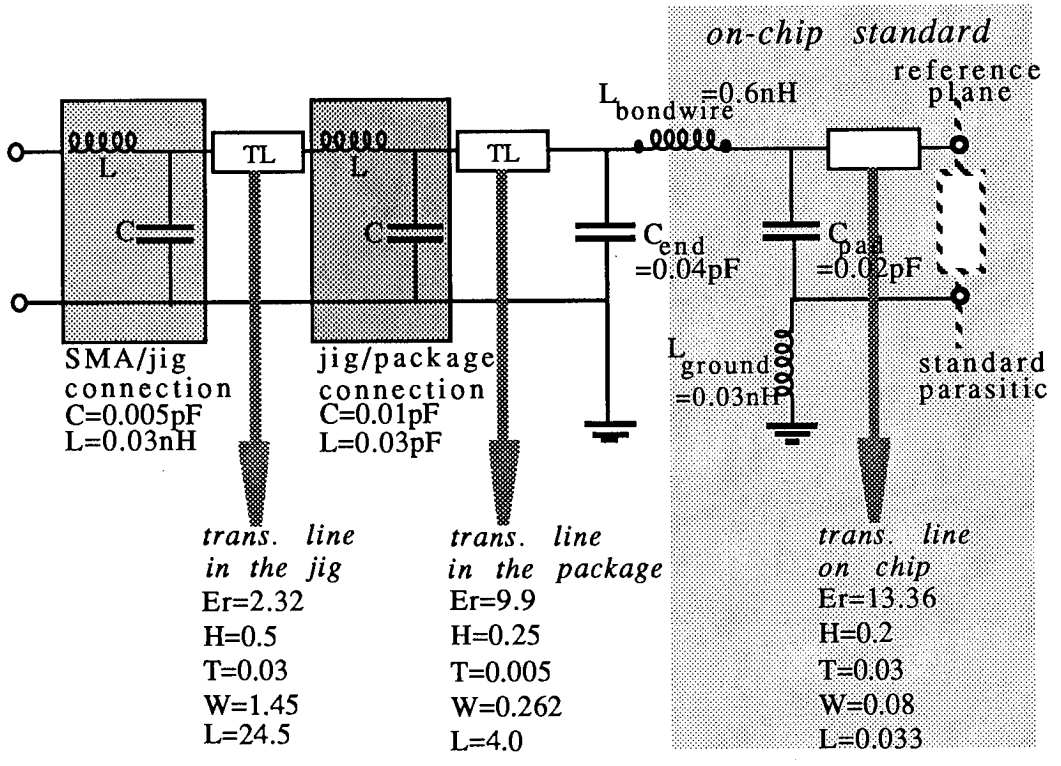


Figure 3.8: Circuit model for the calibration standards, package, jig and connections

To solve this problem, it was necessary to begin by measuring the jig using the through standard with two-port measurements. A greater degree of success was obtained in extracting a model for the jig from the two-port S-parameters than from the one-port measurements. The equivalent circuit for the through standard contained not one but two circuit models connected by a length of transmission line (see Figure 3.9). Because the jig was non-insertable, adapter removal software was used [122] to calibrate the network analyser up to the SMA launchers. The through line connecting the two circuit models was equal to the length of the through standard minus two stub lengths from bond pad to reference plane.

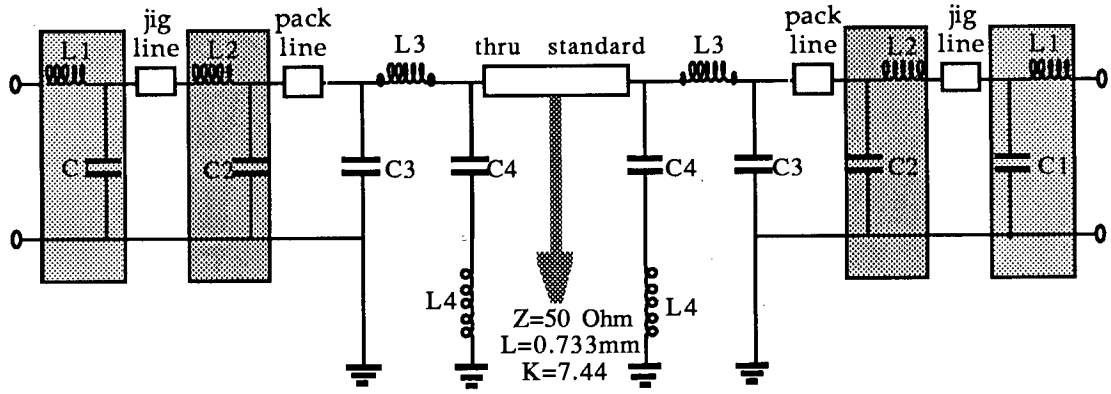


Figure 3.9: Complete equivalent circuit for the through standard

The new circuit model was used to compare the open and short standards with their measurements and a good agreement between model and measurements was achieved with C_{open}=0.012pF and L_{short}=0.03nH. The values of these parasitics were not found to vary greatly with frequency. The load measurements were compared with the circuit model and a load standard model, comprising a thin film resistor with a frequency dependent resistivity, gave good agreement between model and measurements. The DC value of the load impedance was measured as 45.7Ω and the way in which the load changed with frequency was best illustrated with β=0.013.

Comparisons between measured and modelled results for the four standards are given in Figure 3.10. The model of the jig and package predicts the phase and amplitude response of all of the standards very well, especially at low frequencies. Figure 3.11 compares distributed models for the open and short standards with actual measurements for the standards. The measurements were deembedded so that the effects of the modelled jig and package circuit were removed and an excellent agreement between model and measurements can be seen. Figure 3.12 illustrates impedance parameters for an ideal distributed load and deembedded measurements of the load, showing a good agreement at lower frequencies. At higher frequencies, both the real and imaginary components of the measured response diverge from the model, confirming that establishing accurate on-chip load standards at high frequencies is difficult.

3.4.4 Calibration of the 8510 VNA for On-chip Measurement

Having assessed the calibration standards and found that they could be represented by ideal standards with simplified parasitics, the relevant

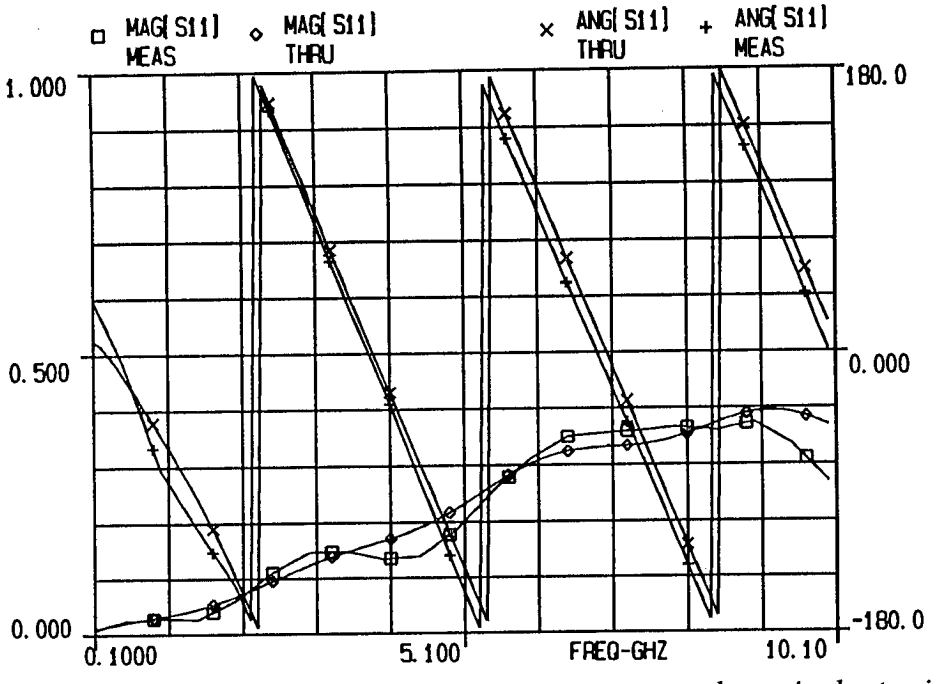


Figure 3.10a: Comparison between measurements and equivalent circuit for through standard reflection coefficients

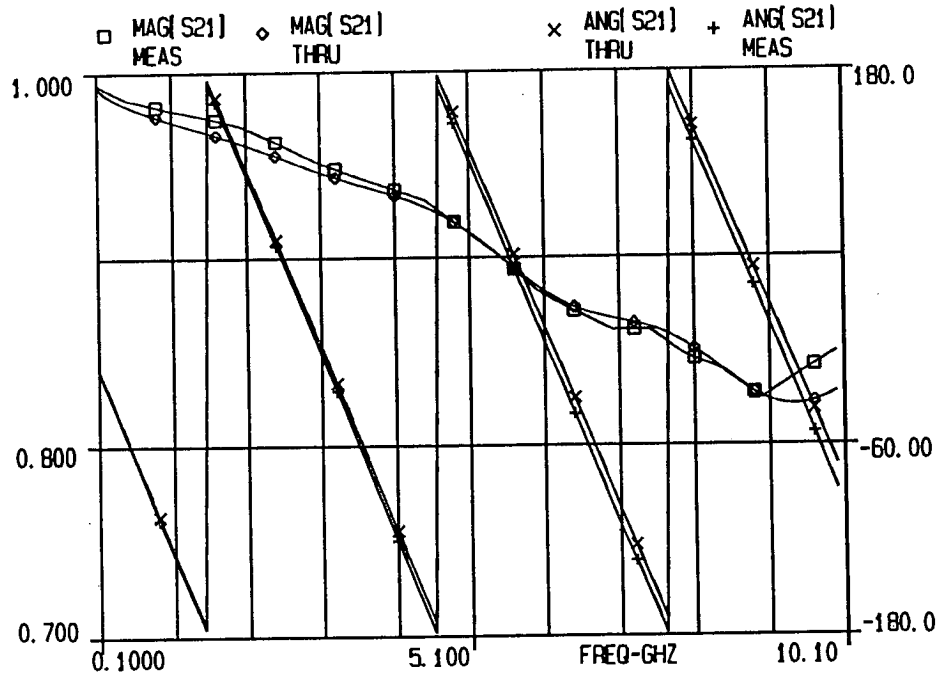


Figure 3.10b: Comparison between measurements and equivalent circuit for through standard transmission coefficients

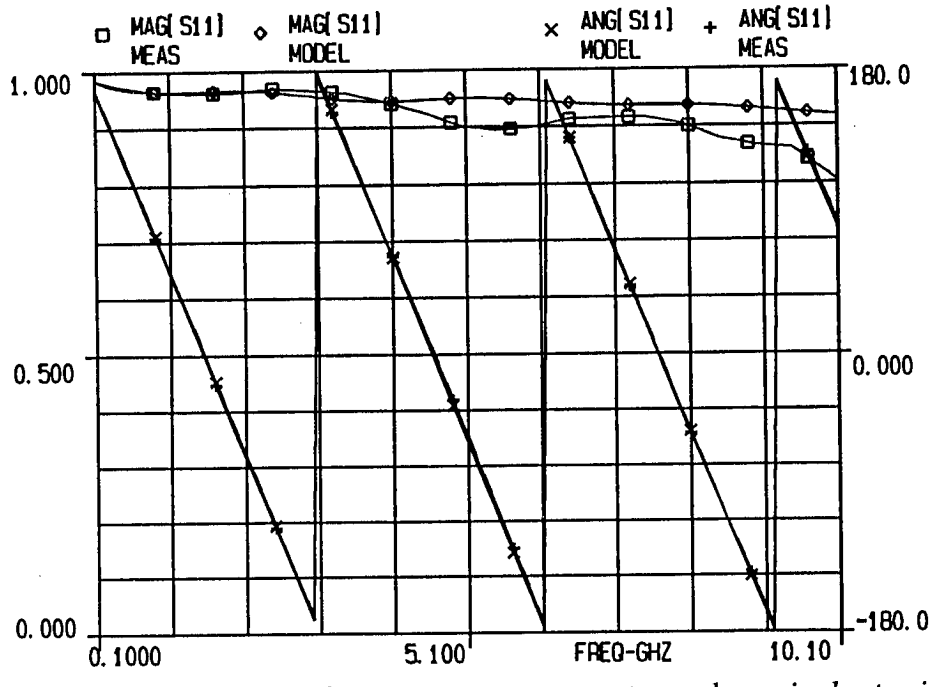


Figure 3.10c: Comparison between measurements and equivalent circuit for short standard

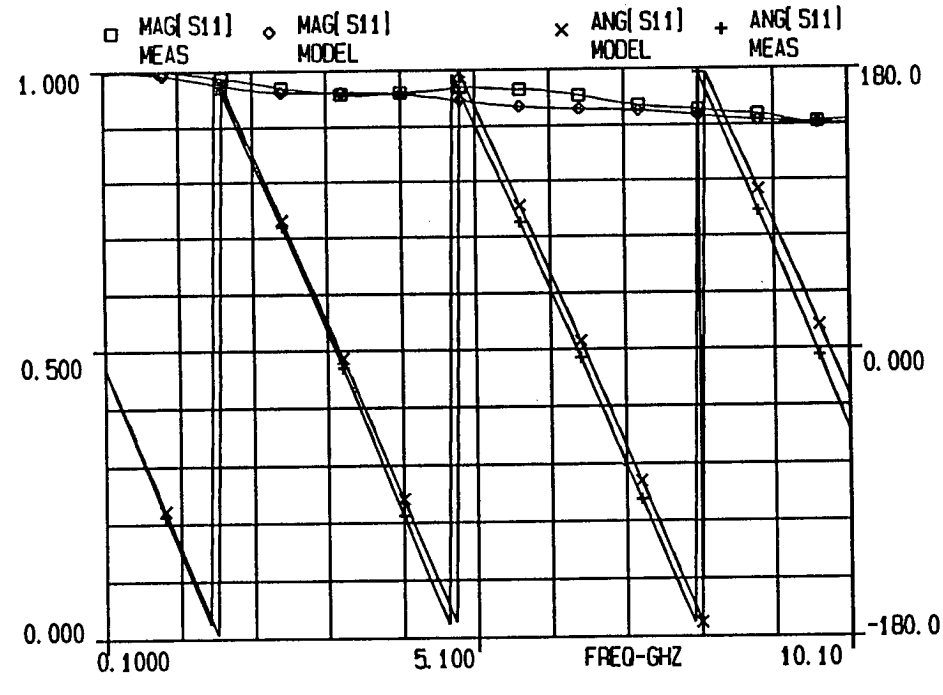


Figure 3.10d: Comparison between measurements and equivalent circuit for open standard

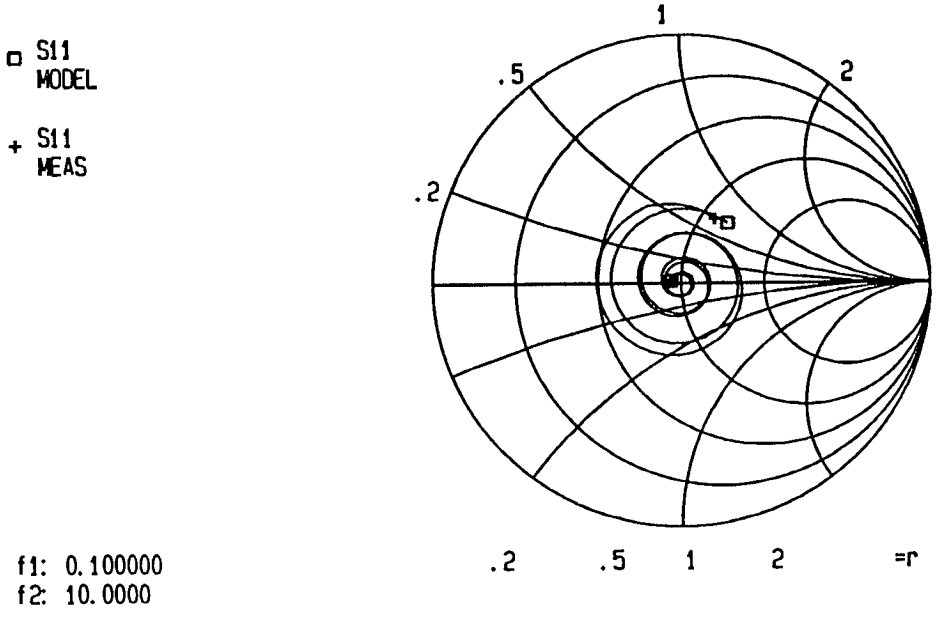


Figure 3.10e: Comparison between measurements and equivalent circuit for ohmic standard

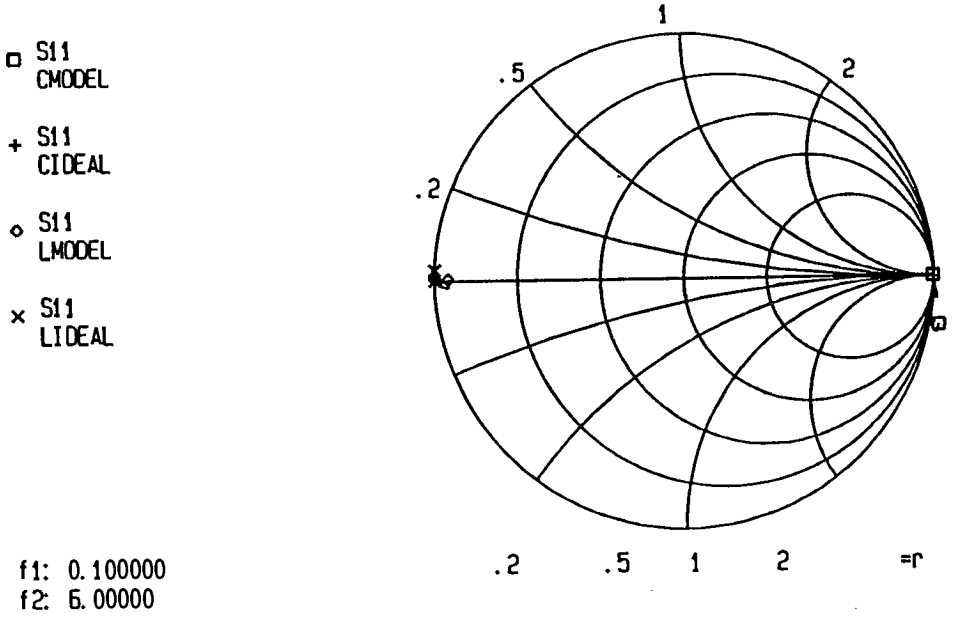


Figure 3.11: comparison between distributed models for open and short standards and actual measurements

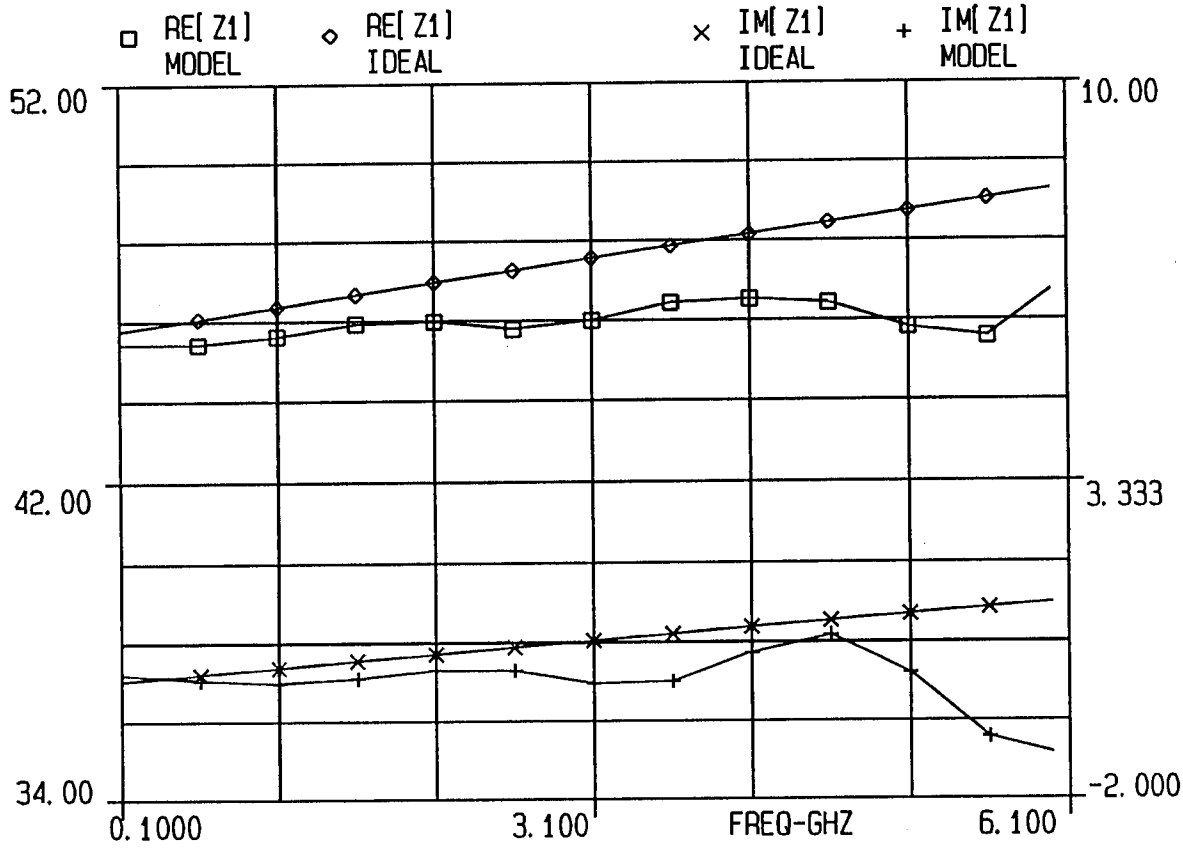


Figure 3.12: Comparison between the impedance of distributed model and measurements of ohmic standard

information was included in the network analyser 'cal-kit' software [114]. The open circuit standard is expressed in the cal-kit as an ideal open with a parasitic capacitance C where $C = C_0 + C_1*F + C_2*F^2 + C_3*F^3$. Since the capacitance was not found to be frequency dependent, C was equal to C_0 (=0.012pF). Similarly, the short circuit standard was stored in the cal-kit as an ideal short with series inductance, modelled, in this case, by a frequency independent inductor, where L=0.03pF.

The load was specified as an arbitrary impedance and although it may have any value of resistive component, no reactive components can be specified for resistive standards. It has already been established that the on-chip load varies with frequency but frequency dependent loads cannot be defined in the cal-kit. The load, however, can be defined in the cal-kit over a frequency band by splitting the band into a maximum of 7 sub-bands, taking the middle frequency of each sub-band and working out the impedance of the load with the formula:

$$R_{rf} = 45.7 \times (1 + \beta F)$$

During the calibration, the user would be prompted for 7 loads when in fact only one physical load is needed, specified with a different impedance for 7 different frequency spans.

The 'cal-kit' through standard is assumed to be an ideal, lossless, zero-length through line with a piece of series transmission line, whose impedance, loss and delay can be given. The through line has a total length from bondpad to bondpad of 738μm and the reference planes are required to be situated 38μm from the bondpads. This gives the through standard an offset length of 738 - (2*38) = 662μm.

All of the standards are defined over the frequency range 0.1 - 10.0 GHz and all have an identical offset which represents the distance of 38

microns from the end of the bond pads to the reference plane. The delay offset is calculated as (length)*$\sqrt{Er}/c$ which for $Er=7.44$ equals 0.35pS.

3.4.5 Verification and Results

After calibration, each of the standards were remeasured and were found to be the same as they had been defined in the cal-kit and this confirmed the good repeatability of the measurement procedure and test jig. A 50Ω chip resistor with a known impedance at frequencies up to 10.0 GHz was also measured correctly.

Additional to the MMIC calibration standards on the design mask, a verification piece in the form of a longer delay line (Figure 3.13) was also fabricated. The total length of the delay line equals 2.32mm which represents a delay of 21.1pS and the line was measured after the calibration had been made. A network analyser plot illustrating the S-parameter measurements of the delay line compared with a TOUCHSTONE simulation of the same delay line (including effects of mitred corners and any cross-coupling) is given in Figure 3.14. There is a good agreement between measured and modelled results indicating that the parasitics of the calibration standards were accurately estimated up to about 10.0 GHz.

The measurements of the delay, chip resistor and standards were all correct and gave confidence in the accuracy of the on-chip SOLT technique.

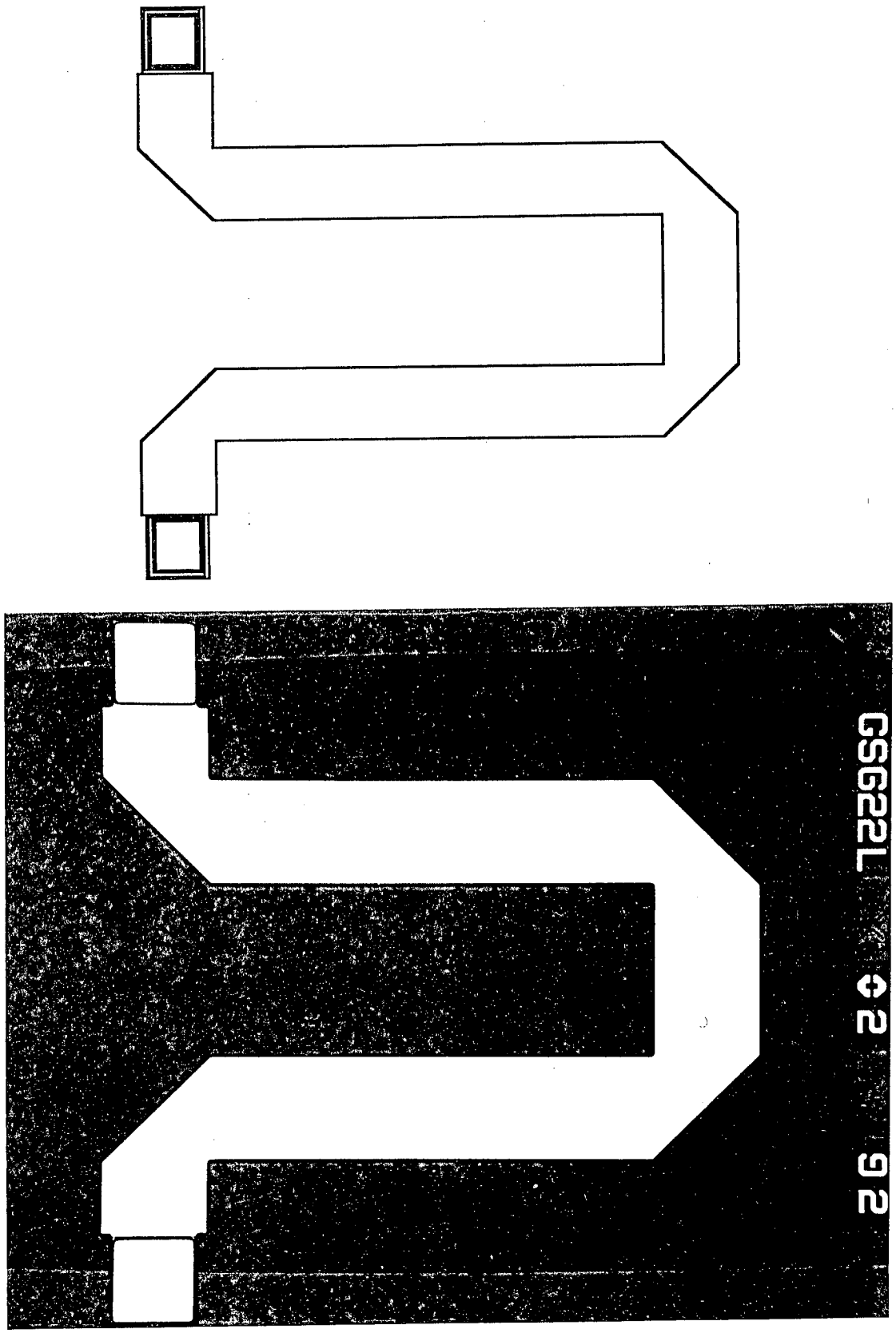


Figure 3.13: Design mask and photograph of the delay line

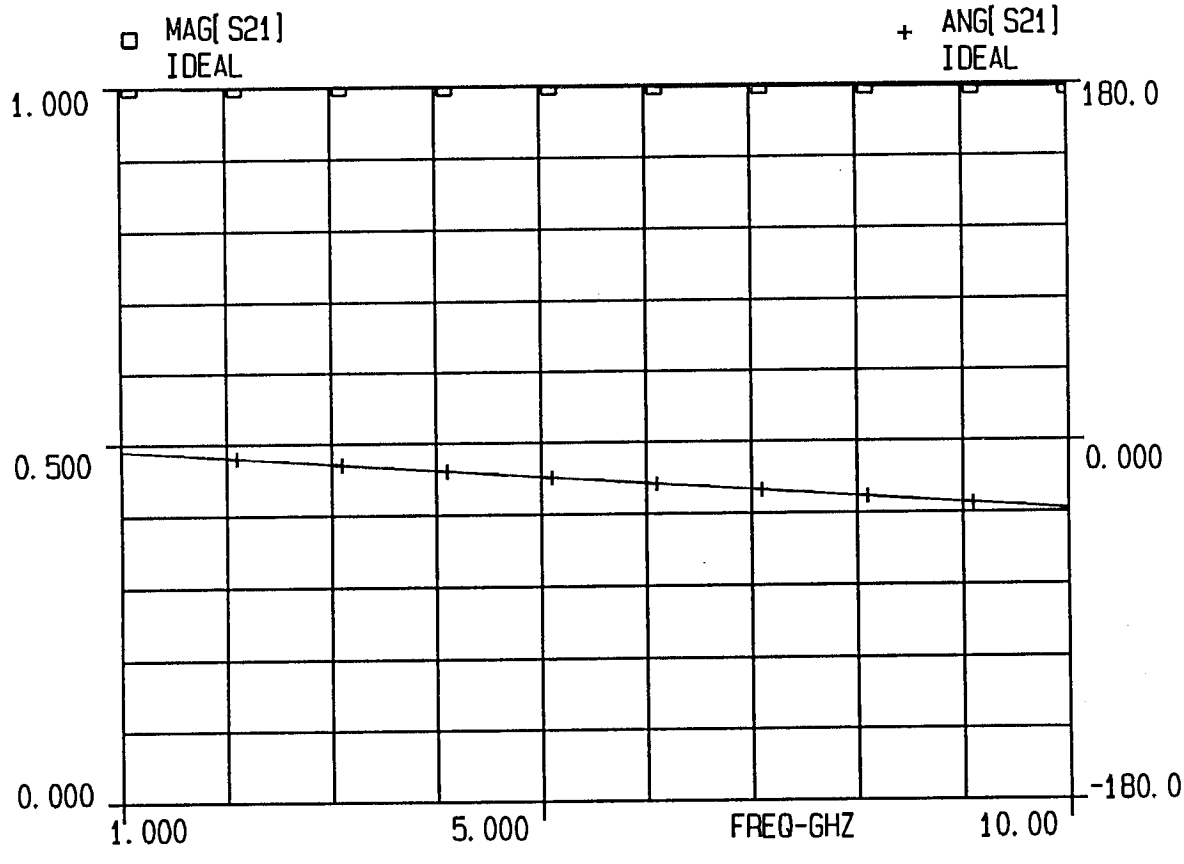


Figure 3.14a: Simulated transmission parameters for the 'on-chip' delay line

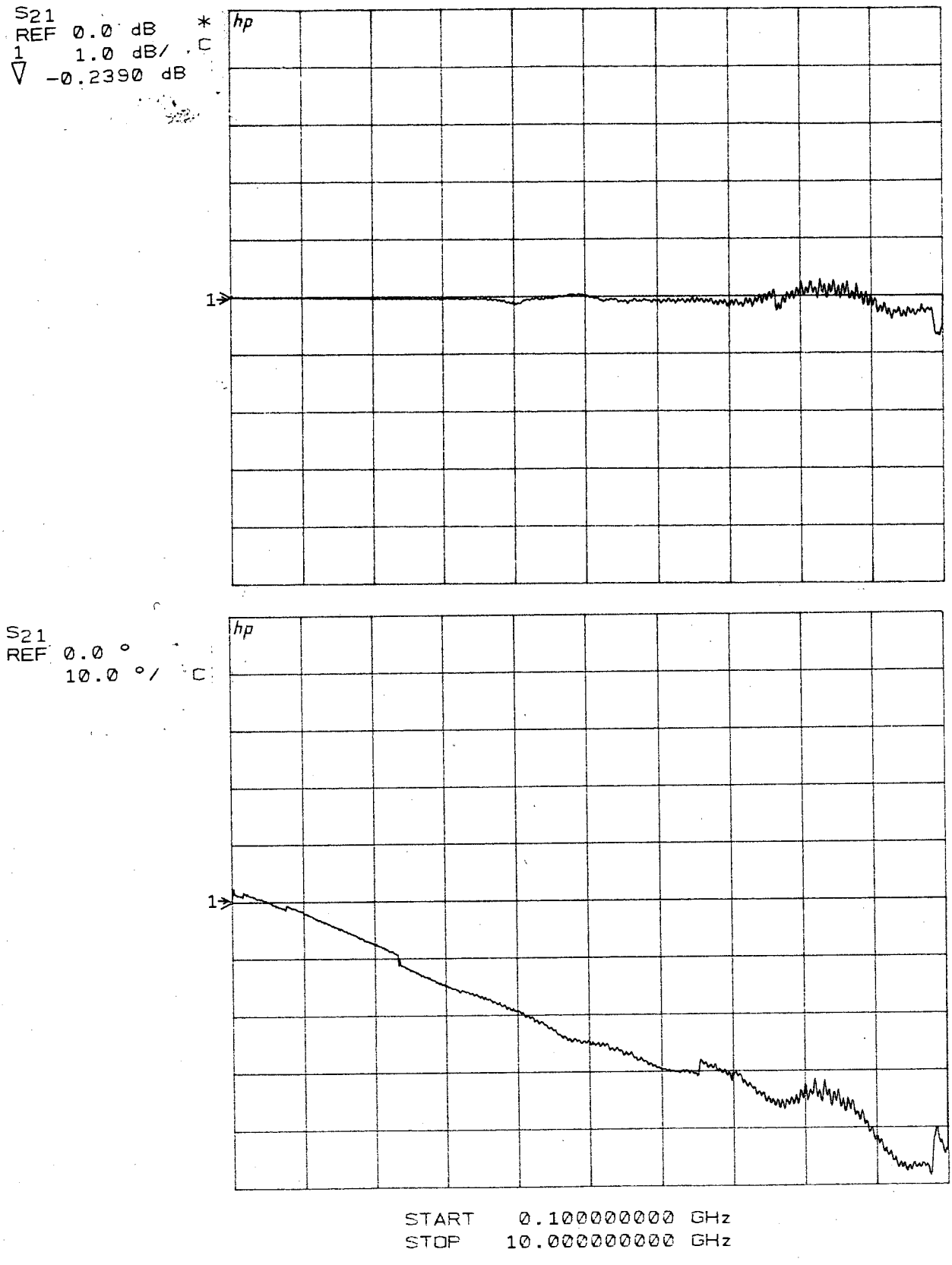


Figure 3.14b: Measured transmission parameters for the 'on-chip' delay line

CHAPTER FOUR - Small-signal Equivalent Circuit and Parameter Extraction

4.1 Introduction

This chapter describes the methods which were used to characterize nonlinearities in the GaAs MESFET. The proposed nonlinear model is based solely on S-parameter measurements where the method used to make accurate S-parameter measurements was discussed in the previous chapter. This chapter describes how the nonlinearities of the MESFET were estimated from the S-parameter measurements. It will be shown that this method is capable of accurately describing the nonlinear behaviour of the MESFET and that the nonlinearities can be explained in terms of device physics. The nonlinear information was used to derive the nonlinear model, using the techniques outlined in Chapter Five.

First of all, S-parameter measurements at many bias points were made. A process, known as 'parameter extraction', was used to derive linear equivalent circuits for the MESFET, from the S-parameter measurements, at each bias point. This was done using a small-signal simulator, and this chapter includes a description of how the simulator was used to produce accurate equivalent circuits. A sensitivity analysis of the model, with respect to bias, determines which of the model elements should be treated as linear and which should be nonlinear.

Parameter extraction techniques are discussed, where linear and nonlinear parameters are extracted from small-signal models. The values of the linear elements are determined and the dependence of the nonlinear elements with bias is discussed. Bias dependent behaviour is also related to device physics. The results of parameter extraction are

presented and compared with other published material.

4.2 Small-Signal Measurements

S-parameter measurements were obtained from test MESFETs, fabricated on the Plessey F1 and F20 processes and the measurements were carried out at Edinburgh University and Thorn-EMI Central Research Laboratories. The most accurate measurements available were a set of wafer-probed S-parameters of F20 devices at various bias points and these were kindly supplied by GEC Plessey Research (Caswell) Ltd.. MESFET measurements were made using a Hewlett Packard 8510B vector network analyser and details of the measurement calibration were given in the previous chapter. The MESFETs were mounted onto microstrip and placed into the jig shown in Figure 4.1. Bias was supplied through bias tees, using a dual power supply.

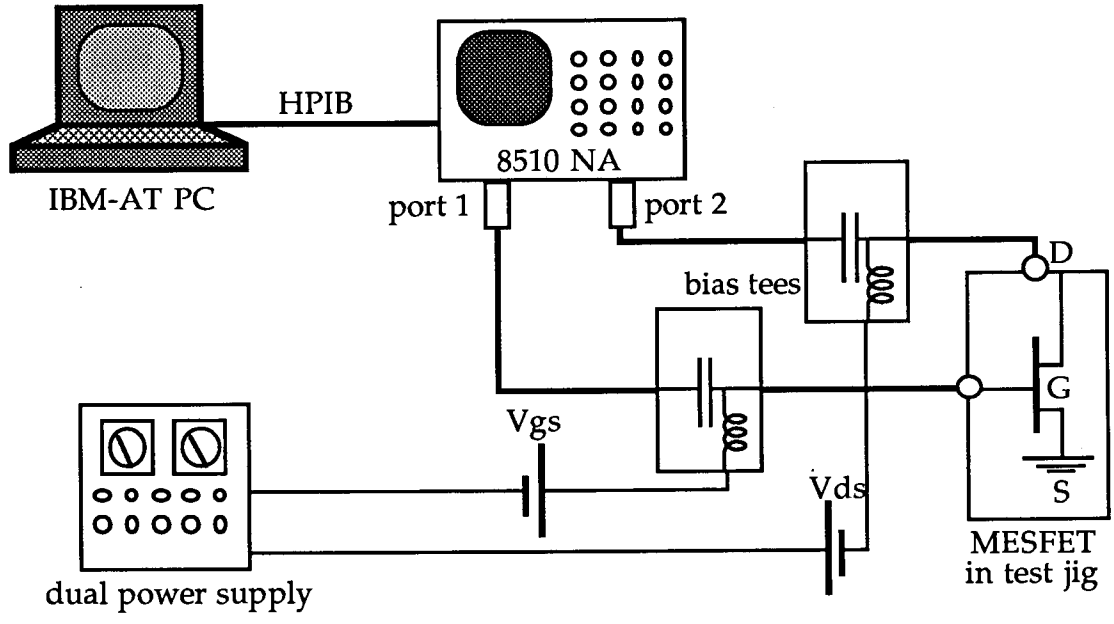


Figure 4.1: Experimental apparatus for making small-signal measurements

The S-parameter results were transferred from the network analyser to an IBM-AT computer which controlled the measurement process via the HP-IB bus. Software was written in HP-BASIC to transfer S-parameters at 75 equally spaced frequency points over the frequency range 0.1 - 10.0 GHz. Data was stored on floppy disks in ASCII files and written in TOUCHSTONE format. A listing of this program is given in Appendix A.

Several sets of FET measurements were made in the course of this project: 'off-chip' TRL measurements were made of 900 micron F1 FETs, 'on-chip' SOLT measurements were made of F20 FETs and wafer-probed measurements were also available for F20 devices, supplied by GEC Plessey Research (Caswell) Ltd.. Because they were the most accurate source of data available, these measurements were finally used to derive the nonlinear model described in this work. S-parameter measurement results at different bias points for the wafer-probed and TRL calibrated F20 devices are illustrated in Chapter Six.

Measurements were made over a range of 0.1-10.0 GHz at accurately measured bias points. The bias settings were determined by the gate and drain voltages where the drain currents were also recorded. Enough points were selected to provide S-parameter measurements over a wide range of bias conditions. It was important to make sure that the MESFETs were well characterized in the linear region, from V_{ds}=0.0 V to the 'knee' point at approximately 1.0 V. Therefore, the interval between bias points in the linear region was smaller than the interval in the saturation region. For the 'on-chip' F20 FETs, bias points were measured for V_{ds}= 0.0, 0.3, 0.6, 1.0, 1.5, 2.2, 3.0, 4.5, 6.0, 7.5, 8.5, 9.9 and 11.5 V and V_{gs}= -2.0, -1.75, -1.5, -1.25, -1.0, -0.75, -0.5, -0.25, -0.13 and 0.0 V. Measurements were made and stored in a matrix of 13*10 bias points for each device. Wafer-probed measurements

for a 300 micron F20 device from Plessey were made at V_{ds}= 0.0, 0.2, 0.4, 0.8, 1.0, 2.0, 3.0, 5.0, 7.0, 9.0 and 10.0 V and I_{ds}= 0.0, 4.0, 10, 20, 30, 40, 50, 60, 80 and 100% I_{dss}. These measurements were more accurate than the 'on-chip' measurements, since the wafer-probe technique tends to produce fewer resonances and a more accurate calibration. Therefore, it was decided that the final nonlinear model should be derived from these measurements, rather that the TRL or the on-chip SOLT measurements.

4.3 Small-Signal Simulator

4.3.1 Introduction

The small-signal simulator is used to translate the S-parameter measurements of the MESFET to an electrical model. Although simulators are used in a variety of calculations, only their use as parameter extractors will be discussed in this section. There are a number of small-signal AC frequency domain packages available and the most widely used are TOUCHSTONE and SUPERCOMPACT, both of which were used in this project. MDS can also be used for parameter extraction.

Figure 4.2 shows the MESFET small-signal model. The reason for choosing this type of topology, over other possible configurations, was discussed in Chapter Two. After S-parameter measurements had been made, a model was required to simulate the measured FET. A listing of the TOUCHSTONE circuit file for the FET model is given below:

```
! simple fet model
! John Simpson
! 12 Jan 1991
DIM
    FREQ GHZ
    RES OH
    IND NH
    CAP PF
    TIME PS
VAR
    CDG\0.120
CKT
    IND  1 2 L=LG
    RES  2 3 R=RG
CAP 3 8 C=CGS
    CAP  3 4 C=CDG
    RES  4 5 R=RDG
    CAP  5 8 C=CDC
    RES  8 9 R=RI
    VCCS 3 5 8 9 M^GM A=0 R1=0 R2=RDS F=0 T=7.0
    CAP  5 9 C=CDS
    RES  5 6 R=RD
```

```
CGS\ 0.30          IND  6 7 L=LD
CDC\0.0013         RES  9 10 R=RS
CDS\0.190          IND  10 0  L=LS
RI\  4.50          DEF2P 1 7 SIMPLEMODEL
GM\  0.04          S2PA  4 5 0 MEASUREMENT_FILE
RDS\ 300           DEF2P 4 5 MEASUREMENT
RS\1.51         OUT
RD\2.60            MODEL SCN
RG\3.50            MEASUREMENT SCN
LS\0.02         FREQ
LD\0.03            SWEEP 1GHZ 3GHZ 0.5GHZ
LG\0.04         OPT
                   SIMPLEMODEL  MODEL  MEASUREMENT
```

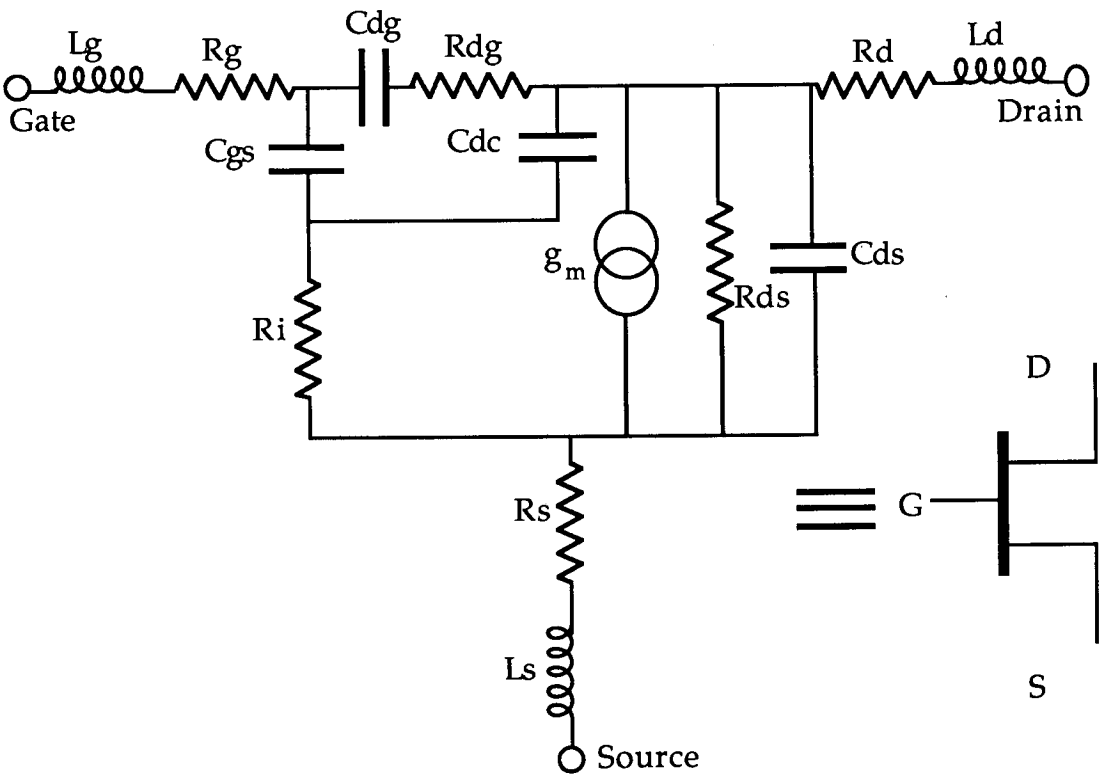


Figure 4.2: The basic small-signal equivalent circuit

Firstly, the simulator calculates the S-parameters for the circuit model, based on the original element values and comparisons are made with the measured S-parameters. Changing the values of some elements in the model may improve the fit between the model and measurements and this can be done using the optimizer, which is part of the software package. The values of model elements can also be changed manually, where the improvement in the correlation between model and measurements can be observed on Smith charts and this can also be done on the simulator. In the following sections, some aspects of the small-signal simulator are explored, which are used for parameter extraction.

4.3.2 Principles of Optimization

In recent years, the need for optimizers in the CAE environment has produced better optimization techniques [123]. For parameter extraction, the optimizer is used to fit complicated models to experimental measurements. Earlier techniques relied on one-dimensional or 'one-at-a-time' searches where each model element was optimized on its own, in an effort to reduce the error (the difference between the model and the measurements). Most modern optimization routines rely on multi-dimensional pattern search techniques, such as the Hooke and Jeeves, Rosenbrock and Powells methods [124].

Three different algorithms are implemented for error minimization in the optimizer incorporated in TOUCHSTONE [32].

(1) Random optimization involves a trial and error process where the original conditions are randomly modified and a note is taken of results indicating a substantial drop in the error.

(2) Gradient optimization is more systematic and for each iterative step of the solution, the gradient of the error is calculated with respect to each model element. The values of the elements are modified and the error is recalculated. This process continues until a minimum is reached and no better results can be found.

(3) The Quasi-Newton optimization is similar to the gradient search but employs an additional formula to find the direction of the search, speeding up the location of the best solution.

4.3.3 The Error Term

There are a number of different ways of emphasizing the error between two sets of data. At a single data point, the error e_j is calculated as the difference between the measurement and the model. The least squares (l_2) error is defined as the square of the error, and the total error E is given as:

$$E = \left[\sum_{j=1}^{m} |e_j|^2 \right]^{1/2}$$

where there are m frequency points. The least squares error is most frequently used and is differentiable, which means that the minimization gradients are easily calculated.

The l_1 error term is calculated from the summation of unsquared errors which attaches more importance to small errors. The l_p error term is calculated from the summation of errors to the power p and for large values of p, more importance is attached to the larger errors. Neither of these error terms are differentiable and minimization of the error requires the use of additional algorithms.

Recent versions of TOUCHSTONE [32] and SUPERCOMPACT [31] offer a greater variety of error terms than in the past. In TOUCHSTONE the least squares error term and two varieties of l_p error calculation known as Minimax and Least p^{th} are available. In practice, the choice of error term for parameter extraction makes little difference to the final result. The least squares error was normally used as there was no particular reason for emphasizing the larger or smaller errors as in the l_1 and l_p error terms. It has been found that the l_2 error term produces the best fit when a model is fitted to noisy measurements, where the noise has a random Gaussian distribution [20].

Having established the required type of error term, it is possible to define goals in the circuit file which emphasize particular S-parameter measurements (S_{11}, S_{21} etc.) or frequency bands. If, for example, a model element affects S_{11} more than it affects S_{21} or S_{22}, the goals are set to emphasize the fit on S_{11}. This may help to optimize the model and increase accuracy of that element value, perhaps at the expense of the accuracy of other element values.

4.3.4 Using the Optimizer for Parameter Extraction

The optimizer assisted in fitting equivalent circuits to the S-parameter measurements. From starting conditions, before any optimization had been used, there was a large error between the equivalent circuit and the measurements.

The gradient or quasi-Newton searches converged on a minimum but this did not always produce the solution with the lowest error. The starting point was too far from the best solution and a local minimum in the error surface had been found instead. Indeed, the task of locating the best minimum in unconstrained optimization has been likened [126] to a

blind man attempting to reach the village of the lowest valley in the Himalayas.

When the error was large, random optimization was used: the lowest error indicated a result in the vicinity of the best minimum and was obtained by altering each circuit element randomly. Typically this would require about 200 steps on the TOUCHSTONE random optimizer. A further 10 steps on the gradient optimizer would then be used to achieve the best minimum.

This method is illustrated in Figure 4.3. The surface represents a plane of possible starting values for two variables x and y (in a small-signal model there are fifteen starting values). Different combinations of x and y produce different values for the resultant error z. A gradient optimization at point A will disappear into a local minimum. Four random optimizations produce starting points at B, C, D, and E. Of these, D is the most promising and after further gradient optimization, the best minimum is reached.

Linden *et al* [127] have examined a method whereby the equivalent circuit is extracted from S-parameters using parallel optimization. Rather than performing one local optimization as is usually the case, a number of local optimizations are carried out before a gradient search begins. This is achieved using a network of transputers and had the effect of increasing the amount of computation that could be administered for each extraction. Results showed that model errors were significantly reduced, although the current limited availability of transputer networks would normally make this method impractical.

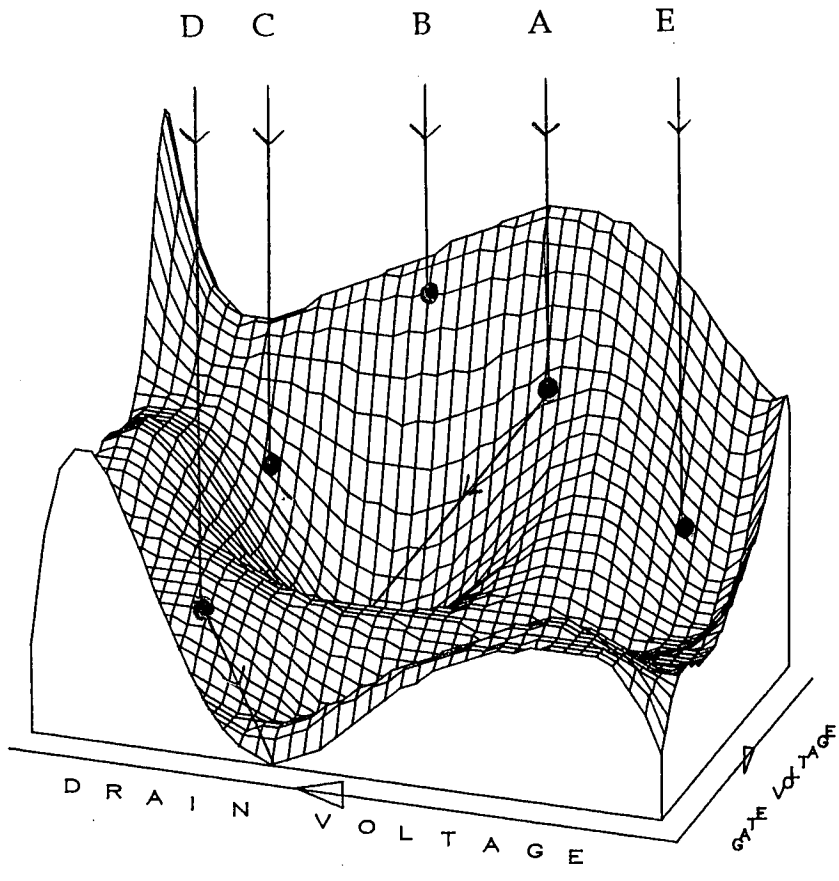


Figure 4.3: 3-D illustration of error surface with local minimum

4.4 Parameter Extraction for Single Bias Measurements

4.4.1 Introduction

Parameter extraction is the process by which experimental measurements (S-parameters) for a test device (the GaAs MESFET) are used to create a linear equivalent circuit model. Small-signal simulation packages, namely SUPERCOMPACT and TOUCHSTONE, are used to extract parameters from the measurements.

Efficient optimization routines are available in most packages and an easy way to achieve an accurate match between the model and the measurements is to attribute each element in the model with an approximate starting value and optimize all of the values until the lowest

error is found. It is possible that many models can be found, all with identical topologies, but where the element values of each model are different. Some of the models are unsuitable because the values of certain elements will not relate to the physical characteristics of the device and a more systematic approach may be needed to calculate the model elements.

For most applications, an improved technique for parameter extraction is needed and these are discussed in the following subsections. Some methods calculate some or all of the parasitic elements (R_g, R_d, L_d etc.) leaving the remainder of the elements to be calculated by optimization as above. Other methods seek to establish all element values without the use of any optimization. Most techniques require additional information such as DC or pulsed I-V characterization, zero channel bias FET measurements or low frequency S-parameters (less than 0.5 GHz) and these are discussed in the following subsections. The chosen method depends on the availability of measurement equipment, the required accuracy of the model and the application for which the model is needed.

4.4.2 DC characterization

The simplest way to characterize the MESFET is to measure the drain current with changes in terminal voltages and gate current with forward gate voltage. However, DC characterization fails to predict MESFET performance at high frequencies (as discussed in Chapter Two) because some of the model elements exhibit frequency dispersion. Some model elements, such as the output conductance, show a strong dispersive nature while others are weaker functions of frequency.

Pulsed I-V measurements offer advantages over DC characterization [128, 129] in that the FET can be characterized over a broader bias range than can safely be achieved with standard DC

measurements. Dispersion effects can be estimated with greater accuracy [130], since pulsed measurements are able to take account of the 'traps' found in GaAs MESFETs. However, the hardware required for pulsed measurements is usually not readily available and normal DC measurements are made instead.

Although DC measurements alone are insufficient to produce a high frequency model, they can be used to establish the value of the parasitic resistances R_g, R_d and R_s using the Fukui method [131, 132]. When the gate junction of the simplified small-signal model in Figure 4.4 is forward biased, it behaves like an ideal diode. The forward conduction properties of the gate junction are represented by the diode D_{gs} across the capacitor C_{gs}, described by the equation:

$$V = nkT/q * \ln (I/I_s + 1)$$

I_s is the reverse saturation current of the Schottky junction, q is the electronic charge, V is the applied forward potential, n is the ideality factor, k is Boltzmann's constant and T is the device temperature. As V increases, so does the effect of the series resistance R_{series} which is found by plotting the forward gate current against the positive gate bias. An example of this is given in Figure 4.5, featuring a 300 micron FET from the Plessey F1 process. Gate current measurements can be made on the MESFET in 3 different ways; with an open-circuited drain terminal where $R_{series} = R_g+R_s$, with an open-circuited source terminal where $R_{series} = R_g+R_d$ and with source and drain connected where $R_{series} = R_g+R_d//R_s$. The parasitic resistances can be now found as there are three equations with three unknowns. The disadvantage of this method is that the measurements are made under forward bias conditions, when in fact the circuit designer is likely to be more interested in negative gate bias points.

The transconductance g_m in the small-signal model is defined as

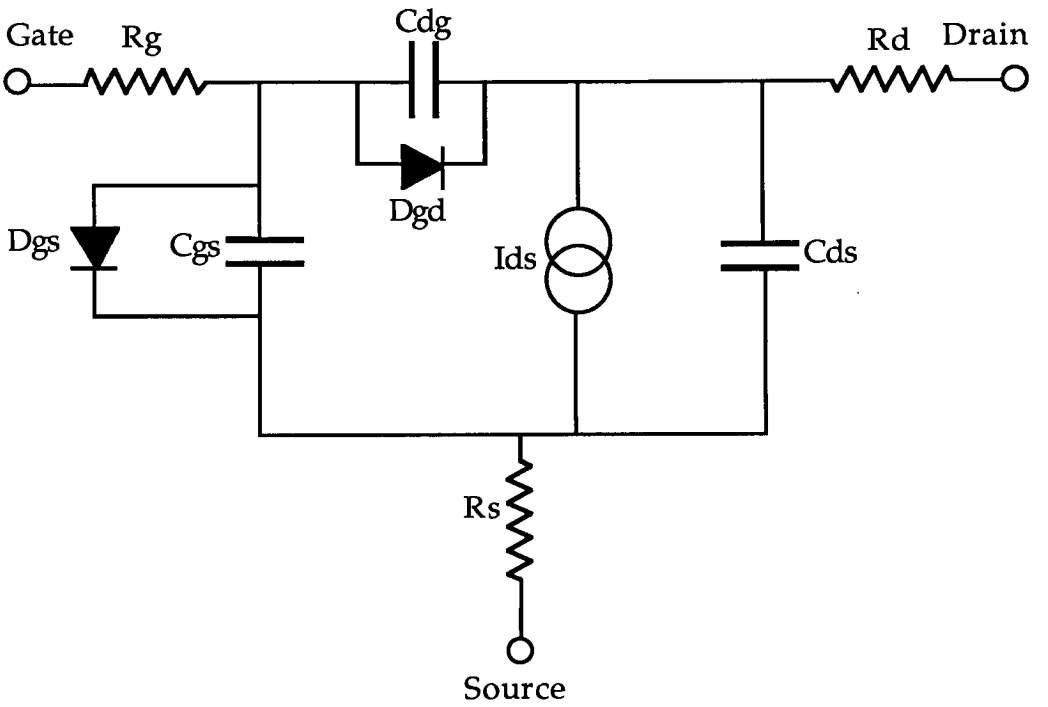


Figure 4.4: Simplified small-signal model

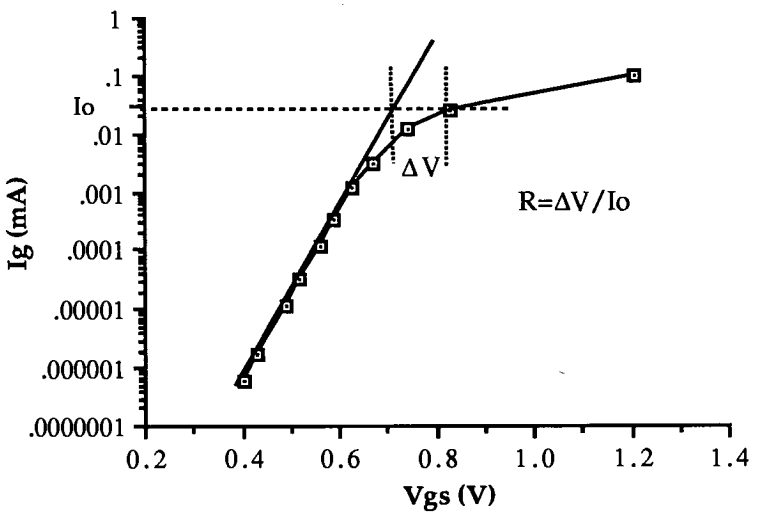


Figure 4.5: Forward gate current of 300 micron F1 MESFET

the change in current with the gate voltage or:

$$g_m = \partial I_{ds}/\partial V_{gs} \,|_{V_{ds}}$$

and the value of g_m at high frequencies is usually assumed [133] as being the same as the value of g_m for DC characteristics. In practice however, this is not usually the case as g_m exhibits frequency dispersion effects, which will be discussed later in this chapter.

4.4.3 Zero Channel Bias Measurements

The equivalent circuit model can be simplified when zero channel bias (V_{ds}=0) or 'cold' measurements are made, making the calculation of the parasitic elements easier [134]. The simplified model includes a distributed gate element and is shown in Figure 4.6. The parasitic resistances are calculated by the Fukui method described in the previous section. Whereas the values of parasitic resistances vary widely with different optimization methods, the values for R, C and the parasitic inductances do not vary much and unique solutions can therefore be found after only a few optimization steps.

Dambrine *et al* [135] have extended this work to find all of the bias independent elements from 'cold' measurements. Two-port Z parameters were evaluated to describe the simplified MESFET model and the parasitic inductances were calculated from these. Two of the three parasitic resistances could then be found provided that the remaining resistance was calculated using Fukui measurements or some other method. The remaining elements were found by calculating the Z-parameters of the 'intrinsic' device from the complete measurements (see Figure 4.7) and converting them into Y measurements [136] where:

$$Y_{11} = R_i C_{gs}^2 \omega^2 + j\omega (C_{gs} + C_{gd}) \qquad (4.1)$$

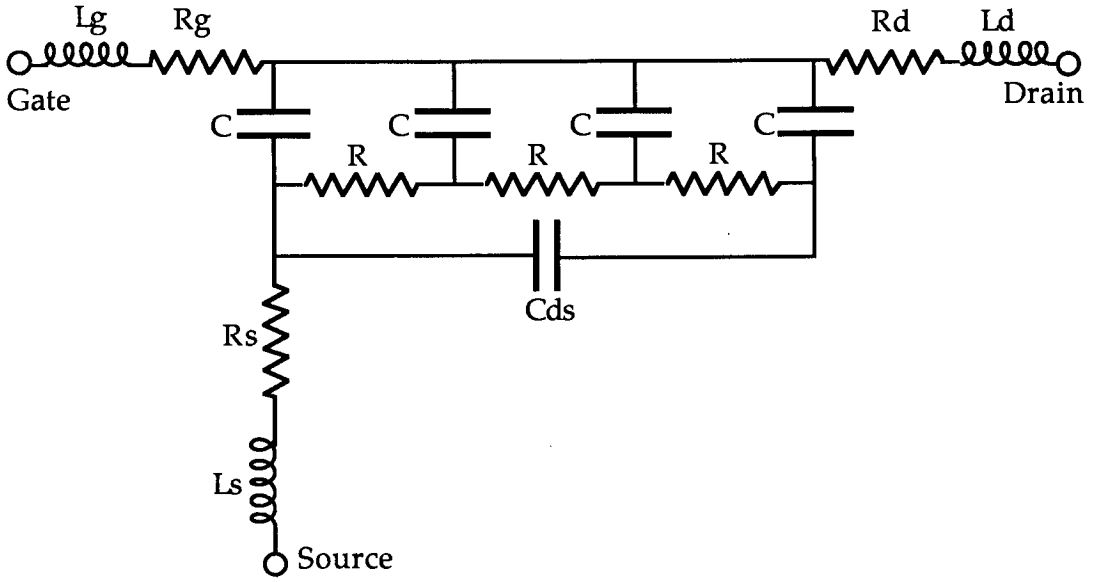


Figure 4.6: Equivalent circuit for 'cold' measurements

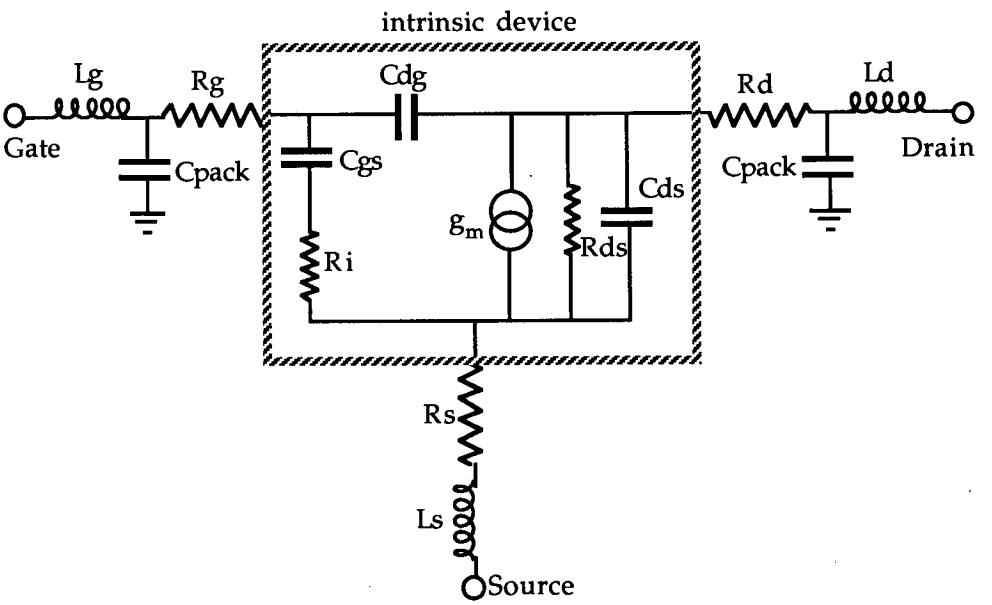


Figure 4.7: Equivalent circuit illustrating the intrinsic device

$$Y_{12} = -j\omega C_{gd} \tag{4.2}$$

$$Y_{21} = g_m - j\omega (C_{gd} + g_m(R_i C_{gs} + \tau)) \tag{4.3}$$

$$Y_{22} = g_d + j\omega (C_{ds} + C_{gd}) \tag{4.4}$$

This approach has also been extended [137-139] to determine the internal device parameters analytically over a larger frequency range. Vickes [140] also used the same approach as Dambrine to derive expressions for all of the elements in the equivalent circuit: his model included the capacitance C_{dc} as it was found to have a significant affect at high frequencies.

4.4.4 Low Frequency S-parameter Measurements

The assumption made at low frequencies is that the inductive parasitics can be neglected [141] since the inductive reactance is much smaller than the reactive component of the Z parameters. As in the previous section, the 'intrinsic' model was derived from the 'extrinsic' model by removing resistive and inductive parasitics. If Z_{ij} represents Z parameters of the whole model and z_{ij} represents the intrinsic model only, then:

$$z_{11} = Z_{11} - (R_g + R_s) - j\omega (L_g + L_s) \tag{4.5}$$

$$z_{12} = Z_{12} - R_s - j\omega L_s \tag{4.6}$$

$$z_{21} = Z_{21} - R_s - j\omega L_s \tag{4.7}$$

$$z_{22} = Z_{22} - (R_d + R_s) - j\omega (L_d + L_s) \tag{4.8}$$

At low frequencies, the inductive terms are neglected and z_{ij} are worked out where the resistive parasitics are already known [131]. The z

parameters are converted to y parameters by the well known formulae and the elements in the intrinsic circuit are calculated from (4.1)-(4.4). At high frequencies any differences between the modelled z parameters and the measured Z parameters are assumed to result from the absence of the inductances.

$$IM[Z_{11}] - IM[z_{11mod}] = \Delta Z_{11} = \omega (L_g + L_s) \quad (4.9)$$

$$IM[Z_{12}] - IM[z_{12mod}] = \Delta Z_{12} = \omega L_s \quad (4.10)$$

$$IM[Z_{21}] - IM[z_{21mod}] = \Delta Z_{21} = \omega L_s \quad (4.11)$$

$$IM[Z_{22}] - IM[z_{22mod}] = \Delta Z_{22} = \omega (L_d + L_s) \quad (4.12)$$

The advantage of this method is that the inductances are evaluated at the same bias point at which the measurements are made, removing inconsistencies arising from bias variation.

4.5 Parameter Extraction over Multiple Bias Points

4.5.1 Introduction

A large-signal model was proposed in Chapter Two where the model elements were to be found from equivalent circuits for the MESFET over a range of bias points. The elements in the equivalent circuit which varied with bias were known as nonlinear or intrinsic elements: those which did not vary with bias were linear or extrinsic elements. When equivalent circuits were derived from S-parameter measurements at different bias points using the methods proposed in Section 4.4, some of the extrinsic elements were found to vary with bias, although the physical definition of these elements suggests that they should not do so.

Therefore, a method had to be adopted, whereby the linear

elements would remain constant in the equivalent circuits at every bias point. A commercially available small-signal simulator TOUCHSTONE was used to derive equivalent circuits from S-parameter measurements at all bias points. Since high frequency measurements were made, frequency dispersion effects in the output conductance and transconductances were taken into account, not possible with standard DC characterization. The multitude of bias points characterizing a device provided so much information that the problem of multiple model solutions was greatly reduced. Since the commercially available small-signal simulators were not designed to be run in batch mode and the evaluation of an equivalent circuit at one bias point took around half an hour, extraction at over 100 bias points was very time consuming.

Some software is now capable of performing parameter extraction at a number of bias points [142, 143]. SOPTIM, developed at the University of Canterbury, has been written specifically to do this and another advantage of using the software is that the equivalent circuits are extracted at all bias points *simultaneously* [144]. More recently, FETMEX [145] has been developed, which can extract linear models, fit DC characteristics to models and perform non-linear RF simulation.

For this project, the equivalent circuits were extracted manually because unconstrained optimization of the small-signal models was required at over 100 bias points and the above software is not presently able to do this. The equivalent circuits were extracted for a number of different MESFETs at different bias points using TOUCHSTONE and SUPERCOMPACT. Details of extraction methods are given in the following sections.

4.5.2 Parameter Extraction

An illustration of the small-signal model used for parameter extraction is given in Figure 4.8, containing a total of 15 elements. Parameter extraction was done using the small-signal simulator TOUCHSTONE and the basic methods of extraction are covered in Section 4.3.

The first approximation for the element values determined the extent of optimization which would be required to converge on the best result. To reduce reliance on the optimizer, the resistances R_s, R_d and R_g were estimated using the Fukui method. The transconductance was estimated from DC I-V curves and the remaining elements in the model were attributed with the starting values stated in the Plessey design manual.

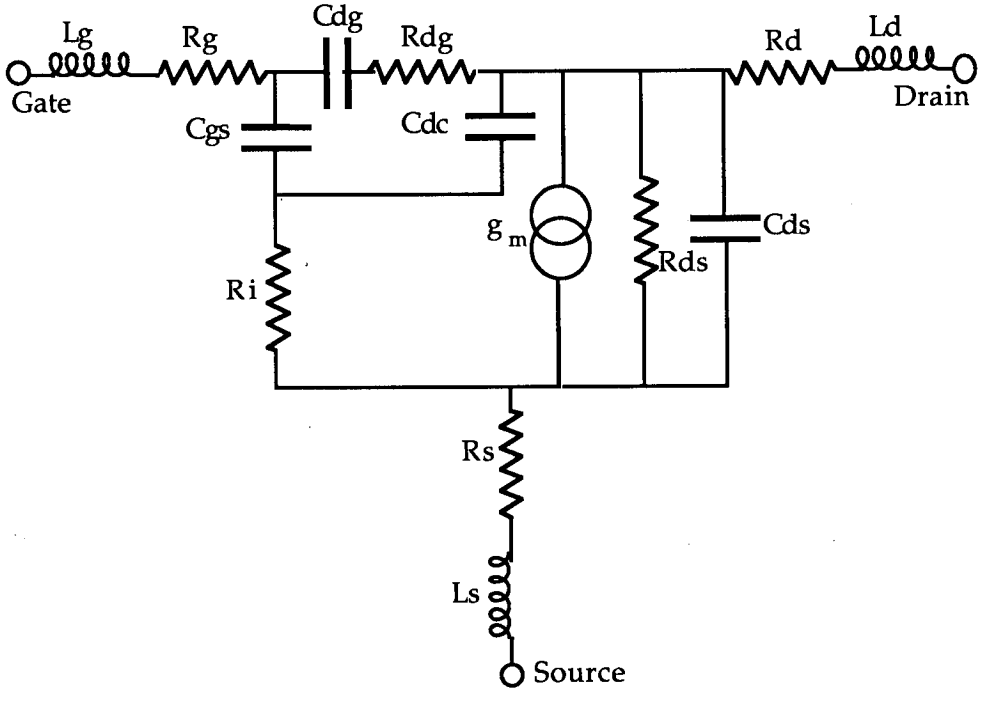


Figure 4.8: Small-signal model used for parameter extraction

Prior to extraction of all of the S-parameter measurements, sample fits were made at a number of different bias points. Models were derived at V_{gs}=-0.7 V from V_{ds}=0 to 11.5 V, V_{ds}=8.5 V from V_{gs}=0 to -2.0 V and V_{ds}=4.5 V from V_{gs}=0 to -2.0 V. The results revealed how individual elements were inclined to change over a wide range of 27 bias points.

Table 4.1 lists the 15 elements in the model for the test extraction at V_{gs}=-0.7 V for V_{ds}=0-11.5 V on a Plessey wafer-probed F20 300 micron gate width MESFET. For the three sets of sample measurements (wafer-probed F20, TRL calibrated F20 and F1) at all of the bias points, the error coefficient for the fits were small and the wafer-probed measurements demonstrated the best overall fits for all bias points. The error was reduced with 200 random optimizations followed by 10 gradient optimizations.

Vgs	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7
Vds	0.0	0.3	0.6	1.0	1.5	2.2
ERROR	0.008	0.20	0.18	0.504	0.038	0.034
Rds	22.0	28.91	60.0	268.87	277.2	297.4
Gm	0.0014	0.11	0.024	0.025	0.027	0.027
Cdg	0.126	0.125	0.104	0.072	0.056	0.051
Cgs	0.26	0.248	0.244	0.236	0.254	0.265
Ri	4.50	4.46	4.26	4.67	4.96	5.40
Rdg	7.41	7.34	7.71	7.25	6.945	6.43
Cdc	0.014	0.011	0.001	0.001	0.001	0.0012
Rg	5.40	6.24	7.80	8.77	8.68	7.91
Rd	0.51	0.59	0.501	1.055	1.02	1.11
Rs	0.58	0.77	0.50	0.50	0.50	0.50
Lg	0.01	0.01	0.01	0.01	0.01	0.01
Ld	0.01	0.01	0.016	0.013	0.012	0.011
Ls	0.013	0.013	0.011	0.011	0.012	0.011
Cds	0.014	0.011	0.001	0.001	0.001	0.001
tau	2.89	2.87	3.08	0.495	0.253	0.82

Vgs	-0.7	-0.7	-0.7	-0.7	-0.7	-0.7
Vds	3.0	4.5	6.0	8.5	9.9	11.5
ERROR	0.022	0.021	0.02	0.019	0.02	0.029
Rds	315.9	319.6	307.0	318.4	312.1	296.7
Gm	0.027	0.033	0.033	0.031	0.0291	0.027
Cdg	0.035	0.034	0.027	0.024	0.023	0.023
Cgs	0.028	0.338	0.358	0.374	0.3666	0.372
Ri	5.48	4.81	4.74	5.059	5.08	5.558
Rdg	6.03	5.67	5.91	3.259	3.18	3.347
Cdc	0.002	0.002	0.0036	0.004	0.004	0.0037
Rg	8.07	5.56	5.71	5.678	6.20	6.99
Rd	1.21	1.22	1.29	1.296	1.238	1.202
Rs	1.49	2.67	2.48	2.136	1.088	1.044
Lg	0.01	0.01	0.01	0.01	0.01	0.01
Ld	0.01	0.01	0.01	0.01	0.01	0.01
Ls	0.01	0.01	0.01	0.01	0.01	0.01
Cds	0.0226	0.021	0.027	0.027	0.022	0.0145
tau	1.90	2.00	2.92	3.19	3.82	4.43

Table 4.1 Test extraction at V_{gs}=-0.7V and V_{gs}=0-11.5V

4.5.3 Sensitivity Analysis Reveals Non-linear Elements

A sensitivity test was performed on all of the elements in the model at one of the sample bias points (V_{ds}=5.0V and $I_{dss}/2$). This was done to establish how critical the value of each element was, to the quality of fit between the model and the measurements. Each element was varied by a maximum of +/- 10% around the optimized value and any changes in the error term were noted. The normalized sensitivity S of model element X to the error term E is given [146] by:

$$S = (\Delta E/E) / (\Delta X/X)$$

S was calculated for all of the model parameters and the results are given below. The highest ranking element is g_m which indicates that the accuracy of the fit is most sensitive to a change in the value of the transconductance:

Element	S	Rank	Element	S	Rank
Lg	1.210	10	Cds	3.630	7
Ld	1.270	9	Rds	10.450	4
Ls	0.064	15	Ri	4.012	6
Rg	0.764	11	Cdg	15.670	3
Rd	0.382	12	Cgs	82.040	2
Rs	3.057	8	gm	184.470	1
Rdg	0.064	14	τ	6.561	5
Cdc	0.255	13			

The error term was very sensitive to changes in R_{ds}, g_m, C_{gs} and to a lesser extent C_{dg} and quite sensitive to R_i and τ. For the sample bias points, those 6 elements also varied systematically with bias and were therefore considered as bias-dependent. This conclusion is in accordance with the finding of other recent work [46,49,75] and the nonlinear elements will be discussed later in this chapter.

4.5.4 Finding the Values of Linear Elements

The error term was not found to be sensitive to the remaining 9 elements in the model. The parasitic inductances were all about 0.01nH and they did not vary strongly with bias. The parasitic resistances also showed an independence of bias: the maximum variation was for R_s which showed a tendency to vary up to 50% with bias but the pattern of change was erratic. The capacitances C_{ds} and C_{dc} were both small compared with other element values and did not vary either greatly or systematically with bias. The same result was found for R_{dg} which varied by a maximum of 12% over the whole bias range.

The linear elements were recalculated by averaging each element over all of the sample points. They were defined in the small-signal simulator as being constant with respect to bias. The averaging excluded 'wild' points at one or two bias points. These resulted from equivalent circuits which had converged on local minima or non-unique solutions and this will be discussed in the next section. The model was then re-optimized and the 6 non-linear elements were recalculated for all of the bias points.

4.5.5 Local Minima

The concept of local minima was discussed in Section 4.3.4. With so many parameters in the model, there were many optimization minima. Sometimes they were easy to locate since the error functions were large and the element values in an equivalent circuit at one bias point varied greatly from neighbouring equivalent circuits. These results accounted for the 'wild' points found during the extraction of sample measurements. The extraction was remedied by modifying and reoptimizing circuits which represented unrealistic solutions, like for example, a circuit where

the gate resistance was 50Ω.

In a number of cases, there was more than one true minimum and a number of different equivalent circuits fitted the measurements to the same degree of accuracy and the circuit solution was said to be non-unique. With measurements at only one bias point, it would have been impossible to chose the best solution to model the physical nature of the MESFET. About 90% of the multi-bias point measurements produced unique equivalent circuits. The 10% of bias points with non-unique solutions could be solved by choosing the solutions which best fitted the neighbouring bias point circuits.

4.5.6 Relation of Circuit Elements to S-parameters

The problems of uniqueness and local minima exacerbated the task of solving the equivalent circuits. Rather than rely completely on the optimizer to yield a final solution, it was often quicker and more accurate to search for the correct result manually. Changing the value of each model element manually revealed the relationship between that element and each of the S-parameters.

A clear example of this, is the relationship between the magnitude of S_{21} and g_m. If the model does not predict the magnitude of S_{21} correctly, then changing the value of g_m will improve the fit for S_{21}. The relationship between individual elements and S-parameters is given below, where the elements with less effect are shown in italics:

Elements	S-parameter
S_{11}	C_{gs}, R_i, *R_g* ,*L_g*
S_{21}	g_m, C_{gs}, *R_{ds}* ,*τ*
S_{12}	C_{dg},*L_s*
S_{22}	R_{ds}, C_{ds}, *R_d* ,*L_d*

It is interesting to note that a slightly better fit could be obtained, especially in S_{22}, if R_d was allowed to become negative for some bias points, most noticeably for bias points in which I_{ds} was large. This negative resistance has been thought to represent the Gunn domain effect which can occur in the MESFET under certain conditions. However the drain resistance was constrained to be constant with bias since this did not affect the quality of the fit by much. Allowing the extrinsic elements to become functions of bias would make the nonlinear model much more complicated.

Some elements, such as the inductances, affect the model mainly at higher frequencies and so higher frequency S-parameters were used when choosing values for the parasitic inductances in the equivalent circuit.

4.6 Bias Dependence of Nonlinear Elements

4.6.1 Defining Non-linear Behaviour

Parameter extraction of the S-parameter measurements over a rectangular grid of bias points was completed. Five of the elements in the equivalent circuit varied as functions of the gate and drain biases, whilst the remaining terms were bias independent (or linear).

The values of the linear elements were found by parameter extracting a sample of S-parameter measurements over a range of bias points. Subsequently, all bias point measurements were extracted, where all of the equivalent circuits were defined with linear elements of the same value. The nonlinear elements were unconstrained during the optimization and were allowed to change in any way which would reduce the error term.

It has been suggested [147] that at the parameter extraction stage, a nonlinear element should be constrained to change with the bias voltages

in a way which can be represented by a predefined analytical function. In this way, the degrees of freedom for individual parameter values are reduced and it was found that this improved the reliability of the solutions, i.e. the constraints did not produce 'wild' solutions where the values of model elements were obviously non-physical. However, this approach was not adopted because by imposing an analytical expression on extracted values, would limit the accuracy of the fit, especially for nonlinear elements which were complicated functions of bias, like for example C_{dg}. This limitation would result from the inability of the expression to accurately predict the change in a nonlinear element with bias. In any case, one of the advantages of the proposed model is that no analytical expressions are needed to calculate a large signal model and, no knowledge of the process parameters or DC characteristics is needed to extract the equivalent circuits.

The following sections describe the bias dependence of the non-linear elements in order of their importance as nonlinear elements (g_m, C_{gs}, C_{gd}, R_{ds}, τ and R_i). The physical description of each element in the MESFET is discussed and it may be useful to refer back to Chapter One which describes the basic operation of the MESFET. Parameter extraction results are given for the wafer-probed F20 devices and comparisons are made with other published work. It should be noted that a relationship exists between the small-signal parameters of g_m and R_{ds} and this will be discussed in Chapter Five.

4.6.2 The Transconductance g_m

The transconductance in the equivalent circuit models one aspect of the channel current and is defined as the change in current with respect to the gate voltage.

$$g_m = \partial I_{ds}/\partial V_{gs} \,|_{V_{ds}}$$

In the simplified small-signal equivalent circuit shown in Figure 4.9, the current source I_{ch} is defined as the product of g_{mo} and the controlling voltage V_{gs} (across the capacitor C_{gs}). In the actual MESFET, the current comprises two components: the channel current I_{ch} and the substrate current I_{subs} [82] where $I_{ds} = I_{ch} + I_{subs}$ (see Figure 4.10). As I_{subs} is dependent on the drain voltage, so is the total nonlinear current I_{ds}.

In the *small-signal* model, g_m does not indicate how the current varies with the drain voltage: this is done with the element R_{ds}. It was shown above that the total current I_{ds} varies with both the gate and drain voltages and therefore the value of g_m is dependent on V_{ds}. In conclusion, g_m in the small-signal model defines the current as a function of the gate voltage only, but over a range of bias points it is itself a function of *both* V_{gs} and V_{ds}. The full relationship between g_m, R_{ds} and the current I_{ds} will be dealt with in Chapter Five.

The transconductance changes with frequency. At DC, g_m is determined from the spacing between the DC I_{ds}/V_{ds} characterization curves at different gate voltages, where g_m is proportional to the distance between curves. The value of g_m changes at high frequencies compared to its value at DC because it exhibits frequency dispersion. Usually the ratio of AC to DC transconductance varies from unity by only a few percent and so g_m is often assumed to be independent of frequency. The dispersion has been shown [29, 148] to result from charge exchange with surface states and affects AC characteristics at around 10kHz.

Plots for the transconductance of a wafer-probed F20 device over a range of bias points are given in Figure 4.11. The transconductance decreases with increasing negative voltage V_{gs}. A negative gate voltage reduces the area of channel through which electrons may pass, the

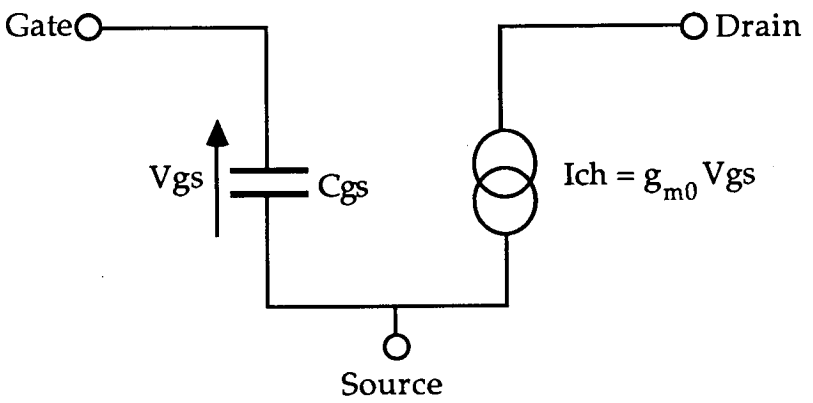


Figure 4.9: Simplified equivalent circuit

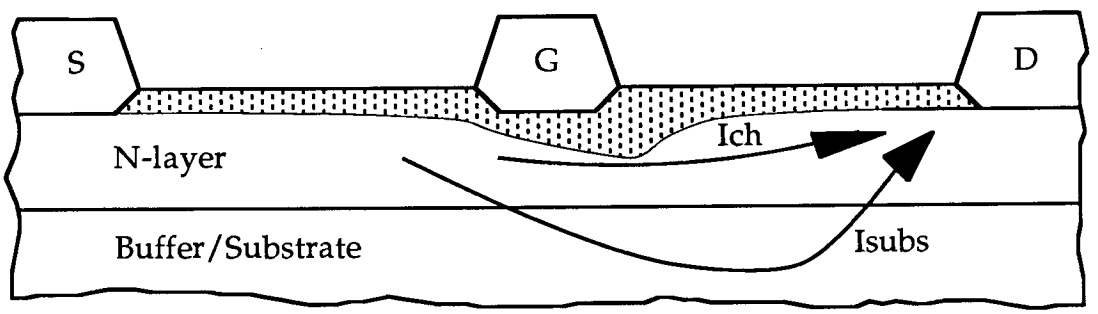
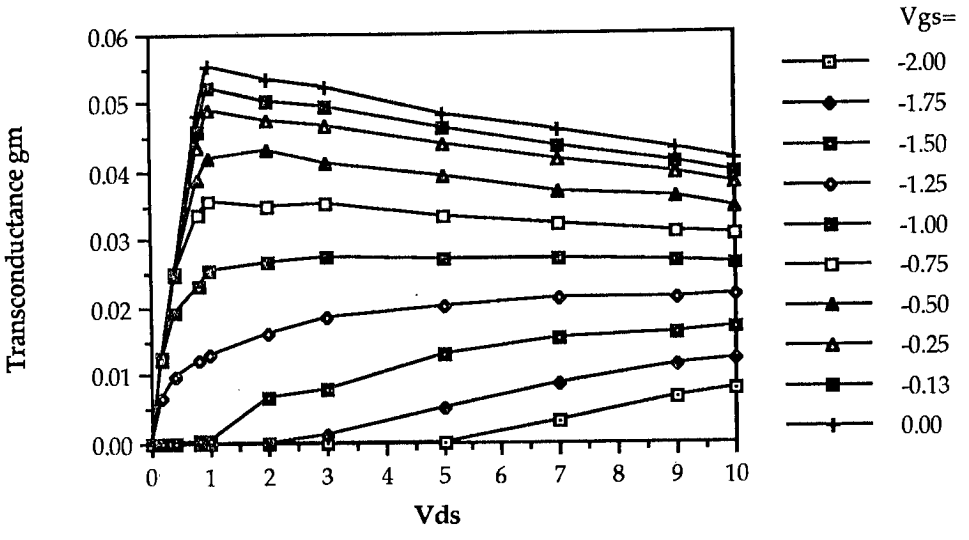


Figure 4.10: The channel and substrate currents



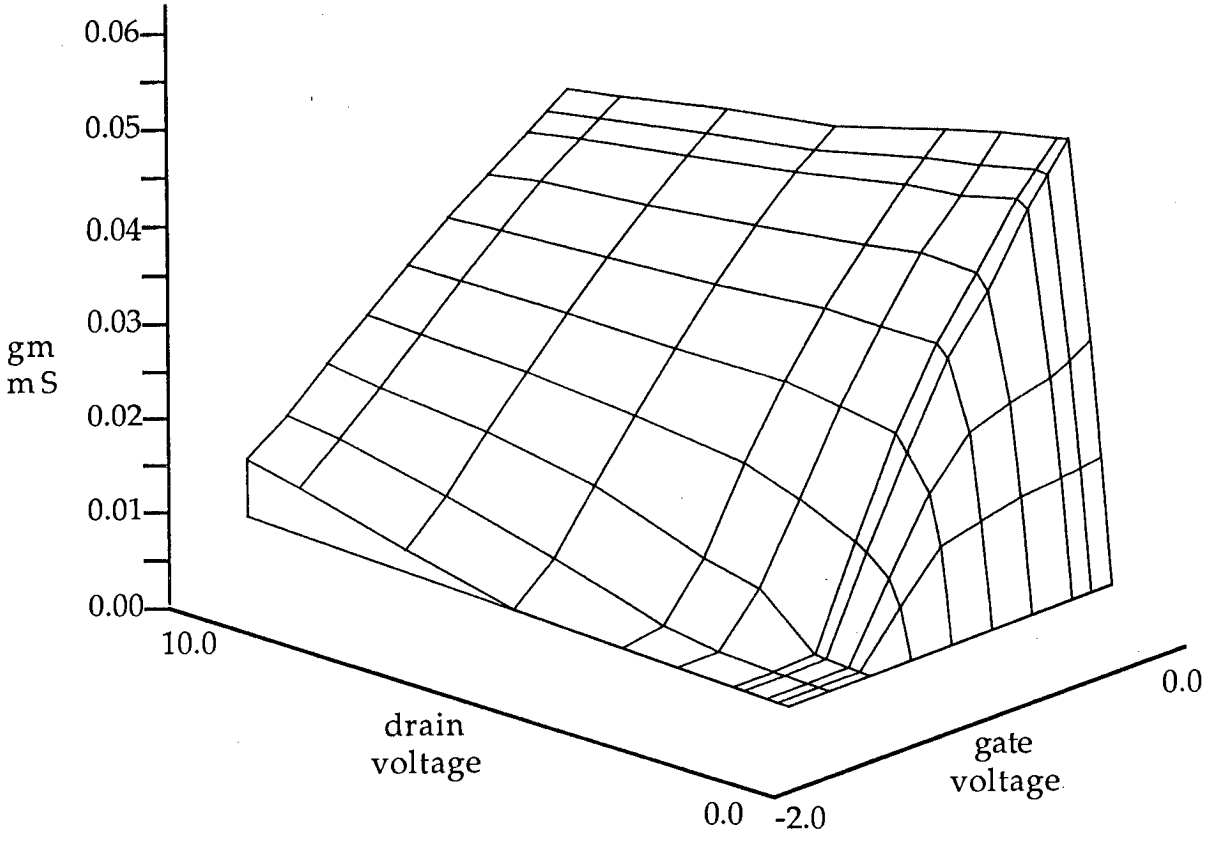


Figure 4.11: DC characteristics of the MESFET

transconductance falls and at pinchoff it is 0.0 mS. As the drain voltage increases, so does the substrate current and this increases the value of g_m.

When the channel is quite open and V_{ds} is high, increasing V_{ds} reduces g_m. Although this effect is not fully understood, it is thought to result from the complex interactions of the space-charge layer and the interface-state charge [82, 96]. The results of the parameter extraction for g_m are very similar to those found by Willing *et al* and others [45, 64].

4.6.3 The Capacitances C_{gs} and C_{dg}

The capacitances C_{gs} and C_{dg} are important in defining the nonlinear behaviour of the MESFET. The sensitivity analysis found them to be the second and third most important elements for accurately describing the model. More effort has been made in the proposed nonlinear model to describe the charge effects in the gate region than can be specified in many existing commercial nonlinear simulators. In many of these, the capacitances are represented as back-biased Schottky barriers, as discussed in Chapter Two.

Both capacitances result from the effects of charge storage under the gate region in the channel. As the depth of the depletion region in the channel is a function of gate and drain voltages, so the capacitances vary with both voltages. The capacitance in the gate is distributed but, for modelling purposes it is considered lumped into C_{gs} and C_{dg}. The ratio of one capacitance to the other is not well defined and the lumped capacitances are non-physical.

When describing the charge storage capacitance, it is useful to assume the channel region as the equivalent circuit in Figure 4.12 [82]. First of all, it is interesting to note how the depletion region changes for an

increase in the gate and drain voltages. For an increasing positive gate voltage, the height of the depletion region is reduced, whereas the length is increased. The length is also increased with an increase in V_{ds} and this does not affect the depletion height.

The distributed capacitor and resistor network ΔC_I and ΔR in the resistive region I can be approximated to a lumped series RC_I pair where the charge in C_I changes with V_{gs} and $R = R_i$. The capacitance in regions II and III, distributed across the current generator $\Delta g_m V_{gs}$, can be re-expressed as a parallel $g_m V_{gs}/C_{II\text{-}III}$ pair where the charge in $C_{II\text{-}III}$ also changes with V_{gs}.

The depletion region extends as the voltage is increased, because the increased current induces more electrons to leave their sites in the space-charge layer. This increases the positive charge, which can be represented by a capacitance C_{dg}. The gate-drain capacitance C_{dg} is defined as:

$$C_{dg} \approx \partial Q/\partial V_{dg}$$

The equivalent circuit for the channel area is given in Figure 4.13 where C_I and $C_{II\text{-}III}$ have combined to form C_{gs}, which is placed in parallel with $g_m V_{gs}$.

Plots for the gate capacitance of a wafer-probed F20 device over a range of bias points are given in Figure 4.14. Increases in V_{ds} produce a monotonic increase in C_{gs}, attributed to charge accumulation effects in the channel as a result of the increased depletion length. Increasing $|V_{gs}|$ causes the value of C_{gs} to rise as the negative voltage increase causes charge accumulation across the depletion region capacitance. The results of the extraction compare favourably with results from other work [44, 45, 82, 96] where the initially decreasing values of C_{gs} with increasing V_{ds} is also reported.

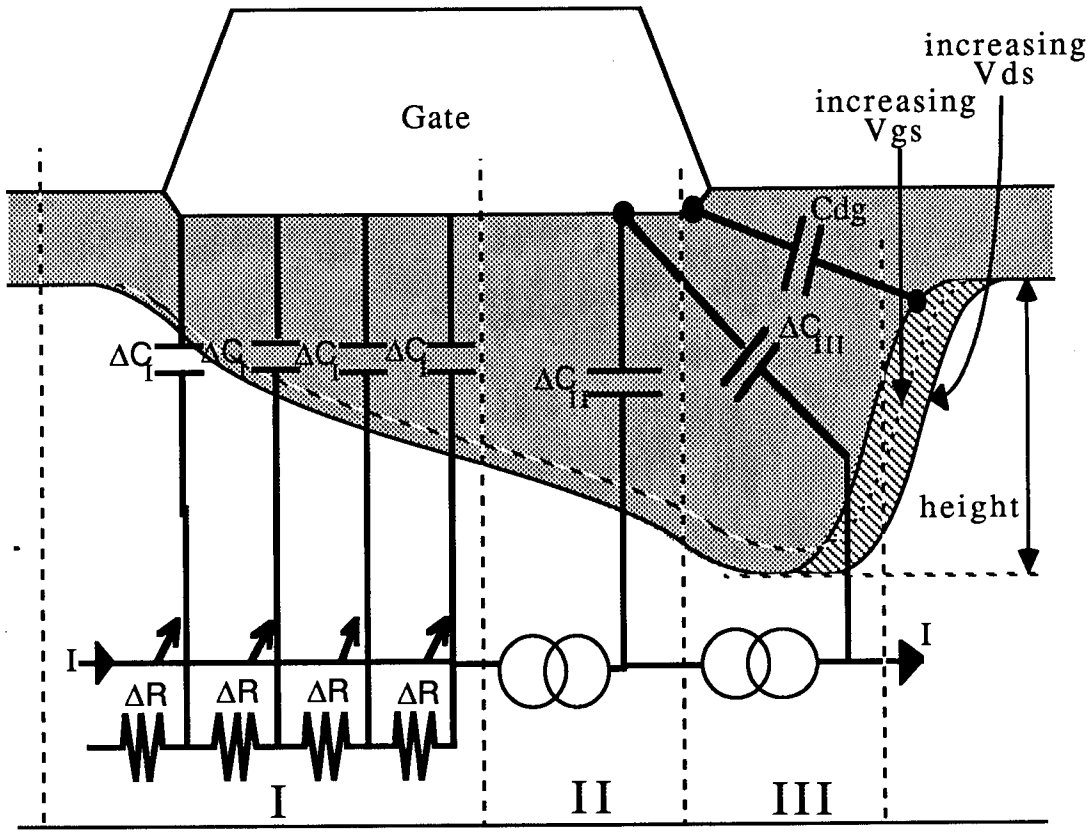


Figure 4.12: Distributed capacitances in the channel region

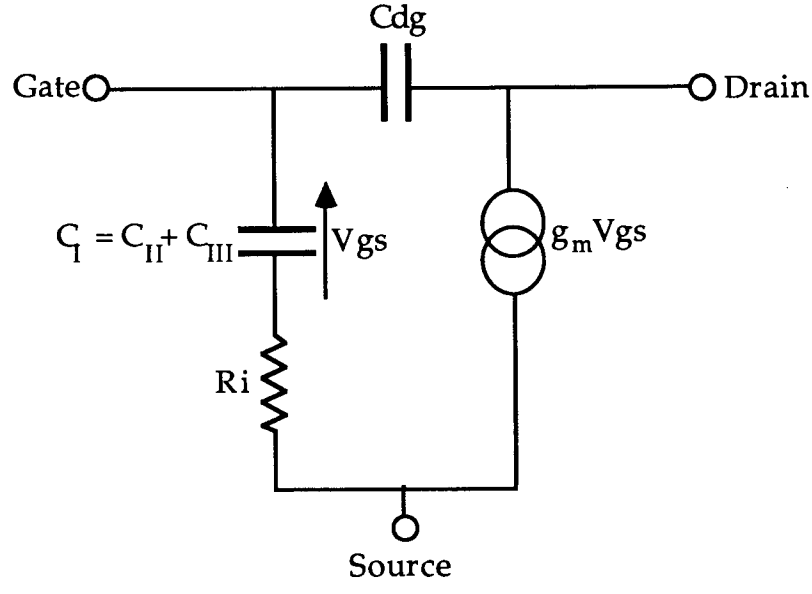
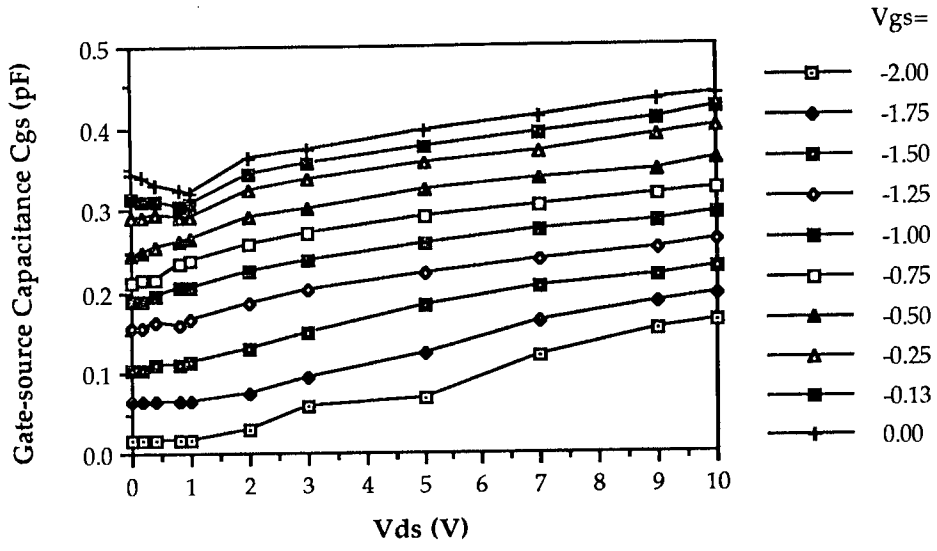


Figure 4.13: Equivalent circuit for channel area



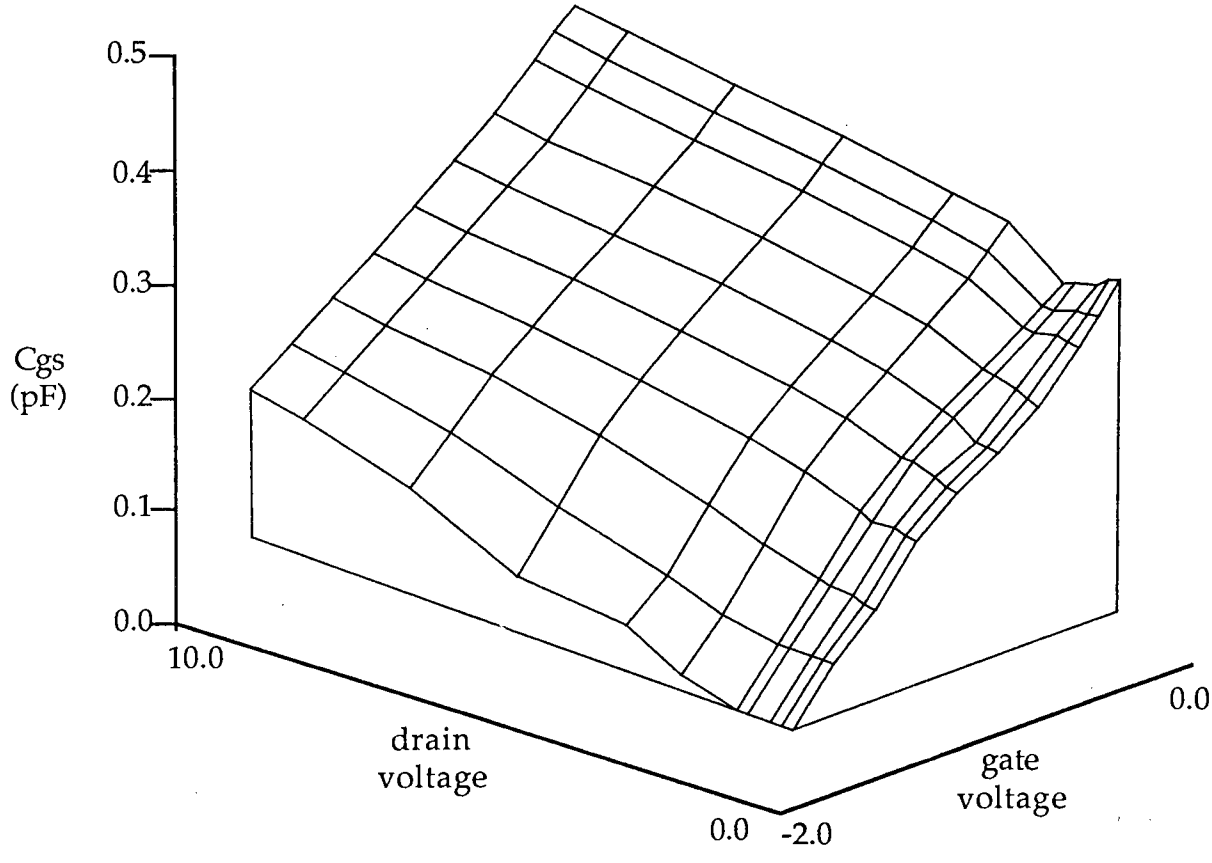


Figure 4.14: Gate capacitance

The curve families for C_{dg} are plotted in Figure 4.15 where the curves for different gate voltages are seen to cross near to V_{sat}. C_{dg} decreases steeply as V_{ds} approaches the saturation point and this effect reduces as $|V_{gs}|$ increases. C_{dg} decreases less steeply beyond the saturation point where the effect of the gate voltage is reversed and C_{dg} increases with $|V_{gs}|$. These results are similar to those found by Willing *et al* [45] and others [77,149] where the crossing of the capacitance curves is also observed.

4.6.4 The Output Resistance R_{ds}

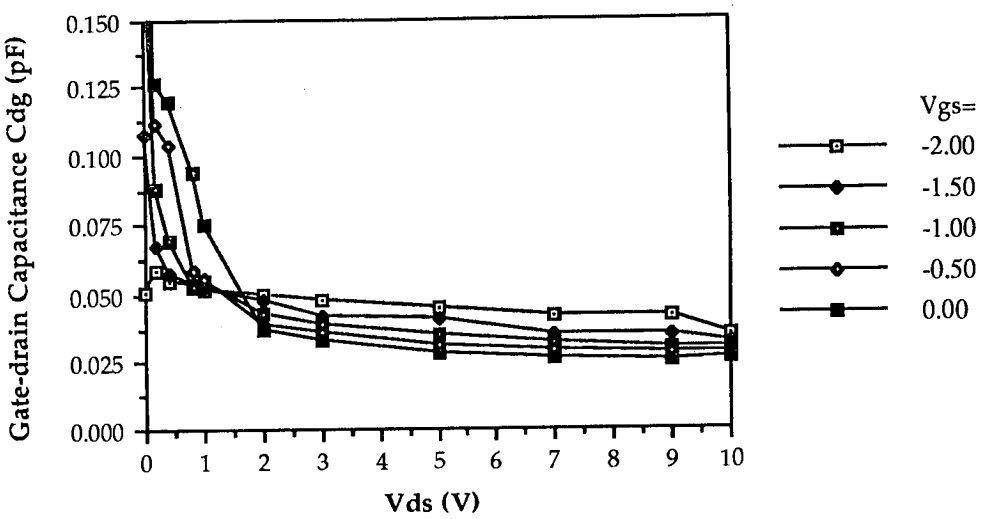
In the small-signal model, the output resistance reflects the change in the channel current with respect to the drain voltage. The output conductance ($g_0=1/R_{ds}$) is defined as:

$$g_0 = \partial I_{ds}/\partial V_{ds} \,|_{V_{gs}}$$

Note the similarity of the expressions for the transconductance and output conductance and that they combine to form the nonlinear current characteristics of the MESFET. The way in which the current is derived from these two parameters is described in Chapter Five.

For the DC characteristics of the MESFET, the greatest change in the current with respect to V_{ds} occurs in the linear region, where values for V_{ds} range from 0.0 to 1.5 V. This is reflected in values of R_{ds} which are very low for small values of V_{ds} and rising rapidly through the linear region. Beyond saturation, R_{ds} rises slowly, indicating only a small increase in the current with increasing drain voltage. The output resistance also varies with the gate voltage and increased with $|V_{gs}|$ rising to thousands of ohms at pinchoff.

The extracted values for R_{ds} differed substantially from those predicted from the DC I/V characteristics, as the output conductance is



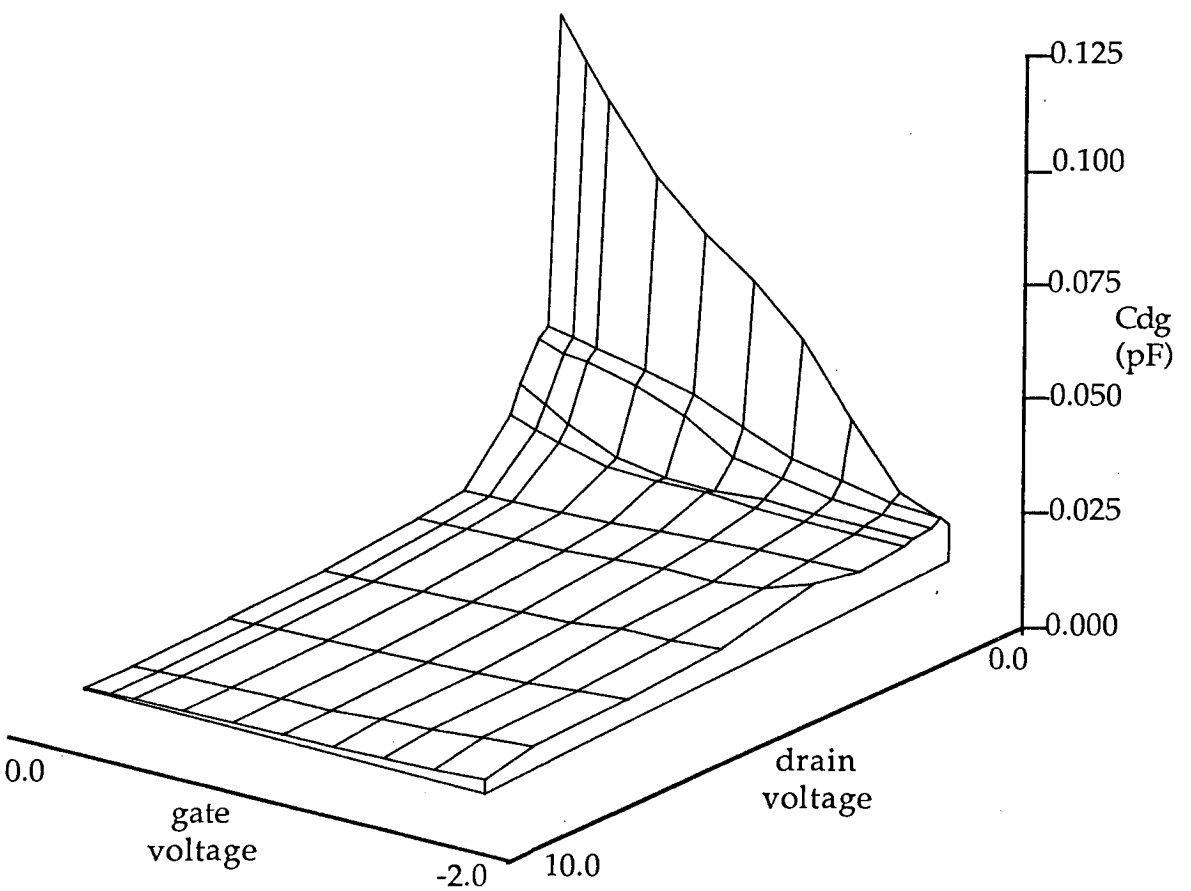


Figure 4.15: Gate-drain capacitance

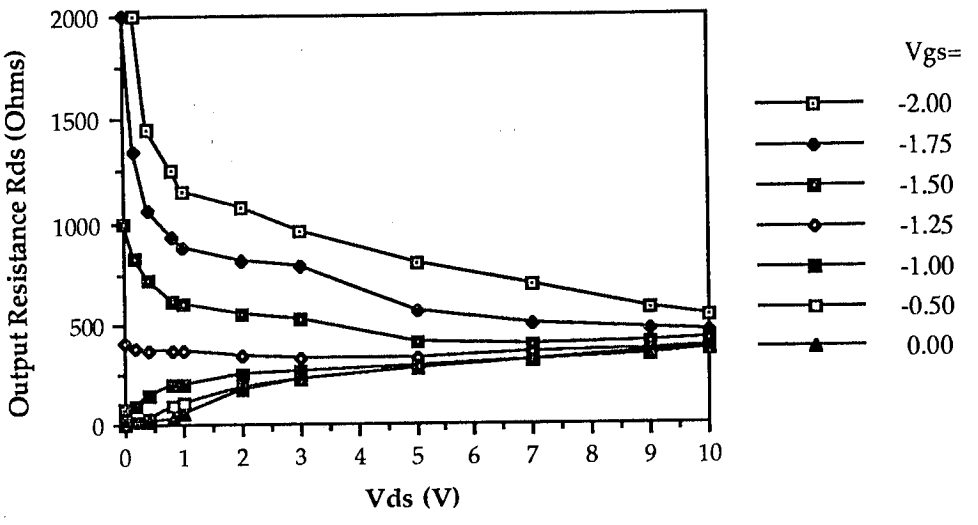
subject to large changes in value between low and high frequency, due to frequency dispersion. The principal cause of frequency dispersion has been reported as the change with frequency of the substrate current with drain voltage and this is due to the presence of traps in the semiconductor lattice. This observation has been made elsewhere [26, 27, 28, 82] and a more detailed account of the relationship between I_{ds}, g_m and R_{ds} will be given in Chapter Five. Plots for the output resistance of a wafer-probed F20 device over a range of bias points are given in Figure 4.16 and agree with other findings [45, 64, 82].

4.6.5 The Transconductance Delay τ

In the equivalent circuit, τ represents the signal delay. This is caused by the propagation delay across the width of the gate and the charging time in the depletion region under the gate.

An illustration of the delay plotted against drain voltage is given in Figure 4.17. τ is very small when V_{ds}=0.0 V and rises rapidly with drain voltage and beyond saturation, it rises less quickly. This can be explained by considering that electrons entering region II (see Figure 4.12) of the channel either form part of the current, or charge the capacitor $C_{II\text{-}III}$ in the depletion layer of region III. As the drain voltage increases, the depletion layer length in region III increases and the capacitor takes longer to charge.

In a similar way, an increase in the gate voltage reduces the depletion area of region I but increases the depletion area of region III, thus increasing the delay. The extracted delay was found to behave as above and is confirmed by other work [61, 82].



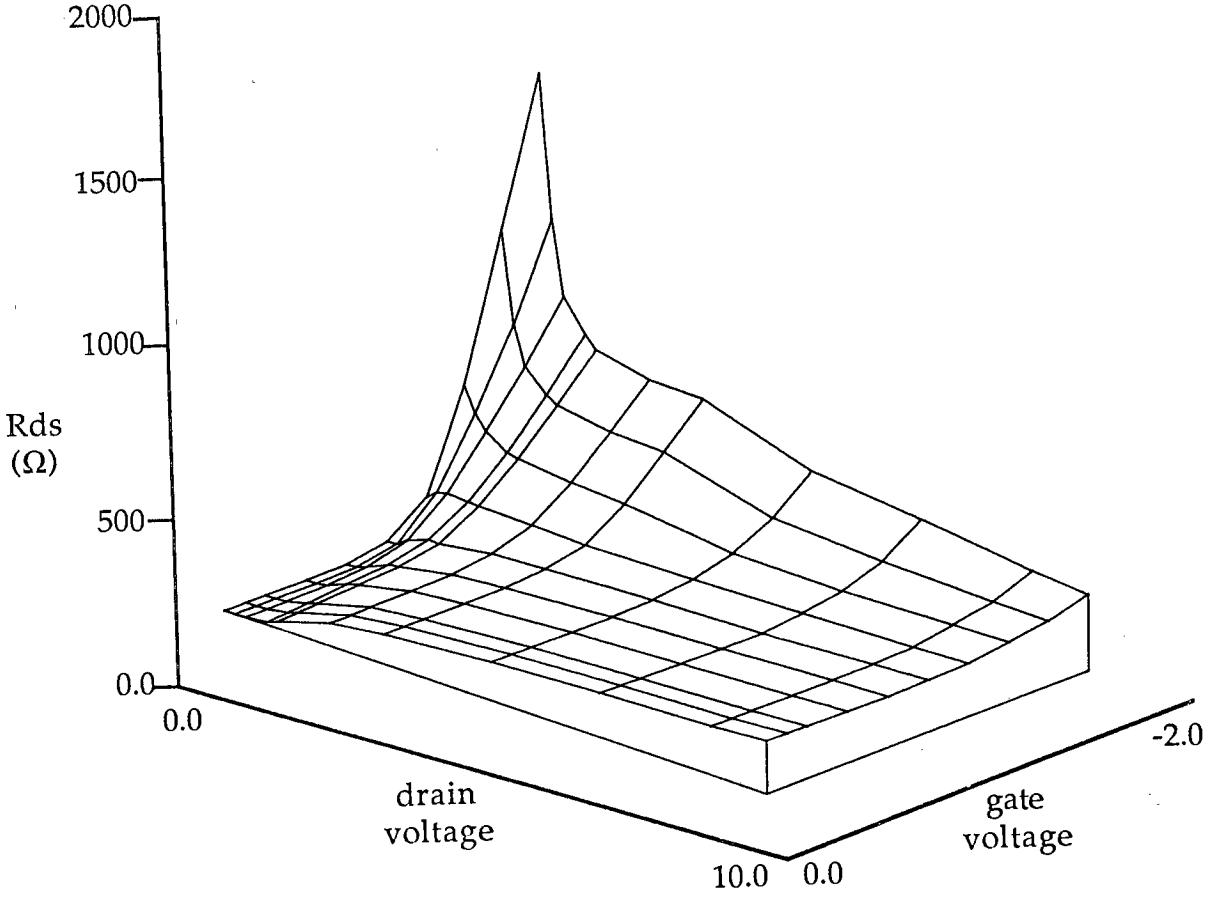


Figure 4.16: Output Resistance

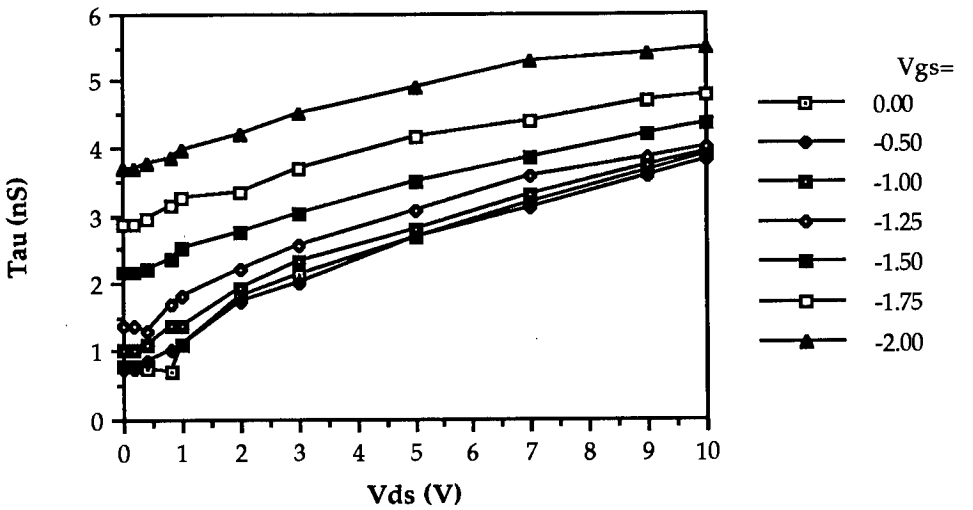


Figure 4.17: The time delay τ

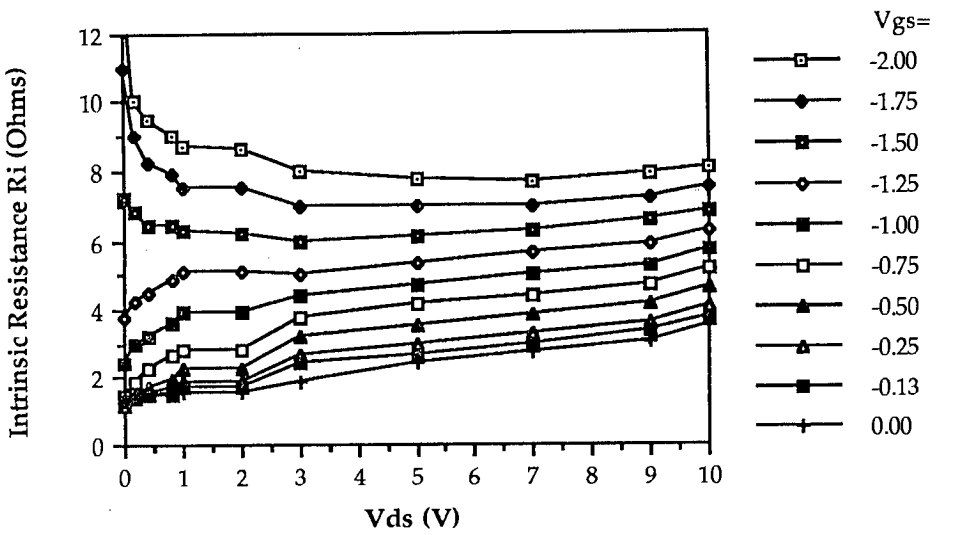
4.6.6 The Intrinsic Resistance R_i

The intrinsic resistance is a lumped approximation of the distributed resistance in the channel. It is the least important of all of the model elements to extract correctly as the error function is least sensitive to it. R_i is also the most difficult parameter to evaluate using parameter extraction because its weak relationship to the error produces many non-unique solutions for each bias point. It has been reported [150] that R_i is sensitive to measurement error and should only be evaluated when the magnitude of S_{11} approaches unity.

The variation of R_i with V_{gs} and V_{ds} is shown in Figure 4.18 which agrees with other published work [45, 64].

4.7 Conclusions

The methods used to extract the linear equivalent circuit at single and multiple bias points have been reviewed. It has been shown that the values of nonlinear elements can be found from sets of S-parameter data of the MESFET over a range of bias points. Because care has been taken to



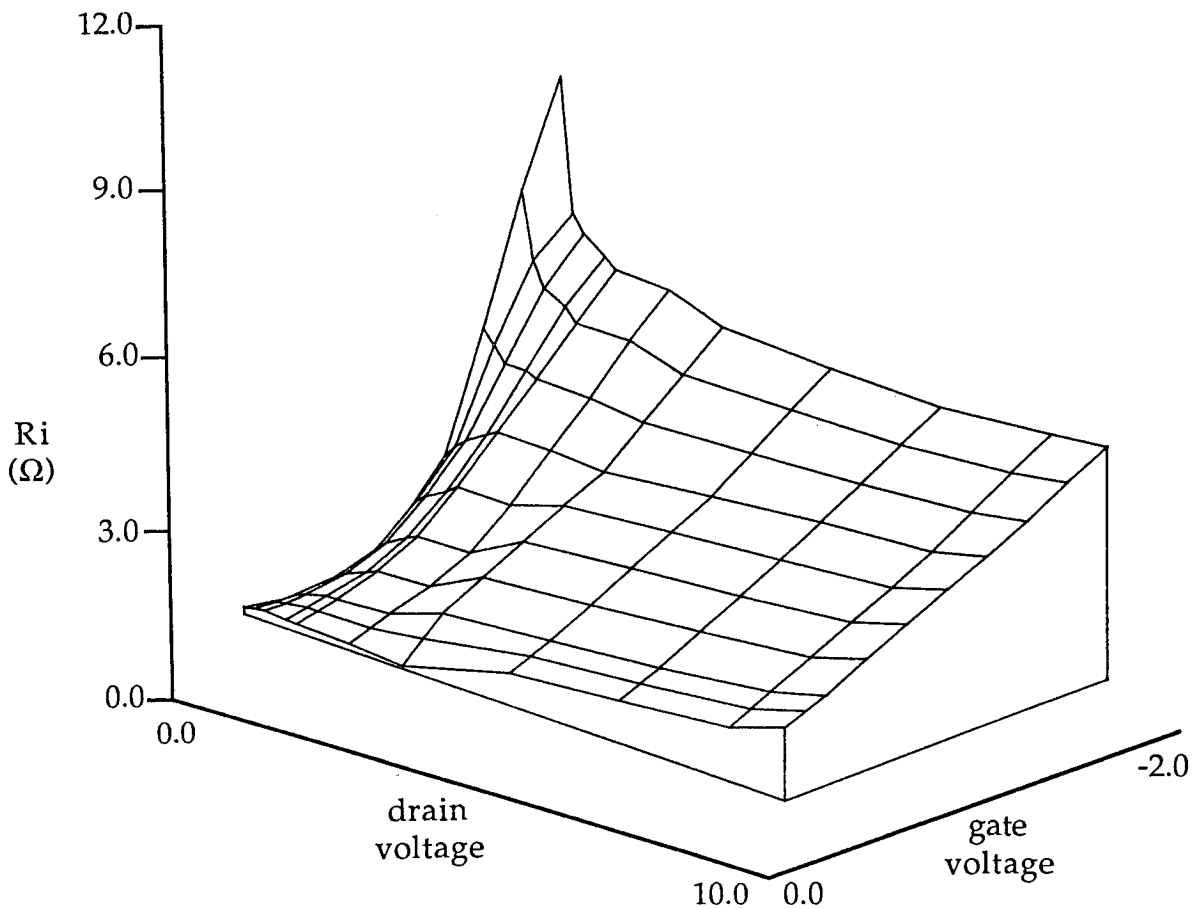


Figure 4.18: Intrinsic resistance

ensure that the equivalent circuit at each bias point represents the real physical behaviour of the device, the nonlinear elements can be seen to change coherently with bias, in a way that can be explained in terms of device physics. All that remains now is to include this extracted information in a nonlinear model, and this is the subject of the next chapter.

CHAPTER FIVE - Nonlinear GaAs MESFET Model

5.1 Introduction

This chapter describes the nonlinear model for the GaAs MESFET, which is based on the equivalent circuit information extracted from small-signal measurements. A method is proposed to derive the MESFET channel current from the small-signal transconductance and output conductance. This requires the inclusion of two extra non-linear model elements in the nonlinear model topology, and these elements are not used in many other models. It is shown that deriving the current solely from S-parameter measurements produces a nonlinear model capable of accurately predicting the small and large-signal characteristics of the MESFET as well as the effects of frequency dispersion.

Curve fitting techniques are described, since nonlinear elements are expressed in the model as two-dimensional polynomial expressions. Finally, details are given about the curve fitting methods used for each nonlinear element and how these elements are implemented in the ANAMIC nonlinear time domain simulator.

5.2 Converting External to Internal Voltages

In Chapter Four, a method was described for extracting nonlinear element values from the small-signal equivalent circuit over a range of bias points. All of the nonlinear elements were functions of both bias voltages, representing the bias applied to the external ports of the MESFET. The internal node voltages are the voltages across each of the circuit elements in the model and these are different from the external voltages.

For most of the elements in the large-signal model, it is more useful to represent the nonlinearities as functions of internal node voltages. For

example, the transconductance, defined as the change in current with gate voltage is controlled by the internal voltage across the gate-source capacitor, and not the external gate bias. Similarly, capacitance is defined as the change in charge with voltage where the voltage is applied across the capacitor and not across the external ports of the MESFET. The current/transconductance and charge/capacitance relationships will be discussed later in this chapter. For a nonlinear element, such as the intrinsic resistance, specifying the nonlinearity in terms of the internal node voltages makes the calculation of the nonlinear resistance arithmetically more efficient.

An illustration of a simplified FET channel and equivalent circuit is given in Figure 5.1. The inductances were neglected for the DC analysis. There is no voltage drop across the resistor R_g as the current through the gate capacitor C_{gs} is very small indeed. The current source I_{ds} was a function of the voltages $V_{gs'}$ and $V_{d's'}$ where $V_{d'}$ and $V_{s'}$ differed from V_d and V_s due to the voltage drops across resistors R_d and R_s respectively. Similarly C_{gs}, C_{dg} and R_i could be reexpressed as functions of $V_{gs'}$, $V_{d's'}$ and $V_{d'g}$.

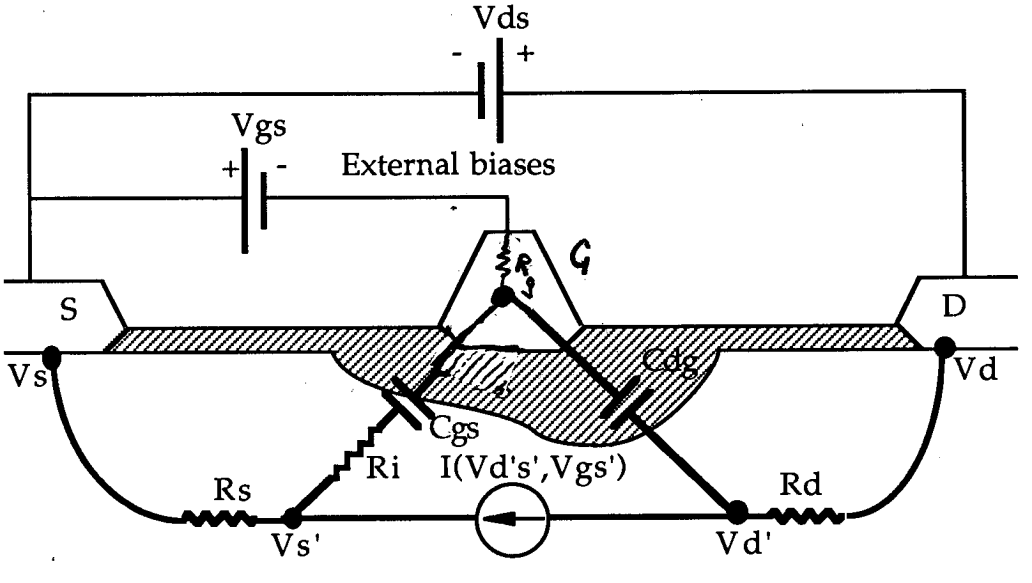


Figure 5.1: Simplified FET channel showing voltage drops across parasitics

The relationship between the internal and external voltages is given as:

$$V_{gs'} = V_{gs} + I_{ds}R_s \quad (5.1)$$

$$V_{d's'} = V_{ds} - I_{ds}(R_d + R_s) \quad (5.2)$$

$$V_{d'g} = V_{d's'} - V_{gs'} = V_{ds} - V_{gs} - I_{ds}R_d \quad (5.3)$$

For the wafer-probed F20 FETs, $R_s = 2.0\ \Omega$ and $R_d = 1.2\ \Omega$. At $V_{ds} = 1.0$ V, $V_{gs} = -0.5$ V and $V_{dg} = 1.5$ V the current was measured as 26.70 mA. $V_{gs'}$ was calculated as -0.55 V, $V_{d's'}$ was 0.91 V and $V_{d'g}$ was 1.46 V.

Once all of the external bias voltages had been converted, all of the nonlinear elements were re-expressed as functions of the internal node voltages. The external voltages in Figure 5.2 were defined over a rectangular grid of points, where the two axes represented the external gate and drain voltages. Expressing the elements as functions of the internal voltages moved each bias point off the grid to a different degree, depending on the voltage drop across each parasitic resistance. Note how the largest deviation from the grid occurred where the drain current was largest, at V_{ds}=10.0 V and V_{gs}=0.0 V. The curve fitting algorithms, described later in this chapter, required that the elements were expressed on a rectangular grid of bias points. Therefore the element values were extrapolated back to a rectangular grid, where the grid voltages had the same values as previously, but represented internal rather than external voltages. The values of the elements had changed slightly as they were now measured at effectively different bias points.

Figure 5.3 shows how the values for g_m altered as the grid of bias points were changed from external to internal voltages. The gradient was found between a point V_{gs1} and its nearest neighbour V_{gs2} and the value of $g_{m'1}$ at $V_{gs'1}$ was calculated as

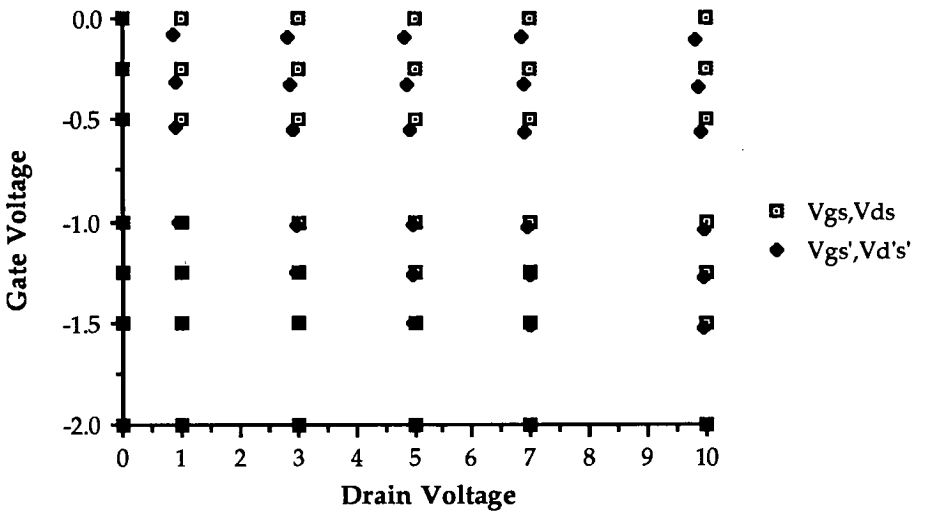


Figure 5.2: Relationship between external and internal voltages

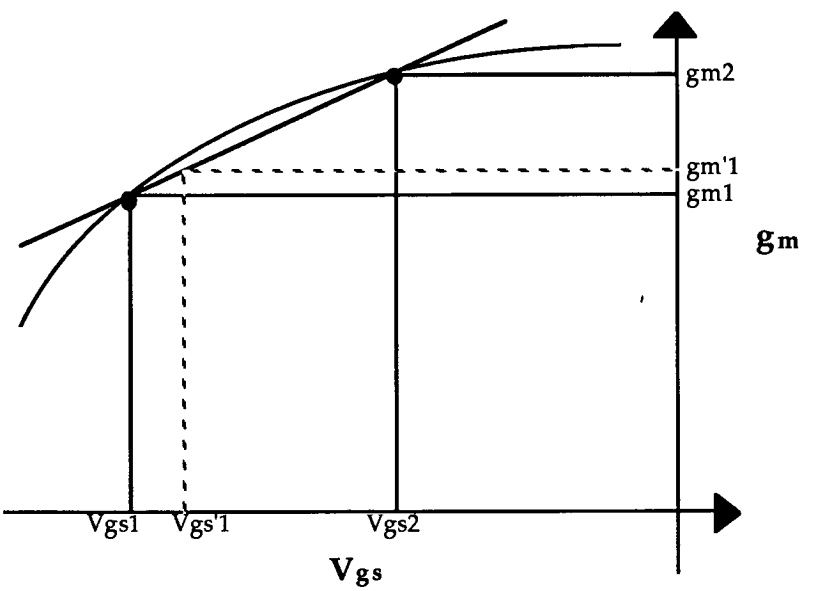


Figure 5.3: Re-expressing element values for internal voltages

$$g_{m'1} = g_{m1} + (V_{gs'1} - V_{gs1}) * (g_{m1} - g_{m2})/(V_{gs1} - V_{gs2}) \quad (5.4)$$

A similar method was used to recalculate the nonlinear elements for the internal drain voltages on the grid. For the remainder of this chapter, references to V_{gs}, V_{ds} and V_{dg} should be interpreted as the internal node voltages of $V_{gs'}$, $V_{d's'}$ and $V_{d'g}$ respectively.

5.3 The Nonlinear Current Source I_{ds}

5.3.1 Introduction

The current generator I_{ds} is the most important component of the large-signal model required to accurately predict the nonlinear behaviour of the MESFET. The DC I/V characteristics of the MESFET reveal the relationship between the channel current and bias voltages. Some nonlinear modelling methods use these DC measurements to predict the current characteristics of the MESFET at high frequencies, as described in Chapters Two and Four, although no account is taken of frequency dispersion in the transconductance and output conductance.

The small-signal MESFET models, over a range of bias points, are derived from high frequency S-parameter measurements and equivalent circuits are derived from these measurements using parameter extraction. The channel current cannot be determined directly from the equivalent circuits but from the elements of transconductance (g_m) and output conductance ($g_d=1/R_{ds}$), which denote the change in the current with gate and drain voltages respectively at that particular bias point. Under DC conditions, the two conductances are defined as

$$g_m = \partial I_{ds}/\partial V_{gs} \,|_{V_{ds}} \quad \text{and} \quad (5.5)$$

$$g_d = \partial I_{ds}/\partial V_{ds} \,|_{V_{gs}} \quad (5.6)$$

By the same token, the equations can be rearranged to express the current I_{ds}

as

$$I_{ds} = \int g_m \, \partial V_{gs} \, |_{V_{ds}} = \int g_d \, \partial V_{ds} \, |_{V_{gs}} \qquad (5.7)$$

The current can be found from a continuous equation for g_m, by integrating it for V_{gs}, with constant V_{ds}. Similarly, the current can also be found from an equation describing g_d and from (5.5)-(5.7) the two currents should be the same. Alternatively, the relationship between g_m and g_d could be verified by integrating g_m with respect to V_{gs} to find the current and differentiating the current with respect to V_{ds} to find the output conductance. Integration, which can be performed either analytically or numerically, of either the transconductance or the output conductance, introduces a 'constant of integration' term. This can be found by considering the known boundary conditions for the nonlinear current I_{ds}, such as I_{ds}=0.0 mA where V_{ds}=0.0 V.

However, for the F1 and F20 devices, the simple relationship between g_m and g_d did not exist and similar findings have been reported elsewhere [26,27,28]. Various reasons have been put forward to interpret this observation and among them are frequency dispersion effects in equivalent circuit elements, drain-lag [151] and hysteresis [152].

The remainder of this section discusses the effects of frequency dispersion, as well as methods used to derive the effective high frequency current/voltage relationships from small-signal measurements.

5.3.2 Frequency Dispersion of g_m and g_d

The model elements of g_m and g_d were found at high frequencies and over a range of bias points, by extracting small-signal models from sets of S-parameters. The current was derived from the sets of transconductances and from the output conductances and was found to be different in both cases, due to frequency dispersion of g_o and g_m.

Frequency dispersion in the transconductance has been observed [23,

24], especially in the bias region of low drain voltages, where the current-voltage relationship is ohmic. A reason for this has been proposed [25] which considers the relationship between g_{m0} and g_m, where g_{m0} is the 'intrinsic' transconductance and g_m is the 'internal' transconductance. This relationship is similar to the comparisons between internal and external node voltages, described earlier in this chapter. The transconductance is defined as

$$g_m = g_{m0} / (1 + g_{d0} (R_s + R_d) + g_{m0} R_s \qquad (5.8)$$

The dispersion in g_m is caused by variations in R_d and R_s with frequency, where R_d is more frequency dependent. This is caused by the change with frequency in the length of the space-charge layer into the gate-drain region [153]. The dispersion in g_m was proved to decrease with V_{gs} and increase with V_{ds} and also relate to the gate length. Figure 5.4 illustrates the change in g_m with frequency [29].

The output conductance is also subject to frequency dispersion. It has been suggested [154] that charge exchange with deep levels are responsible and these are situated at the device surface or in the N-layer to buffer-substrate region. At low frequencies, charge exchange with surface states accounts for a flat drain current response with increasing drain voltage. At higher frequencies, the states cannot follow the applied voltage quickly enough, the output conductance increases and the drain characteristics become steeper.

The result of this is that between DC and microwave frequencies, the output conductance decreases, typically by a factor of three and Figure 5.5 shows how R_{ds} varies with frequency [27].

5.3.3 Modelling the Output Conductance Nonlinearity

The problem of determining the current from small-signal transconductance and output conductance parameters has been widely

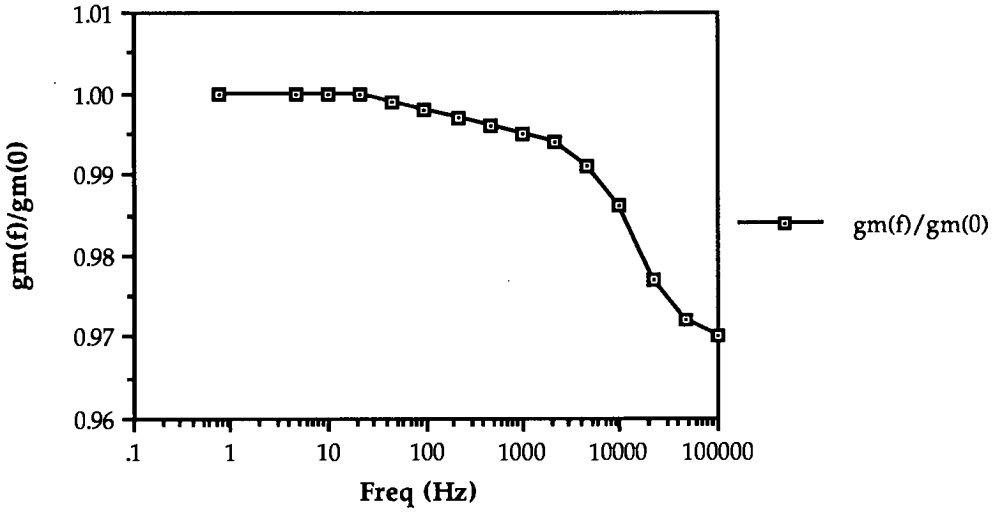


Figure 5.4: Frequency dispersion in the transconductance g_m

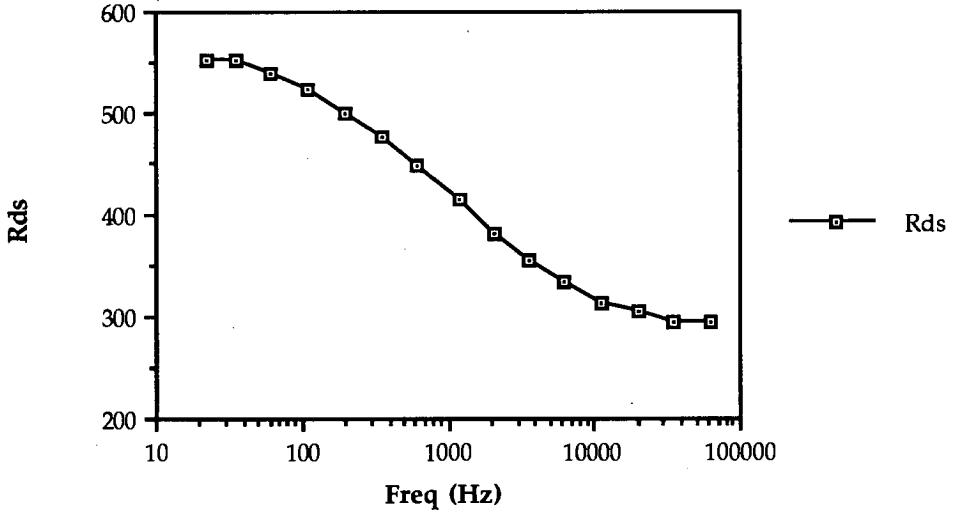


Figure 5.5: Frequency dispersion in the output conductance R_{ds}

reported [26-29] and a number of techniques have been proposed to overcome these difficulties. Camacho *et al* [27] proposed an extension to the basic equivalent circuit, based on an observed frequency dependence of the output conductance. The model included an extra RC pair in parallel with the current I_{ds}. The values of R and C were fitted to low frequency S-parameter measurements with the equation:

$$Z(f) \approx R_{ds}((1 + j\omega RC)/(1 + j\omega C(R + R_{ds})) \qquad (5.9)$$

The time constant for the RC pair related to the trapping time constant for GaAs structures.

Another solution was to restrict the variation of g_m and g_d to only one control voltage each. If g_m is only a function of V_{gs}, and g_d is only a function of V_{ds}, then the current is defined as:

$$I_{ds} = \int g_m \, \partial V_{gs} + \int g_d \, \partial V_{ds} \qquad (5.10)$$

$$\partial I_{ds}/\partial V_{gs} = g_m \quad \text{since} \quad \partial \left(\int g_d \, \partial V_{ds}\right)/\partial V_{gs} = 0 \quad \text{and} \qquad (5.11)$$

$$\partial I_{ds}/\partial V_{ds} = g_d \quad \text{since} \quad \partial \left(\int g_m \, \partial V_{gs}\right)/\partial V_{ds} = 0 \qquad (5.12)$$

However, as shown in this work, g_m and g_d were found to vary with both bias voltages. Attempting to describe the large-signal model in terms of a transconductance which did not vary with the drain voltage would have introduced an unacceptable approximation. The same conclusion could be drawn to similar approximations for the output conductance.

A compromise solution was proposed [28] which allowed one conductance to have bivariable dependence and the other to have single variable dependence. Since the model was most sensitive to a change in g_m, g_d was chosen for the single variable dependence. The expression for g_m was given as:

$$g_m = V_{ds}\,\partial g_d / \partial V_{gs} + F(V_{gs}) \qquad (5.13)$$

where $F(V_{gs})$ is a function of V_{gs} only. However, using this method approximated the output conductance to a function of V_{ds} only and ignored the frequency dispersion of g_d. With the data extracted from the F1 and F20 FETs, it was not possible to make either of these assumptions.

Scheinberg *et al* [26] proposed a new MESFET model consisting of four rather than three ports. The extra port was situated in the middle of the depletion region of the channel. The current equation was modified to include a controlling voltage from the extra port. The derived AC output conductance was found to vary with frequency in a similar manner to the output impedance of measured FETs.

A MESFET model has recently been proposed [155] which seeks to model the effects of frequency dispersion on both the output conductance and the transconductance. The output conductance correction includes the RC pair proposed by Camacho. The parameter Δg_d is defined as the difference between the values for the output conductance at high and low frequencies. The DC current is modified by the equation

$$I_{ds} = I_{ds(dc)}(V_{gs}, V_{ds}) + \Delta g_d(\underline{V}_{gs}, \underline{V}_{ds}).[V_{ds} - \underline{V}_{ds}] \qquad (5.14)$$

where $\underline{V}_{gs}$ and $\underline{V}_{ds}$ are the mean bias voltages, averaged over the appropriate time constant (V_{gs} and V_{ds} are the instantaneous bias voltages).

The current is also modified to account for frequency dispersion effects in the transconductance. Here, ΔR_s is defined as $1/g_{m(hf)} - 1/g_{m(dc)}$. ∂R_s is used to modify the gate and drain currents to become

$$I_g = I_{gdc}(V_{gs} - \Delta V_s, V_d - \Delta V_s)$$

$$I_{ds} = I_{ds(dc)}(V_{gs} - \Delta V_s, V_{ds} - \Delta V_s) + \Delta g_d(\underline{V}_{gs}, \underline{V}_{ds}).[V_{ds} - \underline{V}_{ds}]$$

where $$\Delta V_s = [I_g - \underline{I}_g + I_d - \underline{I}_d].\Delta R_s(V_{gs}, V_{ds}) \qquad (5.15)$$

A series of measurements were made of a power FET. The proposed corrections for the output conductance and transconductance were

implemented and compared with the simulation from DC current data. The result concluded that the inclusion of these effects improved the accuracy of the model and produced simulations from DC data with accuracy similar to that obtainable from pulsed I-V measurements.

For the model proposed in this work, rather than modify the DC current as above, it was decided to abandon the DC current altogether, since the well-known effects of frequency dispersion substantially alter the characteristics of active devices between low and high frequencies. Also, from the above work, it is unclear whether or not the model is able to predict very nonlinear responses.

5.3.4 Proposed Method of Current Derivation

The previous sections discussed the difficulties arising from using the DC current to predict AC behaviour due to frequency dispersion of g_m and g_o, with the derivation of the current from the small-signal transconductance and output conductance. In this section, it will be shown that the inclusion of an extra nonlinear resistor allows the nonlinear model to be derived from S-parameter measurements. Not only can the current be accurately found, but the effects of frequency dispersion are modelled in the new nonlinear model.

The dispersive nature of g_m and g_d has been discussed previously, where g_d was strongly dispersive and g_m was a weaker function of frequency. If g_m was assumed to be constant with frequency, then the current I_{ds} could be found by integrating g_m with respect to V_{gs}. If the current accurately predicted the output conductance, then

$$\partial I_{ds}/\partial V_{ds}\,|_{V_{gs}} = g_d \qquad (5.16)$$

However, because of the dispersive nature of g_d, this equation was not satisfied and the output conductance and simulated output impedance of the model were incorrectly defined. The effects of dispersion in the output

conductance could be modelled by including a resistor R_x in parallel with the current generator I_{ds}.

In Figure 5.6, R_{ds} represents the output conductance extracted from the S-parameter measurements, and R_{ds}' represents $\partial V_{ds}/\partial I_{ds}$ (where I_{ds} is the integral of g_m). The resistor R_x was added in parallel to R_{ds}' such that $R_{ds}'//R_x = R_{ds}$. Here:

$$R_x = R_{ds} \times R_{ds}'/(R_{ds}' - R_{ds}) \qquad (5.17)$$

and at high frequencies, the combination of R_x and R_{ds}' produced an output conductance which matched R_{ds}. The series capacitor C_x ensured that the DC characteristics were unchanged by the inclusion of R_x and that the frequency response of R_{ds} was similar to Figure 5.5.

The resistor R_x was defined as a nonlinear element, since the required correction of I_{ds} was different at each bias point. The capacitor C_x was bias independent or extrinsic, since its value was only important in establishing

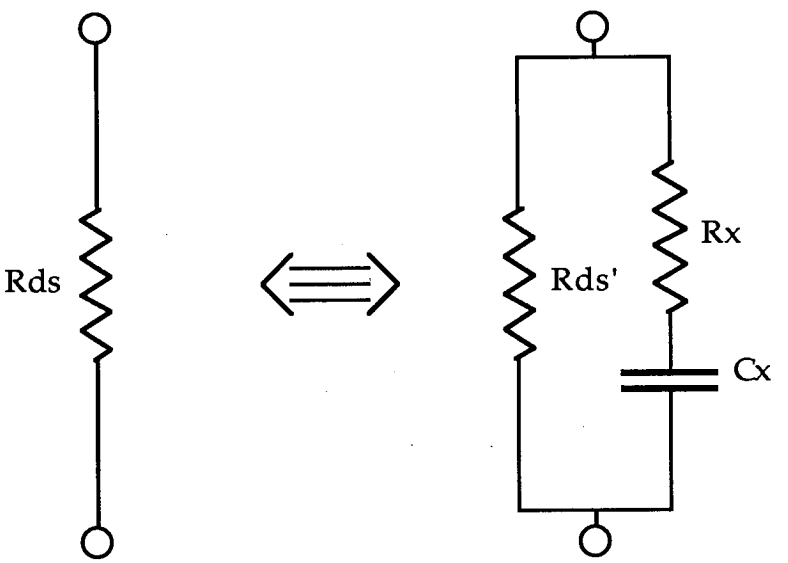


Figure 5.6: Modelling frequency dispersion in the output conductance

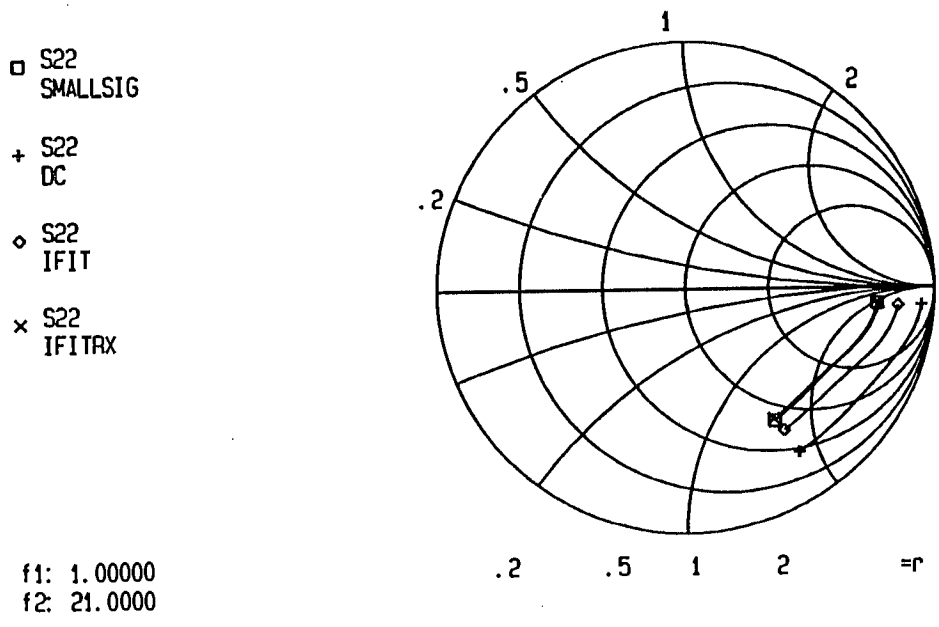
the frequency response and had a negligible effect at high frequencies (> 1.0MHz). The capacitance would require to be accurately known, and made a function of bias, if the model was to be used for simulating video frequency circuits.

As a check on the nonlinear model, we should be able to accurately predict the small-signal as well as the large-signal characteristics of the MESFET. Figure 5.7 clearly demonstrates that this can only be achieved with the inclusion of the R_xC_x pair. S22 and the magnitude of S21 are shown at five different bias points. The S-parameters labelled 'Smallsig' represent the measured characteristics and 'DC' represents a model where g_m and R_{ds} have been derived from the DC characteristics, as in most of the semi-empirical models. The 'Ifit' parameters illustrate a linear model where the current is derived from the integral of g_m only and no attempt has been made to model the frequency dispersion in the output conductance. 'Ifitrx' is similar to 'Ifit', with the inclusion of the R_xC_x pair. From all of the plots it can be seen that the model which best predicts the measured results at all of the bias points is 'Ifitrx' and that the inclusion of the R_xC_x pair is important to accurately predict the small-signal characteristics using the nonlinear model.

5.4 Curve fitting

5.4.1 Introduction

For large-signal modelling, it was necessary to find a way of expressing the nonlinear elements of the equivalent circuits, as functions of the internal gate and drain voltages. The simplest method would be to use a look-up table containing values for all of the nonlinear elements. For a combination of controlling voltages, the table would yield values for the nonlinear elements at the nearest index voltages. For control voltages lying between indexed points in the look-up table, interpolation would be used to calculate element



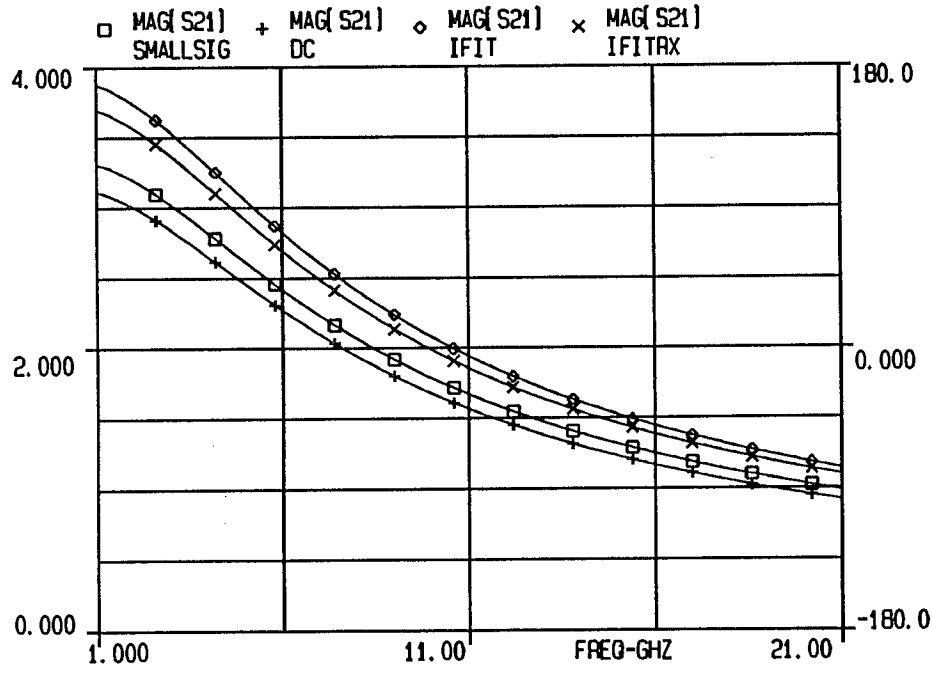
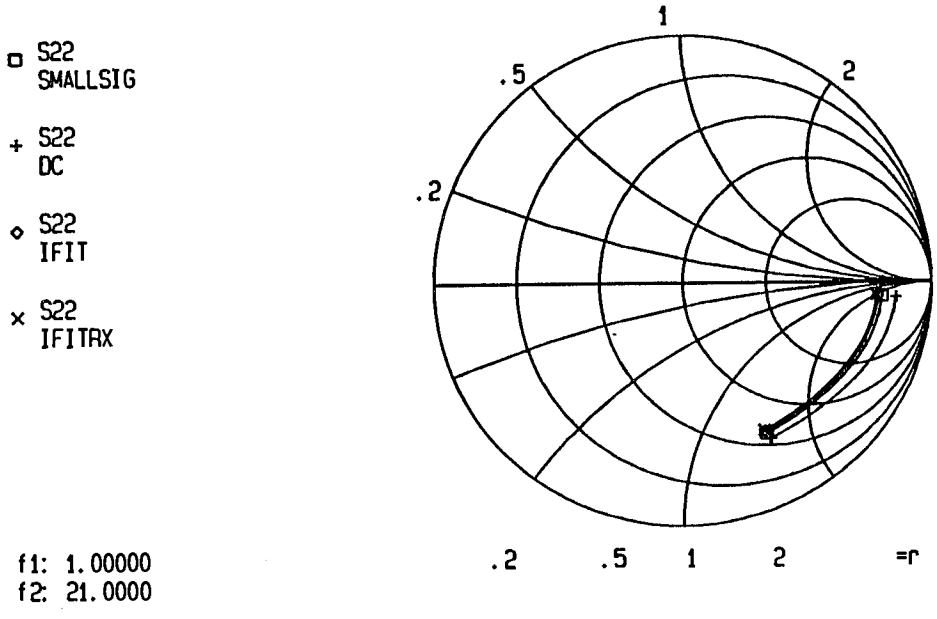


Figure 5.7a: Comparisons between the small-signal characteristics of various nonlinear models at Vds=9V, 100%Idss



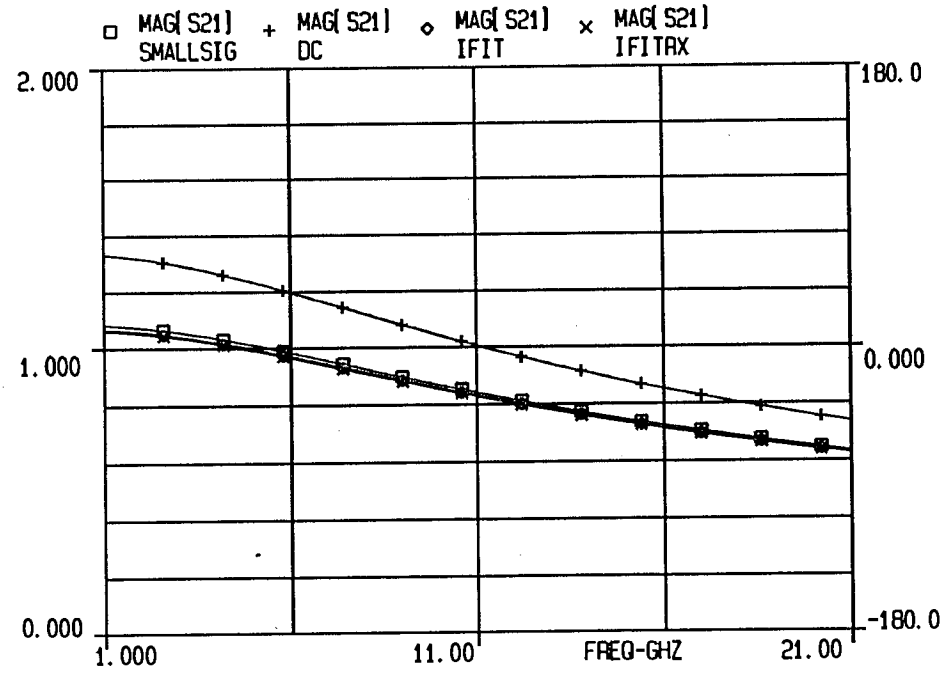
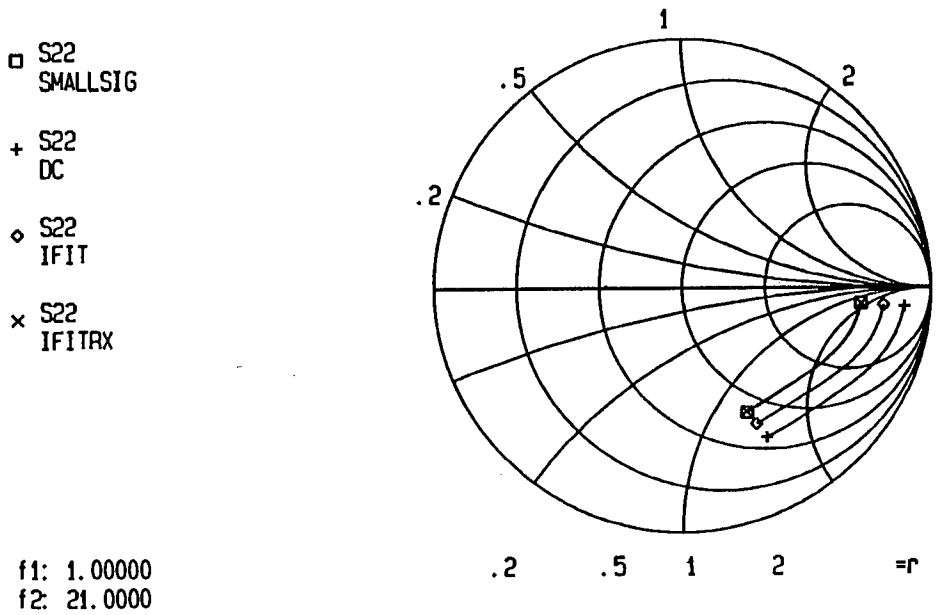


Figure 5.7b: Comparisons between the small-signal characteristics of various nonlinear models at Vds=9V, 10%Idss



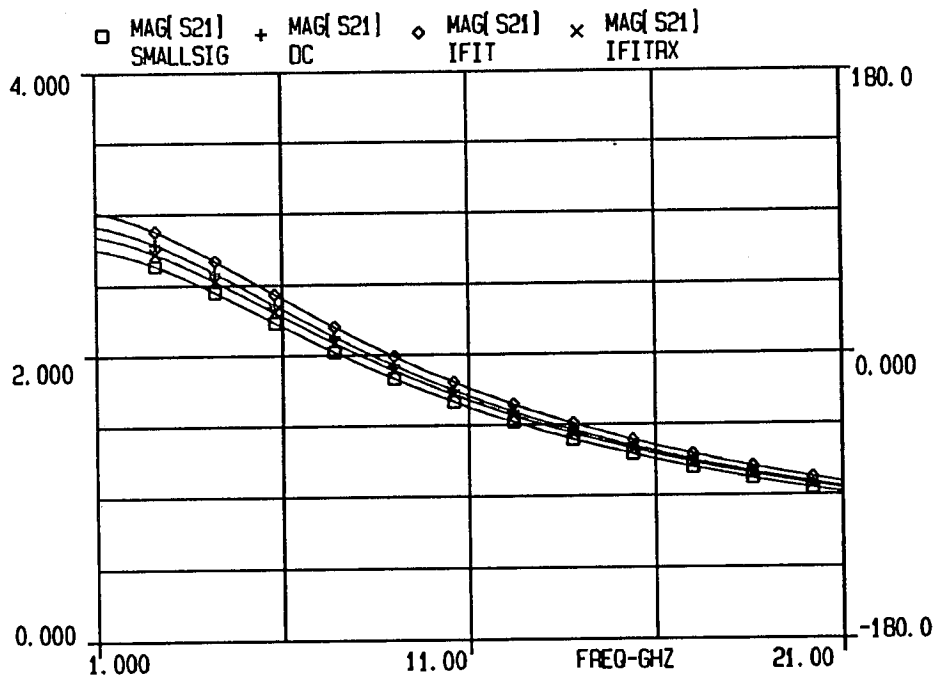
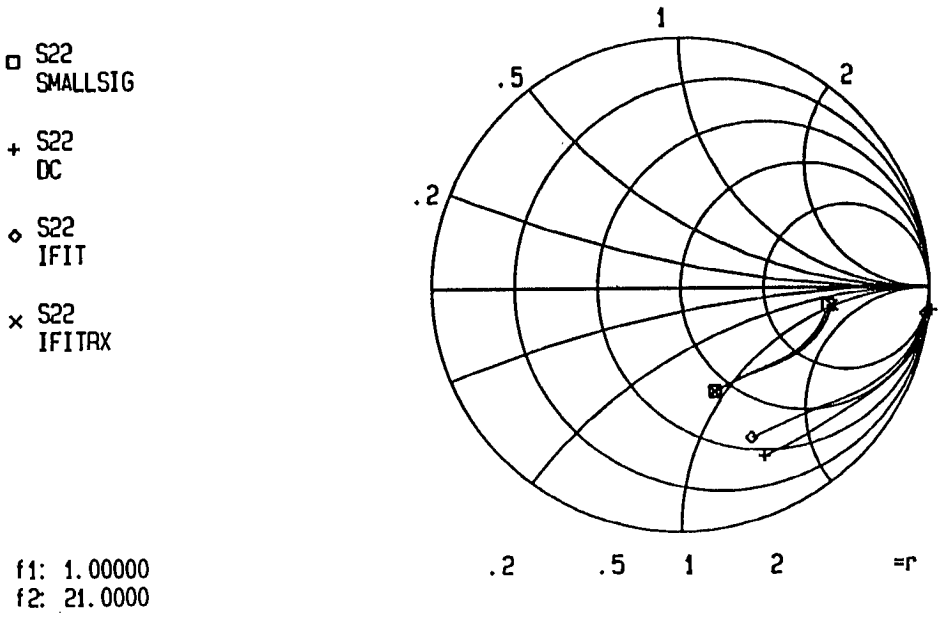


Figure 5.7c: Comparisons between the small-signal characteristics of various nonlinear models at Vds=5V, 50%Idss



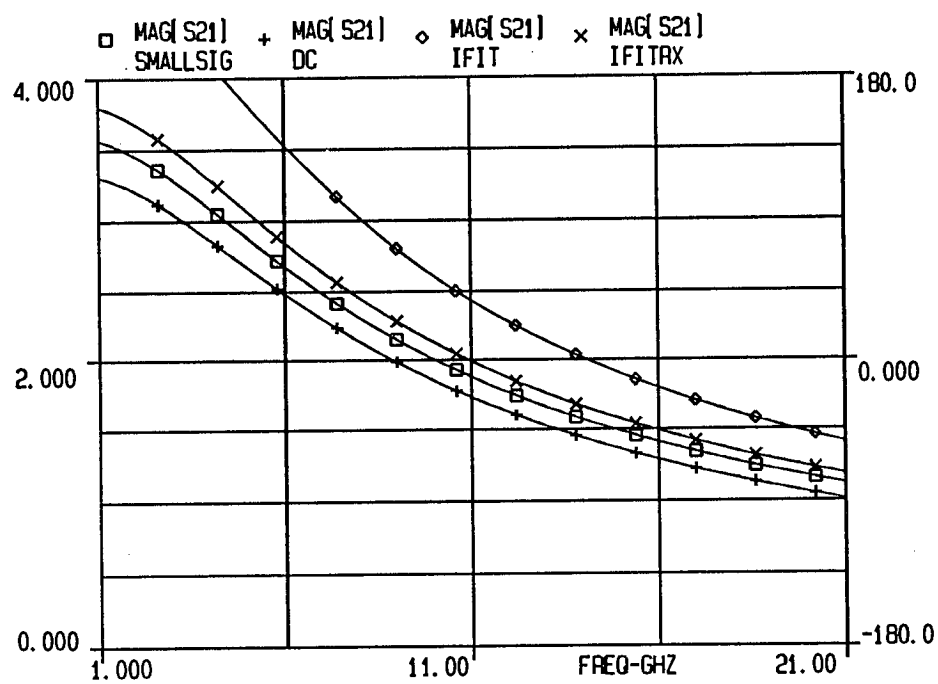
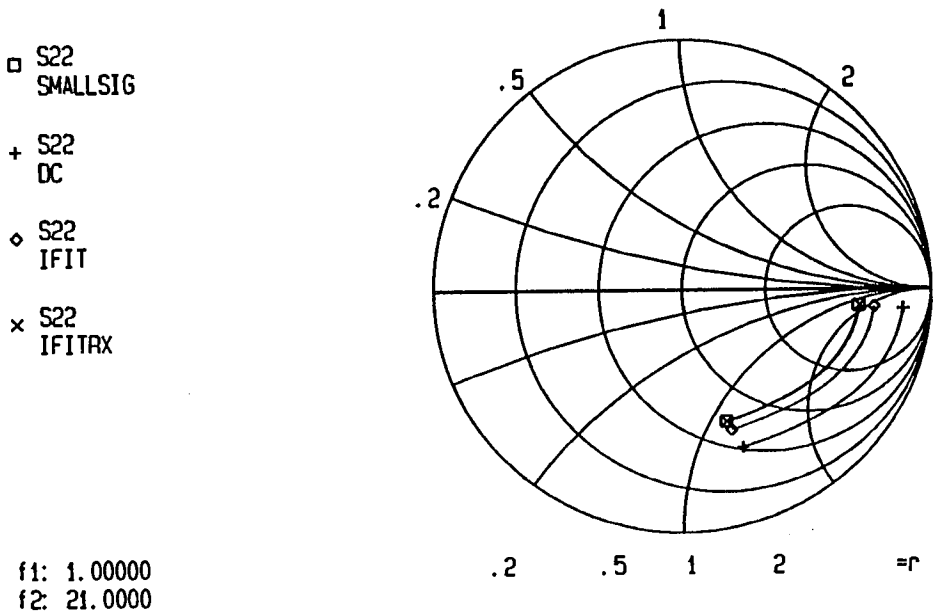


Figure 5.7d: Comparisons between the small-signal characteristics of various nonlinear models at Vds=2V, 100%Idss



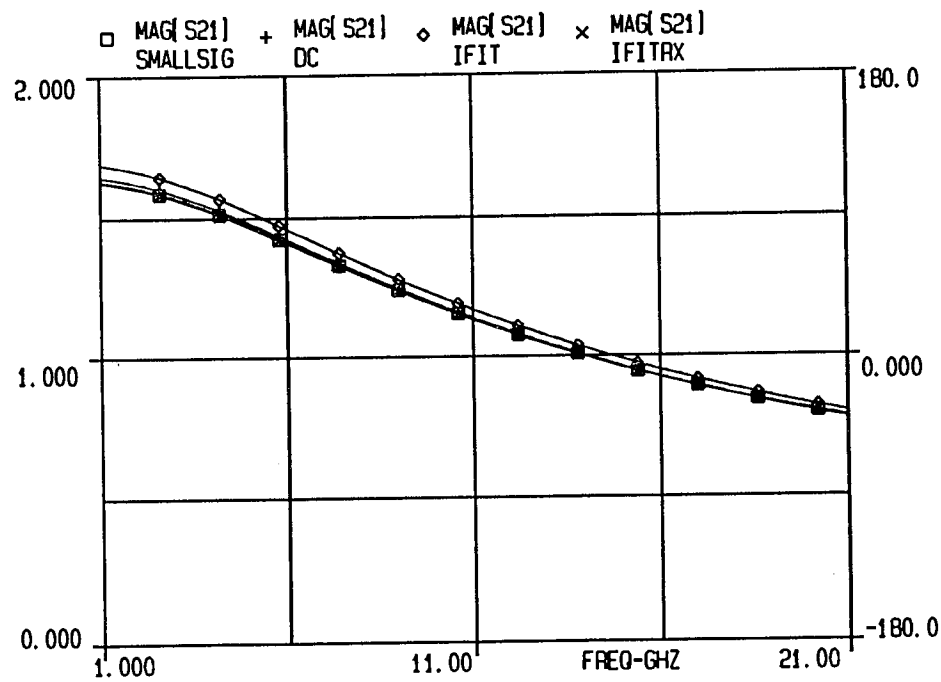


Figure 5.7e: Comparisons between the small-signal characteristics of various nonlinear models at Vds=2V, 10%Idss

values. The disadvantages of this method are that:

- Interpolating between measured control voltages would result in nonlinear functions which were described as a number of straight lines between measured points. In fact, a curve would more accurately describe the variation in the elements with voltage, and the only way of achieving this with a look-up table would be to fit a number of points to a spline curve at each time iteration of the solution.

- Time domain simulators require nonlinear functions which can be differentiated and integrated. For example, the conductances are calculated as differentials of the current and it would not be possible to evaluate these parameters using look-up tables.

- A search through the look-up table and an interpolation calculation would be needed for each step of the simulation, requiring time-consuming computation.

- The look-up table could not predict the values of non-linear elements at voltages lying outwith the range of measured points.

An alternative to the look-up table approach was taken in an attempt to reduce the amount of information needed to calculate the nonlinear expressions. The nonlinearities were expressed in equations as functions of the two controlling voltages. This is known as two-dimensional (or surface) fitting, since one variable F(x,y) is defined by two other variables (x and y). The Numerical Algorithms Group (NAG) libraries, which are commercially

available for use on many machines, include a suite of 26 subroutines for two and three-dimensional curve fitting. The following subsections describe the functions used to model bivariate data and the NAG surface fitting techniques.

5.4.2 Chebyshev Polynomials

Surface fitting is used to evaluate a function F(x,y) from data of a nonlinear function z, in terms of control parameters x and y. Polynomials and cubic splines are preferred in surface fitting, because they are simple to calculate, derive, differentiate and integrate. The cubic spline is the most versatile function to which data can be fitted: it consists of a number of cubic polynomial segments joined end to end with continuity at the joins, in the first and second derivatives. The x and y values of the joins are called knots, and the number of knots determines the coefficients of the spline function, in the same way that the degree determines the number of coefficients in a polynomial. The disadvantages of the cubic spline are that it is less convenient to integrate and implement in a large-signal simulator.

The standard two-dimensional polynomial is defined as

$$\begin{aligned} F(x,y) = {} & a_{00} + a_{01}y + a_{02}y^2 + \ldots + \\ & a_{10}x + a_{11}x\,y + a_{12}x\,y^2 + \ldots + \\ & a_{20}x^2 + a_{21}x^2y + a_{22}x^2y^2 + \ldots + \\ & + \ldots \end{aligned} \tag{5.18}$$

The Chebyshev function is slightly different and is defined as

$$F(x,y) = 0.5\,a_{00}T_0(x)T_0(y) + 0.5\,a_{01}T_0(x)T_1(y) + 0.5\,a_{02}T_0(x)T_2(y) + \ldots +$$

$$0.5\,a_{10}T_1(x)T_0(y) + \quad a_{11}T_1(x)T_1(y) + \quad a_{12}T_1(x)T_2(y) + \ldots +$$
$$0.5\,a_{20}T_2(x)T_0(y) + \quad a_{21}T_2(x)T_1(y) + \quad a_{22}T_2(x)\,T_2(y) + \ldots +$$
$$+ \ldots \tag{5.19}$$

where $T_i(x)$ and $T_j(y)$ are Chebyshev polynomials.

In this work, the Chebyshev polynomial was used in the surface fitting algorithms, since their advantages [156] over the standard polynomial are that a greater accuracy in the computation of the polynomial coefficients, for a given polynomial degree, is possible and that evaluation of the fitted polynomial at specific points is more accurate. The latter (i.e. higher order) terms decrease more rapidly than equivalent terms in the standard polynomial and can sometimes be neglected, indicating that the degree of polynomial can be reduced for a given degree of fit.

The bivariate Chebyshev polynomial can be written as

$$F(x,y) = \sum_{i=0}^{K} \sum_{j=0}^{L} a_{ij}\,T_i(x)\,T_j(y) \tag{5.20}$$

where K and L represent the degree of fit in x and y, and $T_i(x)$ and $T_j(y)$ are Chebyshev polynomials [157] of the first degree, where

$$T_i(x) = \cos i\beta \text{ for } \cos\beta = x \tag{5.21}$$

$$T_0(x) = \cos 0\beta = 1$$

$$T_1(x) = \cos 1\beta = \cos(1\times\arccos x) = x$$

$$T_2(x) = \cos 2\beta = \cos(2\times\arccos x)$$

etc.

Following the standard convention, the first terms in x and y (for which i=0 and j=0) are halved; for i=j=0, the coefficient is quartered. Note that for $-1 \le x$

≤ 1, $0 \leq T_i(x) \leq 1$. Therefore values for x and y are normalized to the range -1 to +1 where the value of the coefficients represent the maximum value for the Chebyshev polynomial for any value of x. Using normalization also improves the computational accuracy. The variable x is normalized to x_{norm} by

$$x_{norm} = (2x - (x_{max} + x_{min}))/(x_{max} - x_{min}) \quad (5.22)$$

where x_{max} and x_{min} are the largest and smallest values for x over all of the data points. Y is normalized in a similar way. Chebyshev polynomials may also be expressed as terms of standard polynomials.

$$T_0(x) = 1$$

$$T_1(x) = x$$

$$T_2(x) = 2x^2 - 1$$

$$T_3(x) = 4x^3 - 3x$$

$$T_4(x) = 8x^4 - 8x^2 + 1$$

$$T_5(x) = 16x^5 - 20x^3 + 5x$$

$$T_{n+1}(x) = 2x * T_n(x) - T_{n-1}(x) \quad \text{for } n \geq 1 \quad (5.23)$$

5.4.3 Integrating and Differentiating Chebyshev Polynomials

The nonlinear elements were expressed as Chebyshev polynomials in the form described in the previous section. Some of the nonlinear elements were required to be integrated and differentiated and this could be done once they had been fitted to Chebyshev polynomials. For example, the transconductance was integrated to find the current and the capacitances were integrated to find the charge; differentiation was required to find the value of the resistor R_x from the current.

Most of the nonlinear functions could be expressed as polynomial

functions of V_{gs} and V_{ds} to the 4th degree. The remainder of this section describes the method by which a Chebyshev polynomial was integrated and differentiated, and this is illustrated with a 4th order polynomial, describing the transconductance g_m.

From (5.20), where K=L=4,

$$\begin{aligned} g_m = \; & a_{00} + a_{01}T_1(y) + a_{02}T_2(y) + a_{03}T_3(y) + a_{04}T_4(y) \\ & + a_{10}T_1(x) + a_{11}T_1(x)T_1(y) + a_{12}T_1(x)T_2(y) + a_{13}T_1(x)T_3(y) + a_{14}T_1(x)T_4(y) \\ & + a_{20}T_2(x) + a_{21}T_2(x)T_1(y) + a_{22}T_2(x)T_2(y) + a_{23}T_2(x)T_3(y) + a_{24}T_2(x)T_4(y) \\ & + a_{30}T_3(x) + a_{31}T_3(x)T_1(y) + a_{32}T_3(x)T_2(y) + a_{33}T_3(x)T_3(y) + a_{34}T_3(x)T_4(y) \\ & + a_{40}T_4(x) + a_{41}T_4(x)T_1(y) + a_{42}T_4(x)T_2(y) + a_{43}T_4(x)T_3(y) + a_{44}T_4(x)T_4(y) \end{aligned} \quad (5.24)$$

where x and y are the normalized variables of V_{gs} and V_{ds} respectively (see equation (5.22)). The coefficients for x and y for i=0 and j=0 had been halved already. Each of the Chebyshev functions were substituted with the equivalent standard polynomial expression from (5.23) to give

$$\begin{aligned} g_m = \; & a_{00} + a_{01}y + a_{02}(2y^2-1) + \ldots \\ & + a_{10}x + a_{11}xy + a_{12}x(2y^2-1) + \ldots \\ & + a_{20}(2x^2-1) + a_{21}(2x^2-1)\,y + a_{22}(2x^2-1)(2y^2-1) + \ldots \\ & + \ldots \end{aligned} \quad (5.25)$$

This equation is rearranged so that g_m is now expressed in terms of standard polynomials:

$$\begin{aligned} g_m = \; & b_{00} + b_{01}y + b_{02}y^2 + b_{03}y^3 + b_{04}y^4 \\ & + b_{10}x + b_{11}xy + b_{12}xy^2 + b_{13}xy^3 + b_{14}xy^4 \\ & + b_{20}x^2 + b_{21}x^2y + b_{22}x^2y^2 + b_{23}x^2y^3 + b_{24}x^2y^4 \\ & + b_{30}x^3 + b_{31}x^3y + b_{32}x^3y^2 + b_{33}x^3y^3 + b_{34}x^3y^4 \\ & + b_{40}x^4 + b_{41}x^4y + b_{42}x^4y^2 + b_{43}x^4y^3 + b_{44}x^4y^4 \end{aligned} \quad (5.26)$$

The relationship between a_{ij} and b_{ij} coefficients for two-dimensional 3rd and 4th order Chebyshev polynomials is given in Appendix B. The current I_{ds} is defined as

$$I_{ds} = \int g_m \, \partial V_{gs} \, |_{V_{ds}} \tag{5.27}$$

From (5.22), x is defined as

$$x = (2V_{gs} - V_{g1})/V_{g2} \tag{5.28}$$

where $V_{g1} = (V_{gsmax} + V_{gsmin})$ and $V_{g2} = (V_{gsmax} - V_{gsmin})$ (5.29)

$$\Rightarrow \quad \partial x = 2\partial V_{gs}/V_{g2} \tag{5.30}$$

$$\Rightarrow \quad I_{ds} = V_{g2}/2 \left(\int g_m \, \partial x \, |_{V_{ds}} \right) \tag{5.31}$$

From (5.26) and (5.31),

$$\begin{aligned} I_{ds} = V_{g2}/2 \, [\; & b_{00}x + b_{01}xy + b_{02}xy^2 + b_{03}xy^3 + b_{04}xy^4 \\ & + b_{10}x^2/2 + b_{11}x^2y/2 + b_{12}x^2y^2/2 + b_{13}x^2y^3/2 + b_{14}x^2y^4/2 \\ & + b_{20}x^3/3 + b_{21}x^3y/3 + b_{22}x^3y^2/3 + b_{23}x^3y^3/3 + b_{24}x^3y^4/3 \\ & + b_{30}x^4/4 + b_{31}x^4y/4 + b_{32}x^4y^2/4 + b_{33}x^4y^3/4 + b_{34}x^4y^4/4 \\ & + b_{40}x^5/5 + b_{41}x^5y/5 + b_{42}x^5y^2/5 + b_{43}x^5y^3/5 + b_{44}x^5y^4/5 \\ & + K_0 + K_1y + K_2y^2 + K_3y^3 + K_4y^4 \;] \end{aligned} \tag{5.32}$$

where the K_i terms are the constants of integration and contain polynomial terms of y only. If an indefinite integral is required, then the K_i terms are evaluated by assuming that at $V_{gs}=V_{gsmin}$, the current I_{ds} is equal to the DC current for all V_{ds}. Since this is close to the pinch-off voltage, a negligible error is introduced by this assumption. When $V_{gs}=V_{gsmin}$, x=-1 and (5.32) becomes

$$\begin{aligned} I_{ds} = V_{g2}/2 \, [\; & (K_0 - b_{00} + b_{10}/2 - b_{20}/3 + b_{30}/4 - b_{40}/5) + \\ & (K_1 - b_{01} + b_{11}/2 - b_{21}/3 + b_{31}/4 - b_{41}/5)y + \\ & (K_2 - b_{02} + b_{12}/2 - b_{22}/3 + b_{32}/4 - b_{42}/5)y^2 + \\ & (K_3 - b_{03} + b_{13}/2 - b_{23}/3 + b_{33}/4 - b_{43}/5)y^3 + \end{aligned}$$

$$(K_4 - b_{04} + b_{14}/2 - b_{24}/3 + b_{34}/4 - b_{44}/5)y^4 \ ] \qquad (5.33)$$

The five K_i terms can be found by choosing five different values for V_{ds} and substituting them into (5.33). This produces five equations with five unknowns and can be solved for K_i using Gaussian elimination.

The Chebyshev polynomials are easy to differentiate. The current I_{ds} in (5.32) can be differentiated with respect to V_{ds} to give the output conductance, where

$$\partial y = 2\partial V_{ds} / V_{d2} \qquad (5.34)$$

$$\Rightarrow \quad g_d = V_{g2} (\partial I_{ds} / \partial y) \ / \ V_{d2} \qquad (5.35)$$

Therefore from (5.32) the output conductance is given by

$$\begin{aligned} g_d = V_{g2}/V_{d2} [\ & b_{01}x + 2b_{02}xy + 3b_{03}xy^2 + 4b_{04}xy^3 \\ & + b_{11}x^2/2 + 2b_{12}x^2y/2 + 3b_{13}x^2y^2/2 + 4b_{14}x^2y^3/2 \\ & + b_{21}x^3/3 + 2b_{22}x^3y/3 + 3b_{23}x^3y^2/3 + 4b_{24}x^3y^3/3 \\ & + b_{31}x^4/4 + 2b_{32}x^4y/4 + 3b_{33}x^4y^2/4 + 4b_{34}x^4y^3/4 \\ & + b_{41}x^5/5 + 2b_{42}x^5y/5 + 3b_{43}x^5y^2/5 + 4b_{44}x^5y^3/5 \\ & + K_1 + 2K_2y + 3K_3y^2 + 4K_4y^3 \ ] \end{aligned} \qquad (5.36)$$

5.4.4 Surface Fitting Techniques

It has been shown that the Chebyshev polynomial is the most convenient way in which the nonlinear expression can be implemented into the simulator. In this section, the software tools which were used to fit the nonlinear data to the Chebyshev polynomials will be described.

The NAG library routine E02CAF [158] fits bivariate data to a two-dimensional Chebyshev polynomial, and is an implementation of the method described by Clenshaw *et al* [159]. Some fitting algorithms offered the option of 'smoothing', where experimental errors were smoothed out in the fitting process. An alternative method for smoothing the errors, was to reduce the degrees of the polynomial function. In both cases, there was a

conflict between smoothness and closeness of fit and, for this application, emphasis was placed on the closeness of fit for all of the nonlinear functions.

A weighting factor was specified for each data point. The purpose of the weighting was to estimate the accuracy of the data point: a low weight would indicate a point of uncertain value which would not have a large influence on the final function. The weights could also be used to remove undesirable ripples from the final fit.

There were two ways of estimating the quality of fit between the data and the Chebyshev polynomial. A normalized error function E was calculated for the fit, representing the difference between the data and polynomial over all data points. The error was defined as:

$$E = 100 * \sum (\mid \text{data-polynomial} \mid) \; / \; \sum (\text{data}) \qquad (5.37)$$

The quality of the fit could also be estimated by inspection and a programme was written to plot the data, polynomials and relative errors.

Generally, for each of the nonlinear elements, the degree of fit was maintained as low as possible. High order fits contained many coefficients which greatly increased the computation time during large-signal simulation. Low order fits contained few coefficients but the polynomial fit was often poor. The optimum fit was obtained by continually reducing the highest degree of polynomial for each control voltage until the quality of the fit started to deteriorate.

In some cases, instability would result from fits using high polynomial degrees. This occurred when there were insufficient data points to describe the smoothness of the surface for high order fits. In Figure 5.8, instability results from the high rather than the low order fit. Instability was removed by adding extra interpolated points to the data to smooth the high order fit. These points were estimated from neighbouring data points.

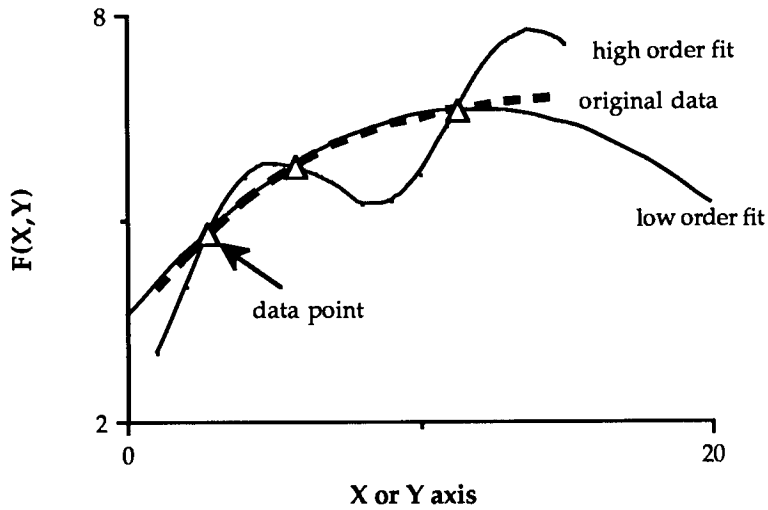


Figure 5.8: Instability with fitting high order functions to data

5.5 Fitting the Nonlinear Elements to Chebyshev Polynomials

5.5.1 Introduction

For each of the six nonlinear elements, a Chebyshev polynomial was evaluated, and altogether they were implemented in the nonlinear simulator ANAMIC. The smoother nonlinear surfaces could be described by low order polynomials whereas those with steep arches and humps required high order polynomials. This section describes the individual polynomials which were fitted to each of the nonlinear expressions, where the polynomial degree was chosen by the shape of the surface and the importance of the nonlinear element.

In ANAMIC, the nonlinear components of current, capacitance and resistance are described as nonlinear voltage and current generators. The polynomial nonlinearities were calculated in Fortran subroutines and linked to the main program; they were then compiled before simulation. Appendix

C lists the library file, which includes Fortran subroutines for each of the nonlinear elements.

A circuit definition for τ, the transit delay under the gate, was not implemented as there was no way of describing the time delay in ANAMIC. This slightly reduced the accuracy of the model but since τ was a secondary effect, the results obtained from the model were still valid. One method has been suggested [61] for modelling the time delay. If

$$I_{ds} = I\ [\ V_{gs}(t - \tau),\ V_{ds}\ ] \tag{5.38}$$

then I_{ds} can be approximated as

$$I_{ds} = I\,[v] - \tau\, \partial I\,[v] / \partial t \tag{5.39}$$

where

$$\partial I\,[v] / \partial t = [\ \partial I\,[v] / \partial V\ ]\,|_{V_{ds}} \times \partial V_{gs} / \partial t \tag{5.40}$$

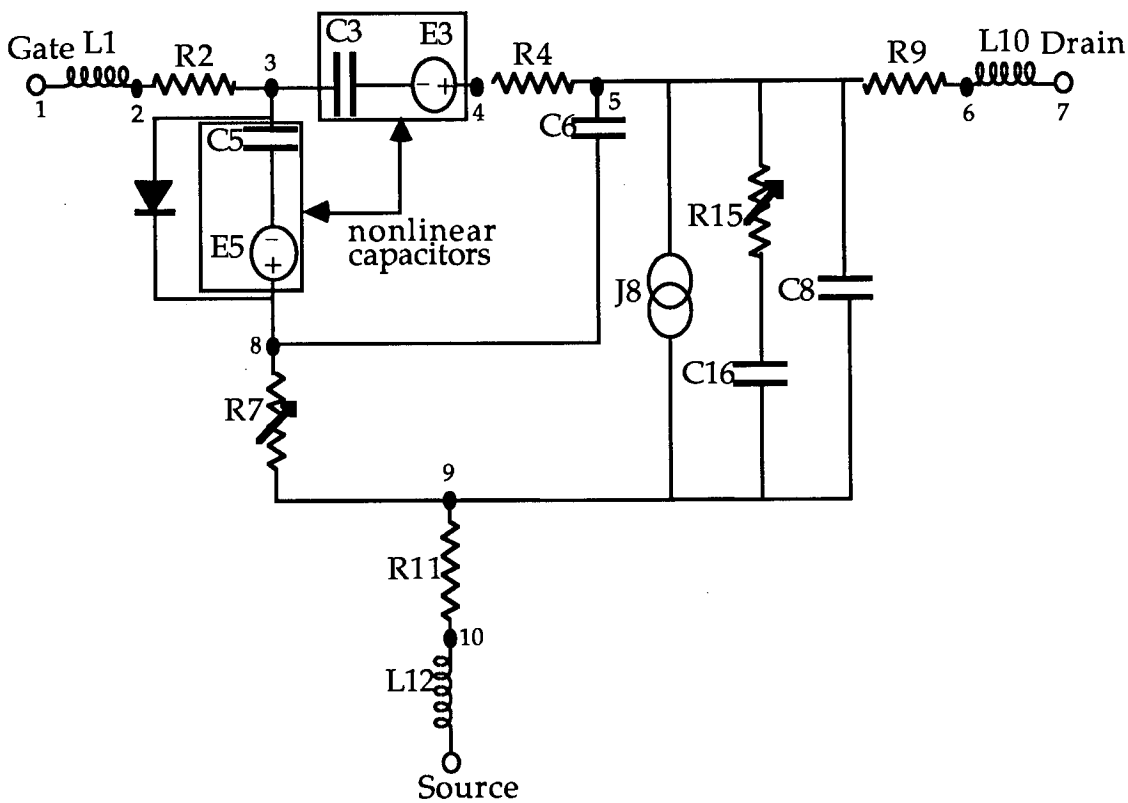


Figure 5.9: The large-signal model in ANAMIC

Details of the implementation of each of the nonlinear elements in ANAMIC and the curve fitting procedures to define their respective two-dimensional polynomials are discussed below. The large-signal model is illustrated in Figure 5.9, which includes numbered elements. The voltage and current for the nonlinear element N_x are V_x and I_x respectively.

5.5.2 The Current Ids

In ANAMIC, the channel current was defined as a voltage controlled current source $I_{ds}(V_1, V_2, ...,)$. The current was derived from the integral of the transconductance and comprised a nonlinear current source in parallel with a series R_xC_x pair, as discussed in Chapter Five.

It was important to model the nonlinearity of the current I_{ds} accurately, as the model was most sensitive to the current. One method for defining I_{ds} would be to fit a two-dimensional third or fourth order Chebyshev polynomial to the transconductance and integrate the polynomial expression mathematically with respect to the gate voltage. In this integration however, any inaccuracy of the transconductance surface fit would accumulate as errors in the current. The transconductance surface contained a sharp 'knee' point, representing the transition from the linear to the saturation region (see Figure 4.11) and a higher order polynomial was needed to describe the surface.

Mathematical integration of a two-dimensional 8th or 9th order polynomial is very complicated (see eqn. (5.32)) and the current was therefore calculated by integrating the transconductance numerically. This was done prior to surface fitting, using the graphics and spreadsheet package MATLAB. The transconductance data points were defined for a series of gate voltages at each drain voltage and were fitted to a high-order one-dimensional spline curve $H(V_{gs})$ with negligible error. The spline was integrated with respect to

the gate voltage to give the current Ids:

$$Ids = \int_{-\infty}^{Vgs} H(Vgs)\,\partial Vgs \tag{5.41}$$

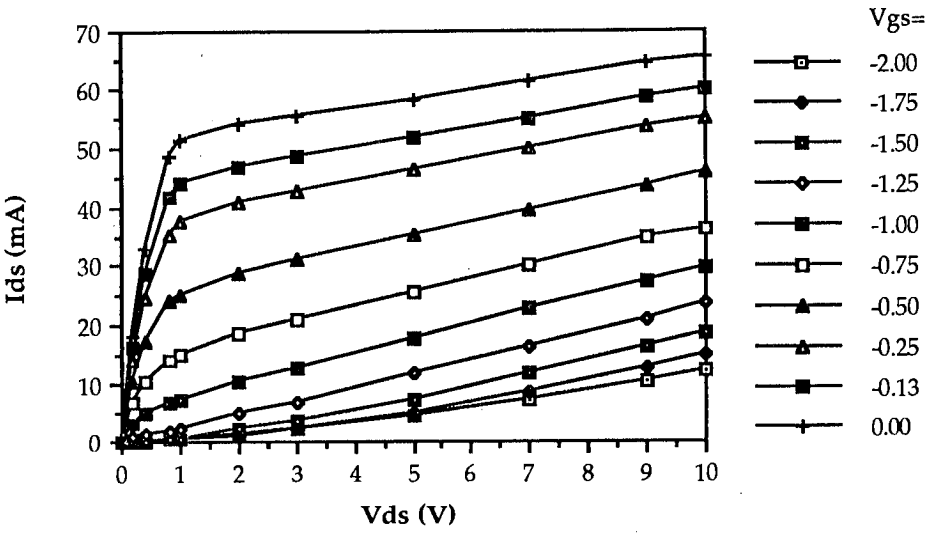
Since the data for the transconductance was only available over a grid of bias points, the current below the minimum gate voltage of -2.0 V (which was very small) was assumed to be the DC current and thus (5.41) became:

$$Ids = \int_{-2.0}^{Vgs} H(Vgs)\,\partial Vgs + Idc(Vgs=-2.0V,Vds) \tag{5.42}$$

Results for the integration of the transconductance of a wafer-probed F20 FET are given in Figure 5.10, where the DC current for $V_{gs} < -2.0$ V has been added. For illustration, Figure 5.11 also shows the DC I/V curves for the same FET. The comparison between the two I/V curves shows that the current rises more steeply with increasing drain voltage at high frequencies, demonstrating the effect of frequency dispersion of g_m and g_o due to the charge exchange effects, as discussed in Section 5.3.2.

The remaining task was to fit the current equation to a polynomial expression. The current 'knee' point on the I/V curve (see Figure 5.11) was impossible to represent using a low order curve. Intermediate degree polynomials fitted the shape of the knee at the expense of adding ripples in the saturation region, along the drain voltage axis. The ripples altered the gradient of the current with respect to the drain voltage, changing the values of the output conductance by a significant amount. Relatively small ripples in the fitted current would affect the output conductance to a large degree and because the output conductance is a very important element in the large-signal model, a high order polynomial was chosen to represent the current. Figure 5.12 illustrates the relationship between the error E and the degree of fit in the polynomial.

A two-dimensional 5th*8th order polynomial was used to fit the



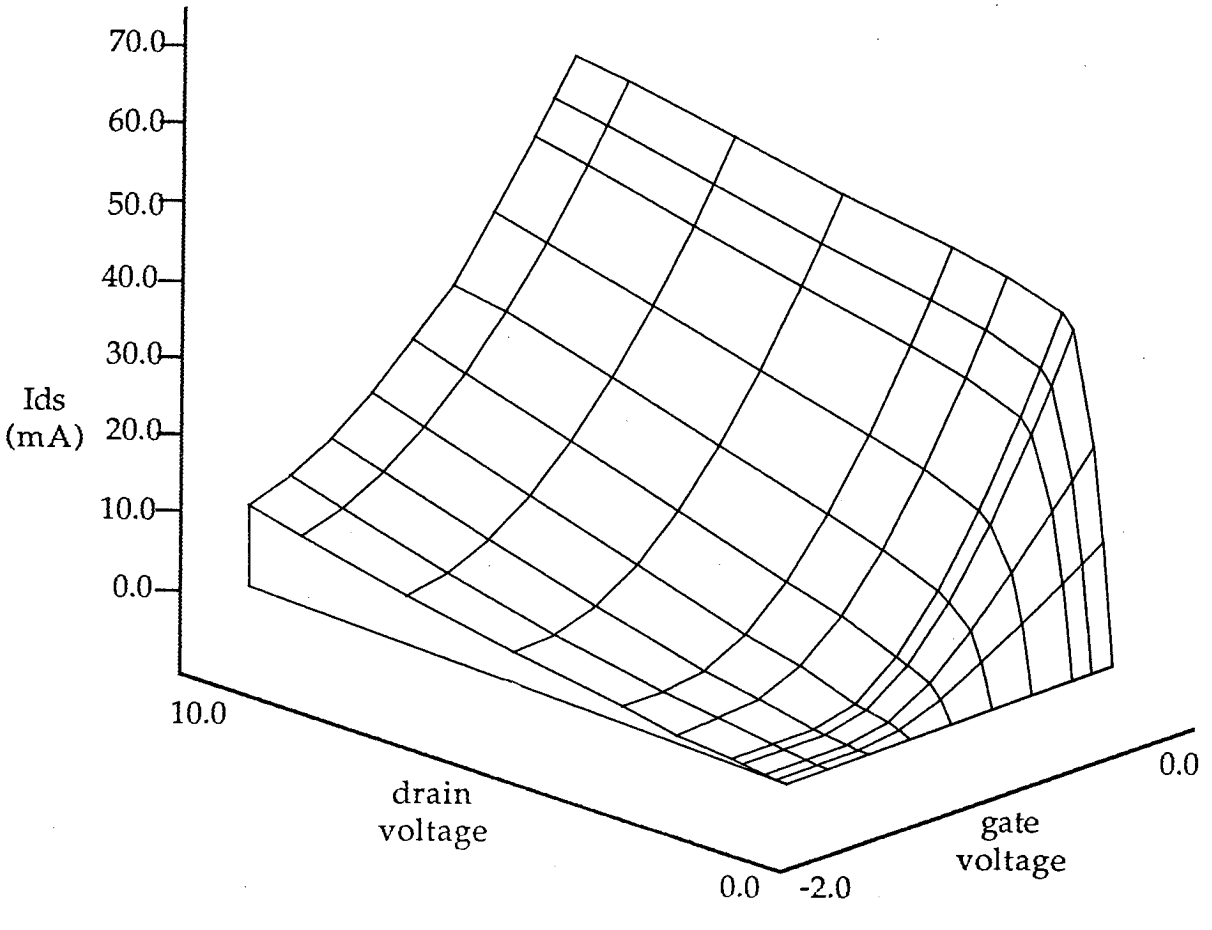


Figure 5.10: The current Ids derived from the transconductance

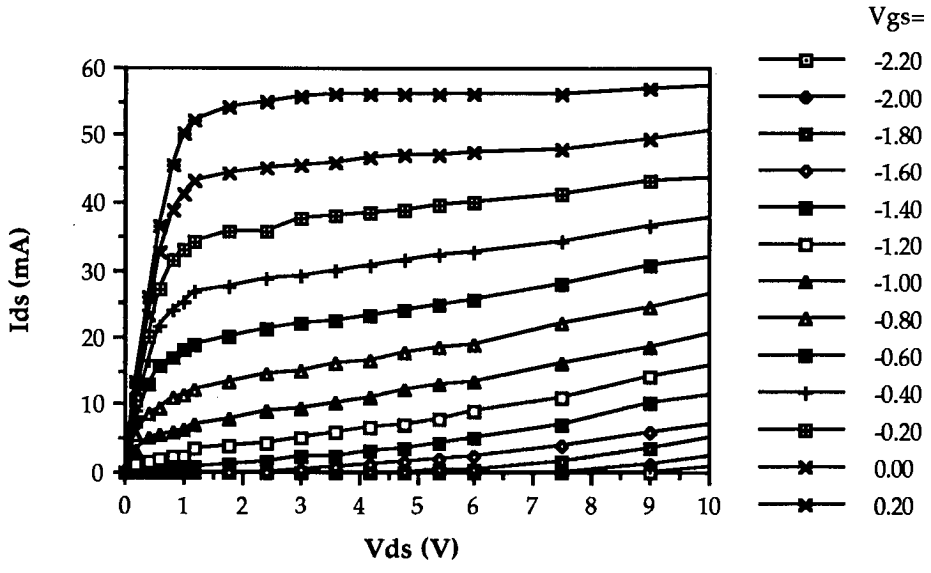


Figure 5.11a: DC I/V curves for 300 micron MESFET

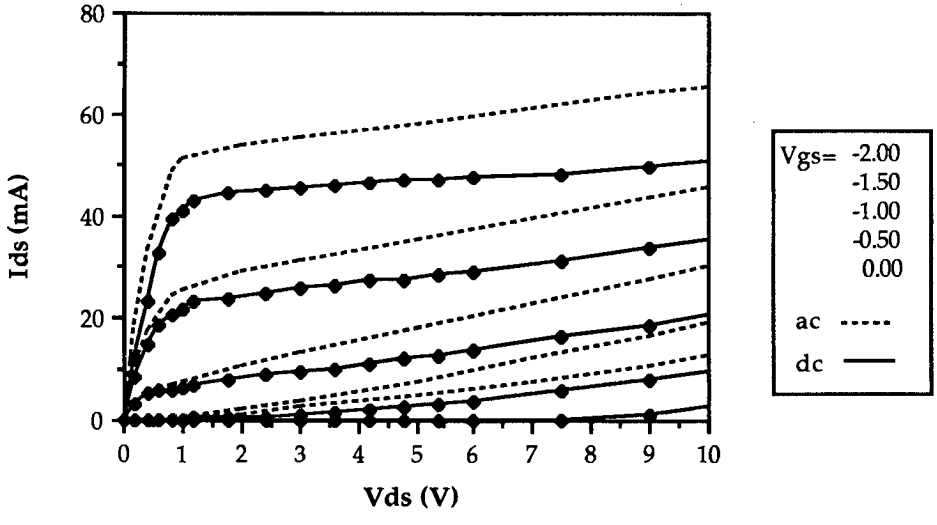


Figure 5.11b: Comparison between DC and AC current characteristics

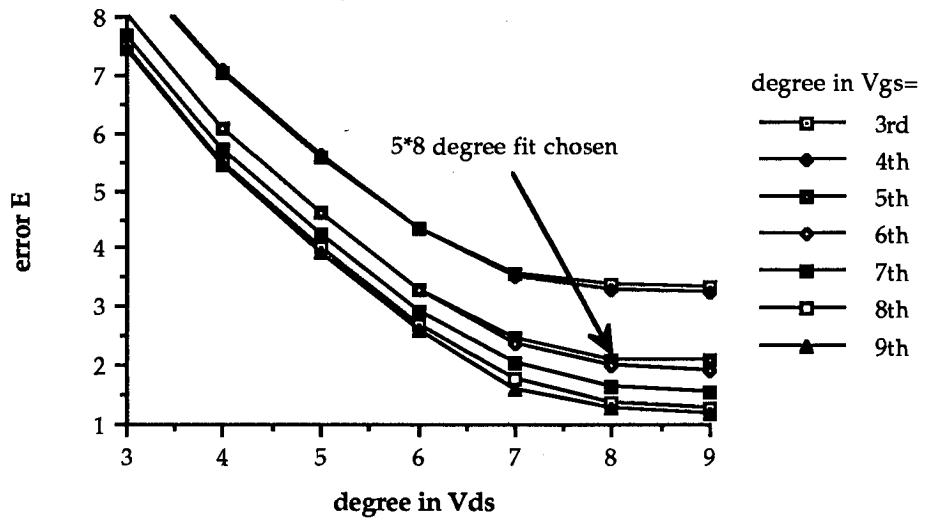


Figure 5.12: Relationship between error and degree of fit

current equation. The 8th order fit was required to fit the current to the drain voltage variable. Lower orders produced a ripple in the current which would degrade the accuracy of the output conductance. When the fitted surface was plotted for each of the original data points, the error appeared to be small. When the polynomial was plotted for a finer distribution of points, as in Figure 5.13, instability was observed. The values for the polynomial at measured points was correct, but at other points the fit was unsuitable, due to the numerical instability of using an 'overspecified' polynomial (for example, one whose order is greater than the number of data points). The fit was improved by adding extra interpolated data points along the drain axis between the original measurements and these were calculated using MATLAB. The maximum gap between two consecutive data points was reduced from 2.0 V to 0.5 V.

The current surface was also extended into the negative gate region to improve the current definition at pinchoff. The extra data points relating to the channel current for V_{ds} at very negative gate voltages were taken with

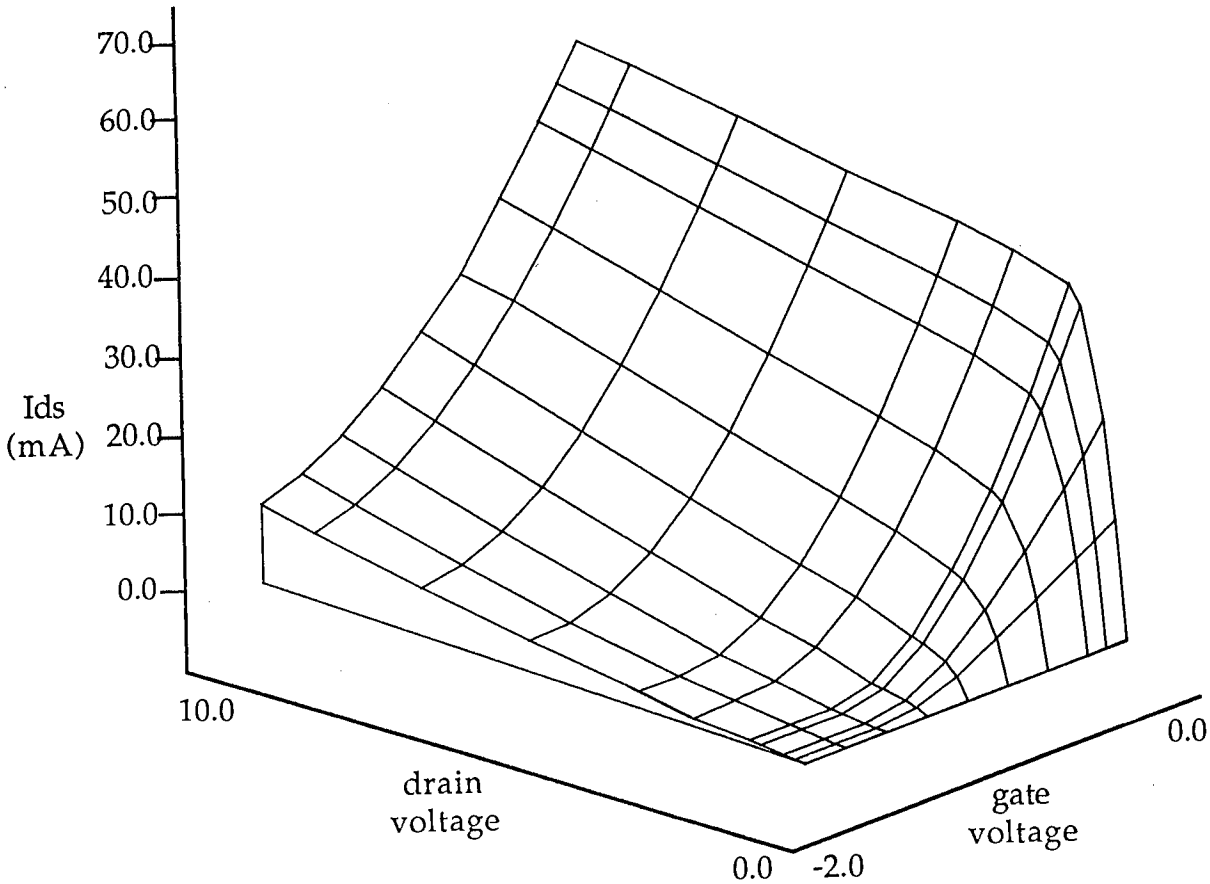


Figure 5.13a: Current fit plotted at each data point appears to be stable

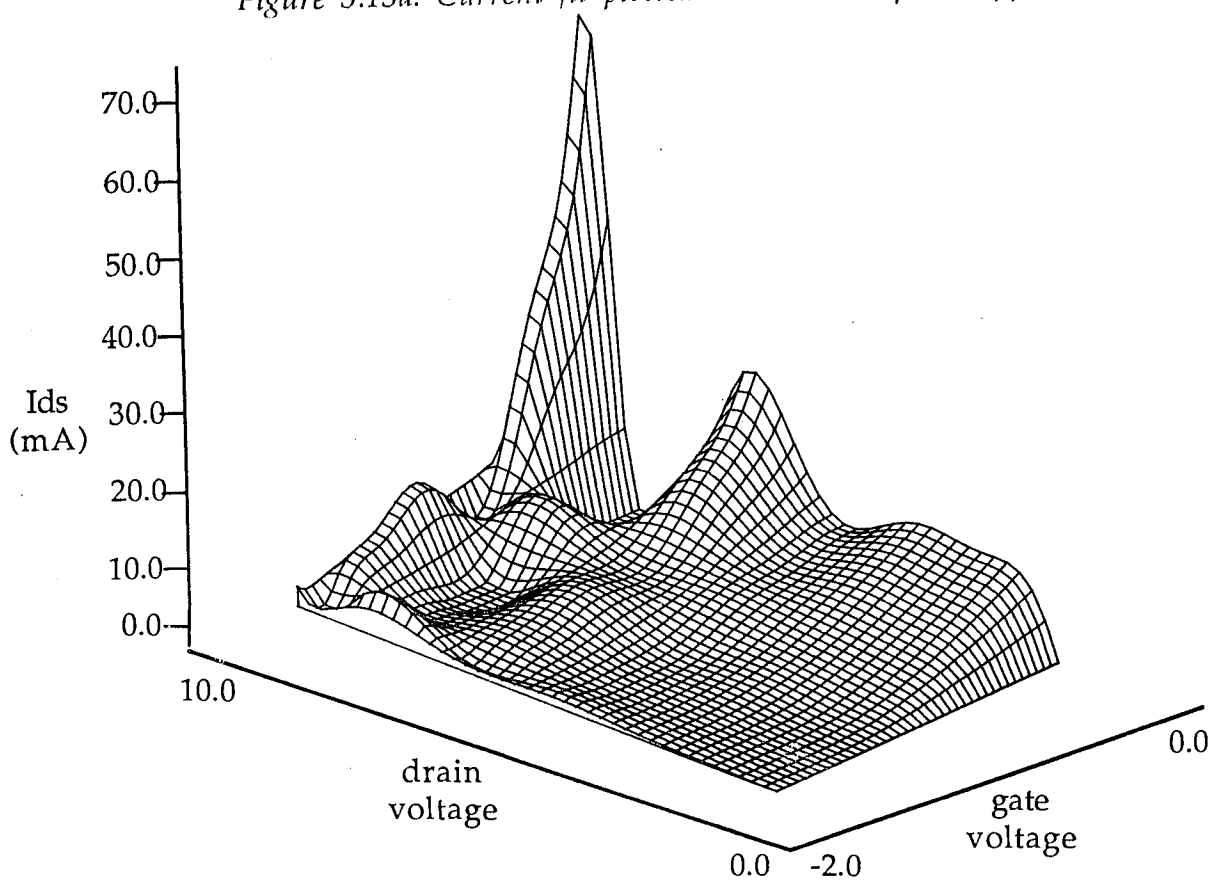


Figure 5.13b: Instability can be seen in the current at intermediate points

negligible error from the DC characteristics of the FET. The current was refitted and is illustrated in Figure 5.14.

The current equation was now defined within a rectangular window of points for V_{ds} and V_{gs}, where:

$$I = I_{ds}(V_{gs}, V_{ds})$$
$$\text{for } -3.0\text{ V} < V_{gs} < 0.0\text{ V}$$
$$\text{and } 0.0\text{ V} < V_{ds} < 10.0\text{ V} \qquad (5.43)$$

The window was extended for a much wider operation range by setting the current to zero for gate voltages more negative than the pinchoff voltage V_p. V_p changed with the drain voltage and was defined as a second order one-dimensional polynomial using MATLAB. The pinchoff voltage and polynomial are plotted in Figure 5.15 and for $V_{gs} < V_p$, the current equalled zero. For $V_{ds} < 0$, the current was assumed to be symmetrically opposite to the current for positive V_{ds}, or:

$$I = -1 \times I_{ds}(V_{gs}, |V_{ds}|) \text{ for } V_{ds} < 0 \qquad (5.44)$$

For $|V_{ds}| > 10.0$V, the current increase with drain voltage was defined as:

$$I = I_{ds}(V_{gs}, 10.0\text{V}) + I_{dg} \qquad (5.45)$$

where the current source I_{dg} was included to represent the drain-gate avalanche effects found at high drain voltages. The purpose of this was not to accurately represent the channel current above V_{ds}=10.0 V, but to provide numerical stability for the convergence of simulation results. The avalanche current was approximated to the forward conduction properties of a Schottky barrier diode. Figure 5.16 illustrates the current I_{ds} in which the definition has been expanded beyond the original measurements, and this expression is used in the nonlinear model.

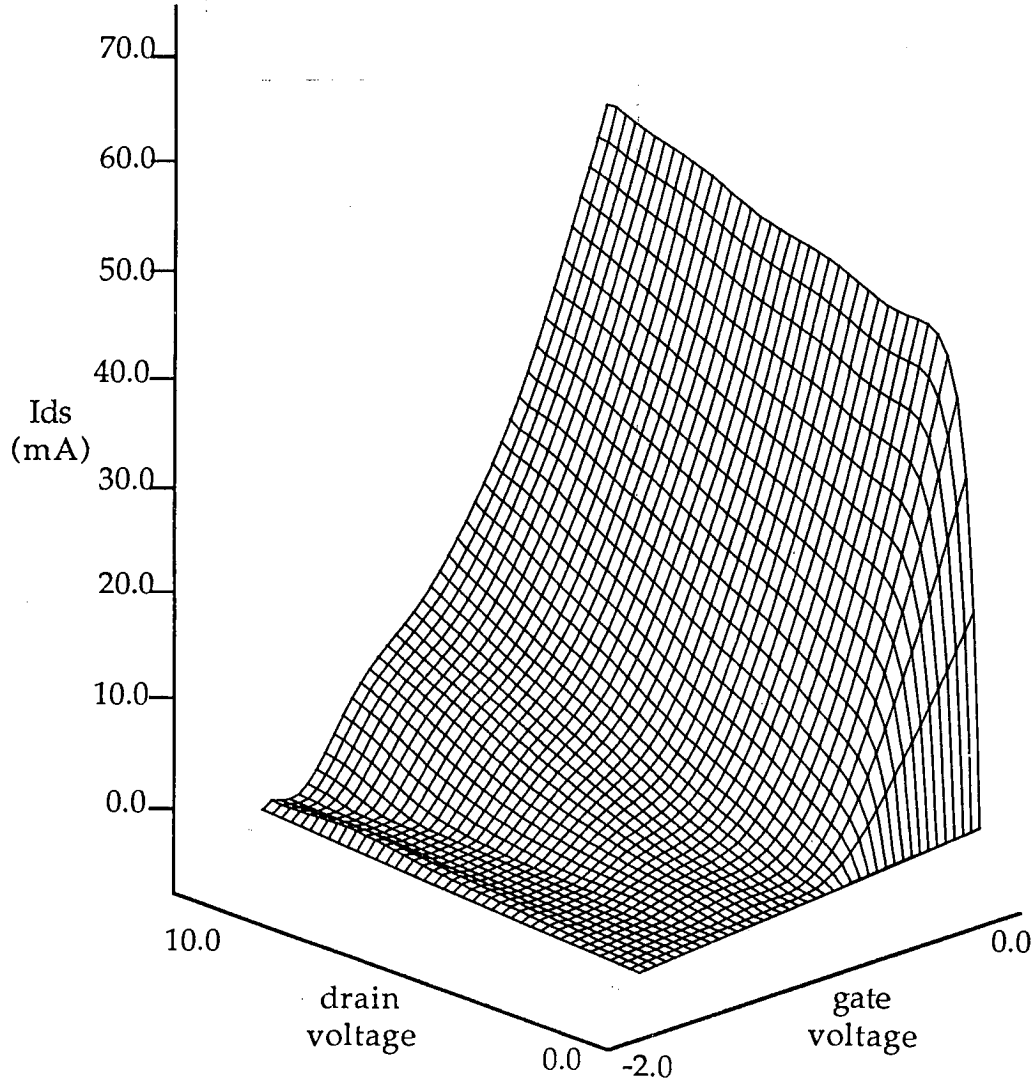


Figure 5.14: Refitted current expression

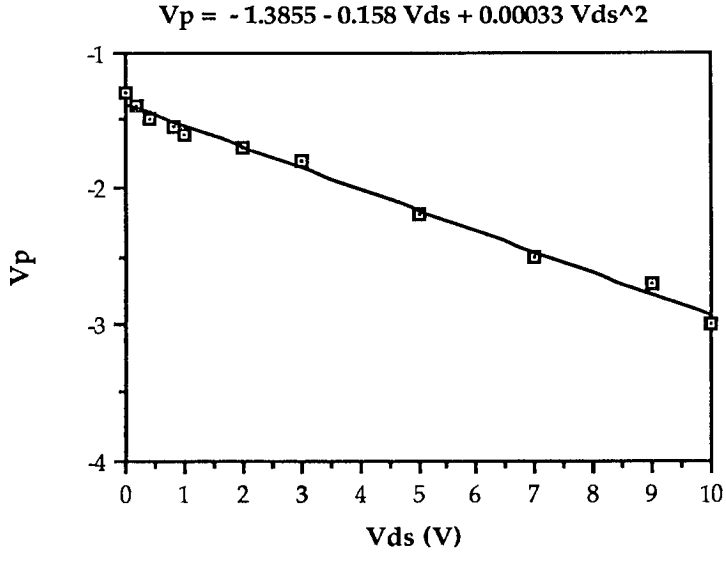


Figure 5.15: The pinchoff voltage as a function of Vds

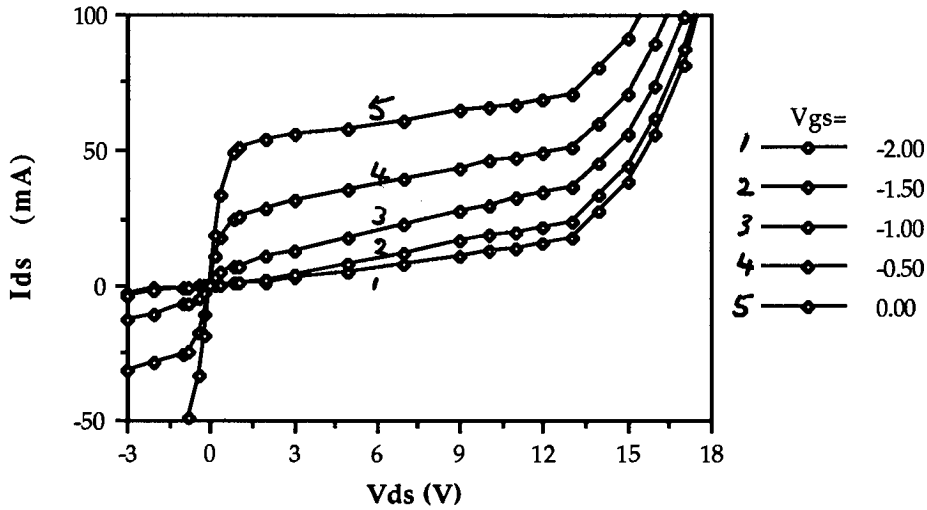


Figure 5.16: The complete current equation

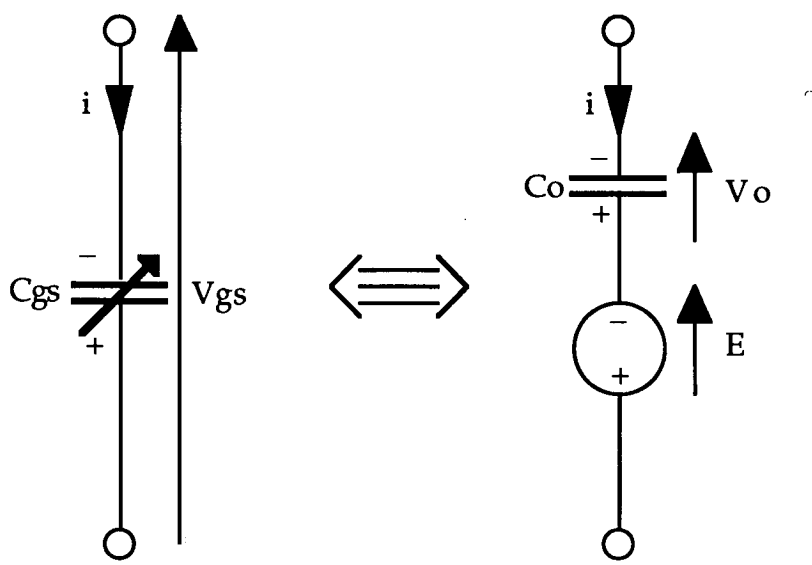


Figure 5.17: The nonlinear gate capacitor in ANAMIC

5.5.3 The Gate-source Capacitance C_{gs}

The gate-source capacitance is the second most important nonlinearity to model in the large-signal simulator. In ANAMIC, it is represented as the charge on the capacitor [43], where

$$i_c = \partial Q/\partial t = (\partial Q/\partial v) \times (\partial v/\partial t) \tag{5.46}$$

The nonlinear capacitor can be expressed [160] as a linear capacitor C_0 in series with a nonlinear voltage source E, as shown in Figure 5.17. Defining nonlinear capacitance in this way improves the computational efficiency of ANAMIC, which uses the state-space approach to circuit simulation. The nonlinear capacitance is expressed as a function of two control voltages and the charge on the capacitor is found by integrating the capacitor with respect to the voltage across it.

$$C_{gs} = F(V_{gs},V_{ds}) \tag{5.47}$$

$$Q_{gs} = \int F(V_{gs},V_{ds})\, \partial V_{gs} = G(V_{gs},V_{ds}) \tag{5.48}$$

The expression for the charge is rearranged, so that the voltage across the capacitor is defined in terms of the charge in the capacitor and the drain voltage.

$$V_{gs} = H(Q_{gs},V_{ds}) \tag{5.49}$$

From Figure 5.17, $V_{gs} = V_0 + E$, where V_{gs} is the voltage across the nonlinear capacitor, V_0 is the voltage across the linear capacitor and E is the nonlinear voltage source. The charge on the capacitor is given as $C_0 \times V_0$ and from (5.49), the total voltage across the capacitor is:

$$V_{gs} = H(C_0 \times V_0,V_{ds}) \tag{5.50}$$

$$E = V_{gs} - V_0 \tag{5.51}$$

$$= H(C_0 \times V_0,V_{ds}) - V_0 \tag{5.52}$$

Therefore, the nonlinear capacitor is described by a linear capacitance and nonlinear voltage source in series. The process of converting the data for the

nonlinear capacitance into the nonlinear voltage source is described below.

The capacitance data was fitted to a fourth order Chebyshev polynomial, in the general form of (5.24). The fit was accomplished to a high degree of accuracy with a total error term of E=1.958, as the gate capacitance surface contains only lower order gradients and curves. The Chebyshev curve was rearranged to become a series of standard polynomials (5.26). The charge on the capacitor was found by integrating the capacitance with respect to the gate voltage. At V_{gs}=0.0 V, the charge on the capacitor would also be zero, since the depletion region containing the charge would have disappeared. A substitution integral similar to equations (5.27-5.32) was performed on the capacitance, producing the charge:

$$\begin{aligned} Q_{gs} = Vg2/2\,[\;& b_{00}x + b_{01}xy + b_{02}xy^2 + b_{03}xy^3 + b_{04}xy^4 \\ & + b_{10}x^2/2 + b_{11}x^2y/2 + b_{12}x^2y^2/2 + b_{13}x^2y^3/2 + b_{14}x^2y^4/2 \\ & + b_{20}x^3/3 + b_{21}x^3y/3 + b_{22}x^3y^2/3 + b_{23}x^3y^3/3 + b_{24}x^3y^4/3 \\ & + b_{30}x^4/4 + b_{31}x^4y/4 + b_{32}x^4y^2/4 + b_{33}x^4y^3/4 + b_{34}x^4y^4/4 \\ & + b_{40}x^5/5 + b_{41}x^5y/5 + b_{42}x^5y^2/5 + b_{43}x^5y^3/5 + b_{44}x^5y^4/5 \\ & + K_0 + K_1y + K_2y^2 + K_3y^3 + K_4y^4\;] \end{aligned} \tag{5.53}$$

Q_{gs}=0.0 C when V_{gs} =0.0 V and x=1. Therefore

$$\begin{aligned} Vg2/2\,[\;& (K_0 + b_{00} + b_{10}/2 + b_{20}/3 + b_{30}/4 + b_{40}/5) + \\ & (K_1 + b_{01} + b_{11}/2 + b_{21}/3 + b_{31}/4 + b_{41}/5)y + \\ & (K_2 + b_{02} + b_{12}/2 + b_{22}/3 + b_{32}/4 + b_{42}/5)y^2 + \\ & (K_3 + b_{03} + b_{13}/2 + b_{23}/3 + b_{33}/4 + b_{43}/5)y^3 + \\ & (K_4 + b_{04} + b_{14}/2 + b_{24}/3 + b_{34}/4 + b_{44}/5)y^4\;] = 0 \end{aligned} \tag{5.54}$$

for all y, and

$$K_0 = -1*(b_{00} + b_{10}/2 + b_{20}/3 + b_{30}/4 + b_{40}/5)$$
$$K_1 = -1*(b_{01} + b_{11}/2 + b_{21}/3 + b_{31}/4 + b_{41}/5)$$
$$K_2 = -1*(b_{02} + b_{12}/2 + b_{22}/3 + b_{32}/4 + b_{42}/5)$$
$$K_3 = -1*(b_{03} + b_{13}/2 + b_{23}/3 + b_{33}/4 + b_{43}/5)$$
$$K_4 = -1*(b_{04} + b_{14}/2 + b_{24}/3 + b_{34}/4 + b_{44}/5) \qquad (5.55)$$

The gate charge was calculated from (5.48) and is illustrated in Figure 5.18. Rather than rearranging this equation to express V_{gs} as a function of Q_{gs} and V_{ds} mathematically, the data was rearranged and refitted so that Q_{gs} and V_{ds} were expressed as a function of V_{gs}. Since the original data had already been smoothed during the first fit, the second fit was completed with a very small error of E=0.350. Figure 5.19 illustrates the surface fits for C_{gs} and $V_{gs}(Q_{gs}, V_{ds})$.

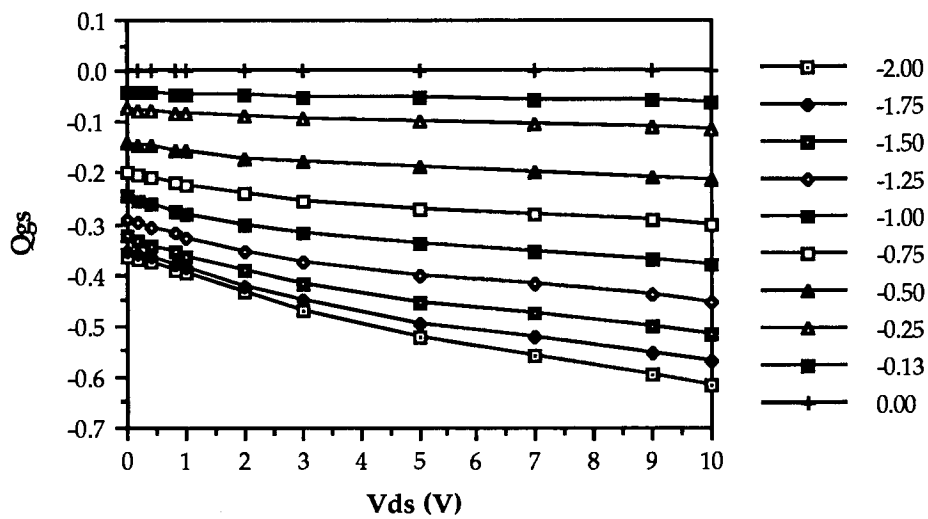


Figure 5.18: The gate charge

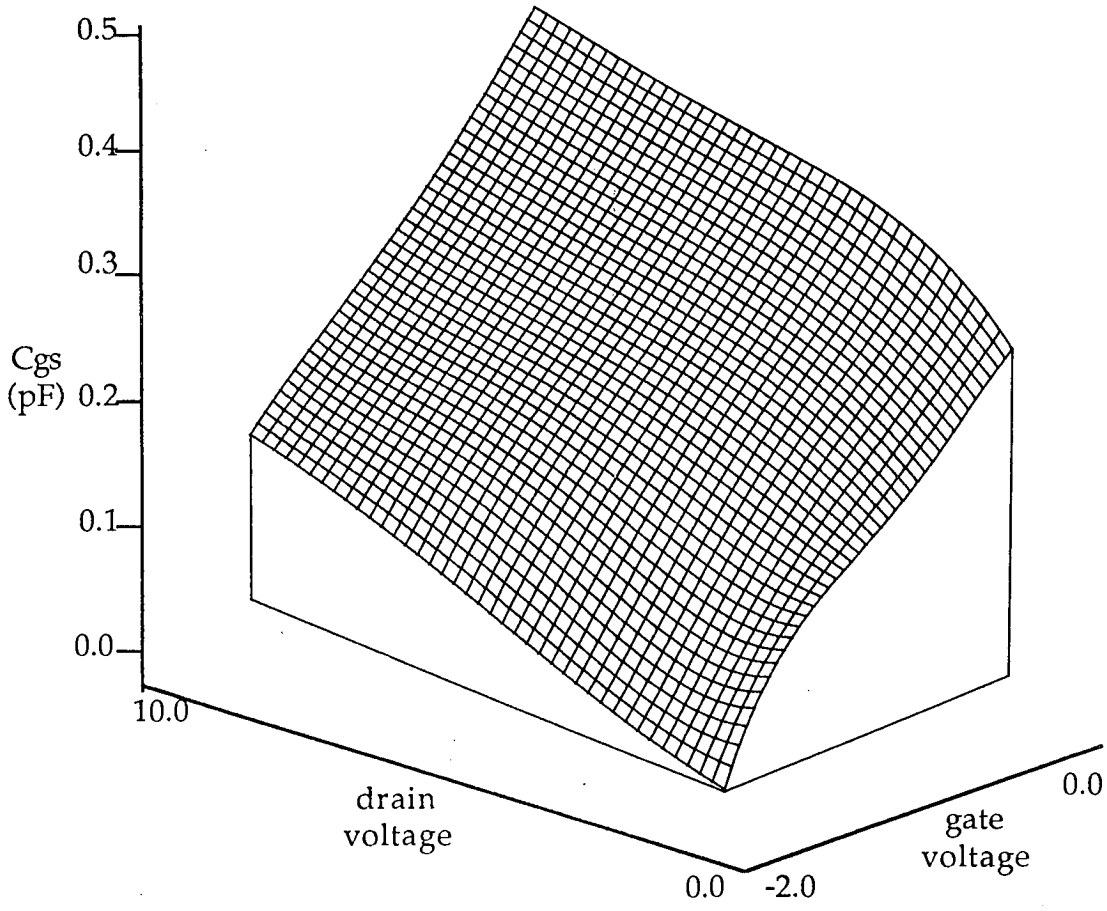


Figure 5.19a: The nonlinear gate-source capacitance

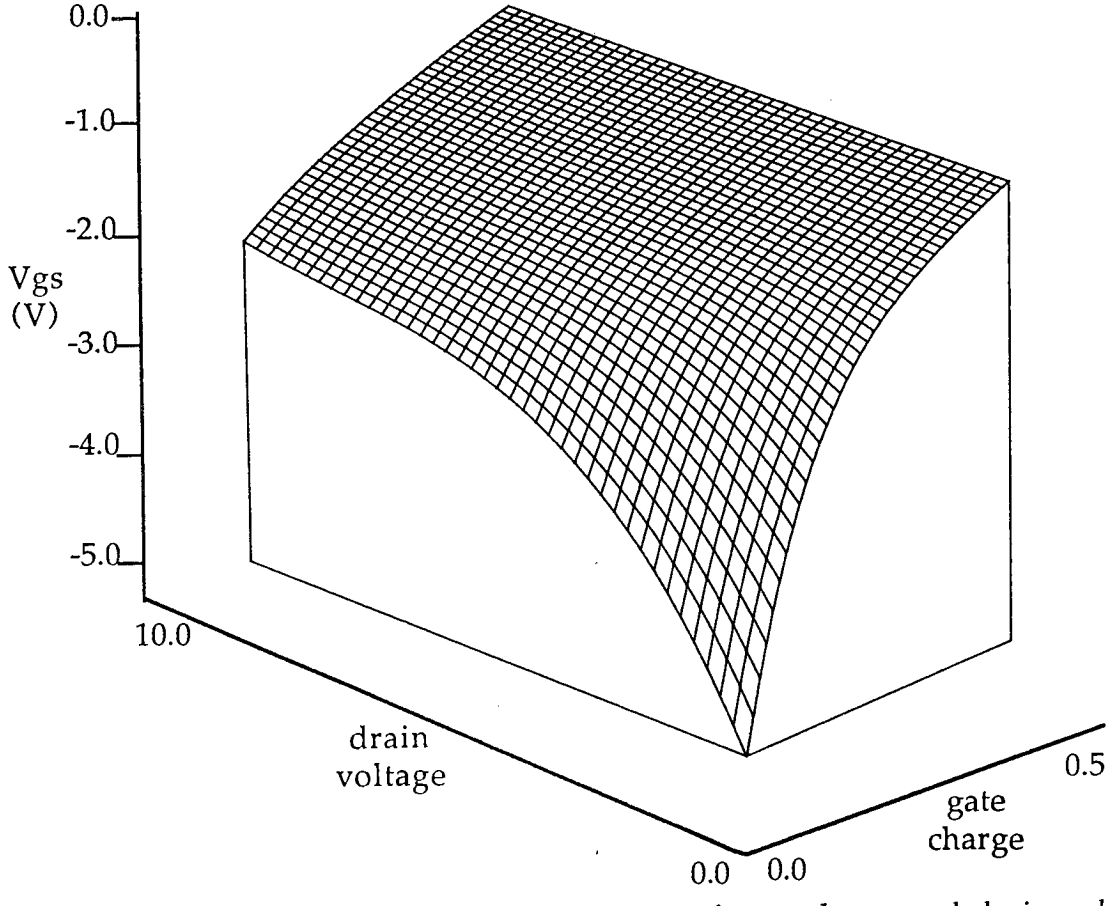


Figure 5.19b: Gate-source voltage as a function of gate charge and drain voltage

The Fortran subroutine which defined the gate capacitance is listed in Appendix C as AFN8. V_{gs0} and V_{ds} are the gate and drain voltages and C_{gs0} is the value of the linear capacitor C_0. The charge on the capacitor is $C_{gs0} \times V_{gs0}$ and the nonlinear voltage source E is equal to $V_g(C_{gs0} \times V_{gs0}, V_{ds}) - V_{gs0}$.

A diode was added in parallel to the nonlinear gate capacitance to simulate the forward gate current. The diode switched on when a voltage of +0.8 V was applied across its terminals and this effectively limited the voltage on the gate capacitance to 0.8 V.

5.5.4 The Drain Capacitance C_{dg}

The small-signal model was less sensitive to the drain capacitance than to either the current or the gate capacitance, although a nonlinear expression for the drain capacitance was still essential for a good large-signal model. The nonlinear drain capacitance, illustrated in Figure 5.20, was implemented in ANAMIC in a similar way to the gate capacitance with a few slight variations.

The capacitance was re-expressed as charge and the charge equation was rearranged so that the voltage on the capacitor was defined in terms of Q_{dg} and V_{gs} (see (5.47) to (5.52)). The charge on the capacitor was defined [161] as the integral of the capacitance with respect to the voltage across the capacitor.

$$C_{dg} = F(V_{gs}, V_{dg}) \tag{5.56}$$

$$Q_{dg} = \int F(V_{gs}, V_{dg})\, \partial V_{dg} = G(V_{gs}, V_{dg}) \tag{5.57}$$

The integral was performed with respect to the drain-gate voltage V_{dg} but the values for the capacitance, calculated from parameter extraction, were given as functions of V_{gs} and V_{ds}. Therefore, the values for C_{dg} were recalculated as functions of V_{gs} and V_{dg}, where $V_{dg} = V_{ds} - V_{gs}$. The variation of C_{dg} with

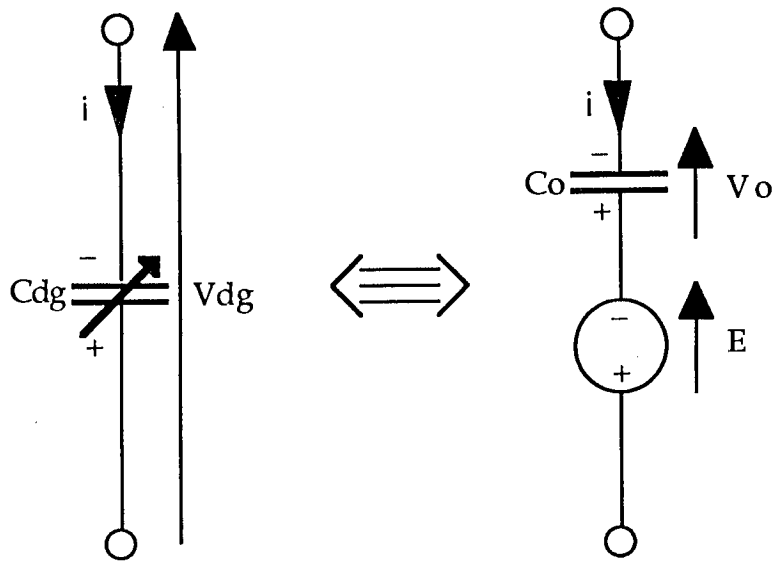


Figure 5.20: The nonlinear drain capacitance in ANAMIC

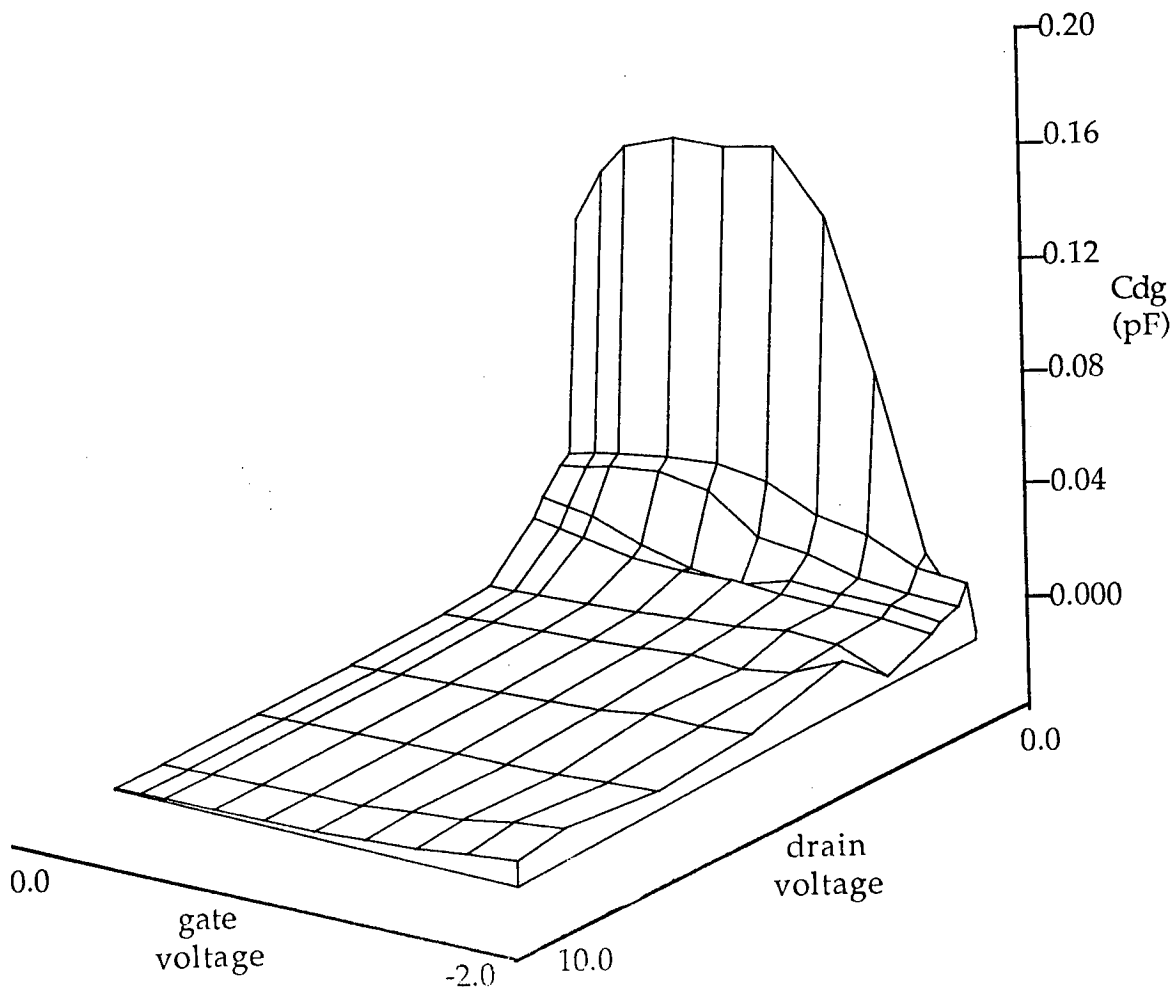


Figure 5.21: The nonlinear gate-drain capacitance

V_{dg} is illustrated in Figure 5.21 which is noticeably different from the plot of C_{dg} against V_{ds} in Figure 4.16.

C_{dg} was fitted to a 4th order Chebyshev function with a total error E of 14.23. The error was higher than for the gate capacitance because the surface defining the drain capacitance contains a steep slope around V_{ds}=0.0 V and V_{gs}=0.0 V. However, the error was not large enough to significantly reduce the accuracy of the large-signal model, since the Chebyshev function was accurate at most other voltage points. For a more accurate function for C_{dg}, MATLAB could be used to numerically integrate the capacitance to calculate charge, which could be surface fitted using a higher order of Chebyshev polynomial.

The charge Q_{dg} on the capacitor was calculated as the integral of C_{dg} with respect to the drain-gate voltage. At V_{ds}=0.0 V, the depletion region relating to C_{dg} disappears and Q_{dg}=0.0 C. A substitution integral was performed on the capacitance, producing the charge:

$$\begin{aligned} Q_{dg} = Vd2/2\,[\; & b_{00}y + b_{01}y^2/2 + b_{02}y^3/3 + b_{03}y^4/4 + b_{04}y^5/5 \\ & + b_{10}xy + b_{11}xy^2/2 + b_{12}xy^3/3 + b_{13}xy^4/4 + b_{14}xy^5/5 \\ & + b_{20}x^2y + b_{21}x^2y^2/2 + b_{22}x^2y^3/3 + b_{23}x^2y^4/4 + b_{24}x^2y^5/5 \\ & + b_{30}x^3y + b_{31}x^3y^2/2 + b_{32}x^3y^3/3 + b_{33}x^3y^4/4 + b_{34}x^3y^5/5 \\ & + b_{40}x^4y + b_{41}x^4y^2/2 + b_{42}x^4y^3/3 + b_{43}x^4y^4/4 + b_{44}x^4y^5/5 \\ & + K_0 + K_1x + K_2x^2 + K_3x^3 + K_4x^4 \;] \end{aligned} \tag{5.58}$$

Q_{dg}=0.0 C when V_{ds}=0.0 V and y=-1. Therefore

$$\begin{aligned} Vd2/2 \quad & [\,(K_0 - b_{00} + b_{01}/2 - b_{02}/3 + b_{03}/4 - b_{04}/5) + \\ & + (K_1 - b_{10} + b_{11}/2 - b_{12}/3 + b_{13}/4 - b_{14}/5)x + \\ & + (K_2 - b_{20} + b_{21}/2 - b_{22}/3 + b_{23}/4 - b_{24}/5)x^2 \\ & + (K_3 - b_{30} + b_{31}/2 - b_{32}/3 + b_{33}/4 - b_{34}/5)x^3 + \\ & + (K_4 - b_{40} + b_{41}/2 - b_{42}/3 + b_{43}/4 - b_{44}/5)x^4\,] = 0 \end{aligned} \tag{5.59}$$

for all x, and

$$K_0 = -1 \times (- b_{00} + b_{01}/2 - b_{02}/3 + b_{03}/4 - b_{04}/5)$$
$$K_1 = -1 \times (- b_{10} + b_{11}/2 - b_{12}/3 + b_{13}/4 - b_{14}/5)$$
$$K_2 = -1 \times (- b_{20} + b_{21}/2 - b_{22}/3 + b_{23}/4 - b_{24}/5)$$
$$K_3 = -1 \times (- b_{30} + b_{31}/2 - b_{32}/3 + b_{33}/4 - b_{34}/5)$$
$$K_4 = -1 \times (- b_{40} + b_{41}/2 - b_{42}/3 + b_{43}/4 - b_{44}/5) \qquad (5.60)$$

The drain charge Q_{dg} is illustrated in Figure 5.22. The expression was rearranged to express V_{dg} as a function of Q_{dg} and V_{gs} in a similar way to the gate capacitance, with a surface fit error E of 0.500. Figure 5.23 illustrates the surface fits for C_{dg} and $V_{dg}(Q_{dg}, V_{gs})$.

The Fortran subroutine defining the drain capacitance is listed in Appendix C as AFN7. V_{gs} + E_{gs} gives the value of the gate voltage and V_{gd} is the gate-drain voltage, which is the inverse of the drain-gate voltage V_{dg}. The inversion of the node voltage resulted from the node voltage definition in ANAMIC, producing the opposite voltage to the voltage which was required. C_{dg0} is the value of the linear capacitor C_0. The charge on the capacitor is $C_{dg0} \times V_{dg}$ and the nonlinear voltage source E is equal to $V_{dg}(C_{dg0} \times V_{dg0}, V_{gs})$ + V_{gd}.

5.5.5 The Intrinsic Resistance Ri

The nonlinear model is least sensitive to changes in the value of the intrinsic resistance and therefore this resistance is the least important nonlinear parameter to model accurately. In ANAMIC, a nonlinear resistor can be described as having either a voltage or current control. In the user-defined library, the value of the resistance is calculated and for the voltage

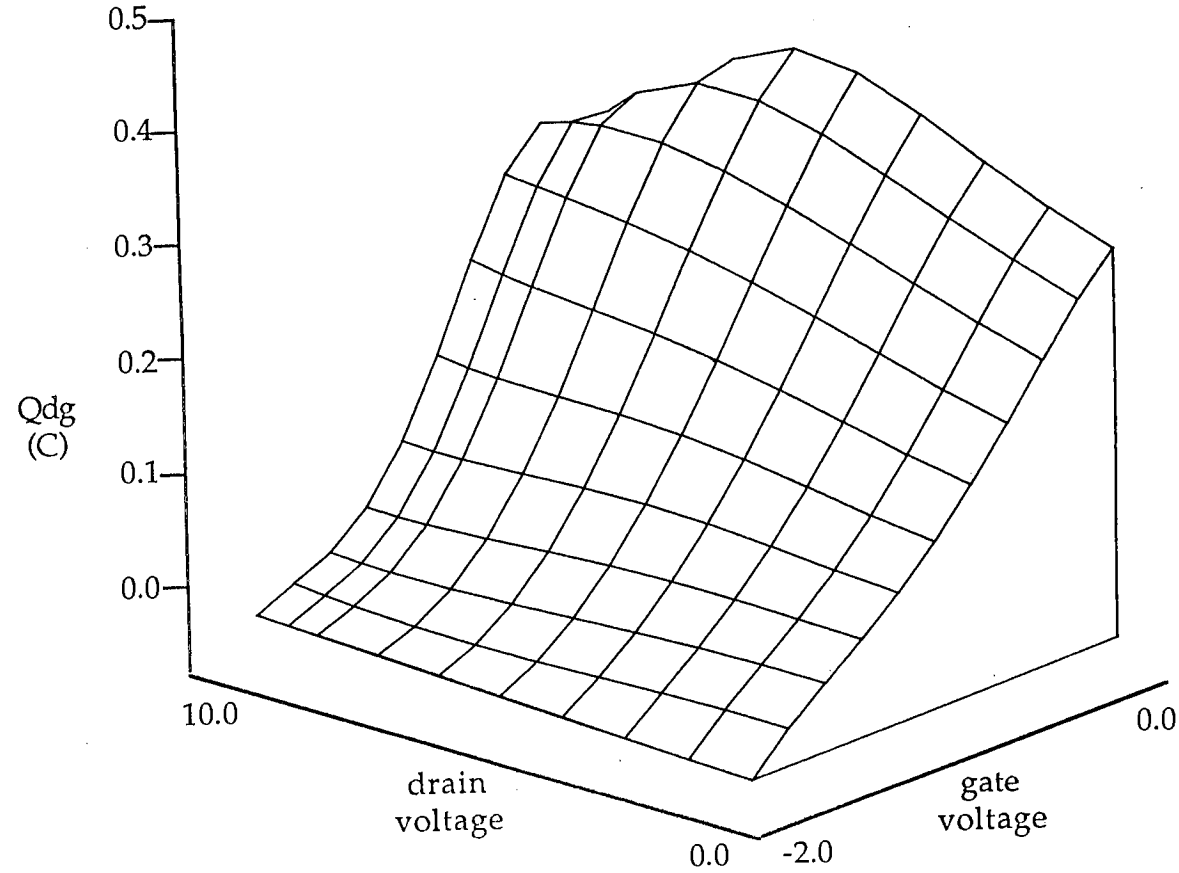


Figure 5.22: The gate-drain charge

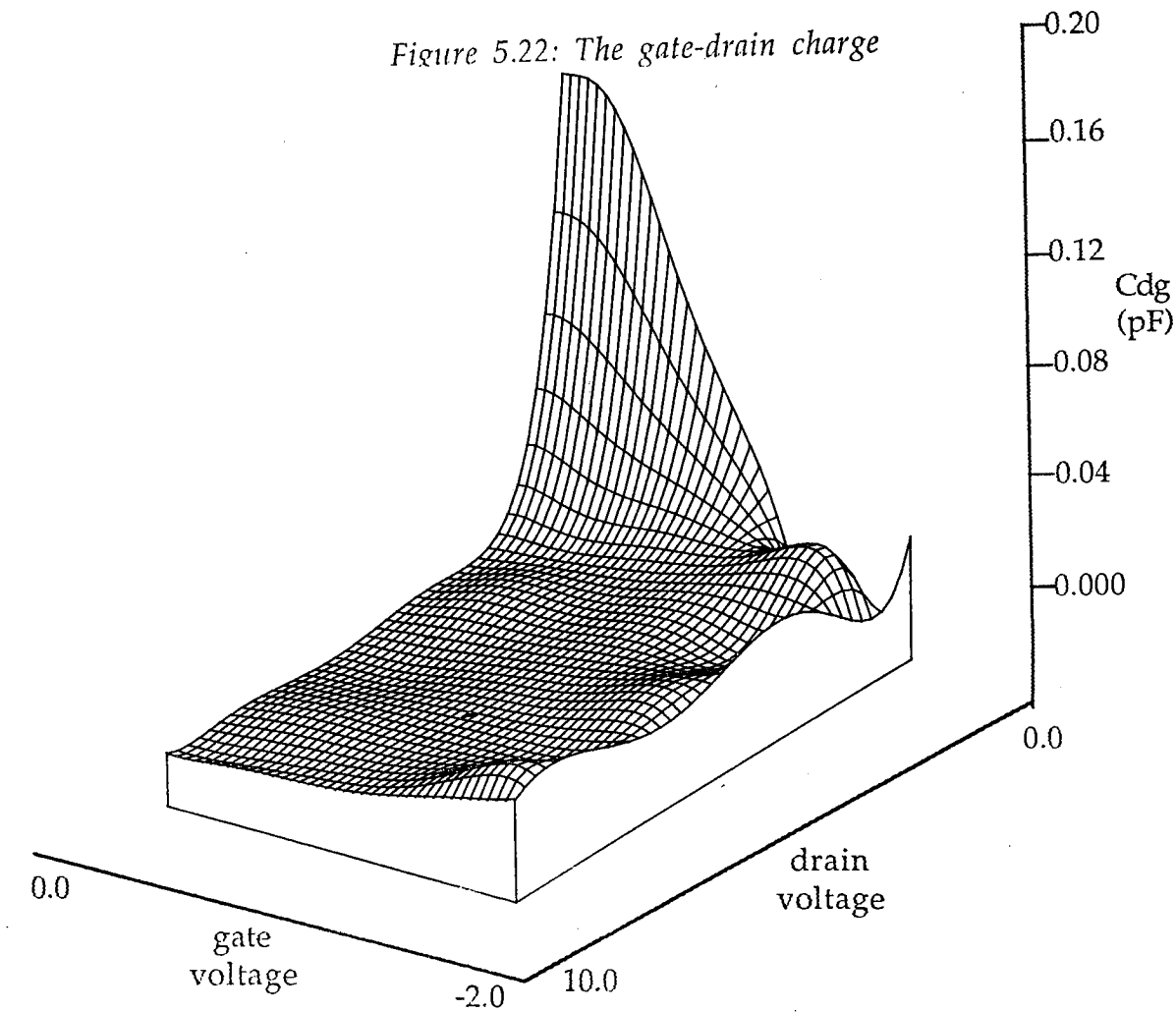


Figure 5.23a: The nonlinear gate-drain capacitance

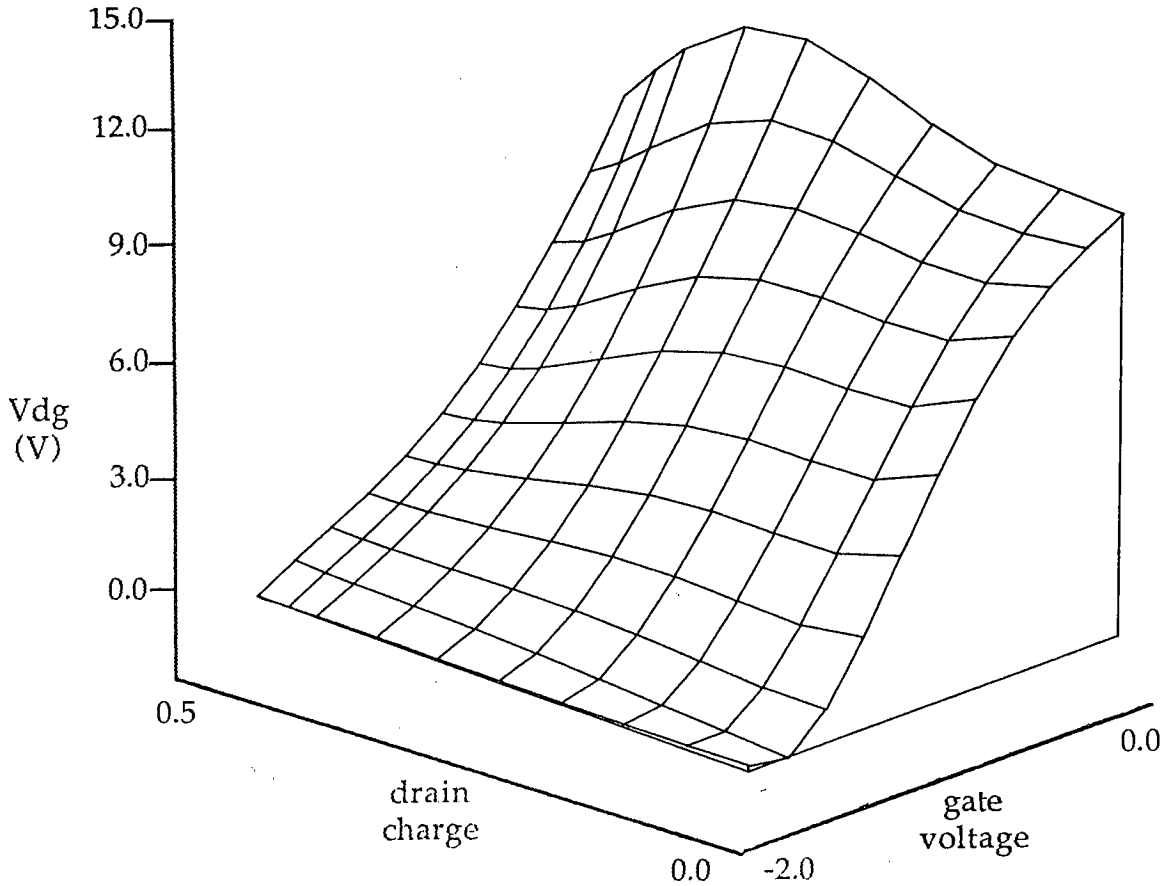


Figure 5.23b: Gate-drain voltage as a function of Qdg and gate voltage

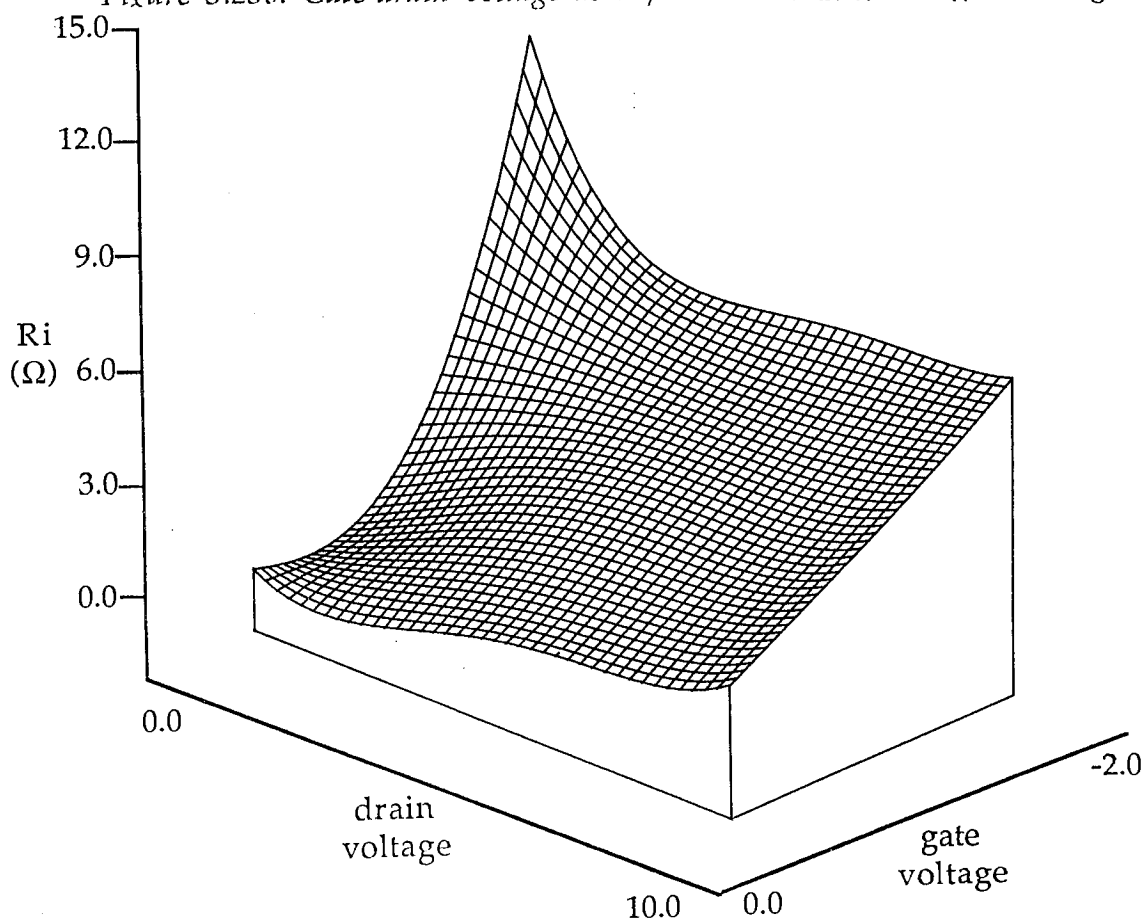


Figure 5.24: Surface fit for the intrinsic resistance

controlled resistance, the nonlinearity is expressed in terms of the current through the resistor where the voltage across the resistor is known. For the current controlled resistor, the nonlinearity is expressed in terms of the voltage across the resistor, where the current is known.

For reasons of stability, the current controlled resistor was chosen to represent the nonlinear resistor. The gate voltage, drain voltage and resistor current were read by the user-defined subroutine. The voltage across the gate was calculated as $I_{Ri} \times R_i$. If the voltage controlled resistor was chosen, then the current would have been calculated from V_{Ri} / R_i and for $R_i \approx 0$, would have produced a simulation error.

The surface of R_i shown in Figure 5.24 was quite smooth and did not contain any sharp curves or humps. A fourth order Chebyshev polynomial was used and the total error E was 5.315 which reflected a good fit, especially for higher drain voltages. For gate and drain voltages outside the boundaries of the measured data, the value for R_i was given as the value at the boundary, and this was done to ensure stability in the nonlinear model. For example, at a given gate voltage, the value for R_i at $V_{ds} > 10.0$ V was equal to the value of R_i at $V_{ds}=10.0$ V. The Fortran subroutine defining R_i is listed in Appendix C as AFN6.

5.5.6 The AC Output Resistor Rx

An important inclusion in this nonlinear model was the resistor R_x, which models the frequency dispersion of the output conductance as a nonlinear resistor, defined by equation (5.17). The differential of the current with respect to the drain voltage was R_{ds}' and the output conductance, calculated from the extraction of S-parameters at a given bias point, was R_{ds}. R_x represented the value of resistor which when placed in parallel with R_{ds}', would create an output impedance, equalling the small-signal R_{ds}. R_{ds}, R_{ds}'

and therefore R_x all varied with gate and drain voltages. The surface for R_x contained many curves and was fitted to a two-dimensional 9th order polynomial with a total error E of 21.30.

The best surface fit was made by fitting the polynomial to G_x ($G_x = 1/R_x$), since it was not important to achieve a good fit for high values of R_x, but instead for low values. Another factor was that as R_x was calculated at high values of bias voltage, a resistance might increase until it suddenly became negative. This indicated that the R_{ds}' was higher than R_{ds} at low bias, and less than R_{ds} at high bias. It was easier to a fit a curve to G_x than to R_x since this conductance did not pass through any points of discontinuity.

R_x was expressed in ANAMIC similar to R_i, i.e. as a current controlled resistor. The Fortran subroutine for R_x is given in Appendix 5.C as AFN10. Figure 5.25 shows three-dimensional plots for G_x calculated for all bias points and the fitted function for G_x. If G_x was found to be zero over the entire bias range, then it could be assumed that the device exhibited no frequency dispersion. The value of G_x was largest for small values of drain bias, where the MESFET channel was fully open, suggesting that frequency dispersion in the output conductance is most in evidence for small gate bias at low drain voltages.

5.6 Conclusions

A method has been proposed in which the nonlinear model can be derived solely from S-parameter measurements. The nonlinear current expression is reconstituted from the transconductance and the output conductance. A resistor and capacitor are added in parallel to the current source in the nonlinear model, to account for the effects of frequency dispersion in the output conductance. It has been shown that the resistor must be nonlinear to define the channel current correctly. It has also been

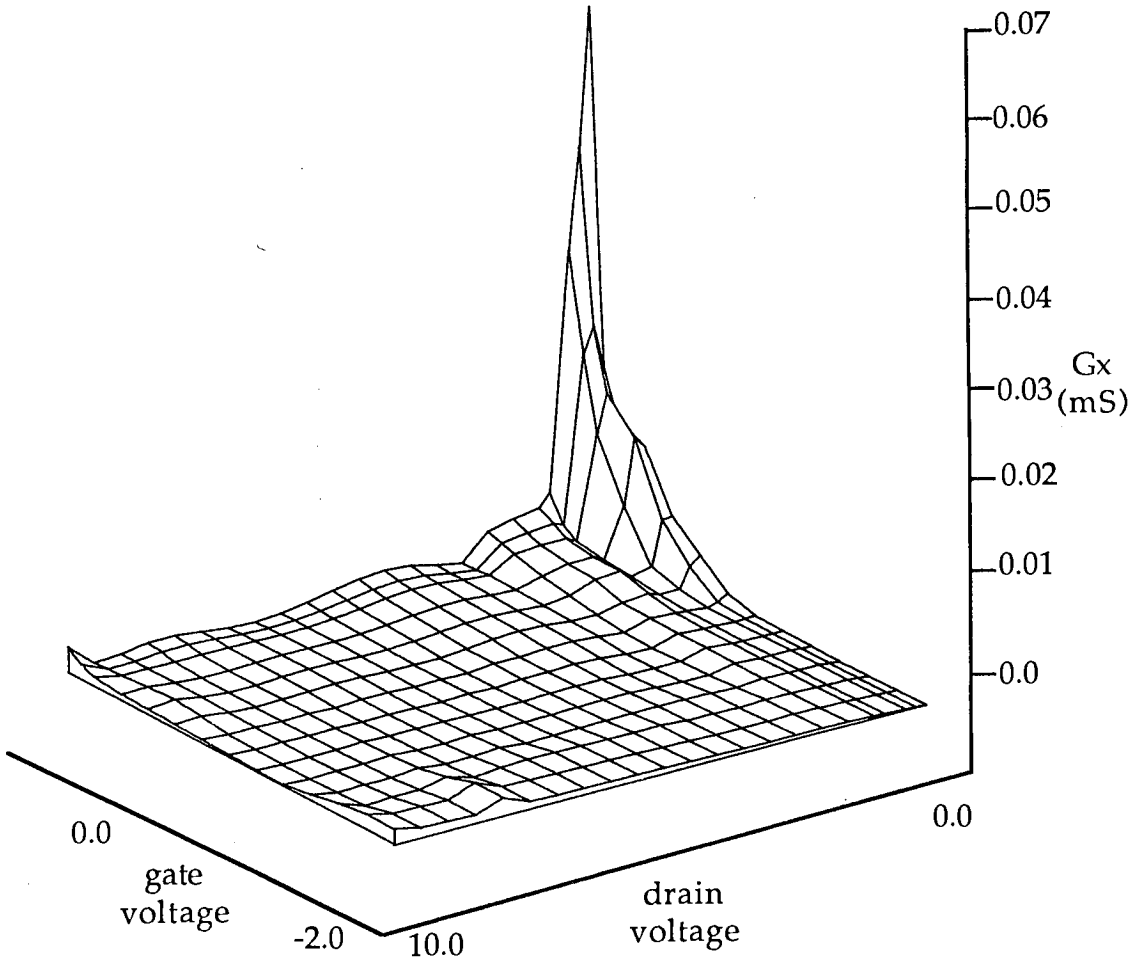


Figure 5.25a: Nonlinear resistance Gx data points

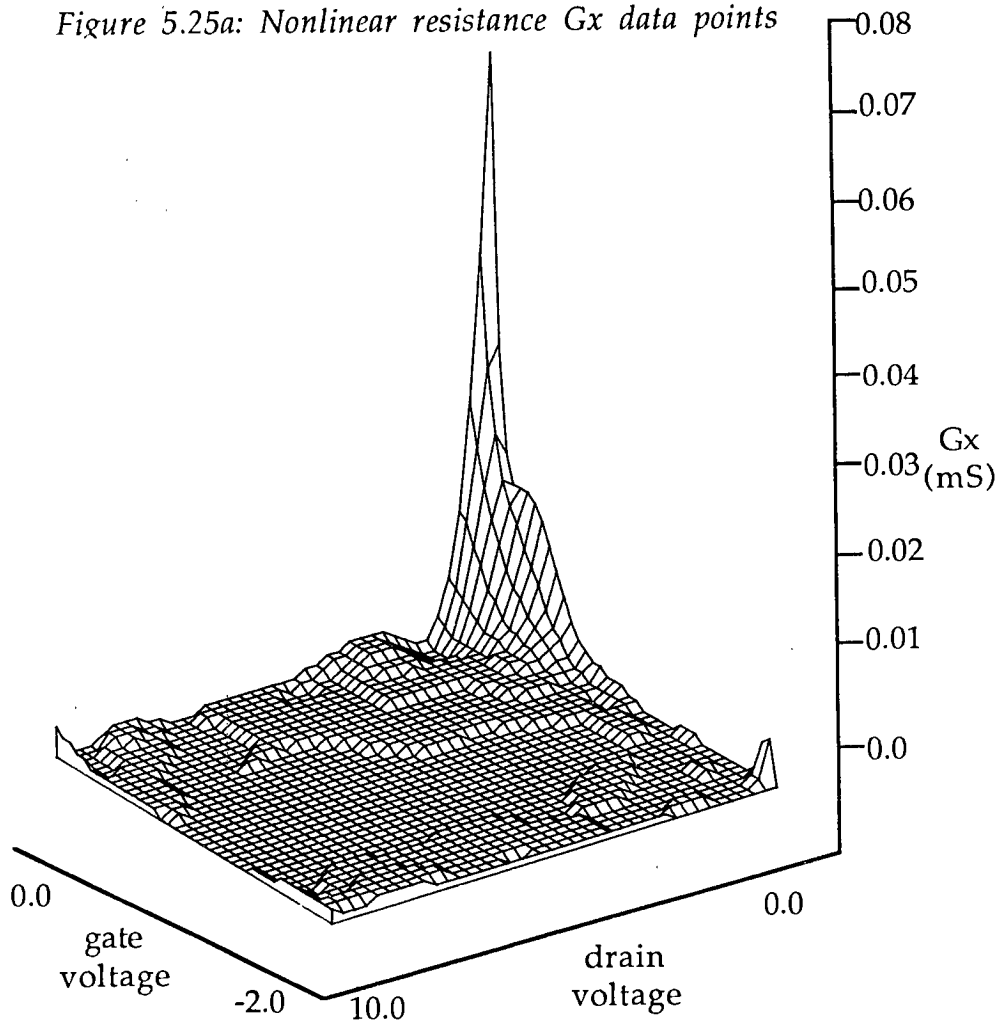


Figure 5.25b: Nonlinear resistance Gx fitted function

shown that this current expression produces a more accurate small-signal response than a current expression derived solely from DC characteristics.

The nonlinear expressions for current, capacitance and resistance were accurately fitted to two-dimensional Chebyshev polynomials. It was shown how easy it is to integrate and differentiate these Chebyshev expressions and find the constants of integration using known boundary conditions. In the next chapter, the nonlinear model will be used in the time-domain program ANAMIC to simulate large-signal circuits and the results of these simulations will be compared with actual measurements.

6.1 Introduction

A new nonlinear model has been proposed which is based solely on S-parameter measurements. The nonlinear model has been installed on a time-domain simulator (ANAMIC), where the nonlinearities of the MESFET are represented by Chebyshev polynomials in Fortran subroutines. In this chapter, the results of linear and nonlinear simulations of circuits containing the modelled GaAs MESFET are compared with experimental measurements of similar circuits.

To facilitate testing the nonlinear model, test MESFETs and MMIC circuits were designed at Thorn-EMI Central Research Laboratories and fabricated on the Plessey F20 MMIC process. The test circuits consisted of MESFETs, with half micron gate lengths and 75, 150, 300 and 450 micron gate widths.

Two single-stage MMIC amplifiers were designed and fabricated. One of the amplifiers (JS1) was externally biased, where bias for the amplifier was designed to be fed directly through the RF ports using bias tees. This type of design reduced the number of circuit components and made circuit simulation more simple. Another amplifier was designed, containing bias circuitry (JS2) as this type of configuration is more representative of a typical MMIC. Power measurements were made of both amplifiers, over a range of frequencies, biases and input power levels and corresponding simulated results were calculated. Additional 'load-pull' measurements were made of the test FETs, and these results were also compared with ANAMIC simulations. Photographs of the F20 amplifier designs for JS1 and JS2, which were included on the MMIC mask, are illustrated in Figure 6.1.

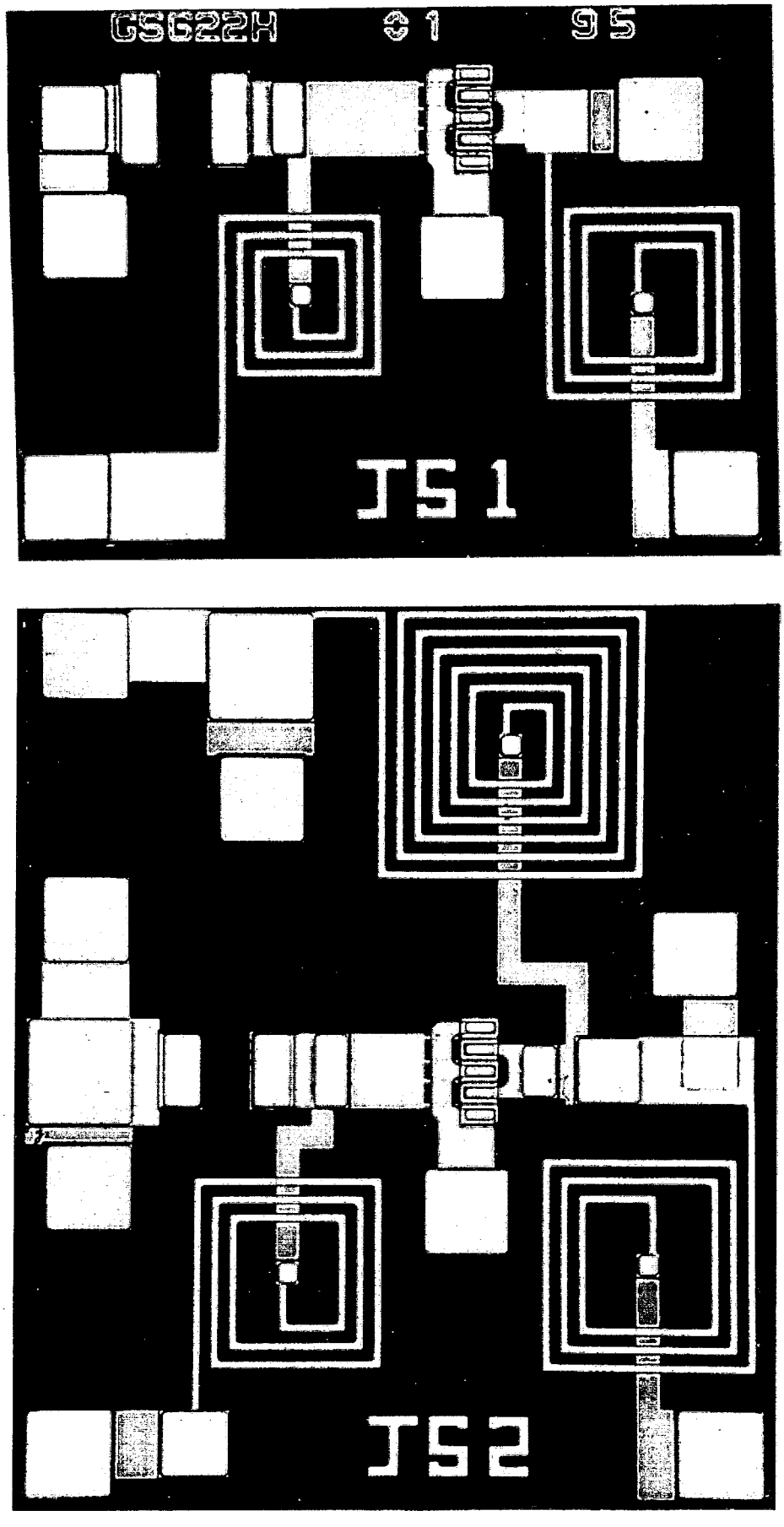


Figure 6.1: Photographs of the single-stage amplifiers JS1 and JS2

6.2 S-Parameter Measurements on Test FETs

S-parameter measurements were made of the test MESFETs, in order to derive the large-signal model using the methods proposed in this work. Two sources of test FET measurements were available: initially TRL measurements were used (measured at Thorn-EMI CRL) and, later in the work, wafer-probed measurements were supplied (by GEC Plessey Research (Caswell) Ltd.). The Plessey measurements were made over a wider frequency band than the TRL measurements and contained fewer inaccuracies introduced by experimental and TRL deembedding techniques. These were therefore better for the development of the model and were chosen to construct the final nonlinear model, using the techniques detailed in Chapters Four and Five.

In Figure 6.2, five sets of wafer-probed S-parameter measurements are shown. Each set was measured at a different bias point, and over the frequency range of 1.0-21.0 GHz. The five bias points are at V_{ds}=9.0 V for 100% and 10% I_{dss}, V_{ds}=2.0 V for 100% and 10% I_{dss} and V_{ds}=5.0 V for 50% I_{dss}. Plotted with each curve are the simulated S-parameter measurements of the derived equivalent circuits. Generally, the fit between the measurements and the model is excellent, especially at low frequencies. The agreement for both the magnitude and phase of S21 is almost perfect at all of the bias points. The fit for S11 and S22 is best at lower values of I_{ds}, and the fit is quite good for I_{ds} = 100% I_{dss}, the bias point at which a negative drain resistance would improve the fit, as discussed in Chapter Four. The fit for S12 was the most difficult to achieve, although it was quite reasonable for all of the bias points.

Figure 6.3 illustrates the S-parameters and equivalent circuit simulations at three bias points made from TRL measurements at Thorn-EMI. The bias points are at V_{ds}=2.2, 4.5, 8.5 V with V_{gs}=-1.0, -0.7 and 0.0 V.

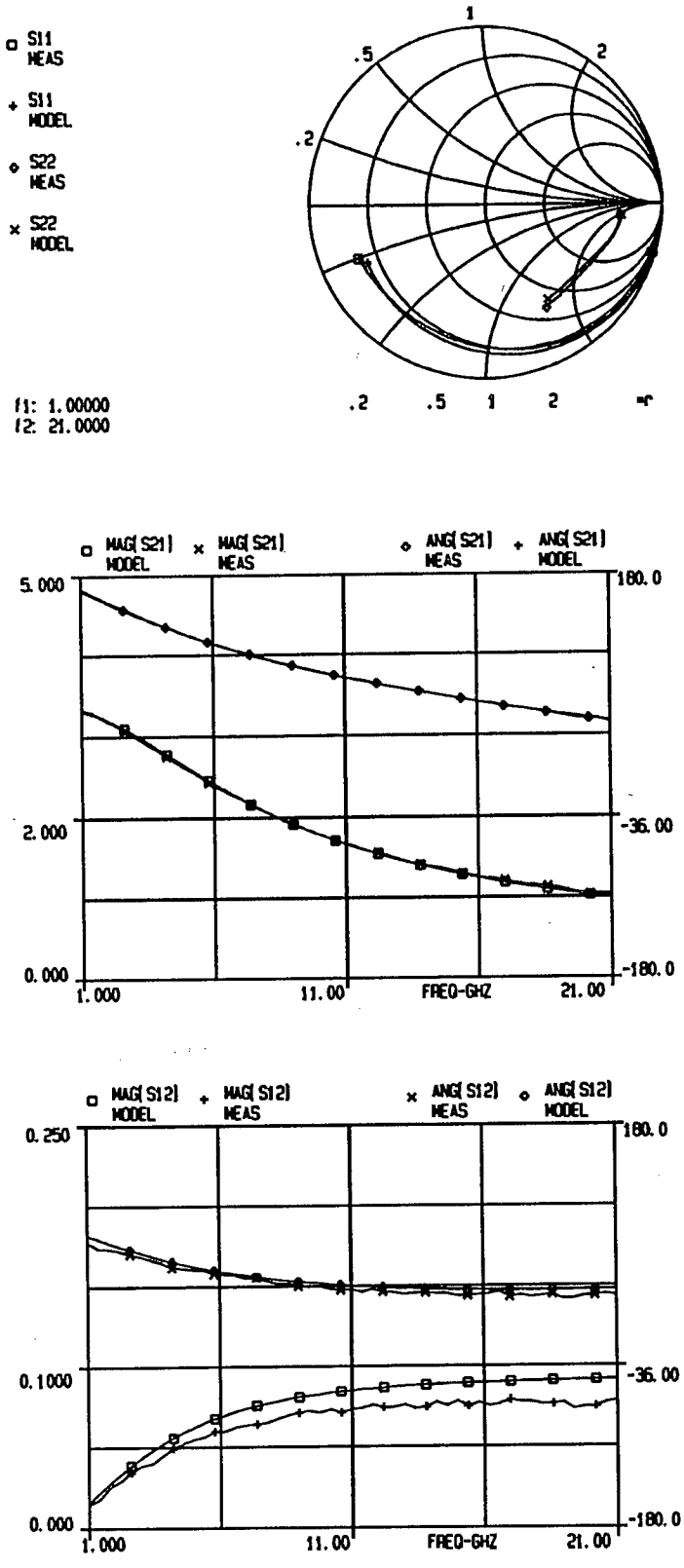


Figure 6.2a: Model and wafer-probed measurements at V_{ds}=9.0V, 100%I_{dss}

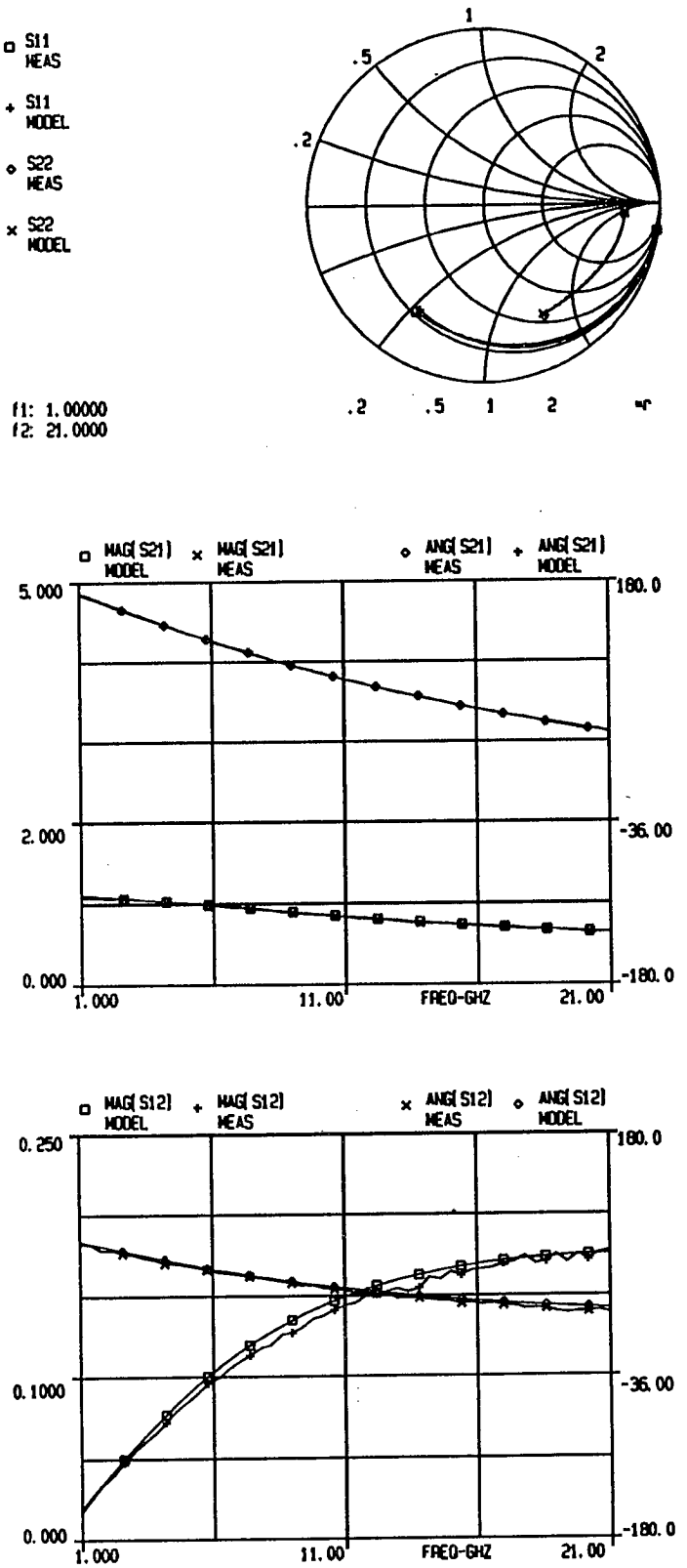


Figure 6.2b: Model and wafer-probed measurements at V_{ds}=9.0V, 10%I_{dss}

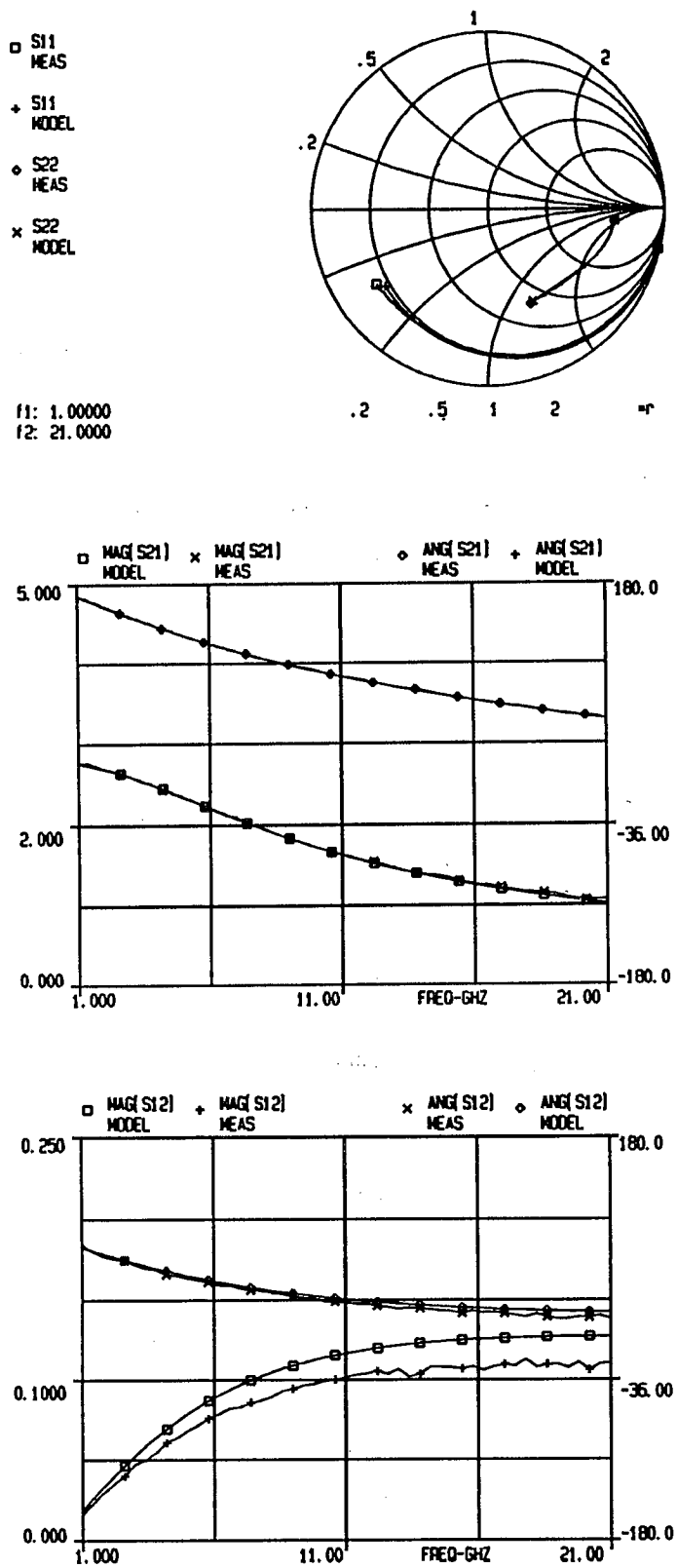


Figure 6.2c: Model and wafer-probed measurements at V_{ds}=5.0V, 50%I_{dss}

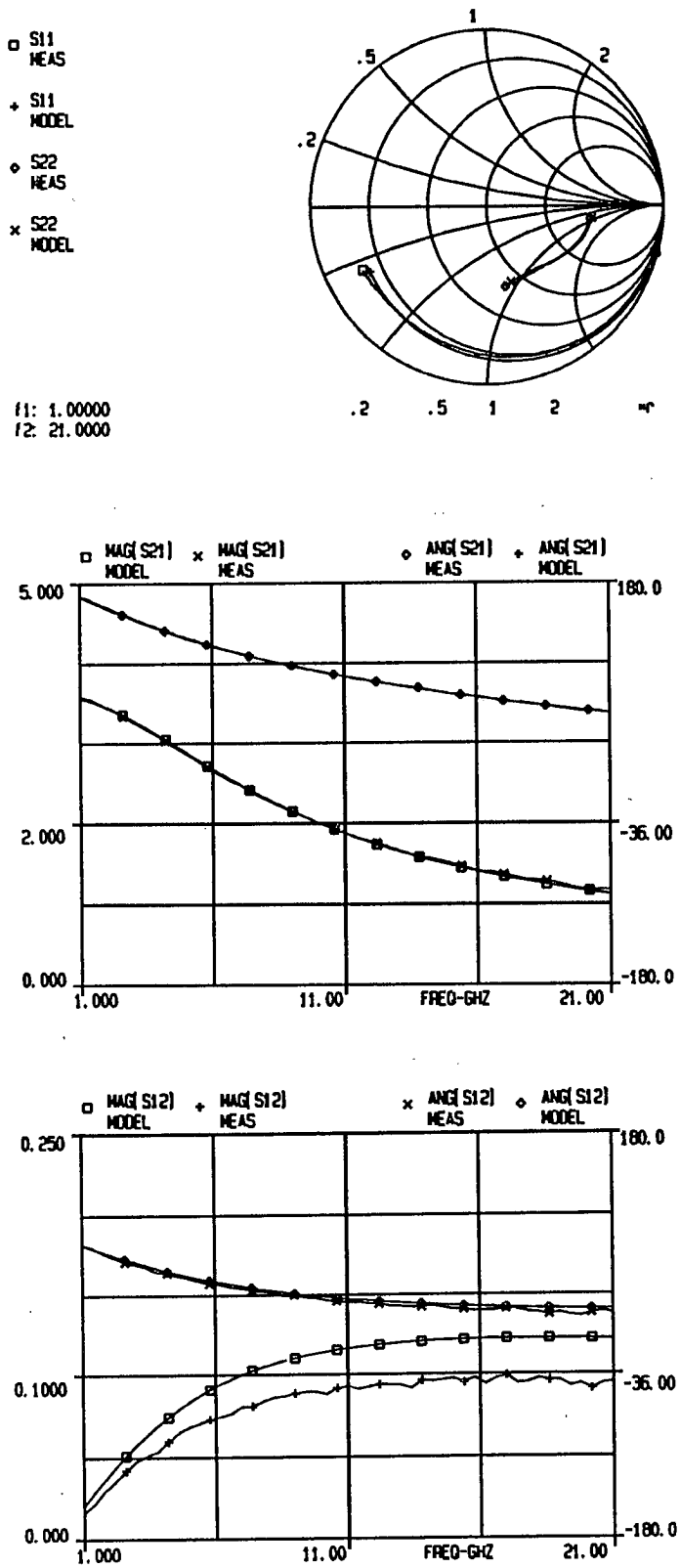


Figure 6.2d: Model and wafer-probed measurements at V_{ds}=2.0V, 100%I_{dss}

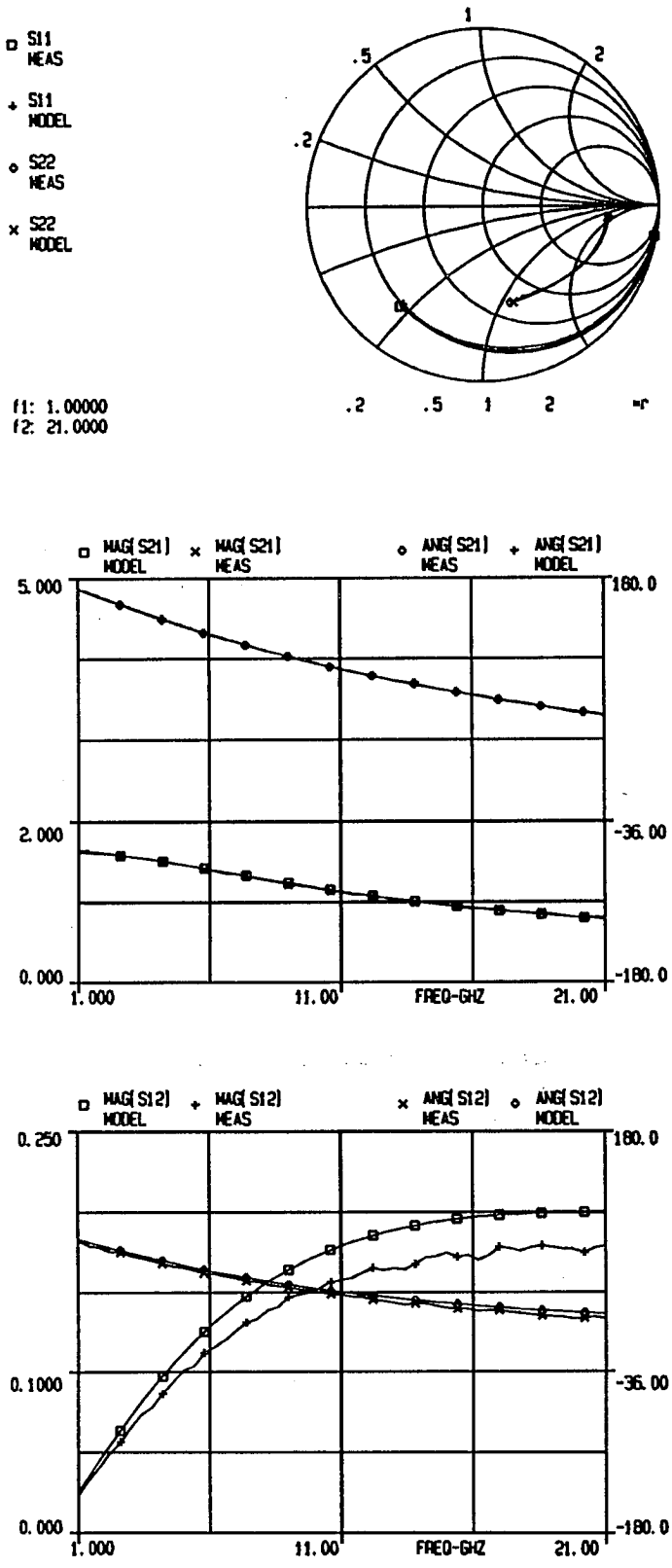
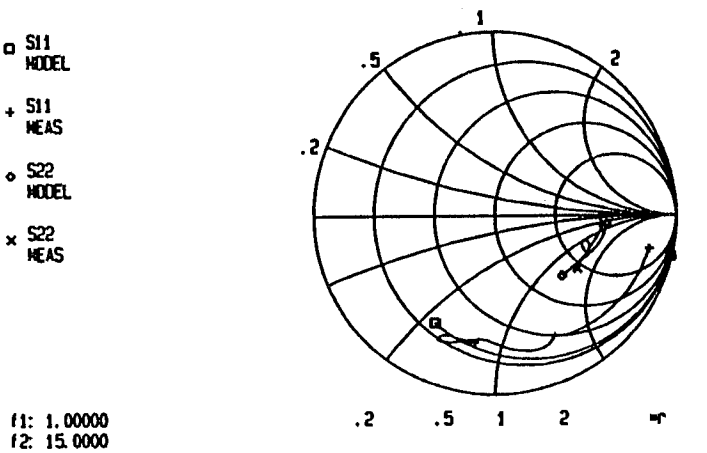
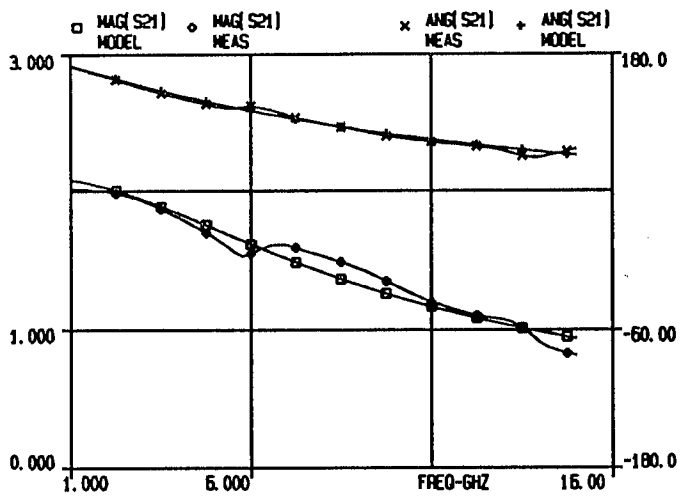


Figure 6.2e: Model and wafer-probed measurements at V_{ds}=2.0V, 10%I_{dss}





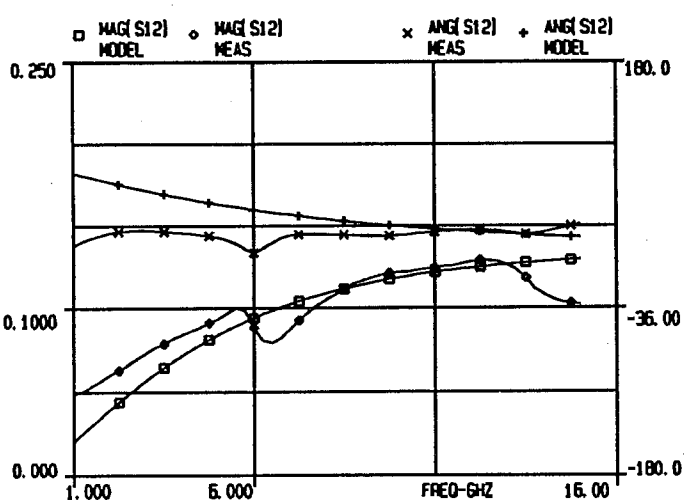


Figure 6.3a: Model and TRL measurements at Vgs=-1.0V and Vds=2.2V

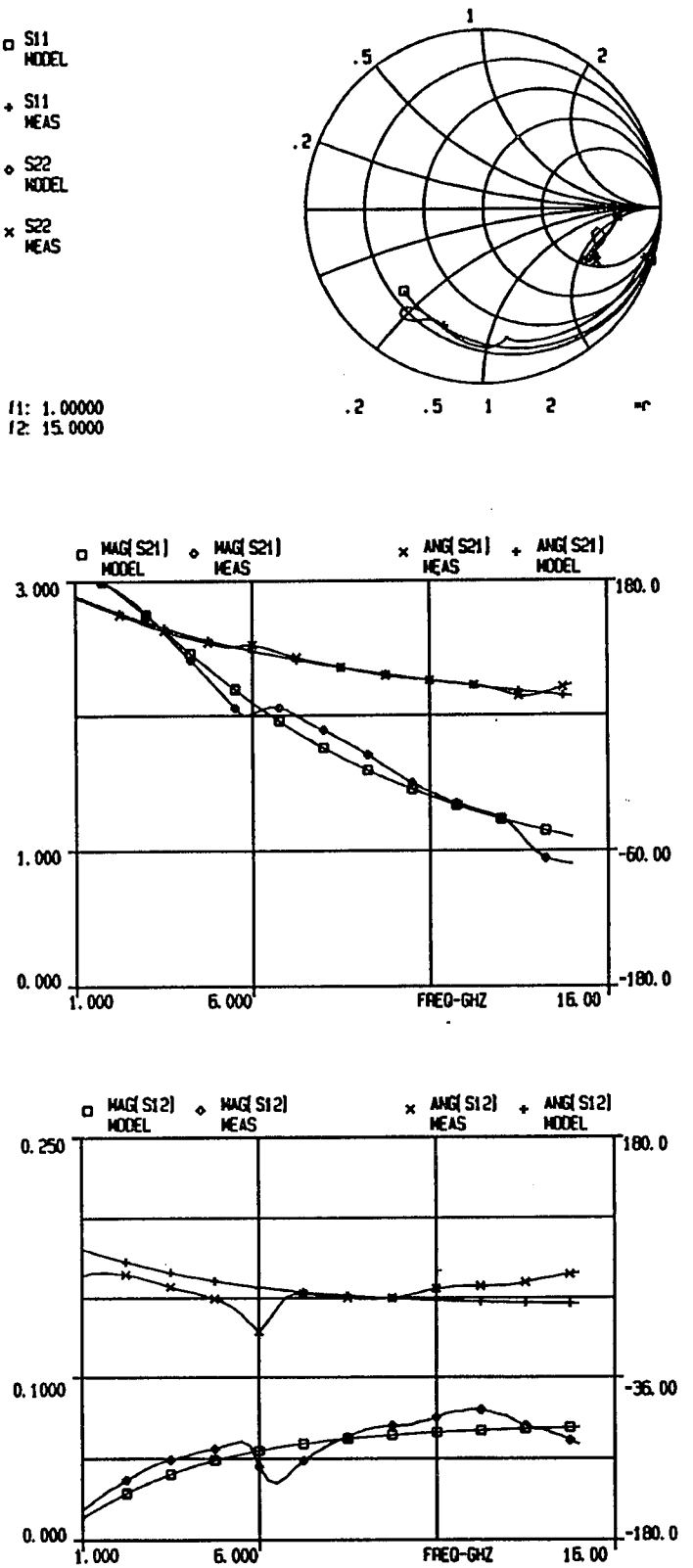
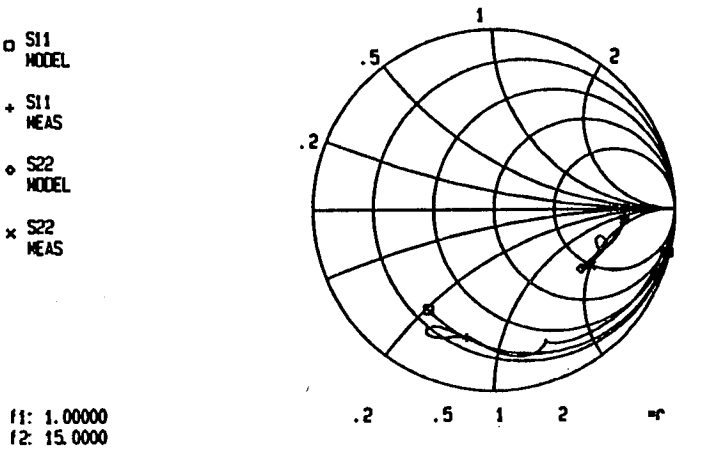
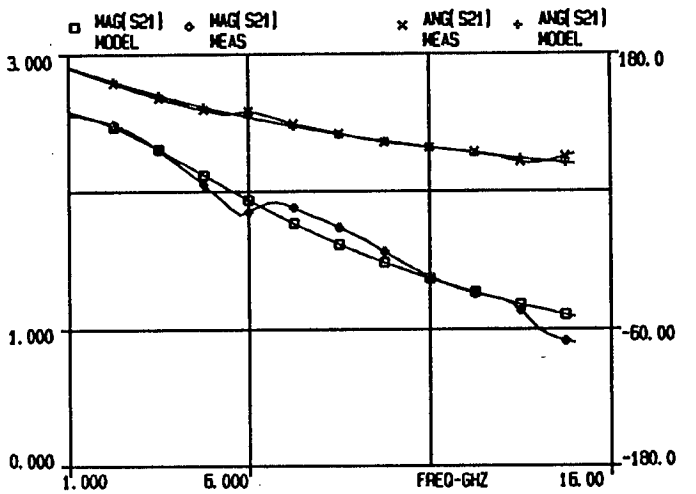


Figure 6.3b: Model and TRL measurements at Vgs=-0.0V and Vds=8.5V





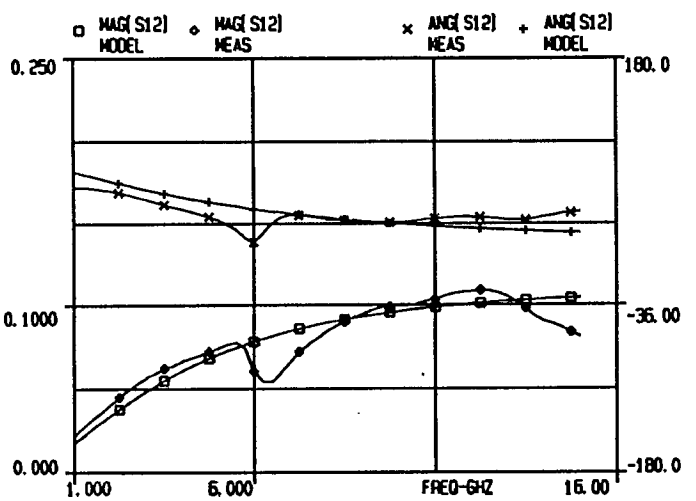


Figure 6.3c: Model and TRL measurements at Vgs=-0.7V and Vds=4.5V

These results are inferior to the wafer-probed measurements and the resonances at approximately 6.8 GHz and 14.0 GHz were probably caused by resonances in the Thorn microstrip test jig (see Chapter Three).

The models extracted from the two sets of measurements were similar and small differences, particularly in the transconductance and gate capacitance, could be attributed as much to the different fabrication batches which the two sets of test FETs were made as to measurement errors in the TRL calibration. The extracted models for the test MESFETs were used to derive the nonlinear model using the procedures outlined in the previous chapters.

6.3 Externally biased, Single-stage Amplifier JS1

6.3.1 Design, Layout and Small-signal Characteristics

Single-stage MMIC amplifiers were fabricated, consisting of a 300 micron MESFET matched at the input and output. The purpose of building these amplifiers was to verify the nonlinear model by comparing nonlinear measurements of the MMICs with simulations of the same circuit.

A diagram of the self-biased, single-stage amplifier JS1 is shown in Figure 6.4. It comprises a 300 micron gate width F20 MESFET (4*75) with input and output matching networks. The series components of both networks are inductive, allowing the bias to be fed directly through the RF ports. The input circuit consists of a resistor, capacitor and inductor and the output circuit consists of a capacitor and inductor. The small-signal characteristics were modelled before fabrication using TOUCHSTONE, and the values of the passive components were optimized to produce the best performance over the frequency span of 4.0-6.0 GHz. Parasitics for the passive components, vias and bondpads, also shown in Figure 6.4, were

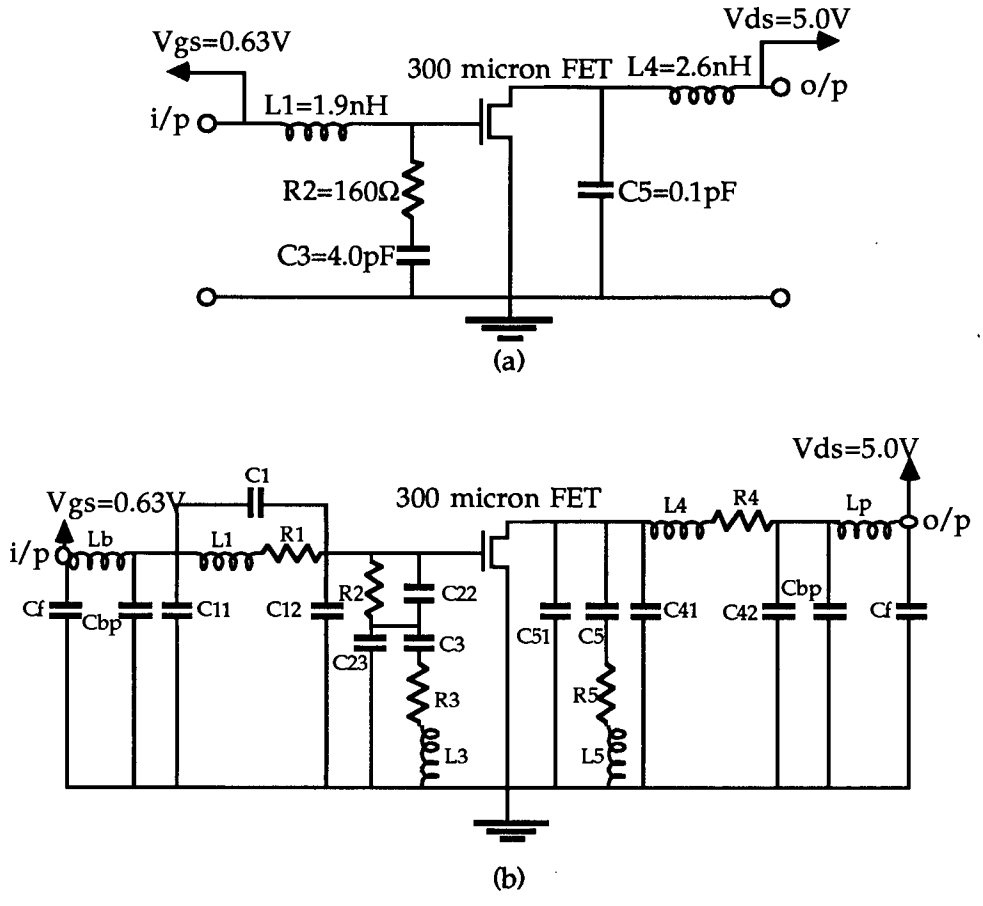


Figure 6.4: Self-biased, single-stage amplifier JS1

(a) without parasitics, (b) with parasitics

added to the small-signal model and the values for these were found in accordance with the Plessey design rules.

The amplifier MMICs were designed to fit into the same package and use the same bondpad arrangement as the 'on-chip' calibration standards, allowing accurate circuit calibration to be made. The amplifier was cut from the fabricated wafer set and mounted on the same type of package used for on-chip calibration (see Chapter Three). Care was taken to

ensure that the bondwires were of similar length to the bondwires on the calibration package and that the chip was situated symmetrically in the middle of the package.

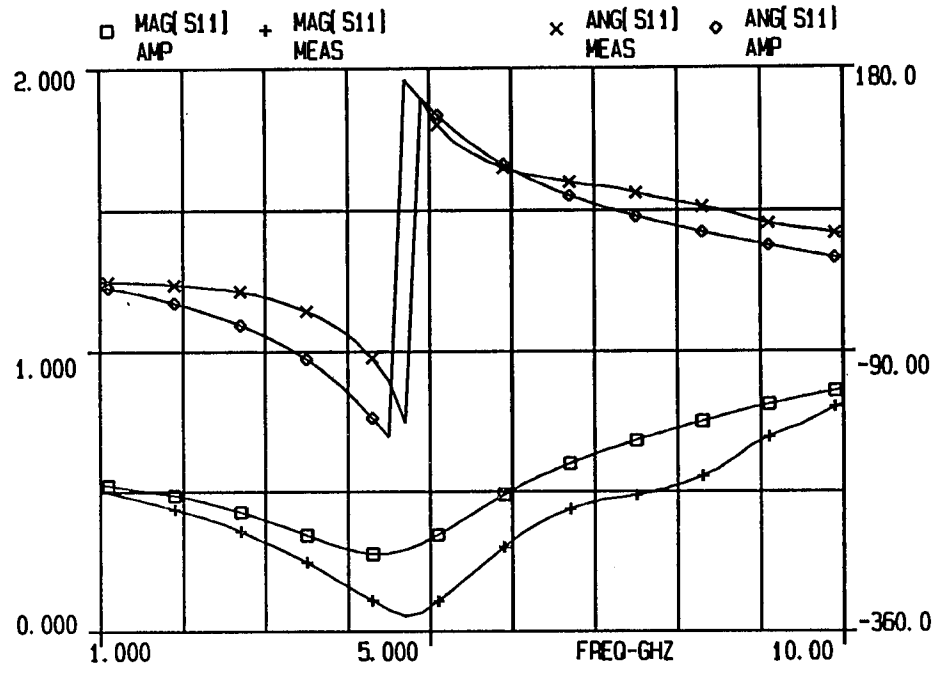
In order to assess how accurately the design had been fabricated, a series of small-signal S-parameter measurements were made of the amplifier over the range 1.0-10.0 GHz. The initial design was made using S-parameter data for an F20 FET at I_{ds} = 50% I_{dss} (V_{gs}=-0.63 V) and V_{ds} = 5.0 V. Therefore the bias was carefully set at V_{gs}=-0.63 V and V_{ds}=5.0 V and it was noted that at V_{gs}=-0.63 V, I_{ds} was 56% I_{dss}. For I_{ds} = 50% I_{dss}, V_{gs} had to be reduced to -0.8 V.

The S-parameter results from the 8510 VNA were stored on an IBM-PC using the HP-IB controller and compared to the original design data in Figure 6.5. The phase response for the measured amplifier agrees well with the design for all of the S-parameters. For S11, the input reflection coefficient is slightly lower than predicted and for S22, the reflection coefficient is slightly higher.

The largest and most significant discrepancy can be seen in the gain response of the amplifier. The measured results are almost uniformly 2.0dB less than the design predictions and can be attributed to one of three types of error:

(1) different characteristics between the FET in the fabricated JS1, and the FET used to model the original design. From DC measurements, Idss for the FET in JS1 is 37.3mA and Idss for the FET in the original design is 47.0mA, indicating a significant difference.

(2) tolerances for passive components. In the Plessey rules, passive



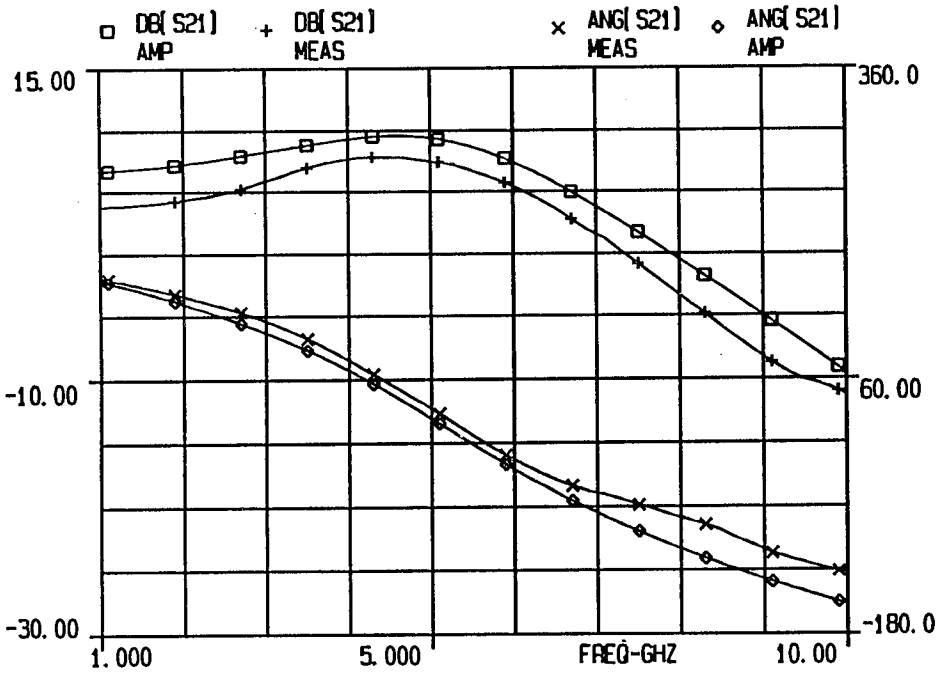
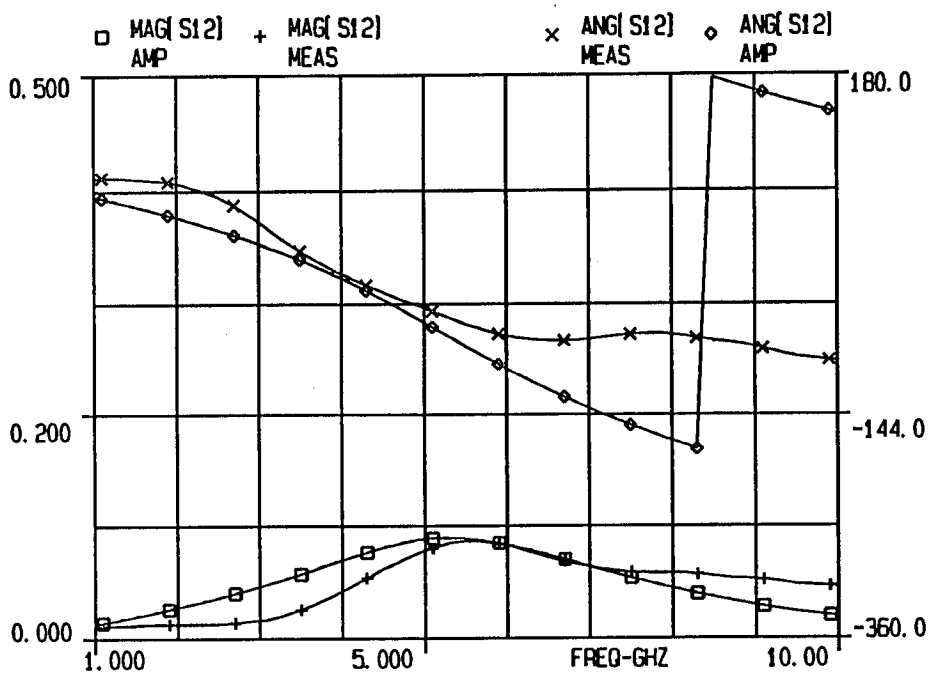


Figure 6.5a: S11, S21 measurements and original model for JS1



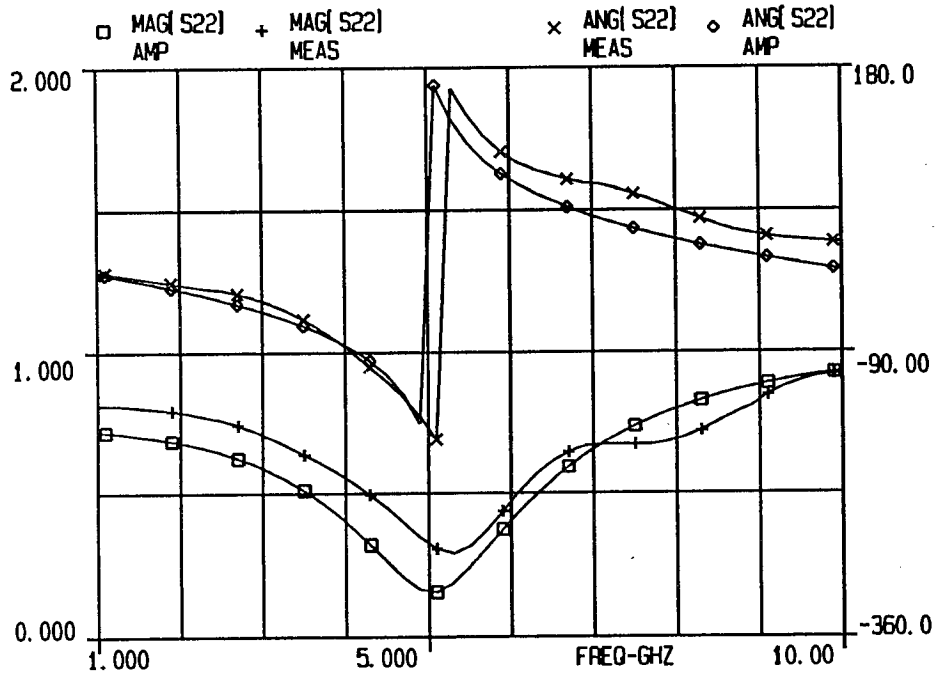


Figure 6.5b: S12, S22 measurements and original model for JS1

components are accurate to within 10%.

(3) Possible small measurement inaccuracies caused by network analyser, calibration etc.

(4) Incorrect estimation of parasitics for passive elements in the design.

Since (1) indicates a 20% difference between the DC characteristics of the measurements and the model, it is likely to be larger than either (2), (3) or (4). The possible effects of (2) and (4) were investigated by allowing the main circuit elements to vary by +/- 10% and the parasitics to vary freely, within realistic limits. The model was reoptimized to fit the measurements and the results of the optimization are shown in Figure 6.6.

Element	Original Values	Optimized Values	Element	Original Values	Optimized Values
L1	1.90	1.78	C12	0.04	0.04
R2	160	133	C22	0.05	0.05
C3	4.00	5.20	C23	0.14	0.14
L4	2.60	2.64	R3	0.50	0.50
C5	0.10	0.11	L3	0.01	0.01
Cf	0.02	0.02	C51	0.01	0.01
Lb	0.18	0.23	R5	1.00	0.87
Cbp	0.06	0.06	L5	0.02	0.02
C1	0.03	0.03	R4	2.20	2.13
R1	2.00	7.41	C41	0.06	0.02
C11	0.06	0.03	C42	0.04	0.07

Figure 6.6: Optimization of values in small-signal model

The fits of S11, S12 and S22 remain quite good and the difference in gain between the model and the measurements has been reduced from 2.0 dB to 0.2 dB, although this value varies with frequency. Figure 6.7 shows how the values of the elements in JS1 changed to improve the small-signal fit.

6.3.2 Power Saturation Curves for Single-stage Amplifier JS1

The nonlinear behaviour of the amplifier JS1 was characterized using power saturation measurements. The output power response was recorded for a number of input powers at different frequencies and bias points. The equipment used for these measurements is shown in Figure 6.8 and comprises two bias tees, a microwave source capable of delivering up to 20.0 dBm available power, a test fixture into which the packaged amplifier was placed and a power meter.

Firstly, the power source was checked to ensure that it was accurately calibrated. The power meter was connected directly to the power source and a series of power measurements were made at 2.0, 3.0, 4.0 and 5.0 GHz. The output power readings determined the actual power delivered to a 50 Ω load, rather than the power setting on the source and these were used to plot the power saturation curves. The indicated source level and the power meter reading agreed at all frequencies to within +/- 0.5 dBm.

A series of power saturation curves were measured for JS1 at V_{ds} = 5.0 V and V_{gs} = -0.63 V from 2.0-5.0 GHz, and these are plotted in Figure 6.9. For low input powers, the output power increased with frequency to about 4.0 GHz, above which it remained constant. Simulations for the nonlinear model on ANAMIC at the same bias and RF input frequencies are shown in Figure 6.10. The shapes of the power saturation characteristics are accurately predicted although the model produces output powers which

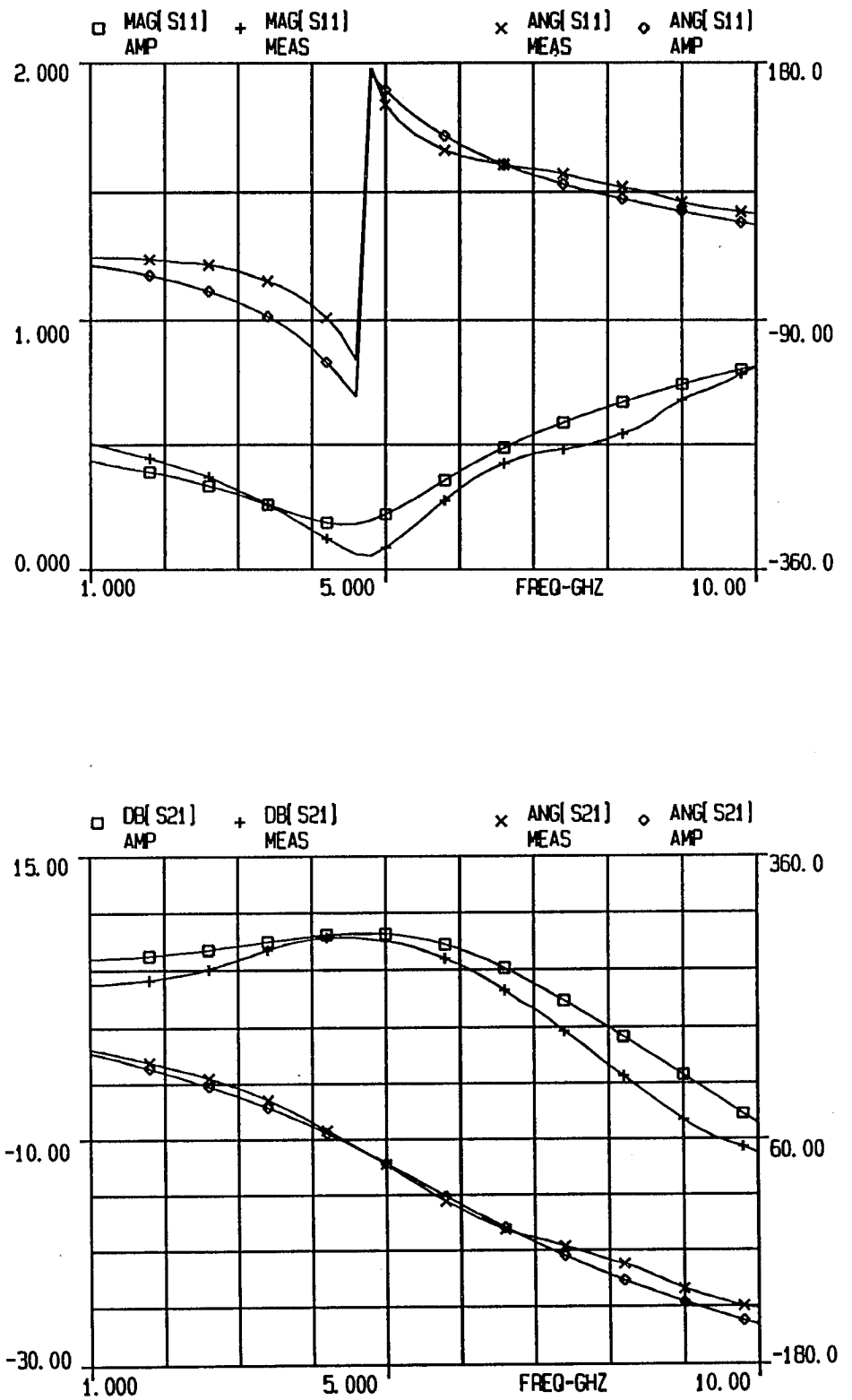
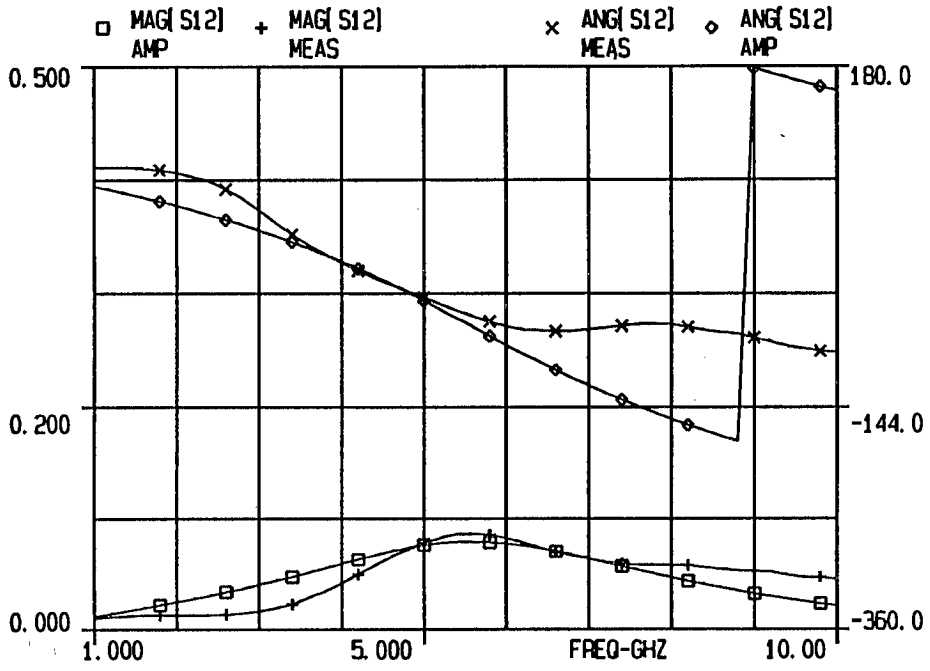


Figure 6.7a: S11, S21 measurements and optimized model for JS1



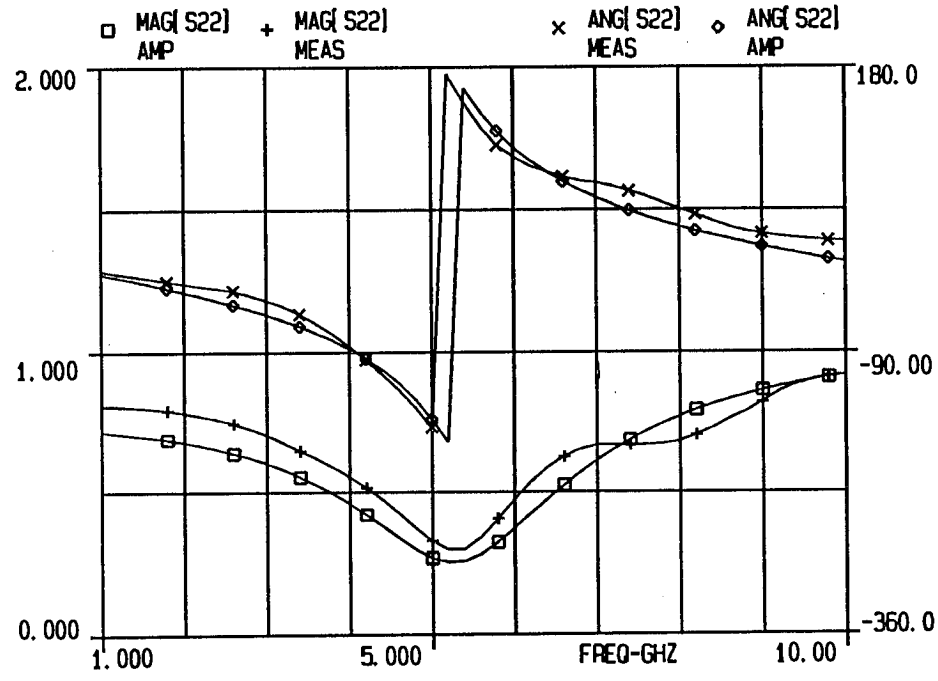


Figure 6.7b: S12, S22 measurements and optimized model for JS1

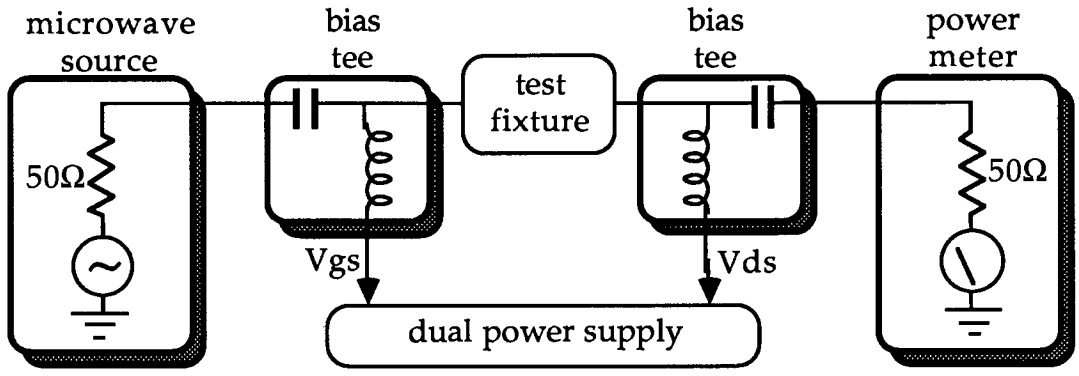


Figure 6.8: Apparatus for making power saturation measurements

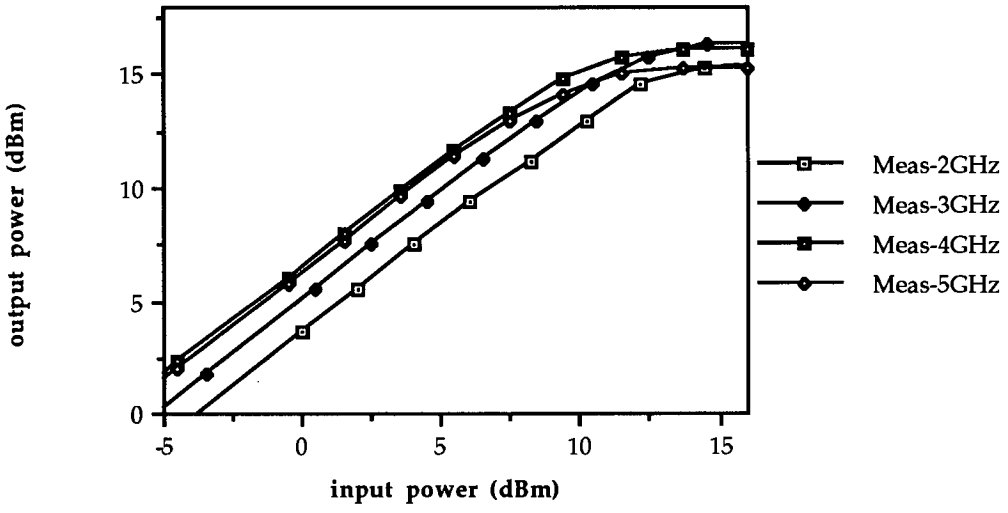


Figure 6.9: JS1 power saturation measurements at V_{gs}=-0.63V, V_{ds}=5.0V

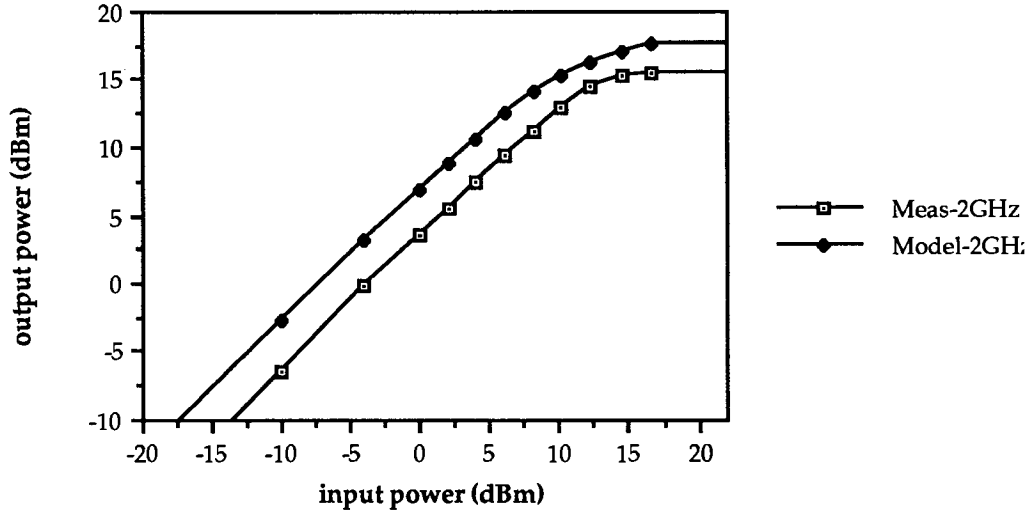


Figure 10a: Measurements and simulation for JS1 at 2.0 GHz

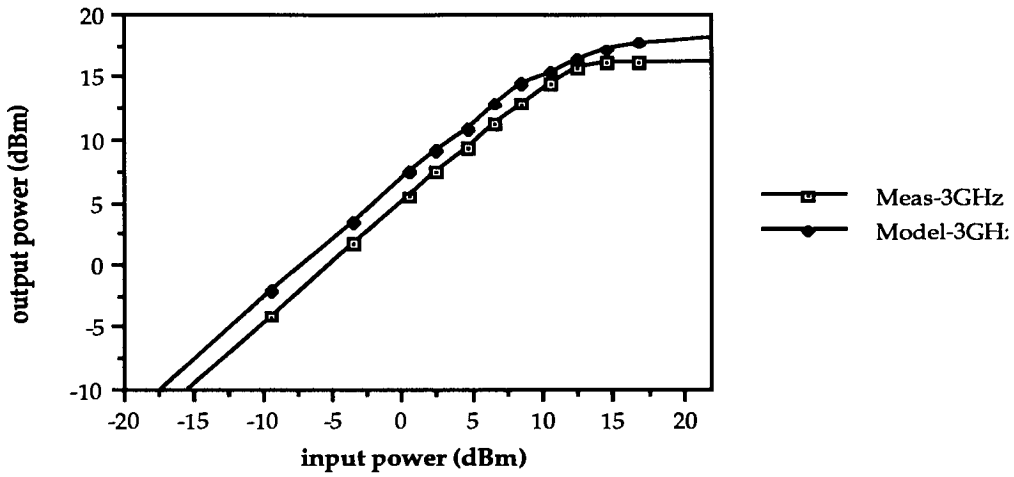


Figure 10b: Measurements and simulation for JS1 at 3.0 GHz

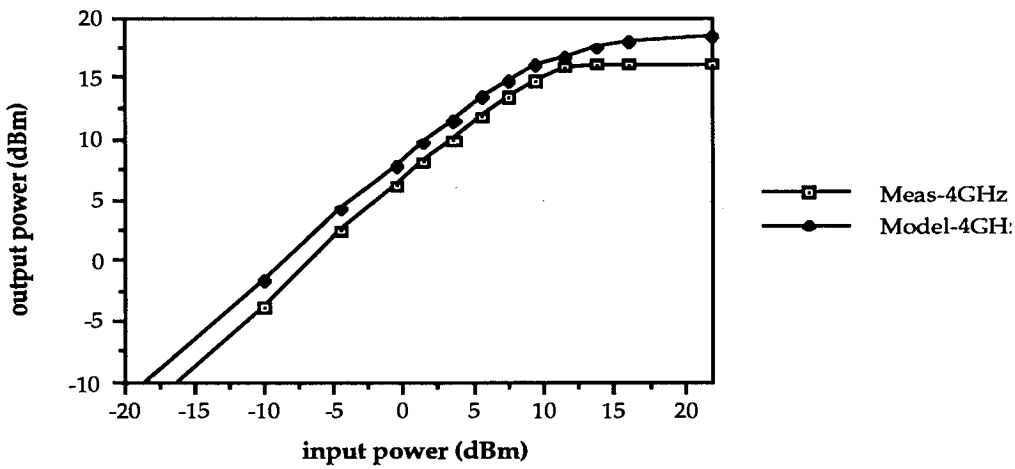


Figure 10c: Measurements and simulation for JS1 at 4.0 GHz

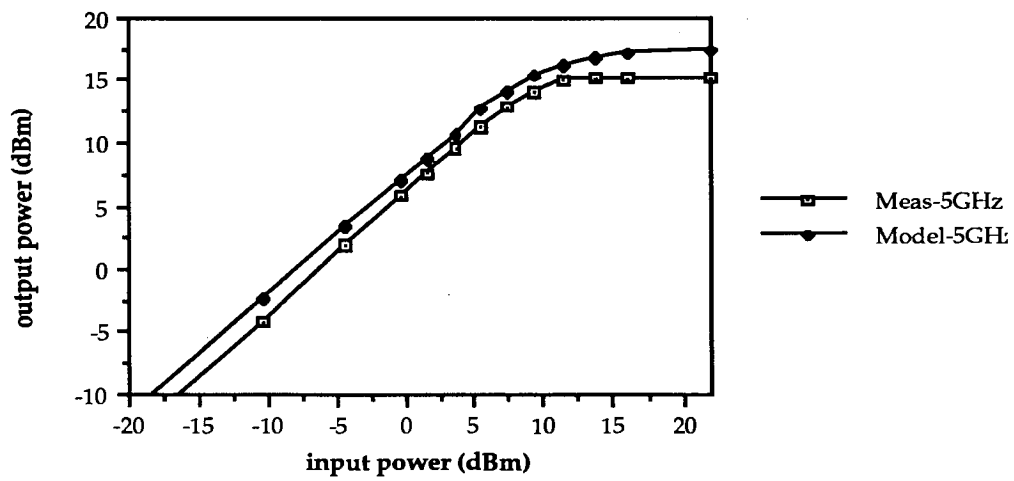


Figure 10d: Measurements and simulation for JS1 at 5.0 GHz

are almost uniformly 1.5 dBm higher than the measurements. The frequency response is reproduced in Figure 6.11 and compares well with the measurements in Figure 6.9.

The difference between the measured and simulated curves can be attributed to experimental error, model error and most importantly, the difference in the characteristics of the FET of the amplifier design and the FET used to construct the nonlinear model. It has already been shown that Idss for the FETs varies by 20% *and* the small-signal measurements of the amplifier are also noticeably different from the linear model of the original test FET.

An interesting test was performed, comparing the gain from the power measurements at 2.0, 3.0, 4.0 and 5.0 GHz for an input power of -5.0 dBm (3.5, 5.8, 6.1 and 5.9 dBm), with the small-signal gain from S-parameter measurements (4.34, 5.84, 7.65 and 7.47 dBm respectively). In theory, the results of small-signal measurements and the power measurements at very low input power levels should be very similar. The difference between the two sets of readings can only be attributed to experimental errors in both the power saturation and the S-parameter measurements, and it can therefore be concluded that a small amount of experimental error exists.

Small-signal measurements of the amplifier, mentioned in the previous section, revealed that the values of passive components in the fabricated MMIC were significantly different from the passive values used for the MMIC design. The fabricated values were estimated by fitting the S-parameter measurements of the MMIC to an equivalent circuit. An interesting exercise involved comparing nonlinear simulations for the amplifier containing the initial passive component values with simulations containing the optimized passive values and these are shown

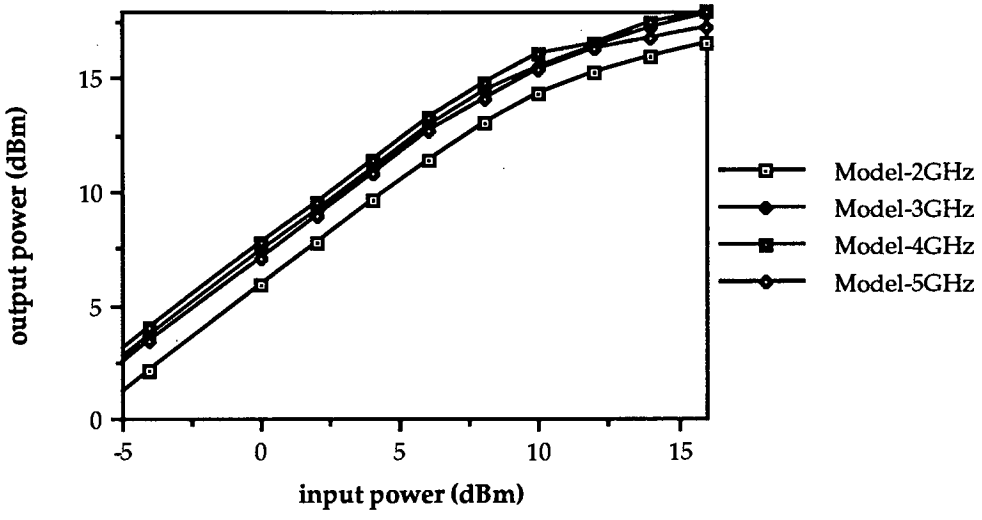


Figure 6.11: JS1 power saturation simulations at V_{gs}=-0.63V, V_{ds}=5.0V

in Figure 6.12. The results show that the simulations containing the initial component values ('initial') are not as accurate as those containing the optimized elements ('model'), confirming that the passive components do, in fact, have a tolerance of 10%, and that the component values in JS1 are slightly different from those used in the initial design.

A series of simulations were made, where the nonlinear resistor R_x was replaced by a linear resistor. The resistance value was determined by the simulation bias point and the resistor corrected the output conductance for frequency dispersion at the chosen bias point only. The results in Figure 6.13 compare measurements 'Meas' with simulated results for the model 'Model'. As expected, simulations for the linear resistor 'ConstRx' in the model did not change the model response at low power levels but at higher power levels, where the effective bias was changing continuously, the model performance had changed and the model was less accurate. This shows that the inclusion of a bias dependent R_x in the model increases the

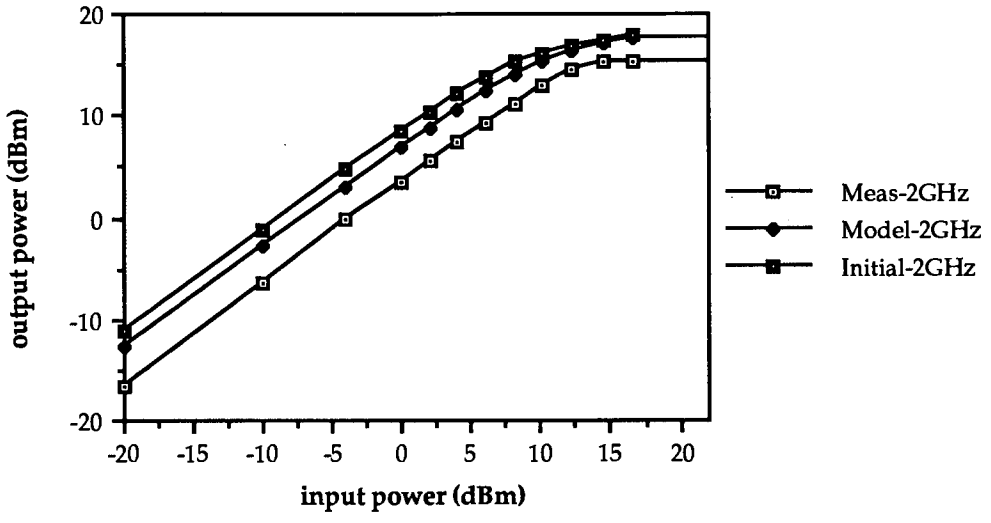


Figure 6.12: Comparison between simulations containing original and optimized passive components in MMIC circuit at 2.0 GHz

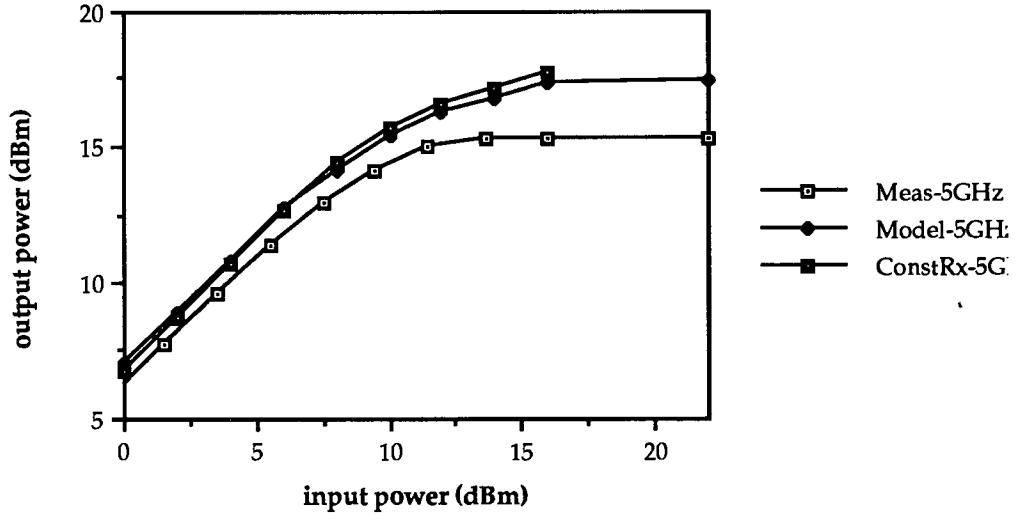


Figure 6.13: Comparison between nonlinear models containing linear and nonlinear Rx at 5.0 GHz

accuracy of the nonlinear simulation by as much as 0.7 dBm in the output power characteristics. These results provide firm evidence that a nonlinear resistance is required for R_x in nonlinear models for circuits where high signal power levels are used.

Another series of simulations, where the R_xC_x pair was removed altogether, are shown in Figure 6.14. 'Meas' are the measurements, 'Model' is the nonlinear model and 'NoRx' is the same model without the R_xC_x pair, where no effort is made to account for the effects of frequency dispersion. This is very similar to using the DC I/V curve data as the basis for the nonlinear current source in the model, instead of the high frequency data. As expected, the accuracy of the simulated power saturation curves without the R_xC_x pair is much worse.

Simulations were made of the nonlinear model at different bias points and compared to actual measurements. Results in Figures 6.15 and 6.16 illustrate the power saturation curves for JS1 at V_{gs} = 0.0 V and -0.8 V respectively (with V_{ds} = 5.0 V) and the simulated output power characteristics of the model compared well to the measurements.

Figure 6.17 shows a simulation for the nonlinear model, where the forward bias diode across the gate capacitance C_{gs} has been removed. The curve labelled 'nodiode' corresponds to simulations where the gate diode was omitted from the nonlinear model. At low power levels, its characteristics are similar to those of 'model', the standard nonlinear model. At input power levels over 10.0 dBm the fit deteriorates, indicating that the inclusion of the gate diode is necessary. This result is to be expected since, at higher power levels, the voltage on the gate in some part of the r.f. excitation will cause forward conduction and the omission of the gate diode means that this current is not modelled.

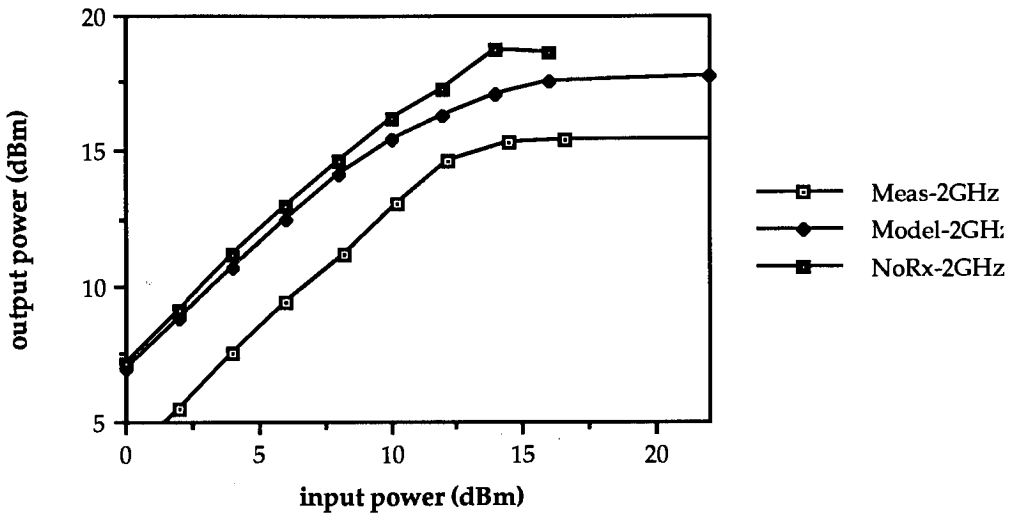


Figure 6.14: Comparisons between simulations with and without the effects of frequency dispersion modelled

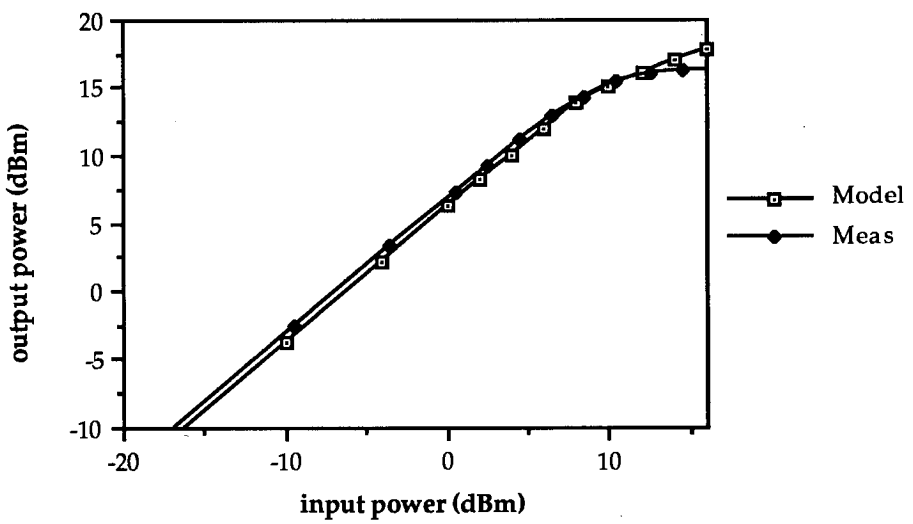


Figure 6.15: Model and measurements at Vgs=0.0V and Vds=5.0V

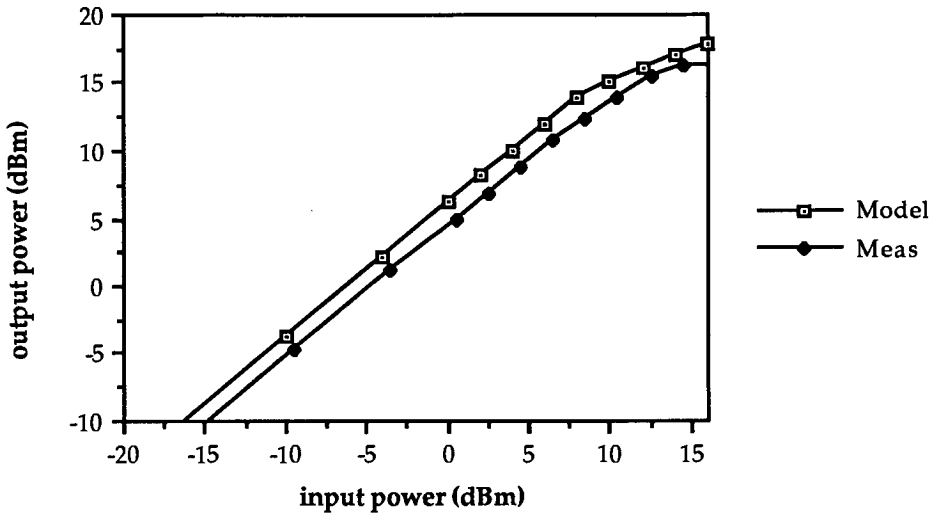


Figure 6.16: Model and measurements at Vgs=-0.8V and Vds=5.0V

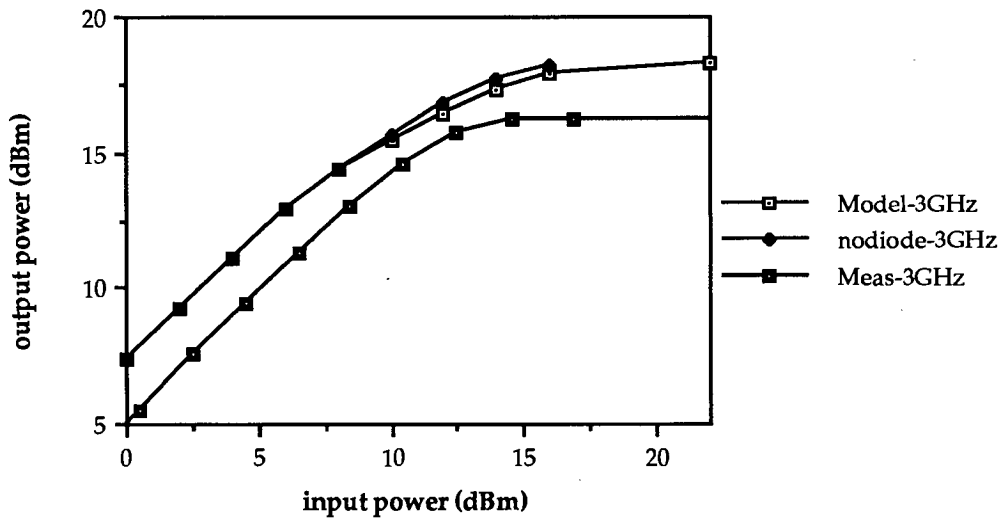


Figure 6.17: Simulations with and without the forward gate conduction diode at 3.0 GHz

6.4 Single-stage Amplifier with 'On-chip' Bias Circuit JS2

6.4.1 Design, Layout and Small-signal Characteristics

A diagram of the single-stage amplifier JS2 is shown in Figure 6.18. It is similar to JS1 and consists of a matched 300 micron FET, with bias networks. The gate bias is supplied from pad V_{gs1}, through the resistor of the input matching network and the drain bias is supplied from pad V_{ds1}, through the RF choke. 'On-chip' DC blocking capacitors have been added to both the input and output matching networks. The small-signal characteristics of JS2 were modelled using TOUCHSTONE and the amplifier was packaged, bonded and measured in a similar manner to the amplifier JS1.

The small-signal model for JS2 is compared to the measurements in Figure 6.19, where a good correlation can be seen. The measured gain response is slightly lower than the gain predicted by the model and the overall fit between the two sets of parameters was improved by allowing some of the passive components and parasitics to vary by +/- 10%. The improved response is illustrated in Figure 6.20. Here the input and output reflection coefficients are very accurately modelled and the gain response is predicted to within 0.2 dB.

6.4.2 Power Saturation Curves for Single-stage Amplifier JS2

A series of nonlinear circuit simulations were made for JS2 using ANAMIC. Essentially, these were similar to the simulations for JS1, although the circuit topology for JS2 was slightly more complicated and hence prone to more errors if, as seen, these passive components have tolerances in fabrication. The optimized values for the passive components were chosen for the simulation, since these provided a better representation of the fabricated amplifier.

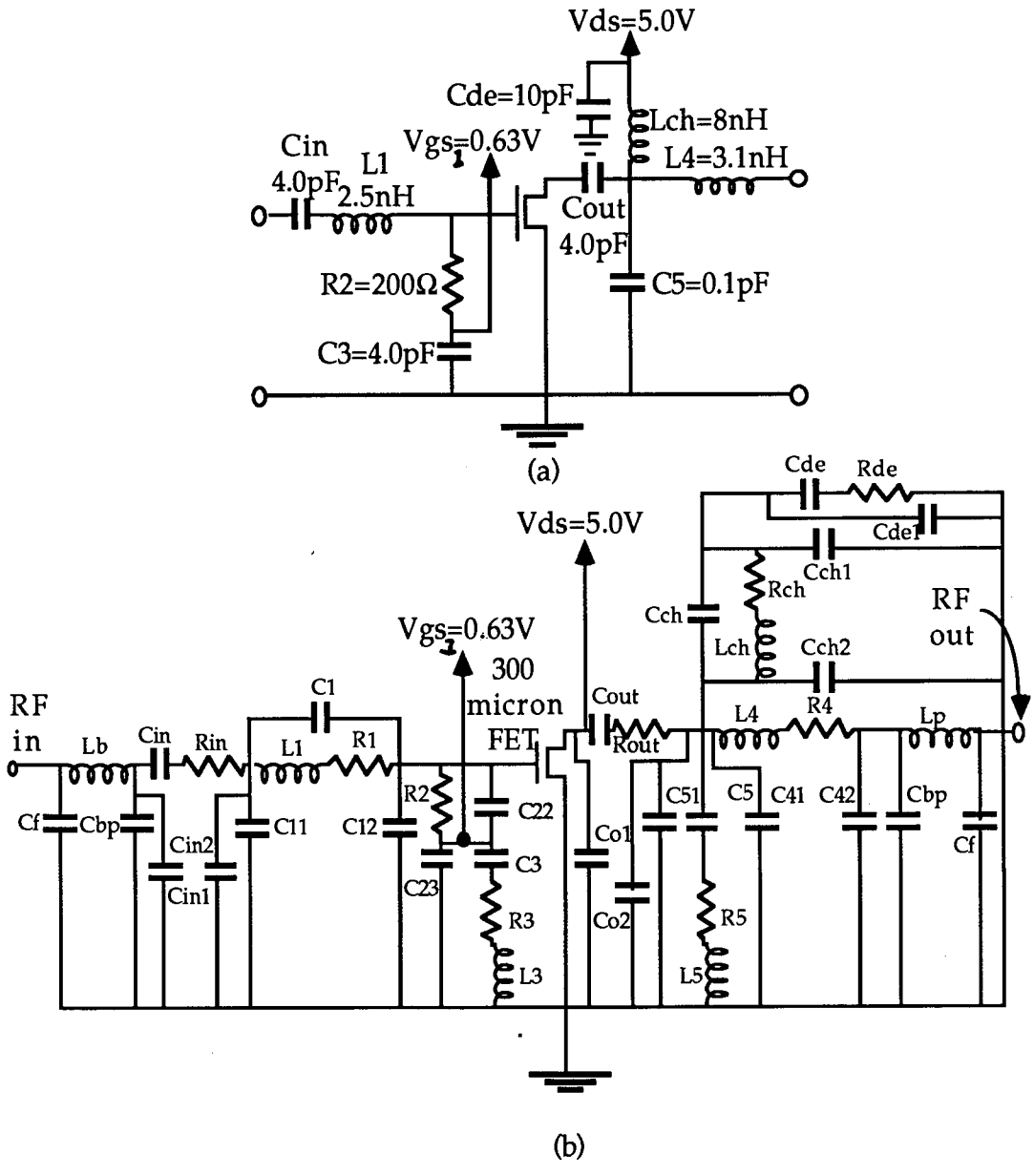


Figure 6.18: Self-biased, single-stage amplifier JS1

(a) without parasitics, (b) with parasitics

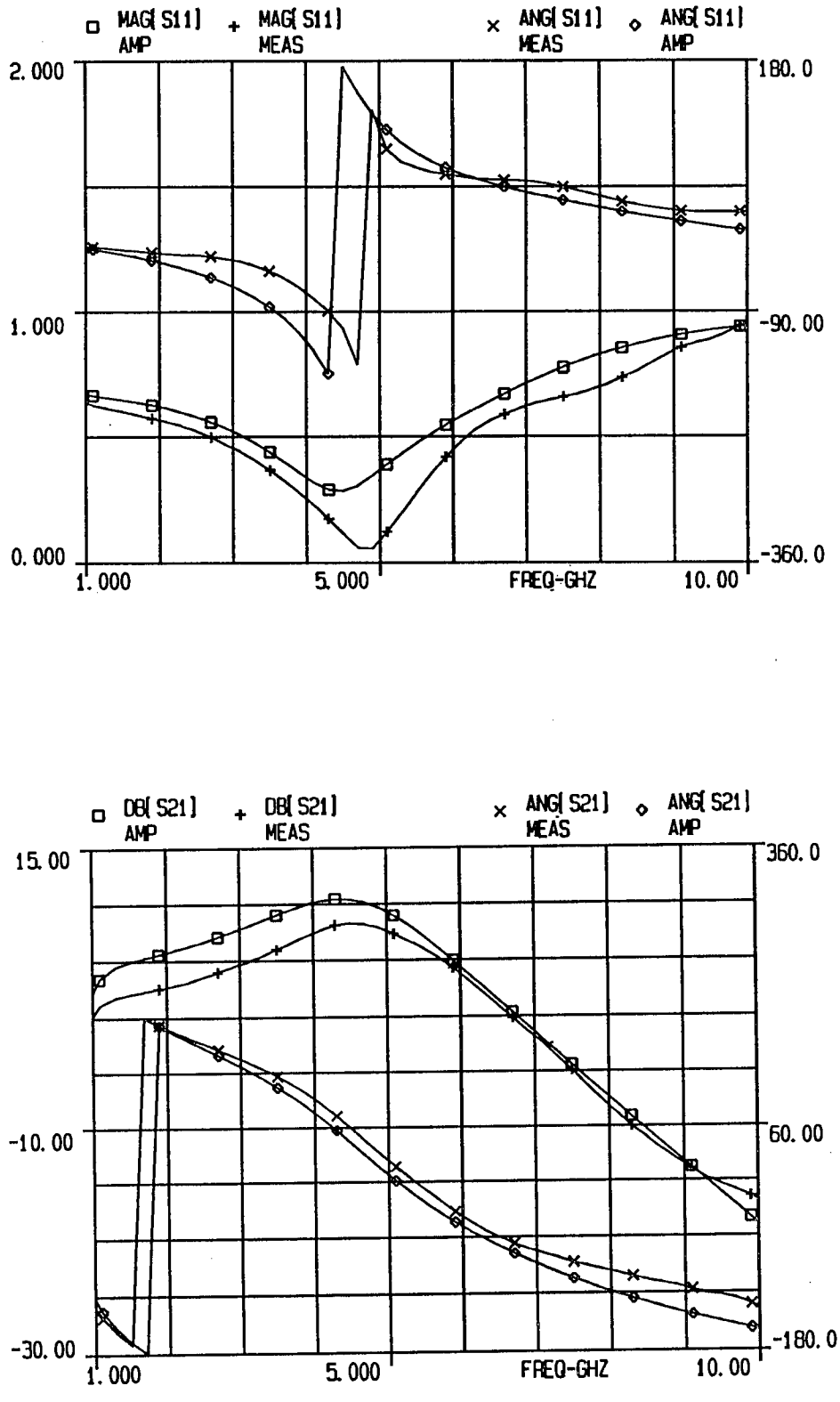


Figure 6.19a: S11, S21 measurements and original model for JS2

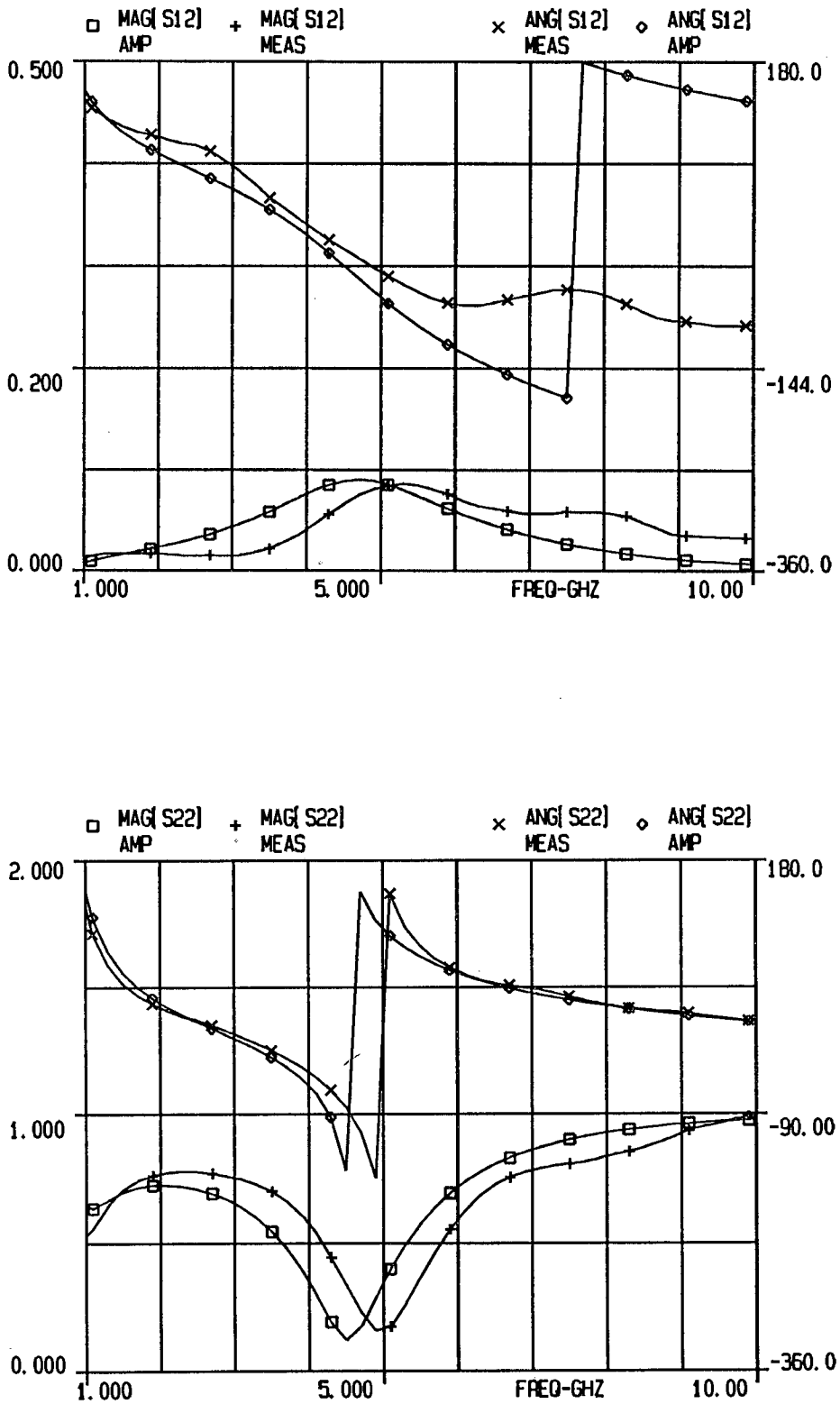


Figure 6.19b: S12, S22 measurements and original model for JS2

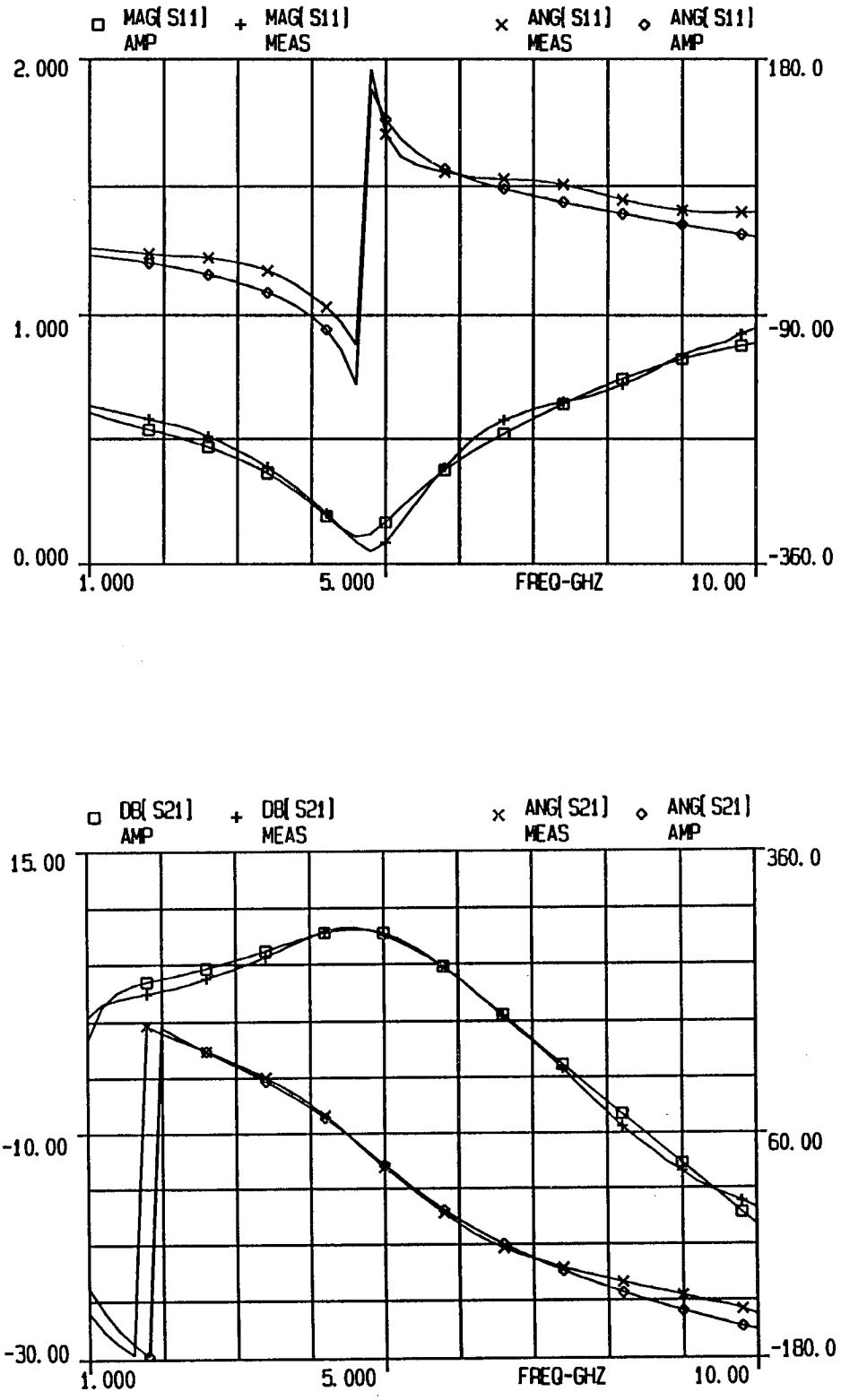


Figure 6.20a: S11, S21 measurements and optimized model for JS2

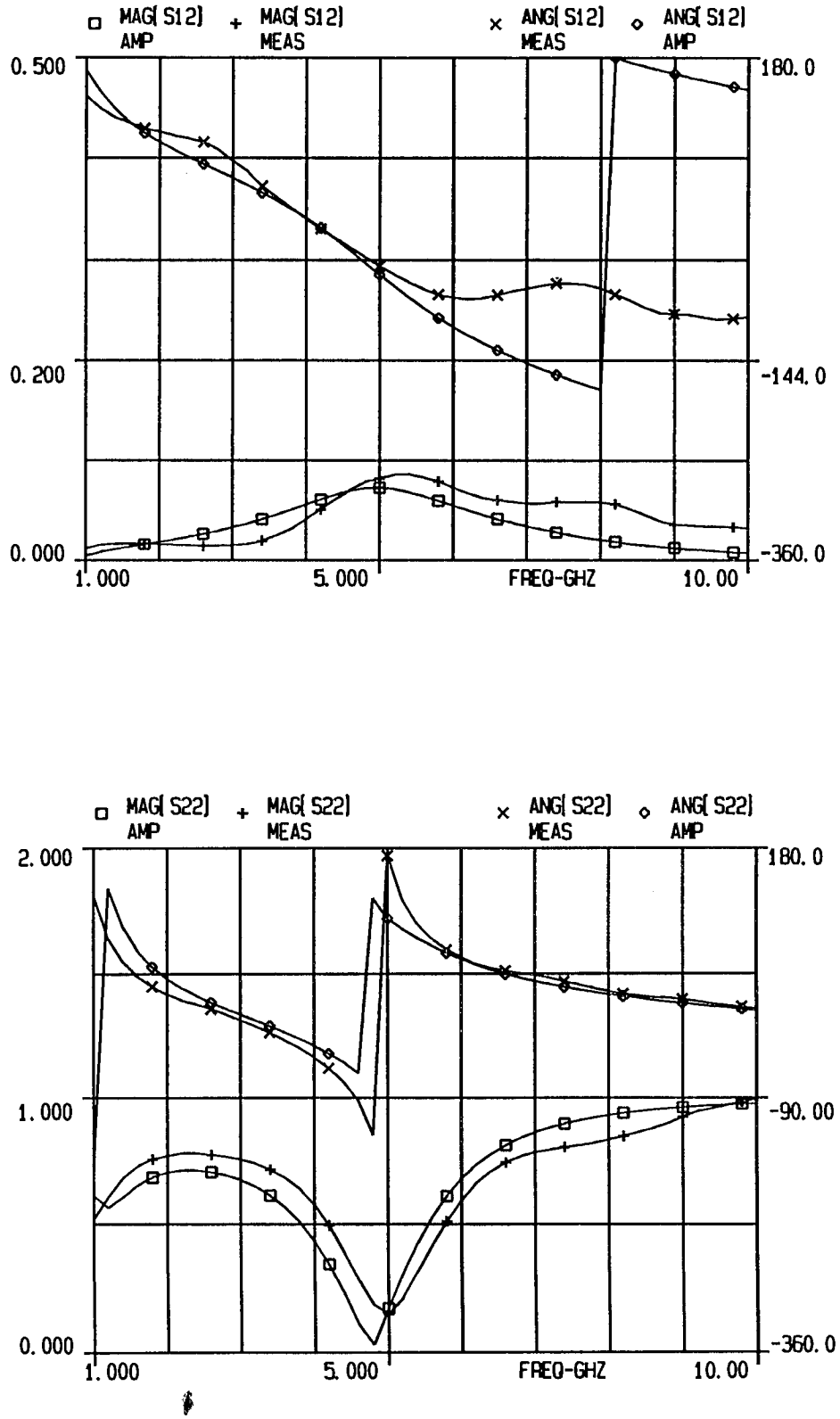


Figure 6.19b: S12, S22 measurements and optimized model for JS2

Figures 6.21-6.24 compare modelled and simulated power saturation curves for JS2. The measurements are accurately predicted, especially around 4.0-5.0 GHz and these results are in accordance with the small-signal fit, which is also very accurate around these frequencies (see Figure 6.20). In general, the correlation between model and measurements was better than for the JS1 amplifier. No reason can be attributed to this, other than the possibility that the characteristics of the JS2 fabricated MESFET were more similar to the nominal design MESFET (on which the nonlinear model was based) than the JS1 FET. This is perhaps indicated, where the DC characteristics of the FET in JS2 were more similar to the FET used to derive the nonlinear model than the FET in JS1. I_{dss} for the modelled MESFET is 46.0mA; for the JS2 FET I_{dss} is 42.0mA, whereas for JS1 I_{dss} is 39.7mA.

Simulations were made of JS2 where the nonlinear resistance R_x in the model was replaced by a linear resistance. Comparisons between the simulations for both linear and nonlinear resistance indicate clearly that at high power levels, the inclusion of the nonlinear resistor (R_x) into the model significantly improves the simulation accuracy and this is illustrated in Figure 6.25. The 'Meas' curve represents the measurements, 'model' is the full nonlinear model and 'ConstRx' represents the model where R_x is set to a bias independent fixed value.

Another set of simulations were made where the R_xC_x pair were removed completely (see Figure 6.26). The removal of the RC pair meant that there was no correction for frequency dispersion in the model and is similar in effect to using the DC curves as the basis of the nonlinear current source in the model rather than the derived AC values. The simulation accuracy fell for 'NoRx' (where the R_xC_x pair where omitted) by

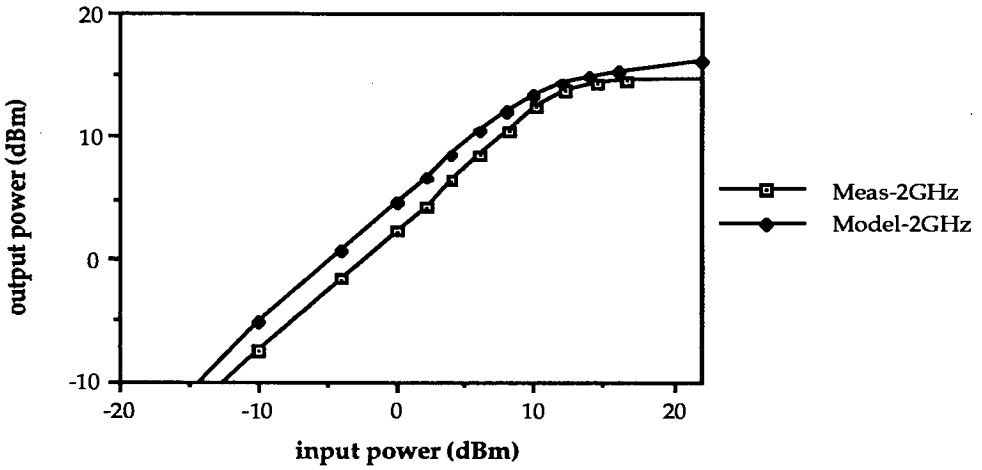


Figure 6.21: Measurements and simulation for JS2 at 2.0 GHz

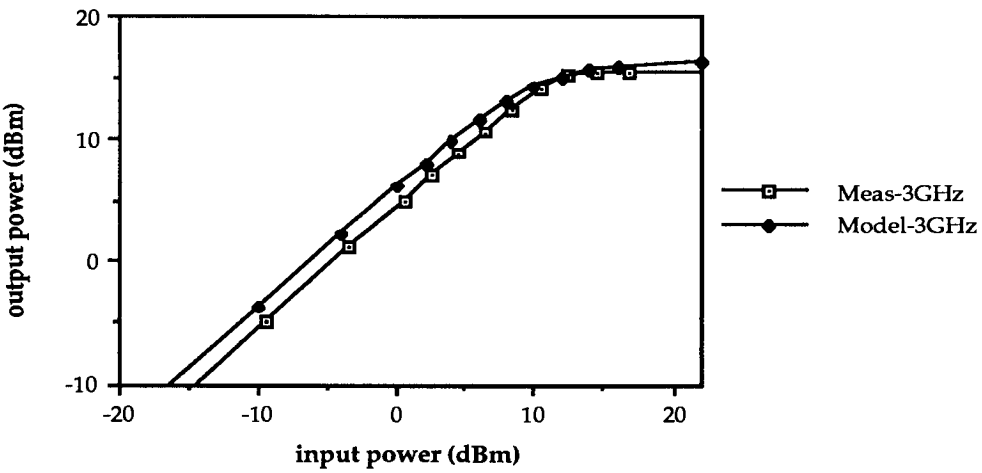


Figure 6.22: Measurements and simulation for JS2 at 3.0 GHz

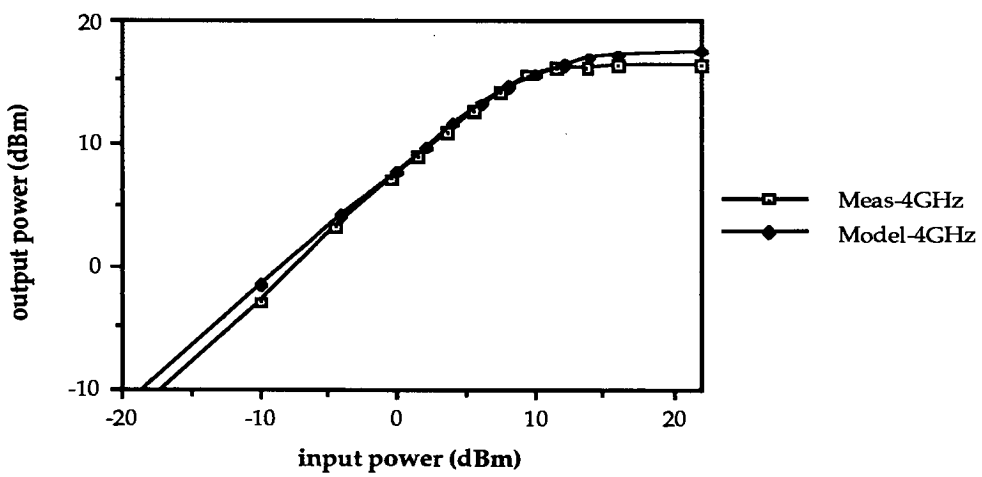


Figure 6.23: Measurements and simulation for JS2 at 4.0 GHz

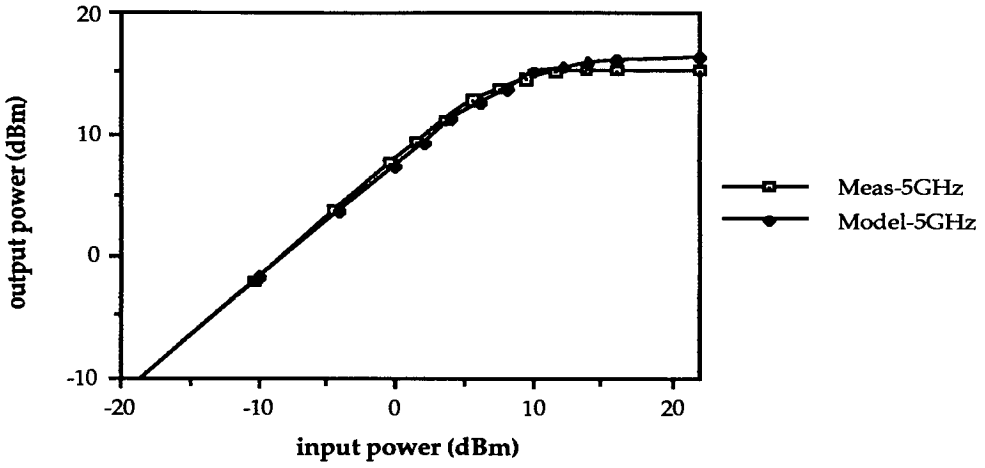


Figure 6.24: Measurements and simulation for JS2 at 5.0 GHz

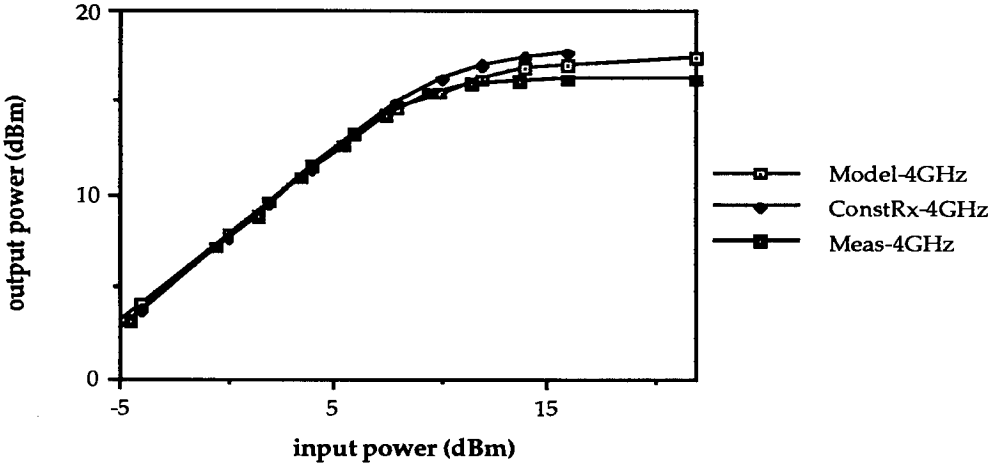


Figure 6.25: Simulations for JS2 with linear and nonlinear Rx

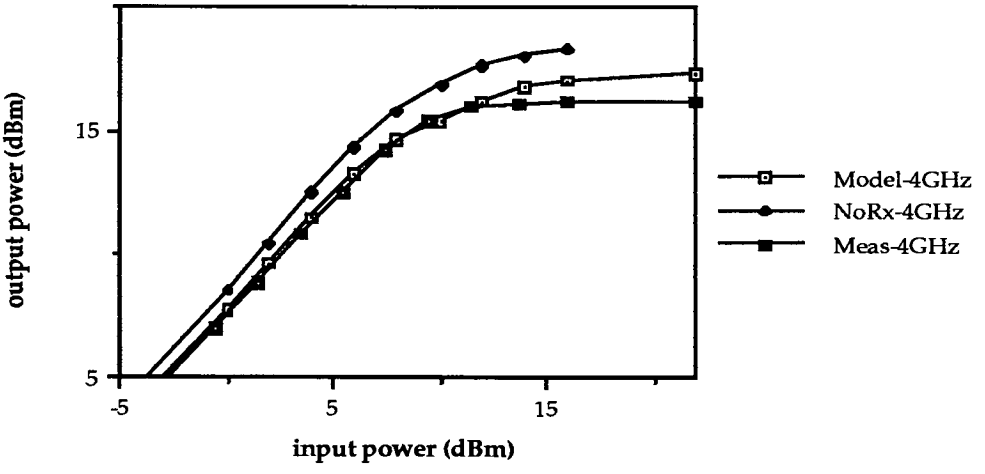


Figure 6.26: Simulations of JS2 with and without correction for dispersion effects in output conductance

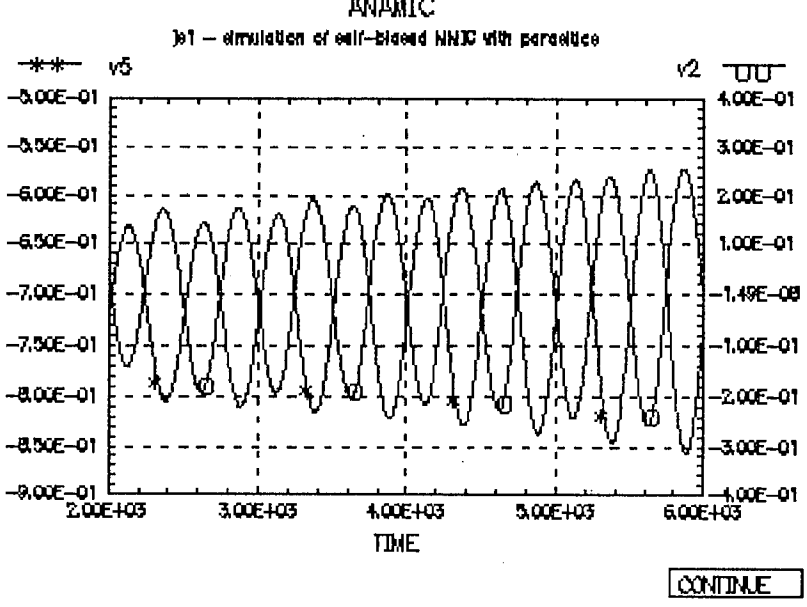
about 1.2 dBm at high power levels.

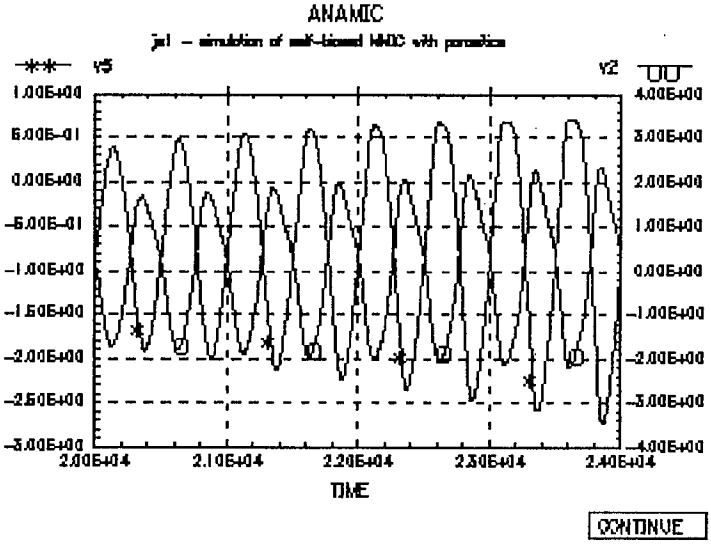
Finally, a time-domain response is illustrate for JS2 in Figure 6.27. A 2.0 GHz input signal is ramped exponentially from 0 to 30 nS. Initially, the power of the input signal is small and the response is linear. As the input power increases, the nonlinearities in the large-signal model start to produce nonlinear behaviour, until the output response is decidedly nonlinear. Figure 6.27 illustrates three time windows, corresponding to linear operation, the onset of nonlinear behaviour and very nonlinear behaviour.

6.5 Load-Pull Measurements

6.5.1 Introduction

Measurements are needed to characterize active devices, such as power amplifiers, to relate the impedances presented to the device with the output power characteristics. 'Load-pull' measurements have traditionally been used to provide such characterization, involving the measurement of the output power from a device as a function of the output load, at a fixed input impedance and at a single frequency. The results of these measurements are usually plotted on a Smith chart in the form of a series of circular contours. The central point of the contours represents the optimum load at which the maximum power (P_{opt}) is delivered. Each successive concentric ring from the centre is formed from the output impedances which, applied to the device, produced output powers of one, two, three dBms less than P_{opt} (P_{opt-1} dBm, P_{opt-2} dBm, P_{opt-3} dBm etc.). Load circles differ according to whether the device is being characterized for optimum power, efficiency, or intermodulation. The contours rarely form perfect circles, especially at high power levels, where the shape can appear more elliptical or distorted.





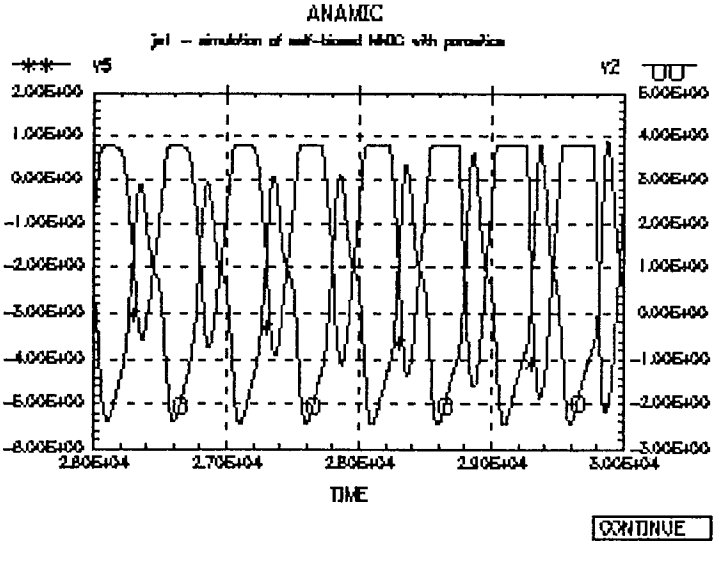


Figure 6.27: Time domain simulations (0-30nS) for ramped input power

Standard load-pull measurements are time-consuming to make and the scope for experimental error is quite large. Consequently, a number of modifications to the basic experimental setup have been suggested. Takayama [162] designed an equivalent load-pull apparatus which dispensed with the need for an output load. Instead, both the input and the output ports of the transistor were driven with external signals at the same frequency and the 'equivalent' output load was calculated from measurements of the output incident and reflected voltages. This equivalent load-pull method has been used successfully elsewhere [163,164].

Another experimental technique [165] involves the use of a computer-controlled, slide-screw tuner so that manual load-pull measurements could be replaced with automated measurements. Additionally, it was noted that the practice of seeking load impedances, which produced the quantized output powers (P_{opt-1} dBm, P_{opt-2} dBm, P_{opt-3} dBm etc.) for power circles, was time-consuming. Instead, measurements were made at discrete load impedances over an area of the Smith chart. The output power data was used to produce power contours that were plotted using computer software.

The methods used to implement the load-pull measurements are described in Section 6.5.2 and were developed so that accurate measurements could conveniently be made with the equipment available. The results of load-pull measurements are given in Section 6.5.3.

6.5.2 Experimental Setup

The apparatus for the first load-pull measurements is shown in Figure 6.28. At a single bias point and at a fixed frequency, the double stub tuners at the input and output were manipulated to find the optimum

power. The first power circle was found by recording a set of output impedances which produced an output power of 1.0 dBm less than the maximum output power.

Since the repeatability of the tuners was poor, the impedance of the output load was measured directly after each power reading. Using the experimental layout above, this required that the tuner was disassembled from the setup and presented to the network analyser for each load-pull measurement. Repeatedly disassembling the tuner was time-consuming, prone to measurement error and reduced the life expectancy of the connectors. Therefore, an alternative experimental setup was developed which made use of a microwave switch, and is shown in Figure 6.29.

The microwave source was connected to the input port of the jig via the double stub tuner and bias tee. The output of the jig was connected to a power meter via another bias tee and double stub tuner. A microwave switch was added so that with the switch in position '1' the power from the test device could be measured. With the switch in position '0', the impedance of the one-port system from the calibration plane AA to the 50 Ω load in the power meter was measured.

The network analyser was calibrated to the AA plane, removing the effects of the switch from B0 to the AA plane and the transmission line to the network analyser. The actual impedance presented to the device comprised the measured load impedance plus the effects of the switch and transistor fixture. To establish the characteristics of the switch, a series of two-port measurements were made from the AA plane to C0 and these were stored in a TOUCHSTONE format file (the repeatability of the switch was also investigated and it was found that the switching reliability was very good for both channels). The switch was found to have the same transmission S-parameter in both switch positions to within 0.07dB and

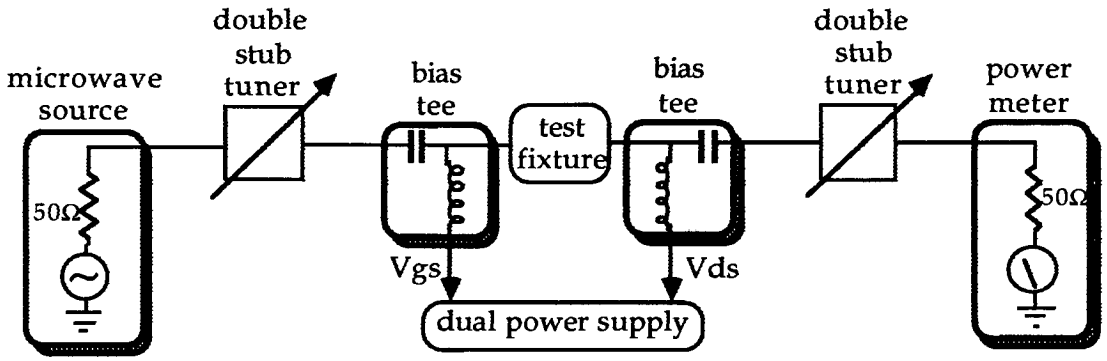


Figure 6.28: Apparatus for first load-pull measurements

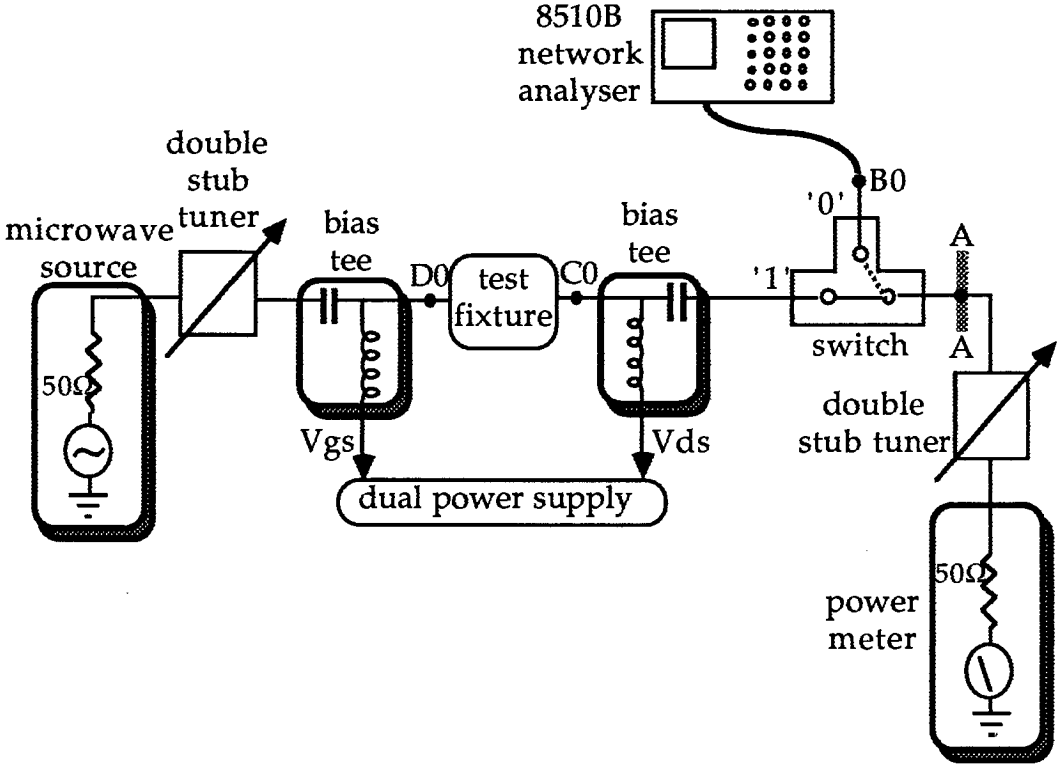


Figure 6.29: Load-pull setup with microwave switch

1.5° of phase. The transistor fixture had already been characterized for on-chip calibration (see Chapter 3) and had been accurately modelled. The one-port measurements at the AA plane were modified to include the effects of the switch and jig and this was done using TOUCHSTONE.

The input impedance remained constant for a complete set of power circles and only had to be measured once. This was done by connecting point D0 to the end of the reference plane of the network analyser and measuring the impedance. The effects of the fixture were included by adding the equivalent circuit of the jig in the measured results, again using TOUCHSTONE.

An experimental setup has been described for making accurate load-pull measurements. For a specified input power, input impedance and frequency, the optimum output power can be found by manipulating the output double stub tuner. The impedance corresponding to this power level can be found by changing the microwave switch from position '1' to '0' and recording the one-port impedance on the network analyser. This procedure is repeated until a series of power circles can be drawn from the impedance plots on the Smith chart.

6.5.3 Load-Pull Results

The above apparatus was used to measure a Plessey 300 micron test FET, similar to the device from which the nonlinear model was derived. The MESFET was selected and packaged and DC measurements of the MESFET ensured that it was representative of the batch: it was packaged and bonded in the same manner as the calibration standards, so that it could be used in the Tektronix jig (see Chapter Three).

Two sets of load-pull curves for the 300 micron MESFET are illustrated in Figure 6.30. Both sets were taken at Vgs=0.0V and Vds=5.0 V

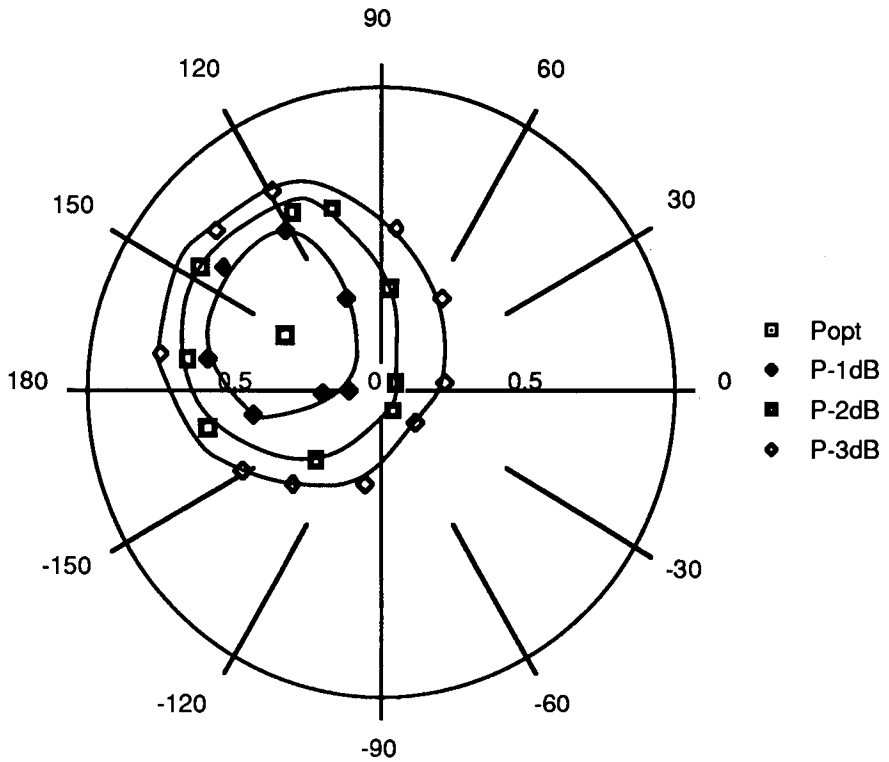


Figure 6.30a: Measured load-pull results at 2.0GHz

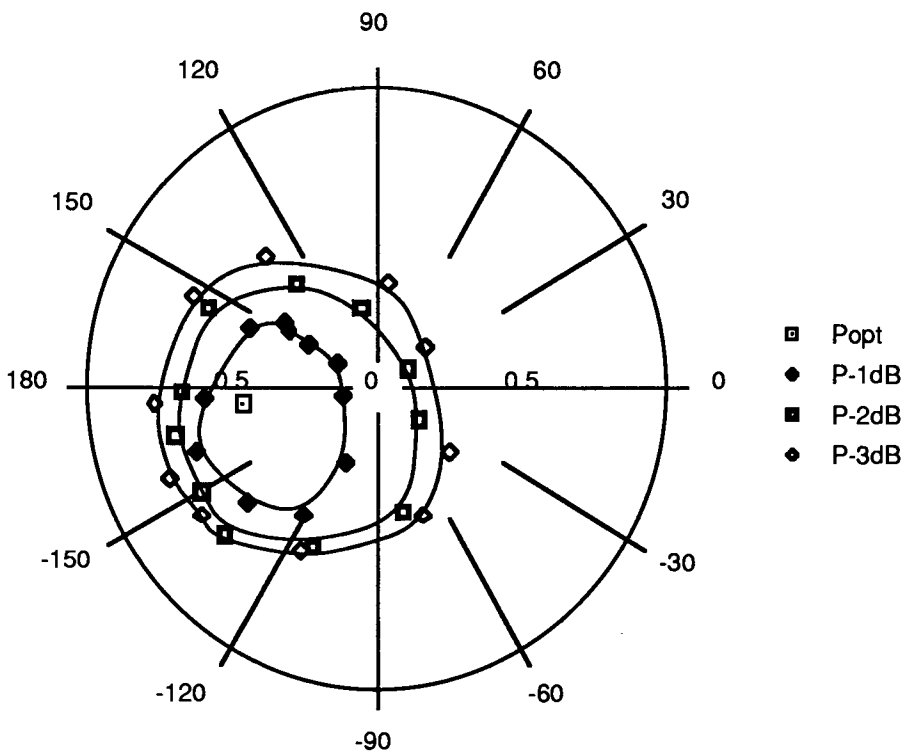


Figure 6.30b: Measured load-pull results at 3.0GHz

and the input signal power was at 12.0 dBm. The frequency of the input signal in set A was 2.0 GHz and in set B was 3.0 GHz. Figure 6.31 illustrates the corrected power circles for sets A and B, where the effects of the switch and transistor fixture have been added to the output impedance.

For set A, the optimum power was measured as 15.7 dBm and for set B the optimum power was 16.0 dBm. Losses in the switch and transistor fixture at 2.0 GHz were found from the two-port S-parameter measurements made of the switch and the equivalent circuit for the jig and these equalled 0.45 dB. Some power was also dissipated in the load-pull setup between the reference plane AA and the power meter, and these losses were measured as 1.2 dB. Therefore the total loss in the load-pull apparatus was 1.65 dB. All of the power measurements were higher than the power meter readings and the corrected optimum power point was 17.35 dBm for set A and 17.65 dBm for set B.

Simulations were made of the load-pull measurements using ANAMIC. A set of 100 load impedances were chosen, which formed a grid when plotted on the Smith chart. Each impedance was represented in the circuit file as either a series RL or RC pair, depending on whether the impedance lay on the top or bottom half of the Smith chart. Simulation results for set A are shown in Figure 6.32.

The shape of the load-pull circles in Figures 6.31 and 6.32 are almost identical and can be mapped almost exactly onto eachother as illustrated in Figure 6.33. For this to be achieved however, a small section of transmission line and a series capacitance of 1.1 pF would need to be added to the measured load-pull circles. A detailed examination of the load-pull setup did not reveal a way in which such additional elements could have been overlooked.

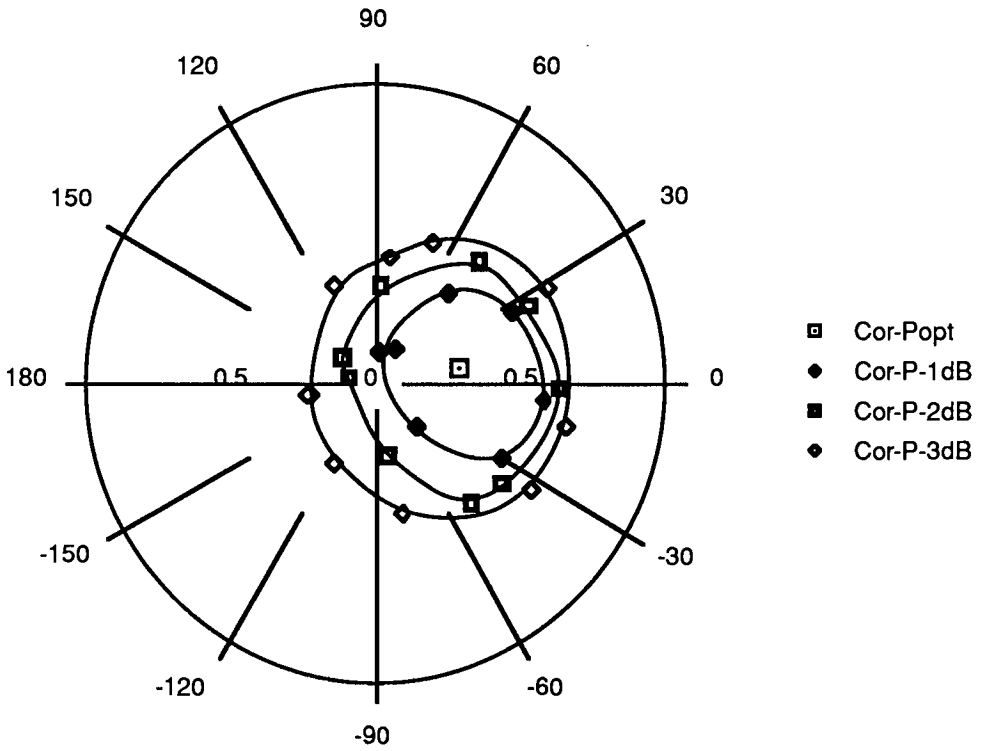


Figure 6.31a: Deembedded measured load-pull results at 2.0GHz

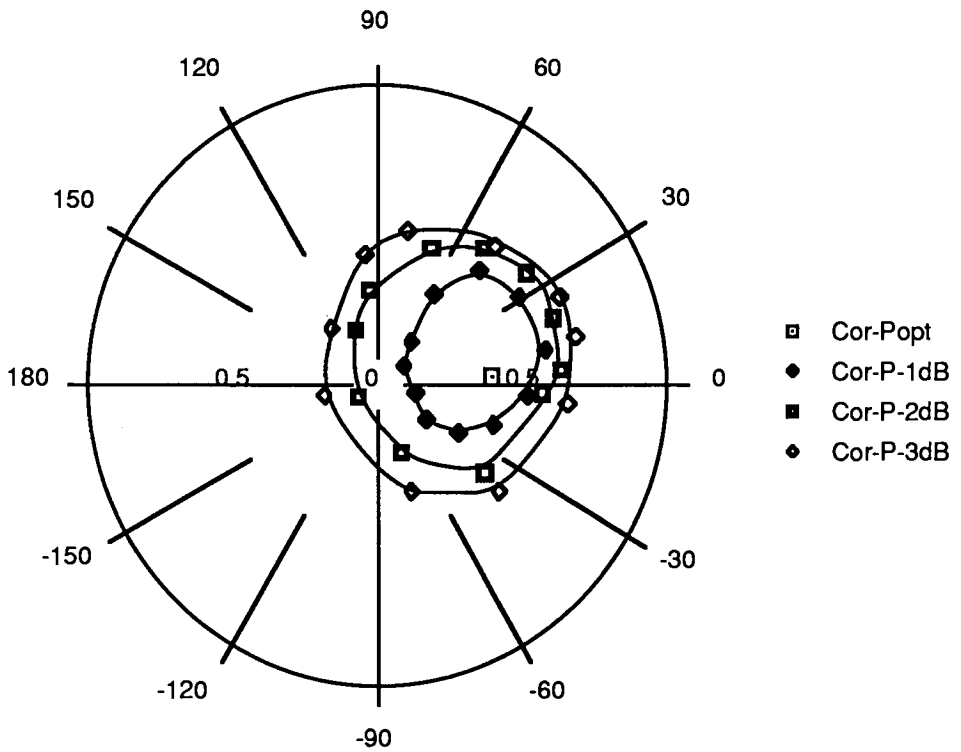


Figure 6.31b: Deembedded measured load-pull results at 3.0GHz

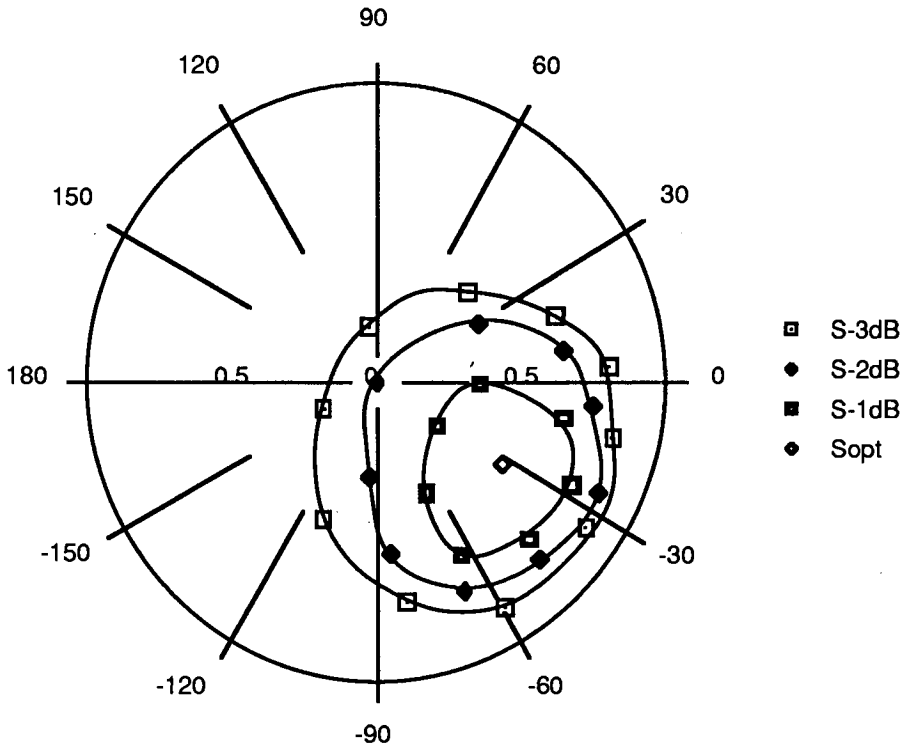


Figure 6.32: Load-pull simulations at 2.0 GHz

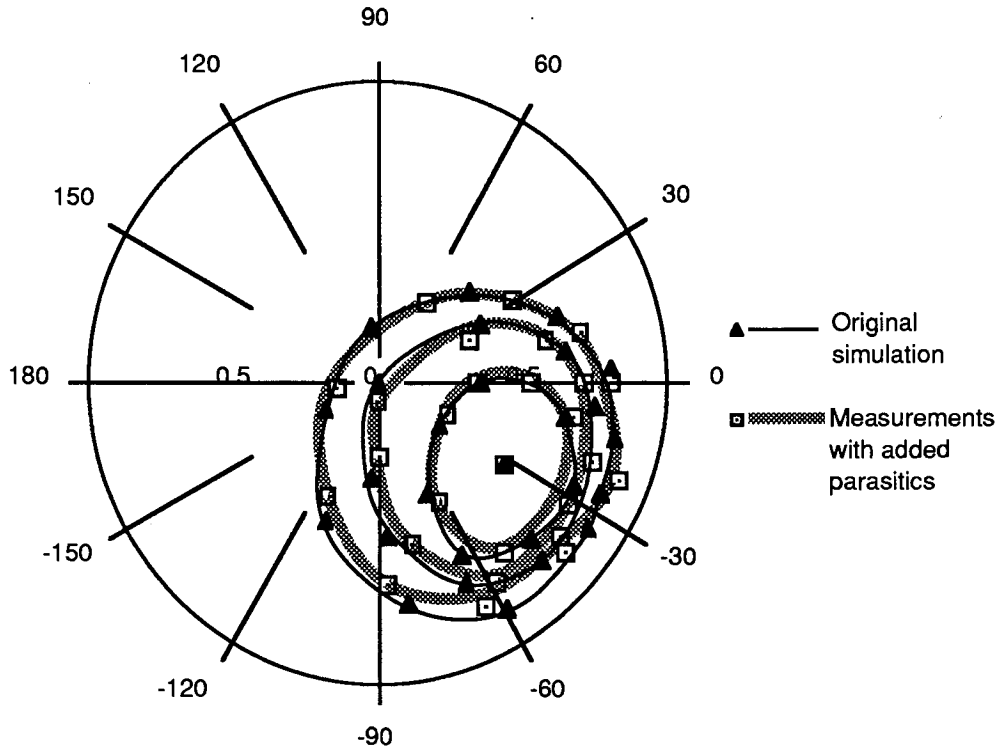


Figure 6.33: Load-pull simulations and corrected measurements at 2.0 GHz

A small shunt capacitance of 0.51 pF would transform the load-pull measurements of set A in Figure 6.31 to the load-pull circles illustrated in Figure 6.34. The small shunt capacitance might have arisen from poor repeatability in the C-type connectors used on the microwave switch. Figure 6.34 compares favourably with Figure 6.31 and the small difference between the two sets of curves could be attributed to the fact that the FET used for the load-pull measurements is significantly different to the FET from which the nonlinear model was derived. A similar discrepancy was found between the set B measurements and nonlinear simulations. Similarly, the addition of a small shunt capacitance to the load-pull measurements improved the comparison with the simulations.

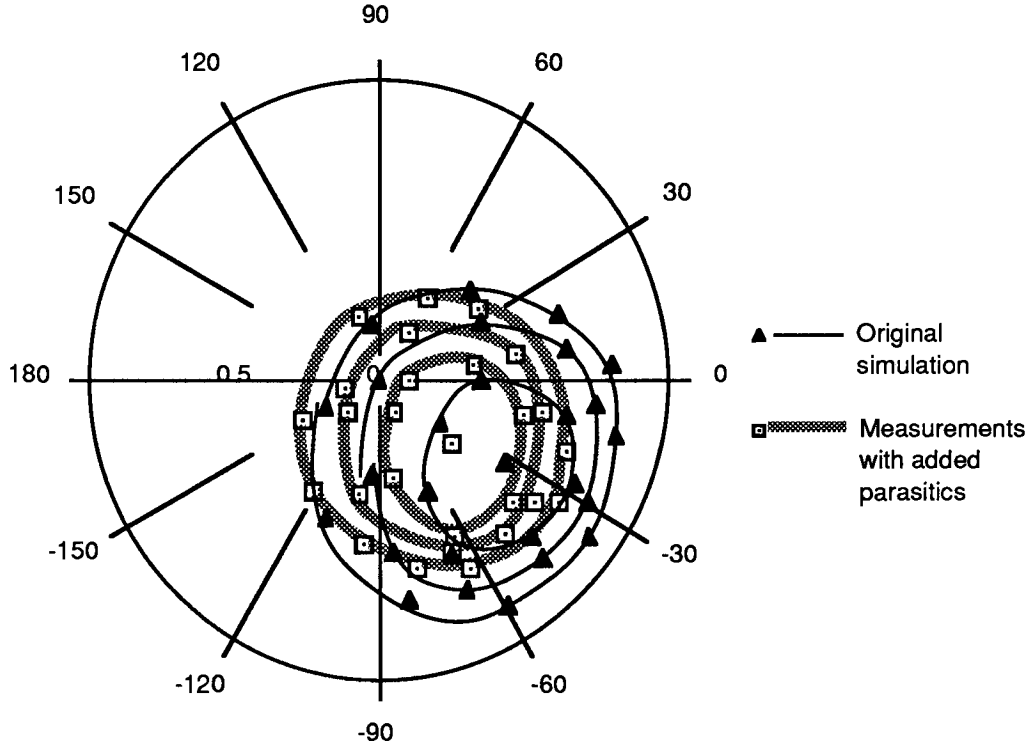


Figure 6.34: Load-pull simulations and corrected measurements at 2.0 GHz

6.4 Conclusions

Linear and nonlinear measurements of test FETs and fabricated MMICs have been compared with similar frequency and time-domain simulations. The S-parameter measurements for the MMIC amplifiers demonstrated that the fabricated circuits differed slightly from the original circuit design. This can be attributed to both the tolerances in the passive elements which are known to exist and also it is known that the characteristics of the MESFET were different to those used in deriving the CAD model. These effects contributed to the divergence between the simulated and measured results.

Small discrepancies were found in comparisons between the nonlinear power saturation measurements and the model simulation. Otherwise, the simulated results were very good, indicating that the nonlinear model was capable of accurately predicting the nonlinear characteristics of the MESFET in MMIC circuits. In retrospect, it would be more desirable to evaluate the nonlinear model using MMICs which were fabricated on the same wafer as the test FETs used to derive the model. Differences between the model and the measurements would therefore only be attributed to either experimental errors or to inaccuracy of the nonlinear model. However, in this project such an approach was not possible, due to the timetable of fabrication runs and the availability of mask space. A greater number of measurements would have ensured a more representative batch of devices had been chosen, but the number of MESFETs measured was limited by the time required to take measurements and process the results.

The load-pull simulations illustrated how a set of output power circles could be obtained by changing the simulated output load impedance. The characteristics of the circles compared well with actual

load-pull measurements, although the optimum load impedance of the simulations (represented by the centre of the load-pull circles) was different from that of the measurements. Further load-pull measurements must be made in order to determine the cause of this offset.

CHAPTER SEVEN - Conclusions

7.1 Summary

The investigation of a nonlinear model for GaAs MESFETs has been carried out so that nonlinear device behaviour in microwave circuits can be simulated. The nonlinear model can been derived in a number of different ways: an analytical approach can be taken, where the MESFET is described in terms of device structure and geometry, or a more empirical approach can be used where the device performance is based on a series of characterizing measurements.

An empirical approach was chosen which meant that the bias dependent characteristics were not derived from process parameters supplied by the manufacturer. These are often only approximations and they were not available in any case. Values for the doping profile, charge concentration, charge distribution, channel length and channel width were not needed, nor were expressions for the charge conduction in the channel, breakdown and built-in voltages. Instead, these were found empirically from actual measurements of fabricated MESFETs.

Essentially, the nonlinear model derives from sets of S-parameter measurements made over a range of bias points. Each set of measurements are fitted to an equivalent circuit model and this can be achieved by introducing only very small errors. Five of the elements in the model were found to vary systematically with bias and these observations could be explained in terms of device physics. The results agreed with many previously published findings [45, 61, 64, 77, 82, 149].

Because the empirical model is derived from high frequency measurements, the effect of frequency dispersion on circuit elements is modelled. Unlike most of the semi-empirical models, which assume

(often incorrectly) that the high frequency current characteristics are the same as the DC characteristics, the current equation of the empirical model is derived solely from high-frequency measurements: DC characterization is only used to test whether a FET is 'typical' in a batch of identical FETs. Frequency dependence was most evident in the output conductance and could be modelled by a series R_xC_x pair, placed in parallel with the channel current source.

The nonlinear model was implemented on ANAMIC, a time-domain simulator which calculates the voltage and current relationships using the state-space approach. The current source was the main nonlinearity in the model and the capacitances C_{gs} and C_{dg} were also strongly nonlinear. A novel feature of this work was that the frequency dependence resistor in the output conductance (R_x) was bias dependent. The value of the nonlinear resistance was calculated from S-parameter measurements at each bias point and could not be accurately assessed from analytical or semi-empirical modelling. The equivalent circuit was found to be very sensitive to changes in C_{dg} and particularly C_{gs}, and both of these parameters were found to change substantially with bias. Therefore, these capacitance were modelled as nonlinear elements and were functions of both gate and drain voltages. The intrinsic resistance R_i was also defined as a nonlinear element, although its effect on the overall large-signal performance of the model was secondary and is omitted in other models.

The nonlinear elements were all expressed as Chebyshev polynomials whose coefficients had been evaluated using the NAG surface fitting algorithms. The current generator required the highest order polynomial, with a total of 53 coefficients and this compared with a total of 110 measured bias points.

A disadvantage of the fully empirical method, is that many measurements are needed to characterize every size of MESFET from every type of process. This is, however, this is much less of a problem than it would have been a few years ago since automated measurement equipment and more sophisticated parameter extraction software are now more widely available. The model is also sensitive to changes in MESFET characteristics between processes and modelling errors will increase where these differences are large. The solution is to ensure repeatability and continuity in the fabrication process.

7.2 Discussion of Results

Small-signal analysis is a subcategory of nonlinear analysis, where a restriction has been placed on the power of the input signal. Therefore, nonlinear models, tested under small-signal conditions, would be expected to compare well to small-signal measurements such as S-parameters. This was illustrated in Section 5.3.4, where the empirical nonlinear model was tested under small-signal conditions and compared to another model, in which the current generator was defined by the DC current (i.e. it had not been corrected for the effects of frequency dispersion in the output conductance). The empirical model was found to be considerably more accurate than the DC model and agreed with the S-parameter measurements very well.

A number of nonlinear measurements were made on single FETs and single stage MMIC amplifiers. The power saturation simulations of the amplifiers compared well with measured power saturation curves. Changes in the characteristics of the saturation curves with bias and frequency were accurately predicted. Some discrepancy was evident especially at low frequencies: the gain of the model was always higher than

the gain in the actual measurements. Similar observations were made between S-parameter measurements and the original small-signal design models for the single-stage amplifiers. The gain of the measured S-parameters was consistently smaller than the model, especially at lower frequencies. The discrepancy between the simulated and measured power saturation curves was due to the fact that the fabricated devices displayed subtly different characteristics from the devices from which the nonlinear model was derived and this was due to fabrications on different batches.

Some nonlinear simulations were carried out where the forward gate breakdown diode had been removed. At low input power levels this did not affect the saturation characteristics but at high power levels (especially at gate biases around 0.0 V) the reduction in the model accuracy was significant, as could be expected.

Other simulations were performed where the resistance of R_x was constant, rather than bias dependent. Results showed that including R_x as a nonlinear element was as important as adding the forward gate breakdown diode. Removal of the R_xC_x pair altogether dramatically decreased the accuracy of the model.

The load-pull simulations demonstrated that the model was capable of producing self-consistant power curves. The shape of the power curves were very similar to measured results although they did not coincide on exactly the same part of the Smith chart. At this stage, it is unclear whether the difference between the measurements and simulations is due to experimental error in making the load-pull measurements, a difference between the FETs used in the load-pull measurements or some unforeseen error. Further load-pull measurements and new nonlinear model component values (derived from the test FETs used in the load-pull experiment) would help to clarify

this observation. At this stage, the differences between the load-pull measurements and simulations are attributed to a combination of the experimental errors and differences in the characteristics of the FETs.

Ideally, the nonlinear measurements should have been made on devices from the same batch run as the modelled FET although, due to the timescales and availability of process runs, this was not possible. It was observed that S-parameter and DC measurements of different batch runs were different, indicating that device characteristics vary from batch to batch. It is difficult to establish how much these differences account for discrepancies between the nonlinear model and experimental measurements.

Finally, an 'on-chip' calibration technique was developed using customized standards. This type of calibration had the advantage that systematic test jig and network analyser errors could be removed right up to the test device, including bonding and packaging parasitics. The calibration technique was successfully characterized for use over the frequency range of 0.5-9.0 GHz.

7.3 Future work

It has been shown that a nonlinear model, derived solely on small-signal S-parameter characterization, enables accurate nonlinear simulations of MESFETs to be made. The overall accuracy and computational efficiency of the model can be improved by carrying out further work.

One of the most important areas for future work involves further testing of the model under load-pull conditions in order to improve the fit between the model and the measurements. Firstly, the original load-pull measurement procedure should be repeated to confirm that no

experimental errors had been made. A nonlinear model derived from the MESFETs in the load-pull experiments should be used in the simulations, rather than a device from a different process, so that all uncertainties relating to differences between different fabrication runs could be removed.

The Chebyshev functions, which were used to express the nonlinear elements, contained many coefficients (in some cases as many as 53 terms). The shape of the nonlinear functions for each element did not change substantially from device to device and therefore a 'generic' equation, containing fewer constants could be used to express some of the nonlinearities. This is similar to the way in which the channel current is expressed in many of the semi-empirical models, where the current equation is fitted to channel current data by varying the size of the constants. However, these equations would have to be considerably more complicated than existing expressions to accurately model the variation of element values with *both* V_{gs} and V_{ds} and this is especially the case for the nonlinear capacitances.

It may also be possible to express the nonlinear elements as look-up tables in the nonlinear simulator, dispensing with the need for any polynomial calculations during simulation. However, reading the look-up table into memory for each iteration of the simulation may prove slower than calculating the more complex polynomials. Additionally, the derivatives of a nonlinear expression derived from a look-up tables may be ill-defined and may require separate
tables.

A quantitative analysis should be made, illustrating how each nonlinear element affects the accuracy of load-pull and power saturation measurements. Results would indicate to what extent the accuracy of the

elements with constants, which would reduce the simulation time.

Power simulations for the existing nonlinear model and another model, where the current generator and RxCx pair had been replaced by the DC characteristics of the FET, would show that the former model is more accurate. This is because the existing model is designed to characterize the effects of frequency dispersion in the output conductance, whereas the model with the DC current cannot. Further comparisons could be made with a nonlinear model containing a current generator derived from pulsed I/V measurements.

Between DC and microwave frequencies the output conductance may change by a factor of three. Although the transconductance varies by only a few percent with frequency, its inclusion in the model may produce more accurate simulations. Therefore the model could be modified to include the effects of frequency dispersion, perhaps using a method similar to Davis and Allenson [155].

Finally, it would be useful to investigate ways in which the simulation time for the model could be reduced. The simulation time increased by a factor of four after the RxCx pair had been added. It may be possible by redefining the topology in some way, or reexpressing the nonlinear elements in order to reduce the time factor.

7.4 Conclusions

This project has demonstrated how an empirical nonlinear model for the GaAs MESFET can be defined solely from S-parameter measurements. The model has been implemented on a time-domain simulator and compared with nonlinear device measurements. It could also be used in harmonic balance simulators to predict the behaviour of MESFETs in nonlinear circuits such as power amplifiers, mixers and

MESFETs in nonlinear circuits such as power amplifiers, mixers and oscillators.

The principal advantage of the empirical approach is that the nonlinear model can be constructed without any knowledge of device fabrication parameters. Thus, the design engineer can build nonlinear circuits without fabrication information from the process engineer. The empirical model is free from errors which would result from an incomplete understanding of GaAs MESFET operation. Whilst physical models are presently capable of predicting GaAs MESFET behaviour in the saturation region with a high degree of detail, they are as yet unable to predict behaviour at low V_{ds} values as every aspect of charge conduction is not yet fully understood.

The time and effort required to make S-parameter measurements and perform parameter extraction at many bias points can be reduced with automation. With a personal computer, network analyser and computer controlled biasing circuitry, a large number of S-parameter measurements can be made and stored. No significant problems can be envisaged in automating the parameter extraction process, as the technique used to extract nonlinear models applies to all devices and already a number of automated multi-bias extraction programs are under development [142, 143].

The results of this project have indicated that a viable nonlinear model can be derived for the GaAs MESFET solely from S-parameter measurements at different bias points. With the appropriate equipment it would be possible to make and extract quick and accurate measurements. Some areas for future work have been suggested which would improve the accuracy and computational efficiency of the model.

REFERENCES

1 W. Shockley: "A Unipolar 'Field-Effect' Transistor", *Proc. IRE* , vol. 40, pp. 1365-1376, November 1952

2 C. A. Liechti: "Microwave Field-Effect Transistors", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-24, pp. 279-300, June 1976

3 J. Eisenberg, W. Ou, J. Archer: "A .5-6 GHz High Gain Low Noise MMIC Amplifier" in *1989 GaAs IC Symp. Tech. Dig.* (San Diego), October 1989, pp. 83-86

4 J. Turner: "GaAs Power FETs", Allen Clark Research Centre Annual Review, pp. 43-47, 1981

5 H. L. Hung, G.M. Hegazi, K.E. Peterson, H.C. Huang: " Design and Performance of GaAs Power MESFET Amplifiers at K and Ka Bands", Microwave Journal, pp. 177-190, June 1988

6 R. S. Pengelly: "Broadband lumped-element X-band GaAs FET amplifiers", in *Proc. 5th European Microwave Conf.* , September 1975, pp. 301-305

7 R. S. Pengelly, J.A. Turner: "Monolithic broadband GaAs FET amplifiers", *Electron Lett.*, vol. 12, pp. 251, 1976

8 H.L. Hung, A. Ezzeddine, F. R. Phelleps, J. F. Bass, H. C. Huang: "GaAs MMIC Power FET Amplifiers at K-Band", in *Proc. 17th European Microwave Conf.* (Rome), September 1987, pp. 255-260

9 Y. Tajima, T. Tsukii, R. Mozzi, E. Tong, L. Hares, B. Wrona: "GaAs monolithic wideband (2-18GHz) variable attenuators", in *1982 IEEE MTT Symp. Dig.* (New York), 1982, pp. 479-481

10 T. Yahara: "A note on designing digital diode loaded line phase

shifters", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-20, pp. 703-704, 1972

11 S. Stapleton, M. Stubbs: "GaAs monolithic frequency halver", *Electron. Lett.*, vol. 22, pp. 173-174, 1986

12 P. Dautriche, V. Pauker, A. Collet: "GaAs monolithic circuits for TV tuners", in *1985 IEEE GaAs Integrated Circuits Symp.* (New York), 1985, pp. 165-168

13 S. Hori, K. Kamei, K. Shibata, M. Tatematsu, K. Mishima, S. Okano: "GaAs monolithic MIC's for Direct Broadcasting Satellite Receivers", *IEEE Trans. Electron Devices* , vol. ED-30(12), pp. 1867-1874, December 1983

14 C. Kermarrec: "The first GaAs fully integrated microwave receiver for DBS applications at 12 GHz", in *Proc. 14th European Microwave Conference* (Liege), September 1984, pp. 749-754

15 J. R. James: "Magical Microwaves: the exploitation of the century", *Proc. IEE*, vol. 136, Pt. H, No. 1, pp. 1-12, February 1989

16 "TeMCAD-CAD package for microwave artwork", British Telecom Business Operations Division, Martlesham Heath, UK

17 "CAD packages for the RF and microwave industry" (EESOF, USA)

18 D. Haigh (ed.), J. Everard (ed.), P. Saul: *GaAs Technology and its impact on circuits and systems: Technology comparison - Gallium Arsenide vs. Silicon* , Chapter 5, London, Peter Peregrinus, 1989

19 P. Ladbrooke: "Modelling of a physical device at microwave", in *Lectures on Computer-aided design and optimization of microwave circuits* (University of Durham), December 1988

20 R. Soares (ed.): *GaAs MESFET Circuit Design* , London, Artech

House, 1988, pp. 227

21 P. Ladbrooke: "Reverse Modelling of GaAs MESFETs and HEMTs", *GEC Journal of Research* , vol. 6, no. 1, pp. 1-9, 1988

22 R. Goyal: *Monolithic Microwave Integrated Circuits: Technology and Design* , London, Artech House, 1989

23 J. Graffeuil, Thesis, University Paul Sabatier, Toulouse, France (1977)

24 M. Ozeki, K. Kodama, A. Shibatomi: "GaAs and related compounds", in *Int. Symp. - Inst. Phys. Conf.* (Oiso), 1981, pp. 323

25 J. Graffeuil, Z. Hadjoub, J. Fortea, M. Pouysegur: "Analysis of capacitance and transconductance frequency dispersions in MESFETs for surface characterization", *Solid State Electronics* , vol. 29, no. 10, pp. 1087-1097, 1986

26 N. Scheinberg, R. Bayruns, R. Goyal: "A low frequency GaAs MESFET circuit model", *IEE Journal of Solid-state Circuits* , vol. 23, no. 2, pp. 605-608, April 1988

27 C. Camacho-Penalosa, C. Aitchison: "Modelling frequency dependence of output impedance of a microwave MESFET at low frequencies", *Electron. Lett.* , vol. 21, no. 12, pp. 528-529, June 1985

28 R. Minasian: "Modelling the MESFET output nonlinearity", *Electron. Lett.* , vol. 15, no. 17, pp. 515-516, August 1979

29 P. Ladbrooke, S. Blight: "Low-field, low-frequency dispersion of transconductance in GaAs MESFETs with implications for other rate-dependent anomalies", *IEEE Trans. Electron Dev.* , vol. ED-35, no. 3, pp. 257-267, March 1988

30 T. Winslow, D. Fan, R.Trew: "Gate-drain breakdown effects upon the large-signal performance of GaAs MESFETs", in *1990 IEEE MTT-S*

Int. Microwave Symp. Dig. (Dallas), May 1990, pp. 315-318

31 SUPER-COMPACT *User Manual* , Version 1.8, Communication Consulting Corporation, Paterson, NJ, November 1984

32 TOUCHSTONE *User Manual* , EESOF Inc., Westlake Village, CA, 1982

33 MDS *User Manual* , Hewlett Packard Co., Palo Alto, Calif., 1989

34 ACADEMY *User Manual* , EESOF Inc., Westlake Village, CA, 1988

35 SPICE *User's Guide* , Department of Electrical Engineering and Computer Science, University of California, Berkeley, California, 1983

36 A. Jastrzebski, M. Sohby: *ANAMIC User Manual: Release 3.0* , University of Kent, Canterbury, 1988

37 CIRCEC: *A Time Domain Program Analysis for Non-linear Circuits* , Thomson Information Service, Paris

38 Microwave Spice User Manual, EESOF Inc., Westlake Village, Calif., 1988

39 T. Brazil, S. El-Rabaie, E. Choo, V. Fusco, C. Stewart: "Large-signal FET simulation using time domain and harmonic balance methods", *Proc. IEE* , vol. 133, Pt. H, no. 5, pp. 363-367, October 1986

40 P. O'Halloran, T. Brazil: "Comparative study of nonlinear circuit simulators", in*14th ARMMS Conference* (Belfast), pp. 161-166, March 1991

41 C. Camacho-Penalosa: "Numerical steady-state analysis of nonlinear microwave circuits with periodic excitation", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-31, no. 9, pp. 724-730, September

1983

42 T. Brazil, S. Scanlan: "Nonlinear Design procedures for single-frequency and broad-band GaAs MESFET power amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. 36, no. 2, pp. 388-393, February 1988

43 S. Maas: *Nonlinear Microwave Circuits* , London, Artech House, 1988

44 R. Davis, J. Gaskell, G. Ball, M. Allenson: "The validation of nonlinear FET modelling and circuit simulation", in *IEE Colloquium on Non-linear Modelling* (London), June 1990

45 H. Willing, C. Rauscher, P. de Santis: "A technique for predicting large-signal performance of a GaAs MESFET", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-26, no. 12, pp. 1017-1023, December 1978

46 C. Rauscher, H. Willing: "Simulation of nonlinear microwave FET performance using a quasi-static model", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-27, no. 10, pp. 834-840, October 1979

47 M. Weiss, D. Pavlidis: "Power optimization of GaAs implanted FETs based on large-signal modelling", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-35, no. 2, pp. 175-188, February 1987

48 Y. Tajima, P. Miller: "Design of brad-band power GaAs FET amplifiers", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-32, no. 3, pp. 261-267, March 1984

49 W. Curtice: "A MESFET model for use in the design of GaAs integrated circuits", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, no. 5, pp. 448-455, May 1980

50 D. Peterson, A. Pavio, B. Kim: "A GaAs FET model for large-signal

applications", *IEEE Trans. Microwave Theory Tech.* , MTT-32, no. 3, pp. 276-281, March 1984

51 W. Curtice, M. Ettenberg: "A nonlinear GaAs FET model for use in the design of output circuits for power amplifiers", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-33, pp. 129-135, February 1985

52 S. Maas, A. Crosmun: "Modeling the gate I/V characteristics of a GaAs MESFET for Volterra-Series Analysis", *IEEE Trans. Microwave Theory Tech.*, vol. MTT-37, no. 7, pp. 1134-1136, July 1989

53 I. Smith: "Dynamic modelling of nonlinear microwave devices", *Electron. Lett.* , vol. 25, no. 18, pp. 1237-1239, August 1989

54 S. Carr, V. Fusco, J. Stewart: "Experimental considerations when measuring MESFET harmonic output power", in *14th ARMMS Conference* (Belfast), pp. 143-146, March 1991

55 E. Graham, R. Chaffin, C. Gwyn: "Large-signal S-parameters: modelling and radiation effects in microwave power transistors", *Microwave Transistors* , pp. 87-99, 1973

56 R. Chaffin, W. Leighton: "Large-signal S-parameter characterization of UHF power transistors", in *Digest of Tech. Papers, Proc. 1973 IEEE Microwave Theory Tech. Int. Microwave Symp.* (University of Colorado), Boulder, June 1973, pp. 155-157

57 S. Mazumder, P. van der Puije: " 'Two-signal' method of measuring the large-signal S-parameters of transistors", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-26, no. 6, pp. 417-420, June 1978

58 R. Tucker: "RF characterization of microwave power FETs", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-29, no. 8, pp. 776-781, August 1981

59 H. Umeda, M. Nakajima: " Analysis of a FET amplifier using power-

dependent S-parameters", *IEE Proc.*, vol. 135, pt. G, no. 4, pp. 162-166, August 1988

60 S. Sze: *Physics of Semiconductor Devices* , New York, Wiley, pp. 340-362, 1969

61 W. Curtice: " GaAs MESFET Modeling and Nonlinear CAD (inv. paper)", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-36, no. 2, pp. 220-230, February 1988

62 S. Sussman-fort, S. Narasimhan, K. Mayaram: "A complete GaAs MESFET computer model for SPICE", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-32, no. 4, pp. 471-473, April 1984

63 H. Statz, P. Newman, I. Smith, R. Pucel, H. Haus: "GaAs FET device and circuit simulation in SPICE", *IEEE Trans. Electron Dev.*, vol. ED-34, no. 2, pp. 160-169, February 1987

64 M. Sango, O. Pitzalis, L. Lerner, C. McGuire, P. Wang, W. Childs: "A GaAs MESFET large-signal circuit model for nonlinear analysis", *IEEE Microwave Theory Tech.-S Int. Conf. Symp. Dig.* (New York), 1988, pp. 1053-1056

65 D. Brookbanks: "A large-signal equivalent circuit model for an ion implanted MESFET", in *IEE Colloquium on Nonlinear Modelling* (London), June 1990

66 A. McCamant, G. McCormack, D. Smith: "An improved GaAs MESFET model in SPICE", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-38, no. 6, pp. 822-824, June 1990

67 S. Carr, V. Fusco, J. Stewart, S. Seawright: "Feasible large-signal MESFET equivalent circuit modelling", in *IEE Colloquium on Nonlinear Modelling* (London), June 1990

68 C. Guo, M. Camiade, D. Rousset, A Cessey, J. Obregon, A. Bert:

"Optimum design of nonlinear FET amplifiers", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-35, no. 12, pp. 1348-1354, December 1987

69 T. Taki: "Approximation of junction field-effect transistor characteristics by a hyperbolic function", *IEEE Journal of Solid-State Circuits* , vol. SC-13, no. 5, pp. 724-726, October 1978

70 T. Kacprzak, A. Materka: "Compact DC model of GaAs FETs for large-signal computer calculation", *IEEE Journal of Solid-State Circuits* , vol. SC-18, no. 2, pp. 211-213, April 1983

71 A. Materka, T. Kacprza: "computer calculation of large-signal GaAs FET amplifier characteristics", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-33, no. 2, pp. 129-135, February 1985

72 V. Hwang, T. Itoh: "An efficient approach for large-signal modelling and analysis of the GaAs MESFET", *IEEE Trans. Microwave Theory Tech.* , vol. MTT-35, no.4, pp. 396-402, April 1987

73 L. Larson: "An improved GaAs MESFET equivalent circuit model for analogue integrated circuit applications", *IEEE Journal of Solid-State Circuits* , vol. SC-22, no. 4, pp. 567-574, August 1987

74 W. White, M. Namordi: "GaAs MESFET model adds life to SPICE", *Microwaves and RF* , pp. 200-204, September 1984

75 A. Jastrzebski: "Nonlinear MESFET models", in *IEE Colloquium on Nonlinear Modelling* (London), April 1988

76 Z. Hu, J. McKeown, T. Brazil, J. Stewart: "Comparison of GaAs MESFET DC models", *1990 IEEE MTT-S Int. Microwave Symp. Dig.* (Dallas), 1990, pp. 311-314

77 J. Golio, J. Hauser, P. Blakey: "A large-signal GaAs MESFET model implemented on SPICE", *IEEE Circuits and Devices Magazine* , pp.

21-29, September 1985

78 R. Goyal, N. Scheinberg, R. Bayruns: "MESFET model improves accuracy, cuts CPU time", *Microwave and RF* , pp. 71-77, April 1987

79 Y. Tajima: "GaAs FET Large-signal model and its application to circuit designs", *IEEE Trans. Electron Dev.* , ED-28, no. 2, pp. 171-175, February 1981

80 L. Larson: "GaAs switched-capacitor circuits", *Ph.D dissertation* , University of California, Los Angeles, 1987

81 C. Snowdon: "Computer-aided design of MMICs based on physical device models", *IEE Proc.* , vol. 133, pt. H, no. 5, October 1986

82 P. Ladbrooke: *MMIC Design: GaAs FETs and HEMTs* , London, Artech House, 1989

83 M. Shur: "Analytical model of GaAs MESFETs", *IEEE Trans. Electron Dev.* , vol. ED-25, no. 6, pp. 612-618, June 1978

84 A. Grove: *Physics and Technology of Semiconductor Devices* , New York, Woley, 1967

85 A. Madjar: "An improved analytical AC large-signal model for the GaAs MESFET", *IEEE Trans. MTT* , vol. MTT-37, no. 10, pp. 1519-1522, October 1989

86 A. Madjar, F. Rosenbaum: "A large-signal model for the GaAs MESFET", *IEEE Trans. MTT* , vol. MTT-29, no. 8, pp. 781-788, August 1981

87 P. Sandborn, P. Blakey: "MESFET simulation oriented toward computer-aided microwave circuit design", *IEEE Trans. MTT* , vol. MTT-38, no. 4, pp. 426-429, April 1990

88 R. Johnson, B. Johnson, J. Baird: "A unified physical DC and AC MESFET model for circuit simulation and device modelling", *IEEE Trans. ED*, vol. ED-34, no. 9, pp. 1995-2001, September 1987

89 M. Khatibzadeh, R. Trew: "A large-signal, analytical model for the GaAs MESFET", *IEEE Trans. MTT*, vol. MTT-36, no. 2, pp. 231-238, February 1988

90 R. Trew, D. Stoneking: "GaAs power MESFET performance sensitivity to profile and process parameter variations", *IEEE Trans. MTT*, vol. MTT-36, no. 12, pp. 1873-1876, December 1988

91 R. Pantoja, M. Howes, J. Richardson, C. Snowdon: "A large-signal physical MESFET model for computer-aided design and its applications", *IEEE Trans. MTT*, vol. MTT-37, no. 12, pp. 2039-2045, December 1989

92 M. Ino, M. Hirayama, K. Kurumada, M. Ohmori: "Estimation of GaAs static RAM performance", *IEEE Trans. ED*, vol. ED-29, pp. 1130-1134, July 1982

93 K. Yamaguchi, S. Asai, K. Kodera: "Two-dimensional numerical analysis of stability criteria of GaAs FETs", *IEEE Trans. ED*, vol. ED-23, pp. 1283-1290, December 1976

94 W. Curtice, Y. Yun: "A temperature model for the GaAs MESFET", *IEEE Trans. ED*, vol. ED-28, pp. 954-962, 1981

95 N. Song, T. Itoh: "Accurate simulation of MESFET by finite element method including energy transport and substrate effects", in *Proc. 1985 European microwave Conf.*, 1985, pp. 245-250

96 R. Englemann, C. Liechti: "Gunn domain formation in the saturated region of GaAs MESFETs", *IEEE Int. Electron. Dev. Tech. Dig.*, pp. 351-354, December 1976

97 R. Englemann: "Low noise Schottky barrier FET transistor (InP)", Hewlett-Packard Laboratories Semiannual Report ECOM-75-1300-1, October 1975

98 R. Englemann, C. Liechti: "Bias dependence of GaAs and InP parameters", *IEEE Trans. ED* , vol. ED-24, pp. 1288-1296, November 1977

99 M. Shur, L. Eastman, " Current-voltage characteristics, small signal parameters and switching times of GaAs FETs", *IEEE Trans. ED* , vol. ED-25, June 1978

100 D. Kennedy, R. O'Brien: "Computer-aided two-dimensional analysis of the junction field-effect transistor", *IBM Journal Res. Dev.* , pp.95-116, March 1970

101 M. Reiser: "A two-dimensional numerical FET model for DC, AC and large-signal analysis", *IEEE Trans. ED* , vol. ED-20, pp. 34-45, January 1973

102 H. Grubin: "Large-signal numerical simulation of field-effect transistors", in *6th Biennial Conf. on Active Microwave Semiconductor Devices and Circuits* (Cornell Univ.), August 1977

103 C. Snowdon, D. Loret: "Two-dimensional hot-electron models for short-gate-length GaAs MESFETs", *IEEE Trans. ED* , vol. ED-34, pp. 212-223, February 1987

104 C. Snowdon, M. Howes, D. Morgan: "Large-signal modeling of GaAs FET operation", *IEEE Trans. ED* , vol. ED-30, pp. 1817-1824, December 1983

105 J. Reynoso-Hernandez, J. Graffeuil: "Output conductance frequency dispersion and low-frequency noise in HEMTs and MESFETs", *IEEE Trans. MTT* , vol. MTT-37, no. 9, pp.1478-1481, September 1989

106 R. Vaitkus: "Uncertainty in the values of GaAs MESFET equivalent circuit elements extracted from measured two-port scattering parameters", in *Proc. IEEE/Cornell Conf. High Speed Semiconductor Devices and Circuits* , 1983, pp. 301-308

107 O. Cutteridge, Y. Zhang: "Computer-aided linear modelling of high-frequency bipolar transistors", *Proc. Inst. Elect. Eng.* , vol. 131, pt. G, pp. 252-260, 1984

108 M. Dowson: "Computer-aided design of equivalent circuit models for microwave frequencies", *Computer-aided design* , vol. 17, no. 8, pp. 353-362, 1985

109 J. Mondal: "Distributed scaling approach of MESFETs and its comparison with the lumped-element approach", *IEEE Trans. MTT*, vol. MTT-37, no. 7, pp. 1085-1090, July 1989

110 E. Ongareau, M. Aubourg, M. Gayral, J. Obregon: "A nonlinear distributed FET model for millimeter-wave circuit design by harmonic balance techniques", in *1990 IEEE MTT-S Int. Microwave. Symp. Dig.* (Dallas), 1990, pp. 323-326

111 J. Muller: "Investigation of GaAs MESFET small-signal equivalent circuits for use in a cell library", in *19th European Microwave Conf.* (London), September 1989, pp. 991-996

112 R. Soares (ed.): *GaAs MESFET Circuit Design* , London, Artech House, 1988, pp. 51

113 Avantek Application Note: *Measurements and modelling of GaAs FET chips* , Avantek Inc., Bowers Ave., Santa Clara, Calif., October 1983

114 Hewlett Packard Product Note: *Specifying calibration standards for the HP 8510 network analyser* , HP Product Note 8510-5A, Hewlett Packard, 1987

115 J. Curran: "Applying TRL calibration for noncoaxial measurements", *MSN & CT* , pp. 91-98, March 1988

116 A. Rhodes: "Measurement methods", in *Lectures on Computer-aided design and optimization of microwave circuits* (University of Durham), December 1988

117 B. Buck, I. Eddison: "On-wafer testing of GaAs monolithic microwave integrated circuits (MMICs)", *Allen Clark Research Centre - Annual Review* , pp. 105-112, 1985

118 Hewlett Packard Product Note: *Network analysis - Applying the HP 8510B TRL calibration for non-coaxial measurements* , HP Product Note 8510-8, Hewlett Packard, 1987

119 Triquint Product Information: *MICRO-S Evaluation test fixture* , Triquint Semiconductor, Group 700, Beaverton, OR, 1987

120 Triquint Product Information: *MMIC Ceramic Package PK-MLC20/8L* , Triquint Semiconductor, Group 700, Beaverton, OR, 1990

121 Plessey F20 Process Design Manual, *Plessey Three-Five Group* , The Plessey Co., Towcester, Northants., 1989

122 Hewlett Packard Product Note: *Measuring noninsertable devices - A new technique for measuring components using the HP 8510B network analyser* , HP Product Note 8510-13, Hewlett Packard, 1987

123 J. Bandler, S. Chen: "Circuit Optimization: The state of the art", *IEEE Trans. MTT* , vol. MTT-36, no. 2, pp. 424-443, February 1988

124 H. Ross: "Introduction to optimization", in *Lectures on Computer-aided design and optimization of microwave circuits* (University of Durham), December 1988

125 H. Ventzel: The Theory of probability, Mir, Moscow, 1973, pp. 339-342

126 R. Soares (ed.): *GaAs MESFET Circuit Design* , London, Artech House, 1988, pp. 203

127 P. Linden, V. Fusco, J. Stewart: "Parallel computing applied to GaAs MESFET parameter extraction", in*14th ARMMS Conference* (Belfast), pp. 138-140, March 1991

128 C. Guo: "Optimum design of nonlinear FET amplifiers", *IEEE Trans. MTT* , vol. MTT-35, no. 12, pp. 1348-1354, December 1987

129 M. Smith: "RF nonlinear device characterization yields improved modelling accuracy", in *1986 IEEE MTT-S Dig.* , pp. 381-384, 1986

130 M. Paggi, P. Williams, J. Borrego: "Nonlinear GaAs MESFET modelling using pulsed gate measurements", *IEEE Trans. MTT* , vol. MTT-36, no. 12, pp. 1593-1597, December 1988

131 H. Fukui: "Determination of the basic device parameters of a GaAs MESFET", The Bell SYStem Technical Journal, pp. 771-797, March 1979

132 R. Goyal: *Monolithic Microwave Integrated Circuits: Technology and Design* , London, Artech House, 1989, pp. 222

133 D. Haigh (ed.), J. Everard (ed.), A. Jastrzebski: *GaAs Technology and its impact on circuits and systems: MESFET modelling and parameter extraction* , Chapter 3, London, Peter Peregrinus, 1989

134 W. Curtice, R. Camisa: "Self-consistent GaAs FET models for amplifier design and device diagnostics", *IEEE Trans. MTT* , vol. MTT-32, no. 12, pp. 1573-1578, December 1984

135 G. Dambrine, A. Cappy, F. Heliodore, E. Playez: "A new-method for determining the FET small-signal equivalent circuit", *IEEE Trans.*

MTT , vol. 36, no. 7, pp. 1151-1159, July 1988

136 R. Minisian: "Simplified GaAs FET model to 10GHz", *Electron. Lett.* , vol. 13, no. 8, pp. 549-541, 1977

137 G. Ghionne, C. Naldi, F. Filicori: "Physical modeling of GaAs MESFETs in an integrated CAD environment: from device technology to microwave circuit performance", *IEEE Trans. MTT* , vol. MTT-37, no. 3, pp. 457-468, March 1989

138 M. Berroth, R. Bosch: "Broad-band determination of the FET small-signal equivalent circuit", *IEEE Trans. MTT* , vol. MTT-38, no. 7, pp. 891-895, July, 1990

139 M. Berroth, R. Bosch: "High-frequency equivalent circuit of GaAs FETs for large-signal applications", *IEEE Trans. MTT* , vol. MTT-39, no. 2, pp. 224-229, February 1991

140 H. Vickes: "Determination of intrinsic FET parameters using circuit partitioning approach", *IEEE Trans. MTT* , vol. MTT-39, no. 2, pp. 363-366, February 1991

141 E. Arnold, M. Golio, M. Miller, B. Beckwith: "Direct extraction of GaAs MESFET intrinsic element and parasitic inductance values", 1990 IEEE MTT-S *Int. Microwave Symp. Dig.* (Dallas), May 1990, pp. 359-362

142 A. Jastrzebski: *SOPTIM User Manual* , Release 3.0, Sobhy and Jastrzebski Microwave Consultants, 1988

143 RoMPE User Manual, *Report OSA-88-RO-19-M* , Optimization systems Associates Inc., Dundas, Ontario, Canada, October 1988

144 A. Jastrzebski: "Parameter extraction for non-linear MESFET models", in *IEE Colloquium on Nonlinear Modelling* (London), April 1988

145 A. Jastrzebski, A. Davies: "Efficient extraction of MESFET models for CAD applications", in*14th ARMMS Conference* (Belfast), pp. 95-98, March 1991

146 R. Soares (ed.): *GaAs MESFET Circuit Design* , London, Artech House, 1988, pp. 198

147 J. Bandler, S. Chen, S. Ye, Q. Zhang: "Integrated model parameter extraction using large-scale optimization concepts" , *IEEE Trans. MTT* , vol. MTT-36, no. 12, pp. 1629-1638, December 1988

148 J. Graffeuil, Z. Hadjoub, J. Fortea, M. Pouysegur: "Analysis of capacitance and transconductance frequency dispersions in MESFETs for surface characterization", *Solid-state Electronics* , vol. 29, no. 10, pp. 1087-1097, October 1986

149 T. Chen, M. Shur: "A capacitance model for GaAs MESFETs", *IEEE Trans. ED* , vol. ED-12, no. 5, pp. 883-891, May 1985

150 R. Goyal: *Monolithic Microwave Integrated Circuits: Technology and Design* , London, Artech House, 1989, pp. 227

151 N. Scheinberg: "Designing high-speed operational amplifiers with GaAs MESFETs", in *IEEE Int. Symp. Circuits and Systems* (Philadelphia), May 1987

152 T. Ducourant: "3 GHz, 150mv, 4 bit GaAs analogue to digital convertor" in *Proc. GaAs IC Symp.* , 1987, pp. 209-212

153 P. Ladbrooke: *MMIC Design: GaAs FETs and HEMTs* , London, Artech House, 1989, pp. 142

154 P. Ladbrooke, S. Blight: "Drift and unpredictability in the Dc and microwave characteristics of GaAs MESFETs due to surface states", in *JEDEC Workshop on GaAs Reliability* (Grenelefe), paper I-1, FL,

October 1986

155 R. Davis, M. Allenson: "The validity of the quasi-static GaAs MESFET model", in *IEE Colloquium on Non-linear Modelling* (London), June 1990

156 J. Hayes (ed.): *Numerical approximation to Functions and Data* , London, Althone Press, 1970

157 M. Cox, J. Hayes: *Curve fitting - a guide and suite of algorithms for the non-specialist user* , National Physics Lab., Teddington, Middlesex, Report NAC26, 1973

158 NAG User Manual, Chapter E02 - Curve and Surface fitting, Numerical Algorithms Group, Publication NP1490/13, 1988

159 C. Clenshaw, J. Hayes: "Curve and Surface fitting", *Journal. Inst. Maths. Applications* , vol. 1, pp. 164-183, 1965

160 M. Sobhy, A. Jastrzebski: "Direct integration methods of nonlinear microwave circuits", in *15th European Microwave Conf.* (Paris), pp. 1110-1117, 1985

161 P. Ladbrooke: *MMIC Design: GaAs FETs and HEMTs* , London, Artech House, 1989, pp. 108

162 Y. Takayama: "A new load-pull characterization method for microwave power transistors", *1976 IEEE MTT-S Int. Microwave Symp. Dig.* (Cherry Hill), June 1976, pp. 218-220

163 M. Lajugie, F. Grossier, A. Silbermann, Y. Bender: "Full characterization of GaAs power MESFET and accurate load-pull contours prediction", *1986 IEEE MTT-S Int. Microwave Symp. Dig.* , 1986

164 Y. Crosnier, H. Gerard, G. Salmer: "Analysis and understanding of

GaAs MESFET behaviour in power amplification", *Proc. IEE* , vol. 134, No. 1, February 1987, pp. 7-16

165 M. Pierpoint, R. Pollard, J. Richardson: "An automated measurement technique for measuring amplifier load-pull and verifying large-signal device models", *1986 IEEE MTT-S Int. Microwave Symp. Dig.*, 1986, pp. 625-628

Appendix A

Listed below is a program, written in HP-BASIC, which was used to store measurement data from the 8510 vector network analyser onto floppy disk.

```
10    ASSIGN @HPIB TO 7
20    ASSIGN @NWA TO 716; FORMAT ON
30    PRINTER IS 1
40    REAL FREQ, MAG, PHASE
50    REAL FIRST, LAST
60    DIM COMMENT$[100]
70    DIM STRING$[100]
80    DIM FR$(1:75)[12]
90    DIM MAG$(1:75,1:4)[14]
100   DIM PHASE$(1:75,1:4)[14]
110   DIM READING$(1:4)[8]
120   INTEGER I
130   REMOTE @HPIB
140   ABORT @HPIB
150   CLEAR @NWA
160   READING$(1)='S11'
170   READING$(2)='S21'
180   READING$(3)='S12'
190   READING$(4)='S22'
200   START=0.1
210   LAST=10.0
220   MASS STORAGE IS "\BLP\JOHN:DOS,C"
```

```
230    INPUT "DO YOU WISH TO CREATE A NEW FILE (Y/N)",
ANS$
240    INPUT "FILENAME FOR DATA STORAGE", FILE$
250    IF ANS$="N" THEN PURGE FILE$
260    CREATE FILE$,1
270    INPUT "WOULD YOU LIKE TO INSET COMMENTS (Y/N)",
ANS$
280    IF ANS$="Y" THEN
290    INPUT "TYPE OUT LINE", COMMENT$
300    COMMENT$="!"&COMMENT$
310    END IF
320    ASSIGN @PATH_1 TO FILE$; FORMAT ON
330    OUTPUT  @NWA;"CONT;CHAN1;"
340    FOR K=1 TO 4
350    OUTPUT @NWA; READING$(K);"LINP;"
360    PRINT "READING"; READING$(K);
370    FOR I=1 TO 75
380    IF I MOD 10=0 THEN PRINT ".";
390    FREQ=FIRST+((I-1)/74)*(LAST-FIRST)
400    MARKER(@NWA, FREQ, MAG, PHASE)
410    A$=VAL$(FREQ)
420    IF A$[1;1]="." THEN A$="0"&A$
430    PNT$="NO"
440    LENGTH=LEN(A$)
450    FOR J=1 TO LENGTH
460    IF A$[J;1]="." THEN PNT$="YES"
470    NEXT J
480    IF PNT$="NO" THEN A$=A$&"."
```

```
490   FOR J=1 TO (8-LEN(A$))
500   A$-A$&"0"
510   NEXT J
520   FR$(I)=A$&"    "
530   MAG$(I,K)=VAL$(MAG)
540   PHASE$(I,K)=VAL$(PHASE)
550   IF MAG$(I,K)[1;1]="." THEN MAG$(I,K)="0"&MAG$(I,K)
560   IF MAG<0.0001 THEN MAG$(I,K)="0.0000000"
570   IF PHASE<0 THEN PHASE=PHASE*(-1)
580   IF PHASE<0.0001 THEN PHASE$(I,K)="0.00000000"
590   MAG$(I,K)=MAG$(I,K)[1;5]&"  "
600   PHASE$(I,K)=PHASE$(I,K)[1;6]&"   "
610   NEXT I
620   PRINT
630   NEXT K
640   IF COMMENT$<>"" THEN OUTPUT @PATH_1;COMMENT$
650   FOR I=1 TO 75
660   OUTPUT STRING$;FR$9I);MAG$(I,1);PHASE$(I,1);MAG$(I,2);
      PHASE$(I,2);MAG$9I,3);PHASE$(I,3);MAG$(I,4);PHASE(I,4)
670   PRINT STRING$
680   OUTPUT  @PATH_1;STRING$
690   NEXT I
700   END
710   SUB  MARKER(@N,F,A,B)
720   OUTPUT  @N;"MARK1";F;"GHZ;OUTPACTI;"
730   ENTER @N;F
740   F=F/1.E+9
750   OUTPUT  @N;"OUTPMARK;"
```

```
760     ENTER @N;A;B
770     SUBEND
```

Appendix B

The following equations enable Chebyshev polynomials to be converted to standard polynomials. The first block of equations is derived for a two-dimensional 3rd order polynomial and the second block is for a two-dimensional 4th order expression. The Chebyshev polynomial coefficients are represented by 'A' terms and the standard polynomial coefficients by 'B' terms.

3rd Order Expressions

$B_{00} = A_{00} - A_{02} - A_{20} + A_{22}$

$B_{01} = -3A_{03} - A_{21} + 3A_{23} + A_{01}$

$B_{02} = 2A_{02} - 2A_{22}$

$B_{03} = 4A_{03} - 4A_{23}$

$B_{10} = A_{10} - A_{12} - 3A_{30} + 3A_{32}$

$B_{11} = A_{11} - 3A_{13} - 3A_{31} + 9A_{33}$

$B_{12} = 2A_{12} - 6A_{32}$

$B_{13} = 4A_{13} - 12A_{33}$

$B_{20} = 2A_{20} - 2A_{22}$

$B_{21} = 2A_{21} - 6A_{23}$

$B_{22} = 4A_{22}$

$B_{23} = 8A_{23}$

$B_{30} = 4A_{30} - 4A_{32}$

$B_{31} = 4A_{31} - 12A_{33}$

$B_{32} = 8A_{32}$

$B_{33} = 16A_{33}$

4th order expressions

$B_{00} = A_{00} - A_{02} + A_{04} - A_{20} + A_{22} - A_{24} + A_{40} - A_{42} + A_{44}$

$B_{01} = A_{01} - 3A_{03} - A_{21} + 3A_{23} + A_{41} - 3A_{43}$

$B_{02} = 2A_{02} - 8A_{04} - 2A_{22} + 8A_{24} + 2A_{42} - 8A_{44}$

$B_{03} = 4A_{03} - 4A_{23} + 4A_{23}$

$B_{04} = 8A_{04} - 8A_{24} + 8A_{44}$

$B_{10} = A_{10} - A_{12} + A_{14} - 3A_{30} + 3A_{32} - 3A_{34}$

$B_{11} = A_{11} - 3A_{31} + 9A_{33} - 3A_{13}$

$B_{12} = 2A_{12} - 8A_{14} - 6A_{32} + 24A_{34}$

$B_{13} = 4A_{13} - 12A_{33}$

$B_{14} = 8A_{14} - 24A_{34}$

$B_{20} = 2A_{20} - 2A_{22} + 2A_{24} - 8A_{40} + 8A_{42} - 8A_{44}$

$B_{21} = 2A_{21} - 6A_{23} - 8A_{41} + 24A_{43}$

$B_{22} = 4A_{22} - 16A_{24} - 16A_{42} + 64A_{44}$

$B_{23} = 8A_{23} - 32A_{43}$

$B_{24} = 16A_{24} - 64A_{44}$

$B_{30} = 4A_{30} - 4A_{32} + 4A_{34}$

$B_{31} = 4A_{31} - 12A_{33}$

$B_{32} = 8A_{32} - 32A_{34}$

$B_{33} = 16A_{33}$

$B_{34} = 32A_{34}$

$B_{40} = 8A_{40} - 8A_{42} + 8A_{44}$

$B_{41} = 8A_{41} - 24A_{43}$

$B_{42} = 16A_{42} - 64A_{44}$

$B_{43} = 32A_{43}$

$B_{44} = 64A_{44}$

Appendix C

Listed below is the Fortran subroutine (USERLIB.f) which contains all of the nonlinear routines used in the nonlinear simulator ANAMIC. The first four functions are empty and the remaining six describe the following nonlinear elements; I_{ds}, R_i, C_{dg}, C_{gs}, I_{ds} (low order polynomial) and R_x.

```
C*************************************************************
C  PART 3C—LIBRARY OF USER FUNCTIONS FOR ANAMIC3  *
C*************************************************************
C              FORTRAN 77 version in double precision
C*************************************************************
C             Created by John Simpson on 13-11-90
C          FUNCTIONS ARE AS FOLLOWS:—
C             AFN5—Vgs(5) by Vds(8) current Ids
C             AFN6—Ri
C             AFN7—Cdg
C             AFN8—Cgs
C             AFN9—Current
C             AFN10—Rx (current corrector)
C*************************************************************
      DOUBLE PRECISION FUNCTION AFNl (NV,X,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION X(NV)
      RETURN
      END
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN2 (NV,X,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION X(NV)
      RETURN
      END
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN3 (NV,X,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION X(NV)
      RETURN
      END
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN4 (NV,X,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
```

```
      DIMENSION X(NV)
      RETURN
END
C*******************************************************
      DOUBLE PRECISIONFUNCTION AFN5(NV,V,KL)
C Parameters: Vgslin, Vds, Egsnonlin
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
      DIMENSION B(6,9),Bl(9),B2(9),B3(9),B4(9),B5(9),B6(9
C B(a,b) where a-l= degree of fit in Vgs and b-l= fit in vds
DATA Bl    / 7.0331E—02,    1.7979E—02,   —4.3192E—03,
+            4.2631E—03,   —3.3972E—03,    2.2945E—03,
+           —1.5741E—03,    8.6434E—04,    4.4890E—04
DATA B2  /   5.0260E—02,    9.8346E—03,   —4.5231E—03,
+            3.4889E—03,   —2.8618E—03,    2.0305E—03,
+           —1.3235E—03,    7.7547E—03,   —3.7217E—04/
DATA B3/     1.7487E—02,   —4.2365E—04,   —2.8980E—03,
+            2.1601E—03,   —1.6812E—03,    1.1927E—03,
+           —7.8829E—04,    4.4623E—04,   —1.8277E—04/
DATA B4    / 3.4612E—03,   —5.8491E—04,   —3.2166E—04,
+            8.3427E—04,   —6.2840E—04,    3.7533E—04,
+           —2.5998E—04,    1.0587E—04,    2.5889E—06/
DATA B5/    —1.7640E—04,    4.7491E—04,    7.4604E—05,
+           —1.8381E—04,    5.1032E—05,    1.9947E—05,
+            5.7302E—05,   —3.9692E—05,    5.5310E—05/
DATA B6 /   —1.3213E—03,   —1.6140E—04,   —9.8622E—06,
+           —1.4405E—04,    1.5564E—04,   —8.7760E—05,
+            6.6978E—05,   —5.1598E—05,    1.3174E—05/
      DO 10 I=l,9
            B(l,I)=Bl(I)
            B(2,I)=B2(I)
            B(3,I)=B3(I)
            B(4,I)=B4(I)
            B(5,I)=B5(I)
            B(6,I)=B6(I)
10          CONTINUE
      MAXVDS=O
      FORC=O
      X=(2*(V(l)+V(3))+3.0)/3.0
      Y=(2*V(2)-10.0)/10.0
      YINV=(—2*V(2)—10.0)/10.0
      IF (X.LT.—l.O) X=—l.O
      IF (Y.GT.l.O) Y=l.O
      IF (Y.LT.-1.0) Y=-1.0
      IF (X.LE.l.O) GOTO 18
            X=l.O
            FORC=V(l)+V(3)
      IF (FORC.GT.0.8) FORC=0.8
18    IF (V(2).LT.O) Y=YINV
```

```
      IF (Y.LT.1.O) GOTO 19
      Y=1.O
      MAXVDS=1.O
      IF (V(2).LT.O) MAXVDS=—1.O
19    AX=ACOS(X)
      AY=ACOS(Y)
      CURR=O
      DO 30 I=1,6
      DO 20 J=1,9
            IF (I.EQ.1) B(I,J)=B(I,J)*0.5
            IF (J.EQ.1) B(I,J)=B(I,J)*0.5
            CURR=CURR+B(I,J)*COS((I—1)*AX)*COS((J—1)*AY)
20    CONTINUE
30     CONTINUE
      CURR=CURR*1000
      IF (FORC.GT.O) CURR=CURR+FORC*CURR/1.6
      IF (V(2).LT.O) CURR=CURR*—1.O
      IF (MAXVDS.EQ.O) GO TO 40
      CURR=CURR+(V(2)—10.O*MAXVDS)*3.0
40    AFN5=CURR
      RETURN
      END
C*********************************************************
C AFN6 - Requires four parameters; the first is the          *
C current across the resistor itself, the second is the      *
C gate voltage  and the third is the drain voltage.          *
C*********************************************************
      DOUBLE PRECISION FUNCTION AFN6 (NV,V,KL)
C Ri resistance = f(I,Vgs,Vds,Egs)
C Parameters: Irc, Vgs, Vds, Egs
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
      DIMENSION B(5,5),XX(5),YY(5)
   DATA B/   4.849067000,    —2.61813770,    —0.43735660,
+           —0.109882150,      0.45323446,
+             0.692877310,     1.18676730,    —0.95363787,
+           —0.961629040,      1.32494480,
+           —1.506854300,    —1.94810740,      5.07305790,
+             1.046010500,   —4.07068100,
+             0.763430110,   —0.09783727,    —1.29277950,
+             1.407473100,   —1.21059750,
+             0.806046290,     1.14725040,     2.28807650,
+           —1.437766300,      3.5356504/
C
      X=(2*(V(2)+V(4))+2.0)/2.0
      Y=(2*V(3)-10.0)/10.0
      IF (X.LT.—1.O) X=—1.O
      IF (X.GT.1.O) X=1.O
      IF (Y.LT.—1.O) Y=—1.O
```

```
      IF (Y.GT.1.O) Y=1.O
      XX ( 1 ) =1
      XX ( 2 ) =X
      XX(3)=X*X
      XX ( 4 ) =X*X*X
      XX ( 5 ) =X*X*X*X
      YY ( 1 ) =1
      YY(2)=Y
      YY(3)=Y*Y
      YY ( 4 ) =Y*Y*Y
      YY ( 5 ) =Y*Y*Y*Y
      RI=O
      DO 11 I=1,5
      DO 10 J=1,5
            RI=RI+B(I,J)*XX(I)*YY(J)
10    CONTINUE
11    CONTINUE
      RI=V(l)*RI/1000.0
      AFN6=RI
      RETURN
      END

C*************************************************************
C AFN7  Requires  three parameters; the first is the voltage     *
C across a linear capactitor CO.  The charge Qdg is              *
C calculated from Qdg = CO * Vdg. The second parameter is        *
C Vgs which is the voltage across Cgs. The 4th order             *
C polynomial calculates the value of voltage Vdg, which          *
C would create charge Qdg. The value returned is the             *
C value calculated in the polynomial minus the origional         *
C value for Vdg. Things are slightly confused bu the fact        *
C that v3 in the USERMODEL is the inverse of the voltage         *
C Vdg. Therefore multiply Vdg by -1.                             *
C The fourth parameter is Cgdo.                                  *
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN7(NV,V,KL)
C Parameters: Vgd, Vgs, Egs, Cgdo
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
      DIMENSION B(5,5),QQ(5),YY(5)
DATA B/      4.6435275,      7.0744342,      1.7732460,
+            -1.2048453,     -0.52881665,
+             0.2586719,      2.6693894,     1.1224574,
+            -1.8368649,     -0.53643640,
+            -0.7089518,      0.0469047,     2.1335486,
+            -1.6555617,     -3.10001960,
+             0.0813670,     -0.1695668,     0.3843811,
+            -1.7388506,     -1.62002800,
+             0.4207158,      0.1361210,     1.4475719,
```

```
+                -0.8162263,        0.39838756/
      Q=((-2*V(l)*V(4)-0.5)/0.5)
      Y=(2*(V(2)+V(3))+2)/2
      IF (Q.LT.—l.O) Q=—l.O
      IF (Q.GT.0.6) Q=0.6
      IF (Y.LT.—l.O) Y=—l.O
      IF (Y.GT.l.O) Y=l.O
      QQ(l)=l
      QQ(2)=Q
      QQ(3)=Q*Q
      QQ(4)=Q*Q*Q
      QQ(5)=Q*Q*Q*Q
      YY ( 1 ) =1
      YY(2)=Y
      YY(3)=Y*Y
      YY ( 4 ) =Y*Y*Y
      YY ( 5 ) =Y*Y*Y*Y
      VDG =O
      DO 11 I=1,5
      DO 10 J=1,5
            VDG=VDG+B(I,J)*QQ(I)*YY(J)
10    CONTINUE
11    CONTINUE
      VDG=VDG*—l.O
C so now the var Vdg is in the same direction to V(l)
      IF (V(l).LT.—8.0) VDG=VDG+(8.0+V(l))
       IF (V(l).GT.O) VDG=VDG+V(l)
      VDG=VDG—V(l)
C make the returned voltage the difference ie E = VO - VT
      AFN7=VDG
      RETURN
      END
C*************************************************************
C AFN8 takes vgs(vl), vds(v2), cgso(v2) and works out first the  *
C charge on CO (QO=CO*vl). Knowing QO and V2, Vlnew can be       *
C calculated. Vlnew-Vl is therefore the voltage of the non       *
C linear voltage source which makes the capacitor appear to      *
C behave as the non-linear capacitor Cgs C The third  is Cgso.   *
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN8(NV,V,KL)
C Parameters: Vgso, Vds, Cgso
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
      DIMENSION B(5,5),QQ(5),YY(5)
DATA B/     -0.84940978,       1.0211989,       -0.30894962,
+            0.30624852,      -0.17094195,
+            0.10808949,      -0.1807408,       0.34925350,
+           -0.56373070,       0.28620342,
+           -0.09542596,       0.2385697,       0.43864401,
```

```
+              0.54867161,      -0.25373632,
+              0.16794571,      -0.4137449,       0.35501372,
+              -0.02494182      -0.08366359,
+              -0.07583968,      0.2119140,      -0.12772429,
+              -0.18997305,      0.18325812/
C note, on next line C0=0.30pF
      Q=((2*V(1)*V(3)+0.6)/0.6)
      Y=(2*V(2)-10.0)/10.0
      FLAG=O
      IF (Q.GE.—1.O) GO TO 8
      Ql=Q
      Q=-1.0
      FLAG=1
8     IF (Q.GT.1.O) Q=1.O
      IF (Y.LT.—1.O) Y=—1.O
      IF (Y.GT.1.O) Y=1.O
      QQ(1)=1
      QQ(2)=Q
      QQ(3)=Q*Q
      QQ(4)=Q*Q*Q
      QQ(5)=Q*Q*Q*Q
      YY ( 1 ) =1
      YY(2)=Y
      YY(3)=Y*Y
      YY ( 4 ) =Y*Y*Y
      YY ( 5 ) =Y*Y*Y*Y
      VG=O
      DO 11 I=1,5
      DO 10 J=1,5
            VG=VG+B(I,J)*QQ(I)*YY(J)
10    CONTINUE
11    CONTINUE
      VG=VG-V(1)
      IF (Q.EQ.1.O) VG=VG+V(1)
      IF (FLAG.EQ.1.O) VG=VG+(Q—Ql)*V(1)
      AFN8=VG
      RETURN
      END
C*************************************************************
C Current equation for the F20 FET derived from Gm using      *
C MATLAB. The current was fitted to a 4th order poly in       *
C terms of Vgs and Vds. No Tau term.                                *
C*************************************************************
      DOUBLE PRECISION FUNCTION AFN9(NV,V,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
      DIMENSION B(5,5),XX(5),YY(5)
DATA B/     0.0178673200,     0.028299576,     0.014669281,
+           -0.0012469576,    -0.000779199,
```

```
+              0.0111913620,     -0.005839964,     -0.014964163,
+              0.0000292348,      0.004218153,
+              0.0007301400,      0.003700258,      0.009321828,
+              0.0011667137,     -0.003879557,
+              0.0032224030,      0.017786900,      0.019202818,
+             -0.0000973138,     -0.004536685,
+             -0.0035367600,     -0.017353416,     -0.018152714,
+             -0.0000122440,      0.004187927/
      X=(2*V(1)+2.0)/2.0
      Y=(2*V(2)-10.0)/10.0
      IF (X.LT.—l.O) X=—l.O
      IF (X.GT.l.O) X=l.O
       IF (Y.LT.—l.O) Y=—l.O
      IF (Y.GT.l.O) Y=l.O
      XX (1) =1
      XX(2)=X
      XX (3) =X*X
      XX (4) =X*X*X
      XX (5) =X*X*X*X
      YY (1) =1
      YY(2)=Y
      YY(3)=Y*Y
      YY (4) =Y*Y*Y
      YY (5) =Y*Y*Y*Y
      CURR=O
      DO 11 I=1,5
      DO 10 J=1,5
            CURR=CURR+B(I,J)*XX(I)*YY(J)
10    CONTINUE
11    CONTINUE
      CURR=CURR*1000
      AFN9=CURR
      RETURN
      END
C*************************************************************
C Expression for non-linear resistor Rx which adds          *
C frequency correction to current in AFN9. Rx is placed     *
C in parallel to I and in series with capacitor Cx which    *
C decouples the resistor from DC bias.                          *
C V(l)=current across resistor
*
C V(2)=gate voltage                                             *
C V(3)=drain voltage                                        *
C V(4)=gate source                                              *
C Rx becomes vl/(rx/1000) because I(mA)=v/r                     *
C*************************************************************
      DOUBLE PRECISION FUNCTION AFNlO(NV,V,KL)
      IMPLICIT DOUBLE PRECISION (A—H,O—Z)
      DIMENSION V(NV)
```

```
      DIMENSION B(lO,lO),Bl(lO),B2(10),B3(10),B4(10),
      B5(10),B6(10),B7(10),B8(10)
DATA Bl/ 1.3445E—02,   —9.3365E—03,   6.6293E—03,  —4.2558E—03,
 +         2.6079E—03,   —1.1722E—03,   2.3550E—04,   3.0316E—04,
 +       —1.7937E—04,    6.3152E—05/
DATA B2/ 9.1457E—03,   —7.6003E—03,   5.1468E—03,  —3.4591E—03,
 +         1.7735E—03,   —6.3241E—04,  —1.0609E—04,   6.1004E—04,
 +       —1.6506E—04,    2.3611E—04/
DATA B3/ 5.1739E—03,   —4.8094E—03,   3.4824E—03,  —2.3618E—03,
 +         1.0385E—03,   —2.8402E—04,  —1.7486E—04,   3.0103E—04,
 +         6.6926E—05,   —2.1lllE—05/
DATA B4/2.1411E—03,   —2.0268E—03,    1.4840E—03,  —9.8818E—04,
 +         3.4715E—04,    9.5194E—06,  —1.8854E—04,   1.2548E—04,
 +         9.4324E—05,   —8.2969E—05/
DATA B5/1.2758E—03,   —9.1594E—04,   8.3894E—04,  —5.7252E—04,
 +         4.9476E—04,   —3.6979E—04,   2.1196E—04,  —2.8391E—04,
 +         1.4486E—04,   —2.3534E—04/
DATA B6/ 1.2681E—03,   —9.4232E—04,   1.0347E—03,  —8.0643E—04,
 +         8.3538E—04,   —7.3369E—04,   5.6432E—04,  —5.7275E—04,
 +         2.9039E—04,   —2.9258E—04/
DATA B7/ 1.0584E—03,   —9.0741E—04,   9.7599E—04,  —8.2367E—04,
 +         7.8719E—04,   —6.7564E—04,   5.4476E—04,  —5.1147E—04,
 +         3.0901E—04, —2.3395E—04/
DATA B8/ 8.9431E—04,   —6.7973E—04,   7.6258E—04,  —6.4768E—04,
 +         7.1258E—04,   —6.0337E—04,   4.9882E—04,  —4.4374E—04,
 +         2.3683E—04,   —2.4931E—04/
      DO 10 I=l,10
      B(l,I)=Bl(I)
      B(2,I)=B2(I)
      B(3,I)=B3(I)
      B(4,I)=B4(I)
      B(5,I)=B5(I)
      B(6,I)=B6(I)
      B(7,I)=B7(I)
      B(8,I)=B8(I)
10    CONTINUE
      X=(2*(V(2)+V(4))+2.0)/2.0
      Y=(2*V(3)-10.0)/10.0
      YINV=(—2*V(3)—10.0)/10.0
      IF (X.LT.—l.O) X=l.O
      IF (X.GT.l.O) X=l.O
      IF (Y.LT.—l.O) Y=—l.O
      IF (Y.GT.l.O) Y=l.O
      AX=ACOS(X)
      AY=ACOS(Y)
      GX=O
      DO 30 I=1,8
      DO 20 J=l,10
            IF (I.EQ.l) B(I,J)=B(I,J)*0.5
```

```
            IF (J.EQ.1) B(I,J)=B(I,J)*0.5
            GX=GX+B(I,J)*COS((I—1)*AX)*COS((J-1)*AY)
20      CONTINUE
30      CONTINUE
        IF (GX.LT.0.0002) GX=0.0002
        IF (GX.GT.0.1) GX=0.1
        RX = 1/GX
        RX = V(1)*RX/1000
        AFN10 = RX
        RETURN
        END
```

Appendix D

The following paper was presented at the 14th Automated RF & Microwave Measurement Society Conference in Belfast, Northern Ireland, March 1991

Modelling of GaAs MESFET's for Large Signal Circuit Analysis and MMIC Design

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Introduction

A novel method of deriving a nonlinear CAD model for GaAs MESFET's has been investigated. The model makes no assumptions about the structure or solid state physics of the GaAs MESFET and is derived solely from small-signal S-parameter measurements made at a number of bias points over the entire operating range of the MESFET. The linear and nonlinear parameters of the equivalent circuit are then extracted, at each bias point, using "TOUCHSTONE", and the nonlinear elements of the equivalent circuit expressed as 2-dimensional Chebyshev polynomials in V_{ds} and V_{gs}. This approach to modelling avoids the simplification inherent in many SPICE (or SPICE derived) models which only allow nonlinear elements to be fixed functions of a single voltage (e.g. modelling of C_{gs} and C_{dg} as reverse-biased diodes with capacitances a fixed function of V_{gs} or V_{gd} respectively).

Other novel features on this model are, firstly, that the current equation is derived solely from the S-parameter measurements and, secondly, that the output conductance of the MESFET model is bias dependent. These features are not possible using standard SPICE, or SPICE derived, models or on models based on d.c. I/V measurements. The use of small-signal S-parameters also avoids errors caused by transconductance dispersion, which is inherent when d.c. current curves are used for predicting a.c. behaviour.

S-Parameter Measurement and Nonlinear Parameter Extraction

The S-parameters used in this model development were provided by Plessey Research (Caswell) Ltd. The S-parameters of a 300 μm × 0.5 μm F20 process MESFET were measured over the frequency range 1–21 GHz at 168 different bias points. These bias points comprised variations in the drain source voltage and the gate-source voltage such that:

$$V_{ds} = 0.2, 0.4, 0.6, 0.8, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 \ volts$$

$$I_{ds} = 4\%, 7\%, 10\%, 20\%, 40\%, 50\%, 60\%, 70\%, 80\%, 90\%, 100\% \ of \ I_{dss}$$

The S-parameters were measured using on-wafer probing, allowing extremely accurate "de-embedded" results to be obtained. The S-parameters at each bias point were extracted by fitting the measured results to an equivalent circuit (Fig. 1) using "TOUCHSTONE" linear CAD. A good fit between the standard small signal model and the measured results was obtained, as shown in Figs. 2 and 3. The 14 element circuit was divided into the linear (i.e. non-bias dependent) and nonlinear (i.e. bias dependent) elements. The linear elements were fixed at those optimised for the $V_{ds} = 5\ V$, $I_{ds} = 50\%\ I_{dss}$ point and kept at these values for all bias points. The six bias dependent elements were: g_m, R_{ds}, R_i, C_{gs}, C_{dg} and τ (*gate transit time*).

The variation of the 6 nonlinear elements can be plotted as a function of bias. Fig. 4 shows the experimental data for the C_{dg} as a function of V_{ds} for various drain current values. The plot of C_{dg} shows that the feedback capacitance cannot be accurately modelled by a simple reverse biased diode as is done for "SPICE" (and SPICE derived) models. This observation can also be made for other bias dependent elements such as C_{gs}, R_i and τ [1].

The variation of these elements with V_{gs} and V_{ds} can be fitted to 2-D Chebyshev polynomials whose coefficients are passed as parameters to the nonlinear simulation

software. Fig. 5 show the 3-dimensional plot of the experimental data and surface fitted Chebyshev polynomials for the nonlinear element C_{dg}.

Nonlinear CAD model and simulated S-parameters

The data derived from the extracted element values is used to create the large signal model in ANAMIC. The nonlinear capacitors are implemented as *linear* capacitances in series with nonlinear voltage dependent voltage sources and the nonlinear resistors are implemented as nonlinear voltage dependent current sources.

Like all nonlinear simulators, ANAMIC requires that the drain-source current is expressed as a function of $V_{g's'}$ and $V_{d's'}$ (the internal node voltages) not, as provided by the small signal model, a transconductance g_m and an output resistance R_{ds}. SPICE models are often implemented using measured d.c. I/V curve and represent the nonlinear voltage controlled current source by one of the "standard" equations as developed by Curtice, Statz or others. In modelling GaAs MESFET's, however, this leads to 2 errors, both caused by material defects in GaAs MESFET's.

Firstly, the MESFET transconductance is a function of frequency. At d.c. the transconductance is up to 10% higher than the of transconductance measured at frequencies above $\approx$1kHz [2]. Secondly, the output resistance is also a function of frequency. The value of output resistance at d.c. is considerably higher than at a.c. frequencies of > 10kHz (typically 3 times) [3]. SPICE simulations of GaAs MESFET's sometimes attempt to model this output resistance variation by placing an a.c. coupled fixed value resistor across the current source to "correct" the value of output resistance. To accurately model this effect, however, the resistor should vary quite considerably with bias.

The model presented in this work (Fig. 6) has two novel features. Firstly, the a.c. output conductance *is* modelled by a bias-dependent resistor (varying between 12.5Ω and >3$k\Omega$) and, secondly, that the nonlinear current source reflects the a.c. values of transconductance and not those from the d.c. current measurements. Both of these features are possible due to the fact that the model is derived solely from S-parameter measurement.

The small-signal transconductance g_m is related, at each bias point, to the current equation as:

$$g_m = \frac{\partial I(V_{gs}, V_{ds})}{\partial V_{gs}}$$

Thus, from knowledge of the transconductance at bias points all over the MESFET operating region, we can reconstruct the current curves by numerical integration:

$$I(V_{gs}, V_{ds}) = \int_{pinchoff}^{V_{gs}} g_m(V_{ds}, V_{gs})\, dV_{gs}\,|_{V_{ds}}$$

Chebyshev polynomials can be used to surface-fit the current values in a similar manner to the bias-dependent circuit elements. When comparing the a.c. derived current curves to the measured d.c. current curves, a difference can be observed. The output resistance is modelled as an a.c. coupled bias dependent resistance whose conductance is the *difference* between the output conductance derived from the computed I-V curves and the output conductance of the small signal model at that bias point.

To test this model, and the enhancements between use of d.c. and a.c. derived current polynomials, the S-parameters of the 300 μm × 0.5 μm MESFET were calculated from the model at a variety of bias points across the operating range. Figure 7 shows the value of S_{22} and S_{21} at one of these bias points (V_{ds} = 2 V, I_{ds} = 100% I_{dss}).

The curves show the measured S-parameters, the simulated S-parameters using the d.c. current points, the simulated S-parameters using a.c. derived current data and finally the simulated S-parameters using a.c. derived current data and the a.c. coupled bias dependent output resistance.

These resimulations showed that the large signal model developed in this work accurately represents the actual state of the GaAs MESFET right across its operating range.

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References

[1] "*MMIC Circuit Design: GaAs FET's and HEMT's*", Peter H Ladbrooke; Artech House, 1989.

[2] "*Low-field Low-frequency Dispersion of Transconductance in GaAs MESFET's with Implications for other Rate Dependent Anomalies*", P.H. Ladbrooke and S.R. Blight; IEEE Trans. Electron Devices **ED-35** 3 pp 257-267.

[3] "*Modelling of Frequency Dependence of Output Conductance of a Microwave MESFET at Low Frequencies*", C. Camacho-Penalosa and C.S. Aitchison; Electron. Lett. **21** 12 pp 528-529.