Methods and Structures for Characterising Integrated Circuit Interconnect Materials and Processes

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Abstract

Advances in the semiconductor industry have introduced the demand for smaller devices with higher performance. Specific interest to this work is the manner in which new materials and processes are being adopted for the fabrication of IC interconnects. Process monitoring and material characterisation is achieved with the use of microelectronic test structures to assist in the development of new fabrication techniques. This thesis investigates a number of emerging areas in interconnect metrology with a concentration on the use of electrical test structures to extract parameters such as line width, sheet resistance, and the overlay of multiple layers.

To address the issue of calibrating optical overlay tools, a novel design for an overlay test structure is described for use as a reference material. It was developed to demonstrate the implementation of a technique devised in collaboration with researchers at NIST and allows the cross correlation between measurements of overlay taken with electrical and optical techniques. This evaluation was demonstrated successfully with close agreement of less than 10 nm between electrical and SEM extracted overlay values from the fabricated test structures.

The next portion of this thesis presents a test structure to evaluate the emerging field of copper interconnects. It is designed to allow electrical measurements from all-copper features, and therefore removes the complications introduced by barrier materials. The structure is intended to be used for reference material applications and traceability of the measurements is provided by a number of previously reported techniques which claim line width measurement accuracy to within 5 nm. The process is then used to fabricate a test chip containing line widths from 10 to 0.55 μm for the evaluation of various methods for ECD extraction. In this work, sheet resistance is extracted from three varieties of test structure designs with an investigation to support the results obtained. Following this, Kelvin-tapped bridge resistor structures are measured electrically to allow the line width to be determined. Three different approaches to analysing this parameter are examined and compared to line width values taken from SEM imaging. The closest agreement between SEM and ECD values is achieved using a new method presented in this thesis. Furthermore, an investigation was conducted to support the choice of this algorithm and the results obtained.

The final area of this work concentrates on the developing field of MEMS thick film power devices. An implementation of traditional interconnect test structures in thick copper conductive tracks is conducted to evaluate their potential for process and material characterisation. This was realised with the combination of thick film photoresist processing and copper electroplating to fabricate the test structures. The results of this study revealed that the methods used in standard interconnect test structures are not easily transferred to the MEMS field. An algorithm is presented which permits values for line width to be extracted from Kelvin-tapped bridge resistors without the use of predetermined sheet resistance values.

Declaration of originality

I hereby declare that the research recorded in this thesis, unaided except where otherwise acknowledged in the text, and the thesis itself was composed and originated entirely by myself in the School of Engineering and Electronics at The University of Edinburgh. This work has not been submitted for any other degree of professional qualification.

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Contents

Declaration of originality . . . iii
Acknowledgements . . . iv
Contents . . . v
List of figures . . . viii
List of tables . . . xii
Acronyms and abbreviations . . . xiii
Nomenclature . . . xiv

1 Introduction **1**
1.1 Motivation . . . 1
1.2 Microelectronic test structures . . . 2
1.3 Objective . . . 5
1.4 Thesis overview . . . 6

2 Background to Semiconductor Metrology **9**
2.1 Introduction . . . 9
2.2 Physical metrology . . . 10
2.2.1 Optical methods . . . 10
2.2.2 Electron microscopy . . . 11
2.2.3 Stylus profilometry . . . 15
2.2.4 Scanning probe microscopy . . . 18
2.3 Electrical metrology . . . 21
2.3.1 Four point probe . . . 21
2.3.2 Test structures . . . 23
2.4 Reference material . . . 29
2.5 Conclusions . . . 30

3 Test Structure for Optical-Electrical Overlay Calibration **33**
3.1 Introduction . . . 33
3.2 Background . . . 33
3.2.1 Optical overlay measurement . . . 34
3.2.2 Electrical overlay measurement . . . 37
3.3 Design . . . 39
3.4 Fabrication . . . 43
3.5 Results . . . 45
3.6 Conclusions . . . 50

4 Fabrication of All-Copper ECD Structures **52**
4.1 Introduction . . . 52
4.2 Background . . . 52
4.2.1 Copper damascene process . . . 53
4.2.2 Barrier layers . . . 56
4.3 Requirements for a Cu ECD test structure . . . 58

4.4 Fabrication process 60
4.4.1 Silicon preform 60
4.4.2 Creation of the preform mould 67
4.4.3 Create trench 70
4.4.4 Copper damascene 77
4.5 Testing strategy 85
4.6 Conclusions 88

5 ECD Extraction from All-Copper Test Structures **90**
5.1 Introduction 90
5.2 Background 90
5.3 Method 93
5.3.1 Sheet resistance 94
5.3.2 Line width 95
5.4 Results 100
5.4.1 Sheet resistance 102
5.4.2 Line width 105
5.5 Conclusions 110

6 MEMS Test Structure Evaluation **113**
6.1 Introduction 113
6.2 Background 113
6.2.1 Thick film photoresist 115
6.2.2 Electroplating 116
6.3 Fabrication process 118
6.3.1 Substrate preparation 118
6.3.2 Mould patterning 119
6.3.3 Track formation 125
6.3.4 Post processing 128
6.4 Results 128
6.4.1 Greek cross 130
6.4.2 Kelvin bridge 131
6.5 Conclusions 134

7 Conclusions and Future Work **136**
7.1 Introduction 136
7.2 Conclusions 136
7.2.1 Test structure for optical-electrical overlay calibration 136
7.2.2 Fabrication of all-copper ECD structures 137
7.2.3 ECD extraction from all-copper ECD structures 139
7.2.4 Evaluation of test structures for MEMS 140
7.3 Future work 141
7.3.1 Test structure for optical-electrical overlay calibration 141
7.3.2 Fabrication of all-copper ECD structures 142
7.3.3 ECD extraction from all-copper ECD structures 150
7.3.4 Evaluation of test structures for MEMS 151
7.4 Final remarks 151

A Publications **153**
A.1 International Conference on Microelectronic Test Structures, ICMTS (Austin, Texas, USA, 2006) 154
A.2 International Conference on Microelectronic Test Structures, ICMTS (Tokyo, Japan, 2007) 161
A.3 International Conference on Microelectronic Test Structures, ICMTS (Tokyo, Japan, 2007) 168
A.4 Frontiers of Characterization and Metrology for Nanoelectronics (Gaithersburg, Maryland, 2007) [In Press] 175

B Process Equipment **181**
B.1 Fabrication 182
B.2 Physical metrology 184
B.3 Electrical test 185

C Run Sheets **186**
C.1 Fabrication of optical-electrical overlay calibration test structures 187
C.2 Fabrication of all-copper ECD test structures 189
C.3 Fabrication of power MEMS test structures 193

References **195**

List of figures

1.1 Fabricated ACME 99 test chip demonstrating $2 \times n$ probe pad layout. . . 4
1.2 Schematic illustration of drop-in and scribe line arrangement for test structure location 6

2.1 Optical extraction of line width from Al track patterned on SiO_2. 12
2.2 SEM extraction of line width from Al track patterned on SiO_2. 14
2.3 HRTEM image of single crystal silicon showing the lattice planes (inset). Reproduced with permission from the National Institute of Standards and Technology 16
2.4 Schematic illustration of the principles of stylus profilometry and the effect of the stylus on the extracted profile. 17
2.5 Schematic illustration of the principles of atomic force microscopy. . . . 19
2.6 AFM scan of an Al track patterned on SiO_2. 20
2.7 Schematic illustration of the principles of four-point probe measurements. 23
2.8 Schematic illustration of van der Pauw measurement of a structure with arbitrary shape and placement of contacts. 25
2.9 Schematic illustration of a van der Pauw cloverleaf structure for reduction of contact errors. 26
2.10 Schematic illustration of commonly adopted patterned test structures used to measure sheet resistance of hatched area based on van der Pauw method. 26
2.11 Schematic illustration of a Kelvin-tapped bridge resistor structure. . . . 27
2.12 A cross-bridge test structure for extracting sheet resistance and line width from a single structure. 28

3.1 Schematic illustration of the overlay components of a multilevel interconnect system. 35
3.2 Schematic illustration of the optical overlay structure. 36
3.3 Schematic illustration of the sliding wire potentiometer structure and measurement technique [59]. 37
3.4 Schematic illustration of the digital vernier structure with measurement principle [68]. 39
3.5 Layout of single test cell of the NIST 47 design with (a) frame-in-frame structure and (b) diagonal arrangement of contacts. 40
3.6 Schematic illustration of reference bar with design related parameters and corresponding binary signature. 41
3.7 Layout of NIST 47 design; the test structure described is the 16 by 18 array of cells indicated. 42
3.8 Fabricated test chip with corresponding magnified image centre of test cell. 45

3.9 Relationship between calculated misalignment measurements vs programmed structure offset for single die. 48
3.10 SEM extraction of overlay achieved from frame-in-frame structure using intensity profile. 49

4.1 Schematic illustration of the main steps in subtractive processing of interconnects. 54
4.2 Schematic illustration of the major steps in damascene processing of interconnects. 55
4.3 Schematic illustration of the major stages in the fabrication of all-copper ECD test structures. 59
4.4 Schematic illustration of the detailed process employed for all-copper ECD structure fabrication. 61
4.5 Cross section of initial experimental batch to demonstrate feasibility of Cu ECD process. 62
4.6 Setup used for TMAH etching of Si wafers 65
4.7 Etched silicon preform with hard mask still in place. 67
4.8 Structure after deposition of both LPCVD and PECVD SiN. 69
4.9 Structure after CMP planarisation of the nitride layers. 70
4.10 Result of SF6 plasma etching of silicon preform to form trench. 71
4.11 Result of XeF_2 vapour etching of silicon preform to form trench using HF dip prior to etch. 73
4.12 Cross section demonstrating the sidewall deformation after the trench oxidation step. 74
4.13 Relationship between the stress and deposition method for "as annealed" and "as deposited" PECVD Si_xN_y films. 76
4.14 Cross sectional SEM of trench after XeF_2 etch and oxidation step. 76
4.15 FIB cross section demonstrating voids in narrow line width Cu tracks as a result of DC PVD sputtering. 77
4.16 FIB cross section of Cu electroplating experiments. 79
4.17 Simple plating setup used for deposition of Cu onto 3 inch wafers. 80
4.18 FIB cross section of wafer with electroplated Cu film. 81
4.19 FIB cross section demonstrating the structure after PVD Cu deposition with RF bias without voids. 82
4.20 Cross section demonstrating the structure after the Cu CMP stage using the iCue 5001 slurry. 83
4.21 AFM profile of a 2.5 μm wide Cu line after CMP with 600Y75 slurry. . . . 85
4.22 AFM profile of 2.5 μm wide cu line after CMP with C7092 slurry. 86
4.23 FIB cross section of final fabricated Cu ECD test structure. 86
4.24 Design of structure used for all-copper ECD reference material 87

5.1 Fabricated test chip used for Cu ECD analysis using the NIST 35 design. 94
5.2 Test structures used to extract sheet resistance for Cu interconnect features (a) Greek cross (b) corner-tapped box cross and (c) side-tapped box cross 95
5.3 Test structure used to extract line width for Cu interconnect features . . 96
5.4 Images identifying the presence of facets in intersecting angles of Cu lines. 98

5.5 Results of resistance versus current measurements on electrical test structures employed in this study. 102
5.6 Results of Rs values measured from a single die using the three van-der-Pauw structures shown in figure 5.2. 103
5.7 Results for the individual segment analysis 107
5.8 Results for the multiple segment analysis 107
5.9 Results for the individual segment analysis with δL correction factor included 108
5.10 Results for the multiple structure analysis of separate columns 108
5.11 Results for the multiple structure analysis with all structures 109
5.12 Results of equivalent Rs values extracted using the multiple structure analysis. 110

6.1 Typical setup employed in the electrochemical deposition of metals on semiconductor wafers. 117
6.2 Overview of MEMS mould process to form Cu conductor 119
6.3 Result of film thickness against spin speed experiments. Also displayed are the data sheet values provided by Futurrex for reference. 121
6.4 Schematic illustration of the dimensions of the edge bead effect on the resist. Included is the point at which edge bead removal (EBR) is used to dissolve the thicker resist. 123
6.5 Cross sectional SEM demonstrating the result of a PEB using 80 °C. . . . 124
6.6 Cross sectional SEM demonstrating the result of a PEB using 100 °C. . . 124
6.7 Cross sectional SEM demonstrating the dome shaped top to the Cu track or the "bread loaf" effect. 127
6.8 Cross sectional SEM demonstrating the near rectangular shaped profile of the Cu track. 127
6.9 Optical micrograph of the cross-bridge test structure used in this study. . 129
6.10 Relationship between resistance and drawn line width of the structures. 132
6.11 Relationship between line width values and drawn line width of the structures for both electrical and SEM measurements. 133
6.12 Results of equivalent Rs values based on dimensional measurements and resistance values for each structure. Extracted Rs value from the Kelvin bridge measurements (dashed line) are presented for comparison. 134

7.1 Illustration of a portion of the silicon showing a typical representation of facets seen using single anisotropic wet etch. 144
7.2 Schematic illustration of the process suggested for the hybrid etch approach to reduce the facet formation. 145
7.3 Illustration of a portion of the silicon showing expected result of using hybrid etch approach. 145
7.4 Schematic illustration of the process steps involved in dual-layer patterning technique. (Note direction cross section is drawn from, top or side) 147
7.5 SEM of a sample fabricated using the dual-layer patterning technique. Note that there is still a small degree of rounding at the intersecting angle between the two lines. 148

7.6 Layout of test chip for dual-layer patterning evaluation. 149

List of tables

3.1 Selected data from electrical overlay structure. 46

4.1 Results of uniformity experiments for TMAH wet etch on (110) Si wafers. 66
4.2 Plating recipe used for damascene copper plating trials. 78
4.3 Recommended process conditions for Cu CMP trials. 83

5.1 Drawn dimensions of Kelvin-tapped bridge resistor structures 96

Acronyms and abbreviations

AFM	Atomic Force Microscope
Al	Aluminium
CD	Critical Dimension
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
Cu	Copper
CVD	Chemical Vapour Deposition
DC	Direct Current
ECD	Electrical Critical Dimension
FIB	Focused Ion Beam
HF	Hydrofluoric Acid
HRTEM	High Resolution Transmission Electron Microscopy
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
LPCVD	Low Pressure Chemical Vapour Deposition
MEMS	MicroElectroMechanical Systems
NIST	The National Institute of Standards and Technology
OCD	Optical Critical Dimension
PECVD	Plasma Enhanced Chemical Vapour Deposition
PVD	Physical Vapour Deposition
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscopy
SOI	Silicon On Insulator
SPM	Scanning Probe Microscopy
TEM	Transmission Electron Microscopy
UV	Ultra Violet

Nomenclature

δL	Line length shortening variable
I	Current
I_X	Current at terminal X with relation to ground
I_{XY}	Current measured between terminals X and Y
L_i	Length (or tap separation distance) of segment i.
ρ	Resistivity
R	Resistance
Rs	Sheet resistance
Rs_n	Sheet resistance of structure n
t	Thickness
V	Voltage
V_X	Voltage at terminal X with relation to ground
V_{XY}	Voltage difference between terminals X and Y
W	Line width
W_m	Measured line width
W_d	Drawn line width

Chapter 1
Introduction

This chapter outlines the motivations and objectives behind the work conducted and reported in this thesis. It provides a brief background to semiconductor devices and the integration of interconnect wiring schemes to meet the requirements of todays modern technology. After this introduction, the role of microelectronic test structures is described to support the work conducted for the latter chapters. The primary area of interest is the use of semiconductor metrology techniques coupled with novel test structure designs to enable material and process characterisation. Finally, after a brief look at the objectives of this work, an overview for the remainder of this thesis is presented.

1.1 Motivation

Microelectronic devices have been around for well over a half a century now. The first implementation was demonstrated in 1947 with the creation of the point contact transistor at Bell Laboratories [1]. Since then the microelectronics community has seen huge advances in fabrication technology, allowing billions of these transistors to be placed onto a single chip. This has enabled the fabrication of items such as microprocessors, memory chips, discreet transistors and many more electronic components. The key to the future of semiconductors is the ability to decrease the size of the devices whilst at the same time improving their performance.

The many transistor devices contained on a single chip communicate with one another, as well as the outside world, with microscale wires used to electrically connect them together. These wires, or *interconnects*, occupy a large portion of the area on an Integrated Circuit (IC) chip. As the speed and performance of these devices increases then so must the capability of the interconnect wires. The parameters of an interconnect system which affect the operating conditions of the signals are its resistance and capacitance. These are collectively referred to as the R-C timing delays.

The work presented in the remainder of this thesis centres around the improvement of the resistance component. This has led to improvements in fabrication methods along with the choice of new materials for the implementation of the wires and tracks. However, in this world of shrinking dimensions the tolerance and room for error during fabrication becomes increasingly small. This is such that the performance of a device can be dramatically influenced by any number of parameters involved in the interconnect system such as the physical dimensions of the tracks and the connections between different layers of tracks. In order to evaluate and understand these parameters, interconnect metrology is adopted to provide a measure of the performance and characteristics of a particular process, design or material. Test structures play a key role in allowing parameter extraction and process/design qualification. With parameter extraction, semiconductor manufacturers can decide whether a device has met design specifications and if not it is typically scrapped. This prevents applying functional testing to poorly fabricated wafers, which is a costly and time consuming process.

1.2 Microelectronic test structures

Microelectronic test structures are an essential resource to the development and manufacture of successful IC devices. The structures themselves typically consist of lithographically formed patterns in the same manner that the actual IC patterns are defined. They allow engineers within the semiconductor community to characterise a device both during processing as well as after it has been fully fabricated. These test structures permit the extraction of parameters relating to (amongst others) their electrical and physical properties, depending on the design and implementation. The key challenge in test structure design is creating features which allow a reliable, efficient and accurate measure of the parameters under investigation.

Test structures are found in a wide area of semiconductor manufacturing including:

- Process control and development [2]
- Modelling and simulation parameter extraction [3]
- Reliability and defect testing [4]

- Equipment characterisation [5]
- Material property analysis [6]
- Metrology [7]
- Yield analysis [8]

There are two main methods used to extract parameters from these test structures. The first is with the use of tools that determine the physical parameters of the structures including line width, trench depth, roughness, etc. For the most part these are well defined and established techniques used regularly during semiconductor manufacture. The challenge is interpreting how the physical parameters of the interconnects affect their functionality and performance aspects. Electrical parameter extraction, on the other hand, provides a functionally relevant picture of the various properties associated with the operation of a component or circuit. On the down side, the electrical measurements and analysis can be more time consuming and, in most circumstances, require physical contact to be made to the structures resulting in possible contamination due to the generation of particles.

Electrical measurements are provided for with *probe pads* to allow wires to be connected from the device under test (DUT) to the equipment being used for parameter extraction. There are two methods for arranging the probe needles or tips to make physical contact with the probe pads. The first is achieved using micromanipulators to move the tips in X, Y, and Z directions relative to the surface of the wafer. In this method, the user arranges the probe tips to correspond to the pitch that the probe pads are patterned. On the other hand, probe cards place the tips in a fixed arrangement to correspond to the pad layout. This method is commonly used for repetitive measurements from regular test structure layouts.

The act of positioning of the wafer and contact of the arranged probe tips to the probe pads is referred to as *probing*. In manual probing the user aligns and lowers the arranged probe tips to contact the test structures across the surface of a wafer using a microscope and X-Y-Z wafer table. This presents a flexible system, independent of design, for electrical contact. However, it can prove to be time consuming to setup and conduct measurements from large arrays of structures. The alternative is to use semi-automated or automated probing. In this approach, a probe station is programed with

information pertaining to the dimensions and layout of a test chip. After the wafer has been aligned in the test system, either manually by the user or automatically using pattern recognition software, the probe station automatically positions and moves the wafer or probes to contact with the test structures. These automated systems are linked to the test equipment to coordinate the measurements and positioning of the wafer.

In most cases, the probe pads themselves are placed in standardised row and column format to facilitate automated probing routines with dedicated hardware. The most common arrangement is the "2 × n" pad layout which allows a single probe card to be used to probe all the structures within the whole chip [9]. An image of an ACME[1] test chip demonstrating a "2 × n" pad layout is found in figure 1.1. To minimise the test structure area, probe pads tend to occupy the smallest possible footprint without being so small that they are difficult to make repetitive contact with during probing. Pad sizes typically range in the order of 40 to 120 μm square.

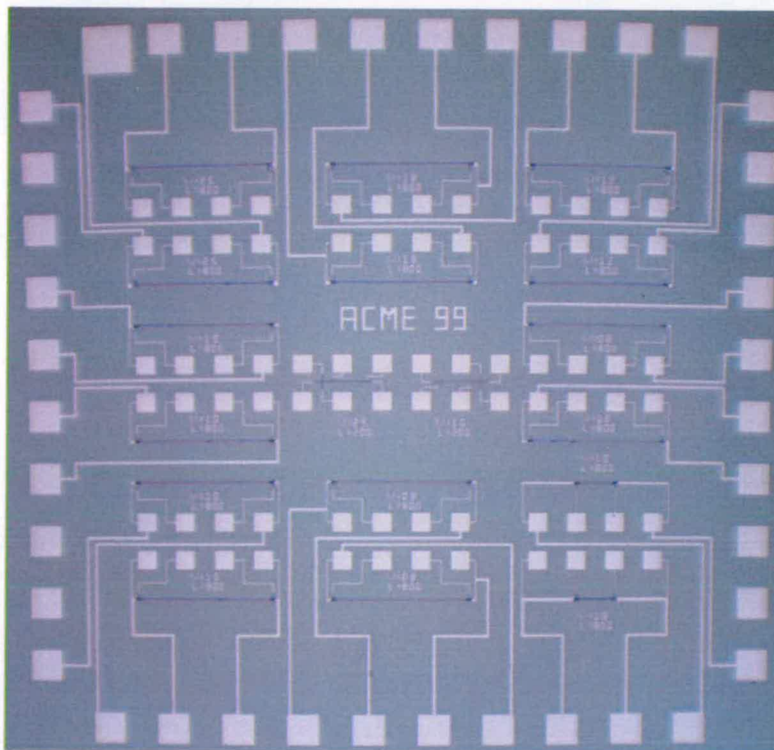


Figure 1.1: *Fabricated ACME 99 test chip demonstrating 2 × n probe pad layout.*

There are two main arrangements by which the test structures are incorporated into a production semiconductor wafer, both of which are illustrated in figure 1.2. The first

[1] ACME:Aluminium to Copper Metallisation project undertaken by The University of Edinburgh.

is with "drop-in" chips, where the test structures occupy their own die site in place of a product die on the wafer being manufactured. This allows the designer to create a vast number of test structures in the large area that has been allocated. One of the drawbacks with this method is that the drop-in sites occupy what would have other wise been a product chip, and as such a balance between the number of drop-in chips required to provide a clear picture for process control while maintaining the greatest possible number of product chips must be maintained to maximise the profit of that particular wafer. As the structures occupy a whole die, a mask change is required to pattern the drop in sites and additional process time is introduced.

The alternative is to incorporate the test structures into unused portions of the wafer. While it is rare to find these unused areas within the boundaries of an IC device, the most common location is in the scribe channels of the wafer [10]. In this manner the test structures allow the extraction of parameters, while still maximising the profit of the wafer by not occupying valuable semiconducting real estate, as the scribe channels are consumed during the wafer dicing step. As the scribe channels extend across the full surface of the wafer and hence the test structures as well, a vast amount of information can be gathered from a single wafer. This extends to the ability to use wafer mapping from the large array of data obtained to characterise the process and equipment used. The one draw back to this method is that the scribe channels tend to be only as wide as the tool used for dicing requires. As a result, the available area for the test structures is limited, introducing the requirement for unique designs to fully exploit the available space.

Just as test structures are unique to a specific problem or property of interest, the analysis techniques applied to them for data extraction forms an essential element in material and process characterisation. Each test structure generally has one or more methods for deriving the desired parameters and tends to be application specific as to which algorithm selected.

1.3 Objective

The work presented in this thesis aims to benefit the metrology community through the development of new techniques and processes for test structure implementation

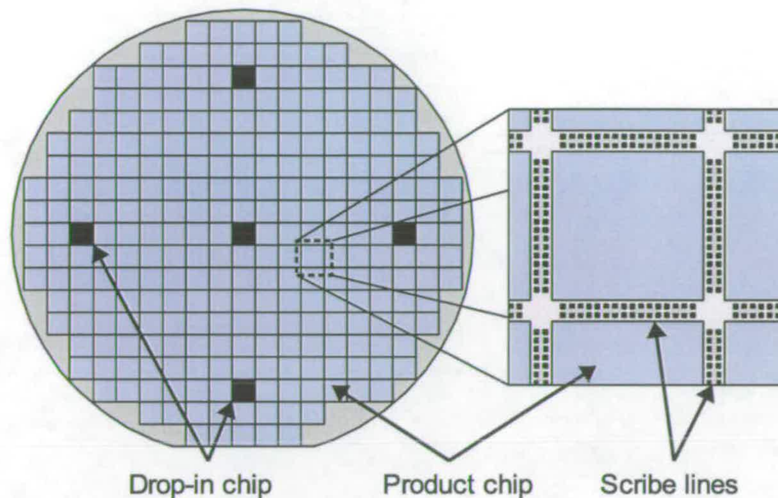


Figure 1.2: *Schematic illustration of drop-in and scribe line arrangement for test structure location*

and analysis. More specifically test structures to electrically measure parameters such as overlay, line width and sheet resistance of IC interconnects. Novel processes are described in this thesis which allow these test structures to be implemented in manners specific to the application they are investigating. Furthermore, full analysis based on existing as well as some new methods are presented on these structures. The work described addresses three main areas of IC metrology. The first is the manner in which the alignment of multiple layers in a interconnect system is measured using optical tools and how it relates to the electrical functionality of the systems. The next area is the use of copper interconnects in modern day semiconductor IC systems, where a test structure is required to serve as a critical dimension reference material to allow material and device characterisation. Finally, the emerging field of thick film power MEMS devices similarly demands the use of test structures for process monitoring and as such an evaluation into the implementation and analysis of these test structures is required. The information contained in this dissertation has been partly published in five conferences [11–15]. A copy of some of these papers is presented in Appendix A.

1.4 Thesis overview

This thesis is the result of studies conducted for the degree of Ph.D. and is divided into three main sections. The first provides a detailed background to the work being

conducted, including an in depth literature review in to the subject area. After this, the experimental procedures and results along with their analysis are presented. Finally conclusions are drawn and further work on the subject areas is suggested. An overview of the chapters is as follows:

Chapter 2: Background to semiconductor metrology. Semiconductor metrology provides engineers with the ability to extract a wide number of parameters from a specific process or design. A detailed review of the published work on these subjects is presented in this chapter in relation to the manner in which they are adopted for this thesis. The scope of the literature survey ranges from blanket film metrology to patterned structure testing, and from physical extraction methods to the more functionally relevant electrical methods. Finally, the concept of reference material is introduced as a means for calibrating and evaluating semiconductor metrology equipment.

Chapter 3: Test structure for optical-electrical overlay calibration. This chapter presents a novel design and implementation for a test structure which addresses one of the key areas of interconnect manufacturing. This structure serves as an application specific reference material for the cross correlation between electrical and optical measurements of overlay values. A brief overview of the subject is presented before looking at the technique demonstrated in the design of the structure. A standard fabrication process, traditionally found for aluminium tracks, is described for the implementation of the test structure. Then, a detailed analysis of the structure based on both electrical and SEM measurements is presented.

Chapter 4: Fabrication of all-copper ECD structures. Due to the demand for lower resistance interconnects, copper has been introduced as the preferred interconnect material of choice amongst many semiconductor manufacturers. A unique process is described in this chapter which combines the experience and techniques gained through silicon ECD structures with the need for an all-copper ECD structure. This novel approach results in a test structure which allows the extraction of line width and sheet resistance values from copper tracks which are not encapsulated by conducting barrier films. Traceability is provided between measurements taken using electrical extraction techniques and from methods such as AFM, CD-SEM, and HRTEM. After detailing the integration of the various steps involved, an overview of

the measurement strategy is explained.

Chapter 5: ECD extraction from all-copper test structures. Using the process described in Chapter 4, a thorough investigation was conducted to evaluate the process and test structure design used. Electrical measurements were taken with a DC parametric test system to extract values for both sheet resistance as well as line width of the all-copper features. Three variations of van der Pauw cross bridge resistors were employed to extract sheet resistance measurements. On the other hand, line width measurements are provided for with multiple-tapped Kelvin bridge resistor structures. SEM images have also been taken as a means for comparison to the electrical results. A number of different algorithms are reviewed and evaluated to determine values for line width and sheet resistance. Finally conclusions are drawn regarding the design and process used for the fabrication of the devices based on the results of the measurements.

Chapter 6: MEMS test structure evaluation. While the previous experimental chapters have focused on novel techniques and test structures to extract parameters from interconnect features with small dimensions, this chapter evaluates the area of thick film MEMS interconnects. These types of structures enable designers and manufacturing companies to integrate components, which were once placed separately on a PCB, on top of the semiconductor control circuitry. A technique for fabricating thick film copper conducting wires is evaluated for power MEMS devices. The fabrication has been demonstrated based on two enabling technologies, including thick film photoresist as well as electroplating of conductive materials. The goal of this study was to evaluate the use of traditional test structures for characterisation and process monitoring in MEMS thick film manufacturing. These structures have been measured and results presented based on an analysis of this data.

Chapter 7: Conclusions and future work. This final chapter reviews the information presented in this thesis and draws conclusions based on the experimental work which has been conducted. A more in depth look at the areas for further work is also presented including suggested designs and plans to allow this work to continue into the future.

Chapter 2
Background to Semiconductor Metrology

2.1 Introduction

One could argue that the art of measurement dates back to the scientific programs of Galileo Galilei, where his motto was: "Count what is countable. Measure what is measurable. And what is not measurable, make measurable." Toward the end of the 19th century and at the beginning of the 20th century, the importance of measurement and the need for agreement between nations was recognised to be a requirement for the advancement of trade, technology and science. As a result, *metrology*, the science of measurement, became an important part of the infrastructure of a nation. So much so, that governmental organisations were appointed to develop and maintain a system of national measurements, often called "National Metrology Institutes" [16]. Metrology is widely used in today's rapidly changing market place, from industrial manufacturing to biological experiments. The semiconductor industry similarly relies on the use of metrology techniques to provide control and feedback during both development and manufacture of devices. One specific area of interest is the use of metrology in semiconductor interconnect fabrication.

In relation to the work conducted for this thesis, interconnect metrology has been divided into two types of extraction method: physical and electrical. The physical measurements relate the properties of a process or device to the International System of Units (SI), such as the metre. Typical parameters include film thickness, feature widths, relative placement of features, structure profiles, etc. These are also referred to as the critical dimensions (CD) and are the dimensions of the geometrical features formed during wafer processing. On the other hand, electrical methods provide a measure of the circuit behavior of a specific material or device. Typical parameters in electrical metrology include capacitance, inductance and resistance. As will be seen

later, these parameters can be used to extract information relating to the physical properties of a feature. The unique challenge posed is to determine the functional relevance of each method and furthermore to determine the relationship between the physical and electrical properties of a process or design.

2.2 Physical metrology

The techniques described in this section are based on those currently in practice in semiconductor manufacturing environments. The measurements themselves are either conducted on blanket films, the actual device, or test structures designed specifically for the purpose of parameter extraction.

2.2.1 Optical methods

Optical microscopy is one of the most commonly used methods for metrology and inspection during wafer manufacture. It is the preferred tool due to the non-invasive and non-destructive nature of the measurements. Furthermore, the optical measurements can be integrated for real-time monitoring due to their robustness, high accuracy, low cost and small footprint. Optical microscopes are commonly found for use in inspection systems to monitor and qualify processes. However, in the context of the work conducted in the later chapters of this thesis, optical microscopes can also be used for metrology to extract line width from structures.

The most simple form of optical metrology is the use of a microscope with suitable hardware and software to extract the required parameters. Typically the additional hardware consists of an imaging camera that can provide suitable resolution to match the dimensions of the sample, along with image processing software to extract the desired parameters. This arrangement tends to be used to measure the lateral dimensions on a wafer, such as line width and feature placement (or overlay). Measurements are taken based on the reflected light intensity captured across a broad band wavelength range. Optical CDs (OCD) can be extracted using a single scan taken perpendicular to the feature of interest and applying data analysis techniques on the reflected light intensity profile. A typical method for analysis involves setting a threshold level on the profile and measuring the points at which the profile intersects

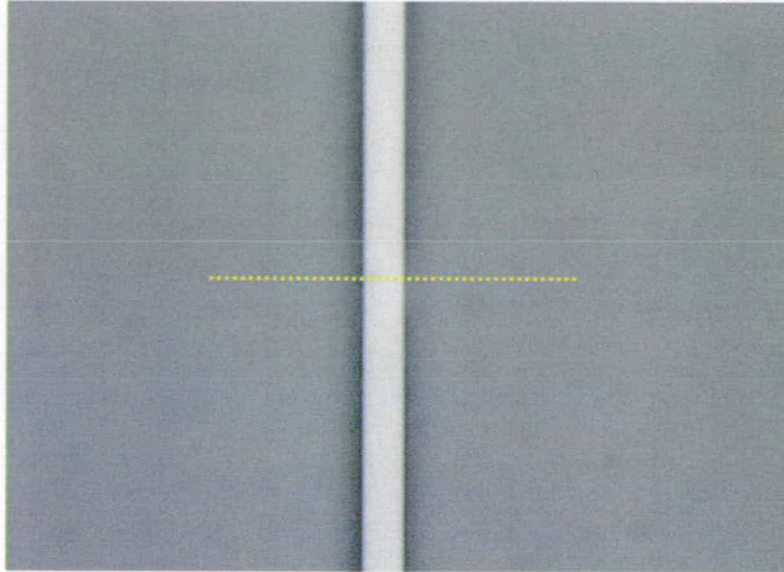
the threshold. Figure 2.1 displays an optical image taken from an Al track and the resulting intensity profile with threshold and equivalent line width marked.

The one draw back to this method is that as CDs decrease in size, optical measurements are not able to provide the accuracy required because the wavelengths used by these tools are comparable to the patterned dimensions. New developments using deep ultra-violet (DUV) and extreme ultra-violet (EUV) are allowing optical methods to be extended beyond the traditional methods. Other optical CD measurement techniques include scatterometry [17] and optical profilometry [18]. However, these are beyond the context of the work conducted for this thesis.

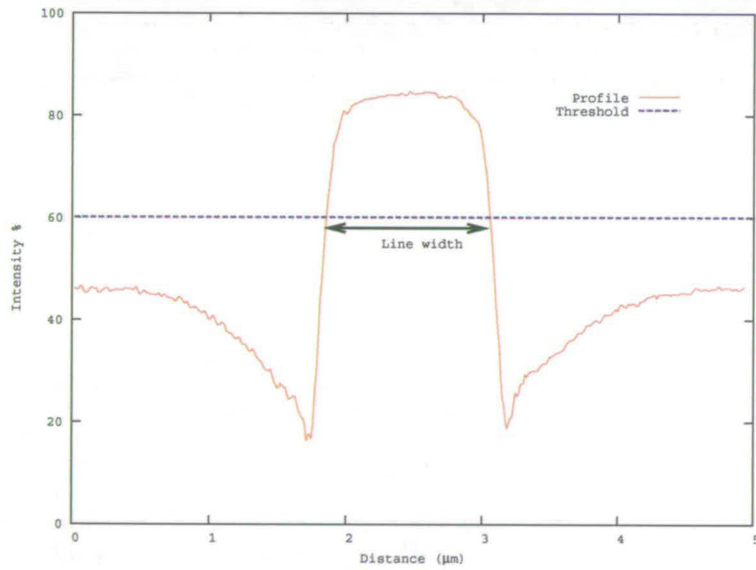
2.2.2 Electron microscopy

The use of electron microscopes in semiconductor metrology has been well established and understood. The principle of this technique is that a beam of electrons are accelerated towards and focused on the surface of the sample being inspected. The image is formed based on the signal strength of the detected electrons after they have interacted with the surface of the sample. The two main types of electron microscope are the transmission electron microscope (TEM) and the scanning electron microscope (SEM). The TEM was the first type of electron microscope developed and forms an image from the electrons which have traveled through the sample and into a detector located behind it. The SEM, on the other hand, detects the secondary electrons (SE) that result from the interaction between the surface and the primary beam of electrons which are reflected off of the surface of the sample and into the detector. Both types of microscope can be found in modern day CD metrology environments.

The use of an SEM to determine line width is performed in a similar manner to that used for optical line width measurements. A profile is extracted based on the intensity of the SE detected from a single line scan perpendicular to the feature being measured. For comparison with the optical line width extraction example presented in figure 2.1, an SEM image and corresponding intensity profile is displayed in figure 2.2. With this profile, a threshold or similar edge detection method can be used to determine the line width. To facilitate these type of measurements in semiconductor metrology, special SEMs for CD extraction, known as CD-SEMs, are used.



(a) Optical image

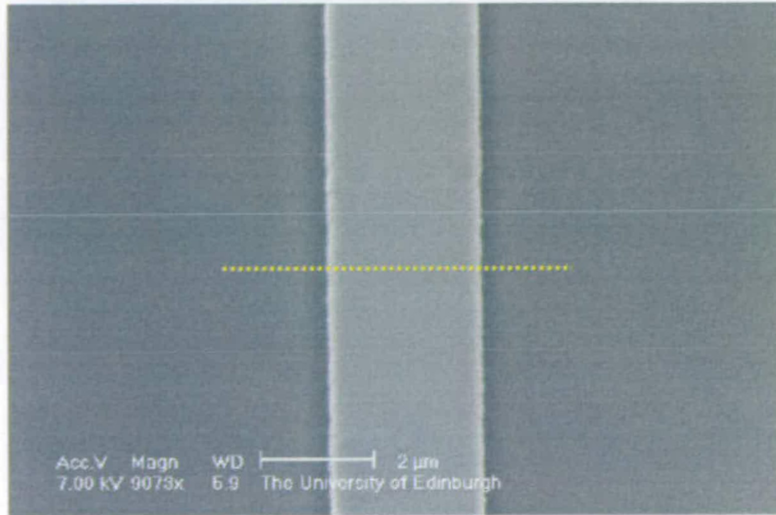


(b) Intensity profile

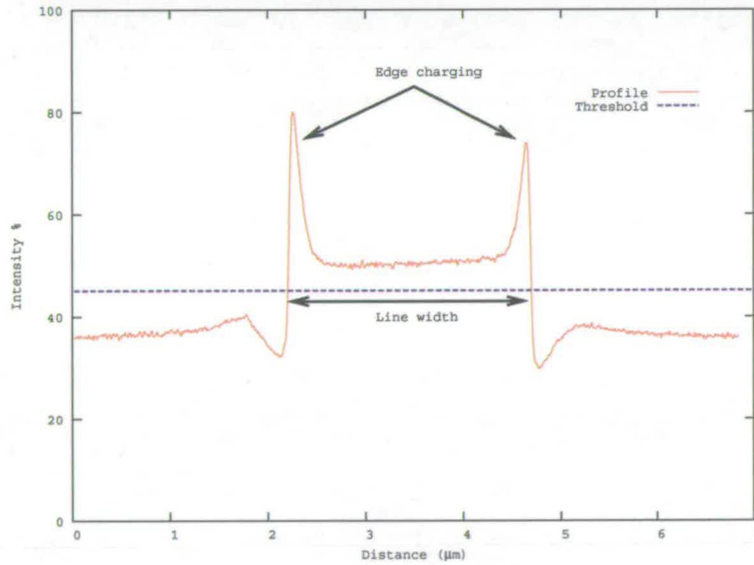
Figure 2.1: *Optical extraction of line width from Al track patterned on SiO_2.*

There are a number of problems associated with CD metrology in SEM tools. The first is the charging effects caused by the material interactions with the electron beam. As can be seen in both the SEM image as well as the intensity plot in figure 2.2, the intensity of the Al track (as with other metal lines) is much higher at the edges than in the centre. This makes it difficult to determine the "true" edge of the track and hence determine the line width. One way of reducing this effect, as reported by Postek [19], is to use a low accelerating voltage on the SEM. Further more, this paper describes the use of backscattered electrons (BSE) detectors, as opposed to the SE detectors traditionally used in SEM imaging, to provide better edge detection for CD metrology purposes. The second problem associated with SEM metrology is the fact that the electron beam can result in the deposition of materials, mainly carbon, onto the surface of the sample during imaging. The result being that the extracted line width appears larger than the actual dimensions of the feature being measured. Finally, similar to optical techniques, as the SEM image is taken perpendicular to the surface of the sample, it does not contain sufficient information regarding the sidewall profile of the features being measured. However, a number of researchers are currently working on special techniques to extract sidewall information from a CD-SEM. Marschner and Stief [20] have demonstrated the ability to reconstruct the sidewall profile of a structure based on two images taken from a sample with varying tilt angles. Alternatively, Su et. al. [21] use a technique where the sidewall angle is determined from a single top down image. In this approach, the sidewall angle is calculated from the height of the track and the lateral difference between the edges of the top surface and those of the bottom interface of the track as detected from the extracted profile from a feature. However, this method requires the use of additional metrology tools and measurement processes to determine the step height of the track.

Another technique commonly used in semiconductor inspection and metrology is cross-sectional SEM imaging (X-SEM). A pre-requisite to this method is that samples must be prepared prior to imaging using either cleaving, dicing, or polishing tools to expose the area of interest. The imaging procedure requires that the sample be mounted and rotated using suitable fixtures and hardware to allow sample tilting and manipulation. Typically X-SEM images are taken at 90° relative to the wafers surface. When observing a sample in X-SEM analysis, information about the line width, feature height, sidewall profile, defects and many more areas can be determined.



(a) SEM image



(b) Intensity profile

Figure 2.2: *SEM extraction of line width from Al track patterned on* SiO_2.

Unfortunately the preparation routines are time consuming operations, sometimes requiring specialist equipment. Additionally, as this approach is a destructive technique, it cannot be used for in-line monitoring.

The use of TEMs in semiconductor metrology is rarely seen due to the fact that samples must be thin enough to allow the transmission of electrons. As such, samples must be prepared using a number of available techniques to reduce the area of interest to a region a few hundred nanometres thick. Such techniques are similar to those used for X-SEM sample preparation, including dicing, cleaving, polishing and focused ion beam (FIB) milling [22]. However, Warren and Stein [23] demonstrate a technique to overcome this preparation routine, where the sample to be analysed is deposited directly over a thin membrane of silicon nitride supported by a silicon frame which is defined in the substrate. Using this method, line width can be extracted from the intensity profile generated by the transmitted electrons.

Although TEM is not viable as an in-line metrology tool, a considerable amount of work has been conducted by researchers at NIST to develop techniques for extracting CDs from single crystal Si samples when analysed under a high resolution transmission electron microscope (HRTEM) [24–27]. The authors detail the fabrication of CD line width features patterned in (110) mono-crystalline Si substrates. When the samples are observed in cross section, through an isolated patterned line in an HRTEM, the crystal lattice is made apparent, as seen in figure 2.3. By counting the number of lattice planes across the width of the patterned structure and with a knowledge of the atomic spacing of the silicon lattices, the line width can be determined. In work by Allen et. al. [26] specially designed image analysis software is described that allows the lattice planes to be counted in an automated fashion based on a fringe detection algorithm. This decreases the time required for the measurements and increases the throughput. The authors of this work claim that this method can produce values with uncertainties less than 2.5 nm for line width.

2.2.3 Stylus profilometry

The next method of extracting dimensional information is based on the mechanical interactions between the sample and a measurement stylus. As a result it is not subject to the charging and edge effects seen with electron microscopy. In stylus profilometry a

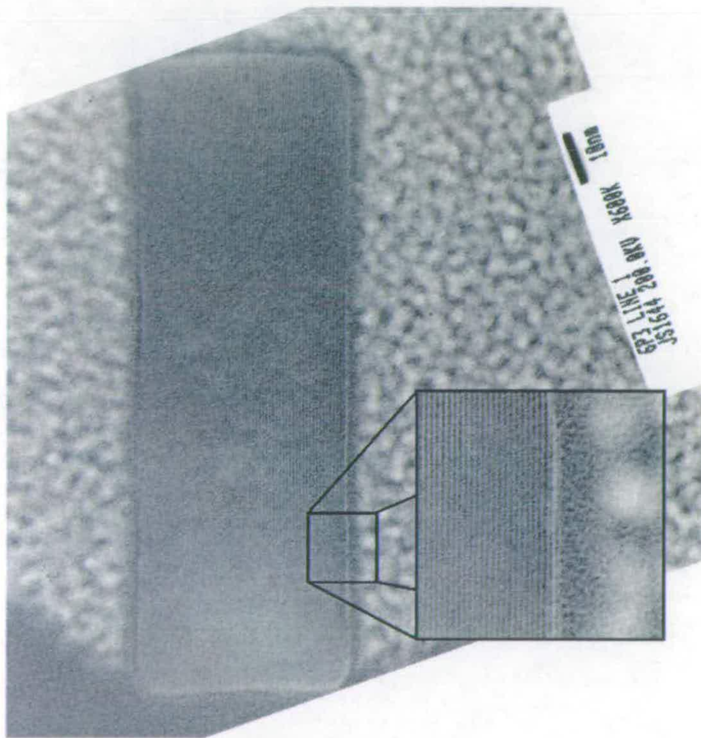


Figure 2.3: *HRTEM image of single crystal silicon showing the lattice planes (inset). Reproduced with permission from the National Institute of Standards and Technology*

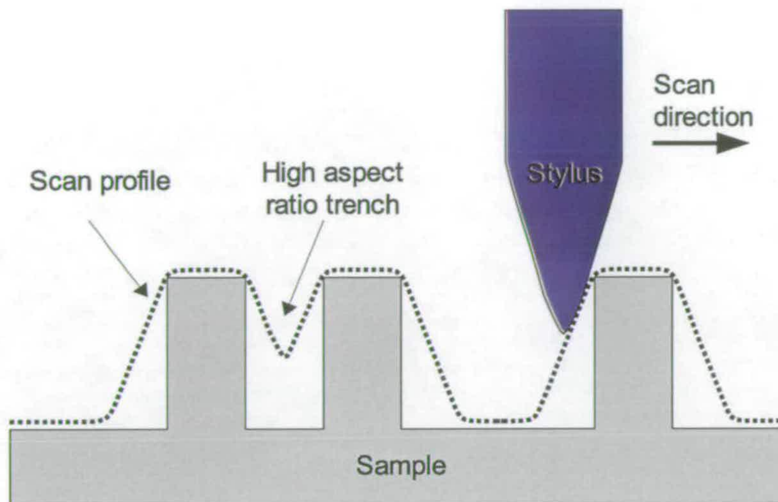


Figure 2.4: *Schematic illustration of the principles of stylus profilometry and the effect of the stylus on the extracted profile.*

stylus is driven across the surface of a sample while the vertical position is monitored, typically with a capacitance sensor, to determine height variations. This method is used to extract two dimensional (2-D) information about surfaces based on a single line scan containing height values. However, there are some tools which allow three dimensional (3-D) information to be gathered from a stylus profilometer using an X-Y raster scan technique.

As this metrology tool uses physical contact with the sample being measured, the stylus must be mechanically robust to prevent excessive wear. As a result, the stylus tends to be rather large in comparison to the feature being measured. Figure 2.4 illustrates the principles and typical issues associated with stylus profilometry. The first issue is that the extracted scan profile is only able to measure information about the sidewalls of features where the sidewall has a slope less than the angle of the stylus. Furthermore the stylus is unable to measure trenches which have an aspect ratio greater than the dimensions of the stylus used to measure it.

Line width is determined using the extracted profile based on either a threshold limit or the point in which the stylus detects the edge of the top side of the structure. However, the main use of this method is to extract topographic information such as surface roughness or step height of features.

2.2.4 Scanning probe microscopy

Scanning probe microscopy first began with the development of the scanning tunneling microscope (STM) which, in turn, lead to the more commonly used atomic force microscope (AFM) [28]. As in stylus profilometry, the AFM uses a tip to scan across the surface of the sample. However, instead of using physical contact with the surface, it monitors the interactions between the sample and the probe, which is positioned just above the surface of the sample. In AFM the van der Waals forces between the tip and the surface are used to determine topographic information about the sample. These forces result in varying degrees of deflection of the probe depending on the properties of the material used both for the tip and the sample. A diagram illustrating the components of an AFM operated in tapping mode (described later in this section) is seen in figure 2.5.

The probe itself is fabricated using MEMS processing techniques to produce a small tip fixed to a cantilever. As described by Wolter et. al. [29], traditionally the tips are fabricated from silicon to form a small radius point. The drawback of this process is that the silicon tips are fragile and the probes have a finite lifetime before they need to be replaced. To address this issue, Shibata et. al. [30] describe a technique used to fabricate AFM tips from diamond films. In comparison to the silicon tips, the benefits include longer life times for the probes and also the ability to be used in harsh chemical environments. The physical displacement of the probe is monitored using an optical measurement system [31] where a light source (often a laser) is aimed onto the back of the cantilever whilst a detector monitors the position of the reflected beam of light as shown in figure 2.5.

There are a number of different modes that an AFM can be operated in, with the choice depending on the properties of the sample being measured and the desired results. Of relevance to the work described in this thesis is the use of *tapping mode* AFM (TM-AFM) which is one of the most widely used instruments for atomic-resolution imaging [32]. In this mode, the probe is vibrated at, or near, its resonant frequency while the tip is scanned across the surface of the sample. The tip deflection that results from the forces that occur during the interaction between the probe and the sample is monitored. The probe is scanned in a raster like fashion across the surface to create either a 2-D or 3-D image of the sample. The image of a sample is formed from a reconstruction of the

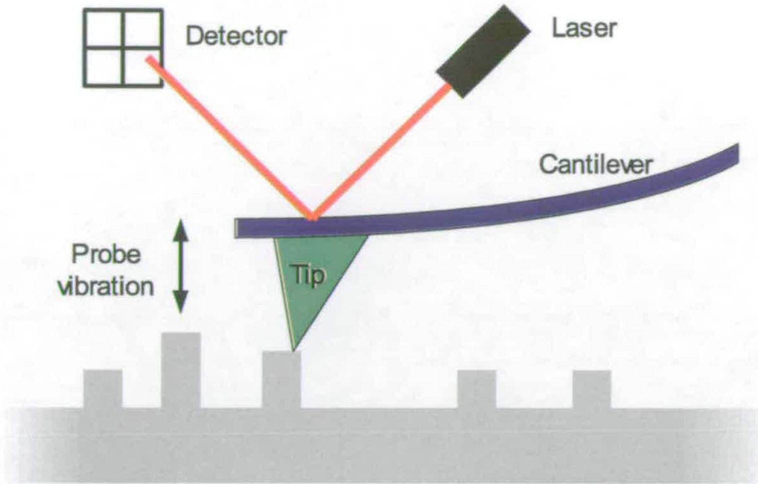
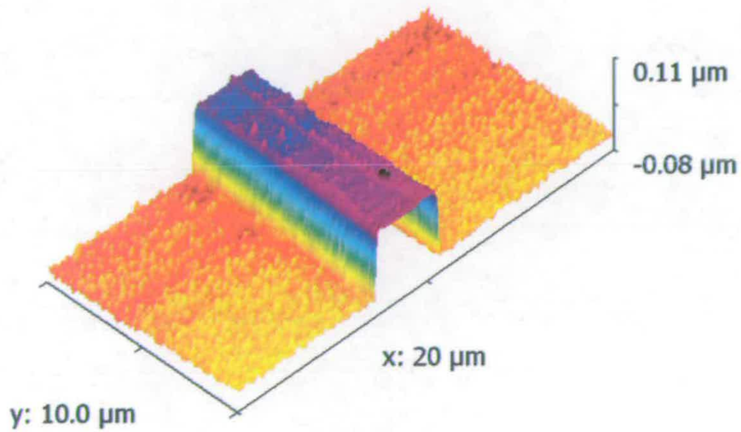


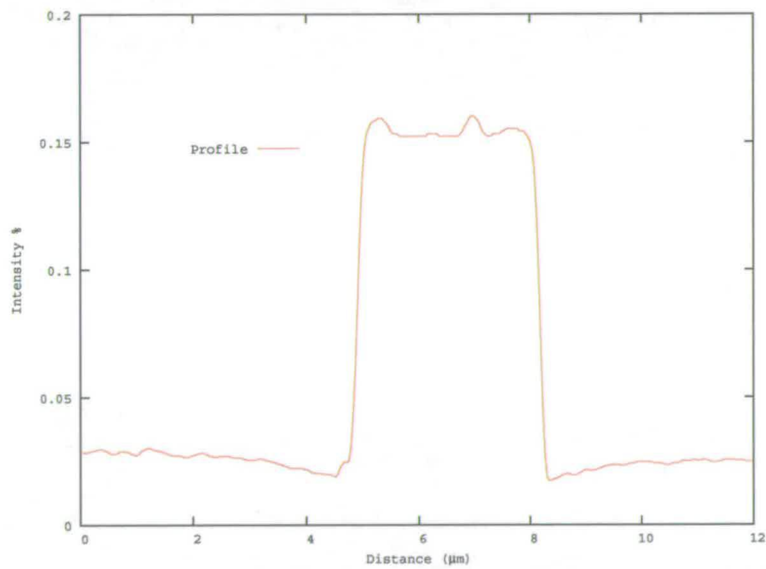
Figure 2.5: *Schematic illustration of the principles of atomic force microscopy.*

height information against the position of the tip. An example of such an image is shown in figure 2.6(a). In this image it can be seen that the AFM provides such high resolution that the surface roughness of the field area dielectric can be seen. From this 3-D image a single line scan can be extracted, as shown in figure 2.6(b) to measure the line width. This can be achieved either by setting a threshold or by determining the point at which the tip detects the edges of the sample.

The use of micro machining means that the dimensions of the tip are typically much smaller than those used for stylus profilometry. Although the measurements themselves are still subject to the effects of tip geometry on the extracted profile, as seen with stylus profilometry, they are less significant. Furthermore, special tips can be obtained that have been designed to allow measurements of high-aspect ratio trenches by using a long, narrow profile. One such probe is realised with the use of carbon nanotube technology as described by Morimoto et. al. [33]. In this paper, the authors describe the "STEP-IN" AFM approach where the thin carbon nanotube tip is of small enough radius to step into the trenches of a sample. Further more, the tips are angled at 15° to allow accurate detection of the leading edge of the sidewall at the bottom of a trench or feature. However, this does not provide the accuracy required to extract critical dimension parameters for the sub-100 nm requirements of modern day semiconductors. One key enabling technology to allow AFM to be used as a metrology tool for line width parameters is the use of unique "boot shape" tips to image the sidewalls of a feature. Guerry et. al. [34] as well as Martin and Wickramasinghe [35]



(a) 3-D reconstruction of scanned data



(b) Single line scan profile

Figure 2.6: *AFM scan of an Al track patterned on SiO_2.*

report on the use of such a tip to measure sidewalls. This allows the user to gather information such as sidewall roughness and line width over the entire vertical profile. Such tips are used in conjunction with special AFM systems called CD-AFM (also 3D-AFM) [36]. It is these tools which enable accurate results for feature metrology in the semiconductor industry [37].

2.3 Electrical metrology

While the techniques described above allow CDs to be extracted based on the physical dimensions of the features, the true behavior of an IC component is realised using electrical testing. Electrical metrology takes two forms, measurements from blanket films and those from patterned test structures. The blanket measurements reflect properties of the materials under evaluation, including film thickness and resistivity, and tend to be used to characterise the process used to deposit them. Test structures, on the other hand, can be designed to extract parameters ranging from material properties to dimensional information including thickness and line width. The test structures also allow information to be extracted regarding design parameters used in an IC.

2.3.1 Four point probe

The four point probe (FPP) measurement is one of the most widely used techniques for evaluating the resistance of a blanket film or substrate as discussed by Schroder [38]. Its use was originally developed by Wenner [39] to measure the resistivity of the earth. In 1954 the FPP was adopted by Valdes [40] for use in the semiconductor industry to measure the resistivity of wafers. This method evolved from the use of a simple two electrode setup which made contact to the surface of a conducting sample where impedance is sensed between the two terminals. The problem with this method is that contact effects between the electrodes and the surface contribute to the measured impedance values, making the interpretation of the measured data more difficult. This has since been overcome with the introduction of the four electrode arrangement illustrated in figure 2.7, in which four probes are placed in-line and equally spaced onto the surface of the sample. Typical values for the separation of the contact electrodes (S) are in the order of 0.5 to 1.5 mm. The measurement technique is

commonly referred to as the *Kelvin technique* where a constant current source is used to force a current through the outer pair of electrodes and at the same time the potential difference between the inner pair of electrodes is sensed. Provided the four points are placed collinearly, the resistivity of a material is found using the formula in equation (2.1), where ρ is the resistivity of the material, and I is the current forced and V is the potential difference sensed during the measurement.

$$\rho = 2\pi S \left(\frac{V}{I}\right) \tag{2.1}$$

However equation (2.1) is based on the assumption that measurements are taken from a symmetrical sample of semi-infinite lateral and vertical dimensions. In semiconductor applications, the thickness (t) of the conducting material being measured is typically much less than the electrode separation distance. Additionally, when using silicon wafers, the films are limited to the lateral dimensions of the wafer. Therefore corrections are introduced to address these finite geometries, the result of which allows the resistivity (ρ) of the thin material to be found using the modified formula in equation (2.2), provided the thickness is known.

$$\rho = \frac{\pi t}{ln(2)} \frac{V}{I} \tag{2.2}$$

Conversely, if the resistivity of a material is known, equation (2.2) can be solved to extract the thickness of the layer. However, it is not always possible to know either the resistivity or thickness of a material and therefore *sheet resistance* is introduced as a means to characterise films without the need for dimensional information. The sheet resistance (Rs) is equivalent to the resistivity divided by the thickness of the film (equation (2.3)) and represents the resistance of a square area (length $\times$ width) of conducting film. Values for Rs are expressed in units of ohms per square ($\Omega/\Box$).

$$Rs = \frac{\rho}{t} \tag{2.3}$$

One downside to the FPP method is the prerequisite for large areas of un-patterned film with which to make contact, therefore making it difficult to integrate with

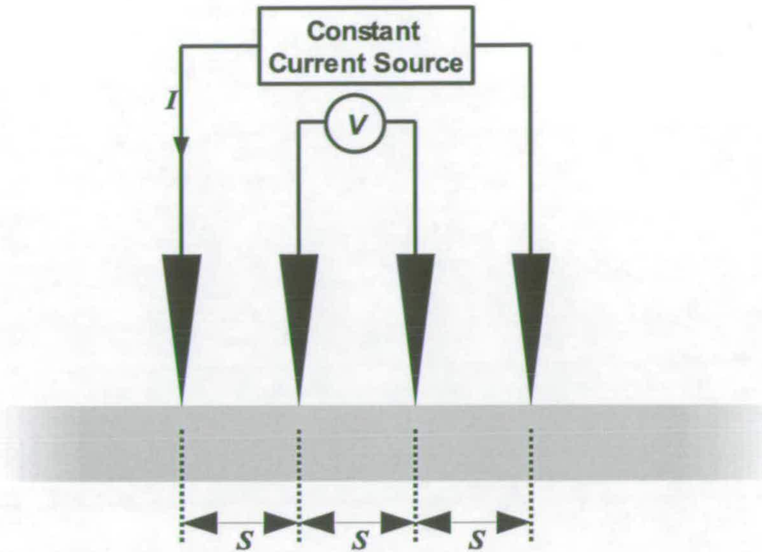


Figure 2.7: *Schematic illustration of the principles of four-point probe measurements.*

traditional product wafers where open/un-patterned areas of the wafer can reduce the profit of each wafer. One way of overcoming this has been presented by Guillaume et. al. [41], in which a method of extracting local sheet resistance using a "small-area four-point probe" technique is described. In this paper, the authors employ a four electrode setup which occupies a 160 μm × 160 μm square array applied to patterned films. Measurements were conducted using the van der Pauw approach, as will be discussed later in this section. The corresponding sheet resistance of the material is calculated by referencing measured resistance values with computer simulations of the configuration.

2.3.2 Test structures

Van der Pauw

One of the most widely adopted methods to measure the sheet resistance of patterned films is the use of van der Pauw structures [42, 43]. They are similar to the FPP measurements, but allow much smaller areas to be investigated and can take advantage of semiconductor patterning techniques. The theory and practice behind this method originated from work reported by van der Pauw in 1958 [44,45] to extract resistivity values and Hall coefficients from structures of arbitrary shape. In this study, four contacts (A,B,C,D) are placed along the periphery of a sample, as seen in the

configuration depicted in figure 2.8. Van der Pauw states that when a current is applied to contact A and taken off at contact B (I_{AB}), and the potential difference is measured between terminals D and C ($V_D - V_C$) then $R_{AB,CD}$ is defined as

$$R_{AB,CD} = \frac{V_D - V_C}{I_{AB}} \tag{2.4}$$

In a similar convention, $R_{BC,DA}$ can be calculated by applying a current between contacts B and C whilst measuring the potential difference between D and A. The van der Pauw measurement technique is based on the theory that between $R_{AB,CD}$ and $R_{BC,DA}$ there exists the simple relation shown in equation (2.5), where ρ is the resistivity of the material and t is the thickness.

$$exp\left(-\frac{\pi t}{\rho}R_{AB,CD}\right) + exp\left(-\frac{\pi t}{\rho}R_{BC,DA}\right) = 1 \tag{2.5}$$

Provided values for $R_{AB,CD}$, $R_{BC,DA}$, and t are known, then the numerical solution to equation (2.5) yields the value for ρ. The sheet resistance is similarly found by substituting the relation described in equation (2.3). This measurement approach is based upon the assumption that the material is of homogeneous thickness and resistivity, and that the contacts are finitely small and form only a single point of contact with the material.

In cases where the sample under investigation possesses 90° rotational symmetry and the contacts are equally spaced on the perimeter, it can be deduced that $R_{AB,CD} = R_{BC,DA} = R$. Placing this relationship back into the formula in equation (2.5) reveals the simplified version as

$$\rho = \frac{\pi t}{ln(2)}R \tag{2.6}$$

The one issue with using this approach is that the electrodes used will be of finite dimensions and do not satisfy the assumptions made earlier. To account for this, and to minimise any effects of the contacts on the measurements, van der Pauw introduced the cloverleaf configuration shown in figure 2.9. Further work by Buehler et. al. [42,43] found that, instead of contacting the corners of a structure, placing the electrodes at

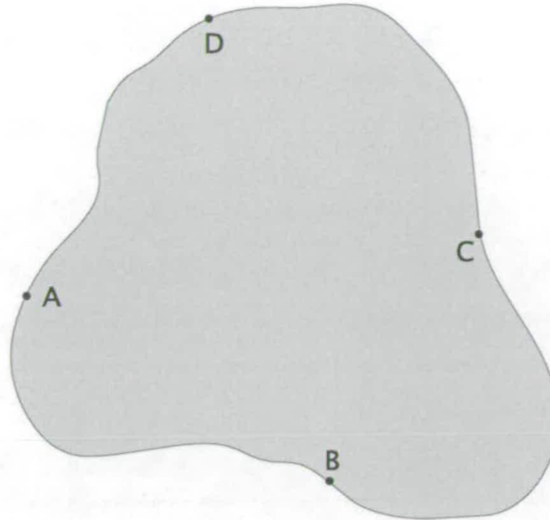


Figure 2.8: *Schematic illustration of van der Pauw measurement of a structure with arbitrary shape and placement of contacts.*

the midpoints of the sides of the structure led to lower sensitivity to the design related parameters of the test structures. These findings resulted in the development of the *Greek cross* test structure in IC test structure metrology. Using lithographic techniques, as employed in IC fabrication, it is possible to make these structures on the micro scale allowing numerous structures for a given area in comparison to the large area required for the FPP. A diagram of the Greek cross is presented in figure 2.10(a), and the Rs extraction routine follows that described for the above van der Pauw structures based on electrical contact at points A,B,C, and D. Other variations on the van der Pauw structure include the corner-tapped box cross and side-tapped box cross structures seen in figures 2.10(b) and 2.10(c).

Kelvin-tapped bridge resistor

One of the most frequently measured parameters in semiconductor analysis is the line width of fabricated structures. Monitoring this value provides information on lithography, etching and many of the other processes involved in wafer manufacture. A number of physical methods for extracting this parameter have already been described in the previous section. Electrical line width extraction is traditionally based on the tapped bridge resistor illustrated in figure 2.11. This structure uses the Kelvin technique to measure the potential drop between two taps placed along the bridge and is often referred to as the *Kelvin-tapped bridge resistor*. Measurements are conducted

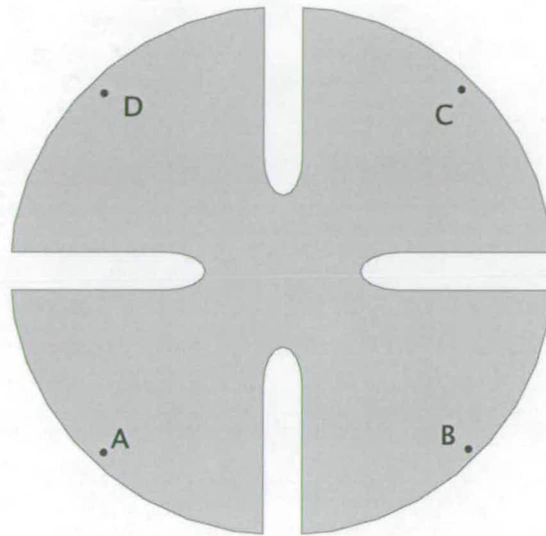


Figure 2.9: *Schematic illustration of a van der Pauw cloverleaf structure for reduction of contact errors.*

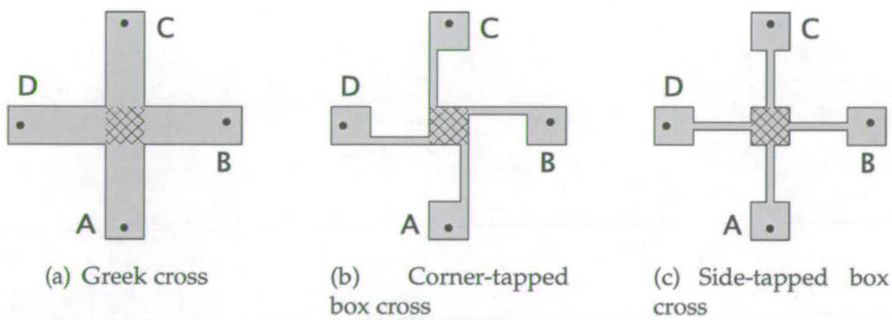


Figure 2.10: *Schematic illustration of commonly adopted patterned test structures used to measure sheet resistance of hatched area based on van der Pauw method.*

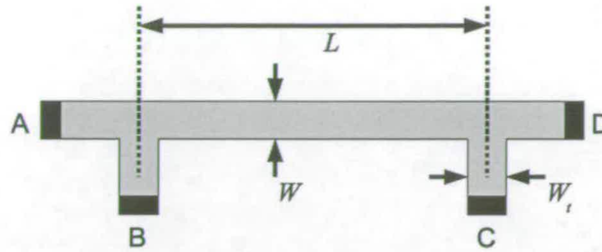


Figure 2.11: *Schematic illustration of a Kelvin-tapped bridge resistor structure.*

by applying a current along the bridge from contacts A to D (I_{AD}) while sensing the potential difference between contacts B and C (V_{BC}). Similarly, reversing the current and repeating the measurement allows averaging to determine R using

$$R = \frac{V_{BC} + V_{CB}}{I_{AD} + I_{DA}} \tag{2.7}$$

To calculate the line width (W) of a structure fabricated using the bridge resistor, the sheet resistance must first be known. For this reason, the Kelvin-tapped bridge is typically complemented by a van der Pauw cross resistor (such as a Greek cross) to provide a standalone structure capable of providing line width measurements as seen in figure 2.12 [43]. This combination is often referred to as the *cross-bridge* test structure. It is important to note that the accuracy of the sheet resistance is critical as any error in sheet resistance will be directly transferred into an error in the line width extracted from the Kelvin-tapped bridge resistor. With a value for Rs determined using the methods described in previous sections, the line width is found using equation (2.8), where L is the length of the bridge.

$$W = \frac{Rs \times L}{R} \tag{2.8}$$

One assumption made in the calculation of line width is that the bridge length is defined by the centre to centre distance between the two voltage taps (B and C in figure 2.11). However, as discovered in [46,47] the tap width (W_t) can lead to an over-estimation of the line width due to the effective bridge widening at their interface with the line. To prevent the need for data correction, the error introduce by the taps can be minimised by following strict design rules for the dimensions of these structures as explained in [48–50].

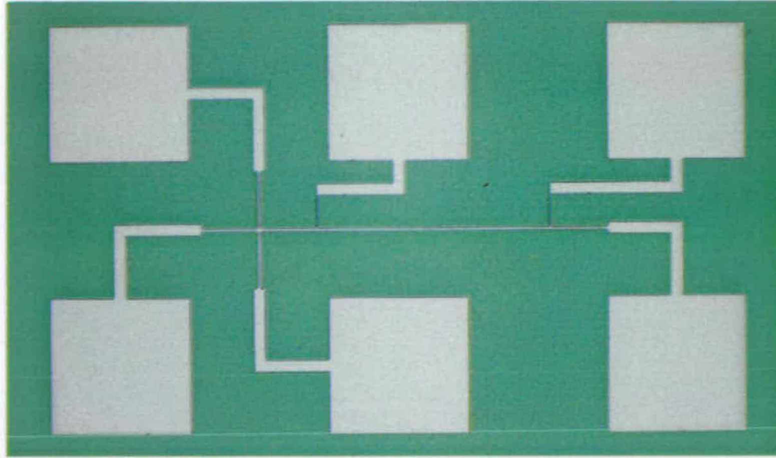


Figure 2.12: *A cross-bridge test structure for extracting sheet resistance and line width from a single structure.*

Applications

Both the van der Pauw and Kelvin-tapped bridge resistor structures have found many applications in test structure design and parameter extraction. First, by replicating cross-bridge structures over the surface of a wafer, a contour map can be generated based on extracted sheet resistance and line width values, to characterise tools and processes used during fabrication. Yen et. al. [51] describe an implementation of the cross-bridge test structure to characterise the uniformity of an IC lithography system. In this paper, the authors demonstrate high accuracy line width measurements using electrical test structures. By creating a contour map of the line width across the surface of a wafer, it was possible to make comparisons and evaluate the step-and-repeat lithography tool used.

Mian et. al. [52, 53] describe a test structure based on the van der Pauw principle to measure stress in packaged semiconductor die. Its operation is based on the relationship between the resistivity of the film and the stress applied to it. They report that this new structure and method allow three times higher sensitivity to stress than the traditional resistor based sensor alternatives.

Both van der Pauw cross resistor and bridge resistor have been used in the extraction of overlay in the manufacture of multi-layer devices. A detailed review of previously reported literature for overlay test structures is presented in Chapter 3.

2.4 Reference material

According to NIST, a reference material (RM) is a "material or substance one or more of whose property values are sufficiently homogeneous and well established to be used for the calibration of an apparatus, the assessment of a measurement method, or for assigning values to materials" [54]. They are essential for the continued development of metrology amongst the academic, commercial and government communities. More importantly RM provides traceability for CD measurements from features and materials during routine metrology. In the context of CD metrology, *traceability* is "the property of the result of a measurement or the value of a standard whereby it can be related to stated references, usually national or international standards, through an unbroken chain of comparisons, all having stated uncertainties" [55].

One major contributor to the development and manufacture of semiconductor critical dimension reference material (CD-RM) is NIST. Researchers at NIST have employed a common measurement technique in the establishment of line width CD-RM for the semiconductor industry. This is the use of HRTEM (as described previously) to calibrate measurements taken with electrical test structures. Allen et. al. [25] describe the requirement for CD-RM as structures which produce consistent results regardless of the metrology tool used for measurements. Furthermore, the authors describe a fabrication technique used to produce features on mono-crystalline bonded-and-etched-back silicon-on-insulator (BESOI) to yield rectangular cross sections. This allows structures to be fabricated with known sidewall angles, planar surfaces, and uniform material composition. These structures allow electrical measurements to be extracted and compared to HRTEM line width values to provide traceability. More recently an implementation of these structures has been reported [14] of RM on 200 mm Si wafers for automated metrology tool applications.

As one of the key properties of a RM is to define values of uncertainty, it is important to evaluate and reduce this where possible. As such, the authors of this paper report a 2.50 nm uncertainty in the HRTEM measurements, as derived from the fraction of the lattice planes which lie at the interface between the silicon and silicon oxide on the sides of the feature, as well as the accuracy of the lattice plane constant (the width of a silicon atom). The electrical CD (ECD) measurements, on the other hand, produce uncertainties of 5 nm for cases where the length of the Kelvin-tapped bridge (between

two adjacent taps) is not measured. This is reduced to a value of 0.9 nm when the bridge length is measured using a line scale interferometer tool [56].

Recently, Allen et. al. [57] have reported on the use of patterned grating structures to serve as OCD RM. In this approach, line width is determined based on an optical signature taken from spectroscopic ellipsometry experiments. The authors note that this technique has produced line width values which agree to within 10 nm with CD-SEM extracted values. While this uncertainty value is greater than the values seen with the HRTEM approach, OCD measurements benefit by being much faster and non-destructive in comparison. This area of work has contributed significantly to the development of methods other than HRTEM for CD-RM material evaluation.

2.5 Conclusions

A wide variety of measurement techniques have been described that are employed for semiconductor metrology. These were divided into both physical and electrical methods for measurements of critical dimensions.

Optical CD metrology tools are favoured in industry because of the fast, non-destructive and low cost nature of the measurements they provide. The key to extracting accurate measurements is the analysis and line width extraction algorithms used on the intensity profile taken from a structure. Standard SEM based metrology uses a similar approach for line width extraction. One of the problems encountered is that the images exhibit charging effects which cause higher intensity readings at the edges of lines. This has been accounted for in a number of previously reported papers by the use of a low voltage SEM to reduce the charging effects. Furthermore, other published work describes unique methods to analyse sidewall profiles in a SEM, allowing three dimensional information to be gathered about a structure.

The most accurate method for metrology to date has been demonstrated with the use of high resolution transmission electron microscopy (HRTEM). This method provides atomic resolution of the crystal planes in Si structures permitting the line width to be calculated based on the number of atoms across the width of a patterned feature. However, these measurements are very time consuming in both analysis as well as sample preparation.

Another non-destructive technique is the use of either stylus profilometry or scanning probe microscopy. In stylus profilometry, the measurements are limited by the physical dimensions of the stylus. While this is reduced when an AFM is used, the problem of tip geometry on the extracted profiles still exists. Novel techniques have been reported to allow the fabrication of more robust and narrower tips. However, it is only with boot-shaped tips for use in AFM metrology that information from the sidewalls of structures can be extracted. Further more, this technique has shown to be useful in extracting line width from structures based on a full three dimensional scan.

Electrical measurement techniques utilise well established methods for parameter extraction. The four-point probe method is routinely used in manufacture to measure the sheet resistance of materials and hence evaluate their resistivity and film thickness. These parameters can also be extracted using patterned test structures, such as the Greek cross, together with the van der Pauw measurement approach. The cross resistor structure provides a local measure of sheet resistance and can be patterned to dimensions comparable with IC devices being manufactured allowing easy integration. Line width, on the other hand, is traditionally measured using the Kelvin technique along with a tapped bridge resistor. Both the van der Pauw cross and the Kelvin-tapped bridge resistors can be combined to compliment each other and provide a cross-bridge test structure capable of extracting the line width of a standalone conductive feature.

Finally, the measurement techniques described above are only as accurate as the standards with which they are calibrated. By using RMs, critical parameters such as line width can be extracted to known values with stated uncertainty. To date, the use of HRTEM in CD measurement has proven to be the most accurate method of extracting line width. Work is ongoing to establish higher accuracy in RM characterisation as well as on fabrication techniques to ensure that the dimensions of the RM are more aggressive than the applications they are being used for. Furthermore, new methods for RM characterisation are currently being developed to reduce the time required for measurements as well as improve the accuracy of the extracted values.

The measurements and analysis presented in the remainder of this thesis are built upon these existing and well documented techniques and structures. Of specific relevance is the ability to measure structures electrically to relate the dimensional

parameters of line width and film thickness, and hence provide traceability for the measurements back to known standards. All fabrication and metrology tools used during the work conducted for this thesis are summarised in Appendix B.

Chapter 3
Test Structure for Optical-Electrical Overlay Calibration

3.1 Introduction

The relative alignment of the numerous layers within a modern Integrated Circuit (IC) is critical in order to ensure optimal performance of a device as well as improving yield. The metrology tools commonly employed during wafer manufacture to monitor the alignment of these layers require calibration to ensure that they provide accurate measurements. With IC dimensions constantly reducing and performance requirements increasing, the tolerances on misalignment between layers are becoming tighter. This, along with other demands such as tool matching and performance evaluation, places an increase on the importance of the accuracy and methodology used for calibration. This chapter examines this issue and presents a test structure which has been designed to serve as an application specific reference material for the accurate extraction of overlay. The target use of this structure is to calibrate measurements from optical tools against those taken from electrical testing.

3.2 Background

An important function of the manufacturing process is controlling the geometrical superposition of the various layers of patterned material in an IC, more specifically assuring that the lateral components of alignment are within design tolerances. In this and other stages of wafer fabrication, the term *overlay* quantifies the degree of superposition. It is a vector which is parallel to the wafer surface and is defined at every location on a composite pattern of two layers. The magnitudes of its two components are measures of the relative lateral locations of features of the second layer with respect to corresponding ones of the first layer. The ideal value of both

components of the overlay vector is zero. An important example of overlay is correct lateral superposition of vias in the L1-L2 (layer 1 to layer 2) inter-layer dielectric (ILD) relative to L1 and L2 patterned features. This is illustrated in figure 3.1, where a two layer interconnect system is used to demonstrate the lateral components (both X and Y) of overlay between layer 1 and via (Fig. 3.1(a)) as well as via and layer 2 levels (Fig. 3.1(b)). The resulting structure (Fig 3.1(c)) is subject to effects from both sets of overlay individually.

3.2.1 Optical overlay measurement

During wafer manufacture, the overlay at one or more locations on one or more die sites is sampled to confirm that it is within design specifications. The sampling is applied to the overlay between the patterned first layer and either the developed resist or the actual features of the second layer after completion of patterning. In both cases, overlay information is traditionally extracted by optical inspection with a highly specialized optical microscope, commonly known as an *overlay tool*. Such tools obtain local overlay values by capturing the image of a dedicated target structure, which is replicated on a die site specifically and exclusively to facilitate overlay metrology. A common target has the so-called *frame-in-frame* architecture, shown in figure 3.2(a), which exemplifies the overlay-vector components. The key property of the target is that the outer frame is patterned in one layer and the inner frame is patterned in the material of the other. Analysis of the image of the target, as collected by the overlay tool, is performed by well-established image-processing techniques and is rapid and economic. Overlay is determined by measuring the lateral spacing between the inner and outer frames of the structure, as depicted in figure 3.2(b).

The problem posed by this method is that the values of overlay obtained using optical means can be affected by two types of error [58]. The first type is tool-induced shift (TIS). This factor is the inherent error associated with the measurement tool employed, and is typically due to asymmetry of the metrology optics. Examples of these asymmetries include asymmetry in illumination of the sample and non-uniformity of the imaging optics. The effect of TIS can be quantified by conducting two sets of measurements, rotating the sample by 180° between each measurement. The difference between the measurement taken at 0° and 180° provides the degree

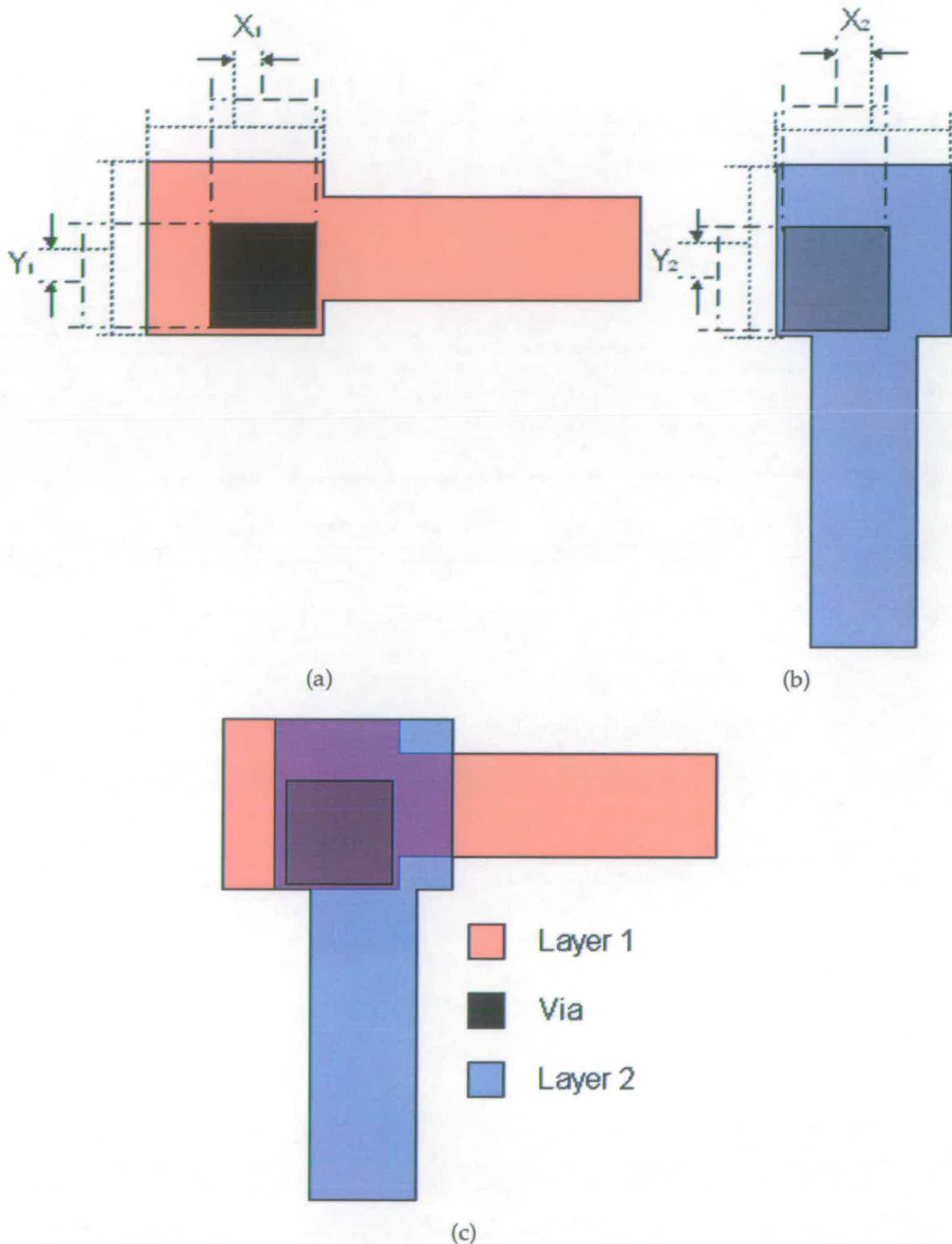
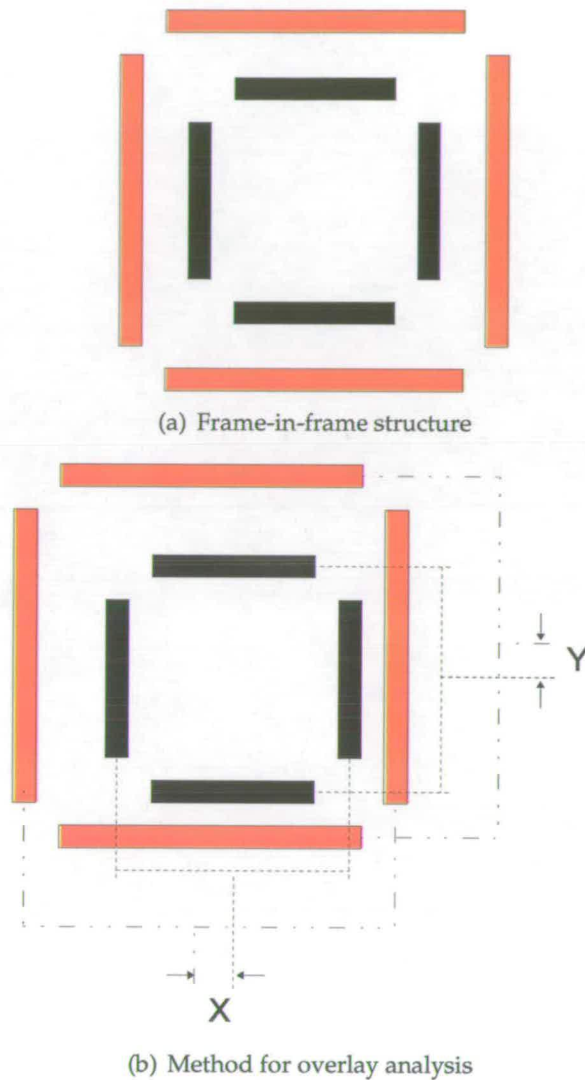


Figure 3.1: *Schematic illustration of the overlay components of a multilevel interconnect system.*

in which TIS is contributable to the extracted values. The second factor is wafer-induced shift (WIS) and is characterised by asymmetries due to process related effects. Examples of this factor include asymmetry due to metal deposition and/or chemical mechanical polishing (CMP) of wafers where the resulting structure may experience heavier deposition or polishing on one side of the structure. This type of asymmetry



(a) Frame-in-frame structure

(b) Method for overlay analysis

Figure 3.2: *Schematic illustration of the optical overlay structure.*

is typically seen as a shift in extracted overlay, from a single site, between the measurement taken from the developed resist and then taken again from the processed structure. As WIS is process dependant, it will vary to an unknown degree from one manufacturing process to another. The outcome is that the result of the frame-in-frame measurement typically includes elements due to either, or more likely both, TIS and WIS. Thus the reported optical overlay value generally differs by an unknown amount from a value based on optimum geometrical (and hence electrical) integrity of the conductor-via contact. The latter is referred to as the electrical overlay.

3.2.2 Electrical overlay measurement

Electrical measurements provide semiconductor manufacturers with a more functionally relevant measure of overlay in comparison to optical extraction. For the purposes of this study the previously reported test structures for extracting overlay using electrical measurements have been divided into two main categories. The first is test structures which measure overlay using analogue measurement techniques. A widely adopted structure to analyse overlay between two conducting layers as determined by the placement of an inter layer via has been published by Cresswell et. al. [59] called the sliding wire potentiometer. Referring to figure 3.3, current is forced along the bridge, from pads A to E , and voltage is sensed between pads B and D to extract the reference voltage for the bridge (V_r). Similarly measuring the voltage drop between pads B and C provides a value (V_m) which corresponds to the overlay of the patterned via relative to the underlying structure. Placing these measured values into equation (3.1) allows one to solve for the overlay (x) of the structure.

$$\frac{V_r}{V_m} = \frac{L/2 + x}{L} \tag{3.1}$$

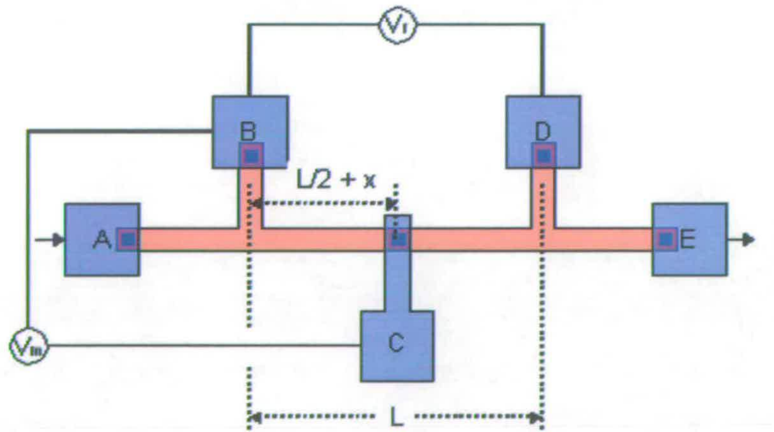


Figure 3.3: *Schematic illustration of the sliding wire potentiometer structure and measurement technique [59].*

With this structure replicated for both horizontal and vertical arrangements, measurements for both X and Y components of the local overlay can be taken. Buehler et. al. [60] and Creswell et. al. [61, 62] further present a design and method of analysis for a hybrid structure which enables both optical and electrical measurements

to be taken from a single structure to determine the overlay. This work was an exploratory investigation into the use of electrical measurements to calibrate optical overlay instruments and closely follows the technique mentioned above for the sliding wire potentiometer structure. Other work exists which presents similar structures that rely on a difference in resistance to determine the overlay of two layers with respect to the first patterned layer [63–66]. One of the issues in using this method for overlay metrology is the high dependence on the sheet resistance of the patterned materials. This is such that variations of resistance within the test structures may result in inaccurate measurements due to non-uniform voltage measurements when a constant current is forced.

The second category of electrical overlay structures is those that use a digital structure to measure overlay. The digital vernier structure, as reported by Henderson et. al. [67], is not limited in resolution of the measurement by the uniformity of the conducting layer, as is typically seen with analogue devices. Digital vernier structures, which have previously been published [68–70], rely on the establishment of electrical continuity between two sets of adjacent conducting teeth. The teeth of these structures are arranged at different pitches as determined by the resolution of the vernier as shown in figure 3.4. The measurements are taken by sensing continuity between the conducting vias (or contacts) and the teeth of the structure. The resulting measurements are therefore able to determine the overlay to an accuracy of the resolution of the teeth. One drawback with this approach is that, as the resolution of the structure is directly proportional to the number of teeth employed, a large number of probe pads are required to make electrical contact resulting in a proportionally large footprint. However this issue has been addressed with the use of integrated circuitry to reduce the number of probe pads required and maintain a smaller footprint. Morrow et. al. [70] report on the implementation of the digital vernier structure where diodes are used to increase the number of configurations possible for a given number of probe pads.

Though these methods for electrical extraction of overlay provide functionally relevant values, there are some drawbacks in comparison to optical methods. The first is that in order for electrical measurements to be conducted the processing must be carried out to the point at which electrical contact can be made. As a result the

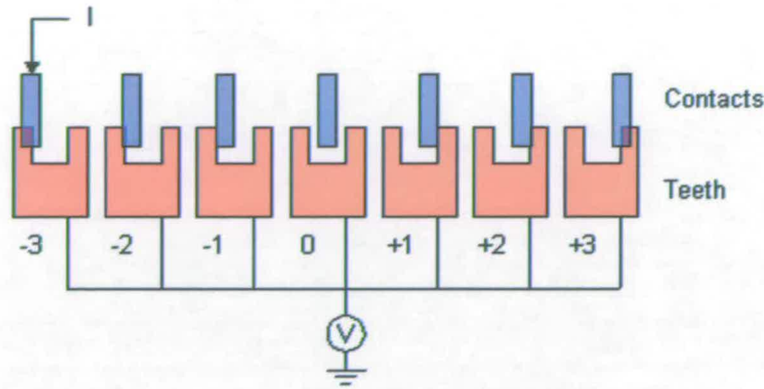


Figure 3.4: *Schematic illustration of the digital vernier structure with measurement principle [68].*

wafer has been fabricated to the extent where re-work is no longer possible and hence the wafer is of no value if the overlay is outwith design tolerances. On the other hand, optical measurements are typically applied after imaging the photoresist of the upper conductive layer. If measurements of the frame-in-frame show the overlay to be out of specification, the photoresist can be removed and the wafer re-patterned. Another issue with electrical measurements is the fact that physical contact is typically required to the probe pads and this, in semiconductor manufacturing, can be a source of particulate contamination.

3.3 Design

Working in collaboration with NIST, a test chip (*NIST 47*) was designed to evaluate the technique described in [71, 72]. The electrical component of the test structure evolved from the work reviewed in Section 3.2.2 on digital vernier overlay test structures. The technique involves conducting measurements to determine the unknown difference between optical and electrical extraction of overlay and hence provide necessary calibration values. Furthermore, the measurement strategy for this structure does not require precision equipment, enabling it to be easily adopted amongst the semiconductor community. As the key role of this test structure is to evaluate the relationship between both optical and electrical measurement approaches, the design incorporates separate features for both types.

The three levels employed in this application are lower conductor (L1), via, and upper

conductor (L2). (Note that this new test structure is not designed to replace the optical overlay test structure in routine applications.) In the case designed here, the overlay is measured between the lower conductor and the via layer with both the electrical and optical structures, however this technique can be modified to suit many applications. A traditional metal 1 (M1) to dielectric via to metal 2 (M2) interconnect process was chosen for implementation.

The composite test structure is comprised of a regular array of 287 similar cells, each of which can be interrogated individually to provide a thorough picture of the overlay for the test chip. Each test cell, one of which is shown in figure 3.5, has separate elements to determine both the X and Y components of the local overlay of the dielectric-via level to the first metal level by electrical means as discussed below. Each of the two elements has a reference feature which is replicated in the first metal level. It is arranged vertically for the X-axis element (this is the vertical feature in the detail box in figure 3.5(b)) and horizontally for the Y-axis. At the completion of the fabrication, this reference feature is nominally connected to a layer 2 test pad through a group of vias as shown schematically in figure 3.5. Seven vias through the L1-L2 inter-layer dielectric layer are regularly distributed along a line inclined to, and intersecting, the reference line. It is key at this point to remind the reader that the overlay is determined in this implementation of the test structure only between the first metal and the via layer. The second metal serves only to distribute the desired electrical signals to the probe pads.

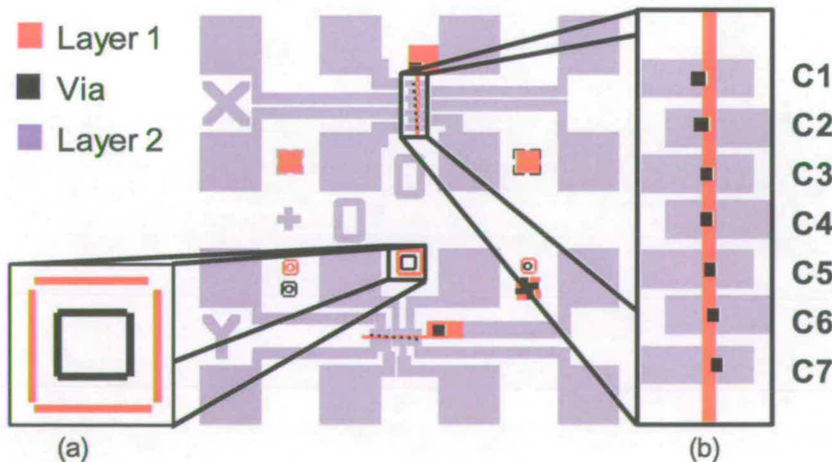


Figure 3.5: *Layout of single test cell of the NIST 47 design with (a) frame-in-frame structure and (b) diagonal arrangement of contacts.*

The via *pitch* is the component of the drawn lateral separation of adjacent vias in

a direction perpendicular to the reference line, as shown in figure 3.6(a). In the design used here, the pitch between adjacent vias is either 0.5 μm or 1.0 μm, with the pitch between the end vias totaling 5.0 μm. In each element of the test cell, the as-fabricated *mis-registration* of a particular via is its centre-to-centre perpendicular distance from the reference line as shown in figure 3.6(b). It is equal to its as-drawn lateral displacement from the reference line plus the as-fabricated misalignment of the cell. The *misalignment* of the cell is the cell's programmed offset plus the overlay with which the test structure is fabricated. The *programmed offset* is the value by which each cell's via layer is wholly shifted in both X and Y directions relative to the zero offset cell. All cells of the test structure are fabricated with the same overlay but are replicated with their own unique programmed offsets.

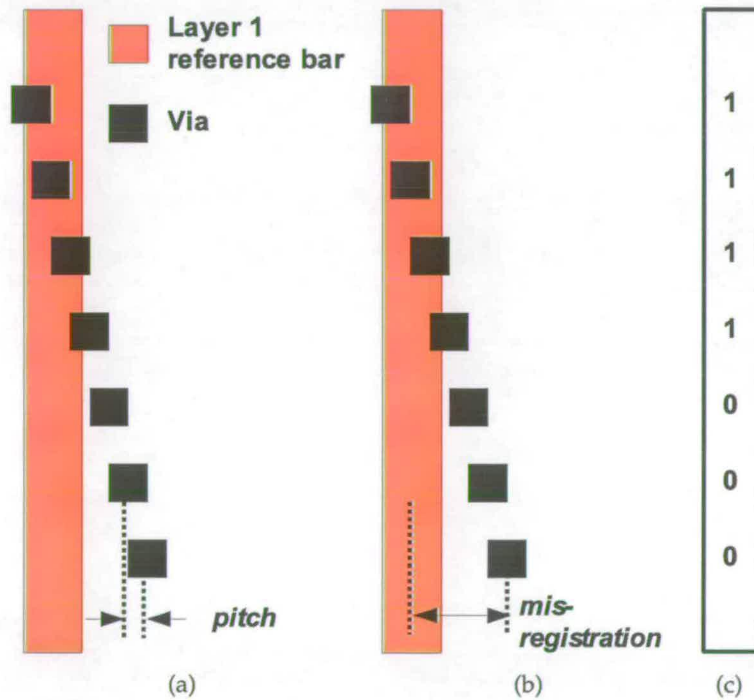


Figure 3.6: *Schematic illustration of reference bar with design related parameters and corresponding binary signature.*

Electrical contact to the filled vias, some of which may be in contact or in partial contact with the L1 reference line, is provided by their connection to test pads on the L2 level as illustrated in figure 3.5. This arrangement enables electrical continuity to be sensed between the reference line patterned on the lower metal level and the contacts connected to the test pads on the upper metal level. The results are recorded in binary format where a "1" represents electrical continuity and a "0" represents an electrical

open. In principle, the misalignment of a cell can be determined to within a resolution of the via pitch from the binary continuity signature (Fig. 3.6(c)) of the cell in a manner similar to that reported for the vernier type structures discussed previously.

Within each test cell there is also a standard frame-in-frame optical overlay target as shown in figure 3.5(a), which provides features to measure both X and Y components of the overlay. The placement of these features matches the as-fabricated misalignment of the cell, which is made up of the programmed offset of the cell plus the overlay with which the test structure is fabricated. The cell misalignment is designed to be measured optically using the same tool that is to be calibrated.

Figure 3.7: *Layout of NIST 47 design; the test structure described is the 16 by 18 array of cells indicated.*

In the test structure, which is a regular array of 16 by 18 cells, each cell has its own programmed offset in multiples of 10 nm. The complete test structure, shown in figure 3.7, enables the cross comparison of optical and electrical overlay between ±1.43 μm in both the X and Y directions in steps of 10 nm for the purpose of application-specific calibration-curve construction. Each cell is systematically placed in an ordered row and column format for simplifying analysis. However, the

arrangement is such that the cells are effectively randomized across the complete test structure in both the X and Y directions. This ensures that any systematic change in overlay, for example increasing from left to right across the complete structure, does not appear as an offset during analysis. Each column contains 16 cells, where the individual cells have sequential programmed offsets of 10 nm ordered such that the programmed offsets decrease from the top to the centre of the column in odd-number multiples of 10 nm. The programmed offsets similarly decrease in even-number multiples of 10 nm from the bottom to the centre of the column. The columns, of which there are 18, are arranged such that the leftmost column contains the set of cells offset in the extreme negative direction, while the rightmost column contain those in the extreme positive direction. Progressing horizontally towards the centre of the die sees the offset values for each column alternate in direction (positive and negative axis) whilst decreasing in value.

3.4 Fabrication

In order to validate the design, a traditional two layer metal process fabricated on bulk silicon wafers was implemented. The fabrication uses standard processes and equipment as typically seen in industry. The actual process employed is described in the run sheet presented in Appendix C.1.

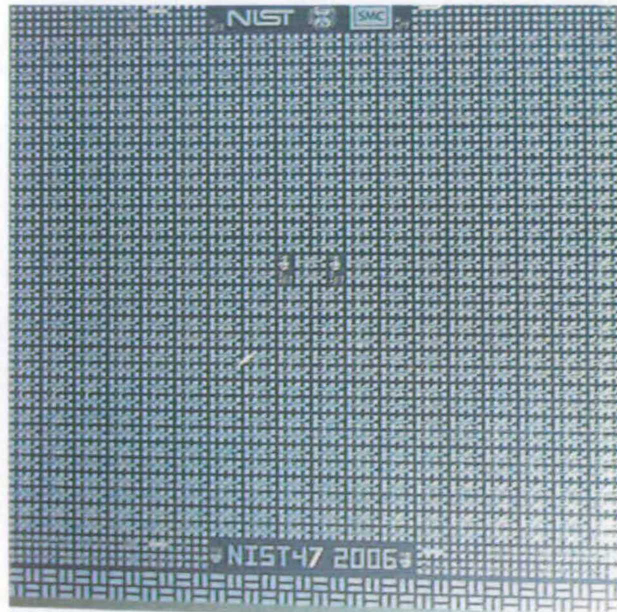
The substrates used were 3 inch bulk (100) Si wafers. The wafers first underwent a thermal oxidation to provide electrical isolation from the substrate, resulting in 0.5 μm of silicon dioxide (SiO_2). Then a thin layer of Al was deposited using physical vapour deposition (PVD), also referred to as sputtering. The thickness of this layer greatly depends on the process under evaluation, for this study a 0.2 μm layer was employed. This first layer of metal was then patterned with the M1 reference line of the electrical structure along with the external frame of the optical structure. Standard photolithography [73] techniques were used to define the pattern in photoresist. During this process, the stepper used for the lithography was also commanded to place global alignment marks on a horizontal plane, across the diameter, near the wafer's edge. These alignment marks provide a structure by which the subsequent layers can be aligned. More precise and accurate alignment is provided for within each imaged die using lithography tool specific alignment marks. The Al layer was etched with a

reactive ion etching tool (RIE) using a chlorine based etch chemistry. The photoresist is then removed in an oxygen plasma asher.

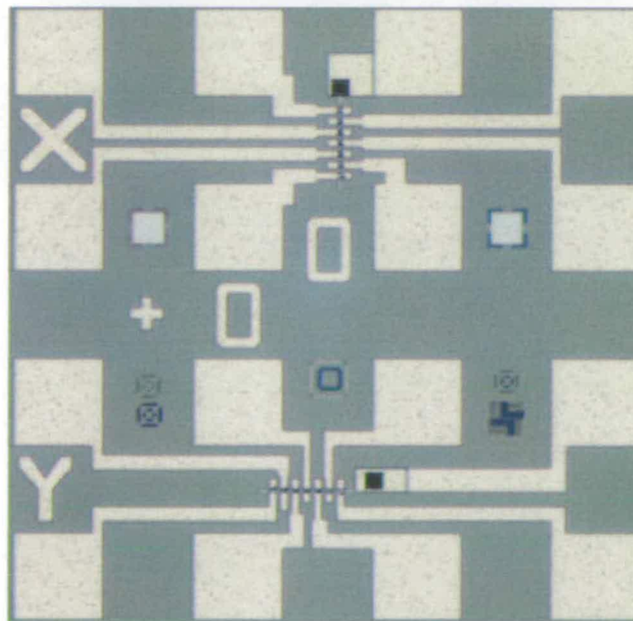
In the next stage a dielectric layer of SiO_2 is deposited over the surface of the wafer using high frequency plasma enhanced chemical vapour deposition (PECVD). Once again the thickness of this layer depends on the process under evaluation. Furthermore, the thicker this layer becomes the larger the aspect ratio of the vias becomes as the dimensions of each via are fixed at mask level. For this reason a thickness of 0.5 μm was used, providing an aspect ratio of 1:4, based on a via size of 2 μm by 2 μm. The contacts, as well as the inner frame of the optical structure, were then patterned using the same photolithography process as described above for the M1 reference bar. The pattern was etched into the dielectric layer, using an RIE tool and a fluorine based chemistry, until the M1 layer was exposed under those vias which are aligned over the reference bar. Due to the smaller dimensions of the vias (2 μm by 2 μm) in comparison to the frame-in-frame structure, which was 2 μm by 16 μm, the optical overlay structure became over etched. This is because smaller features require longer etch times than larger features, due to pattern dependencies and loading during etching [74].

Finally a film of Al was deposited and patterned with the same photolithography and RIE process as that used for the M1 layer, providing the probe pads and interconnect necessary for electrical measurements. In order to provide sufficient material for the electrical test probes to make contact with the probe pads, without puncturing through the layer, the Al was PVD sputtered to a thickness of 1 μm for M2. An image showing the "as-fabricated" test chip is presented in figure 3.8(a) along with a magnified image of the centre test cell (Fig. 3.8(b)).

An important factor to note is that although this design has been demonstrated with Al, it can be implemented with other interconnect materials such as Cu. Varying the implementation may, in some instances, require modification of the masks used for lithography patterning due to the manner in which the interconnect materials are defined, for example, a reverse field mask would be used for damascene patterning.



(a)



(b)

Figure 3.8: *Fabricated test chip with corresponding magnified image centre of test cell.*

3.5 Results

Complete arrays of 287 cells were measured electrically to determine the continuity between the reference line and the seven contacts shown in figure 3.5. The electrical measurement setup consists of a high sensitivity volt/ohm-meter configured to

	Contact						
	C1	C2	C3	C4	C5	C6	C7
Programed offset (μm)	-2.5	-1.5	-0.5	0	0.5	1.5	2.5
Resistance ($k\Omega$)	0.01	0.0092	0.0087	0.013	0.0095	0.011	17050
Binary equivalent	1	1	1	1	1	1	0
Weight multiple (μm)	0.5	1.0	0.5	0	0.5	1.0	0.5

Table 3.1: *Selected data from electrical overlay structure.*

operate in resistance mode, along with a probe station and probe card fixtures to make physical contact with the probe pads. The resistance meter was programmed to take the average of five measurements in order to reduce measurement error. Using the setup described above, the resistance between the reference bar and the seven contacts was measured individually to determine continuity. This data was exported directly from the measurement system to be analysed offline. The analysis was conducted using a standard package of software for simple data analysis[1]. The resistance measurements were imported into a spreadsheet and arranged by structure and contact number. Table 3.1 displays some sample data as extracted from a single cell of the test structure. From this point the binary equivalents of each contact are then derived. A threshold resistance of 1 kΩ was decided upon due to the fact that vias in contact with the reference bar measured 10 Ω on average on the resistance meter whilst vias which are not in contact measured 17050 kΩ (the limit of the tools measurement range). Contacts with resistance values higher than this threshold are classed as a binary "0" (open) and those less than the threshold a binary "1" (short). The results presented in Table 3.1 indicate that the via with a pitch of 2.5 µm (C7) does not make contact and is misaligned positively with respect to the M1 reference line. To represent the misalignment of each cell, the binary signature is weighted and summed together using equation (3.2), where C1 to C7 are the individual bits of the binary signature.

$$Misalign_{(cell)} = ((C5 \times 0.5) + (C6) + (C7 \times 0.5)) - ((C1 \times 0.5) + (C2) + (C3 \times 0.5)) \quad (3.2)$$

[1]Microsoft Excel (Office 2003)

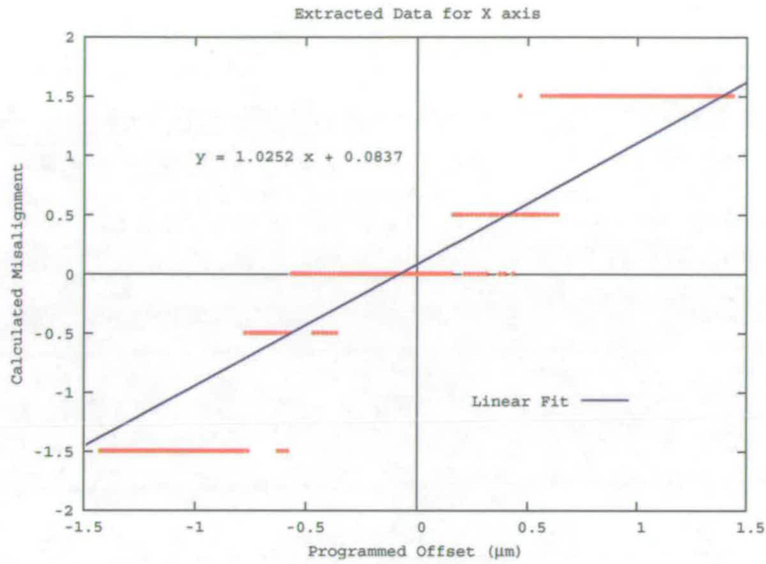
The weight multiples are determined such that the resulting calculated misalignment value provides a rough measure of the overlay for each cell against its programmed offset. The whole test structure combines these values to provide a much better measure of overlay, with a resolution of 10 nm. The actual weight multiples employed for each via are provided in Table 3.1. With the weighted sums for each contact calculated, the leftmost three contacts (C1, C2, C3) are subtracted from the rightmost three contacts (C5, C6, C7), ignoring the centre contact as it has a zero relative centre-to-centre distance from the reference line (assuming zero programmed offset). The resulting value corresponds to the mis-registration of the contacts with respect to the centre of the reference line.

A plot of the derived values for the complete array of 287 structures, for both X and Y axis, on a single chip is presented in figure 3.9. The values are plotted as the calculated misalignment (from equation 3.2) against the programmed offset for each test cell. The electrical overlay value is then extracted from this data by first calculating the median overlay value for each data set. For example, referring to figure 3.9(a), the set of data which lies on the calculated misalignment value of 0.5 ranges in programmed offset from 0.17 μm to 0.63 μm making the centre lie at 0.4 μm. This process is repeated for the remaining sets of data, in this case the 0 and -0.5 calculated misalignment sets. (Note: As the two data sets which extend to the limits of the programmed offset, both positive and negative, may contain data beyond those points, these sets cannot be used in the calculation. In this case the ± 1.5 data sets.) Linear regression is then used to determine the best fit of a line connecting the median points for the sets of data ranging from -1.43 μm to 1.43 μm programed offset as described by equation (3.3).

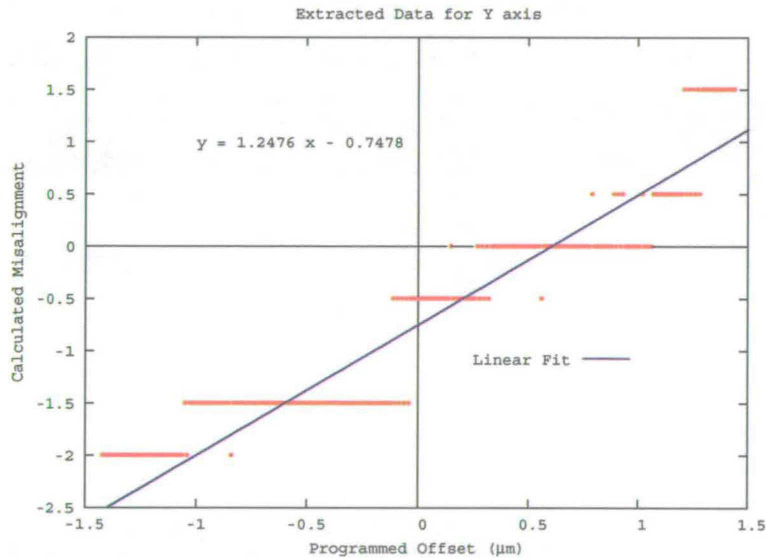
$$Misalign_{(structure)} = A \times Offset_{(programmed)} + B \tag{3.3}$$

Solving equation (3.3) to determine the $Misalign_{(structure)} = 0$ intercept for this line provides a value for the overlay in the X direction of the structure under test. The same process is then repeated for the data representing the Y axis.

Using this particular set of data a value of -81.6 nm was calculated for the overlay in the X direction. To provide measurement assurance, SEM images (Fig. 3.10(a)) were taken of the frame-in-frame structure and measured to determine the overlay from the



(a) Offset in X Axis



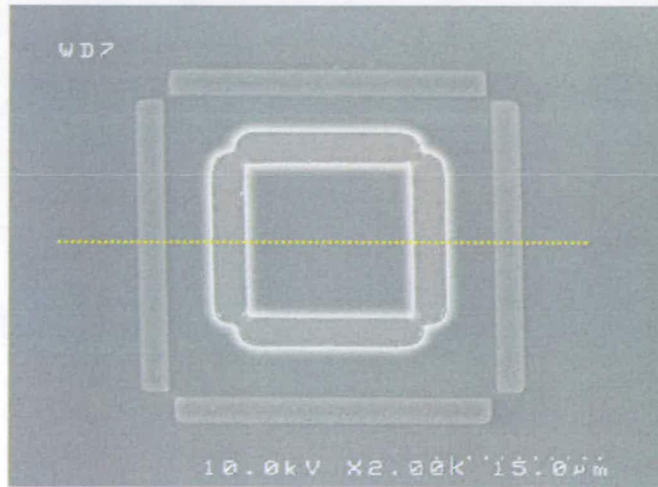
(b) Offset in Y Axis

Figure 3.9: *Relationship between calculated misalignment measurements vs programmed structure offset for single die.*

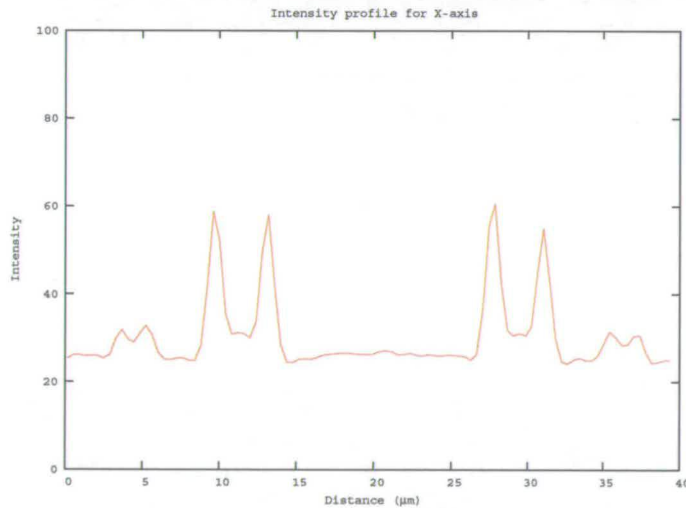
optical structures. These measurements are conducted by extracting a single line scan profile from the image of the frame-in-frame structures along a perpendicular axis to the lines patterned in layer 1 for each direction. This profile was extracted using readily available image processing software[2]. An example of one of these profiles as used for the X direction is displayed in figure 3.10(b). With this intensity profile, the alignment

[2]Gwyddion - SPM data analysis software (gwyddion.net)

can be determined by calculating the differences between the inner and outer frames, represented by the outer pair (for the outer frame) and inner pair (for the inner frame) of profiles in the intensity plot. The result of this measurement yielded a value of -80.6 nm, thereby demonstrating the functionality of the electrical measurements taken from this test structure.



(a) SEM image



(b) Extracted intensity profile

Figure 3.10: *SEM extraction of overlay achieved from frame-in-frame structure using intensity profile.*

Repeating this method of analysis for the data for the Y direction produces an electrically extracted overlay value of 629.8 nm, while the SEM intensity profile extracts the overlay as 638.4 nm. It can be observed that the values for the Y alignment

differ by 9 nm in contrast to the 1 nm difference in the X direction. One possible explanation for this could be uncertainty in the measurements which result from non-uniformities in the processing. For example, if there is any line roughness produced as a result of the RIE etching of the metal lines then noise will be introduced as seen by inconsistencies in contact between the reference bar and adjacently offset vias. Alternatively, the error might be attributable to the TIS-WIS interaction of the SEM measurements and process used. One observation from comparing figure 3.9(a) and figure 3.9(b) is that the slopes of the lines relating the median points differ slightly. The precise cause for this is currently unknown and requires further investigation.

3.6 Conclusions

This chapter presented the issues involved in both optical and electrical measurement of the misalignment of multiple layers in semiconductor IC devices. The benefit of using optical measurements is their low cost and high efficiency per measurement. However these measurements are subject to either, or more likely both, TIS and WIS. Electrical measurements, on the other hand, provide a functionally relevant measure of the overlay of layers, though they require electrical contact and therefore the wafer under test can not be reused if it falls outside of the design tolerances. To allow accurate measurements from optical tools in interconnect overlay metrology, the TIS and WIS interactions must be measured and accounted for through calibration of the equipment used. Therefore it can be deuced that the key factor in monitoring overlay for process control and characterisation is ensuring the accuracy of the reference material used for calibration.

The technique presented in this chapter serves to allow overlay tool calibration by providing a means to determine the difference between optical and electrical measurements of overlay. A novel hybrid design (NIST 47) was created to allow electrical structures to be measured and used to calibrate commercially available optical overlay tools. This is achieved by embedding optical frame-in-frame structures alongside electrically testable overlay structures. A digital electrical test structure is employed to overcome the limitations posed by typical analogue structures for overlay extraction. The test structure incorporates a large array of cells to facilitate analysis from the vast amount of measurement data.

A standard process has been used to fabricate the design and then demonstrate its application to evaluate the misalignment on an interconnect process. As was highlighted in section 3.4 the process used for the implementation can be varied to match the one under evaluation. The success of the fabrication is reflected by the ability to extract and compare both electrical and SEM extracted overlay values.

As the measurement strategy specifies, the necessary electrical measurements are simply used to determine continuity. Therefore, readily available measurement tools can be used to electrically determine the overlay as was demonstrated with the use of a resistance meter. Furthermore, traditional wafer probing equipment was used to provide the electrical contact to the probe pads of each test cell. The analysis method described in this chapter calculates a misalignment value for each test cell in the array of features. Using simple linear-regression techniques, the relationship between the measured data and the programmed offsets of the cells could be determined. The overlay value, as extracted from the electrical measurements, is then found by solving equation (3.3) for the situation where $Misalign_{(structure)} = 0$.

In conclusion, the design and fabrication of a hybrid array based optical-electrical overlay test structure has been successfully demonstrated. This is supported in the results with values agreeing to within 1 nm in the X direction and 9 nm in the Y taken from both electrical and SEM measurements. Subject to further work to evaluate the use of optical tools and the relation of the measurements to the electrical test structures, the design presented can be considered a feasible candidate for use in overlay calibration.

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Chapter 4
Fabrication of All-Copper ECD Structures

4.1 Introduction

This chapter addresses a current gap in semiconductor interconnect test structures for CD extraction. While Si ECD structures are well establish for reference material (RM) applications and provide highly accurate measurements based on the use of HRTEM, a similar structure for metal interconnects does not exist. More specifically a structure is required that will provide the academic, commercial and governmental communities with the ability to conduct thorough experiments on new interconnect technologies such as copper (Cu). This requirement is further extended to the need for a standard reference material (RM) fabricated in Cu. Another key area of interest is the ability to study the electron transport mechanism in Cu lines unaffected by the barrier metals used in industry. These have been addressed with the design and fabrication of a novel all-copper test structure presented in this chapter. This structure is based on the combination of fabrication techniques from Si ECD structures and the Cu damascene process. To understand the fabrication process employed, a brief background to Cu interconnect fabrication, as seen in the semiconductor industry, is first presented. The second half of this chapter will look in detail at the process steps used and their integration to achieve the desired structure.

4.2 Background

With the push by the semiconductor industry to meet ever more strict R-C timing requirements, new materials have been adopted in interconnect wiring schemes. The major recent change has been the replacement of Al-based materials by Cu as the interconnect metal of choice. The main reasons for choosing Cu are its lower resistivity and better immunity to the damaging effects caused by electromigration

compared to Al [75]. However, because of the manner in which Cu interconnects are fabricated and integrated using barrier layers in modern IC devices, standard electrical metrology methods do not provide sufficient accuracy to be used as standard reference measurements.

There have been a number of publications addressing methods of extracting the ECD values from Cu interconnect features [76–78]. However, these all concentrate on how to minimise the effect of the conducting barrier layers and as a result are not suitable approaches for a reference standard as the presence of the conductive barrier layers produce interconnects which are non-homogenous. Other papers [24–27,61,62,79–89] have been published that describe electrical line width test structures fabricated in mono-crystalline Si for use as reference material. These papers describe means by which CD standards can be derived from electrical test structures. However, electrical measurements on their own "have not yet shown to be able to provide traceability with acceptable levels of uncertainty" [76]. Hence, to be a traceable standard the electrical measurements of line width must be calibrated to proven high accuracy methods such as HRTEM measurements [24–27].

4.2.1 Copper damascene process

In order to place the process employed in Cu interconnect schemes into perspective, it is first necessary to discuss previous multilayer interconnect technologies such as that used for Al tracks. This metal was traditionally implemented using a subtractive processing technique with a silicon dioxide (SiO_2) inter-layer dielectric (ILD), as outlined in figure 4.1. This interconnect process derives its name from the fact that the Al material that is not covered by the photoresist pattern is subtracted (etched) from the blanket film to leave the patterned tracks. The subtractive approach begins with the blanket deposition of the Al metal using an appropriate method, of which a number of options exist such as physical vapour deposition (PVD), chemical vapour deposition (CVD), evaporation, etc (Fig. 4.1(a)). Next the interconnect pattern is defined in a photoresist layer on top of the metal using standard photolithography techniques [73] with a light field mask (Fig. 4.1(b)). The pattern is then transferred into the metal using either wet or dry etching process [90,91] (Fig.4.1(c)). Dry etching, using a reactive ion etch tool (RIE), is the preferred method because of its ability to produce

anisotropic profiles [92]. After the pattern is etched, the photo resist is removed (Fig. 4.1(d)). To isolate the current layer from the subsequent layers in the wiring scheme a layer of SiO_2 is deposited over the metal line (Fig. 4.1(e)). In traditional IC implementations, multiple layers of interconnect are used to meet the requirement for high density yet small IC devices. The result of this is that the topography and height variations on the top surface of the wafer increase with each additional patterned layer. This introduces problems such as variations in photoresist thickness and lithography variations due to depth of focus issues. It therefore becomes necessary to reduce the topography accumulated through the fabrication of the device and accommodate subsequent processing steps. A planar surface is achieved using chemical mechanical polishing (CMP) of the SiO_2 layer (Fig. 4.1(f)). Further processing is conducted as required by repeating the above sequence. Cu, on the other hand, is unable to be etched using an RIE tool due to the fact that there does not exist a chemistry which reacts or produces appropriate by-products with the Cu metal to pattern it. For this reason, the damascene method for patterning is typically used.

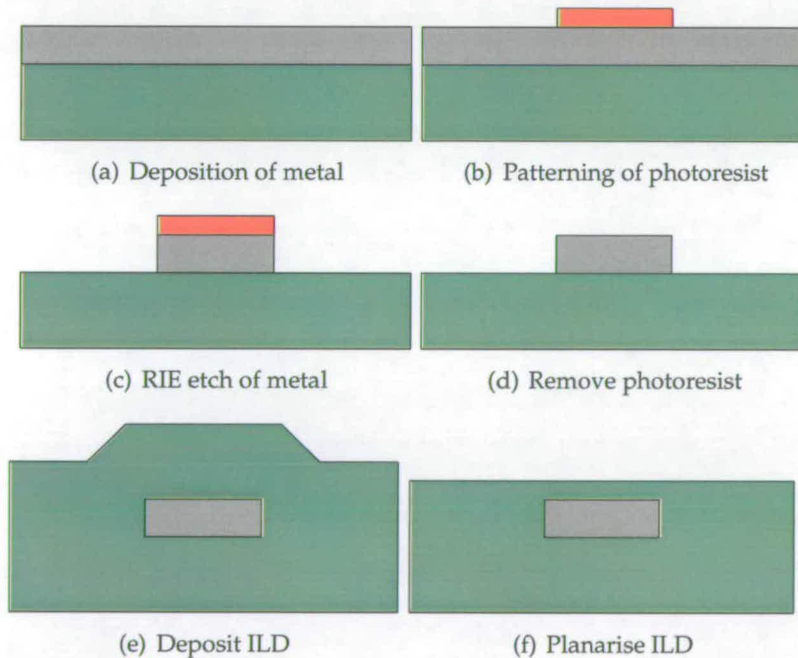


Figure 4.1: *Schematic illustration of the main steps in subtractive processing of interconnects.*

While the traditional approach to Al interconnect fabrication uses dry etching to pattern the metal directly, the damascene method takes a different approach. In principle, the ILD is used to define the interconnect pattern and the metal is deposited

to fill this trench as outlined in figure 4.2. The fabrication first begins by depositing the ILD onto the substrate (Fig. 4.2(a)). Following this, photoresist is used to define the interconnect pattern on the ILD using similar photolithography process as used with subtractive processing but with a dark-field mask (Fig. 4.2(b)). An RIE tool is then used to etch a trench into the ILD using an anisotropic etch process (Fig. 4.2(c)). After the photoresist has been stripped (Fig. 4.2(d)), Cu deposition is conducted over the entire surface of the wafer using one of a number of available techniques including: PVD, CVD, evaporation, and electroplating (Fig. 4.2(e)). A subsequent planarisation step reveals the patterned Cu interconnect feature as defined by the ILD trench (Fig. 4.2(f)). Further processing can similarly be conducted, as required, by repeating the above steps.

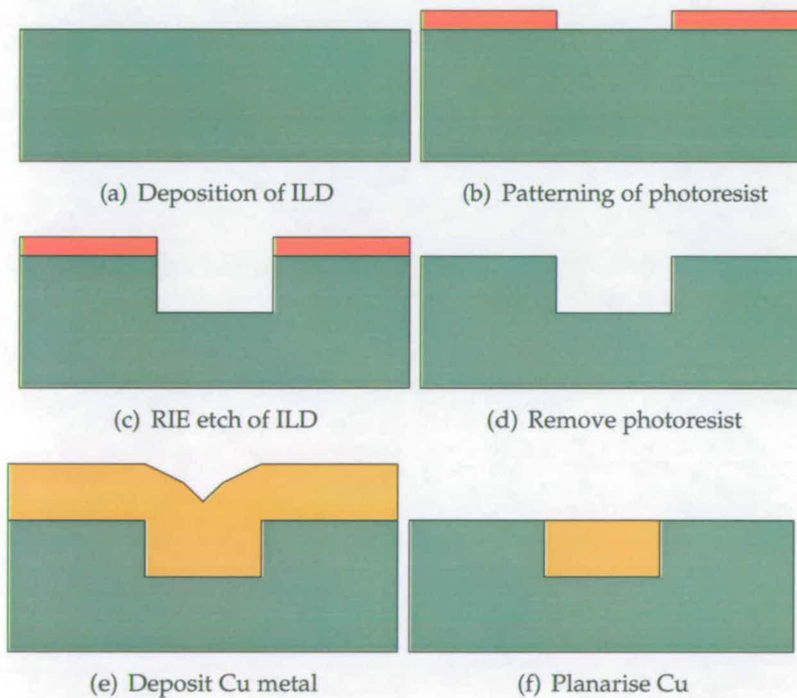


Figure 4.2: *Schematic illustration of the major steps in damascene processing of interconnects.*

In traditional semiconductor IC manufacturing, the last step in a process is the deposition of a dielectric material to passivate the chip. This applies to both the subtractive as well as the damascene processes.

4.2.2 Barrier layers

When implementing Cu as a semiconductor interconnect material, compatibility issues must be addressed over and above that for previous technologies. These can be grouped into three main categories: oxidation of the Cu, diffusion of the Cu into the substrate, and adhesion of the Cu to the substrate [93]. Each one of these plays an important role in the fabrication and performance of the interconnect system.

First Cu readily oxidises in atmosphere and the oxidation is not self-limiting and, unless it is protected, the interconnect line will be wholly consumed as it turns into Cu oxide (Cu_xO). This issue is typically addressed by encapsulating the interconnect track in a material which is impervious to oxidising atmospheres. Additionally, Cu ions can easily diffuse through most of the commonly employed ILD layers, including SiO_2 [94]. If these ions reach the semiconducting devices beneath the interconnect wires they can detrimentally effect the performance of the circuit and introduce reliability issues. The diffusion of Cu can be prevented either by choosing a more appropriate ILD material, or by placing another material (either conductive or dielectric) capable of preventing the diffusion between the track and the ILD. The final issue with Cu interconnects is more relevant during the fabrication, as Cu on its own does not provide sufficient adhesion to SiO_2 to survive the CMP stage, as well as other stages, of the manufacturing process. The solution to this problem is similar to that for the diffusion of the Cu, in that either an additional material is used between the interconnect and the ILD or an ILD which adheres better to Cu is chosen. These three issues tend to collectively be addressed with the use of various types of barrier layers in modern manufacturing processes. The barrier layers are typically placed at the interface between the Cu line and the ILD.

There are two main types of barrier layers for use with Cu interconnects, namely conductive barrier materials and dielectric barrier materials. In practice, a conductive barrier metal is typically used to line the trench prior to Cu deposition. This prevents the oxidation as well as the diffusion of the Cu through the dielectric. Furthermore, the adhesion between the ILD and the Cu is improved with the presence of a barrier metal. The initial choice of materials for the barrier layer was the use of titanium (Ti) and titanium nitride (TiN) combinations [95–97], as a result of the large amount of knowledge and experience gained with Al interconnect fabrication. It was found that a

TiN layer placed between an Al track and the ILD improved the adhesion of the track to the substrate. However, this material alone did not provide sufficient protection against the diffusion of Al ions through the ILD [98] and therefore an additional layer of Ti was used between the TiN and the ILD. As well as improving the diffusion properties of the composite barrier layer, the additional layer increased the adhesion between the metal track and the ILD.

The information and experience gained through Al interconnect processing was transferred to Cu interconnects during early implementations [99]. Continued research and experience with fabrication methods found that tantalum (Ta) performed considerably better than the previously used Ti based layers [100, 101]. A large number of published work describe the barrier properties of Ta and TaN (tantalum nitride) films with respect to the diffusion and adhesion properties associated with Cu [102, 103]. While these metallic barriers provide sufficient protection against the common issues associated with Cu interconnects, they also affect the electrical properties of the track. As a result the resistance of the metal track, given a constant barrier thickness, becomes increasingly dominated by the barrier layer as the line width of the interconnect decreases [104]. This is because the most common barrier metals have a high resistivity value; for example Ti has a resistivity of 39×10^{-8} Ωm and Ta has a value of 12.2×10^{-8} Ωm in comparison to the resistivity of Cu at 1.539 10^{-8}Ωm [105] [1].

Dielectric barriers tend to be used to cover the upper surface of the Cu interconnect tracks and are referred to as *capping layers*. They can either be placed in between the multiple layers of a wiring scheme or used as the final passivation layer. Although SiO_2 films can be used with the above mentioned metal barrier layers as the ILD for a Cu wiring scheme, they are not suitable for capping the lines. This is a result of the oxidation, adhesion, and diffusion issues described above. However, it has been found that silicon nitride (SiN) films provide sufficient protection against this problem for Cu lines, and as such are employed as capping and passivation layers [106–109]. Work by Prasad et. al. [110] and Tsui et. al. [111] suggest that the inclusion of carbide precursors to form either SiCN or SiCO layers provides similar barrier properties to those of SiN films but with improvements in operation of the interconnect system due to lower

[1]Quoted resistivity values are representative of pure metals at a temperature of 273 K

dielectric constants. Although in theory these dielectric materials can be integrated as a trench liner to provide sufficient protection in an IC, it is not as simple to implement in practice. The most effective barrier materials (such as LPCVD Si_3N_4) require high temperatures to create low defect films. These high temperatures are not compatible with the underlying circuitry and hence this method cannot be used. As the dielectric liners are non-conductive, they require further processing such as etch steps to allow electrical contact through vias.

4.3 Requirements for a Cu ECD test structure

The key features of Si ECD structures, as discussed in Chapter 2, that allow them to be used as standard reference materials are:

1. Rectangular cross-section of the features.
2. A heavily doped single crystal conducting track with a uniform resistivity for electrical measurements.
3. The "as-fabricated" line width is related to the number of Si atoms across its width.

Reference Cu ECD structures obviously need similar features but their implementation requires significant modifications. The major differences are:

1. Cu cannot be etched with atomically vertical sidewalls.
2. Cu tracks are typically encased in a diffusion/adhesion barrier such as tantalum nitride (TaN) which makes them non-homogeneous, resulting in a non-uniform resistivity.
3. Cu does not have a regular crystal structure that can be used to determine line width.

These differences make producing a Cu ECD structure a much more challenging task. However, despite these differences the strategy used to produce Si ECD reference material can be adapted to fabricate Cu reference structures.

The design of an all-copper ECD structure was conducted in collaboration with NIST with an overview of the steps involved in its fabrication is presented in figure 4.3. This unique approach allows a damascene trench to be created using a moulding process which transfers the lateral dimensions from a preformed feature to the trench and therefore provides traceability for measurements. First a Si mesa is etched in (110) Si in a very similar manner to that used for Si ECD reference test structures (Fig. 4.3(a)). This structure, referred to as a *silicon preform* serves as the preform in the mould process to define the line width which will be duplicated in the Cu trench. A dielectric is then deposited to form a mould of the Si feature and preserves the line width during future fabrication steps (Fig. 4.3(b)). After the mould is in place a portion of the Si is selectively removed to create the trench for the Cu track (Fig. 4.3(c)). Finally a traditional Cu damascene approach for the deposition and patterning of Cu is used to complete the structure (Fig. 4.3(d)).

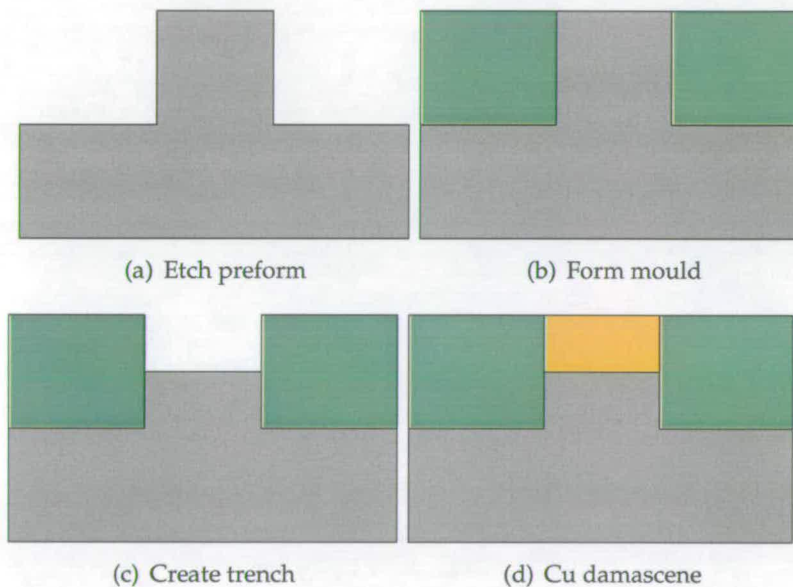


Figure 4.3: *Schematic illustration of the major stages in the fabrication of all-copper ECD test structures.*

The key element borrowed from the Si ECD RM fabrication is the use of (110) Si to produce mesas with rectangular cross sections that act as moulds for the Cu tracks. This approach also provides a reference measurement capability, as the single crystal Si underneath the Cu track (and with the same line width) can be used to calibrate the electrical measurement of the Cu track. Additionally, conducting barriers are not used to line the trenches prior to Cu deposition because this makes the tracks non-

homogeneous. This test structure enables line width to be determined using HRTEM (as well as similar techniques like AFM, SEM, SPM) and by electrical measurements. The key to the process described here is the ability to fabricate Cu lines using the damascene approach as detailed previously (Section 4.2.1).

4.4 Fabrication process

The fabrication process is outlined in figure 4.4 and the following sections provide full details of the process. Most of the tools and procedures employed during this study are typically found in traditional micro fabrication facilities for the manufacture of semiconductor devices. All processing was conducted on 3 inch Si wafers in a CMOS compatible fabrication facility. The final fabrication process is detailed in the run sheet presented in Appendix C.2.

An experimental batch of wafers was initially run to demonstrate the feasibility of the process described, as the specified substrate material ((110) Si wafers) was not available at the beginning of this study. The patterning of the silicon preform was accomplished using dry etching techniques [92,112] to define the pattern in (100) single crystal bulk Si wafers, which are more readily available than those of the (110) single crystal variety. This initial run of the process highlighted various issues associated with the design, all of which were improved upon for the subsequent iterations of the process until the resulting structure met the specifications for an all-copper ECD structure. Figure 4.5 shows a cross sectional SEM image of one of these initial experimental structures with the key components of the structure labelled. Note that the Cu track does not possess a rectangular cross section because of the use of dry etching of the silicon preform.

4.4.1 Silicon preform

The material chosen to serve as the preform in the moulding procedure is bulk Si wafers. This is because the structural and mechanical properties of Si allow it to withstand the fabrication steps involved in this process [113]. Si has been used in semiconductor engineering for over 50 years and as a result there is a significant knowledge-base of fabrication techniques and tools underpinning the development

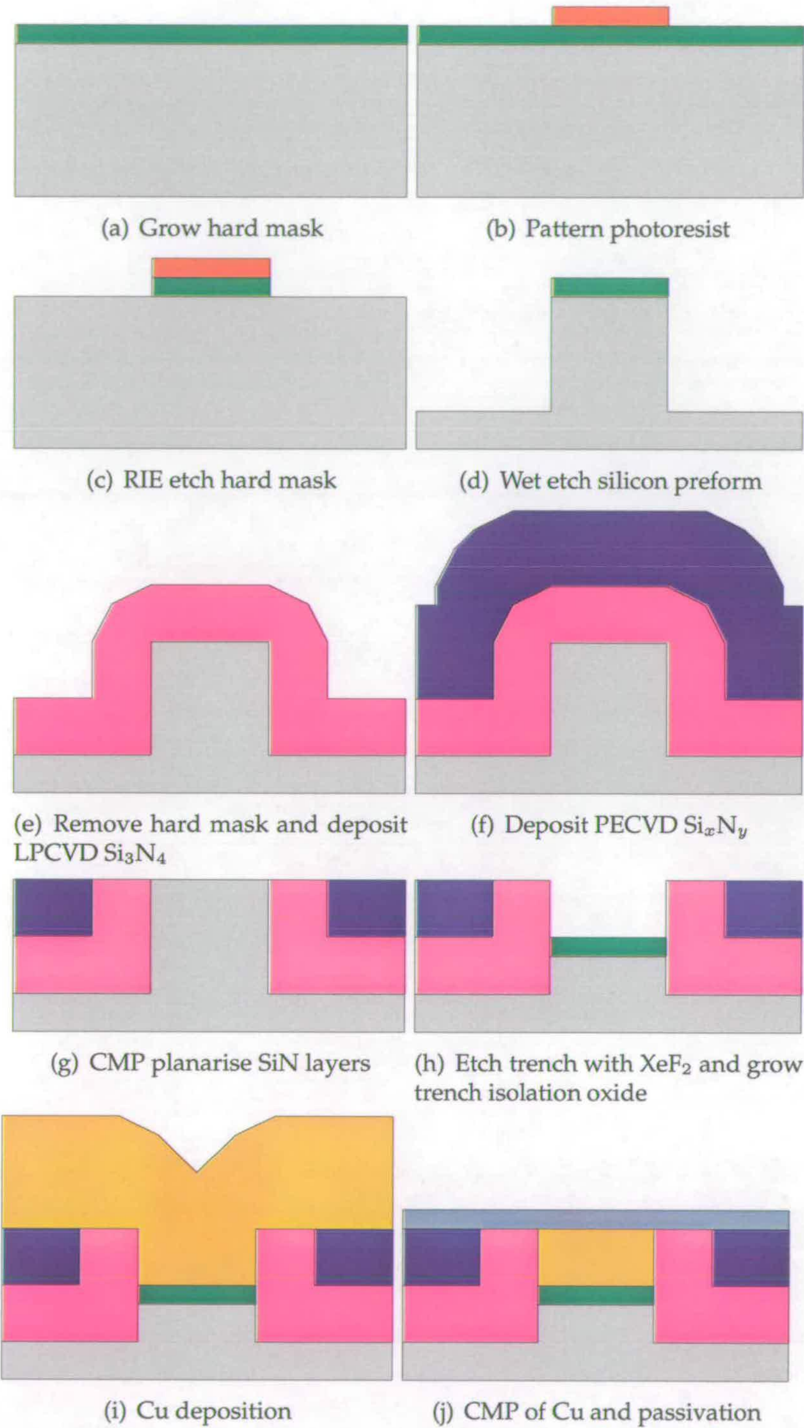


Figure 4.4: *Schematic illustration of the detailed process employed for all-copper ECD structure fabrication.*

of this process. Another, and possibly the most important, feature is the anisotropic etch nature of single crystal Si. This is such that standard techniques exist to selectively

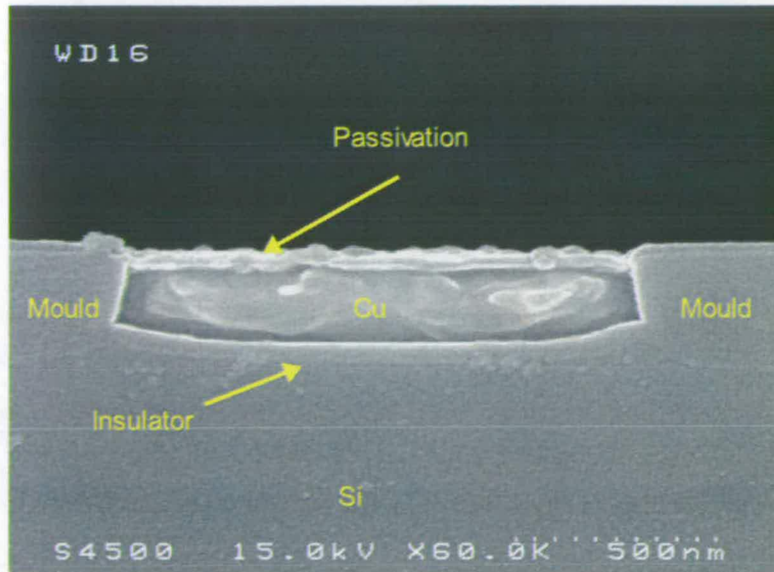


Figure 4.5: *Cross section of initial experimental batch to demonstrate feasibility of Cu ECD process.*

etch Si along specific planes in its crystal structure [114]. Based on previously reported work into anisotropic etching of Si [115,116] and the requirements for the current test structure, (110) Si wafers are used as the substrate for this study. When a pattern is aligned to the {112}crystal direction in (110) Si and then anisotropically etched, the resulting structures possess a rectangular cross section with nearly atomically parallel sidewalls defined by the {111} crystal planes. This is due to the inherent lattice plane selectivity of the wet anisotropic etch solutions employed in this type of work. As the wafers are of single crystal nature, HRTEM can also be used to accurately determine the line width of etched (110) Si features by counting the lattice planes across the width of the structure [24]. This method has been adopted in the current test structure design to determine the line width of the Cu tracks and also to provide a source of traceability for the structure.

The pattern used for both electrical measurement and the HRTEM measurement is defined using a light field mask such that the etched structure forms free standing Si tracks. The first step in this process is to thermally grow a 0.2 μm thick SiO_2 film to act as a hard mask (Fig.4.4(a)). The hard mask is employed to provide a high selectivity material to transfer the pattern into the Si substrate during the wet etch step that follows. Photoresist is then spun on top of the SiO_2 layer, patterned using a 5x image reduction stepper and developed to form the resist pattern (Fig.4.4(b)). To

ensure the pattern is aligned to the crystal planes as far as possible, the stepper aligns the mask reticle to the wafer flat prior to printing. After this an RIE tool is used to transfer the pattern into the SiO_2 film (Fig.4.4(c)). The photoresist is then removed using an oxygen plasma asher.

At this point, the pattern is ready to be transferred into the Si wafer (Fig.4.4(d)). The literature generally reports on two main etch chemistries for anisotropic wet etching of Si. These are potassium hydroxide (KOH) and tetramethylammonium hydroxide (TMAH). Of these, TMAH solutions are gradually replacing KOH chemistries as they have higher selectivity to SiO_2 films and do not contain ions that are harmful to semiconducting devices [115]. As this work is concentrating on developing a process for CD material fabrication, the etching of the masking film during the wet etch could produce non-uniformities in the etched structure. To minimise any sources of contamination in the CMOS compatible fabrication facility, KOH was avoided due to the harmful potassium ions [117], and hence TMAH chemistry has been chosen for this study.

One area of caution with the procedures and methods for TMAH etching of Si, as found in the literature, is the high etch rates generally reported, with typical values ranging from 0.5 μm min^{-1} to 1.6 μm min^{-1} [115]. The main application of TMAH etching is in bulk micro machining through large masses of Si and hence large etch rates are beneficial. The Cu ECD process here, on the other hand, specifies structures with dimensions of ≤ 1 μm deep and such high etch rates do not provide control over etch depth and uniformity. Sonphao and Chaisrikul [118] describe the results of a range of experiments conducted to determine the effect of temperature and concentration of TMAH on the etch rate of (100) Si material. In this work it was found that the higher the concentration (concentration ranged from 5 wt% to 40 wt% TMAH) the lower the etch rate, additionally the higher the temperature (temperature was ranged from 60° C to 90° C) the higher the etch rate. This work is supported by Steinsland et. al. [119] who report on the etch rates of (110) Si wafers, amongst others, and also extend the experiments to determine the etch rate against temperatures down to room temperature. These results led to the conclusion that high concentrations of TMAH at low temperatures will provide lower etch rates and hence better control over etch depth. These papers also report on the variation of etch rate due to equipment

setup and conditions used during wafer processing. In an effort to justify the values reported and determine an appropriate process for the current work, an experiment was conducted based on the values reported in these papers.

Samples were prepared using the SiO_2 hard mask growth and photolithography aligned to the {112} crystal planes as described above. The highest concentration of TMAH solution available for use was 25 wt% and therefore was chosen as a constant for the experiment. Figure 4.6 details the etch setup for the processes used in the study. A standard Pyrex™ beaker placed on a temperature controlled hot plate is used. The Si wafers are supported using a Teflon™ wafer holder in the centre of the beaker with a magnetic stirrer to agitate the solution and distribute the temperature in the etch bath. The TMAH solution was maintained at a temperature of 50 °C to provide control over uniformity whilst still maintaining a reasonable etch time for the 1 μm depth required. The wafer was held using the vertical wafer holder shown in figure 4.6(b).

From initial etch experiments it was observed that the Si did not react with the etch solution for an extended period of time (in the order of 1 to 2 hours) when initially submerged into the solution. This was believed to be caused by the native oxide (SiO_2) which forms on the surface of the Si after only a matter of hours of exposure to atmospheric conditions [120]. This native oxide was removed with a brief dip in a low concentration (1%) HF solution. This dilute solution and short etch time was chosen to minimise any etching of the patterned hard mask that might occur. The addition of this step allowed the TMAH etching to commence as soon as the wafer was submerged in the solution.

Samples were etched for a constant time of 10 minutes and the step height measured using a surface profilometer. The resulting average etched depth of the Si structures was between 1.2 μm and 1.5 μm, which compares favorably with the 0.15 $\mu m\ min^{-1}$ etch rates reported in the literature [119]. During this experiment it was observed that the etch rate varies considerably with the temperature of the etch bath as mentioned in most of the literature on the subject. Ideally an etch bath with rigorous control over etch temperature and recirculation would be specified to achieve optimal performance and repeatability. However, when measuring the height of the etched silicon preforms to establish etch rates, a consistent variation in depth from top to bottom of the wafer was detected, therefore highlighting the non-uniform nature of the etch system being

used.

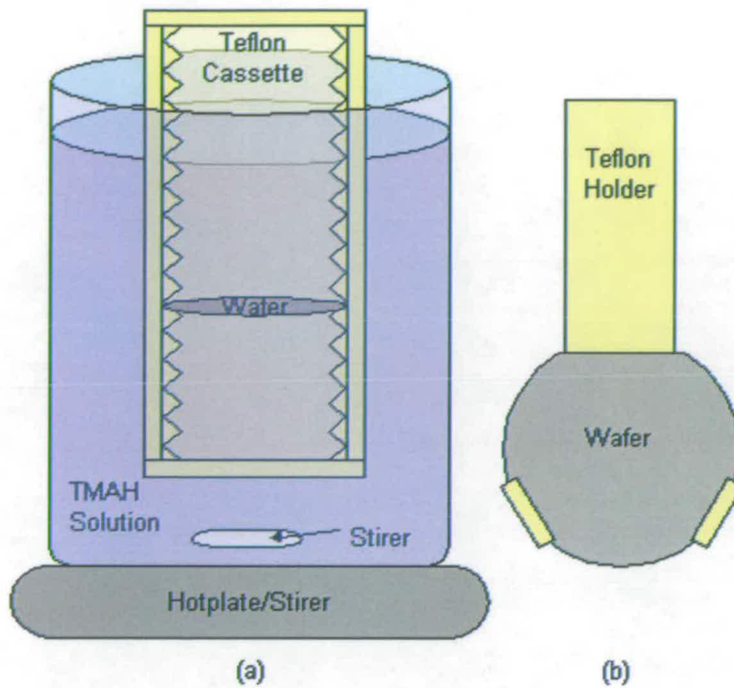


Figure 4.6: *Setup used for TMAH etching of Si wafers*

Along with etch rate, the uniformity of the feature height is an important aspect of the silicon preform formation when considering the further processing steps required. For example, non-uniformities in the etch step can translate to varying degrees of planarity in the CMP stage due to the feature height differences and resulting step coverage of the mould material. The positioning of the wafer was the focus of an experiment to determine the optimum conditions for the etch depth distribution using the available wet etch setup. In an attempt to minimise the quantity of solution used and to maintain a small footprint for the hot plate, a beaker with a 4 inch diameter was used.

First, a Teflon™ wafer cassette which could hold wafers in a horizontal position whilst submerged in the etch solution was investigated as shown in figure 4.6(a). There were two variations on this approach for uniformity, patterned surface of the wafer directed upwards and downwards. The second setup used the wafer holder shown in figure 4.6(b) to stand the wafers in a vertical orientation whist in the solution. The two variations of this test were with the wafer flat directed towards the top of the beaker for the duration of the etch, and then a separate test where the wafer was rotated by 90° at even intervals during the etch. In this experiment the wafers were etched for a constant

time of 10 minutes in a 25 wt% TMAH solution at 50 °C. Uniformity is quantified using a surface profilometer to measure 13 points over the surface of the wafer for step height of the Si features. Results from these experiments are presented in Table 4.1 with uniformity calculated using equation 4.1, where Max and Min represent the largest and smallest measured heights respectively.

$$Uniformity = \frac{Max - Min}{Max + Min} \times 100\% \tag{4.1}$$

Position	Etch uniformity
Horizontal face up	15.4%
Horizontal face down	40.2%
Vertical flat up	32.6%
Vertical rotated	38.4%

Table 4.1: *Results of uniformity experiments for TMAH wet etch on (110) Si wafers.*

Based on the results of these experiments, the final optimised process converged on an etch solution of 25 wt% TMAH at 50 °C with the wafer supported in the horizontal position and with the surface of the wafer facing up. The desired etch depth of 1 μm was achieved with a time of between 7 and 8 minutes with the above setup. The height of the silicon preforms was measured prior to the removal of the hard mask to ensure they were to the specified dimensions. After etching the silicon preform, the SiO_2 hard mask was removed in a buffered HF (BHF) dip.

A cross sectional SEM image of the wafer after patterning and etching is presented in figure 4.7. This image demonstrates the vertical profile which exists in the sidewalls of the etched feature. It can be seen from the overhang of the SiO_2 film that the line width of the etched silicon preform does not match that defined by the hard mask. This was observed repeatedly on numerous samples and to varying degrees. This is due to the misalignment of the wafer flat with the crystal orientation and can be directly attributed to the rotational line width reduction theory described by Allen et. al. [121]. The authors state that "the width of the feature W_f can be estimated from the design width W_d and the rotation angle".

The wafers themselves contain a flat which has been cut aligned to the {112} crystal plane of the Si by the wafer manufacturer. The photo-lithography stage employed

to pattern these structures uses the wafer flat to align the pattern. However, the accuracy of the pattern alignment with the crystal plane relies on the ability of the wafer manufacturer to accurately define the orientation of the wafer flat relative to the crystal planes. Typical values for the tolerance of the wafer flat alignment to the crystal plane are in the order of ± 1°. While this issue does not pose a large problem for the processing of the structure, it will produce a variation of line width between different wafer lots. If the pattern is excessively misaligned to the crystal planes, small line widths could be completely over etched and no longer useable.

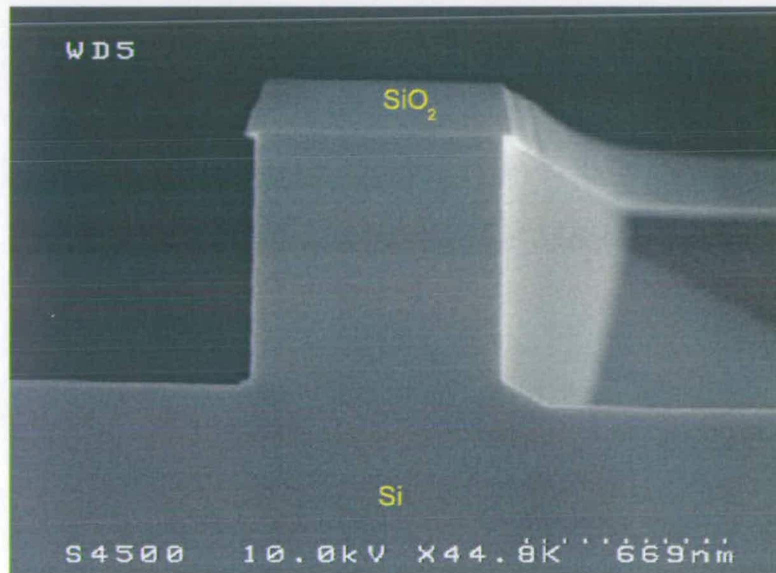


Figure 4.7: *Etched silicon preform with hard mask still in place.*

4.4.2 Creation of the preform mould

The next major stage is to ensure the dimensions of the silicon preforms are preserved and hence provide traceability for the CD of the Cu trench. To accomplish this a dielectric film is blanket deposited over the wafer surface. This creates a mould around the silicon preform and acts to physically maintain its line width especially during the etching of trenches for Cu deposition. This dielectric film must possess good mechanical, chemical, and electrical properties in order that further processing steps can be conducted while still maintaining the dimensions of the trench. A non-conductive film is selected to prevent interference with the electrical measurements during parameter extraction. Another important point to note with the choice of the material for the mould is its compatibility with Cu. These compatibility issues

include meeting the requirements for adhesion, diffusion and oxidation as set out previously (Section 4.2.2), bearing in mind that no barrier metal is being used. Cu has been reported to have a high adhesion strength to low pressure chemical vapour deposition (LPCVD) stoichiometric SiN (Si_3N_4) [122,123]. This is of importance for the following Cu CMP stage of the damascene process where poor adhesion will result in delamination of the film due to the forces involved. Furthermore LPCVD Si_3N_4 provides sufficient barrier properties to prevent the diffusion and oxidation of the Cu track. The adhesion of the Cu to the LPCVD Si_3N_4 was confirmed by a successful result from the standard *tape test*.

One potential issue associated with LPCVD Si_3N_4 is the high stress induced as a result of the deposition, which can cause deformation or cracking of the film and structures on the wafer [124]. As such the film thickness should be kept to a minimum to prevent any of these effects. However, the dielectric mould layer must be of greater thickness than the silicon preform to allow the CMP stage to be conducted without excessive dishing of the dielectric. To address this, plasma enhanced chemical vapour deposition (PECVD) can be operated in regimes where the stress and density of the film can be controlled. In the initial architecture a thin layer (50 nm) of LPCVD Si_3N_4 was deposited over the surface of the etched Si wafer. This thickness was chosen as it is comparable to barrier layer thicknesses employed as trench liners in Cu damascene patterning for larger line widths. However, because of stress concerns, highlighted later in this chapter, the thickness of the LPCVD Si_3N_4 was increased to 500 nm to provide additional mechanical support during the formation of the trench step (Fig. 4.4(e)).

Following this, PECVD Si_xN_y is blanket deposited in sufficient thickness (1 μm) to provide a surface for CMP planarisation that will also minimise any erosion or dishing effects (Fig. 4.4(f)). The PECVD Si_xN_y also acts to provide further structural support in addition to the LPCVD nitride to form the dielectric mould. The PECVD film was initially deposited using a mixed frequency[2] recipe at a ratio of 6:2 (high frequency:low frequency) to a thickness of 1 μm. This ratio was chosen so that the resulting film exhibited near zero stress at room temperature as deposited. Figure

[2]Mixed frequency PECVD films are composed of alternating cycles between the high frequency and low frequency components. The stress of the mixed frequency film can be altered by specifying the ratio of deposition times at each of the two frequencies.

4.8 displays a cross section of the structure after deposition of the two layer SiN mould of the silicon preform.

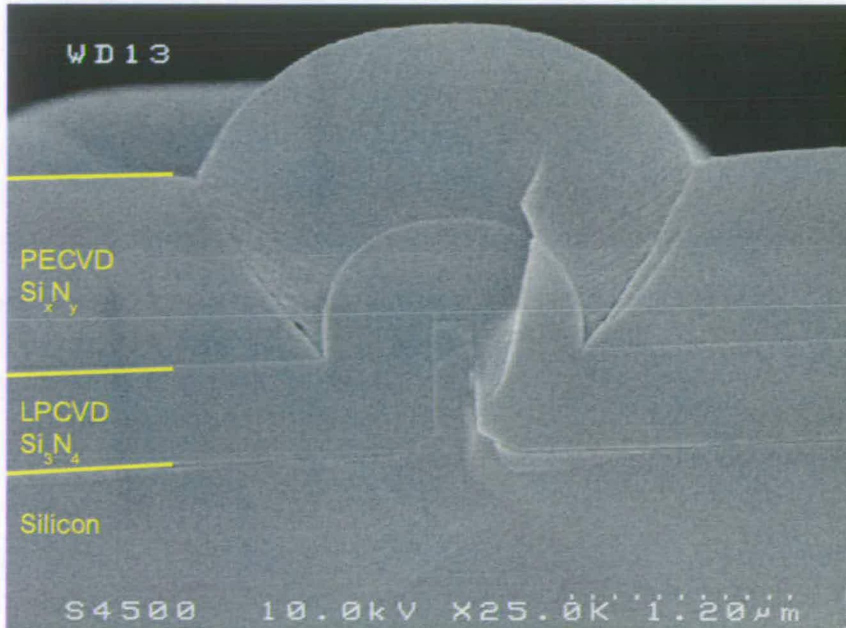


Figure 4.8: *Structure after deposition of both LPCVD and PECVD SiN.*

The next step is to expose the tops of the silicon preform and provide a planar surface for the Cu damascene process. This is accomplished using CMP to polish the wafer until the silicon preforms are exposed on the top surface, at which time the planarisation is complete (Fig. 4.4(g)). Unfortunately industry does not have much experience with planarising SiN in this manner which requires polishing of 2 different flavours of SiN layers and stopping on Si mesas. Hence, no appropriate recipe or slurry exist. For this reason a standard SiO_2 damascene recipe was used as the starting point to develop a new recipe for SiN planarisation. The slurry used was Klebosol 30HB50 which contains 30% abrasive content and allows planarisation of dielectric materials. An IC1000 K-groove pad on a SUBA-IV backing from Rohm and Haas was used as the polishing surface.

The actual recipe employed for the final product used a two step polishing sequence. The first stage was a bulk removal and was used to reduce the thickness of the SiN over the silicon preforms. This also accomplished the majority of the planarisation of the wafer. When the thickness of SiN over the preforms was reduced to ~200 nm through polishing, the first stage was completed. The second stage uses a much lower down-

force on the wafer and removes the SiN material at a much slower rate. This results in greater control of the CMP process which can be stopped when the silicon preforms are exposed. This minimises the degree of over polishing that would otherwise result in dishing of the field area. As no endpoint detection is provided on the available tool, the wafer was polished on a controlled time basis. In this method the removal rates are determined for the materials and then used to program the time for the polishing recipe.

After the wafers are polished sufficiently, a post-CMP clean using a high pressure DI water scrubber was used on all wafers to prevent particulate contamination from slurry residue on the surface of the wafer. Figure 4.9 demonstrates the planarity of the wafer after this unique CMP process and the ability to expose the top of the silicon preform.

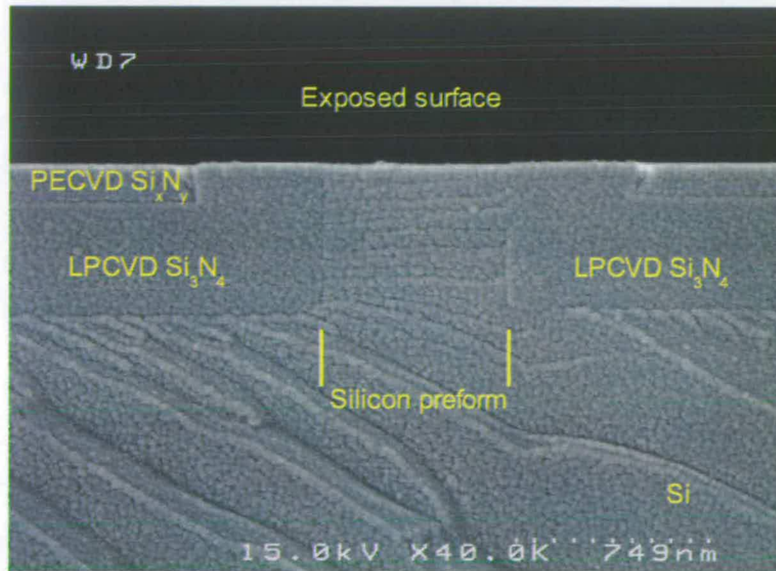


Figure 4.9: *Structure after CMP planarisation of the nitride layers.*

4.4.3 Create trench

With the top of each Si structure exposed and the rest of the wafer protected by SiN, the next step is to etch vertically into the silicon preform from the top surface to create trenches for the Cu lines. This must be performed such that a horizontal and flat surface is present in the bottom of the newly formed trench (Fig. 4.4(h)). This is important as a track with a rectangular cross section is required to provide greater

traceability between the electrical measurements and the HRTEM line width count. Another requirement for this etch is that it must have extremely high selectivity to both varieties of SiN such that the sidewalls of the trench are not attacked and the CD is maintained throughout the height of the structure. Two different methods were investigated to accomplish this task.

A sulphur hexafluoride (SF_6) based RIE etch was first used based on the theory that the isotropic nature of the plasma etch would maintain the horizontal bottom of the trench. However, in a number of experiments used to establish a base recipe for the process it was observed that the PECVD Si_xN_y film was etched along with the Si at comparable rates of ~3:1 (Si:SiN). Referring to figure 4.10, the poor selectivity to PECVD Si_xN_y can be observed by its decreased thickness with relation to the top of the LPCVD Si_3N_4, which has better resistance to the etch. As a result this method for creating the trench was abandoned for alternative approaches.

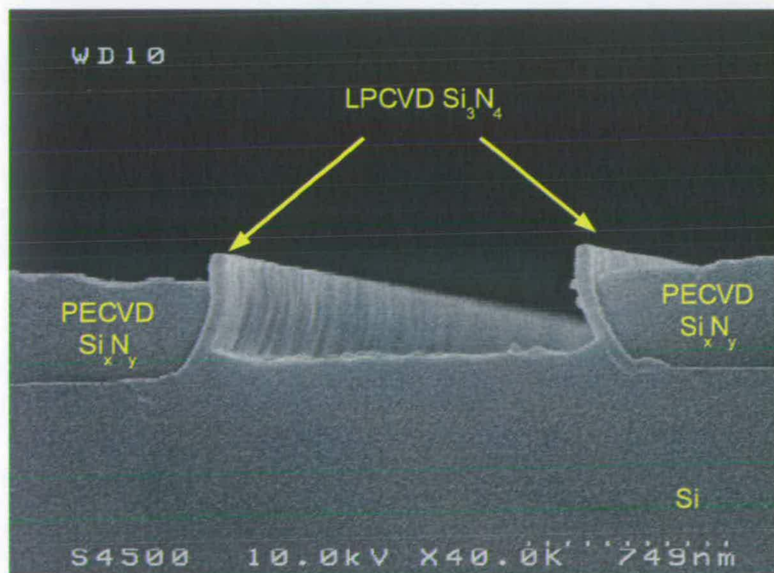


Figure 4.10: *Result of SF6 plasma etching of silicon preform to form trench.*

Next xenon difluoride (XeF_2) was selected to etch the silicon to create the trench. XeF_2 is typically used in vapour form to isotropically etch Si and poly-Si films in MEMS applications for release etches [125]. The tool used for these studies is a research size vapour etch tool which allows the user to program any of the parameters involved in the etch. The system uses a carrier gas of helium which is flown through solid XeF_2 crystals to generate the XeF_2 vapour used in the etch chamber. Work by Williams and

Muller [90] reports that the selectivity of Si to SiN in XeF_2 is roughly 500:1 (depending on deposition method) and that SiO_2 does not etch enough to measure. Therefore, this should largely overcome the selectivity issues that arose with the use of the SF_6 RIE etch.

Initial experiments with this stage used samples after the CMP step with no additional preparation and then subjected them to the XeF_2 etch. Measurements from these samples demonstrated that the Si did not etch for approximate 1 minute when exposed to the vapour, furthermore, when the Si did etch it presented a rough and uneven surface on the trench bottom. After careful consideration, it was believed that this was caused by the thin native film of SiO_2 that forms on Si similar to that observed during the TMAH etching of the Si preforms mentioned previously. Whilst this film tends only to grow to approximate 10 angstroms thick [120], it provides enough resistance to the XeF_2 vapour to delay the etching of the Si and cause the rough surface. This theory was investigated using a brief dip in a dilute (1%) solution of HF. One point to note is that the HF does also attack the PECVD Si_xN_y at nearly equal rates, while the LPCVD Si_3N_4 is known to etch very slowly if at all [91]. However as the trench has not been etched the line width is not effected, also the HF solution is very dilute and etches only a matter of nanometers from the PECVD Si_xN_y along with the native SiO_2.

In a further effort to optimise the flatness of the trench bottom, the maximum trench etch depth is kept less than 0.5 µm. To enable such a shallow etch, the conditions on the XeF_2 vapour etch tool were adjusted to heavily dilute the XeF_2 vapour with large amounts of helium which has the effect of reducing the etch rate. It was found that the lowest etch rate was achieved by using the maximum helium dilution as well as reducing the flow of XeF_2 vapour. The ratio of flow of helium to XeF_2 vapour used for this slow etch is 100:1 and provides an etch rate of between 0.35 and 1 $\mu m\ min^{-1}$ depending on exposed Si area. These high etch rates are the result of the loading effect on the vapour etch. As the majority of the field area of the wafer is covered with the SiN films, the exposed Si represents only a small portion of the whole wafer. As a result the Si etches much faster than it would had more Si area been exposed to the vapour. Unfortunately the etch cannot be made to slow down any more in the tool used for this work. Fortunately the etch is repeatable enough to allow the user to run a portion of the expected etch time on a sample, then measure the depth of the trench to

determine the etch rate of that particular setup. The sample can then be etched again with adjustments to the total etch time made to reflect the etch rate achieved from the first portion of this step. Figure 4.11 confirms that the HF dip immediately prior to etching permitted the XeF_2 etch to create the trench while maintaining a flat bottom. This was determined by observing the image captured from the SEM and identifying that the trench bottom is all contained on the same row of pixels [3].

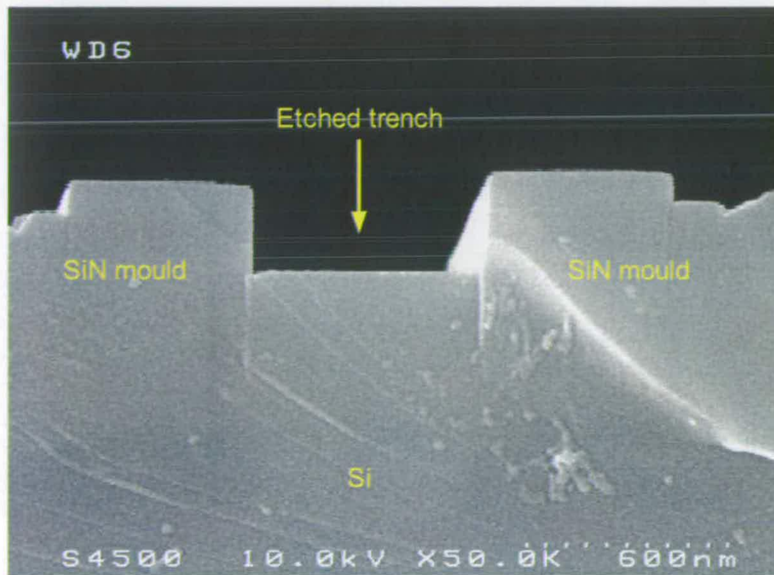


Figure 4.11: *Result of XeF_2 vapour etching of silicon preform to form trench using HF dip prior to etch.*

The final step in the trench formation process is to isolate the trench from the underlying bulk Si. This is accomplished with a thin layer of SiO_2 grown (Fig. 4.4(h)) with a process similar to that employed to grow gate oxide films in semiconductor fabrication. This film was initially grown using a high temperature furnace tube in an oxidising environment. A standard process that was developed for gate oxidation known as "WETOX11" was used at a temperature of 950 °C, taking approximate 1 hour to grow a targeted 200 nm film. This process used a mix of hydrogen and oxygen to form an H_2O atmosphere and accelerate the oxidation of the Si. When the initial batch (which employed the 50 nm LPCVD Si_3N_4) of devices experienced this thin gate oxidation to isolate the trench prior to Cu deposition, it was noticed that the width of the trench increased at the top when compared to the bottom of the trench as shown in figure 4.12. The cause of this was later confirmed to be due the high temperature

[3]Optics used in the SEM permit an image resolution of 640 × 480

growth of SiO_2, which also resulted in the annealing of the PECVD Si_xN_y film. This caused the stress in the SiN to become more tensile, at room temperature, and created a pulling force on the trench sidewalls causing the deformation of the trench. As a result the CD dimension, that up to this point had been preserved, was altered and no longer traceable.

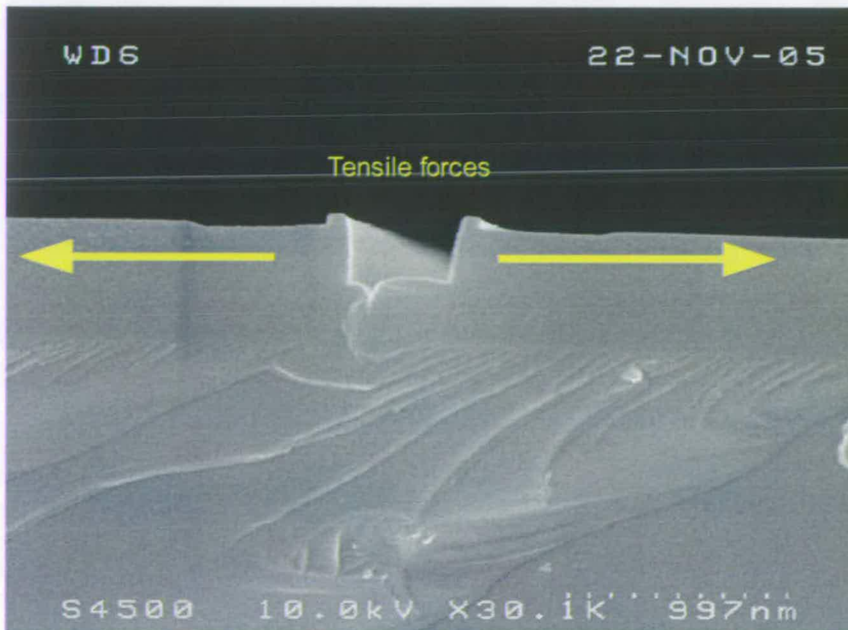


Figure 4.12: *Cross section demonstrating the sidewall deformation after the trench oxidation step.*

An extensive experiment was conducted to characterise these stresses and fully understand the source of the problem. This experiment involved depositing low frequency (LFSIN), high frequency (HFSIN), and mixed frequency (MFSIN) PECVD Si_xN_y films and measuring their "as deposited" and "as annealed" stresses. Wafer stress was calculated by measuring the wafer bow using a stylus profilometer and calculating the wafer radius both before and after the deposition and anneal steps. These values could then be used with Stoney's formula [126] to calculate the stress in each film. The anneal step was used to simulate the thermal cycle involved in the oxidation without introducing the oxidising environment and was conducted at 1000 °C in a nitrogen rich atmosphere.

The results of this experiment are presented in figure 4.13. With this in mind, the HFSIN recipe was comprised of 100 % high frequency, the LFSIN was 0 % high frequency (all low frequency) and the MFSIN recipe was 80 % high frequency (Ratio of

6:2 high to low frequency). The stress of the high frequency "as deposited" SiN film is ~530 MPa tensile and becomes ~1500 MPa tensile after the anneal process, an increase of ~1000 MPa of tensile stress. The low frequency "as deposited" stress is ~600 MPa compressive and becomes ~400 MPa tensile after annealing. Therefore the increased stress induced by the anneal (~1000 MPa tensile) of the low frequency deposited film is comparable with that observed for the high frequency SiN. On the other hand the MFSIN recipe saw a change of ~1200 MPa going from almost zero stress to ~1220 MPa tensile. This increased change of stress is believed to be attributable to the sandwich of layers used in the mixed frequency SiN deposition process and their interaction during the anneal cycle.

Based on these results, it can be observed that the low frequency film has the lowest absolute stress value after the anneal step, despite being in tensile stress and having a comparable change in stress during the anneal. With this information, the process was modified to reflect these findings and a LFSIN deposition recipe was used to deposit the PECVD Si_xN_y portion of the SiN stack. As a further measure to prevent sidewall deformation, the LPCVD Si_3N_4 layer was increased in thickness from the 50 nm used initially to provide additional structural support. The total thickness of this film is limited to approximately 700 nm, because the accumulated stress and the possibility of cracking in the film and therefore cannot be used to make up the complete preform mould. As a precaution the target deposition thickness of the Si_3N_4 was kept to 500 nm, and the remaining required film thickness (1 μm) of the preform mould was made from the PECVD Si_xN_y.

To minimise the stress that results from thermal cycling and annealing of the SiN film, the $Si0_2$ film is thermally grown at a reduced temperature of 800°C using a slow ramp from room temperature to oxidation temperature and back to room temperature again over a 10 hour period using a 5 °C per minute ramp rate. This slow controlled ramping process allows the film to relax more during the thermal cycle and reduces the thermal shock that could otherwise exist. The oxidation process used a "wet" recipe with an H_2O atmosphere. This type of recipe was chosen as an oxygen rich environment on its own did not provide sufficient SiO_2 thickness within a reasonable period of time. The thickness of the isolation layer was also reduced to 20 nm to minimise any forces resulting from the growth of the film inside the trench. When observing cross section

images of the trench after the modified oxidation step in figure 4.14 it is made apparent that the sidewalls are not deformed in the same manner as seen previously. However, charging of the sample as a result of the SEM imaging technique makes it unclear whether the sidewalls are truly "vertical" and further analysis is required.

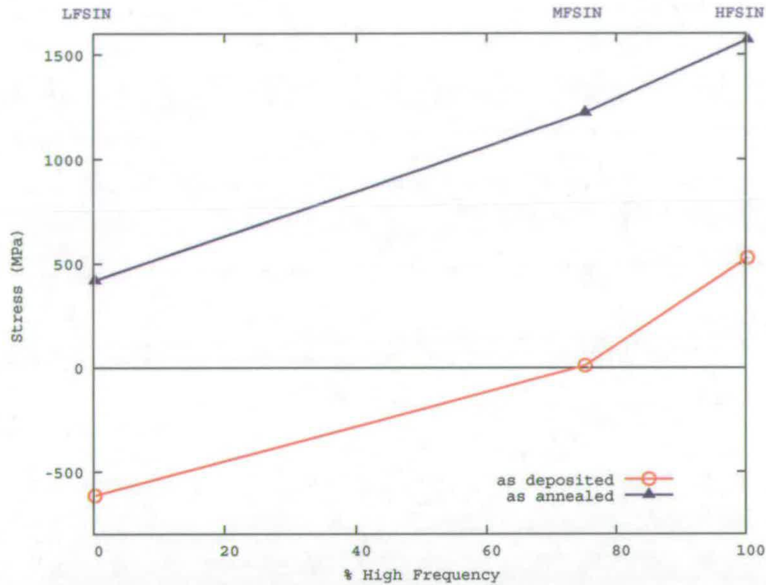


Figure 4.13: *Relationship between the stress and deposition method for "as annealed" and "as deposited" PECVD Si_xN_y films.*

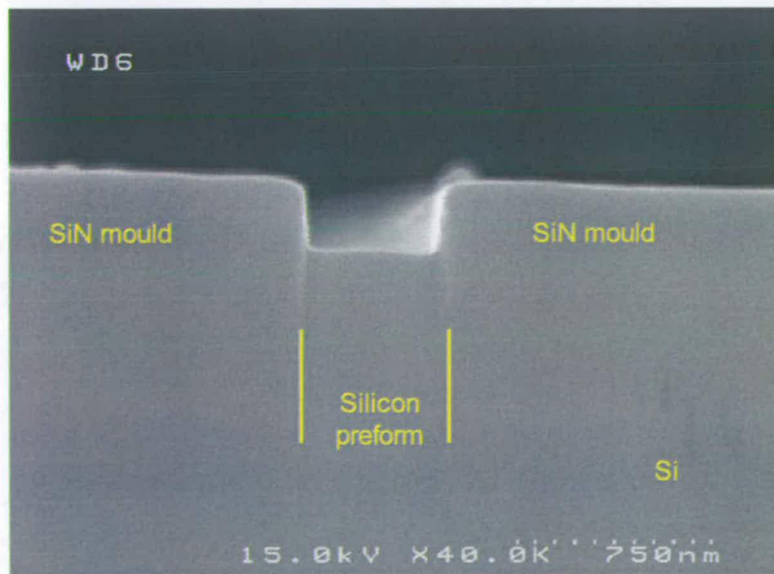


Figure 4.14: *Cross sectional SEM of trench after XeF_2 etch and oxidation step.*

4.4.4 Copper damascene

The final process sequence is the creation of the Cu tracks and hence the final test pattern. This starts with the blanket deposition of Cu over the surface of the wafer (Fig. 4.4(i)). Initial trials were used to evaluate the extent to which DC magnetron PVD sputtering of Cu could be used. Investigations were concentrated on the fill capability of narrow line widths, those less than 0.5 μm (the equivalent of a 1:1 aspect ratio). The Cu is deposited to a thickness of 1.5 μm to allow CMP planarisation to be conducted with minimal dishing, in the same way that the PECVD Si_xN_y was deposited thicker than the height of the silicon preform. A standard sputter recipe was used to deposit the required thickness using a 1 kW DC power at low (3 mT) pressure. Cross sections revealed that this resulted in the formation of voids in the narrower line widths as seen in figure 4.15.

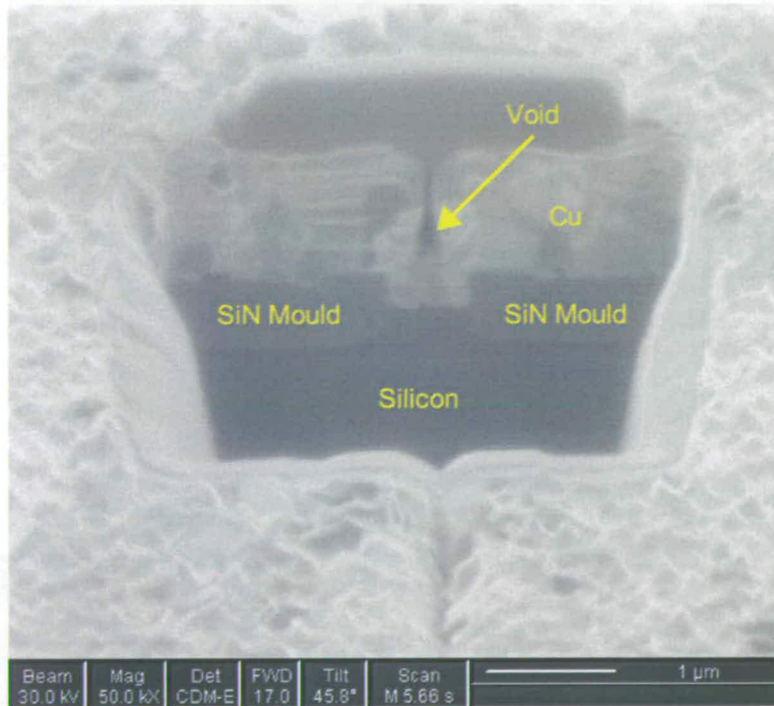


Figure 4.15: *FIB cross section demonstrating voids in narrow line width Cu tracks as a result of DC PVD sputtering.*

In an effort to improve the fill capability of the Cu film, and hence avoid the formation of defects in narrow line widths, a number of experiments focusing on the use of Cu electroplating were carried out. The goal of the experiments was to determine if the plated film could overcome the issues of poor fill and void formation seen in the PVD

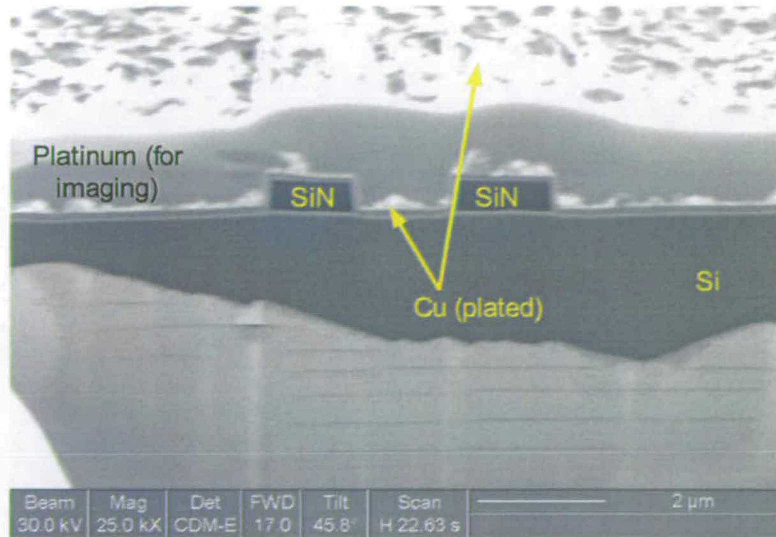
deposition results.

While commercial Cu plating equipment and chemistries do exist, they can be costly, and require expensive setups to maintain them at optimum conditions. This type of tool was not available during this portion of the work. The basic theory and principles around electroplating are discussed in Chapter 6. For the purpose of these experiments a simple electroplating setup was used employing a beaker, simple electrolyte, anode and sample holder. The electrolyte was based on a recipe reported by Liu et. al. [127] containing copper sulphate (Cu_2SO_4) and sulphuric acid (H_2SO_4) with DI to make up the volume as described in Table 4.2. A sheet of Cu metal was used as the anode material so that the depleted Cu ions would be replenished by the dissolution of the anode material. Using information and advice from staff in the School of Chemistry at the University [128, 129], a set of initial parameters were established.

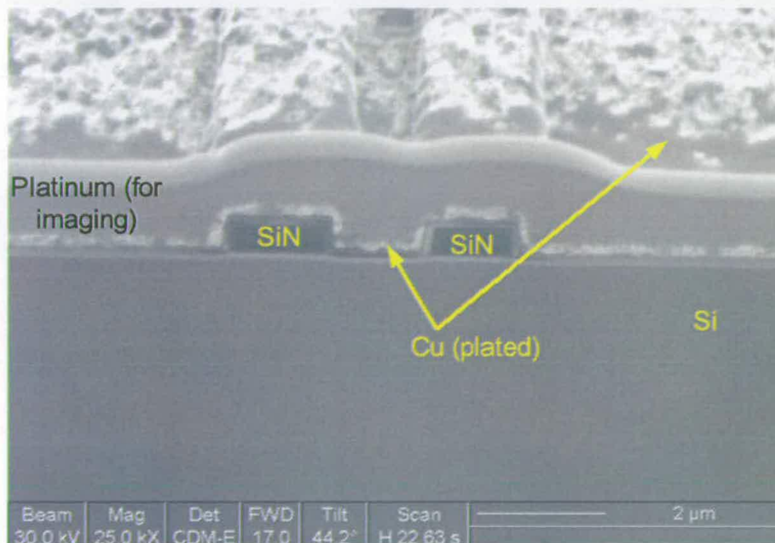
Samples were prepared with trench patterns etched into a 500 nm thick layer of SiO_2 to emulate the conditions seen in the preform trench. They were then coated with a 50 nm layer of PVD Cu to act as a seed layer. The first attempt at plating used a conductive, spring loaded clamp to make electrical contact with the seed layer of the samples. Initial plating runs at three different current densities were used to establish the settings to achieve a uniform film within a structure. Two of these are documented in Table 4.2, while another, higher (60 mA cm^{-2}), current density was found to result in the decomposition of water, forming hydrogen on the wafer surface and consequently has not been used in the subsequent comparison. Results of the plating trials are shown in the cross sections in figure 4.16 for the two lower current densities. From these images it can be observed that the high current density recipe provides a more conformal coating of plated material. The lower current density results in larger grain growth, but the grains are more sparsely distributed and present a rougher surface.

Component	Concentration (g/L)
Copper sulphate	50
Sulphuric acid	20
Experiment	**Current density (mA cm^{-2})**
Low current density	5
High current density	25

Table 4.2: *Plating recipe used for damascene copper plating trials.*



(a) Low current density



(b) High current density

Figure 4.16: *FIB cross section of Cu electroplating experiments.*

Based on the results obtained from these preliminary trials a simple setup was established to plate entire 3 inch wafers. This consisted of a large beaker, Cu anode and a custom built 3 inch wafer holder. The setup is displayed in figure 4.17. Based on the higher current density recipe and established deposition rate, wafers were electroplated to evaluate the fill properties of the Cu film. Figure 4.18 shows a cross section image taken through a trench that has been filled by Cu using this electroplating process, and demonstrates the ability to fill these narrower trenches without forming voids. However, the measured thickness across the wafer exhibited a

variation in excess of 100% the mean thickness and hence the process did not provide a uniform enough film for the CMP stage. Such thickness variations would make planarisation and the control of dishing difficult in subsequent processing steps.

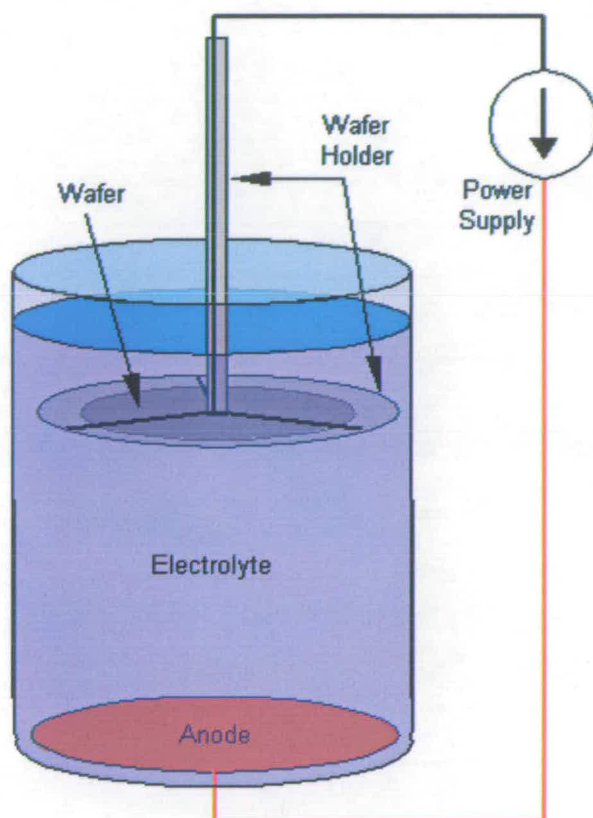


Figure 4.17: *Simple plating setup used for deposition of Cu onto 3 inch wafers.*

As PVD deposition is able to provide a very uniform film across a 3 inch wafer, this process was revisited to attempt modifications to the original recipe with the intent of improving the fill properties of the film. The addition of an RF bias to the wafer during DC sputtering increase the velocity of the metal ions near the wafer surface and results in re-sputtering of some of the deposited film onto the sidewalls of the trench, thereby improving the fill properties of the Cu in narrow trenches. This helps to prevent the problem of pinch-off as typically seen in DC PVD sputtering of high aspect ratio trenches by providing a more conformal fill. The FIB cross section in figure 4.19 shows the result of the Cu deposition stage using an RF bias of 300 W and a 1 kW DC power on the target. Note that no seams or voids are present in the trench area, enabling this process to be used for the Cu ECD fabrication.

After Cu deposition, the wafers are polished until the Cu film is removed from the

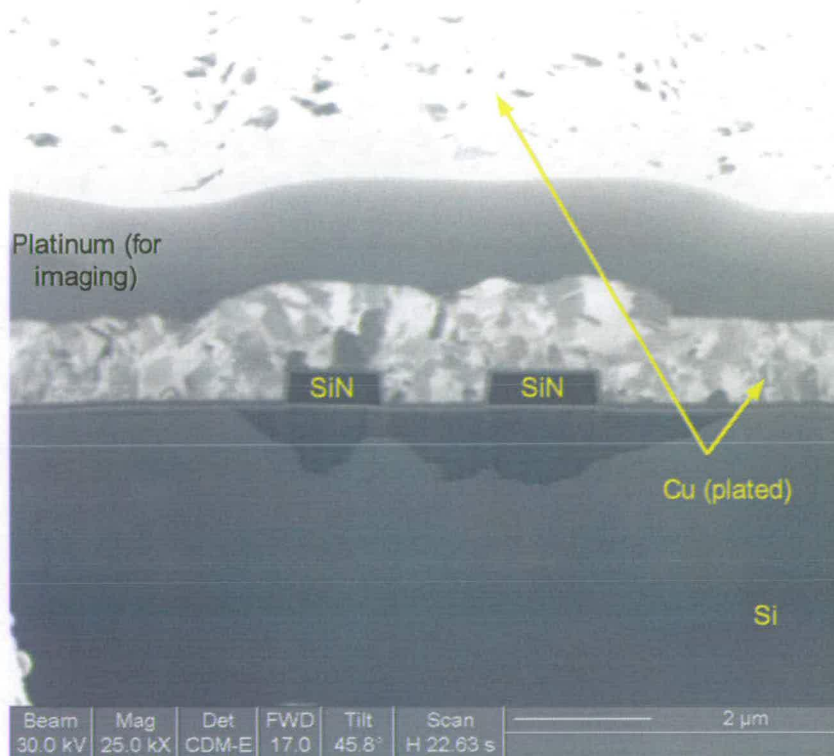


Figure 4.18: *FIB cross section of wafer with electroplated Cu film.*

field area using CMP (Fig. 4.4(j)). It is important to ensure that the finished product of this stage produces Cu tracks that are planar with the top of the trenches and do not suffer from the effects of dishing or erosion. Initial experiments utilised a slurry designed for use in damascene applications where barrier metals are employed, as typically seen in industry. This slurry (Cabot iCue-5001) is provided as a two component polishing process. The first component is used to remove the bulk of the Cu and stop on (or not polish) the barrier metal. At this point the slurry is changed and the barrier metal is polished selective to the Cu track. This combination process prevents excessive dishing of the Cu which would otherwise tend to occur in a single polish step. However, as no barrier metal is present in this implementation and hence only the first component of the slurry is used, the benefits of this product were not fully exploited. Therefore, dishing of the Cu tracks was observed at approximate 100 to 200 nm below the SiN mould surface as seen in figure 4.20.

More appropriate slurries for a single component polishing process are available from Cabot microelectronics [130] and so two newer products targeted at Cu CMP were evaluated. These slurries rely more on the process conditions during polishing to

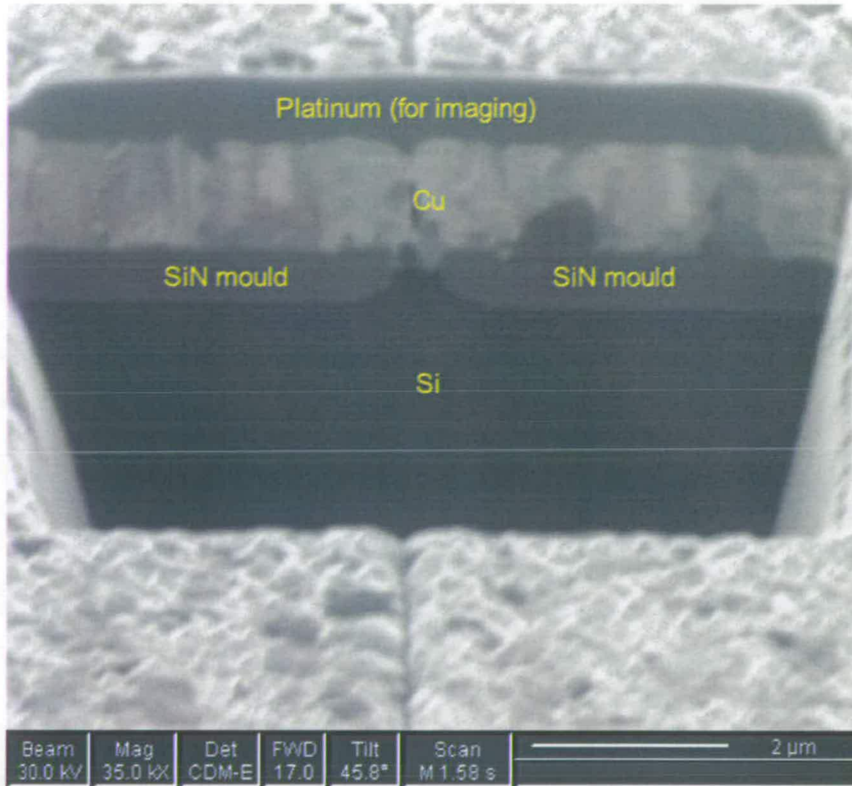


Figure 4.19: *FIB cross section demonstrating the structure after PVD Cu deposition with RF bias without voids.*

control removal rates rather than the selection of slurry chemistries. The first product was C7092 and was a concentrated single component slurry which required dilution of 2 parts DI water to 1 part C7092 prior to use. The other product was iCue 600Y75 and was similarly a single component slurry. All Cu polishing slurries used during this work require the user to agitate the slurry prior to use in order to evenly distribute the abrasive component of the mixture. During this mixing process, a small quantity (1-5 %) of hydrogen peroxide (H_2O_2) is included. This adds an oxidising component to the composite slurry that reacts with the Cu film to assist with the removal of the metal film in a controlled manner.

A direct comparison of the two slurries was carried out using the parameters recommended by Cabot Microelectronics [130] as summarised in Table 4.3. The samples used for this experiment consisted of trenches patterned in a SiN film with PVD Cu deposited on top. The structure used for comparison was a 2.5 μm track with a 5 μm track either side. Optimal conditions of use recommended a 2 step process similar to that used for the SiN polishing. The first step, *bulk process*, is used to remove

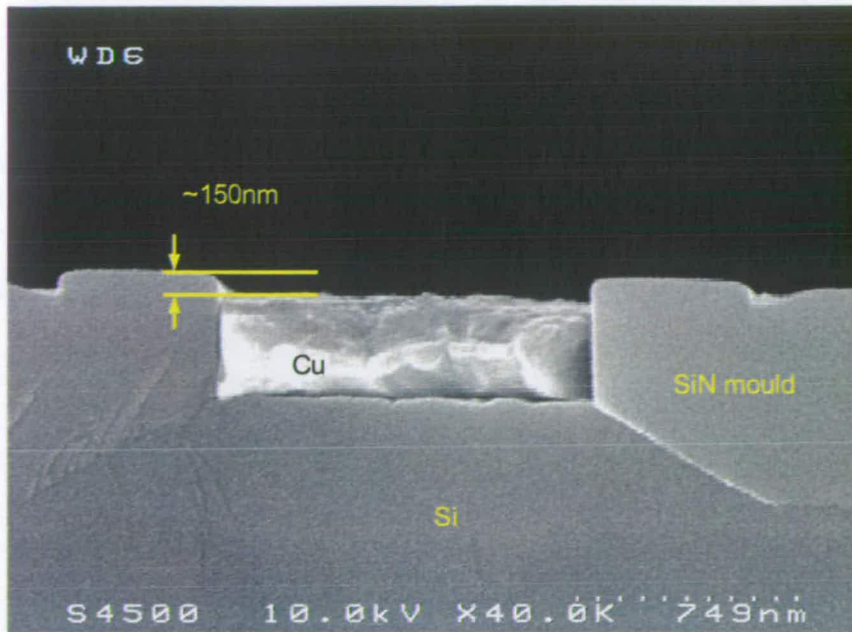


Figure 4.20: *Cross section demonstrating the structure after the Cu CMP stage using the iCue 5001 slurry.*

the bulk quantity of the Cu film and planarise the wafer's surface. When the thickness of the Cu has been reduced to about 200 nm above the field area, the *soft landing* removal step is begun. This uses a lower pressure on the wafer down force to control the point when the Cu film is removed from the field area but remains in the trench with minimal dishing.

Slurry	H_2O_2 content (%)
600Y75	3
C7092	1

Slurry	Bulk process		
	Wafer down force (psi)	Platen speed(rpm)	Slurry flow (mL min^{-1})
600Y75	3	60	75
C7092	2	60	100

Slurry	Soft landing		
	Wafer down force (psi)	Platen speed (rpm)	Slurry flow (mL min^{-1})
600Y75	1.5	60	150
C7092	1.2	60	150

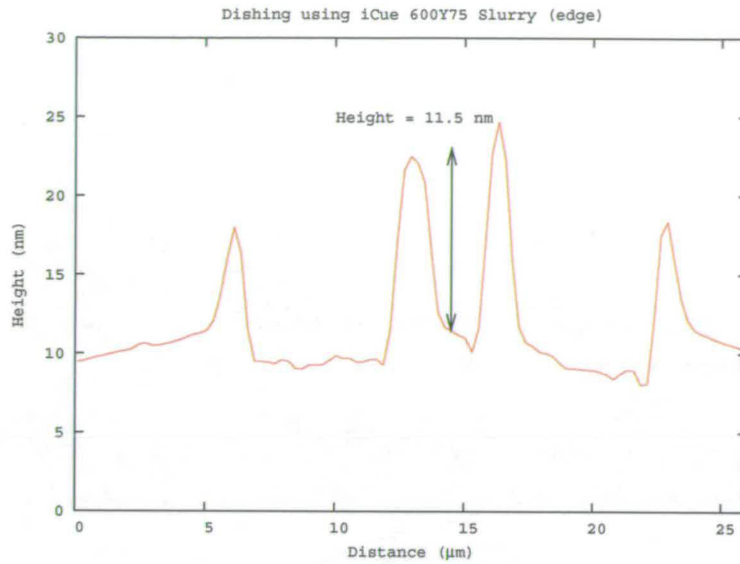
Table 4.3: *Recommended process conditions for Cu CMP trials.*

AFM measurements were used to quantify the degree of dishing and erosion of the

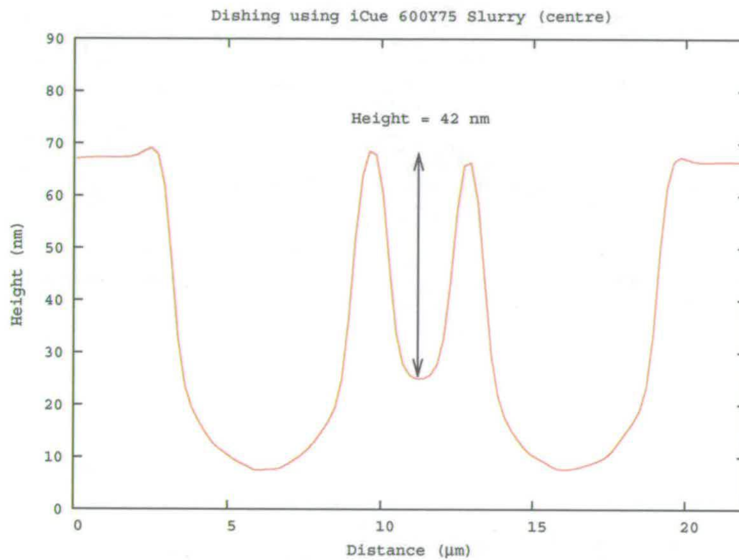
wafers as a result of the two different slurries. Analysis of these scans found that with both slurries, erosion of the dielectric was observed as denoted by the height difference between the interface at the edge of the metal track and the dielectric in the field area. However, with the iCue 600Y75 slurry, in the outer 50% of the wafer, the Cu track itself is only dished to roughly 11.5 nm as shown in figure 4.21(a). On the other hand, near to the wafer's centre, the Cu tracks experienced dishing of 42 nm (Fig. 4.21(b)). This was presumed to be due to the oxidising and chemical etch properties of the slurry. When using the C7092 slurry typical values for dishing were in the order of 9 nm as figure 4.22 shows. This value was consistently observed over the wafer with no excessive dishing observed in the scans taken. One possible explanation for the large dishing value seen in figure 4.21(b) could be the fact that the 600Y75 slurry contains 3% H_2O_2 while the C7092 has only 1%. This difference could contribute to higher oxidation and hence removal rates in areas of the wafer which do not receive high mechanical abrasion. While dishing and erosion are well understood effects of polishing, they cannot be completely removed from the process. Based on the results, the C7092 slurry was used to fabricate the Cu test structures. This reduced dishing value allows the final Cu track to possess a more rectangular cross section in comparison to that achieved with the iCue 5001 slurry that was initially used.

Finally, to prevent any oxidation of the Cu line which may occur over time, a passivation layer must be deposited over the Cu tracks to isolate them from atmospheric conditions (Fig. 4.4(j)). There are many choices for this material, however Parylene has been reported to be very compatible with Cu interconnects [131] and is also deposited at room temperature. Parylene™ is able to provide sufficient protection against the oxidation, adhesion and diffusion properties when implemented with Cu. A 50 nm thick Parylene film is blanket deposited using an LPCVD process at room temperature, and therefore will not affect the properties of the Cu line through thermal stress. To allow electrical testing this film can be selectively removed over the probe pads with appropriate photolithography steps and an oxygen or argon plasma etch.

The final fabricated structure is displayed in the FIB cross section in figure 4.23



(a) Edge of wafer



(b) Centre of wafer

Figure 4.21: *AFM profile of a 2.5 µm wide Cu line after CMP with 600Y75 slurry.*

4.5 Testing strategy

The test structure (Fig. 4.24) fabricated using the above process, has been specifically designed so that line width can be extracted using two methods. These are electrical measurements to extract resistivity and hence electrical line width and the use of HRTEM on the single crystal feature below the Cu track to determine the physical line width. The electrical measurements are designed to be taken with wafer probing

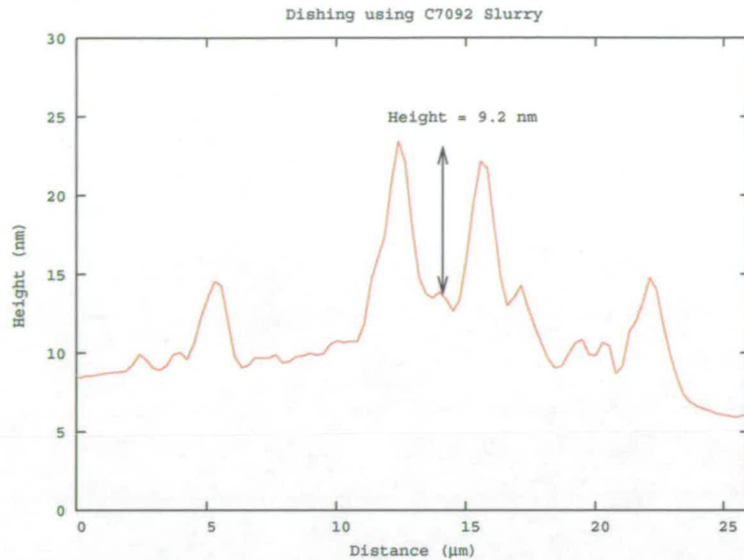


Figure 4.22: *AFM profile of 2.5 µm wide cu line after CMP with C7092 slurry.*

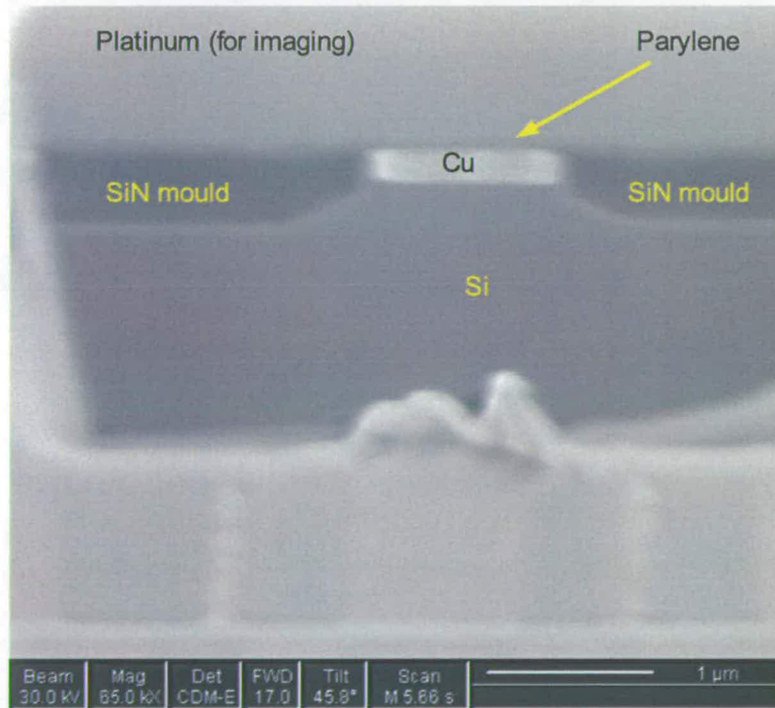


Figure 4.23: *FIB cross section of final fabricated Cu ECD test structure.*

equipment and parametric test equipment capable of sensing the resistance to the high resolution required to accurately determine the line width values. Using DC parametric extraction techniques, I-V (current and voltage) measurements can be used to determine resistance values, and with appropriate calculations the line width can be

determined. For reference measurements, the ECD feature can be placed in an HRTEM to capture an image of the crystal lattice that makes up the silicon preform remaining below the Cu track. From this image the procedure described in Chapter 2 for line width extraction from HRTEM images can be applied. This enables the electrical CD measurements to be calibrated using the HRTEM lattice plane count of the Si feature. The results from these measurements should determine the repeatability of the process as well as identify any other issues with the current design and fabrication process.

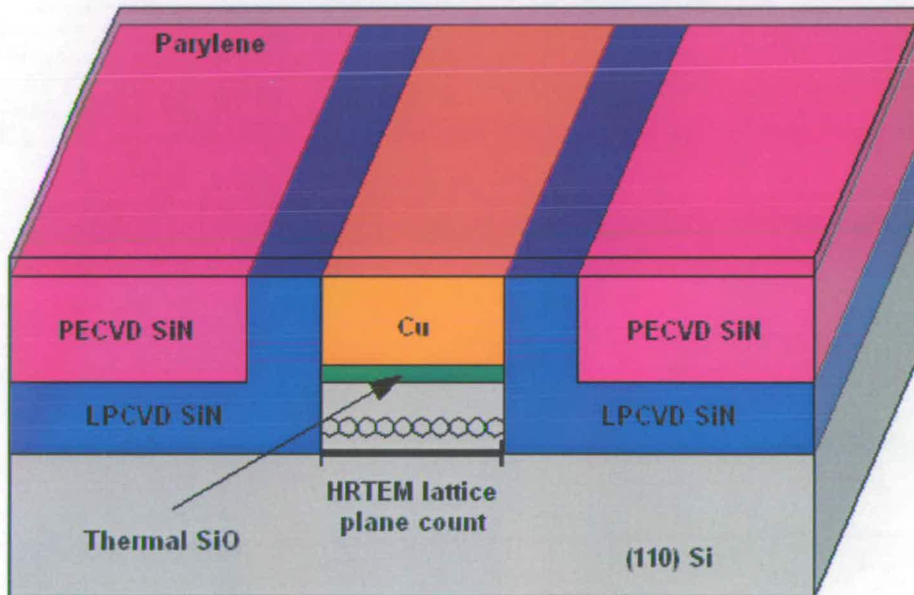


Figure 4.24: *Design of structure used for all-copper ECD reference material*

Although this structure was designed to incorporate structures for HRTEM lattice plane counts, it is by no means limited to this technique. As the structure possesses a rectangular cross section, the line width at the top of the track is consistent throughout the vertical cross section of the line allowing top down measurement of line width. Many existing metrology tools and approaches can be applied to determine the line width of the structures employed here. For example, SEM images of the top of the structure can be used to measure the line width using established techniques as described in Chapter 2. Other techniques such as AFM, optical microscopy, and SPM can also be used in the same manner.

4.6 Conclusions

This chapter has presented a process used to fabricate a test structure to serve as a Cu ECD reference material. The process described in section 4.4 is based on the combination of previously reported work on Si ECD structures with the Cu damascene process to provide a traceable structure for ECD extraction. One of the most important aspects of this work was to ensure that the fabrication steps and materials were selected such that the line width of the Cu interconnect line remains the same as that of the silicon preform remaining directly under the trench. Providing this is achieved, then electrical measurements of the Cu track can be calibrated using HRTEM line width measurements from the Si reference feature, providing a means for traceable ECD extraction. Additionally, this structure allows the extraction of line width from other tools used in interconnect metrology such as CD-SEM, AFM, etc. and can therefore be used for calibration and measurement reference.

The fabrication process defines a Si structure of which a mould is used to preserve the lateral dimensions throughout the various processing steps involved. After a portion of the Si has been removed, Cu is used to fill the trench and define the final test pattern. The final fabricated structure has been demonstrated using commercially available processing tools and materials. The success of this work can be measured by comparing the designed process flow (Fig. 4.4) with the cross section SEM images taken of the structures at various points throughout the fabrication. Although the test structure has been implemented with Cu tracks, it is suitable for use with any damascene compatible material to produce ECD reference material.

During the development of the fabrication process, the initial SiN mould was found to introduce a considerable error in the CD transfer. This was overcome by using a thicker LPCVD Si_3N_4 coupled with a PECVD low frequency Si_xN_y film. However, there is still the requirement to confirm that the dimensions of the silicon preform have been faithfully transferred to the Cu line width. In addition, more precise testing is required to determine if the proposed design does indeed maintain the CD of the silicon preform after the various processing steps. Another area that requires further characterisation is the uniformity of the etch and oxidation step at the bottom of the track and any effect of the XeF_2 etch on the width of the SiN mould. These can be achieved using a CD-AFM tool (unavailable at the time of this study) to take a 3-D

image of the trench and evaluate the rectangular nature of the trench through the process. HRTEM evaluation of the single crystal Si under the Cu track will also be invaluable in characterising the full extent of any effects of stress.

The results from preliminary work to deposit Cu into the narrow trenches employed in this study demonstrated the presence of voids (Fig. 4.15). While the use Cu electroplating produced improved fill properties in the cross section through a trench (Fig. 4.18), the uniformity of the deposited film measured across the surface of the wafer was inadequate to be used for the CMP step. The final recipe converged on a standard 1 kW PVD sputter power with a 300 W RF bias. The results of this modification produced optimal results in the ability to conformally fill a 1:1 aspect ratio trench (Fig. 4.19).

The initial CMP recipe and slurry employed for the planarisation step in the damascene process was found to introduce considerable dishing to the degree of $\sim$150 nm in the Cu lines (Fig. 4.20). To ensure that the structure approximates closely to a rectangular cross section, a modified process using a new slurry product was implemented. The results of this produced Cu lines with minimal dishing, measured at less than 10 nm (Fig. 4.22).

In conclusion, it has been demonstrated that it is possible to combine the fabrication of Si ECD structures with the Cu damascene process to produce a structure that can serve as a Cu ECD reference material.

Chapter 5
ECD Extraction from All-Copper Test Structures

5.1 Introduction

The information in this chapter provides an in-depth analysis of the extraction of Electrical Critical Dimension (ECD) values from all-copper test structures. The structures themselves have been fabricated using the novel process described in Chapter 4, which produces Cu structures that are not encapsulated by conductive metal barrier layers as seen in industry. The advantage of this implementation is that electrical measurements can be taken to evaluate the properties of the Cu lines without the complications of additional materials. The structures used in this study were fabricated with line widths comparable to those in current Integrated Circuit (IC) technologies. Furthermore, the electrical measurements provide a non-destructive and efficient method for determining CD values. This chapter evaluates the current design and compares a number of different approaches for extracting values for both line width (W) as well as sheet resistance (Rs). Electrically extracted line width values have been compared to physical line width values taken using an SEM to determine the relation between the presented algorithms.

5.2 Background

As discussed in Chapter 2, reference materials (RM) are essential in CD metrology to ensure the accuracy of extracted measurements. The concept of traceability can be extended to RM, where an electrical line width measurement from a test structure must be traceable to a physical line width in order to serve as an ECD standard. While this type of reference structure has yet to be successfully implemented in Cu, the large amount of information and experience gained through Si ECD RM analysis provides a starting point for the current work.

Work reported by Cresswell et. al. [87] describes a number of approaches taken to extract sheet resistance values from Si RM structures. The structures used in this study are fabricated from mono-crystalline (110) Si in the same way that the silicon preforms described in Chapter 4 are created. To facilitate electrical measurements, the Si is doped to make it highly conductive and the features are fabricated on SOI wafers to isolate them from the substrate. Because of the use of (110) silicon and the requirement for rectangular cross sections in the fabricated structures, the features intersect at angles determined by the crystal planes of the silicon. The angle of intersection of the <112> planes is 70.526° and, as the structure does not possess 90° rotational symmetry, sheet resistance extraction is not able to use the widely adopted approach which utilises the formula presented in equation (5.1), where the $\langle V/I \rangle$ value represents the average of eight[1] measurements taken across adjacent terminals of a Greek cross or box cross resistor.

$$Rs = \left(\frac{\pi \langle V/I \rangle}{ln2} \right) \tag{5.1}$$

Instead, Rs values are obtained from the numerical solution to the expression presented in equation (5.2), where $\langle V/I \rangle_1$ and $\langle V/I \rangle_2$ are the average measurements from both sets of the acute and obtuse angles of the cross resistor structures.

$$exp\left(\frac{-\pi \langle V/I \rangle_1}{Rs} \right) + exp\left(\frac{-\pi \langle V/I \rangle_2}{Rs} \right) = 1 \tag{5.2}$$

In addition, this work [87] describes the electrical influence of the facets which form in the acute angles of the etched silicon structures in the context of sheet resistance extraction from van der Pauw structures. Because these facets introduce a nonplanar geometry in the cross section of the structures, the extracted values for Rs do not necessarily reflect the true sheet resistance value of the material being measured. Instead these values are referred to as the *apparent sheet resistance*. To establish a more appropriate extraction algorithm, a study was conducted to evaluate the effect of the line width of the arms of the cross structures and the extracted Rs values. This lead to the conclusion that as the arm width increases, the Rs values decrease towards a presumed "true" value of sheet resistance. A further investigation found that sheet

[1] Based on one measurement from each direction (forward and reverse) of all four intersections of the arms.

resistance could be derived by comparing simulation measurements of cross structures with measured values from fabricated features. However this technique relies on the structures having a uniform resistivity and the design incorporating a range of structures possessing different arm widths from which the $\langle V/I \rangle$ values are measured.

As in the sheet resistance structures, the presence of facets in the line width structures means that standard approaches for line width extraction cannot be used. Further work by Creswell et. al. [61, 85] reports on the evaluation of a number of different algorithms to extract ECD values from Si RM. The structures employed for the silicon line width measurements are multiple-tapped Kelvin bridge resistors. The presence of facets in the intersecting angles, between the voltage taps and the bridge, effectively reduces the electrical appearance of the length of the line segment from the designed tap separation distance due to the current flow during electrical testing. The effect of the facets, along with the arbitrarily wide voltage taps, can be accounted for in the measurements using a modification to the standard Kelvin bridge formula. This line length shortening effect is characterised by the term δL [46,47,132] and is incorporated into the standard Kelvin bridge resistor formula according to equation (5.3).

$$W_m = \frac{Rs_n(L_i - \delta L)}{\langle V/I \rangle_i} \tag{5.3}$$

The value for δL can be calculated provided there are $n \geq 2$ line segments each having the same line width but different tap separation distances from the same structure. The actual procedure for calculating this value is explained in detail in section 5.3.2.2 as used for extracting parameters from Cu ECD structures.

The accuracy of the Rs values is critical to ensure that the extracted line width values reflect the physical line width of the fabricated structures when using the Kelvin bridge line width formula. An alternative method to relying on Rs extraction techniques has been reported by Allen et. al. [82] where the authors have devised a technique to extract line width values from Kelvin-tapped bridge resistor structures without using van der Pauw structures for Rs values. This was achieved by comparing the resistance values from a group of structures against the line width with which they are designed. Linear regression is then used to solve the relationship between the two values. From this comparison, the effective sheet resistance can be extracted and with this value the

line width can be calculated using the method summarised by equation 5.3.

While the above techniques allow the line width to be calculated from electrical measurements, the physical line width must be determined to establish the traceability of the measurements. A considerable amount of work has been conducted by Allen et. al. [24, 26, 27] to reference electrical line width measurements to the physical line width of the structures using HRTEM. The electrical measurements were extracted as described above, while the HRTEM measurements utilised the lattice planes in the Si as described in Chapter 2. At present, a full investigation relating electrical to HRTEM measurements is required to determine the degree of traceability between the two measurements.

The novelty of the work conducted for this chapter is the ability to use the techniques and algorithms designed for silicon ECD structures and apply them to the all-copper structures. The mask set used to pattern the chips here was originally designed for ECD structures replicated in Si substrates, known as *NIST 35* [82]. As a means for determining the traceability of this method as well as providing necessary calibration measurements, the structure reported also allows the line width to be measured using previously demonstrated techniques including: AFM, CD-SEM, optical microscopy, and HRTEM [24, 26, 133]. The aim of this study is to provide a structure and method of analysis that will further the understanding of Cu interconnects implemented both with and without metal barrier layers.

5.3 Method

Electrical measurements have been taken using standard DC parametric test techniques. An automated programmable parametric test system has been employed to provide a current source to the structures as well as controlling switching matrix operations. A precision voltmeter was also used in conjunction with the test system to provide highly accurate voltage measurements. A semi-automatic probe station with a "2×4" layout probe card is used to make electrical contact to the devices and enables the user to set the pitch and step between the test structures during a test cycle. Extracted data values were taken from the measurement system and imported into a

data analysis software package[2] to evaluate the reported algorithms.

Each test cell contains structures to determine both the sheet resistance as well as line width. These test cells are repeated in an array over the full die, as shown in figure 5.1. Furthermore the die is repeated over the full wafer, providing a large number of measurements positions for each fabricated wafer.

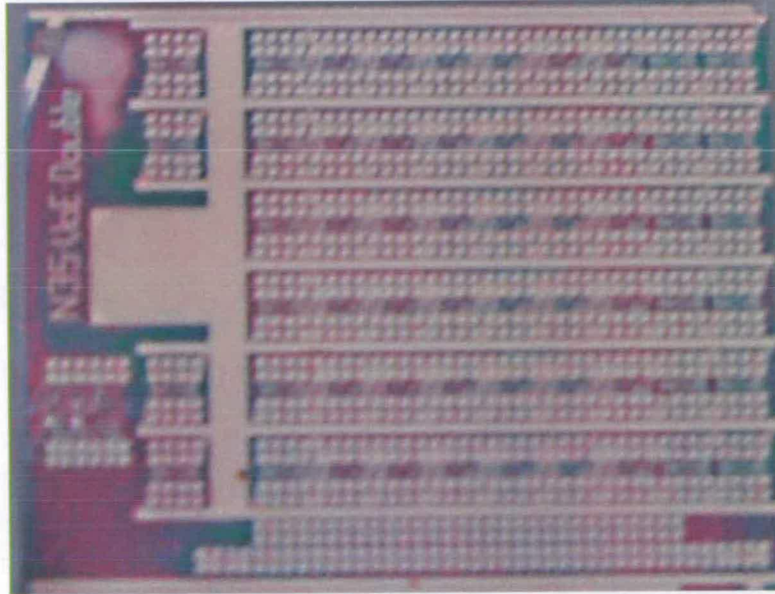


Figure 5.1: *Fabricated test chip used for Cu ECD analysis using the NIST 35 design.*

5.3.1 Sheet resistance

Sheet resistance measurements reflect the thickness and resistivity of the Cu film as well as providing a necessary parameter for traditional line width extraction methods. Current and voltage (I-V) measurements were taken from three different van der Pauw structures located within the array of test cells over the entire die. The three structures are the Greek cross, corner-tapped box cross, and side-tapped box cross as shown in figure 5.2.

With reference to figure 5.2(a) sheet resistance measurements are made as follows. First a predetermined current is forced from arm 4 to 1 and the voltage difference measured between arms 3 and 2. Similarly a current is forced in the reverse direction from 1 to 4 and the voltage between 2 and 3 measured. This provides two values which can

[2]Microsoft Excel (Office 2003)

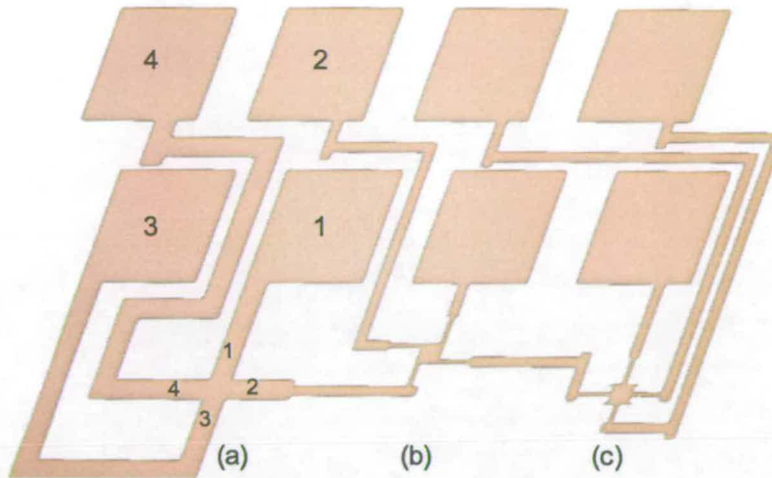


Figure 5.2: *Test structures used to extract sheet resistance for Cu interconnect features (a) Greek cross (b) corner-tapped box cross and (c) side-tapped box cross*

be averaged to determine the $\langle V/I \rangle_1$ value for the obtuse angle of the Greek cross structure. In a similar manner, the acute angle is measured by forcing current in both directions on arms 1 and 2 while measuring the voltage drops between arms 4 and 3, providing $\langle V/I \rangle_2$. The actual sheet resistance value is then calculated using the $\langle V/I \rangle$ values to solve for Rs in the generic van der Pauw equation (5.2) [134].

5.3.2 Line width

The line width test structures used for these measurements are specifically designed to eliminate the need for the strict design rule restrictions seen in standard line width cells [62]. From figure 5.3, it can be observed that the structures consist of multiple tapped bridge resistors with a range of segment lengths having a constant line width from which I-V values can be extracted. The portion of the NIST 35 design used in this study incorporates two types of design for the structures with line widths ranging from 10 μm down to 0.55 μm as detailed in Table 5.1. This design is intended for use with the short bridge technique [46] and therefore employs a constant design width of 1 μm for each voltage tap.

Three different algorithms were investigated in this study to extract line width values. The first two are based on well known and reported approaches in the literature. The last method was devised based on extensive analysis of the measured data and its correlation to the designed line width values of the structures from which it was

extracted.

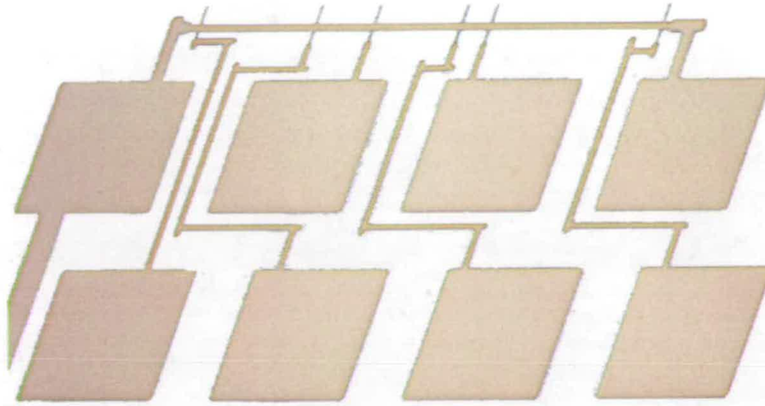


Figure 5.3: *Test structure used to extract line width for Cu interconnect features*

Bridge design parameters		
Type	Design widths (μm)	Design lengths (μm)
Standard	1.00, 0.90, 0.80, 0.70, 0.60, 0.55	8, 16, 24, 32, 48
Long	10.00, 9.00, 8.00, 7.00, 6.00, 5.00, 4.00, 3.00, 2.50, 2.00, 1.50, 1.00	24, 48, 72, 96, 144

Table 5.1: *Drawn dimensions of Kelvin-tapped bridge resistor structures*

5.3.2.1 Individual segment analysis

In this method line width is extracted using the standard formula for the Kelvin bridge resistor as defined in equation (5.4), where W_m is the measured line width, L_i and $\langle V/I \rangle_i$ are the segment length and $\langle V/I \rangle$ values for each segment respectively, and Rs_n is the representative value for the sheet resistance of the bridge resistor.

$$W_m = \frac{Rs_n L_i}{\langle V/I \rangle_i} \tag{5.4}$$

As there are multiple segments in each structure all having the same drawn line width, extracted values for W_m can be taken and averaged to reduce measurement error.

5.3.2.2 Multiple segment analysis

Another approach to extracting ECD values from the test structures is to apply linear regression techniques to solve for line width. One point to note is that the intersection of the line and voltage taps produces facets of unknown dimensions because of the nature of the photolithography and etching of the Si, similar to that described above. Figure 5.4(a) displays these facets replicated in Cu, located in both the obtuse and acute angles of the intersections of the bridge and voltage taps. Additionally, as the cross sectional image in figure 5.4(b) demonstrates, the facets are sloped and do not have vertical sidewalls as does the rest of the structure. This results in asymmetrical current flow through the vertical profile of the tap intersection. It is believed, however, that these facets are of uniform dimensions within each structure if not within each die. Based on the work presented in section 5.2 [46,47,132], the δL term can be incorporated to provide a better approximation of the Kelvin bridge line width equation. Equation (5.3) better defines the formula for determining the line width (W_m) of a given structure by including the numerical effect of the facets on the line length.

The δL term can be calculated from a single Kelvin bridge resistor provided that the test structure has $n \geq 2$ line segments each having the same line width to allow a linear relation to be established between the data points. The process starts by plotting the $\langle V/I \rangle$ values against the tap separation distances of the segments from which they were measured. Then, by applying a least squares regression fit, a linear relation can be derived between the data points as described in equation (5.5), where m is the slope of the line and b is the intercept of the line at the $L_i = 0$ axis.

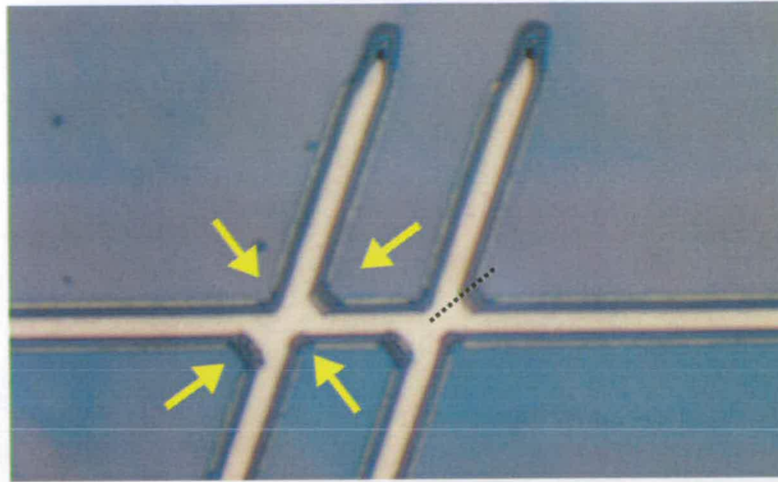
$$\langle V/I \rangle_i = mL_i + b \tag{5.5}$$

The equation described in (5.3) can be re-arranged to

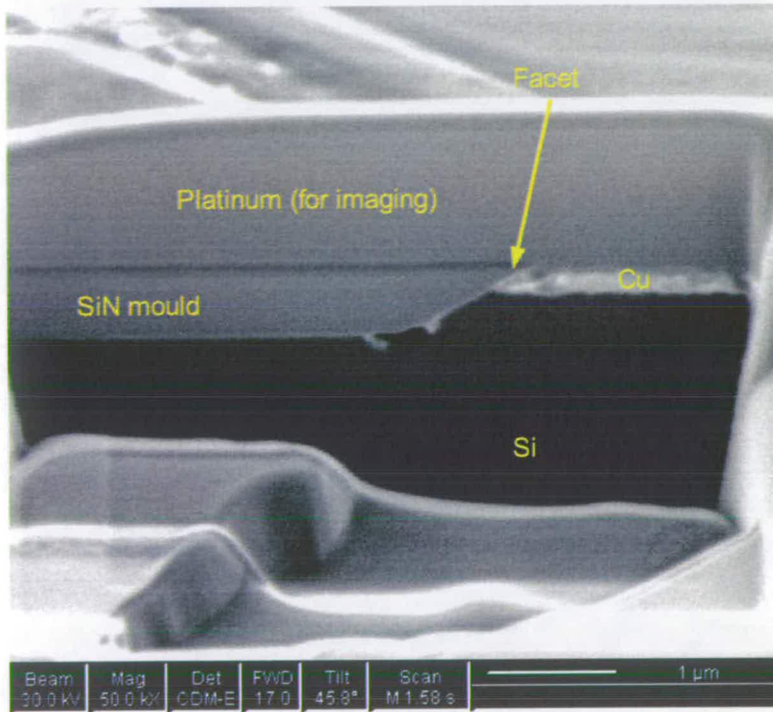
$$\langle V/I \rangle_i = \left(\frac{Rs_n}{W_m}\right) L_i + \left(\frac{Rs_n}{W_m}\right)(-\delta L) \tag{5.6}$$

Comparing equations (5.5) and (5.6) reveals that

$$slope(m) = \left(\frac{Rs_n}{W_m}\right) \tag{5.7}$$



(a) Optical micrograph



(b) FIB cross section at dashed line in (a)

Figure 5.4: *Images identifying the presence of facets in intersecting angles of Cu lines.*

and

$$intercept(b) = \left(\frac{Rs_n}{W_m}\right)(-\delta L) \tag{5.8}$$

Equation (5.7) defines the relationship between Rs and measured line width, while the δL term is found by dividing the intercept of the line relating the segments by the slope of the same line, as seen in equation (5.8). The line width can be calculated using

the slope of the line and a measured Rs value. As the line width can be calculated from the slope formula, the δL term is not directly involved in the multiple segment analysis and is more of an artifact of the structure and analysis technique. However, the line width can also be calculated as described in equation 5.3 with this value.

5.3.2.3 Multiple structure analysis

This final technique further improves upon the values based on the data gathered from the multiple segment approach. As will be seen in the results presented later, inconsistencies arise when using the van der Pauw structures to determine values for Rs. Sheet resistance is used as a measure of resistivity of thin films that have a uniform thickness. One issue with the current van der Pauw structures is due to the facets (as explained earlier) which present an asymmetrical geometry in the structure, and therefore the film in the crosses is not of uniform thickness. Furthermore, when CMP is used, process induced effects result in variations in Rs between the van der Pauw structures and the multiple tapped bridge resistors. This effect can be extended to variations in sheet resistance between the different line width structures due to Cu dishing. The structures can also experience varying degrees of cross sectional thickness along the length of the bridge as a further result of the Cu dishing. Therefore the Rs term used in equations (5.4), (5.3) and (5.7) is not necessarily truly representative of the sheet resistance of the Cu in the structure. As a consequence alternative means for determining Rs values need to be implemented.

This is achieved with a new method of analysis which overcomes the need to use Rs values from van der Pauw structures. A pre-requisite of this algorithm is that there are $n \geq 3$ structures used in the analysis to allow for a non-linear relationship to be determined from the data points. This first starts by comparing drawn line width against the slope values for each device. The drawn line widths of each measured structure are used to provide a relation between the full set of structures without accounting for any process bias that may be present in the fabricated structures. By applying non-linear regression with a least squares fit, a function described by equation (5.9) can be derived to represent the relationship between multiple structures with different drawn line widths, where m_n is the slope of a structure as determined from equation (5.5).

$$m_n = \frac{a}{(W_m)_n^k} \tag{5.9}$$

From simple data modelling it was found that the term a is primarily proportional to the sheet resistance of the measured structures and this is further supported by the similarity between equations (5.9) and (5.7). Using similar modelling and comparison of equations it can be seen that the term k is proportional to the range in measured line width $(W_m)_n$ from the result of the regression fit. A value of "1" for k results in equation (5.9) closely representing that seen in equation (5.7). With values for a and k, the line width for each structure can be calculated by substituting the slope of each line width structure into equation (5.9) and solving for $(W_m)_n$. Furthermore, with the line width value calculated using this algorithm, the Rs value can be determined by substituting for W_m in equation (5.7).

5.4 Results

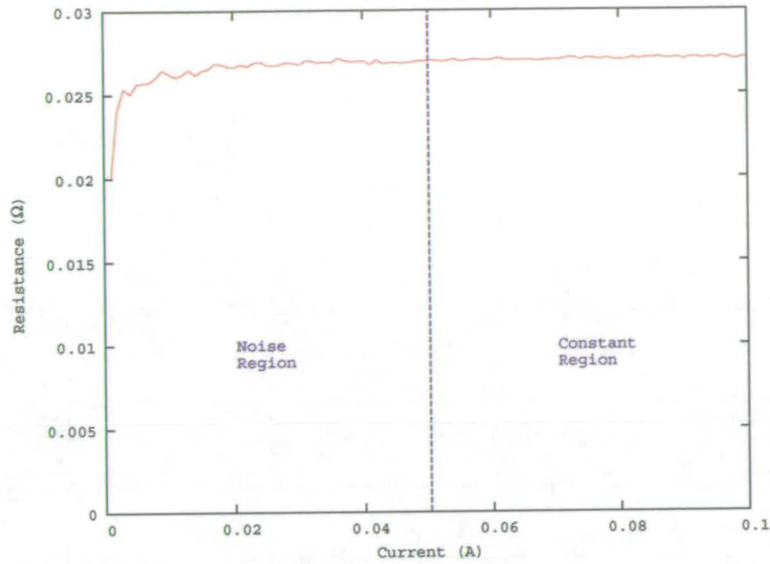
During electrical testing, parameters were chosen to maintain the linearity of the I-V variables and ensure that the measured values closely reflect the properties of the structures under investigation. The main area of caution is the impact of Joule heating, which can result in an increase of the resistivity of the film being measured [135]. To prevent the measurements from being affected by this phenomenon, an experiment was conducted to investigate this effect and determine appropriate values for the measurement setup. The goal of this experiment was to study the effects of the current on the resistance measurements. A manually operated parametric test system was used for these initial tests because of the flexibility provided to the user. The system was set up to sweep a current from 0 to 100 mA (the range of the equipment) in increments of 1 mA whilst simultaneously measuring the resulting voltage drop across the device under test (DUT). The corresponding resistance values were calculated using Ohm's Law of "$V = I \times R$". This method was applied to both the van der Pauw sheet resistance structures as well as the multiple-tapped Kelvin bridge resistors.

Results are presented for each structure by plotting resistance against the current forced, as presented in figure 5.5. For the Kelvin bridge resistor, the 0.55 μm drawn line width structure and the 48 μm bridge segment were chosen for the test as it has

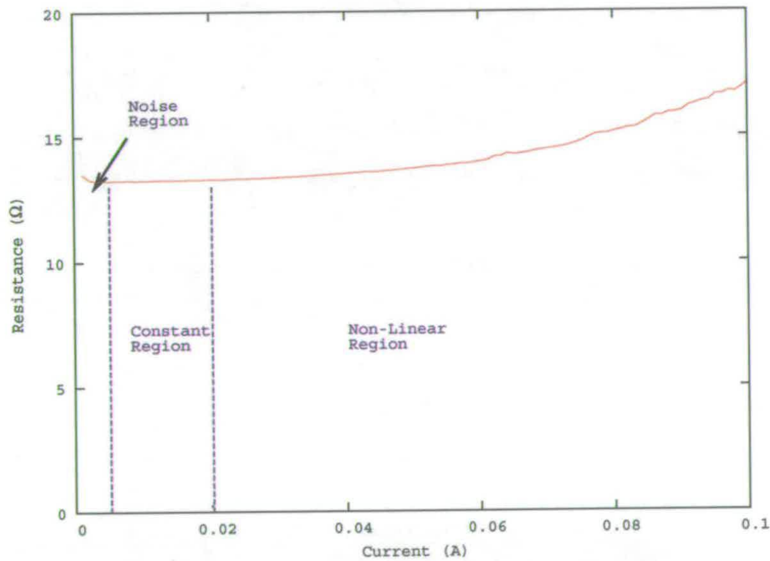
the smallest line width used in this study. This is because the small line width and long segment will have the highest resistance for a given material (in this case Cu) and therefore will demonstrate the case of highest current density over the greatest length for a constant forced current. It is this high current density which causes the Joule heating effect. Similarly, it was found that the Greek cross structure had the greatest resistance in comparison to the other two van der Pauw structures and is therefore used as the DUT.

Referring to figure 5.5(a), it can be observed that there are two distinct portions to the plotted data. Firstly, it can be observed within the identified "Noise Region" (currents less than 50 mA) that the extracted value is a function of the current. This results from the fact that the Cu has a low resistivity value and therefore exhibits a low voltage drop when low currents are forced. These lower measured voltage values are more subject to electrical interference and are near the resolution limit of the voltmeter. On the other hand, at currents above 50 mA ("Constant Region") the extracted resistance is independent of the increasing current. Based on this data, it can be concluded that a current of 100 mA safely places resistance measurements away from the "Noise Region" while not introducing a measurement offset due to Joule heating. This value was therefore chosen as the force current for the van der Pauw measurements.

Next, the data presented in figure 5.5(b) displays three distinct regions in the plot for the Kelvin bridge resistor structure. Similarly to the van der Pauw structures, there exists a region in the current sweep where the noise in the external environment impacts the extracted resistance values, marked "Noise Region". Following this, it can be observed that the "Constant Region" is rather small in this case spanning 5 to 20 mA. Beyond this, the "Non-linear Region" displays the effects of Joule heating on the structure. As mentioned above, the result of this phenomenon causes the resistance of the material to increase in proportion to the current. Furthermore it can be noted that this is a non-linear relationship between current and resistance. In order to conduct the measurement extraction without interference from either the "Noise Region" or the "Non-linear Region" a current value of 12 mA was chosen for the measurements taken in this study.



(a) Greek cross structure

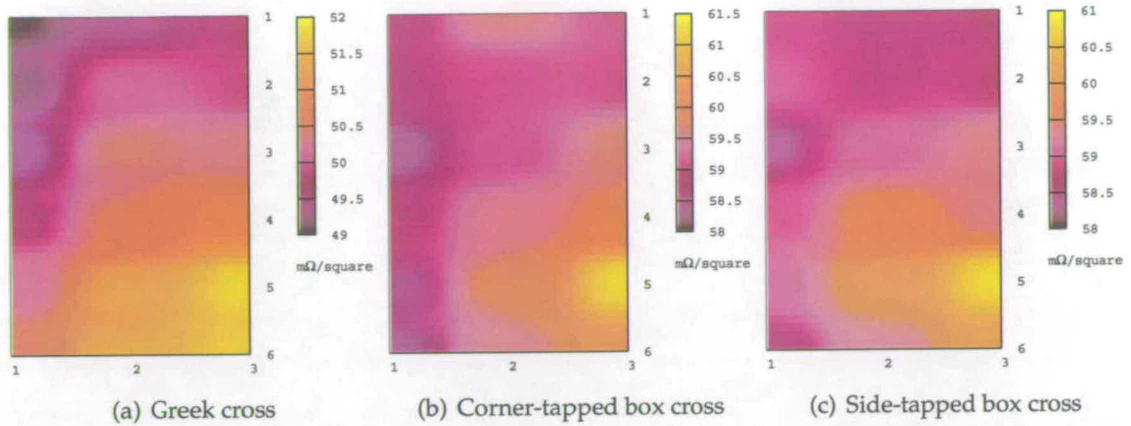


(b) 0.55 μm drawn line width kelvin bridge structure

Figure 5.5: *Results of resistance versus current measurements on electrical test structures employed in this study.*

5.4.1 Sheet resistance

I-V values have been taken from a full array of six by three structures within a single die. Sheet resistance values were then calculated using equation (5.2) based on averaged measurements from both the acute and obtuse angles on the upper and lower portions of the van der Pauw cross structures. A contour plot has then been generated



(a) Greek cross (b) Corner-tapped box cross (c) Side-tapped box cross

Figure 5.6: *Results of Rs values measured from a single die using the three van-der-Pauw structures shown in figure 5.2.*

to represent the sheet resistance over a complete die as seen in figure 5.6. These data display a similar trend in systematic variation, within a single die, for the three different types of van der Pauw structures. There are a number of process induced effects which can explain this occurrence. Firstly, CMP can result in similar systematic variations over a wafer or die due to the effects of dishing. Another possibility is the variations introduced from the trench etch stage of the fabrication process.

To fully understand the range in extracted Rs values, a comprehensive analysis was conducted on the Greek cross structure. The range in measured sheet resistance values from this structure (49 to 52 mΩ/□) translates to an equivalent thickness range from 296 nm to 314 nm[3]. This 18 nm range in thickness could easily be the result of CMP dishing variation over the die. AFM scans were taken of the Greek cross in cell {1,3} and compared to another scan taken from cell {6,3}. The Rs values for these die vary by 1.9 mΩ/□, which has the equivalent thickness variation of approximately 12 nm. Profiles extracted from the AFM scans approximately agree with these predictions by demonstrating a difference in dishing value between the two structures of 18 nm. The deviation in equivalent thickness difference and measured thickness difference can be attributed to factors such as accuracy of measurement equipment as well as the true bulk resistivity value of the deposited and patterned Cu feature, which can vary from the nominal value reported in the literature.

[3]The values reported here, and elsewhere, for equivalent thickness are based on the assumption that the Cu has a bulk resistivity of 1.539 $10^{-8}\Omega m$ [105]

One important factor to note is that the mask set used to define these structures was intended for use on doped SOI structures which would not have undergone a CMP step and would therefore be more likely to have a uniform distribution of sheet resistance over a single die and structure. For this reason, the NIST 35 design includes large (20 μm) crosses/boxes on each of the van der Pauw structures to allow for more accurate measurements of sheet resistance. However these large features pose a problem for the Cu CMP stage as larger line widths are known to dish to a greater extent than smaller line widths [78]. This leads to the need to use smaller dimensions to reduce the dishing of the Cu and provide more appropriate measurements of sheet resistance with minimal variation.

From the contour plots of sheet resistance it can be noted that, while there is a general agreement in the sheet resistance variation over the whole die, there is no specific agreed value between the three van der Pauw structures for each location. The values obtained for Rs from the Greek cross test structures are consistently lower than the other two structures. This is made apparent by an average Rs of 50 m$\Omega/\square$ (implying a Cu thickness of 336 nm) for the Greek Cross, while the values for the corner-tapped and side-tapped box average at 59 m$\Omega/\square$ (implying a Cu thickness of 284 nm). This suggests that the thickness varies between the Greek cross and the other two structures by roughly 50 nm.

The one observation that can be made by comparing the physical layout of these three structures is that the Greek cross employs larger arms to make contact with the central cross/box area. This is supported in the design with the greek cross having 20 μm arms while the two box cross structures have 5 μm arm widths. To determine whether this Rs difference is the result of dishing variations during the Cu CMP stage, AFM scans were taken of all three van der Pauw structures within a single cell. Results of the AFM measurement demonstrate that while there is a slight variation in the degree of dishing (roughly 5 nm difference between the three structures within a single cell), this does not account for the 50 nm equivalent thickness variation observed in the electrical measurements.

The next possible explanation for the Rs difference is that the trench etch stage could have produced varying depths between the Greek cross and the box cross structures, which in turn denotes the final Cu thickness in the trenches, given that the dishing

does not differ much. To test this theory, the Cu was etched from the trench and the AFM used to measure the height profile of each resulting trench. By subtracting the dishing value from the trench depth, the true Cu thickness that was in the trench can be determined. Results from this test show that the Greek cross structure had a Cu thickness of 350 nm while the other box structures had a thickness of 290 nm. This 60 nm difference is due to the trench depth variation between the Greek cross and box cross structures and can account for the range in extracted Rs values between the cross structures. The exact cause for this depth variation is currently unknown, but believed to be related to the larger open area of the Greek cross structure and its effect on the trench etch stage of the fabrication process.

5.4.2 Line width

$\langle V/I \rangle$ values have been measured electrically from the same six by three array as the sheet resistance measurements to fully assess the current design on Cu ECD extraction. Results are presented for each of the analysis approaches described in section 5.3.2. As a means for comparison, SEM images have been taken to extract a value for the physical line width of the structure, which in this case is defined by the width of the track on the surface of the wafer. While the SEM measurement equipment used in this study does not produce results to the degree of accuracy required for CD metrology, it does provide a baseline for comparing the analysis methods. Each line scan from the SEM was taken at the midpoint of the longest bridge segment of each structure (the 144 µm segment for the long design and the 48 µm segment for the standard design). For situations where Rs measurements were required to calculate line width, the average of the values taken from the two box cross variations of the van der Pauw structures for each location on the array were used. This is because AFM scans reveal that the box cross structures more closely match the trench depth of the line width structures compared to the Greek cross structure. Data from each analysis method is presented as a graph of drawn line width minus the extracted line width versus the drawn line width. This applies to both ECD values as well as SEM line width values.

To quantify the degree in which the ECD values agree with the SEM line width values, the sum of the absolute difference between SEM and ECD for each drawn line width data set has been calculated. This value will be referred to as the *agreement factor*. The

ideal instance where the line widths extracted from both methods agree exactly for all drawn line widths would result in an agreement factor of '0'.

5.4.2.1 Individual segment analysis

The individual segment analysis was conducted as described previously. A plot of the results gathered from the average of five segments of the bridge resistor for the array of 18 structures is presented in figure 5.7. The error bars on the individual data points represent the range of line widths extracted from each segment of the multiple-tapped bridge resistor. It can be observed that these errors are proportional to the line width so, as the line width decreases, the range in extracted values also decrease. The agreement factor for this method was calculated at 5.53. This is justified by the separation between the plotted data sets, especially in the central region of the graph.

One source for the difference between the ECD values and the SEM measurements is the use of the sheet resistance structures that are physically separate from the line width structures and are therefore subject to dishing effects caused by physical location differences. Furthermore, the van der Pauw structures are 20 μm wide while the line width structures range from 10 μm to 0.55 μm. This introduces further effects of dishing during CMP which are related to feature size. For example, typical dishing values for the 20 μm wide box crosses are in the order of 50 nm while the 1 μm line has a value of roughly 5 nm based on AFM scans. This difference in dishing results in varying sheet resistance values between the two types of structures and hence introduces uncertainty in the extracted ECD values.

5.4.2.2 Multiple segment analysis

Using the linear regression technique, slope values (m) were determined for each line width structure. By using the average measured Rs value from the van der Pauw structures in closest proximity, the line width was calculated using equation (5.7). A plot of the results, using this method, for all 18 structures is presented in figure 5.8. These values unfortunately do not provide better agreement with the SEM values in comparison to those derived using the individual segment analysis. This is supported by an agreement factor for this approach of 5.80.

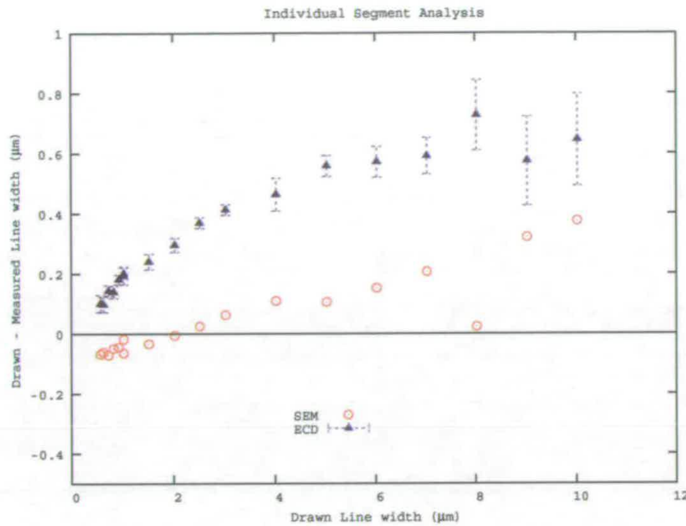


Figure 5.7: *Results for the individual segment analysis*

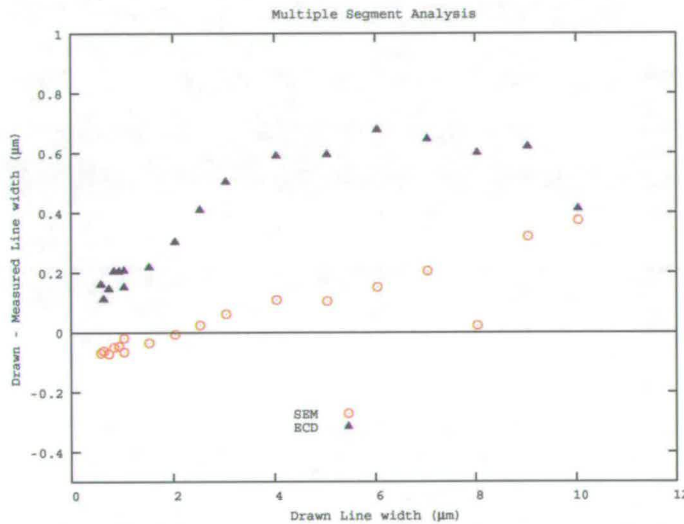


Figure 5.8: *Results for the multiple segment analysis*

Repeating the individual segment analysis with the δL correction makes no improvement in the present set of data, as can be seen in figure 5.9. In fact, with an agreement factor of 5.93, this analysis method produces much poorer agreement than the individual segment analysis. As in figure 5.7, the error bars represent the range in extracted line width values for each segment.

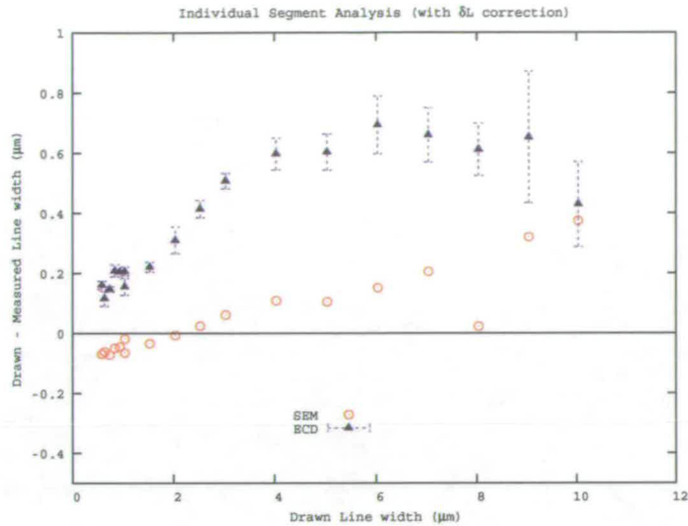


Figure 5.9: *Results for the individual segment analysis with δL correction factor included*

5.4.2.3 Multiple structure analysis

Equation (5.9) was applied to determine the relationship between the slopes and drawn line widths of the structures in the six by three array. The first approach for this technique was to analyse each column individually and plot the results. From figure 5.10 it can be seen that the values extracted for ECD measurements are in better agreement with the drawn line width values. An agreement factor of 1.78 further suggests the improvement in values using this method.

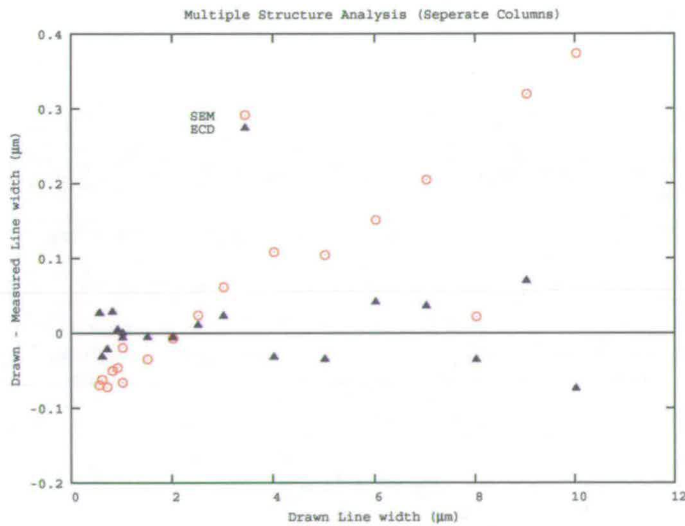


Figure 5.10: *Results for the multiple structure analysis of separate columns*

The second approach used data from the entire array to determine the non-linear relationship and hence can be used as a smoothing for any abnormalities in individual structures. Results from this method are presented in figure 5.11. Once again these data are in agreement with the drawn line widths, with an agreement factor of 1.79. From figure 5.11 it can be observed that the closest agreement between SEM and ECD values is for drawn line widths ranging from 4 to 1 μm. These values correspond to the column of structures that are physically located in the centre of the array of the test cell.

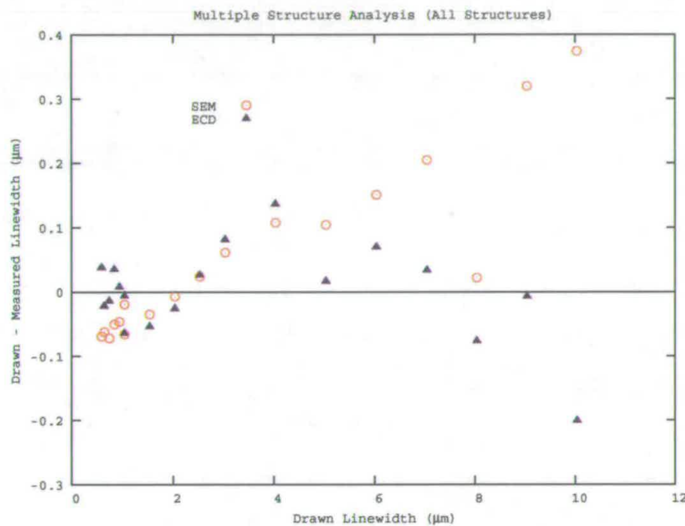


Figure 5.11: *Results for the multiple structure analysis with all structures*

To better understand this observation, an investigation was conducted to measure the trench depth of the tracks in which the Cu was deposited. A number of the Kelvin bridge structures were selected and measured with the use of the AFM. The results highlighted the fact that the depth of the etched trench was dependant on the line width of the initial silicon preform, where wider line widths result in deeper trenches. These deeper trenches translate to lower sheet resistance when filled with the Cu interconnect. This explains why using all the columns in the multiple structure analysis provides the set of results which best agrees with the SEM measured data. Column 2 (central column) contains structures which possess line widths in the middle of the measured range. Column 1 contains line widths greater than the central column, and column 3 contains those structures with line widths less than column 2. Furthermore, the rows are arranged such that the drawn line widths of the structures decreases from top to bottom (row 1 to 6). As the multiple structure analysis

method effectively calculates the sheet resistance value based on the relationship of the measured slope (m) values for the full set of structures the most accurate values for Rs will be found in the centre of the measured range due to the influence of the extreme data points. Therefore it can be deduced that the outer columns (1 and 3) provide an averaging effect which results in the central column (column 2) having the extracted line widths which most agree with the SEM values.

To understand the effect of line width on the Rs values as represented by the multiple structure analysis as well as providing a means for comparison to Rs values which were extracted from the van der Pauw structures, the equivalent Rs values for the full array of structures were calculated. This is achieved by substituting the measured ECD values, from this last analysis approach, into equation (5.7). The results are presented in a contour plot shown in figure 5.12. This data suggests a smoother gradient in the sheet resistance across the die, which supports the earlier conclusion that the line width directly affects the trench depth of the structures. For reference, the design line width of the structure in cell {1,1} is 10 μm while cell {3,6} is 0.55 μm with a sequential gradient in the cells in between. Observing this contour plot it is noted that as line width decreases the trench depth decreases, which translates to an increasing sheet resistance of the Cu occupying the track.

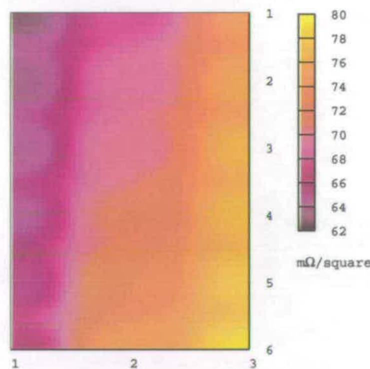


Figure 5.12: *Results of equivalent Rs values extracted using the multiple structure analysis.*

5.5 Conclusions

Electrical measurements have been taken to evaluate the design and process used to fabricate all-copper ECD reference structures. The novel process, described in

Chapter 4, allows electrical measurements to be compared to a number of previously demonstrated CD measurement techniques. Based on data gathered from extensive analyses of electrical measurements from the Cu interconnect features, issues with the current design as well as the fabrication process have been highlighted. To extract values for sheet resistance from all-copper features, a test chip comprising of an array patterned van der Pauw cross resistors was used. Three designs of van der Pauw cross resistors implemented were the Greek cross, corner-tapped box cross and the side-tapped box cross. Similarly, line width extraction is provided with Kelvin-tapped bridge resistor structures in the same array along side the van der Pauw structures.

Sheet resistance measurements were extracted from the three variations of van der Pauw cross structures to provide information over the full die. When observing the extracted data in figure 5.6, the inconsistency in trench depth between the Greek cross structure and the two variations of box cross structure was highlighted from the consistent difference in Rs values. This was supported by a physical analysis (using an AFM) of the van der Pauw structures to determine the geometry of the trench with the Cu metal removed. Furthermore, using similar comparison between electrical measurements and AFM analysis, the systematic variation in Rs values over the die was correlated with the dishing of the Cu tracks.

The Kelvin-bridge resistor structures were measured electrically and analysed with three distinct algorithms. The first two methods benchmarked previously reported techniques for extracting line width which are heavily based on the need to accurately measure the sheet resistance of the structures prior to analysis. A comparison between the ECD values, from these two methods, and SEM line width values (Figs. 5.7 and 5.8) produced an agreement factor of just under 6. Measuring the difference in dishing values between the van der Pauw and Kelvin-bridge resistors explains the difference in measured data. This is in accordance with the information presented in Chapter 2, where the accuracy of line width measurements is heavily reliant on accurate Rs values.

The third algorithm was developed during the work conducted for this chapter to extract line width without the need for Rs measurements. It is conducted by combining work presented in the multiple structure analysis to extract slope (m) values for each structure with non-linear regression techniques. The results (Fig. 5.11)

from this technique were in much better agreement with SEM measurements as demonstrated by an agreement factor of just under 1.8. Furthermore, by using the extracted line width values to calculate the effective sheet resistance of the Kelvin-bridge structures (Fig. 5.12) a dependence of trench depth on the line width of the structures was highlighted.

In conclusion, the information found in this chapter was used to successfully characterise and highlight processing issues in the test structures employed. Furthermore, the analysis methods from this chapter will allow the quantification of future improvements to the processing of the test structures.

Chapter 6
MEMS Test Structure Evaluation

6.1 Introduction

This chapter investigates the use of test structures to evaluate thick film metals in MEMS processing as commonly implemented for power devices on Si substrates. Emphasis is placed on the capabilities of traditional test structures, used in the interconnect metrology field, when replicated in large dimension Cu wires. The two test structures evaluated are the Greek cross and the Kelvin-tapped bridge resistor. This study will benefit the MEMS community by providing information on the use of electrical test structures in process monitoring and material characterisation of thick film devices. Furthermore, it will assist in developing extraction methods and highlighting any potential issues associated with their use. This study was conducted in collaboration with National Semiconductor Corporation to develop a process, based on the combination of thick film[1] photoresist and electroplating technologies, for the characterisation of power MEMS devices. After the fabrication of the structures is presented, an analysis of electrical measurements taken from the structures to extract values for sheet resistance as well as line width is described.

6.2 Background

The introduction of MicroElectroMechanical Systems (MEMS) sparked a revolution in IC fabrication. This concept allows the combination of existing CMOS technology with electronics, sensors, and many other devices that were previously incorporated off-chip as a separate component on a printed circuit board (PCB), onto the silicon chip. The origin of MEMS devices can be traced back to 1954, when it was discovered that a germanium and silicon structure possessed piezoresistive effects that could be used to produce strain gauges [136,137]. Since that date a considerable amount of work has

[1]The term *thick film* in this context refers to layers in excess of 10 μm in thickness.

been conducted to develop IC strain gauges, with the first high volume pressure sensor being marketed by National Semiconductor Corporation in 1974. However, it wasn't until 1987, during a series of workshops on microdynamics, that the term "MEMS" was coined [138].

The applications of MEMS in the IC industry are currently very extensive with continuing possibilities for the future. Some examples of MEMS technologies include:

- Pressure sensors [139]
- Accelerometers [140, 141]
- Power devices [142]
- 3D packaging [143, 144]
- Bioelectronics [145]
- Optical displays [146]

The benefits of integrating MEMS devices with IC chips include reducing effects such as noise and power loss when compared to traditional layouts in which the control circuitry and sensors would be located on separate portions of the PCB. This is because the wires and terminals used to connect the devices together are prone to these effects and placing the components either directly on top of [147] or alongside [148] the IC greatly reduces the effective wire length and hence the possible influence of noise and power loss.

The one specific area of MEMS devices concentrated on in this work is the implementation of power devices using MEMS fabrication techniques. The appliances that employ this type of technology require that the integrated MEMS and CMOS devices be compatible with the high demands for power during operation. To cope with the large currents involved, the MEMS device must incorporate low resistance, large dimension conducting wires. There are two technologies currently available (that are often combined) to accommodate this requirement. The first is thick film photoresist to define the pattern for the wires and the other is electroplating to deposit the interconnect metal in the quantity required to act as the conducting material in the large dimension tracks.

6.2.1 Thick film photoresist

There are a number of commercial products currently available that provide photoresist films with thicknesses ranging from 1 to 100s of µm. The majority of these thick film photoresist are of the negative imaging variety, in that the imaged pattern possesses the reverse image of the photomask used during photolithography. Two main types of thick film photoresist exist depending on the application and requirements. The first is those that are used for applications such as etching and electroplating moulds. In this case the resist forms a sacrificial structure that is designed to be removed after the processing has been completed [149]. The other type is epoxy-based photoresist and as a result is difficult to remove without additional process steps included either prior to or after processing. As a result these resists are well suited to forming part of the physical structure and remain in place for the life of the device. The most commonly used variant of the epoxy- based resists is SU8, originally developed by IBM [150]. For the purposes of this study, a commercially available resist film has been used to define a mould for electroplating which can then be removed to leave a free standing structure.

The patterning of these thick resists was first developed using X-RAY lithography for LIGA[2] processes [151]. However because of the operating cost involved in such a tool, it is not a viable choice for commercial fabrication environments. Significant research and development has led the microsystems field towards the use of traditional ultra-violet (UV) lithography techniques to pattern these resists, with the introduction of the UV-LIGA process [152]. These resists are coated to thicknesses upwards of an order or two of magnitude greater than the thin film resists used in standard CMOS type applications, and it might be expected that the exposure doses would also be proportionally greater. However, in an effort to reduce the time required for the patterning process, a number of key properties have been introduced and modified to allow shorter exposure times for a given exposure intensity. The first is to decrease the absorption coefficient of the resist and therefore allow an even distribution of the light source through the vertical profile of the imaged structures [153]. The second is to select the chemistry of the resist such that it possesses a chemically amplified (CA)

[2]German acronym Lithographie Galvanformung und Abformung for Lithography, Electroplating and Molding. This refers to the process in which a photoresist is lithographically patterned, electroplating is conducted in the resist pattern and the resist is removed to yield the electroplated structures.

nature. This property increases the sensitivity of the resist to the radiation source (in this case UV radiation) used in the lithography process by creating a photo generated catalyst [154].

6.2.2 Electroplating

The use of electrochemical deposition (electroplating) of metals is one of the most common techniques employed in the metallization coating industry. Electroplating first appeared in mainstream IC fabrication when Cu interconnects and the damascene process were introduced [155] and soon became the viable option for filling narrow trenches with optimal fill performance [156]. Extensive work has since been conducted into the use of electroplating in semiconductor devices and an entire industry was evolved around this. The electrodeposition of metals is one of the key enabling technologies for the production of microsystems and MEMS devices because of the low cost advantages over more traditional methods such as PVD sputtering or evaporation [157].

Electrodeposition is the reduction of an electrolyte, containing metal ions, to form a solid metal layer on the surface of a conductive electrode. Figure 6.1 displays a schematic view of the most important components of a typical setup used for electroplating of silicon wafers in the semiconductor industry. The electrolyte (also referred to as the *plating bath*) is a solution containing the salt compound of the metal being plated along with supporting acids or salts and additives to assist with the deposition of the metal. In electroplating of Si wafers, the surface of the wafer contains a conductive film to serve as the electrode. Typically the wafer is coated with a metallic seed layer using PVD sputtering, or similar techniques. This seed layer also serves as a material for the nucleation and growth of the metal as described in [158–161]. The counter electrode, or anode, consists of either an insoluble metal, such as platinum, or of a soluble metal similar to the material being deposited. When a soluble anode is employed, it allows the depleted metal ions from the bath to be replaced by the dissolution of the anode material hence avoiding the need to add chemicals or salts to maintain the ion content. The deposition of the metal is primarily controlled using either a constant current or voltage source connected to both electrodes (wafer and anode). In addition to these key components of a plating system are other periphery

elements to provide agitation, re-circulation, filtration, heating/cooling, electrical connections, etc.

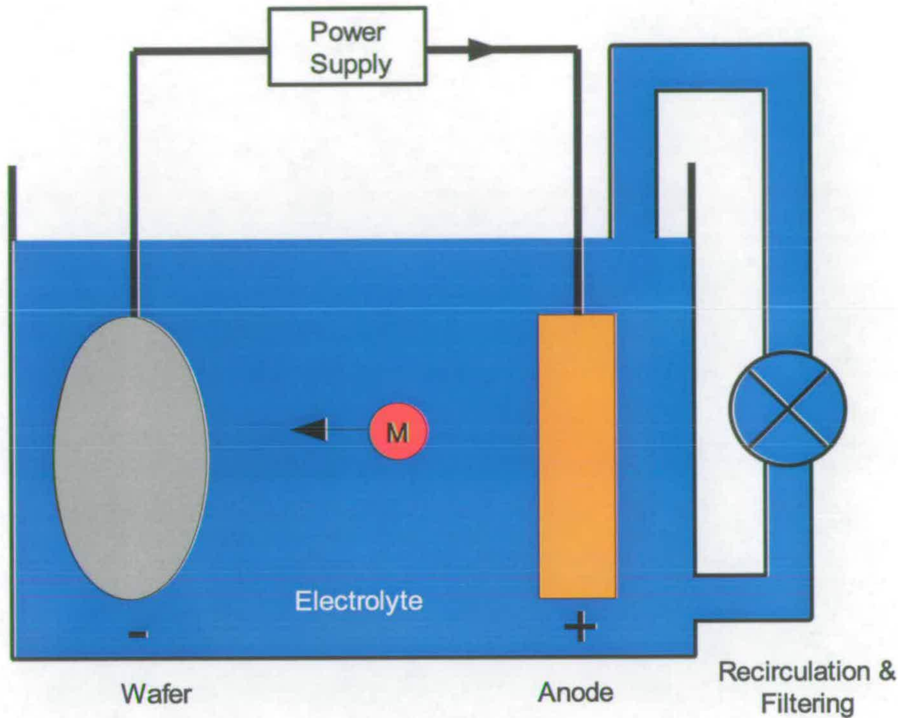


Figure 6.1: *Typical setup employed in the electrochemical deposition of metals on semiconductor wafers.*

During electrodeposition, metal ions travel from the positive anode, through the electrolyte solution to the cathode (or wafer). This results in the deposition of the solid form of the metal onto the wafer surface. While this description provides a basic understanding of the electroplating phenomenon, the actual electrochemical reactions involved in metal deposition can be quite complex. A more detailed description of the fundamentals of electrochemical deposition is provided by Paunovic and Schlesinger [162].

The ability to plate different materials to specific requirements depends on a number of parameters available to the user. First is the choice of the tool and hardware parameters used in the plating process [163]. This includes agitation of the electrolyte solution, temperature of the plating bath, electrical waveform used, current value supplied, etc. The other is the selection of chemistry, of which there exists a number of proprietary solutions tailored for semiconductor manufacturing requirements. These can be further customised with the use of the various additives that exist from vendors

to alter the plating properties and permit deposition in structures that would otherwise not be as possible with a basic electrolyte [156,164].

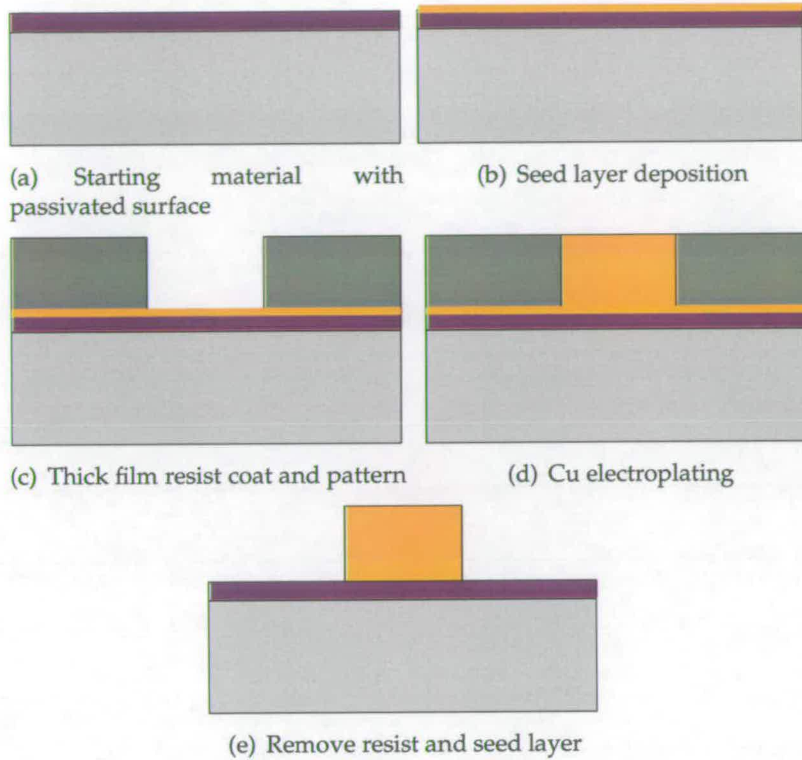
6.3 Fabrication process

The process employed in this study uses a mould based approach to produce patterned Cu wires similar to that used in a LIGA process. An overview of the steps used is presented in figure 6.2. The starting material consists of Si wafers coated with a passivation layer to electrically isolate the Cu lines from the substrate (Fig. 6.2(a)). A seed layer is first deposited on the wafer to provide a conductive film for the Cu metal to grow from during electroplating (Fig. 6.2(b)). The pattern for the Cu wire is then defined with thick film photoresist (Fig. 6.2(c)). After this, Cu electroplating fills the patterned trenches growing from the bottom to the top and forms the wires for the circuit (Fig. 6.2(d)). Finally the photoresist is stripped from the wafer along with the seed layer to leave the isolated Cu tracks freestanding and ready for electrical testing (Fig 6.2(e)).

The fabrication of these devices was conducted using a dedicated MEMS processing area for thick film resist and electroplating. The techniques and methods employed for these structures are based on those used in traditional semiconductor/MEMS manufacturing environments. A detailed list of the process steps used for the fabrication of these devices is presented in the run sheet in Appendix C.3.

6.3.1 Substrate preparation

The substrates used for processing were 8 inch wafers coated with a PECVD Si_xN_y passivation layer for electrical isolation. A three layer blanket metal seed was deposited using PVD sputtering across the entire surface of the wafers. This consisted of a 30 nm layer of titanium (Ti) to serve as an adhesion layer between the Cu seed and the substrate. After this a 300 nm layer of Cu is used to carry the current across the wafer from the edge (where the power supply is connected) to the remaining area of the wafer (where the structures are located) and provides the material from which the electroplated Cu will grow. Finally a further 30 nm of Ti is used as an anti-reflection coating and adhesion promoter for the photolithography used in this



(a) Starting material with passivated surface

(b) Seed layer deposition

(c) Thick film resist coat and pattern

(d) Cu electroplating

(e) Remove resist and seed layer

Figure 6.2: *Overview of MEMS mould process to form Cu conductor*

process. It was found that without this additional Ti layer the patterned resist mould delaminated at the edges and the sidewall profile was difficult to optimise to achieve vertical sidewalls.

6.3.2 Mould patterning

The mould process used for this study requires a thick film, removable photoresist capable of high aspect ratio patterning. The photoresist made available for this purpose was Futurrex NR2 20000P. There is little published information in the literature relating to this resist. Hence, the majority of the process related data was gathered from the manufacturer's data sheet provided and augmented with a number of preliminary experiments. NR2 is a negative photoresist designed for thick film applications and is patterned using traditional UV exposure tools. The advantages of using this product are that the patterning process is similar to standard resist processing and does not require additional hardware or tools. Furthermore, the photoresist pattern can be developed with an aqueous based developer which is

readily available and easily integrated into the dedicated equipment for this process. All of the photolithography was conducted on a mask aligner with the capability to operate in proximity, soft contact, hard contact, and vacuum contact printing modes.

Based on experience gained from preliminary experiments conducted in the early stages of this study, it was found that the processed film properties did not correlate with those reported on the NR2 data sheet. For this reason, a thorough investigation was conducted to establish a recipe starting from the best known method as provided by the data sheet. The first parameter to establish was the film thickness as determined by the coating parameters by plotting spin curves that relate the spin parameters of the coating system with the photoresist thickness. The results of this first experiment, displayed in figure 6.3, are based on an average of measurements taken from a number of wafers at each experimental value. Photoresist is dispensed manually into a puddle in the centre of the wafer and the quantity was kept as close to 8 ml as possible. After this static dispense, the spin chamber was sealed and the wafer spun as per the acceleration, time, and final spin speed denoted in figure 6.3

The first spin coat recipe used a 10 second total spin time with a 3000 revolutions per minute (rpm) per second acceleration to closely match the recommended recipe on the data sheet. When trying to repeat these values at a later date, it was found that this initial recipe was not stable enough and provided values which ranged from the initial spin curve experiments. It was decided that the short duration of the spin recipe could be the root cause for this. Furthermore, as the NR2 is such a viscous film, any misalignment of the dispensed puddle with respect to the central axis of the spin coater results in an uneven weight distribution and, in some cases, causes the wafer to loose contact with the vacuum wafer chuck during the acceleration. As a result the acceleration of the spin recipe was reduced to 1000 rpm per second to allow the resist to spread more evenly across the wafer surface before reaching the final spin speed, therefore reducing the likelihood that an uneven load would be present during high speed rotation. The modified recipe used a 30 second duration to allow the thickness to stabilise more during the spin coating with the results presented in figure 6.3 alongside the previous set of data. This new recipe provided higher repeatability in the thickness of the resist films and was adopted for the fabrication of the test structures. The reported values on the data sheet are plotted alongside the experimental values for

comparison.

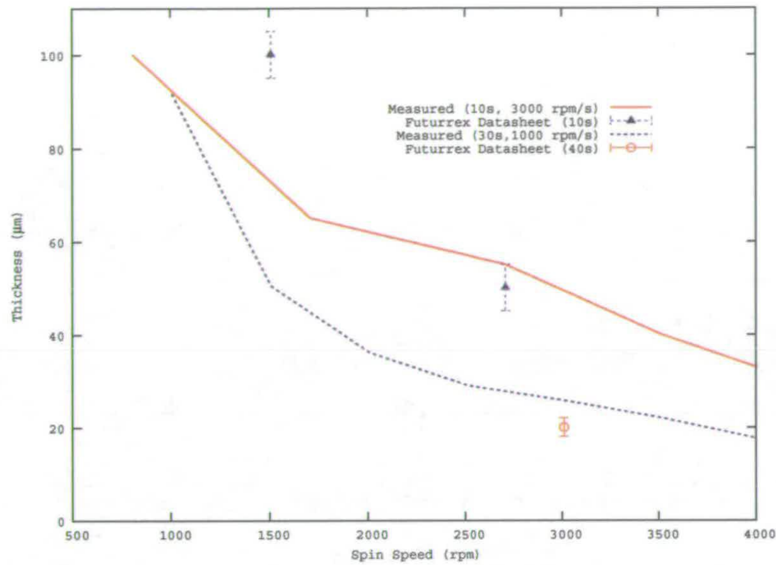


Figure 6.3: *Result of film thickness against spin speed experiments. Also displayed are the data sheet values provided by Futurrex for reference.*

With a uniform film of resist spun to the required thickness of 30 µm, the next step in the process is to soft bake (SB) the wafer in preparation for lithography. In this work, the SB is conducted on temperature controlled hot plates. The SB stage needs to be tailored to sufficiently drive the solvent content out of the resist and produce a "dry" film. At the same time the temperature must be controlled to prevent excessive stress from building up. If the stress is not controlled then cracking and delamination of the film can occur. For a target film thickness of 30 µm, the data sheet recommends a SB time of 90 seconds on a 150 °C hot plate. However, when using this recipe it was found that the resist film still contained sufficient solvent to result in a soft and adhesive surface, causing the wafer to adhere to the photomask during contact printing in the patterning step. Therefore a more conservative modified recipe was established to ensure that sufficient solvent was removed from resist prior to being placed in the mask aligner tool. First, a low temperature (70 °C) hot plate is used to bake the resist for 20 minutes to slowly drive out the bulk quantity of the solvent content. This slow process prevents the top surface of the resist from becoming too dense and forming a "crust" which would inhibit the solvent evaporation. After this, a 140 °C hot plate is used to bake the resist for a further 2.5 minutes to complete the SB procedure and dry the remaining solvent out of the film. This improved recipe presented a more dense

resist film which did not have the same adhesive properties seen before and hence avoided the possibility of sticking to the mask surface in the exposure tool.

After the film has been soft baked, it is ready for the patterning by lithographic imaging. Optimal conditions are achieved by controlling the exposure dose and printing method to achieve the desired resolution in the features. The exposure dose was optimised using a Multi-transmission mask [3] which contains resolution structures to evaluate the photolithographic performance of a photoresist on a mask aligner with dimensions ranging from 50 μm down to 1 μm. The unique property of this mask is that a technology has been incorporated such that the UV radiation energy is filtered at specific gradients across the mask. This allows the user to conduct an exposure dose experiment on a single wafer. The optimal dose is then measured by inspecting the structures and deciding which transmission segment of the wafer produces the optimal resolution in the exposed and developed features. The recipe can then be modified to reflect this optimal exposure dose.

It was during the initial work with this mask on the mask aligner tool that the poor resolution capability of the film in its current state was highlighted. Regardless of the contact method (proximity, soft contact, or hard contact) or exposure dose used, the minimum observed feature size was never less than 20 μm (much higher than the quoted aspect ratios possible). This is a typical effect expected when a large proximity gap is used during exposure. An investigation into the surface topography of the resist prior to exposure found that the resist at the edge of the wafer was approximately two times the thickness of that in the field area. This introduced a large proximity spacer and limited the resolution from the exposure stage. Figure 6.4 displays a diagram of the *edge bead* effect of the resist along with typical dimensions measured from a targeted 30 μm thick film. Because of the high viscosity of the resist and the fact that the film contracts during soft bake, the edge bead occupies approximate a 10 mm ring around the perimeter of the wafer. To remove this problem, an edge bead removal (EBR) process was implemented using a dispense nozzle with PGMEA thinner to dissolve the resist on the outer perimeter of the wafer. While this permits the resolution of much finer features, it also reduced the useable area of the wafer. Repeating the exposure test with the multi-transmission mask yielded an optimal exposure dose of

[3] Purchased from Benchmark Technologies

960 mJ/cm^2.

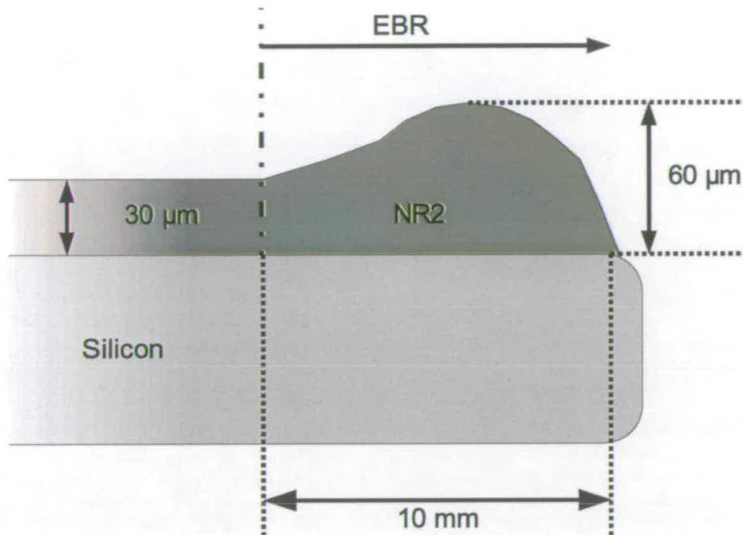


Figure 6.4: *Schematic illustration of the dimensions of the edge bead effect on the resist. Included is the point at which edge bead removal (EBR) is used to dissolve the thicker resist.*

Next the post exposure bake (PEB) must be optimised in order to achieve the desired sidewall profile in the developed structure. Once more, the data sheet provided a starting point with a recipe specifying a 80 °C hot plate for 4 minutes. Cross sectional images from the initial samples processed using this recipe demonstrate negative profiles in the sidewalls of the structures as seen in figure 6.5. This would, in turn, result in positive sidewalls of the Cu tracks plated in the resist mould. Ideally, a rectangular cross section with near vertical sidewalls is required to allow physical line width measurements from the top of the structure to reflect the cross sectional width of the whole feature. After a set of experiments conducted to optimise this issue, it was deduced that a higher temperature and longer time for the PEB recipe created the optimal profile, as seen in figure 6.6. The final recipe involved a 100 °C bake for 10 minutes.

The final step involved in the processing of the resist is developing the pattern. As the resist is negative working, the areas of the resist which were not exposed during the UV exposure stage, and hence not cross-linked, are removed in the developer solution. The process is conducted in a spray develop system, where the user is able to program parameters such as length of spray, duration of puddle, and speed of spin. The actual developer product used was RD6 as recommended and sourced from

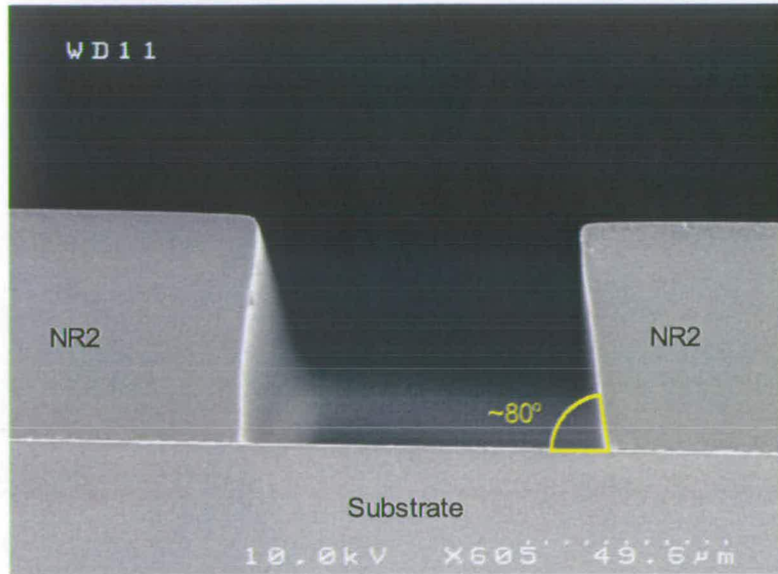


Figure 6.5: *Cross sectional SEM demonstrating the result of a PEB using 80 °C.*

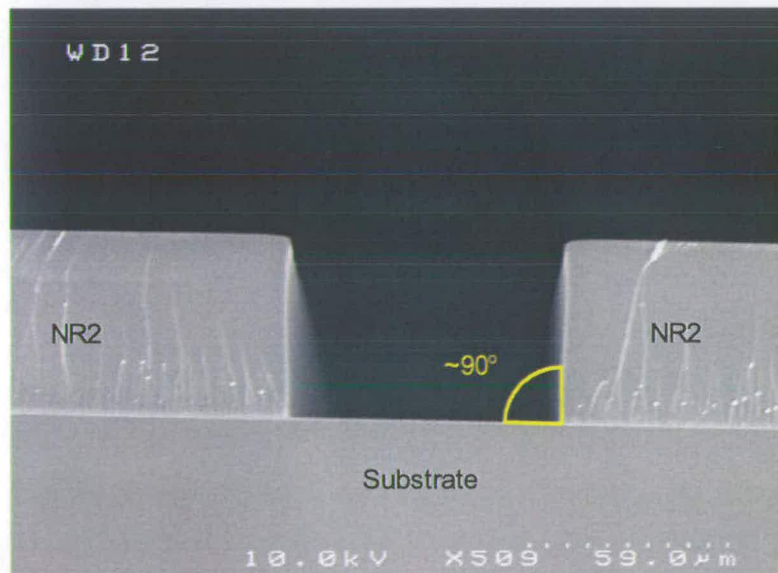


Figure 6.6: *Cross sectional SEM demonstrating the result of a PEB using 100 °C.*

Futurrex. Because of the thickness of this resist, the develop time is long in comparison to traditional thin resist layers.

The actual developer recipe used for this work employed a number of individual puddle sequences to remove the resist followed by a DI water spray rinse to clean the surface of the wafer and a high speed spin to dry. Each puddle sequence begins with a three second spray step in which the solution is dispensed onto the surface of the

wafer to form a uniform puddle. Then the wafer is rotated slowly at 10 rpm to ensure that the surface tension of the developer prevents the puddle from draining from the wafers surface. When the solution has been exhausted and is no longer able to react with the un-exposed resist, it is spun off during a brief high speed spin. This three step sequence is repeated until all the un-exposed resist has been cleanly removed.

6.3.3 Track formation

The Cu tracks themselves are created using electroplating techniques. As mentioned previously, this method uses a bottom-up approach where the Cu film is grown only in the exposed areas of the developed resist. The system used for electroplating of the Cu was a custom made unit to allow up to 8 inch wafers to be electroplated. It has a large plating tank capable of holding up to 50 litres of electrolyte solution. Agitation of the bath is provided by a filtered pump in constant recirculation. Electrical contact is made to the wafer by a wafer holder which incorporates a number of springs contacting the seed layer of the wafer[4]. These spring contacts carry the current to the seed layer during plating and are connected to a common terminal on the power supply. The anode consists of a Ti mesh basket containing Cu pellets to replenish the depleted Cu ions from the electrolyte.

As was discussed briefly in Chapter 4, electroplating of Cu can be difficult to control, especially when considering grain size and uniformity (both locally and globally). For these reasons a proprietary solution, manufactured by Rohm and Haas, was chosen as the plating chemistry. Intervia 8540 was suggested as the most appropriate product for bottom up plating through thick resist patterns [165]. The plating bath itself was made up from the following components: Cu sulphate, sulphuric acid, hydrochloric acid, an additive and a carrier. It is the last two organic components which make this solution unique as they control the grain size and thickness uniformity of the plated film. These individual components were added to the quantities specified as bath formulation 8501 on the Intervia 8540 data sheet. This formulation was chosen to provide medium performance during plating, and was suggested based on the plating bath hardware employed.

To prepare the patterned wafers for electroplating, the top layer of titanium was etched

[4]Sourced from AMMT (Germany)

away using a dilute (1%) HF acid dip to reveal the Cu seed layer. This concentration was selected to maintain a slow etch rate and minimize the undercut of the resist structures.

All electroplating optimisation work was conducted based on a 50 μm design width feature. This dimension was chosen to emphasise any issues related to the structure and profile of the Cu tracks. The actual test structures measured for parameter extraction employ line widths ranging from 25 to 9 μm.

Initial tests were conducted to analyse such factors as the uniformity of the plated material as well as the deposition rate. The first issue that arose from these tests was the large range in thickness of the plated structures across the full surface of the 8″ wafer. Typical values for this were in the order of 33% of the average thickness. Unfortunately in comparison to more advanced semiconductor electroplating tools, this issue is somewhat unavoidable based on the simple design of the plating hardware used. The deposition rate was optimised to achieve an average value of 0.5 μm min^{-1} allowing the targeted 20 μm Cu tracks to be deposited in ~40 minutes. This was achieved using a current density of 24.5 mA cm^{-2}.

The next goal of this study was to optimise the profile of the Cu lines to closely approximate to a rectangular cross section. The initial electroplated samples resulted in a "bread loaf" or dome shaped profile in the cross section of the Cu lines, as is clearly visible in the cross section shown in figure 6.7. This was thought to be due to the interaction of the plating solution and the surface of the resist. More specifically the fact that the "as processed" photoresist experienced a hydrophobic interaction with the liquid, meaning that the liquid is repelled by the resist. To alter this property, an oxygen plasma asher was used to pretreat the wafers prior to the Ti removal and subsequent plating step. The result of this simple additional process was that the wafer became hydrophilic, and the wettability of the surface to the plating solution was improved [166]. Based on this modified approach, the plating profile now more closely approximates to a rectangular cross section as shown in figure 6.8. Furthermore, this profile is now characteristic of the uniform plating expected from the use of the proprietary plating solution.

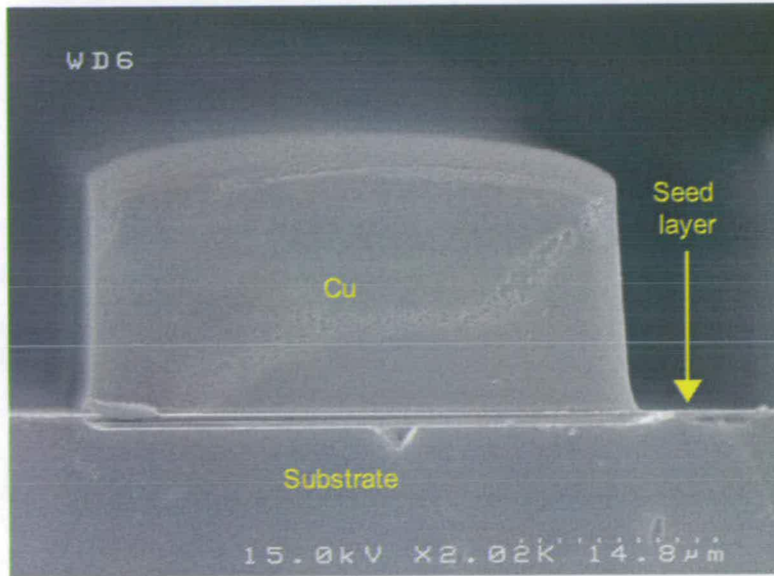


Figure 6.7: *Cross sectional SEM demonstrating the dome shaped top to the Cu track or the "bread loaf" effect.*

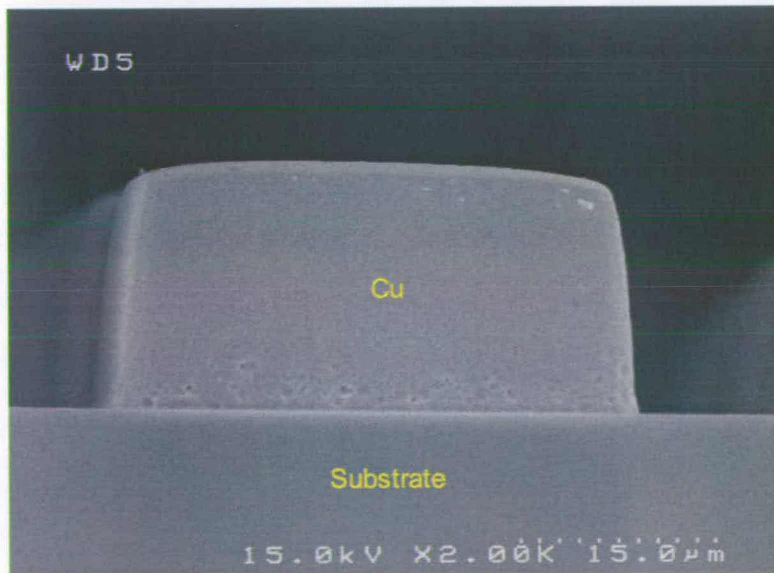


Figure 6.8: *Cross sectional SEM demonstrating the near rectangular shaped profile of the Cu track.*

6.3.4 Post processing

After the Cu tracks have been electroplated, the wafers must be further processed to prepare for electrical testing. First the photoresist is removed using a proprietary resist stripper[5] in a 70 °C heated bath for 10 minutes with ultrasonic agitation. Experience gained during this study found that processing the wafers and removing the resist as soon as possible produces the best results with minimal residue. It was found that a window of 2 days to complete the process was ideal.

The last step in the process is to remove the seed layer remaining exposed in the field area of the wafer to permit electrical testing. This was achieved using a three step process. First the exposed Ti layer is removed using a 1% HF dip similar to that used prior to electroplating. After this the Cu seed layer was etched using a proprietary etch solution designed for Al patterning[6]. A time of 5 minutes in this solution at room temperature with manual agitation at 1 minute intervals was sufficient to remove the Cu seed layer. While this etch also attacks the plated Cu lines, the quantity of material removed is minimal in comparison to the large dimensions they possess. To finish, a further dip in 1% HF solution removes the first layer of Ti. At this point the wafer is ready for electrical testing.

6.4 Results

The main goal of this study was to evaluate two of the most commonly adopted electrical test structures in interconnect metrology on MEMS thick film implementations. These are the van der Pauw cross resistor and the Kelvin bridge resistor and were collectively implemented as the cross-bridge test structure described in Chapter 2. The Greek cross was selected as the implementation of the van der Pauw structure. An image of these two structures as fabricated in the Cu tracks is presented in figure 6.9. In this image it observed that the probe pads are patterned with a waffle like design, which was chosen to present an even local open area density. Without this pattern the large open area of the probe pads could influence the deposition profile of the Cu in the test structure during the electroplating stage. It is important to note

[5] Air products - ACT/CMI PR Stripper
[6] Rockwood - Aluminium Etchant

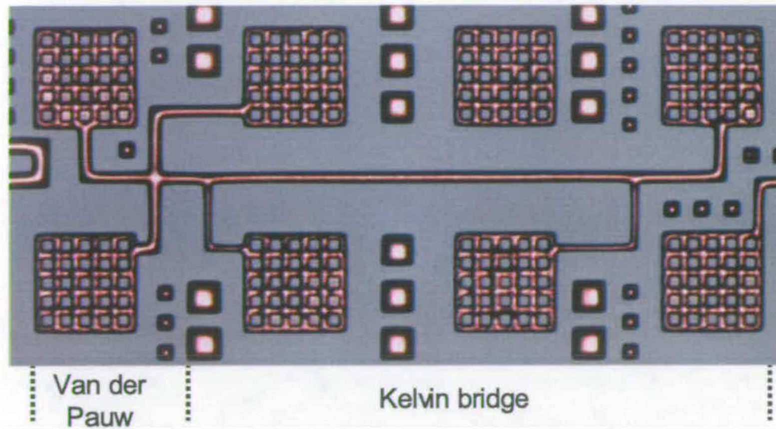


Figure 6.9: *Optical micrograph of the cross-bridge test structure used in this study.*

that this pattern does not affect the electrical measurements as the photoresist mould was removed from the inside of the probe pads and the probe tips were able to make sufficient contact with the pads during testing.

Electrical measurements were taken using a manually operated DC parametric test system. Probe pads are provided in the design to make electrical contact to the test structures while a probe station with manually manipulated probe tips were used to make physical contact with these probe pads. The parametric test system was programed to force current and measure voltage in the traditional fashion described in Chapter 2 for both the van der Pauw and Kelvin bridge resistor. Resulting I-V values were then used to investigate such parameters as sheet resistance and line width of the structures. Based on the effects of Joule heating observed in the thin film Cu ECD test structures described in Chapter 5, a number of preliminary tests were conducted to ensure that the measurements would not be subject to similar influences. In these tests, the current forced through the structures, both Greek cross and Kelvin bridge, was swept from 0 to 100 mA and the voltage monitored. Observing the resistance (R) values during the full sweep of the current cycles lead to the conclusion that as the Cu tracks are so large in cross-sectional area that the extracted values are not subject to Joule heating problems within this measurement range. Similarly measurement parameters were chosen to prevent external noise from interfering with extracted values. All reported values in this section were taken at a current of 50 mA, unless otherwise stated

6.4.1 Greek cross

The first structure under investigation was the Greek cross van der Pauw resistor. This structure is intended to extract the sheet resistance of the metal track. Unfortunately, the test setup employed for these measurements was unable to detect a significant potential drop across the two voltage sense terminals. This was true even when increasing the source current to the maximum possible 100 mA. The reason for this occurrence is believed to be due to the sheet resistance of these structures being much lower than would typically be seen in standard IC interconnect dimensions. As a result there is little voltage drop between the arms of the Greek cross structure.

To evaluate the full reason for this and to understand what equipment would enable such tests, a calculation based study was conducted. First the resistivity (ρ) of the Cu was assumed to be 1.539 $10^{-8}\Omega$m [105] and the Cu thickness (t) was chosen as the target thickness of 20 μm. This resulted in a calculated sheet resistance value of 0.77 m$\Omega/\square$ by placing the above values in equation 6.1.

$$Rs = \frac{\rho}{t} \tag{6.1}$$

The predicted resistance (R) of the corners of the Greek cross, as would otherwise be measured, can be calculated using the Rs value from above and solving for R in equation 6.2.

$$Rs = \frac{R\pi}{ln(2)} \tag{6.2}$$

This resulted in a value of 0.170 mΩ for R. At the maximum current possible on the parametric test system (100 mA), this translates to an estimated voltage drop of 17 μV. Therefore the potential difference is too low to be sensed on the setup used. The manual for the parametric test system used specifies a measurement accuracy of $\pm$ 200 μV for the range used.

This introduces the need for a few modifications to the setup used to permit electrical measurements from the test structures. First is the use of equipment capable of forcing higher currents to provide larger voltage drops across adjacent arms of the structures. Additionally required is a high sensitivity voltmeter with the ability to sense sub μV changes in potential differences. Finally, with such low voltage readings,

the arrangement of probe leads and shielding should be considered to reduce the possibilities of external noise interfering with extracted values.

6.4.2 Kelvin bridge

Next the Kelvin bridge was subject to a series of tests to evaluate its role in the extraction of parameters from thick film MEMS tracks. This setup involved forcing a current along the bridge resistor and measuring the potential drop between the two voltage taps. Fortunately, the design for this structure includes a large tap separation distance (490 µm), which allows a longer section of the bridge to be measured and hence a larger voltage drop. For the 50 mA forced, typical values for the measured voltages ranged from 50 mV to 150 mV, well within the capabilities of the measurement equipment used. This enabled the test structure to be used to analyse values such as sheet resistance and line width of the Cu tracks. The Kelvin bridge structures, in this study, were patterned with line widths of 9, 12.5 15, 20, and 25 µm.

The first parameter of interest is the sheet resistance of the structures to in turn determine the line width. Without this information the standard Kelvin formula can not be used to extract line width values. As the tap separation of the bridge structures is fixed at design level for all the structures, they are not able to be subject to the same study as was conducted on the Cu ECD structures in Chapter 5 (multiple segment analysis). The one variable in the design is the line width in which the structures are replicated in Cu. Therefore an analysis based on the relationship between the $\langle V/I \rangle$ (or R) values and the line widths (W) of the structures was conducted. A plot of the resistance of each structure against the drawn line width from which it was extracted is presented in figure 6.10. Non-linear regression techniques using least squares fit was applied to determine the relationship between the structures. The standard Kelvin bridge formula was fitted to the data as described by equation 6.3, where Wd represents the drawn line width of the structures and is used to establish a constant relationship between the structures without compensating for process biases, L is the tap separation distance (490 µm in this case) and R is the measured V/I value.

$$W_d = \frac{Rs \times L}{R} \tag{6.3}$$

The result of the regression fit to the data yields a value for *Rs* as representative for all the structures. For this particular set of data, an *Rs* value of 1.31 mΩ/□ was determined.

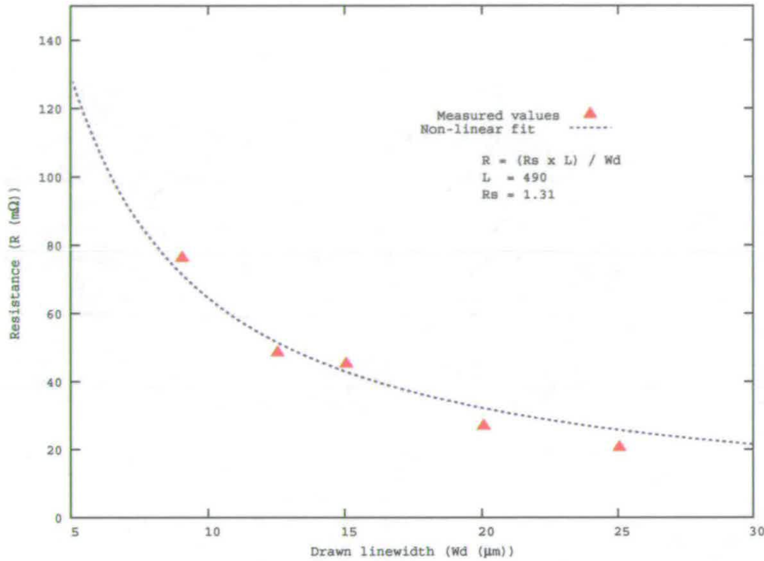


Figure 6.10: *Relationship between resistance and drawn line width of the structures.*

The *Rs* value obtained from the method above can be applied to the Kelvin formula to extract the line width for each test structure individually based on their measured *R* value. To provide a means for comparison, SEM images have been taken and analysed to extract a value for the physical line width. Each structure was measured at three points along the length of the bridge resistor to allow for averaging. After this, image processing software with metrology capability[7] was used to extract intensity profiles and fit a CD algorithm to the profiles. This CD fit provided a value for the line width of each structure. Figure 6.11 presents the results of both the SEM and electrical line width measurements for each of the structures based on their drawn line width. As can be seen from this plot, the electrical measurements appear to have a linear offset when compared to the SEM values for line width.

A separate investigation was conducted to understand the offset in line width values and to compare the value of *Rs* calculated from the Kelvin structures with the expected sheet resistance of the Cu tracks. First, the thicknesses of each structure was determined using a surface profilometer to measure step height. This was then

[7]Gwyddion - SPM analysis software

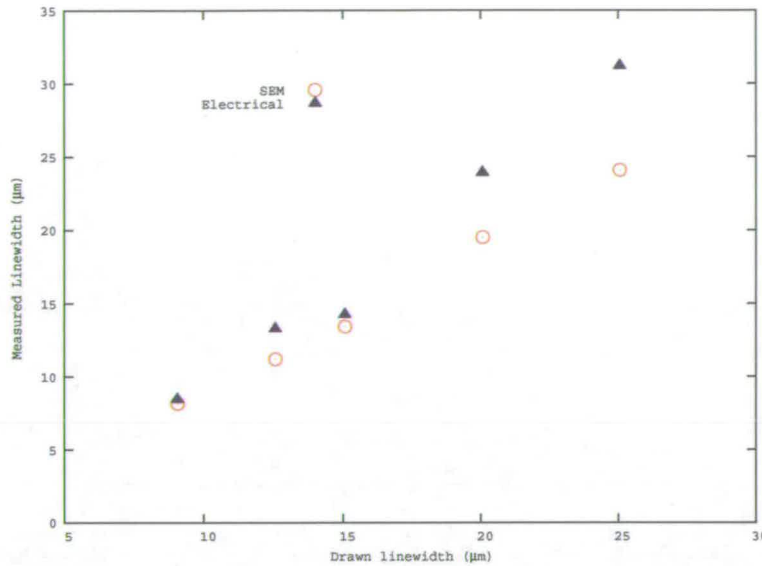


Figure 6.11: *Relationship between line width values and drawn line width of the structures for both electrical and SEM measurements.*

compared with the SEM measured line widths, along with the known tap separation distances, to extract the physical dimensions for each feature. Then, by substituting these dimensional values, along with the measured resistance, back into the Kelvin formula, the *expected sheet resistance* can be calculated. As can be seen from the results presented in figure 6.12, the average sheet resistance value from this physical analysis, calculated at 1.17 $m\Omega/\Box$, is lower than the Rs value extracted from the electrical measurements on the Kelvin bridge resistors. While the exact cause for this is unknown at present, it is thought that it could be related to the electrical influence of the voltage taps on the structure, which is not accounted for. Another possibility is the resistivity of the Cu metal track which could differ from the reported bulk resistivity values in the literature.

It is also noted that the effective sheet resistance values decrease with increasing line width and is supported by the step height measurements which revealed that the thickness conversely increase with increasing line width. This could be due to plating variation due to local current density differences as a function of the position in the die or as a function of line width. Further investigation is required to fully characterise this effect.

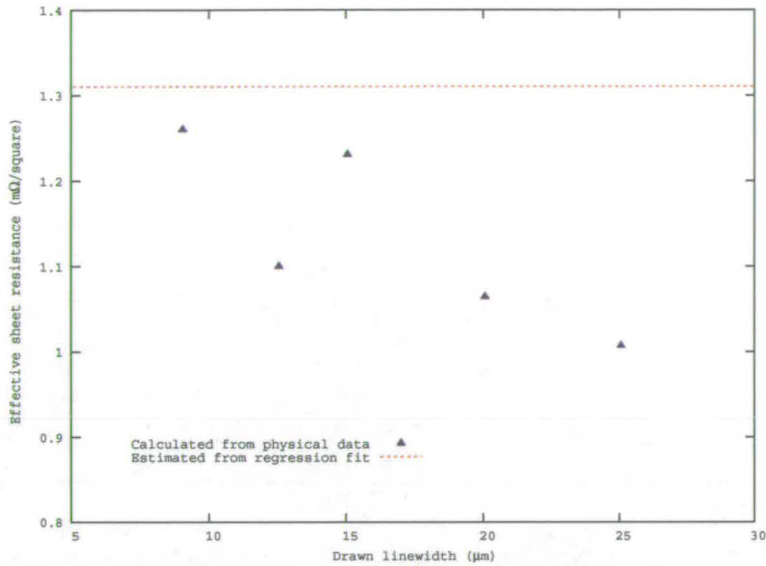


Figure 6.12: *Results of equivalent Rs values based on dimensional measurements and resistance values for each structure. Extracted Rs value from the Kelvin bridge measurements (dashed line) are presented for comparison.*

6.5 Conclusions

This chapter has provided an insight into the use of traditional interconnect test structures to characterise MEMS thick film power devices. An approach was demonstrated to fabricate large dimension interconnect tracks using a combination of thick film photoresist processing and bottom-up electroplating of Cu. Uniting the van der Pauw and Kelvin-bridge resistor to form the cross-bridge test structure (Fig. 6.9) allows the evaluation of sheet resistance and line width using electrical measurements from a range of designed line widths within a single test cell.

When subjecting the Greek cross portion of the test structure to electrical testing to extract Rs values, a large error in the extracted values was detected. To comprehend this occurrence a calculation based study revealed that the dimensions of the Cu track result in an expected voltage drop of 17 µV, a value well below the ±200 µV accuracy of the test system. As a result, the lack of sensitivity in the measurement setup meant that the Greek cross structure was not suitable for sheet resistance extraction.

To permit the extraction of line width from the Kelvin-bridge portion of the cross-resistor, alternative means were devised to determine Rs values. Comparing the measured resistance of each bridge structure with the line width it is designed

(Fig. 6.10), allows non-linear regression to be used to extract the equivalent Rs value for the set of structures under investigation (not accounting for any process bias that might exist). Placing this Rs value into the standard Kelvin-bridge resistor formula (equation (6.3)) allows a value for the line width of each structure to be extracted. Plotting the extracted line width values alongside SEM measured values (Fig. 6.11) demonstrated a linear offset between the two data sets. A physical analysis, using stylus profilometry, revealed that this was the result of height variations in the plated Cu tracks which translate to similarly varying sheet resistances.

In conclusion, the evaluation of traditional interconnect test structures to characterise MEMS power device processing has been successful. It has highlighted the need for continued work to establish measurement equipment and techniques for the accurate determination of sheet resistance values. This study has also revealed that the Kelvin-bridge structures on their own are able to extract equivalent Rs values and further work will determine to what extent this can be used for process characterisation.

Chapter 7
Conclusions and Future Work

7.1 Introduction

This thesis has presented an investigation into methods and structures for the evaluation of IC interconnect materials and processes. A number of applications have been reviewed in this work, including a novel overlay reference material structure, an all-copper ECD reference material structure and finally an evaluation of test structures for use in MEMS thick film power devices. This final chapter will provide a brief review of the conclusions made from the preceding chapters, after which a discussion of the areas for future work will be presented.

7.2 Conclusions

7.2.1 Test structure for optical-electrical overlay calibration

Chapter 3 presented a novel design for technique to determine the relationship between optical and electrical measurements of the overlay between two patterned layers. This technique originated from collaboration between researchers at the University of Edinburgh [67–70] and at NIST [71, 72] and through this collaboration the design and fabrication of the test structure was conducted. The concept was derived from the need to determine and separate the TIS and WIS interactions [58] typically seen in optical overlay tools and hence devise a reference material capable of calibrating the measurements taken from such tools. The NIST47 design was introduced with features to allow both optical and electrical measurements for overlay extraction and calibration.

Optical measurements are provided for with a frame-in-frame structure as traditionally found in the semiconductor industry for optical overlay measurements. The electrical features, on the other hand, used a design similar to digital vernier

structures reported in the past [68–70]. In this design, a reference bar is patterned on the lower conductive layer (layer 1) being examined with contact vias from the top conductive layer (layer 2) distributed on a line inclined to, and intersecting, the reference line. Layer 2 is used to provide electrical contact to each of the vias as well as the underlying reference bar in layer 1. The overlay of the test structure is measured between the first layer and the via layer in this implementation, although the design can be modified to allow other situations to be evaluated. Each test cell in the design contains elements for extraction of both X and Y components of the lateral overlay. The test cells themselves are arranged in a large array, where each test cell contains a unique offset of the via layer with respect to layer 1 allowing overlay to be measured in the range of ± 1.43 µm to a 10 nm resolution.

The design is demonstrated using a standard 2 layer Al interconnect fabrication process with a SiO_2 inter-layer dielectric. A full evaluation using resistance measurements to determine continuity of the electrical structures was conducted using standard test equipment. The results were analysed using a novel algorithm to relate measured data to designed offset values and hence allow the extraction of electrical overlay. A comparison was provided by SEM images from the frame-in-frame structures with the overlay calculated using image processing software. The result of this investigation successfully demonstrated agreement between the SEM and electrical measurements of 1 nm in the X direction with 9 nm in the Y direction.

7.2.2 Fabrication of all-copper ECD structures

Chapter 4 presented a unique design and process to fabricate structures for use as interconnect ECD reference material. The process builds on previously reported work to create Si ECD structures for reference material applications. This was combined with the damascene process to form a structure for evaluating the implementation of Cu ECD reference material. Further more, as no barrier metal was used, the test structure allows parameter extraction from all-copper features as well as fundamental studies into electron transport.

The first step in the process was to define a structure in mono-crystalline Si, called the silicon preform. This Si structure possesses near vertical sidewalls, because of the crystal properties and the nature of the etch solution used, allowing the line width to

be constant for the vertical cross section of the feature. The dimensions of this preform are preserved using a multilayer SiN stack to form a mould of the preform. The mould is then planarised to reveal the top surface of the Si which is partially etched to form a trench. After oxidising the trench bottom to electrically isolate it from the underlying Si, Cu deposition and CMP is used to define the final test pattern. A passivation layer of Parylene™ is then used to protect the structures and prevent oxidation of the Cu lines. The implementation of this structure has been successfully demonstrated using standard fabrication tools and materials found in a semiconductor fabrication facility.

The traceability of the electrical measurements in the design is provided for in a number of ways. The most important is ensuring that a portion of the Si remains in the trench with the same line width as the Cu feature. This allows HRTEM to be used to count the lattice planes in the single crystal Si to accurately extract physical line width similar to that reported in [24–27]. Furthermore, other techniques such as OCD, CD-SEM, and CD-AFM can be used to measure the line width and be used as a comparison to the electrical measurements taken.

There were a number of key issues that were overcome during the development of this fabrication process. The first was the stress present in the SiN films as a result of the thermal oxidation step. To account for this and minimise any deformation of the Cu trench that may still occur a low frequency PECVD Si_xN_y coupled with a thicker film of LPCVD Si_3N_4 were used for the mould. SEM images of the trench after the thermal oxidation stage revealed that no deformation was detectable. The next issue was the formation of voids in the trenches as a result of standard PVD Cu deposition. While the use of Cu electroplating did improve the fill capability of the film, it was unable to provide a uniform thickness over the wafer with the setup employed. Modifying the PVD sputter recipe to incorporate a 300 W RF bias on the wafer permitted the conformal deposition of the film without the presence of voids in the trenches. Finally when polishing the Cu film, with iCue 5001 slurry, to complete the damascene process, the dishing of the tracks was discovered in excess of 150 nm. In an effort to maintain the rectangular cross section of the Cu track, the evaluation of two newer CMP products led to the selection of the C7092. The use of this slurry on the Cu ECD test structures permitted reduced dishing values of approximately 10 nm.

7.2.3 ECD extraction from all-copper ECD structures

With structures fabricated using the process described in Chapter 4, the extraction of sheet resistance and line width from the structures was concentrated on in Chapter 5. This chapter presented the results of an extensive study conducted to evaluate various previously reported methods for extracting the two parameters. The primary extraction techniques employed were parametric DC electrical measurements with SEM line width measurements for comparison.

Measurements from three different types of van der Pauw cross resistors, the Greek cross, corner-tapped box cross and side-tapped box cross were taken to extract sheet resistance values. As the structures used in this study do not possess 90° rotational symmetry, Rs values were determined from the solution to the generic van der Pauw equation for the sheet resistance of a structure of arbitrary shape as described in Chapter 2. The data was expressed as a contour plot of Rs values for each location in the array of structures. Observing this data revealed that the Greek cross consistently produced lower values in comparison to the other two structures. A full investigation found that the Greek cross structure had a greater trench depth than the other two structures and correlated to the decreased Rs values. Similarly, dishing profiles were attributed to the systematic variation present in the Rs values across the entire test chip.

The Kelvin-bridge resistor structures were measured electrically to evaluate line width extraction from three different algorithms. The first was the individual segment analysis which used the standard Kelvin resistor formula along with Rs values from the van der Pauw structures in the same test cell. Comparing these values to SEM extracted line width demonstrated a lack of agreement. This was discovered to be the result of the large difference in dishing between the van der Pauw structures and the Kelvin-bridge structures. A similar lack of agreement was observed between values extracted using the multiple segment analysis and SEM line width. On the other hand, a unique algorithm described by the multiple structure analysis provided ECD values which were in close agreement with SEM line width values. This analysis technique determined the line width of a structure from the relationship between calculated slope values and drawn line widths of each structure. (Slope values were extracted using the technique described in the multiple segment analysis method.)

With the extracted line width values from this last algorithm, the effective sheet resistance of the structures can be calculated and represented in a contour plot similar to those used for the van der Pauw structure evaluation. Observing the data from this revealed a relationship between line width and sheet resistance. This was confirmed by measuring the trench depth using AFM after the Cu metal had been removed, where as line width increases trench depth similarly increases translating to decreased sheet resistance of the Cu track that occupied the trench.

7.2.4 Evaluation of test structures for MEMS

Chapter 6 presented an investigation into the use of test structures to characterise MEMS power devices. Primary interest was placed on the extraction of sheet resistance and line width from thick Cu conductive wires. The two enabling technologies employed for the fabrication of these structures was thick film photoresist for pattern definition and Cu electroplating to form the low resistance conductive wires.

The Cu structures were fabricated to thicknesses of approximately 20 μm. Therefore, a resist process was developed to achieve optimal performance for thick film electroplating applications. The resulting recipe allowed a film of negative photoresist to be spun to thicknesses of $\sim$30 μm and patterned with near vertical sidewalls.

The electroplating was conducted in a custom made plating bath using a proprietary plating chemistry and recipe. Preliminary results demonstrated a dome shaped profile in the tops of the Cu tracks, thereby not allowing the approximation of a rectangular cross section. Optimal plating performance of the Cu tracks was achieved using a surface pretreatment on the patterned resist mould in an oxygen plasma asher prior to the electrodeposition of the Cu. The improved wettability of this pretreatment produced plated Cu tracks with near rectangular profiles.

Electrical measurements were taken from Greek cross and Kelvin-tapped bridge resistor structures. Initial measurements from the Greek cross structure determined that the potential difference between adjacent arms of the Greek cross was not large enough to be sensed with the measurement equipment employed because of the large dimensions of the Cu tracks. On the other hand, the Kelvin-bridge resistor was designed with sufficient separation distance between the taps to result in a suitable

voltage drop measured on the test equipment used. Without the ability to extract the Rs values from the Greek cross structures, alternative means were devised to evaluate line width. Plotting the resistance of each Kelvin-bridge resistor structure against its designed line width allowed non-linear regression to solve for an Rs value for the set of structures being investigated. With a value for Rs, the line width was calculated using the standard line width formula for Kelvin-tapped bridge resistors.

When comparing the ECD values to line width values measured from SEM images, a linear offset was observed. A full investigation determined that this was due to the fact that the structures were plated to different heights depending on their patterned line widths. This in turn resulted in the sheet resistance varying with the thickness of the Cu and hence the equivalent Rs value calculated from the Kelvin-bridge structure did not provide an accurate representation of the sheet resistance.

7.3 Future work

Through the fabrication and analysis of the test structures described in this research, a number of areas for future work have been highlighted. The following sections serve to introduce these areas and provide possible solutions to be evaluated.

7.3.1 Test structure for optical-electrical overlay calibration

The main goal of this study was to develop and evaluate a design to serve as an optical-electrical overlay reference material. Therefore the measurements from the electrical features must provide values which have a higher accuracy than the tools they are calibrating. However to fully assess this, the "true" overlay values must be extracted. The current route for this would be to use a calibrated optical overlay tool to perform a full evaluation of the test design. This would be achieved by taking overlay readings from the frame-in-frame feature located inside each test cell of the full test structure. The result would provide a full picture of the overlay against the programmed offset values for each test cell for both optical and electrical extraction techniques. Comparing these data will determine to what extent the current design can be used for calibration purposes and highlight any abnormalities in either the fabrication or analysis methods.

Furthermore, it should be noted that the NIST 47 design was intended to be used as an initial test platform to understand the processing and analysis of the presented technique. For this reason the dimensions were made large enough to be fabricated within the overlay tolerances of the tools available at the time of this study. Creating a new test design with dimensions comparable to current day roadmap predictions on more modern photolithography tools will evaluate more aggressive CDs and move closer to seeing the technique adopted as a calibration method for optical overlay tools.

7.3.2 Fabrication of all-copper ECD structures

A considerable amount of development has taken place to fabricate a stable device that can be used to evaluate the implementation of Cu structures for ECD reference material applications. However there is still room for improvement to the current process. One of the main concentrations of the work so far has been reducing the stress in the SiN mould film. An investigation to find alternative films with lower stress values would enable greater tolerance in the processing. Furthermore, to quantify whether the residual stress in the films is still acting to deform the sidewalls of the trenches, a CD-AFM would provide invaluable three dimensional information about the trench profile. Similarly, an HRTEM would provide the missing link in the evaluation of the traceability of the structure by evaluating the Si line width and comparing it to the trench width.

As was highlighted in Chapter 6, the trench depth of the Kelvin-tapped bridge structures varies in accordance with the line width. This is presumed to be the result of loading effects present during the XeF_2 etching stage. The work conducted to optimise this stage of the fabrication process focused on achieving a low etch rate and providing uniformity and depth control across a wafer. Required is a continuation of this optimisation to provide a recipe which does not result in the same dependence of etch rate on the line width. An alternative would be incorporating a dummy fill pattern into the design to even the open area of the chip and potentially provide a more uniform etch rate based on a uniform density of the exposed Si. The last option would be to evaluate other possible selective etch processes for the creation of the trench.

Additionally, the use of (110) silicon on insulator (SOI) substrates will provide more

flexibility and tolerance in both the Si etch processes. This is because the buried SiO_2 layer used in these wafers acts as an etch stop, and the uniformity of the etch depth is governed by the thickness of the device (110) Si layer on top of this buried oxide. Therefore, when creating the silicon preforms the TMAH etch can be conducted for additional time without affecting the feature height. Similarly, the XeF_2 etch can be conducted for sufficient time to ensure that all the patterned trenches are cleared of silicon and hence of the same depth without the concern of over etching. However if this approach is adopted, then HRTEM can not be used as for reference measurements as the silicon preform will be completely removed. On the other hand, sufficient traceability can be provided with other existing metrology tools that are themselves calibrated from Si ECD structures which have undergone HRTEM measurements.

One of the well known issues with the use of (110) Si wafers and wet etching techniques is the presence of facets in the intersecting angles of patterned lines. A point to note is that this does not appear to occur on SOI substrates to the same degree as it does with bulk Si, mainly because of the ability to over etch the Si during the anisotropic wet etch step without affecting the feature height. In both cases the facets do affect the electrical measurements because of the three dimensional, non-planar geometries they possess, as in figure 7.1. In the Si ECD implementations this was observed and accounted for as a line-length shortening effect on the electrical measurements [46, 47, 132]. However, the same technique does not reduce the error in extracted values for Cu ECD structures based on the analysis made to date. While this could be the result of other more predominant effects such as Cu dishing and trench depth, reduction of the facets would allow a better understanding of these other effects of the processing. There are two specific techniques presented in the following sections which could allow these facets to be reduced in dimensions. After this a novel technique to fabricate narrow Cu lines is described for future evaluation.

7.3.2.1 Hybrid etch

This approach is similar to that reported by Allen et. al. [82] who describe a three step etch process to define Si structures in the substrate which are narrower than the SiO_2 hard masks used to pattern them. The first step is to use the standard anisotropic wet etch chemistry (KOH in this case) to initially define the height of

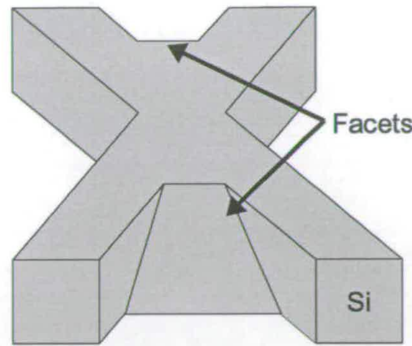
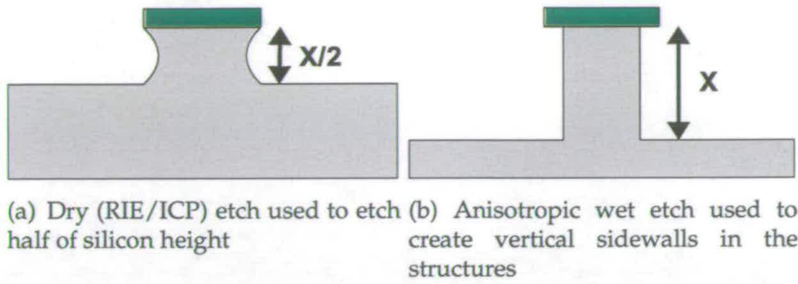


Figure 7.1: *Illustration of a portion of the silicon showing a typical representation of facets seen using single anisotropic wet etch.*

the features. Following this, an isotropic wet etch (HNA[1]) is used to reduce the horizontal dimensions of the structure. Finally, a second anisotropic wet etch ensures the sidewalls of the features are planar and that the characteristic rectangular cross-section is present. However, this method once again relies on the use of SOI substrates to define the vertical dimensions of the structures. Conducting this technique on bulk silicon wafers would result in large step heights which are not compatible with the Cu ECD process.

The suggestion for future work involves using a *hybrid* two stage etch process beginning with a dry etch such as RIE or ICP to define the pattern in the Si as illustrated in figure 7.2(a). This would be conducted to approximately half of the total desired silicon preform height (X/2). An anisotropic wet etch would then be conducted for the remainder of the required preform height (a further X/2) and hence define the sidewalls by the {111} crystal planes producing near vertical sidewalls (Fig. 7.2(b)). This should move the point at which the facet forms to half way down the height of the Si and remove the non-planar component of the facet from the Cu track as seen in figure 7.3. As the process presented in Chapter 4 uses only the top half of the silicon preform structure, during the trench etch, the Cu structure would only occupy the planar portion of the facet. The result of this would allow more accurate representations of sheet resistance providing the Cu is processed with uniform thickness. Hence this would present a rectangular cross section through any portion of the cross area of the van der Pauw structures.

[1] An HNA etch consist of varying parts of Hydrofluoric, Nitric and Acetic Acids



(a) Dry (RIE/ICP) etch used to etch half of silicon height

(b) Anisotropic wet etch used to create vertical sidewalls in the structures

Figure 7.2: *Schematic illustration of the process suggested for the hybrid etch approach to reduce the facet formation.*

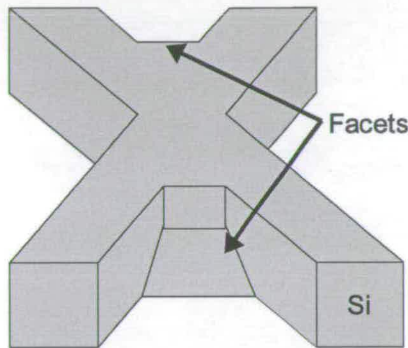


Figure 7.3: *Illustration of a portion of the silicon showing expected result of using hybrid etch approach.*

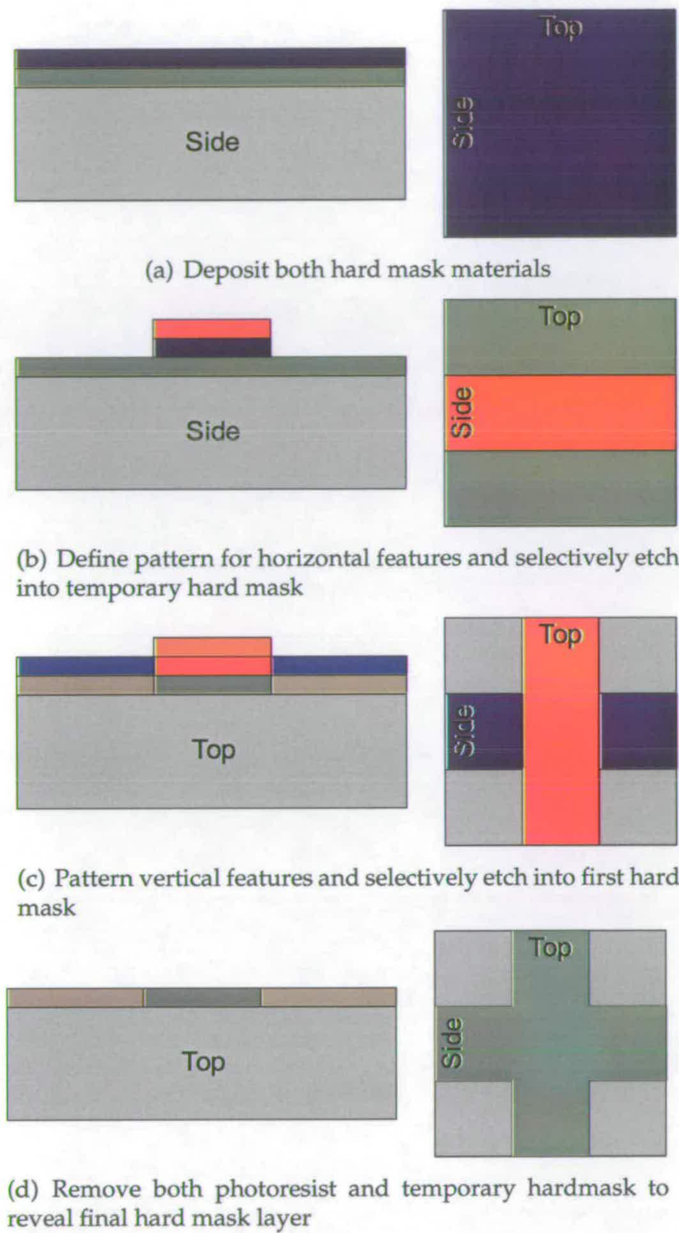
7.3.2.2 Dual-layer patterning

Another limiting factor that contributes to the facets is the result of the photolithography stage. The manner in which the light source is transmitted through the mask reticle and to the resist results in rounding of corners of a feature as described in [167]. While there has been a large amount of research conducted to reduce this effect amongst the lithography community, the modified processes tend to use state-of-the-art imaging tools with advanced photomasks. A more cost effective solution is to use what is referred to as the *dual-layer patterning* technique. This method is designed to reduce the corner rounding effect seen in the acute and obtuse angles of the intersection of two lines in the Cu ECD pattern, and more specifically in the voltage-taps on the Kelvin-bridge resistor structure. The process involves two mask reticles and masking layers to produce the single layer silicon preform structure.

The process designed for dual-layer patterning is illustrated in figure 7.4. First, two masking materials are deposited onto the wafer. The first layer is the hard mask for

the wet anisotropic etching of the Si, while the second is a temporary masking layer to pattern the first hard mask layer. The materials for these layers are selected such that it is possible to etch one of the layers selectively with respect to the other. After the mask deposition, the horizontal features of the pattern are defined in photoresist on top of the wafer. The pattern is then transferred into the temporary masking layer using an etch process which is selective to, and hence will not significantly etch, the underlying hard mask. After removing the existing photoresist, the vertical features are then defined in another layer of photoresist. This particular pattern is then transferred into the first hard mask, similarly using a selective etch to ensure that the temporary masking material remains in place. It is important to note that the horizontal patterns are also transferred into the hard mask during this step due to the patterned temporary masking layer present on top of the hard mask. After the photoresist has been removed along with the temporary masking layer, the final hard mask pattern is complete. To reduce any possible light scattering effects during lithographic patterning, the hard mask layers should be kept as thin as possible. The use of an anti-reflective coating may also assist in this process.

A small amount of "proof of concept" work has already been undertaken to evaluate the choice of masking materials in the dual layer patterning approach. For all the tests, a first layer hard mask of 100 nm of thermal SiO_2 was used. The temporary masking materials experimented with include Al, amorphous-Si, and Parylene™ and were also deposited to 100 nm in thickness. The Al and amorphous-Si were etched using a chlorine based RIE etch chemistry, as it does not significantly etch the SiO_2 hard mask. The Parylene™, on the other hand, was etched in an RIE etcher using an oxygen plasma which similarly did not etch the SiO_2 hard mask. In all cases the SiO_2 layer was etched using a fluorine based chemistry in an RIE etch tool as it was selective to all three temporary masking materials. Figure 7.5 displays a SEM image of a sample which has been processed using the amorphous-Si temporary masking layer with the underlying patterned SiO_2. By observing this image it can be noted that there is still a small degree of corner rounding at the intersecting angle. Similar results were achieved with the other two layers, but the best results to date were observed using the amorphous-Si. The results of the preliminary test demonstrate that materials can be selected to provide the capability conduct the dual layer patterning technique to produce sharp intersecting corner patterns. Continued development should permit



(a) Deposit both hard mask materials

(b) Define pattern for horizontal features and selectively etch into temporary hard mask

(c) Pattern vertical features and selectively etch into first hard mask

(d) Remove both photoresist and temporary hardmask to reveal final hard mask layer

Figure 7.4: *Schematic illustration of the process steps involved in dual-layer patterning technique. (Note direction cross section is drawn from, top or side)*

better resolution of the intersecting angles.

A test chip has also been designed (*UOE01-DLP*) and a mask fabricated to evaluate this method, however because of time restraints it has yet to be used to pattern silicon wafers. The test chip allows for a comparison between single-layer patterning (SLP), as traditionally used in semiconductor patterning, and the dual-layer patterning (DLP) proposed here. The design shown in figure 7.6(a) highlights the areas for SLP

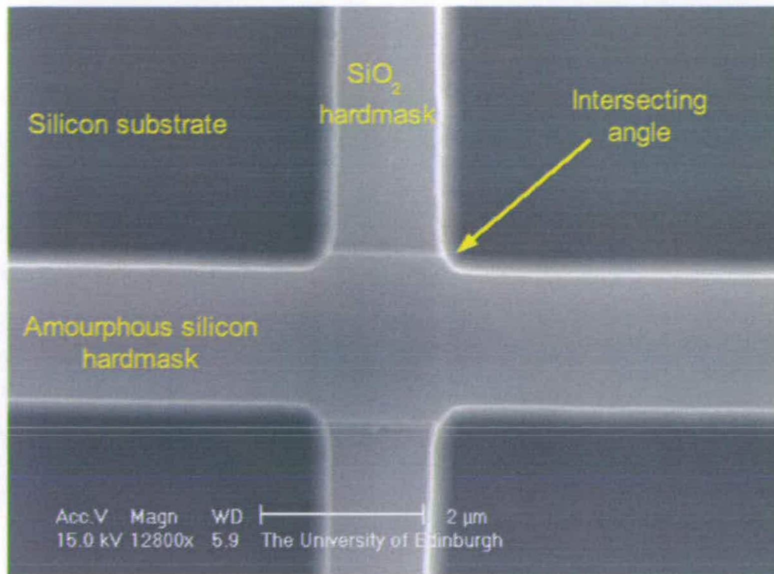


Figure 7.5: *SEM of a sample fabricated using the dual-layer patterning technique. Note that there is still a small degree of rounding at the intersecting angle between the two lines.*

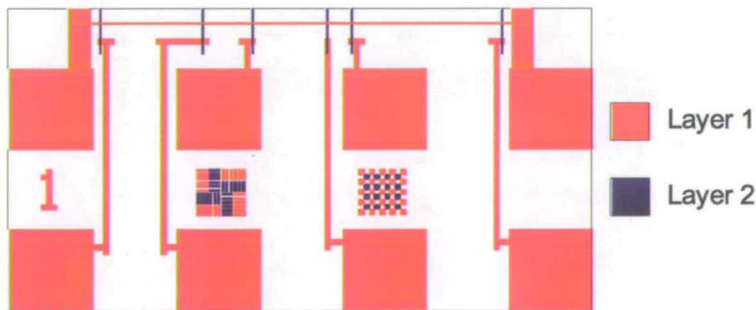
and DLP comparison. The evaluation is intended to be undertaken using electrical measurements from Kelvin-tapped bridge resistor structures, one of which is shown in figure 7.6(b). The success of the technique will be measured by comparing the δL values when applying the multiple segment analysis algorithm described in Chapter 5 to both patterning techniques. This test chip is intended to be fabricated on standard (100) bulk Si wafers and would use a traditional damascene approach to define Cu tracks in a dielectric layer. Pending the outcome of this initial experimental design, a further design could be created and implemented for use on (110) Si wafers with features aligned to the {112} crystal planes to provide vertical sidewalls in the Si.

Finally, combining the hybrid etch with the dual-layer patterning technique should achieve optimal performance and reduce the presence of facets to provide a much more accurate representation of the physical dimensions from the electrical measurements.

7.3.2.3 Hybrid lithography for narrow Cu lines

Further work also concentrates on extending the process described to manufacture Cu tracks with line widths comparable to those reported in current roadmap predictions

(a) Test chip design for evaluating both SLP and DLP patterning techniques



(b) Test structure demonstrating the two individual layers used to form the DLP technique

Figure 7.6: *Layout of test chip for dual-layer patterning evaluation.*

[168]. One key enabling technology for this is the use of e-beam lithography to pattern sub-100 nm lines in photoresist. However, e-beam lithography on its own tends to be very expensive and time consuming to pattern an entire wafer. Therefore a technique of combining both e-beam lithography with standard photo-lithography techniques has been devised to reduce the amount of e-beam work required is described in [15]. In this technique, optical lithography is used to pattern large dimension features such as probe pads and interconnect wires. The e-beam lithography is then used to define narrow lines for the evaluation of sub-100 nm Cu tracks.

The one area that should be borne in mind is the line width reduction theory which is introduced by incorrect alignment to the crystal planes of the Si wafer as observed in section 4.4.1. Fortunately there has been considerable work to establish techniques and structures to address this problem. James et. al. [169] report on the use of an etched crystal plane alignment pattern prior to imaging the actual test pattern which allows the user to inspect and align to the correct crystal plane on a wafer by wafer basis. While this may prove to be time consuming and also introduces additional processing steps, it allows greater control over the lithography to define the final line width of the etched features.

Combining the use of crystal plane alignment structures with the hybrid lithography process should enable Cu lines to be patterned using the process described in Chapter 4. As a result an investigation into narrow Cu lines which are unaffected by metal barrier layers can be conducted.

7.3.3 ECD extraction from all-copper ECD structures

The success of the work conducted to date to extract ECD parameters from the Cu test structures can be justified by the fact that an algorithm has been devised which produces values which more closely agree to SEM extracted line width values when compared with other traditionally adopted approaches. However, the measurements reported closely reflect the performance of the processing of the structures. As such, it is hoped that an improvement in the processing, as described in section 7.3.2, will result in extracted ECD values with closer agreement to physically measured line widths. The true level of success will be achieved when all three presented algorithms (individual segment analysis, multiple segment analysis and multiple

structure analysis) produce values which are in close agreement with each other as well as the physical line width measured from HRTEM extraction. Hence, this will demonstrate a robust test structure that can be used for ECD reference material applications.

One specific area of interest is continued work to further the understanding of the multiple structure analysis presented in Chapter 5. Particularly, a theoretical explanation of the role of the variable k presented in equation 5.9 and its derivation. This will either justify or highlight any unaccounted variables in the use of the non-linear regression approach to relate the measured data to the line width of the structures from which the values were taken.

7.3.4 Evaluation of test structures for MEMS

The work conducted for Chapter 6 was intended to provide an insight into the use of traditional techniques for parameter extraction using electrical test structures replicated in MEMS thick film devices. A more immediate requirement is the need for test equipment with higher sensitivity to detect and measure the voltage difference present in the Greek cross test structure based on the current design dimensions. This also requires a highly shielded test setup to prevent interference from external noise sources based on the low voltage values present. Improving the electroplating process to ensure that the structures are of equal height will allow a better approximation of sheet resistance to be made when conducting the analysis method based on the Kelvin bridge structures. Further work also includes either developing new or exploiting currently existing test structures and extraction algorithms to determine the sheet resistance of a patterned structure. This will allow the cross-bridge test structure to be used to its full extent and allow compensation for local variations in height and hence sheet resistance.

7.4 Final remarks

The work presented in this thesis has investigated a number of novel approaches for the fabrication of, and parameter extraction from, microelectronic test structures. It has built upon existing and previously reported techniques for test structure

design and analysis as well as introducing some new ones. The main concentration was on the development of reference materials for interconnect material and process characterisation. This was achieved with an implementation of an optical-electrical overlay calibration test structures as well as a Cu ECD structure to permit fundamental studies of all-copper lines. The final experimental chapter presented an implementation of standard test structures in thick film MEMS power devices and provided information on the use of interconnect test structures for this new and emerging technology.

This study has covered a number of different areas and has seen the development of various processes and extractions methods used. The information contained here will provide a basis for future research to improve and build upon the methods for interconnect test structure fabrication and analysis. Continued improvement will hopefully see the reference material structures being adopted by national institutions such as NIST.

Appendix A
Publications

This appendix contains copies of papers which were presented during the course of the work conducted for this thesis.

A.1 International Conference on Microelectronic Test Structures, ICMTS (Austin, Texas, USA, 2006)

Design and Fabrication of a Copper Test Structure for Use as an Electrical Critical Dimension Reference

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Abstract— **A novel copper damascene process is reported for fabrication of Electrical Critical Dimension (ECD) reference material. The method of fabrication first creates an initial "silicon preform" whose linewidth is transferred into a trench using a silicon nitride mould. The trench is created by removing a portion of the silicon and replacing it with copper to enable both Transmission Electron Microscopy (TEM) and electrical linewidth measurements to be made on the same structure. The technique is based on the use of anisotropic wet etching of (110) silicon wafers to yield silicon features with vertical sidewalls. The paper demonstrates that this method successfully produces copper lines which serve as ECD control structures and the process can be applied to any damascene compatible material for developing electrical linewidth measurement reference material.**

I. Introduction

With industry's push to meet ever more strict R-C timing requirements, new materials have been adopted in interconnect wiring schemes. The major recent change has been the replacement of aluminium-based materials by copper as the interconnect metal of choice. The main reasons for choosing copper are the lower resistivity and better immunity to the damaging effects caused by electromigration compared to aluminium [1]. There have been a number of publications addressing methods of extracting the electrical linewidth values from copper interconnect features [2], [3], [4]. However, these all concentrate on how to minimise the effect of the barrier layer and as a result are not suitable approaches for a reference standard. However, other papers [5], [6] have been published that describe electrical linewidth test structures fabricated in monocrystalline silicon for use as reference material. This work provides a means by which Electrical Critical Dimension (ECD) standards can be derived from electrical test structures. Unlike Scanning Electron Microscopy (SEM) or Transmission Electron Microscopy (TEM) methods, electrical measurements are a non destructive and cost effective way of determining CD values in the vast quantity that is required for end user applications. However, electrical measurements on their own "have not yet shown to be able to provide traceability with acceptable levels of uncertainty" [2]. Hence, to be a traceable standard the electrical measurements of linewidth must be calibrated to High Resolution Transmission Electron Microscopy (HRTEM) measurements [7] where the number of atoms in the track width is counted and from a knowledge of the atomic spacing the linewidth determined.

[1]Official contribution of the National Institute of Standards and Technology; not subject to copyright in the United States of America

II. Requirements for a Copper ECD Structure

Reference ECD silicon test structures reported in the literature have had the following features [2], [5], [6], [7]:

1) A rectangular cross-section (Fig.1)
2) A heavily doped single crystal conducting track with a uniform resistivity
3) Electrical linewidth is related to the number of silicon atoms across its width

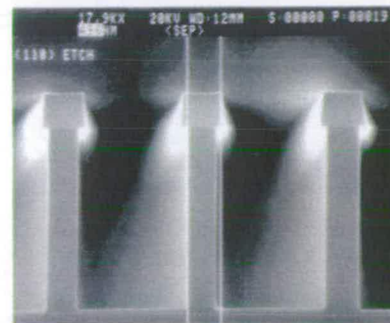

Fig. 1. SEM of feature fabricated in (110) silicon demonstrating rectangular cross section [2]. (Hard mask has not yet been removed)

Reference copper ECD structures obviously need similar features but their implementation requires significant modifications. The major differences are:

1) Copper can not be etched with atomically vertical sidewalls

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2) Copper tracks are typically encased in a diffusion/adhesion barrier such as tantalum nitride (TaN) which makes them non-homogeneous, resulting in a non-uniform resistivity.[8]
3) Copper does not have a crystal structure that can be used to determine line width

These differences make producing a copper ECD structure a much more challenging task. However, despite these differences the strategy used to produce silicon ECD reference material can be adapted to fabricate copper reference structures. The key element borrowed from the silicon reference ECD standard is the use of (110) silicon to produce mesas with rectangular cross sections which are used to form moulds for copper tracks. This approach also provides a reference measurement capability, as the single crystal silicon underneath the copper track (and with the same linewidth) can be used to calibrate the electrical measurement of the copper track. Additionally conducting barriers are not used to line the trenches prior to copper deposition because this makes tracks non-homogeneous. For the structures reported in this paper a silicon nitride barrier has been used.

This test structure enables linewidth to be determined using both TEM and electrical measurements. The key to the process described is the ability to fabricate copper lines using the damascene approach [9], [10]. The damascene implementation first requires a dielectric to be deposited which is then etched with trenches to form the interconnect pattern. After a blanket deposition of copper and a damascene CMP (Chemical Mechanical Polishing) step, the resulting trenches filled with copper form the interconnect track. The final step involves depositing a passivation layer to prevent oxidation of the copper track.

For the copper ECD structure a silicon mesa is etched in (110) silicon in a very similar manner to that used for silicon ECD reference test structures. This preform, shown in Fig. 2(a), is used to define the linewidth of the copper track. The dielectric is then deposited to create a mould of the silicon feature (Fig.2(b)) and also acts to preserve the linewidth during the etching (Fig.2(c)) of the trench and the deposition of the copper (Fig.2(d)).

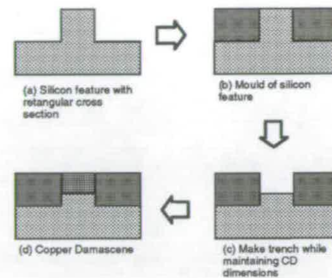


Fig. 2. Overview of copper ECD fabrication

III. Fabrication Process

A. Introduction

The fabrication process is outlined in Fig. 3 and the following sections provide full details of the process.

B. Fabrication of the Silicon Preform

One of the more important elements involved in this work is the silicon substrate which enables tracks with vertical sidewalls to be created. When a pattern is aligned to the (112) crystal direction of a (110) wafer, and then anisotropically etched, the resulting structures have a rectangular cross section and nearly atomically parallel sidewalls. In previous work HRTEM has been used to accurately determine the linewidth of (110) silicon features [7] by counting the lattice planes across the width, and the same approach has been adopted in this work.

The actual structures used for both electrical measurement and the HRTEM measurement are defined using a light field mask such that the masked structure forms free standing silicon tracks. The first step in this process is to thermally grow a 0.5 μm thick silicon dioxide (SiO_2) film to act as a hard mask (Fig.3(a)). This is then patterned using standard photolithography (Fig.3(b)) and the SiO_2 etched using a Reactive Ion Etching tool to transfer the pattern into the film (Fig.3(c)). The photoresist is then removed using an oxygen plasma asher and the exposed silicon etched using Tetramethylammonium hydroxide (TMAH). This etch is inherently lattice-plane selective, creating free standing silicon mesas, and in this paper these structures are referred to as "silicon preforms" (Fig.3(d)). This silicon preform defines the final dimensions of the copper line and provides a structure which can be examined with HRTEM to extract linewidth. After etching the silicon preform, the SiO_2 hard mask is removed in a buffered hydrofluoric acid solution (BHF).

C. Creation of the Preform Mould

The next major step is to ensure the dimensions of the silicon preforms are preserved and hence provide a traceable CD. To accomplish this a dielectric film is blanket deposited over the wafer. This effectively creates a mould around the silicon preform and acts to physically maintain its linewidth especially during the etching of trenches for copper deposition. This dielectric film must possess good mechanical, chemical, and electrical properties in order that further processing steps can be conducted while still maintaining the dimensions of the trench. Another important point to note with the choice of the material for the mould is its compatibility with copper. These compatibility issues include meeting the requirements for adhesion, diffusion and oxidation [8] bearing in mind that no other barrier material is

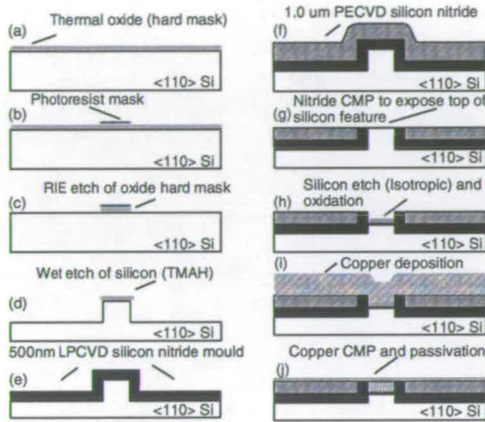


Fig. 3. Fabrication Process

being used. Copper has been reported to have a high adhesion strength to low pressure chemical vapour deposition (LPCVD) Si_3N_4 [11], [12] and meets the above requirements [13]. This is of importance for the following copper CMP stage of the damascene process.

One potential issue associated with using silicon nitride is the high stress induced during deposition, which can cause deformation or cracking of the film and structures on the wafer. However, both LPCVD and plasma enhanced chemical vapour deposition (PECVD) can be operated in regimes where the films' stress and density can be controlled.

In the initial architecture a thin layer (50 nm) of LPCVD Si_3N_4 was deposited over the surface of the etched silicon wafer. As this deposition method produces a dense film of stoichiometric Si_3N_4 it provides mechanical support for the silicon preform and an adhesion layer for the copper interconnect line (Fig. 3(e)). Following this, PECVD silicon nitride is blanket deposited in sufficient thickness (1.5 μm) to provide a surface for CMP planarisation that will also minimise any erosion or dishing effects (Fig. 3(f)). The PECVD silicon nitride also acts to provide further structural support to the LPCVD nitride that will form the copper mould. The PECVD film was deposited using a mixed frequency[2] recipe at a ratio of 6:2 (high frequency : low frequency) such that the resulting film exhibited near zero stress.

The next step is to expose the tops of the silicon preforms. This is accomplished by planarising the wafer using CMP to expose the top of the silicon preform (Fig. 3(g)). With the top of each silicon structure exposed and the rest of the wafer protected by silicon nitride the next step is to etch vertically into the silicon preform to create trenches for the copper lines. This must be performed such that a horizontal flat surface is created in the bottom of the newly formed trench (Fig. 3(h)). This is important as a track with a rectangular cross section is required for the electrical measurements. Another requirement for this etch is that it must have extremely high selectivity with silicon nitride such that the sidewalls of the trench are not attacked and continue to maintain the CD traceability. Xenon difluoride (XeF_2) has been selected to isotropically etch the silicon as it has high selectivity to the nitride mould (SF_6 has also been used but was found to have poor selectivity with nitride). It has been reported in the literature [14] that the selectivity of silicon to silicon nitride in XeF_2 is roughly 500:1 and that SiO_2 does not etch at all. Before the etch step the wafers are dipped in a dilute solution of BHF to remove any native oxide which has formed on the surface of the silicon. In a further effort to optimise the flatness of the trench bottom, the maximum trench etch depth is kept less than 0.5 μm. To enable such a shallow etch the conditions on the XeF_2 vapour etch tool were adjusted to heavily dilute the XeF_2 vapour with large amounts of helium to reduce the effective etch rate. Finally, to isolate the copper tracks from the underlying bulk silicon a thin layer of gate oxide is grown (Fig. 3(h)). To minimise stress and thereby maintain the CD traceability of the trench, the $Si0_2$ film is thermally grown at a temperature of 800°C to a thickness of 20 nm. A thin film such as this minimises the formation of a "birds beak" in the oxide film.

D. Copper Damascene

The final process sequence is the creation of the copper tracks, and this starts with the blanket deposition of copper. There are a number of methods available for this task which include, Physical Vapour Deposition (PVD), chemical vapour deposition, evaporation, and electrochemical deposition. Due to the dimensions used with these devices it was possible to use PVD magnetron sputtering to conformally coat 1.5 μm of copper over the surface of the wafer (Fig. 3(i)). The 1.5 μm thickness of the copper is required for the CMP planarisation. The wafers are polished until the copper film is removed from the field area to reveal copper filled trenches (Fig. 3(j)). It is important to ensure that the copper is planar with the top of the trenches and does not suffer from the effects of dishing or erosion. Finally, to prevent any oxidation of the copper line which may occur over time, a passivation layer must be deposited over the copper to isolate it from the atmosphere. There are many choices for this material, however Parylene[3] has been reported to be very compatible with copper interconnects [15]. A thin Parylene film is blanket deposited at room temperature, which will not affect the properties of the copper

[2]Mixed frequency PECVD films are composed of alternating cycles between the high frequency and low frequency components. The stress of the mixed frequency film can be altered by specifying the ratio of deposition times at each of the two frequencies.

line.

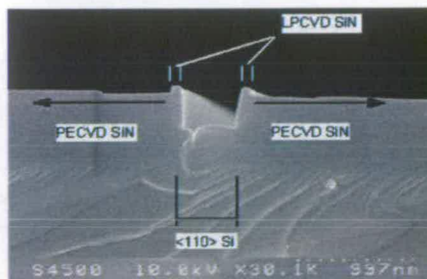
IV. Results

Cross-section SEM pictures for the major processing steps can be seen in Fig. 5. These images were used during fabrication to examine the structure after the various processing steps and identify any issues.

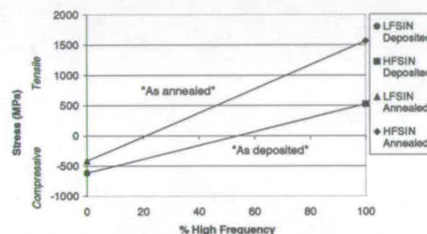
During the fabrication of these devices it was found that the linewidth of the etched silicon preforms was occasionally considerably smaller than that defined by the hard mask. This was due to the misalignment of the wafer flat to the crystal orientation and can be directly attributed to the rotational linewidth reduction theory [16]. If there is a rotational misalignment of the test pattern to the (112) crystal direction then this causes an undercut during the TMAH etch step which can be used to advantage to obtain narrower preforms.

Typical TMAH etch recipes used in industry are designed for high etch rates of around 0.8 μm/min. However, as the structures required for the silicon preforms are targeted at 1 μm in height this etch rate is not appropriate. Hence an adapted etch recipe has been formulated to improve the control over the etch repeatability and uniformity. Using 25 % concentration by weight, TMAH at a temperature of 50°C an etch rate of ~0.2 μm/min has been achieved.

When the initial batch of devices experienced the thin gate oxidation to isolate the trench prior to copper deposition it was noticed that the width of the trench increased at the top (Fig. 4(a)). The cause of this was confirmed to be the high temperature growth of SiO_2, which also annealed the PECVD silicon nitride film. This resulted in the silicon nitride stress becoming more tensile at room temperature and created force on the silicon features which caused a slight deformation of the trench sidewalls. As a result the CD dimension, that up to this point had been preserved, was altered and no longer traceable. To characterise these stresses a number of experiments have been conducted. These experiments involved depositing low frequency, high frequency, and mixed frequency PECVD silicon nitride films and measuring their "as deposited" and "as annealed" stresses. Fig. 4(b) shows that the stress of the high frequency "as deposited" nitride film is roughly 530 MPa tensile and becomes roughly 1500 MPa tensile after the anneal process, an increase of ~1000 MPa of tensile stress. Conversely the low frequency "as deposited" stress is roughly 600 MPa compressive and becomes roughly 400 MPa compressive after annealing. Hence the increased stress induced by the low frequency anneal (~200 MPa tensile) is only about a fifth of that observed in the high frequency silicon nitride. The recipe used for depositing the mixed frequency silicon nitride included a high percentage of high to low frequency deposition and it was surmised that the majority of the sidewall deformation was caused by the tensile stress created during the anneal of the high frequency portion of this film.



(a) Sidewall Deformation

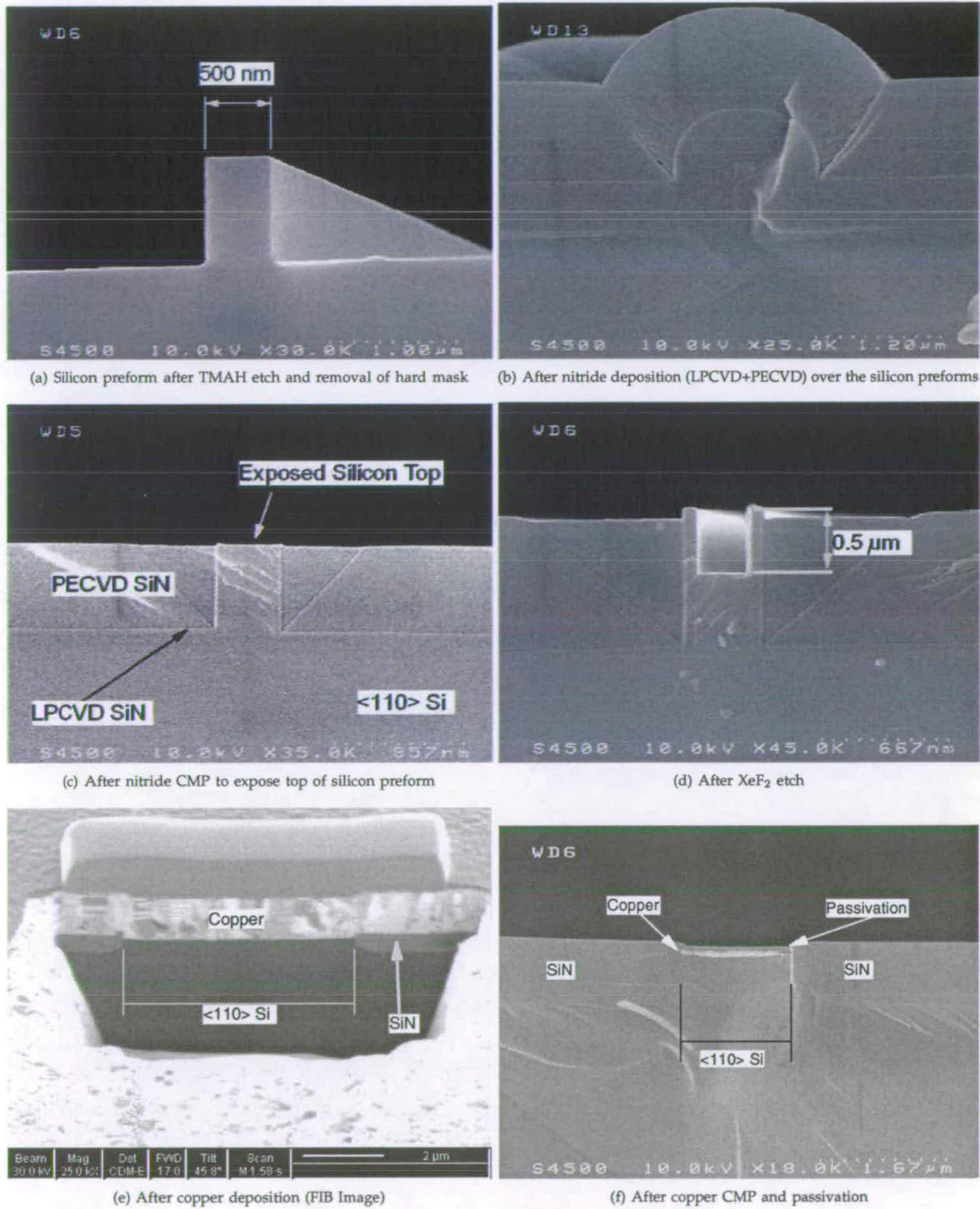


(b) PECVD Silicon Nitride Stress before and after anneal

Fig. 4. Silicon Nitride Stress Issue

To overcome this issue a stronger film with much less stress is desirable. First, as LPCVD Si_3N_4 is a rather dense material and is deposited at a similar temperature to the gate oxidation step, a thicker film (~500 nm) of LPCVD Si_3N_4 was deposited around the silicon preform to provide better mechanical support. LPCVD Si_3N_4 is typically deposited with a tensile stress and so the film thickness is limited to around 0.7 μm to ensure it does not crack. PECVD is then used to deposit a further 1 μm of silicon nitride. Based on the results gathered from the PECVD stress tests, the low frequency recipe exhibits the least change in stress during the thermal anneal. Therefore this film is deposited on top of the LPCVD nitride.

By inspecting the SEM images, Figs. 5(d) and 5(f), at high magnification it was determined that the sidewalls remain vertical and Fig. 5(d) shows that the bottom of the trench is horizontal. However inspection of Fig. 5(f) suggests there is uncertainty as to whether the copper track is horizontal and parallel on top and bottom surfaces. This may be due to SEM charging and/or the section (which is not viewed at 90°) having a non-planar surface. Further work is required to fully characterise this aspect.



(a) Silicon preform after TMAH etch and removal of hard mask

(b) After nitride deposition (LPCVD+PECVD) over the silicon preforms

(c) After nitride CMP to expose top of silicon preform

(d) After XeF_2 etch

(e) After copper deposition (FIB Image)

(f) After copper CMP and passivation

Fig. 5. Cross sections of test structure during processing

V. Testing Strategy

There are two methods for extracting linewidth values for which the test structure has been specifically designed (Fig. 6). These are electrical measurements to extract resistivity and hence electrical linewidth as well as using HRTEM on the single crystal feature below the copper track. This enables the electrical CD measurements to be calibrated using the HRTEM lattice plane count of the silicon feature. The results from these tests should determine the repeatability of the process as well as identify any other issues with the design.

VI. Conclusions

This paper has presented a fabrication process that can create a test structure with the potential to be used as a copper electrical critical dimension reference standard. This damascene process is based on the ability to define a silicon structure of known dimensions and to preserve these dimensions throughout the various processing steps. One of the most important aspects of this process is to ensure that the fabrication steps and materials are selected such that the linewidth of the copper interconnect line remains the same as the linewidth of the silicon preform remaining directly under the copper line. This enables electrical measurements to be calibrated using HRTEM linewidth measurements and hence provide a means for ECD extraction. Although the test structure has been demonstrated with copper tracks, it is suitable for use with any damascene compatible material to produce ECD reference material.

During fabrication, the initial nitride mould was found to introduce a considerable error in the CD dimensional transfer, which could be overcome by using thicker LPCVD nitride coupled with a new PECVD low frequency film. However, there is still the requirement to confirm that the silicon preform dimensions have been faithfully transferred to the copper linewidth. In addition more precise testing is required to determine if the proposed design does indeed maintain the CD of the silicon preform after the various processing steps. Another area that requires further characterisation is the uniformity of the etch and oxidation step at the bottom of the track and any effect of the XeF_2 etch on the width of the silicon nitride mould. HRTEM evaluation of the single crystal silicon under the copper track will be invaluable in fully characterising the full extent of effects.

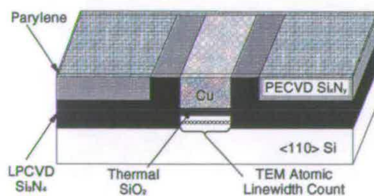


Fig. 6. Structure used for copper ECD reference

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[3]Certain commercial equipment, instruments, or materials are identified in this paper in order to specify the experiment procedure adequately. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.

A.2 International Conference on Microelectronic Test Structures, ICMTS (Tokyo, Japan, 2007)

2007 IEEE International Conference on Microelectronic Test Structures, March 19-22, Tokyo, Japan. 1.3

Extraction of Sheet Resistance and Linewidth from All-Copper ECD Test Structures Fabricated from Silicon Preforms

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Abstract— **Test structures have been fabricated to allow Electrical Critical Dimensions (ECD) to be extracted from copper features with dimensions comparable to those replicated in IC interconnect systems. The implementation of these structures is such that no conductive barrier metal has been used. The advantage of this approach is that the electrical measurements provide a non-destructive and efficient method for determining CD values and for enabling fundamental studies of electron transport in narrow copper features unaffected by the complications of barrier metal films. This paper reports on the results of various tests which have been conducted to evaluate the current design.**

I. Introduction

The need to develop a test structure capable of facilitating electrical extraction of parameters such as sheet resistance and linewidth from copper interconnect features has been presented in a number of papers [1]–[3]. A detailed description of the fabrication of a copper test structure that provides such a capability has been recently published [4]. The benefits of using this structure are that, due to the process and nature of the substrate material used, the copper interconnect features possess a nearly rectangular cross section. This allows linewidth to be extracted primarily by way of electrical measurements from specially designed all-copper test structures. Although a copper interconnect, in commercial applications, employs barrier layers for adhesion, diffusion, and oxidation properties, the structure reported here does not include a barrier metal in order to allow fundamental studies of all-copper features. The work aims to further the understanding of copper interconnects both with and without barrier layers. As a means of determining the traceability of this method as well as providing necessary calibration measurements, the structure reported also allows the linewidth to be measured using previously demonstrated techniques including, Atomic Force Microscopy (AFM), Critical Dimension - Scanning Electron Microscopy (CD-SEM), Optical Microscopy, and High Resolution Transmission Electron Microscopy (HRTEM) [5]–[7]. The NIST 35 design [8] was used to fabricate the all-copper test structures. Analyses of extended electrical measurements made on them are presented in this paper.

[1]Official contribution of the National Institute of Standards and Technology; not subject to copyright in the United States of America

II. Fabrication Overview

The substrate material employed for these structures is ⟨110⟩ silicon, chosen for its etch characteristics in anisotropic wet etch solutions. The test patterns are aligned to the ⟨112⟩ crystal-lattice vectors in the surface of the wafer and printed using a silicon oxide (SiO_2) hard mask. The pattern is then etched into the silicon with a tetramethylammonium hydroxide (TMAH) wet etch solution, which is inherently lattice plane selective. Due to the nature of the single crystal silicon and the etch solution, the sidewalls of the structures as defined by the ⟨111⟩ crystal planes provide a rectangular cross section with nearly atomically parallel sides [9]. This resulting silicon mesa is referred to as a "Silicon Preform" and may be used as a reference for linewidth. The dimensions of this silicon preform are preserved with a multilayer dielectric stack of low pressure chemical vapour deposition (LPCVD) and plasma enhanced chemical vapour deposition (PECVD) silicon nitride (SiN). These layers are then chemical mechanical polished (CMP) to expose the top of the silicon preform which also presents a planar surface. A portion of this silicon is isotropically removed to form a trench of which the bottom is oxidised to provide electrical isolation from the substrate. Subsequent copper deposition and CMP steps define the final copper test structures. Throughout the fabrication of these devices, care has been taken with the process steps to ensure that the copper film does not oxidise. The final step involves the deposition of parylene to act as a passivation layer and hence prevent any oxidation of the copper features. The parylene film is removed from probe pads to allow electrical contact during testing. At this point the structure is ready for electrical measurements to extract electrical parameters of sheet resistance and linewidth (Fig. 1). Typical copper thickness seen in the structures used for this study was 300 nm.

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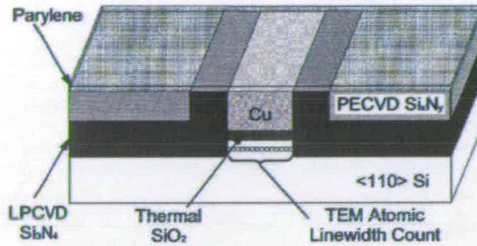

Fig. 1. Diagram cross section of test structure used [4]

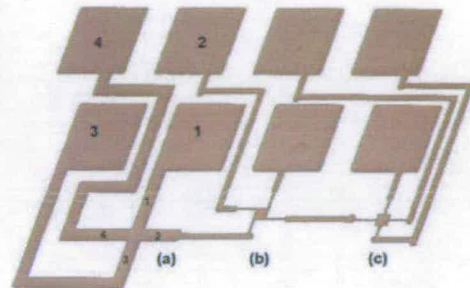

Fig. 2. Test structures used to extract sheet resistance for copper interconnect features (a) Greek Cross (b) Corner Tapped Box Cross and (c) Side Tapped Box Cross

III. Method

The analyses of sheet resistance and linewidth of the copper test structures are based on work which has been reported previously [10]. Measurements are designed to be undertaken using a standard DC parametric test system comprising of a current source and a high sensitivity voltmeter[2]. Electrical contact is made to the devices using a probe station and probe card fixtures. During electrical testing, parameters were chosen to maintain the linearity of the V-I variables and to reduce the impact of joule heating.

A. Sheet Resistance

Sheet resistance measurements reflect thickness variations in the copper film as well as provide a useful parameter for linewidth extraction. V-I measurements were taken from three different van der Pauw sheet resistance structures located at various sites over the entire die. The three structures are the Greek Cross, Corner Tapped Box Cross, and the Side Tapped Box Cross (Fig 2).

Fig. 2(a) is used to explain the measurement strategy for sheet resistance measurements. Forcing a set current from arm 4 to 1 and measuring the voltage drop across arms 3 and 2 as well as similarly forcing current the reverse direction from 1 to 4 and measuring the voltage between 2 and 3 provides two values which can be averaged to determine the $(V/I)_1$ value for the obtuse angle. In the same manner, the acute angle is measured by forcing current in both directions on arms 1 and 2 while measuring the voltage drops across arms 4 and 3, providing $(V/I)_2$. The actual sheet resistance value is then calculated using the (V/I) values to solve for Rs in the generic van der Pauw equation (1) [11].

$$exp\left(\frac{-\pi(V/I)_1}{Rs}\right) + exp\left(\frac{-\pi(V/I)_2}{Rs}\right) = 1 \quad (1)$$

[2]As DC electrical tests are performed to extract parameters from the copper test structures, skin effects, which become noticeable in copper lines at high frequency applications, are not present.

B. Linewidth

The linewidth test structures used for these measurements are specifically designed to eliminate the need for strict design rule restrictions as seen in standard linewidth cells [12]. From Fig. 3 it can be observed that they consist of multiple tapped bridge resistors with a range of segment lengths having a constant linewidth from which V-I values can be extracted.

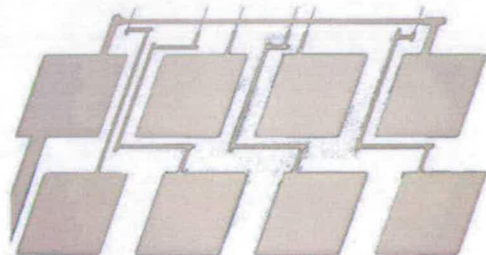

Fig. 3. Test structure used to extract linewidth for copper interconnect features

1) Individual Segment Analysis: In this method linewidth is extracted using the standard formula for Kelvin type bridge resistor structures as defined in equation (2), where W_m is the measured linewidth, L_i and $(V/I)_i$ are the segment length and (V/I) values for each segment respectively, and Rs_n is the representative value for the sheet resistance of the bridge resistor.

$$W_m = \frac{Rs_n L_i}{(V/I)_i} \quad (2)$$

As there are multiple segments in each structure all having the same linewidth, extracted values for W_m can

15

be taken and averaged to reduce measurement error.

2) Multiple Segment Analysis: Another approach to extracting ECD values from the test structures is to apply linear regression techniques to solve for linewidth. One point to note is that, due to the nature of photolithography and the etching of the silicon, the intersection of the line and the voltage taps produce facets of unknown dimensions. These facets present an electrical influence on the structure and hence introduce a source of uncertainty seen as a difference from the drawn line length. Furthermore, at small dimensions, where the tap width is of the same or larger dimension than the bridge structure, further variations in measurements due to the intersection of the taps are experienced. This value of line length variation is described by the term δL [13], [14]. Equation (3) better defines the formula for determining the linewidth (W_m) of a given structure by including the numerical effect of the facets on the linelength [3].

$$W_m = \frac{Rs_n(L_i - \delta L)}{(V/I)_i} \tag{3}$$

This method requires that the test structure has $n \geq 2$ line segments each having the same linewidth. The process starts by plotting the (V/I) values against the tap separation distances of the segments from which they were measured. Then by applying least squares fit a linear relation can be derived to relate the data points to one another as described in equation (4), where m is the slope of the line and b is the intercept of the line at the $L_i = 0$ axis.

$$(V/I)_i = mL_i + b \tag{4}$$

The standard equation of a line becomes apparent by re-writing equation (3) to the form seen in (5).

$$(V/I)_i = \left(\frac{Rs}{W_m}\right) L_i + \left(\frac{Rs_n}{W_m}\right)(-\delta L) \tag{5}$$

Therefore:

$$slope(m) = \left(\frac{Rs}{W_m}\right) \tag{6}$$

and

$$intercept(b) = \left(\frac{Rs}{W_m}\right)(-\delta L) \tag{7}$$

Equation (6) defines the relationship between Rs and measured linewidth while the δL term is found by dividing the intercept of the line relating the segments by the slope of the same line as seen in (7). Using the slope of the line and a measured Rs value, the linewidth can be calculated.

[3]Lateral current flow through single-level patterning means that transmission line model issues do not have to be provided for.

3) Multiple Structure Analysis: This final technique further improves upon the values and data gathered from the multiple segment approach. As will be seen in the results presented later, issues arise when using the van der Pauw structures to determine values for Rs. Sheet resistance is used as a measure of resistivity of thin films that have a uniform thickness. One issue with the current van der Pauw structures is due to the facets (as explained earlier) which present an asymmetrical geometry in the structure, and therefore the film in the crosses is not of uniform thickness. Furthermore, when CMP is used, process induced effects, present in small lines used for ECD extraction, result in variations in Rs between the van der Pauw structures and the multiple tapped bridge resistors. The most predominant of these effects is the dishing of the copper lines which can also result in nonuniformity of Rs values within a single structure. For example, the extent of the dishing of the middle of a line may vary from the dishing at the intersection between the line and the taps, hence presenting thickness variations over the length of the structure. Therefore the Rs term used in equations (2), (3) and (6) is not necessarily truly representative of the sheet resistance of the copper in the structure. As a consequence alternative means for determining Rs values need to be implemented.

This is achieved by comparing drawn linewidth against the slope values for each device, provided there are $n \geq 3$ structures. The drawn linewidths are used to provide a measure of the relation between the full set of structures without incorporating any process bias that may be present in the fabricated structures. By applying non-linear regression with a least squares fit approach, a curve described by equation (8) can be used to represent the relationship between multiple structures with different drawn linewidths.

$$m_i = \frac{a}{(W_m)_i^k} \tag{8}$$

In this equation m_i is the slope of a structure as determined from (4), a is a term primarily proportional to the sheet resistance of the measured structures, and k is proportional to the range in measured linewidth $(W_m)_i$ from the result of the regression fit. With values for a and k the linewidth for each structure can be calculated by substituting the slope of each line into (8) and solving for $(W_m)_i$.

IV. Results

A. Sheet Resistance

A contour plot can be generated to represent the sheet resistance over a complete die using data measured from a six by three array of van der Pauw structures. A typical example of one of these contour plots can be seen in Fig 4. These data display a systematic variation for the different types of van der Pauw structures within a single die. There are a number of process induced

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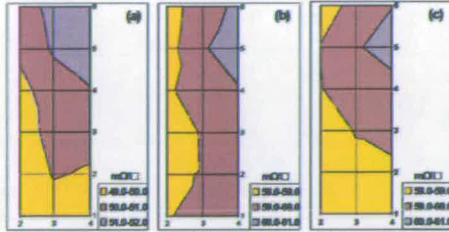

Fig. 4. Contour plot of sheet resistance over the surface of a single die taken from the van-der-Pauw structures shown in Fig. 2 : (a) Greek Cross, (b) Corner Tapped Box Cross, and (c) Side Tapped Box Cross

effects which can be used to explain this occurrence. The first is due to the dependence of the process on CMP for both nitride and copper planarization, where dishing can vary over the wafer as well as within each die. Another source is the trench depth in which the copper is deposited, which can vary in the trench etch stage of the fabrication. One important factor to note is that the mask set used to define these structures was intended for use on doped SOI substrates which would not have undergone a CMP step and therefore be more likely to have a uniform distribution of sheet resistance over a single die. For this reason, the NIST 35 design includes large (20 µm) crosses/boxes on each of the van der Pauw structures to allow for more accurate measurements of sheet resistance. However these large features pose a problem for the copper CMP stage as larger linewidths are known to dish to a greater extent than smaller linewidths [3]. This leads to the need to use smaller dimensions to reduce the dishing of the copper and provide more appropriate measurements of sheet resistance with minimal variation.

The values obtained for the sheet resistance from Greek Cross test structures are consistently lower than the other two structures. This is made apparent by an average sheet resistance of 50 mΩ/□ (implying a copper thickness of 336 nm) for the Greek Cross while the values for the corner tapped and side tapped box are both 59 mΩ/□ (implying a copper thickness of 284 nm). This suggests that the thickness varies between the Greek Cross and the other two structures by roughly 50 nm. Once more, dishing can be used to explain this occurrence. The dimensions of the arms of the Greek cross structure are the same as the body (20 µm), while both the Box Cross structures employ smaller arms for the taps (5 µm) yet maintain a 20 µm body. Because of this, the measurement from the Greek Cross structure is more likely to be influenced by dishing near to the centre of the cross than the other two structures. By observing the contour plots of sheet resistance it can be noted that, while there is a general agreement in the sheet resistance variation over the whole die, there is no specific agreed value between the three structures for each location.

B. Linewidth

Linewidths have been measured electrically, from the same six by three array as the sheet resistance measurements, to fully assess the capabilities of the current design on copper ECD extraction. Results are presented for each of the analysis approaches described in section III-B. As a means for comparison, SEM images have been used to provide a value for linewidth, which in this case is defined by the width of the copper on the surface of the wafer. While the SEM measurements do not produce results to the degree of accuracy required for CD metrology, they do provide a baseline for comparing the analysis methods. For situations where sheet resistance measurements are required to calculate linewidth, the average of estimates produced by all three van der Pauw structures for each location on the die are used. Data from the analysis methods is presented as a graph of drawn linewidth minus the extracted linewidth versus the drawn linewidth. This applies for both ECD values as well as SEM linewidth values.

1) Individual Segment Analysis: The individual segment analysis was conducted as described previously. A plot of the results gathered from the average of 5 segments of the bridge resistor using this method for the array of 18 structures is presented in Fig. 5. The error bars on the individual data points represent the range of linewidths extracted from each segment of the multiple tapped bridge resistor. These errors are proportional to the linewidth, so as the linewidth decreases the range in linewidth values also decrease. One source for the difference between the ECD values and the SEM measurements is the use of the sheet resistance structures that are physically separate from the linewidth structures and subject to dishing effects caused by locality. Furthermore, the van der Pauw structures are 20 µm wide while the linewidth structures range from 10 µm to 0.55 µm. This introduces further effects of dishing during CMP which are related to feature size.

2) Multiple Segment Analysis: Using the linear regression technique, slope values (m) were determined for each linewidth structure. By using the average measured Rs value from the van der Pauw structures in closest proximity, the linewidth was calculated using equation (6). A plot of the results using this method for all 18 structures is presented in Fig. 6. These values are in better agreement with the SEM values than those derived using the individual segment analysis. However, repeating the individual segment analysis with the δL correction makes no improvement in the present set of data.

3) Multiple Structure Analysis: Equation (8) is applied to determine the relationship between the slopes and drawn linewidths of the structures in the six by three

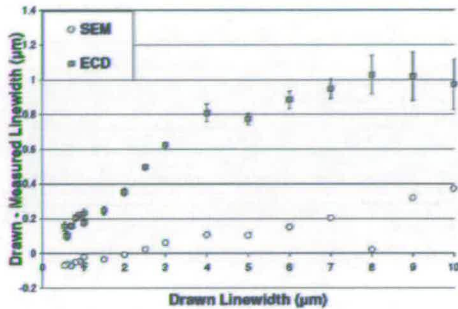

Fig. 5. Plot of drawn linewidth - measured linewidth for individual segment analysis

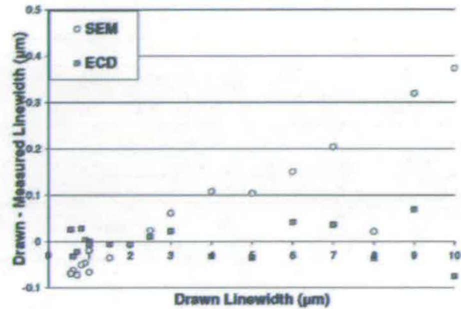

Fig. 7. Plot of drawn linewidth - measured linewidth for multiple structure analysis of separate columns

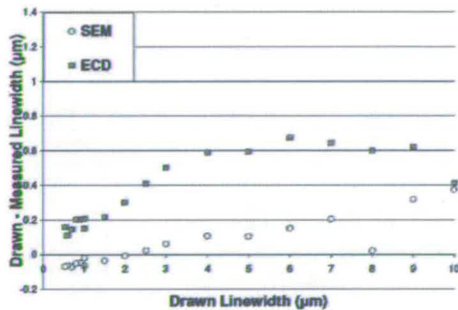

Fig. 6. Plot of drawn linewidth - measured linewidth for linear regression analysis

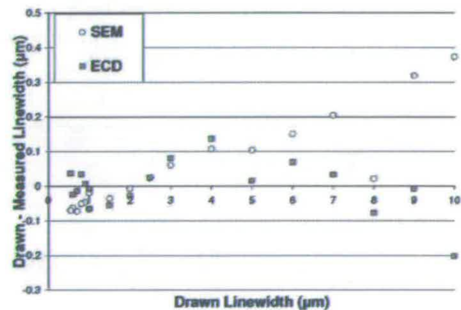

Fig. 8. Plot of drawn linewidth - measured linewidth for multiple structure analysis with all structures

array. The first approach for this technique was to analyse each column individually and plot the results. From Fig. 7 it can be seen that the values extracted for ECD measurements are in better agreement with the drawn linewidth values.

The second approach uses data from the entire array to determine the non-linear relationship and hence can be used as a smoothing for any abnormalities in individual structures. Results from this method are presented in Fig. 8. Once again these data are in agreement with the drawn linewidths, however there is a noticeably better fit to the SEM measurements.

V. Conclusions

Structures have been fabricated using a novel process to produce all-copper ECD test structures. Electrical measurements have been taken to extract various parameters and derive values for sheet resistance and linewidth. Based on data gathered from extensive electrical measurements of the copper interconnect features, issues with the current design as well as the fabrication process have been highlighted. In light of the diverse range of values for sheet resistance, the need to control the dishing of the copper and nitride has become much more critical. This can be achieved with the combination of different CMP slurries and polishing pads, as well as improvements to the process recipes. Dishing of copper lines is a well known phenomenon amongst the semiconductor community, and much work is ongoing to improve this aspect of copper CMP.

The work conducted for the purposes of this paper has highlighted an approach to analysing the data from all copper test structures which yields the best results. Future process improvements can be closely monitored to observe their effect on the extraction of ECD values. Ongoing work will involve the use of more precise CD

measurement tools to determine the linewidth of the copper interconnects and serve as calibration/reference values for more in depth analysis of the presented techniques. For the purpose of this exploratory work, g-line lithography was used to define the pattern. However more advanced technologies, such as i-line and Deep UV (DUV) lithography, can be employed to print much smaller features. Analysis of these smaller features will bring the work in line with current roadmap predictions for copper ECD values.

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2007 IEEE International Conference on Microelectronic Test Structures, March 19-22, Tokyo, Japan.

8.4

Array Based Test Structure for Optical-Electrical Overlay Calibration

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***Abstract*— The novel overlay test structure reported in this paper was purposely designed to serve as an application-specific reference material. It features standard frame-in-frame optical overlay targets embedded in electrical test features and fabricated by the same process as the parts being manufactured. Optical overlay is commonly used in process control applications due to its utility for determining the relative positions of features patterned in photoresist. Electrical overlay, although it can only be measured on fully patterned test structures, is the metric of interest. Using this combined optical/electrical overlay test structure, we can derive the relationship between the routinely measured optical overlay and the electrical overlay for any specific combination of process and optical overlay tool.**

I. Introduction

An important function of manufacturing process control is assuring lateral geometrical superposition of a new additional layer onto an existing layer of patterned material on a partially fabricated wafer to within engineering-design specifications [2]. An important example is correct lateral superposition of vias in the M1-M2 (metal 1 to metal 2) inter-level dielectric relative to M1 patterned features. In this and other stages of wafer fabrication, the term overlay quantifies the degree of superposition. It is a vector which is parallel to the wafer surface and is defined at every location on a composite pattern of two layers. The magnitudes of its two components are measures of the relative lateral locations of features of the second layer with respect to corresponding ones of the first layer. The ideal value of both components of the overlay vector is zero. During wafer manufacture, the overlay at one or more locations on one or more die sites is sampled to confirm that it is within specification. The sampling is applied to the overlay between the patterned first layer and, either the developed resist of the second layer or, actual features of the second layer after completion of patterning. The test structures described in this paper apply to the second case, but their implementation can deal also with the first case. In both cases, overlay information is extracted by optical inspection with a highly specialized optical microscope, commonly known as an overlay tool. Such tools obtain local overlay values by capturing the image of a dedicated target structure, which is replicated on a die site specifically and exclusively to facilitate overlay metrology. A common target has the so-called frame-in-frame architecture shown in Fig. 1(a), which exemplifies the overlay-vector components. The key property of the target is that the outer frame is patterned in one layer and the inner frame is patterned in the material of the other. The analysis of its image, as collected by the overlay tool, is performed by well-established image-processing techniques and is rapid and economic.

The problem that this paper addresses is that the values of overlay obtained using optical means can be affected by two types of error. The first type is tool-induced shift (TIS). This factor often originates in misalignment of the optical axis of the overlay tool. The second is wafer-induced shift (WIS) which originates in any geometrical asymmetries; for example asymmetry in the vertical profiles of contact vias. The outcome is that the result of the frame-in-frame measurement typically includes elements due to either, or more likely both, TIS and/or WIS. Thus the reported optical overlay value

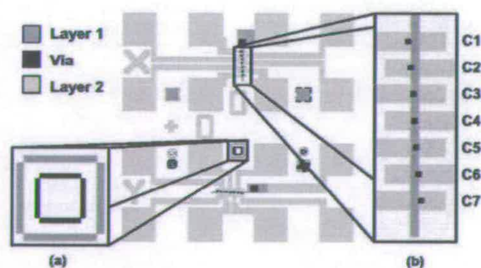

Fig. 1. Layout of single test cell of the NIST47 design with (a) frame-in-frame structure and (b) diagonal arrangement of contacts.

[1]Official contribution of the National Institute of Standards and Technology; not subject to copyright in the United States of America.

[2]Subsequently we use the term first layer to refer to the uppermost existing layer and an additional layer is referred to as the second one.

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generally differs by an unknown amount from a value based on optimum geometrical (and hence electrical) integrity of the conductor-via contact. We refer to the latter value as the electrical overlay. In this paper we report on a technique to determine this unknown difference. Please note that this new test structure is not designed to replace the optical overlay test structure in routine applications. This is because the box-in-box is typically applied after imaging the photoresist of the upper conductive layer. If the box-in-box shows the overlay to be out of specification, the photoresist can be removed and repatterned; if the process were continued to the point at which electrical metrology could be applied, identification of overlay errors is beyond the point at which rework could allow the salvage of the wafer.

II. Design

For demonstrating the technique, a test chip (NIST 47) has been designed [1], [2]. It consists of a regular array of similar cells that can be implemented in a three-level short-loop process . The three levels in this application are a lower conductor, a via, and an upper conductor. In this case we used a traditional metal 1 to dielectric-via to metal 2 interconnect process. Each test cell, one of which is shown in Fig. 1, has separate elements to determine the X and Y components of the local overlay of the dielectric-via level to the first metal level by electrical means as discussed below. Each of the two elements has a reference feature which is replicated in the first metal level (this is the vertical feature in the detail box in Fig 1(b)). At the completion of the fabrication, this reference feature is nominally connected to a metal 2 test pad through a group of vias as shown schematically in Fig. 1. Seven vias through the M1-M2 inter-level dielectric layer are regularly distributed along a line inclined to, and intersecting, the reference line. It is key at this point to remind the reader that the overlay is determined in this implementation of the test structure only between the first metal and the via layer. The second metal serves only to distribute the desired electrical signals to the pads.

The via pitch (p) is the component of the drawn lateral separation of adjacent vias in a direction perpendicular to the reference line, as shown in Fig 2(a). In the design used in this experiment, the pitch between adjacent vias is 0.5 µm or 1.0 µm, with the pitch between the end vias totaling 5.0 µm. In each element of the test cell, the as-fabricated mis-registration of a particular via is its center-to-center perpendicular distance from the reference line as shown in Fig. 2(b). It is equal to its as-drawn lateral displacement from the reference line plus the as-fabricated misalignment of the cell. The misalignment of the cell is the cell's programmed offset plus the overlay with which the test structure is fabricated. All cells of the test structure are fabricated with the same overlay but are replicated with their own programmed (drawn) offsets.

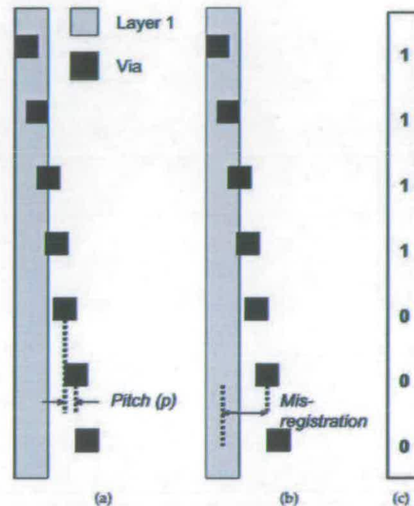


Fig. 2. Illustration of (a) pitch and (b) mis-registration of contact vias with (c) corresponding binary signature.

Electrical contact to the filled vias, some of which may be in contact, or in partial contact, with the M1 reference line, is provided by their connection to test pads on the M2 level as illustrated in Fig 1. This arrangement enables electrical continuity to be sensed between the reference line patterned on the M1 level and the contacts connected to the test pads on the M2 level. The results are recorded in binary format where a 1 represents electrical continuity and a 0 represents an electrical open. In principle, the misalignment of a cell can be determined to within a resolution of the via pitch p from the binary continuity signature (Fig. 2(c)) of the cell in a manner similar to that reported for vernier type structures [3]–[7].

Within each test cell is also a standard frame-in-frame optical overlay target. The placement of its features matches the as-fabricated misalignment of the cell, which is the cell's programmed offset plus the overlay with which the test structure is fabricated. The cell misalignment is measured optically using the same tool that is to be calibrated. In the test structure, which is a regular array of 287 cells, each cell has its own programmed offset which is a multiple of 10 nm. The complete test structure, shown in Fig. 3, enables the cross comparison of optical and electrical overlay between -1.43 µm and 1.43 µm in both the X and Y directions in steps of 10 nm for the purpose of application-specific calibration-curve

construction.

In the test structure design reported here, each cell is systematically placed in an ordered row and column format for simplifying analysis. However, the arrangement is such that the cells are effectively randomized across the complete test structure in both the X and Y directions. This ensures that any systematic change in overlay, for example increasing from left to right across the complete structure does not show up as an offset. Each column contains 16 cells, where the individual cells have sequential programmed offsets of 10 nm ordered such that the programmed offsets decrease from the top to the centre of the column in odd-number multiples of 10 nm. The programmed offsets similarly decrease in even-number multiples of 10 nm from the bottom to the centre of the column. The columns are arranged such that the leftmost column contains the set of cells offset in the extreme negative direction, while the rightmost column contain those in the extreme positive direction. Progressing towards the centre of the die sees the offset values alternate in direction (positive and negative axis) whilst decreasing in value.

III. Fabrication Overview

In order to demonstrate the design, a traditional two layer metal process fabricated on bulk silicon wafers was implemented. The wafers first undergo a thermal oxidation to provide electrical isolation from the substrate. Then a thin layer of aluminium is deposited and patterned with the M1 reference line of the electrical structure along with the external frame of the optical structure. Following this a dielectric layer of silicon

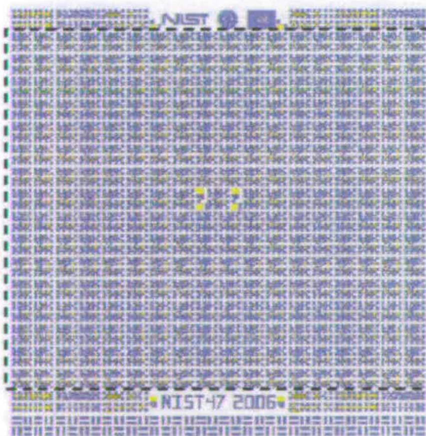


Fig. 3. Layout of entire chip for NIST 47 design; the test structure described in this paper is the 16 by 18 array of cells indicated.

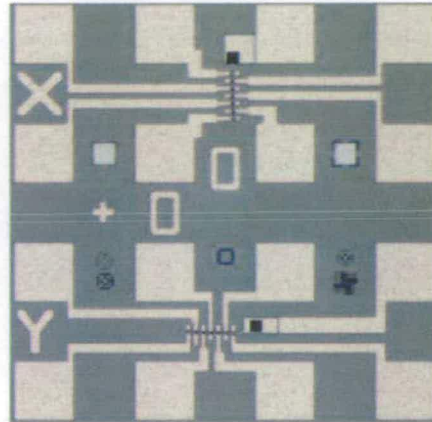


Fig. 4. Image of the as fabricated cell with zero programmed offset.

dioxide (SiO_2) is deposited over the surface of the wafer using plasma enhanced chemical vapour deposition (PECVD). The contacts, as well as the inner frame of the optical structure, are then patterned and etched into the dielectric layer until M1 is exposed under each via. Finally M2 is deposited and patterned providing the probe pads and interconnect necessary for electrical measurements. An image of one of the patterned cells is shown in Fig. 4.

Though this design is demonstrated with aluminium, it can be implemented with other interconnect materials such as copper.

IV. Results

Complete arrays of 287 cells were measured electrically to determine the resistance between the reference line and the 7 contacts shown in Fig. 1. Electrical measurements used a standard resistance meter, as a means for determining continuity, along with a probe station and probe card fixtures to make physical contact with the probe pads. The frame-in-frame structures have also been measured using a SEM to compare with the electrical results. Table I shows some selected data extracted from the central structure along with the corresponding binary equivalents. The binary values are determined by setting a threshold resistance, where values greater than the threshold are classed as a "0" (open) and a "1" (short) for those below the threshold. As the difference between contacts that are conducting and those that are not is so large, a threshold of 1 kΩ is used for all measurements. The results presented in Table I indicate that the via with a pitch of 2.0 μm (C7) does not make contact and is misaligned positively with respect to the M1 reference

TABLE I

SELECTED R VALUES FROM ELECTRICAL OVERLAY STRUCTURE AND CORRESPONDING BINARY REPRESENTATIONS.

	Contact						
	C1	C2	C3	C4	C5	C6	C7
Programed Offset (μm)	-2.5	-1.5	-0.5	0	0.5	1.5	2.5
Weight Multiple (μm)	0.5	1.0	0.5	0	0.5	1.0	0.5
Resistance ($k\Omega$)	0.01	0.0092	0.0087	0.013	0.0095	0.011	17050
Binary	1	1	1	1	1	1	0

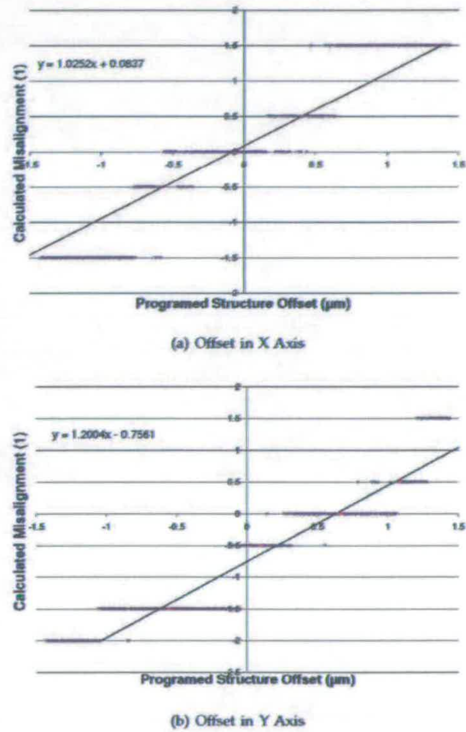
line. In order to represent the misalignment of each cell, the binary signature is weighted and summed together using equation (1), where C1 to C7 are the individual bits of the binary string.

$$((C5 \times 0.5) + (C6) + (C7 \times 0.5)) - ((C1 \times 0.5) + (C2) + (C3 \times 0.5)) \quad (1)$$

The weight multiples are determined such that the resulting calculated misalignment value provides a rough measure of the overlay for each cell. The whole test structure combines these values to provide a much better measure of overlay. The actual weight multiples employed for each via are provided in Table I. With the weighted sums for each contact calculated the leftmost 3 contacts (C1, C2, C3) are subtracted from the rightmost 3 contacts(C5, C6, C7), ignoring the centre contact as it has a 0 relative centre-to-centre distance from the reference line. The resulting value corresponds to the alignment of the contacts with respect to the centre of the reference line.

A plot of the derived values for the complete array of 287 structures, for both X and Y axis, on a single chip as determined by equation (1) is presented in Fig. 5. The electrical overlay value is then extracted from this data by calculating the median overlay value for the entire data set. For example, referring to Fig. 5(a), the set of data which lies on the calculated misalignment value of 0.5 ranges in programmed offset from 0.17 µm to 0.63 µm making the centre lie at 0.4 µm. This process is repeated for the remaining sets of data, in this case the 0 and -0.5 calculated misalignment sets. (Note: As the two data sets which extend to the limits of the programmed offset, both positive and negative, may contain data beyond those points, these sets can not be used in the calculation. In this case the ± 1.5 data sets) Linear regression is then used to determine the best fit of a line connecting the median points for the data ranging from -1.43 µm to 1.43 µm programed offset. Using the equation for the line relating the median points, the Y=0 intercept of this line provides a value for that particular chip's overlay in the X direction. The same process is then repeated for the data representing the Y axis.

Using this particular set of data a value of -81.6 nm was calculated for the overlay in X. To provide measurement assurance, SEM images (Fig. 6(a)) were taken of the frame in frame structure and measured to determine the overlay error from the optical structures. These measurements are conducted by extracting an intensity profile of the frame in frame structures along a perpendicular axis to the lines for each direction. An example of one of these profiles as used for the X direction is displayed in Fig. 6(b). With this intensity profile, the alignment can



(a) Offset in X Axis

(b) Offset in Y Axis

Fig. 5. Plot of misalignment measurements calculated using equation (1) vs programmed structure offset for single die.

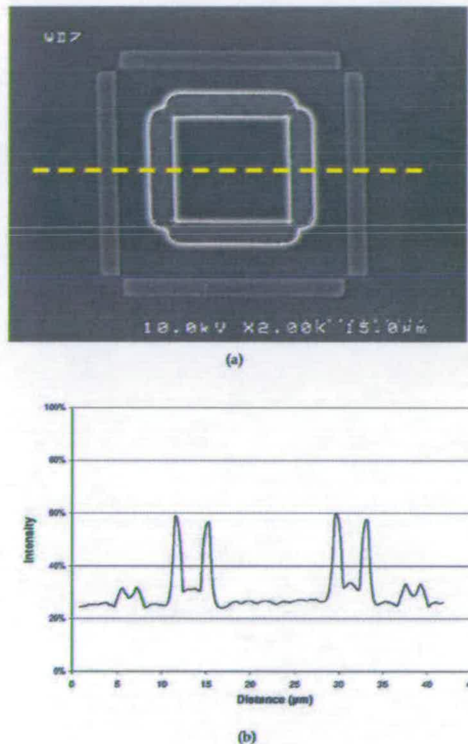


Fig. 6. Optical structure used for determining overlay. (a) SEM of frame in frame structure showing location of intensity profile. (b) Extracted intensity profile from above structure.

be determined by calculating the differences between the inner and outer frames, represented by the outer pair (for the outer frame) and inner pair (for the inner frame) of profiles in the intensity plot. The result of this measurement yielded a value of -80.6 nm, thereby demonstrating the functionality of this test structure.

Repeating this method for analysis of the data for the Y direction gives an electrically extracted overlay value of 629.8 nm, while the SEM intensity profile extracts the overlay as 638.4 nm. It can be observed that the values for the Y alignment differ by 9 nm. One possible explanation for this could be due to uncertainty in the measurements which result from non-uniformities in the processing. For example, if there is any fluctuation in via size caused by non-uniformity in the etch process, the cells will obviously produce different measurements depending on their location.

One observation from comparing Fig. 5(a) and Fig. 5(b) is that the slopes of the lines relating the median points differ slightly. The precise cause for this is currently being investigated.

V. Conclusions

A test structure for measuring overlay in interconnect systems has been presented which provides the necessary measurements to serve as an application-specific reference material. By incorporating a hybrid design approach, electrical structures are used to calibrate measurements taken from commercially available optical overlay tools. This is achieved by embedding optical frame-in-frame structures along side electrically testable overlay structures. This provides a straightforward method to relate optical overlay measurements with functionally relevant electrical overlay values. The NIST 47 design incorporates a large array of 287 test cells with an offset in increments of 10 nm that are used to determine overlay. An important aspect of this design is that as a standard 2 layer process is used, it is able to be fabricated by the same process as the parts being manufactured. Also, as the necessary electrical measurements are simply continuity measurements, readily available measurement tools can be used to electrically determine the overlay.

Electrical and SEM measurements have been compared and are in good agreement, providing overlay readings agreeing to within 1 nm in the X direction and 9 nm in the Y. Improving the process uniformity when fabricating these devices should help to produce much more accurate results in the future. Another source of error in this process, as with other processes utilizing lithography to define structures, is the registration of the features used in the patterning of the structures. The specific mask set used for these structures is reported to have a feature registration tolerance of ± 12 nm wafer level (based on ± 60 nm reticle tolerance using a 5x stepper for lithography).

VI. Acknowledgements

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A.4 Frontiers of Characterization and Metrology for Nanoelectronics (Gaithersburg, Maryland, 2007) [In Press]

CD Reference Materials Fabricated on Monolithic 200 mm Wafers for Automated Metrology Tool Applications[1]

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Abstract. Recently, prototype isolated-line, single-crystal critical dimension (CD) reference materials (SCCDRMs) with linewidths as narrow as 40 nm ± 1.5 nm have been reported. These reference materials, designated NIST Prototype Reference Material (RM) 8111, were configured as 10 mm by 11 mm silicon test chips mounted in 200 mm carrier wafers. The RM 8111 chips were fabricated using microelectromechanical (MEMS) process techniques, which assure the alignment of the sidewalls of the features to silicon (111) lattice planes, and were calibrated in a sequence involving atomic force microscopy (AFM) and high resolution transmission electron microscopy (HRTEM) metrology. This paper reports initial results on SCCDRMs fabricated on 200 mm bulk wafers; this monolithic approach would eliminate the need for carrier wafers.

Keywords: Metrology, Linewidth, Critical Dimension (CD), Reference Material (RM), Optical Critical Dimension (OCD), Scatterometry.
PACS: 61.46.-w

INTRODUCTION

In response to requests from the semiconductor industry, prototype isolated-line, single-crystal CD reference materials (SCCDRMs) with linewidths as narrow as 40 nm ± 1.5 nm (expanded uncertainty) were developed at the National Institute of Standards and Technology.[1,2] These reference materials, designated RM 8111, met the requirements for the 40 nm technology node (2011) specified in the *2006 International Technology Roadmap for Semiconductors* (ITRS).[3] In this paper we describe our research to respond to requests from industrial users of RM 8111 to provide the capabilities of RM 8111 in a different form.

RM 8111 was delivered with six features ranging from 40 nm to 250 nm to allow for use at a range of magnifications. Figure 1 is a sample of a calibration curve constructed from measurements made on two of these SCCDRMs with calibrated widths ranging from 40 nm to 250 nm.

Each of these reference materials was configured as a 10 mm by 11 mm silicon test chip mounted in a 200 mm carrier wafer. The carrier wafer was used to allow these SCCDRMs to be utilized in metrology tools that can only accept 200 mm wafers.

These prototype SCCDRMs were fabricated on (110) SIMOX (Separation by IMplantation of OXygen) wafers using the anisotropic wet etch techniques common to MEMS processes. Appropriate orientation of the lithography assures the alignment of the sidewalls of the features to silicon (111) lattice planes and allows for the AFM-HRTEM calibration procedure.[4]

[1] Official contribution of the National Institute of Standards and Technology; not subject to copyright in the United States of America

Through chemistry improvements, and closer process control, a selection of features, with linewidths as low as 20 nm, have now been fabricated. They are anticipated to exhibit expanded uncertainties on the order of 1 nm. This extraordinary result is being achieved through formally designed experiments to identify factors that optimize reference-feature etching chemistry.[5]

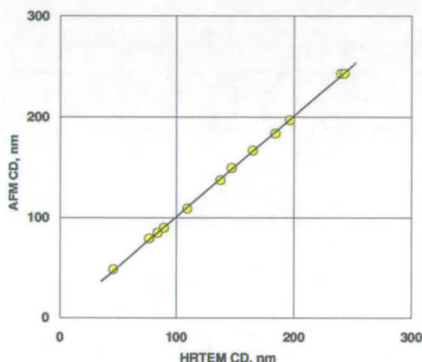

FIGURE 1. Calibration curve from recent release of prototype SCCDRMs.

Even in light of these recent improvements in linewidth and uncertainty, many in the end-user community have made it clear that the biggest enhancement that is now required is a monolithic implementation to replace the carrier-wafer assembly of individual chips. This is a major challenge because, although 200-mm wafers are considered acceptable by end users, silicon-on-insulator (SOI) having the necessary (110) orientation is unavailable in quantities commensurate with requirements. This paper thus reports progress towards fabricating a monolithic version of the CD reference materials on boron-implanted bulk (110) material. This implementation also offers a beneficial side effect over SIMOX and other SOI materials; since its features are conductive, they are much less subject to charging and hydrocarbon contamination under scanning electron microscope (SEM) inspection.

TEST STRUCTURE PROCESSING PROCEDURE

Three NIST wafers were patterned with the design NIST45A. NIST 45A is a modification of the NIST45[1] design used on RM 8111 with the following minor changes:

- Rotation of the elements of the test chip design so that the sidewalls of the feature align to the (111) planes on the 200 mm wafers
- Adjustments to allow patterning on the Nikon[2] Body 9, i-line, 0.57 NA, (8"), 5X reduction stepper with 0.45 micron resolution over a 2.2 cm square field by a lithography tool at the Scottish Microelectronics Centre at the University of Edinburgh.

Note that the first of these was required since the original NIST45 was patterned in 150 mm (110) silicon. On the 150 mm wafers, one of the (111) family of planes is parallel to a flat. In contrast, there is no flat on the 200 mm wafers; rather there is a notch. The notch is centered between the two families of (111) planes. The easiest way to understand this is to consider a v-shaped notch, with a 70.529° angle between the sides. The two families of (111) planes perpendicular to the (110) surface are parallel to the edges of the "v".

In addition, since the family of (111) planes is symmetrical relative to the notch, there is no longer the need for separate "11:00" and "1:00" designs.[1]

After patterning, one of the wafers was diced for process evaluation. Two of the chips were processed using the process flow previously optimized for use with SIMOX wafers.[5] This process was chosen as the baseline since it provided the best edge uniformity for processing the SIMOX chips.

- Acetone rinse to remove the photoresist
- Isopropyl Alcohol (IPA) rinse to remove the acetone residue
- Buffered oxide etch (BOE) for 12 s to pre-thin the hard mask
- 12 ½% Potassium Hydroxide (KOH) at 80 °C with ultrasonic agitation:
    - Chip 1: 10 s
    - Chip 2: 25 s
- BOE (20 s) for hard-mask strip.

After completion of the process, the chips were imaged by optical microscopy (Figure 2) and by SEM. The images showed the lines to have successfully patterned with provisionally acceptable uniformity. However, one concern was the surface of the field region. The KOH etch left the field region pitted and non-uniform. Since the tops of the features, as well as

[2] Certain commercial equipment is identified in this paper to describe the experimental procedure adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology or the University of Edinburgh, nor does it imply that the equipment identified is necessarily the best available for the purpose.

the surface of etched region, are bulk material, the primary contrast between the two is due to the non-uniform surface in the field region.

FIGURE 2. 16 μm segment of SCCDRM fabricated in bulk silicon on 200 mm wafer.

AFM CD MEASUREMENTS AND DATA ANALYSIS

Selected features from these two initial chips, including the one shown in the optical micrograph in Figure 2, were measured for CD and line uniformity using a CD-AFM (atomic force microscope) at NIST for which traceability and uncertainty budgets have been established.[6] The central 2.0 μm region of the 16 μm structure was measured. Figure 3 shows an example of the results of this measurement.

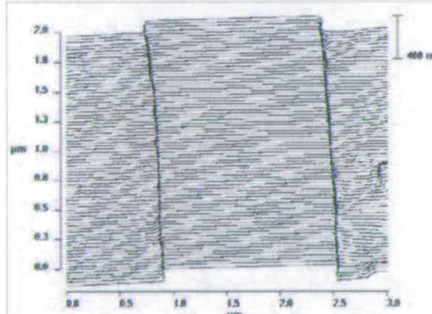

FIGURE 3. AFM scan of central region of 16 μm feature shown in Figure 2.

The first step in the analysis of the AFM data to determine the typical uncertainty of the CDs for these features was to fit a smoothing spline model[7] to the data. The smoothing spline model is a non-parametric regression model that allows us to separate the deterministic structure in the data as a function of position along the line from the noise, without having to assume a specific functional form for the relationship between CD and position. The data from one of the reference features studied as part of this work with a smoothing-spline fit through the points are shown in Figure 4.

Next a region in the center of the line of approximately 0.5 μm in length was identified as the portion of the line over which the non-uniformity of the CD would be determined. This length, which can be tailored to match different levels of navigational capability when the reference feature is used, was chosen to match the lengths used in the earlier development, calibration, and optimization of these types of reference features in single-crystal silicon[1] to facilitate comparisons between the different materials. The portion of the spline fit in the target region is surrounded by a box in Figure 4 to differentiate the target area. The approximate CD over the target length of line was then estimated using the mean of the predicted values from the smoothing spline model at the positions along the line where data was taken.

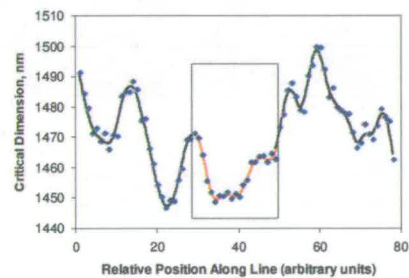

FIGURE 4. A smoothing spline model fit to AFM data on the CD of a reference line fabricated in bulk Si as a function of the position along the line.

The standard uncertainty in the CD due to non-uniformity of the reference feature was determined by a Type B evaluation[8,9] with assumption of a triangular probability distribution over the range of CD values over the target area of the line, as shown in Figure 5. Under this model, which is a simplified version of the uncertainty assessment used in the development of similar reference features using single-crystal silicon[1], the standard uncertainty due to the non-uniformity of the reference feature is given by $u_n = r_n/(2/\sqrt{6})$, where u_n is the standard uncertainty due to reference

feature non-uniformity and r_n is the range of the non-uniformity. By using this approach, the standard uncertainties due to non-uniformity for the reference features shown in Figures 4 and 5 were determined to be $u_n = 4.4$ nm and $u_n = 3.7$ nm, respectively.

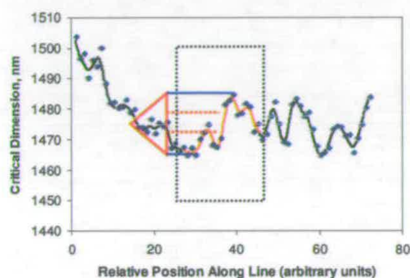

FIGURE 5. Illustration of triangular probability distribution used to obtain standard uncertainty due to feature non-uniformity.

To compare the uncertainties for the bulk Si reference features being reported here with our previously developed materials, a lower bound on the expanded uncertainty of the CDs determined for these two features were also determined. This was done by first determining a lower bound on the combined standard uncertainty, u_c for each feature and then computing an expanded uncertainty, U, from the formula $U = ku_c$, where k is a coverage factor used to control the approximate level of confidence associated with the expanded uncertainty. The sources of uncertainty included in the combined standard uncertainty, in addition to the standard uncertainty due to non-uniformity, were the standard uncertainty for the reproducibility of the AFM measurements (0.5 nm) and the standard uncertainty for the correction of the AFM offset (0.29 nm). To compute the expanded uncertainty, a coverage factor of $k = 2$ was used which corresponds to an approximate confidence level of 95 %. Some other minor potential sources of uncertainty from the estimation of the CD were not included, and so the results obtained from these computations are lower bounds for the expanded uncertainties for the CDs for each feature, which were $U \geq 8.8$ nm and $U \geq 7.5$ nm, respectively.

CONCLUSIONS

In this paper we have described work to extend the successful NIST Prototype Reference Material RM 8111 to a monolithic implementation to meet the needs of the semiconductor industry. The initial results presented here are promising, but do not yet meet the uniformity and dimension requirements achieved in RM 8111. One potential advantage of using bulk silicon is that the feature height is no longer limited to the depth of the SIMOX device layer – typically 150 nm for SIMOX – but is completely a function of etch time. In this example, the KOH etch provided features 130 nm deep and 550 nm deep for 10 s and 25 s etches, respectively.

The initial results of patterning prototype SCCDRMs on 200 mm bulk silicon wafers have shown promise. However, it appears that we will not be able to use the optimized SIMOX process to reach our width and uniformity goals; rather, a new process must be developed.

These data do not yet show that the bulk material is capable of providing the same level of sidewall flatness and CD uniformity that are responsible for the previously achieved CDs of about 50 nm ± 2 nm observed for SCCDRMs fabricated in SOI material.

This work highlights an issue that may need to be addressed before acceptance of bulk silicon SCCRMs. This issue is the condition of the field area. Although the surface roughness of the field area does not affect the uniformity of either the top surface of the features or, more importantly, the sidewalls, its presence may serve to inhibit acceptance of such reference materials.

In future work, we plan to continue a two-prong development of monolithic SCCDRM on 200 mm wafers, continuing to investigate bulk silicon as well as continuing to procure 200 mm SOI wafers.

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Appendix B
Process Equipment

This appendix details the process equipment in the context in which they are used throughout the fabrication of devices for this thesis. All equipment is held at the Scottish Microelectronics Centre, University of Edinburgh.

B.1 Fabrication

Process	Tool	Details
Aluminium etch	Surface Technology Systems Multiplex RIE Etcher	Able to etch using chlorine based chemistries on wafers from 3 to 8 inches in diameter
CMP	Presi Mecapol E460 CMP tool	Allows the chemical-mechanical polishing of whole wafers from 3 to 8 inch diameter. Able to polish a wide range of materials including silicon nitride, silicon dioxide, copper, aluminium, etc...
Copper electroplating	SMC platting tool	Custom made unit capable of plating copper films for sample sizes up to 8 inch in diameter
Dielectric etch	Plasma therm PK2440 RIE tool	Capable of etching silicon nitride and silicon dioxide on 3 inch wafers
Post CMP clean	Ultratech plate cleaner	Uses high pressure DI water to clean particles from surfaces of mask reticles and wafers up to 4 inches
PECVD Si_xN_y	Surface Technology Systems PECVD system	Uses plasma enhanced chemical vapour deposition of silicon dioxide and silicon nitride films at ~300°C
Photolithography (mask aligner)	Karl Suss Mask Aligner MA8	1:1 Proximity/contact printing of 3 to 8 inch wafers using an i-line source
Photolithography (stepper)	Optimetrix 5x wafer stepper	G-line image reduction stepper to image patterns onto 3 to 6 inch wafers using 5 inch mask reticles

Continued on next page

Process	Tool	Details
Photoresist (standard)	Silicon Valley Group 3 inch track coater	Automated track system for 3 inch wafer processing including all steps involved in photoresist coat and develop after exposure
Photoresist (thick film)	Semiconductor Production Systems APT-Polos MCD200-NPP	Manual spin coat system for 3 to 8 inch wafers
Photoresist baking (thick film)	Electronic MicroSystems Hot plate	8 inch wafer hot plate with programmable temperature and time
Photoresist strip	Electrotech Barrel Asher	Uses an oxygen plasma to remove standard photoresist films from wafers up to 8 inches in diameter
LPCVD Si_3N_4	Tempress LPCVD furnace tube #2	Horizontal furnace for 3 to 8 inch wafers. Uses low pressure chemical vapour deposition techniques and accommodates the deposition of Stoichiometric as well as low stress silicon nitride films
SF_6 etch	Vacutech RIE etcher	Research tool with SF_6 etch chemistry for 3 and 4 inch wafers
Thermal oxidation	Tempress furnace tube #10	Horizontal furnace for 3 inch wafers. Accommodates Dry and Wet oxidation processes
Wafer dicing	DISCO wafer saw	Able to dice wafers up to 8 inches in diameter
XeF_2 etch	Point 35 Microstructures MEMSTAR vapour etch tool	Uses solid crystal XeF_2 to vapour etch silicon and poly-silicon films

B.2 Physical metrology

Process	Tool	Details
AFM	Digital Instruments D5000 Atomic Force Microscope	High resolution surface profilometer. It can be used up to scan sizes of 70 x 70 μm and can be used in Tapping Mode and Contact Mode.
Cross section preparation and imaging	FEI FIB 200xP	Focused Ion Beam system allowing cutting of most semiconductor materials for cross section imaging on up to 1 inch sample sizes
Dielectric film thickness	Nanospec 3000 spectroscopic reflectometer	Measures the thickness of optically transparent films usually deposited on silicon substrates.
Line width and cross section imaging	Hitachi S4500 SEM	Scanning electron microscopy of samples up to 3 inches in diameter. Allows cross sectional images with tilting stage on cleaved samples.
Surface Profilometry	Veeco Dektak 8000 Profilometer	Capable of measuring step height, surface roughness, and wafer curvature for stress calculation
Wafer inspection and optical imaging	Reichert Jung Polyvar Microscope	For inspection of wafers during and post-process with magnification up to 2000 times. Allows image capture with digital camera.

B.3 Electrical test

Process	Tool	Details
DC Parametric System (Automated)	HP 4062B	Rack mounted parametric test system consisting of switching matrix, C-V meter, and Current source-meter
DC Parametric System (Manual)	HP 4156B	Self contained parametric test system with integrated source measure units (SMU)
Manual probe station	Wentworth 6200A	Uses manual movement of wafer stage and micromanipulators for electrical contact to probe pads
Precession voltmeter	Solartron 7065 Microprocessor Voltmeter	Measures voltage and resistance with a sensitivity of 1 μV on a range of $\pm$10 mV.
Semi-automatic probe station	Teledyne TAC PR-53	Allows programming of pitch to step between test structures using a probe card to make electrical contact

Appendix C
Run Sheets

This appendix details the process steps involved in the fabrication of the structures reported in this thesis. They are provided to allow researchers the ability to conduct the reported experiments and pursue future work.

C.1 Fabrication of optical-electrical overlay calibration test structures

Run Sheet

Author: Byron Shulver **Batch number:** **Mask set ID: NIST 47**

Product: Optical-Electrical Overlay Reference Material **Quantity:**

Starting material: (100) Si 3" wafers 381 μm **Date:**

General: carefully inspect the product after each process step before proceeding to the next one.

Step	Process	Tool	Process details	Comments
1.	Substrate isolation	Tempress furnace 10	WETOX14 Time: 00:40:00	500 nm
2.	Al deposition	OPT Plasmalab 400	1 KW DC Time: 00:45:00	0.25 μm
3.	Resist coat	SVG 8500 3" coat track	Program: 1,1,1 Resist: SPR-2	1.15 μm
4.	Align and expose pattern	Optimetrix 5X stepper	Mask Ref: NIST47_metal1 Program: nst-4701	
5.	Develop	SVG 8500 3" develop track	Program: 1,1,1 Developer: MF26a	
6.	Etch Al	STS Aluminium RIE	Program: AL3IN Time: 00:03:00	
7.	Resist strip	Electrotech barrel asher	Time: 00:60:00 standard conditions	
8.	Deposit ILD	STS PECVD	HFSIO Time: 00:17:00	0.5 μm SiO_2
9.	Resist coat	SVG 8500 3" coat track	Program: 1,1,1 Resist: SPR-2	1.15 μm
10.	Align and expose pattern	Optimetrix 5X stepper	Mask Ref: NIST47_contact Program: nst-4702	Align to metal1
11.	Develop	SVG 8500 3" develop track	Program: 1,1,1 Developer: MF26a	
12.	Etch vias	Plasmatherm PK220	10 sccm H_2 & 60 sccm CF_4 Power: 750 W Time: 00:45:00	Long etch required to clear the small contacts
13.	Resist strip	Electrotech barrel asher	Time: 00:60:00 standard conditions	
14.	Deposit Al	OPT Plasmalab 400	1 KW DC Time: 03:00:00	1 μm
15.	Resist coat	SVG 8500 3" coat track	Program: 1,1,1 Resist: SPR-2	1.15 μm
16.	Align and expose pattern	Optimetrix 5X stepper	Mask Ref: NIST47_metal2 Program: nst-4701	Align to contacts
17.	Develop	SVG 8500 3" develop track	Program: 1,1,1 Developer: MF26a	
18.	Etch Al	STS Aluminium RIE	Program: AL3IN Time: 00:03:00	
19.	Resist strip	Electrotech barrel asher	Time: 00:60:00 standard conditions	
20.	Dice	Disco wafer saw		

C.2 Fabrication of all-copper ECD test structures

Run Sheet

Author: Byron Shulver **Batch number:** **Mask set ID: NIST 35**

Product: Copper ECD Reference Material **Quantity:**

Starting material: (110) Si 3" wafers 381 μm **Date:**

General: carefully inspect the product after each process step before proceeding to the next one.

Step	Process	Tool	Process details	Comments
1.	Grow hard mask	Tempress furnace 10	Program: WETOX11 Time: 01:00:00	200 nm
2.	Resist coat	SVG 8500 3" coat track	Program: 1,3,1 Resist: SPR-2	1.15 μm
3.	Align and expose pattern	Optimetrix 5X stepper	Mask Ref: NIST35d Program: nst-3504	Align to flat
4.	Develop	SVG 8500 3" develop track	Program: 1,1,1 Developer: MF26a	
5.	Etch hard mask	Plasmatherm	Recipe: 10 sccm H_2 60sccm CF_4 Time: 00:25:00	
6.	Resist strip	Electrotech barrel asher	Time: 00:60:00 standard conditions	
7.	Etch silicon preforms	TMAH	25 wt% @ 50°C Time: 00:07:00	Based on 0.15 μm min^{-1}
8.	Remove hard mask	Wet deck	4:1 Buffered HF *(40% NH_4F : 48% HF)*	Etch till clear
9.	Nitride mould 1	Furnace 3 LPCVD	500nm Si_3N_4 Time: 08:00:00	
10.	Nitride mould 2	STS PECVD	Recipe: LFSIN Time: 00:20:00 @ 60 W	1.0 μm
11.	SiN planarise	PRESI CMP	Bulk process: See recipe "SiN CMP bulk process" below Slow removal: See recipe "SiN CMP Soft landing" below	Remove SiN covering silicon preform
12.	Remove native oxide	Wet deck	1% HF in DI water Time: 00:00:30	Transfer to vapour etch immediately
13.	Trench etch 1	MEMSTAR vapour etch tool	XeF_2 Vapour etch to determine etch rate Time: 00:00:10 Conditions: 10 sccm He -> XeF_2, 1000 sccm He -> process gas Constant pumping 100%	
14.	Trench etch 2	MEMSTAR vapour etch tool	XeF_2 Vapour etch remaining height using etch rate from step 1	Target 300 nm trench depth
15.	Clean wafer	Electrotech barrel asher	Time: 00:60:00 standard conditions	
16.	Trench isolation	Furnace 10	WETOX08 Time: 00:30:00	
17.	Cu deposition	OPT Plasmalab 400	1KW DC with 300W RF Bias Time: 03:00:00	

18.	Cu planarise	PRESI	Bulk process: See recipe "Cu CMP bulk process" below Slow removal: See recipe "Cu CMP soft landing" below	
19.	Post CMP clean	Ultratech plate cleaner	Time: 00:03:00 - clean Time: 00:03:00 - dry	
20.	Passivation	SCS Parylene tool	100nm Parylene	As per "weight vs. thickness" calculations
21.	Dice	Disco wafer saw		

SiN CMP bulk process	Stage 1	Stage 2	Stage 3	Stage 4
Slurry	Klebosol 30HB50	Klebosol 30HB50	DI water with 1% TMAH	DI water
Slurry feed rate	75 mL min^{-1}	75 mL min^{-1}	150 mL min^{-1}	-
Pad rotation	40 rpm	60 rpm	40 rpm	2 rpm
Holder rotation	40 rpm	60 rpm	40 rpm	2 rpm
Back pressure	-	0.20 bar	-	-
Head supply pressure	0.25 bar	0.30 bar	0.25 bar	0.25 bar
Polish time	00:00:10	~00:08:00	00:01:00	00:00:02

SiN CMP soft landing	Stage 1	Stage 2	Stage 3	Stage 4
Slurry	Klebosol 30HB50	Klebosol 30HB50	DI water with 1% TMAH	DI water
Slurry feed rate	75 mL min^{-1}	75 mL min^{-1}	150 mL min^{-1}	-
Pad rotation	40 rpm	25 rpm	40 rpm	2 rpm
Holder rotation	40 rpm	55 rpm	40 rpm	2 rpm
Back pressure	-	0.05 bar	-	-
Head supply pressure	0.25 bar	0.15 bar	0.25 bar	0.25 bar
Polish time	00:00:10	~00:01:30	00:01:00	00:00:02

Cu CMP bulk process	Stage 1	Stage 2	Stage 3	Stage 4
Slurry	Cabot C7092 2:1 (DI:Slurry)	Cabot C7092 2:1 (DI:Slurry)	DI water with 1% TMAH	DI water
Slurry feed rate	75 mL min^{-1}	75 mL min^{-1}	150 mL min^{-1}	-
Pad rotation	40 rpm	60 rpm	40 rpm	2 rpm
Holder rotation	40 rpm	60 rpm	40 rpm	2 rpm
Back pressure	-	0.08 bar	-	-
Head supply pressure	0.15 bar	0.15 bar	0.15 bar	0.1 bar
Polish time	00:00:10	~00:20:00	00:01:00	00:00:02

Cu CMP soft landing	Stage 1	Stage 2	Stage 3	Stage 4
Slurry	Cabot C7092 2:1 (DI:Slurry)	Cabot C7092 2:1 (DI:Slurry)	DI water with 1% TMAH	DI water
Slurry feed rate	150 mL min^{-1}	150 mL min^{-1}	150 mL min^{-1}	-
Pad rotation	40 rpm	60 rpm	40 rpm	2 rpm
Holder rotation	40 rpm	60 rpm	40 rpm	2 rpm
Back pressure	-	-	-	-
Head supply pressure	0.1 bar	0.1 bar	0.1 bar	0.1 bar
Polish time	00:00:10	~00:02:00	00:01:00	00:00:02

C.3 Fabrication of power MEMS test structures

Run Sheet

Author: Byron Shulver **Batch number:** **Mask set ID: SMC1**

Product: Thick Film MEMS Test Structures **Quantity:**

Starting material: (100) 8" Si wafers with Passivation layer **Date:**

General: carefully inspect the product after each process step before proceeding to the next one.

Step	Process	Tool	Process details	Comments
1.	Deposit seed layer	OPT Plasmalab 400	Ti: 1 KW DC Time: 00:10:00 Cu: 1 KW DC Time: 00:30:00 Ti: 1 KW DC Time 00:10:00	Ti / Cu / Ti to thicknesses of 10 nm / 300 nm / 10 nm
2.	Resist coat	SPS Polos spin coater	Pour 8 mL NR2 20000P onto centre of wafer, Spin at 3000 rpm 1000 rpm/s Time: 00:00:30	30 µm
3.	Soft bake	EMS hotplate	70°C Time: 00:20:00 140°C Time: 00:02:30	
4.	Edge bead removal	Brewer Science track CEE	Program: EBR 8.10mm	10 mm edge bead removal using PGMEA
5.	Expose	Karl Suss MA8	Contact WEC, Soft contact printing mode, Exposure Dose: 960 mJ	
6.	Post exposure bake	EMS hotplate	100°C Time: 00:10:00	
7.	Develop	SPS Polos developer	RD6 developer 7 x Time: 00:01:00 puddles 3 x Time: 00:02:00 puddles 1 x Time: 00:05:00 puddles	
8.	Pre-treatment	Electrotech barrel asher	Time: 00:05:00 standard conditions	
9.	Etch top Ti layer	Wet Deck	1% HF in DI water Time: 00:00:30	
10.	Electroplate Cu	SMC Tool	2.8 A Time 00:45:00	20 µm
11.	Strip resist	Ultra sonic bath	Air Products ACT/CMI PR Stripper Ultrasonic Agitation, 70°C Time: 00:10:00	
12.	Strip seed layer	Wet Deck	1% HF in DI water for Top Ti Time: 00:00:30 Rockwood Al etchant for Cu Time: 00:05:00 1% HF in DI water for bottom Ti Time: 00:00:30	
13.	Dice	Disco wafer saw		

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