Integrating CAM and Process Simulation to Enhance the Analysis and Control of IC Fabrication

Thesis submitted by
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To my parents.

Declaration

I declare that all the work done in this Thesis is entirely my own except where otherwise indicated.

This Thesis is the result of a CASE project with Plessey Semiconductors Ltd.

Contents

Abstract

The application of advanced manufacturing technology (AMT) to semiconductor manufacturing has made great improvements to the productivity and cost effectiveness of the industry. In particular, the application of computer aided manufacturing (CAM) to integrated circuit (IC) fabrication has helped to reduce costs, increase asset utilization and throughput, and improve yields. It is anticipated that market forces and technical constraints will bring about a more flexible approach to production that will depend heavily on manufacturing control systems. However, the current generation of CAM systems do not provide the level of analysis and control required by flexible manufacturing environments.

This Thesis introduces a method for integrating process simulation with a commercial CAM system to enhance the analysis and control of IC fabrication. A structured interface has been developed that will allow a process engineer to interactively use process simulation to verify past processing and estimate the effect of future operations. This results in a better understanding of the process within the manufacturing environment, the ability to analyse the fabrication sequence, and decision support for feed-forward control. The information used to control the simulations is held within the CAM system. The new system has been implemented using the CAM system COMETS and the process simulators SUPREM-II and SUPREM-3. It is believed that this is the first time that process simulation has been made available as a manufacturing tool.

To support the application of process simulation to manufacturing a specification control system has also been developed. This system adds recipe management to the COMETS CAM system by explicitly representing process information within its database. Apart from enhancing process analysis through process simulation, this system simplifies process maintenance, improves the integrity of process specifications, and allows effective on-line control of production.

In addition to these original contributions, this Thesis provides extensive reviews of fabrication specification and control, semiconductor CAM systems, and the application of process simulation to manufacturing processes.

Publications

Publications by the author relevant to this work include:

A.J. MacDonald, A.J. Walton, J.M. Robertson, *Integrating COMETS and Process Simulation*, COMETS International User Conference, Phoenix, Arizona, September 1988.

A.J. MacDonald, A.J. Walton, J.M. Robertson, R.J. Holwill, *Computer Aided Manufacturing in the Semiconductor Industry*, Sunderland Advanced Manufacturing Technology Conference, Sunderland, UK, March 1989.

A.J. MacDonald, A.J. Walton, J.M. Robertson, R.J. Holwill, *Integrating CAM and Process Simulation*, (invited paper), COMETS European User Conference, Hayes, UK, May/June 1989.

A.J. MacDonald, A.J. Walton, J.M. Robertson, R.J. Holwill, *Integrating Computer Aided Manufacturing and Process Simulation for the Production of ASICs*, Microelectronics'89, Brisbane, Australia, July 1989.

A.J. MacDonald, A.J. Walton, J.M. Robertson, R.J. Holwill, *Integrating CAM and Process Simulation to Enhance On-Line Analysis and Control of IC Fabrication*, To be published in IEEE Trans. on Semiconductor Manufacturing,

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Chapter 1

Introduction

Over the last twenty years the semiconductor industry has come to play a major role in the world economy. Not only are integrated circuits (ICs) an internationally saleable commodity in themselves, but they also influence the market for many other products, such as computer and audio equipment. In turn the market for these products effects the value of ICs, often resulting in cyclical variations in demand. The major players in the production of ICs are the United States, Japan and Europe. These factors cause IC manufacture to be regarded as a strategic industry, which has led to the international market being distorted by political intervention. However, despite these influences companies are very aware of the need to remain competitive on price and quality and so share a common goal of achieving world-class manufacturing.

IC manufacture requires a tremendously high capital investment before production can begin [1], and yet more capital becomes tied up in the value of the work-in-progress once production is underway. The result is that it is essential to make the most efficient use of both time and equipment. Such economic constraints are paralleled by technical constraints. ICs are required to meet specifications which are at the edge of processing limits, and the task is complicated by the need to fabricate ever smaller features on increasingly large wafers.

In response to the economic and technical constraints on IC manufacturing, the industry has largely polarised into commodity and application specific production. Figure 1.1 shows the spectrum of fabrication lines which exist to meet the needs of the market. Commodity-style manufacture seeks to achieve the lowest possible cost per unit and so tends towards producing high volumes of only a few products. For example, the fabrication of memory and microprocessor circuits in standard product or dedicated production facilities. Application specific-style manufacture aims for the more specialised end of the market where products can command higher selling prices. A consequence of this is that more products are made in lower volumes and so the facilities must be flexible enough to

make changes in product-mix very quickly. The range of production facilities that perform flexible manufacturing include application specific IC (ASIC), research and development, captive, and some standard product facilities.

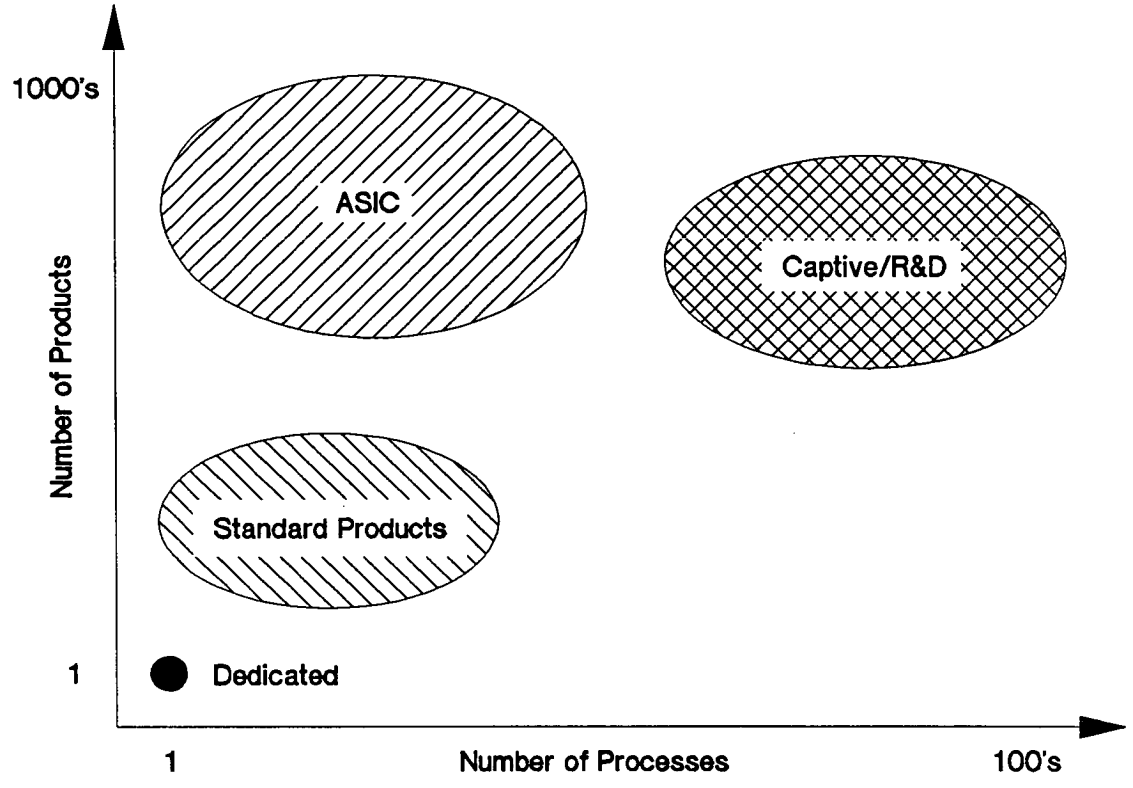

Figure 1.1 The wafer fabrication line spectrum, after [1].

The search for more efficient production, and thence world-class manufacturing, has led companies from all sectors of the IC industry to begin adopting advanced manufacturing technology (AMT). This includes automated material flow, integrating computer systems, factory simulation, statistical quality control, and expert systems. The most widely applied technology, however, is computer aided manufacture (CAM). CAM systems provide tools to perform tracking of work-in-progress, planning of production, collection of engineering data and report generation. Where implemented they are reported to have improved cycle times, equipment utilization and yield [2].

1.1. IC Manufacture

Integrated circuits are fabricated on wafers of semiconducting material, normally silicon, which are then cut-up into die, or chips, before being packaged and subjected to

functional testing. Though only a simple outline, this description serves to highlight the major areas of IC manufacture. AMT has been applied, to some extent, in each of these areas but with the greatest effort being made in wafer fabrication. This is largely because during fabrication there is the greatest increase in the value of the products being manufactured.

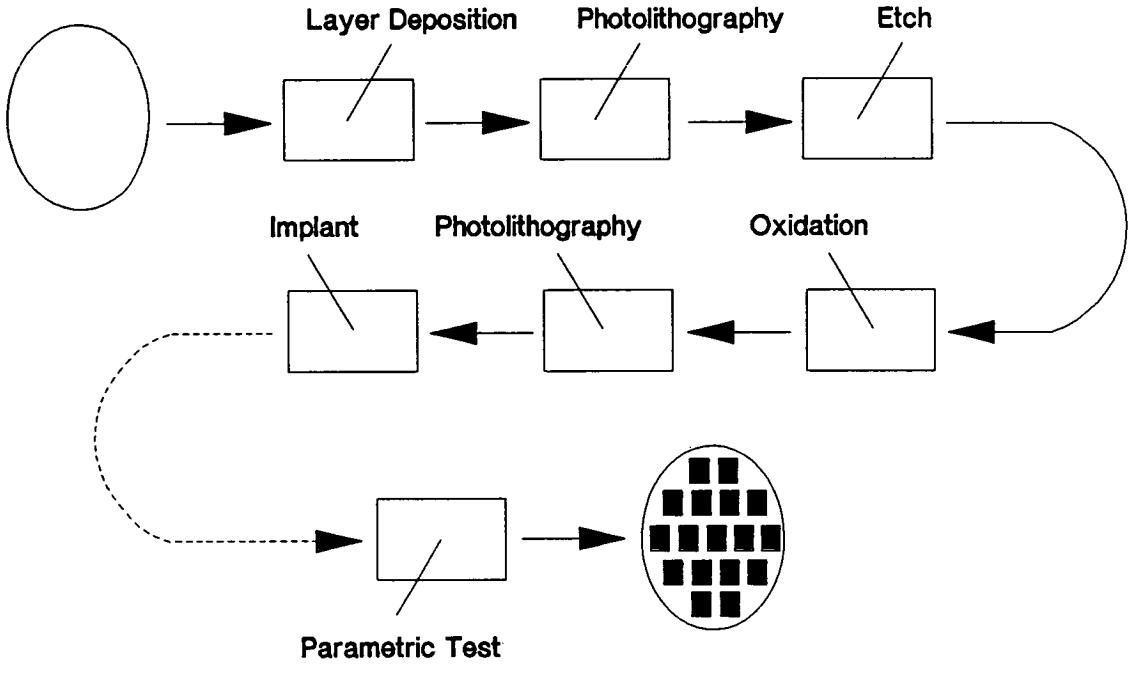

Figure 1.2 An MOS IC fabrication sequence.

A wafer fabrication process consists of many hundreds of individual steps. These are performed on batches of wafers which pass serially between the process steps; there being no sub-assemblies in wafer fabrication. As is apparent from figure 1.2 a process consists of a set of steps, many of which are repeated throughout the fabrication sequence. After certain process steps, measurements are made to verify part of the previous processing. Only a limited number of these tests can be made without damaging the wafers and so few test are performed in-line on product wafers. Consequently it is not known until the end of the process whether the devices being fabricated will have the desired electrical parameters. The yield of the process is dependent on both the control parameters for each operation, and the accuracy of the process equipment. The ensuing causal relationships are extremely complex. Achieving a satisfactory yield is further complicated by the fact that both the

operating ranges of the processing equipment, and the device geometries are approaching the physical limits of technology.

The goal of every manufacturing facility is to make the right products at the right time for the right cost [3]. As suggested earlier, the production methodologies used to achieve this objective range from commodity to application specific manufacture. Historically the dominant production philosophy has been stable commodity-style manufacture, but this is giving way to more flexible approaches to manufacturing [4]. This can be regarded as the movement from load-oriented systems, where product is 'pushed' through the line, to process-oriented systems, where market demand 'pulls' product through the line [5].

Commodity production is normally characterised by having a high volume throughput on a single process with large batch sizes and very few products. The goal is to achieve minimum time per operation with maximum output per unit of time, although this does result in long set-up times. Application specific production, in contrast, tends to have smaller batch sizes with many products each being fabricated in a comparatively low volume. There is also the potential for many processes being run at one time. Application specific manufacture generally seeks to achieve minimum time per order, maximum utilization of facilities per time period, and set-up times close to zero. Though the terms 'commodity' and 'application specific' are useful for characterizing fabrication facilities, instances do exist of facilities that have some of the characteristics of both types of manufacture. For example, a nominally ASIC gate array production facility can be based on very high volume with only a single product until just prior to metallization. After this the single product can become many hundreds of different products, each being fabricated in very low volume.

1.2. Advanced Manufacturing Technology

The objective of introducing advanced manufacturing technology (AMT) into IC production is to increase profitability. Therefore any new addition to the existing manufacturing tools could be described as AMT. However, the technologies that have received the most attention over the last few years have been factory automation and computer integrated manufacturing (CIM).

Factory automation is a broad term that has been used to describe the automation of processing equipment, the mechanization of the wafer transfer and handling equipment, and the computer networks required to track, control and distribute information around

an automated environment [6]. There have been many discussions on the use of robots, track systems and automated guided vehicles (AGV) [6, 7, 8, 9, 10, 11] to achieve material transfer for semiconductor manufacturing. Automation is driven by technological needs: smaller device geometries; increasing wafer sizes; and cleaner fabrication environments [12].

However, there are very few cases of automated wafer transfer systems, perhaps because these systems will not fit into existing clean-rooms. Where factory automation has been implemented it has been either as full mechanization, or as more flexible *islands-of-automation*. Mechanization of wafer fabrication is an inflexible approach where machines are hard-wired together and wafer transport between processing stations is by fixed track systems. These systems are best suited for producing high volumes of only a few products on a single process; that is, commodity production. As a result they offer better turn-around-times, and improvements in process and defect control [3]. This approach to manufacturing has been favoured by the Japanese in the semiconductor and other industries [13]. Although normally there is very little published on Japanese methods of IC manufacture, the level of automation achieved by the company NMB has been well documented [9, 14, 15] and similar work by Mitsubishi has also been reported [16]. Published research in the USA, into fully mechanised systems, includes the automated IC packaging system Odyssey from National Semiconductor [7].

The idea of a 'clean-box' rather than a 'clean-room' has been employed with some success to reduce particle counts, and thereby defects, in automated environments [8, 17, 18, 19, 20]. The semiconductor manufacturing interface (SMIF) box is used to transfer wafers between pieces of automated processing equipment, thus reducing the amount of contact between operators and wafers.

As with many other industries, flexible manufacturing systems (FMS) have emerged as a manufacturing methodology that is capable of reacting quickly to the demands of the market. An FMS consists of equipment grouped into cells with control of equipment and material flow being performed by a distributed computer system [21]. Automated cells, or islands-of-automation, are of considerable individual value but may introduce problems because of the lack of communication between them [22]. Cells may be classed as either functional or sequential [23]. In a functional cell, the processing equipment runs the same type of process, such as dry etching. Equipment inside a sequential cell performs a logical sequence of process steps, for example, a photolithography sequence. A number of cell

implementations have been reported [3, 24, 25, 26].

Various control hierarchies have been suggested for implementing automated IC fabrication [27, 28], these can be generalised to the form shown in figure 1.3. Such hierarchies are used in both commodity and application specific manufacturing environments as the levels of the hierarchy correspond to levels of management control rather than the distributed nature of wafer processing.

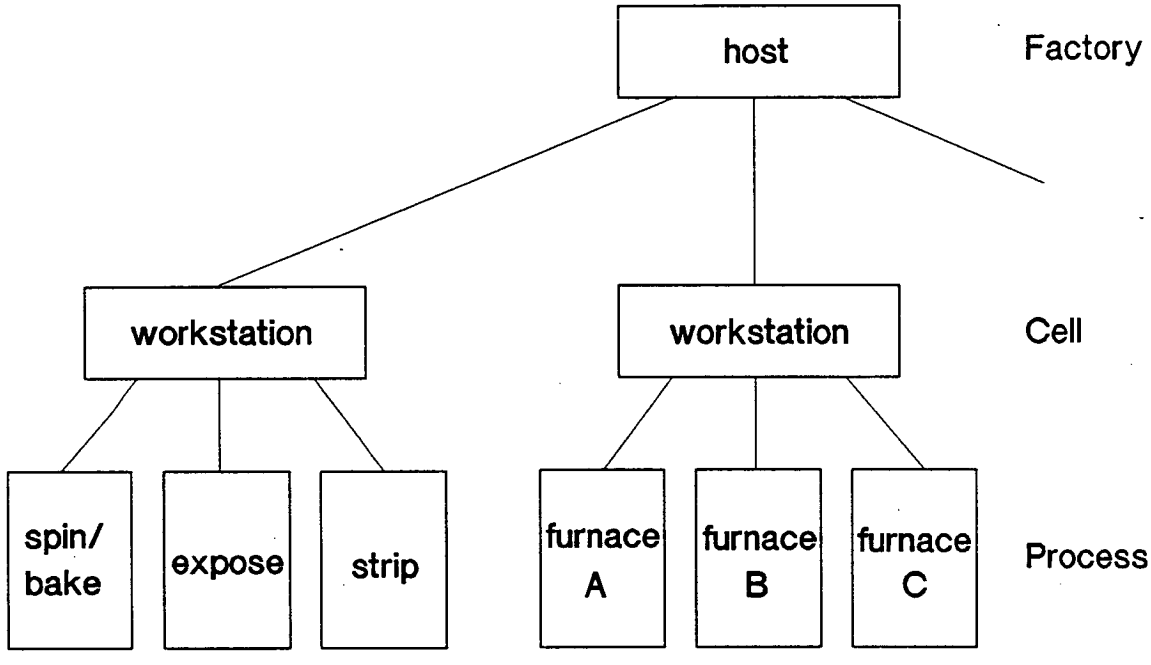

Figure 1.3 Generalised manufacturing control hierarchy

At the most basic level of figure 1.3 are dedicated microprocessors performing the real-time control of the processing equipment. They apply the control parameters to the equipment and collect raw data to be passed to the next level in the hierarchy. In many cases equipment controllers are being shipped with the processing equipment. The next level is that of the cell, which physically might be a workstation, performing a certain amount of data reduction and downloading recipes to equipment controllers. Further capabilities might be included at this level; including process monitoring and feedback control based on sensory data, scheduling, and expert systems. Information from the cell computer is then passed up to the host system. The host is normally a larger computer with extensive data storage capabilities, and supports a comprehensive computer aided

manufacturing (CAM) system [29, 30, 31, 32, 33]. These systems perform the overall work-in-progress tracking, capacity planning, scheduling of the movement of work between cells, and assorted data analysis functions. Though the hierarchy of systems has been described here as physically distributed over different computers, they could potentially all be implemented on one computer, assuming that it is capable of handling the data transactions within an acceptable amount of time.

The equipment to computer interfaces for semiconductor manufacturing play an important role in factory automation, for data collection and remote control. This has resulted in the development of the SEMI Equipment Communications Standard (SECS) [34]. The standard has been developed in two parts. SECS-II defines a set of data and messages types for communication between a host computer and semiconductor processing equipment. SECS-I describes the procedure to block these messages and transfer them to processing equipment. In time it is anticipated that these basic standards will be developed further [35, 36]. Currently SECS is peculiar to the semiconductor industry, a review of other communications standards is given in [37].

The use of computers in this environment to integrate the control of processes, product handling, and information flow can lead to higher levels of process control, repeatability and equipment utilization; this is often referred to as computer integrated manufacturing (CIM) [3]. In the same way as automation is driven by technology concerns, CIM is driven by production concerns: better plant utilization; increased ability to manage complexity in a mixed processing environment; cost reductions; and improved customer satisfaction [38]. However, CIM is seen as more than simply advanced computerised manufacturing. CIM can also include computer aided design (CAD), CAM and management information systems (MIS) [5, 25, 37, 38, 39, 40, 41, 42]. Thus a CIM system can allow data to be shared freely throughout a company.

The availability of information characterizing the shop-floor has encouraged the application of new management philosophies such as just-in-time (JIT) [43, 44]. For a review of production scheduling methodologies, including manufacturing resource planning (MRP) and JIT, see [45].

Although complete CIM is yet to be achieved, the spread of manufacturing control systems has led to the availability of previously unattainable data. Consequently many tools are being applied to the analysis of data in order to aid decision making.

Simulation tools have been developed to analyse the operation of semiconductor manufacturing facilities [46, 47, 48, 49]. These simulation techniques have led to enhancements in capacity planning, equipment maintenance management, production scheduling, the forecasting of product delivery, and resource requirements scheduling [50, 51, 52, 53].

Statistical process control (SPC) has recently emerged as a method of analysing the vast amounts of data which can be collected in an IC manufacturing facility [54, 55, 56, 57, 58, 59, 60]. In addition, expert systems have been investigated as a method for aiding decision making in the complex fabrication environment [61, 62, 63, 64].

1.3. Motivation

This Ph.D. originally set out to investigate the application of CAM to IC fabrication. The motivation for this lay in the need to develop CAM systems that could meet the combined challenges of flexible manufacturing and increasingly complex processing. It became apparent during this investigation that there are very few tools available to enhance manufacturing productivity. Therefore, particular emphasis has been given to considering what aids are required for the analysis and control of semiconductor processes.

Currently available tools, such as SPC, can be used for production analysis but provide no insight into how a process works. In order to understand a process it is necessary to model it. Process simulation is a method that can be used to explore the physical effects of process steps and their interaction in a complete process. This Thesis shows how process simulation can be integrated with CAM to perform process analysis and feed-forward control.

In implementing this system it was noted that the current generation of CAM systems do not provide an explicit description of processing. Therefore, this Thesis also demonstrates how specification control, or recipe management, can be implemented as part of a flexible manufacturing control system.

1.4. Structure of Thesis

This chapter has presented a broad background to the application of computer aided manufacturing for the production of ICs. However, to fully appreciate the rationale behind the use of process simulation for the analysis and control of IC fabrication a more detailed discussion of the control of IC fabrication is presented in chapter 2. Chapter 3 presents the current state of CAM systems for the semiconductor industry and describes the implementation of the commercial system COMETS. A brief review of process

simulation is presented in chapter 4 along with examples of how both one- and two-dimensional simulators can be calibrated to a manufacturing process. In chapter 5 these strands of information are brought together to describe the fundamental concepts of this Ph.D. and its contribution to the field of CAM for the production of ICs. Chapters 6 and 7 describe in detail the original work carried out as part of this Ph.D.: the integration of process simulation and CAM is described in chapter 6; and chapter 7 presents a new method for fully describing the manufacturing sequence using process recipes. Finally some conclusions are drawn on the work presented within this Thesis and some suggestion for further work are outlined.

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Chapter 2

Specifying and Controlling IC Fabrication

2.1. Introduction

Since the development of the first integrated circuit (IC) by Kilby [1] in 1958 a massive industry has developed around producing ever faster and more functional ICs at lower cost. As the intricacy of these products has evolved so too has the complexity of the processes required to manufacture them. In response to this the semiconductor industry has polarized into commodity manufacturers producing standard products in high volume, eg. memory and microprocessors, and application specific integrated circuit (ASIC) manufacturers satisfying the demand for custom products in lower volumes. This has resulted in the availability of a wide range of production technologies and materials. Despite this the majority of ICs are still fabricated on silicon. Therefore in this chapter we will restrict our discussion of IC processing to silicon based technologies.

The manufacture of ICs is performed in a number of stages. During the first stage the wafers upon which the ICs are fabricated are sliced from specially grown single crystals of silicon. Current wafer diameters vary from three to circa eight inches in diameter, with some advanced fabrication facilities using even larger wafers. The second stage is wafer fabrication where each layer of the circuit design is applied to sites on the wafer surface. The whole fabrication process can take anything from three to ten weeks to complete, the cycle time being very dependent upon the layout and scheduling of the individual facility. Following from wafer fabrication is assembly where the circuits on the wafers are cut into separate *die*, or *chips*, and then packaged to form the saleable product. Finally, functional testing is performed to check that the packaged circuits will perform as designed and within specification.

When attempting to maximise the productivity of IC manufacturing emphasis must be placed on wafer fabrication. This is because, for most processing scenarios, wafer fabrication has the greatest impact on the cost per unit of the final product; which is evident when one considers that a raw wafer may only cost a few tens of dollars while the fully

processed wafer can be worth many thousands of dollars.

In this chapter an overview of wafer fabrication is presented. The steps which go to make up a fabrication process are then discussed, with emphasis on the parameters required to control these steps and the engineering data that can be collected to perform process monitoring and control. Finally the integration of these process steps is demonstrated using, as an example, the Edinburgh Microfabrication Facility (EMF) 1.5 micron nMOS process.

2.2. Wafer Fabrication

The processes which are used to fabricate ICs are among the most complex performed today. This complexity is a function of the high number of steps which make up a process and the way that all of these steps are interrelated. Ultimately however all IC fabrication processes have the same objective: to produce a high yield of reliable ICs in the most cost effective manner.

Within any IC fabrication plant much time and effort is directed towards achieving a clean, vibration free, highly organised environment where temperature and humidity are tightly controlled. The objective being to maintain consistent processing, reduce the presence of particles, improve alignment accuracies during photolithographic process steps, and avoid the breakages and misprocessing that occurs. To appreciate why the manufacturing environment need be so well maintained one must look more closely at the generic characteristics of an IC process and come to understand the rationale behind the construction of the process.

The objective of processing a wafer is to build electrical circuitry across its surface. Commonly this takes the form of many separate sites on the wafer surface, that may either be the same circuit replicated many times or a mixture of different circuit designs. Each circuit can be made up of transistors, resistors, capacitors and other electrical devices. These are fabricated as three-dimensional structures, a section through a typical structure is shown in figure 2.1. Note that this device is made up of layers, both above and below the surface of the wafer. Each layer is defined by a mask which corresponds to a level of the circuit design.

The mask is applied by spinning a photoresist onto the surface of a wafer and exposing the photoresist to light through the mask. When the resist is developed a pattern of exposed wafer surface results. Then the exposed material can be etched or doped and the

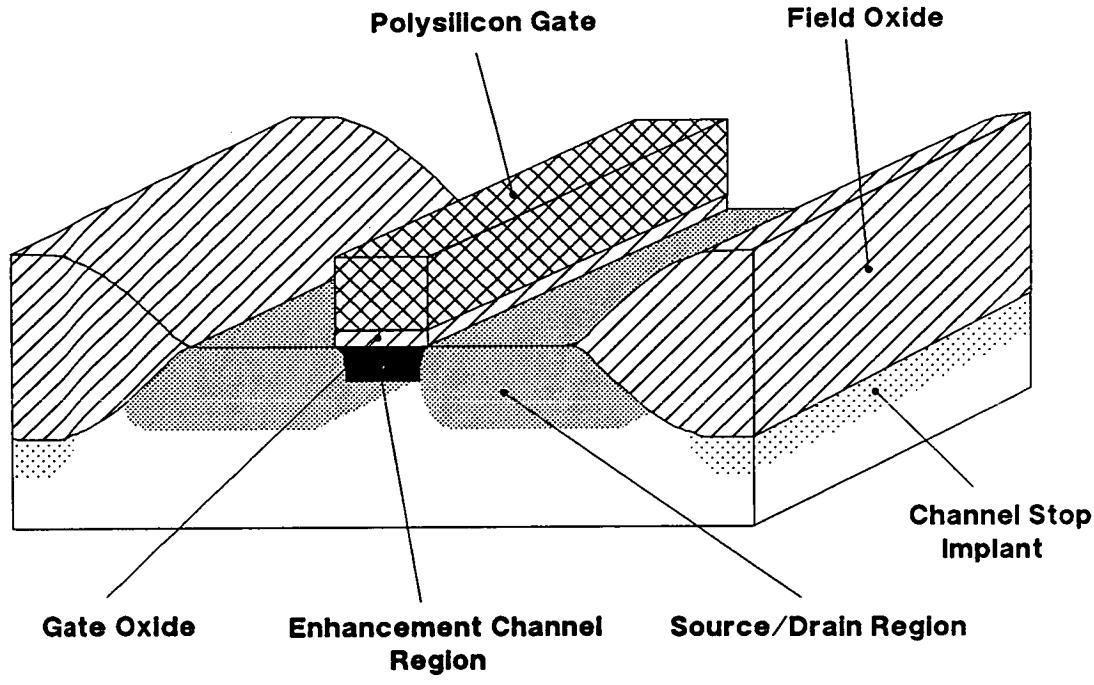

Figure 2.1 Section through an enhancement mode nMOS transistor.

remaining photoresist is stripped off.

The range of materials include conductors (eg. aluminium), semiconductors (eg. doped silicon), and insulators (eg. silicon dioxide). The level and type of doping of the semiconductors dictate their conductivity. Common dopants are boron (p-type), arsenic, antimony and phosphorus (all n-type). The level and type of doping through a wafer is termed its doping profile.

Two distinct types of IC fabrication processes have evolved: bipolar and Metal-Oxide-Semiconductor (MOS). Initially bipolar developed as the leading technology and spawned such device families as TTL, ECL and I^2L, all of which are still used widely. The main characteristic of bipolar silicon circuits is their speed. However, they are also power hungry and generate a great deal of heat. The first MOS technology to emerge was p-type MOS (pMOS), but this was later superseded by n-type MOS (nMOS) which is faster, due to the higher mobility of electrons than holes, and offers greater packing densities. Then followed CMOS where both p- and n-type MOS devices are used. Although not inherently offering the same high packing densities as nMOS, CMOS requires very little power. For a full discussion of silicon IC technologies see Hillenius [2].

2.3. Process Steps

Wafer fabrication is a serial process. As each process step is performed it influences the other steps in the fabrication sequence. For example, when a process step includes a heat component it will cause some redistribution of the dopants introduced during previous process steps. Another example is the use of oxide layers as masks to prevent dopants being introduced to certain areas of a wafers surface. From these examples, it is evident that there is a strong interrelation between the steps of a process.

Though there are many ways in which ICs may be fabricated there are only a limited set of operations which can be performed. These range from oxidation to lithography, each requiring very different control parameters. For an operation to become a step in a manufacturing process the input parameters must be carefully considered so that the function performed plays its part in terms of the whole process. Engineering data can then be collected to verify that the intended processing has actually occurred.

Figure 2.2 shows a generic process step in terms of the information required to control the step and the information which may be collected from this step. The input parameters can be passed as a complete recipe definition from a control system. The data collected from monitoring the processing equipment and from measurements made on the product and test wafers can be passed back to the control system so that process control may be performed. Where possible, in a production environment, process measurements are made on the product wafers, as test wafers take up space which otherwise would be used for product wafers. The data collected during the process is from physical measurements made on the surface of the wafer during or after each process step. Parametric data is also collected after metallization by measuring the electrical characteristics of test devices to produce engineering yield data. The test devices are often sited on process monitor chips (PMC) [3], which take up wafer sites normally used for product chips, or in the scribe lines between devices [4]. The uniformity of the collected physical and electrical parameters is often displayed to the process engineer as a wafer map [5]. In many cases it possible to collect parametric data using computer controlled equipment.

However, it is not always possible within a manufacturing environment to verify processing as it is performed. For example, when a gate oxide is grown during an MOS process one may wish to test the doping density at the surface of the wafer to find out how much dopant has been leached out of the silicon by the growth of the silicon dioxide. Unless a destructive test is performed at this point then it is necessary to wait until a later

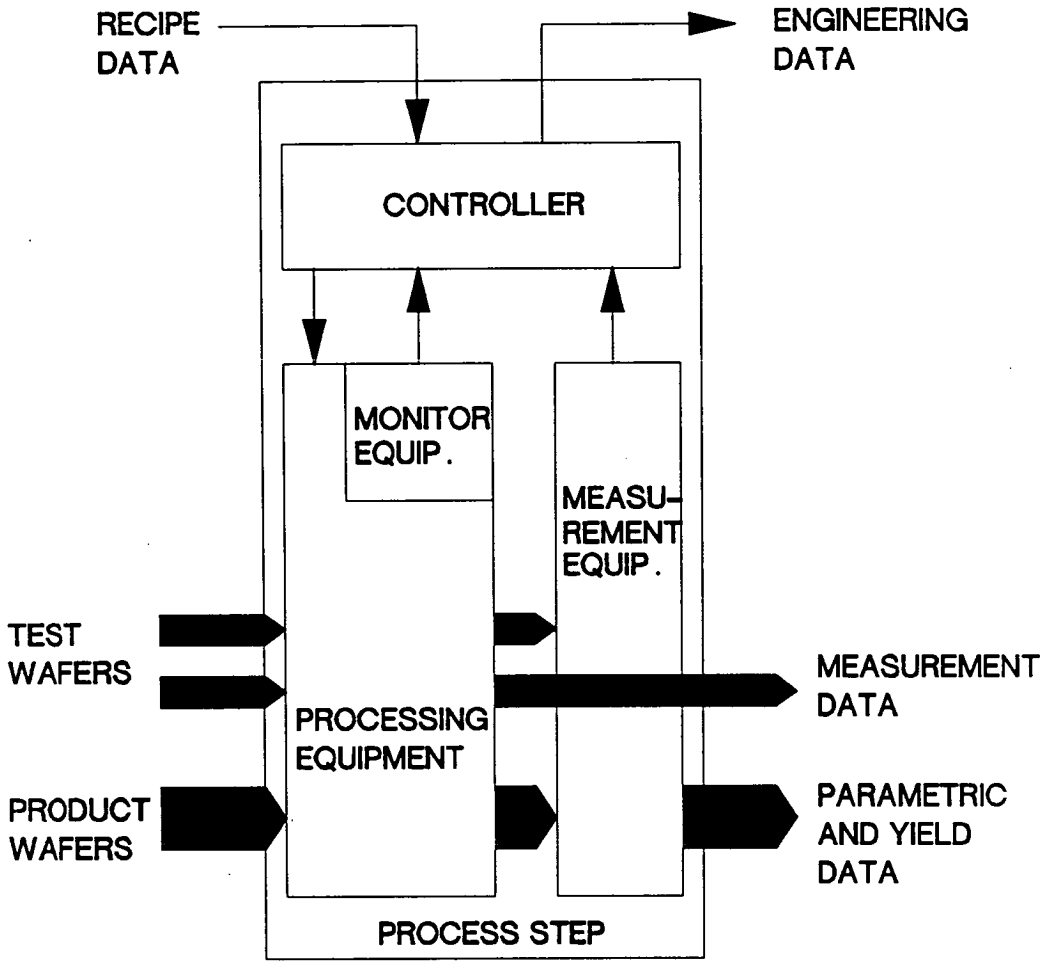

Figure 2.2 Generic wafer fabrication process step

process step has exposed the wafer surface before the doping density can be established. Destructive testing is not generally desirable during manufacture as it is wasteful of both time and potential product.

From this we can see that our ability to track and control a process is dependent on the interrelation of the process steps. Thus we must consider the operations which can be performed, paying particular attention to why they are performed, how they are performed, the effect they have on previously defined layers, and how they are controlled and monitored.

2.3.1. Oxidation

The oxidation of silicon is very important in semiconductor manufacturing as the

natural oxide of silicon is a key component in the structure of all devices. Indeed, planar processing technology derives much of its success from the properties of thermally grown silicon dioxide. These properties allow the oxide to be used for several purposes: as a masking layer against implanted ions and dopant diffusion; as a surface passivation layer; and as an isolation layer/region both between the conducting layers of a device and between devices. A common characteristic of all these oxides is that they must be of high quality and be produced in a controlled and repeatable manner.

Although thermal oxidation is the most prevalent technique for producing an oxide it is also possible, and sometimes necessary, to use other methods. These range from wet anodization through chemical vapour deposition (CVD) to plasma oxidation. For example, in laying down a passivation layer over metal the CVD method must be used.

Within thermal oxidation there are essentially two chemical mechanisms; as shown in equations 2.1 and 2.2.

$$Si(solid) + O_2 \rightarrow SiO_2(solid) \tag{2.1}$$

$$Si(solid) + 2H_2O \rightarrow SiO_2(solid) + 2H_2 \tag{2.2}$$

For thin oxides dry oxidation (eqn. 2.1) is normally used while for thicker oxides the faster wet mechanism (eqn. 2.2) is preferred.

Both forms of thermal oxidation are performed in tube furnaces where gas flows, temperatures and sequencing are microprocessor controlled. In normal processing the wafers are loaded into the furnace at an idling temperature of 700-900°C before the temperature is ramped up for processing. After the oxidation the temperature is ramped down again. Ramping is employed to minimise wafer warpage.

Prior to oxidation it is necessary to clean the wafers. This removes any contaminants, arising from previous process steps or handling, that might degrade the electrical characteristics of devices or increase the defect density.

The dry oxidation of silicon requires only simple processing equipment and produces a slow growth of oxide at moderate temperatures (c. 950°C). Dopants in the silicon will also redistribute during oxidation as a result of the high temperature.

For dry oxidation the growth rate may be enhanced by modifying the recipe control parameters. For example, higher temperatures will result in a thicker oxide. Though this can also cause an extensive redistribution of dopants. Alternatively the pressure may be

increased to give a larger oxide but with little redistribution of dopants. However, to-date there has been limited development of high-pressure processing equipment [6]. Another approach is the introduction of HCl [7] which increases the oxidation rate and improves gettering.

The oxidation mechanism used during wet oxidation results in a higher oxide growth rate than can normally be achieved during dry oxidation. There are two commonly used methods for producing a wet ambient: steam oxidation and pyrogenic oxidation. In steam oxidation oxygen is bubbled through water before entering the furnace tube. This produces a large oxide at moderate temperatures and times. However, the bubbler system can easily become contaminated. These problems may be avoided by using pyrogenic oxidation. Here the water vapour is created in the furnace tube by direct combination of hydrogen and oxygen. It is also possible to perform wet oxidation with dry, or dry-HCl, oxidation in the same tube and thereby tailor the characteristics of the oxide. This is only achieved however at the expense of equipment complexity.

As with dry oxidation the increase of temperature will result in larger oxide growths. However, the presence of HCl will have little or no effect. When pressure is increased there is a subsequent rise in oxidation rate. Though maintaining a consistent pressure profile throughout a furnace and from run to run is very complex, and failing to do so can result in erratic oxide growth [8].

The trend towards smaller, faster devices has led to the increasing use of thin oxides in the range of 50-200 Å. This places additional restraints on the growth of the oxides as thinner oxides are more sensitive to fatal defects and are harder to grow uniformly. As with normal oxides there are a number of ways in which a thin oxide can be grown. However, for a dry oxidizing ambient there is an initial rapid oxide growth to around 200 Å making thin oxide growth difficult to control. Techniques using lower temperatures and reduced pressures have been developed to combat this problem [9, 10]. For wet oxidations a consistent low growth rate can be achieved in a high pressure steam ambient at lower temperatures than for normal oxides [11]. For a review of rapid thermal processing see Sedgwick [12].

Monitoring the thickness of a grown oxide and its uniformity across both wafer and batch can be achieved using reflective/refractive techniques such as spectrophotometry and ellipsometry on the product wafers [13]. This is important as, for example, variations in the gate oxide of an MOS device can cause substantial threshold voltage variations. To

obtain useful uniformity data it is important to make many thickness measurements across the surface of a wafer, so these measurements are normally performed using automated measurement equipment.

2.3.2. Diffusion

The diffusion of dopants in silicon is a crucial mechanism in planar processing. Introducing a dopant and controlling its concentration can be used to alter both the type and the electrical conductivity of silicon. In MOS technology it is used to form source/drain regions, deep wells, and to dope polysilicon. To achieve devices with electrical characteristics which adhere to specification it is important that dopant diffusion is uniform and reproducible.

There are a number of ways in which a dopant can be introduced into the surface of a wafer: a chemical source in a vapour, deposition of a doped oxide source, and ion implantation. The method chosen for doping the wafers is dependent on the required doping profile and surface concentration. Heating the wafers to a high temperature in the presence of a chemical vapour for the whole of the diffusion will result in a complementary error function (erfc) distribution. Whereas if a *pre-deposition* of the dopant is performed at a lower temperature followed by a *drive-in* at a higher temperature a gaussian distribution can be obtained. High temperature diffusion is used not only to distribute the dopant but also to electrically activate the dopants; a technique called *annealing*. A similar effect to that of a pre-deposition step can be produced by using a doped oxide source. The introduction of impurities by ion implantation is considered separately in section 2.3.3.

Deposited dopant concentrations tend to be high which makes shallow abrupt junctions difficult to form. The high temperatures associated with diffusion cause lateral as well as vertical distribution of dopants. For a detailed study of the distribution of dopants in silicon at diffusion temperatures see Fair [14].

The diffusion of dopant through other materials than single crystal silicon is also of interest; particularly polysilicon and silicon dioxide.

Polysilicon is used both for self-aligned gates and as an intermediate semiconductor between two layers of a device. Boron, phosphorus and arsenic are often used to reduce the resistivity of polysilicon.

Silicon dioxide is commonly used as a masking layer to prevent the introduction of dopants into silicon over predefined areas of a wafer. Because of the slow diffusion of

most dopants through silicon dioxide it is convenient to make sure that the oxide is simply thick enough to act as a barrier to the dopants. However, it has been noted that during oxidation some dopants will diffuse further in the regions exposed to an oxidizing ambient [15].

So far consideration has been restricted to vertical diffusion, however in a three dimensional structure diffusion also occurs laterally. This effect is noticeable where an area of silicon has been masked off for pre-deposition such as during the formation of a source or drain region in an MOS device. Here we see that the junction formed by the lateral diffusion under the mask is at about 3/4 the distance from the mask edge as the vertical junction is from the surface. In fabricating a device with a short drain region it is essential that the source and drain regions do not meet otherwise the device will short circuit. This emphasises the importance of considering the two dimensional diffusion of dopants in small geometry VLSI devices.

The diffusion of dopants is performed in furnace tubes under similar control regimes to those of oxidation. For the deposition of dopants on the wafer surface liquid or solid sources are commonly used. When a liquid source is used oxygen can be introduced to form a doped oxide layer over the wafer surface during the diffusion rather than a chemical vapour. Phosphorus and boron may be also be deposited using this method. Wafers of boron nitride and phosphorus oxide are used as solid sources. They are interleaved with the product wafer to ensure a uniform distribution over the surface of the wafers. The deposition of arsenic is not normally performed in this way as it is too toxic, ion implantation is used instead.

Time, temperature and concentration have a first order effect on the deposition and diffusion of impurities in silicon. In a practical system the timing will be bracketed, as with oxidation, by temperature ramp-up and a ramp-down periods.

A diffusion operation may be monitored by measuring the junction depth and sheet resistance of the processed wafers. The junction depth can be measured by grinding a wedge shape in the wafer and staining the sample so that the junction between p- and n-type materials can be identified, this is called the bevel and stain technique. The sheet resistance of the surface of the wafer can be measured using a four-point probe or Van der Pauw technique [16]. These sheet resistance techniques can be used in-line on product wafers as they are non-destructive, quick and easy to automate. The measurement of the junction depth is slow and destructive, and must therefore be performed on a test wafer.

To obtain further information on the outcome of a diffusion it is necessary to establish the concentration profile of the dopants through the wafer. This may be measured using the spreading resistance technique [17], the Secondary Ion Mass Spectrometry (SIMS) [18], or the capacitance-voltage (C-V) technique [19]. The measurement of the doping profile is normally only used when characterizing or developing a process.

2.3.3. Ion Implantation

Since its inception in the 1960's ion implantation has played an increasingly important role in wafer fabrication, particularly for MOS structures. Implantation is achieved by sweeping an ion beam over the surface of a silicon wafer in high vacuum. The areas to be doped are defined using a masking layer which may be photoresist, oxide, nitride, or polysilicon. The ability of the ions to penetrate the masking layer is dependent on both the masking material and the thickness of the layer. Damage to the silicon lattice during this process can be repaired by a later anneal step.

Ion implantation provides an alternative to dopant diffusion techniques for introducing controlled amounts of impurities into a silicon wafer. As discussed in section 3.2.2 diffusion has a number of disadvantages which make well controlled, uniform and reproducible doping profiles difficult to achieve.

Using ion implantation doping levels can be accurately controlled and the impurity distribution profiles can be adjusted during the implantation process. Processing is performed at low temperatures which also results in little lateral spread of impurities. However, where diffusion may be performed on several hundred wafers at one time and thus has a very high throughput, ion implanters have a much smaller capacity and are comparatively slow to load. Because of their complexity ion implanters also tend to be unreliable and expensive.

For MOS processing ion implantation can be used to perform threshold adjustment, well implantation, and source and drain doping. When higher power implanters are used it is possible to form buried junctions.

Implantation is controlled to the first order by modifying beam-current and beam-energy [20]. The current of the ion beam is used to control the speed at which the wafers are implanted while the energy of the beam defines the depth of the implanted dopant in the wafer.

During ion implantation wafers can suffer from a number of problems which will effect yield. These include surface damage and ion channelling. The former is caused by the impact of the dopant atoms on the wafer surface and is either annealed out or prevented by laying a thin layer of photoresist or oxide over the wafer and implanting through this. The latter occurs when a dopant ion travels between the rows of a crystal lattice deep into the substrate which could make a significant difference to the doping profile of a device. Channeling can also be reduced by growing a thin layer of amorphous material over the wafer surface prior to implantation to de-channel the incident ions.

In a production environment particle contamination, surface charging and wafer heating may be added to the list of potential problems. Particle contamination is the greatest problem as a particle on the surface of a wafer may prevent part of a device being implanted thereby directly effecting yield. Surface charging can occur because of the high electric field present when an ion beam sweeps over a wafer, this can cause non-uniform implantation or trapping of charges in the wafer. Finally wafer heating under the influence of an ion beam can cause warpage and parasitic thermal diffusion.

The implantation of a dopant into silicon is not enough to change its electrical characteristics, the dopant must also be electrically activated. This is achieved by annealing, which puts dopant atoms on substitutional sites and repairs any damage to the silicon lattice caused by implantation. Annealing is performed in a furnace tube, much as for diffusion, but in an inert ambient. Times are normally of the order of tens of minutes and temperatures in the 900-1000°C. Recently a technique called rapid thermal annealing (RTA) has emerged as an alternative to furnace annealing. Here a wafer is heated to a high temperature for a period of seconds by using a high-energy laser pulse. The result is that lattice damage is repaired and the dopant electrically activated with minimal diffusion. This feature is particularly attractive for shallow junction formation.

Many techniques can be used to evaluate the accuracy, uniformity and reproducibility of ion implantation [21]. Four point probing measures sheet resistance on test wafers after an anneal has been performed. Thermal wave analysis measures crystal damage, is non-contact, non-damaging and can be used directly after implantation. Ellipsometry uses optical means to measure the crystal damage caused by implantation. Capacitance-voltage (CV) analysis using test wafers is used to produce dopant concentration profiles.

Other techniques such as spreading resistance probing (SRP) are very useful for supporting development and process characterization.

As ion implantation is used for more and more applications it becomes increasingly important to control the implantations in real time and to increase the throughput of the implanters. The latter is being achieved by applying automation to the transport and loading of wafers. The former however is complicated by the need to integrate in-situ process monitoring data with data collected after the implant to provide feed-back control. This is also resulting in techniques such as thermal wave probing being preferred as an analysis technique because they do not diminish the implanters throughput.

2.3.4. Deposition

The deposition of material films plays many important roles in wafer fabrication. Deposition is used to form layers of material such as silicon dioxide, silicon nitride, polysilicon and metals. Doped oxides can be used as diffusion sources as discussed in section 2.3.2. The method used for deposition varies, but may be classed as evaporation, sputtering or chemical vapour deposition (CVD). Each of these techniques must produce material layers which have good adhesion, are uniform, and have a constant film composition.

Thermal evaporation is the simplest technique for depositing a film. A source material, normally solid, is heated in a vacuum until it evaporates and then condenses on the wafers forming a film. Heating methods include a hot plate or filament and electron bombardment (e-beam). Evaporation is often used for laying down metallization layers which are then etched to become interconnect. The most common material for this purpose is aluminium, which evaporates at a low temperature. However, the uniformity, or step coverage, for thermal evaporation over an uneven surface topography is often unsatisfactory, particularly for the thin metal films required in VLSI applications. Despite this evaporation is still widely used because of its relatively low cost.

Sputtering is a development of the evaporation technique, replacing thermal heating of the source with bombardment by energetic ions. The ions can be generated in a number of ways but two popular methods are ion beam sputtering and magnetron sputtering. In the former an ion beam is directed at the source so that the sputtered material deposits in a controlled manner on the wafer surface. This method has the advantage of producing very pure films, but is slow and therefore has a low throughput. However, it is the second method which is most widely used. Here the atoms are charged to form a plasma glow in front of the target material. The argon ions are then accelerated towards the material which they strike causing sputtering of source atoms that are then directed

towards the target wafers. Magnetron sputtering provides good step coverage and can be controlled to achieve good reproducibility. It also provides a high throughput. Sputtering differs from thermal evaporation in that it can be used to perform well controlled deposition of all materials: metals, alloys, semiconductors and insulators. Damage to the wafer surface caused by sputtering can be removed by a low temperature anneal. For sputtering the deposition rate and final layer thickness can be accurately controlled by varying the substrate bias, the wafer temperature, the pressure inside the chamber and the time.

CVD is widely used for depositing silicon and its compounds on a wafer surface. Like evaporation and sputtering, CVD is performed in a chamber but the source of the deposited material is a gas above the surface of the wafers. The gas is heated so that a chemical reaction occurs depositing a film on the wafers. The most widely used materials for film deposition are single crystal silicon, polycrystalline silicon, silicon dioxide and silicon nitride. These materials can be doped during the deposition process by introducing dopants into the source gas. Some metals and metal silicides can also be deposited using CVD.

CVD can be divided into three basic categories: atmospheric deposition (APCVD); low pressure deposition (LPCVD); and deposition in the presence of a gas plasma (PECVD). High wafer throughputs can be achieved using all CVD techniques making them suitable for volume production.

APCVD is mostly used for the deposition of single crystal silicon, or epitaxial, layers with the same crystal orientation as the substrate. This process is important in bipolar processes but is rarely used in fabricating MOS structures. Epitaxial deposition is commonly performed at around 1200°C.

LPCVD is used to deposit polysilicon, silicon nitride and silicon dioxide. This is achieved at a lower temperature (c. 800°C) and with higher throughput than for APCVD, it also produces layers with better thickness and composition uniformity. The deposition of metals using LPCVD results in better step coverage than can be achieved using evaporation or sputtering and so is the preferred technique when forming multi-layer interconnect.

PECVD allows very low temperatures (c. 300°C) to be used in material deposition by reacting the source gases in a plasma. Silicon dioxide and silicon nitride are deposited using this technique. However, PECVD is a very complex process and therefore more difficult to control than other CVD methods.

Monitoring the growth of thin films during their deposition can be performed using a number of techniques. Quartz crystal microbalance (QCM) technology is often used for measuring deposition rate and film thickness in physical vapour deposition processes, ie. evaporation and sputtering. QCM also has the advantages of not requiring calibration and being inexpensive. Other methods, such as mass spectrometry, measure the partial pressure of the gas species being deposited and infer the thickness and deposition rate. Ellipsometry may also be used to measure the thickness and refractive index of some materials as they are deposited.

Techniques for measuring the thickness of films after their deposition may be classed into those which can be performed on product wafers and those for which a test wafer must be introduced into the process. The techniques used to measure film thicknesses on product wafers all depend on the reflective/refractive properties of the material. These include reflection spectrophotometry, which allows small areas of the wafer to be inspected very quickly but requires empirical calibration, and ellipsometry. Measurements which are normally made on test wafers include electrical techniques, such as four point probing, and destructive techniques.

The move towards sub-micron geometries places harsh restrictions on deposition techniques. For example, they must be low temperature, have uniform step coverage, few process-induced defects and a high throughput. Thus the use of evaporation and sputtering techniques is likely to diminish except where there comparative low cost over CVD systems makes them desirable. For MOS technologies emphasis is most likely to be placed on LPCVD and PECVD.

2.3.5. Etch

Along with lithography (section 2.3.6) etching is used to define the structural elements of devices on a silicon wafer. Thus to fabricate an nMOS device of the type shown in figure 2.1 etching techniques must be used throughout the whole process to selectively remove areas of deposited/grown layers. Etching processes therefore exist to remove all the materials used in wafer fabrication. The method chosen for any particular etch is dependent on the desired shape of the resultant feature.

The most important properties of a feature formed by an etching process are size and profile (isotropic, anisotropic, etc.) but other properties are also important in determining the suitability of an etching operation. These include the uniformity of etch across the wafer, the ratio of the etch rate of the film to the etch rate of the substrate, called

selectivity, and the number of impurities and defects which the operation will introduce. For a production environment throughput is also of concern.

In an nMOS process, for example, etching is used for many purposes: to expose an area of the silicon wafer surface for following ion implantation and oxide growth steps during the formation of a field region; and to remove areas of polysilicon leaving only polysilicon gate regions. However, an etching process cannot be considered in isolation, it must be designed with an understanding of the topography formed by preceding steps and the requirements of the following steps. As an example, a material deposited over an abrupt edge can require over-etching before the process is complete. Alternatively, prior to interconnect metallization, the etch used to open up contact windows must not leave behind sharply defined window edges lest the metal deposited over these edges be prone to breakage.

There are essentially two types of etching used in semiconductor fabrication: wet and dry. Wet etching is the simplest mechanism, here the prepared wafer is dipped in an appropriate chemical solution and remains there until a sufficient amount of material has been removed. Such a process is isotropic and may only be controlled by varying the chemical concentration, the temperature and the time. The rate and uniformity of the etch is also influenced by agitation of the wafers while in the etchent. Chemical mixes have been devised for removing all the material commonly used during wafer fabrication, however care must be taken as some of the chemicals are highly toxic. Because of its simplicity wet etching can have a very high throughput making it an attractive option in a production environment. Careful choice of chemicals can also lead to highly selective etching, although monitoring the rate of etching and the time at which the etch is completed is very difficult. Wet etching may also be non-uniform across the surface of the wafer. As a consequence it may be necessary to routinely over-etch, which along with its isotropic nature makes wet etching unsuitable for defining very small features. However, for more tolerant features wet etching still remains a useful technique.

Dry etching is performed in a chamber where a relatively inert input gas is excited by a plasma discharge producing reactive species that combine with the exposed film to form volatile products which are vented from the chamber. The application of r.f. power to create the plasma also directs the reactive ions onto the surface of the wafer resulting in an highly anisotropic etch. This ability makes dry etching eminently suitable for defining critical VLSI device features such as MOS gates. Dry etching also offers lower chemical costs

and tends to introduce fewer defects than wet etching. However, the selectivity of dry etching is lower than wet etching as reactive ions tend not, for example, to differentiate between silicon and silicon dioxide. Dry etching also suffers from very high equipment costs, although these can be offset by automating the loading/unloading process and, in some cases, using fast single wafer processing to increase their throughput.

Dry etching is classed as either plasma etching or reactive ion etching (RIE). In both cases the wafers are laid out on an electrode with the plasma being generated immediately above their surfaces, they differ in the polarity of their electrodes. RIE etchers also have a lower operating pressure and higher energy ions and are therefore preferred in production environments because of their speed. The actual mechanisms involved in dry etching are complex and not well understood thus controlling the etch rate is very difficult. For both classes of etcher there are the following control parameters: r.f. frequency and power used to excite the input gas; flow rate of the gases (both input and output); and pressure inside the reaction chamber.

Monitoring of the etch rate for wet etching is not normally performed, the time spent by the wafers in the chemical being determined empirically. Visual inspection is then used to check whether the etch has completed over the whole surface of the wafer. In dry etching, however, the end-point of the etch can be monitored using optical emission spectroscopy or mass spectroscopy. These techniques provide information on the concentration of reactant and etch product which change when the film being etched is used up. Laser reflectance techniques can also be used to perform in-situ measurement of film thickness. The end-point detected using these techniques does not guarantee the removal of all the exposed film so it is necessary to add an over-etch period to remove any excess film; it is important that this period be minimised.

With the exception of etching very large features wet techniques are being replaced by dry. The preferred dry technique being low pressure RIE because of its speed and therefore higher throughput. The need to maintain consistent etching from wafer to wafer makes single wafer processing an attractive option, especially if this can be linked with automatic wafer movement and feed-back control based on process monitoring, in order to improve throughput and yield.

2.3.6. Photolithography

In IC manufacturing photolithography is the process by which circuit designs are transferred to the surface of a wafer. It is therefore the means by which a feature of a

device structure, such as the gate in an nMOS device, is defined when its material layer is deposited/grown. Thus it is photolithography which controls the functionality and geometric features of the final devices.

Photolithography consists of a number of steps, first the deposition of a photo sensitive resist that is exposed to a light source through a mask upon which is patterned the design for the current material layer. The wafer is then immersed in a developer to remove the exposed areas of resist leaving a patterned masking layer on the surface of the wafer. This may then be used to define doping regions in the material layer below by performing ion implantation or deposition, or to define the areas on the wafer which are to be etched. After this operation the remaining resist is stripped. For a review of the photolithographic process see Stevenson and Gundlach [22].

It is important that the times and temperatures used during the bake operations are accurately controlled, otherwise the resist may not have the correct adhesion characteristics. The spin speeds used when applying the resist are also of importance because these will influence the thickness and uniformity of the resist. These parameters are normally set when the materials and machinery are characterised and so are rarely modified in a processing environment. The only monitoring which is performed is visual inspection of the success of the develop and resist strip steps. If these are found to be unsatisfactory the development/strip time can be extended. In the case of the develop step completely failing the resist can be stripped and the photolithography sequence repeated.

Numerous exposure techniques have been developed for transferring the design on the mask to the wafers surface. The choice of exposure technique depends on both technical and economic factors. The basic requirement is that it must be capable of achieving the resolution and registration tolerance demanded by the product, at an economic yield. Most presently available exposure techniques are optical, though x-ray and ion beam lithography are being used. Of the optical techniques contact printing has been the most widely used. Here the mask, which contains the design pattern for the whole wafer, is brought into contact with the surface of the wafer during the exposure step. Though this method offers very high throughput and good optical contrast, the intimate contact between mask and wafer causes damage to the wafer surface that can result in significant yield loss for small geometry circuits. An alternative is to have a reticle, containing the design for one IC imaged directly onto the wafer surface at each site. This is called direct step on wafer (DSW) and offers very good resolution, i.e. fine control of critical dimen-

sions, and copes well with distortions of the wafer that can occur during processing. Thus a better layer-to-layer registration is possible than with contact printing. The drawbacks associated with DSW machines are their low throughput and high cost, although for small geometry circuits these additional costs are justified by the higher yield that can be achieved.

The primary measurement used for monitoring the photolithographic process is the linewidth of a track in the developed photoresist. This measurement is used to check the resolution and minimum geometry of the lithographic step. Measurement techniques are either optical or electrical. The majority of optical linewidth measurements being based on optical microscopy. Electrical measurements of linewidth are normally performed during parametric test using extended Van der Pauw structures [23].

The requirement to produce smaller geometry devices forces tighter tolerances on the alignment accuracies of masks/reticles and linewidth measurements. As a result, DSW machines with automatic alignment mechanisms will probably continue to replace contact printers.

2.4. Process Integration

The purpose of IC fabrication is to produce complex systems of circuitry, in high volume, that perform to a set of predefined electrical characteristics. This is achieved by processing a batch of wafers, in this case silicon, through a series of process steps of the type described in section 2.3. Together these steps form the features of devices, interconnects and isolation regions of the type shown in figure 2.1. Though a typical process may consist of hundreds of process steps performed one after another, many are performed cyclically as illustrated in figure 2.3. The outcome of the fabrication sequence is a batch of wafers upon which have been formed circuits with the structural and electrical characteristics intended by the designer.

It is essential that during the process sequence a batch of wafers pass through the process steps in the correct order and that the control parameters of the machinery have the appropriate settings. In order to be able to verify each operation performed on this batch and monitor the performance of the processing equipment measurements must be made on the wafers. This information must then be maintained in an accessible format. In the EMF this role is satisfied by the *runsheet* which contains the recipe information, including control parameter values, for a process. A runsheet is produced for each new batch and then travels with it throughout its fabrication sequence. As the batch passes through the

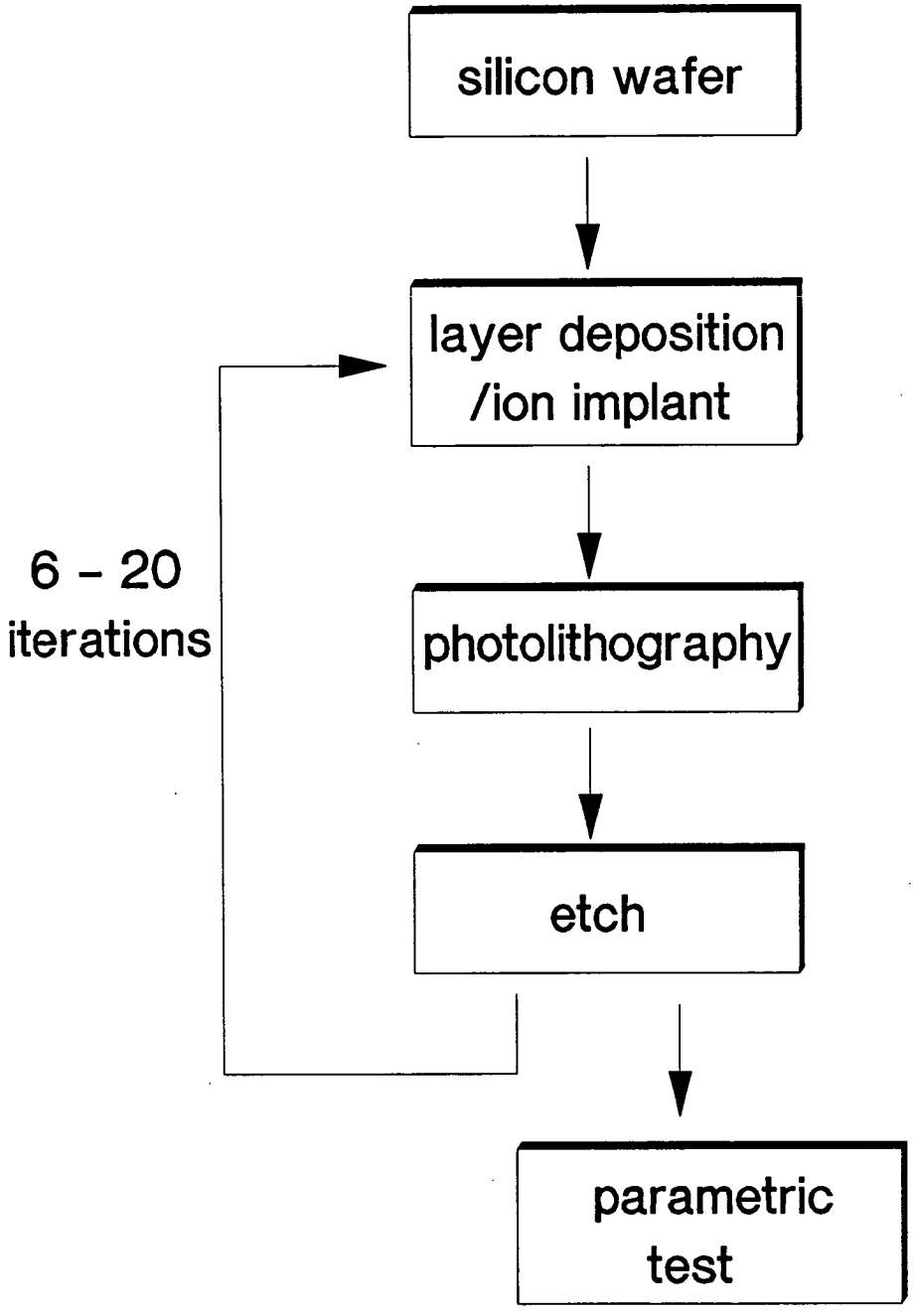

Figure 2.3 MOS wafer fabrication sequence.

process steps the control parameters for each operation are taken from the runsheet. When the measurement of a parameter is specified, that value is noted down on the runsheet. Once a process step has been completed the runsheet is signed by the operator and the batch can then progress onto the next step. In this way the runsheet serves to document the processing history of a batch.

Thus for a low volume research establishment such as the EMF the runsheet is an excellent method for the basic tracking of production. However, the runsheet is of limited value for more demanding production environments. This is because it is not flexible enough to represent the full range of information which a manufacturing facility could produce and by itself would not be suitable for disseminating processing information to all those who might require it. Nevertheless, the process runsheet represents a formal definition of an integrated process. It can therefore be used to demonstrate the interrelation of process steps and the information generated in controlling a process flow.

2.4.1. The EMF 1.5μm nMOS Process

A 1.5μm nMOS process was developed for the EMF in 1986 by Z. Chen, A. Gundlach and others. Although full processes of this geometry had been reported previously [24] no complete description of the process recipe was available. As a result this process was developed from a 6μm nMOS process already in use at the EMF [25]. The process produces self-aligned MOS structures with a polysilicon gate and a single metallization layer.

nMOS transistors consist of source, drain and gate regions, isolated by thick field oxides. They operate by causing a negative charge to move from source to drain in response to a positive charge on the gate. If the charge on the gate is sufficient to increase the gate-to-source voltage above a threshold voltage (V_T) electrons are attracted to the region under the gate forming a conducting path between source and drain [26]. If V_T is greater than zero then the devices are enhancement mode; if less than zero then they are depletion mode.

The process comprises seven photolithographic stages and is based on lightly doped p-type wafers. The first steps of the process lay down an initial pad oxide and a silicon nitride layer. Areas of the wafer are then exposed through these layers using the 1st PHOTO (figure 2.4a). In these areas a boron implant is used to create a channel stop region for the following field oxide. The 2nd PHOTO serves to define the depletion gate region, which is doped using doubly ionized arsenic implant (figure 2.4b). A sacrificial

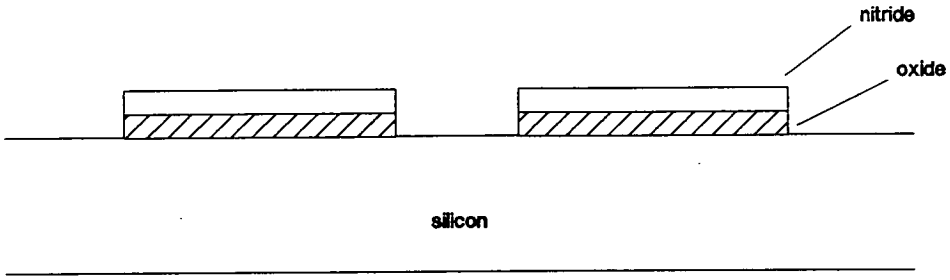

Figure 2.4a nMOS section after 1st PHOTO.

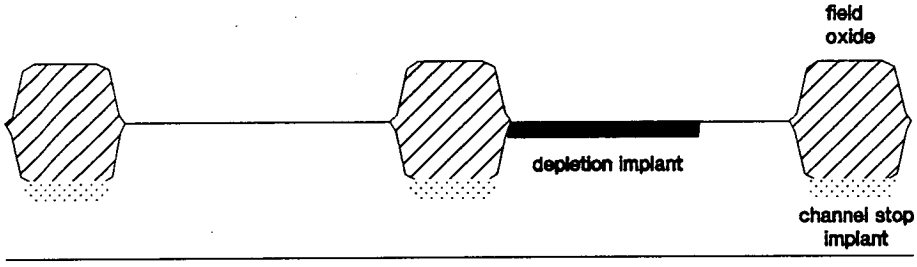

Figure 2.4b nMOS section after 2nd PHOTO.

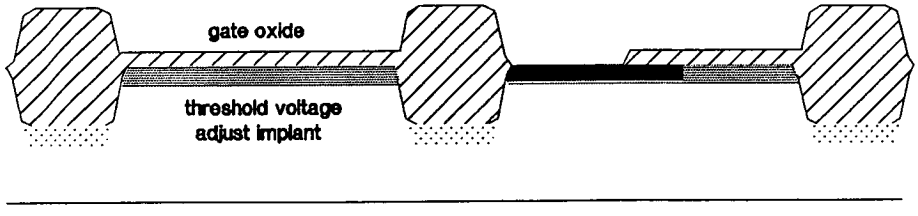

Figure 2.4c nMOS section after 3rd PHOTO.

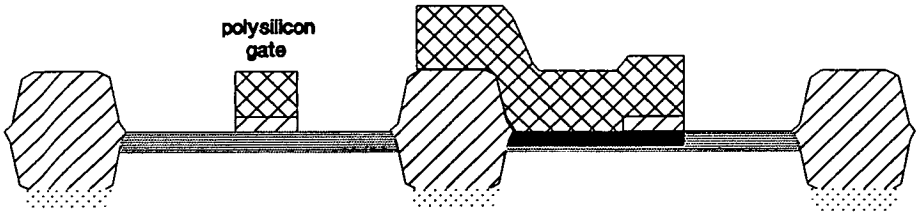

Figure 2.4d nMOS section after 4th PHOTO.

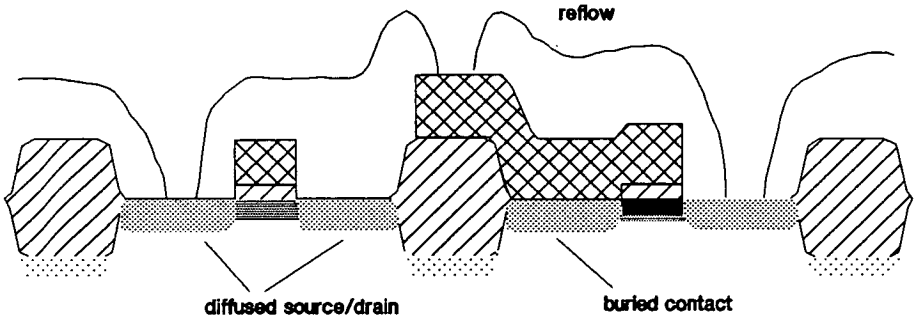

Figure 2.4e nMOS section after 5th PHOTO.

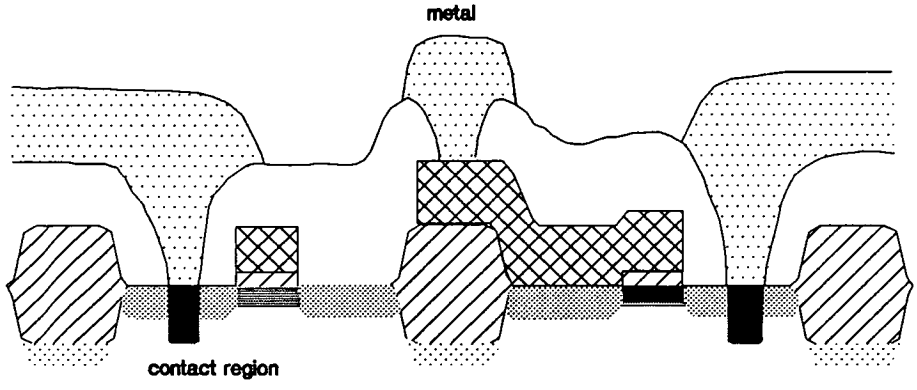

Figure 2.4f nMOS section after 6th PHOTO.

oxide is then grown and etched prior to the growth of a high quality gate oxide. The areas to become buried contacts are then exposed using the 3rd PHOTO (figure 2.4c). Two boron implants - one low energy, one high energy - are then used to adjust the threshold voltage and reduce the likelihood of punch-through occurring. After this a phosphorus doped polysilicon layer is deposited to form the self aligned gates. The 4th PHOTO defines the regions in which the polysilicon and oxide should be removed, in particular the source/drain regions (figure 2.4d). An arsenic implant is then used to create the n^+ source/drain regions. Following an anneal to electrically activate these regions a protective pyro glass is deposited across the whole wafer. High temperature reflow steps are then performed to redistribute the dopants introduced into the substrate by earlier steps. A 5th PHOTO mask defines the areas where metal contact will be made to the diffused regions and the polysilicon (figure 2.4e). Phosphorus is then deposited to reduce the sheet resistivity of the contact regions. A layer of aluminium is then evaporated over the wafer and a 6th PHOTO defines the interconnection pattern (figure 2.4f). Finally a sintering step is performed. A two dimensional cross-section of the type of structures resulting from this process is shown in figure 2.1.

Once fabrication is complete, parametric tests are made on standard test structures which are included on a strip along the top of each chip design [27]. Test structures include standard devices, resistor chains, capacitors and ring oscillators. The measurements made on these structures are used to establish whether the fabricated devices will meet their specifications.

2.4.2. The Process Runsheet

The runsheet for the EMF 1.5μm nMOS Process is listed in appendix A. When a runsheet is initiated with a batch, that is the batch identification and masking information are entered on it, it becomes the source for a set of information components. These components are as follows:

- The starting materials.
- The order of processing.
- The equipment to be used.
- The equipment control parameters.
- Actions to be performed with the processing equipment.

- Masking information.
- Inclusion of test wafers.
- Inspection and measurement instructions.

The completed runsheet also acts as a repository for other information:

- The size of the batch.
- Monitoring data.
- Starting dates and times for process steps.
- DC electrical parametric test data.

All this data can then be associated with either the Facility, the Product, the Process or the Batch. Figure 2.5 shows how this classification can be applied to the start of the runsheet.

In addition to processing data the runsheet implicitly describes the interrelation of the process steps. For example the FURNACE 7 (STEAM) process step is performed to provide a masking oxide for the IMPLANT PHOSPHORUS n-well definition implant. The definition of the areas to be implanted being provided by the 1st PHOTO lithography step, an etch and a resist strip.

Towards the end of the runsheet the ELECTRICAL TEST step is used to collect parametric test data. No specification of the measurements, etc. is provided in the runsheet as the measurements are performed using automatic test equipment (ATE). This equipment stores the test data and provides some basic analysis software to produce trend charts and wafer maps.

The runsheet can be used to control/track a process sequence that has been modified in-line. However, applying overrides to the runsheet instructions as paper addenda is an ad-hoc approach that can only work effectively in research environments. In a production environment such an approach would become cumbersome and impossible to schedule for, thus reducing flexibility and efficiency.

2.5. Summary

In this chapter we have evolved a view of silicon wafer fabrication based upon the function and information content of the process-steps involved. The information content consists of the input control parameters, or recipe, and the engineering data which can be

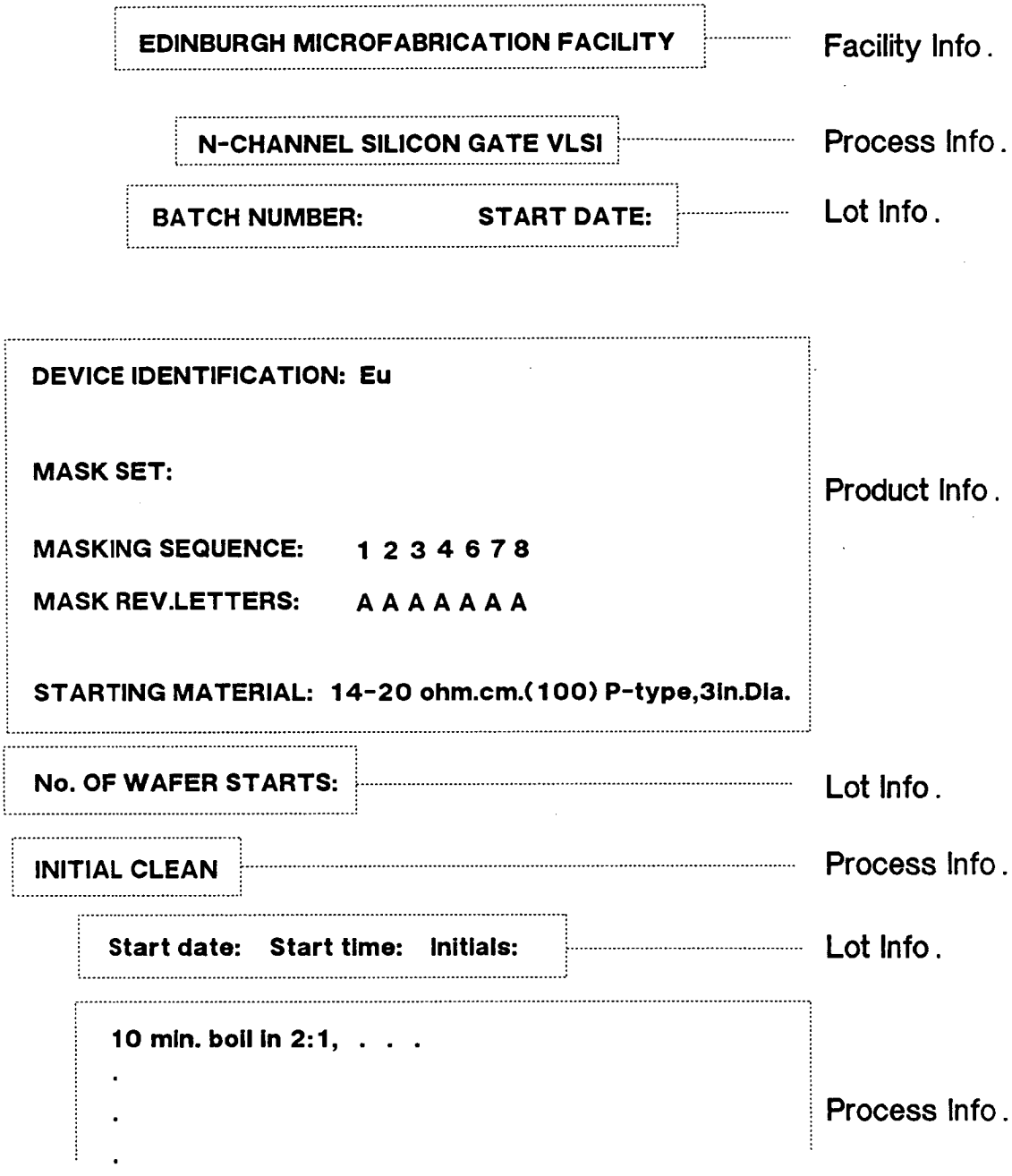

Figure 2.5 Information content of nMOS process runsheet header.

collected to monitor the operation of the processing equipment and verify the processing performed.

As an example of this the EMF 1.5 μm nMOS process has been described in term of its runsheet. The runsheet, it has been noted, is a method of lot tracking, recipe control and processing history maintenance. When analysed it can also produce a significant amount of information on the functionality of the processing equipment, i.e. non-lot tracking. The limitations of this approach have been pointed out: it is suitable for a research facility but does not offer the integrity and consistency of data which is required in a production environment.

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Chapter 3

Computer Aided Manufacturing

3.1. Introduction

Computer aided manufacturing (CAM) systems are widely used to improve the efficiency of manufacturing processes. This they achieve by providing structured storage of manufacturing information with the software tools to manipulate and present that information. The success of CAM as a technology is demonstrated by its application in many environments [1]. Though all CAM systems are designed to perform production control, their implementation differs greatly between industries so that they can satisfy the needs of their particular manufacturing environment.

There is no definitive statement that can be made about the features which constitute a CAM system. In some industries CAM means little more than computer numerically controlled (CNC) machinery, although now the general consensus is that CAM must also encompass factory management as well as manufacturing control [2]. For the purpose of this thesis a CAM system will be regarded as being able to perform the following functions:

- Collect manufacturing information.
- Aid decision making.
- Disseminate directives and control information.

To meet these requirements a CAM system must support the following features:

- A structured user interface.
- A database.
- A set of application programs for database interrogation and data presentation.

A system which exhibits these features is potentially very sophisticated and should be regarded as a major component of any computer integrated manufacturing (CIM) system.

This chapter presents an overview of CAM systems as they are currently used in the semiconductor industry. Where relevant comparisons are drawn with the application of CAM in other industries. COMETS is introduced as an example of a commercial CAM system that has been designed for use in semiconductor manufacturing. Its major functions are discussed with a critical analysis of how these can be used to enhance production control. Finally, an approach to implementing CAM systems is described; using the application of COMETS to the Edinburgh Microfabrication Facility (EMF) as a case study.

3.2. CAM for the Semiconductor Industry

CAM represents a major component of any semiconductor manufacturing facility. Throughout IC manufacturing (fabrication, assembly and test) CAM systems are used to plan, schedule, track and control production. In particular wafer fabrication has acted as a focus for CAM system implementations as improvements in throughput time and yield have a large bearing on the cost effectiveness of a facility. This is a consequence of the sharp increase in value of product as it is fabricated. For example, a single six inch wafer can increase in value more than a thousand-fold during a state-of-the-art process. Therefore, the following discussion of the role of CAM in the semiconductor industry will concentrate on its application within wafer fabrication.

All IC fabrication facilities have a set of common characteristics [3], such as:

- Large capital investment.
- High process complexity.
- High information content.
- Long throughput time.

Evidently performing production and process control in this environment is a task which will make demands on manufacturing control systems that go far beyond those of other industries. The result has been the evolution of specialised systems that provide not only the necessary functionality but maintain, and make accessible, the large amounts of data which are needed to analyse and control IC production.

In order to meet the requirements of present-day IC manufacturing a CAM system

must satisfy the definition of CAM given in section 3.1 but must also provide the following functionality [4]:

- Production planning.
- Scheduling of processing, including equipment utilization and wafer transport.
- Work-in-progress (WIP) tracking.
- Engineering data collection and analysis.

Thus we form a description of a generic semiconductor CAM system of the type shown in figure 3.1.

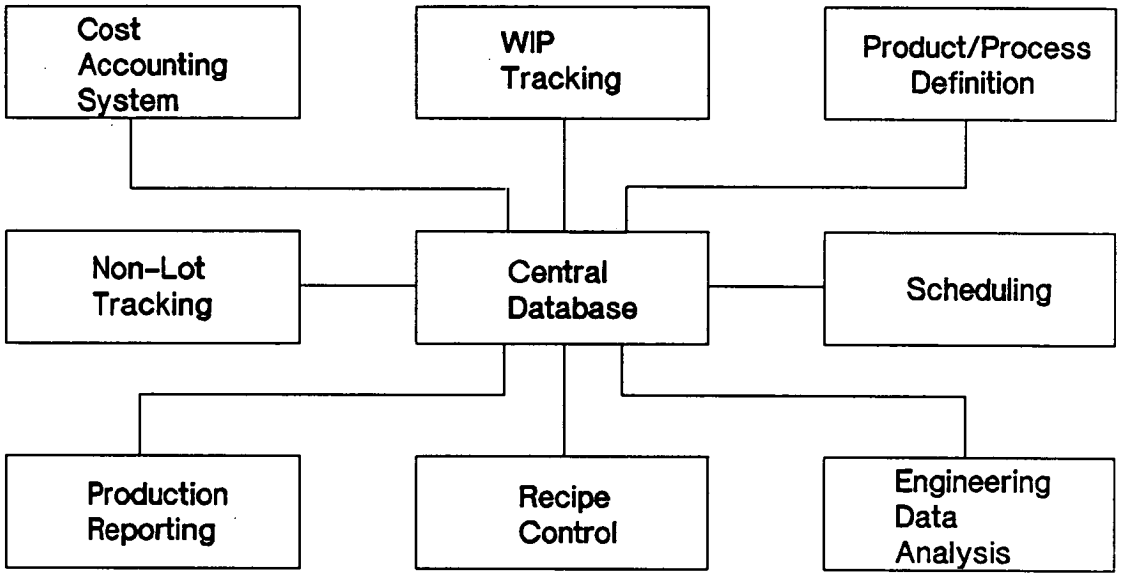

Figure 3.1 Functional model of generic semiconductor CAM system.

Here a set of functional modules share the resource of a common central database. Within this database the products to be fabricated are defined along with the fabrication processes. This allows the sequence of process steps, through which a batch of product wafers passes, to be regulated. The processing applied to each lot can be specified by a recipe management system. Tracking of lot movement, or WIP, through a facility creates within the database a representation of the distribution of product through a facility. When combined with the collection of engineering data, this allows process monitoring

and control to be performed. In addition, non-lot tracking can also be used for facilities and equipment monitoring. Therefore with all product/process and facility data accessible from the database it becomes possible to perform: planning; scheduling, of processing and maintenance; and production reporting.

In order for a database to support these functions it must be secure, to prevent unauthorised access to important information and prevent accidental corruption of data. This is normally performed by a database management system (DBMS) which controls access to the database thus maintaining security and data integrity.

The user interface of a CAM system is also very important as it provides easy and comprehensive access to the functionality of the system. Interfaces should also be consistent and logical to promote familiarity and thereby avoid the need for users to constantly 're-learn' the systems.

Most IC fabrication can be classed as belonging to one of two types[†]: commodity or application specific. The difference between these approaches to production results in very different demands being made on their manufacturing control systems. However, as has been indicated, there are certain common goals. These include performing the correct processing on the correct lot, and maximizing equipment utilization. The CAM systems differ in the way they represent production, which is reflected in the design of their databases.

Commodity production, as typified by memory IC manufacture, is currently the largest sector of the semiconductor industry [5]. Very high throughput volumes, with few products and often only one process, result in a stable manufacturing environment. This allows processes to be tuned over time to maximise yield and maintain a consistent distribution of product throughout the facility. Consequently production planning is simplified and scheduling is used primarily to take account of equipment downtime. Production lots normally contain only one product which increases productivity and allows engineering data to be collected on a simple per-lot basis. Hence, very few demands are made on the flexibility of the CAM systems; emphasis being placed instead on reactive WIP tracking, data collection and production reporting. The exception to this condition is when a new process, which has not been developed within the production facility, is implemented. This generally requires many man hours and much experimentation to tailor the process to the particular facility. As a result the CAM system is not generally used to control the

[†] As discussed in Chapter 1.

implementation, the new process data is simply entered into the system once the implementation has been completed.

Describing a commodity process within a CAM system equates to defining a set of manufacturing data objects. As indicated in figure 3.2 this would include: a product in terms of its name and type; the process steps which the product must be pass through and the order in which this must happen; the processing equipment; the processing recipe specifications; the lots which must be created and moved through the process; the engineering data which must be collected for each lot; and the engineering data which is associated with the equipment. With this information the functional modules of the CAM system can be used to track, plan/schedule, and interrogate the manufacturing facility.

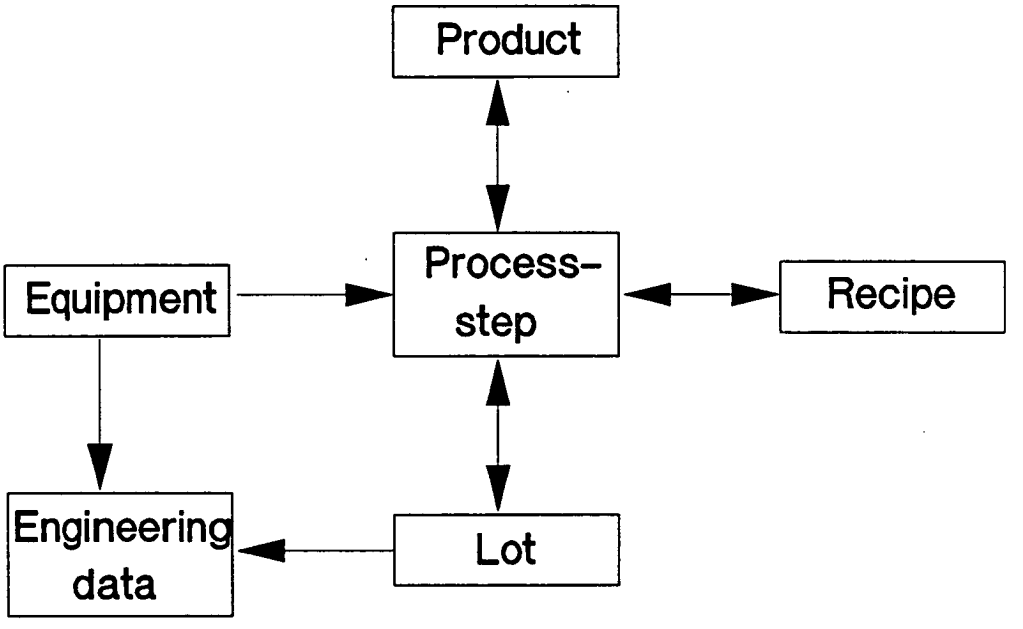

Figure 3.2 Data objects and relations required to define a commodity process.

Application specific production is playing an increasingly important role in the semiconductor industry and are likely to continue to do so [5]. In contrast to commodity manufacture, application specific production is often performed in lower volumes with a higher product mix and potentially many processes. Batches tend to be smaller and can have a mix of product across the lot and even across each wafer. In the case of gate arrays, for example, lots are partially processed and then broken up or combined for the committal stage of their manufacture. Evidently great flexibility of the manufacturing

environment is required to minimise lead-times and satisfy demands for short cycle times but it is difficult to reconcile this with achieving a high productivity. It is also important that acceptable yields must be guaranteed at the wafer level [3]. For example, where a customers requirement for a particular product is quite low the design may only be fabricated occasionally. In this case misprocessing must be avoided as this could put back delivery time of the product by several weeks. Therefore both product and process must work right-first-time [6]. All these factors complicate the tracking of product, the scheduling of production, and the control of processing [7].

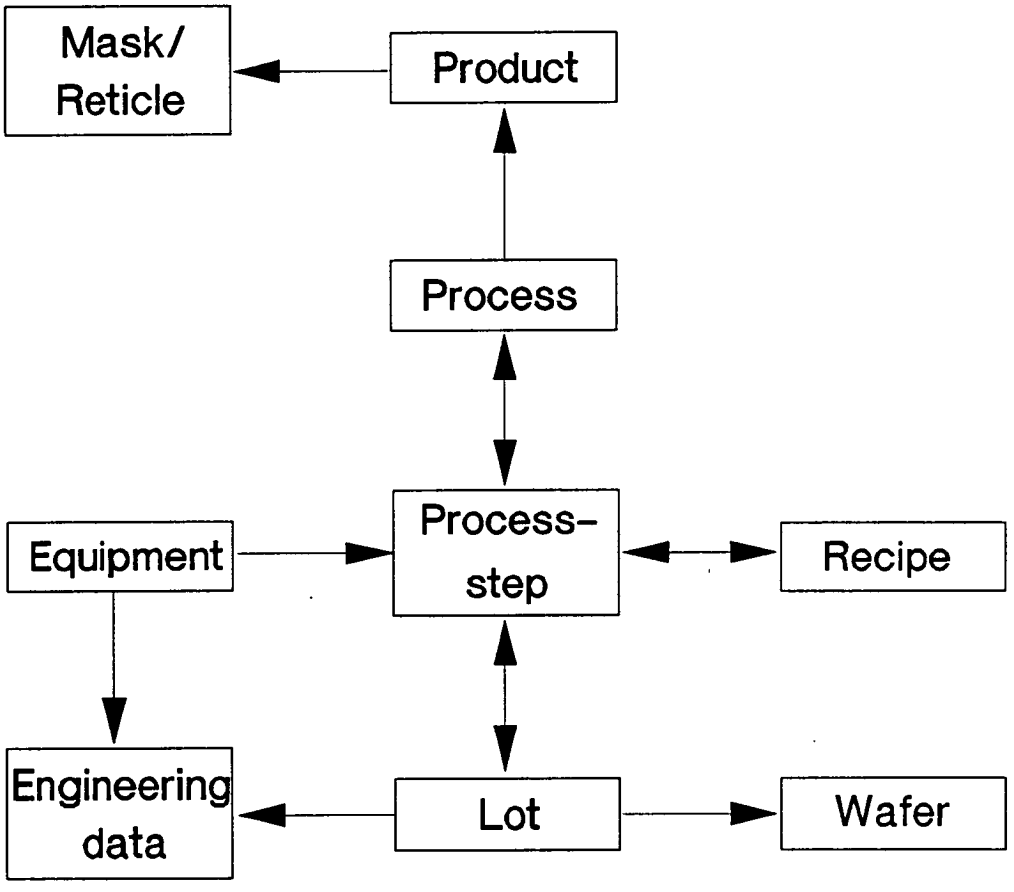

Figure 3.3 Data objects and relations required to define an application specific process.

To represent an application specific process within a CAM system requires a data model which is more complex than that described for commodity production. Figure 3.3 shows the enhanced data model. New data objects include a process entity, a wafer entity, and a mask/reticle entity. Functional CAM modules will now be able to access data relat-

ing to the processing of individual die and wafers as well as lots. This data will then also be related to the mask/reticle used to make the product. The presence of a process entity is important as it allows new products and modified processes to be introduced into the fabrication facility without requiring a CAM system expert to define them.

Currently there are many semiconductor CAM system in use around the world, some developed in-house others by dedicated software companies. However, the expense involved in developing state-of-the-art CAM systems that provide a real competitive advantage has made in-house development impractical and forced a consolidation of the market around a few commercial systems, the most prevalent of which are COMETS followed by PROMIS [8].

Benefits which have been attributed to existing CAM systems include [9]:

- Fewer misprocessed lots.
- Lower WIP.
- Shorter cycle times.
- Reduced lead-times.
- Increased equipment utilization.
- Improved yield.

All of these points have a strong bearing on the economic viability of a wafer fabrication facility. In particular, reduction in WIP has shown dramatic effects on lower reject rates and increased output [10]. However, current CAM systems are all inherently reactive and so cannot be used to perform on-line analysis and control of IC processing. The result is that though they may be suitable for commodity production they are unable to offer the kind of process analysis and control required for efficient application specific production.

3.3. A Commercial CAM System

COMETS (Comprehensive On-line Manufacturing and Engineering Tracking System) was developed in the mid nineteen-seventies by Consilium Inc. as a factory shop-floor control system. Since then it has become widely used throughout the semiconductor industry for many facets of facility management. As a CAM system it has proved to be adaptable enough to be used for all phases of semiconductor manufacturing from mask making through wafer fabrication, assembly, test and store. In recent years it has also been

implemented by other industries, such as aerospace and chemical, where tracking individual batches of product is also essential to controlling manufacture.

COMETS was developed primarily for production scenarios where a range of products are each manufactured with their own fixed set of operations. This is suitable for assembly, test and commodity style wafer fabrication but less so for wafer fabrication when there is a changeable mix of products and processes.

The major functions of COMETS are [11]:

1. Tracking of all WIP, operators, machines, fixtures and tools in a facility.
2. Control of manufacturing based on process specifications.
3. Down-loading of control instructions for automated equipment.
4. Data collection for quality control, production control, engineering and management.
5. Planning and scheduling to determine processing priorities and meet production schedules.
6. Costing of the manufacturing sequence so that forecasts can be made on the financial impact of modifying production.
7. Reporting on the state of the production facility.
8. Communication to inform key personnel of events that occur within the facility.
9. Analysis of data stored within the system, using third-party software.

COMETS consists of a set of functional modules which share data through a central database. These modules relate loosely to the generic CAM system layout of figure 3.1. Processing is defined using the WIP and SPC modules. The tracking of lots, equipment, etc. is performed by the WIP and NTC modules. Engineering and facilities monitoring data are collected by the EDC and MDC modules. Production control is distributed amongst a number of modules including EDC, where engineering data is collected, and SQC where statistical routines are used to analyse production data for control. Tools for automating manufacturing are provided by the PAM module. Planning and scheduling as provided by CWP, APD and SIS can be used to establish a master schedule for a company and determine the priorities and kind of work that need to be performed within each production site to meet this schedule. For each facility the movement of lots can then be

dynamically scheduled to take account of work loads and equipment availability. This segmentation of scheduling into a hierarchy simplifies implementation as it matches the organizational structure of a company, so the people responsible for the success of the work being scheduled are actually in control of the scheduling [12]. The aim of using these tools is to increase the efficiency of the facility by maximizing equipment utilization, improve line balancing, reduce throughput times, and enhance the reliability of production. However, scheduling remains a complex problem because of the difficulty of defining criteria by which a schedule can be considered optimal, and the dynamic nature of wafer fabrication where unexpected events, such as equipment breakdowns, occur at frequent intervals [13]. Calculating the cost of production and forecasting how the changes to the manufacturing sequence will effect this are carried out by the CAS module. This is achieved by simply assigning a fixed cost to each process step. Reports on any information held in the database can be generated using the appropriate functions which are spread throughout the system [11]. Communication, using both VMS mail and messages written to the COMETS screens, is performed using the FCM module. Finally, analysis of information stored within the database is provided by third-party software, such as RS/1 for engineering analysis and Datatrieve for data manipulation and report generation. Table 3.1 lists and briefly describes each of the COMETS modules.

The COMETS database acts as a medium for sharing the data required by the functional modules, and maintains historical data. Therefore the database serves to characterise the production facility for which it has been implemented. The structure of the database allows this by having data objects which relate to physical entities within the manufacturing environment. For example, a product within a facility will have a corresponding PRODUCT data object within the database. Any processing information that might be used to define the manufacturing sequence used for this product is associated with the PRODUCT data object.

Figure 3.4 shows the relationships that exist in the database between the physical entities used to model wafer fabrication. The purpose of the data objects depicted here are discussed in sections 3.3.1 through 3.3.5.

Additional flexibility is built into the database by the General Tables System (GTS) which is used to, amongst other things, define general classes of data objects against which specific objects can then be verified. For example, if data were being collected on a particular machine then when an operator enters this data the name and type of machine

Module	Function	Description
APD	Activity planner and dispatch	Define production schedules and monitor work
BOM	Bill of materials	Maintains lists of components required to build or assemble products
CAS	Cost accounting system	Provides costing information for process manufacturing
CWP	Company wide planning	Coordinate master schedule across facilities
EDC	Engineering data collection	Collects engineering data at a process step
FCM	Factory communications	Handles inter personnel mail and message passing, also notifies of error conditions occurring
MDC	Monitored data collection	Collects data being monitored by external systems
NTC	Non-lot tracking	Tracks movement and utilization of equipment and people
PAM	Process automation	Communicates with automated processing equipment
SCR	Script	Used to define steps to be performed at an operation
SIS	Short interval scheduling	Generates processing order for lots at equipment
SPC	Specification	Presents processing instructions to an operator at a process step
SQC	Statistical quality control	Monitors and analyses data as it is collected
WIP	Work-in-progress	Defines production sequence and tracks lot movement

Table 3.1 The COMETS functional modules and their application areas.

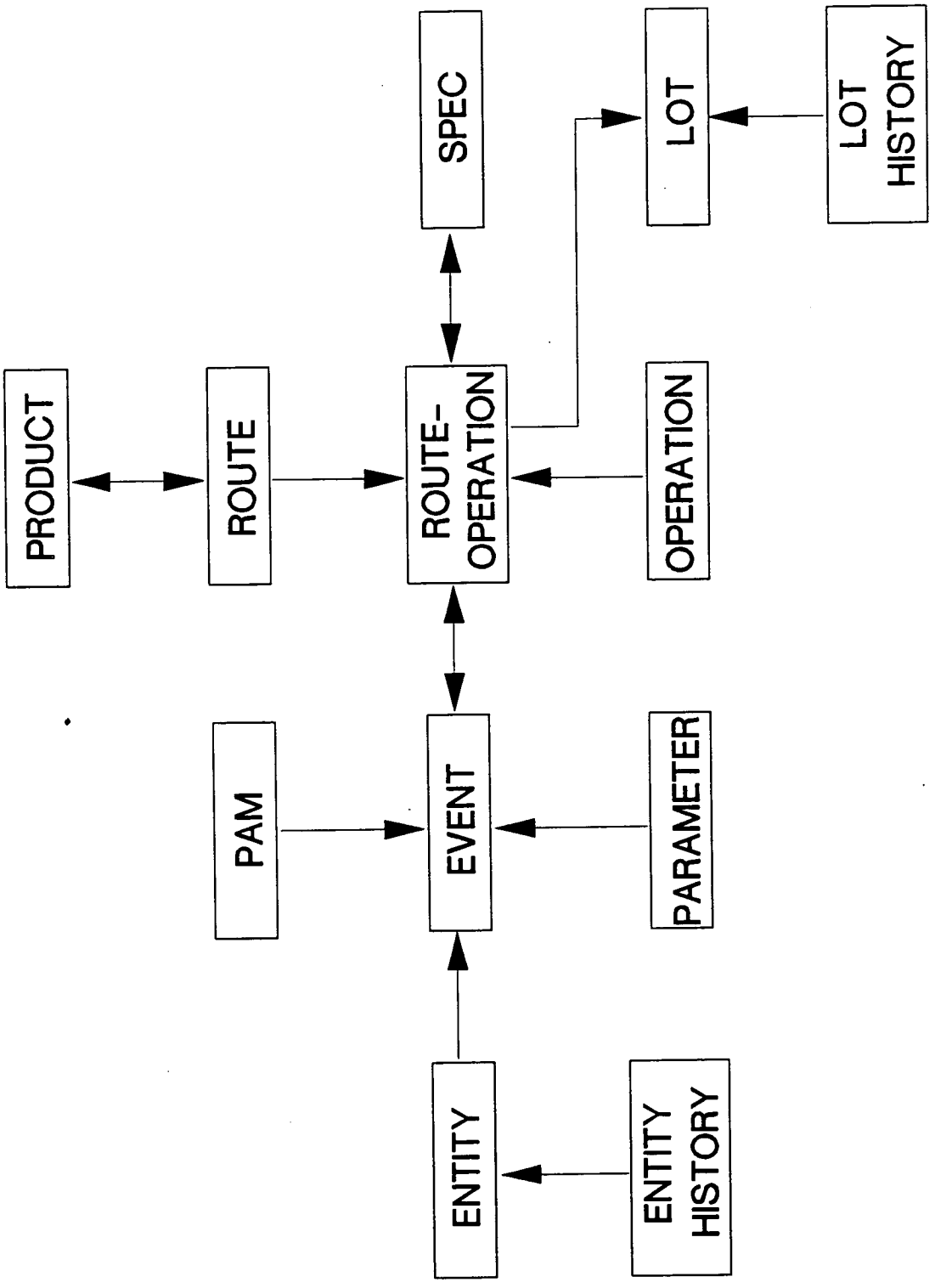

Figure 3.4 Data model of objects used by the COMETS database to represent wafer fabrication.

could be verified against a predefined set of known machines in a GTS table.

```
CMI001S                    COMETS MASTER MENU (CMIM)          SYS 11/10/89 16:44:34
EDINBURGH UNIV.                        EMF
                                    FUNCTION..____
                    WIP TRACKING MAIN MENU.....(WIPM)
                    SPECIFICATION MENU.....(SPCM)
                    COSTING MAIN MENU.....(CSIM)
                    GENERAL COMETS MAINT & UTILITIES MENU...(GCMM)
                    COMPANY-WIDE PLANNING MAIN MENU.....(CWPM)
                    ACTIVITY PLANNER/DISPATCH MAIN MENU.....(APDM)
                    SHORT INTERVAL SCHEDULING MAIN MENU.....(SISM)
                    FACTORY COMMUNICATION MAIN MENU.....(FCMM)
                    NON-LOT TRACKING(TM) MAIN MENU.....(NTCM)
                    PROCESS AUTOMATION MANAGEMENT(TM) MENU..(PAMM)
                    ENGINEERING DATA COLLECTION MAIN MENU...(EDCM)
                    STATISTICAL QUALITY CONTROL MAIN MENU...(SQCM)
                    SUPERVISOR STATUS BOARD MAIN MENU.....(SSBM)
                    FACTORY MONITOR BOARD MAIN MENU.....(FMBM)
                    VAX UTILITIES MENU.....(VAXM)
                    CHANGE LOGON/FACILITY.....(LOGN)
                    LOGOFF COMETS.....(FIN)
RETURN = PROCESS
```

Figure 3.5 COMETS main menu screen.

The interface used by COMETS is menu based. The structure of these menus is such that a hierarchy of menus exists for each functional module. The main COMETS menu is shown in figure 3.5. It is evident that this menu has a very definite structure; it consists of time and date information, the name of the current menu screen, a decision line upon which a four letter abbreviation of one of the possible choices should be entered, two message lines on which warnings and special instructions are given, and a number of special functions, which normally include HELP and EXIT. HELP is used to gain more information about the current menu screen and the functions it makes available. EXIT is used to move up to the screen in the hierarchy on which the current screen is defined, in the case of the main menu this is the log-on screen. The same menu structure is used for all COMETS screens so that if a user is familiar with one module then he, or she, can use another module without having to learn a new interface.

Customization of COMETS can be achieved by modifying the GTS or special parameters set aside by Consilium. Alternatively additional programs can be linked into

COMETS by attaching these to the *user-exits* that Consilium have inserted into certain COMETS programs. User-exits are guaranteed not to be modified or removed by system upgrades.

COMETS is available to run only on Digital Equipment Corp. VAX computers under the VMS operating system. It also depends on the layered products DBMS manager, which is a hierarchical database, and CDD, which is the data dictionary used to generate the data structures within the database. COMETS itself is written in Cobol.

3.3.1. WIP Tracking

WIP tracking is an important feature of a CAM system in environments where it is essential to be able to identify all product within a manufacturing facility. For microfabrication, CAM systems must be able to guide and track the movement of lots. The objective is to be able to specify the fabrication sequence for each lot and then be able to view the status of the facility by looking at how far through its manufacturing sequence each lot has progressed. If required, more detailed production information can be obtained by defining the basic trackable unit as a wafer rather than a lot.

The COMETS WIP module [14] is used to track lots, and potentially wafers, through a facility. When setting-up a new fabrication facility, functions exist in the menu structure to allow the definition of products, the production sequence, and the lots to be fabricated. The manufacturing environment is represented within the database as a set of data objects with constraints on their relationships. The first object to be defined must be the FACILITY, for which PRODUCTS can then be created. Processing is broken down into a series of steps, each of which can be represented by an OPERATION. An example of such a step would be an oxidation, or the spinning on of resist. These steps can then be grouped into ROUTES, such as a photolithographic sequence. An individual process step is uniquely defined as the combination of ROUTE and OPERATION; a photolithography ROUTE could include one of a number of resist spin OPERATIONS, while a particular resist spin OPERATION could belong to a number of photolithography ROUTES. Figure 3.4 shows the relationships between these data objects within the COMETS database.

When a lot is scheduled for production it is created within the CAM system as a LOT and then moved from ROUTE-OPERATION to ROUTE-OPERATION. This is performed using the functions provided within the menu hierarchy. Normally the movement of lots is carried out by operators who are informed by the system which step is to be performed next and when processing is complete are prompted to provide data on any

wafers removed from the lot, added to the lot, or assigned for rework. Additional functions are available to specify that lots are being split, merged and reworked. As processing proceeds a LOT HISTORY is developed for each LOT. The LOT HISTORIES contain all the information on the status of each lot and how this has changed during fabrication. The LOT and LOT HISTORY data objects and their relationships are shown in figure 3.4 along with the data objects used to define the production sequence.

The functions provided by the WIP module are grouped together within the menu hierarchy according to their usage. The product/production definition functions are on one set of menus, the processing functions on another, and the reporting functions separate again. Figure 3.6 shows the structure of the WIP module menu hierarchy. This segregation of functionality makes the system both easier to use and more secure.

3.3.2. Recipe Management

Recipe management within a CAM system allows the presentation of process specification data to operators to be associated with WIP tracking. This has the advantage that when a lot is moved-in to a process step the appropriate recipe is displayed, thus helping to reduce misprocessing. Security over access to process recipes is also easier to control if a comprehensive recipe management facility is available.

Within COMETS recipe management is performed by the SPC module [15]. The menu hierarchy of the SPC module provides functions for the definition of SPECS, which are associated within the database with ROUTE-OPERATIONS. These SPECS represent the actual processing to be performed and so complete the definition of processing within the database. However, the recipe data which is presented to an operator is in fact stored within text files, of which only the file name is stored within the database. Security over these files is maintained by limiting access to the directory in which they are held.

Maintaining process recipes within text files affords a great degree of flexibility in the formatting of the data. Commonly these files are used to store safety information, equipment set-up instructions and equipment control parameters. Overriding the data within these files is allowed only if the name of a file containing the override text is specified in the file. Once a SPEC file has been created, COMETS functions are used to validate the contents of the file, and freeze it so that unauthorised modification of the file is prevented. The SPEC can then be used as part of a production sequence.

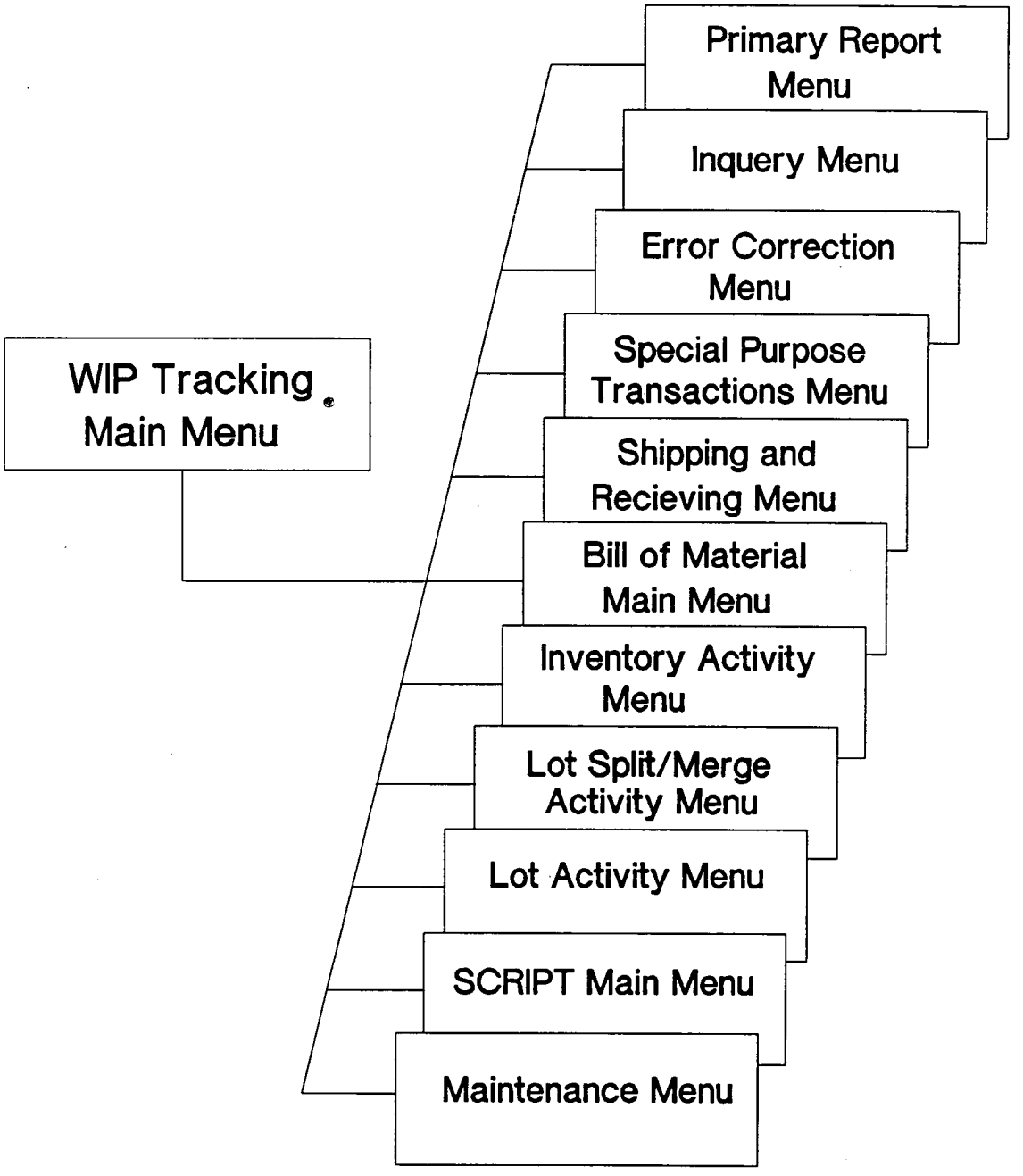

Figure 3.6 WIP module menu structure.

3.3.3. Data Collection

Process data collection is an essential feature of a semiconductor CAM system because of the necessity to analyse processing before it can be controlled. Data must therefore be collected for equipment as well as for lots. In addition, environmental variables , such as humidity, temperature and particle count, should be monitored to provide a complete view of the conditions under which processing is being performed. The collection points for the data being the process steps through which product lots pass. Once the data is collected it can be compared to pre-set parameter limits so that misprocessing can be identified, or used with statistical analysis to characterise equipment, and the environment, over time.

The EDC module [16, 17] is used to perform engineering data collection. The menu hierarchy of this module provides functions for defining what data should be collected and where. A data parameter is defined within COMETS as a PARAMETER, which has a value, a unit, and potentially a number of measurements which should be collected for it. PARAMETERS are associated with a processing point (figure 3.4). This may be an OPERATION, a ROUTE-OPERATION, or some other event such as the use of a particular piece of equipment. The data is entered by the operator or imported from a file and inserted into a lots and/or equipment's history, as specified in the parameter definition. Limits can be set for the acceptable range of a parameter. If these limits are violated then, for example, a mail message could be sent to the engineer in charge or the lot put on hold. Analysis of the data can also be performed as it is collected using the functions of the SQC module, if required then the results of the analysis can be stored in the database rather than the raw data.

The MDC module [18] works in conjunction with EDC to collect environmental data that is generated by monitoring systems. Once environmental data PARAMETERS have been defined they can be analysed and inserted into the database along with the EDC PARAMETERS.

3.3.4. Non-Lot Tracking

Non-lot tracing provides up-to-date information on the current state and the past history of items which are not classed as work-in-progress. This includes process equipment, durables such as masks, and operators. Being able to track such items with a CAM system builds up a model of the facility. Hence, it is possible to calibrate equipment, schedule maintenance, re-order durables before they are exhausted, and audit the amount and type

of work being performed by operators. In combination with WIP tracking, non-lot tracking allows the whole shop-floor to be controlled.

The NTC module [19] carries out the non-lot functions within COMETS. It is widely applied to controlling the utilization of processing equipment [20, 21]. The functions of the NTC menu structure allow the definition of equipment, durable and operator items as ENTITIES. When some action is performed on an ENTITY, such as calibration or clocking-in, then this is represented as an EVENT. As with LOTS in the WIP module, ENTITIES have HISTORIES so that, for example, utilization of a piece of equipment can be analysed over time. EVENTS are normally logged explicitly by operators by calling the appropriate COMETS function. However, it is also possible to collect engineering data for equipment by specifying PARAMETERS in EDC. The relationship between the data objects described here and other COMETS data storage elements is shown in figure 3.4.

3.3.5. Process Automation

Automating a wafer fabrication process requires the automation of processing equipment, inter equipment material transport, and information flow. The latter should be provided by the CAM/CIM system. In order to achieve the automation of information flow the system must perform the following sequence of functions for an automated device:

1. Recognise and validate a lot when it arrives at a processing device.
2. Update the status of the lot and equipment.
3. Control the loading of the lot in to the equipment.
4. Download the appropriate process recipe(s).
5. Initiate and monitor processing.
6. Handle any alarms generated by the device during processing.
7. Collect engineering data.
8. Update the status of the lot and equipment.

These functions should all be performed without operator intervention. Ideally equipment interfacing should adhere to the SECS standards [22]. Functionality should also be present to control the movement of lots between the processing stations.

The PAM module [23, 24, 25, 26] integrates automation management into the

COMETS factory management system. PAM has been developed so it can be mounted on a separate node of a computer network from the main body of COMETS. This allows PAM to be dedicated to controlling one process device or automated cell in real-time.

PAM supports a set of features including data collection, remote control, recipe downloading and control, and equipment status enquiry. It also deals with device initiated alarms. When these features are integrated with those of the WIP and NTC modules, COMETS satisfies the requirements for automation control set out previously.

A set of standard equipment software interfaces are provided as part of PAM. These adhere to the SECS protocols. Tools are available for the development of non-standard interfaces. However recipes are normally created and edited on the devices which will use them. They are then uploaded into the CAM system.

3.4. Implementing CAM Systems

Implementing a CAM system is not a trivial task. A commercial CAM system can never fit perfectly with a management structure or work practices that have developed over time and so will require to be tailored to the specific environment. Therefore, for a successful implementation, all the groups of people who will be expected to use the system must be involved in its installation. This includes management, support staff and departmental users. Without this involvement the system is unlikely to satisfy all the needs of the users and so can become a liability.

When implementing a CAM system it is advisable to start with a basic CAM package that includes production control, planning and reporting. Additional facilities can be made available as experience grows. Thus achieving a successful implementation is a long-term learning and integration project. It takes about a year after implementation before the capabilities of a CAM system are fully exercised [9].

Before attempting an implementation it is important to develop a model of the facility. This model must represent production, in terms of work-units and processing stations, at the level of detail which is required to control processing. The level of detail will depend primarily on the type of production being employed. For example, if production consists of lots of the same product being fabricated on one stable process then a relatively small amount of engineering data will be required for statistical control to be maintained. However, in a dynamic environment much more data will need to be collected as the application of statistical process control is questionable when a piece of equipment is used

for a number of different processes alternately. It is therefore important to decide whether a step such as the spinning on of photoresist must be represented explicitly or as a sub-step of a photolithography step. In the same way, data collection can be performed for each lot, each wafer, or even each chip site. It should be remembered when developing the model that data collection takes a finite amount of time, and that all the information must be stored and used as part of, for example, reporting transactions. Consequently the impact on the computing resources must also be considered. When completed the model can be transferred to the CAM system.

COMETS was installed at the Edinburgh Microfabrication Facility in October 1987. In the months prior to this an investigation was carried out on how best to represent the EMF using this system. The EMF performs a mixture of research and specialised manufacturing, so its production characteristics are similar to those of a low volume ASIC manufacturer. As COMETS is designed to meet the needs of commodity manufacturing this installation required a non-standard approach. With the help of Ferranti Electronics Ltd. an initial model of the facility was developed using COMETS terminology [27].

An OPERATION was loosely defined as a set of processing actions, at one site or on one piece of equipment, that has a unique set of processing instructions associated with it. In most cases this would correspond to one step on a runsheet. Within COMETS an OPERATION is uniquely defined by a four digit number. A numbering convention was devised which separated numbers into blocks of one thousand, with each block denoting a type of processing action. The convention used is as follows:

1000	Implantation	2000	Oxidation
3000	Deposition	4000	Heat Steps
5000	Parametric Test	6000	Etch
7000	Lithography	9000	Bonding/Packaging

The numbers between 1000 and 1999 were assigned to implantation steps, the numbers between 2000 and 2999 were assigned to oxidation steps, and so forth. This leaves from 0000 to 0999 free for unusual OPERATIONS or for dealing with overflows. The 8000 to 8999 block was left free in case of additional photolithography steps.

A ROUTE was defined as consisting of a group of OPERATIONS which would normally be associated with one another. For instance the photolithography sequences were described as ROUTES, as were oxidations which consisted of clean and oxidation

OPERATIONS. Though this approach results in many ROUTES having only one OPERATION, each ROUTE defines a sequence of process steps, the engineering data which must be collected and the process specifications for the steps. The result is that a ROUTE describes a sub-set of a process, which is reflected in the naming convention adopted. For example, 'NITDP N1.5' is a silicon-nitride deposition ROUTE for a 1.5 μm nMOS process. Thus by concatenating the SPEC files of a process the equivalent of a runsheet would be formed. However, when ROUTES are grouped together within COMETS they form a PRODUCT rather than a process. In the EMF there are many circuit designs being fabricated at one time, often on the same wafer, so there was no straightforward way to assign a circuit design to a PRODUCT. Instead, a PRODUCT was used to describe a process. Thus PRODUCTS would exist called '1.5 micron nMOS', '3 micron CMOS', etc. It was hoped that it would be possible to employ WIP wafer tracing to keep track of the product designs on each mask set, but this facility of COMETS did not prove to be flexible enough. To enable the storage of circuit design data (design numbers, designers name, etc) an initialising OPERATION was added to each PRODUCT definition. These OPERATIONS would collect the necessary information as engineering data.

Due to the inflexibility of wafer tracing and the amount of data that would require to be entered at each process step, it was decided not to track individual wafers. Instead, lots were chosen as the basic tracking unit, but with in-line engineering data being collected for each wafer and parametric data being collected for each chip-site. Each LOT is identified by a lot number, the format of which is EU for the university of Edinburgh, followed by the year and lot number. For example, 'EU89001' is for the first lot in 1989.

COMETS was installed at the EMF with two databases [28], a production database and a test database, the latter to be used for teaching. The model of the EMF manufacturing environment was then transferred into the production database as a single FACILITY called 'EMF'.

3.5. Summary

CAM systems have come to play an important role in the manufacturing of integrated circuits. Their replacement of manual and paper methods has led to improvements in productivity, asset utilization and yield.

Current systems comprise a database and a set of functional programs. The core programs perform WIP tracking, recipe management, data collection, non-lot tracking,

reporting and aid costing and scheduling. The movement towards CIM has also resulted in the integration into CAM systems of functions to automate information flow. Other features such as engineering data analysis and statistical process control have also become available.

The time and expense involved in developing a CAM system has resulted in the industry becoming dependent on a few commercial systems. Though these have proved adaptable enough to meet the needs of most modes of manufacture, much effort must still be put into tailoring them to the needs of any specific environment.

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Chapter 4

Process Simulation

4.1. Introduction

Process simulation is the modelling of the physical changes which wafers undergo during the fabrication of integrated circuits. Given the sequence of steps used in a process, the control parameters for these steps, and the device layout; a simulator can be used to calculate the doping profiles and structural features of the fabricated devices. Computer based modelling of semiconductor fabrication was first used in the 1960's to investigate process dependencies in the fabrication of bipolar devices. However, since the mid 1970's process simulation has matured as a result of the need to produce smaller and faster MOS devices. For a review of the development of process simulation see [1].

The most widely used process simulators are one-dimensional [2, 3, 4], modelling a 1D section normal to the surface of the wafer. For larger process geometries this level of detailing is sufficient, but for geometries approaching one micron it is essential to also model the two-dimensional effects of fabrication. For example, the lateral distribution of dopants under the gate of a short channel transistor. Several 2D simulators have been reported [5, 6, 7], but solution times are much longer than for 1D simulations. Consideration is now being given to developing 3D simulators in order to model devices with geometries significantly less than one micron, although the complexity of these models requires enormous computational power [8].

Simulation originally came to the fore as a method for reducing the number of experimental fabrication runs that are required during process development. Latterly it has also become tightly associated with device and circuit simulation as a computer aided design (CAD) tool for IC fabrication. The application of physical process simulation has allowed design engineers to simplify the development and optimization of fabrication processes, but has found limited application in manufacturing environments. This is largely a result of the complexity and unsuitable user interfaces of the current generation of process simulators, which makes them very difficult to use. Where the interface to process simulation

has been considered it has been as a design tool [9, 10].

The CAD tools which are used to design fabrication processes are capable of evaluating the performance characteristics of devices and circuits only for nominal values of control parameters. In order to model the statistical distributions which characterise the electrical performance of the devices fabricated during a manufacturing process it is necessary to perform statistical variations of the simulator input parameters [11]. A number of programs have been developed which use process simulation as part of a tool to analyse process variance and thereby predict manufacturing yield. FABRICS [12] and CASTAM [13] are tools which combine simple analytic process and device models to reduce the computational overhead. The reported use of a statistical approach to the application of standard process simulators is limited to an investigation of parameter variation using experimental design [14]. A review of manufacturing based simulation is given in [15]. Note, however, that these tools are not being applied to the on-line analysis of processing, ie. computer aided manufacture (CAM), but are being used for CAD of processing.

This chapter discusses how process simulation can be used to effectively model a fabrication process. Consideration is given first to the input parameters and models used by typical 1D and 2D simulators; SUPREM-3 and SUPRA. A demonstration is then given of how SUPREM-3 has been calibrated to the Edinburgh Microfabrication Facility (EMF) 1.5 micron nMOS process, and the results compared.

4.2. One Dimensional Simulation

Current process simulators cannot model all the events which could effect a process operation. However, they can solve a simplified problem that can be used to provide a basic understanding of process phenomena. They can also be used as an engineering tool for process design, development and optimization. The most gross simplification is to study the vertical formation of layers and distribution of dopant by modelling a one-dimensional section through a wafer. In order to simulate the fabrication of a device it is therefore necessary to simulate a number of 1D sections through the major regions of the device. Figure 4.1 shows an nMOS device structure with a set of 1D sections indicated.

The first general purpose process simulator to be widely accepted was SUPREM-II [2]. This simulator can be used to perform 1D simulations of both bipolar and MOS processes. Although developed in the mid 1970's, this simulator is still widely used throughout industry and academia, partially because it is in the public domain, but largely

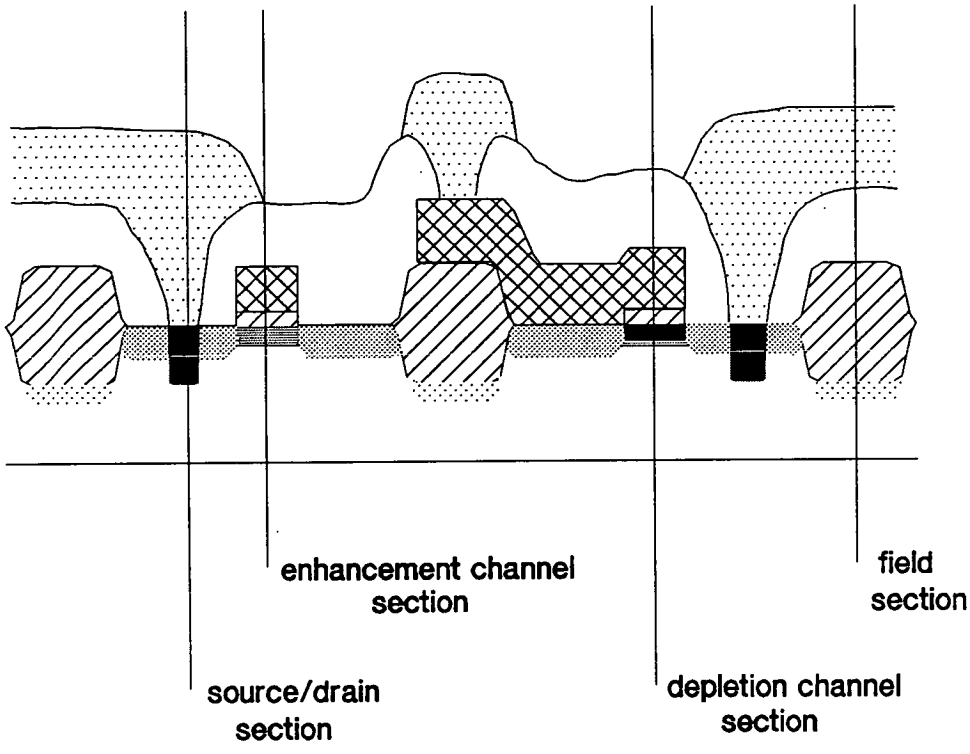

Figure 4.1 Section through an nMOS device with the 1D sections for simulating major regions indicated.

because of its mature and well understood models. These models contain simple physical solutions, supplemented by empirical data, for ion implantation, oxidation, diffusion, epitaxy and etching. However, SUPREM-II is limited in that its default models only allow it to simulate the distribution of boron, phosphorus and arsenic in silicon and silicon dioxide.

SUPREM-II has been superseded by SUPREM-3 [3, 16] which allows more complex multilayer structures to be modelled and also includes default data for polysilicon, silicon-nitride and photoresist. The basic models of SUPREM-II have been replaced by more accurate models. Where possible, these models are based on physical data rather than empirical fits to data. This allows the simulator to be used outside the specific ranges of the data sets from which the simulator was developed. In this section a discussion of SUPREM-3 will be used to demonstrate the current status of one-dimensional process modelling.

To simulate a 1D section through a device SUPREM-3 requires a certain set of input information. This includes:

- wafer material, orientation and doping
- a simulation space defined as a grid
- the process step specifications in the order of the fabrication sequence

The output from the simulator includes:

- physical data, such as charge densities and layer thicknesses
- electrical data, such as threshold voltages and sheet resistivities
- graphical plots showing the structure and doping profile of the simulation space

The doping profile is particularly useful as it gives a qualitative representation of the distribution of dopants in the substrate. Measuring this information during a production run is a very difficult and costly operation to perform. Simulating the gate section of the nMOS device in figure 4.1 results in the profile shown in figure 4.2. Starting from the vertical axis to the left of the figure are the polysilicon gate, the gate oxide and the silicon substrate. The electrical characteristics of this device will be influenced by both these physical characteristics and by the presence of phosphorus and boron dopants in this region of the device.

The simulation described above was carried out using a grid structure normal to the surface of the silicon. This is necessary as the continuous physical processes are modelled by a system of differential equations that must be solved for points through the structure of the wafer. In order to achieve an efficient simulation with the limited number of grid points available in SUPREM-3, it is a good policy to concentrate the grid points in the area where the impurity distribution is changing quickly, ie. the active areas, and use fewer grid points where there is less change, ie. the bulk of the silicon.

SUPREM-3 has its own control language in which the simulation is initialised, the process steps defined, and the format of the output specified. It is possible to use this language interactively to control the simulator, but for long simulations it simpler to insert the input statements in a file and submit this to the simulator. Figure 4.3 shows the outline of the input file used in the previous example. Although the bulk of the actual processing statements have been omitted from figure 4.3, it is evident that to perform a full process simulation requires a high degree of experience with the simulator. For a complete description of the input format for SUPREM-3 see [16].

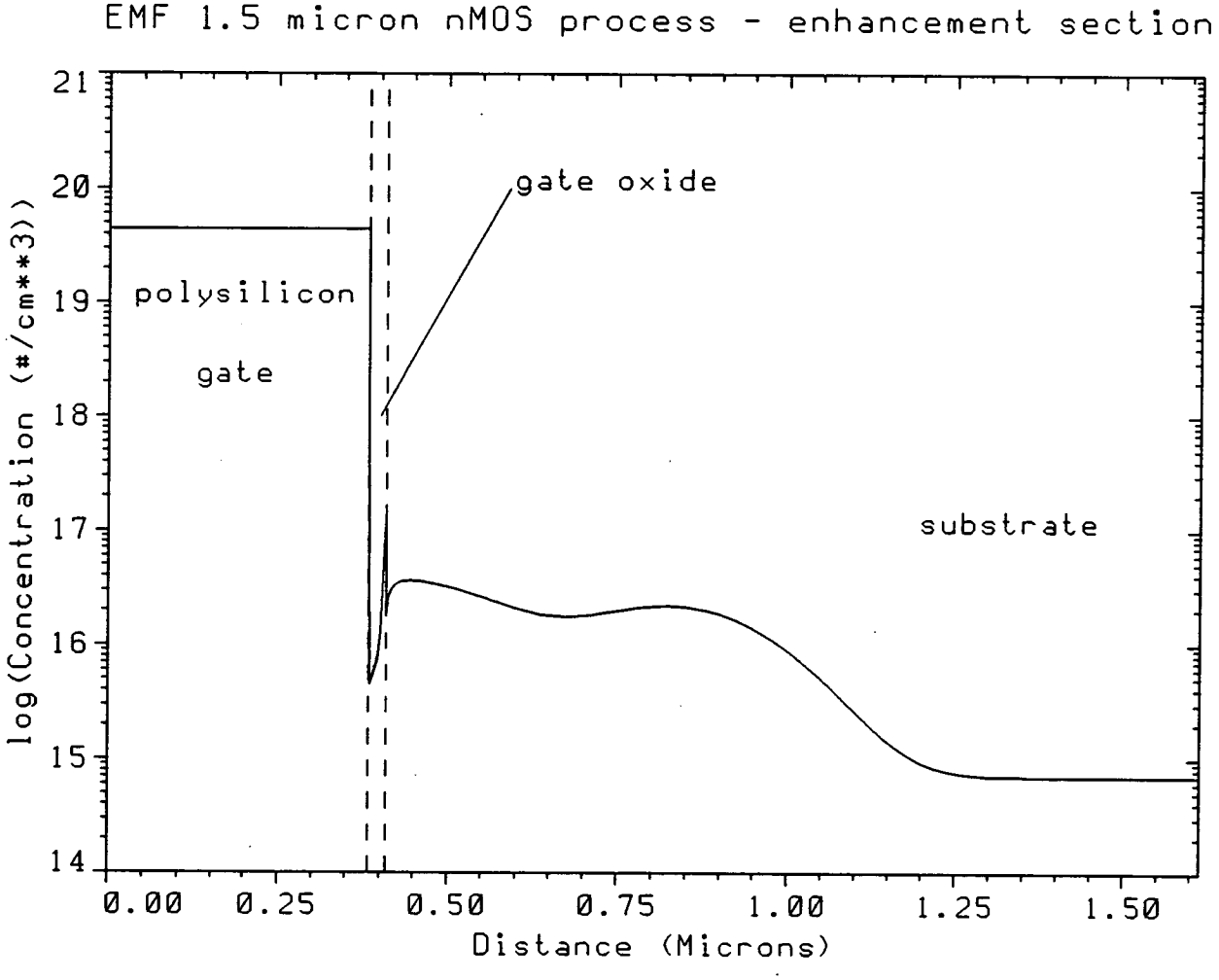

Figure 4.2 1D doping profile through the enhancement region of an nMOS device; profile is net dopant concentration.

```
title  EMF 1.5 micron nMOS process
+      n-channel enhancement section

$  Initialize the silicon substrate
initialize  <100>  silicon boron=7e14
+           thickness=1.25  DX=0.001 spaces=100

$ calculate ionization impurity concentrations
material silicon semiconductor ionizati

$ increase dry-oxide growth rate
ambient O2  <100>  H.LIN.0=0.2e6

$ reduce wet-oxide growth rate
ambient H2O <100> H.PAR.0=5.8

$ stop phosphorus diffusion through oxide
impurity phosphor oxide dix.0=0

$  INITIAL CLEAN

$  INITIAL OXIDE
diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5 F.O2=1.5
print layers

$  SILICON NITRIDE DEPOSITION
deposition nitride thickness=0.1 temp=800 time=25

$  LAYER 1 PHOTO(1) - ISOLATION REGIONS

$  SILICON NITRIDE RIE ETCH

$  FIELD IMPLANTATION

$  LAYER 1 RESIST STRIP

$  FIELD OXIDE
diffusion temp=950 time=220 inert


   ..........................


$ End of Enhancement Section Simulation
stop
```

Figure 4.3 Outline of SUPREM-3 input file used to create the profile shown in figure 4.2.

In the following sub-sections the models used by SUPREM-3 are considered, indicating the input parameters that equate to equipment control parameters†.

4.2.1. Oxidation

Due to the importance of oxidation in the fabrication of bipolar and MOS devices, the modelling of oxidation was one of the first areas to receive attention. The models which are incorporated in SUPREM-3 allow for the oxidation of single crystal silicon, polysilicon and silicon nitride to be performed. All the factors, used in a simulation, that influence the growth of oxide in these regimes are physically modelled with the exception of HCl which is handled empirically.

The oxidation models within SUPREM-3 can be used to simulate many different process condition. These range from long LOCOS oxidation to form isolation regions, to very short oxidations to grow gate oxides.

The growth of oxide on silicon and polysilicon is a development of the classic Deal and Grove equation [17]

$$t = \frac{X_o^2 - X_i^2}{B} + \frac{X_o - X_i}{B/A} \qquad (4.1)$$

where t is time, X_o is the oxide thickness, X_i is the thickness of any oxide present at t=0, B is the parabolic growth rate, and B/A is the linear growth rate. When this equation is solved in SUPREM-3 it also includes terms for rapid initial oxide growth, and the presence of HCl [16]. A separate set of equations is used for oxide growth on nitride. These equations are calculated as a partial differential equation for each point in the 1D simulation grid at each time step.

The SUPREM-3 instruction which is used to indicate an oxidation is the DIFFUSION statement, for which must be specified a time, a temperature and an ambient. Available default ambients are pure oxygen, pyrogenic steam, and 100% steam. Alternatively the gas flows into the furnace may be specified directly. The latter form is particularly useful in a manufacturing environment as it may be directly related to the actual gas flows.

Additional parameters can be used to specify the growth of doped oxides, the pressure in the furnace during the oxidation, and the percentage of HCl present as an alterna-

† As discussed in Chapter 2.

tive to its flow into the furnace. To model ramping of temperature and pressure in a furnace, their parameters can be specified with a rate of change. If necessary, it is possible to directly specify that a given temperature and time will result in a given oxide thickness.

4.2.2. Diffusion

The models for impurity diffusion in a process simulator are used to generate the doping profiles. It is, therefore, very important that these be accurately calculated. In SUPREM-3 diffusion models are present for polysilicon, nitride, and the oxides of silicon and nitride, as well as for silicon itself. A range of dopants can be modelled including antimony, arsenic, boron and phosphorus. Each of these has a set of associated physical models that are solved numerically.

Diffusion takes place during every heat step used in a fabrication process. This includes oxidation, deposition, and annealing. The diffusion models of SUPREM-3 are therefore used to simulate many process steps, from the diffusion of the channel stop implant during a LOCOS oxidation, through the redistribution of phosphorus in an nMOS polysilicon gate, to the drive-in of all the dopant present during the final reflows. It is also possible to model the introduction of dopants during a heat step. For example, diffusing in phosphorus from a solid source in a furnace.

The simulation of diffusion processes in SUPREM-3 involve the complete one-dimensional continuity equation

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial X}\left(D\frac{\partial C}{\partial X}\right) \pm \frac{q}{kT}\frac{\partial}{\partial X}\left(D\hat{C}\frac{\partial \phi}{\partial X}\right) \tag{4.2}$$

where D is the effective diffusivity, and C and $\hat{C}$ are the total and electrically charged impurity concentrations, respectively. The potential ϕ is

$$\phi = \frac{kT}{q}\ln\frac{n}{n_i} \tag{4.3}$$

where n and n_i are the electron and intrinsic carrier concentrations, respectively, at the diffusion temperature. As implemented, this equation models the diffusion of impurities as a vacancy-assisted mechanism. In silicon account is also taken of high concentrations of phosphorus, the presence of oxidizing silicon or polysilicon surfaces, and transient diffusivity enhancement which may result, for example, from implant damage. In addition, with multiple-layer structures, dopant transport and segregation across material interfaces is included in the impurity diffusion models. For a more detailed discussion of the models

used for diffusion in SUPREM-3 see [3].

The DIFFUSION statement is used to explicitly simulate a diffusion of dopant through a device structure. This includes the oxidizing ambients described in section 4.2.1 or for an inert ambient such as nitrogen. When a diffusion is being performed the parameters for time, temperature and ambient must be specified. For a simple diffusion where dopants are present in the structure being simulated it is not necessary to specify these as the simulator will automatically perform the appropriate diffusion calculations for each impurity present. As with oxidation, the rate of diffusion will be affected by the ramping rate of the temperature during the process step, but will not be directly affected by the pressure coefficient.

In manufacturing it is unusual to simply perform a diffusion without the associated growth or deposition of a layer. The DIFFUSION statement is therefore very useful for modelling the heat component of process steps whether or not they result in layers being grown or deposited for the section being simulated.

4.2.3. Ion Implantation

The almost universal use of ion implantation in fabricating small geometry devices has resulted in the development of new models for this important processing operation. The models provided by SUPREM-3 allow either analytically or numerically calculated solutions to be applied to the implantation of impurity ions into a device structure.

Ion implantation is the preferred method of introducing dopants when only a shallow doped region is required, or the concentration of the dopant must be closely controlled. These situations arise during the fabrication of small geometry devices where it may be necessary to have very shallow source and drain regions. Implantation can also be performed through multiple layers of a structure. For example, during the threshold voltage adjust implant of an nMOS process the dopant is implanted through a thin oxide into the substrate.

SUPREM-II utilized look-up tables based on LSS theory [18] to construct range distributions for implanted ions. SUPREM-3 continues to offer such analytical techniques for modelling ion implantation but also introduces a numerical method. The analytical techniques use a simple Gaussian, two-sided Gaussian, or Pearson IV distributions. Exponential tails may be added to the analytic distributions in silicon to model channeling more accurately. The numerical method is based on a solution of the Boltzmann transport equa-

tion [19]. Though much slower to solve, the numerical system of equations can provide a much greater accuracy than the analytical solutions [3]. The numerical solution does not, however, allow any modelling of ion channeling.

The analytic calculations represent an impurity distribution I(x) as

$$I(x) = N\left[f(x) + f_t(x)\right] \tag{4.4}$$

where N is the concentration of the dopant provided by the implanter, f(x) is a normalised distribution, such as Gaussian, and $f_t(x)$ is defined as an exponential tail added to f(x) in silicon. The concentration of the dopant is a function of ion beam current, while both f(x) and $f_t(x)$ are found from look-up tables and are dependant on both ion beam current and energy.

Implantations are initiated in SUPREM-3 by using the IMPLANT statement. This requires the dopant ion, the concentration of the implanted ions, the acceleration energy of the ion beam, and the solution method to be specified. Any dopant may be used although the range characteristics for the analytic solutions are only available for antimony, arsenic, boron and phosphorus. The Boltzmann solution depends only on the characteristics of the implanted impurity and the materials present in the structure.

Although the analytic methods of modelling ion implantation are very efficient, the additional accuracy offered by the numerical method is preferable when simulating the implants into small devices.

4.2.4. Deposition

A deposition process is modelled by SUPREM-3 as the addition of a layer to the top of an existing structure. Default models exist for the deposition of silicon, silicon dioxide, silicon nitride, polysilicon, aluminium and photoresist. However, because of the vast range of techniques which can be used to perform these depositions in manufacturing, the simulator requires that either the thickness to be achieved or the growth rate of the material be specified. The deposited materials can also be specified as being doped with impurities such as antimony, arsenic, boron and phosphorus.

This simplified approach to deposition allows SUPREM-3 to model many deposition processes, including evaporation and sputtering of metals, CVD and LPCVD of silicon based materials, and spin-on of resist. In this way, for example, SUPREM-3 can be used to simulate the presence of interconnect, or the use of polysilicon in MOS gates and buried contact. The ability to model resist allows the photolithographic steps to be at least

nominally modelled by the simulator.

No numerical or analytic models are included to explicitly model the deposition of a material layer. For low temperature processes the material is simply added to the structure and for a high temperature process the diffusion models described in section 2.4.2 are used to take account of the heat component of the step. The exception to this is polysilicon, the multiple-crystallite and grain-boundary structure of which requires models for grain growth, dopant segregation, and carrier trapping at the grain boundaries. Models are also included to simulate the growth of thin polysilicon films. A full description of the models used by SUPREM-3 for polysilicon can be found in [20].

The DEPOSITION statement requires only that the material and the thickness or growth rate be specified for low temperature deposition. For high temperature deposition the temperature and, with the exception of polysilicon, the time must also be specified. In addition, if dopants are to be included then the impurity and its uniform concentration, or resistivity, must be specified. For polysilicon, parameters exist for both pressure and the initial grain size.

Although the approach to layer deposition in SUPREM-3 is highly simplified, one-dimensional simulation does not include any topographic detailing and so this approach can be justified.

4.2.5. Etch

The etching process modelled by SUPREM-3 removes all, or part, of a specified material from the top of the current structure. This is, in effect, the inverse of deposition as it is possible only to specify the thickness, or etch rate, of the material to be removed. The materials range include silicon, silicon dioxide, silicon nitride, polysilicon, aluminium and photoresist. The presence of dopants in these material is not treated explicitly.

As both the dry and wet etching processes used in IC fabrication are very difficult to control, the simulation of an etching step must be calibrated to the actual outcome of the step. Therefore, once calibrated, SUPREM-3 can be used to simulate any pre-specified etch, from the removal of a photoresist, to the etching of multiple layers of nitride and oxide performed prior to an MOS LOCOS step.

No models are used directly to represent the removal of material layers during an etch process. However, if an etch is performed at a high temperature then the diffusion equations of section 4.2.2 are solved for each impurity.

The ETCH statement requires only that the material and the thickness to be removed be specified for a low temperature etch. A high temperature etch must also have the time and temperature, and can include the etch rate, instead of the thickness to be removed. It is also possible to specify the ramping of the temperature for high temperature steps.

For the simulation of etching to be used effectively in a manufacturing environment, the etch steps must be well characterised in advance. If this is not done then the simulation results can become unreliable, particularly when attempting to estimate the effect of over-etching.

4.2.6. Electrical

The physical structures and profiles of dopants produced by SUPREM-3 can be used to calculate the electrical characteristics for the simulated section. This allows a process or device engineer to relate the process sequence to the electrical performance of devices fabricated using a process. As a CAD tool this information can be used to optimise the device performance. While device modelling programs have been developed to simulate 1D [21] and 2D [22] sections, SUPREM-3 can provide a basic set of electrical parameters. These include net charge, conductivity and sheet resistance, for every layer in the simulated structure. The threshold voltage of an MOS capacitor can also be calculated.

The simulated electrical parameters for a section can be compared with parameters measured in-line and can therefore be used to calibrate the simulator to the fabrication environment. Of particular importance here is sheet resistance. The fully simulated gate region of an MOS transistor can be used to calculate the threshold voltage (V_T) which can be compared to the measurements made during parametric test on the fabricated devices. This is most accurate for long channel devices where the combined layers of doped polysilicon, oxide and doped substrate (see figures 4.1 and 4.2) effectively form a capacitor and can therefore be simulated as such.

The electrical parameters are calculated by solving Poisson's equation numerically with a series of specified bias conditions. The one dimensional Poisson's equation used by SUPREM-3 is

$$\frac{\partial}{\partial x}\left[\epsilon(x)\,\frac{\partial \psi(x)}{\partial x}\right] = \begin{cases} -q\left[p - n + N_D^+ - N_A^-\right] & \text{semiconductor} \\ 0 & \text{insulator} \end{cases} \qquad (4.5)$$

where ϵ is the dielectric constant of a material layer, ϕ is the potential, p is the hole concentration, n is the electron concentration, and N_D^+ and N_A^- are the sums of the ionized electrically active donor and acceptor impurity concentrations, respectively. The threshold voltage is calculated by extrapolating tangentially to zero conductance from the point of maximum slope in the variation of conductance versus bias.

The ELECTRICAL statement is used to initiate the Poisson's equation, if V_T is to be calculated then a number of bias steps should be specified. The default value for biases is zero volts, but if the BIAS statement is used then the layers of the structure can be biased individually. The presence of a surface charge on the substrate (Q_{ss}) can be specified by using the QSS statement. The final electrical statement is END.ELECTRICAL which terminates the solution of Poisson's equation. Figure 4.4 shows the electrical statements that might be applied to the structure of figure 4.2 to calculate V_T.

```
ELECTRICAL  STEPS=18  VTH.ELEC  LAYER=1
BIAS        LAYER=3  V=-0.2  DV=0.1  ABSCISSA
QSS         LAYER=1  CONC=5E10
END.ELECTRICAL
```

Figure 4.4 SUPREM-3 input statements to perform Poisson's equation to calculate V_T for an MOS capacitor.

The input statements to control the calculation of electrical parameters in SUPREM-3 bear no relation to the commands that might be used to control their measurement. However, they can be used to aid the initial calibration of the simulator thus improving the accuracy of its calculations in a predictive role. This enhances the applicability of SUPREM-3 to both design and manufacturing environments.

4.3. Two-Dimensional Simulation

As devices are scaled down, the two-dimensional effects of impurity profiles and surface topology become critical in determining device performance. This has given rise to the development of 2D simulators such as SUPRA [5], SUPREM-4 [7] and COMPOSITE [6]. These have been used to investigate features such as the lateral diffusion of dopants under the gate of a short channel MOS transistor, and the bird's-beak effect that results from a LOCOS process. Figure 4.5 shows a 2D section covering these features for one half of an nMOS enhancement transistor.

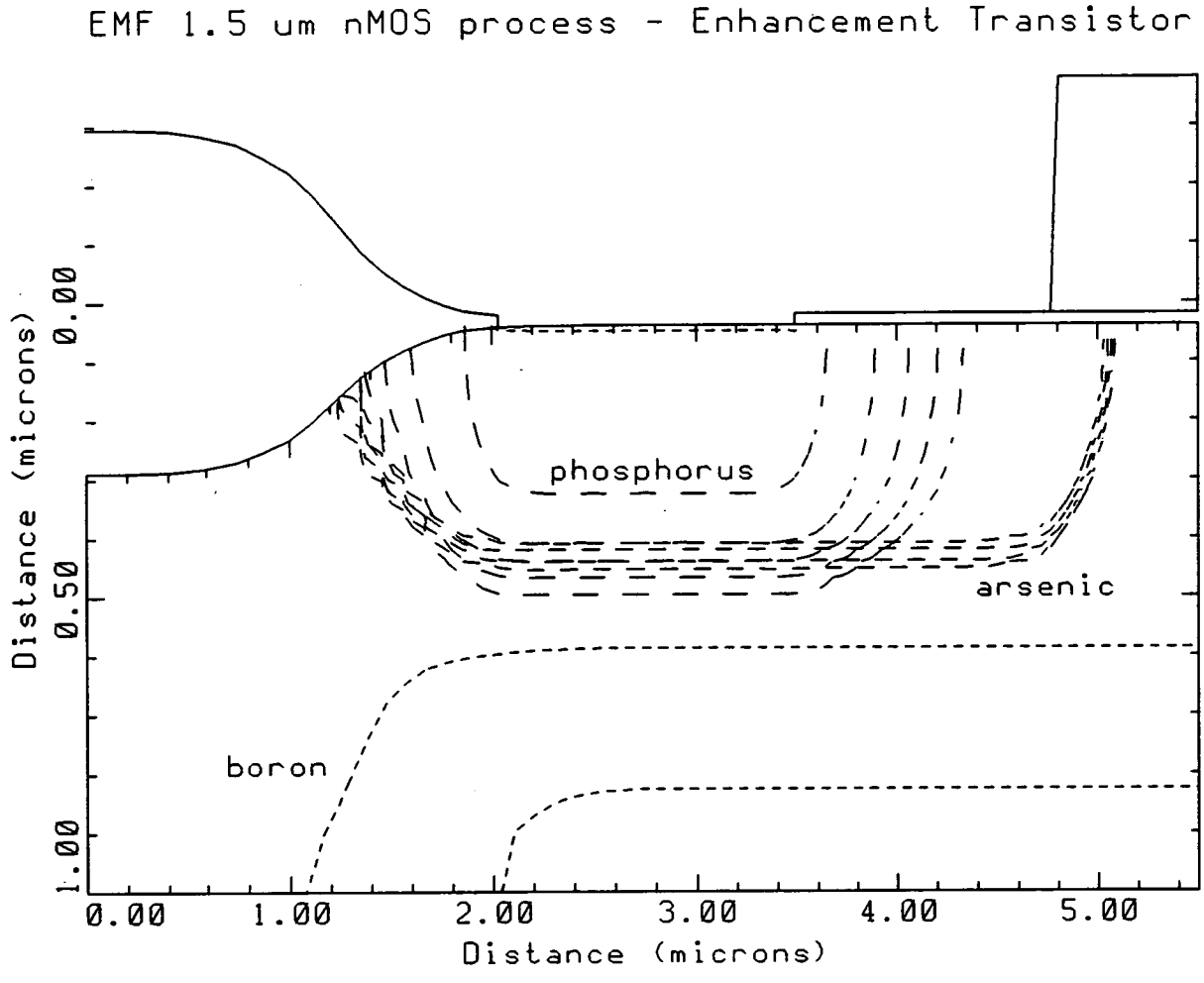

Figure 4.5 nMOS device as modelled by SUPRA.

SUPRA is capable of simulating inert ambient drive-ins, silicon oxidation, ion implantation, and low temperature deposition and etching for multi-layer device structures. Many of the process models used within SUPRA are based on those of SUPREM-3, and the input language is very similar to that of SUPREM-3. All of the models may be solved either analytically or numerically; with the exception of thermal oxidation which cannot be performed in numeric mode, and diffusion in a doped inert ambient which must be performed numerically. A further constraint is that numerical solutions may be performed after analytic but not visa versa. The applicability of the simulator is also limited in that only silicon may be oxidised and dopant diffusion may only take place in the silicon substrate and in one additional silicon, or silicon dioxide, layer. Analytic models are included in SUPRA as they can be solved much more quickly than for numerical models. However numerical models provide a much higher degree of accuracy where high dopant concentrations are present, eg. in source/drain regions. The 2D grid structure used by SUPRA is only required for solving the numerical models. For a full discussion of the input statements which are used to control SUPRA see [23].

SUPREM-4 is a more recent two-dimensional development, and includes some more advanced analytic and numerical models than are provided by SUPRA. However, SUPREM-4 is still a relatively immature simulator. COMPOSITE has a separate development history from the SUPREM family of simulators, but uses models for diffusion and oxidation which are two-dimensional developments of those used in SUPREM-3. It also includes physically based models for deposition, etching and lithography which are not available in SUPRA or SUPREM-4.

The simulators discussed here are designed to produce 2D sections of the physical device structures and dopant profiles. They do not, however, provide the electrical characterization capability of SUPREM-3. Therefore in order to calculate electrical parameters to compare with those of SUPREM-3 it is necessary to pass the simulated 2D section to a 2D device simulator, such as PISCES [24] or CANDE [25]. Device simulators can be used to calculate such parameters as V_T, which can be extracted from curves of source-drain current (I_{DS}) against gate-source voltage (V_{GS}), and sheet resistance.

Evidently 2D process simulators are more complex to use than 1D simulators. This is largely because of the additional complexity of the 2D models over their 1D counterparts. The level of model maturity is also less than that found in 1D simulators. Consequently 2D process simulators are likely to produce less accurate simulations of vertical doping pro-

files. The additional complexity of the models also means that more cpu power/time is required to model a given device structure. The cpu time for a 2D simulation of the device shown in figure 4.1 could easily be in excess of an order of magnitude greater than that for a set of 1D simulations.

4.4. Simulating the EMF 1.5μm nMOS Process

Proper calibration and verification of simulation tools are very important when attempting to fully model a manufacturing process. This is because the physical models used in process simulators have a limited range of applicability and so the built in default parameters may not give good results for every fabrication environments [26].

This section sets out to demonstrate how one-dimensional process simulators may be calibrated to a manufacturing process. The simulations are carried out using the TMA package SUPREM-3. The process chosen for this demonstration is the EMF 1.5μm nMOS process†, the runsheet for which is listed in appendix A. A discussion of the simulation of the EMF 6μm nMOS process using the Stanford version of SUPREM-III can be found in [27].

Whenever possible the values of the process parameters listed in the runsheet have been used in the simulator input statements. The result is that the process models have been modified rather than the process recipe and consequently SUPREM-3 has been calibrated to the fabrication environment rather than just the 1.5μm nMOS process.

Table 4.1 sets out typical values for the parameters that are measured during a normal run of this process. Table 4.2 set out the parameters for this process that are not measured during normal lot runs, but are significant in defining the process.

To calibrate SUPREM-3 to the EMF 1.5 μm nMOS process the four 1-D sections of figure 4.1 must be simulated. The objective is to obtain simulation results that compare well with those listed in tables 4.1 and 4.2. Where necessary, each step of the process described in the runsheet is modelled. The output files for these simulations are listed in appendix C.

The enhancement channel region

The input file for this simulation starts by declaring the initial state of the wafers in terms of their silicon orientation and uniform doping level. As a 1.5μm nMOS device has

† As described, with diagrams, in chapter 2.

Parameter		Target Value
Initial oxide thickness	=	380 Å
Silicon Nitride thickness	=	1000 Å
Field oxide thickness	=	6000 Å
Gate oxide thickness	=	250 Å
Deposited gate polysilicon	=	4000 Å
Phosphorus doped polysilicon sheet resistance	=	50 Ω/□
Deposited reflow pyro thickness - undoped	=	1500 Å
Deposited reflow pyro thickness - plus phosphorus	=	4500 Å
Polysilicon gate sheet resistance after first reflow	=	50 Ω/□
Active area sheet resistance after first reflow	=	50 Ω/□
Enhancement transistor threshold voltage	=	0.6 V
Zero bias source-drain current (I_{DS0})	=	20 mA

Table 4.1 In-line measured process parameters.

Parameter		Target Value
Depth of source/drain region	=	0.3 μm
Depletion threshold voltage	=	-4 V
Fixed $Si-SiO_2$ surface charge (Q_{ss})	=	3×10^{10} atoms cm^{-2}

Table 4.2 Non in-line process parameters.

quite a shallow structure it is sufficient to set the depth of the simulation grid to 1.25μm. The highest density of grid points is specified to be near the surface of the wafer, as discussed in section 4.2, where the greatest change in dopant concentration can be expected.

The default models for silicon and polysilicon assumes that any dopant is completely ionized. However, this is not always necessarily the case [28] and therefore by specifying that the level of ionization must be calculated for silicon, electrical calculations can be performed more accurately. Due to the high concentration of phosphorus, the polysilicon gate can be assumed to be completely ionized.

The ambient for dry oxidations has been modified by increasing one of its parameters (H.LIN.0), used to calculate the linear oxide-growth coefficient, above its default value. This affects the rate at which dry oxides are grown, and results in higher values for the thickness of the initial and gate oxides. Although included for the enhancement section, the new value specified for one of the wet ambient parameters (H.PAR.0) is primarily intended to affect the growth of the field oxide.

The default model, used by SUPREM-3, to simulate the diffusion of phosphorus through silicon dioxide allows the high concentration of phosphorus, introduced into the polysilicon gate, to punch through the thin gate oxide into the substrate. This is not what happens in reality and so to prevent this, the diffusion coefficient for phosphorus in silicon dioxide has been set to zero, which stops any phosphorus diffusion through silicon dioxide.

Once the environment has been specified the process steps can be simulated. The first process step to be explicitly simulated is the growth of the initial oxide. The thickness of this oxide is simulated at 372 Å which is close to the typical measured value. Note that the three phases of the oxidation are modelled separately. The deposition of silicon nitride, however, cannot be modelled in this way and so a target value for its thickness is specified.

It is only necessary to simulate the growth of the field oxide, for this section, by including its heat component.

Simulating the growth of the gate oxide gives a thickness of 254 Å, which matches the target value of 250 Å. It is important that this feature be modelled accurately as it has a large influence on the threshold voltage of the final devices. Achieving this level of accuracy is only possible by modifying the oxidation growth rates as described previously.

An analytic model was used for the threshold adjust implants as this was found to

give good results, and was also more robust than the numeric model.

The deposition rate of polysilicon over the gate oxide is not known so it is convenient to use a target value for this step. Depositing phosphorus from a solid-source, to dope the polysilicon, is not easy to model because of the difficulty in monitoring the concentration of phosphorus at the surface of the wafers during processing. However, it is important to get a low resistivity in the polysilicon gate. Experimenting with the phosphorus concentrations shows that a concentration of 1.65×10^{20} atoms cm^{-3} is sufficient to give a polysilicon sheet resistivity of 46.7 Ω/□ after the deposition and 51.2 Ω/□ after all processing.

The process steps that follow the oxidation of the polysilicon gate are simply modelled as heat steps. This is possible because the layers produced by these steps do not effect the measured values. Figure 4.6 shows the layers and doping profile produced by the simulation of the enhancement channel region.

After the physical simulation has been completed, an electrical simulation is performed. The value of the fixed oxide charge (Q_{ss}) is included at this point as it affects the solution of Poisson's equation. A set of bias voltages are applied to the polysilicon gate resulting in the curve of figure 4.7. From this is calculated the threshold voltage of 0.53 V. The target value is a little higher at 0.6 V, but this is still a reasonable fit.

The depletion channel region

The simulation of the depletion channel region differs from that of the enhancement channel region only in the inclusion of an arsenic depletion implant. As a doubly ionized species is used for this implant it is necessary to double the energy of the implant to model the effect of the double ionization. The resulting threshold voltage for this region is -3.62 V. Although differing from the target value by around 0.4 V, the simulated value is sufficiently negative to be acceptable. Figure 4.8 shows the doping profile for this section.

The source/drain region

The simulation of the source/drain region is also based on that of the enhancement channel region. This section differs, however, in that both the polysilicon and oxide layers of the gate region are etched, and an arsenic implant is performed to form the source/drain regions themselves.

After the first reflow the wafer surface for this region has a simulated sheet resistance of 48.8 Ω/□ against a measured value of 50 Ω/□. When the process is complete the n-type/p-type junction depth is 0.35 μm, only 0.05 μm deeper than the target depth. Figure

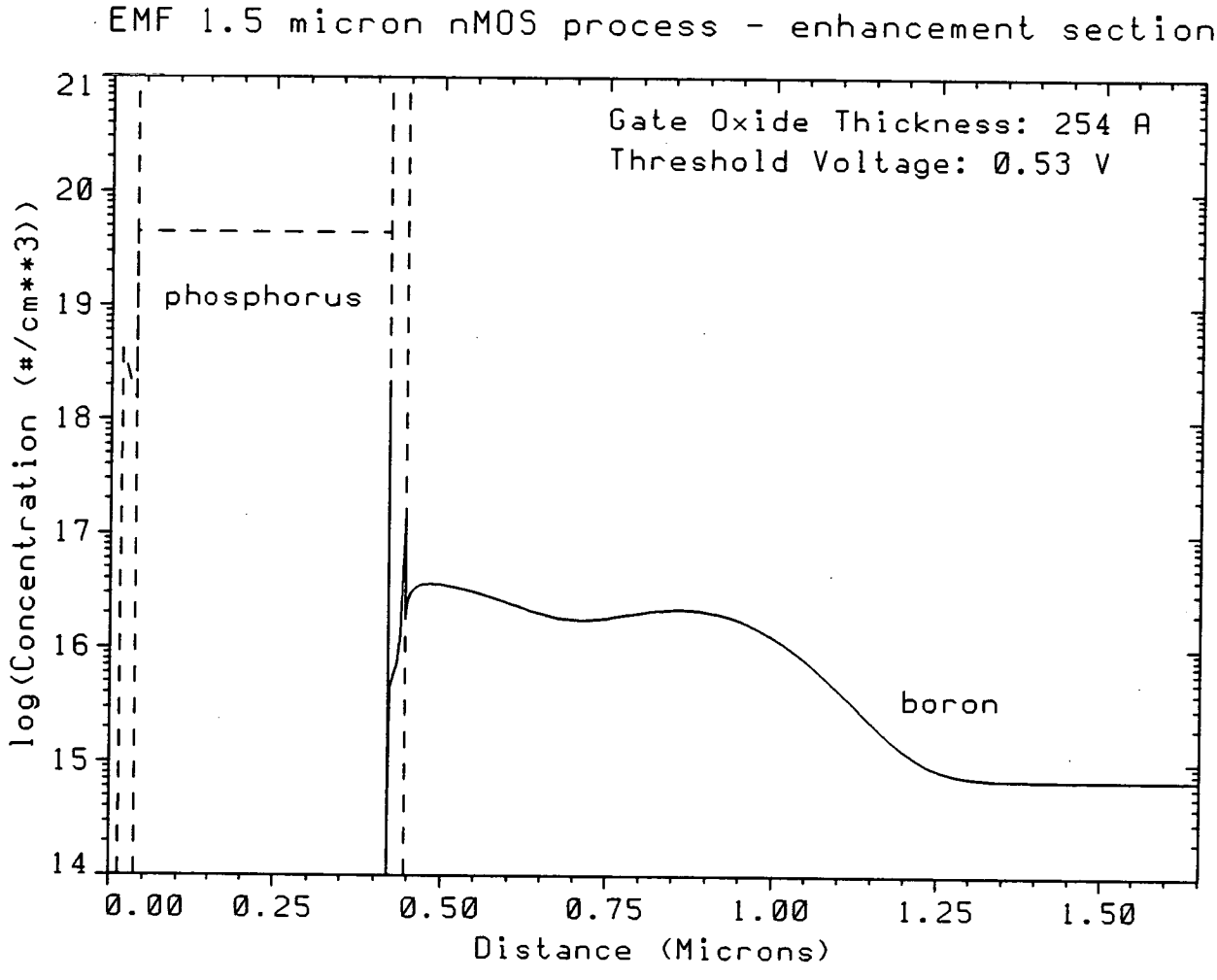

Figure 4.6 1D doping profile through the channel region of an enhancement mode nMOS device.

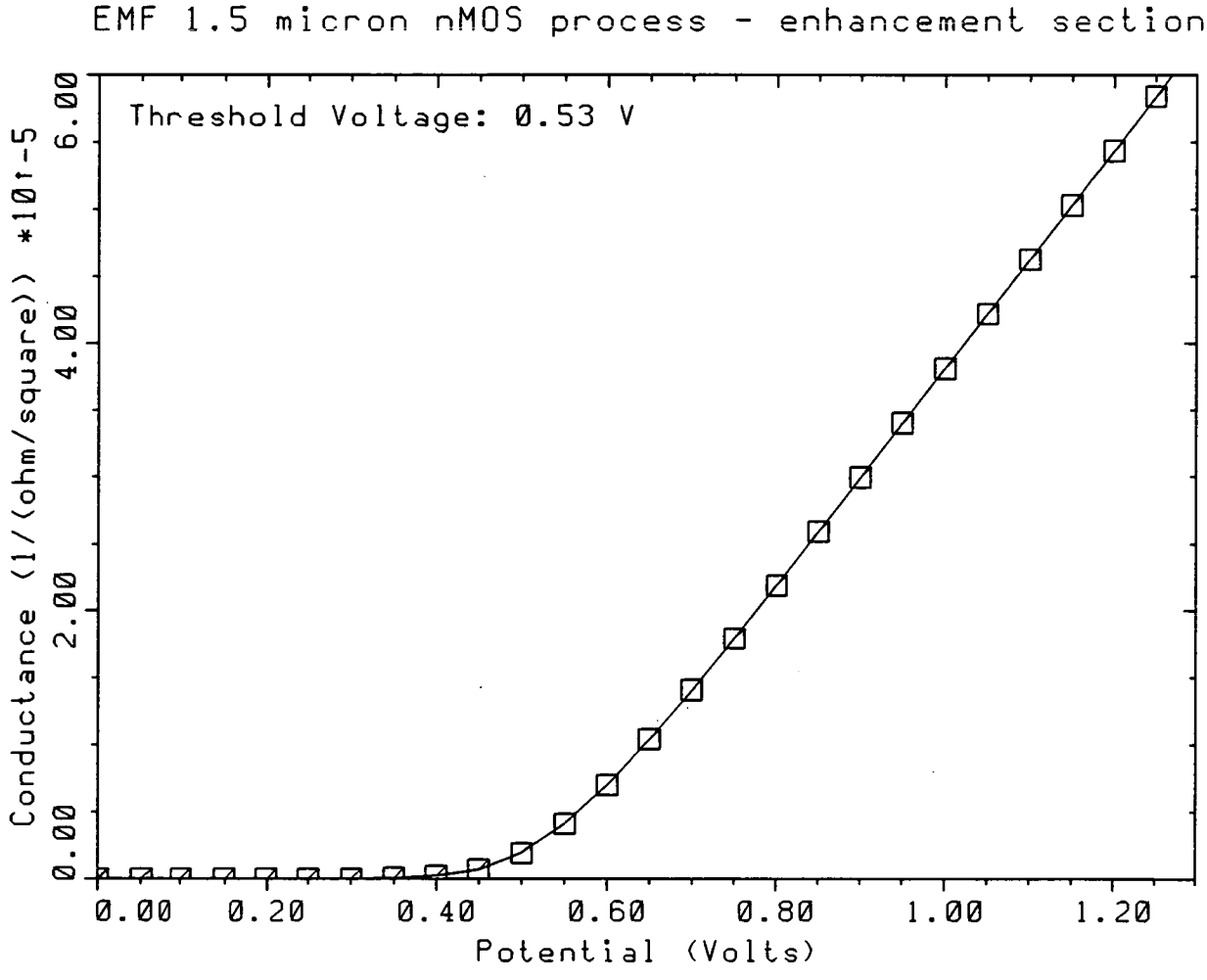

Figure 4.7 1D conductance/voltage curve for an enhancemet mode nMOS device.

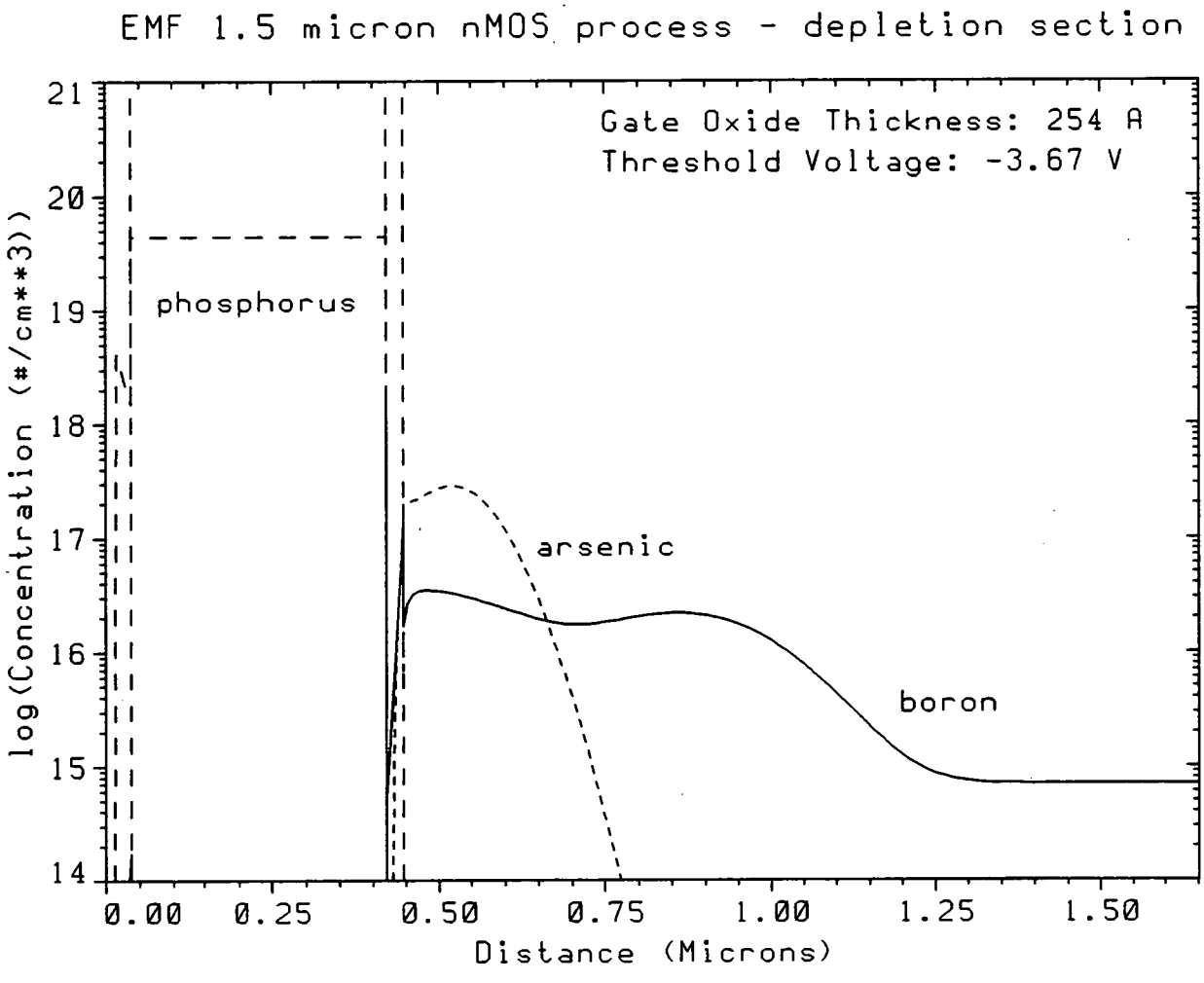

Figure 4.8 1D doping profile through the channel region of a depletion mode nMOS device.

4.9 shows the doping profile at this stage of the simulation.

Where the interconnect forms a contact with the active region, the surface of the silicon is exposed to the same level of phosphorus doping as the polysilicon gate. The result is a region of lower sheet resistivity (29.0 Ω/□) in the center of the active region, as show in figure 4.1. Figure 4.10 shows the doping profile for this low resistivity region.

The field region

The simulation control file for the field region includes many of the same control statements as were used for the other regions. As indicated earlier, the final thickness of the field oxide has been tailored by modifying one of the terms (H.PAR.0) that is used in the calculation of the parabolic oxide growth-rate for a wet ambient.

After simulating the channel stop boron implant, each of the separate field oxidations are modelled. The total oxide thickness is 6043 Å, against a target value of 6000 Å. By the end of the process this has been reduced to 5407 Å. Figure 4.11 shows the doping profile for this section.

4.5. Summary

This chapter discusses the application of process simulation to modelling the manufacture of integrated circuits. Both one- and two-dimensional simulation is considered, but with the greatest emphasis being placed on the one-dimensional simulator SUPREM-3. A review of the major physical and electrical models used by SUPREM-3 is included along with a description of the type of input data that is required by the simulator and the output it can generate. The current generation of two-dimensional simulators is then compared with SUPREM-3. Although providing useful capabilities for modelling lateral diffusion in small geometry devices they are found to lack the accuracy of SUPREM-3 and demand a much greater computational overhead. Finally, a demonstration is given of how SUPREM-3 can be calibrated to a process, so that the results produced by the simulator match well with the target values for the measurements made during the process.

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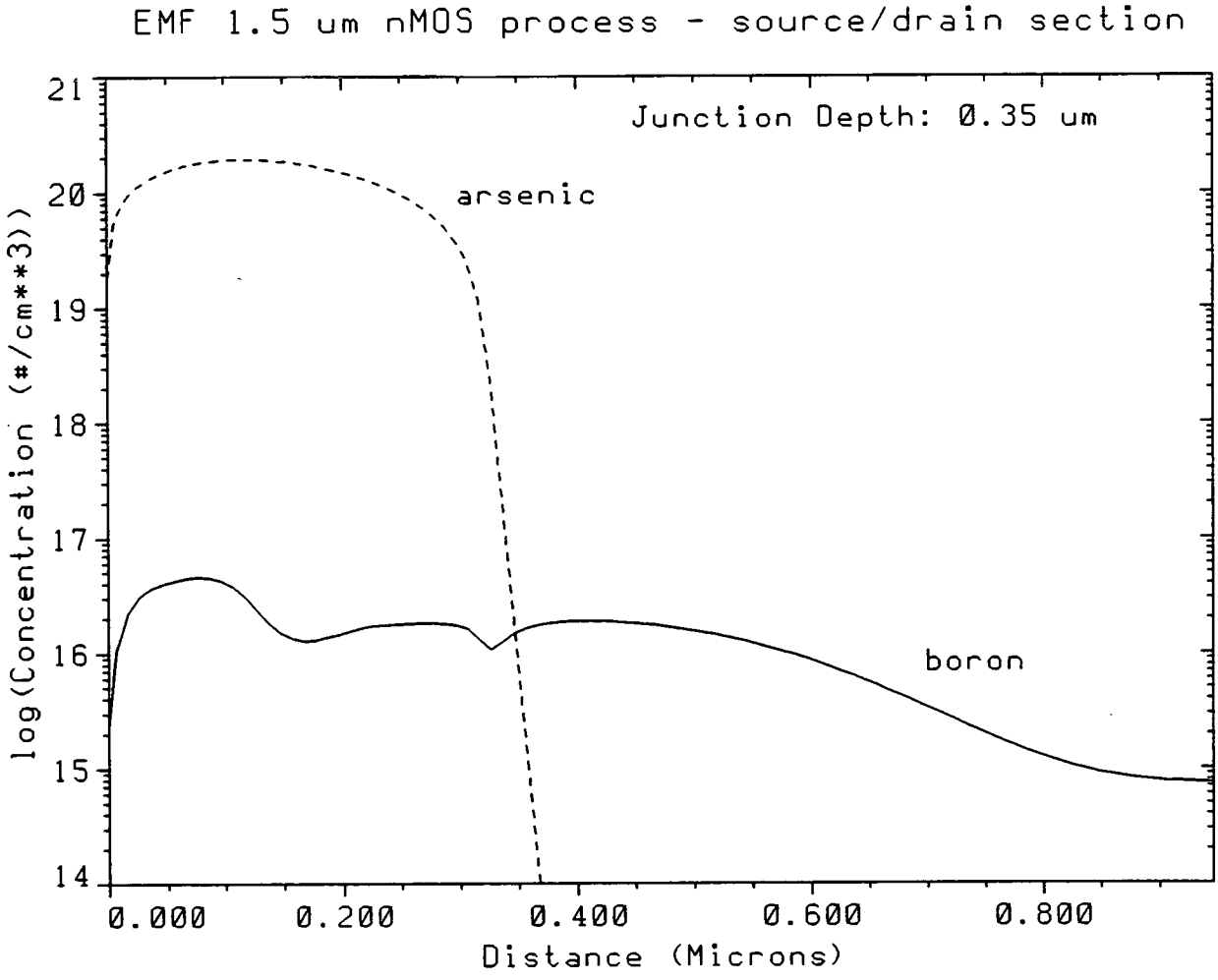

Figure 4.9 1D doping profile through the source-drain region of an nMOS device.

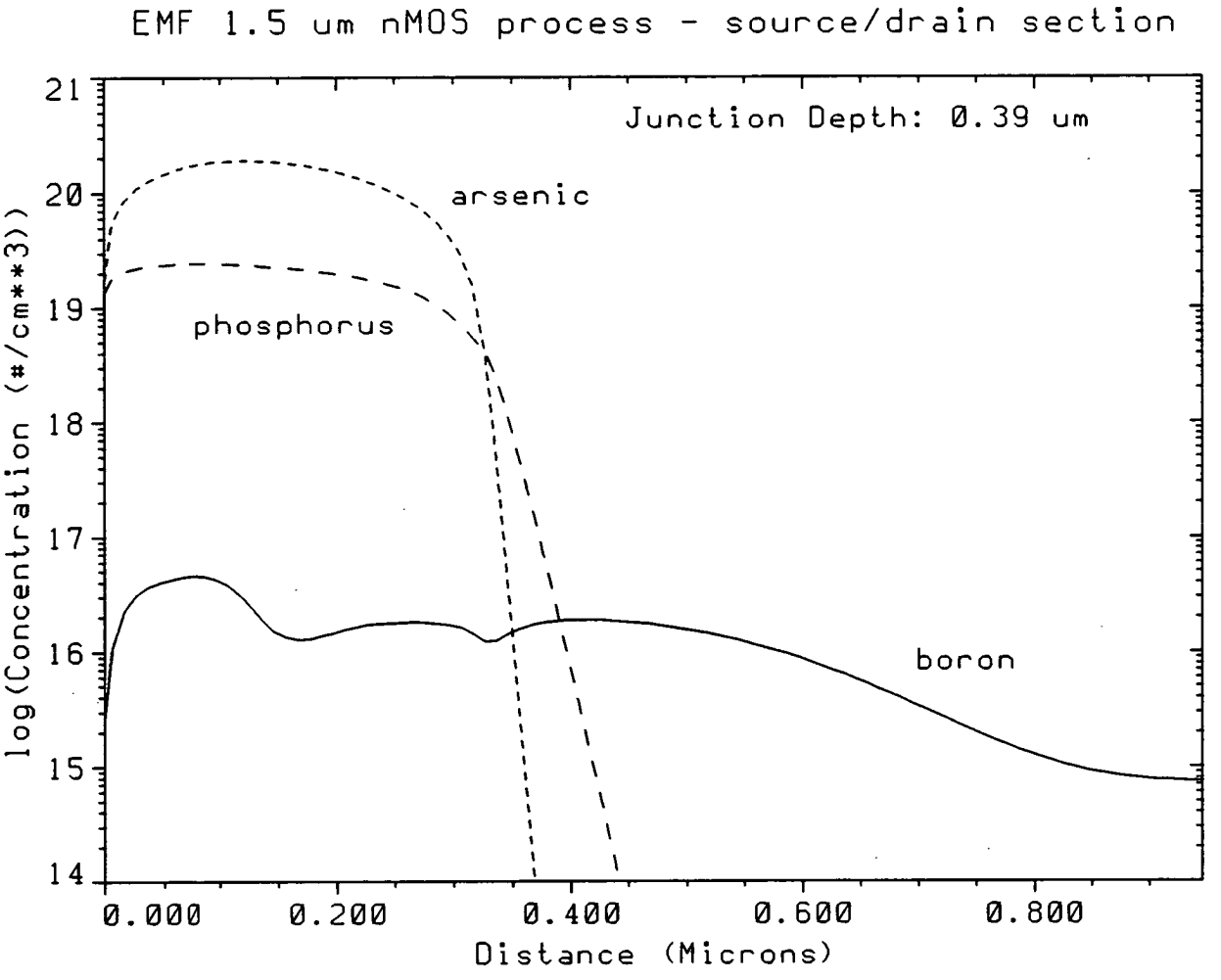

Figure 4.10 1D doping profile through the contact area within the source-drain region of an nMOS device.

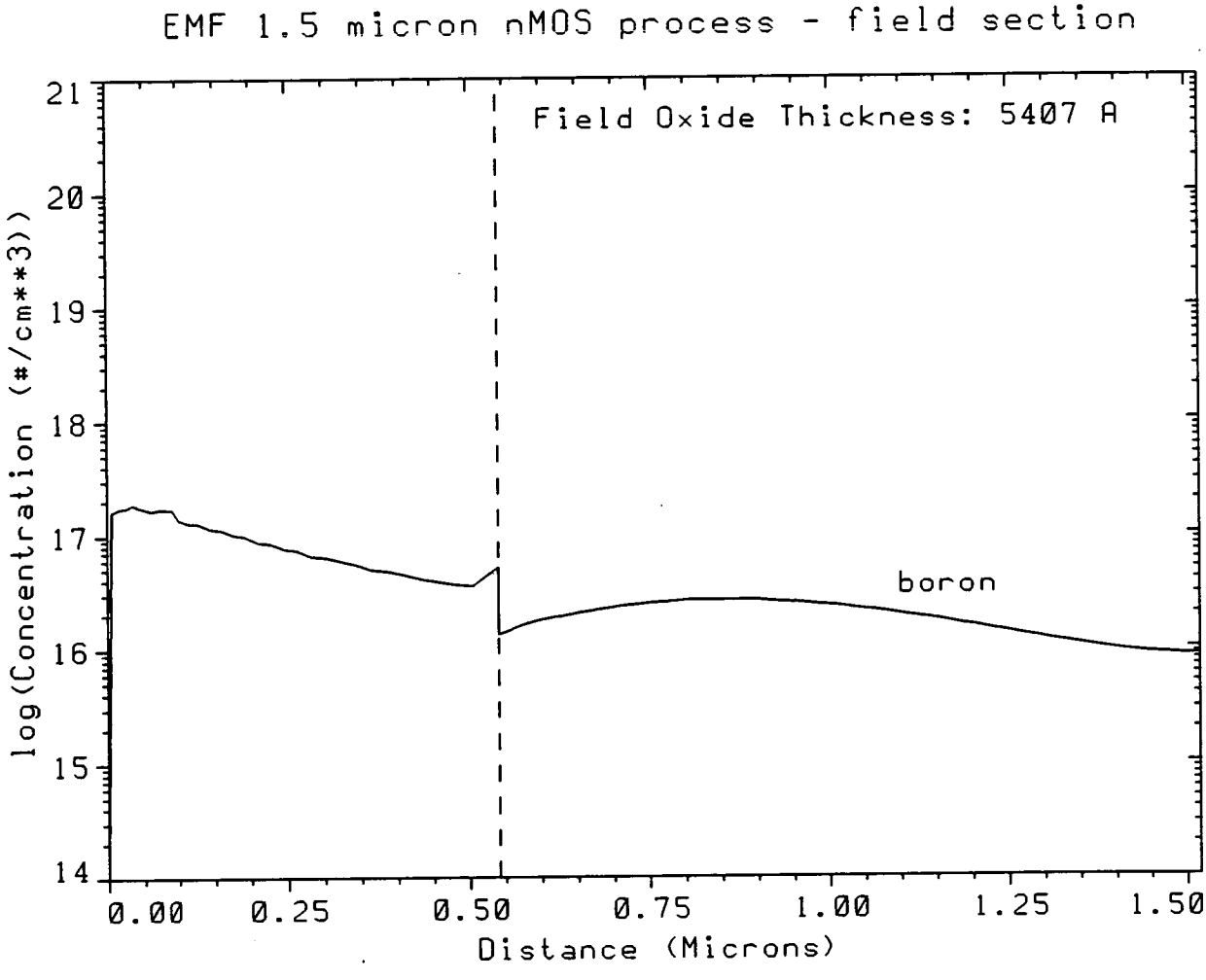

Figure 4.11 1D doping profile through the field region of an nMOS device.

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Chapter 5

Enhancing On-line Analysis and Control of IC Fabrication

5.1. Introduction

In order to control any manufacturing process it is important to be able to specify process then track and understand how it changes over time. The process is normally specified by defining the production sequence and each operation in the sequence. Engineering data can then be collected and analysed to characterise the products being made, the processing equipment and the process itself. This data can then be used to reduce variability, increase yield, and improve productivity. For IC fabrication, data analysis has become widely applied within the context of computer aided manufacturing (CAM) systems. These systems were originally developed to satisfy the needs of largely stable, and therefore commodity, manufacturing. Thus they are well suited to production tracking and control. However, the CAM systems which are currently available do not support the kind of tools that are necessary for the analysis of flexible manufacturing and for performing on-line process control.

This chapter sets out to describe the contributions this PhD makes to the analysis and control of flexible IC manufacturing. Firstly, process simulation has been integrated with a CAM system to make modelling of the fabrication sequence available as an analysis tool for the manufacturing environment. Thus by using information stored within the CAM system it becomes possible to interactively explore processing options on a lot-by-lot basis. Secondly, the CAM system has then been enhanced by including a method for explicitly describing the fabrication process within its database. The availability of recipe management at the host level allows on-line control of flexible production.

5.2. A New Method of Process Analysis

Semiconductor CAM systems have emerged as an effective method for reducing the number of misprocessed lots, lowering work-in-progress, shortening cycle times, reducing

lead-times and improving yield. Control of processing is reactive and based on simple analysis being performed on data as it is collected. For example, in the COMETS CAM system, when engineering data is collected it can be compared with boundary conditions and then either the lot can continue processing, be put on hold, or warning messages can be sent. More sophisticated analysis can be performed using the Statistical Quality Control (SQC) module, to analyse trends in the collected data, or a third party statistical analysis package such as RS/1[†]. Statistical methods are becoming widely used for data analysis and reduction. Their successful application to the reduction of process variation has been well documented [1,2,3]. However, statistical process control (SPC) is dependent on there being a large volume of data available for analysis. Although for a stable manufacturing environment it is not normally a problem as process steps are repeated consistently, this need not be the case for a flexible manufacturing environment. For example, a spin-on-resist step will be repeated many times throughout a process and will normally be expected to produce the same thickness and uniformity of resist. Therefore, it is possible to measure the critical process parameters for every occurrence of this step and use SPC to obtain a consistent resist thickness. However, an oxidation furnace may be used during a process to perform both initial and gate oxidations. Since the furnace will therefore be expected to continually change its operating range, it can become difficult to build up a statistically valid characterization of the equipment.

It is evident from this argument that alternate capabilities are required to analyse flexible manufacturing. For example, in an ASIC production facility, the presence of many products and processes makes short lead times important, and also makes yield significant on a lot-by-lot basis. Thus increased information collection and accessibility is necessary. In order to be able to satisfy these requirements it must be possible not simply to analyse a process, but analyse the processing of individual lots. Statistical methods are not suitable for this sort of task and a new approach must be taken to analyse processes in a flexible manufacturing environment.

For a commodity production facility, the rationale for lot-by-lot process analysis lies in the, often poor, match between product and process tolerances. This allows product lots to give a very low yield despite each of the processing parameters remaining within their respective specifications.

[†] RS/1 is a product of BBN Software Inc., Mountain View, CA, USA.

Process simulation could potentially be used to overcome these problems by modelling the fabrication sequence for each lot. However, current process simulators are not suitable for application to manufacturing environments. Their interfaces were designed for use in research facilities and as a result allow great flexibility, but at the price of complexity. This complexity means that a long learning period is required before the simulators can be used effectively. Process simulators also tend to run in batch mode which makes it difficult to perform interactive simulations. It is largely for these reasons that process simulation has never been applied to manufacturing analysis and control.

Process simulation can be made available in the manufacturing environment by integrating it into a commercial CAM system. In this way the simulator adopts the interface of the CAM system, and becomes a new functional module of the generic CAM model described in chapter 3. Figure 5.1 shows the enhanced CAM layout. However, to make process simulation an effective tool for the manufacturing environment a new approach must be taken to applying its functionality.

For the analysis of a manufacturing process, the simulator must be capable of simulating the complete process. If the simulator is calibrated to the processing environment then it can be used to analyse how changes in control parameters will effect the electrical characteristics of the fabricated devices; ie. differential analysis. Taking this further, it should be possible to perform this analysis at the level of the process step. Hence making it possible to investigate the relationships between individual process steps. For example, a process engineer could simulate a process step by simply naming that operation rather than having to form the full set of input statements that are required by the simulator.

To work effectively the simulator must have a global and consistent view of the data used to describe the process. This is important as the simulator is potentially modelling all the interrelations between process steps.

These factors suggest that not only should process simulation be accessible through the existing CAM interface, but that the simulator should use the processing information stored within the CAM system. In this way it would be possible to perform powerful *what-if* and *look-ahead* type simulations. For example, what-if a lot is processed on a rework sequence of steps, or, what-if the control parameters for a particular step were modified. Once such what-if simulations have been performed, then the user could look-ahead to the end of the process to see what effect any change in processing might have on the electrical characteristics of the fabricated devices.

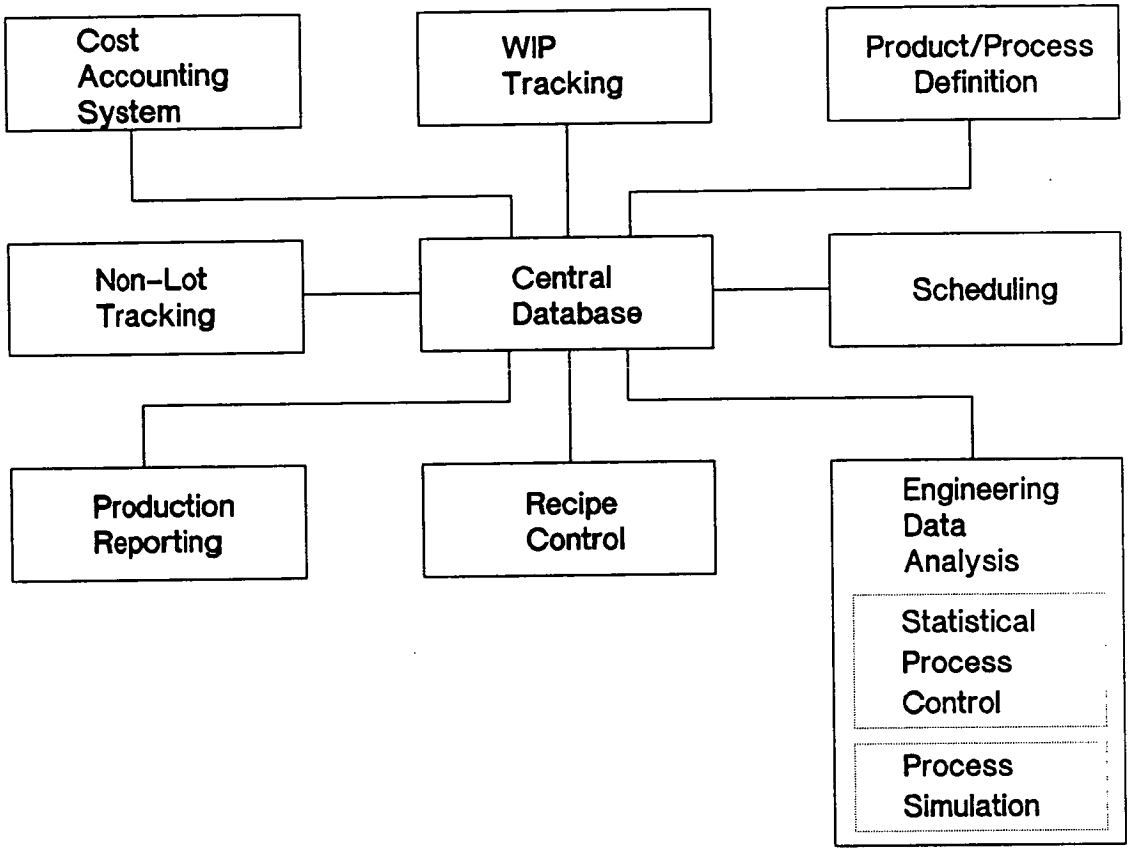

Figure 5.1 Process simulation as part of a generic CAM system.

These tools for the interactive analysis of flexible processing offer great potential for improving the engineer's understanding of a process. They might also be applied to investigating options for corrective processing of a misprocessed lot; ie. feed-forward control. When it is essential that a particular lot meets specification and is fabricated on time, a tool that would allow options for corrective processing to be explored in a scientific way could be very valuable. Without a method for the formal analysis of processing options it would be easy to either scrap a batch of good wafers, or continue to process bad wafers; both of which are very expensive options.

The functions described here have been implemented using the COMETS CAM system. As COMETS is a modular system it was decided to develop a new module that would integrate a process simulator into the CAM package. Thus the SIM module was developed to make a set of process simulation functions available through the existing COMETS menu structure. Figure 5.2 show how the SIM module fits within the context of

the COMETS system. The simulator shown in this diagram is SUPREM. The initial implementation of the SIM module used SUPREM-II as this program was available on the same computer as COMETS. A later implementation uses the more advanced simulator SUPREM-3† which became available over the computer network during the course of this PhD. Both SUPREM-II and SUPREM-3 are one-dimensional simulators and are able to generate results in a short enough time to allow them to be used intuitively for process analysis. Two-dimensional simulators are currently too computationally expensive to provide this facility.

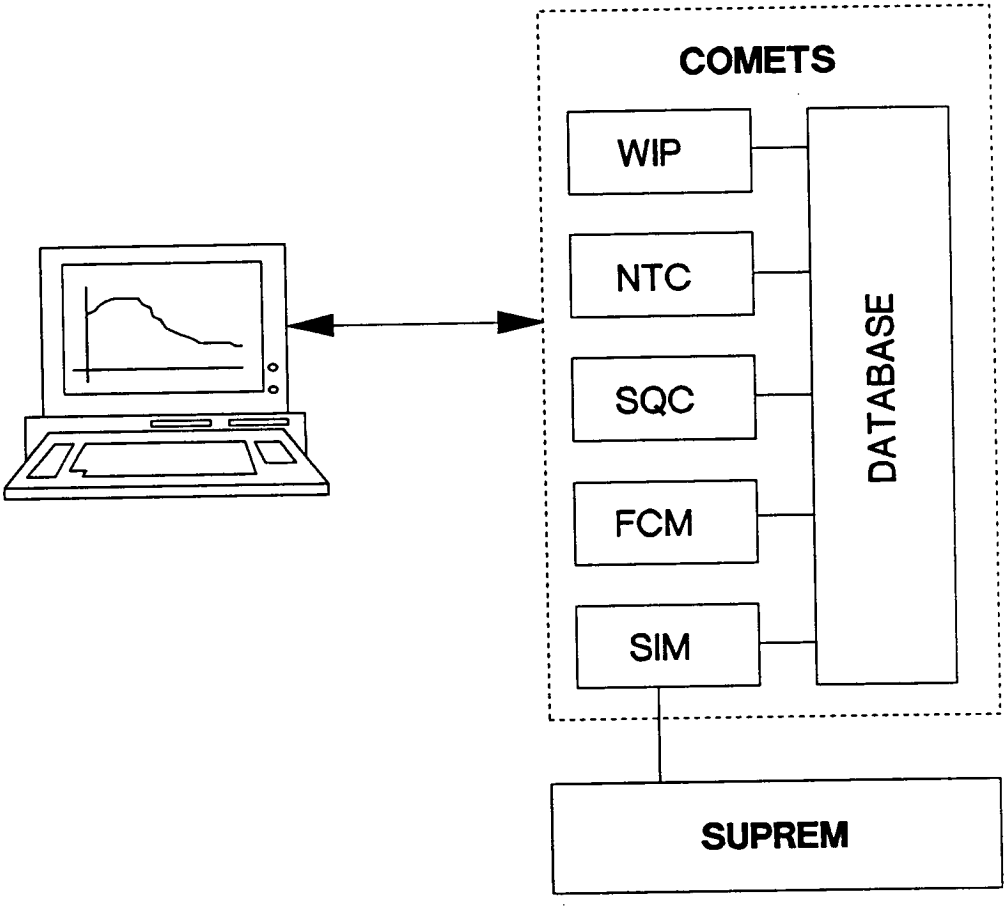

Figure 5.2 The SIM module integrates SUPREM and COMETS.

In order to parallel the generation of lot-histories by the COMETS WIP module the SIM module creates simulation-histories. As a lot moves out of a process step, the process-

† SUPREM-3 is a product of TMA Inc, Palo Alto, CA, USA.

ing is simulated and the results are associated with the lot-history for this step. Thus when a what-if or look-ahead type simulation is performed for a lot, the simulation is carried out from the current status of the lot thereby reducing the amount of time for the simulation. In cases where misprocessing occurs it is possible to resimulate a process step with modified input parameters in order to match the simulation to the actual processing. The results of the resimulation can then be associated with the lot-history for this step. Using the SIM module it is also possible to simulate the complete fabrication sequence that would be used for a product lot on a process. In COMETS terminology this simulation is performed for a PRODUCT. The SIM module also offers direct access to the simulator, which allows interactive simulations to be performed without the structured interface of the SIM module, and without the processing information stored within the CAM system. Figure 5.3 shows the menu hierarchy which gives access to the functions of the SIM module.

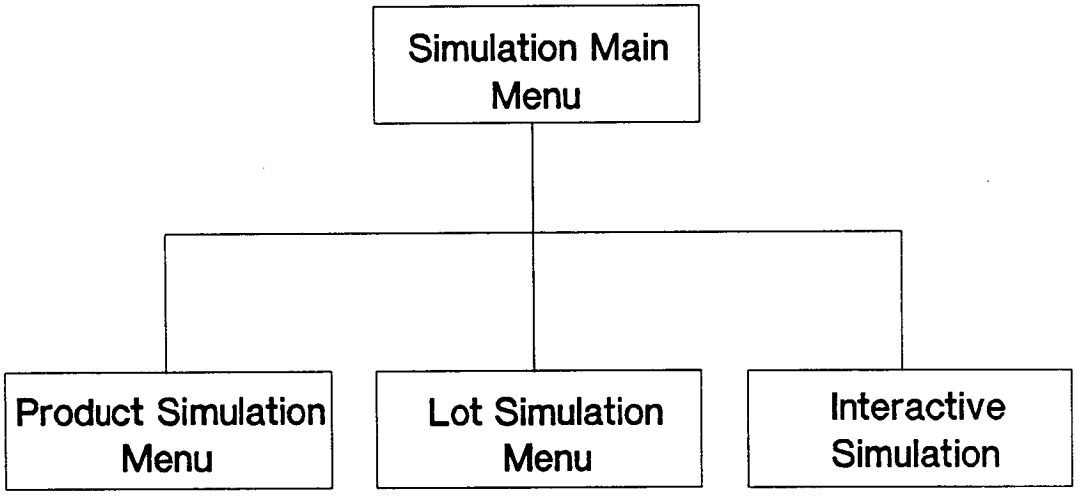

Figure 5.3 The SIM module menu structure.

In COMETS the processing sequence of a lot is described in terms of ROUTES and OPERATIONS, that are associated with the PRODUCT for which the LOT is to be created. The remaining processing information, such as equipment control parameters, is then stored in SPEC files which are attached to the ROUTE-OPERATIONS†. For the purpose of this discussion it is important only to note that the information used to control the processing at a step is maintained by the CAM system as a text file. The unstructured

† A full explanation of these terms and their application is provided in chapter 3.

format of the SPEC files make them suitable for storing the data required to control the simulations of the process steps. In this way, when a LOT is MOVED-OUT of a ROUTE-OPERATION the SPEC file will contain the input statements that are required to perform the simulation of this step. Figure 5.4 shows a SPEC file for a gate oxidation to which has been appended the SUPREM-II input statements that are required to simulate the step.

```
GATE OXIDE


Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen          20%     (1.5  l/min.)
HCl             15%     (0.15 l/min.)
Hydrogen        10%     (1.7  l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen  +  HCl
17min.Oxygen  +  HCl  +  Hydrogen
5 min.Oxygen

Measure: oxide thickness


**  FIELD
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
**  DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
**  ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
**  SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
```

Figure 5.4 SPEC file for nMOS gate oxidation with SUPREM-II input statements.

A possible application scenario for the SIM module is shown in figure 5.5. Here it is assumed that a lot is being processed normally when, after a particular step, a measure-

ment which has been made is found to be outside the expected range and the lot is put on hold. The SIM module might then be used by an engineer to analyse the misprocessing and investigate the possibility of corrective processing. The step is first resimulated so that the simulated results match the actual processing. The engineer can then use the SIM module to look-ahead to the end of the process to see if the misprocessing is likely to effect the electrical characteristics of the fabricated devices. If the simulated electrical parameters are still within specification then processing could continue as normal. However, if the simulated electrical parameters are out of specification then there are a number of possible options. The lot might be placed on a rework route, or some change to the standard process might be used to bring the electrical characteristics back within specification. These what-if type simulations could be performed many times, each followed by a look-ahead to the end of the process, before an acceptable solution is found. If no solution can be found then it might be better to scrap the lot and start again. The SIM module is not intended to instruct the user what to do; rather, it allows the user to explore the available options and make a more informed decision.

The presence of a process simulator within a CAM system also leads to the relationships that exist between process steps, and much of the contextual information for the facility, being captured. The result is that processes become better documented which makes it simpler to transfer them; whether that be to a different facility or to the same facility but some time in the future.

Expert systems may prove to play an important role in the application of process simulation to manufacturing. They can maintain qualitative information about a process so that it is not necessary to rely on exhaustive qualitative runs of simulation software to fully analysing a process. This would reduce the computational overhead associated with analysis by simulation and could lead to the use of more complex two- and three- dimensional simulators.

In chapter 6 of this thesis the integration of process simulation and CAM is described in detail, showing how the requirements for a flexible manufacturing analysis system have been realised.

5.3. Forming a Complete Process Definition

The unstructured format of the SPEC files allows whatever format of input statements required by a simulator to be assigned to a process step. This means that very little of the SIM module's code has to be modified if this simulator is replaced by another. However,

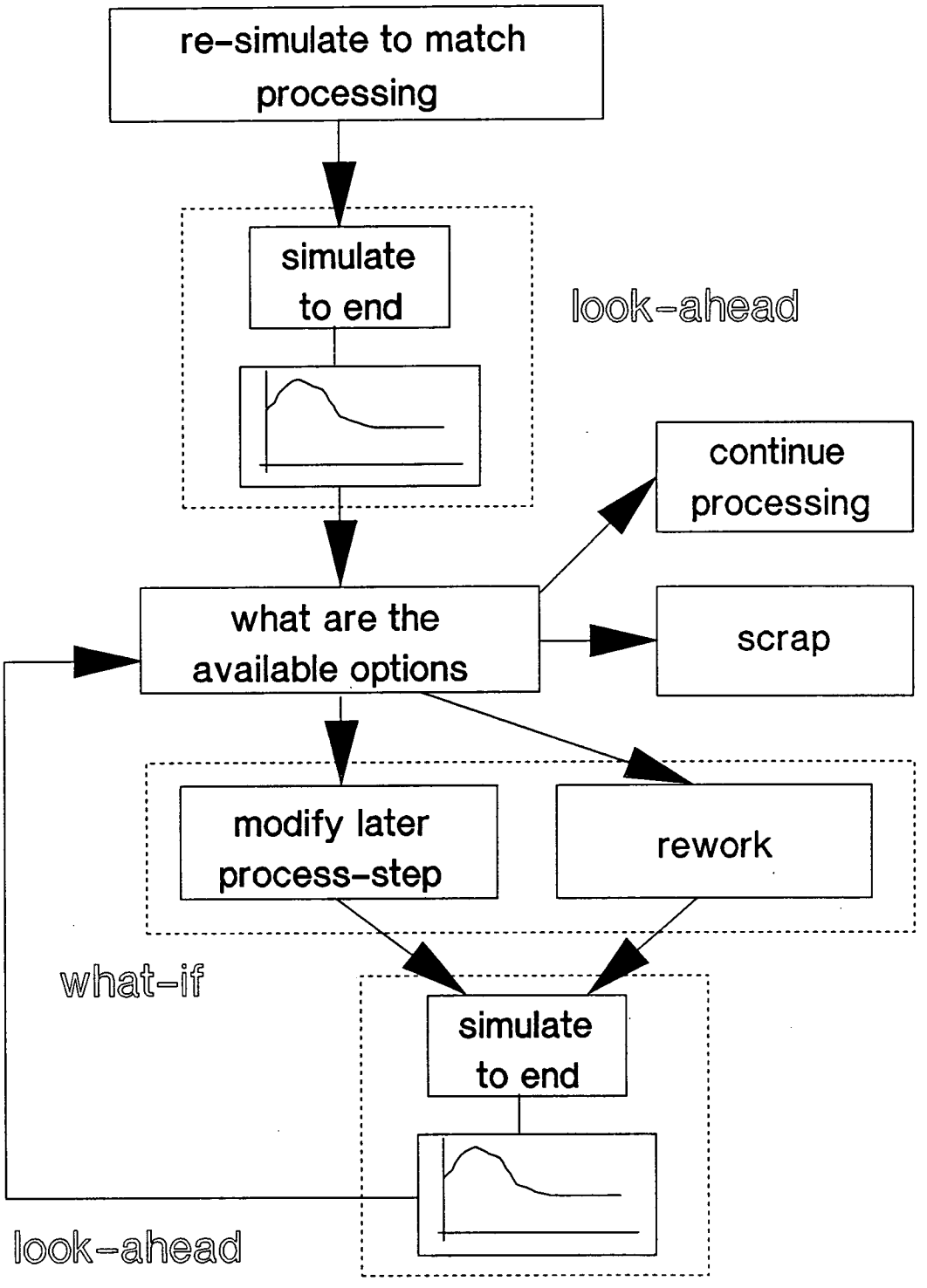

Figure 5.5 Flow diagram showing a possible application for the SIM module.

the control statements in the SPEC files are only accessible to the SIM module because markers are used to delineate the simulator input statements within the process recipe. In figure 5.4 the input statements are indicated by markers, such as '** FIELD'. It is necessary to enforce this sort of structure because though most of the information that is required by the simulator is already in the SPEC file it is unstructured and therefore inaccessible to applications programs such as the SIM module.

One of the results of the inaccessibility of process control data in the COMETS system is that when process information needs to be shared, then other systems are developed to perform the data management. Consequently data becomes distributed over a number of systems, often being stored in more than one place. This makes process definition, maintenance and security very difficult. Therefore it would be advisable to rationalise the distributed process data by enhancing the ability of the CAM systems to store this information in an accessible format. However, no systems currently exist which will allow this for semiconductor manufacturing.

Research into describing IC fabrication processes has focused on programming language [4] and knowledge-based [5] representations for semiconductor manufacturing. These approaches have identified some of the main requirements for a recipe description/management system; namely that the recipes be: complete, readable, portable, modifiable, and suitable for processing by other programs. However, they have been limited in their ability to describe the complexity of IC fabrication in a manufacturing environment. For example, in a flexible manufacturing environment there is virtually no limitation on how lots could move within a facility, and lots can also be split or merged at points in the process that cannot be identified *a priori*. This thesis presents an alternative method for process definition that takes advantage of the database structure inherent in a semiconductor CAM system; extending the structure so that it is capable of completely describing a fabrication process and its flow.

Storing a complete process definition in the CAM database would allow the SIM module to be driven directly from the database. This combination of information held within the simulator, describing the interrelation of process steps, and within the database, describing the equipment control and measurement target data, could be used to simplify the implementation of an existing process within a new facility. Typically, this might be of benefit in moving a process from development to production where there is rarely an overlap in the engineering staff and so knowledge about the process can be lost. Re-

developing this knowledge in the production environment is potentially a lengthy and expensive process.

The existence of a single source of production data could be combined with heuristic rules as part of an expert system to control the application of this information. Such a system could be used to aid many of the tasks which depend on this data: from process design, through analysis to scheduling.

Integrating the process definition into the CAM database would also require new data access screens to be added to the COMETS menu structure. Such an interface would alleviate the need for the user to be familiar with the input format required by the simulators and therefore, although requiring more coding, would allow the simulator to be changed without the need to re-educate the users. Using a single area for the storage of the process recipe data would also, as suggested earlier, simplify the definition of processes, reduce maintenance overheads, and allow security to be applied consistently to all production data.

Where the control of an automated facility has been considered, the control of processing is often placed at the cell level [6, 7]. Although the downloading of recipes to processing equipment can be performed at this level, particularly if the cell controller is in charge of a pool of similar equipment, it does not provide the global view of the processing operations that should be applied to a lot. A global view of processing is important when using the SIM module, when considering the scheduling of lot movement between processing stations, and when controlling the fabrication sequence in a flexible manufacturing environment. Controlling the processing of an individual lot, as might occur in ASIC production, using feed-forward control is only possible if the control system extends across all the process equipment that is involved. Therefore, to implement factory automation, control information must be passed from the host level system to the cell controllers and then on to the processing equipment. In return the equipment passes raw measurement data to the cell controller where it might be reduced before being passed up to the host. Figure 5.6 illustrates this relationship between host, cell and equipment. At each level of figure 5.6, however, the control information can take a different form. At the equipment level the control information will normally be proprietary and represented in a SECS format. The cell controller may perform the translation from an equipment-generic process recipe into the equipment-specific SECS messages. The process recipes will be defined and maintained at the host level. In the case of COMETS, the process recipe information should be

associated with the ROUTE-OPERATIONS of the PRODUCTS being fabricated. In this way, not only will the production sequence of a lot be defined, but also the processing.

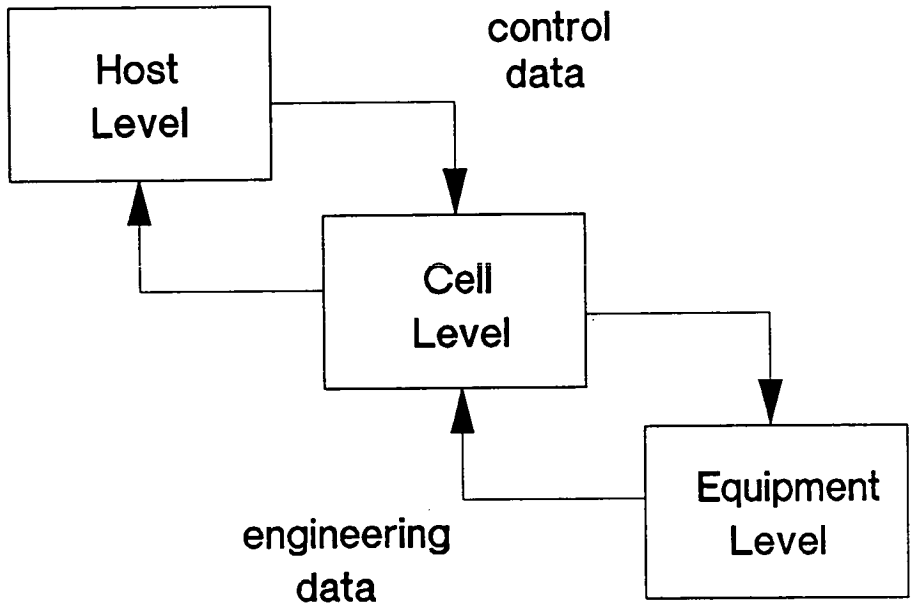

Figure 5.6 Flow of control and collected data in an automated factory.

Being able to specify a fabrication process within a CAM system means that the CAM system can then be used to control the process. In order that the control of each process step is applied for the correct lot on the correct equipment, process control must be tied tightly to the production control facilities of the CAM system. This means that the specification system must be capable of maintaining recipes for each process step, and be able to override these for particular lots, products, time periods, etc. For the specification system to satisfy the requirements of flexible manufacturing this recipe management must be controllable on-line and in real-time, while maintaining the security of the processing data.

The COMETS SPC module satisfies the requirement of associating recipe information with process steps, and allowing overrides to be applied. However, not only is the recipe data in an unstructured format but the overrides can only be applied to products and must be defined at the same time as the recipe. Thus the SPC module cannot be used for on-line control of processing. If a new recipe management system is integrated into COMETS

then it must replace the SPC module; it must provide structured storage of recipes with overrides that can be applied on-line; while retaining the best features of SPC, such as the inclusion of graphics. A new module has been developed which satisfies these requirements, it is called the Recipe Management (RCP) module and adheres to the interface and coding conventions used in COMETS.

The recipes maintained by the RCP module describe the processing to be performed at each ROUTE-OPERATION. They are therefore capable of describing oxidation, deposition, masking, etching, and so forth. Each of these types of process step requires very different information to be stored. Oxidation is defined by a set of parameters that include temperature, time and gas flow rates. Masking is defined by parameters such as reticle numbers and the names of stepper control programs. Thus the RCP module was designed to store information in a format which was not specific to the current generation of fabrication steps. Recipes are implemented as collections of text files, ingredients, and override recipes. The text files store information such as certain equipment set-up data and graphics that might be required by operators. Ingredients are intended to store equipment control parameters and other information that might be required by applications programs. Alternatively the ingredients can be used to store the names of machine specific recipes for environments which are not fully automated. Overrides have been implemented as additional recipes that are associated with the standard recipes but are only used if specified production conditions occur. Such conditions can be identified by:

- LOT NUMBER
- PRODUCT
- PRODUCT GROUP
- OWNER
- CREATE CODE
- TIME PERIOD
- EVENT
- ENTITY

In reality the relationship between a recipe for a process step and its control information is not as simple as has been portrayed. A recipe may consist of a number of sets of ingredients which must be applied one after the other. For example, an oxidation may consist of three separate phases; ramp-up, dwell, and ramp-down. Each of these phases will require a different set of ingredients. Thus in the RCP module a recipe will consist of text files, overrides and sub-recipes with their associated ingredients. Figure 5.7 shows this relationship.

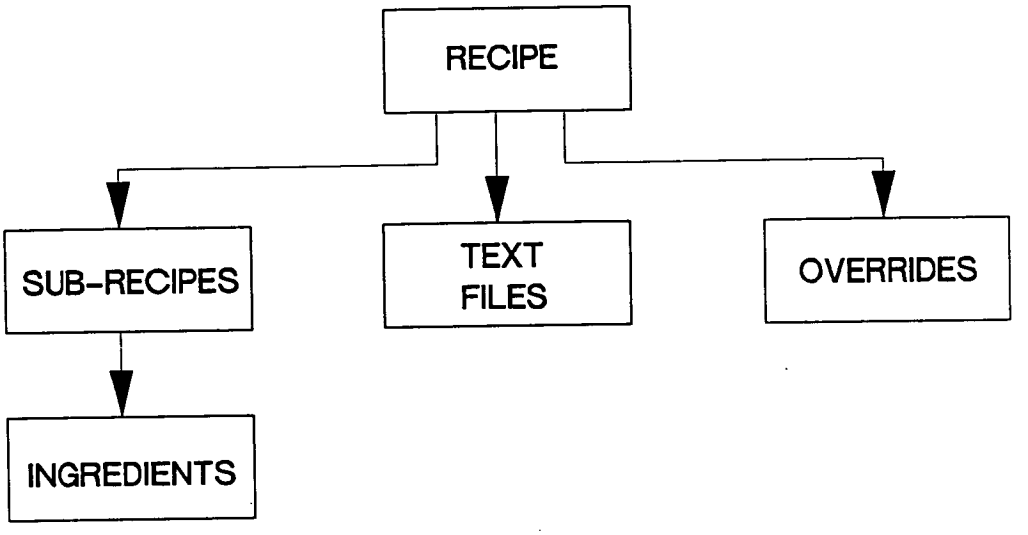

Figure 5.7 Relationship between data objects used by the RCP module.

As has been indicated, recipe data can be associated with processing equipment as well as lots. Thus we should be able to specify control parameters that are equipment specific, or simulation control data that is equipment specific. This data would then be merged with lot based recipe data before the complete recipe is made available.

The SPEC file of figure 5.4 can be translated into the sub-recipes and ingredients of figure 5.8. It should be noted from this example that each ingredient must be able to store the name of the parameter, a value and a unit. In environments where the process data is presented to operators, rather than automatically downloaded, it may also be desirable not to display all the process information. In this case, the parameters that are only required by the process simulator can be accessible only to the process engineer.

The interface of the RCP module for the definition and maintenance of recipes is an extension of the existing COMETS menu hierarchy. Menus have been created that will allow process recipes to be defined and then associated with processing points, either WIP or NTC. Menus have also been introduced that will allow override recipes to be attached with an existing recipe to a process point. Figure 5.9 shows an outline of the menu hierarchy provided by the RCP module.

By using the menus of the RCP module to define and maintain process recipes and their overrides, the COMETS CAM system can be used to control flexible IC fabrication.

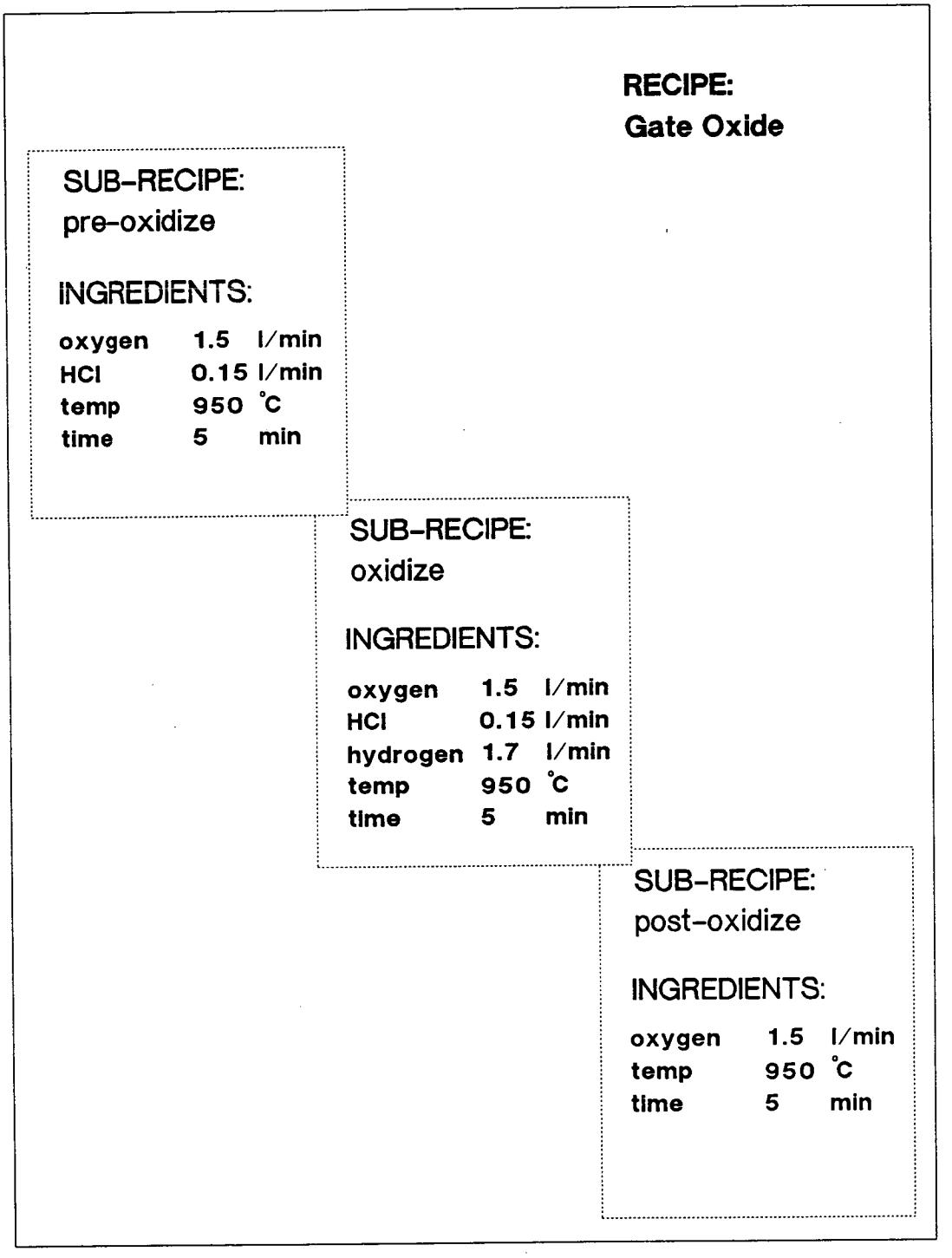

Figure 5.8 A process recipe for gate oxidation seperated into its constituent sub-recipes and ingredients.

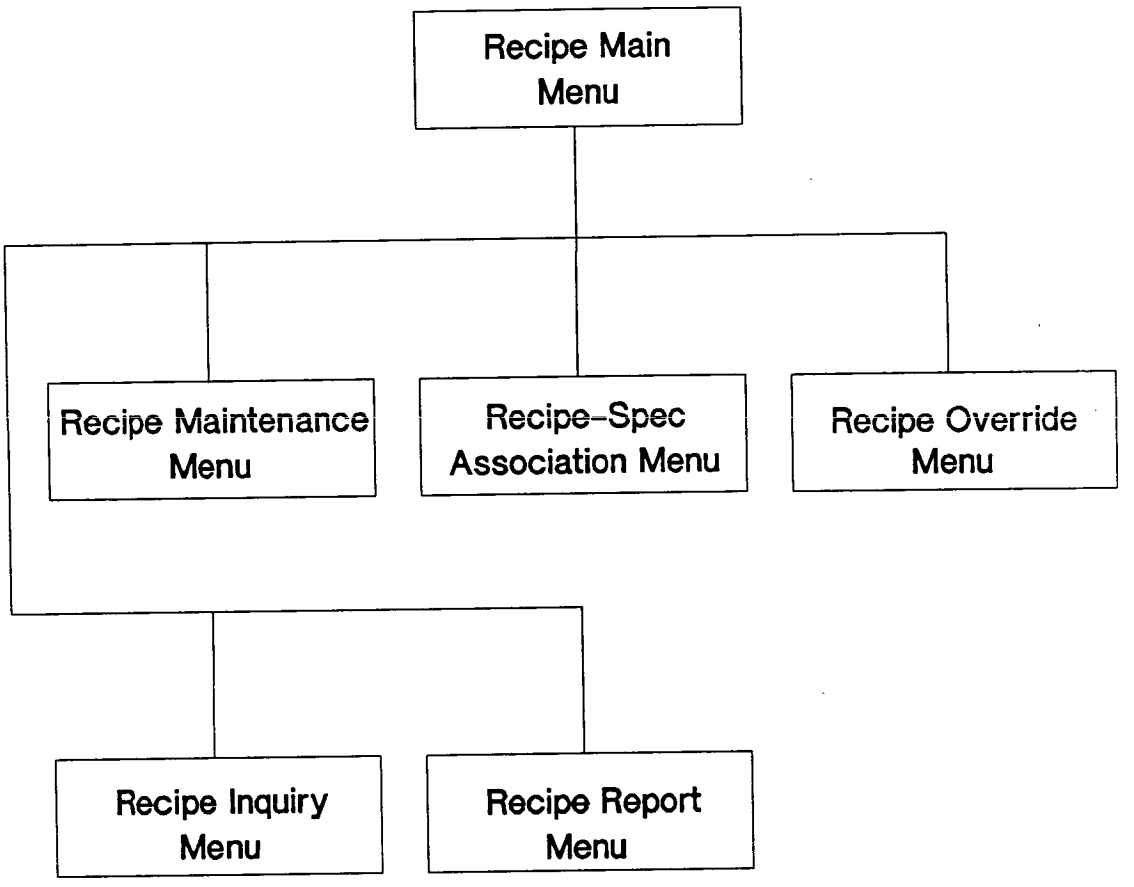

Figure 5.9 The RCP module menu structure.

Because of the generality of the implementation of the process definitions in this system it can also be applied to the control of assembly and test facilities. In an automated environment the process control parameters are available to be downloaded automatically, and in a non-automated environment the process ingredients can be inserted into the recipe text files and presented to the operators. The details of the implementation of this module and examples of its usage are presented in chapter 7 of this thesis.

5.4. Summary

This chapter has introduced original developments in the control of flexible IC production. Process simulation can be integrated with a commercial CAM system to provide powerful tools for the analysis of processing on a lot-by-lot basis, and can be used to investigate options for corrective processing when misprocessing occurs. This has been achieved by the development of the SIM module, which acts as an interface between user and simu-

lator. The importance of allying such a tool with a structured and explicit description of the process has been noted. In particular its application to process transfer, and the potential of expert systems that could be used to simplify the interpretation and application of the data.

To provide this capability, the CAM system has been enhanced by another module, RCP, which allows recipes to be defined, maintained and updated on-line. The recipes can also be overridden thus allowing on-line control of processing for individual lots, equipment, etc. Recipes stored in this way provide a host level view of the processing that occurs within a facility. As part of a CAM system, recipe management extends its data storage capacity to include all the information that would traditionally be stored in a runsheet in an explicit and generally accessible form. The result is that maintenance and security for a facility become simpler, which in turn adds to the integrity and quality of the information stored in the CAM system. It also allows provides a platform of explicit process data from which process simulation, and automated equipment control, can be performed.

It is believed that this is the first time that process simulation has been made available as a manufacturing tool, and that on-line recipe management is essential to the control of a flexible IC fabrication facility.

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Chapter 6

Integrating CAM and Process Simulation

6.1. Introduction

The increasing complexity of IC processing, the growing need to manufacture a variety of products within a single facility, and the rapid rate of change in product and process technologies have all given rise to the need for more sophisticated tools for process analysis and control. However, the current generation of CAM systems have so far proven to be unable to meet this need. This is largely due to the lack of knowledge, within these CAM systems, about the complex relationships that exist between the steps of a semiconductor process.

Potentially this problem could be tackled by introducing process simulation into the manufacturing environment, as a component of a CAM system. In reality, however, it is not obvious how this might be achieved.

This chapter presents a method by which process simulation may be integrated with a commercial CAM system to provide a set of powerful tools for process analysis and control. With these, an engineer can interactively explore a process so as to verify past processing and estimate the effect of future operations. This results in a better understanding of the process within the manufacturing environment, and provides a capability for analysing the fabrication sequence on-line and in real-time. These tools can also be used to aid decision making for feed-forward control.

6.2. Requirements and Constraints

In developing a system which integrates CAM and process simulation three goals were set for its functionality. These were:

1. To make process simulation available for diagnostic analysis of processing in a manufacturing environment.

2. To help provide the process engineer in the manufacturing environment with a greater understanding of the relationships that exist between process steps.

3. To allow feed-forward control in real-time.

Achieving these would require a commercial CAM system so that the system could be demonstrated to apply to real world production environments. The CAM system should therefore act as the operating environment for the simulator so that users would be familiar with the interface and would be constrained to use the simulator in such a way as to simplify the task of process analysis. This would also reduce the need to develop an expert knowledge of the syntax and structure of the simulation control statements. In order for the simulator to be used intuitively, it is also important that the simulations be interactive, providing a fast and graphic interpretation of the effect of a process step to the user. Finally, the data to control the simulator should be held within the CAM system. This should be the case for both the statements required to simulate each step, and to calibrate the simulator to the process. This would allow users to concentrate on the interrelation of process steps and their effect on device characteristics if they did not wish to become involved with the actual data required to model each step.

The choice of the COMETS CAM system as a basis for the introduction of process simulation into the manufacturing environment was a major constraint on the approach taken to implement this enhanced system. However, the ideas demonstrated by this implementation are free of any such constraint.

To simplify the portability of the new system to other sites, no modification should be make to the COMETS code or to the structure of the database. If this could be achieved then it would be possible to avoid the need to upgrade the simulation integration software as the CAM system was upgraded, thus reducing maintenance requirements. To simplify further development and maintenance the software should also follow the coding conventions used within COMETS. This included the use of the COBOL language and the adoption of the methods used by Consilium to access the database, present screens and handle errors.

Finally, the new system should be adaptable enough that any simulator might be used, with the minimum of change being required to the system code.

6.3. Developing the SIM Module

To achieve this level of functionality a software module, called SIM, was developed. As figure 6.1 shows, the SIM module interfaces with a number of other COMETS modules. Each of these modules (WIP, SPC, FCM and, optionally, SCR) are required for the SIM module to work.

To maintain the integrity of the COMETS system and to allow for upgrades, SIM makes extensive use of the user exits and the General Tables System (GTS). The code is written in Cobol with the exception of some Fortran graphics routines. When interfacing with the VAX/VMS operating system, logicals and routines from the Run Time Library (RTL) are used.

From the point of view of the user, SIM consists of four parts:

1. In-process simulations which are used to maintain a simulation log of the processing for each lot.
2. The product simulation menu which allows the processing of individual products to be simulated and the results inspected.
3. The lot simulation menu which allows *look-ahead* and *what-if* simulations of individual lots to be performed and the results inspected. It also allows the simulation histories of lots to be investigated.
4. The program INTERSUP which allows SUPREM to be used interactively.

The in-process part of the SIM module was developed to integrate CAM and process simulation at the level where the CAM software actually interfaces with the processing of lots in the clean-room. Therefore, the process step of SUPREM required an equivalent object in the COMETS database; the most obvious candidate being ROUTE-OPERATION. Figure 6.2 shows a simple data model of the objects used within COMETS for WIP tracking. It is also necessary to be able to specify the one-dimensional sections simulated by SUPREM. These are defined by the identifier SECTION.

The MVIN function was chosen to be the point where a process step should be simulated since it is a WIP function which can always be associated with a ROUTE-OPERATION, and is called prior to any processing of a lot being performed. Within the MVIN code, two user exits are available: USR500 and USR010. The latter was chosen to

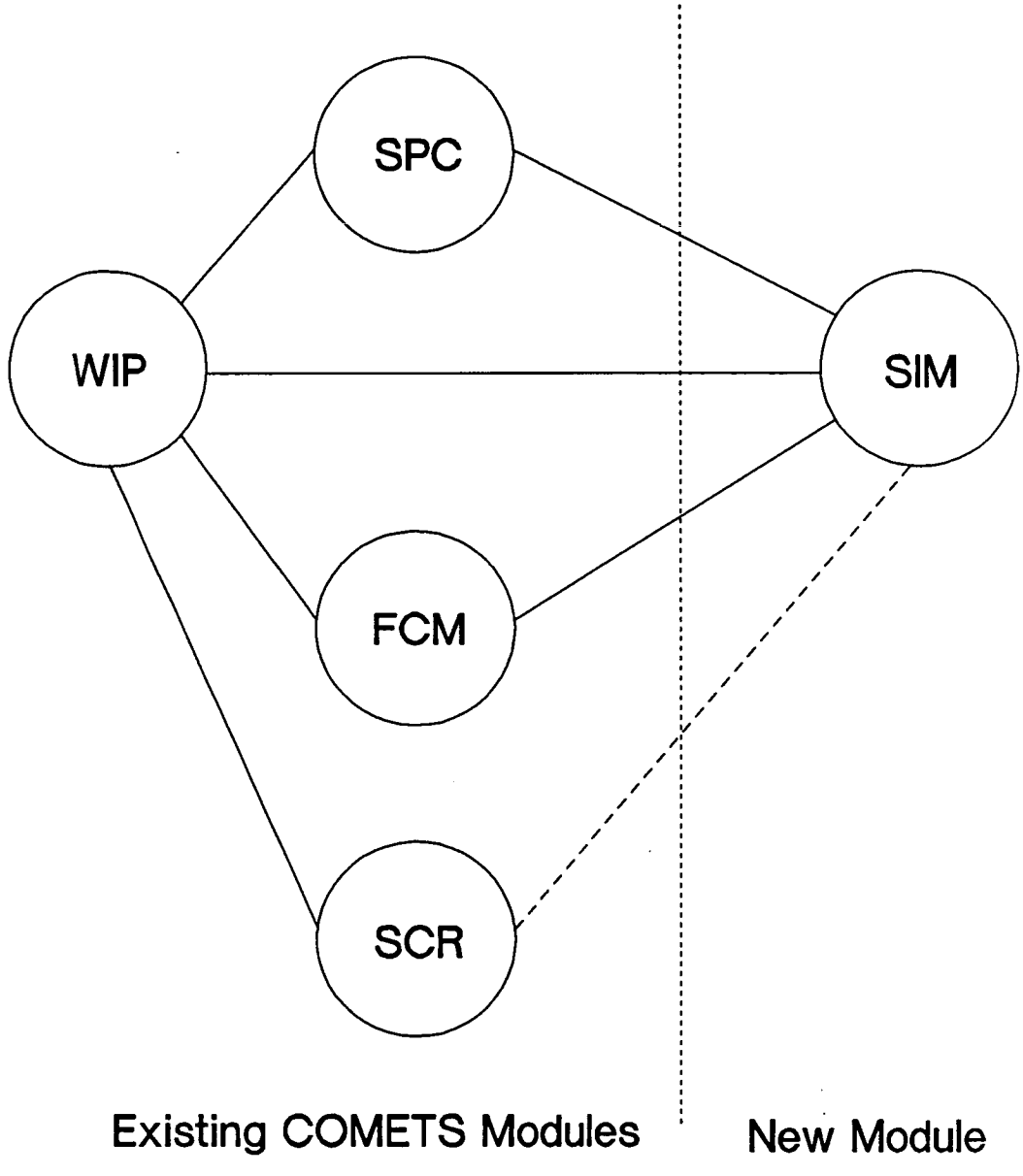


Figure 6.1 The SIM module interfaces with some of the existing COMETS modules.

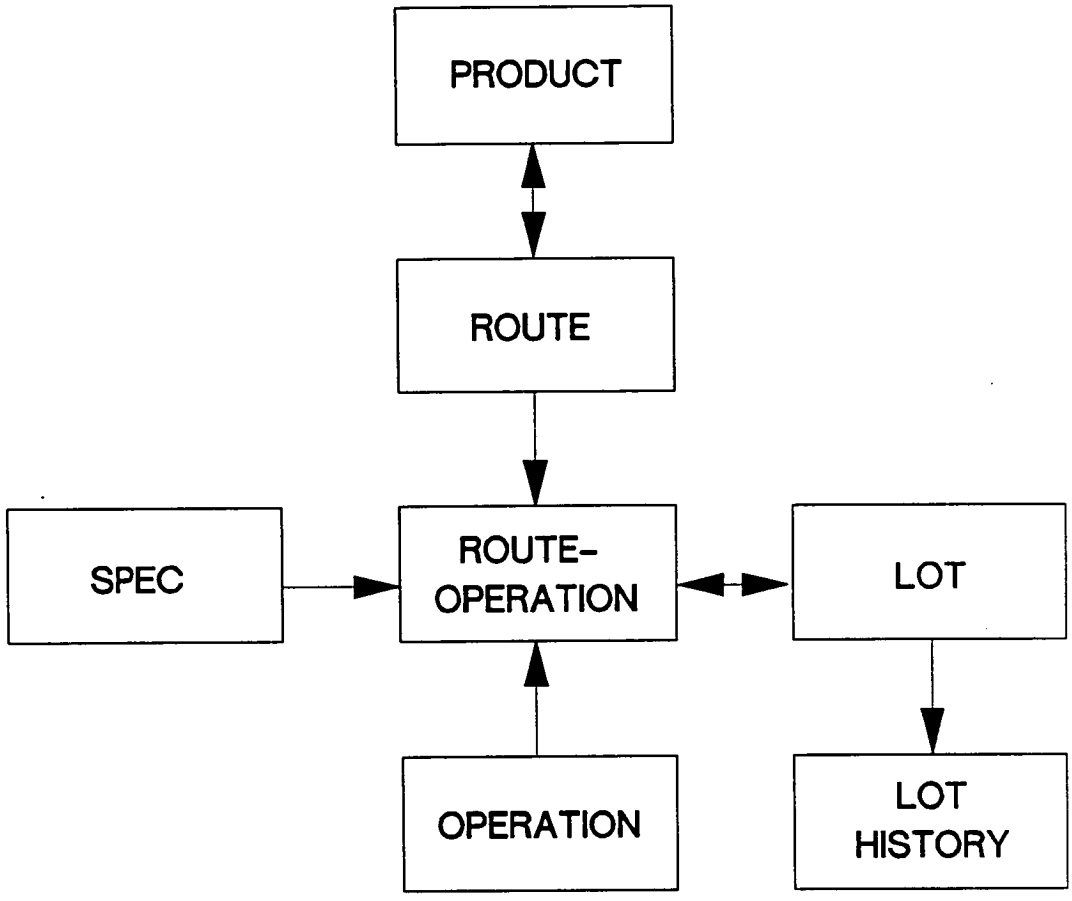


Figure 6.2 Data model of objects used by the COMETS WIP module.

attach the simulation code as USR010 is called only once, whereas, because of the review facility, USR500 could be called many times, causing many unnecessary simulations to be performed.

To automatically simulate each step, the data to run SUPREM has to be stored in the CAM system without modifying the database. Using the GTS for this purpose was explored but proved to be restrictive on the way data was stored, and it was also awkward to use. Instead the text files of the SPC module were chosen because they do not restrict the format or number of SUPREM statements required to simulate a process step and also enforce some structure on the way simulation control data is maintained, ie. through the AUTHORIZATION, SCANNING and FREEZING of SPECS. SUPREM processing statements are added to the bottom of each SPEC file as show in figure 6.3. Four sets of SUPREM statements are required to define an nMOS process (field, source-drain, enhancement channel and depletion channel), each is preceded by a line with two stars

and a character string. The stars identify the beginning of each SECTION and the character string is the SECTION-NAME. As with the MVIN function, SPEC files can be associated with ROUTE-OPERATIONS.

```
GATE OXIDE

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen          20%     (1.5  l/min.)
HCl             15%     (0.15 l/min.)
Hydrogen        10%     (1.7  l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
2.2 min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure: oxide thickness


** FIELD
STEP TYPE=OXID,TEMP=950,TIME=12.2,MODL=NIT0
** DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
** ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
** SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
```

Figure 6.3 A recipe file for gate oxidation which has been extended for use with the SIM module.

As a lot is completing the MVIN, control is passed to the user exit, this calls the simulation routine for each SECTION in the ROUTE-OPERATION SPEC file which validates the SECTION-NAME against a table - SIM$SECTIONS - in the GTS. The SUPREM input file is generated from both the SPEC file and data held in the PRODUCTS user defined fields. A sub-process is then spawned to run SUPREM. All the files

generated are in a directory pointed to by COMETS$SIMULATIONS, with each set of files having a unique identifying prefix. This is formed from the LOT-NUMBER, the SECTION-NAME, the ROUTE and the OPERATION. Each simulation run produces four files, denoted here by their suffixes:

LIS - The SUPREM input file.

DAT - The data file produced by SUPREM.

SAV - The structure of the section after the current simulation step. The next step for this lot and section will use this data as a starting point.

LOG - The completion status of the simulation.

Feedback to the operator is confined to messages written to the bottom of the screen announcing the completion of each simulation. In the event of an error occurring during the simulation a mail message is sent to the user names held in the FCM table called SIM$MAIL.

When processing is being controlled using SCRIPT, the START instruction must be used in order to perform the in-process simulation. Following this, the CALL USER ROUTINE instruction may be used to produce, on a graphics screen, a plot of the doping profile for the current LOT. For example:

```
CALL USER ROUTINE "PROFILE ENHANCEMENT"
```

where ENHANCEMENT is the name of the SECTION. When this facility is used the user exit USR018 calls routines in the SIM module to actually produce the plot.

The product simulation menu, lot simulation menu and INTERSUP are accessed through the simulation main menu which is in turn accessed through the user main menu, ie. the user exits USR001 and USR002.

6.4. The SIM Menu Structure

Each function of the SIM module is represented by a four character mnemonic, the first of which is always a zero. This is so that these mnemonics do not clash with any that may later be introduced by Consilium. The functions made available by the SIM module menus are discussed below.

Simulation main menu (0SIM)

This menu (figure 6.4) shows the available functional menus within the SIM module. Although useful to the novice user, more experienced users would normally directly invoke the specific function they wished to use.

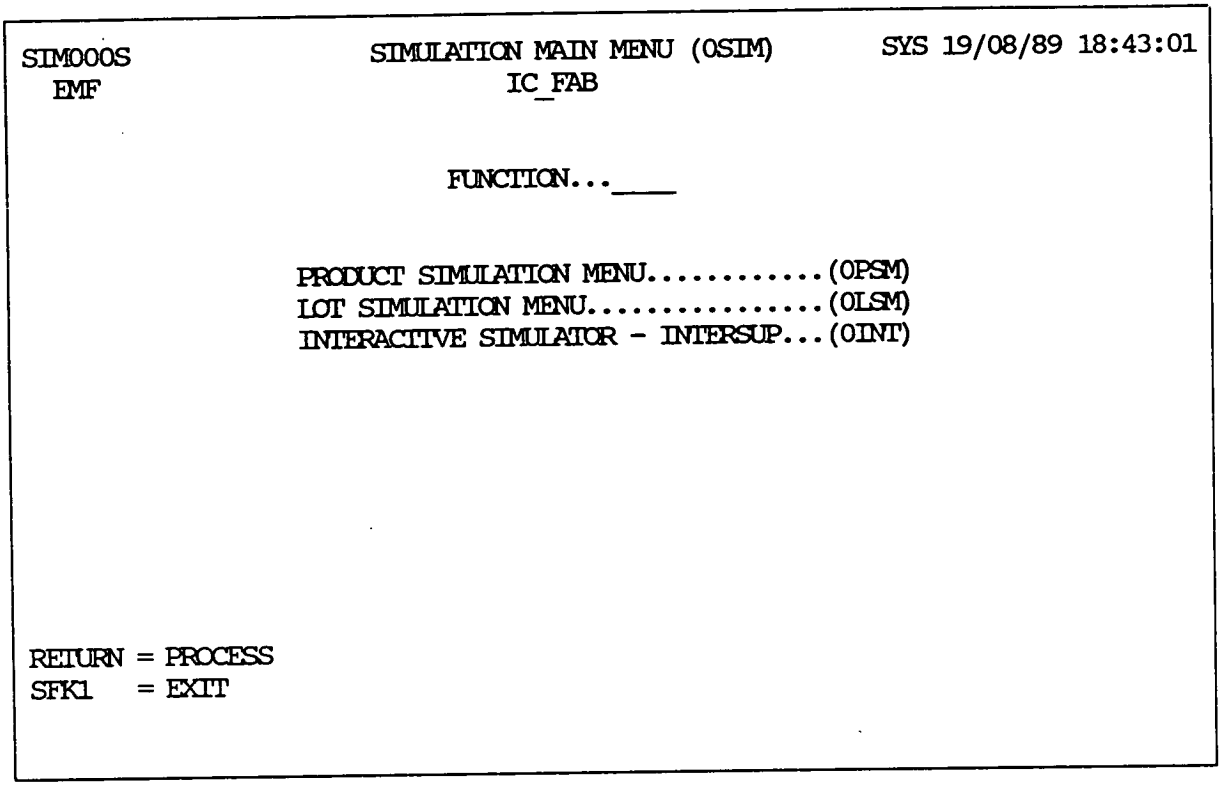


Figure 6.4 Main menu for the SIM module.

Product simulation menu (0PSM)

The functions under the product simulation menu (figure 6.5) allow the fabrication of a lot to be simulated and the results of the simulation inspected both on screen and as hardcopy. The availability of this facility is particularly important in environments where processes are variable. For this menu a valid PRODUCT and SECTION must be specified. A valid SECTION is defined as a 1D simulation section name as held in a GTS table. The valid names relate to the simulation control data held within the SPEC files. For example the section 'FIELD' in figure 6.3.

The simulation of the fabrication of a SECTION is performed using the 0PPS function. The results of the simulation can be inspected either: on screen using 0VPP and

```
SIM010S                  PRODUCT SIMULATION MENU (OPSM)          SYS 19/08/89 18:43:16
  EMF                              IC_FAB


                        FUNCTION.....____
                        PRODUCT.....________________________
                        SECTION.....____________


                PERFORM PRODUCT SECTION SIMULATION.....(OPPS)
                VIEW DOPING PROFILE OF PRODUCT SECTION...(OVPP)
                VIEW DATA FILE FOR PRODUCT SECTION.....(OVPD)
                PLOT DOPING PROFILE OF PRODUCT SECTION...(OPPP)
                LIST DATA FILE FOR PRODUCT SECTION.....(OLPD)



RETURN = PROCESS
SFK1   = EXIT                          SFK2 = HELP
```

Figure 6.5 Product simulation menu for the SIM module.

```
SIM020S                  LOT SIMULATION MENU (OLSM)              SYS 19/08/89 18:43:24
  EMF                              IC_FAB

                        FUNCTION.....____
                        LOT.....__________
                        SECTION.....____________
                        ROUTE (opt.).....__________
                        OPERATION (opt.)...____

               SIMULATE TO END OF PROCESS.....(OSTE)
               SIMULATE REWORK ROUTE.....(OSRR)
               (RE-)SIMULATE ROUTE-OPERATION.....(ORSC)
               INSERT SIMULATION RESULT IN HISTORY..(OARS)
               RETURN TO ORIGINAL SIMULATION STATE..(ORCS)
               VIEW DOPING PROFILE FOR SIMULATION...(OVDP)
               VIEW SIMULATION DATA.....(OVSD)
               PLOT DOPING PROFILE FOR SIMULATION...(OPDP)
               LIST SIMULATION DATA.....(OLSD)

RETURN = PROCESS
SFK1   = EXIT                          SFK2 = HELP
```

Figure 6.6 Lot simulation menu for the SIM module.

0VPD; or as hardcopy using 0PPP and 0LPD.

Lot simulation menu (0LSM)

The functions of the lot simulation menu (figure 6.6) allow verification of past processing as well as examination of the effect of future processing. For this menu a valid LOT identifier and SECTION name must be specified. The ROUTE and OPERATION are optional. If they are not specified then the current ROUTE-OPERATION is taken as the default.

Simulating to the end of the process using the 0STE function provides a powerful *look-ahead* capability. This allows investigation of how further processing will effect the physical and electrical characteristics of product devices. A variety of future scenarios, *what-if* simulations, can also be explored by using some of the other functions.

The effect of one process step can be examined by using 0RSC, while a rework route can be simulated by using 0SRR. When simulating to the end of a process after a rework the current process step is included in the simulation. After each set of simulations the current state of simulation can be reset to that of the last 'real' process step by using the 0RCS function.

The 0RSC function can also be used to re-simulate a process step where a lot has been misprocessed. The results of this simulation can then be substituted into its lot history by using 0ARS.

Inspection of the simulated results under this menu are performed in a similar way to the product simulation menu, using 0VDP, 0VSD, 0PDP, 0LSD. These functions also allow simulation lot histories to be examined.

INTERSUP (0INT)

Calling 0INT gives direct access to the INTERSUP program which allows SUPREM-II to be used interactively. This allows the simulator to be used without any of the restrictions implicit in the menu structures described previously. However, using SUPREM efficiently in this way does require the user to be familiar with the simulator.

All the data files used by the functions of the product and lot simulation menus are stored in the users current directory. This protects the files in the simulation history directory from being modified unintentionally. The only way in which data files can be inserted into the simulation history directory is by using the associate simulation history function, for example after the re-simulation of a process step.

The hardware used for this implementation is a VAX 8350 which runs COMETS and SUPREM-II. Although in a manufacturing environment a hardware platform would normally be dedicated to running COMETS, SUPREM-II is light enough on resources not to make a noticeable impact on the response times of most COMETS transactions.

6.5. Replacing the Simulator

In a further development of the system, SUPREM-II has been replaced by SUPREM-3. Making the change in simulators is conceptually a straightforward task as there is very little of the SIM module code that must be modified. The SPEC files, however, that contain the SUPREM-II statements must be edited to contain the equivalent SUPREM-3 statements. The only real complication is that SUPREM-3 is not licensed to run on the same hardware platform as COMETS.

The hardware used for the SUPREM-3 implementation is based upon a local area VAX cluster, where COMETS runs on a VAX 8350 (CAM1) and the simulation software on a MICROVAX 3500 (SIM2). Disk space is shared throughout the cluster so that splitting the system over more than one computer does not hinder data transfer. This implementation has the advantage that the I/O intensive CAM software does not interfere with the CPU intensive simulation software, which is important since the response times of a CAM system can become very long when a large number of transactions are being processed. Figure 6.7 shows the layout of the computing resources used during this phase of the project.

There a three techniques that could be used to run SUPREM across the network. The first would be to submit a command file, which calls SUPREM, to a batch queue on the SIM2 node. Though simple this method allows COMETS no direct control over how and when SUPREM is run. Its execution is more dependent on the priority of the queue than on when the job is submitted, requiring the SIM module to return control to the user and expect him to wait for a message confirming completion of the job. This fails the requirement for the SIM module to perform simulations interactively.

The second method for running SUPREM would entail creating a special account on the SIM2 node that is dedicated to running the simulator for COMETS. Using this method a command file to run SUPREM could be created within the file-space for this account, and the SIM module could perform a proxy login to run that command file on the remote node. The instruction to perform this is:

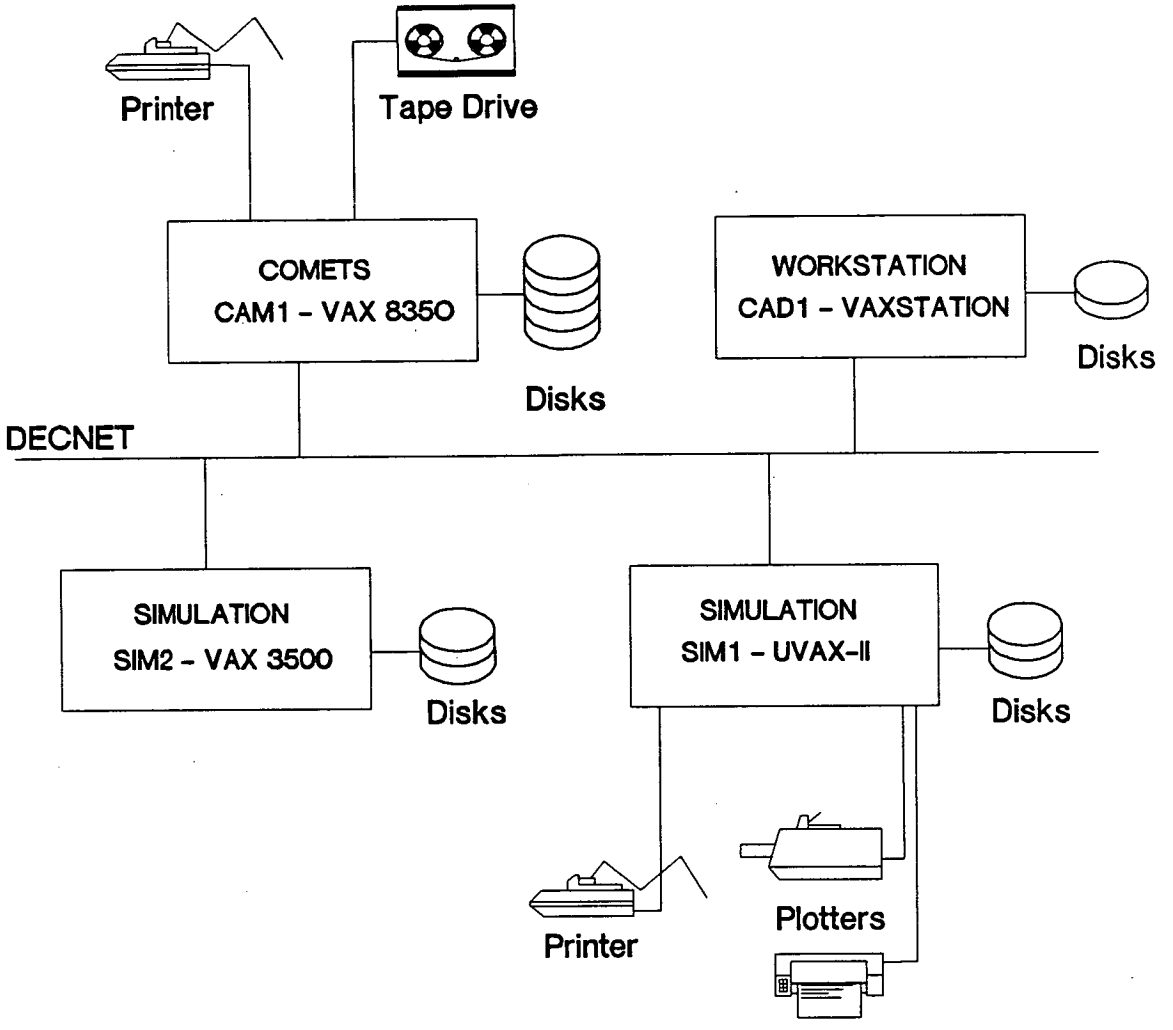


Figure 6.7 Layout of the network used to implement the integrated COMETS and SUPREM-3 system.

```
TYPE SIM2"username password"::"TASK=commandfile"
```

This is a simple method of transparently running the simulator across the node and gives the user interactive control over its running.

A third approach to running the simulator remotely would require another process to be running continuously on SIM2 and interfacing with the SIM module using VMS mail-boxes. This is the most sophisticated method and gives the highest degree of control, it also avoids the need for a proxy login to be performed before the simulator can be run. It does not, however, have the simplicity of the other methods.

In order to demonstrate the applicability of running SUPREM-3 across a network the second method was chosen as it provided the required functionality with a low software overhead. An account called COMETS was created on SIM2, which shares its home directory with the logical COMETS$SIMULATIONS. This is useful as it simplifies the file management that is necessary when running SUPREM-3 from within the CAM system. Below are listed the file types that can be created for a run of SUPREM-3, all but the '.COM' file are placed in the users home directory when the simulator is invoked from the LOT or PRODUCT simulation menus.

COM - The command file containing logical assignments and a call to SUPREM.

DAT - The SUPREM-3 input statements.

DIA - Diagnostic output.

INF - Informational output.

INT - PRODUCT/SECTION initialisation file.

LOG - Log file to capture data directed to the users terminal.

OUT - The file used to capture data sent to the standard output.

PLT - Plot file for hardcopy graphics.

SAV - Structure file saved for use as input to next step simulation.

SCR - Plot file for screen graphics.

Other temporary, data and diagnostic files are used by SUPREM-3 during a run, but these are of little interest unless a detailed investigation of the operation of SUPREM-3 is necessary.

The most significant addition to the list of files used by the SIM module is the '.INT' file, this contains the definition of the grid structure used to simulate a SECTION of a PRODUCT. For example, the FIELD section of a product called SRAM in a facility called EMF has an initialisation file called EMFSRAMFIELD.INT. This file is formed by the set of SUPREM-3 statements shown in figure 6.8. Each PRODUCT/SECTION to be simulated must have an initialisation file resident in COMETS$SIMULATIONS.

```
title   EMF 1.5 micron nMOS process
+       n-channel field section

$  Initialise the silicon substrate
initialize  <100>  silicon boron=7e14
+           thickness=1.25  DX=0.001 spaces=100

$  Save the initialisation file structure
$  for use by the SIM module
savefile    structure file=EMFSRAMFIELD.INT

stop
```

Figure 6.8 SUPREM-3 control file used to generate a '.INT' file for a specific SECTION and PRODUCT.

The only change to be made to the SIM module menu screens is the replacement of the 0INT function by 0DAS. This mnemonic stands for Direct Access to Simulator. As with 0INT, it allows the simulator to be used outwith the constraints imposed by the functions of the SIM modules menu hierarchy.

6.6. Applications and Results

Process Control

In order to demonstrate how the SIM module can be used in a manufacturing environment the processing of a lot on the Edinburgh Microfabrication Facility (EMF) 1.5 micron nMOS process will be considered. The simulator used in this example is SUPREM-3.

Within COMETS the 1.5 micron nMOS process is broken down into ROUTES and OPERATIONS. These have been designed so as to be intuitively obvious; for example, a spin on resist step is an OPERATION and a set of lithography steps form a ROUTE. This allows both precise production control and detailed data collection. One of the results of this is that a large amount of engineering data can be collected during

manufacture, which is desirable for process analysis although not always practical for high volume production.

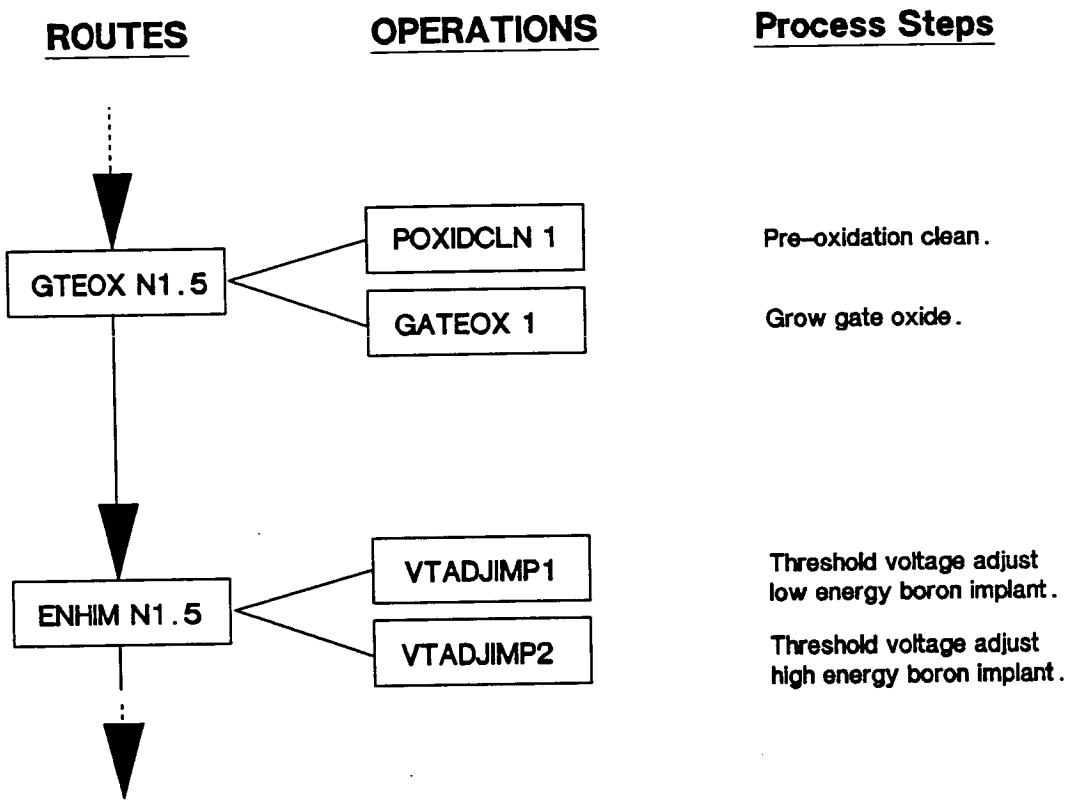


Figure 6.9 Detail of the ROUTES and OPERATIONS used by COMETS to model the EMF 1.5μm nMOS process.

When a LOT is scheduled for production it is created within COMETS for the appropriate PRODUCT. During its process sequence the lot reaches OPERATION 'GATEOX 1' on ROUTE 'GTEOX N1.5' (figure 6.9). The process recipe for this step is shown in figure 6.10. This SPEC file is the SUPREM-3 version of the SPEC shown in figure 6.3. Note that although all the regions of the wafers are exposed to an oxidizing ambient during this operation, it is only necessary to simulate the heat component for the FIELD section. This is because the increase in the thickness of the field oxide during the gate oxidation step has no significant effect on the performance, or structure, of the device.

If the oxide thickness that is actually grown during this step exceeds its preset limits then the lot will be put on hold. The engineer responsible for this part of the process can

```
GATE OXIDE

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen          1.5  l/min.
HCl               0.15 l/min.
Hydrogen        1.7  l/min.
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen  +  HCl
3 min.Oxygen  +  HCl  +  Hydrogen
5 min.Oxygen
Measure: oxide thickness

**  FIELD
diffusion temp=950 time=13 inert
**  DEPLETION
diffusion temp=950 time=5    F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3    F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5    F.O2=1.5
**  ENHANCEMENT
diffusion temp=950 time=5    F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3    F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5    F.O2=1.5
**  SOURCE-DRAIN
diffusion temp=950 time=5    F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3    F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5    F.O2=1.5
```

Figure 6.10 The recipe file of figure 6.3 that has been updated for use with SUPREM-3.

then use the functions of the SIM module to explore the available options.

Figure 6.11 shows the sequence of steps which could be performed using the SIM module to analyse the problem. The first action is to re-simulate the current process step so as to simulate the processing which actually occurred. The re-simulated results for this process step can then be associated with the history of the lot.

The reason for the extra growth of oxide can be investigated by re-simulating the enhancement channel section. Performing this simulation suggests a probable cause of the additional oxide is that the wafers have spent a minute longer than specified in the wet oxidizing ambient of the gate oxide step (figure 6.10). This extra time will not only effect the gate oxide thickness but also oxides in other regions and the distribution of dopants throughout the wafer. The modified doping profile and increased oxide thickness will change the threshold voltages of the devices on the product wafers, the extent of which can

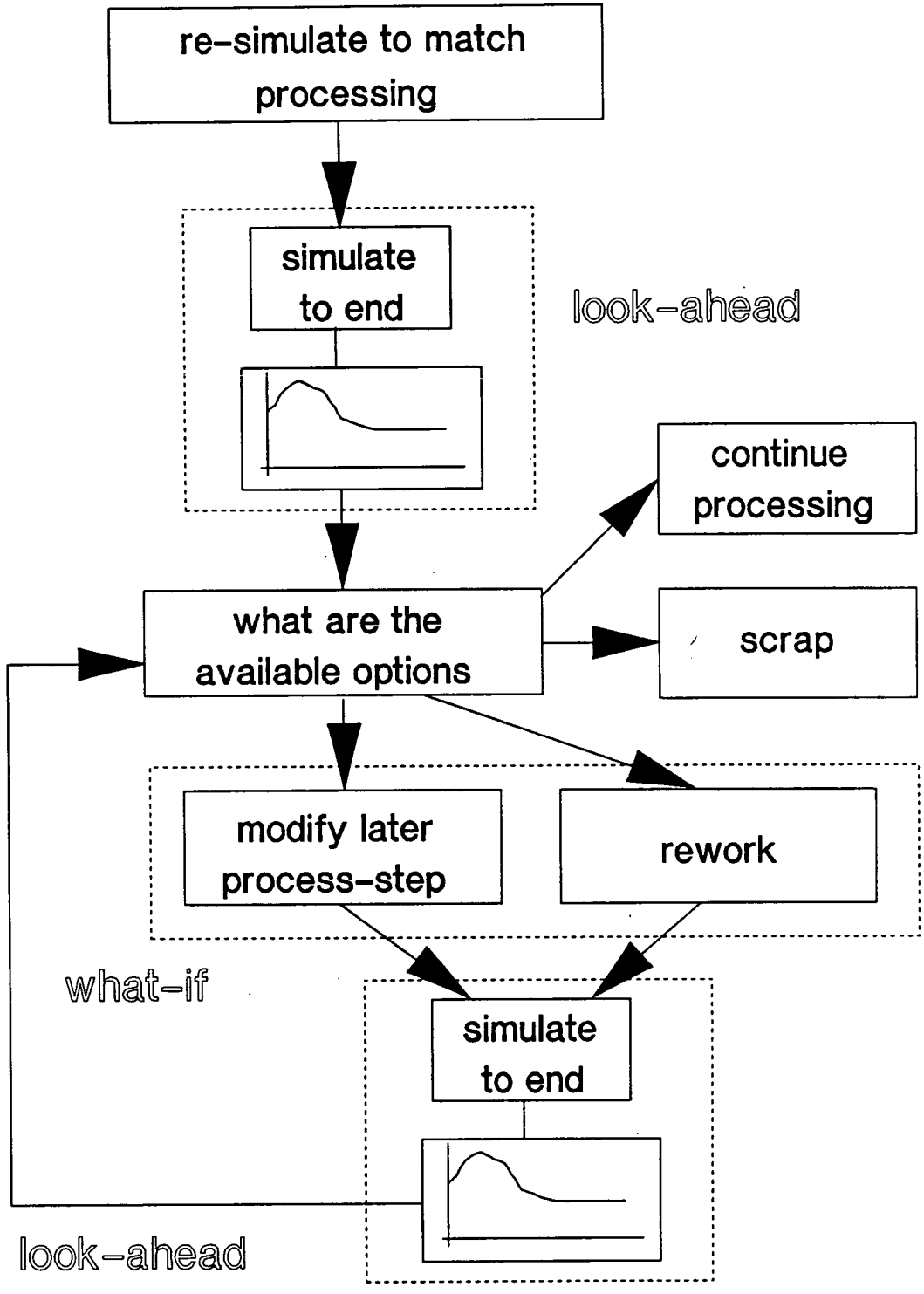


Figure 6.11 Application scenario for the SIM module as a process analysis and control tool.

be checked using the look-ahead function. If the threshold voltages are still within specification then processing could continue as normal. However, if they are out of specification then the processing for the lot might require to be modified, ie. feed-forward control. A series of what-if and look-ahead simulations could be performed to investigate the effect of specific process modifications and estimate how these will influence the final physical and electrical device characteristics. Should corrective processing not be possible then it would be necessary to scrap the lot and re-schedule another start; although this is normally the least desirable option.

Assuming that the threshold voltage of the enhancement devices is out of specification then there are a number of possible options for corrective processing. The SIM module look-ahead and what-if functions can be used to explore the controllable parameters which effect threshold voltage: gate oxide thickness and channel doping [1]. The results of these simulations are shown in table 1. Note that although the simulator cannot take account of all the factors which influence threshold voltage it has been calibrated for this process. Each of the trial process modifications must also be applied to the other 1D nMOS sections to ensure that all physical and electrical parameters remain within specification. The target values of table 1 show the simulated results of an enhancement channel section for normal production, following this are the re-simulated values for the misprocessed lot. The extra minute in the wet gate oxide ambient has resulted in an increase in the gate oxide thickness (T_{ox}) of 44 Å and an increase in the enhancement threshold voltage (V_{Tenh}) of 35%. This could potentially be corrected by reworking the lot, stripping off the oxide and regrowing. However, this will also effect the field oxide thickness, which may be undesirable for some processes. An alternative is to modify the channel doping by reducing the threshold voltage adjust implant. Two boron implants are available at this point (figure 6.9): the first is a low energy implant to adjust the surface dopant concentration, the second is higher energy and is used to reduce punch through, both effect the threshold voltage. By reducing the dose of the low energy implant from 7.0×10^{11} to 5.0×10^{11} atoms cm^{-2} V_{Tenh} can be readjusted to around the target value.

The process modifications that will compensate for the changes of the enhancement transistors have a different effect on the depletion devices. Table 2 shows how the depletion threshold voltage (V_{Tdep}) changes with the various processing options described above. After the gate oxidation step the depletion gate region will have the same oxide thickness as the enhancement gate region, but this will result in an increase in the magnitude of V_{Tdep} by 15%. The modified V_T adjust implant increases its magnitude by a further 5%.

If increasing V_{Tdep} does not violate the process specification then this may be a good solution. However, if V_{Tdep} is out of specification then the depletion implant mask could be reused and another implant introduced to readjust the threshold voltage. Simulating this option suggests a low energy boron implant of 7.1×10^{11} atoms cm^{-2} would readjust V_{Tdep} to around its target value.

The best processing option for this lot will ultimately depend upon the process specification and economic factors, such as the value of the product and the cost of adding an extra masking layer. The SIM module provides a process engineer with the tools to rigorously explore the options before a decision is made. Using the module to compare physical features as well as electrical characteristics an engineer can also examine the potential implications for reliability of any modified processing. Figure 6.12 compares the profiles of the standard and modified processes for the depletion channel section. The solid line indicates the target profile and the dashed line shows the profile after the corrective depletion region boron implants have been applied. Not only have the threshold voltages been readjusted but the doping profiles correlate well. Hence the devices produced by the modified process can be expected to have similar reliability characteristics to devices processed according to the specification.

The application discussed above is relevant to any fabrication facility. However, it is potentially of most benefit in an ASIC environment where a particular product may only be fabricated once. In this case it is important that the lot is fabricated right-first-time. However, if misprocessing should occur then the decision to continue processing or to scrap the lot would have to be made quickly. In this case the SIM module would act as a decision support tool allowing the process engineer to make decisions after having rigorously explored all the options.

The SIM module is a tool that allows engineers to rigorously explore processing options before deciding on what should be done with a particular lot. This is important since scrapping potentially good product and processing non-functional wafers are both expensive alternatives. In custom or application specific production, where a product may only be fabricated once, the time taken to fabricate product wafers which meet specification is also an important factor.

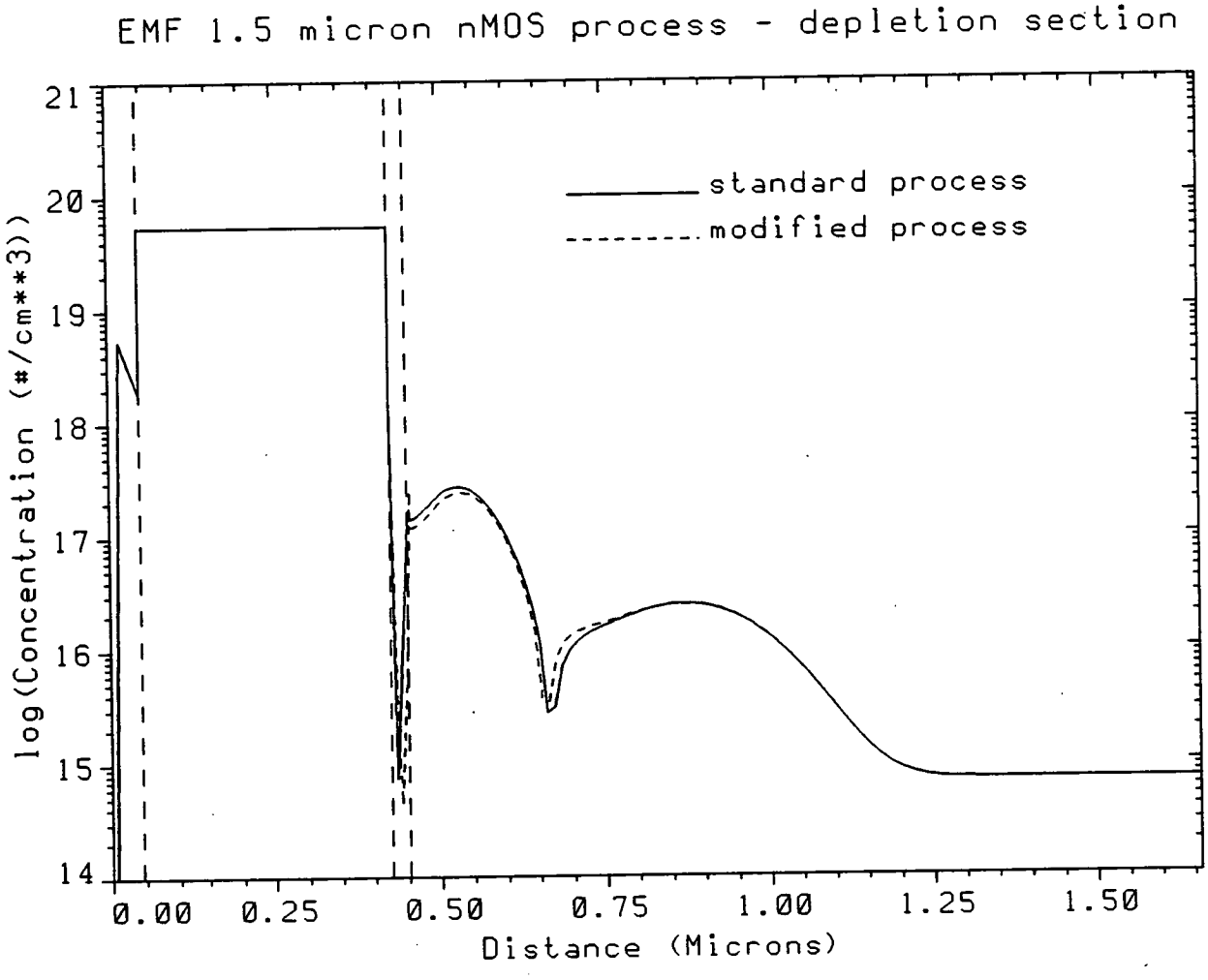


Figure 6.12 Comparison of depletion section net doping profiles for standard and modified processes.

Process transfer

The SIM module can also be used to help in the transfer of processes from the prototype stage to high volume production. The system effectively documents the process and the interactions between the process steps. This information is far more detailed than the standard specifications. Such an approach puts the knowledge base built up during the development phase into the CAM system. As a result the production engineers have easy access to this detailed information, which should help to speed-up the implementation of new processes.

Expert systems

Though the SIM module is a powerful tool for process analysis, it does not contain any knowledge about how to apply the simulation models to develop process modifications. In contrast, an expert can provide a set of rules for corrective processing, but will probably be unable to give exact values for parameter settings. Thus a combination of simulation models and expert heuristics would provide a framework for an active process control system. The SIM module can therefore be considered as the first step towards the implementation of an expert system for process analysis and diagnosis.

6.7. Summary

This chapter has shown how process simulation can be integrated with a CAM system to perform process analysis, diagnosis and feed-forward control. The CAM system COMETS and the one-dimensional process simulator SUPREM-II and SUPREM-3 have been used as vehicles for this demonstration. It should be noted that any other CAM system or simulator could easily be used in their place.

It is believe this is the first time that physical process simulation has been integrated with software that is widely employed in the manufacturing environment. The system has been implemented by extending COMETS with a new module called SIM. This module allows the CAM system to be used as an operating environment for the process simulator. The data for controlling the simulator is stored within the CAM system itself. Functional capabilities of the new system include: generation of simulation histories for lots processed; simulation of the fabrication of individual products; and powerful *look-ahead* and *what-if* functions. The module can also be used to investigate whether changes to the process are likely to alter the anticipated reliability of the product devices. The proposed approach is particularly applicable to flexible manufacture and to speeding-up the transfer of processes

from development to production facilities. A potential also exist for the addition of heuristics to help direct the development of solutions using the capabilities of the SIM module.

It is interesting to note that the software commitment for the SIM module is approximately three times greater than that for the existing COMETS statistical quality control (SQC) module. If developed as a commercial product the SIM module would probably only require a limited amount of further investment in software development.

References

1. S.M. Sze, *Physics of Semiconductor Devices*, John Wiley & Sons, New York, USA, 1981.

Chapter 7

Recipe Management for CAM

7.1. Introduction

The fabrication of integrated circuits is a dynamic and often non-linear process. Consequently a large amount of information is required to define the production sequence. A similarly large amount of data can be collected to characterise the process and the products being fabricated.

Through the application of CAM the collected engineering data can be analysed, possibly reduced, and stored. It can then be related to the production sequence and the equipment used, to analyse production on a lot, product, process or environment basis. However, the specification data that describes equipment control and the target values for processing parameters tends to be distributed around a facility and are stored in either a form which is not machine readable or one that is dedicated to a particular piece of processing equipment. That is, the information is stored implicitly, as in a text or SECS control file, rather that explicitly, as in a structured database.

Dependence on distributed, and implicit, process specifications has a number of consequences for an IC fabrication facility. Once there are more than a few products or processes, maintenance of the data becomes difficult. This can result in the integrity, and therefore quality, of the data being degraded. The distribution of data around the facility can also make security unmanageable. For semiconductor manufacturing it is not practical to have a single process dedicated to a single set of equipment running a single set of recipes. Therefore unless the process recipes and their relation to the lots being fabricated are accessible, then full process analysis is not possible. This problem is exacerbated where many products/processes are present, such as in a flexible manufacturing environment. In particular, the analysis of data on a lot basis, leading to corrective processing[†], is not possible unless the data is re-expressed in a format that can be used by a simulator.

[†] As described in Chapter 6.

Having a single, complete definition of a process could be used to overcome these problems. It could also play an important role in analysing and controlling processing. This could then lead to simplifying the transfer of processes from development to production.

In this chapter a method for describing IC processing is presented. A system has been developed which will allow an explicit representation of process recipes to be integrated with production specifications and engineering data; thus helping support analysis of lots, products and processes. It is shown that this system may be used to enhance the application of process simulation for process analysis in a manufacturing environment. The flexibility of this system also allows the on-line control of production with the use of overrides to implement feed-forward control. Finally, some further applications for recipe management are considered.

7.2. Specifying a Recipe Management System

In response to the need for recipe management within CAM a new module has been developed to integrate with COMETS. The Recipe Management, RCP, module is designed to support the SIM module and work within the context of the other data management facilities of COMETS. The RCP module was developed with constraints that were similar to those for the SIM module. As the data is to be stored explicitly it is preferable to use the same type of database as is used by COMETS, and as the COBOL programming language may only *bind* to one database at a time it is necessary to modify the existing COMETS database by adding the appropriate data structures. Despite this modification, it is possible to avoid any change to the existing COMETS source code.

COMETS currently supports a specification system known as the SPC module†. This module uses a combination of database structures and text files to maintain processing instructions. A specification (SPEC) is held in the database and can be associated with a process step or, for example, the arrival of a lot at a piece of equipment. These are known as ROUTE-OPERATIONS and EVENTS for an ENTITY, respectively. A data model of these relationships is shown in figure 7.1. SPECS are implemented within the database as control records each of which can have multiple versions. These versions are associated with files held in a special VMS directory. Figure 7.2 shows a Bachman diagram of the relationships between the database records used by the SPC module.

† See Chapter 3 for a full description.

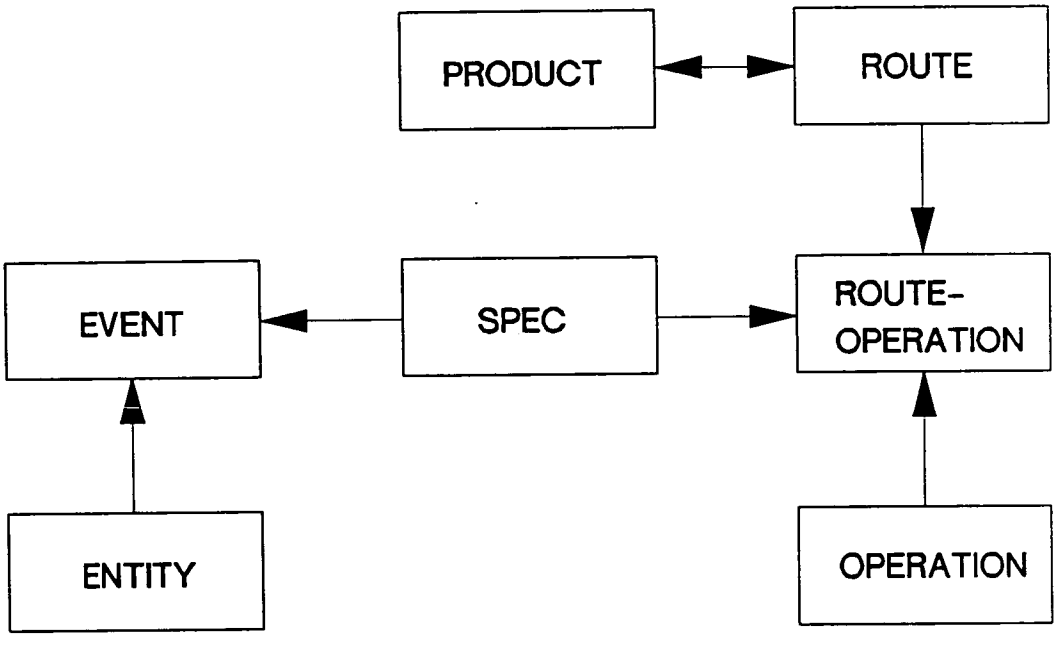


Figure 7.1 Simple data model of the relationship between SPECS and some of the elements of the WIP and NTC modules.

As it is a SPEC version that is associated with the ROUTE-OPERATION and EVENT records a history of the development of a SPEC is maintained. Security for this information is controlled by FREEZING a SPEC version so that it cannot be modified. Overrides, however, must be established before the SPEC version is FROZEN.

Developing a description of a process recipe is complicated by the range of data that might be used to define a process step. Each type of step requires a different set of specification parameters. Some typical examples are shown below:

Oxidation	temperature	°C
	time	min
	Oxygen flow rate	l min^{-1}
	Hydrogen flow rate	l min^{-1}
	HCl flow rate	l min^{-1}
	Nitrogen flow rate	l min^{-1}
	temp. ramp rate	°C min^{-1}

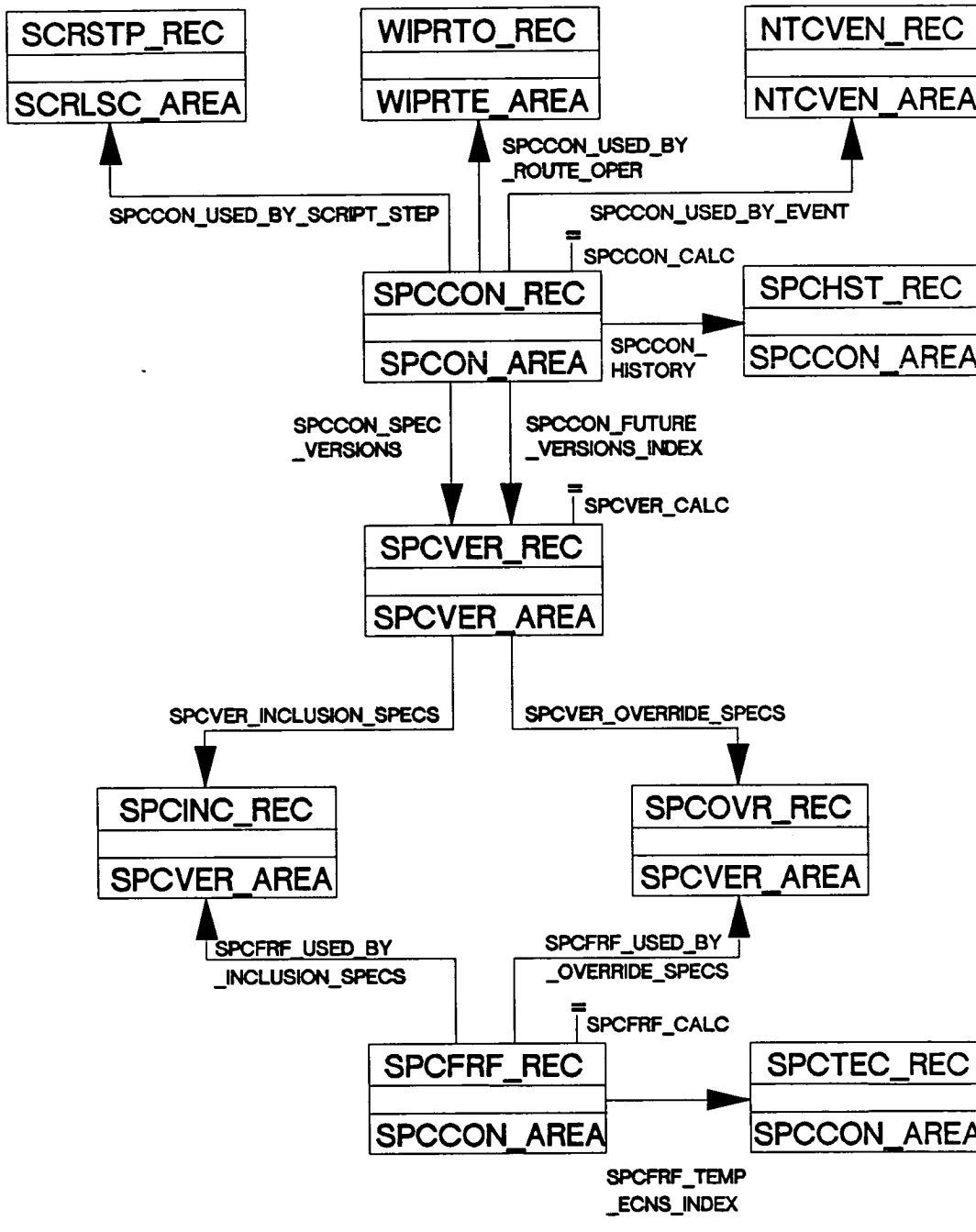


Figure 7.2 Bachman diagram of the records and sets used by the COMETS SPC module.

Implantation	dopant	
	dose	atoms cm^{-2}
	energy	KeV
Exposure	mask/reticle	
	time	seconds

This information is extracted from the nMOS runsheet of appendix A. While this data is applicable to the Edinburgh Microfabrication Facility, it is not necessarily compatible with the data required to describe other environments. For example, another facility may require that the angle of the implant, or that mask numbers and stepper control programs be maintained as part of a recipe. Thus it is not clear that a generic process recipe can be created for each type of process step. More than one recipe can also belong to a process step; thus it is possible to describe the ramp-up, dwell and ramp-down phases of an oxidation, or the use of a number of reticles to pattern a wafer.

In addition to control data, recipes may also be required to maintain data that defines the target values to be reached, such as oxidation thickness or sheet resistivity. If process simulation control files are to be generated from the recipes then it will also be necessary to store parameters that are peculiar to the simulator. Further information may also be required to simply document the recipe.

This discussion of process recipe data has described the information required to define a process, but not the processing equipment. Therefore recipes should be able to store data such as the set-up sequence for the processing equipment, the operating limits for control parameters, and the number of hours between maintenance sessions.

The RCP module must add to the functionality of COMETS. To control the process it must integrate with the Work-in-progress tracking (WIP) and SCRIPT (SCR) modules. To attain the same level of control over the environment and the processing equipment it is also necessary that it integrate with the Non-lot Tracking (NTC) module. The data stored by the RCP module should also be accessible to the SIM module so that the same data used to control processing may be used to drive the simulator for process analysis.

When a lot is at a process step the operator should still be able to view a specification in the normal way. With the exception that the data displayed will be generated from three separate sources. The first is the data associated with EVENTS for an ENTITY, and so may contain equipment set-up data. The second is the process control, and possi-

bly target, parameters that are associated with the ROUTE-OPERATION. The third format is the unstructured text files as currently managed by the SPC module.

The RCP module is, however, not merely a system for improving the storage of the data already handled by the SPC module. Instead it is designed to act as a tool for performing on-line control of a process. Therefore it must be possible to create overrides for recipes that will be used during production when certain override criterion are met. The override capability is intended for the explicit storage of data for use with the WIP and NTC modules rather than the SPEC files.

It is also important that the RCP module should provide a screen interface that will allow the creation, modification and viewing of recipes on-line. This will also apply to override recipes. As reporting is a major component of COMETS it is important that this capability is included in the RCP module. All these functions can be implemented by adding them to the existing COMETS menu structure.

7.3. Recipe Data Structures

When the first proposal for the development of the RCP module was made [1] it was anticipated that this module should completely replace SPC while maintaining its best features. Thus the concept of the SPEC was replaced by the RECIPE, with each RECIPE supporting multiple versions. Whereas the SPEC versions of the SPC module simply maintains a set of files, the RECIPE versions would support the same files but also INGREDIENTS, ACTIONS and OVERRIDES. An INGREDIENT could be, for example, a control parameter for a furnace, such as time or temperature. As a RECIPE might require multiple sets of processing parameters, ACTIONS were proposed as a method of grouping together INGREDIENTS so that complex RECIPES could be created. The concept of the an OVERRIDE was included so that a RECIPE version could be modified on-line, thus avoiding the overhead of SCANNING and FREEZING that were associated with the SPC module. Figure 7.3 show the data model initially proposed for the RCP module.

However, it became apparent that developing the RCP module in this way would require much of the COMETS code, for linking the SPECS to the other WIP and NTC database records, to be re-written. This led to a redesign of the data model that would allow the SPC module to remain in use while integrating recipe management into COMETS.

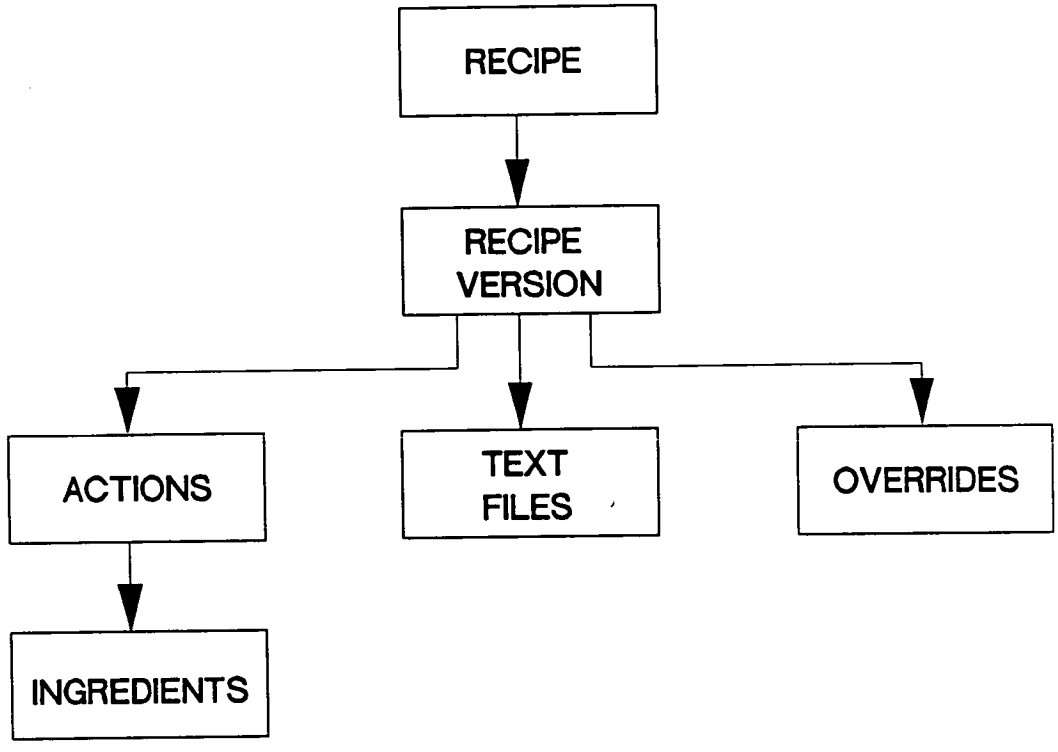


Figure 7.3 Initial data model for the RCP module.

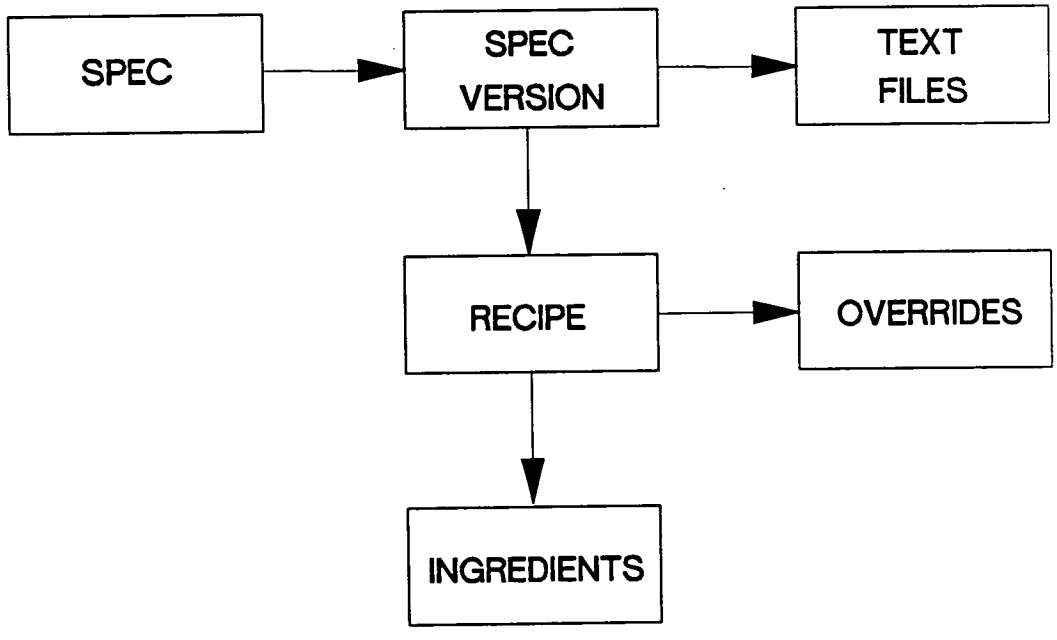


Figure 7.4 Modified data model for the RCP module.

The result has been the addition of new records and sets to the SPC area of the database. These new records do not interfere with the functions of the SPC module yet adopt some useful aspects of the existing data structures. The concept of a RECIPE has been added directly to that of the SPEC in the database. If INGREDIENTS are then added to the RECIPE and OVERRIDES are specified as applying directly to the RECIPES then the RECIPE concept replaces that of an ACTION. Figure 7.4 shows a simple data model for this modified relationship.

The importance of these modifications is more readily appreciated by considering the Bachman diagram of figure 7.5. The RCP records are associated with the SPEC VERSION (SPCVER) records and so adopt the same version control mechanism. This mechanism maintains a current version and a set of historical versions. To each of these can be attached a set of RECIPES. As each RECIPE (SPCRCP) record can belong to many SPEC VERSIONS and vice versa, i.e.. a many-to-many relationship, an intermediate record (SPCVRC) is used to allow the use of one-to-many relationships. This is necessary as VAX DBMS does not support many-to-many relationships.

The SPCRCP and SPCVRC records contain the following data:

SPCRCP
- facility name
- recipe name
- recipe type
- recipe description
- number of ingredients
- creation date and time
- by whom created
- last modified date and time
- by whom modified
- terminated date and time
- by whom terminated

SPCVRC
- specification identifier
- specification version
- recipe name

When searching for the RECIPES that belong to a SPEC, the system takes the current SPCVER belonging to SPCCON and look through the list of SPCVRC records each of

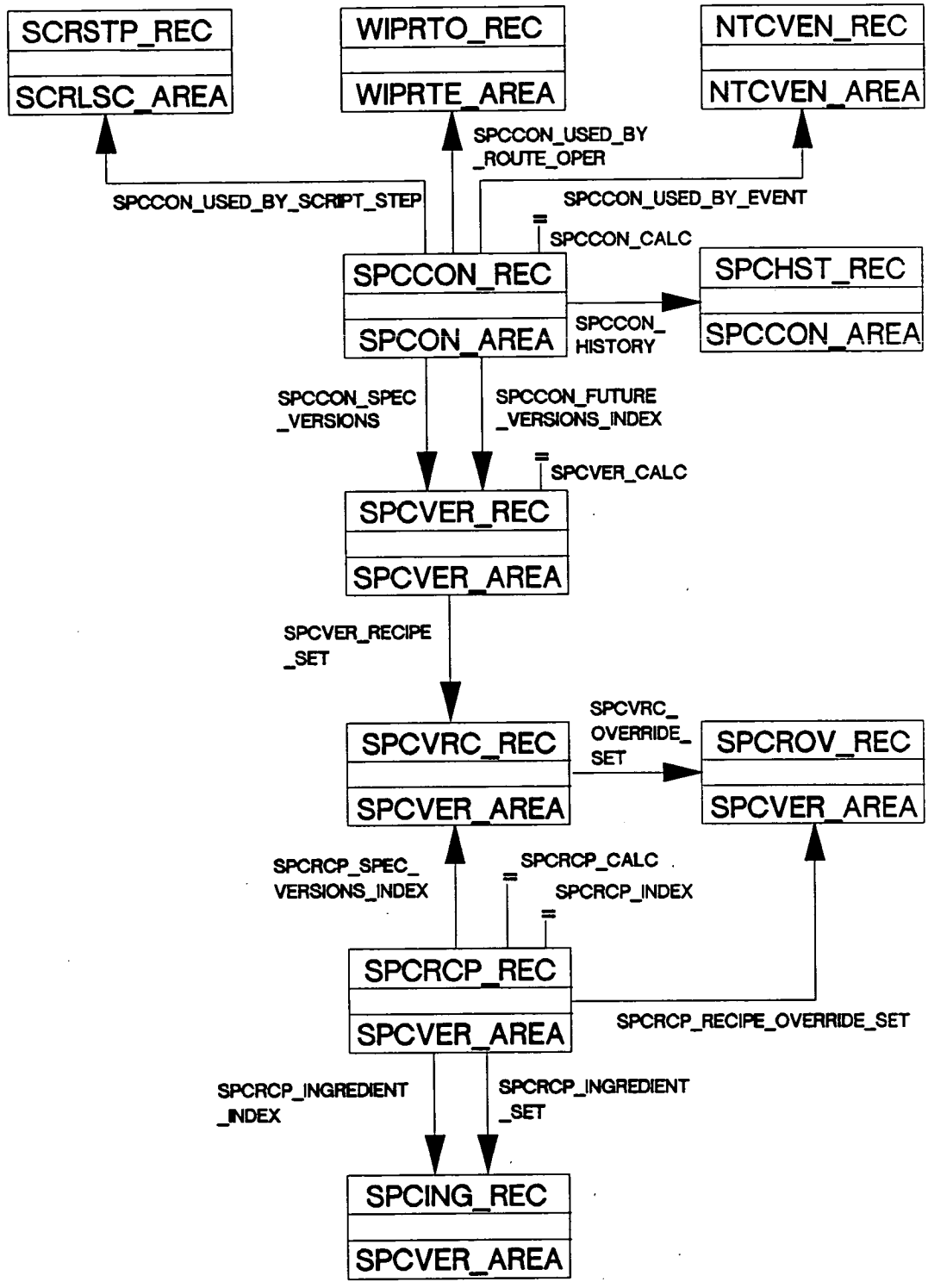


Figure 7.5 Bachman diagram of the records and sets used by the new RCP module.

which contains a unique recipe name. It is then simple to fetch the appropriate SPCRCP record and its associated INGREDIENT (SPCING) records. The SPCING records hold the following data:

SPCING	parameter
	value
	unit
	flag

The parameter is the name of the INGREDIENT, which might be a control parameter or a keyword intended to be interpreted by the SIM module. The flag is used to indicate the type of INGREDIENT, from a list of control, target, comment and simulation.

The OVERRIDE (SPCROV) records are accessed through SPCVRC as they may only be created for a SPEC used at a ROUTE-OPERATION or an EVENT. The following data is held within the SPCROV record:

SPCROV	recipe name	override recipe name
	specification identifier	specification version
	creation date and time	by whom created
	termination date and time	by whom terminated
	override by lot number	override by product name
	override by product group	override by lot owner
	override by lot create code	override over time period
	override for an ENTITY name	override for an EVENT

This information allows a unique RECIPE to be used for overriding an existing RECIPE, or adding to the number of RECIPES of a SPEC. Blank, or null, OVERRIDE RECIPES can be used to simply stop a particular RECIPE being used. This record also stores the criterion for which the OVERRIDE applies. Thus OVERRIDES can be applied on: a lot basis using the lot number, owner or create code; a product basis by specifying the product name or group code; a process basis using time specifiers or perhaps the owner or create codes; and an environment basis by specifying an ENTITY or EVENT. Many OVERRIDES can of course apply to one RECIPE, this is handled by assuming that if conflicts do occur then the last non-terminated OVERRIDE has greater priority.

All the RCP records have been defined as being added to SPCVER_AREA. To

maintain the performance of the SPEC and RCP modules it is important that the sizing of this area be carefully monitored.

The COMETS database is defined using the VAX/VMS Data Definition Language (DDL). Modifying the database to the extent described above can only be achieved by adding the extra record and set definitions to the Database Schema, the Storage Schema, the On-line Sub-Schema, and the Report Sub-Schema. For the currently implemented version of COMETS these schemas are stored in files called MANYSCHEM.DDL, MANYSTOR.DDL, MANYSUB.DDL, and MANRPTSUB.DDL. The additional DDL statements added to these files to extend the COMETS database with the structure shown in figure 7.5 are listed in Appendix D. Upgrading an existing database to include these structures requires the following procedure, assuming the presence of only a single database,:

1. Verify that the Schema, Storage Schema, and Security Schema defined in the database Header match the equivalent information in the Common Data Dictionary (CDD). If they do not then delete the CDD node and integrate the database into the CDD.
2. Modify the DDL files by including the modifications.
3. Convert the database definition in the CDD.
4. Modify the database to match the changes made to the CDD.

This sequence will result in a modified database. However, unless COMETS is modified to recognise these changes then it will be unable to find any of the data in the database.

Most COMETS source code files include a reference to a file containing a definition of the structure of the database. To update this file (CMTSCH), it must be extracted from the COMETS copylibrary, edited to reflect the database changes, and replaced in the library. Each of the COMETS source programs that depend on this data definition must then be compiled, and the object code inserted in the appropriate object library. The executable programs can then be linked. The modifications that must be added to CMTSCH are also listed in appendix D.

It is possible to implement this system upgrade in a period of as little as two days.

7.4. On-line RCP

As with the SIM module, the RCP module has an on-line component that operates as lots are processed. The RCP module differs, however, in that it is associated with the functions of the WIP, NTC, and SCRIPT modules only through the SPC module.

When a SPEC file is created the qualifier /USER2 must be included where the RECIPES for this ROUTE-OPERATION are to be displayed. The file name following this delimiter must be the same as that of the file itself but with the suffix '.RCP'. The file itself is not created by the user but by the RCP module when the SPEC is displayed. Using this approach means that the SPEC displayed to the operator always reflects the current state of the RECIPE information in the database.

The qualifier /USER2 was included by Consilium to display user graphics files by calling the *user-exit* routine USR049. Now that it is used by the RCP module to format RECIPES for visual display it can no longer be used for its original purpose. However, the qualifier /USER1 is still available and performs much the same function.

7.5. The RCP Menu Structures

The RCP module supports a hierarchy of menu screens that match in appearance those of other COMETS modules. These menus allow the creation and modification of recipes, their association with SPECS and through these the process steps and processing equipment, the application of overrides, and various inquiry and reporting facilities. As with the menus of the SIM module, these menus are accessed through the user main menu via the *user-exits* USR001 and USR002. The RCP functions also use similar four letter mnemonics, however, these differ in that they are all character codes which have been chosen for user convenience rather than with a view to future versions of COMETS.

Recipe management menu (RCPM)

This menu (figure 7.6) shows the functional menus within the RCP module. These functional categories are similar to those used by the SPC module.

Recipe maintenance menu (RCMM)

The functions made available through the recipe maintenance menu (figure 7.7) are designed to allow the creation, updating and viewing of a recipe.

To create a recipe, the recipe name and type have to be specified. The recipe name must be unique for the current facility, and the recipe type must have been previously

```
RCP000S                    RECIPE MAIN MENU (RCPM)          SYS  3/11/89 12:14:58
EDINBURGH UNIV.                    EMF

                                FUNCTION...____

                    RECIPE MAINTENANCE MENU.............(RCMM)
                    RECIPE-SPEC ASSOCIATION MENU........(RSAM)
                    RECIPE OVERRIDE MENU................(RCOM)
                    RECIPE INQUIRY MENU.................(RCIM)
                    RECIPE REPORT MENU..................(RCPM)




RETURN = PROCESS
SFK1   = EXIT
```

Figure 7.6 Main menu for the RCP module.

```
RCP100S                RECIPE MAINTENANCE MENU (RCMM)       SYS  3/11/89 12:15:12
EDINBURGH UNIV.                    EMF

                              FUNCTION.......____
                              RECIPE NAME....__________
                              RECIPE TYPE....__________

                    CREATE OR APPEND A RECIPE.............(CRCP)
                    UPDATE A RECIPE.......................(URCP)
                    VIEW A RECIPE.........................(VRCP)
                    VIEW ALL RECIPE NAMES AND TYPES.......(VRCS)
                    LIST ALL RECIPE NAMES AND TYPES.......(LRCS)




RETURN = PROCESS                SFK2 = HELP
SFK1   = EXIT
```

Figure 7.7 Recipe maintenance menu.

defined in the GTS table COM$RCPTYPES. The screen shown in figure 7.8 is where further recipe data can be entered and the list of ingredients is specified. Duplication of ingredients within a recipe is also not allowed. The flag field may be filled with the following letters:

C	control parameter	S	simulation parameter
T	target parameter	*	comment

It is possible to have a special recipe type that is used for the simulation control parameters that may be necessary when the simulator is calibrated to the process, or the processing equipment. Using the delete facility will not actually delete the recipe but only mark it as terminated.

Recipe updating allows the user to modify, delete, add or insert ingredients. The recipe name must be supplied but the recipe type is optional. Figure 7.9 shows the updating screen for a recipe.

Viewing a single recipe shows the same information as the updating screen, but without the editing capability. Viewing all the recipes, however, displays only the recipe name, type and description as shown in figure 7.10. To view all the recipes for the current facility simply call the function, if a recipe name is specified then only that recipe will be shown. Specifying a recipe type without a name will display all the recipes of that type.

Recipe-spec association menu (RSAM)

Once a recipe has been created it can be associated with a SPEC. The association screen (figure 7.11) is accessed by entering the update recipes of a SPEC version mnemonic with a SPEC id. and a version number. Figure 7.12 shows the update association screen. Valid recipe names must be added or inserted to the list, it is also possible to view an existing list of recipes associated with a SPEC version. The equivalent view function to this update displays the same information but will not allow the information to be modified.

Recipe override menu (RCOM)

This menu (figure 7.13) gives access to the override recipe function. To call this function it is necessary to specify the SPEC id. and version, the recipe to be overridden and the override recipe. Normally both the recipe name and the override name will be existing recipes. However, it is possible to use special reserved recipe names in these

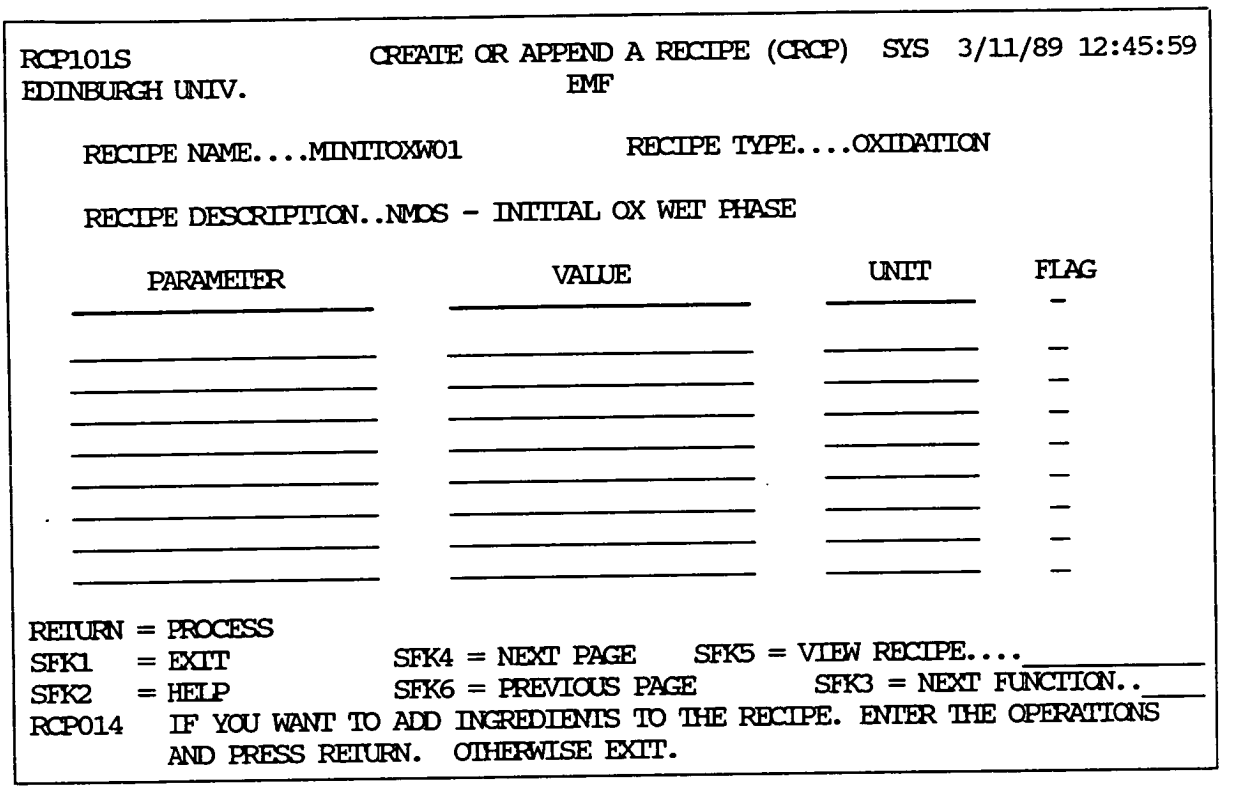


Figure 7.8 Screen for adding ingredients to a new of existing recipe.

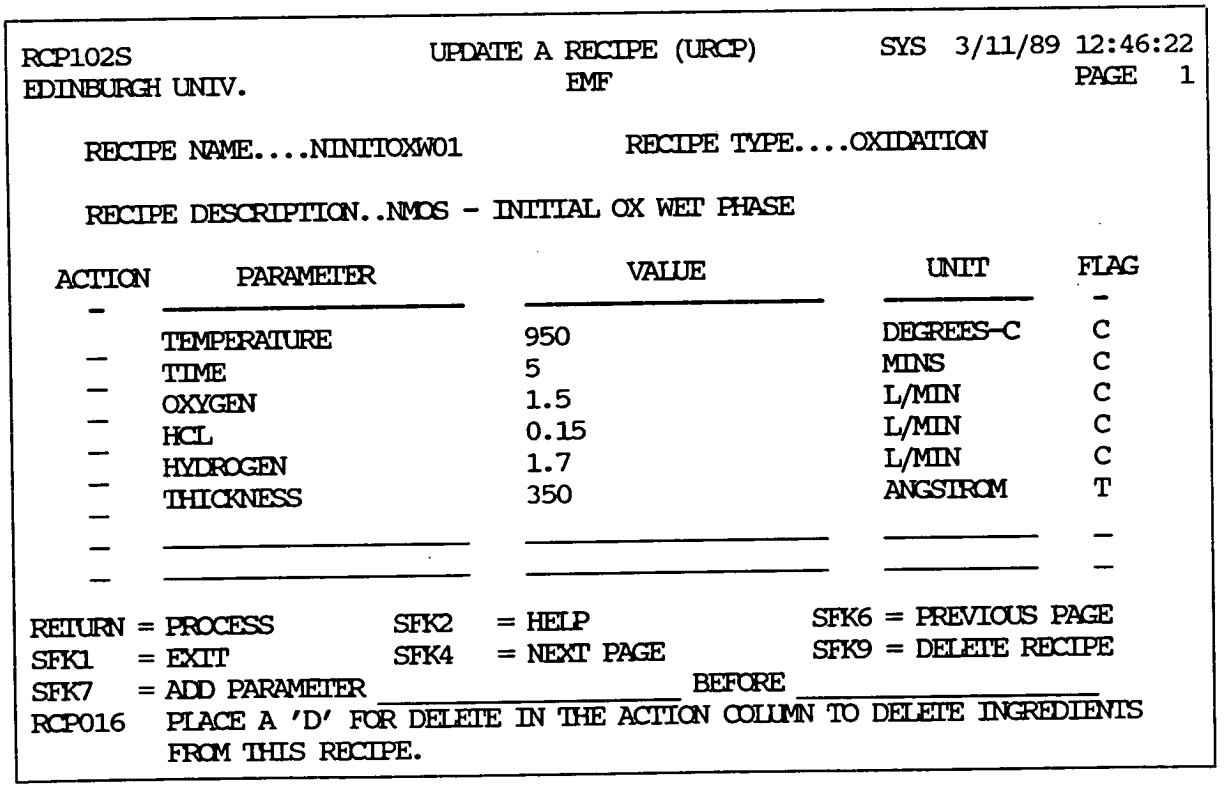


Figure 7.9 Screen for modifying or deleting ingredient from a recipe.

```
RCP105S                          VIEW ALL RECIPES (VRCS)        SYS  3/11/89 12:46:56
EDINBURGH UNIV.                          EMF                                PAGE   1

  RECIPE NAME      RECIPE TYPE                    DESCRIPTION
  ------------     ------------     ------------------------------------
  NPDEP01          DEPOSITION       NMOS - SOLID SOURCE PHOSPHORUS DEP
  NSI3N4DEP01      DEPOSITION       NMOS - DEPOSIT SILICON NITRIDE
  NBIMP01          IMPLANT          NMOS - BORON IMPLANT VT ADJUST 1
  NBIMP02          IMPLANT          NMOS - BORON IMPLANT VT ADJUST 2
  NBIMP03          IMPLANT          NMOS - CHANNEL STOP BORON IMPLANT
  NINITOXD01       OXIDATION        NMOS - INITIAL OX FIRST DRY PHASE
  NINITOXD02       OXIDATION        NMOS - INITIAL OX SCND DRY PHASE
  NINITOXW01       OXIDATION        NMOS - INITIAL OX WET PHASE



SFK1 = EXIT          SFK4 = NEXT PAGE          SFK3 = NEXT FUNCTION..____
SFK2 = HELP          SFK6 = PREVIOUS PAGE
```

Figure 7. 10 An example of the screen format used to view a range of recipes.

```
RCP200S                  RECIPE-SPEC ASSOCIATION MENU (RSAM)    SYS  3/11/89 13:44:37
EDINBURGH UNIV.                          EMF



                              FUNCTION.......____
                              SPEC ID........______________
                              SPEC VERSION..._____


                        UPDATE RECIPES OF A SPEC VERSION.....(URSV)
                        VIEW RECIPES OF A SPEC VERSION.......(VRSV)









RETURN = PROCESS                  SFK2 = HELP
SFK1   = EXIT
```

Figure 7.11 Screen used to attach a recipe to an active SPEC version.

```
RCP201S          UPDATE RECIPES OF A SPEC VERSION (URSV)  SYS  3/11/89 13:45:20
EDINBURGH UNIV.                      EMF                              PAGE   1

    SPEC ID.....NINITOX                  SPEC VERSION...1

                              RECIPE
                              ________

                              ________
                              ________
                              ________
                              ________
                              ________
                              ________
                              ________
                              ________

RETURN = PROCESS        SFK2   = HELP              SFK6 = PREVIOUS PAGE
SFK1   = EXIT           SFK4   = NEXT PAGE          SFK9 = REMOVE ASSOC.
SFK7   = ADD RECIPE _________ BEFORE _________
RCP020   IF YOU WANT TO ADD RECIPES TO THIS SPEC VERSION. ENTER THE RECIPE
         NAMES AND PRESS RETURN.  OTHERWISE EXIT.
```

Figure 7.12 Screen used to modify recipes associated with a SPEC version.

```
RCP300S                  RECIPE OVERRIDE MENU (RCOM)      SYS  3/11/89 13:51:42
EDINBURGH UNIV.                  EMF

                         FUNCTION.....____
                         SPEC ID.....________________
                         SPEC VERSION..._____
                         RECIPE NAME....__________
                         OVERRIDE NAME..__________

                    OVERRIDE EXISTING RECIPE.....(OERC)

RETURN = PROCESS            SFK2 = HELP
SFK1   = EXIT
```

Figure 7.13 Screen used to override a specific recipe.

fields. Instead of a recipe name the words FIRST or LAST may be used. These allow override recipes to be applied before or after the standard recipes. Alternately the override name NULL may be used to effectively remove a particular recipe from the list of recipes associated with a SPEC version.

Figure 7.14 shows the screen used to indicate the criterion by which the override should be applied. Note that only one criterion may be used per override.

Recipe inquiry menu (RCIM)

The inquiry menu (figure 7.15) gives access to a very powerful function for viewing how recipes are being applied. This function provides the user with a view of the recipes and overrides that are associated with all currently active SPEC versions.

Though not implemented, it would be possible to add a number of other functions to this menu screen. For example:

VROA	View all ROUTE-OPER associations.
VREA	View all EVENT associations.
VRSA	View all SCRIPT associations.

These would offer a useful overview of where recipes are being used.

Recipe report menu (RCRM)

The functions of the reporting menu (figure 7.16) produce printed reports of the recipes maintained by the module. The first function produces a listing of the recipes and overrides associated with all currently active SPEC versions. The second simply lists all the recipes available within the current facility.

7.6. Performing Process Simulation using Process Recipes

The data maintained by the RCP module can be used to support the functionality of the SIM module. Rather than abstracting simulation control statements from SPEC files the explicit control, target and simulation INGREDIENTS stored in a RECIPE can be used to generate these statements.

In order to achieve this, additional constraints must be applied to the data stored in a RECIPE. These constraints cover the TYPES of RECIPE which are used and the PARAMETER names of the INGREDIENTS. If a RECIPE is to be used by the SIM module then it must be of one of the following RECIPE TYPES:

```
RCP301S              OVERRIDE AN EXISTING RECIPE (OERC)     SYS  3/11/89 14:07:16
EDINBURGH UNIV.                        EMF                                PAGE   1

    SPEC ID.........NINITOX                  SPEC VERSION...1
    RECIPE NAME....NINITOXW01                OVERRIDE NAME..OVNIOXW01

    REICPE IS OVERRIDEN FOR THE FOLLOWING CONDITION :

      _ LOT NUMBER .......__________
      _ PRODUCT...........______________________________
      _ PRODUCT GROUP.....__________
      _ OWNER.............__________
      _ CREATE CODE......._____
      _ PERIOD FROM.......__/__/__ TO __/__/__.
      _ EVENT.............__________
      _ ENTITY............__________


RETURN = PROCESS          SFK2   = HELP
SFK1   = EXIT             SFK9   = TERMINATE OVERRIDE
RCP025   MARK CHOICE WITH AN 'X' AND ADD APPROPRIATE CONDITION.
         WHEN DONE PRESS RETURN.   OTHERWISE EXIT.
```

Figure 7.14 Screen used to specify reicpe override criterion.

```
RCP400S                  RECIPE INQUIRY MENU (RCIM)          SYS  3/11/89 14:36:24
EDINBURGH UNIV.                        EMF


                          FUNCTION.......____
                          RECIPE NAME....__________


                   VIEW ALL SPEC ASSOCIATIONS.............(VRSA)









RETURN = PROCESS              SFK2 = HELP
SFK1   = EXIT
```

Figure 7.15 Screen used to perform on-line inquiries about recipes.

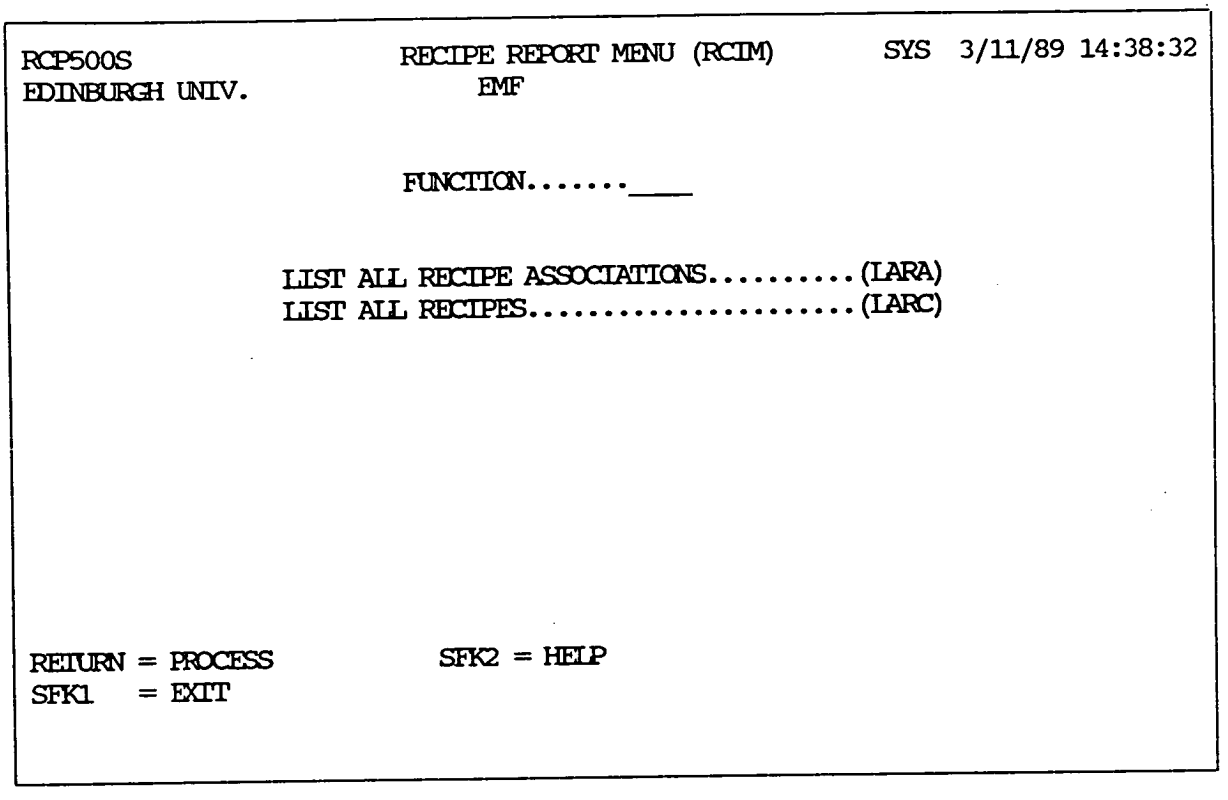


Figure 7.16 The report generation menu.

OXIDATION	ANNEAL
DRIVE-IN	DIFFUSION
DEPOSITION	ETCH
IMPLANTATION	EPITAXY
CLEAN	EXPOSURE
MEASUREMENT	SIMULATION

Some of these are synonymous; they are maintained purely for user convenience.

In most cases the control INGREDIENTS of a RECIPE will be sufficient to generate a complete simulation control statement. For example, TEMPERATURE, TIME and a set of gas flow INGREDIENTS can be used in a OXIDATION TYPE RECIPE to form a syntactically correct SUPREM-3 diffusion statement. In some cases the control INGREDIENTS may require to be supplemented by target INGREDIENTS, an example of which is the deposition of polysilicon when no deposition rate is available. However, it may occasionally be necessary to include parameters that are only meaningful to the simulator, as in the case of a phosphorus deposition when the dopant comes from a solid source

heated in the furnace along with the product wafers.

Storing simulation control statements in a SPEC file allows separate sets of statements to be stored for each 1-D section to be simulated. Specifying which recipes should be performed for each section is achieved by listing the SECTION names in a proceeding EXPOSURE RECIPE. The SECTION name is entered as a simulation PARAMETER, with a keyword in the VALUE field to indicate how the following steps should be interpreted. This may be FULL to indicate a complete translation, HEAT to indicate that only the high temperature components of steps should be simulated, and NONE if the following steps should be ignored for this section.

Figure 7.17 shows a VRCP screen for an OXIDATION RECIPE, while figure 7.18 shows the equivalent SUPREM-3 statement. These diagrams indicate how a simple RECIPE, for part of a gate oxidation, is translated directly into a simulation control statement. In the runsheet of appendix A, however, the gate oxidation is more complex than this example. The oxidation actually consists of a three oxidations in different ambients: dry + HCl, followed by wet + HCl, followed by dry. Assuming the simulator had been calibrated to the equipment on which this process runs then the oxide growth parameters for the furnace should also be stored within the recipe system. Figure 7.19 indicates how the simulation control file for a process step would be formed.

7.7. Further Applications for Process Recipes

The RCP module has been developed to act as a general repository for process data. Consequently it can be used for other applications than generating the input to a process simulator.

Automated control

Perhaps the most obvious application would be to use the recipe data within the RCP module to provide direct control of automated processing equipment. This might take one of two forms. If equipment specific data were stored as part of a recipe then it would be possible to use this information to generate the equipment control files in a SECS format and download them to the equipment using the PAM module. Alternatively the recipes might be used to store more generic/logical recipes that could be passed to cell/equipment controllers that would apply equipment specific details to the recipes and thereby form the equipment control files. This topic is worthy of further investigation but is beyond the scope of this PhD.

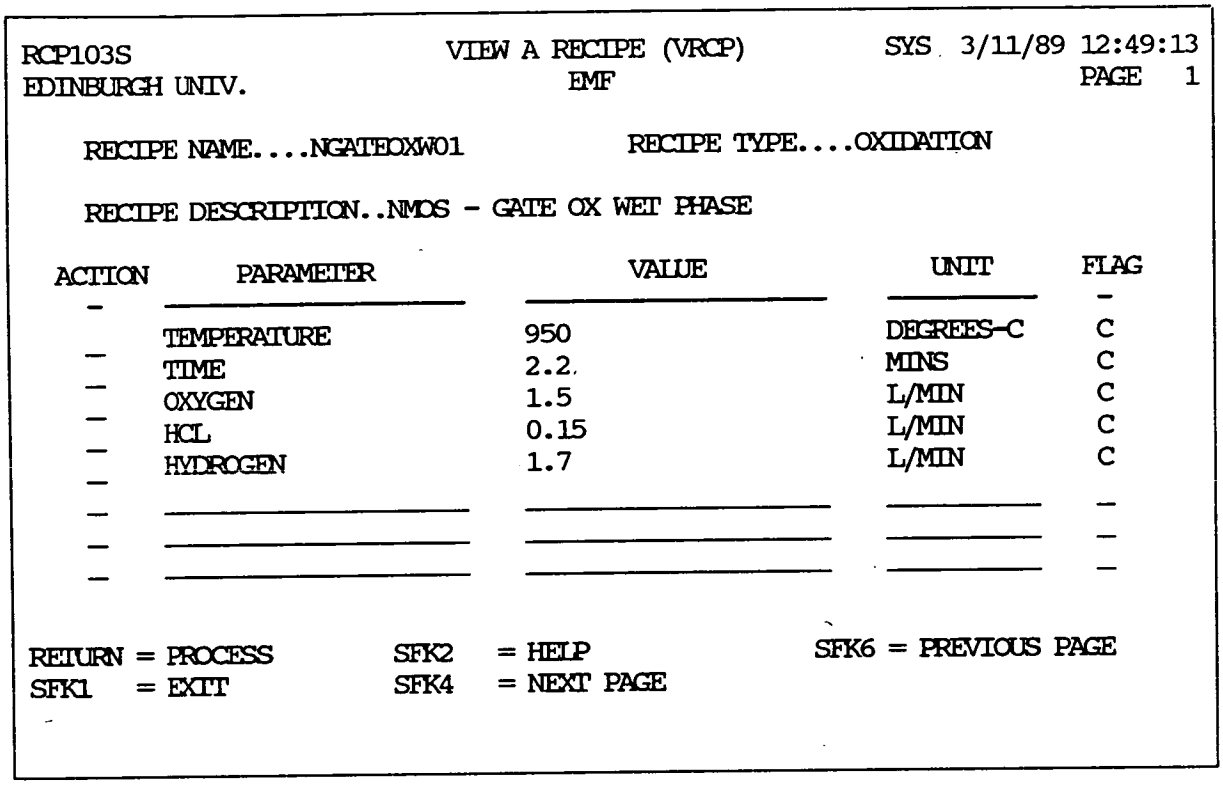


Figure 7.17 Ingredients for the wet phase of an nMOS gate oxidation.

```
$ NGATEOXW01 OXIDATION
diffusion temp=950 time=2.2 F.O2=1.5 F.HCl=0.15 F.H2=1.7
```

Figure 7.18 Simple SUPREM-3 equivalent of the recipe shown in figure 7.17, as formed by the RCP module.

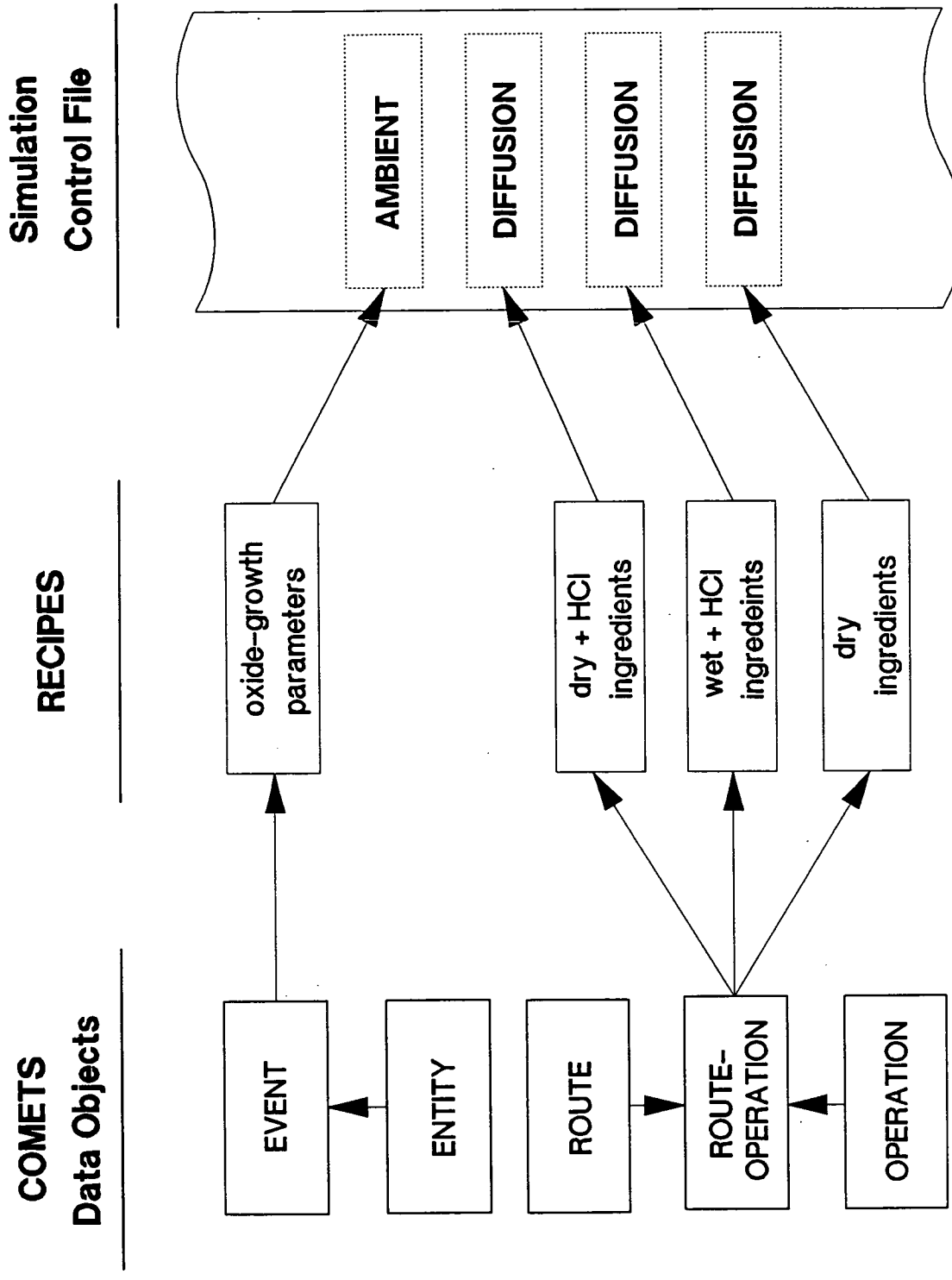


Figure 7.19 Approach taken to forming a simulation control file from the COMETS WIP data objects used to define a process.

Process transfer

The RCP module could potentially be used to aid process transfer. Already, within COMETS, it is possible to store information about the process sequence and the role played by processing equipment. The RCP module can then be used to explicitly specify the processing that should occur. Explicitly describing a process in this structured way encourages the development of more complete specifications than does a flat text file format. Then integrating process simulation into the CAM system through the SIM module allows more facility specific data to be incorporated. This data includes doping profiles, charge distributions and electrical characteristics at each process step. Without the combination of the RCP and SIM modules it is difficult to achieve this level of detail process description when transferring a process. The advantage is that when a process is transferred using these modules, the implementing engineers have a full specification for process step, not just for the process as a whole. Thus process transfer could be achieved more quickly and accurately than is currently possible.

Process development/compilation

Combining the functions of the SIM module with some sort of expert system could provide a framework for active process control[†]. This capability could be enhanced by the presence of the RCP module and its ability to provide on-line overrides of process recipes. With an appropriate expert system shell, the combination of RCP, SIM and the other COMETS modules might be used to investigate the development of processes that adhere to real production constraints; leading ultimately to automatic process compilation. In which case it would be sufficient to simply specify the desired final characteristics of the devices, and the process definition would be automatically generated.

Other environments

Finally, the investigation of recipes in this chapter has been limited to their application in IC fabrication. There is, however, no reason why they should not also be used in other phases of IC production. In assembly they might be used to store die bonding coordinates, and in test they could be used to hold test program details. Whatever the application, the RCP module can be used to consolidate production information in the CAM system; thus simplifying maintenance and ensuring security.

[†] As described in Chapter 6.

7.8. Summary

This chapter has described how recipe management can be integrated with a host-level CAM system to enhance the analysis and control of IC fabrication. A new module, called RCP, has been developed for the COMETS CAM system to demonstrate how recipe management could be implemented in a manufacturing environment. It is noted that recipe management can be used to capture all process specification data within one central area, thus greatly simplifying maintenance and security. For IC fabrication the presence of process recipes, along with the specification of the production sequence and engineering data collection, can result in much enhanced analysis and control of processing. From reviews of the literature[†] the RCP module emerges as the first recipe management system to fully describe processing for a flexible manufacturing environment. It is certainly the first to be integrated with the current generation of CAM systems.

The recipe management (RCP) module was developed to provide an explicit representation of processing for the SIM module. The result is a system that allows process information to be associated with processing equipment and with process steps. When a simulation is initiated by the SIM module the recipe information is collated and translated into simulation control files. The RCP module mirrors the flexibility that can be found in certain manufacturing environments by providing for different versions of recipe to be maintained and on-line overrides to be defined for a variety of criterion.

The functionality provided by the SIM module also allows the RCP module to work with the existing COMETS specification system to direct operators, and might be used to control processing in an automated environment. Recipe management at the host level therefore promises a high degree of flexibility for on-line analysis and control of IC fabrication.

It is evident that the RCP module could be used for more applications that IC fabrication. The system could easily be applied to assembly or test. Furthermore, recipe management, as part of a CAM system, could be used as a platform for expert systems to aid process analysis, development, and control. Alternatively, it could be used to capture the implicit context of a process and thereby streamline the transfer of processes between facilities.

In terms of software commitment the RCP module only amounts to about half of that

[†] As discussed in chapters 1 and 5.

of the COMETS SPC module. This is largely because the software of the RCP module is designed to take maximum advantage of the existing SPC programs.

References

1. A.J. MacDonald, "A Process Specification System for the Plessey Semiconductors Oldham Facility," Collaborative Report, EMF, Dept. of Elec. Eng. University of Edinburgh, Edinburgh, UK, March 1989.

Chapter 8

Conclusions

The application of advanced manufacturing technology (AMT) is seen as crucial to the future of semiconductor companies competing in highly volatile international markets. It is likely that AMT, and in particular manufacturing control systems, will need to be developed to allow greater flexibility and control of production. This Ph.D. tackles this issue; concentrating upon the enhancement of computer aided manufacturing (CAM) to provide powerful tools for the analysis and control of integrated circuit (IC) fabrication.

Presented here is a synopsis of the work covered during this Ph.D. and a discussion of its significance. Some directions for future research are also indicated.

The world market for semiconductors is subject to a myriad of influences. One consequence of which is that manufacturers are facing increasing pressure to react more quickly to the demands of the market in order to remain competitive. This can be seen in the movement away from the traditional dependence on maintaining a stable production environment towards the adoption of more flexible manufacturing technologies. Another consequence has been the polarisation of processing into single product/process commodity production, and multiple product/process application specific production. It is worth noting that flexibility is important for both of these approaches, although not always for the same reasons. Commodity manufacturers must satisfy product tolerances while process tolerances change over time. Manufacturers of lower volume standard products, and application specific ICs (ASICs), must be able to switch between processes at frequent intervals. All manufacturers must take account of equipment downtime, and be able to introduce new processes in the shortest possible time.

Paralleling the market trends that demand greater flexibility are the movements towards smaller device geometries and higher packing densities. These push processing equipment to their limits and make control very difficult. The importance of maximizing yield also discourages the use of destructive testing during processing, requiring process control to rely on in-line tests that are unable to verify all aspects of processing. Problems

are also being faced in matching product and process tolerances, and reducing lead-times for products that may only have a short life-span.

AMT has emerged as an approach to solving many of the problems caused by market demands and technical constraints. One of the most widely applied of these technologies has been CAM. This has been reported to provide improvements in production scheduling, and in production analysis and control through statistical methods. More long term goals have been set in terms of integrating all functions of a company in Computer Integrated Manufacturing (CIM) and achieving complete factory automation.

To be able to fully control IC fabrication it is essential to understand how all the operations of a process influence the final product. However, though there are only a basic set of manufacturing operation, processes tend to be highly dynamic and non-linear. Process steps are also strongly interdependent. Consequently the ability to track and analyse all processing has become very important. Without this capability it is very difficult to effectively control a fabrication process.

The process runsheet is a well tried method for collating information about process steps into a description of the process. A runsheet will normally contain the data necessary to specify, and control, the processing for a lot. However, runsheets lack the flexibility to describe lot movement that cannot be established *a priori*, such as reworking. They are also difficult to update if the process is modified during processing and generally do not capture all the contextual information about a facility. Analysing information that is stored over a series of runsheets is also difficult. A review of process control and the role of the runsheet is presented in chapter 2.

Encouraged, in part, by the limitations of runsheets, CAM systems have emerged as an essential tool for analysing and controlling IC fabrication. Around the core of work-in-progress (WIP) tracking have been developed functions for scheduling, statistical process control, costing, etc. In order to perform WIP tracking it is necessary to transfer the structure of the runsheet into the database of the CAM system. The additional flexibility of a computer system allows the tracking of lot movement to be represented more faithfully, including the splitting, reworking and merging of lots. Data collection also allows more powerful tools to be used for process analysis as all data can be easily accessed.

COMETS is probably the most widely used of semiconductor CAM systems. It consists of a set of modules that implement the basic CAM functions. COMETS was primarily designed for stable manufacturing environments and does not adapt well to flexible

manufacturing. This is largely because it does not provide the tools that are necessary to analyse IC fabrication, and because it is unable to effectively specify the level of control that is necessary for on-line flexible manufacturing.

At the core of all CAM/CIM systems is the database. The ability of manufacturing control systems to analyse and control processing is dependent on the way in which the facility is represented in the database. The current generation of CAM systems, such as COMETS, are unable to describe the relationships that exist between process steps, and so are only able to reactively track the movement of lots, rather than apply on-line control of processing. A fuller discussion of CAM system, and in particular COMETS, is provided in chapter 3.

Software models have been developed to describe the physical effect of performing a process step on a wafer. These models have been combined together to form process simulators that can be used to investigate the interrelation of operations in a process, and their effect on the final electrical characteristics of devices. Simulators are available to perform one-, two- and three-dimensional modelling of a process. 1D simulators, such as SUPREM-3, offer simpler and more robust models than more advanced 2D and 3D simulators. They also require dramatically less computational power which means that they can be used for a more intuitive investigation of processing. Chapter 4 provides an example of how the 1D simulator SUPREM-3 can be calibrated to a process; giving values for physical and electrical parameters that match well with those measured directly.

Though process simulation has become widely used for process development and optimisation, it is rarely applied to manufacturing. This is largely due to their inappropriate user interfaces, their complexity, and the fact that they tend to be batch oriented. Yet, much of the information that is required to control a simulator can be related to the information that is used to control processing. Much of the information that is used to establish physical environmental parameters can also be associated with processing equipment.

Integrating CAM and process simulation could be used to overcome many of the problems discussed so far. An understanding of the function and interrelation of process steps could be incorporated into the CAM system, and process engineers could be given access to the simulators through an interface that is familiar and that encourages interactive, and intuitive, use. This would lead to improvements in the understanding of processing on the shop-floor and thereby improve analysis and control. Process simulation could also be used to capture much of the contextual information in the facility, thus improving

the documentation of the process and easing process transfer.

To implement such a system it is important that the process simulator be integrated with a commercial CAM system so as to demonstrate its practical applicability. This has been achieved using the COMETS CAM system and the 1D simulators SUPREM-II, later replaced by SUPREM-3, as described in chapter 5 and 6. It should be noted, however, that these software packages could easily be replaced by others. The CAM system acts as an operating environment for the simulator controlling the simulation of each lot (in-process) as it moves through the facility so that a simulation history is developed. It also allows the complete fabrication of a product to be simulated, and the simulation of a single lot to be investigated. The control files used by the simulators are formed from information held within the CAM system.

The integrated system is implemented as a new module, called SIM, that has been added to COMETS. The in-process simulation functions are hidden from the user, but the interface to the product and lot simulation functions is structured and fits within the existing COMETS menu hierarchy. The lot simulation menu provides powerful *what-if* and *look-ahead* functions that allow interactive and intuitive investigation of processing. Ultimately the analysis capabilities provided by the SIM module can be used to apply feed-forward control of corrective processing. An example of this is given in chapter 6.

The input files for the simulator are generated from process recipe data that has been re-expressed in a format that can be used by the simulator. This has an intrinsic limitations in that it assumes that the user has some understanding of how the simulator is controlled. Ideally the simulator should be controlled with the same information used to control the process; i.e.. the information presented to the operator or downloaded to automated equipment. This would require that an explicit representation of the process be available within the CAM system.

A recipe management system has been developed to support the integration of process simulation and the COMETS CAM system. As described in chapters 5 and 7, this has been achieved by extending the COMETS database to include process information. Though primarily to provide a platform for the SIM module this information could also be used to store information to be used by operators, automated equipment, or other applications programs. Recipe management also offers the opportunity to perform flexible on-line control of processing through recipe editing functions and the application of overrides. Overrides might be applied for the entire facility, a process, a product, or simply a lot.

Storing the complete description of a process as a set of explicit recipes could also simplify data maintenance while improving security. Further use of process recipes can be found away from wafer fabrication, in assembly, test, and perhaps even in other industries.

Access to, and control of, the recipe information is carried out by another new module, called RCP, that has been added to COMETS. Part of the functionality of this module is used for the on-line presentation of recipe data through the existing COMETS specification system. The remainder is accessed through a set of menus integrated with the existing COMETS menu structure. These allow the creation, updating, and interrogation of recipes, and the application of overrides. All recipe management functions can be applied directly to the process specifications, thus allowing on-line control. A detailed discussion of the RCP module, and its implementation, can be found in chapter 7.

The software developed during this project is quite a significant addition to the volume of COMETS. The volume of code for the SIM module is approximately three times greater than that for the statistical quality control (SQC) module, and the code for the RCP module is about half that of the specification (SPC) module. The latter is largely because as many as possible of the existing SPC programs are also used by the RCP module.

The systems described within this Thesis are a step towards a new generation of integrated manufacturing systems. There are, however, many areas that remain unresearched. The work performed during this PhD might be best continued by investigating the application of artificial intelligence to IC manufacturing control. Expert system technology could be applied to the control of process simulation to provide automatic analysis of fabrication processes. This work could then be taken further to aid in the development of new processes, achieving a form of process compilation. Another area that might be investigated is the application of statistical methods to the process simulation tools described here. Currently this area is being investigated at the Edinburgh Microfabrication Facility by W.J.C. Alexander.

Appendix A

The EMF 1.5μm nMOS Process Runsheet

EDINBURGH MICROFABRICATION FACILITY

N-CHANNEL SILICON GATE VLSI

BATCH NUMBER: START DATE:

DEVICE IDENTIFICATION: Eu

MASK SET:

MASKING SEQUENCE: 1 2 3 4 6 7 8
MASK REV.LETTERS: A A A A A A A

STARTING MATERIAL: 14-20 ohm.cm.(100) P-type,3in.Dia.

No. OF WAFER STARTS:

INITIAL CLEAN

Start date: Start time: Initials:

10 min. boil in 2:1, Sulphuric acid:Hydrogen peroxide in Teflon jig
D.I water wash
Dip 3 min. in 10% HF in Polypropylene jig
Wash and spin dry

Finish date: Finish time: Initials:

INITIAL OXIDE

Start date: Start time: Initials:

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
5 min.Oxygen + HCl + Hydrogen Aim for 350 Angstroms
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

SILICON NITRIDE DEPOSITION

Furnace 3, 800oC
Preset flows: Dichlorosilane,30 cc/min. Ammonia,90 cc/min.
Deposition time: min. (aim for 1000 Angstroms)
Pressure during deposition: mTorr

Measure Si3N4 thickness:

Finish date: Finish time: Initials:

batch#

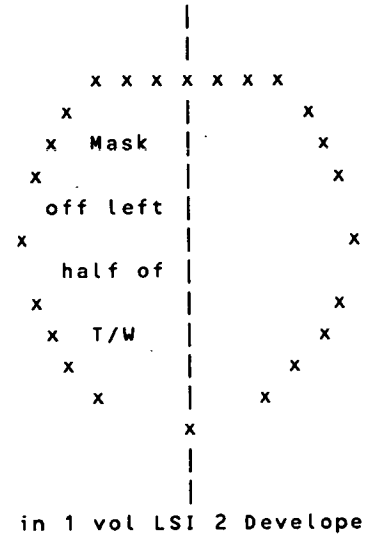
1st PHOTO (POSITIVE RESIST) LAYER 1

Start date: Start time: Initials:

HMDS vapour box prime for 30 min.

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven

Align and expose for secs. (Stepper)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130,oC for 30 min. in static oven
Inspect for proper baking

Finish date: Finish time: Initials:

SILICON NITRIDE RIE ETCH

Start date: Start time: Initials:

RIE etch 48 cc/min CF4 + 8 cc H2, 30 mTorr, 750 W

Repeat above with wafers face downwards to etch backs.

Finish date: Finish time: Initials:

BORON IMPLANT

Start date: Start time: Initials:

B11+ 7 e12 atoms/sq.cm. 70 keV

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Oxygen plasma ash
Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

FIELD OXIDE

Start date: Start time: Initials:

Furnace 7, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 24.5% (1.22 l/min.)
Hydrogen 20% (2.0 l/min.)
HCl 10% (0.1 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
0.5 hours Oxygen + Hydrogen + HCl
3.0 hours Oxygen + Hydrogen Aim for 6000 Angstroms
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

RESIST COAT

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs.
Hard bake for 30 min. at 130oC in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

4:1 ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF
Etch time: (Backs dewet)
Wash and spin dry

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry

Inspect for removal of resist.

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF for 15 secs.
Wash and spin dry

Finish date: Finish time: Initials:

SILICON NITRIDE WET ETCH

Start date: Start time: Initials:

Heat Orthophosphoric Acid to 165oC
Immerse wafers on Teflon jig for 0.5 hr or until nitride removed.
Wash and spin dry

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet scribelines
Wash and spin dry

Measure etched image: microns

Finish date: Finish time: Initials:

2nd PHOTO (POSITIVE RESIST) LAYER 2

Start date: Start time: Initials:

Pre-spin bake, furnace1, 950oC, Nitrogen 20% (2 l/min), 5 min.

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Stepper)
Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

ARSENIC IMPLANT

Start date: Start time: Initials:

As75++ 4.0e12 atoms/sq.cm. 90 keV

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Finish date: Finish time: Initials:

SACRIFICIAL OXIDE

Start date: Start time: Initials:

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:

Oxygen	20%	(1.5 l/min.)
HCl	15%	(0.15 l/min.)
Hydrogen	10%	(1.7 l/min.)

Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
5 min.Oxygen + HCl + Hydrogen Aim for 400 Angstroms
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

4:1 ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF
Etch time: Dewet scribelines
Wash and spin dry

Finish date: Finish time: Initials:

RCA CLEAN

Start date: Start time: Initials:

10 min. 80oC in 1:1:5, Ammonia:Hydrogen peroxide:water in Teflon jig
D.I water wash
10 min. 80oC in 1:1:5, HCl:Hydrogen peroxide:water in Teflon jig
D.I water wash
Wash and spin dry

Finish date: Finish time: Initials:

GATE OXIDE

Start date: Start time: Initials:

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min. Oxygen + HCl
2.2 min. Oxygen + HCl + Hydrogen Aim for 250 Angstroms
5 min. Oxygen

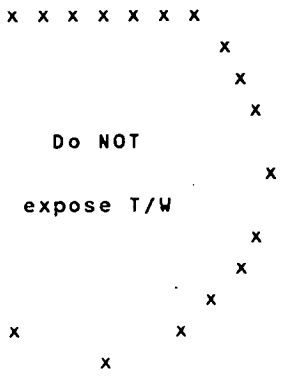
Measure oxide thickness:

Finish date: Finish time: Initials:

3rd PHOTO (POSITIVE RESIST) LAYER 3

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Stepper)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

4:1 ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF
Etch time: Dewet scribelines
Wash and spin dry

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

BORON IMPLANT (Double Implant)

Start date: Start time: Initials:

B11+ 7.0 e11 atoms/sq.cm. 25 keV
B11+ 7.0 e11 atoms/sq.cm. 140 keV

Finish date: Finish time: Initials:

RCA CLEAN

Start date: Start time: Initials:

10 min. 80oC in 1:1:5, Ammonia:Hydrogen peroxide:water in Teflon jig
D.I water wash
10 min. 80oC in 1:1:5, HCl:Hydrogen peroxide:water in Teflon jig
D.I water wash
Wash and spin dry

Finish date: Finish time: Initials:

POLY-SILICON DEPOSITION

Start date: Start time: Initials:

Furnace 4, 600oC
Preset flows: Silane,60 cc/min.
Deposition time: 40 min. (aim for 4000 Angstroms)
Pressure during deposition: mTorr

Measure poly-silicon thickness:

Finish date: Finish time: Initials:

PHOSPHORUS DEPOSITION (SOLID SOURCE)

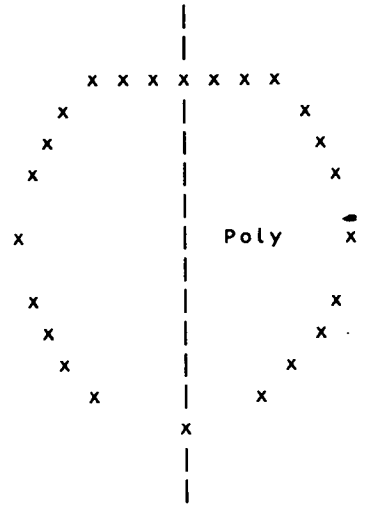
Start date: Start time: Initials:

Furnace 5, 850oC, idling on Nitrogen
Preset gas flows as follows:
Nitrogen 50 (2.0 l/min.)

Insert wafers at 4 ins./min.
20 min. ramp at 8.1oC/min. to up 1000oC

15 min. soak
20 min. ramp at 8.1oC/min. down to 850oC
Remove wafers at 4ins./min.

Measure sheet resistances



Poly: ohms/sq.

Finish date: Finish time: Initials:

PHOSPHORUS DEGLAZE

Start date: Start time: Initials:

Immerse for 30 secs. in 10% HF (1 vol HF, 9 vols DI)
Wash and spin dry

Finish date: Finish time: Initials:

POLY OXIDE

Start date: Start time: Initials:

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:

Oxygen	20%	(1.5 l/min.)
HCl	15%	(0.15 l/min.)
Hydrogen	10%	(1.7 l/min.)

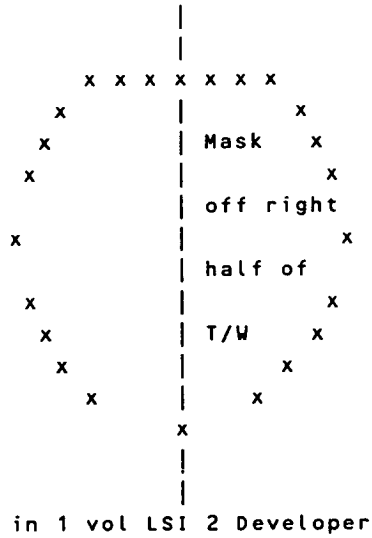
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
3 min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Finish date: Finish time: Initials:

4th PHOTO (POSITIVE RESIST) LAYER 4

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Stepper)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet t/w
Wash and spin dry

Finish date: Finish time: Initials:

POLY SILICON RIE ETCH

Start date: Start time: Initials:

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

ARSENIC IMPLANT

Start date: Start time: Initials:

As75+ 7.0e15 atoms/sq.cm. 90 keV

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Oxygen plasma ash 30 min.
Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

RESIST STRIP (KARO'S ACID)

Start date: Start time: Initials:

10 min. boil in 2:1, Sulphuric acid:Hydrogen peroxide in Teflon jig
D.I water wash
Wash and spin dry

Finish date: Finish time: Initials:

ANNEAL

Start date: Start time: Initials:

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (2.0 l/min.)
Load wafers into furnace for 10 min.

REFLOW PYRO DEPOSITION NO PHOSPHINE

Start date: Start time: Initials:

PWS 2000 Hotplate at 430oC, in right hand rest position.
Preset SPEED: 900 NOTE DIFFERENT SPEED FROM USUAL
Preset gas flows as follows:
Nitrogen(02),80 (4.0 l/min):Nitrogen(SiH4),60 (2.9 l/min)
5%Silane,110 (1.3l/min): Oxygen,60 (0.65l/min)
Water flow, 100

Include one fresh 14-20 ohm.cm. P-type test wafer per batch.

Place up to 6 wafers onto hotplate as close as possible to centre.
Press button <-- to deposit
When hotplate stops, remove wafers to steel worktop with Bernoulli tweezer
Reload with fresh wafers and press button -->

Continue with whole batch.

Measured thickness: Aim for 1500 Angstroms

Finish date: Finish time: Initials:

REFLOW PYRO DEPOSITION

Start date: Start time: Initials:

PWS 2000 Hotplate at 430oC, in right hand rest position.
Preset SPEED: 300 NOTE DIFFERENT SPEED FROM USUAL
Preset gas flows as follows:
Nitrogen(02),80 (4.0 l/min):Nitrogen(SiH4),60 (2.9 l/min)
5%Silane,110 (1.3l/min): 1%Phosphene,80 (0.96l/min): Oxygen,60 (0.65l/min)
Water flow, 100

Include one fresh 14-20 ohm.cm. P-type test wafer per batch.

Place up to 6 wafers onto hotplate as close as possible to centre.
Press button <-- to deposit
When hotplate stops, remove wafers to steel worktop with Bernoulli tweezer
Reload with fresh wafers and press button -->
Continue with whole batch.

Measured thickness: Aim for 4500 Angstroms

NOTE: Proceed immediately to First Reflow

Finish date: Finish time: Initials:

FIRST REFLOW
FURNACE 2 (02)
Temperature: 1000oC NOTE LOWER TEMPERATURE
Idling ambient: Oxygen

Preset gas flows as follows:
Oxygen 50 (2.0 l/min.)

Start date: Start time: Initials:

10 min. furnace time

Etch reflow pyro off extra T/W in 4:1, NH4F:HF.

Measure sheet resistance at 5 points: ohms/sq.
Discard T/W after use.

Finish date: Finish time: Initials:

DENSIFICATION OF REFLOW PYRO

Start date: Start time: Initials:

Furnace 7, 950oC, idling on oxygen
Preset gas flows as follows:

Oxygen 28% (1.4 l/min.)
Hydrogen 20% (2.0 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen
10 min.Oxygen + Hydrogen
5 min.Oxygen

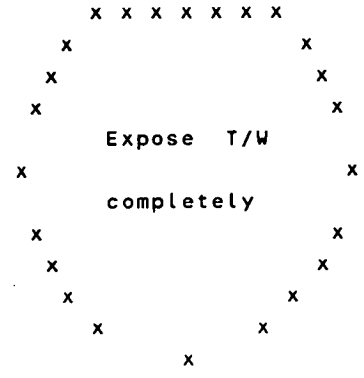
NOTE: Proceed immediately to resist spin for contact photo.

Finish date: Finish time: Initials:

5th PHOTO (POSITIVE RESIST) LAYER 6

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Stepper)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

R I E to clear contacts

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Oxygen plasma ash
Immerse in Fuming Nitric Acid 10 min

Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

PHOSPHORUS DEPOSITION (SOLID SOURCE)

Start date: Start time: Initials:

Furnace 5, 850oC, idling on Nitrogen
Preset gas flows as follows:
Nitrogen 50 (2.0 l/min.)

Insert wafers at 4 ins./min.
20 min. ramp at 8.1oC/min. to up 1000oC
10 min. soak
20 min. ramp at 8.1oC/min. down to 850oC
Remove wafers at 4ins./min.

Finish date: Finish time: Initials:

PHOSPHORUS DEGLAZE

Start date: Start time: Initials:

Immerse for 14 secs. in 10% HF (1 vol HF, 9 vols DI)
Wash and spin dry

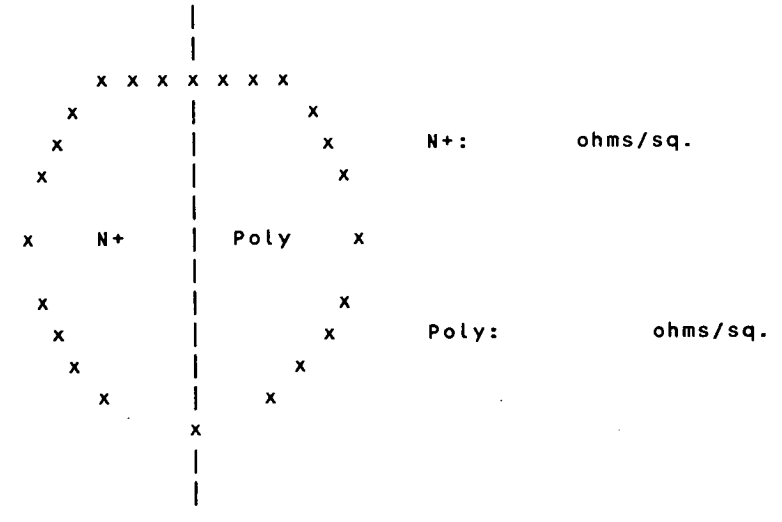
Finish date: Finish time: Initials:

PRE-ALUMINIUM EVAPORATION CLEAN

Start date: Start time: Initials:

Dip 20 secs. in reflow etch: 25 vols Ammonium Fluoride soln.(40%w/v),1 vol HF
Wash and spin dry

Re-measure sheet resistances



Discard test wafer

Finish date: Finish time: Initials:

ALUMINIUM EVAPORATION (Al-Si)

Start date: Start time: Initials:

Load wafers on palettes and load into Balzers BAS 450 coater.
Pump system to 5e-6 or better with Meissner trap.
Close shutter
Throttle pump and admit argon at 2e-3.
Set integrator at 9500, Range 3 (Aim for 1 micron)
Run up Aluminium/Silicon target to 6 kW.
Open shutter until integrator times out.
Warm up Meissner and chamber.
Vent system and remove wafers.

Finish date: Finish time: Initials:

6th PHOTO (POSITIVE RESIST) LAYER 7

Start date: Start time: Initials:

Spin HPR 204 at 4000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Stepper)
Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for >60 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

ALUMINIUM ETCH

Start date: Start time: Initials:

R.I.E. etch to clear patterns.

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Measure AlSi thickness: Microns

batch#

Finish date: Finish time: Initials:

SINTER

Start date: Start time: Initials:

Furnace 8, 435oC, idling on Nitrogen
5 min. Nitrogen,25,(1 l/min.)
10 min. 40% Hydrogen/Nitrogen,25,(1 l/min.)
5 min. Nitrogen

Finish date: Finish time: Initials:

ELECTRICAL TEST

Start date: Start time: Initials:

Finish date: Finish time: Initials:

Appendix B

nMOS Process ROUTES and OPERATIONS

ROUTE :	**NITDP N1.5**	**CLEAN, OXIDE AND NITRIDE 1.5UM NMOS**
6000	INITCLEAN1	INITIAL WAFER CLEAN 1
2000	PAD OX 1	INITIAL PAD OXIDATION 1
3000	NITRIDE 1	SILICON NITRIDE DEPOSITION 1
ROUTE :	**LITH1 N1.5**	**1ST PHOTO 1.5UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7200	EXPOSE 1	EXPOSE 1 (MASK LEFT HALF OF T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**RNIT1 N1.5**	**REMOVE NITRIDE 1 1.5 UM NMOS**
6400	NITETCH 1	SILICON NITRIDE (RIE) ETCH 1
ROUTE :	**FLDIM N1.5**	**BORON FIELD IMPLANT 1.5UM NMOS**
1000	FIELDIMP1	BORON FIELD IMPLANT 1 (7E12,70KEV)
ROUTE :	**RSTP1 N1.5**	**RESIST STRIP 1 1.5 UM NMOS**
6100	RESSTRIP 1	RESIST STRIP 1 (NITRIC ACID)
ROUTE :	**LOCOS N1.5**	**FIELD OX GROWTH 1.5UM NMOS**
2200	FIELD OX 1	FIELD OXIDATION 1
ROUTE :	**RMBOX N1.5**	**RESIST COAT FRONT,OX ETCH 1.5UM NMOS**
7010	RESCOAT1	RESIST COAT AND HARD BAKE
6210	OXIETCH 2	4:1 AMMONIUM FLUORIDE:HF OX ETCH 2
6120	RESSTRIP 2	RESIST STRIP 2 (NITRIC ACID)
ROUTE :	**RNIT2 N1.5**	**OX, NIT & RESIST REMOVE 2 1.5UM NMOS**
6260	OXIETCH 7	4:1 AMMONIUM FLUORIDE:HF OX ETCH 7
6410	NITETCH 1	SILICON NITRIDE PLASMA ETCH 1
6220	OXIETCH 3	4:1 AMMONIUM FLUORIDE:HF OX ETCH 3

ROUTE :	**LITH2 N1.5**	**2ND PHOTO 1.5UM NMOS**
7620	PSPNBAKE 1	PRE-SPIN BAKE
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7210	EXPOSE 2	EXPOSE 2 CONTACT RESIST (POS)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1

ROUTE :	**DEPIM N1.5**	**AS++DEPLETION IMPLANT 1.5UM NMOS**
1400	DEPLIMP 1	AS++ DEPLETION IMPLANT 1 (4E12,90KEV)

ROUTE :	**RSTP2 N1.5**	**RESIST STRIP 2 1.5UM NMOS**
6120	RESSTRIP 2	RESIST STRIP 2 (NITRIC ACID)

ROUTE :	**GTEOX N1.5**	**SACRIFICIAL & GATE OX GROWTH 1.5UM NMOS**
2500	SACROX 1	SACRIFICIAL OXIDE 1
6230	OXIETCH 4	4:1 AMMONIUM FLUORIDE:HF OX ETCH 4
6010	POXIDCLN 1	PRE-OXIDATION CLEAN 1
2400	GATEOX 1	GATE OXIDATION 1

ROUTE :	**LITH3 N1.5**	**3RD PHOTO 1.5UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7220	EXPOSE 3	EXPOSE 3 (DO NOT EXPOSE T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1

ROUTE :	**GOXET N1.5**	**GATE OXIDE ETCH & STRIP 1.5UM NMOS**
6230	OXIETCH 4	4:1 AMMONIUM FLUORIDE:HF OX ETCH 4
6120	RESSTRIP 2	RESIST STRIP 2 (NITRIC ACID)

ROUTE :	**ENHIM N1.5**	**VT ADJUST ENHANCE IMPLANT 1.5UM NMOS**
1200	VTADJIMP 1	VT ADJUST IMPLANT 1 (7.0E11,25KEV)
1210	VTADJIMP 2	VT ADJUST IMPLANT 2 (7.0E11,140KEV)

ROUTE :	**POLY N1.5**	**CLEAN, POLY DEP, DOPE & OX 1.5UM NMOS**
6020	PPDEPCLN 1	PRE-POLY DEPOSITON CLEAN 1
3100	POLY-SI 1	POLY-SILICON DEPOSITION 1
3200	PDEP 1	PHOSPHORUS DEPOSITION 1 (SOLID)
6600	DEGLAZE 1	PHOSPHORUS DEGLAZE 1
2600	POLYOX 1	POLY OXIDE OXIDATION 1

ROUTE :	**LITH4 N1.5**	**4TH PHOTO 1.5UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7230	EXPOSE 4	EXPOSE 4 (MASK RIGHT HALF OF T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1

ROUTE :	**RPOLY N1.5**	**OX, POLY & RESIST REMOVAL 1.5UM NMOS**
6240	OXIETCH 5	4:1 AMMONIUM FLUORIDE:HF OX ETCH 5
6420	PSIETCH 1	POLY SILICON PLASMA ETCH 1
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2

ROUTE :	**SDIMPL N1.5**	**AS+SOURCE DRAIN IMPLANT 1.5UM NMOS**
1450	SDIMPL 1	AS+SOURCE DRAIN IMPLANT 1 (7.0E15,90KEV)

ROUTE :	**RSTP3 N1.5**	**RESIST STRIP 3 N1.5UM NMOS**
6130	RESSTRIP 3	RESIST STRIP 3 (NITRIC ACID)
6140	RESSTRIP 4	RESIST STRIP 4 (SULPHURIC/H.PEROXIDE)

ROUTE :	**SDANL N1.5**	**SOURCE DRAIN ANNEAL 1.5UM NMOS**
4000	SDANNEAL 1	SOURCE DRAIN ANNEAL 1

ROUTE :	**PYROD N1.5**	**PYRO DEP,1ST REFLOW & DENS 1.5UM NMOS**
3300	PYRO DEP 1	PYRO DEPOSITION 1
3310	PYRO DEP 2	PYRO DEPOSITION 2 (REFLOW)
2800	1 REFLOW 1	FIRST REFLOW OXIDATION 1

6310	TWPYRE 1	T/W REFLOW PYRO ETCH (NH4F:HF) 1
2810	DEPYRO 1	DENSIFICATION OF REFLOW PYRO 1
ROUTE :	**LITH5 N1.5**	**5TH PHOTO 1.5UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7240	EXPOSE 5	EXPOSE 5 (EXPOSE T/W COMPLETELY)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**ALCON N1.5**	**OX ETCH, STRIP & 2ND REFLO 1.5UM NMOS**
6240	OXIETCH 5	OXIDE (RIE) ETCH 5
6100	RESSTRIP 1	RESIST STRIP 1 (NITRIC ACID)
ROUTE :	**DPCON N1.5**	**PHOSPHORUS DOPE CONTACTS 1.5UM NMOS**
3200	PDEP 1	PHOSPHORUS DEPOSITION 1 (SOLID)
6600	DEGLAZE 1	PHOSPHORUS DEGLAZE 1
ROUTE :	**ALDEP N1.5**	**CLEAN AND AL SPUTTER 1.5UM NMOS**
6040	PRE-AL 1	PRE-ALUMINIUM EVAPORATION CLEAN 1
3500	AL EVAP 1	ALUMINIUM EVAPORATION 1
ROUTE :	**LITH6 N1.5**	**6TH PHOTO 1.5UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7210	EXPOSE 2	EXPOSE 2 CONTACT RESIST (POS)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**ALETC N1.5**	**AL ETCH, STRIP & SINTER 1.5UM NMOS**
6800	AL ETCH 1	ALUMINIUM ETCH 1 (R.I.E.)
6130	RESSTRIP 3	RESIST STRIP (NITRIC ACID) 3
4400	SINTER 1	ALUMINIUM SINTER 1

ROUTE :	**PARAM N1.5**	**PARAMETRIC TEST 1.5UM NMOS**
5000	PARA TST 1	PARAMETRIC TEST 1

Appendix C

SUPREM-3 output files for the 1.5μm nMOS process

The SUPREM-3 output files for the following nMOS sections have been included in this appendix:

(a) The enhancement channel section.

(b) The depletion channel section.

(c) The source/drain section.

(d) The source/drain section, inside the contact region.

(e) The field section.

```
*********************************************************
***                      SUPREM-3                     ***
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*********************************************************

                      1-NOV-89 15:02:51


  Statements input from file section.file



1... title  EMF 1.5 micron nMOS process
 ... +      n-channel enhancement section

2... $  Initialize the silicon substrate
3... initialize  <100>  silicon boron=7e14
 ... +           thickness=1.25  DX=0.001 spaces=100

4... $ calculate ionization impurity concentrations
5... material silicon semiconductor ionizati

6... $ increase dry-oxide growth rate
7... ambient O2  <100>  H.LIN.0=0.2e6

8... $ reduce wet-oxide growth rate
9... ambient H2O <100> H.PAR.0=5.8

10... $ stop phosphorus diffusion through oxide
11... impurity phosphor oxide dix.0=0

12... $  INITIAL CLEAN

13... $  INITIAL OXIDE
14... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
15... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
16... diffusion temp=950 time=5 F.O2=1.5
17... print layers

18... $  SILICON NITRIDE DEPOSITION
19... deposition nitride thickness=0.1 temp=800 time=25

20... $  LAYER 1 PHOTO(1) - ISOLATION REGIONS

21... $  SILICON NITRIDE RIE ETCH

22... $  FIELD IMPLANTATION

23... $  LAYER 1 RESIST STRIP

24... $  FIELD OXIDE
25... diffusion temp=950 time=220 inert
```

```
26... $  RESIST COAT

27... $  ETCH BACK OF WAFER

28... $  RESIST STRIP

29... $  ETCH PARASITIC OXIDE

30... $  ETCH PROTECTIVE NITRIDE
31... etch nitride

32... $  ETCH INITIAL OXIDE
33... etch oxide

34... $  LAYER 2 PHOTO(2) - DEPLETION CHANNELS

35... $  DEPLETION IMPLANT

36... $  LAYER 2 RESIST STRIP

37... $  SACRIFICIAL OXIDE
38... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
39... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
40... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15

41... $ SACRIFICIAL OXIDE ETCH
42... etch oxide

43... $  RCA CLEAN

44... $  GATE OXIDE
45... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
46... diffusion temp=950 time=2.2 F.O2=1.5 F.HCL=0.15 F.H2=1.7
47... diffusion temp=950 time=5 F.O2=1.5
48... print layers

49... $  LAYER 3 PHOTO(3) - BURIED CONTACTS

50... $  OXIDE ETCH

51... $  LAYER 3 RESIST STRIP

52... $  THRESHOLD VOLTAGE IMPLANTATION
53... implant boron dose=7e11 energy=25
54... implant boron dose=7e11 energy=140
55... print layers

56... $  RCA CLEAN

57... $  POLYSILICON DEPOSITION
58... deposit polysilicon temperature=600 thickness=0.4

59... $  PHOSPHORUS DEPOSITION
60... diffusion temp=850 time=20 t.rate=7.5 inert
61... diffusion temp=1000 time=15 phosphorus=1.65e20
62... diffusion temp=1000 time=20 t.rate=-7.5 inert
```

```
63... print electrical

64... $  PHOSPHORUS DEGLAZE

65... $  POLYSILICON OXIDATION
66... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
67... diffusion temp=950 time=3 F.O2=1.5 F.HCL=0.15 F.H2=1.7
68... diffusion temp=950 time=5 F.O2=1.5

69... $  LAYER 4 PHOTO(4) - POLYSILICON GATES AND INTERCONNECTS

70... $  POLYOXIDE ETCH

71... $  POLYSILICON RIE ETCH

72... $  LAYER 4 RESIST STRIP

73... $  IMPLANT SOURCE DRAIN REGIONS

74... $  SOURCE DRAIN ANNEAL
75... diffusion temp=950 time=10 inert

76... $  REFLOW PYRO DEPOSITION NO PHOSPHINE

77... $  REFLOW PYRO DEPOSITION

78... $  FIRST REFLOW
79... diffusion temp=1000 time=10 inert

80... $ DENSIFICATION OF REFLOW PYRO
81... diffusion temp=950 time=20 inert

82... $  LAYER 6 PHOTO(5) - DEFINE METAL CONTACTS

83... $  ETCH PYRO OXIDE

84... $  LAYER 6 RESIST STRIP

85... $  PHOSPHORUS DEPOSITION
86... diffusion temp=850 time=20 t.rate=7.5 inert
87... diffusion temp=1000 time=10 inert
88... diffusion temp=1000 time=20 t.rate=-7.5 inert

89... $  PHOSPHORUS DEGLAZE

90... $  PRE-ALUMINIUM EVAPORATION CLEAN

91... $  ALUMINIUM EVAPORATION

92... $  LAYER 7 PHOTO(6) - DEFINE WINDOWS

93... $  ALUMINIUM ETCH

94... $  LAYER 7 RESIST STRIP

95... $  SINTER
```

```
 96... print layer electric

 97... $----------------------------------------------------------------

 98... $ perform electrical calculations to get the threshold voltage
 99... electrical vth.elec steps=31 layer=1 ^print  file=section.elec
100... bias layer=3 V=0 dv=0.05 abscissa
101... qss conc=3e10 layer=1
102... end

103... extract name=gox thickness layer=2
104... extract name=vt  v.threshold

105... $  plot the resulting chemical concentrations of the net boron
106... $  and phosphorus distributions.
107... plot chemical boron line.type=1 device=4010
   ... +    title="EMF 1.5 micron nMOS process - enhancement section"
   ... +    plot.out=section.profile
108... plot chemical phosphorus line.type=3 add

109... assign name=gox n.value=1*nint(1e4*&gox)
110... label label="Gate Oxide Thickness: "&gox" A" x=1
111... assign name=vt n.value=.01*nint(1e2*&vt)
112... label label="Threshold Voltage: "&vt" V"

113... label label="boron"       x=1.2  y=3e15
114... label label="phosphorus"  x=0.15 y=1e19

115... $  plot the electrical characteristics
116... plot file=section.elec e.cond device=4010 plot.out=section.cvplot
   ... +    layer=1 bottom=0 top=0.6e-4
   ... +    title="EMF 1.5 micron nMOS process - enhancement section"
   ... +    ^Y.LOG symbol=1
117... label label="Threshold Voltage: "&vt" V"

118... $ End of Enhancement Section Simulation
119... stop

Input line    3
Coefficient data group read
File: S3COF0
Date: 28-AUG-89 16:03:07
Documentation from data file:

SUPREM-3 Revision 8834 coefficient initialization
```

EMF 1.5 micron nMOS process
n-channel enhancement section
INITIAL OXIDE

Material layer information
Input line 17

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0372	0.0100	0.00	398	407	
1	silicon	1.2336	0.0010	0.00	408	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-3.9290E+09	-3.9290E+09	3.9290E+09	3.9290E+09
1	-8.3408E+10	-8.3408E+10	8.3408E+10	8.3408E+10
sum	-8.7337E+10	-8.7337E+10	8.7337E+10	8.7337E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	3.9290E+09	3.9290E+09
1	8.3408E+10	8.3408E+10
sum	8.7337E+10	8.7337E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region.

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0372	3.9290E+09	3.9290E+09
1	1	p	0.0000	1.2336	8.3408E+10	8.3408E+10

EMF 1.5 micron nMOS process
n-channel enhancement section
GATE OXIDE

Material layer information
Input line 48

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-1.6823E+09	-1.6823E+09	1.6823E+09	1.6823E+09
1	-7.8089E+10	-7.8089E+10	7.8089E+10	7.8089E+10
sum	-7.9771E+10	-7.9771E+10	7.9771E+10	7.9771E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	1.6823E+09	1.6823E+09
1	7.8089E+10	7.8089E+10
sum	7.9771E+10	7.9771E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	1.6823E+09	1.6823E+09
1	1	p	0.0000	1.2048	7.8089E+10	7.8089E+10

EMF 1.5 micron nMOS process
n-channel enhancement section
THRESHOLD VOLTAGE IMPLANTATION

Material layer information
Input line 55

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-2.1054E+10	-2.1054E+10	2.1054E+10	2.1054E+10
1	-1.4532E+12	-1.4532E+12	1.4532E+12	1.4532E+12
sum	-1.4743E+12	-1.4743E+12	1.4743E+12	1.4743E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	2.1054E+10	2.1054E+10
1	1.4532E+12	1.4532E+12
sum	1.4743E+12	1.4743E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	2.1054E+10	2.1054E+10
1	1	p	0.0000	1.2048	1.4532E+12	1.4532E+12

EMF 1.5 micron nMOS process
n-channel enhancement section
PHOSPHORUS DEPOSITION

Electrical information
Input line 63

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	1.579E+15	2.1423E-02	4.6679E+01	1.3260E+07	7.5413E-08
1	1	p	3.387E+04	4.1690E-12	2.3987E+11	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	1.140E+12	7.5259E-05	1.3287E+04	3.3147E-01	3.0168E+00

EMF 1.5 micron nMOS process
n-channel enhancement section
SINTER

Material layer information
Input line 96

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
4	oxide	0.0374	0.0100	0.00	368	370	
3	polysilicon	0.3835	0.0100	0.00	371	410	0.3776
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	boron	phosphorus
3	9.9119E-01	8.5487E-01

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
4	9.2677E+12	9.2677E+12	9.2677E+12	9.2677E+12
3	1.6924E+15	1.6924E+15	1.6924E+15	1.6924E+15
2	2.8028E+10	2.8028E+10	1.8258E+11	1.8258E+11
1	-1.3963E+12	-1.3963E+12	1.3963E+12	1.3963E+12
sum	1.7003E+15	1.7003E+15	1.7032E+15	1.7032E+15

Integrated Dopant (/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
4	3.2817E+07	3.2817E+07	9.2677E+12	9.2677E+12
3	6.3138E+08	6.3138E+08	1.6924E+15	1.6924E+15
2	7.7275E+10	7.7275E+10	1.0530E+11	1.0530E+11
1	1.3963E+12	1.3963E+12	0.0000E+00	0.0000E+00
sum	1.4742E+12	1.4742E+12	1.7017E+15	1.7017E+15

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
4	2	p	0.0000	0.0000	5.5693E-08	5.5693E-08
4	1	n	0.0000	0.0374	9.2677E+12	9.2677E+12
3	1	n	0.0000	0.3835	1.6924E+15	1.6924E+15
2	2	n	0.0000	0.0014	1.0496E+11	1.0564E+11
2	1	p	0.0014	0.0254	7.6936E+10	7.6936E+10
1	1	p	0.0000	1.2048	1.3963E+12	1.3963E+12

EMF 1.5 micron nMOS process
n-channel enhancement section
'SINTER

Electrical information
Input line 96

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	1.446E+15	1.9549E-02	5.1154E+01	1.3289E+07	7.5252E-08
1	1	p	7.629E+04	9.6257E-12	1.0389E+11	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	1.164E+12	7.7311E-05	1.2935E+04	1.4949E-01	6.6892E+00

```
EMF 1.5 micron nMOS process
n-channel enhancement section
perform electrical calculations to get the threshold voltage

Electrical information
Input line  102


Electron threshold (volts) :   5.3269E-01
 Extrapolated from :
  index= 21  bias=  1.0000E+00  conductance=  3.8117E-05
  index= 22  bias=  1.0500E+00  conductance=  4.2195E-05


*** END SUPREM-3 ***
```

```
**********************************************************
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**********************************************************

                      1-NOV-89 15:04:21


  Statements input from file section.file


1... title  EMF 1.5 micron nMOS process
 ... +      n-channel depletion section

2... $  Initialize the silicon substrate
3... initialize  <100>  silicon boron=7e14
 ... +           thickness=1.25  DX=0.001 spaces=100

4... $ calculate ionization impurity concentrations
5... material silicon semiconductor ionizati

6... $ increase dry-oxide growth rate
7... ambient O2  <100>  H.LIN.0=0.2e6

8... $ reduce wet-oxide growth rate
9... ambient H2O <100> H.PAR.0=5.8

10... $ stop phosphorus diffusion through oxide
11... impurity phosphorus oxide dix.0=0

12... $  INITIAL CLEAN

13... $  INITIAL OXIDE
14... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
15... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
16... diffusion temp=950 time=5 F.O2=1.5
17... print layers

18... $  SILICON NITRIDE DEPOSITION
19... deposition nitride thickness=0.1 temp=800 time=25

20... $  LAYER 1 PHOTO(1) - ISOLATION REGIONS

21... $  SILICON NITRIDE RIE ETCH

22... $  FIELD IMPLANTATION

23... $  LAYER 1 RESIST STRIP

24... $  FIELD OXIDE
25... diffusion temp=950 time=220 inert
```

```
26... $  RESIST COAT

27... $  ETCH BACK OF WAFER

28... $  RESIST STRIP

29... $  ETCH PARASITIC OXIDE

30... $  ETCH PROTECTIVE NITRIDE
31... etch nitride

32... $  ETCH INITIAL OXIDE
33... etch oxide

34... $  LAYER 2 PHOTO(2) - DEPLETION CHANNELS

35... $  DEPLETION IMPLANT
36... implant arsenic dose=4e12 energy=180

37... $  LAYER 2 RESIST STRIP

38... $  SACRIFICIAL OXIDE
39... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
40... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
41... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15

42... $  SACRIFICIAL OXIDE ETCH
43... etch oxide

44... $  RCA CLEAN

45... $  GATE OXIDE
46... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
47... diffusion temp=950 time=2.2 F.O2=1.5 F.HCL=0.15 F.H2=1.7
48... diffusion temp=950 time=5 F.O2=1.5
49... print layers

50... $  LAYER 3 PHOTO(3) - BURIED CONTACTS

51... $  OXIDE ETCH

52... $  LAYER 3 RESIST STRIP

53... $  THRESHOLD VOLTAGE IMPLANTATION
54... implant boron dose=7e11 energy=25
55... implant boron dose=7e11 energy=140
56... print layers

57... $  RCA CLEAN

58... $  POLYSILICON DEPOSITION
59... deposit polysilicon temperature=600 thickness=0.4

60... $  PHOSPHORUS DEPOSITION
61... diffusion temp=850 time=20 t.rate=7.5 inert
62... diffusion temp=1000 time=15 phosphorus=1.65e20
```

```
63... diffusion temp=1000 time=20 t.rate=-7.5 inert

64... $  PHOSPHORUS DEGLAZE

65... $  POLYSILICON OXIDATION
66... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
67... diffusion temp=950 time=3 F.O2=1.5 F.HCL=0.15 F.H2=1.7
68... diffusion temp=950 time=5 F.O2=1.5

69... $  LAYER 4 PHOTO(4) - POLYSILICON GATES AND INTERCONNECTS

70... $  POLYOXIDE ETCH

71... $  POLYSILICON RIE ETCH

72... $  LAYER 4 RESIST STRIP

73... $  IMPLANT SOURCE DRAIN REGIONS

74... $  SOURCE DRAIN ANNEAL
75... diffusion temp=950 time=10 inert

76... $  REFLOW PYRO DEPOSITION NO PHOSPHINE

77... $  REFLOW PYRO DEPOSITION

78... $  FIRST REFLOW
79... diffusion temp=1000 time=10 inert

80... $ DENSIFICATION OF REFLOW PYRO
81... diffusion temp=950 time=20 inert

82... $  LAYER 6 PHOTO(5) - DEFINE METAL CONTACTS

83... $  ETCH PYRO OXIDE

84... $  LAYER 6 RESIST STRIP

85... $  PHOSPHORUS DEPOSITION
86... diffusion temp=850 time=20 t.rate=7.5 inert
87... diffusion temp=1000 time=10 inert
88... diffusion temp=1000 time=20 t.rate=-7.5 inert

89... $  PHOSPHORUS DEGLAZE

90... $  PRE-ALUMINIUM EVAPORATION CLEAN

91... $  ALUMINIUM EVAPORATION

92... $  LAYER 7 PHOTO(6) - DEFINE WINDOWS

93... $  ALUMINIUM ETCH

94... $  LAYER 7 RESIST STRIP

95... $  SINTER
```

```
 96... print layers electrical

 97... $----------------------------------------------------------------

 98... $ perform electrical calculations to get the threshold voltage
 99... electrical vth.elec steps=61 layer=1 ^print  file=section.elec
100... bias layer=3 V=-6 dv=.1 abscissa
101... qss conc=3e10 layer=1
102... end

103... extract name=gox thickness layer=2
104... extract name=vt  v.threshold

105... $  plot the resulting chemical concentrations of the net boron
106... $  and phosphorus distributions.
107... plot chemical boron line.type=1 device=4010
   ... +    title="EMF 1.5 micron nMOS process - depletion section"
   ... +    plot.out=section.profile
108... plot chemical arsenic line.type=2 add
109... plot chemical phosphorus line.type=3 add

110... assign name=gox n.value=1*nint(1e4*&gox)
111... label label="Gate Oxide Thickness: "&gox" A" x=1
112... assign name=vt n.value=.01*nint(1e2*&vt)
113... label label="Threshold Voltage: "&vt" V"

114... label label="boron"       x=1.2   y=3e15
115... label label="arsenic"     x=0.65  y=7e16
116... label label="phosphorus"  x=0.15  y=1e19

117... $ End of Depletion Section Simulation
118... stop

Input line    3
Coefficient data group read
File: S3COF0
Date: 28-AUG-89 16:03:07
Documentation from data file:

SUPREM-3 Revision 8834 coefficient initialization
```

EMF 1.5 micron nMOS process
n-channel depletion section
INITIAL OXIDE

Material layer information
Input line 17

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0372	0.0100	0.00	398	407	
1	silicon	1.2336	0.0010	0.00	408	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-3.9290E+09	-3.9290E+09	3.9290E+09	3.9290E+09
1	-8.3408E+10	-8.3408E+10	8.3408E+10	8.3408E+10
sum	-8.7337E+10	-8.7337E+10	8.7337E+10	8.7337E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	3.9290E+09	3.9290E+09
1	8.3408E+10	8.3408E+10
sum	8.7337E+10	8.7337E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0372	3.9290E+09	3.9290E+09
1	1	p	0.0000	1.2336	8.3408E+10	8.3408E+10

EMF 1.5 micron nMOS process
n-channel depletion section
GATE OXIDE

Material layer information
Input line 49

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	2.2092E+10	2.2092E+10	2.5428E+10	2.5428E+10
1	3.8929E+12	3.8929E+12	4.0491E+12	4.0491E+12
sum	3.9150E+12	3.9150E+12	4.0745E+12	4.0745E+12

Integrated Dopant (/cm**2)

layer	boron		arsenic	
no.	active	chemical	active	chemical
2	1.6679E+09	1.6679E+09	2.3760E+10	2.3760E+10
1	7.8105E+10	7.8105E+10	3.9710E+12	3.9710E+12
sum	7.9773E+10	7.9773E+10	3.9947E+12	3.9947E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	2	p	0.0000	0.0000	2.4877E+02	2.5700E+02
2	1	n	0.0000	0.0254	2.2092E+10	2.5428E+10
1	2	n	0.0000	0.2645	3.9571E+12	3.9826E+12
1	1	p	0.2645	1.2048	6.4210E+10	6.6445E+10

EMF 1.5 micron nMOS process
n-channel depletion section
THRESHOLD VOLTAGE IMPLANTATION

Material layer information
Input line 56

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	2.6946E+09	2.6946E+09	4.4826E+10	4.4826E+10
1	2.5178E+12	2.5178E+12	5.4242E+12	5.4242E+12
sum	2.5205E+12	2.5205E+12	5.4690E+12	5.4690E+12

Integrated Dopant (/cm**2)

layer	boron		arsenic	
no.	active	chemical	active	chemical
2	2.1066E+10	2.1066E+10	2.3760E+10	2.3760E+10
1	1.4532E+12	1.4532E+12	3.9710E+12	3.9710E+12
sum	1.4743E+12	1.4743E+12	3.9947E+12	3.9947E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	3	p	0.0000	0.0044	3.5595E+08	3.8846E+09
2	2	n	0.0044	0.0218	5.7138E+09	3.3927E+10
2	1	p	0.0218	0.0254	2.6632E+09	7.0144E+09
1	2	n	0.0000	0.2282	3.2512E+12	4.6737E+12
1	1	p	0.2282	1.2048	7.3342E+11	7.5046E+11

EMF 1.5 micron nMOS process
n-channel depletion section
SINTER

Material layer information
Input line 96

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
4	oxide	0.0374	0.0100	0.00	368	370	
3	polysilicon	0.3835	0.0100	0.00	371	410	0.3776
2	oxide	0.0254	0.0100	0.00	411	415	
1	silicon	1.2048	0.0010	0.00	416	500	<100>

Polysilicon Ratios of Chemical Interior Grain to Total Concentrations

layer no.	boron	phosphorus	arsenic
3	9.9120E-01	8.5487E-01	8.8261E-01

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
4	9.2676E+12	9.2676E+12	9.2676E+12	9.2676E+12
3	1.6923E+15	1.6923E+15	1.6923E+15	1.6923E+15
2	5.1461E+10	5.1461E+10	2.0606E+11	2.0606E+11
1	2.5744E+12	2.5744E+12	5.3670E+12	5.3670E+12
sum	1.7042E+15	1.7042E+15	1.7072E+15	1.7072E+15

Integrated Dopant (/cm**2)

layer	phosphorus		arsenic	
no.	active	chemical	active	chemical
4	9.2676E+12	9.2676E+12	8.3525E+03	8.3525E+03
3	1.6923E+15	1.6923E+15	8.8162E+06	8.8162E+06
2	1.0471E+11	1.0471E+11	2.4050E+10	2.4050E+10
1	0.0000E+00	0.0000E+00	3.9707E+12	3.9707E+12
sum	1.7017E+15	1.7017E+15	3.9947E+12	3.9947E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
4	3.2748E+07	3.2748E+07
3	6.3125E+08	6.3125E+08
2	7.7302E+10	7.7302E+10
1	1.3963E+12	1.3963E+12
sum	1.4742E+12	1.4742E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
4	2	p	0.0000	0.0000	5.5245E-08	5.5245E-08
4	1	n	0.0000	0.0374	9.2676E+12	9.2676E+12
3	1	n	0.0000	0.3835	1.6923E+15	1.6923E+15
2	2	n	0.0000	0.0180	1.0707E+11	1.3191E+11

2	1	p	0.0180	0.0254	5.5608E+10	7.4155E+10
1	2	n	0.0000	0.2156	3.3055E+12	4.5443E+12
1	1	p	0.2156	1.2048	7.3113E+11	8.2271E+11

EMF 1.5 micron nMOS process
n-channel depletion section
SINTER

Electrical information
Input line 96

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	2	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	1.447E+15	1.9554E-02	5.1141E+01	1.3292E+07	7.5232E-08
1	2	n	2.818E+12	2.2720E-04	4.4014E+03	1.9615E+03	5.0981E-04
1	1	p	3.784E+06	4.7382E-10	2.1105E+09	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	2	n	1.224E+01	6.3662E-16	1.5708E+15	0.0000E+00	
1	1	p	6.190E+11	4.2559E-05	2.3497E+04	2.9995E-03	3.3339E+02

```
EMF 1.5 micron nMOS process
n-channel depletion section
perform electrical calculations to get the threshold voltage

Electrical information
Input line  102


Electron threshold (volts) :  -3.6155E+00
 Extrapolated from :
  index= 58  bias= -3.0000E-01  conductance=  2.0941E-04
  index= 59  bias= -2.0000E-01  conductance=  2.1573E-04


*** END SUPREM-3 ***
```

```
**********************************************************
***                      SUPREM-3                      ***
***              Version C, Revision 8834              ***
***   Copyright (C) 1983,1984,1985,1986,1987,1988      ***
***       Technology Modeling Associates, Inc.         ***
***                All Rights Reserved                 ***
**********************************************************

                      1-NOV-89 14:48:34


  Statements input from file section.file


1... title  EMF 1.5 micron nMOS process
 ... +      n-channel source/drain section

2... $  Initialize the silicon substrate
3... initialize  <100>  silicon boron=7e14
 ... +           thickness=1.0  DX=0.01 spaces=100

4... $ increase dry-oxide growth rate
5... ambient O2  <100>  H.LIN.0=0.2e6

6... $ reduce wet-oxide growth rate
7... ambient H2O <100> H.PAR.0=5.8

8... $ stop phosphorus diffusion through oxide
9... impurity phosphor oxide dix.0=0

10... $  INITIAL CLEAN

11... $  INITIAL OXIDE
12... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
13... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
14... diffusion temp=950 time=5 F.O2=1.5
15... print layers

16... $  SILICON NITRIDE DEPOSITION
17... deposition nitride thickness=0.1 temp=800 time=25

18... $  LAYER 1 PHOTO(1) - ISOLATION REGIONS

19... $  SILICON NITRIDE RIE ETCH

20... $  FIELD IMPLANTATION

21... $  LAYER 1 RESIST STRIP

22... $  FIELD OXIDE
23... diffusion temp=950 time=220 inert

24... $  RESIST COAT

25... $  ETCH BACK OF WAFER
```

```
26... $  RESIST STRIP

27... $  ETCH PARASITIC OXIDE

28... $  ETCH PROTECTIVE NITRIDE
29... etch nitride

30... $  ETCH INITIAL OXIDE
31... etch oxide

32... $  LAYER 2 PHOTO(2) - DEPLETION CHANNELS

33... $  DEPLETION IMPLANT

34... $  LAYER 2 RESIST STRIP

35... $  SACRIFICIAL OXIDE
36... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
37... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
38... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15

39... $  SACRIFICIAL OXIDE ETCH
40... etch oxide

41... $  RCA CLEAN

42... $  GATE OXIDE
43... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
44... diffusion temp=950 time=2.2 F.O2=1.5 F.HCL=0.15 F.H2=1.7
45... diffusion temp=950 time=5 F.O2=1.5
46... print layers

47... $  LAYER 3 PHOTO(3) - BURIED CONTACTS

48... $  OXIDE ETCH

49... $  LAYER 3 RESIST STRIP

50... $  THRESHOLD VOLTAGE IMPLANTATION
51... implant boron dose=7e11 energy=25
52... implant boron dose=7e11 energy=140
53... print layers

54... $  RCA CLEAN

55... $  POLYSILICON DEPOSITION
56... deposit polysilicon temperature=600 thickness=0.4

57... $  PHOSPHORUS DEPOSITION
58... diffusion temp=850 time=20 t.final=1000 inert
59... diffusion temp=1000 time=15 phosphorus=1.65e20
60... diffusion temp=1000 time=20 t.final=850 inert
61... print electrical

62... $  PHOSPHORUS DEGLAZE
```

```
63... $  POLYSILICON OXIDATION
64... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
65... diffusion temp=950 time=3 F.O2=1.5 F.HCL=0.15 F.H2=1.7
66... diffusion temp=950 time=5 F.O2=1.5

67... $  LAYER 4 PHOTO(4) - POLYSILICON GATES AND INTERCONNECTS

68... $  POLYOXIDE ETCH
69... etch oxide

70... $  POLYSILICON RIE ETCH
71... etch polysilicon

72... $  LAYER 4 RESIST STRIP
73... print layers

74... $  IMPLANT SOURCE DRAIN REGIONS
75... implant arsenic dose=7.0e15 energy=90

76... $  SOURCE DRAIN ANNEAL
77... diffusion temp=950 time=10  F.O2=2
78... print electrical

79... $  REFLOW PYRO DEPOSITION NO PHOSPHINE

80... $  REFLOW PYRO DEPOSITION

81... $  FIRST REFLOW
82... diffusion temp=1000 time=10 inert

83... $ DENSIFICATION OF REFLOW PYRO
84... diffusion temp=950 time=20  inert

85... $  LAYER 6 PHOTO(5) - DEFINE METAL CONTACTS

86... $  ETCH PYRO OXIDE
87... etch oxide

88... $  LAYER 6 RESIST STRIP

89... $  PHOSPHORUS DEPOSITION - plus phosphorus
90... $diffusion temp=850 time=20 t.final=1000 inert
91... $diffusion temp=1000 time=10 phosphorus=1.65e20
92... $diffusion temp=1000 time=20 t.final=850 inert

93... $  PHOSPHORUS DEPOSITION - heat component only
94... diffusion temp=850 time=20 t.final=1000 inert
95... diffusion temp=1000 time=10 inert
96... diffusion temp=1000 time=20 t.final=850 inert

97... $  PHOSPHORUS DEGLAZE

98... $  PRE-ALUMINIUM EVAPORATION CLEAN

99... $  ALUMINIUM EVAPORATION
```

```
100... $  LAYER 7 PHOTO(6) - DEFINE WINDOWS

101... $  ALUMINIUM ETCH

102... $  LAYER 7 RESIST STRIP

103... $  SINTER
104... print layers electrical

105... $-----------------------------------------------------------------

106... extract name=jn  chemical net x.extract y=0

107... $  plot the resulting chemical concentrations of the net boron
108... $  and phosphorus distributions.
109... plot chemical boron line.type=1 device=4010
   ... +    title="EMF 1.5 um nMOS process - source/drain section"
   ... +    plot.out=section.profile
110... plot chemical arsenic line.type=2 add
111... plot chemical phosphorus line.type=3 add

112... assign name=jn n.value=.01*nint(1e2*&jn)
113... label label="Junction Depth: "&jn" microns" x=0.5

114... label label="boron"       x=0.7  y=7e15
115... label label="arsenic"     x=0.3  y=8e19
116... $label label="phosphorus"  x=0.08 y=6e18

117... $ End of Source-Drain Section Simulation
118... stop

Input line    3
Coefficient data group read
File: S3COF0
Date: 28-AUG-89 16:03:07
Documentation from data file:

SUPREM-3 Revision 8834 coefficient initialization
```

EMF 1.5 micron nMOS process
n-channel source/drain section
INITIAL OXIDE

Material layer information
Input line 15

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0372	0.0100	0.00	398	400	
1	silicon	0.9836	0.0100	0.00	401	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-3.1591E+09	-3.1591E+09	3.1591E+09	3.1591E+09
1	-6.5743E+10	-6.5743E+10	6.5743E+10	6.5743E+10
sum	-6.8902E+10	-6.8902E+10	6.8902E+10	6.8902E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	3.1591E+09	3.1591E+09
1	6.5743E+10	6.5743E+10
sum	6.8902E+10	6.8902E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0372	3.1591E+09	3.1591E+09
1	1	p	0.0000	0.9836	6.5743E+10	6.5743E+10

EMF 1.5 micron nMOS process
n-channel source/drain section
GATE OXIDE

Material layer information
Input line 46

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer no.	Net active	Net chemical	Sum active	Sum chemical
2	-1.3783E+09	-1.3783E+09	1.3783E+09	1.3783E+09
1	-6.0249E+10	-6.0249E+10	6.0249E+10	6.0249E+10
sum	-6.1628E+10	-6.1628E+10	6.1628E+10	6.1628E+10

Integrated Dopant (/cm**2)

layer no.	boron active	boron chemical
2	1.3783E+09	1.3783E+09
1	6.0249E+10	6.0249E+10
sum	6.1628E+10	6.1628E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	1.3783E+09	1.3783E+09
1	1	p	0.0000	0.9549	6.0249E+10	6.0249E+10

EMF 1.5 micron nMOS process
n-channel source/drain section
THRESHOLD VOLTAGE IMPLANTATION

Material layer information
Input line 53

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer no.	Net active	Net chemical	Sum active	Sum chemical
2	-2.0754E+10	-2.0754E+10	2.0754E+10	2.0754E+10
1	-1.4354E+12	-1.4354E+12	1.4354E+12	1.4354E+12
sum	-1.4561E+12	-1.4561E+12	1.4561E+12	1.4561E+12

Integrated Dopant (/cm**2)

layer no.	boron active	boron chemical
2	2.0754E+10	2.0754E+10
1	1.4354E+12	1.4354E+12
sum	1.4561E+12	1.4561E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	2.0754E+10	2.0754E+10
1	1	p	0.0000	0.9549	1.4354E+12	1.4354E+12

EMF 1.5 micron nMOS process
n-channel source/drain section
PHOSPHORUS DEPOSITION

Electrical information
Input line 61

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	1.578E+15	2.1418E-02	4.6689E+01	1.3258E+07	7.5428E-08
1	1	p	5.881E+04	7.5027E-12	1.3328E+11	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	1.112E+12	7.3338E-05	1.3635E+04	1.9513E-01	5.1247E+00

EMF 1.5 micron nMOS process
n-channel source/drain section
LAYER 4 RESIST STRIP

Material layer information
Input line 73

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	8.3071E+11	8.3071E+11	1.0220E+12	1.0220E+12
1	-1.3582E+12	-1.3582E+12	1.3582E+12	1.3582E+12
sum	-5.2745E+11	-5.2745E+11	2.3801E+12	2.3801E+12

Integrated Dopant (/cm**2)

layer	boron		phosphorus	
no.	active	chemical	active	chemical
2	9.5624E+10	9.5624E+10	9.2633E+11	9.2633E+11
1	1.3582E+12	1.3582E+12	0.0000E+00	0.0000E+00
sum	1.4538E+12	1.4538E+12	9.2633E+11	9.2633E+11

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	2	n	0.0000	0.0125	9.2087E+11	9.3180E+11
2	1	p	0.0125	0.0254	9.0158E+10	9.0158E+10
1	1	p	0.0000	0.9549	1.3582E+12	1.3582E+12

EMF 1.5 micron nMOS process
n-channel source/drain section
SOURCE DRAIN ANNEAL

Electrical information
Input line 78

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
1	2	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	3.200E+15	2.0481E-02	4.8826E+01	8.1157E+05	1.2322E-06
1	1	p	1.198E+09	1.6383E-07	6.1038E+06	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	5.940E+11	4.0795E-05	2.4513E+04	0.0000E+00	

EMF 1.5 micron nMOS process
n-channel source/drain section
SINTER

Material layer information
Input line 104

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
1	silicon	0.9463	0.0100	0.00	405	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
1	3.2708E+15	4.2144E+15	3.2734E+15	4.2169E+15
sum	3.2708E+15	4.2144E+15	3.2734E+15	4.2169E+15

Integrated Dopant (/cm**2)

layer	boron		arsenic	
no.	active	chemical	active	chemical
1	1.2742E+12	1.2742E+12	3.2721E+15	4.2156E+15
sum	1.2742E+12	1.2742E+12	3.2721E+15	4.2156E+15

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
1	2	n	0.0000	0.3477	3.2713E+15	4.2164E+15
1	1	p	0.3477	0.9463	4.7384E+11	4.8954E+11

EMF 1.5 micron nMOS process
n-channel source/drain section
SINTER

Electrical information
Input line 104

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
1	2	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	3.271E+15	3.0361E-02	3.2937E+01	1.7044E+06	5.8672E-07
1	1	p	2.126E+09	2.8894E-07	3.4609E+06	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	2.917E+11	2.1314E-05	4.6917E+04	0.0000E+00	

*** END SUPREM-3 ***

```
*********************************************************
***                      SUPREM-3                     ***
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*********************************************************

                      1-NOV-89 15:07:41

  Statements input from file section.file


1... title  EMF 1.5 micron nMOS process
 ... +      n-channel source/drain section

2... $  Initialize the silicon substrate
3... initialize  <100>  silicon boron=7e14
 ... +           thickness=1.0  DX=0.01 spaces=100

4... $ increase dry-oxide growth rate
5... ambient O2  <100>  H.LIN.0=0.2e6

6... $ reduce wet-oxide growth rate
7... ambient H2O <100> H.PAR.0=5.8

8... $ stop phosphorus diffusion through oxide
9... impurity phosphor oxide dix.0=0

10... $  INITIAL CLEAN

11... $  INITIAL OXIDE
12... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
13... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
14... diffusion temp=950 time=5 F.O2=1.5
15... print layers

16... $  SILICON NITRIDE DEPOSITION
17... deposition nitride thickness=0.1 temp=800 time=25

18... $  LAYER 1 PHOTO(1) - ISOLATION REGIONS

19... $  SILICON NITRIDE RIE ETCH

20... $  FIELD IMPLANTATION

21... $  LAYER 1 RESIST STRIP

22... $  FIELD OXIDE
23... diffusion temp=950 time=220 inert

24... $  RESIST COAT

25... $  ETCH BACK OF WAFER
```

```
26... $  RESIST STRIP

27... $  ETCH PARASITIC OXIDE

28... $  ETCH PROTECTIVE NITRIDE
29... etch nitride

30... $  ETCH INITIAL OXIDE
31... etch oxide

32... $  LAYER 2 PHOTO(2) - DEPLETION CHANNELS

33... $  DEPLETION IMPLANT

34... $  LAYER 2 RESIST STRIP

35... $  SACRIFICIAL OXIDE
36... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
37... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
38... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15

39... $  SACRIFICIAL OXIDE ETCH
40... etch oxide

41... $  RCA CLEAN

42... $  GATE OXIDE
43... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
44... diffusion temp=950 time=2.2 F.O2=1.5 F.HCL=0.15 F.H2=1.7
45... diffusion temp=950 time=5 F.O2=1.5
46... print layers

47... $  LAYER 3 PHOTO(3) - BURIED CONTACTS

48... $  OXIDE ETCH

49... $  LAYER 3 RESIST STRIP

50... $  THRESHOLD VOLTAGE IMPLANTATION
51... implant boron dose=7e11 energy=25
52... implant boron dose=7e11 energy=140
53... print layers

54... $  RCA CLEAN

55... $  POLYSILICON DEPOSITION
56... deposit polysilicon temperature=600 thickness=0.4

57... $  PHOSPHORUS DEPOSITION
58... diffusion temp=850 time=20 t.final=1000 inert
59... diffusion temp=1000 time=15 phosphorus=1.65e20
60... diffusion temp=1000 time=20 t.final=850 inert
61... print electrical

62... $  PHOSPHORUS DEGLAZE
```

```
63... $  POLYSILICON OXIDATION
64... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
65... diffusion temp=950 time=3 F.O2=1.5 F.HCL=0.15 F.H2=1.7
66... diffusion temp=950 time=5 F.O2=1.5

67... $  LAYER 4 PHOTO(4) - POLYSILICON GATES AND INTERCONNECTS

68... $  POLYOXIDE ETCH
69... etch oxide

70... $  POLYSILICON RIE ETCH
71... etch polysilicon

72... $  LAYER 4 RESIST STRIP
73... print layers

74... $  IMPLANT SOURCE DRAIN REGIONS
75... implant arsenic dose=7.0e15 energy=90

76... $  SOURCE DRAIN ANNEAL
77... diffusion temp=950 time=10  F.O2=2
78... print electrical

79... $  REFLOW PYRO DEPOSITION NO PHOSPHINE

80... $  REFLOW PYRO DEPOSITION

81... $  FIRST REFLOW
82... diffusion temp=1000 time=10 inert

83... $ DENSIFICATION OF REFLOW PYRO
84... diffusion temp=950 time=20  inert

85... $  LAYER 6 PHOTO(5) - DEFINE METAL CONTACTS

86... $  ETCH PYRO OXIDE
87... etch oxide

88... $  LAYER 6 RESIST STRIP

89... $  PHOSPHORUS DEPOSITION - plus phosphorus
90... diffusion temp=850 time=20 t.final=1000 inert
91... diffusion temp=1000 time=10 phosphorus=1.65e20
92... diffusion temp=1000 time=20 t.final=850 inert

93... $  PHOSPHORUS DEPOSITION - heat component only
94... $diffusion temp=850 time=20 t.final=1000 inert
95... $diffusion temp=1000 time=10 inert
96... $diffusion temp=1000 time=20 t.final=850 inert

97... $  PHOSPHORUS DEGLAZE

98... $  PRE-ALUMINIUM EVAPORATION CLEAN

99... $  ALUMINIUM EVAPORATION
```

```
100... $  LAYER 7 PHOTO(6) - DEFINE WINDOWS

101... $  ALUMINIUM ETCH

102... $  LAYER 7 RESIST STRIP

103... $  SINTER
104... print layers electrical

105... $--------------------------------------------------------------

106... extract name=jn  chemical net x.extract y=0

107... $  plot the resulting chemical concentrations of the net boron
108... $  and phosphorus distributions.
109... plot chemical boron line.type=1 device=4010
   ... +    title="EMF 1.5 um nMOS process - source/drain section"
   ... +    plot.out=section.profile
110... plot chemical arsenic line.type=2 add
111... plot chemical phosphorus line.type=3 add

112... assign name=jn n.value=.01*nint(1e2*&jn)
113... label label="Junction Depth: "&jn" microns" x=0.5

114... label label="boron"       x=0.7  y=7e15
115... label label="arsenic"     x=0.3  y=8e19
116... label label="phosphorus"  x=0.08 y=6e18

117... $ End of Source-Drain Section Simulation
118... stop

Input line    3
Coefficient data group read
File: S3COF0
Date: 28-AUG-89 16:03:07
Documentation from data file:

SUPREM-3 Revision 8834 coefficient initialization
```

EMF 1.5 micron nMOS process
n-channel source/drain section
INITIAL OXIDE

Material layer information
Input line 15

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0372	0.0100	0.00	398	400	
1	silicon	0.9836	0.0100	0.00	401	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-3.1591E+09	-3.1591E+09	3.1591E+09	3.1591E+09
1	-6.5743E+10	-6.5743E+10	6.5743E+10	6.5743E+10
sum	-6.8902E+10	-6.8902E+10	6.8902E+10	6.8902E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	3.1591E+09	3.1591E+09
1	6.5743E+10	6.5743E+10
sum	6.8902E+10	6.8902E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0372	3.1591E+09	3.1591E+09
1	1	p	0.0000	0.9836	6.5743E+10	6.5743E+10

EMF 1.5 micron nMOS process
n-channel source/drain section
GATE OXIDE

Material layer information
Input line 46

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-1.3734E+09	-1.3734E+09	1.3734E+09	1.3734E+09
1	-6.0254E+10	-6.0254E+10	6.0254E+10	6.0254E+10
sum	-6.1628E+10	-6.1628E+10	6.1628E+10	6.1628E+10

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	1.3734E+09	1.3734E+09
1	6.0254E+10	6.0254E+10
sum	6.1628E+10	6.1628E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	1.3734E+09	1.3734E+09
1	1	p	0.0000	0.9549	6.0254E+10	6.0254E+10

EMF 1.5 micron nMOS process
n-channel source/drain section
THRESHOLD VOLTAGE IMPLANTATION

Material layer information
Input line 53

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-2.0749E+10	-2.0749E+10	2.0749E+10	2.0749E+10
1	-1.4354E+12	-1.4354E+12	1.4354E+12	1.4354E+12
sum	-1.4561E+12	-1.4561E+12	1.4561E+12	1.4561E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	2.0749E+10	2.0749E+10
1	1.4354E+12	1.4354E+12
sum	1.4561E+12	1.4561E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0254	2.0749E+10	2.0749E+10
1	1	p	0.0000	0.9549	1.4354E+12	1.4354E+12

EMF 1.5 micron nMOS process
n-channel source/drain section
PHOSPHORUS DEPOSITION

Electrical information
Input line 61

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
3	1	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	1.578E+15	2.1418E-02	4.6689E+01	1.3258E+07	7.5428E-08
1	1	p	5.882E+04	7.5048E-12	1.3325E+11	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
3	1	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	1.112E+12	7.3342E-05	1.3635E+04	1.9511E-01	5.1253E+00

EMF 1.5 micron nMOS process
n-channel source/drain section
LAYER 4 RESIST STRIP

Material layer information
Input line 73

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0254	0.0100	0.00	401	403	
1	silicon	0.9549	0.0100	0.00	404	500	<100>

Integrated Dopant (/cm**2)

layer no.	Net active	Net chemical	Sum active	Sum chemical
2	8.3076E+11	8.3076E+11	1.0219E+12	1.0219E+12
1	-1.3582E+12	-1.3582E+12	1.3582E+12	1.3582E+12
sum	-5.2745E+11	-5.2745E+11	2.3801E+12	2.3801E+12

Integrated Dopant (/cm**2)

layer no.	boron active	boron chemical	phosphorus active	phosphorus chemical
2	9.5577E+10	9.5577E+10	9.2633E+11	9.2633E+11
1	1.3582E+12	1.3582E+12	0.0000E+00	0.0000E+00
sum	1.4538E+12	1.4538E+12	9.2633E+11	9.2633E+11

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	2	n	0.0000	0.0125	9.2087E+11	9.3180E+11
2	1	p	0.0125	0.0254	9.0112E+10	9.0112E+10
1	1	p	0.0000	0.9549	1.3582E+12	1.3582E+12

EMF 1.5 micron nMOS process
n-channel source/drain section
SOURCE DRAIN ANNEAL

Electrical information
Input line 78

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
1	2	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	3.200E+15	2.0482E-02	4.8824E+01	8.1150E+05	1.2323E-06
1	1	p	1.198E+09	1.6381E-07	6.1046E+06	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	5.940E+11	4.0796E-05	2.4512E+04	0.0000E+00	

EMF 1.5 micron nMOS process
n-channel source/drain section
SINTER

Material layer information
Input line 104

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
1	silicon	0.9463	0.0100	0.00	405	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
1	3.8726E+15	4.7928E+15	3.8752E+15	4.7953E+15
sum	3.8726E+15	4.7928E+15	3.8752E+15	4.7953E+15

Integrated Dopant (/cm**2)

layer	phosphorus		arsenic	
no.	active	chemical	active	chemical
1	6.1006E+14	6.1851E+14	3.2638E+15	4.1755E+15
sum	6.1006E+14	6.1851E+14	3.2638E+15	4.1755E+15

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
1	1.2737E+12	1.2737E+12
sum	1.2737E+12	1.2737E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
1	2	n	0.0000	0.3911	3.8730E+15	4.7949E+15
1	1	p	0.3911	0.9463	3.8942E+11	4.2243E+11

EMF 1.5 micron nMOS process
n-channel source/drain section
SINTER

Electrical information
Input line 104

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
1	2	n		0.0000E+00	0.0000E+00
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	3.873E+15	3.4461E-02	2.9018E+01	2.1221E+05	4.7124E-06
1	1	p	3.522E+08	4.5238E-08	2.2105E+07	0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	2	n	0.000E+00	0.0000E+00		0.0000E+00	
1	1	p	2.496E+11	1.8392E-05	5.4372E+04	0.0000E+00	

*** END SUPREM-3 ***

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*************************************************************
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*************************************************************

                        1-NOV-89 14:57:08


  Statements input from file section.file


1... title  EMF 1.5 micron nMOS process
 ... +      n-channel field section

2... $  Initialize the silicon substrate
3... initialize  <100>  silicon boron=7e14
 ... +           thickness=1.25  DX=0.001 spaces=100

4... $ calculate ionization impurity concentrations
5... material silicon semiconductor ionizati

6... $ increase dry-oxide growth rate
7... ambient O2  <100>  H.LIN.0=0.2e6

8... $ reduce wet-oxide growth rate
9... ambient H2O <100> H.PAR.0=5.8

10... $ stop phosphorus diffusion through oxide
11... impurity phosphor oxide dix.0=0

12... $  INITIAL CLEAN

13... $  INITIAL OXIDE
14... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
15... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
16... diffusion temp=950 time=5 F.O2=1.5
17... print layers

18... $  SILICON NITRIDE DEPOSITION
19... deposition nitride thickness=0.1 temp=800 time=25

20... $  LAYER 1 PHOTO(1) - ISOLATION REGIONS

21... $  SILICON NITRIDE RIE ETCH
22... etch nitride

23... $  FIELD IMPLANTATION
24... implant boron dose=7e12 energy=70

25... $  LAYER 1 RESIST STRIP

26... $  FIELD OXIDE
```

```
27... diffusion temp=950 time=5     F.O2=1.22 F.HCL=0.1
28... diffusion temp=950 time=30    F.O2=1.22 F.H2=2 F.HCL=0.1
29... diffusion temp=950 time=180   F.O2=1.22 F.H2=2
30... diffusion temp=950 time=5     F.O2=1.22
31... print layers

32... $  RESIST COAT

33... $  ETCH BACK OF WAFER

34... $  RESIST STRIP

35... $  ETCH PARASITIC OXIDE

36... $  ETCH PROTECTIVE NITRIDE

37... $  ETCH INITIAL OXIDE
38... etch oxide thickness=0.038

39... $  LAYER 2 PHOTO(2) - DEPLETION CHANNELS

40... $  DEPLETION IMPLANT

41... $  LAYER 2 RESIST STRIP

42... $  SACRIFICIAL OXIDE
43... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
44... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15 F.H2=1.7
45... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
46... print layers

47... $  SACRIFICIAL OXIDE ETCH
48... etch oxide thickness=0.04

49... $  RCA CLEAN

50... $  GATE OXIDE
51... diffusion temp=950 time=5 F.O2=1.5 F.HCL=0.15
52... diffusion temp=950 time=2.2 F.O2=1.5 F.HCL=0.15 F.H2=1.7
53... diffusion temp=950 time=5 F.O2=1.5
54... print layers

55... $  LAYER 3 PHOTO(3) - BURIED CONTACTS

56... $  OXIDE ETCH

57... $  LAYER 3 RESIST STRIP

58... $  THRESHOLD VOLTAGE IMPLANTATION

59... $  RCA CLEAN

60... $  POLYSILICON DEPOSITION

61... $  PHOSPHORUS DEPOSITION
62... diffusion temp=850 time=20 t.rate=7.5 inert
```

```
63... diffusion temp=1000 time=15 inert
64... diffusion temp=1000 time=20 t.rate=-7.5 inert

65... $  PHOSPHORUS DEGLAZE

66... $  POLYSILICON OXIDATION
67... diffusion temp=950 time=13 inert

68... $  LAYER 4 PHOTO(4) - POLYSILICON GATES AND INTERCONNECTS

69... $  POLYOXIDE ETCH

70... $  POLYSILICON RIE ETCH

71... $  LAYER 4 RESIST STRIP

72... $  IMPLANT SOURCE DRAIN REGIONS

73... $  SOURCE DRAIN ANNEAL
74... diffusion temp=950 time=10 inert

75... $  REFLOW PYRO DEPOSITION NO PHOSPHINE

76... $  REFLOW PYRO DEPOSITION

77... $  FIRST REFLOW
78... diffusion temp=1000 time=10 inert

79... $ DENSIFICATION OF REFLOW PYRO
80... diffusion temp=950 time=20 inert

81... $  LAYER 6 PHOTO(5) - DEFINE METAL CONTACTS

82... $  ETCH PYRO OXIDE

83... $  LAYER 6 RESIST STRIP

84... $  PHOSPHORUS DEPOSITION

85... $  PHOSPHORUS DEGLAZE

86... $  PRE-ALUMINIUM EVAPORATION CLEAN

87... $  ALUMINIUM EVAPORATION

88... $  LAYER 7 PHOTO(6) - DEFINE WINDOWS

89... $  ALUMINIUM ETCH

90... $  LAYER 7 RESIST STRIP

91... $  SINTER
92... print layers electric

93... $-------------------------------------------------------------
```

```
94... extract name=fox thickness layer=2

95... $  plot the resulting chemical concentrations of the net boron
96... plot chemical boron line.type=1 device=4010
  ... +    title="EMF 1.5 micron nMOS process - field section"
  ... +    plot.out=section.profile

97... assign name=fox n.value=1*nint(1e4*&fox)
98... label label="Field Oxide Thickness: "&fox" A" x=0.8

99... label label="boron"  x=1.1  y=3e16

100... $ End of Field Section Simulation
101... stop

Input line    3
Coefficient data group read
File: S3COF0
Date: 28-AUG-89 16:03:07
Documentation from data file:

SUPREM-3 Revision 8834 coefficient initialization
```

EMF 1.5 micron nMOS process
n-channel field section
INITIAL OXIDE

Material layer information
Input line 17

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.0372	0.0100	0.00	398	407	
1	silicon	1.2336	0.0010	0.00	408	500	<100>

Integrated Dopant (/cm**2)

layer no.	Net active	Net chemical	Sum active	Sum chemical
2	-3.9290E+09	-3.9290E+09	3.9290E+09	3.9290E+09
1	-8.3408E+10	-8.3408E+10	8.3408E+10	8.3408E+10
sum	-8.7337E+10	-8.7337E+10	8.7337E+10	8.7337E+10

Integrated Dopant (/cm**2)

layer no.	boron active	boron chemical
2	3.9290E+09	3.9290E+09
1	8.3408E+10	8.3408E+10
sum	8.7337E+10	8.7337E+10

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.0372	3.9290E+09	3.9290E+09
1	1	p	0.0000	1.2336	8.3408E+10	8.3408E+10

EMF 1.5 micron nMOS process
n-channel field section
FIELD OXIDE

Material layer information
Input line 31

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.6043	0.0100	0.00	398	443	
1	silicon	0.9841	0.0010	0.00	444	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-5.1833E+12	-5.1833E+12	5.1833E+12	5.1833E+12
1	-1.8896E+12	-1.8896E+12	1.8896E+12	1.8896E+12
sum	-7.0729E+12	-7.0729E+12	7.0729E+12	7.0729E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	5.1833E+12	5.1833E+12
1	1.8896E+12	1.8896E+12
sum	7.0729E+12	7.0729E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.6043	5.1833E+12	5.1833E+12
1	1	p	0.0000	0.9841	1.8896E+12	1.8896E+12

EMF 1.5 micron nMOS process
n-channel field section
SACRIFICIAL OXIDE

Material layer information
Input line 46

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.5758	0.0100	0.00	407	443	
1	silicon	0.9799	0.0010	0.00	444	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-5.1570E+12	-5.1570E+12	5.1570E+12	5.1570E+12
1	-1.8497E+12	-1.8497E+12	1.8497E+12	1.8497E+12
sum	-7.0067E+12	-7.0067E+12	7.0067E+12	7.0067E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	5.1570E+12	5.1570E+12
1	1.8497E+12	1.8497E+12
sum	7.0067E+12	7.0067E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.5758	5.1570E+12	5.1570E+12
1	1	p	0.0000	0.9799	1.8497E+12	1.8497E+12

EMF 1.5 micron nMOS process
n-channel field section
GATE OXIDE

Material layer information
Input line 54

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.5407	0.0100	0.00	412	443	
1	silicon	0.9778	0.0010	0.00	444	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-4.7019E+12	-4.7019E+12	4.7019E+12	4.7019E+12
1	-1.8273E+12	-1.8273E+12	1.8273E+12	1.8273E+12
sum	-6.5292E+12	-6.5292E+12	6.5292E+12	6.5292E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	4.7019E+12	4.7019E+12
1	1.8273E+12	1.8273E+12
sum	6.5292E+12	6.5292E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.5407	4.7019E+12	4.7019E+12
1	1	p	0.0000	0.9778	1.8273E+12	1.8273E+12

EMF 1.5 micron nMOS process
n-channel field section
SINTER

Material layer information
Input line 92

layer no.	material	thickness (um)	dx (um)	xdx (um)	top node	bottom node	orientation or grain size
2	oxide	0.5407	0.0100	0.00	412	443	
1	silicon	0.9778	0.0010	0.00	444	500	<100>

Integrated Dopant (/cm**2)

layer	Net		Sum	
no.	active	chemical	active	chemical
2	-4.7140E+12	-4.7140E+12	4.7140E+12	4.7140E+12
1	-1.8115E+12	-1.8115E+12	1.8115E+12	1.8115E+12
sum	-6.5255E+12	-6.5255E+12	6.5255E+12	6.5255E+12

Integrated Dopant (/cm**2)

layer	boron	
no.	active	chemical
2	4.7140E+12	4.7140E+12
1	1.8115E+12	1.8115E+12
sum	6.5255E+12	6.5255E+12

Boundary Locations and Integrated Dopant Concentrations for Each Diffused Region

layer no.	region no.	type	top depth (um)	bottom depth (um)	net active Qd (/cm**2)	sum chemical Qd (/cm**2)
2	1	p	0.0000	0.5407	4.7140E+12	4.7140E+12
1	1	p	0.0000	0.9778	1.8115E+12	1.8115E+12

EMF 1.5 micron nMOS process
n-channel field section
SINTER

Electrical information
Input line 92

Bias step 1

layer no.	region no.	type	Conductor Bias (volts)	Electron Bias (volts)	Hole Bias (volts)
1	1	p		0.0000E+00	0.0000E+00

Electron Charge, Conductance, and Resistance

layer no.	region no.	type	Electron Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	1	p	0.000E+00	0.0000E+00		0.0000E+00	

Hole Charge, Conductance, and Resistance

layer no.	region no.	type	Hole Charge (/cm**2)	Sheet Conductance (1/(ohm/sq))	Sheet Resistance (ohm/sq)	Vertical Conductance (mho/cm**2)	Vertical Resistance (ohm-cm**2)
1	1	p	2.471E+12	1.6119E-04	6.2040E+03	4.4543E+03	2.2450E-04

*** END SUPREM-3 ***

Appendix D

Data Definitions for COMETS Recipe Management

Modifications to the COMETS database definition were necessary in implementing the Recipe Management (RCP) module. These modifications are listed in this appendix.

Additions were made to four Database Definition Language (DDL) files:

1. MANYSCHEM.DDL
2. MANYSTOR.DDL
3. MANYSUB.DDL
4. MANRPTSUB.DDL

The database definition used by the COMETS programs was also modified.

5. CMTSCH

```
*****************************************************************
*     NEW RECORDS AND SETS ADDED TO MANYSCHEM.DDL
*     FOR THE RCP MODULE
*     Angus J. MacDonald  August 1989
*****************************************************************


*****************************************************************
*     LINK RECORD USED FOR ASSOCIATING SPEC VERSIONS AND RECIPES
*     ALSO PROVIDES TIE IN POINT FOR RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCVRC_REC WITHIN SPCVER_AREA

     ITEM IS SPCVRC_SPEC_ID                    TYPE IS CHARACTER 12
     ITEM IS SPCVRC_SPEC_VERSION               TYPE IS CHARACTER 6
     ITEM IS SPCVRC_RECIPE_NAME                TYPE IS CHARACTER 12


SET IS SPCVER_RECIPE_SET
     OWNER IS SPCVER_REC
     MEMBER IS SPCVRC_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS NEXT

SET IS SPCVRC_RECIPE_OVERRIDE_SET
     OWNER IS SPCVRC_REC
     MEMBER IS SPCROV_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS LAST


*****************************************************************
*    RECIPE RECORD WHICH IS ASSOCIATED WITH A SPEC VERSION
*    OR IS USED AS AN OVERRIDE FOR SAME
*****************************************************************
RECORD NAME IS SPCRCP_REC WITHIN SPCVER_AREA

* GROUP NAME IS SPCRCP_KEY
     ITEM IS SPCRCP_FACILITY                   TYPE IS CHARACTER 6
     ITEM IS SPCRCP_RECIPE_NAME                TYPE IS CHARACTER 12
* ENDGROUP SPCRCP_KEY

     ITEM IS SPCRCP_RECIPE_TYPE                TYPE IS CHARACTER 12

     ITEM IS SPCRCP_RECIPE_DESCRIPTION         TYPE IS CHARACTER 35

     ITEM IS SPCRCP_NUMBER_OF_INGREDIENTS      TYPE IS CHARACTER 6

*   GROUP NAME IS SPCRCP_CREATION_DATE_TIME
     ITEM IS SPCRCP_CREATION_DATE              TYPE IS SIGNED LONGWORD
     ITEM IS SPCRCP_CREATION_TIME              TYPE IS SIGNED LONGWORD
*   ENDGROUP SPCRCP_CREATION_DATE_TIME
```

```
*   GROUP NAME IS SPCRCP_LAST_MODIFIED_DATE_TIME
     ITEM IS SPCRCP_LAST_MODIFIED_DATE        TYPE IS SIGNED LONGWORD
     ITEM IS SPCRCP_LAST_MODIFIED_TIME        TYPE IS SIGNED LONGWORD
*   ENDGROUP SPCRCP_LAST_MODIFIED_DATE_TIME

*   GROUP NAME IS SPCRCP_TERMINATED_DATE_TIME
     ITEM IS SPCRCP_TERMINATED_DATE           TYPE IS SIGNED LONGWORD
     ITEM IS SPCRCP_TERMINATED_TIME           TYPE IS SIGNED LONGWORD
*   ENDGROUP SPCRCP_TERMINATED_DATE_TIME

*   GROUP NAME IS SPCRCP_RESPONSIBILITY_RESTS_ON
     ITEM IS SPCRCP_RECIPE_CREATED_BY         TYPE IS CHARACTER 12
     ITEM IS SPCRCP_RECIPE_MODIFIED_BY        TYPE IS CHARACTER 12
     ITEM IS SPCRCP_RECIPE_TERMINATED_BY      TYPE IS CHARACTER 12
*   ENDGROUP SPCRCP_RESPONSIBILITY_RESTS_ON


SET IS SPCRCP_CALC
     OWNER IS SYSTEM
     MEMBER IS SPCRCP_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED

SET IS SPCRCP_INDEX
     OWNER IS SYSTEM
     MEMBER IS SPCRCP_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS SORTED ASCENDING SPCRCP_FACILITY
                               SPCRCP_RECIPE_NAME
     DUPLICATES ARE NOT ALLOWED

SET IS SPCRCP_SPEC_VERSION_INDEX
     OWNER IS SPCRCP_REC
     MEMBER IS SPCVRC_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS SORTED ASCENDING  SPCVRC_SPEC_ID
                     DESCENDING SPCVRC_SPEC_VERSION
     DUPLICATES ARE NOT ALLOWED

SET IS SPCRCP_RECIPE_OVERRIDE_SET
     OWNER IS SPCRCP_REC
     MEMBER IS SPCROV_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS LAST

SET IS SPCRCP_INGREDIENT_SET
     OWNER IS SPCRCP_REC
     MEMBER IS SPCING_REC
     INSERTION IS AUTOMATIC
     RETENTION IS FIXED
     ORDER IS NEXT
```

```
SET IS SPCRCP_INGREDIENT_INDEX
    OWNER IS SPCRCP_REC
    MEMBER IS SPCING_REC
    INSERTION IS AUTOMATIC
    RETENTION IS FIXED
    ORDER IS SORTED ASCENDING SPCING_PARAMETER
    DUPLICATES ARE NOT ALLOWED


*****************************************************************
*    INGREDIENTS FOR A RECIPE
*****************************************************************
RECORD NAME IS SPCING_REC WITHIN SPCVER_AREA

* GROUP NAME IS SPCING_INGREDIENT_DATA
    ITEM IS SPCING_PARAMETER                TYPE IS CHARACTER 20
    ITEM IS SPCING_VALUE                    TYPE IS CHARACTER 20
    ITEM IS SPCING_UNIT                     TYPE IS CHARACTER 10
    ITEM IS SPCING_DISPLAY_FLAG             TYPE IS CHARACTER 1
* ENDGROUP SPCING_INGREDIENT_DATA


*****************************************************************
*    RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCROV_REC WITHIN SPCVER_AREA

* GROUP NAME IS SPCROV_KEY
    ITEM IS SPCROV_RECIPE_NAME              TYPE IS CHARACTER 12
    ITEM IS SPCROV_OVERRIDE_NAME            TYPE IS CHARACTER 12
* ENDGROUP SPCROV_KEY

    ITEM IS SPCROV_SPEC_ID                  TYPE IS CHARACTER 12

    ITEM IS SPCROV_SPEC_VERSION             TYPE IS CHARACTER 6

*  GROUP NAME IS SPCROV_CREATION_DATE_TIME
    ITEM IS SPCROV_CREATION_DATE            TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_CREATION_TIME            TYPE IS SIGNED LONGWORD
*  ENDGROUP SPCROV_CREATION_DATE_TIME

*  GROUP NAME IS SPCROV_TERMINATED_DATE_TIME
    ITEM IS SPCROV_TERMINATED_DATE          TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_TERMINATED_TIME          TYPE IS SIGNED LONGWORD
*  ENDGROUP SPCROV_TERMINATED_DATE_TIME

*  GROUP NAME IS SPCROV_RESPONSIBILITY_RESTS_ON
    ITEM IS SPCROV_RECIPE_CREATED_BY        TYPE IS CHARACTER 12
    ITEM IS SPCROV_RECIPE_TERMINATED_BY     TYPE IS CHARACTER 12
*  ENDGROUP SPCROV_RESPONSIBILITY_RESTS_ON
```

```
*  GROUP NAME IS SPCROV_TYPE_OF_OVERRIDE
     ITEM IS SPCROV_LOT_NUMBER                TYPE IS CHARACTER 11
     ITEM IS SPCROV_PRODUCT                   TYPE IS CHARACTER 25
     ITEM IS SPCROV_PRODUCT_GROUP             TYPE IS CHARACTER 12
     ITEM IS SPCROV_OWNER                     TYPE IS CHARACTER 12
     ITEM IS SPCROV_CREATE_CODE               TYPE IS CHARACTER 6
     ITEM IS SPCROV_PERIOD_FROM               TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_PERIOD_TO                 TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_MACHINE_ID_OR_ENTITY      TYPE IS CHARACTER 12
     ITEM IS SPCROV_EVENT                     TYPE IS CHARACTER 12
*  ENDGROUP SPCROV_TYPE_OF_OVERRIDE
```

```
*************************************************************************
*    NEW RECORDS ADDED TO MANYSTOR.DDL FOR THE RCP MODULE
*    Angus J. MacDonald  August 1989
*************************************************************************


*************************************************************************
*     LINK RECORD USED FOR ASSOCIATING SPEC VERSIONS AND RECIPES
*     ALSO PROVIDES TIE IN POINT FOR RECIPE OVERRIDES
*************************************************************************
RECORD NAME IS SPCVRC_REC
       PLACEMENT IS CLUSTERED VIA SPCVER_RECIPE_SET

    ITEM IS SPCVRC_SPEC_ID                    TYPE IS CHARACTER 12
    ITEM IS SPCVRC_SPEC_VERSION               TYPE IS CHARACTER 6
    ITEM IS SPCVRC_RECIPE_NAME                TYPE IS CHARACTER 12


*************************************************************************
*     RECIPE RECORD WHICH IS ASSOCIATED WITH A SPEC VERSION
*     OR IS USED AS AN OVERRIDE FOR SAME
*************************************************************************
RECORD NAME IS SPCRCP_REC
       PLACEMENT IS CLUSTERED VIA SPCRCP_CALC

* GROUP NAME IS SPCRCP_KEY
    ITEM IS SPCRCP_FACILITY                   TYPE IS CHARACTER 6
    ITEM IS SPCRCP_RECIPE_NAME                TYPE IS CHARACTER 12
* ENDGROUP SPCRCP_KEY

    ITEM IS SPCRCP_RECIPE_TYPE                TYPE IS CHARACTER 12

    ITEM IS SPCRCP_RECIPE_DESCRIPTION         TYPE IS CHARACTER 35

    ITEM IS SPCRCP_NUMBER_OF_INGREDIENTS      TYPE IS CHARACTER 6

*  GROUP NAME IS SPCRCP_CREATION_DATE_TIME
    ITEM IS SPCRCP_CREATION_DATE              TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_CREATION_TIME              TYPE IS SIGNED LONGWORD
*  ENDGROUP SPCRCP_CREATION_DATE_TIME

*  GROUP NAME IS SPCRCP_LAST_MODIFIED_DATE_TIME
    ITEM IS SPCRCP_LAST_MODIFIED_DATE         TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_LAST_MODIFIED_TIME         TYPE IS SIGNED LONGWORD
*  ENDGROUP SPCRCP_LAST_MODIFIED_DATE_TIME

*  GROUP NAME IS SPCRCP_TERMINATED_DATE_TIME
    ITEM IS SPCRCP_TERMINATED_DATE            TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_TERMINATED_TIME            TYPE IS SIGNED LONGWORD
*  ENDGROUP SPCRCP_TERMINATED_DATE_TIME
```

```
*   GROUP NAME IS SPCRCP_RESPONSIBILITY_RESTS_ON
     ITEM IS SPCRCP_RECIPE_CREATED_BY          TYPE IS CHARACTER 12
     ITEM IS SPCRCP_RECIPE_MODIFIED_BY         TYPE IS CHARACTER 12
     ITEM IS SPCRCP_RECIPE_TERMINATED_BY       TYPE IS CHARACTER 12
*   ENDGROUP SPCRCP_RESPONSIBILITY_RESTS_ON


*****************************************************************
*     INGREDIENTS FOR A RECIPE
*****************************************************************
RECORD NAME IS SPCING_REC
        PLACEMENT IS CLUSTERED VIA SPCRCP_INGREDIENT_SET

* GROUP NAME IS SPCING_INGREDIENT_DATA
     ITEM IS SPCING_PARAMETER                  TYPE IS CHARACTER 20
     ITEM IS SPCING_VALUE                      TYPE IS CHARACTER 20
     ITEM IS SPCING_UNIT                       TYPE IS CHARACTER 10
     ITEM IS SPCING_DISPLAY_FLAG               TYPE IS CHARACTER 1
* ENDGROUP SPCING_INGREDIENT_DATA


*****************************************************************
*     RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCROV_REC
        PLACEMENT IS CLUSTERED VIA SPCVRC_RECIPE_OVERRIDE_SET

* GROUP NAME IS SPCROV_KEY
     ITEM IS SPCROV_RECIPE_NAME                TYPE IS CHARACTER 12
     ITEM IS SPCROV_OVERRIDE_NAME              TYPE IS CHARACTER 12
* ENDGROUP SPCROV_KEY

     ITEM IS SPCROV_SPEC_ID                    TYPE IS CHARACTER 12

     ITEM IS SPCROV_SPEC_VERSION               TYPE IS CHARACTER 6

*   GROUP NAME IS SPCROV_CREATION_DATE_TIME
     ITEM IS SPCROV_CREATION_DATE              TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_CREATION_TIME              TYPE IS SIGNED LONGWORD
*   ENDGROUP SPCROV_CREATION_DATE_TIME

*   GROUP NAME IS SPCROV_TERMINATED_DATE_TIME
     ITEM IS SPCROV_TERMINATED_DATE            TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_TERMINATED_TIME            TYPE IS SIGNED LONGWORD
*   ENDGROUP SPCROV_TERMINATED_DATE_TIME

*   GROUP NAME IS SPCROV_RESPONSIBILITY_RESTS_ON
     ITEM IS SPCROV_RECIPE_CREATED_BY          TYPE IS CHARACTER 12
     ITEM IS SPCROV_RECIPE_TERMINATED_BY       TYPE IS CHARACTER 12
*   ENDGROUP SPCROV_RESPONSIBILITY_RESTS_ON
```

```
*   GROUP NAME IS SPCROV_TYPE_OF_OVERRIDE
     ITEM IS SPCROV_LOT_NUMBER                  TYPE IS CHARACTER 11
     ITEM IS SPCROV_PRODUCT                     TYPE IS CHARACTER 25
     ITEM IS SPCROV_PRODUCT_GROUP               TYPE IS CHARACTER 12
     ITEM IS SPCROV_OWNER                       TYPE IS CHARACTER 12
     ITEM IS SPCROV_CREATE_CODE                 TYPE IS CHARACTER 6
     ITEM IS SPCROV_PERIOD_FROM                 TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_PERIOD_TO                   TYPE IS SIGNED LONGWORD
     ITEM IS SPCROV_MACHINE_ID_OR_ENTITY        TYPE IS CHARACTER 12
     ITEM IS SPCROV_EVENT                       TYPE IS CHARACTER 12
*   ENDGROUP SPCROV_TYPE_OF_OVERRIDE


*****************************************************************
*     NEW SETS ADDED TO MANYSTOR.DDL FOR THE RCP MODULE
*****************************************************************

SET IS SPCVER_RECIPE_SET
     MODE IS CHAIN

SET IS SPCVRC_RECIPE_OVERRIDE_SET
     MODE IS CHAIN

SET IS SPCRCP_CALC
     MODE IS CALC
          MEMBER IS SPCRCP_REC
               KEY IS SPCRCP_FACILITY
                      SPCRCP_RECIPE_NAME

SET IS SPCRCP_INDEX
     MODE IS INDEX
          NODE SIZE IS 200 BYTES

SET IS SPCRCP_SPEC_VERSION_INDEX
     MODE IS INDEX
          NODE SIZE IS 200 BYTES

SET IS SPCRCP_RECIPE_OVERRIDE_SET
     MODE IS CHAIN

SET IS SPCRCP_INGREDIENT_SET
     MODE IS CHAIN

SET IS SPCRCP_INGREDIENT_INDEX
     MODE IS INDEX
          NODE SIZE IS 200 BYTES
```

```
*****************************************************************
*    NEW RECORDS AND SETS ADDED TO MANYSUB.DDL FOR THE RCP MODULE
*    Angus J. MacDonald  August 1989
*****************************************************************


*****************************************************************
*    LINK RECORD USED FOR ASSOCIATING SPEC VERSIONS AND RECIPES
*    ALSO PROVIDES TIE IN POINT FOR RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCVRC_REC

    ITEM IS SPCVRC_SPEC_ID                  TYPE IS CHARACTER 12
    ITEM IS SPCVRC_SPEC_VERSION             TYPE IS CHARACTER 6
    ITEM IS SPCVRC_RECIPE_NAME              TYPE IS CHARACTER 12


SET IS SPCVER_RECIPE_SET
SET IS SPCVRC_RECIPE_OVERRIDE_SET


*****************************************************************
*   RECIPE RECORD WHICH IS ASSOCIATED WITH A SPEC VERSION
*   OR IS USED AS AN OVERRIDE FOR SAME
*****************************************************************
RECORD NAME IS SPCRCP_REC

 GROUP NAME IS SPCRCP_KEY
    ITEM IS SPCRCP_FACILITY                 TYPE IS CHARACTER 6
    ITEM IS SPCRCP_RECIPE_NAME              TYPE IS CHARACTER 12
 ENDGROUP SPCRCP_KEY

    ITEM IS SPCRCP_RECIPE_TYPE              TYPE IS CHARACTER 12

    ITEM IS SPCRCP_RECIPE_DESCRIPTION       TYPE IS CHARACTER 35

    ITEM IS SPCRCP_NUMBER_OF_INGREDIENTS    TYPE IS CHARACTER 6

  GROUP NAME IS SPCRCP_CREATION_DATE_TIME
    ITEM IS SPCRCP_CREATION_DATE            TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_CREATION_TIME            TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_CREATION_DATE_TIME

  GROUP NAME IS SPCRCP_LAST_MODIFIED_DATE_TIME
    ITEM IS SPCRCP_LAST_MODIFIED_DATE       TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_LAST_MODIFIED_TIME       TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_LAST_MODIFIED_DATE_TIME

  GROUP NAME IS SPCRCP_TERMINATED_DATE_TIME
    ITEM IS SPCRCP_TERMINATED_DATE          TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_TERMINATED_TIME          TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_TERMINATED_DATE_TIME
```

```
  GROUP NAME IS SPCRCP_RESPONSIBILITY_RESTS_ON
    ITEM IS SPCRCP_RECIPE_CREATED_BY         TYPE IS CHARACTER 12
    ITEM IS SPCRCP_RECIPE_MODIFIED_BY        TYPE IS CHARACTER 12
    ITEM IS SPCRCP_RECIPE_TERMINATED_BY      TYPE IS CHARACTER 12
  ENDGROUP SPCRCP_RESPONSIBILITY_RESTS_ON


SET IS SPCRCP_CALC
SET IS SPCRCP_INDEX
SET IS SPCRCP_SPEC_VERSION_INDEX
SET IS SPCRCP_RECIPE_OVERRIDE_SET
SET IS SPCRCP_INGREDIENT_SET
SET IS SPCRCP_INGREDIENT_INDEX


*****************************************************************
*     INGREDIENTS FOR A RECIPE
*****************************************************************
RECORD NAME IS SPCING_REC

 GROUP NAME IS SPCING_INGREDIENT_DATA
    ITEM IS SPCING_PARAMETER                 TYPE IS CHARACTER 20
    ITEM IS SPCING_VALUE                     TYPE IS CHARACTER 20
    ITEM IS SPCING_UNIT                      TYPE IS CHARACTER 10
    ITEM IS SPCING_DISPLAY_FLAG              TYPE IS CHARACTER 1
 ENDGROUP SPCING_INGREDIENT_DATA


*****************************************************************
*     RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCROV_REC

 GROUP NAME IS SPCROV_KEY
    ITEM IS SPCROV_RECIPE_NAME               TYPE IS CHARACTER 12
    ITEM IS SPCROV_OVERRIDE_NAME             TYPE IS CHARACTER 12
 ENDGROUP SPCROV_KEY

    ITEM IS SPCROV_SPEC_ID                   TYPE IS CHARACTER 12

    ITEM IS SPCROV_SPEC_VERSION              TYPE IS CHARACTER 6

  GROUP NAME IS SPCROV_CREATION_DATE_TIME
    ITEM IS SPCROV_CREATION_DATE             TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_CREATION_TIME             TYPE IS SIGNED LONGWORD
  ENDGROUP SPCROV_CREATION_DATE_TIME

  GROUP NAME IS SPCROV_TERMINATED_DATE_TIME
    ITEM IS SPCROV_TERMINATED_DATE           TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_TERMINATED_TIME           TYPE IS SIGNED LONGWORD
  ENDGROUP SPCROV_TERMINATED_DATE_TIME

  GROUP NAME IS SPCROV_RESPONSIBILITY_RESTS_ON
    ITEM IS SPCROV_RECIPE_CREATED_BY         TYPE IS CHARACTER 12
    ITEM IS SPCROV_RECIPE_TERMINATED_BY      TYPE IS CHARACTER 12
  ENDGROUP SPCROV_RESPONSIBILITY_RESTS_ON
```

```
GROUP NAME IS SPCROV_TYPE_OF_OVERRIDE
  ITEM IS SPCROV_LOT_NUMBER                TYPE IS CHARACTER 11
  ITEM IS SPCROV_PRODUCT                   TYPE IS CHARACTER 25
  ITEM IS SPCROV_PRODUCT_GROUP             TYPE IS CHARACTER 12
  ITEM IS SPCROV_OWNER                     TYPE IS CHARACTER 12
  ITEM IS SPCROV_CREATE_CODE               TYPE IS CHARACTER 6
  ITEM IS SPCROV_PERIOD_FROM               TYPE IS SIGNED LONGWORD
  ITEM IS SPCROV_PERIOD_TO                 TYPE IS SIGNED LONGWORD
  ITEM IS SPCROV_MACHINE_ID_OR_ENTITY      TYPE IS CHARACTER 12
  ITEM IS SPCROV_EVENT                     TYPE IS CHARACTER 12
ENDGROUP SPCROV_TYPE_OF_OVERRIDE
```

```
*********************************************************************
*    NEW RECORDS AND SETS ADDED TO MANRPTSUB.DDL FOR THE RCP MODULE
*    Angus J. MacDonald  August 1989
*********************************************************************


*********************************************************************
*    LINK RECORD USED FOR ASSOCIATING SPEC VERSIONS AND RECIPES
*    ALSO PROVIDES TIE IN POINT FOR RECIPE OVERRIDES
*********************************************************************
RECORD NAME IS SPCVRC_REC

    ITEM IS SPCVRC_SPEC_ID                  TYPE IS CHARACTER 12
    ITEM IS SPCVRC_SPEC_VERSION             TYPE IS CHARACTER 6
    ITEM IS SPCVRC_RECIPE_NAME              TYPE IS CHARACTER 12


SET IS SPCVER_RECIPE_SET
SET IS SPCVRC_RECIPE_OVERRIDE_SET


*********************************************************************
*   RECIPE RECORD WHICH IS ASSOCIATED WITH A SPEC VERSION
*   OR IS USED AS AN OVERRIDE FOR SAME
*********************************************************************
RECORD NAME IS SPCRCP_REC

 GROUP NAME IS SPCRCP_KEY
    ITEM IS SPCRCP_FACILITY                 TYPE IS CHARACTER 6
    ITEM IS SPCRCP_RECIPE_NAME              TYPE IS CHARACTER 12
 ENDGROUP SPCRCP_KEY

    ITEM IS SPCRCP_RECIPE_TYPE              TYPE IS CHARACTER 12

    ITEM IS SPCRCP_RECIPE_DESCRIPTION       TYPE IS CHARACTER 35

    ITEM IS SPCRCP_NUMBER_OF_INGREDIENTS    TYPE IS CHARACTER 6

  GROUP NAME IS SPCRCP_CREATION_DATE_TIME
    ITEM IS SPCRCP_CREATION_DATE            TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_CREATION_TIME            TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_CREATION_DATE_TIME

  GROUP NAME IS SPCRCP_LAST_MODIFIED_DATE_TIME
    ITEM IS SPCRCP_LAST_MODIFIED_DATE       TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_LAST_MODIFIED_TIME       TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_LAST_MODIFIED_DATE_TIME

  GROUP NAME IS SPCRCP_TERMINATED_DATE_TIME
    ITEM IS SPCRCP_TERMINATED_DATE          TYPE IS SIGNED LONGWORD
    ITEM IS SPCRCP_TERMINATED_TIME          TYPE IS SIGNED LONGWORD
  ENDGROUP SPCRCP_TERMINATED_DATE_TIME
```

```
  GROUP NAME IS SPCRCP_RESPONSIBILITY_RESTS_ON
    ITEM IS SPCRCP_RECIPE_CREATED_BY         TYPE IS CHARACTER 12
    ITEM IS SPCRCP_RECIPE_MODIFIED_BY        TYPE IS CHARACTER 12
    ITEM IS SPCRCP_RECIPE_TERMINATED_BY      TYPE IS CHARACTER 12
  ENDGROUP SPCRCP_RESPONSIBILITY_RESTS_ON


SET IS SPCRCP_CALC
SET IS SPCRCP_INDEX
SET IS SPCRCP_SPEC_VERSION_INDEX
SET IS SPCRCP_RECIPE_OVERRIDE_SET
SET IS SPCRCP_INGREDIENT_SET
SET IS SPCRCP_INGREDIENT_INDEX


*****************************************************************
*     INGREDIENTS FOR A RECIPE
*****************************************************************
RECORD NAME IS SPCING_REC

 GROUP NAME IS SPCING_INGREDIENT_DATA
    ITEM IS SPCING_PARAMETER                 TYPE IS CHARACTER 20
    ITEM IS SPCING_VALUE                     TYPE IS CHARACTER 20
    ITEM IS SPCING_UNIT                      TYPE IS CHARACTER 10
    ITEM IS SPCING_DISPLAY_FLAG              TYPE IS CHARACTER 1
 ENDGROUP SPCING_INGREDIENT_DATA

         .

*****************************************************************
*     RECIPE OVERRIDES
*****************************************************************
RECORD NAME IS SPCROV_REC

 GROUP NAME IS SPCROV_KEY
    ITEM IS SPCROV_RECIPE_NAME               TYPE IS CHARACTER 12
    ITEM IS SPCROV_OVERRIDE_NAME             TYPE IS CHARACTER 12
 ENDGROUP SPCROV_KEY

    ITEM IS SPCROV_SPEC_ID                   TYPE IS CHARACTER 12

    ITEM IS SPCROV_SPEC_VERSION              TYPE IS CHARACTER 6

  GROUP NAME IS SPCROV_CREATION_DATE_TIME
    ITEM IS SPCROV_CREATION_DATE             TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_CREATION_TIME             TYPE IS SIGNED LONGWORD
  ENDGROUP SPCROV_CREATION_DATE_TIME

  GROUP NAME IS SPCROV_TERMINATED_DATE_TIME
    ITEM IS SPCROV_TERMINATED_DATE           TYPE IS SIGNED LONGWORD
    ITEM IS SPCROV_TERMINATED_TIME           TYPE IS SIGNED LONGWORD
  ENDGROUP SPCROV_TERMINATED_DATE_TIME

  GROUP NAME IS SPCROV_RESPONSIBILITY_RESTS_ON
    ITEM IS SPCROV_RECIPE_CREATED_BY         TYPE IS CHARACTER 12
    ITEM IS SPCROV_RECIPE_TERMINATED_BY      TYPE IS CHARACTER 12
  ENDGROUP SPCROV_RESPONSIBILITY_RESTS_ON
```

```
GROUP NAME IS SPCROV_TYPE_OF_OVERRIDE
  ITEM IS SPCROV_LOT_NUMBER                TYPE IS CHARACTER 11
  ITEM IS SPCROV_PRODUCT                   TYPE IS CHARACTER 25
  ITEM IS SPCROV_PRODUCT_GROUP             TYPE IS CHARACTER 12
  ITEM IS SPCROV_OWNER                     TYPE IS CHARACTER 12
  ITEM IS SPCROV_CREATE_CODE               TYPE IS CHARACTER 6
  ITEM IS SPCROV_PERIOD_FROM               TYPE IS SIGNED LONGWORD
  ITEM IS SPCROV_PERIOD_TO                 TYPE IS SIGNED LONGWORD
  ITEM IS SPCROV_MACHINE_ID_OR_ENTITY      TYPE IS CHARACTER 12
  ITEM IS SPCROV_EVENT                     TYPE IS CHARACTER 12
ENDGROUP SPCROV_TYPE_OF_OVERRIDE
```

```
*****************************************************************
*           CMTSCH MODIFIED TO INCLUDE RECORDS FOR THE RCP MODULE
*                       Angus J. MacDonald  August 1989
*****************************************************************

*   DBM_RTB increased to take account of new records
*   added for the RCP module
*   02 DBM_RTB occurs 298 times pic 9(9) comp.
   02 DBM_RTB occurs 306 times pic 9(9) comp.


*****************************************************************
*         NEW RECORDS TO SUPPORT THE RCP MODULE
*         Angus J. MacDonald  August 1989
*****************************************************************

   02 SPCVRC_REC.
      03 SPCVRC_SPEC_ID pic x(12).
      03 SPCVRC_SPEC_VERSION pic x(6).
      03 SPCVRC_RECIPE_NAME pic x(12).
      03 FILLER pic x(2).
   02 SPCRCP_REC.
      03 SPCRCP_KEY.
         04 SPCRCP_FACILITY pic x(6).
         04 SPCRCP_RECIPE_NAME pic x(12).
      03 SPCRCP_RECIPE_TYPE pic x(12).
      03 SPCRCP_RECIPE_DESCRIPTION pic x(35).
      03 SPCRCP_NUMBER_OF_INGREDIENTS pic x(6).
      03 SPCRCP_CREATION_DATE_TIME.
         04 SPCRCP_CREATION_DATE pic s9(6) usage is comp.
         04 SPCRCP_CREATION_TIME pic s9(6) usage is comp.
      03 SPCRCP_LAST_MODIFIED_DATE_TIME.
         04 SPCRCP_LAST_MODIFIED_DATE pic s9(6) usage is comp.
         04 SPCRCP_LAST_MODIFIED_TIME pic s9(6) usage is comp.
      03 SPCRCP_TERMINATED_DATE_TIME.
         04 SPCRCP_TERMINATED_DATE pic s9(6) usage is comp.
         04 SPCRCP_TERMINATED_TIME pic s9(6) usage is comp.
      03 SPCRCP_RESPONSIBILITY_RESTS_ON.
         04 SPCRCP_RECIPE_CREATED_BY pic x(12).
         04 SPCRCP_RECIPE_MODIFIED_BY pic x(12).
         04 SPCRCP_RECIPE_TERMINATED_BY pic x(12).
      03 FILLER pic x(1).
   02 SPCING_REC.
      03 SPCING_INGREDIENT_DATA.
         04 SPCING_PARAMETER pic x(20).
         04 SPCING_VALUE pic x(20).
         04 SPCING_UNIT pic x(10).
         04 SPCING_DISPLAY_FLAG pic x(1).
      03 FILLER pic x(1).
   02 SPCROV_REC.
      03 SPCROV_KEY.
         04 SPCROV_RECIPE_NAME pic x(12).
         04 SPCROV_OVERRIDE_NAME pic x(12).
      03 SPCROV_SPEC_ID pic x(12).
      03 SPCROV_SPEC_VERSION pic x(6).
      03 SPCROV_CREATION_DATE_TIME.
```

```
          04 SPCROV_CREATION_DATE pic s9(6) usage is comp.
          04 SPCROV_CREATION_TIME pic s9(6) usage is comp.
       03 SPCROV_TERMINATED_DATE_TIME.
          04 SPCROV_TERMINATED_DATE pic s9(6) usage is comp.
          04 SPCROV_TERMINATED_TIME pic s9(6) usage is comp.
       03 SPCROV_RESPONSIBILITY_RESTS_ON.
          04 SPCROV_RECIPE_CREATED_BY pic x(12).
          04 SPCROV_RECIPE_TERMINATED_BY pic x(12).
       03 SPCROV_TYPE_OF_OVERRIDE.
          04 SPCROV_LOT_NUMBER pic x(11).
          04 SPCROV_PRODUCT pic x(25).
          04 SPCROV_PRODUCT_GROUP pic x(12).
          04 SPCROV_OWNER pic x(12).
          04 SPCROV_CREATE_CODE pic x(6).
          04 SPCROV_PERIOD_FROM pic s9(6) usage is comp.
          04 SPCROV_PERIOD_TO pic s9(6) usage is comp.
          04 SPCROV_MACHINE_ID_OR_ENTITY pic x(12).
          04 SPCROV_EVENT pic x(12).

*****************************************************************
*                CMTSCH END OF NEW RECORDS FOR THE RCP MODULE
*****************************************************************
```

Appendix E

Reprints of Published Papers

Integrating COMETS and Process Simulation

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Abstract

Software has been developed to integrate the SUPREM-II process simulator with the COMETS CAM system. The simulator is controlled interactively from within COMETS; the input being generated from the database and the output presented graphically. The presentation shows how this system may be used to aid process development and control the processing of individual lots.

Introduction

The COMETS Computer Aided Manufacturing (CAM) system has a significant user base in the semiconductor industry. This is, in part, due to the structure and adaptability of COMETS. The structure is a function of the user interface and the format of the database which control the movement and storage of information. Its adaptability comes from its modularity which allows COMETS to meet the differing needs of its users.

In this paper we demonstrate how process simulation may be integrated with the COMETS CAM system without compromising the structure or adaptability of COMETS. A new module - SIM - has been developed which consists of a series of routines that interface COMETS and the process simulator SUPREM-II. Figure 1 shows the SIM module in relation to the rest of COMETS. The SIM module has the following capabilities: it maintains a simulation history for each lot processed, allows the processing of whole products to be simulated, provides powerful 'look-ahead' and 'what-if' functions for controlling the processing of individual lots, and allows interactive simulations to be performed. The result is an environment which can be used to aid new process development and also process maintenance.

In order to maintain the integrity of the COMETS-user interface, the SIM module uses a set of menus which have been added to the existing COMETS menu system. SIM has also been implemented without modifying the existing COMETS code or the database. Instead, this implementation takes advantage of the user exits and the General Tables System (GTS) which means that SIM should integrate with future updates of COMETS without requiring any modification.

The rest of this paper considers in more detail the process simulator and the implementation of the SIM module. An example of its use for an nMOS process is discussed and an appendix summarises the technical specifications of the SIM module.

Process Simulation

The simulation of semiconductor fabrication dates back to the 1960's when process models were developed for bipolar technology. In the mid 1970's modelling MOS technology became more important. For MOS, both doping profile and oxide thickness play a key role in determining the electrical characteristics of devices. The development of process simulation programs which could sequentially model individual process steps demonstrated the applicability of process simulation to process design, since simulation offers great cost savings over experimentation. With increasing computer power the use of process simulation has increased so that it is now commonly used to support all aspects of new process development. However, simulation can also potentially be used for diagnostic analysis during routine production. This aspect of its application is less well

developed and it forms the basis of this paper.

SUPREM-II was chosen to demonstrate how process simulation and CAM may be integrated because of its maturity, its wide availability and because it can be used for real-time simulation. SUPREM-II is a one-dimensional non-interactive process simulator which sequentially simulates the effect that individual process-steps have on silicon. Figure 2 shows how a number of one-dimensional sections can give a simple two-dimensional picture of the effect processing has on an nMOS device. The models within SUPREM-II allow a full range of process-steps to be simulated directly. These include: diffusion, oxidation, deposition, implantation and etch steps. Process-steps which cannot be directly simulated can often be modelled using combinations of these. It is also possible to tailor SUPREM-II to a processing environment which allows more accurate results to be obtained.

SUPREM-II is operated by a series of statements in a text file. These define the individual process-steps and the input/output formats for data. An example of such a file is shown in figure 3. After any process-step it is possible to display or save the current state of the simulation. For this application a graphics package is used to plot the concentration of impurities in the silicon against depth from saved simulation data. Figure 4 shows an example of the doping profile of a one-dimensional section simulated by SUPREM-II

Implementation

As figure 1 shows, the SIM module interfaces with a number of other COMETS modules. Each of these modules (WIP, SPEC, FCM and, optionally, SCRIPT) must be present for the SIM module to work.

To maintain the integrity of the COMETS system and to allow for updates to COMETS, SIM makes extensive use of the user exits and the General Tables System (GTS). The code is written in Cobol with the exception of some graphics routines which are written in Fortran. When interfacing with the VAX/VMS operating system, logicals and routines from the Run Time Library (RTL) are used.

From the point of view of the user, SIM consists of four parts:

1. In-process simulations which are used to maintain a simulation log of the processing for each lot.

2. The product simulation menu which allows the processing of individual products to be simulated and the results inspected.

3. The lot simulation menu which allows 'look-ahead' and 'what-if' simulations of individual lots to be performed and the results inspected. It also allows the simulation histories of lots to be investigated.

4. The program INTERSUP which allows SUPREM-II to be used interactivly.

Reference was made earlier to process development and process maintenance; the former is aided by the functions of the product simulation menu and INTERSUP, and the latter by in-process simulations and the functions of the lot simulation menu. An example of the application of these functions is given in the next section.

The in-process part of the SIM module was developed to integrate CAM and process simulation at the level where the CAM software actually interfaces with the processing of lots in the clean-room. Therefore, the process-step of SUPREM-II required an equivalent object in the COMETS database; the most obvious candidate being ROUTE-OPERATION. Figure 5 shows a simple data model of the objects used within COMETS for WIP tracking and identifies the process-step. It is also necessary to be able to specify the one-dimensional sections simulated by SUPREM-II These are defined by the identifier SECTION.

The MVIN function was chosen to be the point where a process-step should be simulated since it is a WIP function which can always be associated with a ROUTE-OPERATION, and is called prior to any processing of a lot being performed. Within the MVIN code, two user exits are available: USR500 and USR010. The latter was chosen to attach the simulation code as USR010 is called only once, whereas, because of the review facility, USR500 could be called many times, causing many unnecessary simulations to be performed.

To automatically simulate each step, the data to run SUPREM-II has to be stored in or around the database, without modifying the database. Using the GTS for this purpose was explored but proved to be restrictive on the way data was stored and it was also awkward to use. Instead the text files of the SPEC module were chosen because they do not restrict the format or number of SUPREM-II statements required to simulate a process-step and also enforce some structure on the way simulation control data is maintained, ie. through the AUTHORIZATION, SCANNING and FREEZING of SPECS. SUPREM-II processing statements are added to the bottom of each SPEC file as show in figure 6. Four sets of SUPREM-II statements are required to define an nMOS process (field, source-drain, enhancement channel and depletion channel), each is preceeded by a line with two stars and a character string. The stars identify the beginning of each SECTION and the character string is the SECTION-NAME. As with the MVIN function, SPEC files can be associated with ROUTE-OPERATIONS.

As a lot is completing the MVIN, control is passed to the user exit, this calls the simulation routine for each SECTION in the ROUTE-OPERATION SPEC file which validates the SECTION-NAME against a table - SIM$SECTIONS - in the GTS. The SUPREM-II input file is generated from both the SPEC file and data held in the PRODUCTS user defined fields. A sub-process is then spawned to run SUPREM-II. All the files generated are in a directory pointed to by COMETS$SIMULATIONS, with each set of files having a unique identifying prefix. This is formed from the LOT-NUMBER, the SECTION-NAME, the ROUTE and the OPERATION. Each simulation run produces four files, denoted here by their suffixes:

.LIS - which is the SUPREM-II input file.

.DAT - which is the data file produced by SUPREM-II.

.SAV - which contains the structure of the section after the current simulation step. The next step for this lot and section will use this data as a starting point.

.LOG - contains the completion status of the simulation.

Feedback to the operator is confined to messages written to the bottom of the screen announcing the completion of each simulation. In the event of an error occurring during the simulation a mail message is sent to the user names held in the FCM table called SIM$MAIL.

When processing is being controlled using SCRIPT, the START instruction must be used in order to perform the in-process simulation. Following this, the CALL USER ROUTINE instruction may be used to produce, on a graphics screen, a plot of the doping profile for the current LOT. For example:

CALL USER ROUTINE "PROFILE ENHANCEMENT"

where ENHANCEMENT is the name of the SECTION. When this facility is used the user exit USR018 calls routines in the SIM module to actually produce the plot.

The product simulation menu, lot simulation menu and INTERSUP are accessed through the simulation main menu which is in turn accessed through the user main menu, ie. the user exits USR001 and USR002. Figure 7 shows the menu hierarchy for this module, and figures 8 through 10 show the individual screens.

Under the Product Simulation Menu (0PSM) there are five functions:

0PPS - Perform the process simulation for a given PRODUCT and SECTION.

0VPP - View the doping profile produced by this simulation.

0VPD - View the data file produced by this simulation.

0PPP - Write the doping profile to a file in a format suitable for a hardcopy device.

0LPD - List the data file on a hardcopy device.

0PPS acts in a similar way to that of the in-process MVIN simulation, except that rather than generating an input file for one process-step, it compiles all the SECTION data for a PRODUCT into one file before spawning a simulation run.

Under the Lot Simulation Menu (0LSM) there are nine functions:

0STE - Simulate to the end of the process for a given LOT and SECTION.

0SRR - Simulate the processing of one SECTION of a given LOT on a specified rework ROUTE.

0RSC - (Re-)simulate a process-step for a given LOT and SECTION (Assumes last simulated process-step unless ROUTE and OPERATION are specified).

0ARS - Associate the simulation data produced by 0RSC with the appropriate lot history.

0RCS - Return the state of the current simulation to that of the last process-step simulated.

0VDP - View doping profile for a given LOT and SECTION (Assumes last simulated process-step unless ROUTE and OPERATION are specified).

0VSD - View the data file for a given LOT and SECTION (Assumes last simulated process-step unless ROUTE and OPERATION are specified).

0PDP - Write file containing doping profile for a given LOT and SECTION in a format suitable for a hardcopy device (Assumes last simulated process-step unless ROUTE and OPERATION are specified).

0LSD - List data file for a given LOT and SECTION on a hardcopy device, via the queue SYS$PRINT (Assumes last simulated process-step unless ROUTE and OPERATION are specified).

0STE, 0SRR and 0RSC provide powerful look-ahead functions for the process engineer. These functions allow investigation of how further processing will affect a lot. For example, the final electrical parameters of a lot may be compared with the process specifications. A variety of future

scenarios (what-if simulations) can then be explored by using 0RCS after each set of simulations in order to reset the last simulation for this LOT and SECTION to that of the last process-step simulated. When 0STE is called after 0SRR, for a given LOT and SECTION, the current process-step is included in the simulation. 0RSC provides the process engineer with the ability to re-simulate a process step when a simulation has either previously failed or the lot has been malprocessed. This is done by modifying the SUPREM-II statements in the input file. The results of the simulation are then associated with the lot history by calling 0ARS which repositions the '.LIS', '.DAT', '.SAV' and '.LOG' files in the simulation history directory (COMETS$SIMULATIONS).

The final part of the SIM module is INTERSUP, a program which allows SUPREM-II to be used interactively. INTERSUP can be used to develop a description of a process, which may then be entered into the SPEC files for the ROUTE-OPERATIONS of the PRODUCTS fabricated by this process.

All the data files used by the functions of the lot simulation menu, the product simulation menu and INTERSUP are stored in the users current directory. This protects the files in the simulation history directory from being modified unintentionally. The only way in which data files can be inserted into the simulation history directory is by using the associate simulation history (0ARS) function after the re-simulation (0RSC) of a process-step.

This concludes the description of how the SIM module has been implemented. The following section gives an example of how this module might be applied.

Application

Once the SIM module has been installed at a site, it requires a number of set-up steps to be performed for each FACILITY for which it is to be used. At the EMF a FACILITY 'IC_FAB' has been set up to track a 6μm nMOS process using COMETS. For this FACILITY three set-up steps were performed:

1. The valid SECTIONS for this FACILITY were defined by creating the table SIM$SECTIONS in the GTS.

2. The SIM$MAIL table, in the FCM, was created to contain the user ids of those who should be mailed if an error condition occurs during an in-process simulation.

3. New versions of the SPEC files used during this process were created so that each ROUTE-OPERATION which is to be simulated has the corresponding SUPREM-II statements in its SPEC file.

Figure 11 lists the ROUTES and OPERATIONS for a PRODUCT 'DRAM' which shall be used to demonstrate how the SIM module can be applied in practice.

A LOT 'EMF88001' is created for the PRODUCT, and begins processing at the first OPERATION on the first ROUTE. As the LOT is processed it is moved-in to each ROUTE-OPERATION in sequence and data is collected through EDC. When the LOT reaches OPERATION 2400 on ROUTE 'GTEOX N6' it spends too long in the furnace which results in a value for the oxide thickness parameter which is outside the acceptable range, and so the lot is put on hold. An engineer responsible for this part of the process can use the functions of the SIM module to explore the possible repercussions of this error and to devise a solution.

The Re-Simulate Current process-step (0RSC) function can be used to modify the input files for each SECTION simulated during this process-step; to simulate the processing which actually occurred. The re-simulated results for this process step can then be associated with the lot history of the LOT at this point by using 0ARS.

Not only will the extra time which the lot has spent in the furnace effect the thickness of the gate oxide, but it will also effect the distribution of the arsenic implanted earlier (OPERATION 1400). Both effects will result in increased threshold voltages for depletion and enhancement devices, the extent of this can be checked using the look-ahead function 0STE.

If the threshold voltage of the depletion and enhancement devices is found to be outside of specification then the processing for this lot can be modified. It may be possible to modify the following boron implant (OPERATION 1200), or it may prove necessary to rework the lot. A series of what-if simulations can be performed, using 0RSC, 0SRR and 0RCS, to investigate how these options will effect the threshold voltages of the devices and the other electrical parameters. The functions 0VDP and 0VSD would be used for inspecting the results of the simulations.

Conclusion

This paper has shown how process simulation can be integrated with the COMETS CAM system. The new module - SIM - has been implemented without any modification to either the COMETS code or the database. This has been achieved by utilising the COMETS user exits and the general tables system. Control of information flow within the SIM module is achieved by using menus and by strictly controlling the way simulation data is entered and how the results of the simulations are stored. This implementation of the SIM module maintains both the structure and the adaptability of COMETS.

The SIM module provides powerful tools for process development and maintenance, using information held in the database. Available functions include:

1. Simulation of the fabrication of any product.

2. An on-line facility for performing look-ahead and what-if simulations for a lot.

3. Interactive simulation.

4. Both graphical and numeric presentation of the results of the simulations.

The simulator used in the SIM module is SUPREM-II. Although this is only a one-dimensional simulator, and therefore unable to simulate lateral diffusions, it is widely available and relatively light on computer resources. With more powerful computers it will be possible to replace SUPREM-II with a two-dimensional process simulator. This will require only a minor modification of the SIM module.

Acknowledgements

We would like to thank Consilium for providing us with the COMETS system and Digital Equipment Corp. for the VAX8350 on which COMETS is being run. Angus MacDonald would also like to thank SERC and Plessey Semiconductors for their financial support.

Appendix: Technical Specification for the SIM Module

Database areas accessed:

Name	Operation
WIPPRD_AREA	read only
WIPRTE_AREA	read only
WIPLOT_AREA	read only
WIPLTH_AREA	read only
GTS_AREA	read only

Routines:

USR001 -User main exit is used to pass control to the menus of the SIM module. Screen: SIM000.

USR002 -Security routine for the user functions.

USR010 -User exit called after MVIN function, passes control to in-process part of SIM module.

USR018 -User exit allows plotting of doping profiles simulated during SCRIPT START. Calls: SIM120, SIM410.

SIM010 - Screen handling routine for product simulation menu. Screen: SIM010. Calls: SIM011, SIM012, SIM013, SIM014.

SIM011 - Controls product simulation (0PPS) function. Calls: SIM121, SIM200, SIM300.

SIM012 - Controls plotting of product doping profiles (0VPP and 0PPP). Calls: SIM121, SIM410.

SIM013 - Controls viewing of product data files (0VPD). Calls: SIM121, SIM114.

SIM014 - Controls printing of product data files (0LPD). Calls: SIM121, SIM116.

SIM020 - Screen handling routine for lot simulation menu. Screen: SIM020. Calls: SIM021, SIM022, SIM023, SIM024, SIM025, SIM026, SIM027, SIM028.

SIM021 - Controls simulate to end (0STE). Calls: SIM120, SIM200, SIM300.

SIM022 - Controls rework route simulation (0SRR). Calls: SIM120, SIM210, SIM300.

SIM023 - Controls simulation of individual process-steps (0RSC). Calls: SIM120, SIM220, SIM300.

SIM024 - Controls association of re-simulated process-step simulation files with their lot histories (0ARS). Calls: SIM120.

SIM025 - Controls plotting of lot doping profiles (0VDP and 0PDP). Calls: SIM120, SIM410.

SIM026 - Controls viewing of lot data files (0VSD). Calls: SIM120, SIM114.

SIM027 - Controls printing of lot data files (0LSD). Calls: SIM120, SIM116.

SIM028 - Controls return of the current state of simulation to the last process-step simulated (0RCS). Calls: SIM120.

SIM030 - Interfaces with the program INTERSUP.

SIM100 - In-process routine which simulates one process-step. Calls: SIM120, SIM300.

SIM104 - Generates the SUPREM-II statements.

SIM114 - Presents files for viewing. Screen: SIM114.

SIM116 - Prints files. Screen: SIM116.

SIM120 - Forms the simulation file prefix from LOT-NUMBER, SECTION-NAME, ROUTE and OPERATION.

SIM121 - Forms the simulation file prefix from PRODUCT and SECTION-NAME.

SIM200 - Generates the input file for the simulator for the whole PRODUCT, or only part if a starting ROUTE and OPERATION are specified.

SIM210 - Generates the input file for the simulator for one ROUTE.

SIM220 - Generates the input file for the simulator for one ROUTE-OPERATION.

SIM300 - Spawns a sub-process to run SUPREM-II.

SIM410 - Interfaces with the plotting routines. Calls: the plotting routines.

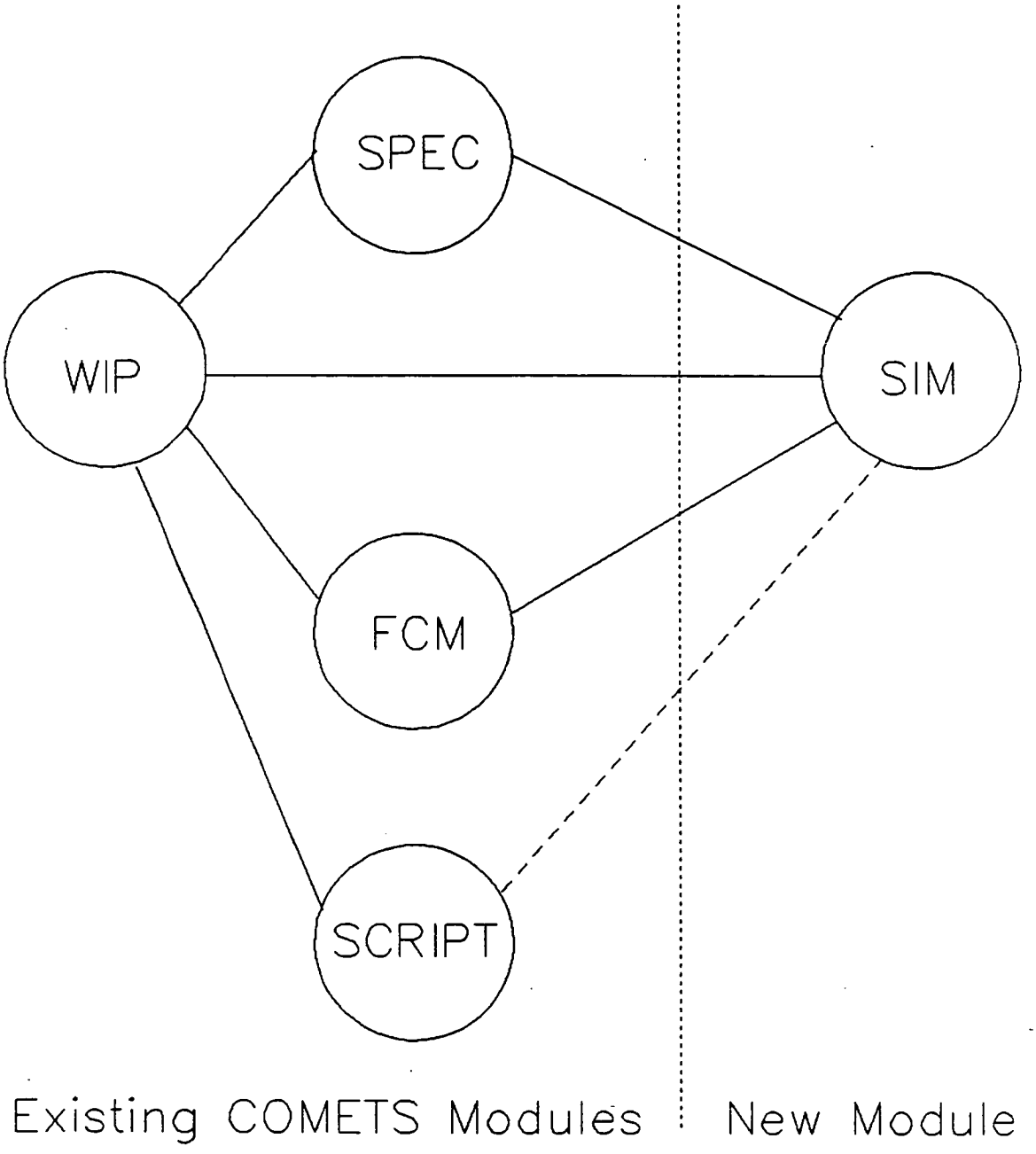

Figure 1. The relationship between the SIM module and other COMETS modules.

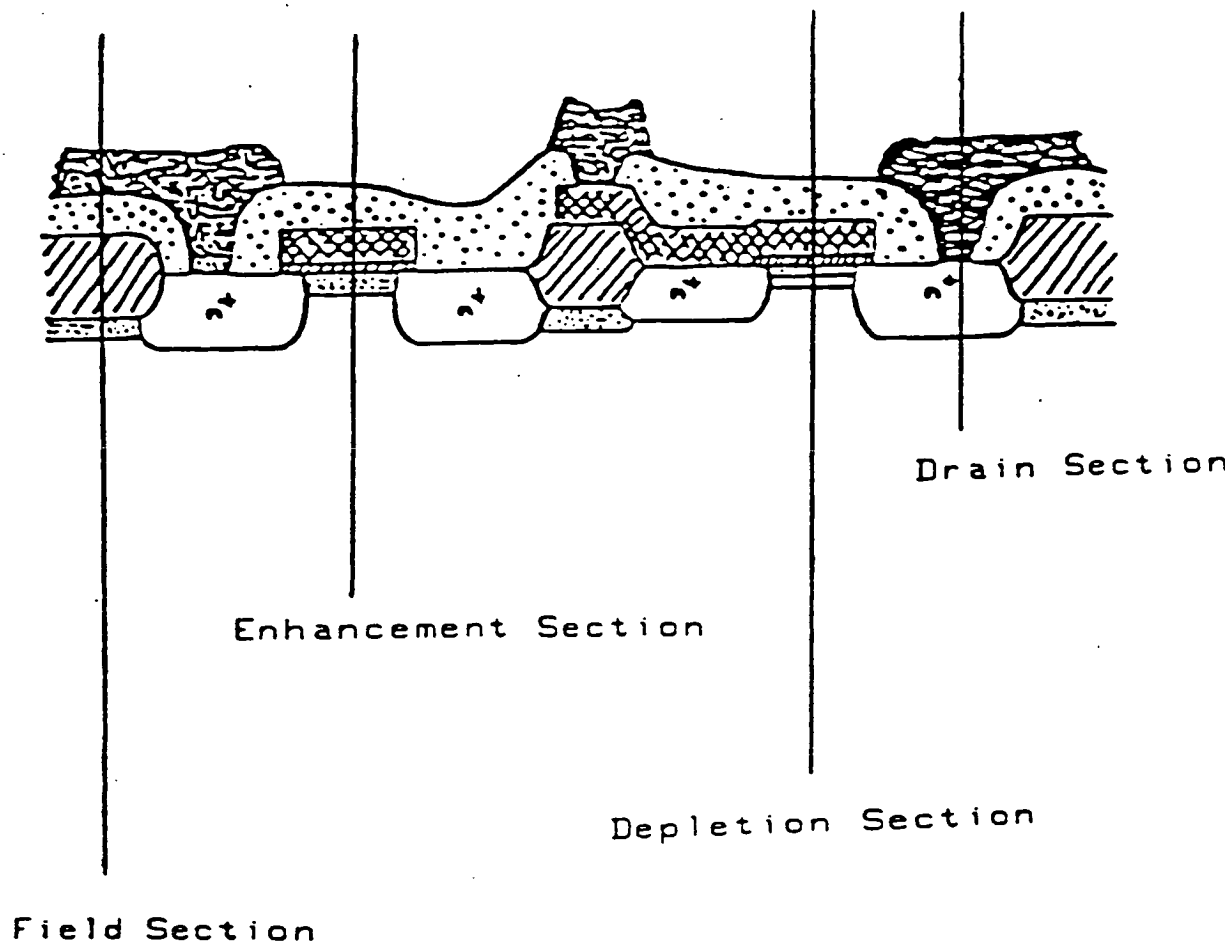

Figure 2. Sections of NMOS enhancement and depletion mode devices.

```
TITL    n-channel, silicon gate, 6μm, emf, enhancement section
SUBS    ELEM=B,CONC=6E14,ORNT=100
GRID    DYSI=7.5E-3,DPTH=0.6,YMAX=1

LOAD    LUNM=23,TYPE=A

PRNT    HEAD=Y
STEP    TYPE=IMPL,ELEM=B,DOSE=4E11,AKEV=40

SAVE    LUNM=23,TYPE=A
END
```

Figure 3. SUPREM-II input file defining a low energy Boron implant.

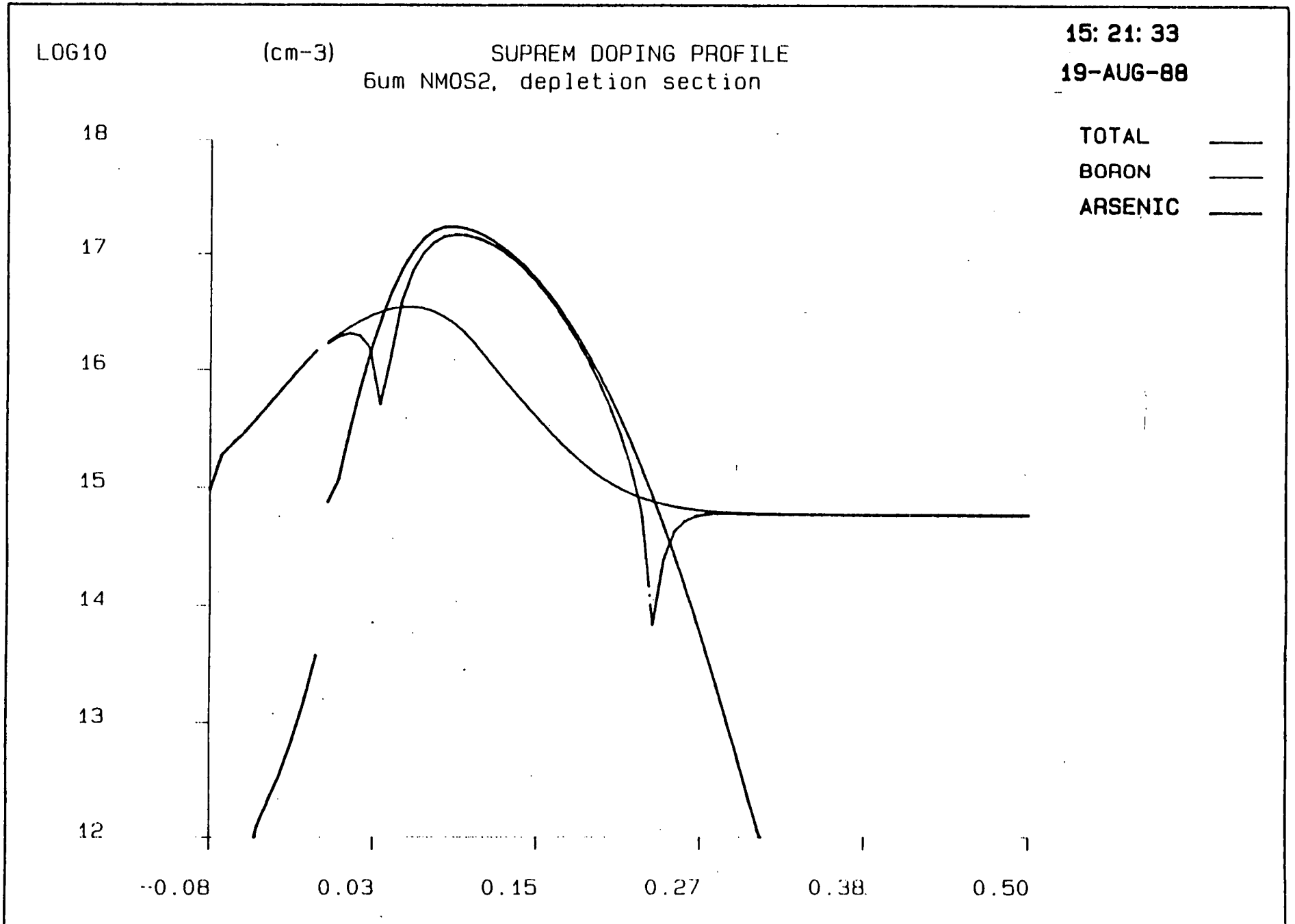

Figure 4. Doping profile from data produced by SUPREM-II.

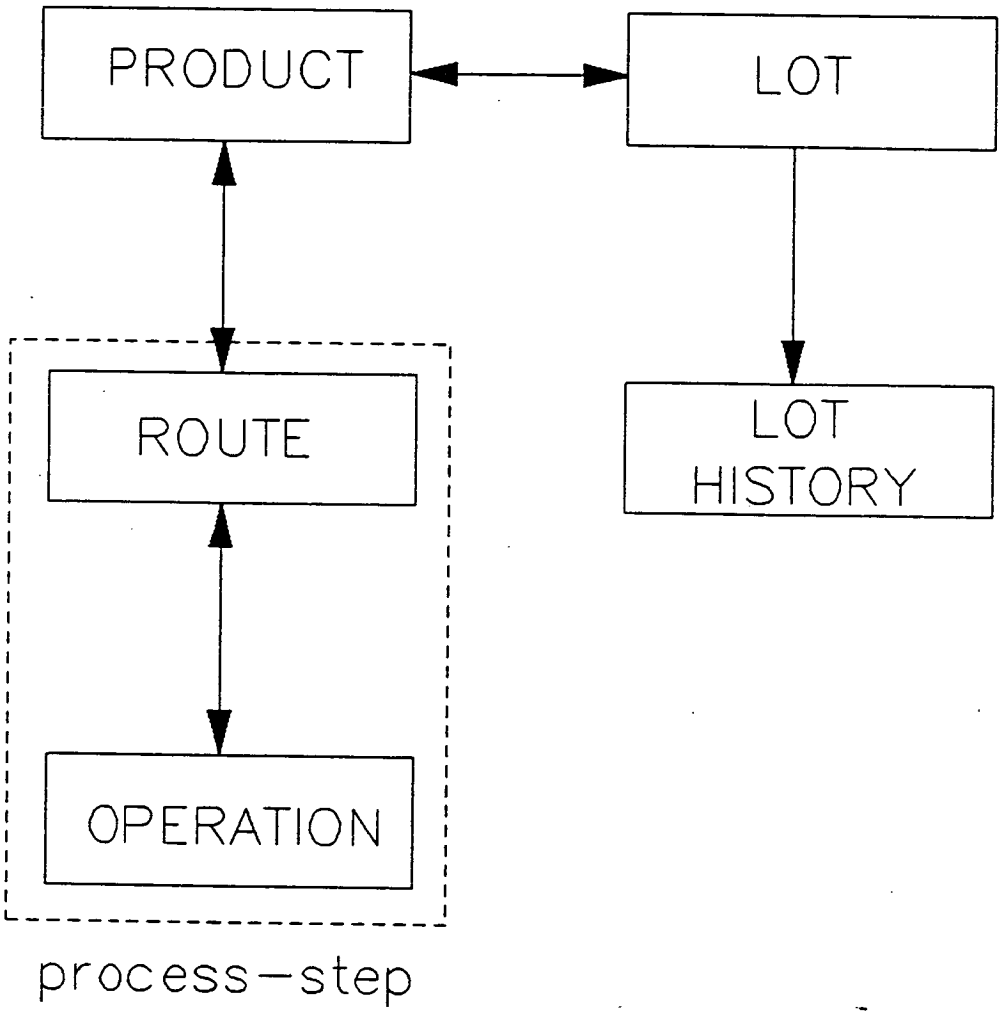

Figure 5. Simple data model of part of the WIP area of the COMETS database.

GATE OXIDE

Furnace 1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
17min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure: oxide thickness

```
** FIELD
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
** DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
```

Figure 6. A SPEC file for gate oxidation which has been extended for use with the SIM module.

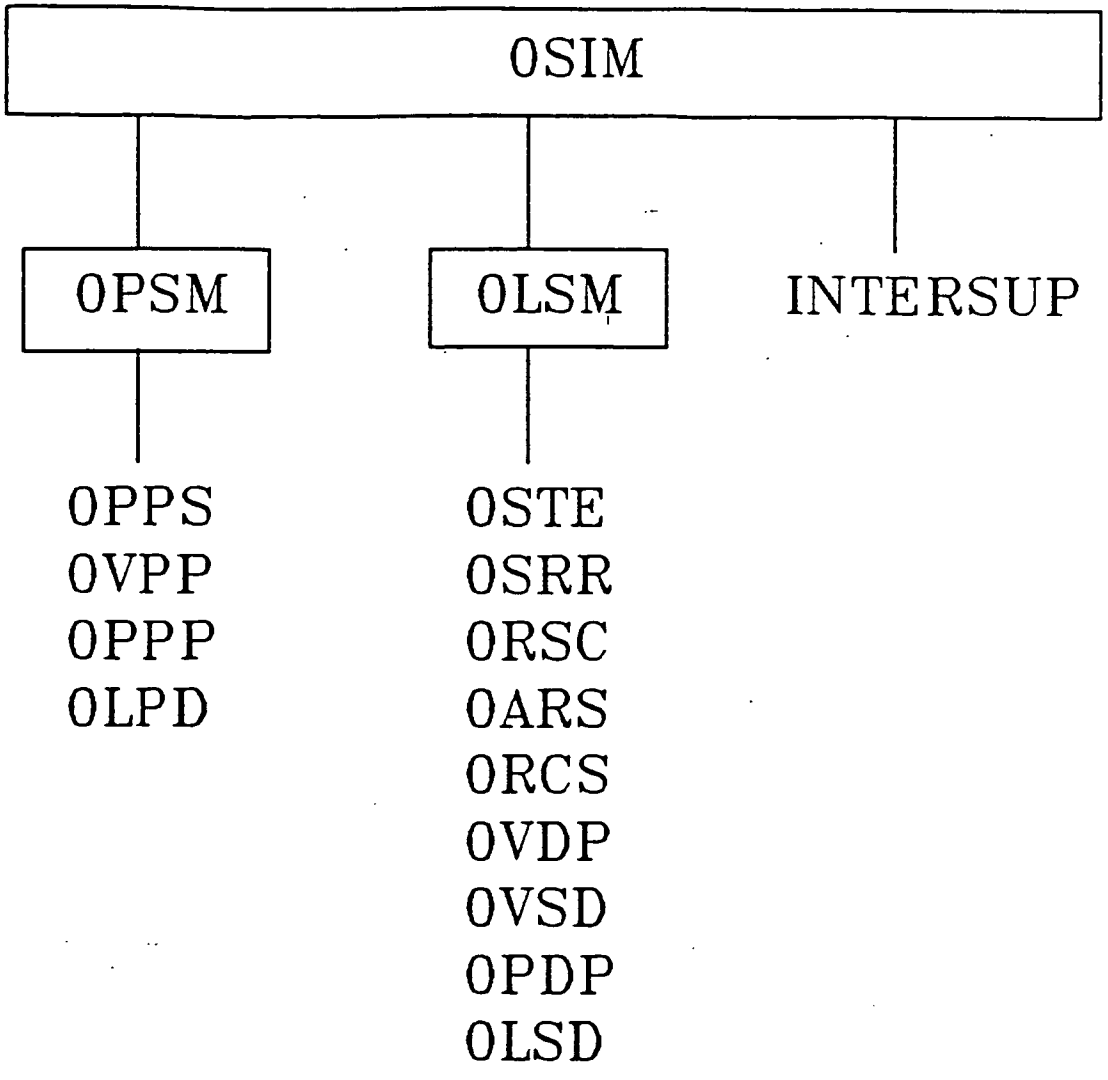

Figure 7. The SIM menu structure.

```
SIM000S                  SIMULATION MAIN MENU (0SIM)        SYS 19/08/88 18:43:01
  EMF                             IC_FAB

                              FUNCTION...____

                    PRODUCT SIMULATION MENU.............(0PSM)
                    LOT SIMULATION MENU.................(0LSM)
                    INTERACITVE SIMULATOR - INTERSUP...(0INT)




RETURN = PROCESS
SFK1   = EXIT
```

Figure 8. The simulation main menu.

```
SIM010S                PRODUCT SIMULATION MENU (0PSM)        SYS 19/08/88 18:43:16
  EMF                            IC_FAB

                      FUNCTION.....____
                      PRODUCT.....________________________
                      SECTION.....____________

              PERFORM PRODUCT SECTION SIMULATION.......(0PPS)
              VIEW DOPING PROFILE OF PRODUCT SECTION...(0VPP)
              VIEW DATA FILE FOR PRODUCT SECTION.......(0VPD)
              PLOT DOPING PROFILE OF PRODUCT SECTION...(0PPP)
              LIST DATA FILE FOR PRODUCT SECTION.......(0LPD)



RETURN = PROCESS
SFK1   = EXIT                          SFK2 = HELP
```

Figure 9. The product simulation menu.

```
SIM020S                  LOT SIMULATION MENU (0LSM)          SYS 19/08/88 18:43:24
  EMF                            IC_FAB

                      FUNCTION.....____
                      LOT.....____________
                      SECTION.....________________
                      ROUTE (opt.).....__________
                      OPERATION (opt.)...____

              SIMULATE TO END OF PROCESS.....(0STE)
              SIMULATE REWORK ROUTE.....(0SRR)
              (RE-)SIMULATE ROUTE-OPERATION.....(0RSC)
              INSERT SIMULATION RESULT IN HISTORY..(0ARS)
              RETURN TO ORIGINAL SIMULATION STATE..(0RCS)
              VIEW DOPING PROFILE FOR SIMULATION...(0VDP)
              VIEW SIMULATION DATA.....(0VSD)
              PLOT DOPING PROFILE FOR SIMULATION...(0PDP)
              LIST SIMULATION DATA.....(0LSD)

RETURN = PROCESS
SFK1   = EXIT                          SFK2 = HELP
```

Figure 10. The lot simulation menu.

ROUTE :	**NITDP N6**	**CLEAN, OXIDE AND NITRIDE 6UM NMOS**
6000	INITCLEAN1	INITIAL WAFER CLEAN 1
2000	PAD OX 1	INITIAL PAD OXIDATION 1
3000	NITRIDE 1	SILICON NITRIDE DEPOSITION 1
ROUTE :	**LITH1 N6**	**1ST PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7200	EXPOSE 1	EXPOSE 1 (MASK LEFT HALF OF T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**FLDIM N6**	**BORON FIELD IMPLANT 6UM NMOS**
1000	FIELDIMP1	BORON FIELD IMPLANT 1 (2E13,130KEV)
ROUTE :	**RNIT1 N6**	**OX, NIT & RESIST REMOVE 1 6UM NMOS**
6200	OXIETCH 1	4:1 AMMONIUM FLUORIDE:HF OX ETCH 1
6400	NITETCH 1	SILICON NITRIDE PLASMA ETCH 1
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2
ROUTE :	**LOCOS N6**	**CLEAN AND FIELD OX GROWTH 6UM NMOS**
6010	POXIDCLN 1	PRE-OXIDATION CLEAN 1
2200	FIELD OX 1	FIELD OXIDATION 1
ROUTE :	**RMBOX N6**	**RESIST COAT FRONT,OX ETCH 6UM NMOS**
7010	RESCOAT1	RESIST COAT AND HARD BAKE
6210	OXIETCH 2	4:1 AMMONIUM FLUORIDE:HF OX ETCH 2
6100	RESSTRIP 1	RESIST STRIP (NITRIC ACID 1)
ROUTE :	**RNIT2 N6**	**OX, NIT & RESIST REMOVE 2 6UM NMOS**
6260	OXIETCH 7	4:1 AMMONIUM FLUORIDE:HF OX ETCH 7
6400	NITETCH 1	SILICON NITRIDE PLASMA ETCH 1
6220	OXIETCH 3	4:1 AMMONIUM FLUORIDE:HF OX ETCH 3
ROUTE :	**LITH2 N6**	**2ND PHOTO 6UM NMOS**
7620	PSPNBAKE 1	PRE-SPIN BAKE
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7210	EXPOSE 2	EXPOSE 2 CONTACT RESIST (POS)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**DEPIM N6**	**AS++DEPLETION IMPLANT 6UM NMOS**
1400	DEPLIMP 1	AS++ DEPLETION IMPLANT 1(1.5E12,90)
ROUTE :	**RSTP1 N6**	**RESIST STRIP 1 6UM NMOS**
6100	RESSTRIP 1	RESIST STRIP (NITRIC ACID 1)
ROUTE :	**GTEOX N6**	**CLEAN AND GATE OX GROWTH 6UM NMOS**
6010	POXIDCLN 1	PRE-OXIDATION CLEAN 1
2400	GATEOX 1	GATE OXIDATION 1
ROUTE :	**ENHIM N6**	**VT ADJUST ENHANCE IMPLANT 6UM NMOS**
1200	VTADJIMP1	VT ADJUST IMPLANT 1 (4E11,40KEV)
ROUTE :	**RSTP2 N6**	**RESIST STRIP 2 6UM NMOS**
6100	RESSTRIP 1	RESIST STRIP (NITRIC ACID 1)
ROUTE :	**ENHAN N6**	**VT ADJUST ENHANCE ANNEAL 6UM NMOS**
4000	ANNEAL 1	VT ADJUST ANNEAL 1
ROUTE :	**LITH3 N6**	**3RD PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7220	EXPOSE 3	EXPOSE 3 (DO NOT EXPOSE T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1

Figure 11. ROUTE-OPERATIONS for the PRODUCT 'DRAM'.

ROUTE :	**GOXET N6**	**GATE OXIDE ETCH & STRIP 6UM NMOS**
6230	OXIETCH 4	4:1 AMMONIUM FLUORIDE:HF OX ETCH 4
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2
ROUTE :	**POLY N6**	**CLEAN, POLY DEP & POLY OX 6UM NMOS**
6020	PPDEPCLN 1	PRE-POLY DEPOSITON CLEAN 1
3100	POLY-SI 1	POLY-SILICON DEPOSITION 1
2600	POLYOX 1	POLY OXIDE OXIDATION 1
ROUTE :	**LITH4 N6**	**4TH PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7230	EXPOSE 4	EXPOSE 4 (MASK RIGHT HALF OF T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**RPOLY N6**	**OX, POLY & RESIST REMOVAL 6UM NMOS**
6240	OXIETCH 5	4:1 AMMONIUM FLUORIDE:HF OX ETCH 5
6410	PSIETCH 1	POLY SILICON PLASMA ETCH 1
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2
ROUTE :	**PDEP N6**	**GATE OX ETCH, CLEAN & PDEP 6UM NMOS**
6240	OXIETCH 5	4:1 AMMONIUM FLUORIDE:HF OX ETCH 5
6030	PPHDPCLN 1	PRE-PHOSPHORUS DEPOSITION CLEAN 1
3200	PDEP 1	PHOSPHORUS DEPOSITION 1 (SOLID)
ROUTE :	**PLYOX N6**	**P DEGLAZE AND POLY OXIDE 6UM NMOS**
6600	DEGLAZE 1	PHOSPHORUS DEGLAZE 1
2610	POLYOX 2	POLY OXIDE OXIDATION 2
ROUTE :	**LITH5 N6**	**5TH PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7220	EXPOSE 3	EXPOSE 3 (DO NOT EXPOSE T/W)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**POXET N6**	**POLY OXIDE ETCH & STRIP 6UM NMOS**
6240	OXIETCH 5	4:1 AMMONIUM FLUORIDE:HF OX ETCH 5
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2
ROUTE :	**PYROD N6**	**PYRO DEP,1ST REFLOW & DENS 6UM NMOS**
3300	PYRO DEP 1	PYRO DEPOSITION 1 (REFLOW)
2800	1 REFLOW 1	FIRST REFLOW OXIDATION 1
6310	TWPYRE 1	T/W REFLOW PYRO ETCH (NH4F:HF) 1
2810	DEPYRO 1	DENSIFICATION OF REFLOW PYRO 1
ROUTE :	**LITH6 N6**	**6TH PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7240	EXPOSE 5	EXPOSE 5 (EXPOSE T/W COMPLETELY)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**ALCON N6**	**OX ETCH, STRIP & 2ND REFLO 6UM NMOS**
6240	OXIETCH 5	4:1 AMMONIUM FLUORIDE:HF OX ETCH 5
6120	RESSTRIP 2	RESIST STRIP (NITRIC ACID) 2
4200	2 REFLOW 1	SECOND REFLOW 1 (INERT)
ROUTE :	**ALDEP N6**	**CLEAN AND AL SPUTTER 6UM NMOS**
6040	PRE-AL 1	PRE-ALUMINIUM EVAPORATION CLEAN 1
3500	AL SPUT 1	ALUMINIUM SPUTTERING 1
ROUTE :	**LITH7 N6**	**7TH PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7210	EXPOSE 2	EXPOSE 2 CONTACT RESIST (POS)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1

Figure 11. (continued)

ROUTE :	**ALETC N6**	**AL ETCH, STRIP & SINTER 6UM NMOS**
6800	AL ETCH 1	ALUMINIUM ETCH 1 (R.I.E.)
6130	RESSTRIP 3	RESIST STRIP (NITRIC ACID) 3
4400	SINTER 1	ALUMINIUM SINTER 1
ROUTE :	**PARAM N6**	**PARAMETRIC TEST 6UM NMOS**
5000	PARA TST 1	PARAMETRIC TEST 1
ROUTE :	**OPDEP N6**	**OVERLAY PYRO DEPOSITION 6UM NMOS**
3310	PYRO DEP 2	PYRO DEPOSITION 2 (OVERLAY)
ROUTE :	**LITH8 N6**	**8TH PHOTO 6UM NMOS**
7000	RESDEPP 1	RESIST DEPOSITION (POSITIVE) 1
7600	SOFTBAKE 1	SOFTBAKE 1
7210	EXPOSE 2	EXPOSE 2 CONTACT RESIST (POS)
7400	DEVELOP 1	DEVELOP RESIST 1 (POS)
7610	HARDBAKE 1	HARDBAKE 1
ROUTE :	**OPETC N6**	**OVERLAY PYRO ETCH & STRIP 6UM NMOS**
6300	PYROETCH 1	OVERLAY PYRO ETCH 1
6100	RESSTRIP 1	RESIST STRIP (NITRIC ACID 1)

Figure 11. (continued)

COMPUTER AIDED MANUFACTURING IN THE SEMICONDUCTOR INDUSTRY

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INTRODUCTION

Computer Aided Manufacturing (CAM) is becoming increasingly important for the production of Integrated Circuits (ICs). Within the semiconductor industry these systems are widely used for production control at all stages of manufacturing. Their application has made possible some dramatic improvements in both manufacturing cycle times and in the quality of the products produced. As circuitry continues to increase in density the problems of manufacturing become even more complex. Such technological advances are set against a backdrop of intense international competition which forces tight economic constraints. Thus the drive to employ CAM systems more effectively is actively being pursued.

In this paper we will discuss the IC manufacturing process, with particular emphasis on wafer fabrication, and show how current CAM systems are used to tackle some of the technical and economic problems faced by the industry. We will then introduce the use of process simulation, as a method for modelling wafer fabrication, and discuss how it may be integrated with a commercial CAM system. This combination provides a set of powerful tools for process development and maintenance which make real-time analysis of the fabrication sequence possible. As a result corrective processing can be investigated and then applied using feed-forward control.

FABRICATING INTEGRATED CIRCUITS

The production of ICs is performed in three stages: wafer fabrication, assembly and test. Wafer fabrication is the process of building three dimensional semiconductor devices (transistors, etc) on a wafer of silicon. This process is complex and hence difficult to control; largely because there are no sub-assemblies, and because many of the process-steps are close to the physical limits of technology. The assembly stage is where the wafers are cut up into *die* (chips) and encapsulated in plastic packages. The packaged ICs are then subjected to functional testing to make sure they perform within the required electrical specification.

Typically a number of wafers are processed together as a *lot*. During fabrication a lot will pass through hundreds of individual process-steps, all of which are carried out within a *clean-room* environment. Although each of these steps performs a different function, the total process can be broken down into a series of process-step sequences each of which applies another layer of the circuit design to the wafer surface. Figure 1 shows the two major types of process sequence: the definition of a new layer and the introduction of a chemical dopant. In both cases the regions that are to be processed are defined using a photolithographic masking procedure. The accurate definition of these masked areas and the control of the quantity of dopants introduced into the silicon is critical to the working of the final ICs. Processing is further complicated when process technology meets physical limitations, eg. linewidths which approach the wavelength of light. There are also many stages where simple measurements cannot be made during processing to verify the success of an operation. As a result it is often not known until the end of the process whether the electrical characteristics of the devices will meet specification.

To achieve the maximum process yield the manufacturing environment must be stable. However consistent processing is often complicated by the large variety and variability of product flow through the clean-room. If misprocessing should occur then it is necessary to rework or scrap whole batches of product. The cost of scrapping a lot is dependent on how far processing has progressed: during a 10 week fabrication cycle the value of a single wafer can multiply by a factor of a thousand.

For a more detailed study of wafer fabrication see Sze (1).

THE ROLE OF CAM SYSTEMS

CAM systems are now widely used in all phases of semiconductor manufacturing. They have supplanted manual methods of production control because they respond more quickly and accurately to engineering changes, management needs and equipment availability.

Current CAM systems typically consist of a database and a set of modules that perform engineering data collection, WIP tracking, scheduling (of lot movement and equipment maintenance) and other ancillary functions. Figure 2 shows how CAM functions relate to one another and to a central database.

CAM systems offer the potential for technical problems to be more easily solved; resulting in fewer misprocessed lots, shorter cycle times and increased yield. Increased equipment utilisation is also possible by using non-lot tracking and scheduling. All of these factors have a large impact on the economic viability of IC manufacturing. However, to the user the performance of a CAM system is more dependent on the integrity and accessibility of data. Thus in a commercial CAM system the user interface and the robustness of the database are very important features.

Despite the benefits provided by currently available CAM systems, they are only reactive offering no predictive capabilities for active process control.

MODELLING WAFER FABRICATION

Current modelling methodologies can be regarded as being of two types: statistical and physical. The former is dependent on there being a large body of characterising data available and can only give reliable results within the bounds of that characterisation. The latter consists of models which describe the effect each process-step will have on the surface of a wafer. While these models are very sophisticated they must be used with a degree of care. To obtain accurate results the model parameters must be tuned to the particular environment which they are to simulate. Alternatively they may be used in a differential mode to examine the kind of effect that variations in process parameters will have on the electrical characteristics of the finished devices.

Process simulators can currently model one- and two-dimensional sections through a wafer. For example, in an nMOS process there are regions that can be simulated to gain an understanding of the whole process. Figure 3 shows a two-dimensional plan where four different one-dimensional sections are indicated. All four of these must be simulated to fully model the fabrication process. 1-d simulations provide less information than 2-d but they are also much lighter on computing resources. It is only when analysing very small geometry devices that it is essential to use 2-d simulators, so for most applications 1-d simulators can be used to identify significant trends.

SUPREM-II is a widely available 1-d process simulator that can model a subset of the manufacturing operations which are performed in wafer fabrication, see Antoniadis and Dutton (2). This capability makes it suitable for estimating electrical characteristics such as threshold voltages and sheet resistivities. Figure 4 shows the SUPREM-II doping profile of the depletion section of figure 3.

Historically process simulators have been used for process development and optimisation. However they can potentially be used for analysis of processing during routine production.

INTEGRATING PROCESS SIMULATION AND CAM

From our discussion of wafer fabrication it is evident that identifying processing errors and being able to perform corrective processing are important to the semiconductor industry.

CAM systems collect engineering data and so can be used to identify processing errors. Process simulators can then be used to verify current processing and investigate the effect of future operations. However currently available process simulators are not suitable for integration into a CAM system: both because of their user interface and because they are inherently batch operating programs.

We have developed a new system by integrating process simulation with a commercial CAM system - COMETS. For the first time, within a manufacturing environment, real-time analysis of processing is possible and feed-forward control can be performed. This has been achieved by developing a black-box system which links the CAM system and the simulator SUPREM-II. This has been implemented by using the *user-exits* provided within COMETS so that it was not necessary to modify its code. The new module is called SIM and interfaces with some of the existing modules, as shown in figure 5.

To make the process simulator more accessible to the process engineers in the clean-room the CAM system must act as the operating environment for the simulator. Therefore the data for controlling the simulations has to be associated with the process definition in the database. However the database could not be modified otherwise the CAM system would no longer be the standard commercial version. Thus the control data for the simulator has been appended to the process recipe files which are part of the process specification and are associated with the database. Figure 6 shows such a recipe file.

The user interface must also appear as if the simulator is part of the CAM system. Thus the interface of the SIM module is an extension of the menu structure of the CAM system. Figure 7 shows the menu structure and the menus themselves. Note that each menu gives access to a number of functions. The Simulation Main Menu allows access to the Product Simulation Menu and the Lot Simulation Menu as well as an interactive version of SUPREM-II (INTERSUP). This interactive code was specially developed for this work.

The Product Simulation Menu allows the fabrication of a whole product to be simulated and the results inspected. The Lot Simulation Menu contains functions which allow *look-ahead* and *what-if* type simulations to be used for investigating various processing scenarios. The functions of this menu are supported by another component of the SIM module which maintains simulation histories of all of the lots processed so that the effect of processing on each lot can be inspected as well as be used as a starting point for further investigation.

APPLYING PROCESS ANALYSIS/CONTROL

The SIM module may be used to perform diagnostic analysis and feed-forward control for lots which have been misprocessed. For a high volume manufacturer this is useful when implementing a new process and for generally increasing the understanding of the process. However for a low volume manufacturer, eg. one producing Application Specific ICs (ASICs), it is particularly important that any misprocessing should be corrected immediately. This is because a product might only ever be fabricated once, so if an error does occur and is not corrected then delivery could be delayed while another lot is processed.

To demonstrate how the SIM module can be employed, the EMF 6 micron nMOS process will be used as an example. During this process an oxide is grown to form the transistor gate. Under normal conditions this should be 640 Å thick, but if the lot is left in the furnace too long then a thicker oxide will result. The consequence of this occurring is that a device at the end of the process will have a higher threshold voltage, which could lead to the ICs failing their final test.

Figure 8 shows a sequence of actions that could be taken when using the SIM module. Once a processing error is identified the first step is to resimulate the process-step until the simulated results match those measured. Then one can look-ahead to the end of the process and examine the final electrical characteristics against the specification. Should this processing result in a threshold voltage outside the desired range then changes to the processing parameters can be investigated. These are known as what-if simulations: what if the lot is reworked, removing the oxide grown so far and growing it again; or, what if a later process-step is modified to adjust the threshold voltage by introducing some additional dopant? After this a suitable change to the process could be made, ie. feed-forward control. If none of these options are feasible then the lot will have to be scraped but at least this is in the light of examining all the engineering options.

Thus the SIM module can be used to analyse processing in real-time for routine production, and for diagnosing corrective processing.

CONCLUSIONS

In this paper we have introduced some of the problems faced by the semiconductor industry and shown how these can been met using advanced manufacturing technology. We have also demonstrated that it is possible, not only to use CAM for the reactive control of the clean-room, but also for active feed-forward control; by using process simulation to verify and predict the effect of operations on individual lots. This has been achieved by the development of a new module, called SIM, which gives the process engineer access to the simulator as if it were part of the CAM system. It uses data held within the CAM system to control the simulations and makes available look-ahead and what-if functions. These allow interactive investigation of the process within a manufacturing environment. The application of this module to controlling a typical process has been presented and it emerges as an important tool for low volume ASIC manufacture.

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2. Antoniadis, D.A., and Dutton, R.W., 1979, IEEE Trans. on Electron Devices, Vol. ED-26, No. 4, 490-500.

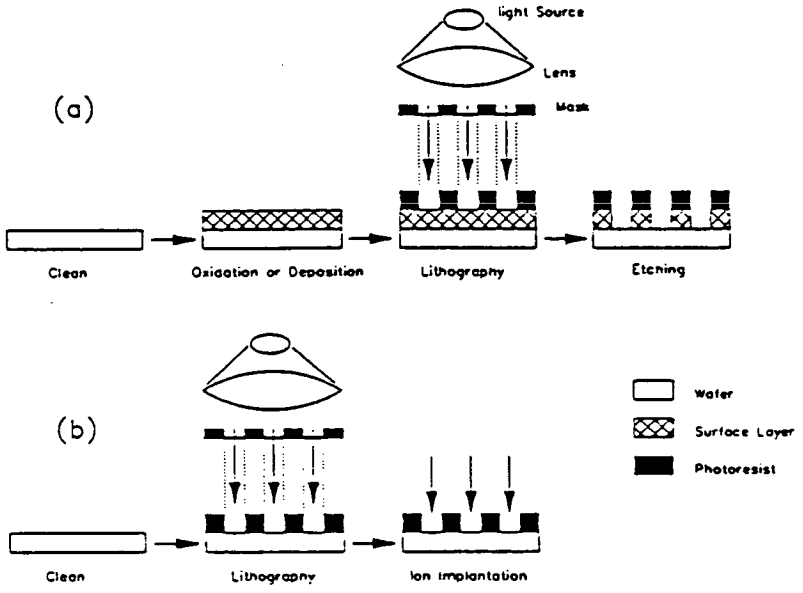

Figure 1. The two major process sequences in integrated circuit manufacture.
(a) Layer definition. (b) Introduction of chemical dopant.

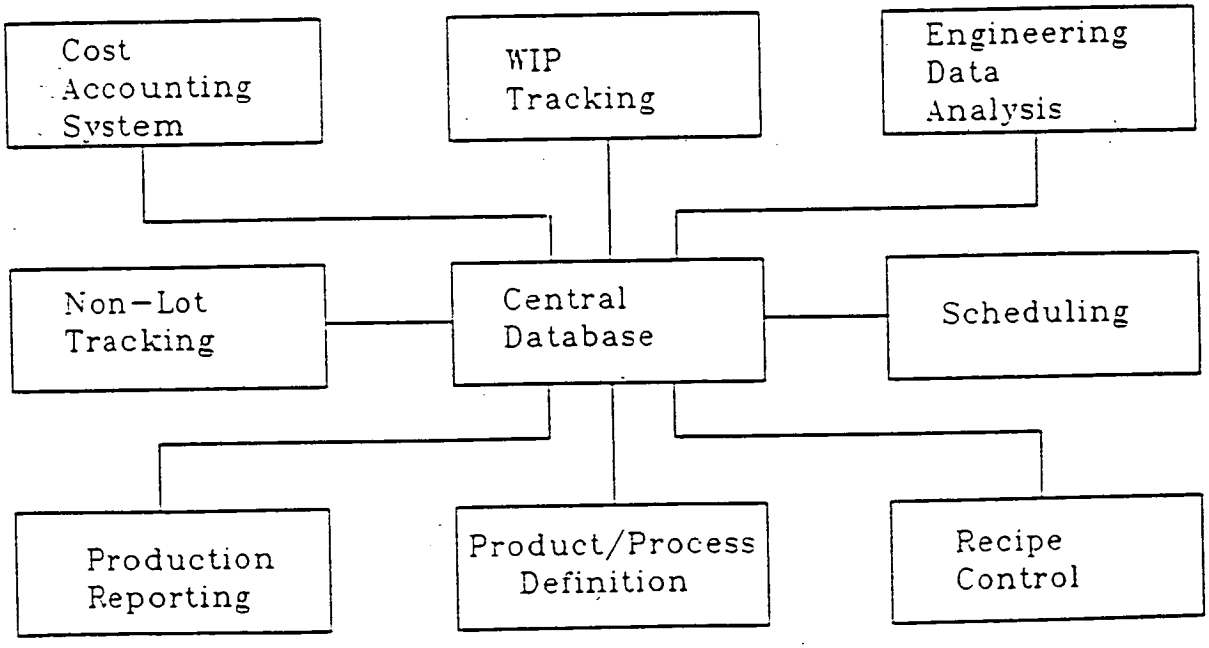

Figure 2. A CAM system consisting of a central database and a set of functional modules.

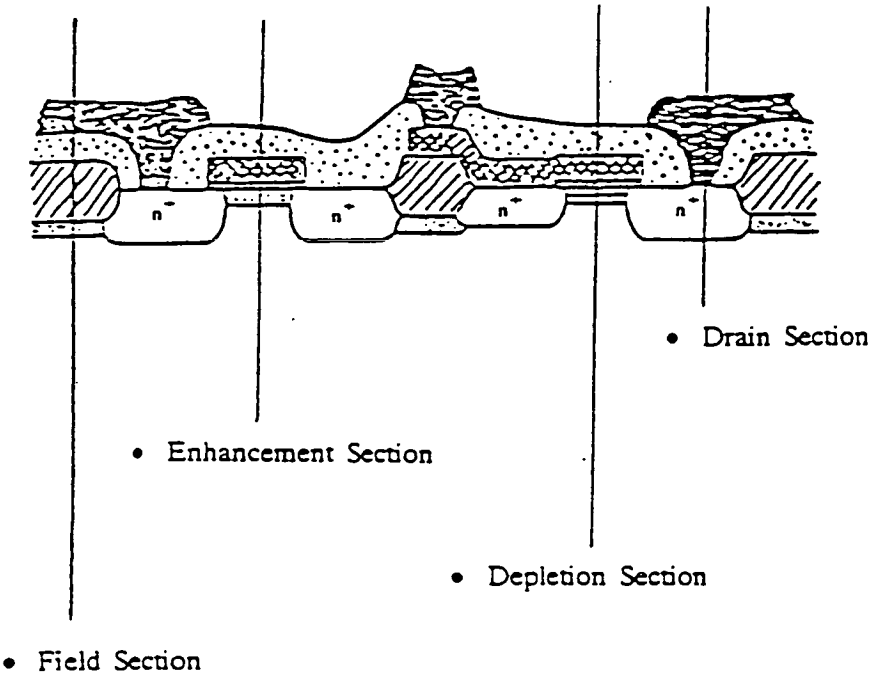

Figure 3. Plan of typical nMOS devices showing 1-d sections required for full simulation of process.

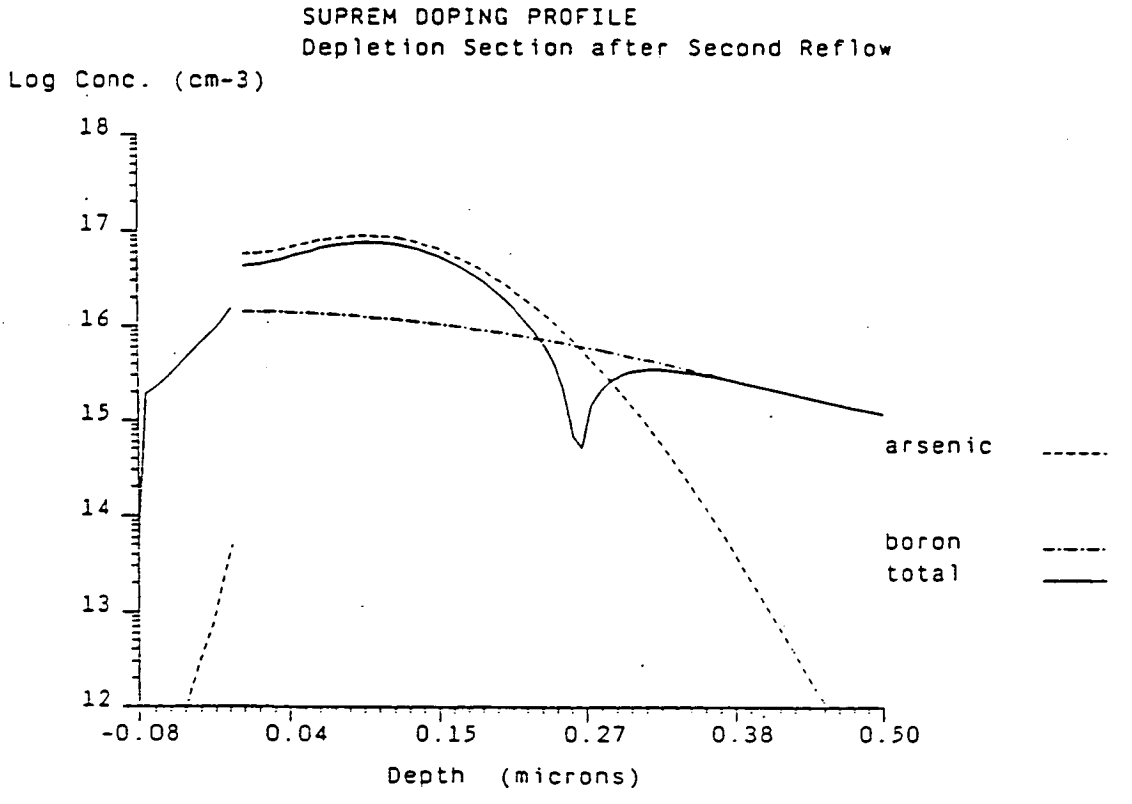

Figure 4. A one-dimensional device doping profile produced by SUPREM-II.

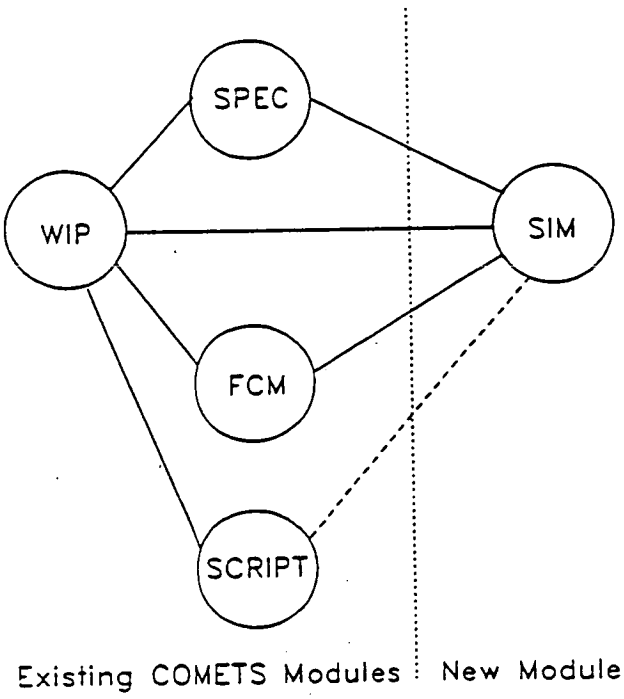

Figure 5. The SIM module interfaces with some existing CAM modules: WIP - work-in-progress tracking module; SPEC - recipe maintenance module; FCM - factory communications module; SCRIPT - process-step action sequencing module.

GATE OXIDE

Furnace 1. 950oC. idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
17min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure: oxide thickness

```
** FIELD
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
** DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
```

Figure 6. Recipe file defining process-step with appended simulation control data.

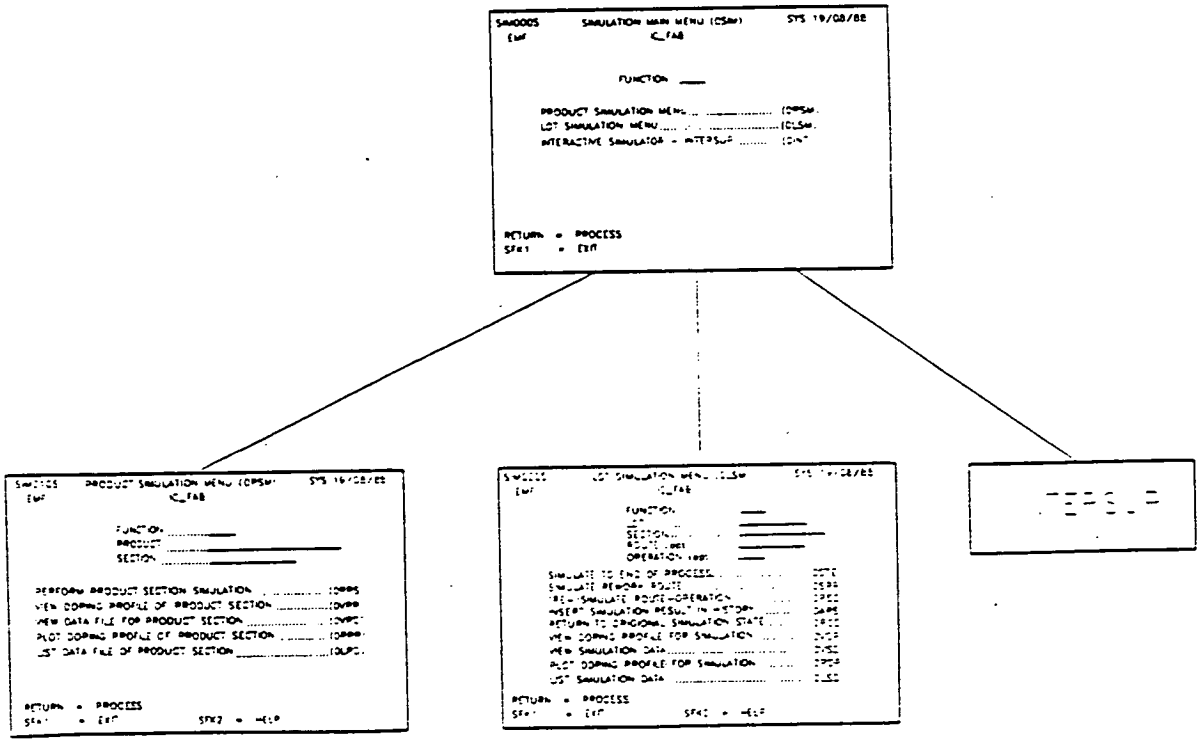

Figure 7. Menu structure of the SIM module.

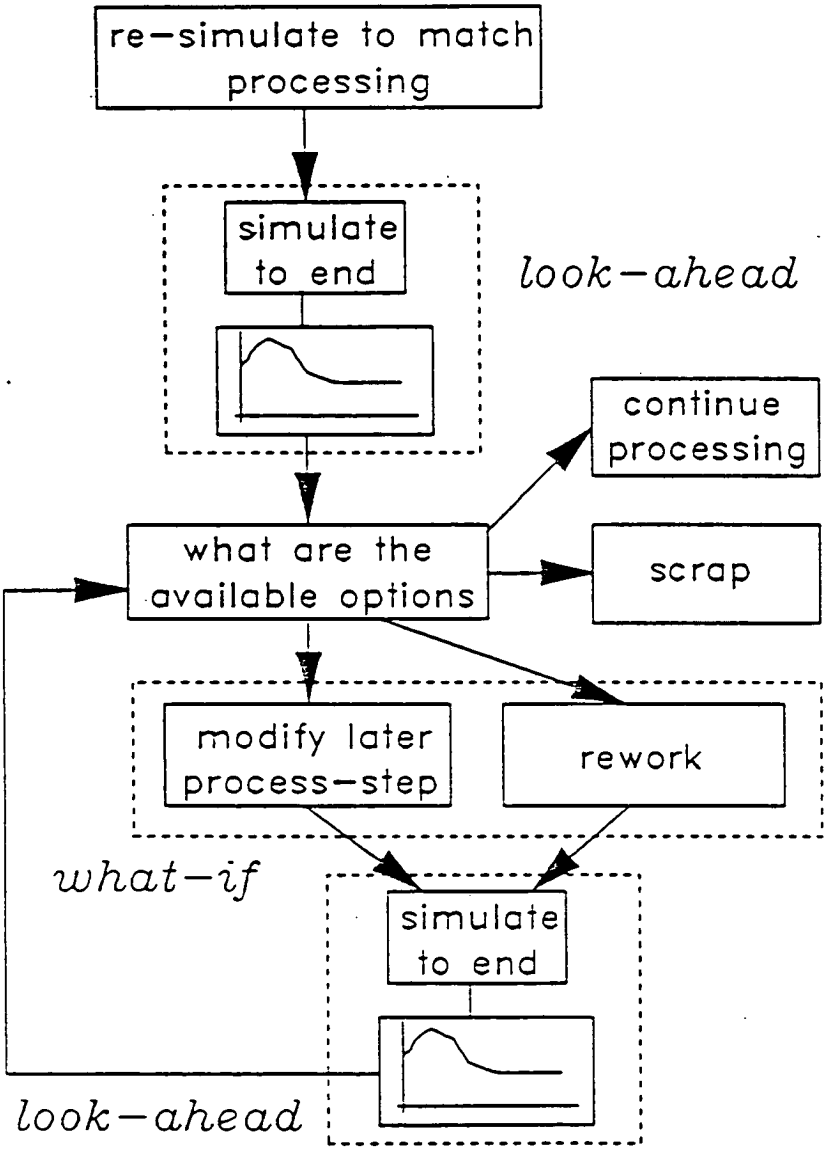

Figure 8. Flow diagram showing sequence of actions taken when using the SIM module.

Integrating Computer Aided Manufacturing and Process Simulation

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1. Introduction

Computer Aided Manufacturing (CAM) systems have become widely used throughout the semiconductor industry and have great potential for improving the efficiency of the manufacturing process [1]. This is largely due to their ability to track the movement of batches, store the relevant processing data, and allow ready access to this information. However currently available CAM systems do not provide the type of tools which are required for real-time analysis and control of a flexible processing environment. Such an environment is application specific integrated circuit (ASIC) production where there can be a large number of products and even processes [2].

This presentation describes the integration of process simulation and CAM to produce a system capable of diagnostic process analysis and feed-forward control. Though process simulation has historically been used in the development and characterization of processes, this is its first application to a manufacturing environment. The use of process simulation is significant because it is the only way in which semiconductor processing can be modelled. Consequently it can be used to verify processing and predict the effect of future operations.

The integration of CAM and process simulation has been implemented using the CAM system COMETS and the process simulator SUPREM-II. The combination of COMETS and SUPREM-II allows on-line interactive access to powerful 'look-ahead' and 'what-if' functions for diagnostic analysis of processing. The advisory aspect of the system, in conjunction with these functions, identifies batches which have been misprocessed and are likely to have unacceptably low yields so that, if possible, feed-forward control can be applied to perform some corrective action. The control files for the simulator are generated from data held within the CAM system.

This paper first considers the potential role of process simulation in a production environment. It then describes how the SIM module has been implemented to make simulation available for diagnostic analysis and control of IC fabrication. An example application is discussed to outline how this module might be used to aid the control of the fabrication of lots on an nMOS process. Finally some extensions to the recipe management capabilities of COMETS are introduced.

2. Process Simulation

Process simulation has historically been used for the development and optimisation of new processes. In this environment both one- and two-dimensional simulators are now widely used [3-5]. However their application to manufacturing has been with simulators using statistical [6, 7] rather than physical modelling. The significance of introducing physical modelling of wafer fabrication into a manufacturing facility is that the input parameters to these models can be easily related to the parameters of the process recipe.

In this paper we show how SUPREM-II [8] has the potential to be used for diagnostic analysis during routine production. SUPREM is a 1D simulator which is capable of predicting the physical characteristics of semiconductor device structures during fabrication Although short channel devices require the use of 2D simulation, it is still possible to obtain a good understanding of process fundamentals by using a one-dimensional simulator. If it has been well calibrated [9] then it is possible to use it to get meaningful absolute values for physical and electrical device parameters. In a differential mode the simulator can be used to investigate how perturbations of process variables from the mean will influence the process as a whole.

The use of SUPREM within a manufacturing environment is complicated by both its user interface and by its batch type operation. However it is fast enough to be used in real-time which makes it very suitable for this application. No conceptual difficulties exist in replacing this 1D simulator with a 2D simulator such as SUPREM-IV or SUPRA. With currently available computers the additional CPU time required to perform 2D simulations prevents them from being used in an interactive fashion. It is expected that in the future faster machines will become available at a reasonable cost which should help to make 2D interactive process simulation generally available.

In order to characterize a process with a 1D simulator it is necessary to model a number of sections. Figure 1 shows the sections required for an nMOS process. To fully simulate fabrication using this technology all applicable sections must be simulated for each process step. For example, a gate oxidation will not only oxidize the channel regions of transistor devices but also the field, source and drain regions. In addition the thermal component of the oxidation will cause a redistribution of dopants throughout the wafer.

The output generated by SUPREM provides information on a number of features of the device structure being simulated. This includes charge densities, layer thicknesses, junction depths, sheet resistances and dopant distributions. An example of some of the output which is available is illustrated in figure 2. For process verification such information can be very valuable. This is because simple on-line measurements, either *in-situ* or after a process step, do not normally provide information on dopant distribution through the substrate. Measurements which can provide this sort of information are typically performed off-line as they are either destructive or require extra masking layers. Wafers that are used for these measurements are therefore unable to yield product.

3. Implementation

When developing the enhanced system to integrate process simulation and COMETS three goals were set for its functionallity. These were:

1. To make process simulation available for diagnostic analysis of processing in a manufacturing environment.
2. To help provide the process engineer in the manufacturing environment with a greater understanding of the relationships which exist between the process steps.
3. To allow feed-forward control in real-time.

To achieve this level of functionallity a software module, called SIM, was developed. As figure 3 shows, the SIM module interfaces with a number of other COMETS modules.

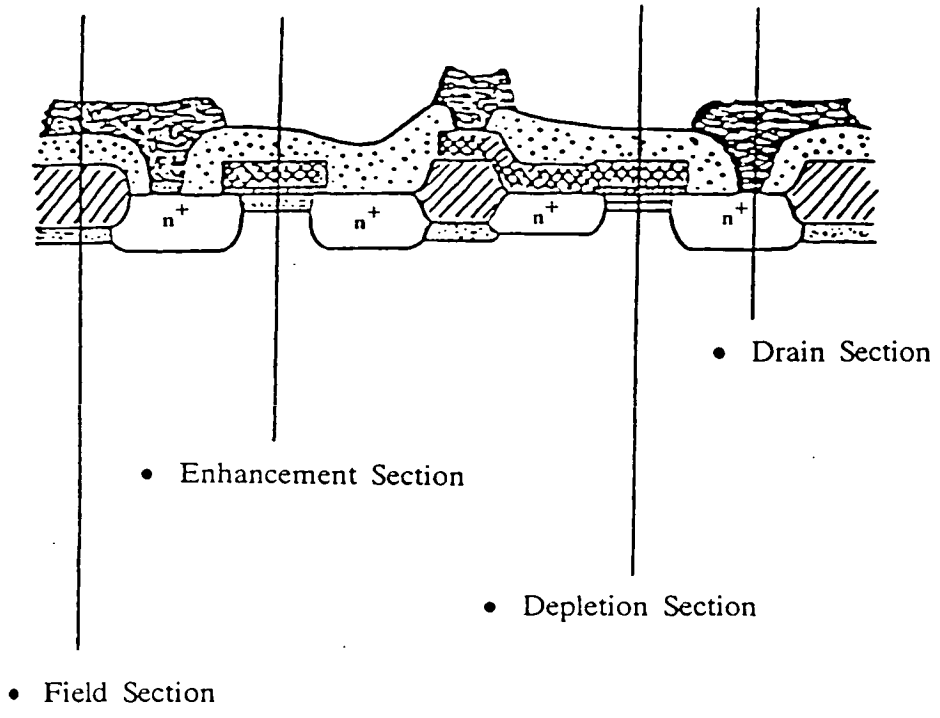

Figure 1 Plan of nMOS inverter structure
with four 1D sections indicated.

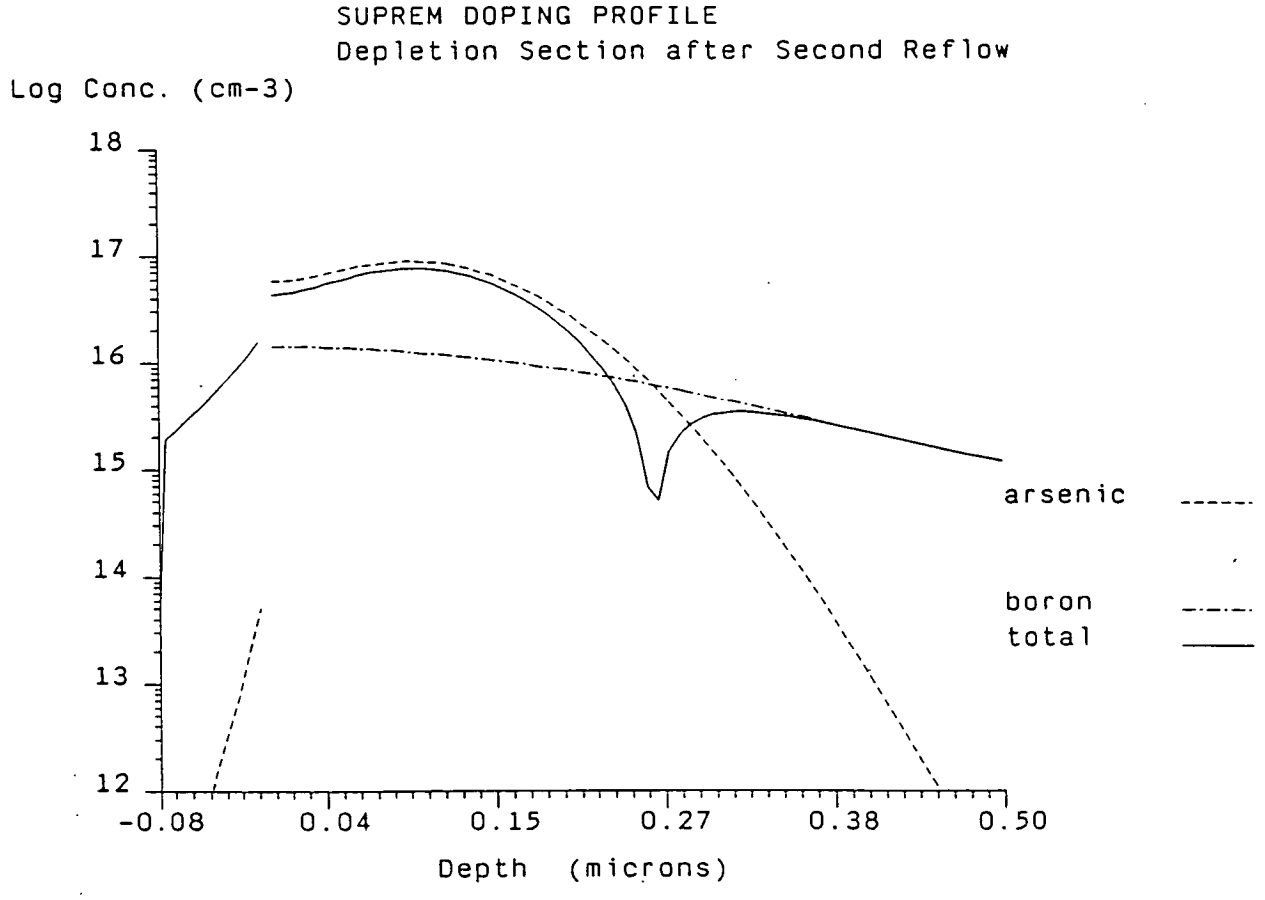

Figure 2 SUPREM doping profile for the depletion section
of a nMOS transistor.

Each of these modules (WIP, SPC, FCM and, optionally, SCR) are required for the SIM module to work.

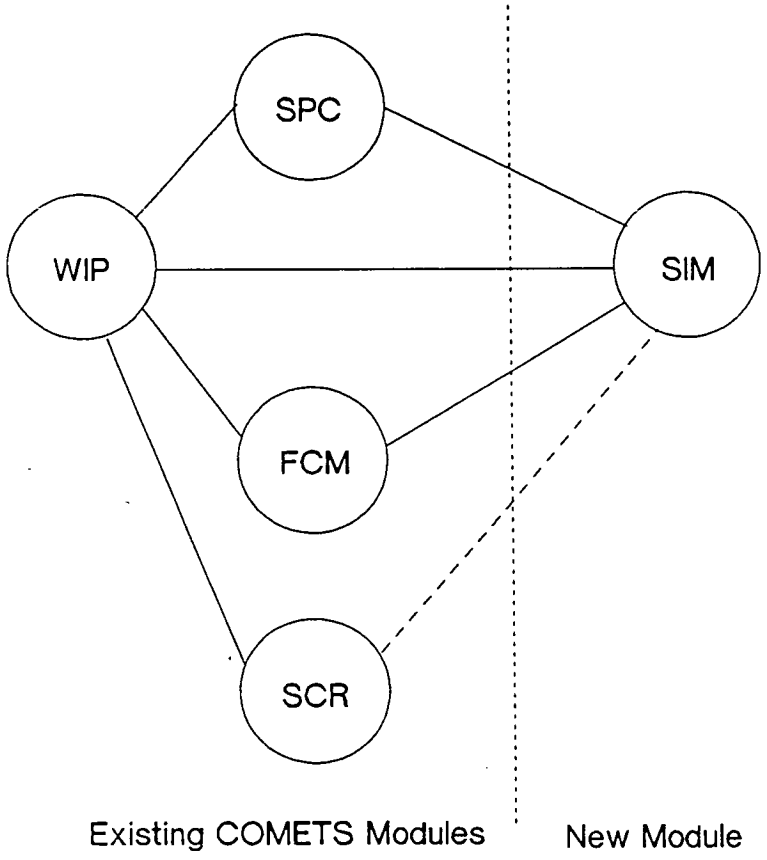

Figure 3 The SIM module integrates with the Work-In-Progress (WIP) Tracking module, the Specification (SPC) module, the Factory Communications (FCM) module, and the SCRIPT (SCR) module.

To maintain the integrity of the COMETS system and to allow for upgrades, SIM makes extensive use of the user exits and the General Tables System (GTS). The code is written in Cobol with the exception of some Fortran graphics routines. When interfacing with the VAX/VMS operating system, logicals and routines from the Run Time Library (RTL) are used.

From the point of view of the user, SIM consists of four parts:

1. In-process simulations which are used to maintain a simulation log of the processing for each lot.
2. The product simulation menu which allows the processing of individual products to be simulated and the results inspected.
3. The lot simulation menu which allows 'look-ahead' and 'what-if' simulations of individual lots to be performed and the results inspected. It also allows the simulation histories of lots to be investigated.

4. The program INTERSUP which allows SUPREM to be used interactivly.

The in-process part of the SIM module was developed to integrate CAM and process simulation at the level where the CAM software actually interfaces with the processing of lots in the clean-room. Therefore, the process step of SUPREM required an equivalent object in the COMETS database; the most obvious candidate being ROUTE-OPERATION. Figure 4 shows a simple data model of the objects used within COMETS for WIP tracking. It is also necessary to be able to specify the one-dimensional sections simulated by SUPREM. These are defined by the identifier SECTION.

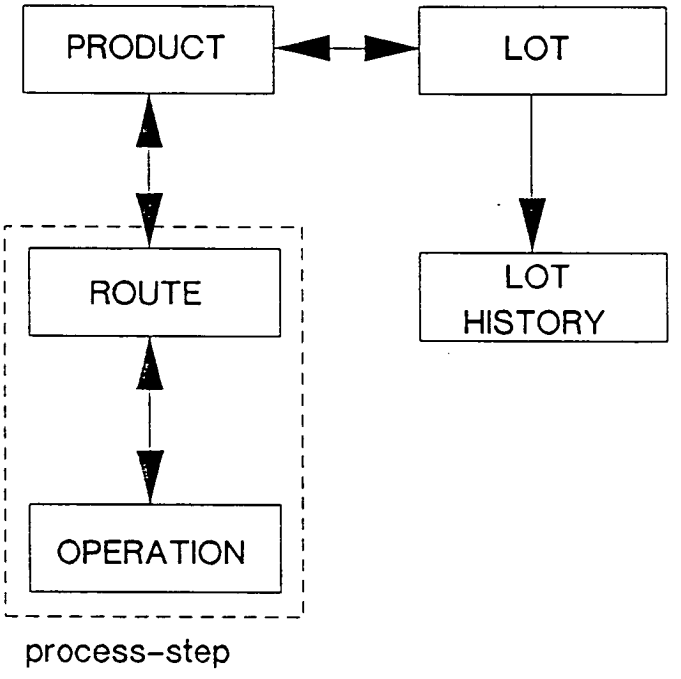

Figure 4 Data model of objects used by the COMETS WIP module.

The MVIN function was chosen to be the point where a process step should be simulated since it is a WIP function which can always be associated with a ROUTE-OPERATION, and is called prior to any processing of a lot being performed. Within the MVIN code, two user exits are available: USR500 and USR010. The latter was chosen to attach the simulation code as USR010 is called only once, whereas, because of the review facility, USR500 could be called many times, causing many unnecessary simulations to be performed.

To automatically simulate each step, the data to run SUPREM has to be stored in the CAM system without modifying the database. Using the GTS for this purpose was explored but proved to be restrictive on the way data was stored and it was also awkward to use. Instead the text files of the SPC module were chosen because they do not restrict the format or number of SUPREM statements required to simulate a process step and also enforce some structure on the way simulation control data is maintained, ie. through the AUTHORIZATION, SCANNING and FREEZING of SPECS. SUPREM processing

statements are added to the bottom of each SPEC file as show in figure 5. Four sets of SUPREM statements are required to define an nMOS process (field, source-drain, enhancement channel and depletion channel), each is preceeded by a line with two stars and a character string. The stars identify the beginning of each SECTION and the character string is the SECTION-NAME. As with the MVIN function, SPEC files can be associated with ROUTE-OPERATIONS.

```
GATE OXIDE

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen        20%    (1.5  l/min.)
HCl           15%    (0.15 l/min.)
Hydrogen      10%    (1.7  l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
2.2 min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure: oxide thickness


** FIELD
STEP TYPE=OXID,TEMP=950,TIME=12.2,MODL=NIT0
** DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
** ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
** SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=2.2,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY0
```

Figure 5 A recipe file for gate oxidation which has been extended for use with the SIM module.

As a lot is completing the MVIN, control is passed to the user exit, this calls the simulation routine for each SECTION in the ROUTE-OPERATION SPEC file which validates the SECTION-NAME against a table - SIM$SECTIONS - in the GTS. The SUPREM

input file is generated from both the SPEC file and data held in the PRODUCTS user defined fields. A sub-process is then spawned to run SUPREM. All the files generated are in a directory pointed to by COMETS$SIMULATIONS, with each set of files having a unique identifying prefix. This is formed from the LOT-NUMBER, the SECTION-NAME, the ROUTE and the OPERATION. Each simulation run produces four files, denoted here by their suffixes:

.LIS - which is the SUPREM input file.

.DAT - which is the data file produced by SUPREM.

.SAV - which contains the structure of the section after the current simulation step. The next step for this lot and section will use this data as a starting point.

.LOG - contains the completion status of the simulation.

Feedback to the operator is confined to messages written to the bottom of the screen announcing the completion of each simulation. In the event of an error occurring during the simulation a mail message is sent to the user names held in the FCM table called SIM$MAIL.

When processing is being controlled using SCRIPT, the START instruction must be used in order to perform the in-process simulation. Following this, the CALL USER ROUTINE instruction may be used to produce, on a graphics screen, a plot of the doping profile for the current LOT. For example:

CALL USER ROUTINE "PROFILE ENHANCEMENT"

where ENHANCEMENT is the name of the SECTION. When this facility is used the user exit USR018 calls routines in the SIM module to actually produce the plot.

The product simulation menu, lot simulation menu and INTERSUP are accessed through the simulation main menu which is in turn accessed through the user main menu, ie. the user exits USR001 and USR002. Figure 6 shows the menu hierarchy and screens for this module.

Under the Product Simulation Menu (0PSM) there are five functions:

0PPS - Perform the process simulation for a given PRODUCT and SECTION.

0VPP - View the doping profile produced by this simulation.

0VPD - View the data file produced by this simulation.

0PPP - Write the doping profile to a file in a format suitable for a hardcopy device.

0LPD - List the data file on a hardcopy device.

0PPS acts in a similar way to that of the in-process MVIN simulation, except that rather than generating an input file for one process step, it compiles all the SECTION data for a PRODUCT into one file before spawning a simulation run. This function is of particular

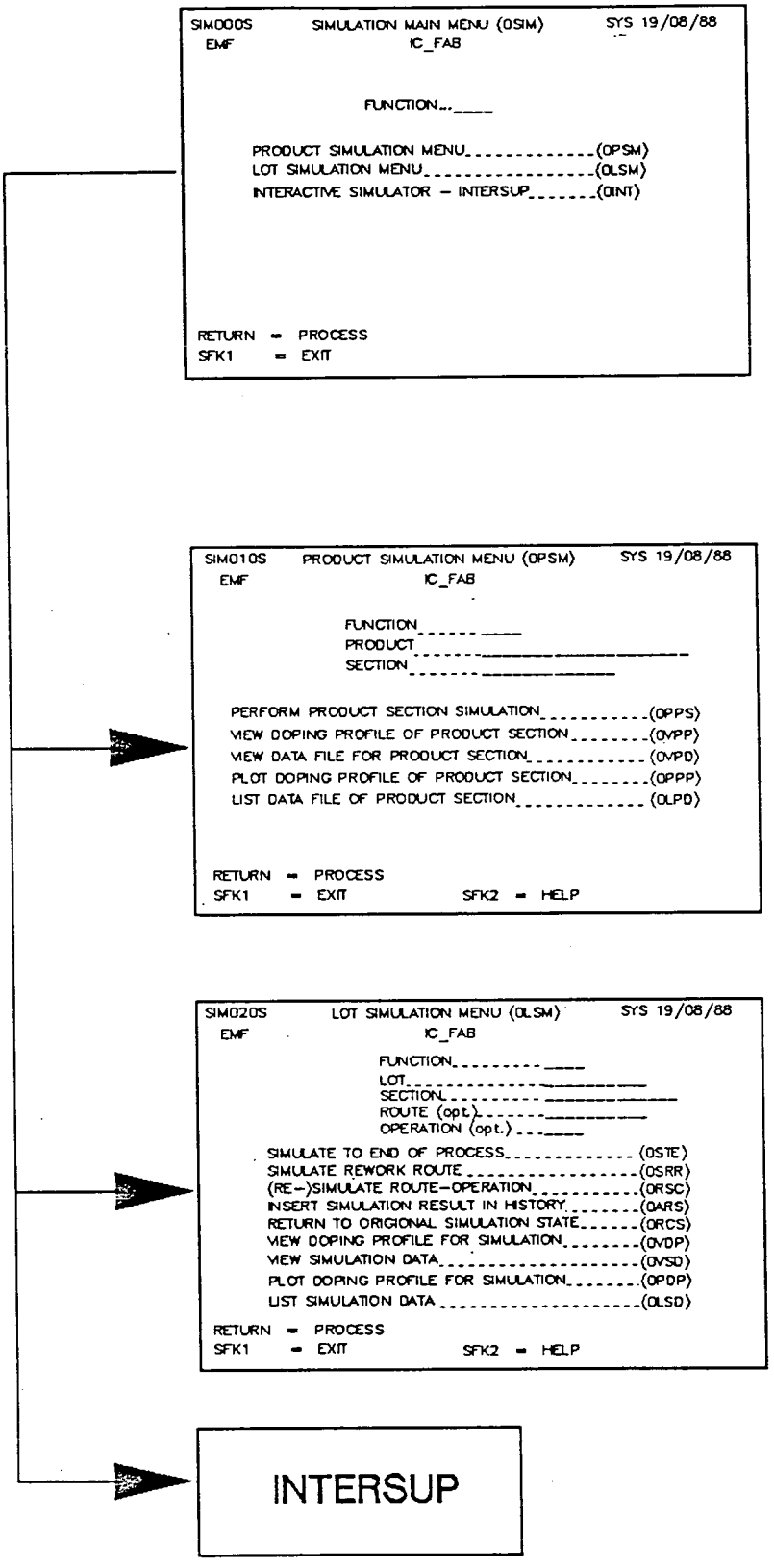

Figure 6 The SIM module menu screens and hierarchy.

benefit where processes are variable and therefore fabrication sequences may require verification.

Under the Lot Simulation Menu (0LSM) there are nine functions:

0STE - Simulate to the end of the process for a given LOT and SECTION.

0SRR - Simulate the processing of one SECTION of a given LOT on a specified rework ROUTE.

0RSC - (Re-)simulate a process step for a given LOT and SECTION (Assumes last simulated process step unless ROUTE and OPERATION are specified).

0ARS - Associate the simulation data produced by 0RSC with the appropriate lot history.

0RCS - Return the state of the current simulation to that of the last process step simulated.

0VDP - View doping profile for a given LOT and SECTION (Assumes last simulated process step unless ROUTE and OPERATION are specified).

0VSD - View the data file for a given LOT and SECTION (Assumes last simulated process step unless ROUTE and OPERATION are specified).

0PDP - Write file containing doping profile for a given LOT and SECTION in a format suitable for a hardcopy device (Assumes last simulated process step unless ROUTE and OPERATION are specified).

0LSD - List data file for a given LOT and SECTION on a hardcopy device, via the queue SYS$PRINT (Assumes last simulated process step unless ROUTE and OPERATION are specified).

0STE, 0SRR and 0RSC provide powerful look-ahead functions for the process engineer. These functions allow investigation of how further processing will affect a lot. For example, the final electrical parameters of a lot may be compared with the process specifications. A variety of future scenarios (what-if simulations) can then be explored by using 0RCS after each set of simulations in order to reset the last simulation for this LOT and SECTION to that of the last process step simulated. When 0STE is called after 0SRR, for a given LOT and SECTION, the current process step is included in the simulation. 0RSC provides the process engineer with the ability to re-simulate a process step when a simulation has either previously failed or the lot has been misprocessed. This is done by modifying the SUPREM statements in the input file. The results of the simulation are then associated with the lot history by calling 0ARS which repositions the '.LIS', '.DAT', '.SAV' and '.LOG' files in the simulation history directory (COMETS$SIMULATIONS).

The final part of the SIM module is INTERSUP, a program which allows SUPREM to be used interactively. INTERSUP can be used to develop a description of a process, which may then be entered into the SPEC files for the ROUTE-OPERATIONS of the PRODUCTS fabricated by this process.

All the data files used by the functions of the lot simulation menu, the product simulation menu and INTERSUP are stored in the users current directory. This protects the files in the simulation history directory from being modified unintentionally. The only way

in which data files can be inserted into the simulation history directory is by using the associate simulation history (0ARS) function after the re-simulation (0RSC) of a process step.

4. Application of the SIM module

In order to demonstrate how the SIM module can be used in a manufacturing environment the processing of a lot on the EMF 1.5 micron nMOS process will be used as an example.

Once the SIM module has been installed at a site, it requires a number of set-up steps to be performed for each FACILITY for which it is to be used. These are:

1. The valid SECTIONS for the FACILITY must be defined by creating the table SIM$SECTIONS in the GTS.
2. The SIM$MAIL table, in the FCM, must contain the user ids of those who should be mailed if an error condition occurs during an in-process simulation.
3. New versions of the SPEC files used during this process must be created so that each ROUTE-OPERATION which is to be simulated has the corresponding SUPREM statements in its SPEC file.

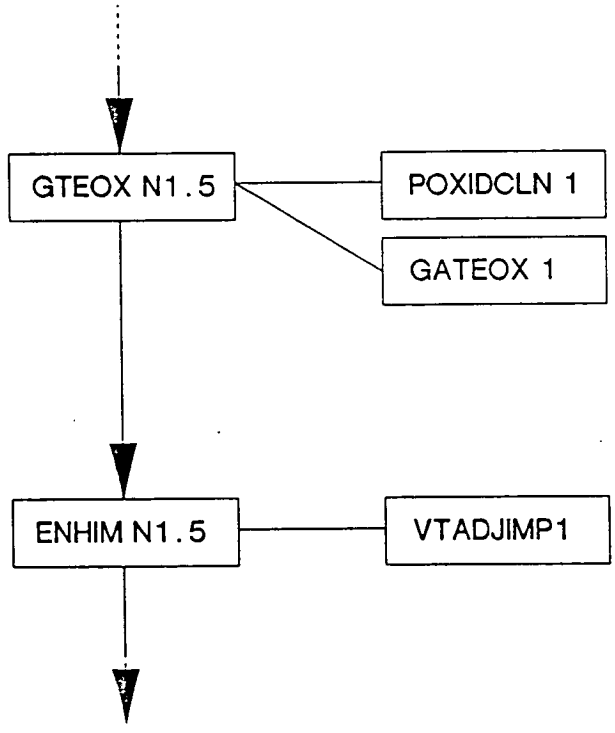

Figure 7 An extract from the process sequence for the EMF 1.5μm nMOS process as defined within COMETS.

The lot to be processed is created within COMETS and its fabrication is tracked through the process sequence. If, for example, when the lot reaches OPERATION 'GATEOX 1' on ROUTE 'GTEOX N1.5' (figure 7) it spends too long in the oxidation

furnace resulting in a gate oxide thickness outside the specified range then the lot will be put on hold. The engineer responsible for this part of the process can then use the functions of the SIM module to explore the available options.

Figure 8 shows the sequence of steps which can be performed using the SIM module to analyse the problem. The first action is to re-simulate the current process step so as to simulate the processing which actually occurred. The re-simulated results for this process step can then be associated with the history of the lot.

The extra time which the lot has spent in the furnace will not only effect the gate oxide thickness but also oxides in other regions and the distribution of dopants throughout the wafer. The modified doping profile and increased oxide thickness will effect the threshold voltages of both depletion and enhancement devices, the extent of this can be checked using the look-ahead function.

If the threshold voltage of the depletion and enhancement devices is found to be out of specification then the processing for this lot can be modified. It may be possible to modify the following boron implant, or it may prove necessary to rework the lot. A series of what-if simulations can be performed to investigate how these options will effect the threshold voltages of the devices and the other physical and electrical parameters.

In this way the SIM module can be used to analyse the processing of individual lots and potentially be used to modify later processing, ie. feed-forward control.

The application discussed above is relevant to any fabrication facility. However it is potentially most relevant in an ASIC environment where a particular product may only be fabricated once. In this case it is important that the lot is fabricated *right-first-time*. However if misprocessing should occur then the decision to continue processing or to scrap the lot would have to be made quickly. In this case the SIM module would act as a decision support tool allowing the process engineer to make decisions after having rigorously explored all the options. This is important since scrapping potentially good product and processing non-functional wafer are both expensive alternatives.

Another application exists in the transfer of a process from a development to a production facility. The SIM module could be used to document the new process and the interrelation of process steps. This approach puts much of the knowledge built up during the development phase into the CAM system. As a result the production engineers have easy access to information which should help in the implementation of new processes.

5. Further Developments

Although the SPC module allows a high degree of flexibility in defining processing instructions it places this information outside the database in simple text files. The result is that there is no inherent structure in the process recipes and therefore the data can only be accessed by a system which is capable of a high level of pattern recognition and analysis; for example, a person. Thus the recipe data that is used by the operators cannot easily be accessed by the SIM module.

A new module, called RCP, is currently being developed to tackle this problem. The aim of this module is to replace the SPC module with a system which keeps the best features of SPC but is able to reduce the maintenance overheads, simplify process definition/control, and improve flexibility. To give this system the widest possible applicability no IC fabrication specific terminology is being hard-coded in. Therefore this module

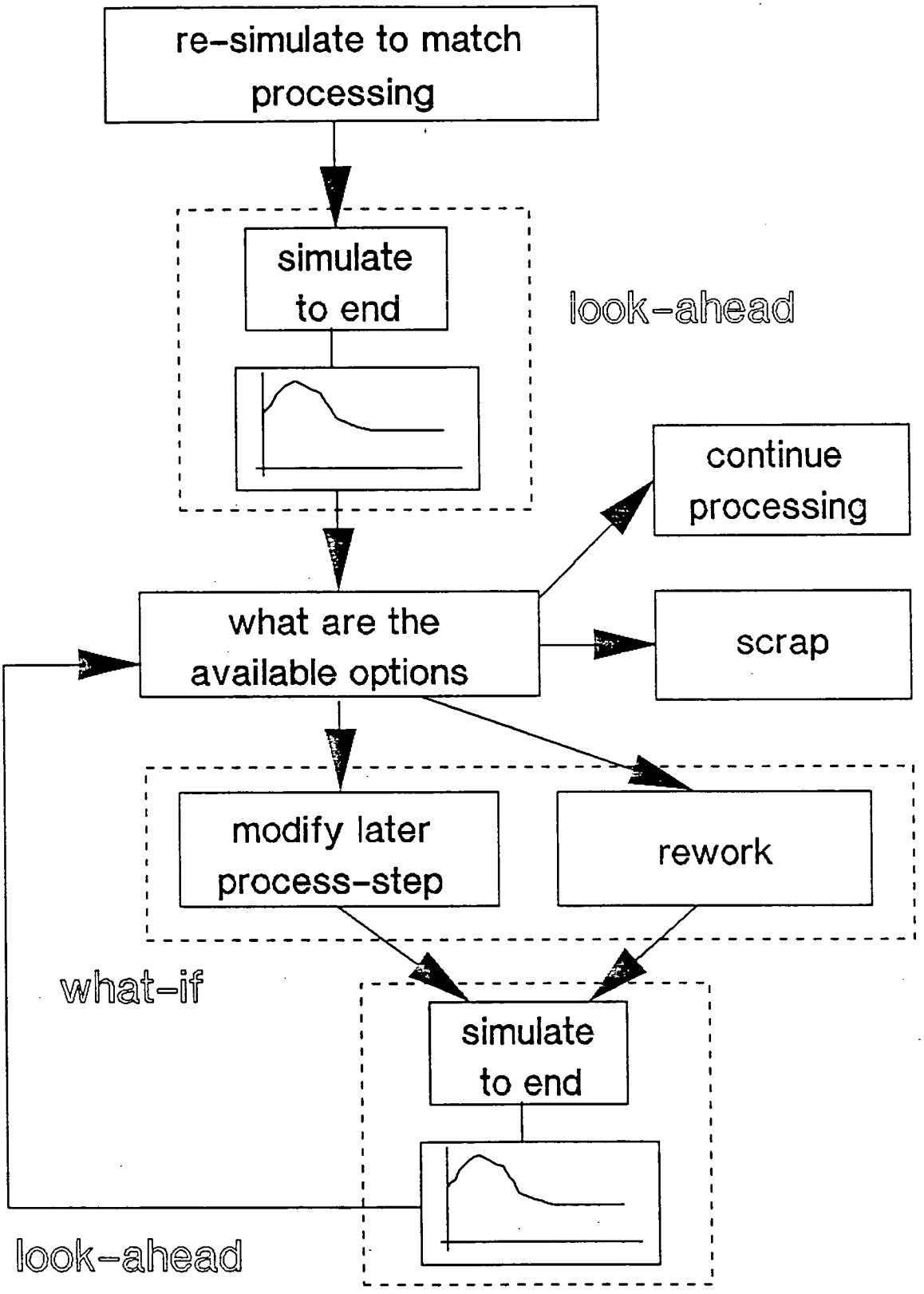

Figure 8 Flow diagram describing application of the SIM module.

should prove useful in IC fabrication, test, assembly and even aerospace and chemical production.

The implemented module is anticipated to use COMETS like menus and present information to the operators in a familiar way. The storage of data will be split between the database and a set of text files. Within the database will be held the equipment control parameters. The text files will be used to store equipment set-up instructions, safety information and graphics, much in the same way as current SPEC files do. Security for the definition of control parameters is being treated in the same way as the existing security of product, route and operation definition. Overrides will also be possible using this system but whereas for the SPC module these had to be set *a priori* they may now be set when and where they are required. The processing data, or recipe, used at each ROUTE-OPERATION for a LOT will be appended to its LOT HISTORY.

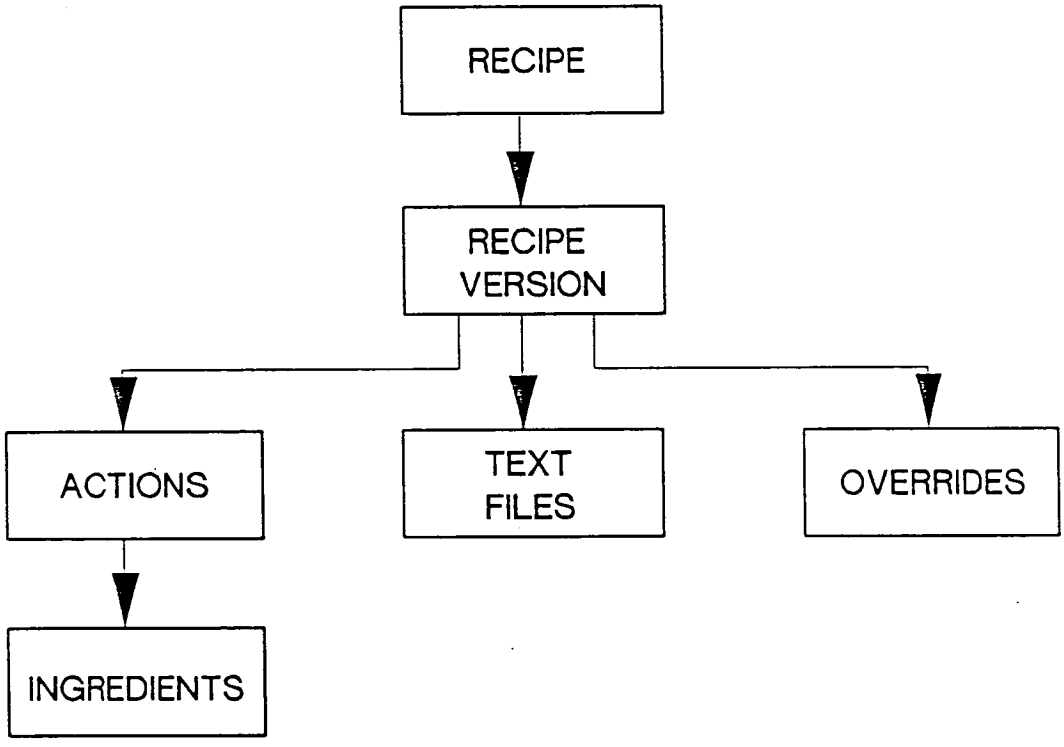

Figure 9 Data model for the RCP module.

Obviously this approach to recipe management will require some modifications to the COMETS database. Figure 9 shows the anticipated structure for the data required by the RCP module. Each process recipe may have a number of versions with associated text files. The equipment control data consists of individual control parameters, such as the temperature, time and gas flow rates for a furnace. However, to extend this example, a process step for a furnace will include ramp-up and ramp-down phases as well as the furnace operation itself. Within the structure of figure 9 this could be represented by having a ramp-up ACTION, a process ACTION, and a ramp-down ACTION. Each of which will

have its own INGREDIENTS or equipment control parameters. Although this example is for IC fabrication this structure is flexible enough to be used to represent virtually any process. Performing overrides of the standard process recipe for a particular product, lot, etc., is catered for by the OVERRIDE data object which also has its own set of ACTIONS and INGREDIENTS. Since the OVERRIDE is within the database it can be applied whenever required without the need for SCANNING and FREEZING of SPECS. This could prove to be very useful for performing on-line feed-forward control.

The modifications to the database that the RCP module require will inevitably incur some additional overhead during upgrades. However the additional storage elements are designed in such a way that this should be minimized.

Achieving Computer Integrated Manufacturing (CIM) for IC fabrication is seen as a necessary development of current manufacturing technology [10]. Maintaining a complete process flow description is a core capability of such a CIM system. To achieve this, the equipment control parameters, or process recipe, must be stored within the systems database. Therefore the recipe manager described here is a significant step toward the implementation of CIM for IC production.

6. Conclusion

This paper has shown how process simulation can be integrated with a CAM system to perform process analysis, diagnosis and feed-forward control. This has been implemented by adding a new module, called SIM, to the COMETS CAM system. The implementation has been performed without any modification to either the COMETS code or the database by making extensive use of *user exits* and the general tables system. Control of information flow within the SIM module is achieved by using menus and by strictly controlling the way simulation data is entered and how the results of the simulations are stored. This implementation of the SIM module maintains both the structure and the adaptability of COMETS.

The SIM module provides powerful tools for process development and maintenance, using information held in the database. Available functions include:

1. Automatic generation of lot simulation histories.
2. Simulation of the fabrication of any product.
3. An on-line facility for performing look-ahead and what-if simulations for a lot.
4. Interactive simulation.
5. Both graphical and numeric presentation of the results of the simulations.

The simulator used in the SIM module is SUPREM-II. Although this is only a one-dimensional simulator, and therefore unable to simulate lateral diffusions, it is widely available and relatively light on computer resources. With more powerful computers it will be possible to replace it with a two-dimensional process simulator. This will require only minor modifications to the SIM module.

Another module is under development which will place the processing data required by the SIM module within the COMETS database. This approach to recipe management is anticipated to have a significant impact on the flexibility and efficiency of manufacturing,

particularly for ASIC production. The inclusion of recipe data within the database also opens the way for the move from CAM to CIM.

Acknowledgements

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Integrating Computer Aided Manufacturing and Process Simulation for Controlling the Production of ASICs

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SUMMARY The process simulator SUPREM-II has been integrated with a commercial CAM system to allow the interactive analysis and diagnosis of processing within a manufacturing environment. Data used for controlling the simulations is stored within the CAM system and the new functions are accessed through the CAM system user interface. It is shown how the new system may be used to perform feed-forward control for corrective processing. The particular relevance of this work to ASIC production is discussed. Currently the system is being used to help control processing in a low-volume ASIC manufacturing facility.

1. INTRODUCTION

Computer Aided Manufacturing (CAM) has become increasingly important to the semiconductor industry. However the available systems are primarily aimed at high volume commodity manufacturers, such as those producing memory chips. In this paper we demonstrate how process simulation can be integrated with a commercial CAM system to provide a process analysis and control system for manufacturers of Application Specific Integrated Circuits (ASICs).

The high capital costs which are associated with integrated circuit (IC) production demand that the most efficient use be made of all resources, particularly equipment and time. This however has proven to be very difficult in wafer fabrication, largely because of the complexity and number of the process steps required. In ASIC manufacturing these problems are exacerbated by the use of small lots (batches) which require fast cycle times, and in lower volume environments there is a potential for many different processes being run at one time. Thus tracking and scheduling the movement of lots being processed can become a nightmare.

It is in this context that CAM systems have been developed to track the movement of lots and store the process and engineering data associated with them. Although they perform this function well they are still unable to offer the kind of process analysis and control required for efficient ASIC production where delivery schedules are critical, and where some products may only be fabricated occasionally. For example, one lot may satisfy a customers annual requirements. Thus for ASIC production the manufacturing process must be very tightly controlled to ensure the optimum use of resources.

To this end the CAM system COMETS and the process simulator SUPREM-II have been integrated to allow on-line access to powerful *look-ahead* and *what-if* functions for both process development and maintenance. Thus lots which have been identified as being misprocessed and are likely to have unacceptably low yields can potentially have corrective processing applied using feed-forward control through the CAM system.

This paper first considers ASIC processing and some of its major characteristics. It then examines commercial CAM systems and process simulators. Following this it is demonstrated how process simulation can be implemented as a component of the COMETS CAM system. Finally we consider the application of this system to a low volume ASIC manufacturing facility where it is currently being used to aid the control of both nMOS and CMOS processes.

2. ASIC FABRICATION

Wafer fabrication is performed using process-oriented batch manufacturing and is therefore far more difficult to control than, for example, assembly line production. During the manufacturing sequence the wafers in a lot can be expected to undergo two or three hundred individual process steps. Each of these steps must be performed in the correct order with the correct control parameters. This in turn requires that the process be monitored (Perloff et al, 1980). Figure 1 shows the flow of data and wafers associated with a process step. Recipe data is used to define the operation to be performed and engineering data is collected for process analysis and control. Product wafers may have measurements made upon them and are ultimately used to provide parametric and yield data. Test wafers are often introduced into the process, for one or more steps, to provide more engineering data.

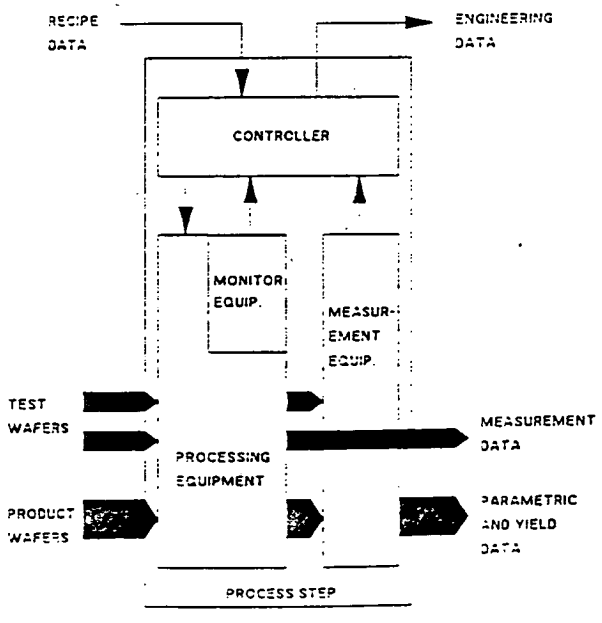

Figure 1. Data flow in a wafer fabrication process step.

With circuit designers demanding greater packing densities and improved device performance the processes have to accommodate ever larger scales of integration with the more advanced facilities producing devices with submicron geometries. This has resulted in process-steps which are close to the physical limits of technology, such as linewidths that approach the wavelength of light, and are therefore very sensitive to equipment control parameters, machine degradation and climatic influences. Allied with this is the difficulty in verifying many processing operations where there is no appropriate in-line measurement that can be easily made in a manufacturing environment. Consequently it is often not known until the parametric tests are made at the end of the process whether the product will meet its specification.

In a high volume single-product environment it is possible to tune a process over time until the devices being fabricated have the desired electrical characteristics and the process yield is optimised. However ASIC production can rarely be treated in this manner.

ASIC manufacturing is normally performed in lower volumes than for commodity ICs, with smaller lots and with faster cycle times often being required. In the case of gate arrays lots are partially processed, and then may be broken up or combined for the committal stage of their manufacture. All these factors complicate both the tracking of product and scheduling of production. Within some ASIC environments more than one process may be supported, for instance to produce products with different geometries or using different technologies. It is also possible to have a mixture of products in a lot and more than one product on a wafer.

Finally, a customers requirement for a particular product may be quite low necessitating a particular design to only be fabricated occasionally. In this case it is particularly important that there is no misprocessing as this may put back delivery time of the product by several weeks. Therefore both product and process must work *right first time*.

3. COMPUTER AIDED MANUFACTURING

CAM systems are now widely used in all phases of semiconductor manufacturing. They have supplanted manual methods of production control because they respond more quickly and accurately to engineering changes, management needs and equipment availability.

The COMETS CAM system has a large user base in the semiconductor industry (Burggraaf, 1987). Like other systems of its kind it consists of a database and a number of functional modules. Figure 2 shows the layout of some of the COMETS modules. These are: the work-in-progress (WIP) module; the engineering data collection (EDC) module; the recipe control (SPEC) module; the non-lot tracking (NTC) module; the scheduling (SIS) module; the intra-factory communications (FCM) module: the process automation (PAM) module; and the statistical quality control (SQC) module. These allow the movement of lots to be tracked, the appropriate recipe to be displayed at each process-step and any engineering parameters to be collected after the operation. They may also be used to perform scheduling and other ancillary functions. Information collected about the processing of a lot is stored in the database as a *lot-history*.

The advantage of using a CAM system to collect processing data is that technical problems can be solved more easily, fewer lots misprocessed, cycle times reduced and thereby yield and throughput increased. Factors that are important in ASIC production and are dependent on the accessibility and integrity of the processing data. Thus the COMETS user interface, which is based on a menu structure, and the robustness of its database are very important features of this CAM system.

Though COMETS is well suited to maintaining information on the state and performance of a manufacturing facility it is a purely reactive system. No tools are associated with COMETS to help process engineers analyse and modify processing of a lot on-line in real-time. Features such as this can be important when processing ASICs.

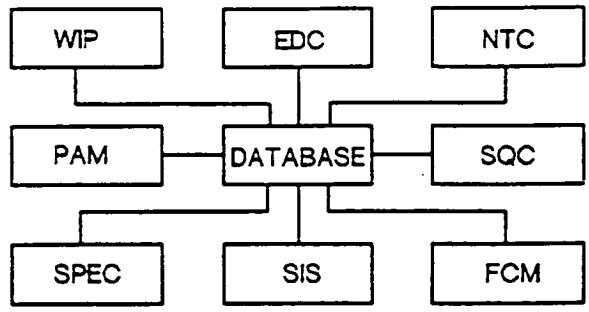

Figure 2. Functional modules and database of the COMETS CAM system.

4. PROCESS SIMULATION

Current methods for modelling wafer fabrication can be regarded as being of two types: statistical and physical. The former is dependent on there being a large body of characterising data available and can only give reliable results within the bounds of that characterisation. The latter consists of models that describe the effect which each process-step will have on a wafer; when integrated into process simulators they form a very powerful tool. While the models are very sophisticated they must be used with a degree of care. To obtain accurate results the model parameters must be tuned to the particular environment which they are to simulate. Alternatively they may be used in a differential mode to examine the kind of effect that variations in process parameters will have on the electrical characteristics of the finished devices.

Process simulators can currently model one- and two-dimensional sections through a wafer. For example, in an nMOS process there are regions that can be simulated to gain an understanding of the whole process. Figure 3 shows a two-dimensional plan where four different one-dimensional sections are indicated. All four of these must be simulated to fully model the fabrication process. 1D simulations provide less information than 2D but they are also much lighter on computing resources. This is an important consideration for real time analysis and control. It is only when analysing very small geometry devices that it is essential to use 2D simulators, so for many applications 1D simulators can be used to identify significant trends.

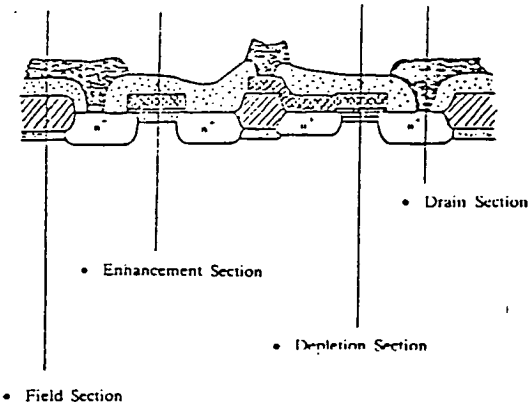

Figure 3. Plan of nMOS inverter structure with 4 1D sections indicated.

SUPREM-II (Antoniadis and Dutton, 1979) is a widely available and well understood 1D process simulator that can model a subset of the manufacturing operations which are performed in wafer fabrication. This capability makes it suitable for estimating electrical characteristics such as threshold voltages and sheet resistivities. Figure 4 shows the SUPREM-II doping profile of the depletion section of figure 3.

Historically process simulators have been used for process development and optimisation. Their user interfaces require inputs that reflect their theoretical models rather than the parameters used to control standard processing equipment. They also tend not to be interactive. However there is obviously the potential to use them for analysis of processing during routine production.

The user interface must also appear as if the simulator is part of the CAM system. Thus the interface of the SIM module is an extension of the menu structure of the CAM system. Figure 7 shows the menu structure and the menus themselves. Note that each menu gives access to a number of functions. The Simulation Main Menu allows access to the Product Simulation Menu and the Lot Simulation Menu as well as an interactive version of SUPREM-II called INTERSUP (Mowat, 1988). The interactive code was adapted for this project.

The Product Simulation Menu allows the fabrication of a whole product to be simulated and the results inspected. The Lot Simulation Menu contains functions which allow *look-ahead* and *what-if* type simulations to be used for investigating various processing scenarios. The functions of this menu are supported

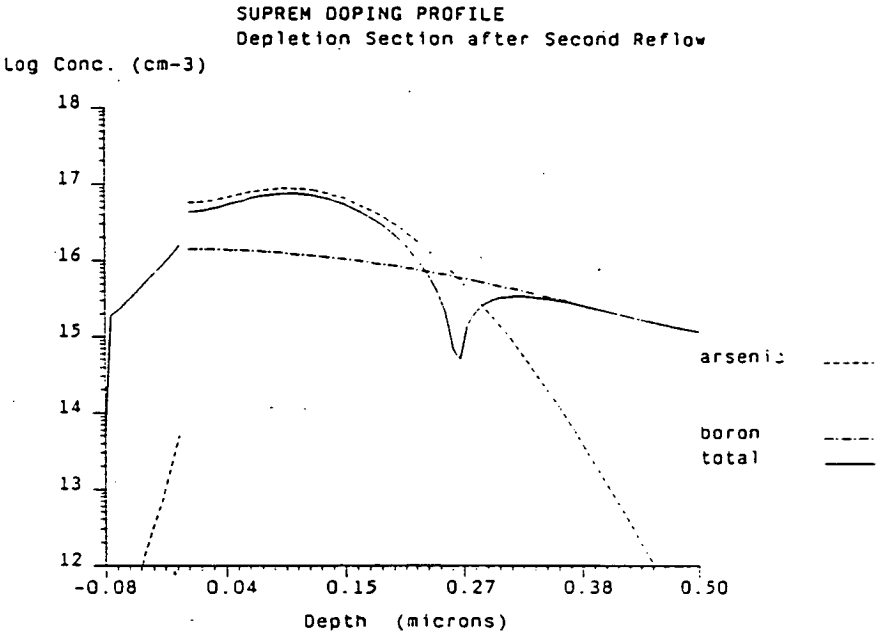

Figure 4. SUPREM-II doping profile of nMOS depletion section.

5. INTEGRATING CAM AND PROCESS SIMULATION

A new process simulation (SIM) module for COMETS which makes the simulator SUPREM-II available as part of the CAM system. For the first time, within a manufacturing environment, real-time analysis of processing is possible and feed-forward control can be performed. This has been implemented in such a way that it unnecessary to modify the COMETS code except where the developers had left exit points to enable customisation. The new module interfaces with some of the existing modules, as shown in figure 5.

To make the process simulator more accessible to the process engineers in the clean-room the CAM system must act as the operating environment for the simulator. Therefore the data for controlling the simulations has to be associated with the process definition in the database. However the database could not be modified otherwise the CAM system would no longer be the standard commercial version and therefore its robustness could be brought into question. Thus the control data for the simulator has been appended to the process recipe files which are part of the process specification and are associated with the database. Figure 6 shows such a recipe file.

by another component of the SIM module which maintains simulation histories of all of the lots processed so that the effect of processing on each lot can be inspected as well as be used as a starting point for further investigation.

6. APPLYING THE SIM MODULE

The SIM module may be used to perform diagnostic analysis and feed-forward control for lots which have been misprocessed. For a high volume manufacturer this is useful when implementing a new process and for generally increasing the understanding of the process. However for an ASIC manufacturer this could mean the difference between product delivered on time within specification, and a lengthy delay while a new lot is fabricated.

To demonstrate how the SIM module can be employed, the EMF 6 micron nMOS process will be used as an example. During this process an oxide is grown to form the transistor gate. Under normal conditions this should be 640 Å thick, but if the lot is left in the furnace too long then a thicker oxide will result. Consequently a device at the end of the process will have a higher threshold voltage, which may lead to the ICs failing to the meet their specifications at parametric test.

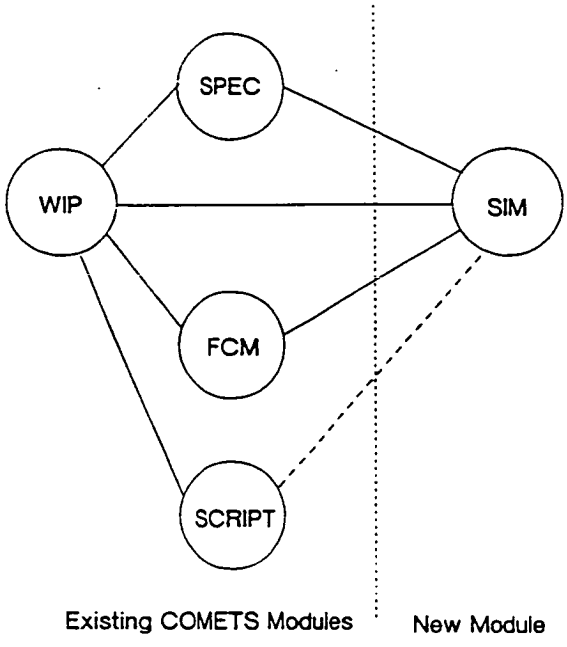

Figure 5. The SIM module interfaces with some existing COMETS modules.

```
GATE OXIDE

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen          20%    (1.5  l/min.)
HCl             15%    (0.15 l/min.)
Hydrogen        10%    (1.7  l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen  +  HCl
17min.Oxygen  +  HCl  +  Hydrogen
5 min.Oxygen

Measure: oxide thickness


** FIELD
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
** DEPLETION
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** ENHANCEMENT
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
** SOURCE-DRAIN
MODEL NAME=DRY1,LRTE=1E5,PRTE=25
MODEL NAME=WET4,PRES=0.74
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
STEP TYPE=OXID,TEMP=950,TIME=17,MODL=WET4
STEP TYPE=OXID,TEMP=950,TIME=5,MODL=DRY1
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Figure 6. A recipe file for gate oxidation which has been extended for use with the SIM module.

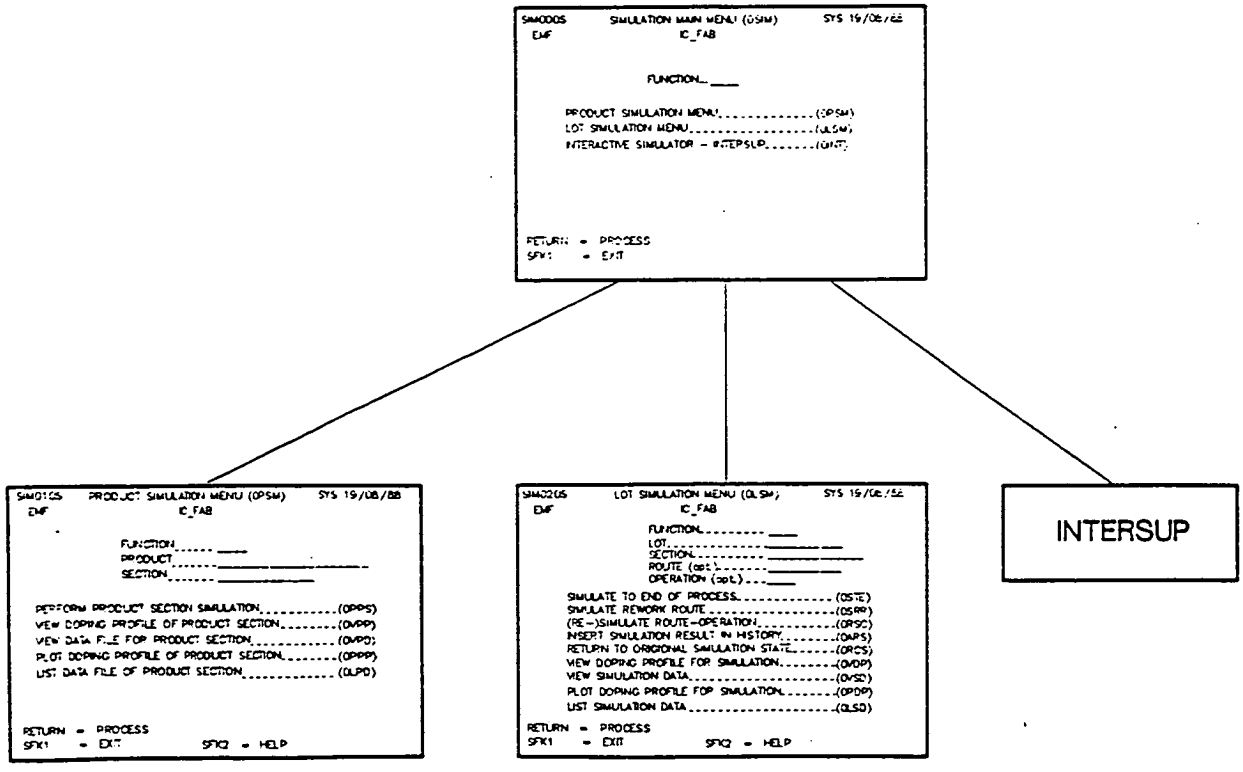

Figure 7. The menu structure of the SIM module interface.

Figure 8 shows a sequence of actions that could be taken when using the SIM module. Once a processing error is identified the first step is to resimulate the process-step (0RSC) until the simulated results match those measured. Then one can look-ahead to the end of the process (0STE) and examine the final electrical characteristics against the specification. Should this suggest, for example, that a threshold voltage outside the desired range will result then changes to the processing parameters can be investigated. These are known as what-if simulations (0RSC, 0SRR and 0RCS): what if the lot is reworked, removing the oxide grown so far and growing it again; or what if a later process-step is modified to adjust the threshold voltage by introducing some additional dopant? After examining the options a suitable change to the process could be made, ie. feed-forward control. If none of these alternatives are feasible then the lot will have to be scraped but at least this is in the light of examining all the engineering options.

Thus the SIM module can be used to analyse processing in real-time for routine production, and for diagnosing corrective processing.

7. CONCLUSIONS

In this paper we have discussed some of the problems faced during ASIC production compared to commodity manufacturing and have shown how a commercial CAM system may be used to monitor IC production. We have also demonstrated that it is possible, not only to use CAM for the reactive control of wafer fabrication, but also for active feed-forward control by using process simulation to verify and predict the effect of operations on individual lots. This has been achieved by the development of a new module for a commercial CAM system, giving the process engineer access to the simulator as if it were part of that system. It uses data held within the database of the CAM system to control the simulations and makes available look-ahead and what-if functions. These allow, for the first time, interactive analysis and diagnosis of processing within a manufacturing environment. The application of this module to controlling a typical process has been presented and it emerges as a potentially important tool for ASIC manufacture.

8. ACKNOWLEDGEMENTS

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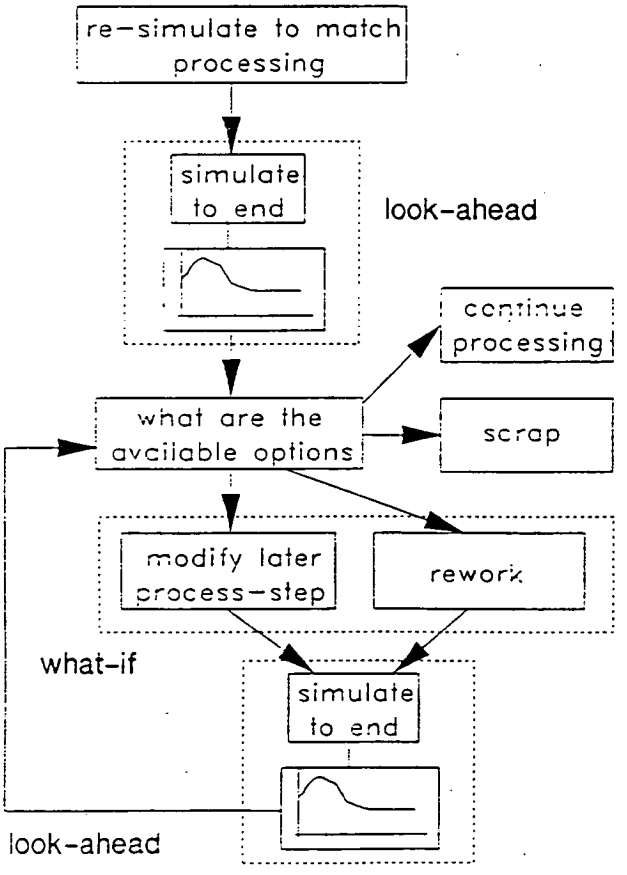

Figure 8. Flow diagram showing typical sequence of actions performed when using the SIM module.

Integrating CAM and Process Simulation to Enhance On-Line Analysis and Control of IC Fabrication

A.J. MacDonald, A.J. Walton, J.M. Robertson and R.J. Holwill

1. Introduction

The current generation of semiconductor computer aided manufacturing (CAM) systems were primarily developed to operate in largely stable production environments. In their present form they are capable of tracking lot movement and collecting engineering data, which allows processing to be analysed using, for example, statistical methods [1, 2]. However, these CAM systems do not contain any knowledge about the interaction of process steps.

In this paper we present a method by which process simulation may be integrated with a commercial CAM system to provide a set of powerful tools for process analysis and maintenance. Thus an engineer is able to interactively explore the process so as to verify past processing and estimate the effect of future operations. This results in a better understanding of the process within the manufacturing environment, and provides a capability for analysing the fabrication sequence in real-time. It can also be employed as a decision support system for feed-forward control.

2. Computer Aided Manufacturing

Computer aided manufacturing (CAM) systems are widely used to improve the efficiency of manufacturing processes. They achieve this by providing structured storage of manufacturing related information and allowing access to this through a common interface. They also allow management and engineers to respond more quickly and accurately to changes in processing requirements and equipment availability than was possible with manual methods.

Currently there are many semiconductor CAM system in use around the world, some having been developed in-house and others by dedicated software companies. However,

the expense involved in developing state-of-the-art CAM systems has made in-house development impractical and forced a consolidation of the market around a few commercial systems [3]. Of these systems the most prevalent are COMETS† and PROMIS‡.

Such systems offer many advantages to wafer fabrication [4], most notable of these are:

- Fewer misprocessed lots.
- Lower work-in-progress.
- Shorter cycle times.
- Increased equipment utilization.
- Increased yield.

All of these points have a strong bearing on the economic viability of a wafer fabrication facility. The emphasis on current CAM systems is on work-in-progress (WIP) tracking, with additional software for data collection and production analysis. Control is restricted to sequencing process steps and reacting to violations of parameter control limits. These systems are therefore not in themselves capable of on-line diagnostic analysis and opportunistic control of IC processing. Although they may be suitable for commodity production they are unable to offer the kind of process analysis and control required for the efficient flexible production.

There is little agreement amongst different manufacturing industries on the definition of a CAM system. However, the demands made on manufacturing control systems by IC processing have led to the general adoption of the format shown in figure 1. In this model the database allows all information to be treated as a common resource by the functional components of the system. This allows it to track the movement of lots, display the appropriate recipe at each process step and collect engineering data. Scheduling of processing and equipment utilization, tracking and other production functions can also be performed using this information.

3. Process Simulation

Process simulation is a method of modeling the physical effects of wafer fabrication.

† COMETS, recently renamed as WORKSTREAM, is a product of Consilium Inc., Mountain View, CA, USA.
‡ PROMIS is a product of Promis Systems Corp., Toronto, Canada.

The application of one- and two-dimensional process simulators to the development and optimisation of processes has been well documented [5, 6, 7]. However, although statistical modeling techniques have been applied to manufacturing [8, 9], there have been no real attempts to do the same with process simulation. This is despite the advantage of being able to relate many of the simulation input parameters to the parameters required for equipment control.

In this paper we show how SUPREM-3† [10, 11] can be used for diagnostic analysis during routine production. SUPREM is a 1D simulator which is capable of predicting the physical characteristics of semiconductor device structures during fabrication. Although short channel devices require the use of 2D simulation, it is still possible to obtain a good understanding of process fundamentals by using a 1D simulator. If the simulator has been well calibrated [12] then it is possible to use it to get meaningful absolute values for physical and electrical device parameters. In a differential mode the simulator can be used to investigate how perturbations of process variables from the mean will influence the concentration profiles and electrical characteristics of the devices being fabricated.

The use of SUPREM within a manufacturing environment is complicated by both its user interface and by its batch type operation. However, it is fast enough to be used in real-time which makes it very suitable for application in a manufacturing environment. No conceptual difficulties exist in replacing this 1D simulator with a 2D simulator such as SUPRA†, although the additional CPU time required to perform 2D simulations using currently available computers prevents them from being used in an interactive fashion. It is expected that in the future, low-cost high-speed computers and the implementation of algorithms for parallel architectures will help to make 2D interactive process simulation generally available [13].

In order to characterize a process with a 1D simulator it is necessary to model a number of sections through typical device structures. Figure 2 shows the sections required for an nMOS process. To fully simulate fabrication using this technology all applicable sections must be simulated for each process step. For example a thermal oxidation will not only oxidize the required areas but will also change the distribution of dopants throughout the wafer.

The output generated by SUPREM provides information on a number of features of the device structure being simulated. This includes charge densities, layer thicknesses,

† SUPREM-3 and SUPRA are products of TMA Inc., Palo Alto, CA, USA.

junction depths, sheet resistances and dopant distributions. An example of some of the output which is available is illustrated in figure 3. For process verification such information can be very valuable. This is because simple on-line measurements, either *in-situ* or after a process step, do not normally provide information on dopant distribution through the substrate. Measurements which can provide this sort of information are typically performed off-line as they are either destructive or require extra masking layers. Wafers that are used for these measurements are therefore unable to yield product.

4. Integrating Process Simulation and CAM

When developing the enhanced system to integrate CAM and process simulation three goals were set for its functionality. These were:

1. To make process simulation available for diagnostic analysis of processing in a manufacturing environment.
2. To help provide the process engineer in the manufacturing environment with a greater understanding of the relationships that exist between process steps.
3. To allow feed-forward control in real-time.

To achieve this level of functionality a software module, called SIM, was developed to integrate CAM and process simulation. It was designed to consist of three components:

1. Simulation logging of the processing for each lot. As each lot is processed the changes to its physical structure are simulated and the results become part of the lot's processing history.
2. Product simulation which allows the processing of individual products to be simulated and the results inspected.
3. Lot simulation which allows *look-ahead* and *what-if* simulations of individual lots to be performed and the results inspected. It also allows the simulation histories of lots to be investigated.

A commercial CAM system is used as a basis for the system so as to ensure that the new software could be evaluated in the context of the constraints imposed by such a system. COMETS was chosen for this project so its architecture obviously influences the implementation. However, it is important to note that the ideas developed in this paper

are applicable to all semiconductor CAM systems.

COMETS consists of a database, a main program which includes basic WIP tracking capabilities, and a set of modules with functionality similar to that described in the generic CAM model of figure 1. The functionality offered by the main program and additional modules is accessed through a comprehensive and consistent hierarchical menu structure. This has the advantage that a user can quickly become familiar with a new module without having to learn a new interface. The database itself is also a hierarchical structure.

The COMETS WIP module is used to track and report on production. Within this module the information that is associated with a process step is represented as an OPERATION. Related operations, as might occur in photolithography, are then grouped together to form a ROUTE. The combination of ROUTE and OPERATION uniquely define a process step. The processing instructions for a process step are stored in a SPEC file which is associated with the appropriate ROUTE-OPERATION. A PRODUCT is then defined by grouping together the appropriate ROUTES. As a LOT is processed a description of this processing is collated as a LOT HISTORY. The production information is stored within the CAM systems database and so is accessible to all the functional programs. Figure 4 shows the relationships that exist between the data objects used by COMETS to describe the fabrication process. Although the terminology used here is particular to COMETS the concepts are generic.

Though this system is well suited to maintaining information on the state and performance of a manufacturing facility it provides no tools to help process engineers analyse and modify processing of a lot on-line. It has, however, been designed to be adapted to the needs of individual environments. For example, software for statistical analysis can be added to the Statistical Quality Control (SQC) module. Other customising software may be linked into the system through the *user-exits* which have been provided. These are 'dummy' subroutine calls that are guaranteed to remain unmodified during system upgrades. Run-time customisation can be performed by editing tables within the General Tables System (GTS).

For the process simulator to become an effective part of the CAM system both the control of the simulations and the presentation of the results should be part of the existing user interface. It therefore follows that the data for controlling the simulator must be held within the CAM system. For this to be the case COMETS obviously has to be extended while still maintaining the integrity of its database. As a result the SIM module was writ-

ten to conform to all the conventions used within the system. This takes advantage of the user-exits and GTS to ensure that none of the code within the SIM module would need to be modified during system upgrades. Figure 5 shows how the SIM module integrates into COMETS.

To automatically simulate each process step, the data to run the simulator had to be stored without modifying the structure of the database. After investigating various options a combination of *user defined fields*, within the PRODUCT definition, and SPEC files, of the Specification (SPC) module, were chosen to store the simulation control data. The former stores the product related data such as the orientation of silicon and the substrate doping. The latter store the process data such as equipment set-up instructions and control parameters. This representation does not restrict the structure or format of the control statements and yet enforces a structure on the way this data is maintained. With this comes the added flexibility that very little code is specific to a particular simulator. An example of a SPEC file for a gate oxidation is shown in figure 6. Note that the SUPREM control statements required to simulate the four 1D sections of figure 3 for this process step have been added to the end of the file. This was necessary as there is no simple way in which the unstructured process recipe information can be interpreted by the simulation software. A new method for explicitly representing process specification data is currently being developed.

During the operation of the SIM module the feedback to the operator is confined to messages written to the bottom of the screen announcing the completion of each simulation. In the event of an error occurring during the simulation, mail messages are sent to those in charge of the process via the Factory Communications (FCM) module. The product and lot simulation components of the system are controlled through COMETS like menus which are accessed through the existing menu structure. Figure 7 shows the menu hierarchy and individual screens for this module.

Each function of the SIM module is represented by a four character mnemonic, the first of which is always a zero. This is so that these mnemonics do not clash with any that may later be introduced in later versions. The functions made available by the SIM module menus are discussed below.

Simulation main menu (0SIM)

This menu shows the available functional menus within the SIM module. Although useful to the novice user, more experienced users would normally directly invoke the

specific function they wished to use.

Product simulation menu (0PSM)

The functions under the product simulation menu allow the fabrication of a lot to be simulated and the results of the simulation inspected both on screen and as hardcopy. The availability of this facility is particularly important in environments where processes are variable. For this menu a valid PRODUCT and SECTION must be specified. A valid SECTION is defined as a 1D simulation section name as held in a GTS table. The valid names relate to the simulation control data held within the SPEC files. For example the section 'FIELD' in figure 6.

The simulation of the fabrication of a SECTION is performed using the 0PPS function. The results of the simulation can be inspected either: on screen using 0VPP and 0VPD; or as hardcopy using 0PPP and 0LPD.

Lot simulation menu (0LSM)

The functions of the lot simulation menu allow verification of past processing as well as examination of the effect of future processing. For this menu a valid LOT identifier and SECTION name must be specified. The ROUTE and OPERATION are optional. If they are not specified then the current ROUTE-OPERATION is taken as the default.

Simulating to the end of the process using the 0STE function provides a powerful *look-ahead* capability. This allows investigation of how further processing will affect the physical and electrical characteristics of product devices. A variety of future scenarios, *what-if* simulations, can also be explored by using some of the other functions.

The effect of one process step can be examined by using 0RSC, while a rework route can be simulated by using 0SRR. When simulating to the end of a process after a rework the current process step is included in the simulation. After each set of simulations the current state of simulation can be reset to that of the last 'real' process step by using the 0RCS function.

The 0RSC function can also be used to re-simulate a process step where a lot has been misprocessed. The results of this simulation can then be substituted into its lot history by using 0ARS.

Inspection of the simulated results under this menu are performed in a similar way to the product simulation menu, using 0VDP, 0VSD, 0PDP, 0LSD. These functions also allow simulation lot histories to be examined.

Direct access to simulator (0DAS)

Calling 0DAS gives direct access to SUPREM-3. This allows the simulator to be used without any of the restrictions implicit in the menu structures described previously. However, using SUPREM efficiently in this way requires the user to be very familiar with the simulator and its interface.

All the data files used by the functions of the product and lot simulation menus are stored in the users current directory. This protects the files in the simulation history directory from being modified unintentionally. The only way in which data files can be inserted into the simulation history directory is by using the associate simulation history function, for example after the re-simulation of a process step.

The hardware used for this implementation is based around a local area VAX cluster where COMETS runs on a VAX 8350 and the simulation software on a MICROVAX 3500. Disk space is shared throughout the cluster so that splitting the system over more than one computer does not hinder data transfer. This implementation also has the advantage that the I/O intensive CAM software does not interfere with the CPU intensive simulation software. This is important since the response times of a CAM system can become very slow when a large number of transactions are being processed.

5. Application of the SIM module

On-line process control

In order to demonstrate how the SIM module can be used in a manufacturing environment the processing of a lot on the Edinburgh Microfabrication Facility (EMF) 1.5 micron nMOS process will be considered. Within COMETS the process is broken down into ROUTES and OPERATIONS. These have been designed so as to be intuitively obvious; for example, a spin on resist step is an OPERATION and a set of lithography steps form a ROUTE. This allows both precise production control and detailed data collection. One of the results of this is that a large amount of engineering data can be collected during manufacture, which is desirable for process analysis although not always practical for high volume production.

When a LOT is scheduled for production it is created within COMETS for the appropriate PRODUCT. During its process sequence the lot reaches OPERATION 'GATEOX 1' on ROUTE 'GTEOX N1.5' (figure 8). The process recipe for this step is shown in figure 6. Note that although all the regions of the wafers are exposed to an oxi-

dizing ambient during this operation, it is only necessary to simulate the heat component for the FIELD section. This is because the increase in thickness of the field oxide during the gate oxidation step has no significant effect on the performance, or structure of the device.

If the oxide thickness that is grown exceeds the preset limits for this parameter then the lot will be put on hold. The engineer responsible for this part of the process can then use the functions of the SIM module to explore the available options.

Figure 9 shows the sequence of steps which could be performed using the SIM module to analyse the problem. The first action is to re-simulate the current process step so as to simulate the processing which actually occurred. The re-simulated results for this process step can then be associated with the history of the lot.

The reason for the extra growth of oxide in the gate region can be investigated by re-simulating the enhancement channel section. Performing this simulation suggests a probable cause of the additional oxide is that the wafers have spent a minute longer than specified in the wet oxidizing ambient of the gate oxide step (figure 6). This extra time will not only affect the gate oxide thickness but also oxides in other regions and the distribution of dopants throughout the wafer. The modified doping profile and increased oxide thickness will change the threshold voltages of the devices on the product wafers, the extent of which can be checked using the look-ahead function. If the threshold voltages are still within specification then processing could continue as normal. However, if they are out of specification then the processing for the lot might require to be modified, ie. feed-forward control. A series of what-if and look-ahead simulations could be performed to investigate the effect of specific process modifications and estimate how these will influence the final physical and electrical device characteristics. Should corrective processing not be possible then it would be necessary to scrap the lot and re-schedule another start.

Assuming that the threshold voltage of the enhancement devices is out of specification then there are a number of possible options for corrective processing. The SIM module look-ahead and what-if functions can be used to explore the controllable parameters which affect threshold voltage: gate oxide thickness and channel doping [14]. The results of these simulations are shown in table 1. Each of the trial process modifications must also be applied to the other 1D nMOS sections to ensure that all physical and electrical parameters remain within specification. The target values of table 1 show the simulated results of an enhancement channel section for normal production, following this are

the re-simulated values for the misprocessed lot. The extra minute in the wet gate oxide ambient has resulted in an increase in the gate oxide thickness (T_{ox}) of 44 Å and an increase in the enhancement threshold voltage (V_{Tenh}) of 35%. This could potentially be corrected by reworking the lot, stripping off the oxide and regrowing. However, this will also affect the field oxide thickness, which may be undesirable for some processes. An alternative is to modify the channel doping by reducing the threshold voltage adjust implant. Two boron implants are available at this point (figure 8). The first is a low energy implant which is used to adjust the surface dopant concentration. The second is higher energy and is used to increase punch through voltage. Both affect the threshold voltage. By reducing the dose of the low energy implant from 7.0×10^{11} to 5.0×10^{11} atoms cm^{-2} V_{Tenh} can be readjusted to around the target value.

The process modifications that will correct for the changes in the enhancement transistors characteristics will have a different effect on the depletion devices. Table 2 shows how the depletion threshold voltage (V_{Tdep}) changes with the various processing options described above. After the gate oxidation step the depletion gate region will have the same oxide thickness as the enhancement gate region, but this will result in an increases in the magnitude of V_{Tdep} by 15%. The modified V_T adjust implant increases its magnitude by a further 5%. If increasing V_{Tdep} does not violate the process specification then this may be a good solution. However, if V_{Tdep} is out of specification then the depletion implant mask could be reused and another implant introduced to readjust the threshold voltage. Simulating this option suggests a low energy boron implant of 7.1×10^{11} atoms cm^{-2} would readjust V_{Tdep} to around its target value.

The best processing option for this lot will ultimately depend upon the process specification and economic factors, such as the value of the product and the cost of adding an extra masking layer. Using the module to compare physical features as well as electrical characteristics an engineer can also examine the potential implications for reliability of any modified processing. Figure 10 compares the profiles of the standard and modified processes for the depletion channel section. The solid line indicates the target profile and the dashed line shows the profile after the corrective depletion region boron implants have been applied. Not only have the threshold voltages been readjusted but the doping profiles correlate well. Hence the devices produced by the modified process can be expected to have similar reliability characteristics to devices processed according to the specification.

The SIM module is a tool that allows engineers to rigorously explore processing

options before deciding on what should be done with a particular lot. This is important since scrapping potentially good product and processing non-functional wafers are both expensive alternatives. In custom or application specific (ASIC) production, where a product may only be fabricated once, the time taken to fabricate product wafers which meet specification is also an important factor.

Process transfer

The SIM module can also be used to help in the transfer of processes from the prototype stage to high volume production. The system effectively documents the process and the interactions between the process steps. This information is far more detailed than the standard specifications. Such an approach puts the knowledge base built up during the development phase into the CAM system. As a result the production engineers have easy access to this detailed information, which should help to speed-up the implementation of new processes.

Expert systems

Though the SIM module is a powerful tool for process analysis, it does not contain any knowledge about how to apply the simulation models to develop process modifications. In contrast, an expert can provide a set of rules for corrective processing, but will probably be unable to give exact values for parameter settings. Thus a combination of simulation models and expert heuristics would provide a framework for an active process control system. The SIM module can therefore be considered as the first step towards the implementation of an expert system for process analysis and diagnosis.

6. Conclusion

This paper has shown how process simulation can be integrated with a CAM system to perform process analysis, diagnosis and feed-forward control. The CAM system COMETS and the process simulator SUPREM-3 have been used as vehicles for this demonstration, but any other CAM system or simulator could easily be used in their place.

We believe this is the first time that physical process simulation has been integrated with software that is widely employed in the manufacturing environment. The system has been implemented by extending COMETS with a new module called SIM. This module allows the CAM system to be used as an operating environment for the process simulator. The data for controlling the simulator is stored within the CAM system itself. Functional capabilities of the new system include: generation of simulation histories for lots processed;

simulation of the fabrication of individual products; and powerful *look-ahead* and *what-if* functions. The module can also be used to investigate whether changes to the process are likely to alter the anticipated reliability of the product devices. The proposed approach is particularly applicable to flexible manufacture and to speeding-up the transfer of processes from development to production facilities. A potential also exist for the addition of heuristics to help direct the development of solutions using the capabilities of the SIM module.

Further development of this system is currently concentrating on explicitly representing the fabrication process within the CAM database. The objective of this is to allow the process specification to be used to generate both the equipment control instructions and the input statements for the simulator.

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nMOS Enhancement Channel Section		
Processing	T_{ox} (Å)	V_{Tenh} (V)
Target Values	256	0.6
Normal gate oxidation plus 1 minute	300	0.77
Etch gate oxide and regrow	256	0.62
Reduce first V_T adjust implant dosage from 7.0×10^{11} to 5.0×10^{11} *atoms* cm^{-2}	300	0.59

Table 1. Gate oxides (T_{ox}) and threshold voltages (V_T) of an Enhancement Mode nMOS transistor after various processing options.

nMOS Depletion Channel Section		
Processing	T_{ox} (Å)	V_{Tdep} (V)
Target Values	256	-3.42
Normal gate oxidation plus 1 minute	300	-3.92
Etch gate oxide and regrow	256	-3.59
Reduce first V_T adjust implant dosage from 7.0×10^{11} to 5.0×10^{11} *atoms* cm^{-2}	300	-4.11
With additional mask and boron implant of 7.5×10^{11} *atoms* cm^{-2} at 25KeV	300	-3.39

Table 2. Gate oxides (T_{ox}) and threshold voltages (V_T) of a Depletion Mode nMOS transistor after various processing options.

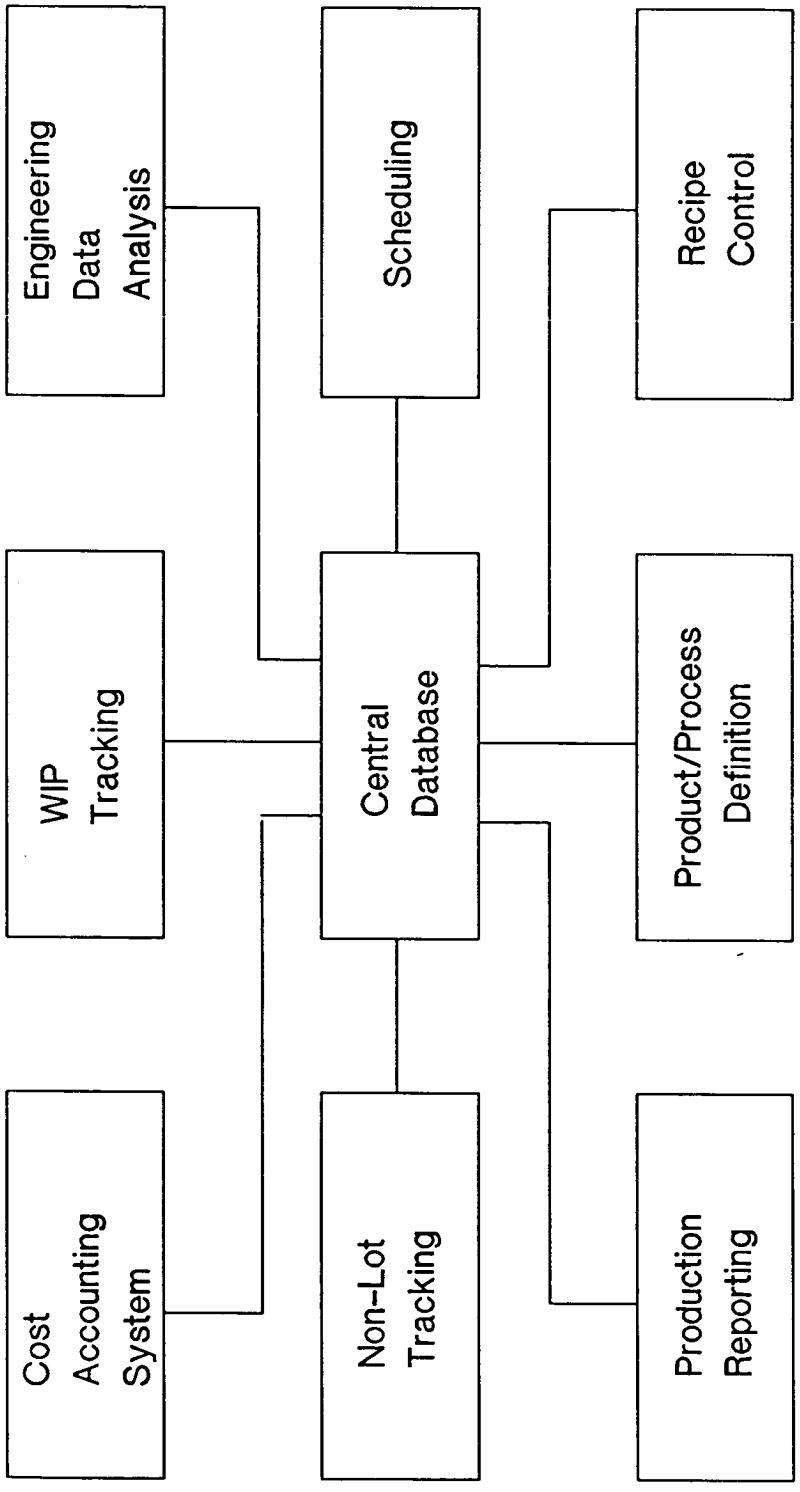

Figure 1. Generic model of a semiconductor CAM system.

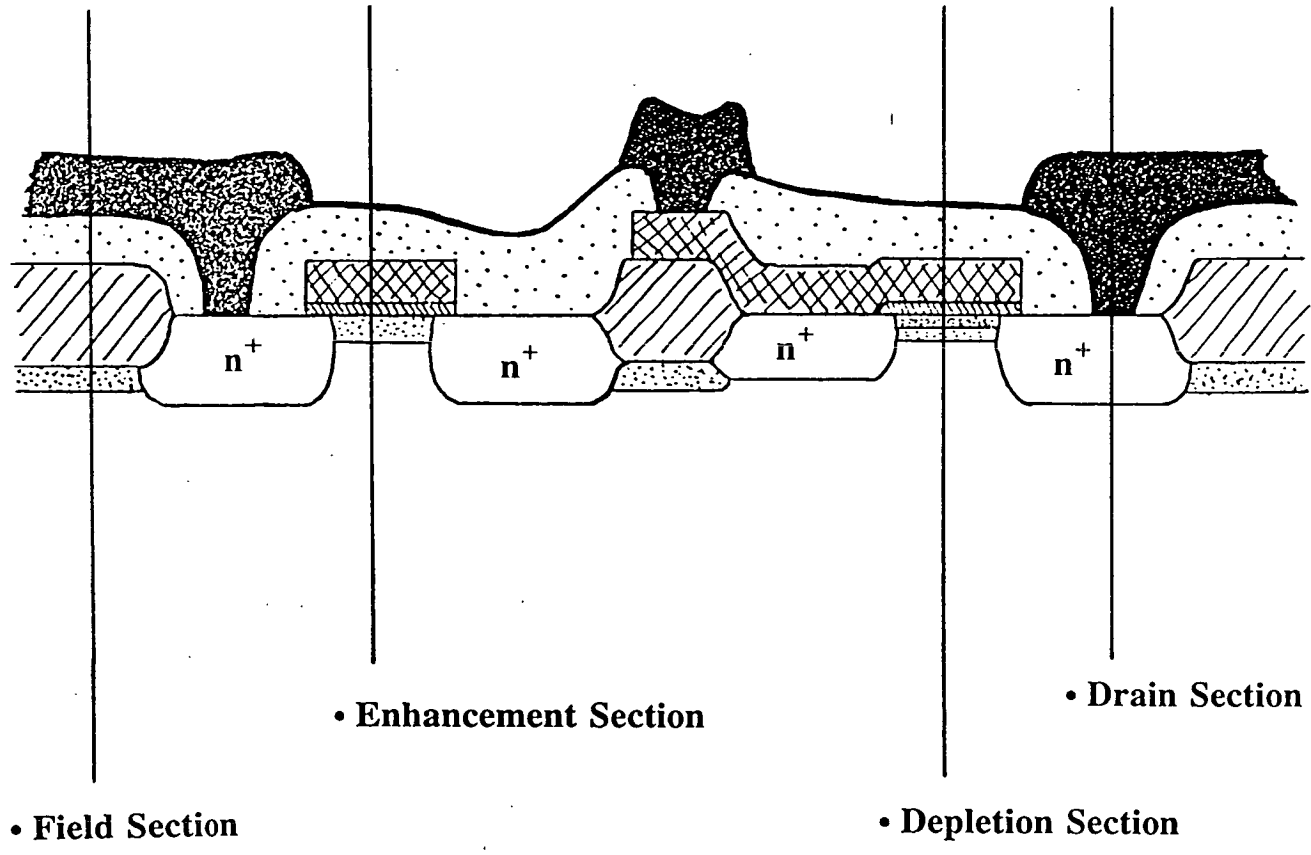

Figure 2. nMOS inverter structure with four 1D sections indicated.

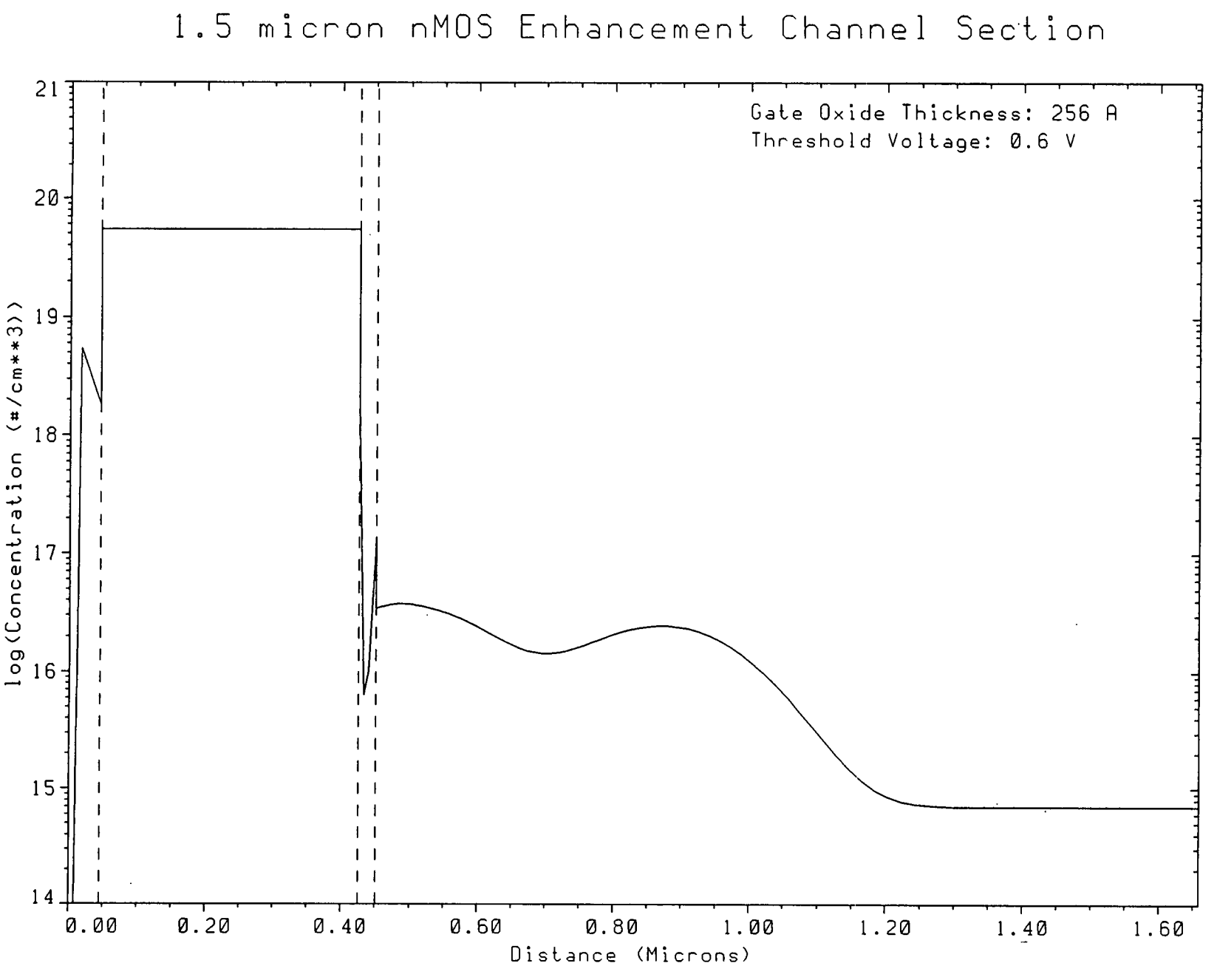

Figure 3. SUPREM doping profile for an enhancement nMOS transistor.

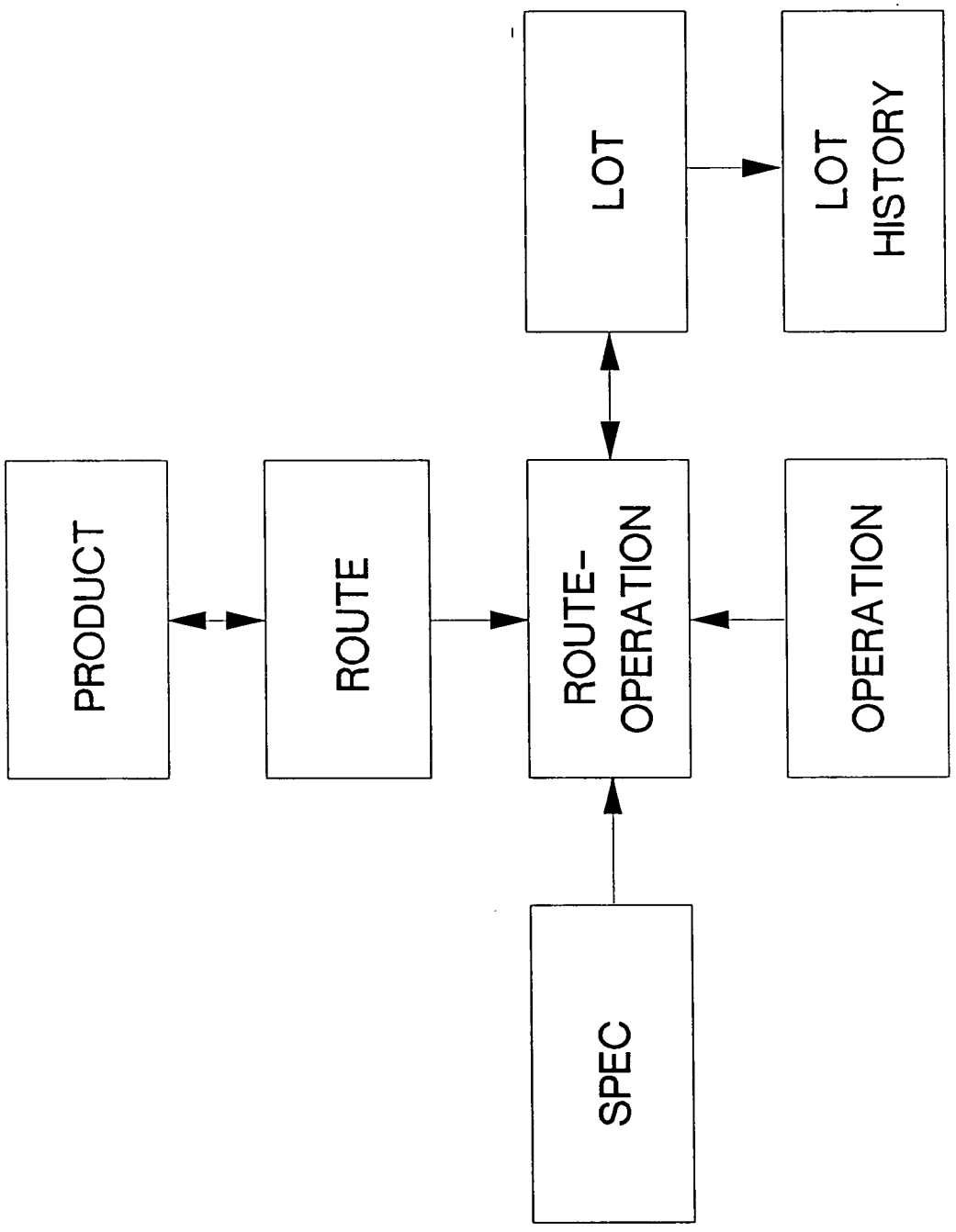

Figure 4. Data model of relationships used by the COMETS to describe processing.

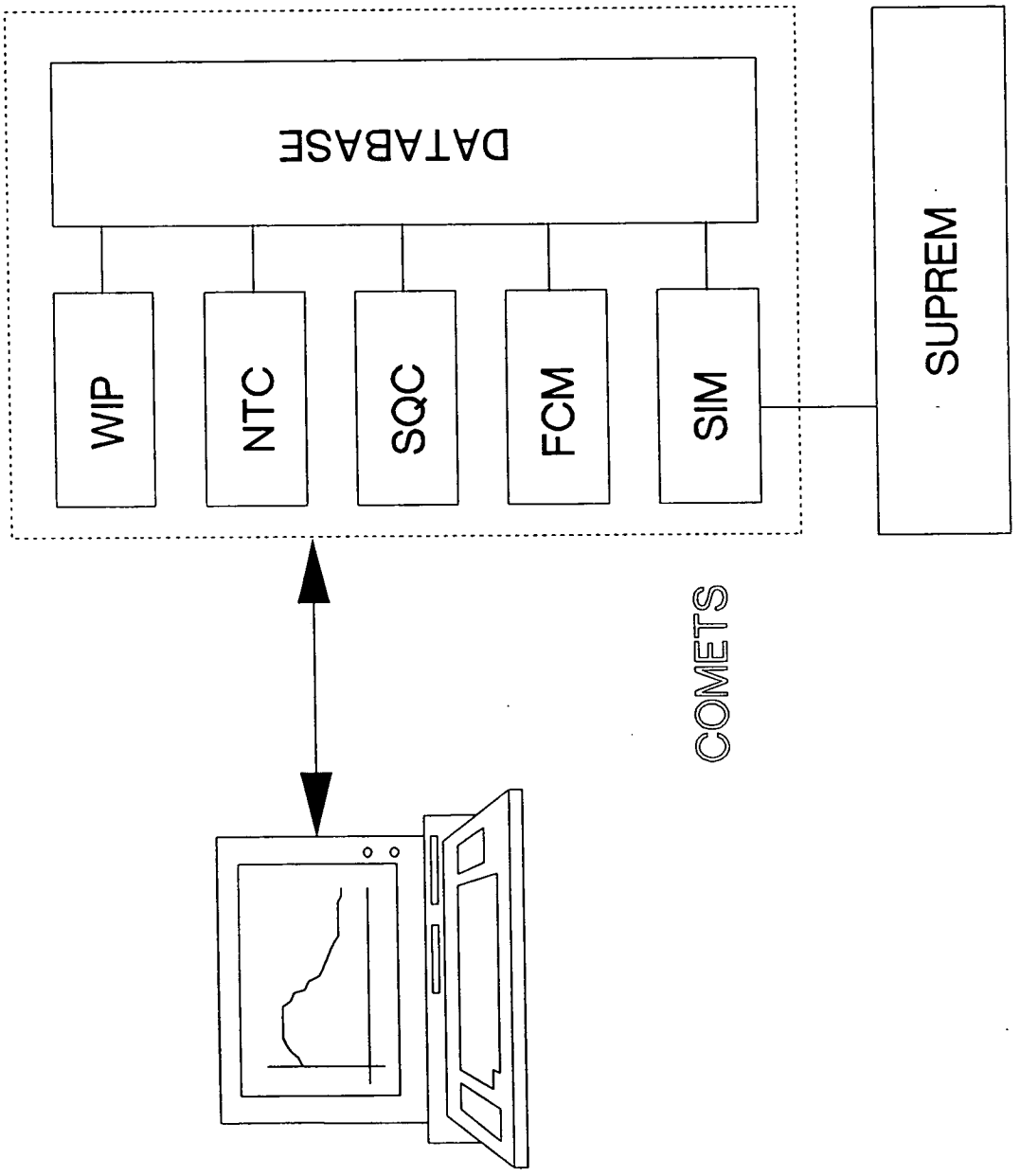

Figure 5. Integration of the SIM module into the COMETS CAM system. The COMETS modules are: WIP - work-in-progress; NTC - non-lot tracking; SQC - statistical quality control; and FCM - factory communications.

GATE OXIDE

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 1.5 l/min.
HCl 0.15 l/min.
Hydrogen 1.7 l/min.
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
3 min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure: oxide thickness

```
** FIELD
diffusion temp=950 time=13 inert
** DEPLETION
diffusion temp=950 time=5   F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3   F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5   F.O2=1.5
** ENHANCEMENT
diffusion temp=950 time=5   F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3   F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5   F.O2=1.5
** SOURCE-DRAIN
diffusion temp=950 time=5   F.O2=1.5 F.HCL=0.15
diffusion temp=950 time=3   F.O2=1.5 F.HCL=0.15 F.H2=1.7
diffusion temp=950 time=5   F.O2=1.5
```

Figure 6. A recipe file for gate oxidation which has been extended for use with the SIM module.

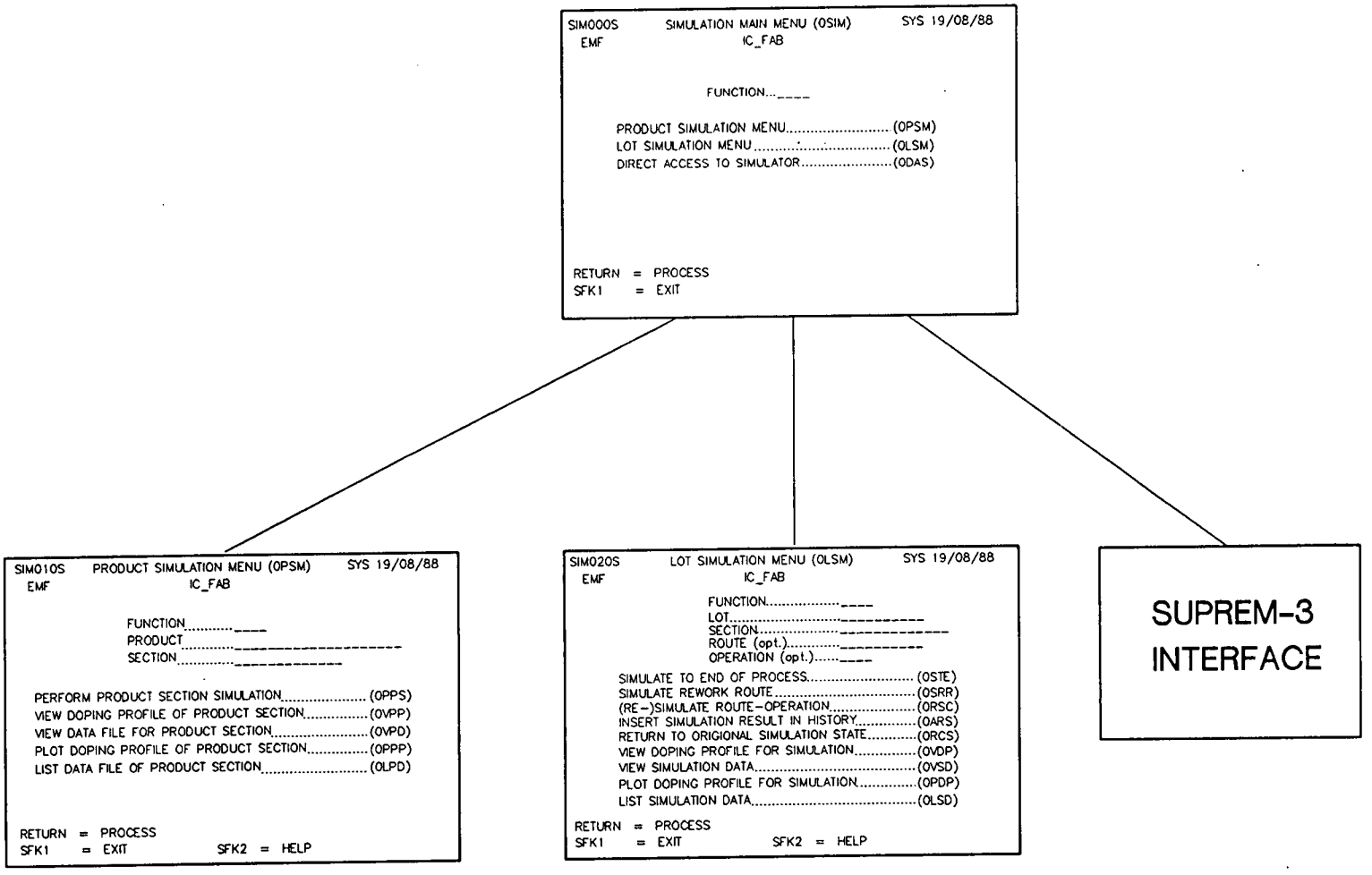

Figure 7. The SIM module menu screens and hierarchy.

Figure 8. Gate oxidation and enhancement threshold implant of EMF 1.5 micron nMOS process as defined within COMETS.

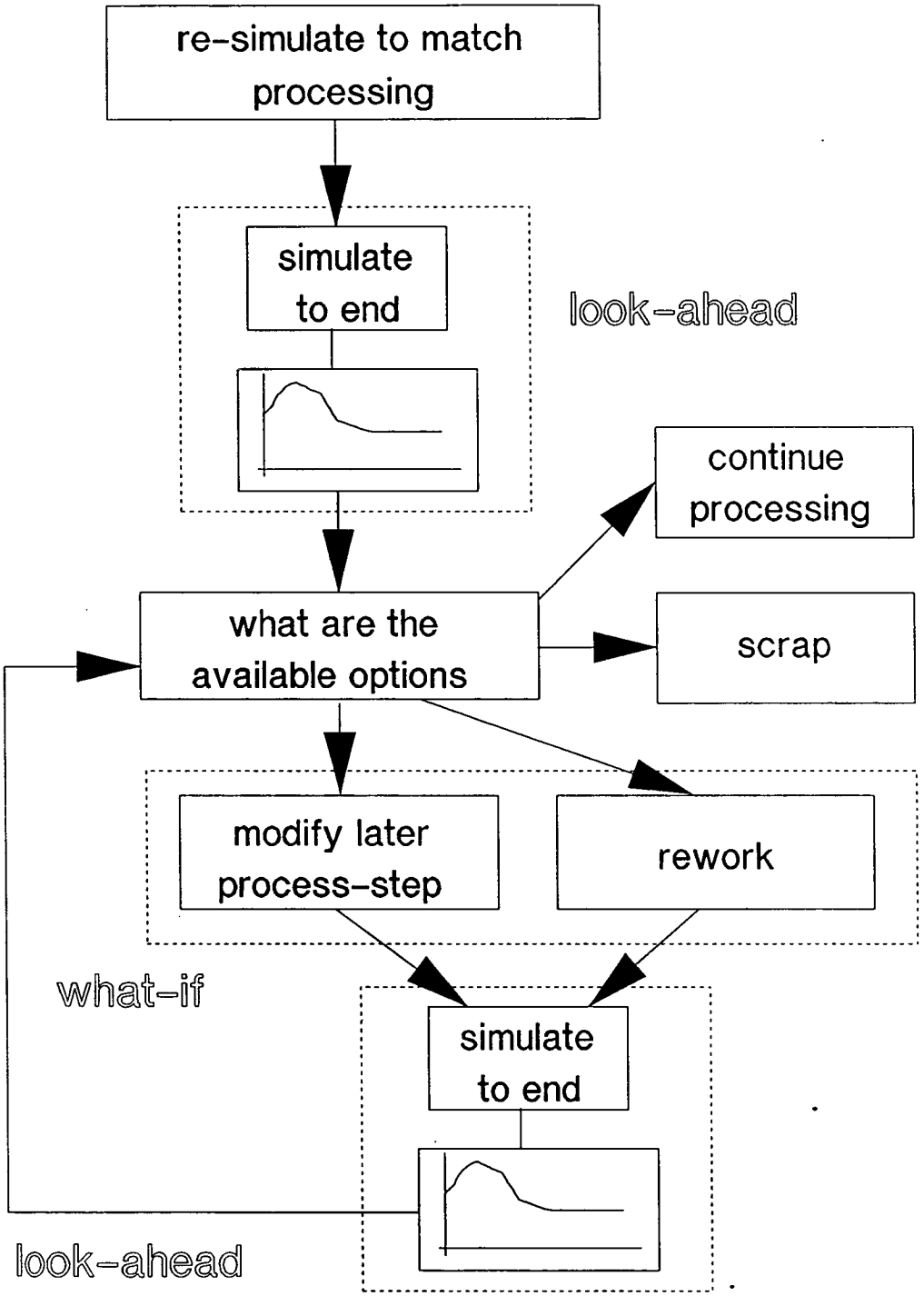

Figure 9. Flow diagram describing application of the SIM module.

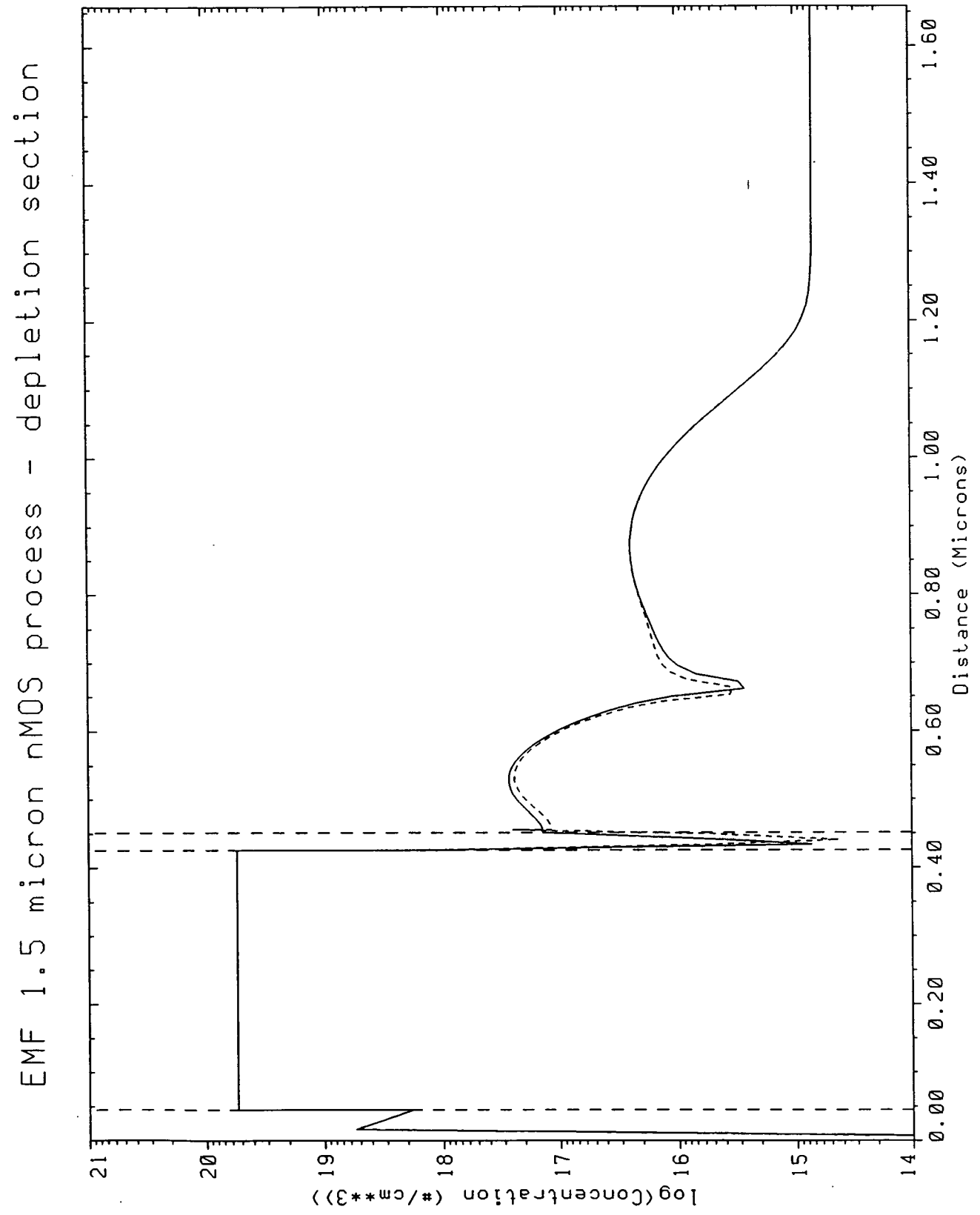

Figure 10. Doping profiles generated by SIM module for an nMOS depletion transistor using standard processing - solid line. The dashed line indicates the profile after the appropriate corrective processing has been performed in order to meet target specifications.