Solid-state imaging: a critique of the CMOS sensor

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Abstract

Over the last decade, there has been considerable research interest in CMOS image sensors. The developed technology continues to occupy a marginal but growing portion of the solid-state imaging market, which is dominated by the CCD sensor. It is often claimed that the CMOS image sensor offers advantages in terms of power consumption, cost, randomly addressable readout and the ability to integrate on-chip signal processing and support circuitry. However, the primary advantage of a CCD sensor: better sensitivity, together with the relative immaturity of CMOS technology, have combined to limit the use of CMOS imagers.

This work investigates the performance limitations of selected CMOS sensor technologies comparing them with an interline CCD imager. The derived performances are used to evaluate whether the claimed benefits mentioned above apply now and will continue to do so over the next decade.

The digital-camera and multimedia markets are widely predicted to expand rapidly within the next few years. In these markets, an essential function of an imaging system is analogue-to-digital conversion (ADC). Consequently, ADC is considered as an example of the on-chip integration of support circuitry. Analysis demonstrates the potential system-power saving of parallel focal-plane signal processing and discusses the most suitable converter architectures.

A test-chip, designed to validate conclusions from the theoretical analysis, is described. Finally, the results from the test-chip are compared to the developed theory.

From this work, conclusions are drawn as to the viability and future development of CMOS imagers; specifically, applications are highlighted where the CMOS imager is most likely to be preferable to the CCD sensor. A number of suggestions for future research are made throughout this work.

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Definitions and Notes

Throughout Chapters 2 and 6 there are graphs which plot the current required to perform a given function. For example, the bias current for an amplifier. These graphs are plots of the estimates of the power consumption derived in the text.

A number of terms used throughout this text are defined below for ease of reference. First a series of definitions, which are used to describe the physical properties of a pixel array.

Column is either the interconnect line that connects the output of pixels together or the series of pixels that share a common output bus. A column is often considered to be a series of adjacent pixels in the y-direction of the pixel array.

Row is a series of pixels orthogonal to a column. These pixels are normally addressed coincidently using common signal lines.

Column amplifier. In a CMOS sensor, at one end of the column of pixels, there is an array of column amplifiers. Typically, there is a single column amplifier *per* pixel column.

n is used for the dimension of an array, throughout this text it is assumed that the array is square, containing $n \times n$ pixels. If the array is not square, n should be assumed to be the number of pixels that share a column.

m is the number of columns of pixels that share a common output stage, *i.e.* the number of column buses that are multiplexed together at the input to the column amplifier.

Fill-factor is the proportion of the pixel cell area that is light sensitive. Traditionally, it is measured as the percentage of the area taken up by the diode.

A second series of definitions are used to describe image defects.

Bright areas in an image can spread and cause two defects:

1. **blooming** is where the charge spreads to adjacent pixels causing a bright spot in the image.

2. **smear** occurs when the bright area spreads along a column of pixels causing a bright vertical line through the image.

fixed-pattern noise (FPN) is systematic variations in the image caused by parallel signal paths. FPN can result from pixel-to-pixel or column-to-column variations. It is calculated as the maximum variation that, on average, will be seen across the pixel array. A tolerable level for viewed images is 0.1% of the signal swing at the pixel.

Image lag is associated with readouts where the signal charge is removed from the pixel cell. It is the proportion of the signal charge that remains after readout and, hence, is added to the next pixel value.

Charge-transfer efficiency is only associated with a CCD element. It is the proportion of the signal charge that is successfully passed from one element to the next.

The last list of definitions are general terms associated with CMOS imaging.

Active pixel a pixel that contains at least one amplifying transistor.

Passive pixel a pixel that does not contain an amplifying transistor.

Correlated-double sampling a signal-processing method where a reset value is subtracted from the signal value to improve the signal-to-noise ratio.

V_{RT} is the pixel reset voltage.

Dynamic range is the ratio of the maximum voltage swing at the pixel output to the system noise floor. It is often expressed in decibels.

Throughout this text pixel arrays are qualitatively classed as small, medium and large; quantitatively this refers to array sizes of up to 128×128, up to 512×512 and larger, respectively.

Chapter 1
Introduction

1.1 Overview

At present, the CCD imager dominates the solid-state imaging market. Over the last decade, an alternative technology, the CMOS imager, has been developed to challenge the CCD-based sensor. The CMOS imager is fabricated using a standard digital CMOS process, which, as discussed in Section 1.2, offers a number of potential advantages over the CCD system. However, the fundamental disadvantage of the CMOS-based sensors, lower sensitivity, has outweighed the advantages.

Recently, the development of CMOS camera-on-a-chip technology has yielded a considerable price advantage over the CCD sensor system. For example, Kempaninen reports a \$20, 640×504 pixel colour imaging chip [44], whereas a similar resolution CCD sensor system costs about \$200. Such advances have led to speculation in the Literature and industry press predicting the supplanting of the CCD camera by the CMOS technology. For example, one of the principal proponents of CMOS technology, Fossum, concluded that

> CCDs are well entrenched in the market place and continue to advance at a rapid rate. ... However, given the relative immaturity of the APS [Active Pixel CMOS Sensor] compared to the CCD, and the level of performance it has already obtained, it is very possible that APS will supplant CCDs in most applications by the turn of the century [45].

Further, in 1997, an article in PC-World concluded that

> The image sensors based on Photobit's high performance CMOS Active Pixel Sensors represent a dramatic breakthrough in this market. For more than 20 years, Sony and Sharp have dominated the image sensor market with their CCD image sensors. Active Pixel Sensors should replace CCDs within the next few years, offering significant advantages over CCDs in cost, performance, and system size [46].

Within the last couple of years, there has been a shift away from using standard CMOS digital processes; a few extra processing steps are added to yield performance benefits. Wilson describes the process developed in the joint venture between Photobit, a leading CMOS camera manufacturer, Kodak and Motorola:

> We start out with the logic process, add some steps to fabricate resistors and capacitors for high-quality analogue circuits and then add some more to improve the sensitivity of the photosensor. The result will share most of the process steps with the logic process, and it will be compatible with our logic libraries and cores. But it will be a PIN diode with much better sensitivity [47].

Kempainen concludes that a hybrid CMOS process may offer performance advantages:

> However, it is premature to claim the dominance of pure CMOS image sensors over mature CCDs. CMOS image quality has yet to match CCD quality, and sensors that use some features of CCD pixels in a CMOS technology are seeing image-quality results. . . . Adding transistors to create active CCD pixels promises CCD sensitivity with CMOS power and cost savings. Image-sensor manufacturers produce these charge-modulated devices by adding only a few steps to a standard CMOS production line[44].

Whether CCD or CMOS technology will dominate the solid-state image market is uncertain. However, it is clear that the market is likely to expand rapidly over the next decade. Ackland concludes that, like the digital clock, consumer electronic cameras will become cheap enough to be integrated in electrical appliances and, hence, will become a ubiquitous feature of everyday life [27]. A topical example of the emergence of new imaging markets is the recently released Nintendo GameBoy camera. The $50 product uses a small CMOS sensor to send images to the GameBoy screen. Even though the camera is delivering poor image quality (150×150 pixel resolution, with 2-bit gray-scale image), the product sold 500,000 units in the first few weeks on the Japanese market.

1.2 Advantages

The development of CMOS imaging technology has been driven by the following advantages over the rival CCD sensors:

- **Standard process.** A CMOS camera is fabricated on an industry standard process, while the CCD imager uses a specialist process.
  - CMOS fabrication accounts for 90% of all semiconductor chips, including microprocessors, ROM and RAM. Consequently, the development cost of the CMOS process does not have to be borne by the imaging technology.
  - CCD image sensors suffer from low yields because over 50% of its area is covered by either thin or inter-poly oxide [48].
- **Power.** Typically, a CCD imaging system consumes 10-100 times more power than a CMOS sensor. The two significant power advantages are:
  1. A CMOS sensor can be designed as a camera-on-a-chip, whereas, a CCD imaging system contains at least two, but more typically four, chips.
  2. A CCD sensor requires multiple supplies and high-voltage clocks.
- **Size.** A single-chip CMOS camera only requires resistors and capacitors as external components.
- **Design resources.** Circuit and system design in CMOS is supported by a vast number of resources, and many cell libraries are available [49].
- **Addressable pixels.** A CCD camera produces a serial output, whereas a CMOS camera can allow X-Y addressing. This yields advantages in applications such as motion detection, tracking, and edge detection.
- **On-chip integration of signal-processing.** An advantage of fabrication on a standard process is that digital and analogue circuitry can be integrated with the image sensor. This has been used to realize, for example, auto-gain control, auto-exposure control, anti-jitter compensation, image compression, motion tracking, and video-signal formatting.

The primary disadvantage of a CMOS sensor is that the photodetectors are not characterized or optimized [49]. Resulting in

> lower sensitivity of the chip [which] meant that you had to have a flash unit to take pictures indoors ... we have to perform about 600 million operations to extract a high-quality image from the noisy output of the sensor[50].

1.3 Camera formats

There are five distinct markets for solid-state image sensors:

1. video.
2. nultimedia.
3. still camera.
4. electronic film.
5. image processing.

Each of which places different demands on the technology, as discussed in the next five sections.

1.3.1 Video

The camcorder market has driven the development of low-cost video technology and is worth 3 million units *per* year in the United States alone [27]. Extended battery life, has become an important selling point and, thus, provides the impetus for low-voltage design. A typical system runs off a 6V battery and dissipates 8W of power using 3.5V and 4.8V supplies. The digital processing consumes 50% of the power budget, motors 25%, and the analogue processing and sensor array the remaining 25% [51].

The required sensor resolution is defined by the television specification, which is 640×480 pixels. At present, pixel resolution is acceptable at 8-bits. However, with the advent of high-definition television, there will need to be an increase in pixel resolution and array size.

1.3.2 Multimedia

Both video and still-image multimedia markets exist, still-image cameras are considered in Section 1.3.3. Sixty million PCs were sold in 1996, therefore, the potential multimedia market is huge. It is anticipated that, if the cost of a peripheral drops below $\$50$, PCs will be bundled with it [27]. Consequently, in this market, cost is a critical issue. While performance is limited by communication rather than the camera unit. For example, the parallel-port limits frame-rates to 10Hz with an 8-bit 100×100 pixel image. With the advent of the 12Mbps USB interface,

which was shipped on 52 million desktop PCs in 1997, an 8-bit 300×300-pixel image can be transfered at 16Hz, however, performance is still limited by the communication system. Power is a further significant factor because it is preferable to use supplies from the host computer, at present 5V for a desktop PC.

Intel, Kodak, and VLSI Vision all offer USB video-cameras, and Xirlink's manufacture a USB video phone solution. It is expected that the launch of Windows 98 will increase the importance of this market [52].

1.3.3 Digital

According to the electronics industry, the digital camera is 1998's must-have accessory for the PC owner [53]. A digital camera is used like a conventional camera. The difference being the storage medium: digital memory rather than film. Images can be retrieved from memory and either printed on a colour printer or down-loaded to a PC. This market demands a higher performance than the previously mentioned markets in term of:

- **large pixel arrays.** The SXGA format is expected to become the industry standard at 1280×1024 pixels.
- **size and power,** because this is a portable application.
- **high-resolution.** At least 8-bit, but preferably 10-bit, performance is required.

1.3.4 Electronic film

The electronic film concept replaces the film in a standard 35mm camera with an imaging array. A host camera body and inter-changeable lenses help to provide improved image quality. In this market, size is a crucial issue because chips are stacked so that the whole system fits into a $35mm$ film-sized cartridge. Ideally, sensors for this market should have five to six million pixels [54].

1.3.5 Image processing

Signal processing can be added to an imaging system to provide extra functionality, for example, edge detection or contamination monitoring. For real-time applications, image pro-

cessing limits the quantity of data that can be processed and, therefore, defines the required pixel array size. Further, if the image is not viewed, the required resolution may be reduced.

1.4 Objectives and scope of thesis

The principal question addressed by this thesis is neatly summarized by Allard Lowenstein:

> The question should be, is it worth trying to do, not can it be done.

With that guiding philosophy in mind, the merits of CCD and CMOS cameras are investigated to determine which markets are suited to each technology. From a theoretical analysis, methods for improving CMOS image sensing technology are identified. A number of these are evaluated through the design of a test-chip, *Ginger Dancer*.

Within the limited time-frame of a Ph.D., research has to be constrained. In this work CMOS and CCD cameras are discussed from the point of view an analogue VLSI engineer. Further, issues within analogue design, such as the modelling of crosstalk, have been left to future work. Perhaps, the most important area excluded from this research is process tailoring for optical performance. In this area, the best source of information is the CCD Literature, however, future work must be carried out to evaluate the trade-off between optical and electrical properties in a hybrid process.

The work was supported by VLSI Vision plc, Edinburgh, one of the prominent developers of CMOS sensor technology. Unless indicated to the contrary, the work described herein was carried out independently and does not necessarily reflect the ideas of VLSI Vision. Naturally, the sponsorship has led to the concentration of this work on CMOS imaging technology; the CCD sensor is discussed to provide a benchmark.

Although there are potentially lucrative markets for sensors where the final image is not viewed, this thesis considers the requirements for markets where the image is viewed. The justification for this is that the technical challenges for a viewed image are more stringent and, therefore, if CMOS sensors are suitable for viewed imagers, they are even more competitive in the non-viewed markets.

1.5 Overview of thesis

This work is neatly divided into two: theoretical and experimental work. The first part of the thesis describes the theoretical work and is broken down into five chapters:

Chapter 2, which describes the fundamentals of CMOS sensor operation. Followed by a review of pixel architectures that compares size, noise performance, pixel voltage swing, saturation charge and sources of fixed-pattern noise.

Chapter 3. This presents the readout schemes for CMOS image-sensors.

Chapter 4 discusses the fundamentals of CCD imaging, and evaluates the potential for development.

Chapter 5 discusses how the scaling of CMOS technology will affect sensor performance.

Chapter 6. As an example of on-chip integration, this chapter discusses the analogue-to-digital converter. Chosen converters are compared for power-consumption and achievable resolution.

The second part of this thesis presents the design of *Ginger Dancer*, a chip used to validate some of the more promising suggestions from the theoretical analysis. It is divided into two chapters:

Chapter 7, which after discussing the chip design, evaluates the results from the test-chip.

Chapter 8 presents the conclusions of this work and summarizes the suggestions for future research.

Chapter 2
The CMOS camera: pixels

2.1 Overview

Over the last twenty years, a bewildering number of pixels suitable for integration on CMOS processes have been proposed. This chapter outlines the fundamental operation of a generic pixel before reviewing other pixel configurations. Promising pixel architectures are compared using a simplified layout model to drive important pixel characteristics. Finally, a number of novel pixel structures are proposed.

2.2 Basic operation

2.2.1 Photocurrent [1]

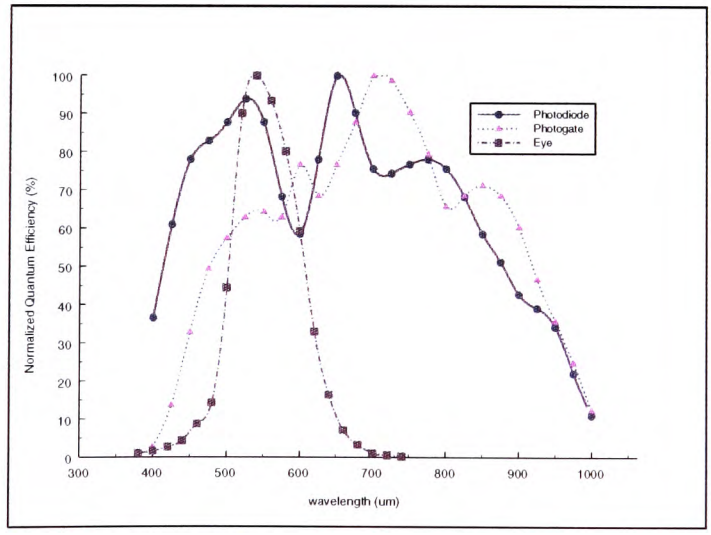


Figure 2.1: *Normalized quantum efficiency for a photogate pixel, photodiode pixel and the human eye [10, 11].*

The light sensitive area of a CMOS camera pixel is a *p-n* junction diode, which is operated under reverse bias. Incident light generates a photocurrent, which adds to the reverse saturation current of the diode. Whether a photon contributes to photo-current is determined by:

- The semiconductor absorption length, $l(\lambda)$, which is a function of wavelength and, in the visible spectrum, is a decreasing function of photon energy.
- The bandgap energy of the semiconductor, which determines the minimum photon energy, or longest wavelength, for absorption.
- The transmittance of the semiconductor surface.

The absorption of a light flux, I, of incident intensity I_o, is described by

$$I = I_o e^{-\frac{x}{l(\lambda)}} \tag{2.1}$$

where x is the distance travelled into the semiconductor. High-energy, short-wavelength photons are, on average, absorbed closer to the semiconductor surface than longer wavelength photons. For example, in the visible spectrum, violet light ($l(\lambda) = 0.3\mu m$) is absorbed closer to the semiconductor surface than red light ($l(\lambda) = 3\mu m$). The spectral response of the diode is a measure of the photocurrent generated *per* incident photon with light wavelength. Figure 2.1 shows the spectral response of two different types of pixel and the human eye.

In order to be absorbed by the semiconductor, a photon must have sufficient energy to generate an electron-hole pair, *i.e.* to excite a valence electron into the conduction band. The minimum change in potential energy is defined by the energy gap of the semi-conductor. This places a lower bound on the energy a photon must have to be absorbed, which, in silicon, corresponds to the far infrared portion of the spectrum (1.1μ). The pixel spectral responses shown in Figure 2.1 exhibit a reduction in absorption efficiency around $950\mu m$ because the photon energy is approximately the same as the semiconductor bandgap and, therefore, the photon is not easily absorbed. At wavelengths less than $400\mu m$, the energetic photons are absorbed before reaching the semiconductor bulk and, consequently, do not contribute to photocurrent.

Whether the electron-hole pair contributes to photo-current depends on where it is created. If it is generated within the depletion region of the diode, it will be swept apart by the electric field, thus, contributing to the photocurrent. A pair generated outside the depletion region will

diffuse through the semiconductor until it recombines or reaches a depletion region where it is swept apart. This may either be at the pixel or some other diffusion, such as a neighbouring pixel or the substrate on an epitaxial process. The number of pairs lost to recombination is a function of the electron and hole lifetime, which is lower at the surface due to the increased number of available recombination centres, often called surface states.

2.2.2 Surface reflection [2]

Before a photon can generate an electron-hole pair, it must pass from the air through surface layers to the silicon. Anagnostopoulos showed that a proper choice of oxide film thickness can substantially increase transmittance over the visible waveband. For example, increasing the gate-oxide thickness from 0.1μ to 0.18μ increased the transmittance by almost 50%. Further improvements could be obtained by using a 0.1μ top oxide, which is the optimal anti-reflection coating for an air-silicon interface.

A typical photosensor spectral response, such as that shown in Figure 2.1, has transmittance peaks, the amplitude and frequency of which are determined by the surface oxide thickness. For example, Anssi found a 20% amplitude variation in the pass band [12]. Results indicate that it is important to evaluate the optical properties of the air-pixel interface when choosing a process. Further, fabricating CMOS cameras on a non-standard process may be beneficial, particularly for pixels containing a polysilicon electrode. Such adjustments can be inexpensive, yet significantly improve imager performance. For example, Aubert improved the spectral response of a standard process by blocking the protective nitride layer and adjusting the oxide thickness over the photodiodes [55].

2.2.3 Reset

The reset operation can be thought of as sampling the reset voltage, V_{RT}, onto the pixel capacitance. There are two cases to consider, depending whether the gate voltage is sufficient to allow complete reset.

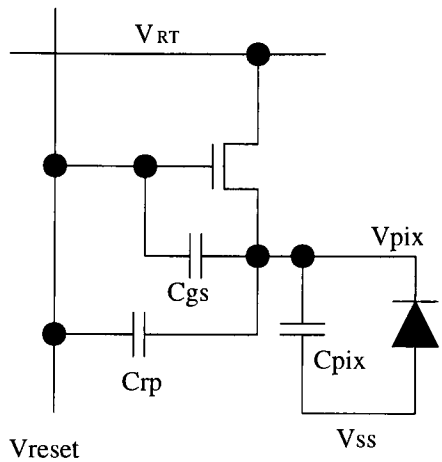


Figure 2.2: *A schematic showing the reset transistor and photodiode with associated signals and parasitic capacitances.*

2.2.3.1 Complete reset

If $V_G > V_{RT} + V_T(V_{RT})$, where V_G is the gate-substrate voltage of the reset transistor and $V_T(V_{RT})$ is the threshold voltage with a source-substrate voltage of V_{RT}, the reset operation is complete *i.e.* V_{pix} can charge to V_{RT}. At the end of the reset cycle, the reset transistor should operate in the linear region where it has a drain-source resistance, R, given by

$$R \approx \frac{1}{\frac{W}{L}k(V_G - V_{RT} - V_T(V_{RT}))} \tag{2.2}$$

Assuming that the reset transistor is able to source sufficient current to make the photocurrent negligible, the pixel voltage approaches the reset voltage with a time constant RC determined by the transistor drain-source resistance and pixel capacitance. A time, t_{res}, should be allowed for the reset operation, where t_{res} is given by

$$t_{res} > \frac{C_{pix}}{\frac{W}{L}k(V_G - V_{RT} - V_T)} \times N \ln 2 \tag{2.3}$$

where N is the desired resolution in bits; W and L are the transistor width and length, respectively; k is the transistor transconductance *per* unit area and C_{pix} is the pixel capacitance. For typical pixel values, even for 16-bit precision, only $10nS$ is required for settling if

$$V_G = V_{RT} + V_T(V_{RT}) + 0.2 \tag{2.4}$$

The maximum gate voltage, V_G, is limited by the process, consequently, Equation 2.4 effectively imposes an upper limit on the diode reset voltage.

Unfortunately, the maximum reset voltage is further limited by variation in the reset transistor threshold voltage, ΔV_T. The maximum threshold voltage that must be considered, $\Delta V_{T(max)}$, is discussed in Section E.2.1 and is shown to depend on array size and transistor dimensions. The upper bound on the reset voltage is given by

$$V_{RT} < V_{dd} - V_T(V_{RT}) - 0.2V - \Delta V_{T(max)} \tag{2.5}$$

If a $0.7V$ threshold voltage is assumed, Equation 2.5 gives a limit of approximately $V_{dd} - 1.3V$.

2.2.3.2 Incomplete reset

If V_G is not sufficient, the reset transistor charges the pixel to $V_{dd} - V_T$ and then enters the subthreshold region. The pixel will continue to charge until the subthreshold current is equal to the photocurrent. Therefore, the reset voltage will be a function of the photocurrent and the transistor threshold voltage. This systematic variation is an example of fixed-pattern noise, which is discussed further in Section 2.3.5.

2.2.3.3 Reset level variation

The reset operation is subject to four non-idealities: reset noise, capacitive coupling, charge injection and the "bowl effect". Each of these is discussed below.

Reset or $\frac{kT}{C}$ noise is introduced by the sampling operation because of the thermal noise present in the reset transistor [56]. For a typical pixel capacitance of $20fF$, the noise is equivalent to a charge, $\bar{q}_{kTC}$, given by

$$\bar{q}_{kTC} = \frac{\sqrt{kTC}}{q} = 57e^- \tag{2.6}$$

or a voltage uncertainty of $0.45mV$, which, if the maximum pixel discharge is 1V, limits the achievable signal-to-noise ratio to 67dB or, equivalently, a maximum digital resolution of 10-bits.

When the reset signal falls, capacitive coupling between the gate and source of the reset tran-

sistor, and the reset line and the pixel causes a drop in reset voltage, ΔV_{RT}, which is given by

$$\Delta V_{RT} = \frac{(C_{gs} + C_{rp}) \times V_{T(V_{RT})}}{C_{gs} + C_{rp} + C_{pix}} \tag{2.7}$$

where the parasitic capacitances C_x are defined in Figure 2.2. For a typical pixel configuration, this reduces the effective reset voltage by a further 0.1V from the value given by Equation 2.5.

During turn-off, the reset transistor channel charge must be distributed between the reset-voltage line and the pixel capacitance. If the signal fall-time is sufficiently long, a majority of the charge flows to the reset-voltage line [57], the remainder increases the pixel reset voltage, mitigating the capacitive coupling effect.

The bowl effect is caused by the variation in V_{RT} due to the finite resistance of the reset-voltage lines, which causes a delay in reseting pixels as distance from the voltage source is increased and a reduction in reset voltage due to the voltage drop caused by the reset current.

With the exception of reset noise, the above effects are constant for a given pixel, therefore, the variation can be cancelled using a stored reset value or by correlated-double sampling, which is discussed in Appendix D. If the pixel reset value is stored after each reset operation, the $\frac{kT}{C}$ noise can also be removed using correlated-double sampling.

2.2.4 Integration

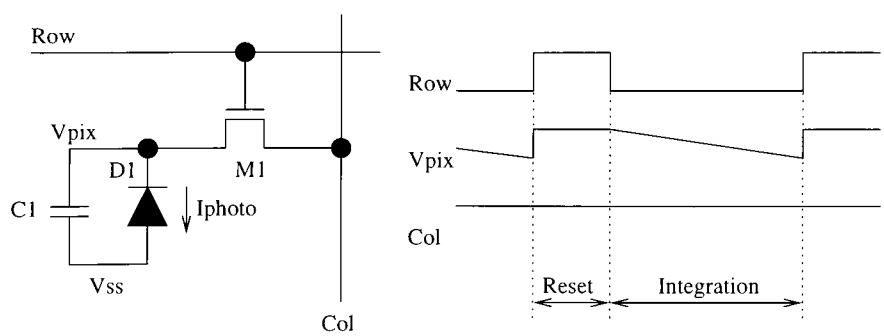


Figure 2.3: *A timing chart to show the reset operation and a simple pixel schematic.*

Under fluorescent lighting, a typical $10 \times 10\mu m^2$ pixel generates a photocurrent of 25pA. Moonlight yields a photocurrent about 3 orders of magnitude less and sunlight 3 orders of magnitude more. Consequently, a solid-state camera should be capable of detecting light over

six orders of magnitude. Equivalently, the readout circuit should be able to sense currents between a few fA and several nA [58]. A current of a few fA is difficult to detect, therefore, signal gain must be applied at the pixel site. The most common method of increasing the pixel output signal is to use an integration mode of operation [59]. At the start of the integration period, the pixel is reset to V_{RT} by the access transistor, M_1 in Figure 2.3, which is then turned off isolating the pixel. The pixel remains isolated for the integration period during which the photocurrent discharges the pixel capacitance to produce an output signal; this is either the drop in pixel voltage or the charge removed from the pixel capacitance.

The charge removed from the pixel is simply the integral of the diode reverse current over the integration time, t_{int}. Under uniform illumination, the signal charge, Q, is given by

$$Q = \int_0^{t_{int}} i_r dt \tag{2.8}$$

where i_r is the sum of the photocurrent and reverse-diode current. It can be seen that the signal charge is linearly proportional to i_r and the integration time, t_{int}.

A significant proportion of the pixel capacitance is the voltage-dependent diffusion capacitance. Hence, whilst the signal charge is linearly proportional to the photocurrent, the signal voltage is not. Weckler showed that, under the assumption of a linear diode junction, the pixel voltage, V_{pix}, is given by

$$V_{pix}(t) = [V_{RT}^{\frac{2}{3}} - \frac{2}{3} j_{photo} (\frac{12}{qa\epsilon^2})^{\frac{1}{3}} t]^{\frac{3}{2}} \tag{2.9}$$

where j_{photo} is the average photocurrent *per* unit area; a is the junction doping profile gradient and other symbols have their usual meaning [59].

A further advantage of using the integration mode of operation is that, by varying the integration time, the pixel output signal can be maximized for the incident light intensity [59]. This is typically done by limiting the number of completely discharged pixels across the array to lie within a given range. The required frame rate limits the maximum integration time and the minimum is determined by the system clock, yielding an exposure ratio of n^2, where n is the number of pixel rows.

A disadvantage of integration is that it results in the attenuation of high-frequency information,

the mean-square-error is given by

$$MSE = \int_{-\frac{1}{2}}^{\frac{1}{2}} (1 - sinc(\pi T f))^2 df \tag{2.10}$$

where T is the integration time [58]. This problem is particularly noticeable under low-lighting conditions, because of the increase in integration time.

2.3 Non-ideal effects

The preceding discussion ignores a number of important non-idealities, which limit the achievable image quality. The most significant effects are discussed in this section.

2.3.1 Dark current [3]

An isolated, reverse-biased diode discharges without any illumination. This is due to so-called dark current, which is composed of the diode leakage current, as predicted by the ideal-diode equation, and current generated in the diode space-charge region. For a typical silicon diode the generation-recombination current is, at least, an order-of-magnitude greater than the diffusion current, which is ignored in the remainder of this work. The photocurrent and generation-recombination current are indistinguishable, therefore, the magnitude of the dark current places a lower limit on the detectable light level.

The generation-recombination current density, J_{gr}, is given by

$$J_{gr} = \frac{q n_i x_d}{2\tau_o} \tag{2.11}$$

where x_d is the width of the space-charge region and τ_o is the minority carrier lifetime. Equation 2.11 shows that the recombination current is proportional to the width of the space-charge region, consequently, by altering the doping profile, a pixel can be designed with a reduced space-charge region width and, therefore, lower dark current [23]. The other significant term in Equation 2.11 is the minority carrier lifetime, τ_o, which is given by

$$\tau_o = \frac{q}{N_t k T \sigma_o} \tag{2.12}$$

where N_t is the number of recombination centres *per* unit area and σ_o is a capture cross-section.

The density of recombination centres is higher at the semiconductor surface, therefore, the surface space-charge region can contribute significantly to the reverse-diode current, and, hence, should be reduced in width. Further, the diode should be shaped to minimize the perimeter-to-area ratio. Ihara suggests that stress and etching damage during fabrication causes an increase in recombination centres and, hence, dark current, which can be mitigated by careful pixel layout [21].

A further important consideration is that the dark-current doubles for every 8^oC increase in temperature [60]. Consequently, in a practical device, where the junction temperature is higher than the ambient temperature, dark current can limit the pixel sensitivity. For example, Smith found that the pixel temperature was 47^oC with an ambient temperature of 25^oC [60]. In the same work dark current fixed-pattern noise was found to limit the achievable signal-to-noise ratio to 28dB for a 200ms exposure. At a frame rate of 30Hz, if the integration time is equal to the frame time, the dark current fixed-pattern noise limits the resolution to 44dB or 6.5bit resolution. The integration time must, therefore, be reduced, which limits the minimum detectable light level. In a digital camera, with a mechanical shutter, the dark current fixed-pattern noise can be suppressed using a second signal reading after a further period in which the sensor is in the dark and hence, pixel discharge is only by dark current [60].

In conclusion, dark current is the fundamental limit to the sensitivity of a CMOS sensor-chip and, therefore, needs to be reduced as far as possible. A number of techniques have been suggested. Firstly, power consumption should be carefully controlled to prevent an increase in operation temperature. Further, care must be taken to ensure that the power dissipation is spread evenly across the chip, so significant temperature gradients do not exist. In parallel with the drive to minimize dark current for a given process, work is needed to optimize pixel layout in order to reduce process stress and to alter the doping profile to further reduce dark current. A departure from standard CMOS processes may also be required to reduce the space-charge region width and mitigate the effect of surface states.

2.3.2 Charge crosstalk

An electron-hole pair generated beyond the pixel space-charge region can contribute to photo-current, provided that it diffuses to the space-charge region. However, due to the random nature of diffusion, the pair may be lost to the substrate or be swept apart in the space-charge region associated with other diffusions, for example, a neighbouring pixel. Under high illumination,

this crosstalk of charge becomes more noticeable, as bright spots or lines in an image. Two image defects caused by the crosstalk of charge are:

- **Blooming,** which is defined as the spread of charge to neighbouring pixels, creating bright spots in an image.
- **Smear**, which results in bright vertical lines in an image, caused by charge collected by diffusions connected to the columns of a diode array.

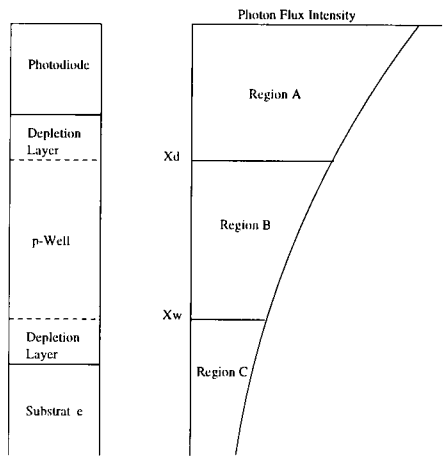


Figure 2.4: *A vertical cross-section through a diffusion-substrate pixel.*

Figure 2.4 shows a vertical cross-section through a diffusion-substrate pixel. If recombination is insignificant, charge generated in region A, from the surface to the depletion layer, is collected as signal charge. Those formed in region C are swept to the substrate. Electron-hole pairs formed in region B can either diffuse to the photo-diode, substrate, or to neighbouring diffusions. A worst-case analysis of the signal-to-crosstalk-charge ratio, R_q, = yields [14]

$$R_q(\lambda) = \frac{q_A}{q_b} = \frac{\int_0^{x_d} e^{-\alpha(\lambda)x} dx}{\int_{x_d}^{x_w} e^{-\alpha(\lambda)x} dx} \tag{2.13}$$

If a pixel formed in a well, such as that shown in Figure 2.4, there is a parasitic vertical bipolar transistor (VBT) formed to substrate and lateral bipolar transistors (LBT) to neighbouring diffusions. The ratio of the current gain of these two transistors determines the proportion of the available smear charge that contributes to smear and blooming.

For a passive pixel, the crosstalk contribution is worse than that predicted by Equation 2.13, because all the pixels on a column contribute to smear. Therefore, the smear charge from all pixels must be summed to calculate the signal-to-smear ratio, SSR, which is given by [14]

$$SSR = \frac{(\beta_l + \beta_v) \int_0^{x_d} e^{-\alpha(\lambda)x} dx}{\beta_l \sum_{i=1}^{N} \int_{x_d}^{x_w} e^{-\alpha(\lambda)x} dx} \tag{2.14}$$

where N is the number of pixels that share the column; β_l is the current gain of the LBT formed by the pixel and column diffusions and β_v is the current gain of the VBT formed by the pixel and substrate. To suppress smear, a reading from a column with no pixels accessed is subtracted from the signal. If voltage-sensing is used, the column bias current should be sufficiently large to make smear charge insignificant. Subthreshold leakage current through the access transistor is a further contributor to smear charge.

A further cause of crosstalk is light leakage by multi-reflection paths, which can be dependent on pixel layout as well as process. Without careful design, a light-shield over the pixel can act as a waveguide, thus, contributing to crosstalk. It has been suggested that light leakage is responsible for a majority of smear because smear increases with incident light angle [14]. This requires further investigation.

2.3.3 Capacitive coupling

Parasitic capacitance contributes to the signal charge by coupling voltage changes on, for example, clock lines to the pixel itself. Further, the variation in parasitic capacitance values leads to fixed-pattern noise [61]. Fry showed that the diode reset voltage, V_{RT}, was given by

$$V_{RT} = V_{RT} - \Delta V(\frac{C_{gs} + \Delta C_{gs}}{C_d}) \tag{2.15}$$

where C_{gs} is the gate-source parasitic capacitance; C_d is the pixel capacitance; ΔV is the reset clock swing and it is assumed that the gate voltage is sufficient to fully charge the pixel. Ohba showed, that for a charge sensing readout, the capacitive coupling from illuminated, integrating pixels to the column could result in a significant contribution to the sensed charge [62].

2.3.4 Random noise

The minimum detectable level of light in a camera is limited by the noise introduced to the camera system. Noise can either be systematic or random. A systematic noise, for example, an offset due to the variation in threshold voltage across the pixel array, is known as fixed-pattern noise and is considered in Section 2.3.5. This section considers how the fundamental noise mechanisms discussed in Appendix B, limit the performance of an arbitrary pixel.

2.3.4.1 Shot noise

Both dark current and photocurrent contribute shot noise, therefore, the spectral density, S_{is}, is given by

$$S_{is} = 2q(I_{photo} + I_{dark}) \tag{2.16}$$

In an integrating sensor, the shot noise contribution is a noise charge, with a spectral density, S_{qs}, given by

$$S_{qs} = 2q(I_{photo} + I_{dark}) \times t_{int} \tag{2.17}$$

As pixel size and the integration time is reduced, shot noise becomes more significant because the photocurrent is proportional to area, whilst the rms shot noise is proportional to the square-root of the product of pixel area and integration time. In practice, shot noise can be insignificant compared to the pixel-to-pixel fixed-pattern noise caused by dark-current. For example, Smith found that the fixed-pattern noise was 20 times greater than the shot current noise [60].

2.3.4.2 Thermal and flicker noise

Due to the requirement for high packing density, the pixel transistors are often minimum size. Therefore, flicker noise, which is inversely proportional to the transistor area, is usually a significant effect. The relative importance of thermal and flicker noise depends on the pixel configuration and subsequent processing; the contribution of each to specific pixel architectures is discussed for each in Section 2.7.3.

2.3.5 Fixed-pattern noise

Fixed-pattern noise is defined as any systematic variation in output signal resulting from the parallel signal paths in a CMOS sensor. Common causes of fixed-pattern noise include transistor dimension variations and threshold-voltage mismatch. Circuits that are frequently used in pixel configurations are considered in this section, other sources are discussed throughout this thesis.

2.3.5.1 The source follower

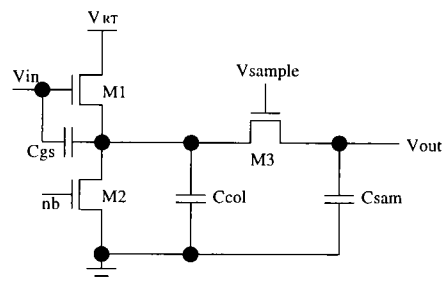


Figure 2.5: *The pixel source follower and column sampling circuit.*

A source follower can be used to buffer the pixel capacitance from the much larger column capacitance. The output voltage, V_{out}, is given by

$$V_{out} = V_{in} - V_{T0} - \gamma(\sqrt{2|\Phi_F| + V_{out}} - \sqrt{2|\Phi_F|}) - \sqrt{\frac{I_{col}}{\mu C_{ox}\frac{W}{L}}} \tag{2.18}$$

The most significant cause of fixed-pattern noise is due to variations in the threshold voltage of the driver transistor, M_1 in Figure 2.5. Unfortunately, the driver transistor is often chosen to be minimum size, which, as discussed in Section E.2.1, increases the threshold voltage variation. In a $0.7\mu m$ process with an average threshold voltage of 0.8V, assuming that the body effect is negligible, the sensor should be designed to tolerate threshold voltage variation between 0.65 and 0.97V. This cause of fixed-pattern noise must be suppressed using correlated-double sampling, or by subtracting a stored pixel offset.

Comparatively, the mismatch due to variations in column current, transistor dimensions and transconductance are small. For example, if the average gate-source voltage is given by $V_T + 0.2V$, a 0.2V variation in gate-source voltage would require the column current to quadruple, or the transistor dimensions to increase by a factor of 4. Figure E.1 shows that the column current

is much more tightly controllable.

A more significant effect is due to the output resistance of the column load and source follower. Often a simple current mirror is used to provide the column load, therefore, there is significant variation in the column bias current with signal voltage. This adds further non-linearity to the voltage signal. In order to reduce this effect long load transistors should be used. Low-voltage operation precludes the use of cascode transistors to improve this aspect of performance.

2.4 Available parasitic diodes.

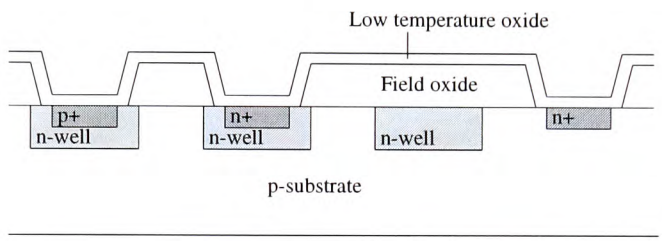


Figure 2.6: *CMOS-compatible photodiodes.*

The parasitic diodes that can be fabricated in a standard n-well process are:

- The n^+–p-substrate diode, which is the most commonly used photoreceptor, because it can be easily integrated into the pixel structure by extending the drain of the appropriate transistor. A further advantage of the pixel is that it does not require a n-well, which would reduce the achievable packing density because of the minimum inter-well gap and the need to include well-contacts.
- The n-well–substrate diode collects charge deep into the substrate. Consequently, it is sensitive to substrate noise and crosstalk from neighbouring pixels. A further disadvantage of this structure is that the reverse-diode current is 5 to 10 times larger than the n^+–p-substrate diode, due to the extended depletion regions [55].
- The n^+–n-well-substrate diode suffers from increased reverse-diode current and area over the diffusion-substrate diode.
- The p^+–n-well diode collection depth is limited by the well. Therefore, pixel crosstalk is reduced at the expense of packing density and a reduction in long-wavelength quantum efficiency.

The variation in spectral response with doping concentration and vertical dimensions needs to be investigated. Where a standard CMOS process is used, neither is optimized for light detection. Section 4.6.1 describes how the doping concentration in a CCD pixel are optimized to reduce the reverse-bias current. It is likely that the junction depth is not critical because the electron and hole diffusion lengths are long compared to the vertical dimensions of a CMOS process [1]. However, well and epitaxial layer depth may be more important in determining the photodiode spectral response.

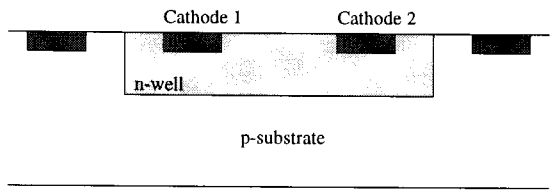


Figure 2.7: *The lateral effect photodiode after Anssi [12]*

An alternative pixel structure to the vertical diodes described previously is shown in Figure 2.7. The lateral-effect photodiode uses a horizontal n^+–n–p–p^+ profile. Consequently, integration density is too low to be considered useful for viewed imagers. A further disadvantage of the lateral-effect photodiode is that the reverse diode current is large because of the doping profile and shallow current flow. If a large multiple-cathode diode is used, the relative current magnitudes at each boundary can be used to determine an image spot position [12].

2.5 A review of pixel architectures

Throughout the review of pixel architectures, pixel operation is described and specific design issues are highlighted. Promising architectures are evaluated in Section 2.7 for

- size
- fill-factor
- saturation charge capacity
- fixed-pattern noise
- sources of random noise

Schematics are presented for selected pixel architectures along with minimum layout patterns. A key to the layout patterns is given in Figure 2.8.

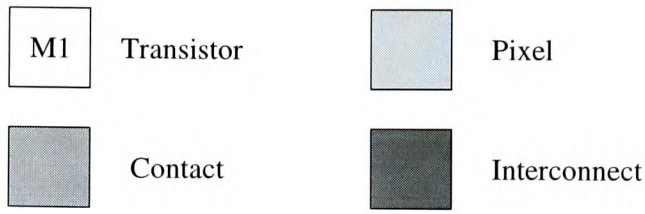


Figure 2.8: *A key for the pixel layout diagrams presented throughout this chapter.*

2.5.1 Charge-readout or passive pixels

By definition, a passive pixel does not contain an amplifying transistor. Consequently, the readout signal is a charge packet, which, in an array architecture, must be sensed on a highly capacitive bit-line. This provides the fundamental performance limit and is discussed in Section 3.4. However, the simplicity of the structure results in a large fill-factor, which, coupled with the maximum possible voltage swing, yields a saturation charge significantly larger than either current- or voltage-readout pixels.

2.5.1.1 The basic passive pixel

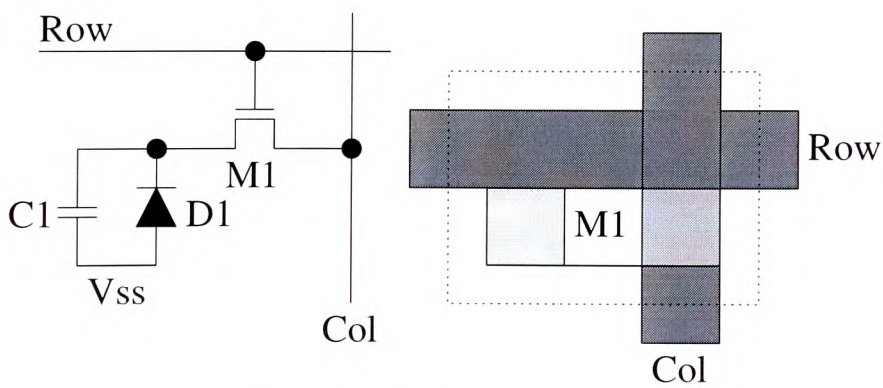


Figure 2.9: *The basic passive pixel.*

The simplest example of a passive pixel is shown in Figure 2.9. It comprises a single access transistor; the drain is extended to form the pixel and the source is connected to the column. At the beginning of the sensing cycle, *Row* is enabled and the pixel is reset to the column voltage,

V_{RT}. When Row returns low the integration period begins. After the integration period, Row returns high and the charge required to charge the pixel to V_{RT} is sensed by a column amplifier. Readout is, therefore, destructive.

2.5.1.2 Fixed-pattern and random noise

Variation in the access transistor channel charge over time and across the array lead to random and fixed-pattern noise contributions, respectively. The random noise contribution is calculated in Section 2.7.3.

The fixed-pattern noise contribution is caused by the variation in threshold voltage and gate-capacitance, which cause a variation in channel charge, Q_g, given by

$$\Delta Q_g = C_g \Delta V_T + \Delta C_g (V_{gs} - V_T) \tag{2.19}$$

where C_g is the access transistor gate-channel capacitance and V_{gs} is the total variation in the access transistor gate voltage over a pixel period. Variations in the gate-drain capacitance also cause a fixed-pattern noise. These sources of fixed-pattern noise can be suppressed by integrating the pixel output over the readout period [62].

An additional problem with large passive pixel arrays is that low charge levels from distant pixels provide insufficient energy to charge the distributed capacitance of the column bus [44].

2.5.1.3 A passive pixel with overflow drain transistor

A second transistor, M_1 in Figure 2.10, can be added to the passive pixel to provide protection from blooming. This overflow drain (OFD) transistor starts to conduct as the pixel voltage drops towards $V_{OFD} - V_T$ and, hence, reduces the pixel discharge rate. Ideally, V_{OFD} is chosen to be a threshold voltage above ground and, hence, the voltage swing at the pixel is not significantly reduced. However, variations in the threshold voltage mean that a higher value of V_{OFD} must be selected. Further, devices exhibiting a low threshold voltage will turn on prematurely saturating the pixel value. Consequently, the voltage swing at the pixel is reduced by the tolerated variation in the threshold voltage of the overflow drain transistor. For this reason, a transistor greater than minimum size is used [13]. The extra transistor and interconnect for the OFD signal reduce the fill-factor by about 8% for a $10\mu m$ pixel pitch in a $0.5\mu m$ technology. The resulting saturation

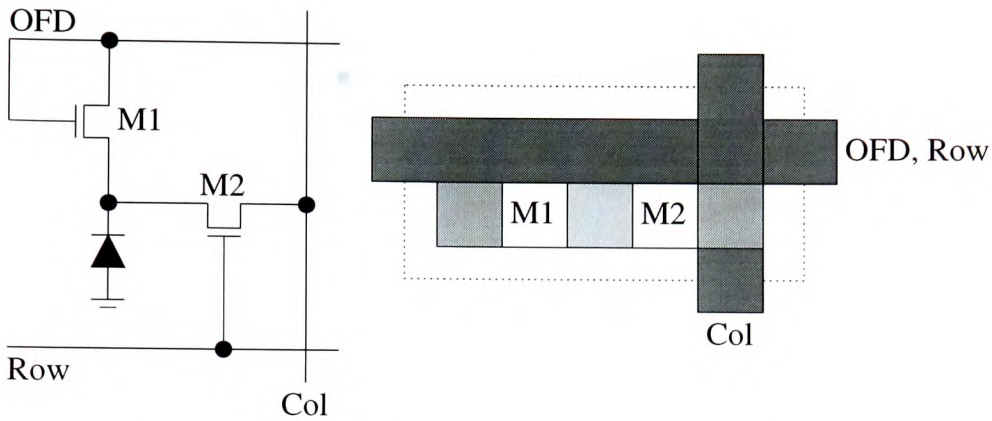


Figure 2.10: *A passive pixel with an additional transistor to limit pixel discharge after Jansson [13].*

charge is still significantly higher than other pixel configurations.

2.5.1.4 Other passive pixel variations

Other variations to the standard passive pixel include:

- A second access transistor, which Ando used to allow X-Y addressability [63].
- A $p^+ - n^+$ photodiode, which was used to increase the capacitance of the photodiode [14, 63]. This yields benefits in increased saturation charge, reduced thermally generated dark-current and an improved signal-to-noise ratio.
- A double-diffused sense-line, as shown in Figure 2.11. The p^+-diffusion under the column diffusion suppresses the action of the lateral bipolar transistor formed by the column implant and pixel and, therefore, reduces smear. The implant extends under the access transistor and, consequently, increases the threshold voltage. In the study by Ohba, the threshold voltage increased to 3V, which renders the technique unsuitable for a low-voltage sensor [14]. A further disadvantage of this technique is that it increases the capacitance of the sense-line, which, as discussed in Section 3.4 reduces the achievable signal-to-noise ratio.

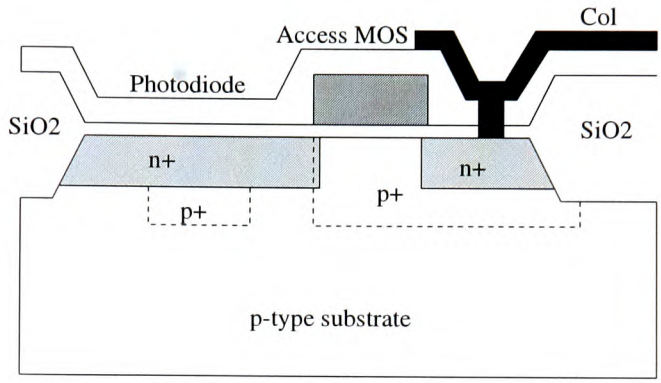


Figure 2.11: *A cross-section of a passive pixel designed to suppress blooming after Ohba[14].*

2.5.2 Active pixels

By definition, an active pixel contains one or more amplifying transistors. The extra transistors are used to either provide gain or to buffer the pixel from the large column capacitance.

2.5.2.1 The standard active pixel

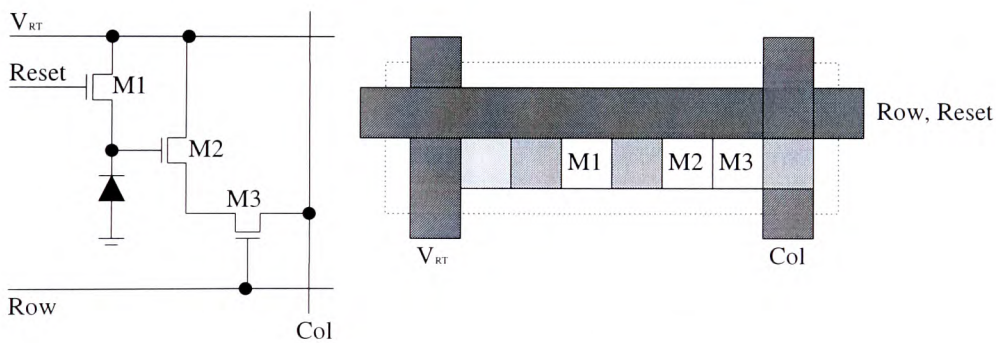


Figure 2.12: *A standard active pixel.*

The standard active pixel, shown in Figure 2.12, comprises a reset transistor, M_1, a source follower, M_2, and a read transistor, M_3, which allows each pixel to be addressed individually. The read transistor can be included above or below the source-follower transistor, as shown in Figures 2.12 and 2.13. The operation of both pixels is comparable, therefore, the choice between the two architectures is made by ease of layout and in order to reduce parasitic capacitances.

The inclusion of a source-follower transistor limits the useful discharge of the pixel and, hence, reduces the achievable voltage swing. The minimum pixel voltage must be sufficient for the

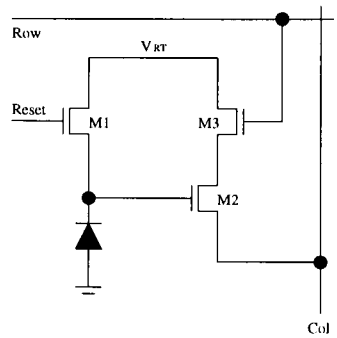


Figure 2.13: *An alternative active pixel configuration.*

column load to remain in saturation and the source-follower transistor to conduct the required column current. Consequently, the voltage swing is limited to $V_{RT} - V_{GS2} - V_{DS}$ where V_{DS} is the saturation voltage of the column current sink and V_{GS2} is the gate-source voltage of the source-follower transistor. Variation in the threshold voltage of the pixel source-follower further decreases the achievable voltage swing.

If it is assumed that a minimum size transistor is used for the in-pixel source follower, the value of V_{GS2} is determined by the minimum column current, which depends on the required readout rate and total capacitance seen at the output of the source follower. For a typical frame rate of 30 Hz, the line time of a 1000 row sensor is $33\mu s$. The amplifier and further signal processing will determine the proportion of this time that can be used to charge the column capacitance. If $5\mu s$ is allowed, the minimum column current, I_{col}, is given by

$$I_{col} = C\frac{dV}{dt} \approx (C_{col} + C_{sample}) \times \frac{V_{swing}}{T_{settle}} = 6pF \times \frac{1}{5\mu} = 1.2\mu A \qquad (2.20)$$

where V_{swing} is the voltage swing at the pixel and the chosen values are typical for the sensor array under consideration. The required column current requires a gate-source voltage of $V_T + 0.1V$ for a typical process. Summarizing, the minimum voltage the pixel can discharge to is $V_T(V_{out}) + 0.3 + V_{DS} \approx 1.3V$ where it is assumed that 0.2V is allowed for threshold voltage variation.

The maximum pixel voltage was derived in Section 2.2.3, which combined with the minimum pixel voltage yields the pixel voltage swing, which is equal to $V_{dd} - 2.5V$. Therefore, if a voltage swing of 1V is assumed, an active pixel sensor fabricated on a $0.8V$ threshold process requires a 3.5V supply, which (as discussed in Chapter 5) is unsuitable for processes beyond the

$0.5\mu m$ generation. For low-power operation, it may be preferable to provide a separate higher supply for pixel reset than the analogue and digital sections of the chip.

2.5.2.2 Minimum column current

In the preceding section, an estimate for the minimum column current was used to calculate the required gate-source voltage for the in-pixel source follower. A more detailed derivation of the column current is presented in this section, which is given for an array of n-pixel rows.

The minimum column current must drive the capacitive load, which comprises the sampling capacitance, C_{sample}, and the parasitic column capacitance, C_{col}. C_{sample} must be sufficient to reduce the $\frac{kT}{C}$ noise to an acceptable level for the given resolution and C_{col} is determined by the array size and layout. The total capacitive load, C_L is given by

$$C_L = nC_{sf} + C_{sample} \tag{2.21}$$

where the column capacitance is represented as $nC_{sf} = C_{col}$ to highlight the linear increase in column capacitance with the number of rows. In order to calculate the minimum column bias current, the maximum permissable settling time, T_{settle}, must also be determined. T_{settle} is given by

$$T_{settle} = \eta \times \frac{1}{nf} \tag{2.22}$$

where f is the frame rate and η is the proportion of the line time that is allowed for settling. Therefore, under the assumption of slew-rate limiting, the minimum column bias current, I_{col}, is given by

$$I_{col} = C_L \times \frac{\Delta V}{T_{settle}} = \frac{nf\Delta V}{\eta} \times (nC_{sf} + C_{sample}) \tag{2.23}$$

Interpretation of Equation 2.23 shows that for large array sizes, where $nC_{sf} \gg C_{sample}$ the total column bias current is proportional to n^3 and, as shown in Figure 2.14, becomes unacceptably high at large array sizes with low η. Note that the values assumed when plotting Equation 2.23 in Figure 2.14 are $\Delta V = 1V$; $f = 30Hz$ and $C_{sf} = 4fF$, which are all typical values for a commercial image sensor. The minimum column current, under the assumption of bandwidth limiting, is also plotted in Figure 2.14. The Figure shows that, for the array sizes

under consideration, the column current is slew-rate limited and, therefore, the analysis of the preceding section is valid.

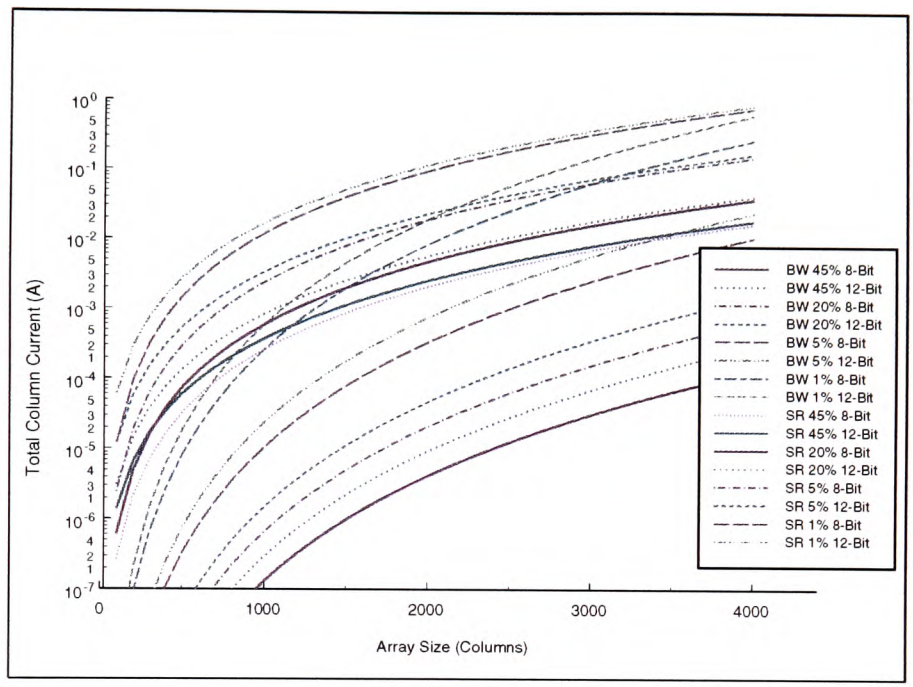


Figure 2.14: *The sampling current required under the assumption of bandwidth (BW) and slew-rate (SR) limiting for selected settling performance and using the given percentages of the readout time for settling.*

2.5.2.3 An active pixel with increased gain

The pixel shown in Figure 2.15 is first considered with M_2 clocked as a standard reset transistor. An extra transistor, M_1, is added to the standard active pixel to act as a common-gate amplifier, buffering the node A from the pixel. The photocurrent flows through M_1 and discharges the capacitance C_A. Therefore, the amplifier achieves a voltage gain of $\frac{C_{pix}}{C_A}$ over a standard active pixel. This pixel is not considered further because:

- The value of $\frac{C_{pix}}{C_A}$ is not well controlled, therefore, fixed-pattern noise is introduced.
- Pixel gain leads to a deterioration in signal-to-noise ratio for two reasons:
  1. The pixel output voltage swing is limited, therefore, if pixel gain is applied, assum-

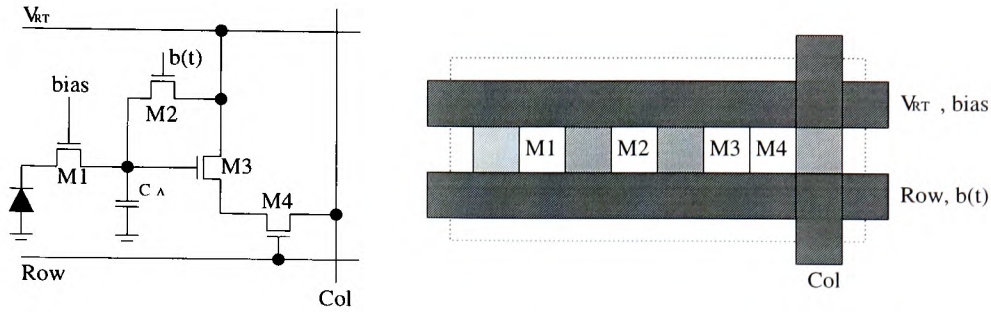


Figure 2.15: *An active pixel after Yamawaki [15] with additional buffer transistor, M_1, using a novel reset transistor clocking scheme, shown in Figure 2.16.*

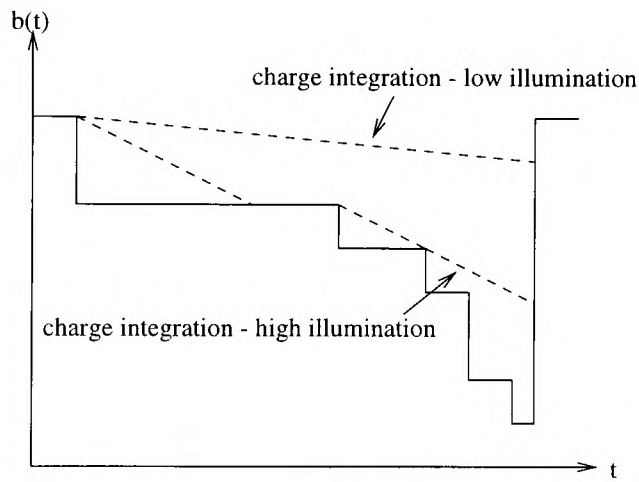


Figure 2.16: *The clocking schemed for $b(t)$ used to increase the effective saturation charge of the active pixel shown in Figure 2.15 [15].*

ing that the pixel-generated noise remains the same and dominates noise from the output stage, the noise charge accounts for a higher percentage of the output swing.

2. Capacitor C_A is smaller than the pixel capacitance, therefore, it will discharge more quickly, reducing the integration time for a given light level. Consequently, because the shot noise contribution is proportional to the square-root of the integration time, while the signal is proportional to the integration time, the signal-to-noise performance of the pixel will deteriorate.

Deckler proposes a novel clocking scheme, shown in Figure 2.16, for the reset transistor [64]. The clocking scheme is applicable to any reset transistor and is considered despite the pixel configuration being disregarded. The reset transistor is used to limit the discharge of the node

A in an identical way to the overflow drain transistor described in Section 2.5.1.3. However, Deckler progressively lowers the gate voltage throughout the integration period. This clocking scheme was used to increases the effective saturation charge of the pixel 20-fold. If the introduced non-linearity is acceptable, the increase in integration time should improve imager performance.

2.5.3 Logarithmic mode of operation

If a standard active pixel is operated with $Reset = V_{RT}$ the pixel output varies logarithmically with illumination intensity [65].The reset transistor, M_1 in Figure 2.12, conducts the photocurrent and, consequently, operates in the subthreshold region, where drain-source current, I_{DS}, is given by [66]

$$I_{DS} = \beta e^{-\frac{V_{T0}}{nU_T}}(e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}}) \tag{2.24}$$

If $Reset = V_{RT} = V_{dd}$ and M_1 is saturated, the pixel voltage is given by [66]

$$V_{pix} = \frac{1}{n}(V_{dd} - V_{T0}) - U_T \ln \frac{i_{photo}}{\beta} \tag{2.25}$$

where n is the subthreshold slope factor, which is given by [66]

$$n = 1 + \frac{\gamma}{2\sqrt{2\phi_F + V_S}} \tag{2.26}$$

where γ is the body effect factor, which is given by [66]

$$\gamma = \frac{\sqrt{2qN_B\epsilon}}{C_{ox}} \tag{2.27}$$

Unlike the previously described modes of operation, an integration time is not used. Therefore, the pixel output is continuously available, allowing the pixel data to be output randomly in time [67]. Typically, the output voltage changes by 50mV per decade of light variation. This is of the same order as pixel offset non-uniformity, consequently fixed-pattern noise renders the raw image useless [68]. Offset subtraction can be used to suppress the fixed-pattern noise below 2%, which may be sufficient for image-processing applications.

Although the output is randomly addressable in time, this advantage is limited because the

sensor output may change at a similar rate to the standard frame-rate. For example, in a dark room the photocurrent, which could be on the order of tens of fA, must discharge the pixel capacitance, leading to a response time as high as 1s [58].

This mode of operation may be useful if image illumination varies over many orders of magnitude. However, the level of fixed-pattern noise is unsuitable for viewed images.

2.5.4 Photogate pixels

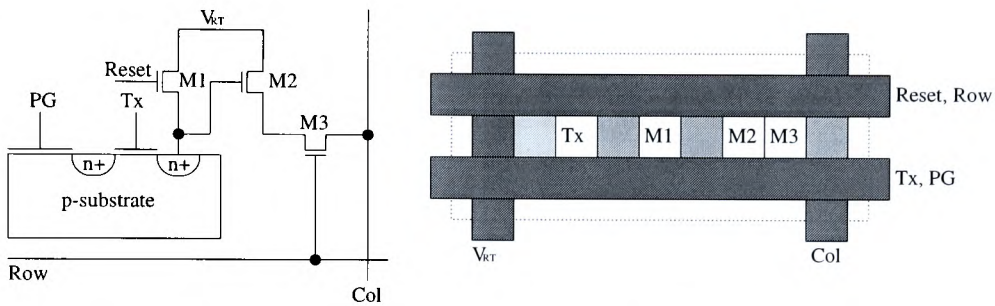


Figure 2.17: *A photogate pixel after Fossum* et al *[16, 17].*

A photogate pixel, such as that shown in Figure 2.17, is essentially a single-pixel surface-channel CCD imager [16, 17]. The pixel comprises two sections: a photosite and charge-sensing amplifier, separated by the transmission gate, T_x in Figure 2.17. Unlike the previously discussed pixels, the electron-hole pairs generated by incident electrons are not separated by the space-charge field of a diode. Instead the photogate, PG is biased to form a well, which separates and stores the generated charge. At the end of the integration time, the following steps are taken to produce an output signal:

1. the floating-diffusion node is reset using transistor M_1.
2. the reset pulse is removed and the floating-diffusion node is allowed to float.
3. a reset output value is stored.
4. the photogate electrode is biased to transfer the charge under the transmission gate to the floating-diffusion node.
5. the signal output value is taken, the difference between this and the stored reset value is the pixel value.

A fundamental problem with the photogate pixel is that incident light must pass through a polysilicon electrode before reaching the substrate. Absorption in the electrode results in reduced short-wavelength responsivity (see Figure 2.1). In order to mitigate this effect, a non-standard process where the transmittance of the electrode is optimized should be used. A further disadvantage of the photogate pixel is that, in a CMOS process, the transfer of charge between the pixel and floating-diffusion node is not optimized, leading to the introduction of $\frac{kT}{C}$ noise and image lag.

Assuming a perfect charge transfer between the pixel and sensing node, the two advantages of a photogate pixel are that

- Correlated-double sampling suppresses $\frac{KT}{C}$ noise without the need for a frame-memory store.
- The sensing capacitance is smaller than the pixel capacitance of a standard active-pixel sensor. Therefore, the pixel yields a relatively high voltage gain, which is defined as $\frac{q}{C_{sf}}$ where C_{sf} is the capacitance at the charge-to-voltage conversion node.

Although pixel gain is often stated as an advantage [17, 69], this may not be the case for two reasons:

1. Variation in the capacitance C_{sf} will cause pixel-to-pixel fixed-pattern noise.
2. The pixel output swing is severely limited and while pixel gain will improve the signal-to-noise ratio due to noise from the readout circuitry, the analysis presented in Section 2.7.3 and 3.5.1 shows that noise originating in the pixel will dominate the overall noise performance. The signal-to-noise ratio due to noise from the pixel will deteriorate with increased pixel gain.

2.5.5 Current-mode pixels

Current-mode pixels can be created using either MOSFET transistors or, more commonly, using a bipolar phototransistor.

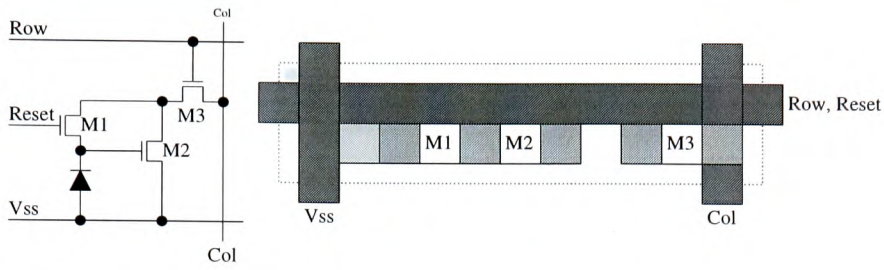


Figure 2.18: *A dynamic current mirror based pixel after McGrath [18].*

2.5.5.1 The dynamic-current-mirror pixel [18]

McGrath proposed a pixel, shown in Figure 2.18, based on an NMOS dynamic current mirror. The pixel is reset by sinking a known reference current, I_{ref}, from the column. At the start of the integration period, the reset signal is removed and the pixel capacitance begins to discharge. At the end of integration, Row is enabled and the current sunk from the column is measured. The difference between this and the reference current is the pixel value.

Expressed mathematically, the pixel value at the beginning of integration, V_{RT}, is given by

$$I_{ref} = \frac{1}{2}\beta(V_{RT} - V_T)^2 \Rightarrow V_{RT} = \sqrt{\frac{2I_{ref}}{\beta}} + V_T \tag{2.28}$$

Integration decreases V_{RT} by ΔV, so that the output current at the end of the integration time, I_{out}, is given by

$$I_{out} = \frac{1}{2}\beta(V_{RT} - \Delta V - V_T)^2 \tag{2.29}$$

substitution for V_{RT} yields

$$I_{out} = I_{ref} + \frac{1}{2}\beta\Delta V^2 - \sqrt{2I_{ref}\beta}\Delta V \tag{2.30}$$

Equation 2.30 shows that the output current is independent of the threshold voltage of transistor M_2. However, fixed-pattern noise is introduced due to variations in the transistor transconductance and column reference current. Charge injection and clock feed-through from the reset transistor are a further source of fixed-pattern noise. Unfortunately, these four sources of fixed-pattern noise are not suppressed by correlated-double sampling. However, for non-viewed images, the fixed-pattern noise residual level of about 1% is satisfactory.

2.5.5.2 The phototransistor

A bipolar phototransistor is used to provide pixel-site gain, which amplifies the photocurrent, which is also the base current, by the transistor gain, β, to produce a collector current, $I_C = \beta I_B$. Further amplification can be obtained by using a Darlington transistor so that the output current is sufficiently large to be used without an integrating mode of operation.

A standard CMOS process allows both lateral- and vertical-bipolar transistor to be constructed [70]. The use of both transistors is limited by non-ideal effects:

- The vertical bipolar uses the substrate as the collector, which must be tied to ground.
- A parasitic vertical-bipolar transistor limits the performance of the lateral transistor. The lateral collector collects only α_L of emitter current, the remainder is collected by the vertical bipolar. The relative gains of the two transistors depends on the surface-area-to-side-wall ratio if the emitter, which should be maximized to increase the lateral current gain.
- The lateral bipolar suffers from a low output resistance, therefore, a CMOS cascode device is often used [24].
- The transient response time of the phototransistor is limited by the rate that the photocurrent can charge the collector-base capacitance [58].
- The dynamic range of a phototransistor is 1-2 decades smaller than a photodiode[71].

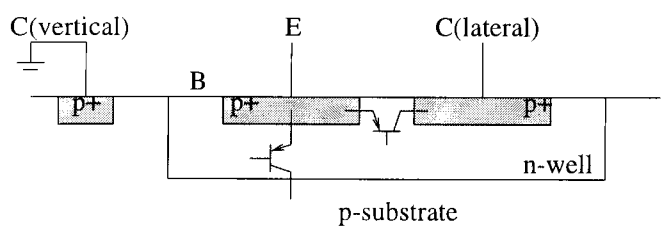


Figure 2.19: *A vertical-bipolar transistor using a CMOS process.*

The fundamental problem with bipolar transistors is the variation in current gain. For example, Sandage found the fixed-pattern noise due to collector current was between 2 and 3 % [72]. If a lateral-bipolar transistor is used, a positively biased, minimum width polysilicon gate can help control the base width and, hence, β variations [73]. However, the fixed-pattern noise remains too high for viewed images.

2.5.6 Charge-sharing pixels

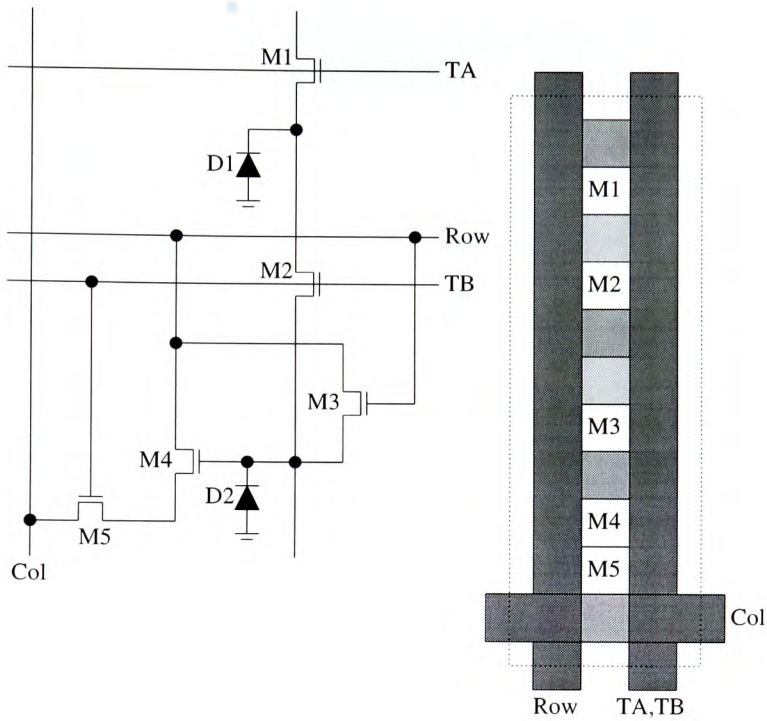


Figure 2.20: *An interlaced, charge-sharing pixel after Yadid [19].*

Yadid proposed a pixel, shown in Figure 2.20, which is effectively a standard active pixel with the pixel divided by a pass transistor, M_2. This design allows a shrink of pixel pitch by approximately a third. However, it must be used in a two-line mixing, interlaced mode. A further disadvantage of this pixel structure is the fixed-pattern noise introduced by variation in the pass-transistor gate-source and drain-source capacitances. This is discussed for a similar pixel structure in Section 7.3.2.4.

2.5.7 Capacitive pixels

Applications such as digital still photography require large array sizes, therefore, to maintain yield, there is a requirement for smaller active pixels with a reduced pixel component count [21]. An example of such a pixel, shown in Figure 2.21, is an active pixel with the read transistor omitted. Functionality is maintained by the coupling capacitance, C_1.

During the read operation, the Row line is taken high, which, through capacitive coupling, turns the source follower transistor on. In the previously discussed active pixels, the source follower

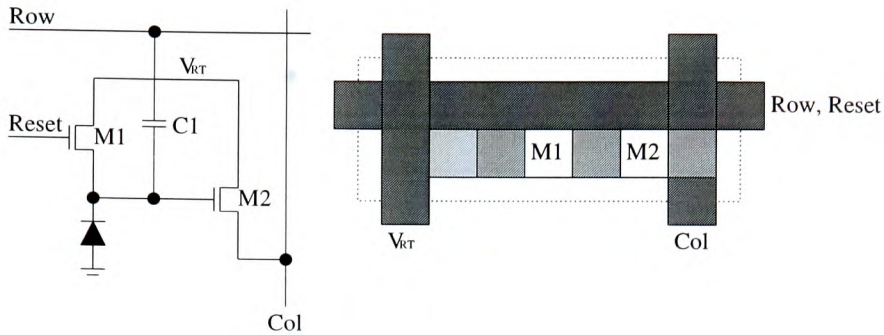


Figure 2.21: *An active pixel without a read transistor (2T-cell) after Oba [20].*

does not conduct current when the pixel is not being accessed because the read transistor prevents current flowing. However, in the proposed pixel the gate-source voltage of the source follower is used to limit current flow. This imposes an upper bound on the pixel reset level, V_{RTmax}, to limit the source follower subthreshold current so that the total leakage current in a column is small compared to the bias current, I_{col}.

In order to correctly bias the in-pixel source follower of a fully discharged, or light, pixel its voltage, V_{pix}, during the read operation, must be increased to

$$V_{pix} > V_{Tmax} + \sqrt{\frac{2I_{col}}{\beta_{M_2}}} + V_{DS(sat)} = V_{pixRd} \tag{2.31}$$

where $V_{DS(sat)}$ is the saturation voltage of the column load transistor. Consequently, the increase in potential of Row, Δ_{Row}, must satisfy

$$\Delta_{Row} > \frac{C_1 + C_{pix}}{C_1} \times V_{pixRd} \tag{2.32}$$

because of the effects of charge sharing between the coupling capacitance, C_1, and the total pixel parasitic capacitance, C_{pix}. Equation 2.32 shows that the coupling capacitance must be on the same order as the pixel capacitance in order to limit the required voltage on Row. It should be noted that part of the pixel capacitance is a non-linear diffusion capacitance. Therefore, this method of reading a pixel introduces further non-linearity into the output value.

Figure 2.22 shows an active pixel configuration without a read transistor and a combined row and reset signal line, a potential diagram to explain the operation is shown in Figure 2.23. This configuration imposes a further limitation on the Row signal: during the read operation V_{Row}

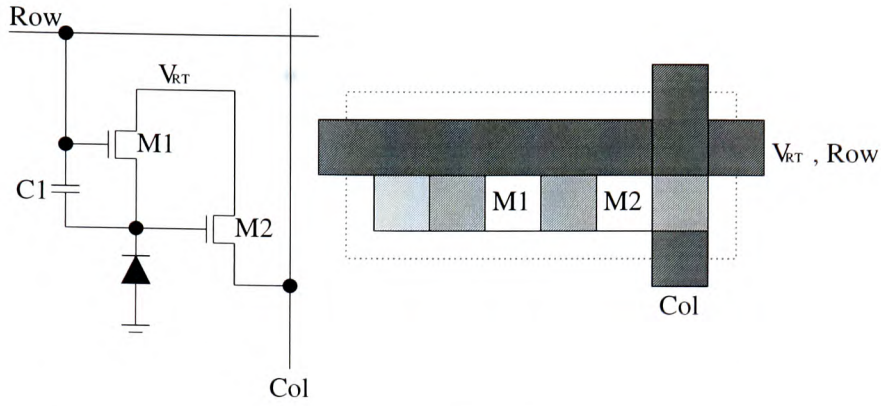


Figure 2.22: *An active pixel without a read transistor or Reset line after Ihara [21].*

must not be high enough to reset the diode. Assuming that Row is held at ground during integration Δ_{Row} must satisfy

$$\Delta_{Row} < \frac{C_{pix}}{C_1} \times V_{Tmin} \tag{2.33}$$

Equations 2.33 and 2.32 show that this pixel requires a multi-threshold process: M_1 should have a higher threshold voltage than M_2.

Another transistor is removed from the pixel shown in Figure 2.24. The read operation is identical to the two previously described pixels, reset, however, is completely different. Instead of using a reset transistor, the stored charge is discharged to substrate by applying a negative pulse to Row. To prevent the need for a negative voltage Row should be biased midway between V_{ss} and V_{dd} during the integrate period. Further investigation of this reset method is required to prove that the reset voltage is independent of the previous pixel value.

Two voltages are commonly defined for capacitive pixels:

1. **The overflow margin,** which is defined as the difference in voltage between the gate of the reset transistor and the pixel voltage of a fully-discharged pixel during a read operation *i.e.* it is a measure of whether the pixel will reset during the read operation.

2. **The access margin,** which is defined as the difference in pixel potential of a fully-discharged pixel during the read operation and a reset pixel.

Good design dictates that these two margins should be equal and must be greater than any fixed-

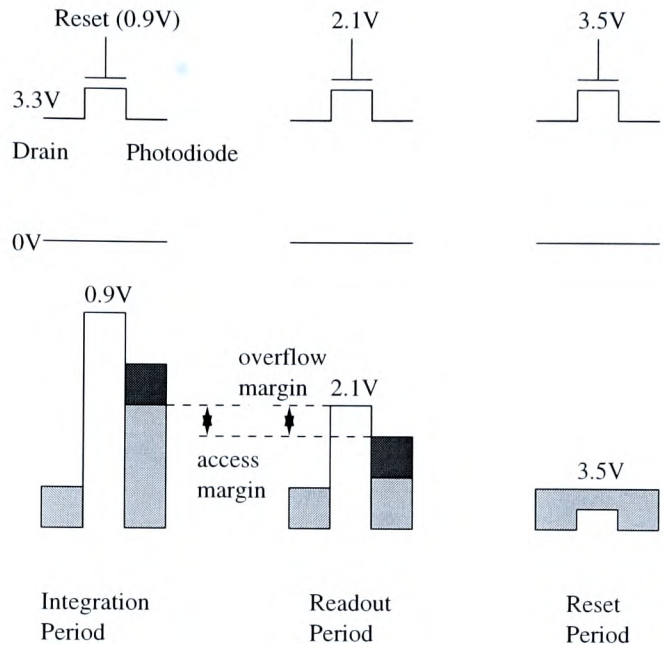


Figure 2.23: *A potential diagram showing the overflow and access margin for the reset transistor after Ihara [21].*

pattern noise due to offsets within the pixel, for example, variations in threshold voltages and in the reset voltage due to variations in the coupling and pixel capacitances.

In order to maximize pixel density, the minimum-area layout patterns, shown in Figure 2.25, have been proposed. These result in a greater horizontal than vertical resolution, which is unsuitable for most imaging applications. Therefore, a zig-zag layout technique, in which one photodiode is present in each unit block, should be used [20].

2.5.8 Shuttered pixels

A shuttered pixel uses a memory element to store the pixel value so that it can be read repeatedly or it can be addressed randomly in time. Figures 2.26 and 2.27 show two examples of shuttered pixels. A pass transistor, M_2, is used to isolate the pixel from the memory element, which is the parasitic capacitance seen at the gate node of the output transistor, M_3 in Figure 2.26 and M_4 in Figure 2.27. Unfortunately, the storage capacitance suffers from leakage and, hence, the output value decays over time. It is expected that dark current associated with the diffusion capacitance at the drain of the pass-transistor will discharge the stored value. However, a number of studies

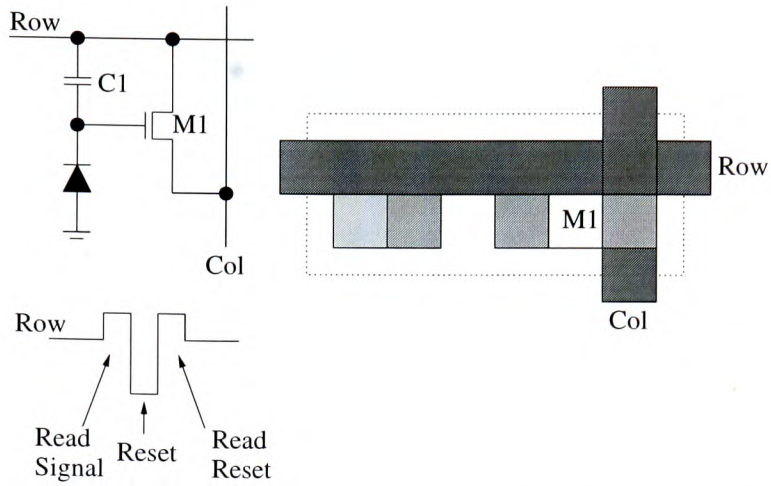


Figure 2.24: *A single transistor active pixel (1T-cell) after Oba [20].*

have indicated that, despite shielding, the discharge is greater than that due to dark current [19, 74]. This discharge is due to photogenerated charge diffusing to the space-charge region associated with the diffusion capacitance.

An alternative method of providing a frame-memory is the on-chip integration of an analogue memory array. For example, Simoni used an array of shielded, passive pixels to store the output value from the sensor array [74]. Unfortunately, this method doubles the chip size and suffers from leakage from the storage capacitances. If a frame-memory is required, an off-chip digital memory is likely to be the most effective solution.

2.5.9 Silicon retina

The term silicon retina is used to describe biologically inspired imaging chips. Such sensors adapt to both local and global light intensity and produce a continuous-time output [49]. A continuous-time output can simplify subsequent image processing [75]. For example, a video-rate image of 30 frames/s allows an object to move several pixels between samples. Motion detection is, therefore, converted from a local problem to a much more difficult correspondence problem. Further, high frequency information is lost [76]. The need for a continuous output renders integrating pixels unsuitable. Consequently, a logarithmic output is often used.

Figure 2.28 shows an implementation of a silicon-retina pixel. Transistor Q_1 is a phototransistor, its base current is amplified by the Darlington-connected transistors, $Q_2 - Q_4$, so that

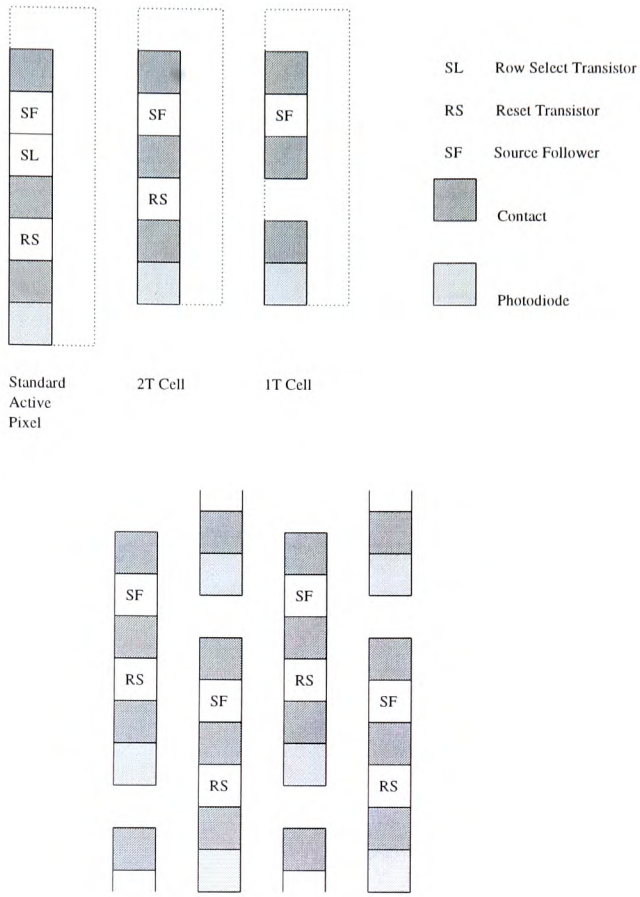


Figure 2.25: *Minimum layout patterns and a zig-zag pixel layout after Oba [20].*

an output current of $I_{photo} \times \beta^4$ is supplied to the load device, M_3. Four bipolar transistors are used to provide sufficient current to drive the load to V_{dd}. Transistors M_1 and M_2 are biased in the subthreshold region and sink a majority of the emitter current from Q_1. The characteristics of the feedback element, which comprises transistors M_1 and M_2 produce an output voltage that is logarithmic, with a slope of 325mV *per* decade over five orders of illumination magnitude. The use of the feedback transistors in the subthreshold region introduces fixed-pattern noise and renders the images unsuitable for viewed video sensors.

2.5.10 Other pixels

Numerous other pixels have been proposed. For completeness these are included in this section along with alternative technologies to standard CMOS and CCD imagers. In general, the alternative technologies suffer from large pixel size and high fixed-pattern noise and are not

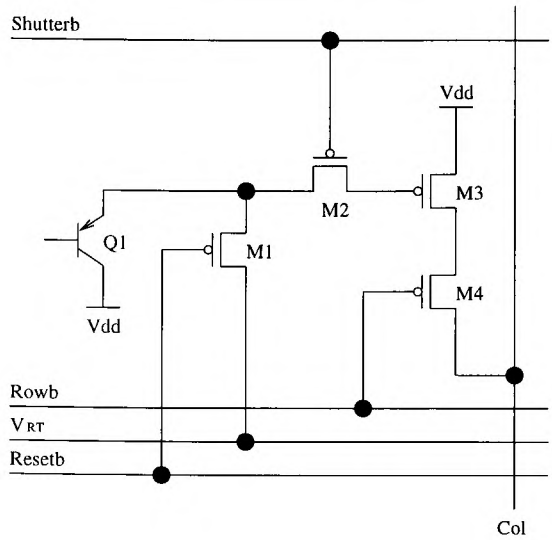


Figure 2.26: *A current-output shuttered pixel after Huat [22].*

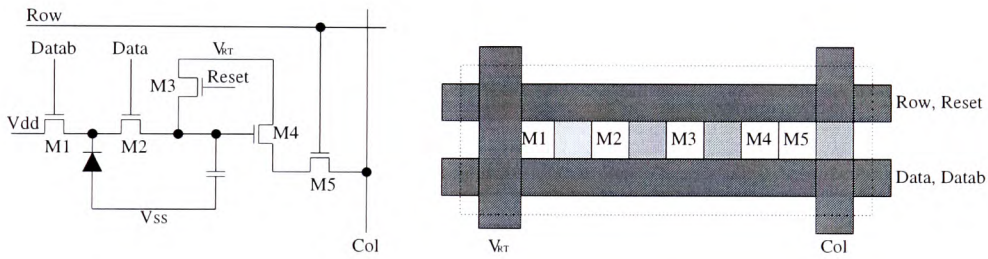


Figure 2.27: *A shuttered active pixel after Kyomasu [23].*

considered as a serious challenger to either CMOS or CCD technology.

2.5.10.1 A ring-oscillator pixel [25]

Figure 2.29 shows a novel pixel that outputs a series of pulses, the frequency of which is proportional to the incident light intensity. The pixel is reset by applying the output pulses to the transistor M_1. If initially the diode is reset, the pixel begins to charge the input node to the first inverter. At some time later, the input voltage exceeds the threshold of the first inverter and the leading edge of the reset pulse travels down the inverter cascade, reseting the diode, which when it is discharged to below the threshold of the first inverter, sends the trailing edge of the reset pulse down the inverter cascade and the integration period begins again.

The pixel achieves a linear response over five orders of magnitude of illumination and benefits

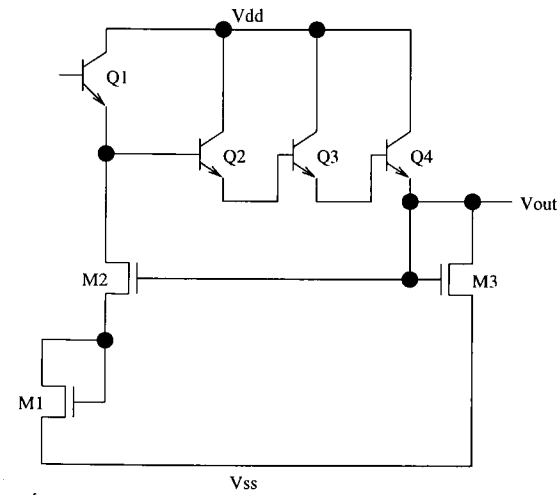


Figure 2.28: *A silicon retina pixel cell after Mead [24].*

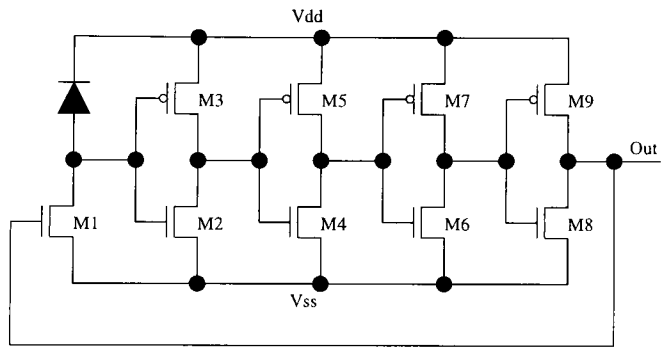


Figure 2.29: *A ring-oscillator based pixel after Yang [25].*

from not needing a global integration time, where the image exposure is determined by the brightest part of the image. However, the pixel is unsuitable for integration on a viewed image sensor because:

- **Pixel size.** The reported pixel size of $107 \times 107\mu m^2$ in a $2\mu m$ technology, precludes integration on viewed image sensors [25].
- **Fixed-pattern noise.** The time taken for a pulse to travel along the inverter cascade will vary with, for example, variation in threshold voltage.
- The **pulse output** will pose considerable design problems, perhaps, requiring a dedicated counter at each pixel site, which is only feasible for a linear sensor.

2.5.10.2 BCAST - buried charge accumulator and sensing transistor [26]

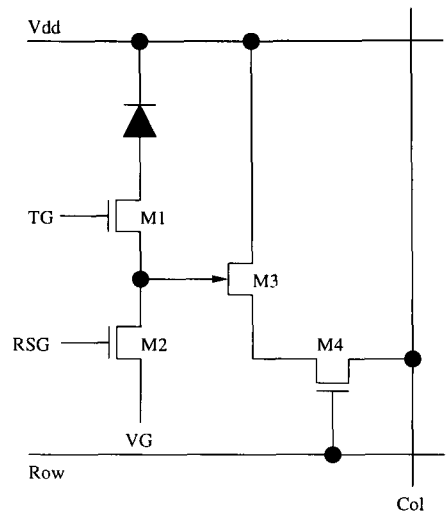


Figure 2.30: *A BCAST pixel after Nomura [26].*

The BCAST pixel, shown in Figure 2.30, is essentially a standard active pixel fabricated in a non-standard process. A buried photodiode is used to reduce dark current and a JFET source-follower transistor further improves the signal-to-noise ratio. Transistor M_1 acts as a shutter and M_2 resets the source-follower transistor prior to readout.

2.5.10.3 Double-gate floating surface transistor

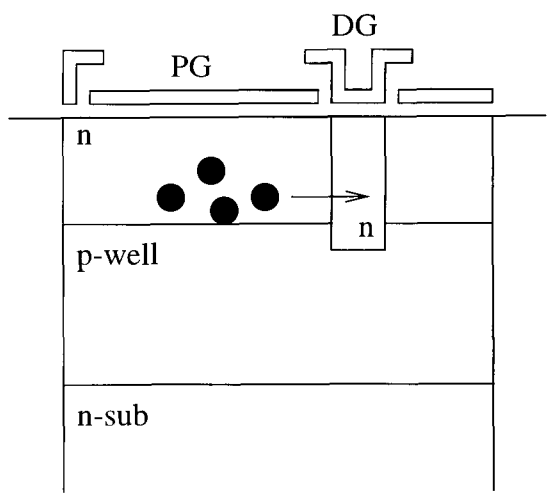


Figure 2.31: *A double-gate floating surface transistor [27].*

The pixel, shown in Figure 2.31, consists of a buried-channel MOS photogate region and a surface PMOS transistor, which is the output amplifier. Optically generated charge is accumulated under the photogate. At the end of the integration time, charge is transfered to the n-doped confinement region, which acts as a back-gate on the PMOS transistor. The integrated charge modulates the PMOS transistor drain-source current to produce an output signal. The double-gate floating surface transistor suffers from about 10% fixed-pattern noise due to potential variations in the sensing transistor. This could be reduced by a form of correlated-double sampling.

2.5.10.4 Charge modulation device

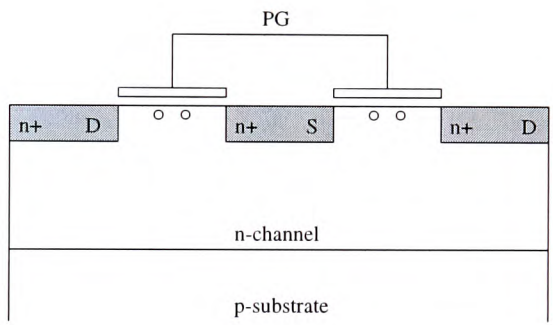


Figure 2.32: *Charge modulation device [27].*

Optically generated hole charge is integrated at the MOS surface. This modulates the channel current of the buried channel NMOS transistor, which surrounds the collection region. The device suffers from high dark current because of the surface states. Further, fixed-pattern noise is high due to geometric variation.

2.5.10.5 Bulk charge modulation device

The bulk charge modulation device is similar to the charge modulation device but is more complex and achieves a higher performance. The buried PMOS readout transistor uses electrons confined in the n-type region as a signal on the backgate. The confinement region is fully depleted by a vertical reset operation that dumps electrons over a p-type barrier into the substrate. A low-noise buried-channel MOSFET is used for readout.

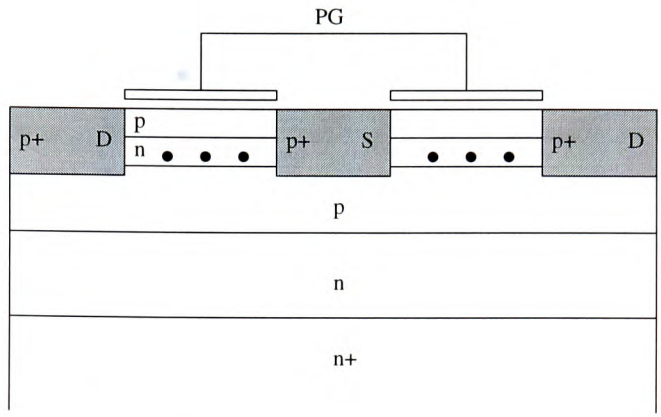


Figure 2.33: *A buried channel charge modulation device [27].*

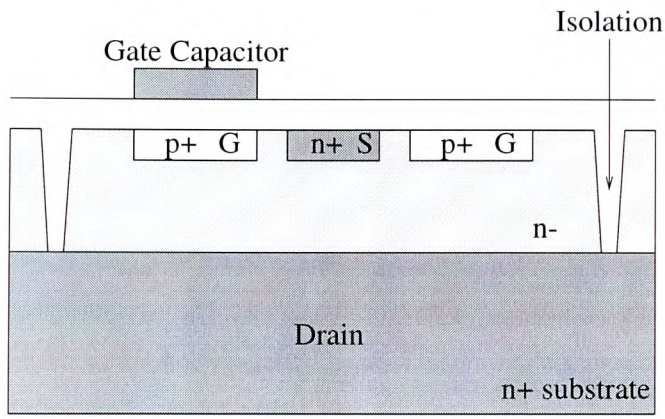


Figure 2.34: *The SIT image sensor after Yusa [28].*

2.5.10.6 SIT image sensor [28]

The SIT imager comprises a n^+ substrate, which acts as the drain, and a n^- epitaxial layer, which contains a n^+ source, which is surrounded by a p^+ gate. A MOS capacitor on gate that is pulsed to reset the device. The gate is reverse biased to create a depletion region where electrons are swept to source or drain and holes accumulate on the gate, increasing the gate voltage, which modulates the drain-source current. Trench isolation is used to stop channels forming from pixel to pixel. The SIT imager suffers from large pixels ($30 \times 30\mu m^2$) and the fact that the junction is not fully depleted during reset and, therefore, is subject to $\frac{kT}{C}$ noise.

2.5.10.7 Alternative materials

The previously discussed pixels have all been fabricated on CMOS-based silicon processes. Huang used the increased absorption coefficient of an amorphous-silicon film to increase the optically active area [77]. The a-Si:H film is overlaid on a MOS transistor array, which senses the potential relief induced on photoconductive film. The transistor size, $720 \times 20\mu m^2$, is impractical for conventional imagers.

2.6 Future-generation pixels

In future generations of CMOS image sensors, improvements to pixel performance will be made through process evolution, pixel layout and circuit architecture. For example, recent advances in CMOS technology, in particular the availability of improved p^+-doping, have allowed IMEC to introduce a barrier around non-photoactive transistors, effectively increasing the pixel sensitivity [50]. If tailored processes with buried photodiodes are not used, a move away from the traditional L-shaped pixel to pixels with reduced perimeter-to-area ratios can be expected to reduce dark current. Changes in pixel architecture aim to improve the pixel packing density and/or performance. Three pixel schemes are presented in the next three sections, two aim to improve the pixel fill-factor for a given pitch, the third uses a shuttered pixel to store the reset voltage to allow true correlated-double sampling.

2.6.1 An active pixel with improved fill-factor

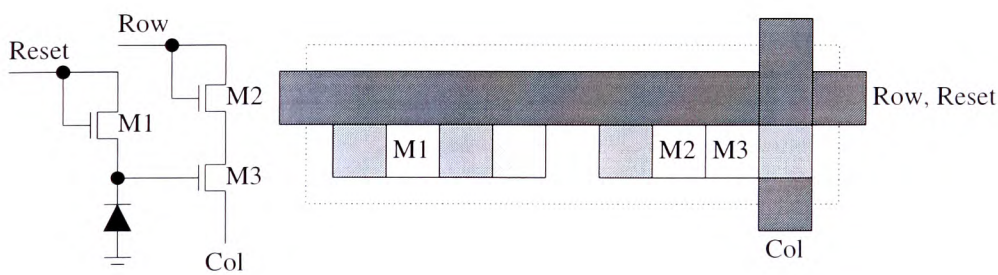


Figure 2.35: *An active pixel without a V_{Rt} line.*

In a standard active pixel, current only flows through the reset transistor when Reset is high. Similarly, the source-follower and read transistors only conduct when Read is high. Consequently, functionality can be maintained using the circuit shown in Figure 2.35. This has

the advantage that a V_{RT} connection is not made to the pixel cell, therefore, one interconnect line can be saved. Analysis in Section 2.7 suggests that this yields a 7% fill-factor increase over a standard active pixel. The improvement in fill-factor must be balanced against the required increase in current supplied by the Reset and Read driver. This technique would, therefore, be more attractive for small and medium array sizes.

2.6.2 A multiplexed active pixel

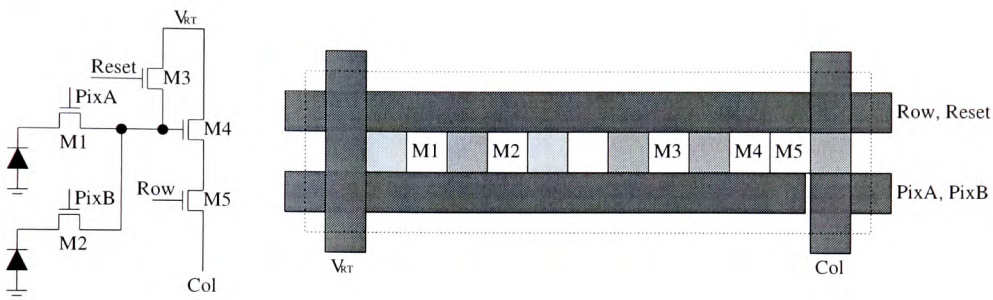


Figure 2.36: *A multiplexed active pixel.*

The source follower, used in a standard active pixel, is only operational during the read cycle. Consequently, if the corresponding read cycles do not overlap, a source follower can be shared between neighbouring pixels. Figure 2.36 shows two pixels that share a common source follower. The analysis in Section 2.7 predicts that, if a source follower is shared between two pixels, there is no improvement in fill-factor over a standard active pixel. However, if the technique is applied to four pixels, there should be a significant increase in the achievable fill-factor.

2.6.3 A shuttered active pixel operated to suppress reset noise

Noise analysis for the active pixel, presented in Section 2.7.3, shows that $\frac{kT}{C}$ noise limits the signal-to-noise ratio to 10-bits. Hurwitz uses an off-chip frame memory [78] to store the reset value. This allows true correlated-double sampling to cancel the $\frac{kT}{C}$ noise, as described in Appendix D. Unfortunately, this solution is impractical for video-rate imagers, which use an alternative form of correlated-double sampling which does not suppress $\frac{kT}{C}$ noise. In Figure 2.37 a timing scheme for a shuttered pixel is proposed to use a pixel-level memory element to store the reset value and, hence, allow true correlated-double sampling. Operation of the pixel is as follows:

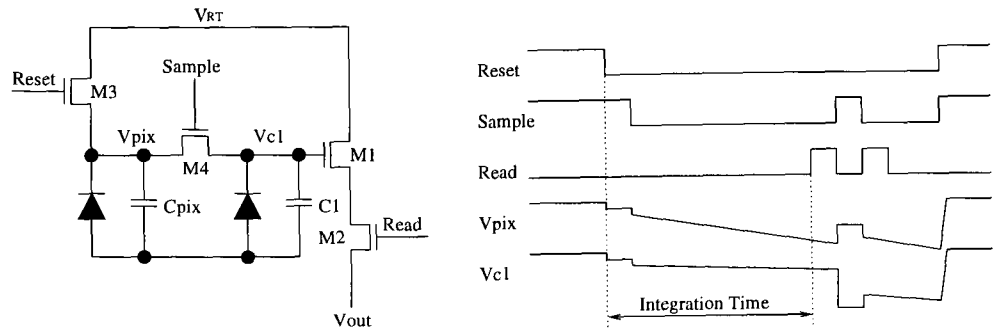


Figure 2.37: *An active pixel schematic and timing diagram showing a mode of operation intended to suppress reset noise.*

1. The pixel and sampling capacitor, C_1, is reset to V_{RT}, with noise uncertainty $\bar{v}_{RT}$ due to noise on the V_{RT} bias line and $\frac{kT}{C}$ noise introduced by the reset transistor.

2. The sampling capacitor is isolated from the pixel and the integration time begins. As Sample goes low, the channel charge is distributed between the pixel and sampling capacitance, and charge is coupled from Sample through the gate-source and gate-drain capacitances. A further non-ideality is the introduced $\frac{kT}{C}$ noise by the sampling transistor gate capacitance, however, this can be substantially smaller than the pixel reset noise charge.

3. Read of the reset value, V_R, which is given by

$$V_R = V_{RT} + \bar{v}_{RT} - \delta V + q_a/C_1 \tag{2.34}$$

where δV is the sampling capacitance discharge over the integration period due to the diffusion of charge from the pixel and photogenerated charge caused by reflected light or transmittance through the shield; and q_a is the charge introduced to C_1 as Sample falls.

4. Sample is pulsed high and the potentials of the pixel and sampling capacitor are equalized.

5. Read of the signal value, V_S, which is given by

$$V_S = \frac{C_1 V_R + C_{pix}(V_{RT} + \bar{v}_{RT} - \Delta V + \frac{q_b}{C_{pix}})}{C_{pix} + C_1} + \frac{q_c}{C_1} \tag{2.35}$$

where q_b is the charge injected onto C_{pix} at the beginning of the integration period and q_c

is the charge injected onto C_1 when the two capacitors are isolated immediately before the signal read.

6. The CDS operation is performed resulting in a pixel output signal, V_{CDS}, given by

$$V_{CDS} = \frac{C_{pix}(\Delta V - \delta V) + q_b + q_c \frac{C_{pix}+C_1}{C_1} - q_a \frac{C_{pix}}{C_1}}{C_{pix} + C_1} \tag{2.36}$$

A number of factors determine whether this operation is feasible:

1. This mode of operation attenuates the signal at the pixel by a factor of $\frac{\Delta V - \delta V}{\Delta V} \times \frac{C_{pix}}{C_{pix}+C_1}$. In order to maintain the present signal-to-noise ratio, this factor must be close to unity i.e. the discharge in the sampling capacitance must be small compared to the pixel discharge and C_1 should be small compared to C_{pix}.

2. The signal due to charge injection will add non-linearity and an offset to the output signal, which must be acceptable.

3. The $\frac{kT}{C}$ noise introduced as the pixel and sampling capacitances are isolated twice must be small compared to the reset noise introduced as the pixel is reset. This will be true if the pixel capacitance is significantly larger than the gate capacitance of the pass transistor, M_4.

This method of operation is experimentally evaluated in Chapter 7.

2.7 A comparison of selected pixels

In this section, promising pixel architectures are analysed for size, achievable voltage swing, saturation charge and fill-factor. A number of assumptions are made to simplify the analysis:

- The supply voltage is $3.5V$ and the maximum threshold voltage is $1V$.
- Size is determined using a technique developed from that presented in [20]. Initially, the area consumed by interconnect is considered. It is assumed that up to two signals can be routed along each pixel edge. If one signal is routed along a pixel edge a minimum wire width and half a minimum spacing is subtracted from the pixel pitch. If a second track is required, a further half minimum spacing is subtracted. The two adjusted pixel pitches

are multiplied together to calculate the area available for the pixel components. A second step accounts for the number of contacts and transistors contained within the pixel. In order to simplify the calculation, an area equivalent to a minimum contact is subtracted from the available area for each contact, transistor and space required in the minimum cell layout. The remaining area is available for the diode.

- The fill-factor is simply the ratio of the diode area to total pixel area, which is expressed as a percentage.
- There are no substrate contacts within the pixel array.
- In order to calculate the saturation charge capacity, the capacitance value must be calculated when reset and when discharged to the lower limit. It is assumed that the pixel capacitance is dominated by the non-linear diffusion capacitance, which has a value, C_{pix}, given by [79]

$$C_{pix} = \frac{AC_{pix0}}{(1 - \frac{V}{\phi_0})} \tag{2.37}$$

where A is the area calculated in the fill-factor calculation; C_{pix0} is the zero-bias capacitance *per* unit area; V is the applied voltage and ϕ_0 is the built-in junction potential. The saturation charge is found by calculating the difference between the charge stored on the pixel capacitance in the reset and discharged states.

The results of these calculations are shown in Table 2.1 and analysed in the remainder of this chapter. After the theoretical analysis of CMOS pixels, three commercially available imaging technologies are compared from manufacturer's data.

2.7.1 Pixel size

Unsurprisingly, the simplicity of the passive pixel results in the largest fill-factor for the selected pixels. At the example pitch of $10\mu m$, the diode is 50% larger than for the active pixel. If an overflow drain transistor is included, this advantage is halved. The capacitive pixels by Ihara and one-transistor pixel by Oba achieve a similar fill-factor to the passive pixel with overflow drain. Two pixels with a significantly smaller fill-factor are the JPL photogate pixel and shuttered pixel; both achieve less than 30% at a $10\mu m$ pitch. Figure 2.38 shows the variation in fill-factor with pixel pitch. An important observation is that the fill-factor advantage is most

Pixel Type	Min Pitch	Voltage Swing	Sat Charge	fill-factor
Passive	$4.25\mu m$	2.3V	$378ke^-$	62%
Overflow Drain	$5.5\mu m$	2.3V	$326ke^-$	53%
Active	$6.5\mu m$	1V	$94ke^-$	41%
$b(t)$	$7.25\mu m$	1V	$79ke^-$	35%
JPL	$7.5\mu m$	1V	$65ke^-$	29%
Dynamic Mirror	$7\mu m$	1.3V	$143ke^-$	42%
Charge Share	$6\mu m$	1V	$113ke^-$	50%
Oba 2T	$6.25\mu m$	0.5V	$83ke^-$	44%
Ihara	$5.75\mu m$	0.5V	$97ke^-$	51%
Oba 1T	$5.75\mu m$	0.5V	$97ke^-$	51%
Shutter	$8\mu m$	1V	$60ke^-$	26%
No Vdd	$6.5\mu m$	1V	$101ke^-$	44%
Multiplexed	$6.5\mu m$	1V	$93ke^-$	41%

Table 2.1: *A comparison of pixel characteristics on a* $0.5\mu m$ *process; pixel-pitch is* $10\mu m$.

significant for small pixel pitches. For example, at a $7\mu m$ pitch, the passive and active pixels achieve fill-factors of 46.4% and 13.8%, respectively.

2.7.2 Pixel-output voltage swing

Further to obtaining the highest fill-factor, the simplicity of the passive pixel results in the largest achievable voltage swing, which is over twice that achieved by the various active pixel configurations. A notably poor voltage swing is achieved by the capacitive pixels because the pixel reset voltage must not turn on the in-pixel source follower.

2.7.3 Noise

In Section 2.3, noise sources due to $\frac{kT}{C}$ noise during pixel reset and diode shot noise have been discussed. This Section presents the noise contribution from pixel transistors due to $\frac{1}{f}$ and thermal noise and calculates the maximum achievable signal-to-noise ratio for a given pixel. Noise figures are calculated using the formulae given in Appendix B given the following assumptions:

- The array size under consideration has 1000 rows. This is used to define the minimum column current and minimum system bandwidth.

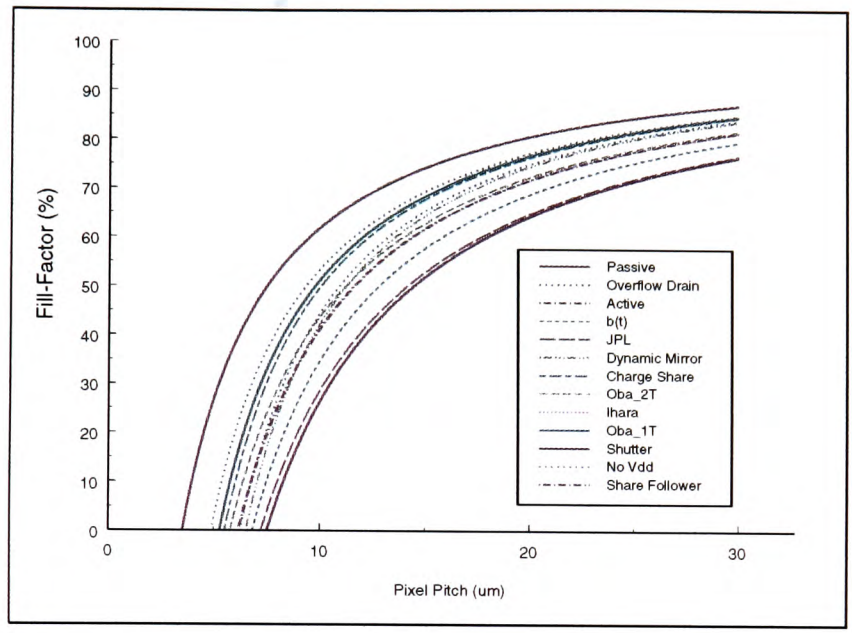


Figure 2.38: *The variation of fill-factor for selected pixels with pixel pitch.*

- True correlated-double sampling is assumed to cancel both $\frac{1}{f}$ noise and $\frac{kT}{C}$ noise. See Appendix D for a discussion on the validity of these assumptions.
- Correlated-double sampling is assumed to increase the thermal noise contribution by a factor of $\sqrt{2}$.
- If the reset samples are not correlated, the reset noise contribution is $\sqrt{2 \times \frac{kT}{C}}$.
- A channel length of $1\mu m$ is assumed for transistors within the pixel and $5\mu m$ for the column current bias transistor.
- The light level is sufficient to fully discharge a pixel. If this is not the case, there is no advantage of increasing the pixel saturation charge.

The results of the calculations are presented in Table 2.2 for transistors commonly found within pixels. Note that the Reset transistor is not included in this table because during readout it does not conduct current. The results presented in table 2.2 show that the noise contribution from individual transistors are an order-of-magnitude less than that from the sum of shot noise

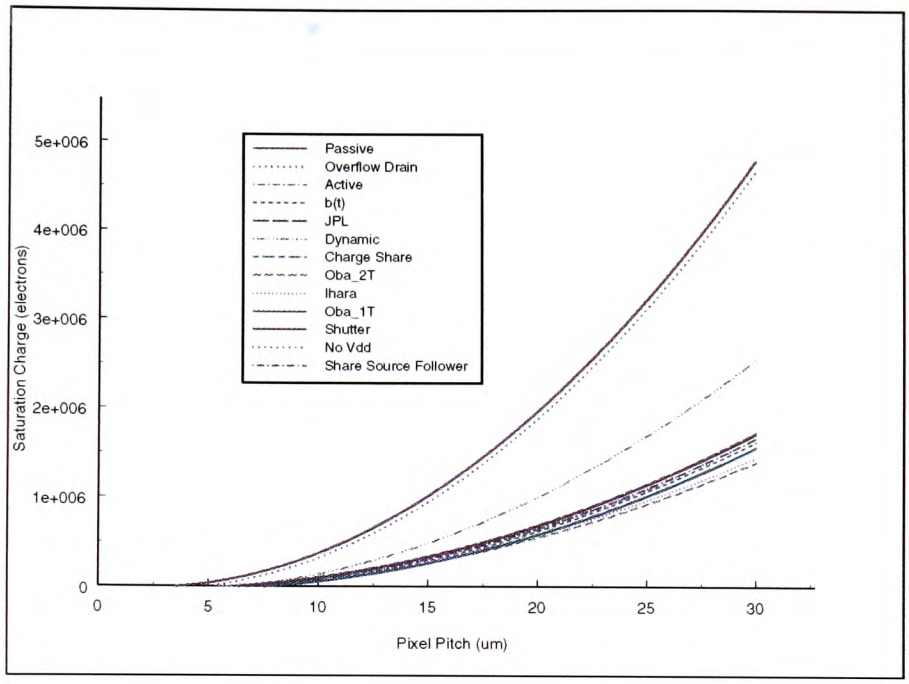


Figure 2.39: *The variation in the saturation charge of selected pixels with pixel pitch.*

and pixel reset noise. Consequently, pixel architecture is not critical in determining the system noise floor.

The total pixel referred noise is shown in Table 2.3 for three pixel configurations. Namely, the passive, active and shuttered pixel. Note that, in order to cancel fixed-pattern noise, it is assumed that correlated-double sampling must be performed on a standard active or shuttered pixel. Further, there are no offsets on a simple passive pixel, therefore, correlated-double sampling is not performed. In order to calculate the achievable resolution for the calculated pixel referred noise, a full-well capacity must be assumed. For an average pixel capacitance of 20fF and a maximum voltage swing of 1V, the full-well capacity is 125k electrons. The achievable resolution for an active pixel is limited to 10-bits with true correlated-double sampling but only 8-bits if the reset values are not correlated. Despite a relative large random noise charge, the large saturation charge of the passive pixel results in the best signal-to-noise ratio, equivalent to 11-bit resolution.

Transistor	Noise Type	rms noise (e^-)
Source Follower	Thermal	3.46
Source Follower	Flicker	3.71
Read	Thermal	0.01
Read	Flicker	0.16
Column Bias	Thermal	3.87
Column Bias	Flicker	0.33
Shutter	Thermal	0.51
Shutter	Flicker	3.25
Pixel	$\frac{kT}{C}$	56.93
Pixel	Shot	13.33

Table 2.2: *Noise sources for selected pixel transistors.*

Pixel	With True CDS	With Standard CDS	No CDS
Active	28.9	108.6	NA
Passive	NA	NA	74.0
Shuttered	34.2	113.9	NA

Table 2.3: *Total input-referred noise for three pixel architectures.*

2.7.4 Summary of pixel comparison

The simplicity of the passive pixel yields the largest fill-factor and achievable voltage swing, which when combined results in the largest saturation charge. Since noise is comparable for the discussed pixel architectures, the large saturation charge results in the best signal-to-noise ratio. Therefore, the passive pixel is the most attractive pixel architecture. The performance of the standard active pixel is sufficient for viewed images. Variations on the passive pixel can also be considered provided that the extra transistors do not introduce fixed-pattern noise. Of the pixels listed in Table 2.1, the capacitive pixels and the dynamic-mirror pixel are unsuitable for viewed image sensors because of the poor voltage swing and introduced fixed-pattern noise, respectively.

2.7.5 A comparison of Texas Instrument's imaging technologies

Table 2.4 shows a comparison of three imaging technologies: a CCD-, CMD- and CMOS-based sensor. In comparison to the other technologies, CMOS suffers from a low fill-factor and, consequently, a poor quantum efficiency. However, of more consequence is the relatively high noise-equivalent illumination and dark signal, which combine to limit the performance of

	TC236 CCD	TC286 CMD	TC288 APS
Format (pixels)	640 × 480	640 × 480	640 × 480
Pixel size (μm^2)	7.4 × 7.4	7.4 × 7.4	7.4 × 7.4
Chip area (mm^2)	42.5	33	33
Fill factor (%)	74	64	27
Quantum efficiency (%)	52	45	19
Sensitivity ($\frac{mV}{lux}$)	41	78	22
Noise floor (mV)	0.2	0.6	1
Noise-equivalent illumination	$4.9mlux$	$7.7mlux$	$45mlux$
Dynamic range (dB)	64	62	60
Dark signal at $50°C$(mV)	0.67	1.5	10
Sensor power supplies (V)	10,8,2,−10	5,8	3.3
Sensor power consumption	60mW	$150mW$	$110mW$
Required peripheral circuits	Timer, driver, CDS, AGC [1], ADC	Timer, driver, AGC, ADC	Timer, ADC
Total system power (mW)	800	400	270

Table 2.4: *A comparison of Texas Instrument's imager technology.*

the CMOS sensor at low-light levels. To the advantage of the CMOS sensor, the high level of integration leads to a factor-of-three reduction in system power over the CCD sensor. However, it is important to note that the sensor chip power consumption is twice that of the CCD sensor chip. The increase in sensor power dissipation may become unacceptable at larger array sizes, eroding the system-power advantage of the CMOS sensor.

The CMD technology offers a significant power advantage over the CCD sensor. However, the noise performance is inferior to the CCD sensor and it does not offer the ability to integrate signal-processing with the sensor array. Consequently, it is not discussed further.

2.8 Conclusions

After a review of the operation of a generic CMOS pixel, a comprehensive review of CMOS pixel architectures was presented. Promising pixel configurations were compared for signal-to-noise ratio, fill-factor and voltage swing. Due to the simplicity of the passive pixel, it achieved the best performance in all the above categories. The active pixel was also identified as a promising pixel architecture, its main disadvantage being the limited voltage swing.

Two novel pixel architectures, designed to increase the fill-factor of a standard active pixel,

were presented. In addition, a mode of operation to suppress reset noise for the shuttered pixel was suggested. This, along with the multiplexed pixel, will be evaluated on the test chip *Ginger Dancer*, which is presented in Chapter 7.

The analysis highlighted the three factors that limit the imaging performance of CMOS imagers:

1. **reset noise**, which can be suppressed by correlated double sampling.
2. **dark current**, which is process dependent and is the dominant issue in the possible move away from the standard CMOS process.
3. **fixed-pattern noise**, which must be suppressed below 0.1% for viewed images and, hence, led to a number of pixel architectures being disregarded.

Chapter 3
The CMOS imager: readout

3.1 Overview

In Section 1.2, it was stated that one of the advantages of a CMOS-based imager over a CCD-imaging system, is that it is possible to integrate signal-processing on a CMOS imager chip. Consequently, CMOS imager readout circuitry can vary greatly. This contrasts with the CCD sensor, where CCD charge transfer readout with a single source-follower is integrated on the sensor chip. This chapter identifies the different readout methods and analyses the limiting factors in their operation.

Initially, a generic readout structure is presented. The design issues relating to voltage- and charge-sensing readout are discussed. Finally, examples of integrated signal processing are given.

3.2 The function of readout circuitry

Figure 3.1 shows a generalised readout structure for a $n \times n$ imaging array. It comprises two distinct parts, a column structure, which is shared between m pixel columns and circuitry, such as the output amplifier, which is common to the entire array. The application determines the proportion of processing that is carried out in the column, rather than serially after the common bus. For example, as discussed in Chapter 6, analogue-to-digital conversion can be performed either by a serial converter or in a semi-parallel approach at each column.

Functions that are often integrated in the column are multiplexing, if a column structure is shared between more than one pixel column, amplification and some signal processing, for example, to cancel pixel-to-pixel fixed-pattern noise. The common readout structure, typically, includes a pad driver and some signal processing, for example, to format a video signal or cancel column-to-column fixed-pattern noise. The pixel architecture determines the column structure, two generic cases are considered, charge- and voltage-sensing. The review of pixel

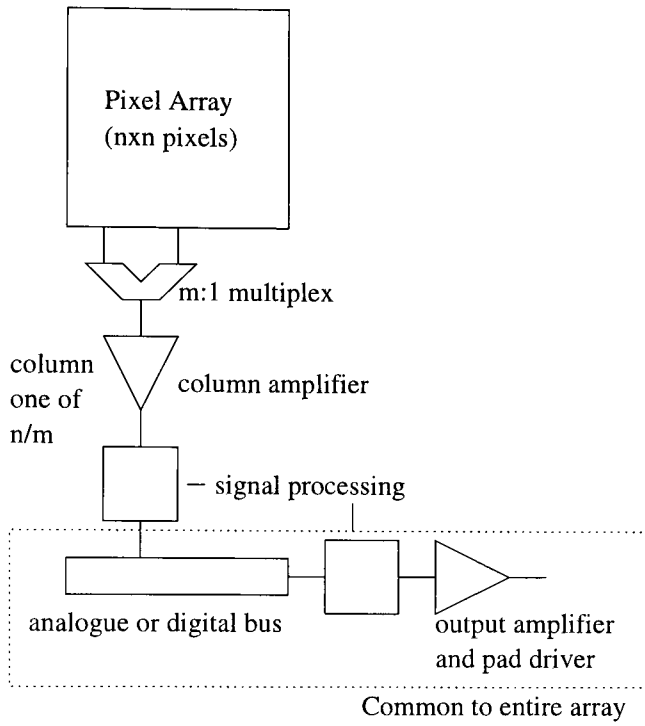


Figure 3.1: *A generic readout architecture.*

structures in the preceding chapter did not include a feasible current-output pixel, therefore, current-sensing output structures are not considered further than referring the reader to a text on current-mode design [80]. However, the comments on fixed-pattern noise are applicable to such readout structures. The elements that comprise a generic readout structure are discussed in the following sections, after general comments on column-to-column fixed-pattern noise have been presented.

3.3 Fixed-pattern noise

Where there are parallel signal paths, for example, in the columns, the readout circuitry can contribute fixed-pattern noise. The most significant sources of fixed-pattern noise are caused by variations in the amplifier input offset and gain. How these non-idealities effect the overall imager performance depends on whether the amplifier is used in a feedback configuration. Each case is discussed in the following sections.

3.3.1 Non-feedback configuration

It is unlikely that an amplifier will be used in an open-loop architecture because the maximum gain is severely limited if clipping is to be avoided. Further, the gain must be well controlled to avoid the introduction of fixed-pattern noise. The one example, where open loop amplifiers are common, is for the input stage to an analogue-to-digital converter. In this case, the amplifier offset adds directly to the input signal and, after suppression, must be less than the desired converter resolution. Two methods exist for suppressing such fixed-pattern noise:

1. input- or output-offset cancelling, which is discussed in Section 6.4.1. These methods use feedback around the amplifier and store the offset on capacitors at the amplifier input or output.

2. correlated-double sampling, which is discussed in Appendix D. In this method, a reference, which is sensed every cycle, is subtracted from the signal. Traditionally, this is performed in the analogue domain, however, it can be easily performed in the digital domain after a semi-parallel analogue-to-digital converter.

Unlike amplifier offsets, gain mismatch is not easy to cancel. Variation in gain results in image striping caused by bright and dark columns.

3.3.2 In feedback

3.3.2.1 Gain variation

In a feedback configuration, the output voltage error is inversely proportional to the amplifier gain-bandwidth product [56]. Therefore, fixed-pattern noise can be introduced due to variation in the column amplifier gain-bandwidth product. In order to suppress column-to-column fixed-pattern noise, the minimum gain-bandwidth product must be sufficient to suppress the error below the desired noise floor.

3.3.2.2 Amplifier offset

The offset voltage is unaffected by the feedback circuit, therefore, the methods discussed in Section 3.3.1 should be used to suppress the input offset.

3.4 Charge-sensing readout structures

Figure 3.2 shows a typical charge-sensing amplifier configuration. The pixel charge is integrated on the feedback capacitor, C_f in Figure 3.2, to produce an output voltage. Since the feedback capacitance determines the gain of the charge-to-voltage conversion, its value must be limited to avoid clipping. In practice, the value of integration capacitance is often chosen to be equal to the pixel capacitance.

3.4.1 Noise performance

A study by Sansen has shown that the input-transistor size is critical in determining the amplifier noise performance for capacitive sensor amplifiers [81]. A similar derivation is presented next, with different assumptions more suitable for a passive-pixel image sensor.

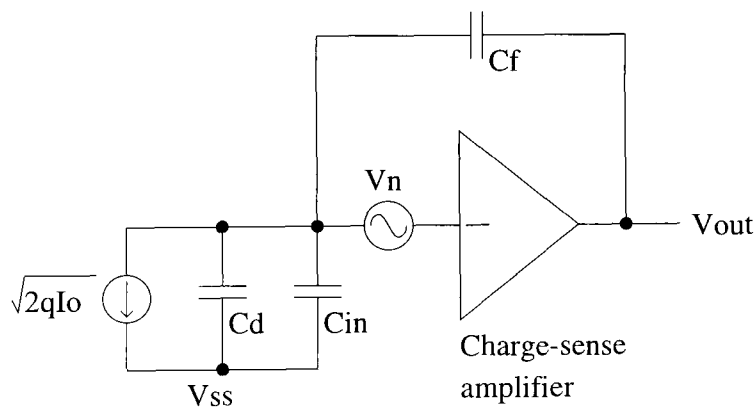


Figure 3.2: *A schematic showing the parasitic capacitances and noise sources used to calculate the pixel-referred noise due to the amplifier input-noise voltage. C_f, C_{in} and C_d represent the feedback, amplifier-input and summed-column-and-pixel capacitances, respectively. V_n is the amplifier input-referred noise voltage and $\sqrt{2qI_o}$ is the pixel shot current.*

For the following analysis it is assumed that the noise performance is dominated by the input device and that the bandwidth is independent of the input device transconductance. The first assumption holds for good analogue circuit design. However, the second assumption is not obviously true because the bandwidth of an amplifier is often proportional to the transconductance of the input transistor. If the amplifier is designed so that it provides just sufficient bandwidth for the application, *i.e.* it is not over-engineered, this assumption is valid.

The gate-referred noise voltage for the input transistor is given by

$$\bar{v}_n^2 = \frac{8kT}{3} \times \frac{1}{g_m} + \frac{K_f}{C_{ox}^2 WLf} \tag{3.1}$$

At the amplifier output, the noise voltage, $\bar{v}_{out}^2$, is given by

$$\bar{v}_{out}^2(f) = \left| \frac{C_d + C_f + C_{in}}{C_f} \right|^2 \bar{v}_n^2 \tag{3.2}$$

In order to calculate the equivalent noise charge, the output noise voltage must be divided by the signal at the amplifier output due to a single electron, $v_{e-} = \frac{q}{C_f}$. Further, to optimise the noise figure, the amplifier input capacitance, C_{in}, must be expressed in terms of the input transistor dimensions:

$$C_{in} = C_{GS} + C_{GD} = \frac{2}{3} C_{ox} WL + C_{ox} WL_D \tag{3.3}$$

After substitution the pixel referred noise charge, $\bar{q}_{pix}$, is given by

$$\bar{q}_{pix}^2(f) = \left| \frac{C_d + C_f + WC_{ox}(\frac{2}{3}L + L_D)}{q} \right|^2 \times \left[\frac{8kT}{3\mu C_{ox} \frac{W}{L} \Delta V_{GS}} + \frac{K_f}{C_{ox}^2 WLf} \right] \tag{3.4}$$

A number of further assumptions are made to determine the maximum achievable signal-to-noise ratio:

1. The transistor length is set to be $2\mu m$ which is a compromise between ease of layout within a column pitch and transistor output resistance.

2. The transistor gate-source voltage is fixed at $0.15V$ to bias the transistor on the edge of the subthreshold region, where the noise performance *per* unit current is optimized [56].

If Equation 3.4 is differentiated with respect to the input transistor width, W, and used to minimise the thermal and $\frac{1}{f}$ noise contribution separately, the optimum input transistor width, W_{opt}, is given by

$$W_{opt} = 3 \frac{C_d + C_f}{C_{ox}(2L + 3L_D)} \tag{3.5}$$

for both thermal and $\frac{1}{f}$ noise. Consideration of Figure 3.3 shows that, while the optimum transistor width is $692\mu m$, more practical widths can be chosen for a small noise penalty, for

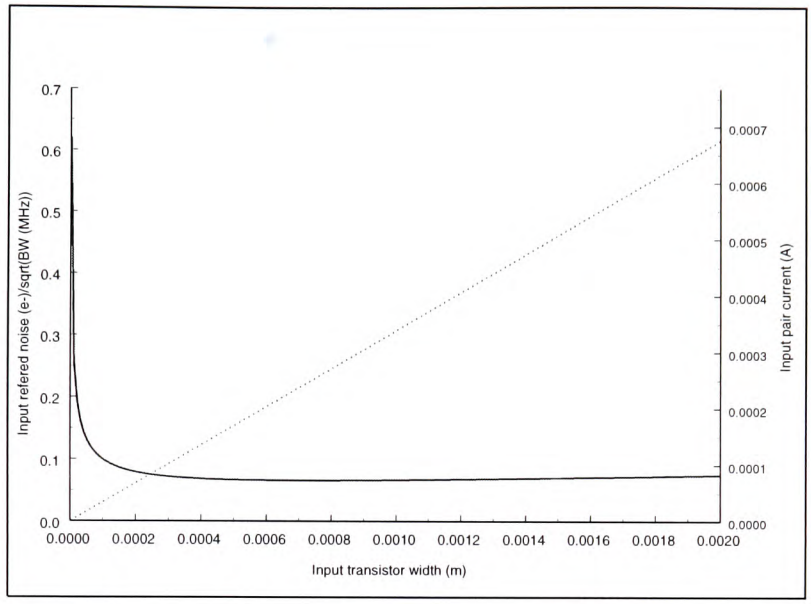


Figure 3.3: *The variation with input transistor width of pixel-referred noise and bias current for an integrating amplifier.*

example, a gate width of $200\mu m$ increases the noise figure by 20% and $100\mu m$ by 50% over the minimum. In order to determine the achievable signal-to-noise ratio, the amplifier bandwidth must be calculated. Figure 3.4 shows the results of this calculation assuming that:

1. In order to achieve a given signal-to-noise performance, which for ease of reference is converted to bits, the amplifier thermal noise can contribute $\frac{1}{4}$-LSB of noise.
2. The amplifier is single-ended. If a differential amplifier is used, the input transistor width must be increased by a factor of $\sqrt{2}$ to achieve the same noise performance.
3. The required bandwidth is calculated using the techniques presented in Section 6.4.
4. The pixel full-well capacity is calculated assuming a $1V$ pixel discharge and a $20fF$ pixel capacitance *i.e.* a saturation charge of 125k electrons.

Figure 3.4 shows that as the pixel array size is increased, the input transistor width must be increased to achieve the same level of performance. At array sizes of 100×100 pixels, the amplifier thermal noise will not limit performance provided that the input transistor width is

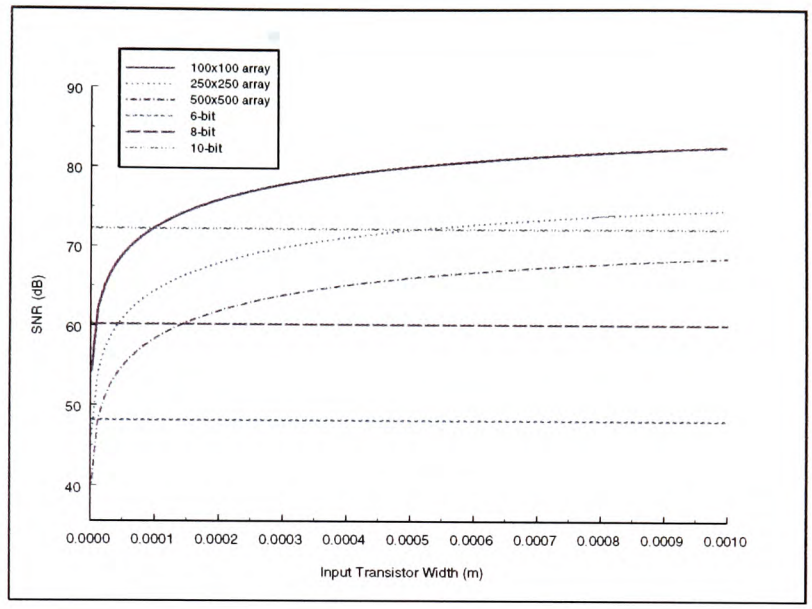


Figure 3.4: *The variation of signal-to-noise ratio with input transistor width for three passive-pixel array sizes:* 100×100, 250×250 *and* 500×500 *pixels.*

greater than $100\mu m$. In contrast, a 500×500 pixel array performance is limited to 8-bit by the amplifier thermal noise contribution. Further, this level of performance is only achieved for an input transistor width of $150\mu m$ for single-ended or $300\mu m$ for differential configurations. Summarising, the passive pixel sensor is most attractive for small array sizes below 250×250 pixels and low-resolution sensors — 6-bit performance can be achieved easily at the array sizes under consideration.

3.5 Voltage-sensing readout structures

A simple voltage-mode readout structure is shown in Figure 3.5 and the associated timing diagram in Figure 3.6. The following description of operation is based on that by Nixon [29]. Each column amplifier comprises a load transistor, M_1, and two branches to store the reset and signal levels. A branch consists of a sample-and-hold circuit, M_3-C_S and M_2-C_R, and a second source-follower transistor, M_7 and M_8, with a column select transistor, M_9 and M_{10}. The load transistors of the second set of source followers, M_{11} and M_{12}, and the subsequent clamp circuits and output source followers are common to the entire array.

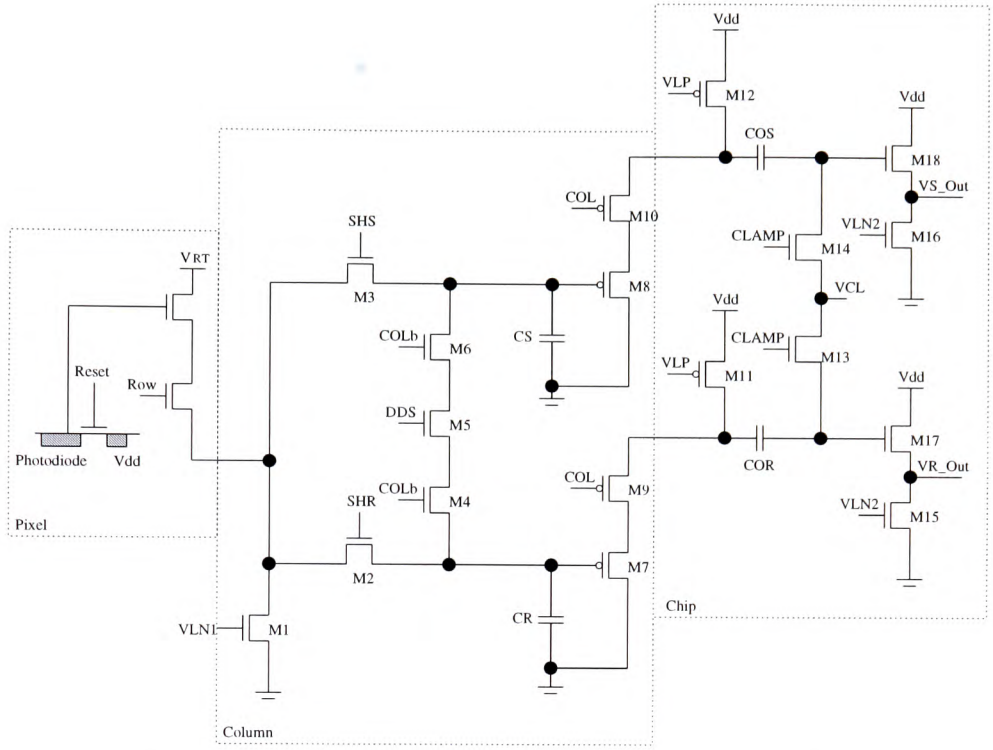


Figure 3.5: *A voltage-mode readout scheme after Nixon[29].*

Operation is as follows, at the end of the integration period, the row is selected and the signal that is present on each column is sampled (SHS) onto the capacitor, C_S. Next, the pixel is reset and the new column level is sampled (SHR) onto the capacitor, C_R. Unfortunately, the column output contains offsets due to threshold voltage variation in the in-pixel and column source-follower transistors. Experimentally, Nixon found this variation to be, typically, 20mV [29], which would limit the achievable resolution to 5-bits. Consequently, it is necessary to suppress this noise. Nixon uses a form of correlated-double sampling, which he names double-delta sampling to eliminate the introduced fixed-pattern noise [29].

Column readout is as follows, first a column is selected (COL). After a settling time, CLAMP is removed and the DDS switch M_5 and two column select switches, M_4 and M_6, are used to short the two sample and hold capacitors. The result is a difference voltage coupled to the output drivers that is free of the voltage threshold component. Prior to CLAMP being deactivated, the output signals are given by

$$VR_{out} = \gamma(V_{CL} - V_{tr}) \tag{3.6}$$

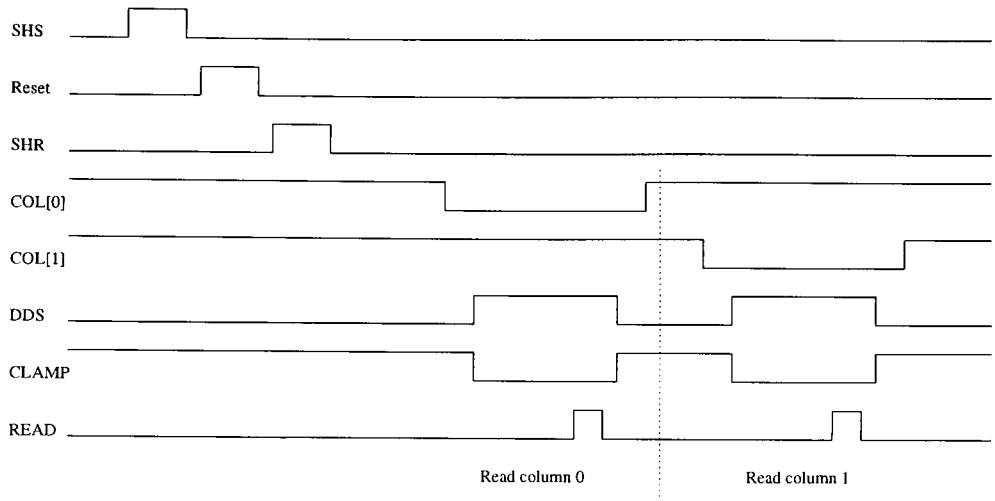


Figure 3.6: *The timing diagram for the voltage-mode readout scheme shown in Figure3.5.*

$$VS_{out} = \gamma(V_{CL} - V_{ts}) \tag{3.7}$$

where γ is the voltage gain of the output followers, which is assumed to be equal and V_{tr} and V_{ts} are the threshold voltages of transistors M_{17} and M_{18} respectively. Deactivation of the clamp circuitry and activation of the DDS switch causes several changes. First, the voltages in the two column branches equalise, which in turn causes a change in V_{colS} and V_{colR}, which is coupled to the output. The result is the differential output voltage, V_{out}, is given by

$$V_{out} = VR_{out} - VS_{out} = \alpha\beta\gamma(V_{pr} - V_{ps} - V_c) \tag{3.8}$$

where V_{pr} is the pixel reset voltage; V_{ps} is the pixel signal voltage and V_c is a constant voltage that is common to the entire array. Therefore, to first order, fixed-pattern noise has been suppressed. However, differences in source follower gain will contribute some fixed-pattern noise.

In a mixed-signal environment, a differential output amplifier is often used to improve the power-supply-rejection ratio. Operation is similar to that described above, however, in this case, parallel columns signal paths are not needed; the differential amplifier is used to subtract the reset value from the signal value [74].

3.5.1 Noise performance of the voltage-sensing readout circuit

In this section, the readout circuitry described in the previous section is analysed for noise performance. In order to perform the calculations, a number of assumptions must be made:

1. A column current is assumed to be the minimum required for a 1000×1000 pixel image sensor.
2. Transistor sizes are chosen to be typical for an image sensor.
3. The sampling capacitors are assumed to be 2pF.

Transistor	Noise Type	rms noise (μV)
M_7, M_8, M_{11}, M_{12}	Thermal	10.96
M_7, M_8, M_{11}, M_{12}	Flicker	0.73
M_9, M_{10}	Thermal	36.23
M_9, M_{10}	Flicker	2.92
M_{15}, M_{16}, M_{17}, M_{18}	Thermal	9.78
M_{15}, M_{16}, M_{17}, M_{18}	0.84	
Sampling capacitors	$\frac{kT}{C}$	45.91
Total		163.7

Table 3.1: *Noise sources for the voltage-sensing output scheme shown in Figure 3.5.*

If a 1V swing is assumed at the pixel output, the noise voltage given in Table 3.1, corresponds to an achievable resolution of 12-bits. Therefore, the pixel structure, limits the noise performance of a voltage-sensing sensor scheme.

3.6 Signal processing

All CMOS image sensors have column amplifiers and address circuitry integrated with the pixel array. Many include further functionality and are genuinely a complete system on a chip. The next two sections briefly discuss two classes of integration. The first class is the so-called camera-on-a-chip, the second are examples of chips that process the image to provide extra functionality.

3.6.1 Camera-on-a-chip

Complete single-chip camera systems have been available since the mid-eighties. Over the last decade, the pixel array size has been increased from a typical 128×128 pixels to array sizes up to 1300×1000 pixels [27]. In 1998, Smith reported a single-chip NTSC video camera, which required six terminating resistors, eleven decoupling capacitors and a crystal for operation. On-chip signal processing performed autoblack calibration and automatic exposure control to optimise camera performance [60]. A year earlier, Hurwitz presented a sensor to be integrated in a digital camera along with memory elements, which provided a frame-store to suppress dark current [78].

Other single-chip cameras include a digital camera by Kawahito, which included an analogue domain 2-dimensional discrete cosine transformation to relax the bandwidth requirements on the analogue-to-digital converter [82]. Perhaps the most ambitious project, that aimed to maximize the advantages of CMOS-based image sensing, was the Microintegrated Intelligent Optical Sensor Systems (MInOSS) project [83], which provided libraries of photodiode arrays, charge amplifiers and on-chip analogue-to-digital converters so that custom single-chip cameras could easily be designed.

Such integrated camera systems result in large chips, which are prone to cross-coupling [23]. For example, in the 1998 chip by Smith, the 25k digital gates, 14k bits of SRAM memory and 400k analogue transistors caused image degradation due to coupling and an increase in the thermally generated dark-current, which was caused by the elevated operating temperature.

3.6.2 Increased functionality

Many machine vision and robotic applications require simple, inexpensive cameras capable of fast operation and on-board processing with little emphasis on colour or high-resolution [84]. Such applications often process extracted information, rather than images, hence, making them suitable for focal-plane integration [68].

Examples of recent products that integrated substantial functionality with a CMOS sensor include:

- A fingerprint verification sensor [85], which has been developed to implement a password system for Compaq computers.

- An optical mouse [86].
- A pointing device that tracks a pattern on a rollerball [87].
- A helicopter oil-debris monitoring device [88].
- A dental probe that integrated x-ray event detection circuitry on an acitve-pixel sensor array [16].
- A device to monitor the azimuth, elevation and intensity of the sun [89].
- A star tracker, which utilised region-of-interest integration times to allow the tracking of relatively dim stars [90].

The common characteristics of these sensors is that they have small pixel arrays, which produce low-resolution images and are, therefore, ideal for integration on a CMOS image sensor. A further feature of many of these applications is that the light intensity can be well controlled so that the poor low-light performance of CMOS sensors is not an issue.

3.7 Multiplexing

In order to increase the effective pixel pitch and, hence, ease the layout of the column amplifier, two techniques can be used. Firstly, adjacent column amplifiers can be placed at alternate ends of the pixel array. Whether this introduces fixed-pattern noise will depend on the amplifier type. For example, increased gain variation would increase the fixed-pattern noise in the case of a source follower amplifier and increased variation in the integration capacitance would increase the fixed-pattern noise introduced by charge-sensing amplifier. The alternative is to multiplex the amplifiers [64], which, unless the amplifier is slew-rate limited, will cause an increase in power consumption. Both these techniques tend to increase the introduced fixed-pattern noise, which must be controlled to within acceptable levels. Experimentation is needed to determine the increase in fixed-pattern noise and whether the increase in pixel pitch allows a significant improvement in analogue performance due to improved matching and the possibility of increasing the length and, hence, output resistance of transistors.

3.8 Conclusions

In the previous chapter, the passive pixel was shown to provide superior noise performance over an active pixel sensor. However, this chapter has shown that the readout mechanism limits performance for medium and large array sizes. Conversely, the readout structure of an active pixel sensor does not limit the achievable noise performance. In conclusion passive pixel sensors are preferable for small to medium sized pixel arrays and active pixels for larger array sizes.

A number of examples of integrated signal processing were given in this chapter. It was concluded that the CMOS imagers provide a significant advantage over a CCD imaging system for small array sizes where the required signal processing can be easily integrated on-chip.

Chapter 4
The CCD camera

4.1 Overview

The CMOS camera is an alternative technology to the present solid-state imaging technology of choice: the CCD-based image sensor. Consequently, to successfully evaluate the potential of CMOS-based imagers a basic understanding of CCD technology, and future development, is required. An additional benefit of this study is that it may highlight possible improvements to CMOS imaging devices.

This chapter briefly describes the operation of a CCD device, for a more detailed analysis refer to a dedicated text, for example, Hobson [4]. Discussion highlights the differences between the two imaging technologies and considers the relative merits.

4.2 CCD image sensor topologies

A CCD sensor chip comprises photosensitive elements, horizontal and vertical transfer structures and an output amplifier. These can be arranged in one of the three planar imaging topologies, shown in Figure 4.1: line transfer, frame-transfer and interline-transfer. Both the line- and frame-transfer topologies use the photo-site cells for vertical transfer from the pixel to the common output bus CCD. Therefore, the images suffer from smearing due to additional charge collection during the vertical transfer. This sharing yields an advantage in minimum pixel pitch or increased fill-factor. In a still camera application, the use of a mechanical shutter would mitigate the image smearing effect, making a line- or frame-transfer CCD more attractive. However, for video applications, the interline-transfer CCD is the standard topology, which is discussed for the remainder of this chapter.

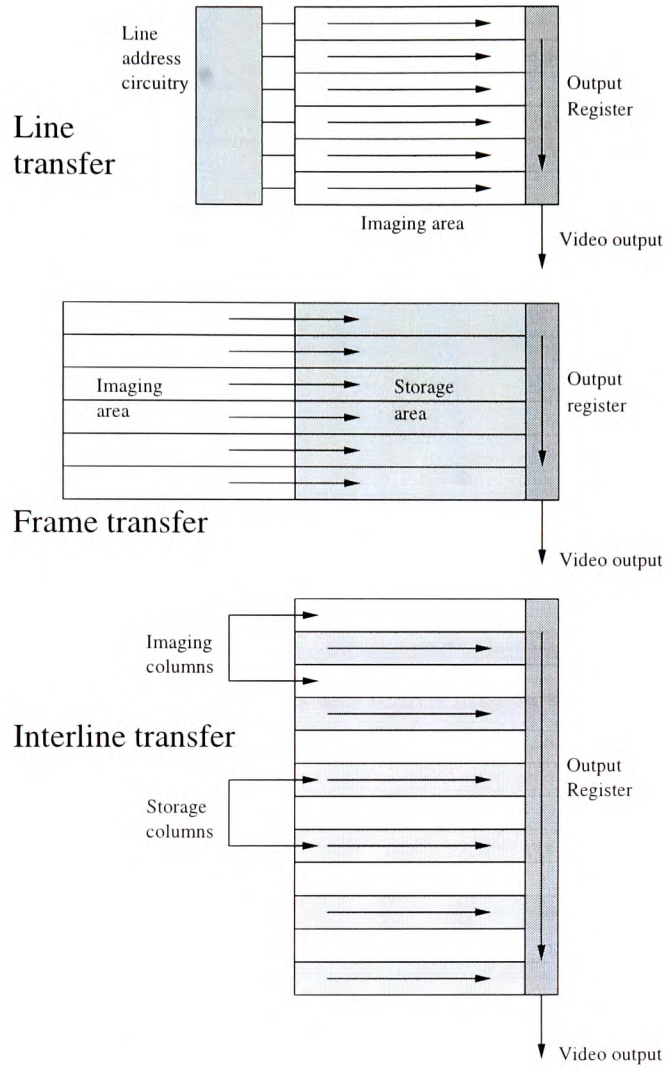


Figure 4.1: *Planar imaging topologies.*

4.3 The interline-transfer CCD image sensor

A schematic diagram of an interline-transfer CCD (IT-CCD) image sensor is shown in Figure 4.2. The sensor comprises an imaging area, a horizontal transfer CCD (HCCD) and an output amplifier. In the imaging area, a unit cell contains a p-n junction photodiode and a vertical transfer CCD (VCCD) cell.

Unlike the CMOS image sensor, a CCD sensor must operate in an integration mode. Signal charge is stored in a potential well formed at the pixel site. At the end of the integration time, the signal charge is transferred to the vertical CCD, which is analogous to the column

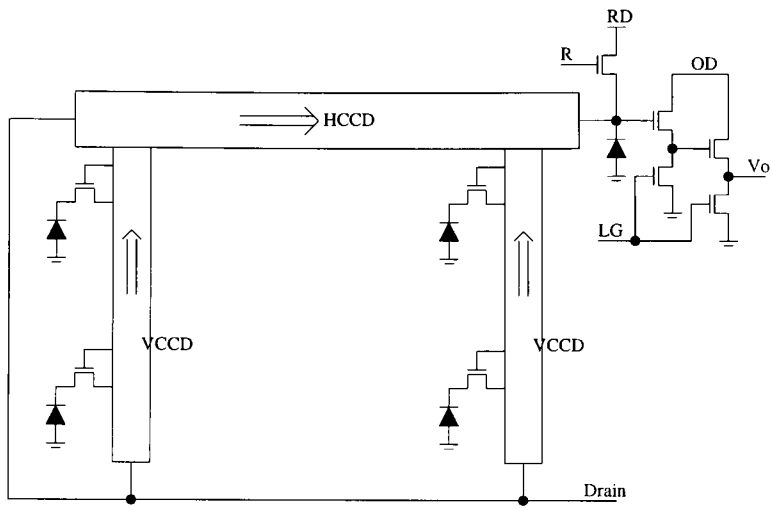


Figure 4.2: *The components of an inter-line transfer CCD image sensor.*

of a CMOS imager. A signal charge packet is transfered along the VCCD until it reaches the horizontal transfer CCD, which passes the charge until it reaches the charge-sensing node. The charge-sensing node is at the input of the on-chip amplifier, which buffers the signal off-chip.

4.4 Charge transfer: motivation

The charge transfer process is fundamental to the operation of a CCD imager. From the description in the previous section, a number of transfers can be identified:

- from the pixel to the vertical transfer CCD.
- between the elements of the VCCD.
- from the VCCD to the HCCD.
- between the elements of the HCCD.

All of these transfers must be optimized. However, the transfers along the horizontal and vertical CCD take place a maximum of n times in a $n \times n$ imager and are, therefore, most critical.

The proportion of the charge successfully transfered from one cell to the next is defined as the charge transfer efficiency, η, which has a value of 1 for a complete charge transfer and 0 if

no charge is transfered. After n transfers of efficiency η, the proportion of the original charge remaining, η_n, is given by

$$\eta_n = \eta^n \tag{4.1}$$

Equation 4.1 shows the exponential relationship between overall charge-transfer efficiency and the number of transfers; this imposes a strict limit on the required individual charge-transfer efficiency. The number of electrons lost during charge transfer is a source of noise because the

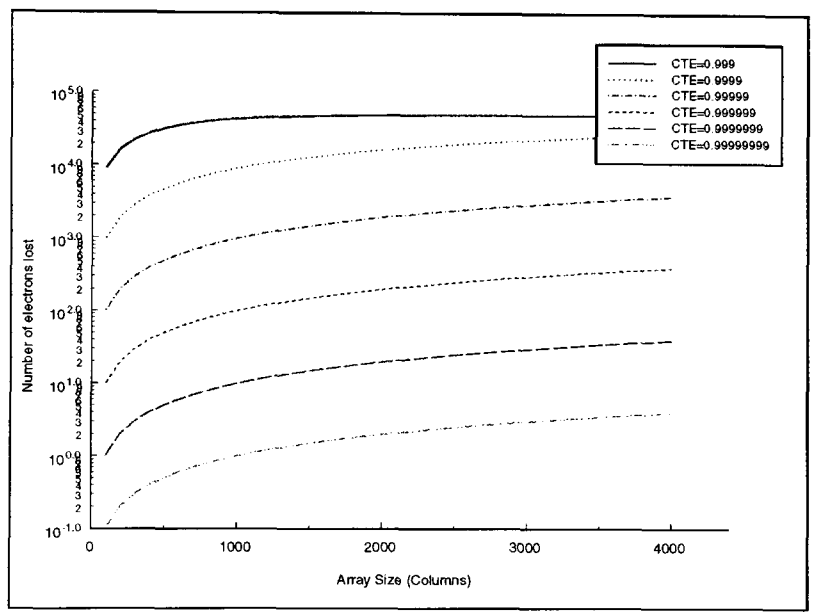


Figure 4.3: *The maximum number of electrons lost through charge-transfer for an $n \times n$ imager with a given charge-transfer efficiency.*

capture process is random and the number of transfers that a charge packet undergoes before reaching the output amplifier is not constant. For example, a charge packet in the 1920×1035, CCD imager presented by Oda [91] undergoes between 10 and 3000 transfers depending on the pixel location. In order to achieve 10-bit resolution, for array sizes greater than 1000×1000, the charge-transfer efficiency should be 0.9999999. A charge-transfer efficiency of this order requires almost perfect silicon, therefore, the process costs are increased. Unfortunately, as array size is increased, the pixel readout frequency must be increased, which has an adverse effect on charge-transfer efficiency, which must meet more stringent conditions due to the increased number of transfers [45].

4.5 Charge transfer: theory

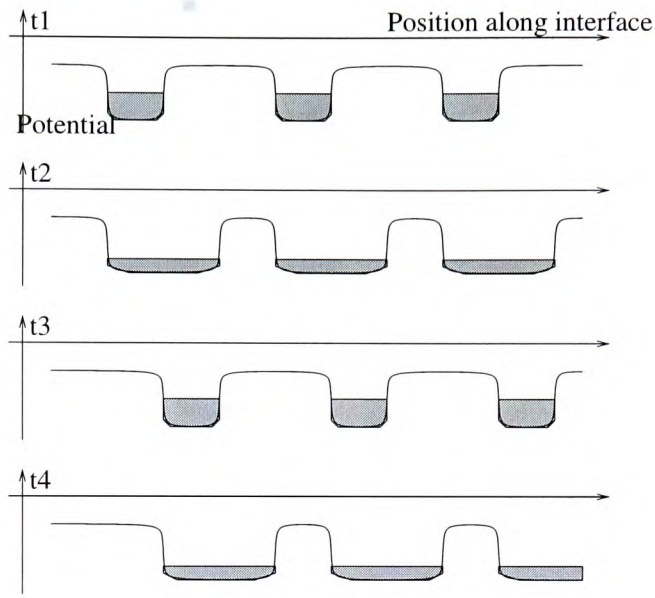


Figure 4.4: *The three-phase charge-transfer process.*

Charge transfer is achieved by modulating the potential of the bulk silicon using MOS gate electrodes. A series of potential wells are created, which act as a charge-store. A simple, ideal, three-phase, charge transfer is shown in Figure 4.4. Lateral charge-transfer is prevented using diffusion implants. Unfortunately, charge-transfer efficiency is limited by parasitic potential barriers and wells. For example, Figure 4.5 shows a potential barrier caused by an inter-electrode gap. When CCD imagers were proposed by Boyle and Smith in 1970, a brute force approach was used to remove the potential barriers: a 20V clock swing was needed to achieve a charge-transfer efficiency of 0.9998 [92]. Later, multilayer gate structures were introduced to reduce parasitic potential barriers, which led to a reduction in the required clock swing and an increase in the charge-transfer efficiency to 0.99999 [92]. A further advantage of the multilayer gate structure is that it yields routing benefits.

Image lag is the proportion of a pixel value that is composed of residual charge from previous pixel values. It is a function of the sensor charge-transfer efficiency. Figure 4.6, shows image lag as a function of transfer gate pulse amplitude for the sensor described by Kuriyama [30]. For the given sensor, the clock voltage must be greater than $10V$ to suppress image lag to acceptable levels.

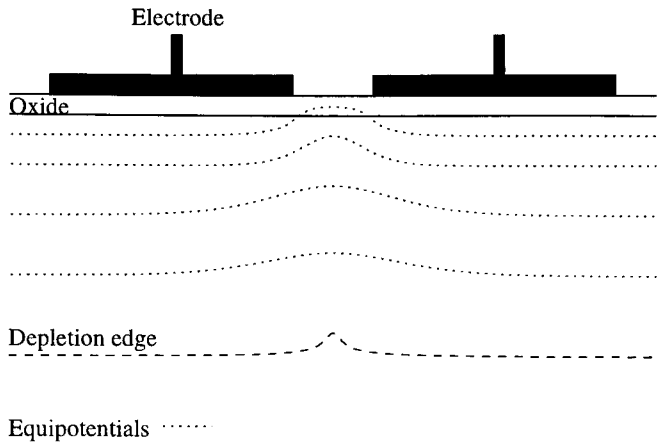


Figure 4.5: *Equipotentials showing the electric field distortion caused by the gap between neighbouring electrodes.*

If electrical fields were not present, thermal diffusion would transfer charge between neighbouring elements of a CCD. The charge-transfer efficiency, η is given by

$$\eta = 1 - be^{-\frac{t}{\tau}} \tag{4.2}$$

where b is a process defined constant and τ is a time-constant given by $\tau = \frac{L^2}{2.5D}$ where L is the centre-to-centre electrode spacing and D is the carrier diffusion constant. A majority of the charge moves quickly, the remainder transfers with an exponential time-constant. Fringing fields established between electrodes help to reduce the transfer time-constant and, hence, increase the maximum operation frequency for a given charge-transfer efficiency. The fringing fields are increased by reducing the gate-oxide capacitance or increasing the gate voltage and reduced by increasing the electrode-to-electrode spacing or dopant density.

Modern devices use a buried-channel CCD configuration to eliminate transfer noise caused by surface states. Furthermore, a buried channel, which is formed by epitaxial deposition onto, or diffusion into, a p-substrate, increases the charge-transfer efficiency by increasing the fringing fields [10].

In an interline-transfer CCD, the vertical CCD is integrated in a column of pixels, consequently, area is an important design parameter. Whereas area is not constrained in the vertical dimension for a horizontal CCD. Consequently, two parallel CCDs can be used to increase the permitted area in the horizontal direction and reduce the required operating frequency[91]. The crucial

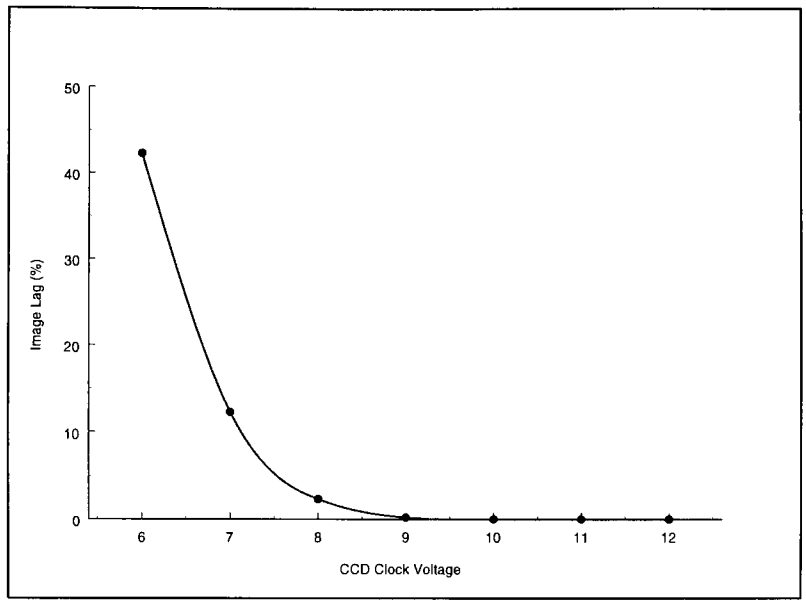


Figure 4.6: *Image lag as a function of the VCCD driving voltage [30].*

design parameter for the HCCD is operating frequency, which must be equal to the pixel rate, or half the pixel rate if a dual HCCD is used. This compares to the VCCD, which can operate at the line rate. Consequently, the vertical and horizontal CCDs should be optimized separately:

- The VCCD uses n^+ diffusion and shallow p^+-well structures to maximize the charge-handling capability *per* unit area. The relatively low operating frequency means that maximizing the charge-transfer efficiency is a secondary consideration.
- The HCCD uses a deep p^--well to strengthen fringing fields and, hence, improve the charge-transfer efficiency [93]. Area is practically unconstrained in the vertical direction, therefore, the high operating frequency requires the charge-transfer efficiency to be optimized.

4.5.1 The output amplifier

A CCD sensor uses a single charge-sensing amplifier to convert a charge packet to a voltage, which is subsequently driven off-chip. Figure 4.7 shows a typical CCD amplifier, which comprises a floating-sense node and a cascade of source followers. Operation is as follows:

1. The floating-diffusion node is reset to a known voltage.
2. The reset signal is removed, allowing the floating-diffusion node to float, and the output voltage level is recorded.
3. The signal charge is dumped onto the floating-diffusion node.
4. The output voltage is read again; the signal is the difference of the two output readings.

If the $\frac{kT}{C}$ noise introduced during reset of the sensing node is suppressed by correlated-double sampling, amplifier noise limits the performance of a CCD image sensor [94]. The floating-diffusion charge detector introduces thermal and $\frac{1}{f}$ noise from MOS transistors. Unfortunately, because the capacitance seen at the detection node determines the charge-to-voltage conversion gain, the first-stage source follower is sized as a compromise between gain and noise performance.

In order to drive a large output capacitance, a multi-stage source follower is used. The number of stages is determined by the required pixel-data rate, for example, a HDTV sensor could need as many as four stages [95]. Subsequent stages are sized to drive the output capacitance, consequently, the first-stage dominates noise performance. The amplifier gain can be improved by reducing the body-effect of source followers using p-well driver transistors. High-frequency performance can be improved by connecting the source and well via a high-pass filter [96]. The minimum capacitance of a floating-diffusion node is limited by the polysilicon contact.

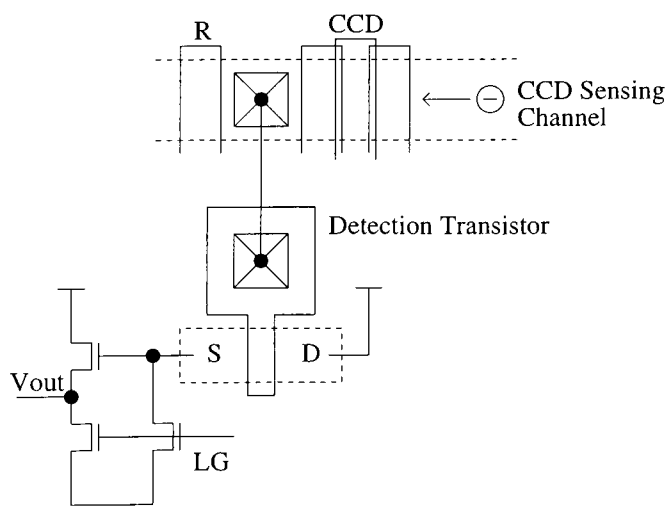


Figure 4.7: *A conventional floating-diffusion charge detector.*

Matsunaga uses a $\frac{kT}{C}$ noise free n-type buried sensing channel and p-channel double-gate floating surface detection transistor to generate a gain of $220\mu Ve^{-1}$ and a total noise equivalent charge of $0.5e^{-}$ within the band 10 kHz to 3.58 MHz [94]. A $\frac{kT}{C}$ noise free operation has a further advantage that correlated-double sampling is not required. Hence, the required amplifier bandwidth is reduced by a factor of two. If thermal noise dominates $\frac{1}{f}$ noise, this reduction in required bandwidth will improve the amplifier noise performance.

4.6 CCD technology

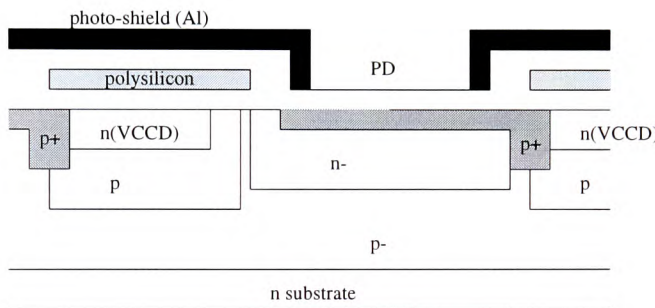


Figure 4.8: *Cross-section of a unit interline-transfer imager cell.*

4.6.1 Pixel cell

The generation of electron-hole pairs is identical to a CMOS pixel. Therefore, like the CMOS sensor, low-illumination performance is limited by dark current. Two methods are commonly used to reduce the effect of surface states and, hence, suppress dark current [10]:

1. A surface p^{+}-diffusion ensures that the electron recombination rate is greater than the generation rate.
2. Appropriate gate bias is applied to attract carriers to the oxide-semiconductor interface.

Dark current suppression techniques are the most important example of where CMOS image sensing technology can benefit from the progress made in the CCD process.

4.6.2 Fabrication[4]

Fabrication of a CCD is more complex and, consequently more expensive than a CMOS based device. The primary reason for the increased complexity is the first oxide layer, which must not be altered by subsequent processing. Further problems are caused by oxide growth under the edges of the first layer of polysilicon, which results in non-uniformities in the channel potential. The difficulties in fabrication cause the second oxide layer to be of lower quality than the first, resulting in:

- greater leakage current, than a planar CCD sensor.
- lower breakdown voltages.
- reduced yield.

4.6.3 Post-fabrication treatment.

Chip packaging costs are a significant proportion of the total sensor cost [27]. Post-fabrication processing is common to CMOS and CCD sensors and, therefore, the costs involved reduce the benefit of a lower cost process. The next section discusses the microlens, which is a good example of CMOS image sensors borrowing a technology from the CCD process.

4.6.3.1 Microlens

A pixel unit is made up of the diode, which is the light sensitive area and a number of other transistors and signal lines. The cell fill-factor, ff, is defined as

$$ff = \frac{A_\nu}{A} \times 100\% \tag{4.3}$$

where A_ν is the diode area and A is the total pixel cell area. The fill-factor is an indication of the proportion of incident light that can contribute to the light signal and is approximately 30% for a commercial image sensor [60]. In order to utilize a higher proportion of the incident light, an array of microlenses is used. Each pixel unit is covered by a miniature lens that focuses light onto the light sensitive area, which increases the effective fill-factor to over 70% [17]. The ratio of condensed light depends upon [97]:

- The microlens radius of curvature.

- The refractive index of the microlens material.
- The height from the photodiode.
- The distance between microlenses.

It should be noted that Equation 4.3 will tend to underestimate the cell fill-factor, since carriers can contribute to photocurrent even if not generated under the diode [11].

4.6.3.2 Post-fabrication treatment [97]

Post-fabrication treatment is used to add filters and microlens to an imaging chip. The required post-fabrication steps are:

1. Planarisation.
2. Deposition of optical filters.
3. Passivation.
4. Addition of the microlens array.
5. Packaging. The package must:
    - have a transparent, hermetically sealed lid.
    - be able to dissipate sensor power.
    - be manufactured, including chip placement, to tolerances sufficient for inclusion in an optical system.

Filters are often organic, consequently, they are heat and chemical sensitive. Subsequent steps, including adding microlenses must, therefore, be simple. The post-fabrication steps are common to CCD and CMOS sensors and the associated costs will tend to mitigate the process price advantage of the CMOS sensor [27].

4.6.4 Blooming protection

Shutter operation and blooming control is provided by an overflow drain, whereby excess charge is removed from the pixel over a potential barrier. In an interline-transfer CCD, smear

occurs if charge diffuses laterally from the photodiode to the shift register. The anti-blooming structures presented in this section may exacerbate this effect, because portions of the image are allowed to move beyond saturation [98].

4.6.4.1 Vertical overflow drain

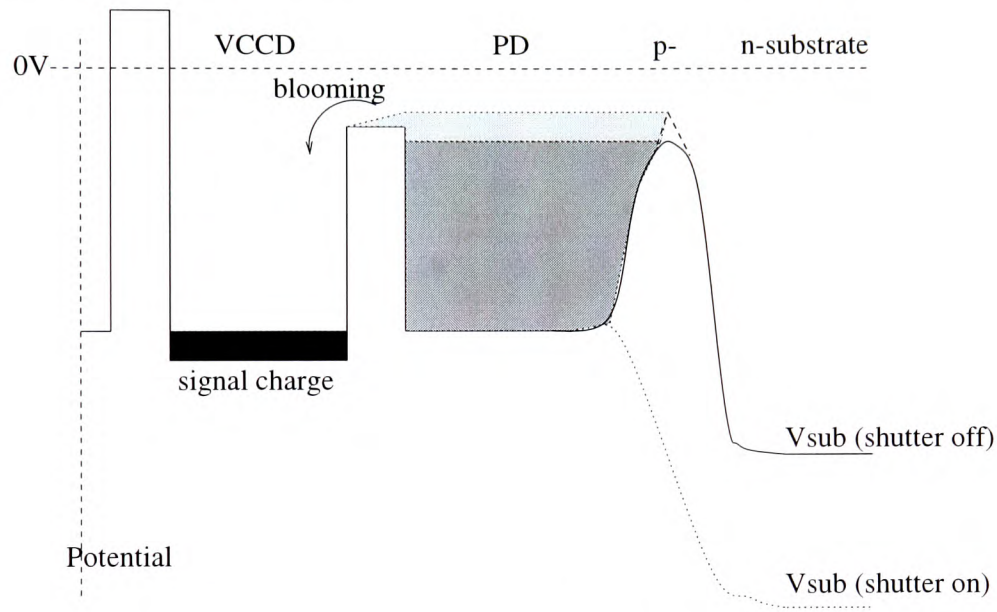


Figure 4.9: *Potential profile of a vertical overflow drain in electronic shutter mode [30].*

Vertical blooming control is provided by modulating the substrate potential, as shown in Figure 4.9. The variation in the substrate potential controls the height of the potential barrier between the well collecting the signal charge and the substrate. In order to provide sufficient anti-blooming protection, the potential barrier height should be less than the potential barrier between the pixel and the vertical CCD. If this technique was used in a CMOS sensor, it would be possible to remove dedicated anti-blooming transistors or reduce the size of reset transistors which are also used for blooming protection. Thus, improving the achievable fill-factor for a given pixel pitch.

4.6.4.2 Lateral overflow drain

A lateral overflow drain uses a second gate to generate a lateral potential barrier. Operation is similar to the overflow-drain transistor discussed in Section 2.5.1.3. The primary disadvantage

of lateral operation is the area penalty. Further to the disadvantage of the lateral technique, any difference in threshold voltage between the reading and shutter gate causes charge to remain after readout. This charge adds to the next pixel value and manifests itself as fixed-pattern noise. Consequently, the photodiode should be in complete depletion when signal charges are read or swept out. Therefore, when activated neither gate should have a potential barrier or dip. To ensure that there is no potential barrier, alignment between the p^+ and n^- diffusion

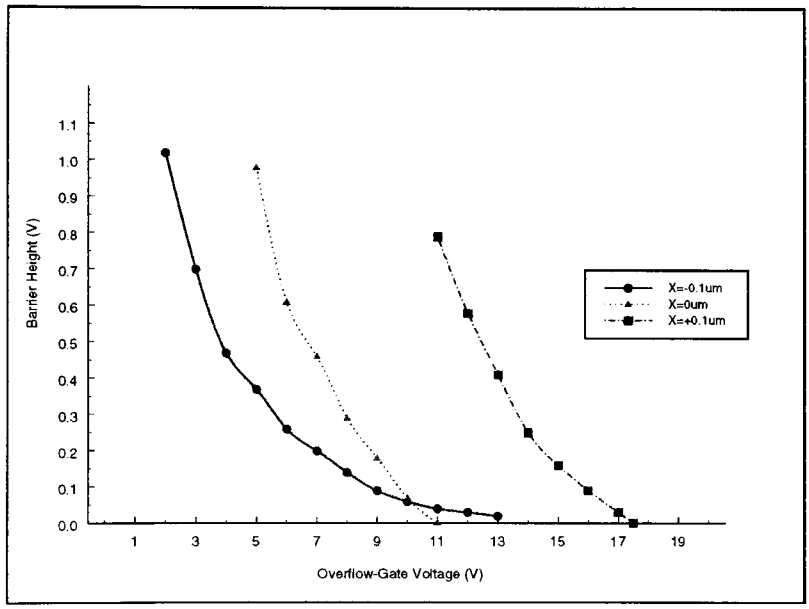


Figure 4.10: *Calculated barrier height of the overflow gate [31].*

is crucial. If the surface p^+ diffusion is shifted towards the overflow gate a potential barrier is formed and the charge-transfer efficiency is reduced. For example, Ando found that if the shift is $0.1\mu m$, a clock voltage of 17V is required to remove the potential barrier, as shown in the curve $X = 0.1\mu m$ in Figure 4.10. In a similar way, a potential barrier is formed with a misalignment towards the photogate. Therefore, in order to maintain a sufficient charge-transfer efficiency, a self-alignment technique should be used[31].

4.7 Noise performance

The worst-case signal charge sensed at the collection diode is given by

$$Q_{signal} = R\eta^{2n}H \tag{4.4}$$

where R is the average diode responsivity; η is the shift-register charge-transfer efficiency; $2n$ is the number of transfers the signal undergoes before reaching the collection diode and H is the incident illumination.

In order to calculate the achievable signal-to-noise ratio, the noise sources listed below are compared to the worst-case signal charge given by Equation 4.4 The sources of noise are [99]

- Nyquist noise, $\bar{q}_n$, at the reset switch and output capacitance, which is given by

$$\bar{q}_n^2 = kTC \tag{4.5}$$

- Shot noise, $\bar{q}_s$, associated with the sensor and the shift register, which is given by

$$\bar{q}_s^2 = q(I_{LR} + I_{LS}(1-\eta)^{2N})\tau \tag{4.6}$$

  where τ is the line readout time; I_{LR} is the total shift-register leakage current and I_{LS} is the pixel leakage current.

- Surface state-noise, $\bar{q}_{ss}$ associated with the transfer of charge to and from the the $Si - SiO_2$ interface states within the sensor, which is given by

$$\bar{q}_n^2 = kTC_{st} \tag{4.7}$$

  where C_{st} is an effective surface state capacitance determined by the number of transfers, the clock frequency and the effective bandwidth of the signal processor.

- Thermal and $\frac{1}{f}$ noise generated by the on-chip amplifier, which because of the relative size, should be less than the contribution of the in-pixel source follower in a CMOS active-pixel sensor.

As discussed in Appendix D, correlated-double sampling can be used to suppress kTC and 1/f noise. In which case, the total random noise contribution is less than $\frac{1}{4}$-LSB at 10-bit resolution.

4.8 Future prospects

The viability of CMOS image sensors depends upon advances in both CCD and CMOS technologies. Consequently, it is interesting to study the likely advances in CCD technology.

4.8.1 Scaling

4.8.1.1 Pixel

In an interline-transfer CCD, pixel scaling is difficult because both the vertical CCD and pixel must be scaled while maintaining sufficient blooming protection. At the beginning of 1990, the state-of-the-art pixel size was $7.3 \times 7.6\mu m^2$ [91]. Recently, two CCD imagers have been presented with pixel sizes of $5 \times 5\mu m^2$ [96] and $4 \times 4\mu m^2$ [100]. Such improvements have been achieved using low-temperature oxidation techniques to limit channel narrowing caused by the lateral diffusion of implants. A further reduction in pixel size is not required until lens technology improves.

4.8.1.2 Sensor chip

Packageless assembly and direct bonding techniques have allowed a 50K pixel sensor, fabricated on a $1.1 \times 1.34mm^2$ chip to be fitted to a camera module measuring $1.2 \times 1.5 \times 2.7(z)mm^3$. Coupled with a power consumption of 5mW, the system is competitive with a CMOS camera system for the miniature camera and probe markets [100].

4.8.2 Combined CCD-CMOS processes

Combined CCD-CMOS processes are based on either a CMOS or CCD process. Extra fabrication steps provide CCD capability on a CMOS process (CMOS with CCD) or CMOS capability on a CCD process (CDD with CMOS). The relative merits of the alternatives are discussed next.

4.8.2.1 CMOS with CCD

In 1985, Terakawa presented a passive pixel sensor with a buried-channel CCD horizontal shift register to transfer the signal from each column to the chip amplifier[101]. More recently, the MOSIS foundry has offered a $2\mu m$ CMOS with CCD process, which achieves a charge-transfer

efficiency of 0.995 [102]. This process has been used to fabricate a 2D real-time motion estimators. The CCD capability was used to provide the pixel array and an area and power efficient correlation function, whilst CMOS was used for a digital interface, winner-takes-all circuitry, and comparators [102, 103]. With reference to Figure 4.3, the charge-transfer efficiency is not sufficient to be used to create an imaging array of appreciable size. If a pixel array is required, CMOS capability must be added to a CCD process.

4.8.2.2 CDD with CMOS

MOS circuits are routinely integrated on CCD image arrays, for example, the on-chip output amplifier, which comprises a cascade of source followers. More complex structures have also been integrated such as bipolar transistors for output drivers [91]; inverters and sample-and-hold functions [104]; and on-chip clock drivers, flip-flops, timing generators and bias circuits [100, 104]. However, a combination of channel length, for example, the 1990 minimum channel length of $4\mu m$ was 5 times greater than the commercially available $0.8\mu m$ CMOS process and NMOS only technology, limits integration to simple circuits. Consequently, multi-chip systems are the norm.

The integration of correlated double sampling, analogue-to-digital conversion, clock drivers and timing generation on-chip would reduce system size, cost, component count and possibly improve performance. To do so, however, would require CMOS transistors comparable to those available on commercial digital processes. With this aim, in 1994 Guidash developed a $2\mu m$ process under the following constraints:

- the baseline steps, effective thermal history, and characteristics of the CCD process should not be altered.
- the NPN and CMOS process modules should be compatible with $2\mu m$ cell libraries.
- the process should be cost effective and manufacturable.

CMOS devices were realized with four additional masks (N-well, P-field threshold, threshold adjust and P^+-source/drain) and three additional implants (N-well, threshold adjust, and p^+-source/drain). Both poly-1 and poly-2 CMOS transistors were available with $\pm 0.75V$ and $\pm 0.95V$ threshold voltages. NPN devices were realized with the addition of an optional buried collector implant, a deep n^+ implant and an intrinsic base implant. Results showed that

integration of a CCD and CMOS process was possible without affecting the CCD imaging performance [105].

Before the integration of significant digital circuitry, a further reduction in channel length is required. However, analogue processing and analogue-to-digital conversion are feasible with this technology. For example, column amplifiers could be integrated with the sensor array, eliminating the high-frequency HCCD.

A number of further problems with combined CMOS-CCD processes remain [49]:

- The efficiency of the read and write circuit for transferring data between CMOS and CCD circuits needs to be improved.
- Cross-coupling from the clock drivers to analogue circuitry limits performance.
- The total chip power consumption needs to be carefully controlled.

4.8.3 Low-voltage CCD cameras [5]

Traditionally, double-electrode structures are used to minimize the inter-electrode gap and, hence, improve the charge-transfer efficiency. A multi-layer CCD process increases the reflection and refraction of light. Further to the advantage of a planar process, the reduction in capacitive coupling between layers improves frequency performance. In 1991 Hoople showed that a planar device with a $0.15\mu m$ inter-electrode gap could be fabricated. The parasitic potential well of $0.15V$, could be removed with a $1V$ difference between gates [92]. Using this technology a planar CCD device was possible.

The power consumed by CCD area image sensors is mainly determined by that of a two-phase horizontal CCD, which is operated at the pixel-data rate. Potential pockets, which appear below inter-electrode gaps are eliminated using a higher driving voltage than a minimum over-swing voltage. The minimum driving voltage for a two-phase H-CCD, ΔV_{min}^{H-CCD}, is given by

$$\Delta V_{min}^{H-CCD} = \Delta V_{min} + \frac{\Delta\phi}{\alpha} \tag{4.8}$$

where $\Delta\phi$ is the potential difference between a storage and barrier channel; and α is the channel potential modulation coefficient. The double-electrode structure prevents the use of self-aligned diffusion implants to reduce the potential pocket, and, consequently, the minimum over-drive

voltage. The single-layer structure shown in Figure 4.11, uses self-aligned boron implants to

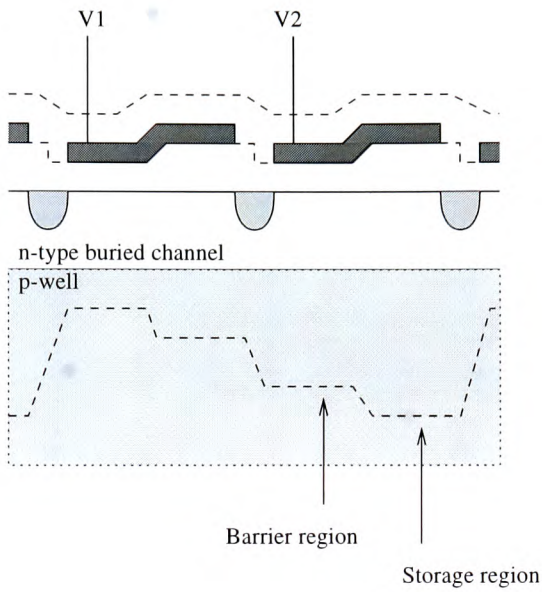


Figure 4.11: *A single-layer electrode CCD after Tanaka [5].*

remove parasitic potential humps and, hence, reduce the required clock swing to 1.8V. Figure 4.12 shows that this is less than half the voltage required for a conventional CCD.

4.9 Signal processing

Modern camcorders use digital processing in the signal path even though the signal from the CCD and signal recorded on the internal VTR are in analogue form. Before the signal can be digitized, clamping and low-noise gain must be applied. These functions are often performed on a dedicated 5V bipolar chip. The drive for reduced power consumption has led to the integration of the ADC, a correlated-double sampling block, a variable-gain amplifier, a black-level correction loop, and input clamp and voltage reference on a single chip consuming 190mW at 3.15V for 10-bit resolution, which corresponds to a factor-of-two reduction in system power consumption [106].

Further power reductions can be obtained if more functions are integrated with the sensor. Even without CMOS capability, limited signal processing can be performed using CCD elements, for example, Figure 4.13 shows a charge averaging operation, which is composed of addition and division by two. Other possible operations are hold, transfer and, using oxide barriers, charge-

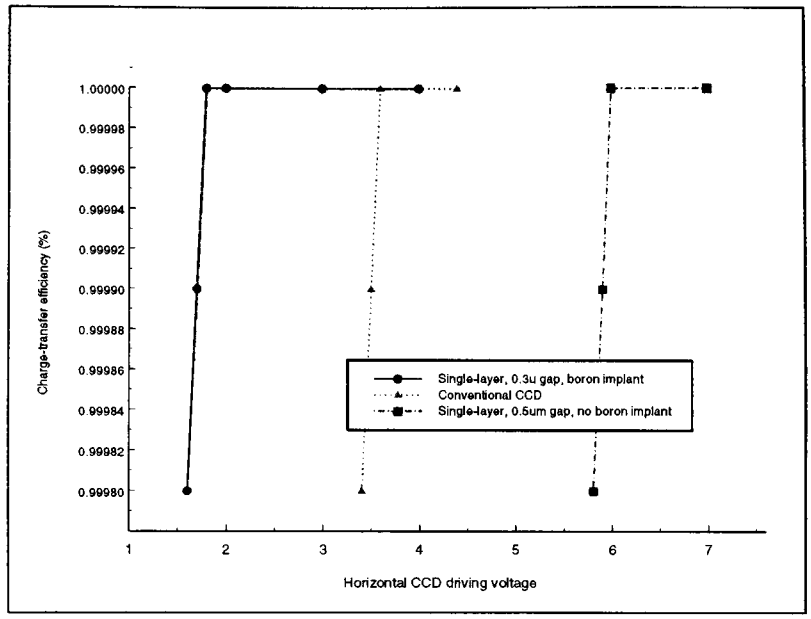


Figure 4.12: *Charge-transfer efficiency as a function of the HCCD driving voltage for a planar CCD, conventional CCD and planar CCD with boron implants [5].*

packet splitting up to 12-bit resolution [107]. These functions are sufficient for the 10-bit, pipelined charge-to-digital converter presented by Paul, which consumed only 13mW for 4V operation at 22Mhz [108]. A fundamental advantage of the charge-to-digital converter is that the correlated-double sampling operation is not required because a reference level does not need to be established.

4.10 Conclusions

Analysis of the CCD sensor has identified two areas where CMOS sensors can borrow technology to improve performance: the reduction of dark current and the use of microlenses. Future trends in CCD imagers are difficult to predict. However, if low-voltage operation or the integration of on-chip signal processing becomes crucial in the solid-state imager market, it has been shown that CCD imager technology can adapt to these new demands.

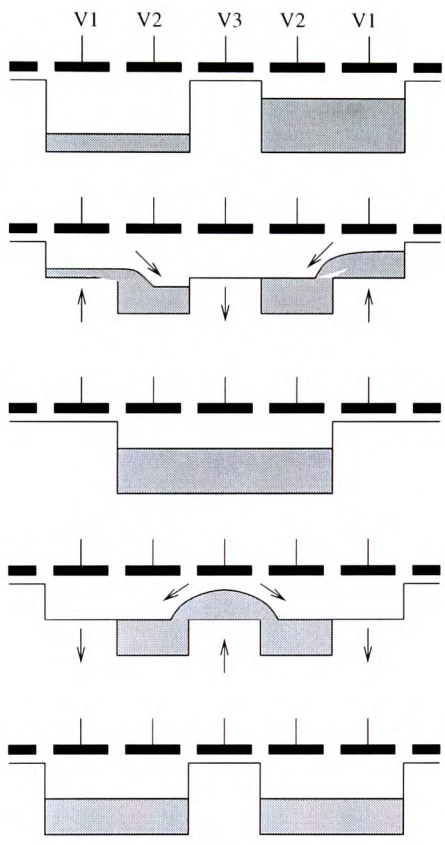


Figure 4.13: *The charge-averaging operation.*

Chapter 5
Technology Scaling

5.1 Overview

Over the last twenty years, the evolution of CMOS technology has followed Moore's Law, which states that: a new technology generation is developed every three years and that, between generations, memory capacity increases by a factor of four and logic circuit density increases by a factor of between two and three. Further, every six years, or two generations, the feature size decreases by a factor of two; transistor density, clock rate, chip area, chip power dissipation and the maximum number of pins doubles. This continual development has led to a reduction in the state-of-the-art, commercially available, minimum lithographic feature size from $3\mu m$ in 1977 to $0.25\mu m$ in 1998 [109]. It is anticipated that it is technically possible to maintain the development, shown in Table 5.1, over the next decade [109]. However, the cost involved could become prohibitively high, for example, a fabrication plant costs 2 billion dollars today and this will double every three years.

Year	1991	1994	1997	1999	2003	2006
Minimum Feature Size (μm)	0.5	0.35	0.25	0.18	0.13	0.09
Supply Voltage, V_{dd} (V)	5	3.3	2.5	1.8	1.5	1.2
Oxide Thickness, t_{ox} (nm)	13.5	9	8	7	4.5	4
Junction Depth, x_j (μm)	0.15	0.15	0.1	0.08	0.08	0.07
Threshold Voltage, V_T [109]	0.7	0.7	0.7	0.7	0.7	0.7
Threshold Voltage, V_T [6]	0.6	0.5	0.45	0.4	0.3	0.3
Metal Layers	3	5	6	$6-7$	7	$7-8$

Table 5.1: *The Evolution of CMOS Technology [42].*

CMOS process development is paid for by the sale volume of standard CMOS logic and memory chips. Hence, CMOS imagers do not have to bear the research costs and, consequently, benefit from cheaper process costs than CCD imagers. Fabrication costs are further reduced, because imagers do not use the state-of-the-art processes; in 1996 $0.35\mu m$ technology was standard, however, commercial imagers used $0.8\mu m$ technology [6].

This chapter investigates how technology scaling will affect CMOS imagers. Initially, scaled-process characteristics are reviewed, after which, the challenges facing imager design on deep-submicron processes are discussed.

5.2 Scaling CMOS processes

A prerequisite of scaling is that the drain-source current is controlled by the gate-source voltage. Therefore, the source and drain depletion regions should not punchthrough and, hence, the substrate doping concentration must be increased as channel length is reduced. A consequence of the increase in substrate doping is that the junction breakdown voltage is reduced and, to avoid breakdown, beyond $0.5\mu m$ the maximum supply voltage must be scaled.

Submicron devices, operated in the saturation region, depart from the traditional square-law model. Both reduced geometry and the increased electric field strength affect device performance. The relative importance of these effects is dependent upon the source- and drain-junction depth and the supply voltage. Geometrical, often called short-channel, effects dominate high-field effects as the supply voltage is reduced and junction depth is increased. It is anticipated that junction depths will be scaled aggressively to suppress short-channel effects [109].

A CMOS process is optimized to maintain digital performance at low supply voltages. Analogue characteristics, however, deteriorate at low supply voltages. Therefore, in future generations of CMOS imagers, signal processing will be increasingly performed in the digital domain, with a minimum number of critical analogue blocks [51].

The remainder of this section discusses the characteristics of a scaled process.

5.2.1 Short channel effects

5.2.1.1 Drain-induced barrier lowering (DIBL)

Drain-induced barrier lowering is a precursor of drain-source punchthrough. The source and drain depletion regions extend into the channel causing a reduction in threshold voltage, ΔV_T, which is given by

$$\Delta V_T \approx V_{dd} e^{-\frac{L}{l_1}} \tag{5.1}$$

where $l_1 \propto x_j^{\frac{1}{3}} t_{ox}$; where x_j is the drain- and source-diffusion junction depth. The extension of drain and source regions into the channel will tend to reduce the device output resistance. Therefore, as a process is scaled, analogue design should use devices further away from minimum size.

The process threshold voltage is determined to suppress the subthreshold current for a minimum sized device to an acceptable level. A consequence of DIBL is that the longer channel length devices used in analogue design will have a larger threshold voltage than is necessary to suppress subthreshold current, reducing the maximum pixel voltage swing.

5.2.1.2 Velocity saturation

When the electric field strength in a channel is increased above a critical value, the channel carrier velocity saturates and is no longer proportional to the electric field. The velocity saturated drain-source current, I_{dsat} is given by

$$I_{dsat} = W \times v_{sat} \times Q_{inv} \tag{5.2}$$

where v_{sat} is the saturated carrier velocity and Q_{inv} is the inversion charge density at pinch-off, which is given by

$$Q_{inv} = C_{ox}(V_{gs} - V_T - V_{dsat}) \tag{5.3}$$

where V_{dsat} is the drain saturation voltage [110]. Equation 5.2 states that, under velocity saturation, the drain-source current is independent of the channel length. Therefore, to provide a greater drive capability *per* unit transistor width, the inversion charge density must be increased. Equation 5.3 indicates that the inversion charge is proportional to the oxide capacitance, C_{ox}. Consequently, in order to increase the saturation charge, the gate-oxide thickness is reduced as devices are scaled.

The drain-source current dependence on the gate-source voltage departs from the quadratic law and obeys a power law, such that $I_{ds} \sim V_{gs}^{\alpha}$ where $1 < \alpha < 2$ [111]. Consequently, drain-source current increases more slowly with gate-source voltage. At reduced supply voltages, if $V_{GS} < 1V$ this effect will be mitigated.

5.2.2 Electric field effects

5.2.2.1 The hot-electron effect

In short-channel devices, the increase in electrical field strength causes an increase in average electron velocity. Upon reaching a sufficient velocity, or becoming hot, an electron can tunnel into the gate-oxide. Trapped electrons increase the oxide charge and, hence, alter the device threshold voltage. This can cause long-term reliability problems. Therefore, special device structures are designed to reduce the hot electron effect, for example, the lightly doped drain transistor [112].

With the proviso that the variation in threshold voltage is sufficiently small not to significantly reduce the pixel voltage swing, CMOS sensor design should be immune to the hot-electron effect because offsets are cancelled to reduce fixed-pattern noise to an acceptable level.

5.2.2.2 Tunnelling

At the $0.18-0.13\mu m$ generation of technology, the p-n diode tunnelling current will surpass the thermally generated diode reverse current seen using the $0.5\mu m$ technology [110]. Dark current will, therefore, increase due to a non-linear voltage dependent tunnelling current. Consequently, low-light level imager performance will deteriorate. PMOS pixels may be used to reduce this tunnelling current [6].

5.2.3 Threshold voltage scaling

It is unclear how rapidly threshold voltages will scale in future generations of technology: Hu predicts that the threshold voltage will remain constant at 0.7V, while Wong expects a reduction from 0.7V at $0.5\mu m$ to 0.4V at $0.18\mu m$ [6, 109]. However, the linear reduction in V_T predicted by Wong is unlikely because of the associated increase in subthreshold current [111]. For example, a $0.2V$ reduction in a V_T of $0.7V$, with a gate-source voltage of $2.5V$, would increase I_{dsat} by 20% but it would increase the subthreshold current by three orders of magnitude.

The relative scaling of the threshold and supply voltage determines the achievable pixel output voltage swing, which limits the achievable signal-to-noise ratio. For an active pixel, as discussed in Section 2.5.2, the maximum voltage swing is given by $V_{dd} - 2V_{T(max)} - 0.2V$, provided that the body effect is negligible. Assuming that the threshold voltage does not scale,

this evaluates to a swing of 2.8V for a $0.8\mu m$ process, reducing to 1.1V at $0.18\mu m$ and to $0V$ by the $0.13\mu m$ generation. For pixel operation, threshold voltage scaling is necessary to increase the voltage swing, whilst the consequent increase in subthreshold current is mitigated because the reset and read transistors have a negative gate-source voltage.

5.2.3.1 Variation in threshold voltage

The previous discussion showed how the threshold voltage limited the voltage swing at the pixel. In practice, the threshold voltage is not constant and, therefore, variations impose a further limit on the achievable voltage swing. For a given process, threshold voltage variation is modelled by

$$\sigma(\Delta_{V_T}) = \frac{A_{V_T}}{\sqrt{WL}} \tag{5.4}$$

where A_{V_T} slowly decreases with L and is $10mV\mu m$ at $0.5\mu m$ channel length [113]. Equation 5.4 shows that as device area is increased, the threshold mismatch is reduced.

Small devices, such as those found in an active pixel, exhibit a greater variation in threshold voltage than predicted by Equation 5.4. The increase in standard deviation is due to the stochastic nature of the diffusion process: for a given volume of depletion region, the number of dopant atoms follow a Poisson distribution with a standard deviation of $\sqrt{N}$ where N is the average number of dopant atoms in the depletion region. The threshold voltage standard deviation, due to the dopant atom distribution, σ_{V_T}, is given by

$$\sigma_{V_T} = \frac{q}{2C_{ox}}\sqrt{\frac{\pi N_A}{2}}(W_{eff}L_{eff})^{-\frac{3}{8}}X_D^{\frac{1}{4}} \tag{5.5}$$

where X_D is the depletion depth and N_A is the doping density. Equation 5.5 evaluates as 20mV in a $0.35\mu m$ technology, increasing to 30mV at $0.1\mu m$ [43]. Burnett found that the total variation in threshold voltage was dominated by this effect in minimum sized devices [43].

In order to calculate the effect of threshold variation on the voltage swing at the pixel, the threshold mismatch of both the reset and source-follower transistor must be considered. Consequently, assuming the variation in threshold voltage is uncorrelated, the total standard deviation is $\sqrt{2}\sigma_{V_T}$. After calculation of the standard deviation, using Equation 5.5, Figure E.2 should be used to determine the number of standard deviations to consider. For example, seven

Process	$0.35\mu m$	$0.25\mu m$	$0.18\mu m$	$0.13\mu m$	$0.1\mu m$
σ_{V_T} (Min size)	$18.7mV$	$20.0mV$	$22.8mV$	$25.9mV$	$27.5mV$
$7\sqrt{2}\sigma_{V_T}$ (Min size)	$0.19V$	$0.20V$	$0.23V$	$0.26V$	$0.27V$
σ_{V_T} (constant size)	$18.7mV$	$17.8mV$	$17.6mV$	$17.3mV$	$17.2mV$
$7\sqrt{2}\sigma_{V_T}$ (constant size)	$0.19V$	$0.18V$	$0.17V$	$0.17V$	$0.17V$

Table 5.2: *Standard deviation for transistor threshold voltage with process scaling after Burnett [43].*

standard deviations is a sensible limit for an array size of 1000×1000. Table 5.2 gives the reduction in voltage swing based on the above assumptions, for two cases: minimum sized devices and constant device size, which is equivalent to a minimum sized device at $0.35\mu m$. The predicted reduction in voltage swing is equivalent to a 30% reduction at $0.18\mu m$, assuming that the threshold voltage is scaled aggressively. Consequently, pixel transistors should be scaled less aggressively than the process dimensions. Further, as the supply voltage is reduced, it is advantageous to increase the size of pixel transistors.

A further consequence of threshold voltage variation is that the variation in propagation delay increases as processes are scaled [114]. Digital circuits design must, therefore, be more conservative.

5.2.4 Silicon-on-insulator substrates [6]

Silicon-on-Insulator (SOI) technology is predicted to become the standard process beyond the $0.25\mu m$ generation [42]. There are four fundamental differences between SOI and present silicon technology:

1. **Charge collection volume.** Typical SOI wafers use a $< 200nm$ thick silicon film, severely reducing the charge collection volume, particularly for long wavelength photons. For example, a $100nm$ film absorbs less than 20% of the incident photons of wavelength greater than $500nm$.

2. **Substrate contacts.** It is unclear whether substrate contacts will be used for SOI technology. For CMOS SOI imagers, it is necessary to remove photo-generated charge via a substrate contact.

3. **Isolation.** Full dielectric isolation will reduce the crosstalk between pixels. However,

this is at the expense of increased pixel pitch.

4. **Parasitic capacitances.** Smaller parasitic capacitances will reduce the crosstalk from digital supplies etc.

5.2.5 Silicide technologies

Technologies after the $0.5\mu m$ generation use silicide films. Unfortunately, the absorption length of titanium silicide at $633nm$ is $20nm$ compared to $0.2 - 5\mu m$ for phosphorus doped polysilicon. Therefore, to improve imager sensitivity, silicide deposition must be blocked around the pixel sites.

5.3 Pixel scaling

Section 5.2 discussed the motivation for the reduction in oxide thickness, diffusion-junction depth and supply voltages. This section examines how CMOS imager performance will be affected by deep-submicron processes.

5.3.1 Fill-factor

The most obvious benefit of finer lithography is that the pixel fill-factor for a given pitch can be improved. Consequently, the minimum practical pixel pitch is reduced. However, this benefit is lessened if transistors are not scaled to maintain analogue performance and to reduce mismatch. Furthermore, pixel scaling beyond $5\mu m$ is not needed because this is the diffraction limit of the current lens technology [27]. Concluding, the increase in fill-factor will be due to:

- **finer line widths.** For example, if a $12\mu m$ pixel pitch is assumed, a minimum width column in metal2 and row in metal1 reduce the available area, as a percentage of the total pixel area, to 72% in a $0.8\mu m$ technology, which increases to 84% at the $0.5\mu m$ generation.
- **stackable contacts.** A contact-via stack increases the available pixel area by 0.8%.
- **more metal and polysilicon layers.** The increase in the number of layers available for interconnect could further improve the pixel fill-factor. However, this is at the expense of

increased capacitive coupling between signals on the focal plane. Further, on planarized processes, there is a maximum distance between instances of each metal layer. Otherwise, floating metal must be added so that depressions do not form on the chip surface. Whether this will make present pixel structures impractical depends upon the permitted gaps between the metal structures.

5.3.2 Spectral response

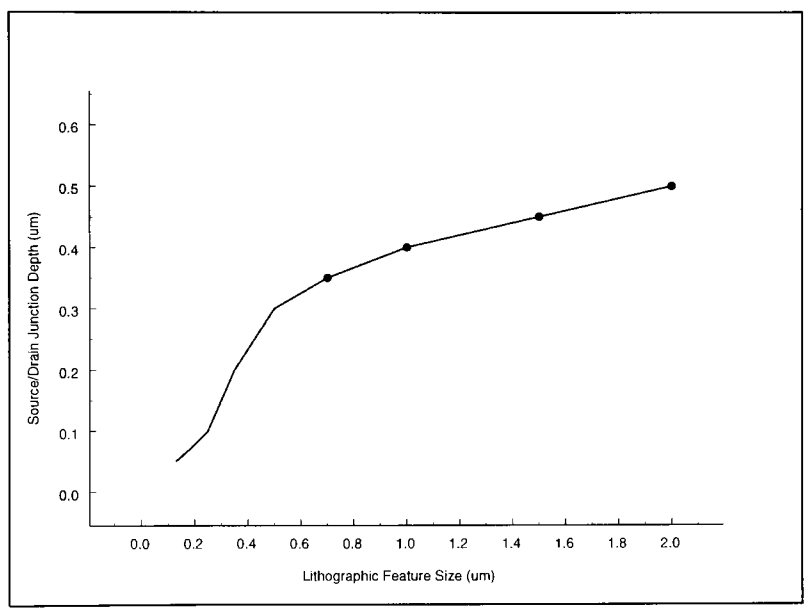


Figure 5.1: *Source and drain junction depth as a function of lithographic feature size [6].*

Figures 5.1, 5.2 and 5.3 show the variation of the source- and drain-junction depth, depletion region depth and the diffusion length of carriers in the semiconductor bulk with minimum lithographic diffusion size. As the process is scaled, the vertical dimensions shrink and the diffusion length is reduced, the affect on pixel spectral response is considered below:

- The reduction in diffusion length will suppress the contribution of longer wavelength light to photocurrent. Furthermore, if the pixel pitch remains constant, pixel crosstalk will be reduced.
- The reduction of vertical dimensions will exacerbate the blue, or short-wavelength, shift in the spectral response.

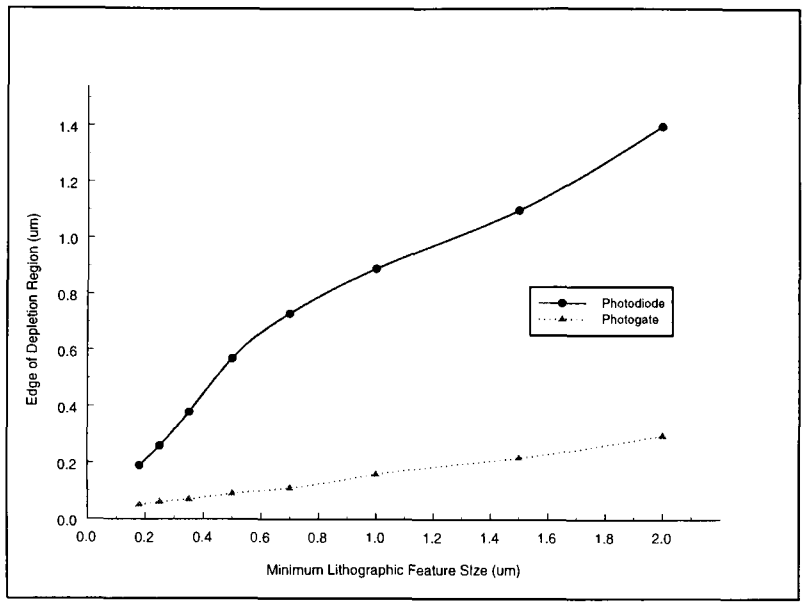


Figure 5.2: *Depletion region depth as a function of lithographic feature size [6].*

- Without improvements in the $Si - SiO_2$ interface, shallower junction depths could cause an increase in dark current due to surface-states.

5.3.3 Noise performance

As discussed below, the total pixel noise contribution will decrease with technology scaling. However, the decrease in supply voltage will erode this benefit.

5.3.3.1 Flicker noise

The flicker noise spectral density is given by Equation B.13, which is repeated below

$$S_{if} = \frac{K_F I_{DS}^{A_F}}{f C_{ox} L^2} \tag{5.6}$$

If the transistor dimensions are not scaled, the increase in gate-oxide capacitance [66] will cause a reduction in the flicker noise contribution for future generations of image sensors.

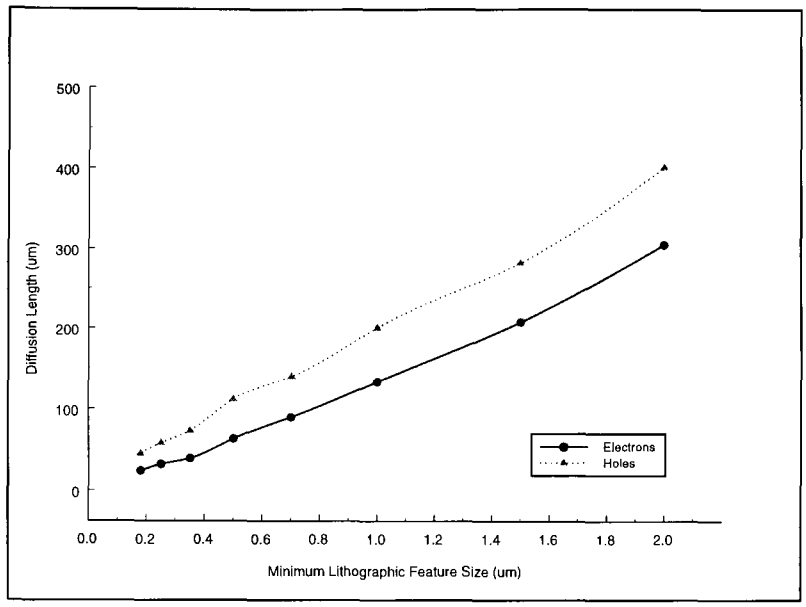


Figure 5.3: *The electron and hole diffusion length as a function of lithographic feature size [6].*

5.3.3.2 Thermal noise

The thermal noise contribution is proportional to the device transconductance and can, therefore, remain constant during technology scaling.

5.3.3.3 Shot noise

The shot noise spectral density is determined by the magnitude of the current flowing accross a junction and, therefore, does not scale with technology.

5.3.3.4 Dark current

The capacitance *per* unit area increases as technology is scaled, therefore, to achieve a given pixel discharge, the integration time must be increased. Consequently, because the shot noise charge is proportional to the square-root of the integration time, the shot noise contribution will be less significant. However, as discussed in Section 5.2.2.2, tunnelling current could dominate thermally generated dark current beyond the $0.18\mu m$ generation. Unfortunately, at this time the magnitude of the tunnelling current is not known and, therefore, the dark current performance

of imagers on processes beyond the $0.18\mu m$ generation is unclear.

5.4 Low-voltage design

As discussed previously, a reduction in supply voltage to 3.3V at $0.35\mu m$ is necessary to avoid junction breakdown. In practice, a more rapid reduction in supply voltage may be desirable for low-power applications and to reduce the power consumption of large-array imagers. This section discusses three generic strategies to realize low-voltage analogue design, namely:

- Low-voltage devices.
- On-chip generated voltages.
- Novel design techniques.

5.4.1 Low-voltage devices

In order to operate in the saturation region, a MOS transistor requires a gate-source voltage greater than the threshold voltage and a drain-source voltage greater than the saturation voltage, $V_{GS} - V_T$. For low-voltage operation a number of operation modes have been suggested to improve the input or output voltage swing.

5.4.1.1 Low-threshold voltage MOS transistors

The most obvious way of increasing the input range of a MOS transistor is to lower the threshold voltage. One method of creating a low-threshold device is to block the threshold adjusting implant during fabrication [115]. An additional benefit of this technique is that the device body effect is reduced. However, such a low-threshold device suffers from an increase in subthreshold current. If the device is biased with a negative gate-source voltage, for example, when used as the reset transistor in a pixel, the increase in subthreshold current should be negligible. If two low-threshold, for example 0.3V, devices were used in an active pixel, the maximum voltage swing would double for a 3.3V supply.

The increase in subthreshold current caused by a significant reduction in threshold voltage increases the steady-state current for a CMOS logic gate. If the power consumption is unacceptable, a variable threshold technique can be used. Kuroda and Oowaki use substrate biasing

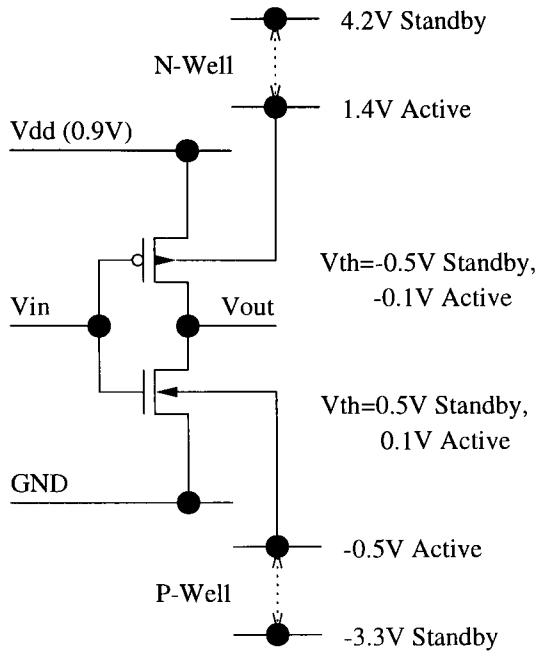


Figure 5.4: *Variable threshold voltage inverter [32].*

to increase the threshold voltage during standby mode [32, 116]. Their technique, shown in Figure 5.4, reduces the leakage current by four orders of magnitude. Although high voltage supplies are used, they are applied to the substrate and not the gate-oxide or source and drain junctions, consequently, a low-voltage process can be used.

5.4.1.2 Bipolar transistors

It is well documented that bipolar transistors can operate at lower supplies than a MOSFET [56, 79]. Two factors make the use of parasitic bipolar transistors unattractive:

1. **area.** Both vertical- and lateral-bipolar transistors use an n-well. Therefore, the achievable packing density is insufficient for use in a column.

2. **input current.** Base current renders the bipolar transistor unsuitable for the column amplifier input devices, because it would discharge the sampled voltage value.

A BiCMOS process would offer smaller, better performance bipolar devices at increased cost. However, the two arguments stated above still hold.

A possible use for bipolar transistors is as driving transistors in the off-chip buffers. As supply voltage is reduced, the size of a MOSFET driver transistor must increase. For example, if the supply voltage of a typical $0.7\mu m$ process is reduced from 3.3V to 2.2V, the driver transistor would have to double in width, whilst the same bipolar transistor could be used.

5.4.1.3 CJFET

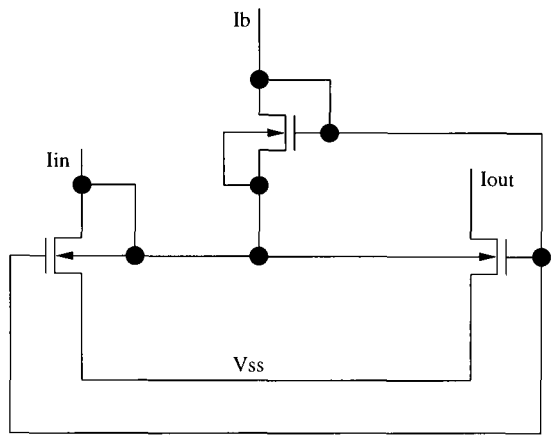


Figure 5.5: *A current mirror using CJFET transistors after Mulder [33].*

A CJFET uses the bulk terminal of a MOSFET transistor as the input node. The MOSFET is biased in the subthreshold region, where the bulk terminal voltage has an exponential influence on drain-source current. Low-voltage operation is achieved, however, the CJFET suffers from a bandwidth four times less than a MOSFET, due to the large input capacitance and resistance [33]. Further problems with the CJFET include: low packing density due to separate wells and limited input range because the substrate leakage current becomes comparable to the input current as the substrate-source diode is forward biased to $0.4V$ [33].

5.4.1.4 Super transistors

A super transistor is a group of transistors that is used to behave as a single transistor with improved characteristics. For example, the Darlington pair is used to increase the current gain of a bipolar transistor [79]. In a low-voltage design, the most common function of a super transistor is to provide increased output resistance, without severely affecting the minimum saturation voltage. The super transistor shown in Figure 5.6 uses the feedback loop $M_4 - M_3 - M_2$ to increase the output resistance of transistor M_1 [34]. Unfortunately, the complex feedback

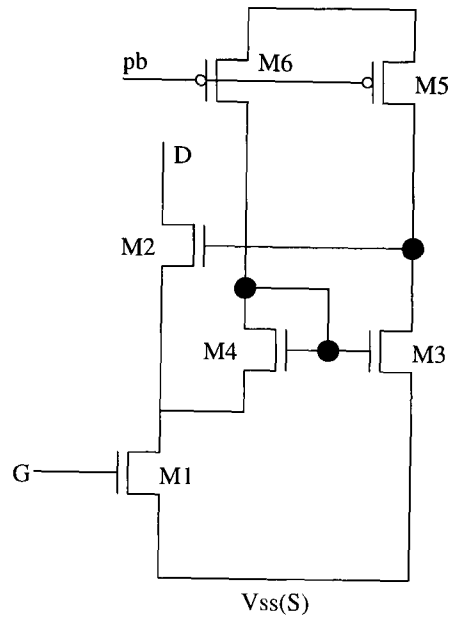


Figure 5.6: *A super transistor after Coban[34].*

structure is difficult to layout within the limited pixel pitch and, therefore, is not suitable for column amplifier design.

5.4.2 Voltage doublers

Voltage doublers are used to generate a supply voltage greater than V_{dd} or less than V_{ss}. The resulting supply can be used to increase the V_{GS} of a critical transistor, for example, the pixel reset transistor or sampling transistors. In order to reduce overall power consumption, the non-critical circuit components are operated at a lower supply voltage.

Figure 5.7 shows the voltage doubler circuit proposed by Favrat [35]. The non-overlapping clocks CK and CKb increase the source potential of transistors M_1 and M_2 respectively. Transmission gates, M_3 and M_4, pass the higher source voltage to the output, V_{out}. The available current is determined by the product of the clock frequency and capacitor sizes. In order to source a few mA drive capability either large capacitors or a high-frequency clock is required. Therefore, external capacitors are often used. The presented circuit achieves a typical efficiency of 80% [35].

There are two fundamental problems with a voltage doubler scheme:

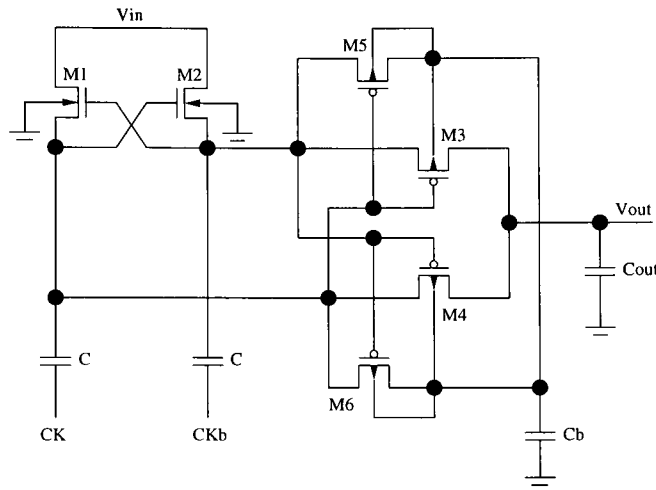


Figure 5.7: *A voltage doubler circuit after Favrat [35].*

1. It is not possible to use a low-voltage process.

2. The inverters and capacitors are either provided off-chip, which increases system power consumption and component count or, if they are integrated on-chip, consume considerable area (for example, in $0.7\mu m$ technology a 2pF capacitor would consume $1000\mu m^2$) and generate digital noise.

5.4.3 Design techniques

In order to maintain the same signal-to-noise ratio, as supply voltage is scaled, noise performance must be improved or the signal swing must be a greater percentage of the supply voltage [115]. If the signal swing is to be increased, standard analogue techniques, such as the cascode and source follower become impractical [51].

In low-voltage design, amplifier output swing is often limited by the saturation voltage, $V_{ds(sat)}$, which is given by

$$V_{ds(sat)} = \sqrt{\frac{2I_{ds}L}{\mu C_{ox}W}} \tag{5.7}$$

There are three methods of reducing the saturation voltage for a given process[51]:

1. **reduce the drain current,** which decreases the maximum slew-rate.

2. **increase the channel width,** which reduces the bandwidth due to increased input capacitance.

3. **decrease the channel length,** which causes greater mismatch, lower output resistance and increases flicker noise.

In practice, the drain-source current is often slew-rate limited and the transistor length is maintained to avoid a reduction in output resistance and, if the circuit is differential, the consequent reduction in the common-mode-rejection ratio. Therefore, the channel width must be increased, or the device must be biased closer to subthreshold operation, which has the advantage of increasing the gain and reducing the thermal noise contribution *per* unit current [56].

5.4.4 Sampling

As discussed in Section 2.2.3 sampling is limited by the available gate-source voltage. At low-voltages, in the middle of the supply voltage, the conductance of an NMOS or PMOS device can be too great to allow an efficient sampling operation. Various schemes have been proposed to overcome this problem, such as [117]:

- low-threshold devices.
- super-supply voltages, for example, generated by a voltage doubler.
- the switched operational amplifier, in which critical switches are eliminated and replaced by opamps with output stages that can be switched off to isolate the output node.

Efficient sampling is critical to the pixel-reset and column-sampling operations, therefore, as supply voltages are reduced, one of the above techniques will have to be employed. For the reset transistor and pixel source follower, a reduced threshold device would be the most attractive option.

5.4.4.1 MOSFET subthreshold operation

If the gate-source voltage is reduced below the threshold voltage, the transistor enters the subthreshold region and the drain-source current is given by Equation 2.24, which is repeated

below

$$I_{DS} = \beta e^{-\frac{V_{T0}}{nU_T}} \left(e^{-\frac{V_s}{U_T}} - e^{-\frac{V_D}{U_T}} \right) \tag{5.8}$$

Advantages of the subthreshold mode of operation include:

- The transistor remains saturated until the drain-source voltage is reduced below $4 \rightarrow 6 \times \frac{kT}{q}$, which is, approximately, $150mV$ at room temperature.
- The maximum transconductance *per* unit current, which results in reduced offset for a differential pair and minimum thermal noise contribution [56].

Unfortunately, the subthreshold mode of operation is not suitable for current mirrors due to the exponential variation in β and, hence, I_{DS} with V_T. In low-voltage design, transistors are often biased on the edge of subthreshold operation, where a suitable simulation tool must be used, such as the EKV model [56].

5.4.4.2 Cascode

At supply voltages of 5V, a cascode transistor is commonly used to increase the output resistance and, hence, gain of stages [56]. Unfortunately, a cascode transistor reduces the output signal range, since the drain-source voltage of each transistor must be larger than the saturation voltage. To provide high gain at low-voltages, a feedback configuration, such as the regulated cascode can be used. Alternatively, further stages must be added to the design. A disadvantage of using a cascade of amplifiers is that each stage adds a dominant pole, reducing the overall bandwidth. Nested Miller compensation can be used to split poles and increase the bandwidth [118].

For a column amplifier, the required bandwidth is normally sufficiently low to allow the use of a cascade of amplifiers, which due to simplicity of layout, is an attractive solution.

5.4.4.3 Complementary input stage

A complimentary input stage uses a parallel combination of both N and P input pairs to achieve rail-to-rail operation. The fundamental design problem is keeping the combined transconductance of the input pair constant. Otherwise, non-optimum compensation is required, the

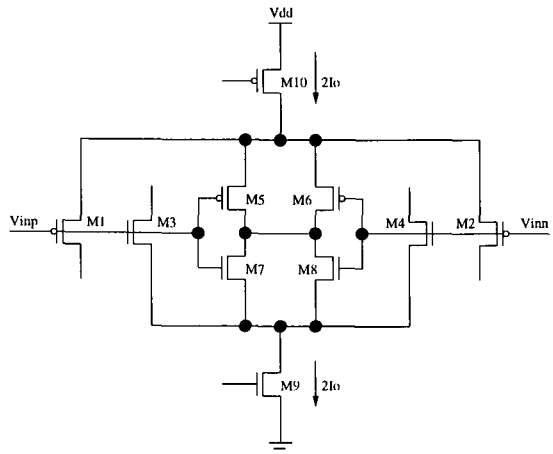


Figure 5.8: *A complimentary input stage after Botma [36].*

common-mode rejection ratio is adversely affected and extra distortion is introduced [33, 34, 36]. There is insufficient room in a single pixel-pitch to layout such an input stage, further, because of the voltage drops associated with the reset transistor and the in-pixel source follower, rail-to-rail input range is not required.

5.5 On-chip integration of signal processing

The on-chip integration of signal processing leads to reduced system-power consumption, system cost and system size and increased reliability. Despite these advantages, only 22% of pressure sensors and 2% of acceleration sensors have significant integrated electronics [119]. Two arguments are commonly given to explain the reticence to integrate signal processing [119]:

1. **Yield loss.** Process yield, $Y(A)$, is modelled by

$$Y(A) = \left(1 + \frac{DA}{\alpha}\right)^{-\alpha} \tag{5.9}$$

where A is chip area, D is the average defect density and α is a process dependent constant, which, typically, lies in the range $0.5 < \alpha < 4$. Equation 5.9 shows that yield decreases with chip size, therefore, yield would be increased and, consequently cost decreased, if separate imaging and processing chips were fabricated. However, the post-fabrication and testing costs dominate fabrication costs, therefore, yield is not a dominant issue, provided that defects can be detected before post-fabrication processing.

2. **Market size.** The more universally applicable a sensor is, the larger the potential market. Therefore, it is attractive to integrate general functions, such as compliance with specific video standards. However, if there is insufficient market to justify an integrated product, unless there are substantial gains in system performance, a hybrid integrated solution utilizing two or more chips is likely to be more attractive than a single-chip solution.

A recent development, which could reduce the development cost associated with the design of on-chip signal processing and increase the number of product derivatives, is system-on-a-chip. Chip designs are becoming increasingly complicated, therefore, common blocks shared between manufacturers, or system-level intellectual property could allow the designer to use a high-level block-based design for chips using standards such as the Virtual Socket Interface [120, 121]. For example, a pixel array could be combined with either an analogue-to-digital converter or a video output block.

5.6 Conclusion

Up to the onset of silicon-on-insulator technology it should be possible to build CMOS imagers on a standard process. Scaling beyond the $0.8\mu m$ technology will improve the achievable pixel fill-factor, mostly because of finer interconnect width. A reduction in vertical distances will lead to a blue-shift in imager spectral response, which must be evaluated experimentally on developed processes. The three consequences of scaling that will prove most problematic are:

1. the reduction in supply voltage. Indeed, if threshold voltages remain constant, it will no longer be possible to operate present active pixel designs on the evolved processes. In order to maximize the achievable voltage swing, it will become important to increase the size of pixel transistors and, thus, reduce process variation. This is more critical as array sizes are increased.

2. the increase in tunnelling and leakage currents, which must remain significantly smaller than the photocurrent.

3. the increased number of metal layers, which must be used across the pixel array without reducing performance.

Summarizing, technology scaling will lead to an improvement in fill-factor rather than a reduction in pixel pitch due to the limitation imposed by current lens technology. Other benefits are likely to be insignificant. Perhaps, the most crucial benefit process evolution could bring to sensor design is low-threshold-voltage devices, however, the industry standard reduction in threshold voltages are not likely to be sufficient. Instead, special low-threshold-voltage transistors are required.

The optical properties of a CCD process should improve over the same time-scale, or if the process is not significantly developed, the price will drop. Consequently, it is likely that the CCD sensor will become more competitive with CMOS sensors manufactured on an industry standard process. Therefore, there will be increasing pressure to develop tailored CMOS processes.

Chapter 6
Analogue-to-digital conversion

6.1 Overview

Market demand for advanced television, multi-media systems, and mobile communication, will drive the state-of-the-art imaging technology. Consequently, there will be an increasing reliance on digital signal processing for video data, accurate transmission, and compression techniques. Further, portable systems require power and weight minimization, therefore, power-efficient analogue-to-digital conversion will become an increasingly important part of an imaging system [122, 123].

This chapter begins by examining the fundamental processes and building blocks required for analogue-to-digital conversion. A discussion of selected converter architectures follows. After a brief description of the operation of an architecture, a power consumption estimate is derived. The power consumption estimates are used to compare the selected architectures for integration on a CMOS image sensor chip. In concluding, this chapter discusses which converter architectures are suitable for on-chip integration at selected converter and image-sensor resolutions.

6.2 Fundamentals of analogue-to-digital conversion

In order to quantize an analogue signal, an analogue-to-digital converter must perform two tasks: reference generation and comparison. Numerous converter architectures have been reported [124], each of which places different requirements on the comparison and reference circuits in terms of speed, accuracy and mismatch. These parameters in turn determine the minimum converter power consumption and area and, hence, whether the architecture is suitable for focal-plane integration [125]. Figures 6.1 and 6.2 show the power consumed and area for chosen converter architectures reported in the literature. Whilst power consumption increases with quantization levels *per* second, area is not clearly correlated with the quantization rate.

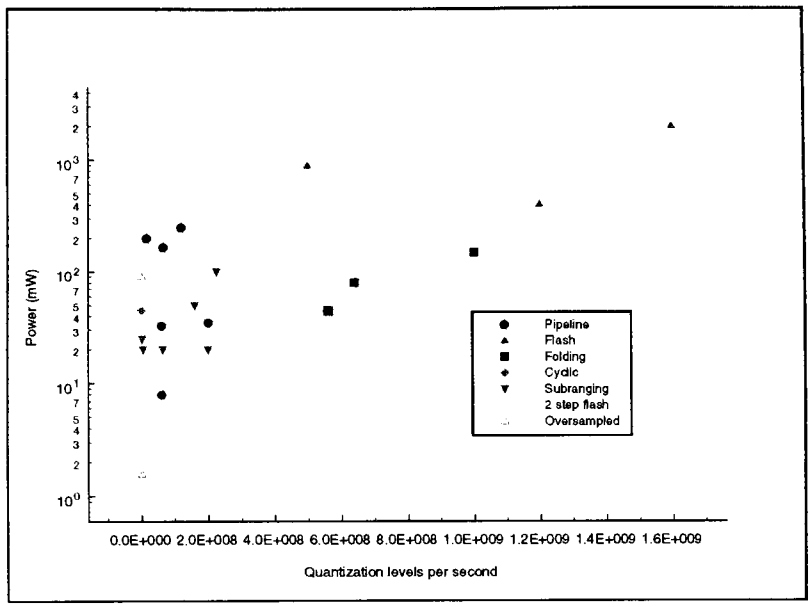


Figure 6.1: *A comparison of power consumption for reported converters.*

A third operation, sampling, is required for a converter integrated with an area image sensor. The remainder of this section discusses the fundamental converter processes and building blocks

6.2.1 Quantization

An analogue-to-digital converter maps a continuous signal onto a finite set of values. Consequently, an error term, e, called quantization noise, is added to the digital representation, $q(x)$, of the analogue signal, x, so that

$$e = q(x) - x \tag{6.1}$$

For a converter with quantization step, Δ, assuming that the error probability distribution function, E_n, is uniform such that $-\frac{\Delta}{2} < e < \frac{\Delta}{2}$, the noise power of a quantizer, σ_E^2, is given by

$$\sigma_E^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12} \tag{6.2}$$

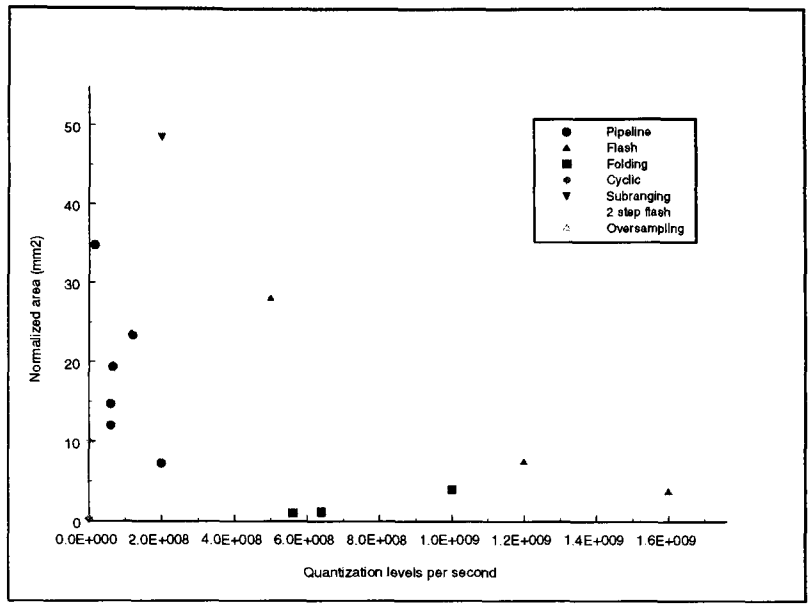


Figure 6.2: *A comparison of area for reported converters.*

6.2.2 Sampling

Sampling introduces thermal, or $\frac{kT}{C}$, noise to the input signal. The thermal and quantization noise sources limit the signal-to-noise ratio of an ideal converter, SNR_{max}, which is given by

$$SNR_{max} = 10 \log \left(\frac{R^2}{\frac{2kT}{C} + \frac{1}{12}(\frac{R}{2^N})^2} \right) \tag{6.3}$$

where R is the input range of the converter, and it is assumed that the converted signal is the difference of two sampled values. Equation 6.3 implies and Figure 6.3 shows that, if the sampling capacitance is increased, $\frac{kT}{C}$ noise is reduced. Eventually, quantization noise dominates introduced $\frac{kT}{C}$ noise and the signal-to-noise ratio reaches a saturation value.

Ideally a sampling capacitor size would be chosen to maximize the signal-to-noise ratio. However the consequent increase in current to charge the sampling capacitor forces a compromise between power consumption and signal-to-noise ratio. A capacitance, C, such that $C > 3kT2^{2N+3}$ limits the thermal noise contribution to be equal to the quantization noise. For example, at 6- and 12-bit resolution a $0.4fF$ and $1.7pF$ capacitance is required respectively.

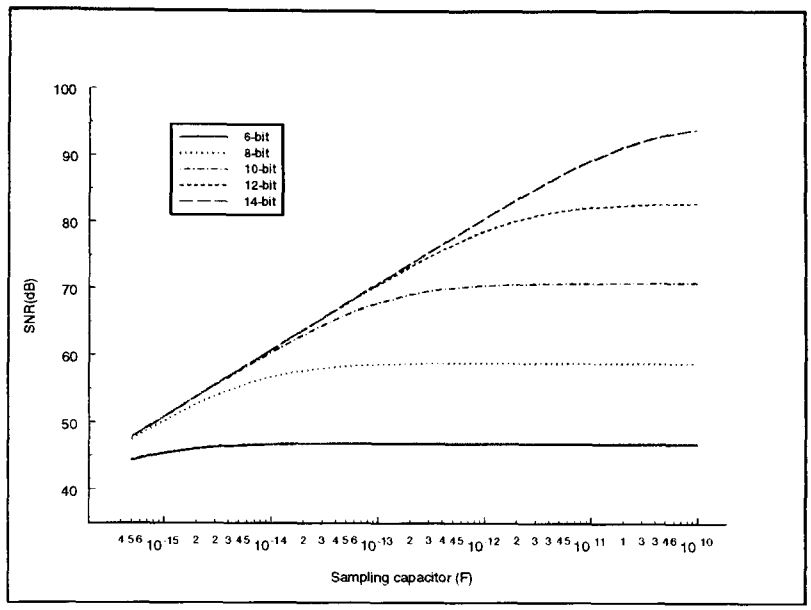


Figure 6.3: *The ideal signal-to-noise ratio for a N-bit, 1V input range, converter.*

6.2.2.1 Power consumption

In a voltage readout image sensor, the column current, I_{col}, must be sufficient to charge the sampling capacitance, C_{sample}, and the parasitic column capacitance, C_{col}, within a fraction of the row time. If the maximum column voltage swing is ΔV, the minimum value of the column current is given by

$$I_{col} = (C_{sample} + C_{col})\frac{nf}{\eta}\Delta V \tag{6.4}$$

where n is the number of rows in the sensor array; f is the frame rate and η is the fraction of the row time allowed for sampling and it is assumed that the column current is slew-rate limited. The maximum settling time, ηt_{row}, is dependent on the column readout structure. For example, if a readout structure is multiplexed between columns, the settling time will decrease.

Interpretation of Figure 2.14, which is repeated as Figure 6.4 for ease of reference, reveals that the minimum column current is slew-rate, rather than bandwidth limited and that an increase in settling time from 1 to 45% of the row time yields a power saving of 98%. A further increase in sampling time is not possible because it is assumed that correlated-double sampling is used,

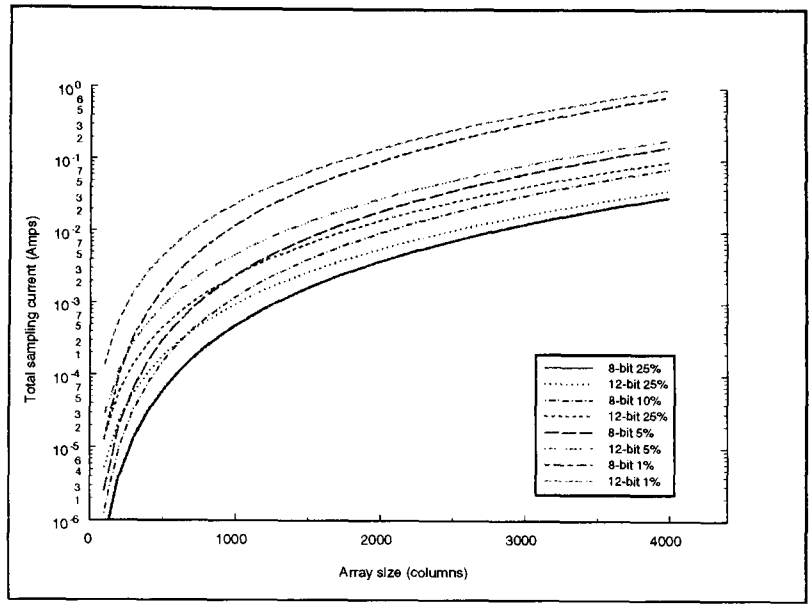


Figure 6.4: *The minimum required column current as a function of η, for an $n \times n$ array at 8- and 12-bit resolution.*

limiting the maximum settling time to less than 50% of the row time.

In order to maximize the settling time and, consequently, minimize the sampling power consumption, two sets of sampling capacitors can be used alternatively. This architecture introduces a row-time delay to the output data, but doubles the available sampling and conversion time leading to a power saving of at least 50%.

Equation 6.4 states that the minimum column bias current increases super-linearly with n, because the parasitic column capacitance increases linearly with n and the sampling time is inversely proportional to n. Consequently, as the array size increases, the in-pixel source-follower width must increase or the gate-source voltage dropped across it must increase. Assuming that the gate-source voltage remains constant at $0.1V$, the required gate-width for a minimum length device in a $0.5\mu m$ technology, is shown in Figure 6.5. If 20% of the row time is available for sampling, a small increase in the minimum size device can conduct sufficient column current. However, if 1 to 5 % of the row time is reserved for sampling, the source follower must increase in size. For example, an 8-bit converter integrated on a 1000×1000 image sensor with 1% of the row time used for sampling requires a source-follower with $\frac{W}{L} = 10$. Conversely, if 45% of

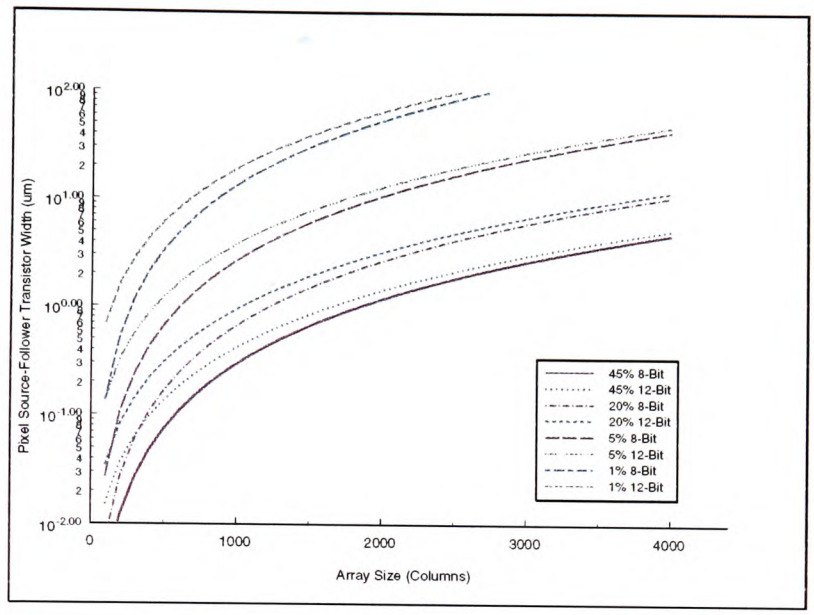


Figure 6.5: *The minimum in-pixel source-follower width for a given array size and converter resolution.*

the row-time is used for sampling, the source-follower transistor should be sized so that $\frac{W}{L} < 1$.

6.2.3 Reference generation

The selection of reference generator depends upon the converter architecture and resolution and the matching properties of the process. There are two generic types of reference: the resistor ladder and capacitor array. Without trimming or excessive area requirements, the accuracy of both reference generators is limited to between 8- and 9-bits [123].

6.2.3.1 Resistance ladder

A series of matched resistances, connected between two reference voltages, divide the input range into, ideally, equal voltage steps. Power consumption depends on the total resistance value and the parasitic capacitance that must be charged through the ladder. The total resistance value is determined by the resistance type, matching requirements and available area [56].

If the reference voltages are sampled, parasitic capacitance is charged through the reference

ladder. In order to achieve settling to N-Bit accuracy, the minimum current, I_{ref} for a given clock frequency, f_{ck}, is given by

$$I_{ref} = (V_{ref(max)} - V_{ref(min)}) \times \frac{f_{ck} C_p N \ln(2)}{4} \tag{6.5}$$

where C_p is the parasitic capacitance that must be charged [125].

6.2.3.2 Capacitor array

The unit capacitor size for a capacitor array is limited by $\frac{kT}{C}$ noise. Consequently, the minimum reference current is given by [125]

$$I_{ref} = \frac{12kT2^{2N} f_{ck}}{V_{ref(max)} - V_{ref(min)}} \tag{6.6}$$

6.3 Comparator limits

Comparator design is crucial to the achievable converter performance. The following comparator design parameters limit converter performance: delay, minimum detectable input voltage, input voltage range, input capacitance and offset. Two additional parameters — power consumption and area — are critical for integrated converters. Area constraints will affect the

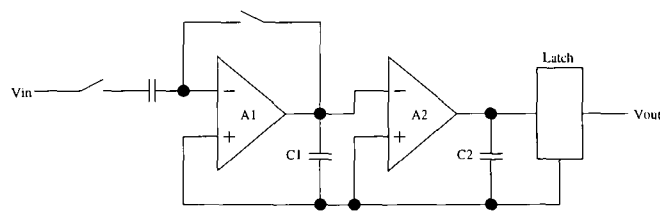


Figure 6.6: *A comparator cascade.*

chosen converter architecture and determine the number of parallel converters that can be integrated on-chip, which in turn defines the necessary comparator throughput. Once the maximum settling time is known, it is possible to estimate the minimum bias current that enables the comparator to amplify the minimum input signal to the desired output level within the given time.

A comparator can be either bandwidth or slew-rate limited, depending on the output capacit-

ance, decision time and gain. For a single-stage comparator, assuming that the input transistors operate in the saturation region and obey the square-law, the minimum bias current, I_{bias}, is given by

$$I_{bias} = \begin{cases} \frac{C_L \Delta V_{out}}{T_{dec}} & \text{if } V_{in(min)}^2 T_{dec} > 2\beta C_L \Delta V_{out} \textit{ i.e.} \text{ slew-rate limited} \\ \frac{1}{2\beta} \times \left(\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}} \right)^2 & \text{otherwise, } \textit{i.e.} \text{ bandwidth limited} \end{cases} \tag{6.7}$$

Quiescent current can be eliminated if a dynamic cross-coupled comparator, or latch, is used. However, the input offset of about 100mV is unsuitable for most converter architectures [125]. A pre-amplifier can be used to reduce the latch offset by the pre-amplifier gain. The total bias current is reduced because the dynamic comparator is used to generate CMOS logic levels, therefore, the pre-amplifier need only amplify the input signal to a level greater than the dynamic comparator offset.

If the comparator is bandwidth limited, further power savings can be realized using a cascade of comparators, as shown in Figure 6.6. For example, a three-stage comparator yields a current saving of a factor of 100 over a single stage [126]. However, if the comparator bias current is slew-rate limited, the minimum bias current is obtained for a single-stage comparator.

6.4 Amplifier limits

The design constraints of an operational amplifier are similar to those of a comparator, namely, the amplifier must provide sufficient gain and the output voltage must change within a given time. If the amplifier is used in a feedback configuration the required gain and bandwidth are altered.

Consider a single-pole amplifier with low-frequency gain A_o and bandwidth, ω_p, the transient response is given by

$$V_{out} = \beta \times \left(1 - e^{-\frac{t}{\omega_p f_b}}\right) \times \left(\frac{1}{1 + \frac{1}{A_o f_b}}\right) \tag{6.8}$$

where f_b is the feedback factor, which is defined as the ratio of the feedback capacitance to the total capacitance seen at the input node [125]. Equation 6.8 shows that the final settling voltage, and the rate at which the amplifier output asymptotically approaches it, is governed

by the feedback factor, which by definition is less than unity. Therefore, the required amplifier bandwidth is reduced, whilst the minimum gain is increased. In order to settle to $\frac{1}{4}$-LSB, the required gain is given by

$$A_o > \frac{2^{N+2}}{f_b} \tag{6.9}$$

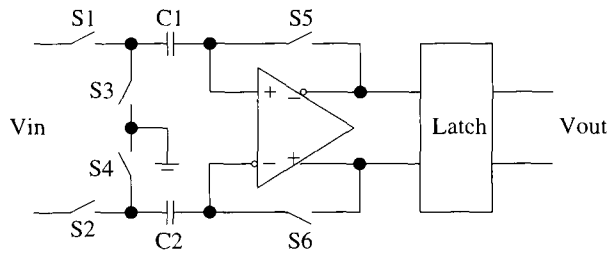
and the minimum bandwidth is given by

$$\omega_p > \frac{(N+2)f_b \ln(2)}{T_{settle}} \tag{6.10}$$

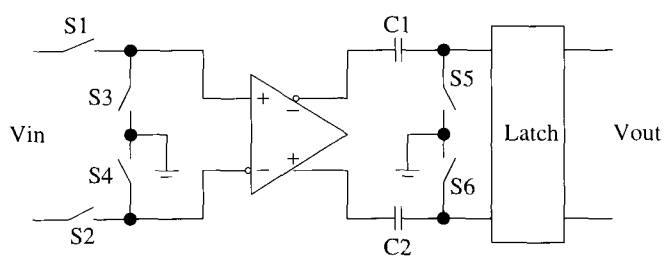
where T_{settle} is the maximum amplifier settling time.

6.4.1 Offset cancelling

On average, a 1000-column image sensor will have three columns amplifiers with an offset greater than 3 standard deviations and forty-six columns with an offset greater than 2 standard deviations. Therefore, for an offset standard deviation of 1mV, 3 columns will have an offset greater than 3mV, which is equivalent to a maximum resolution of 8-bits with a 1V input range. In order to increase the achievable resolution, there are two common methods of offset reduc-



(a) Input offset storage



(b) Output offset storage

Figure 6.7: *Comparator offset cancellation techniques.*

tion: input offset storage (IOS) and output offset storage (OOS). The residual offset for IOS is given by

$$V_{os} = \frac{V_{os1}}{1 + A_o} + \frac{\Delta Q}{C} + \frac{V_{osL}}{A_o} \tag{6.11}$$

and for OOS by

$$V_{os} = \frac{\Delta Q}{A_o C} + \frac{V_{osL}}{A_o} \tag{6.12}$$

where V_{os1} and A_o are the offset and gain of the pre-amplifier; ΔQ is the mismatch in charge injection from switches S_5 and S_6 onto C_1 and C_2 and V_{osL} is the latch offset. Equations 6.11 and 6.12 show that the residual offset can be made smaller using OOS than IOS. However, under OOS, the gain of the amplifier is limited so that the output is not saturated by the effective input signal due to the offset voltage [127].

6.5 A comparison of on-chip versus off-chip converters

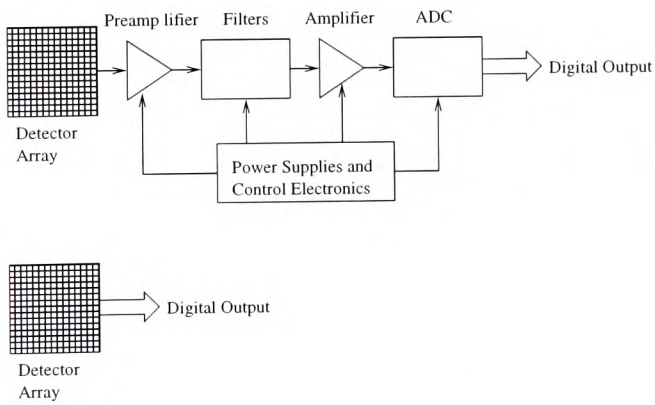


Figure 6.8: *System signal chain with off-chip ADC and on-chip ADC.*

A comparison of system complexity, associated with on- and off-chip conversion, is shown in Figure 6.8. Integration of an on-chip converter leads to an improvement in system power consumption, a reduction in noise introduced whilst transmitting analogue signals off the focal plane and a decrease in system cost and design time[48, 128]. Further, off-chip conversion must be performed at the pixel rate, leading to the maximum introduction of white-noise and an increase in digital noise [129]. However, the improvement in system performance must be balanced against the increase in image-sensor chip power consumption. Figure 6.9 shows that

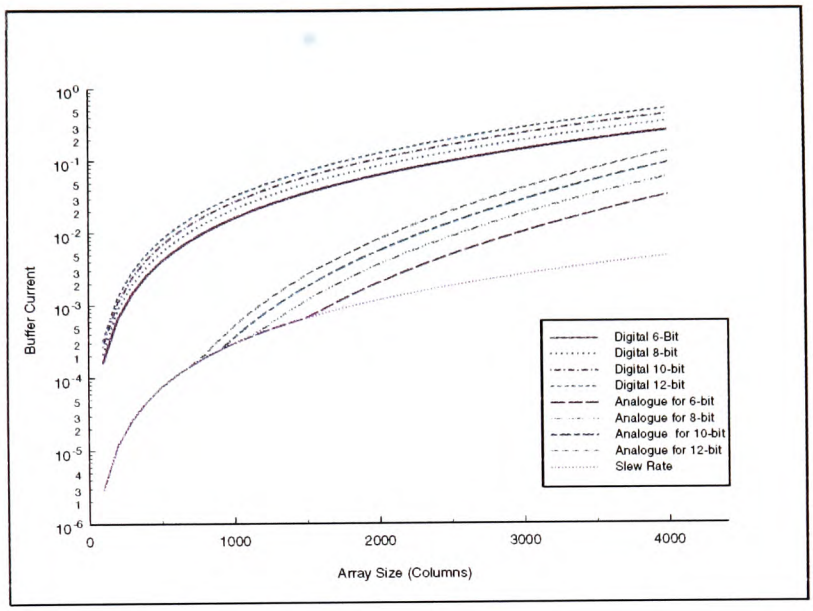


Figure 6.9: *A comparison of the current required to drive an N-bit digital signal off-chip and an analogue signal off-chip to converter off-chip to N-bit resolution.*

the minimum current required to drive an analogue signal off-chip for quantization is more than an order of magnitude less than that to drive the equivalent digital signal off chip. Further to the advantage of off-chip conversion, the buffer current and converter will contribute to digital noise, which may cause crosstalk, disturbing sensitive analogue circuits and, hence, reducing the achievable converter resolution.

On-chip conversion increases chip size, adversely affecting chip yield. A further disadvantage of on-chip conversion is that a specialized sensor and converter process can not be used, for example, the image-sensor can be fabricated using a CCD process and the converter in a high-speed BiCMOS process. Off-chip conversion can also benefit from the converters and signal-processing available for CCD systems.

The choice of on- or off-chip conversion is dependent upon the system application, for example, if power consumption is not a critical design parameter an off-chip solution becomes more attractive. Perhaps more importantly, the signal-processing required can affect the choice of conversion method. For example, the delay introduced by buffering data on- and off-chip may be unacceptable for a motion detection algorithm, which updates a region of interest every

frame [123].

Concluding, the choice between on- and off-chip conversion is not a theoretical one. Experiments must be performed to quantify the contamination introduced to the signal-chain in both strategies. However, if on-chip conversion is a possibility, power efficiency and the reduction of crosstalk are critical issues. The power-consumption of selected converter architectures is considered in the remainder of this chapter, crosstalk and methods of isolation are discussed in Appendix E.

6.6 On-chip conversion

There are three different approaches to on-chip conversion:

- A single converter *per* chip.
- A semi-parallel approach, where a converter is shared between m columns, where $1 \leq m < n$ where n is the number of pixel columns.
- A parallel approach, where a converter is integrated at each pixel site.

The optimum converter strategy is dependent upon the relative importance of the design parameters listed below:

- If an analogue circuit is bandwidth limited, **power consumption** increases super-linearly with data throughput. Consequently, increasing the number of parallel signal paths reduces the total power consumption. Conversely, if the circuit is slew-rate limited the power consumption is independent of the number of parallel signal paths.
- **Design space**, which is relatively unconstrained for a single converter, becomes limited in one-dimension with a semi-parallel approach and the major design issue in a *per* pixel converter. A compromise between a single converter and a converter *per* column is to multiplex the converter between m columns. The choice of m reflects the converter architecture and resolution. An increase in m will allow improved analogue performance in terms of matching and output resistance at the expense of increased throughput and, possibly, power consumption.

- **Fixed-pattern noise** is introduced when converters are used in parallel. In order to be viable for viewed images, the introduced noise must be suppressed below 0.1%, this is critical in a semi-parallel approach because the eye is more sensitive to column-to-column than pixel-to-pixel fixed-pattern noise.
- **Trimming** is only viable for a single converter, but should be avoided due to the increase in cost.
- **The routing and number of signals** becomes critical in a parallel approach. Additional signals required for a *per* pixel converter reduce the pixel fill-factor and increase the capacitive coupling between signals on the focal plane.
- **Focal plane power consumption** causes an elevated pixel ambient temperature, which increases the thermal dark current and, hence, reduces the signal-to-noise ratio.
- **Analogue signal communication** is susceptible to noise due to capacitive coupling, and thermal noise introduced by wide-bandwidth buffers. Communication in the digital domain, conversely, is relatively robust, but can increase power-consumption and generate noise, which can couple to sensitive analogue circuit blocks. The proportion of digital to analogue communication is increased as converter parallelism is increased.

6.7 Parallel or pixel-level conversion

The major design-issue preventing pixel-level conversion is the consequent reduction in fill-factor and increase in pixel pitch, which makes this approach unattractive for viewed image sensors. In order to mitigate the increase in fill-factor, the converter should minimize the required number of signals and bits of memory required *in situ*. Perhaps, the only feasible parallel converter has been designed by Fowler and Yang [48, 130] using an in-pixel sigma-delta modulator, and off-chip decimation. The pixel block diagram for which is shown in Figure 6.10 and the schematic in Figure 6.11. The sensor was fabricated in a $0.8\mu m$ CMOS process. Integration of 19 MOS transistors at the pixel increased the pixel pitch from the state-of-the-art, for the given technology, $12\mu m$ to $30\mu m$. Synchronous system operation eliminated the need for pixel-site memory; after each clock pulse every pixel produces one bit of data, the data from the array forms a bit-plane, L of which are required to produce a single frame, where L is given

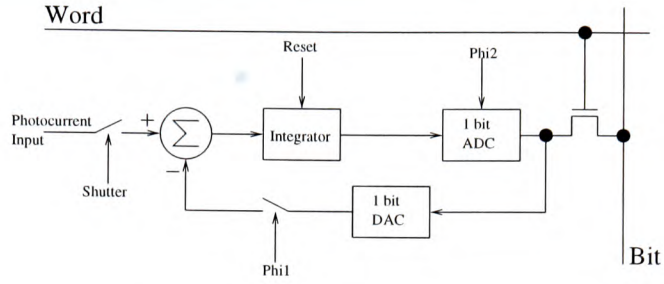


Figure 6.10: *A $\Sigma - \Delta$ ADC pixel block.*

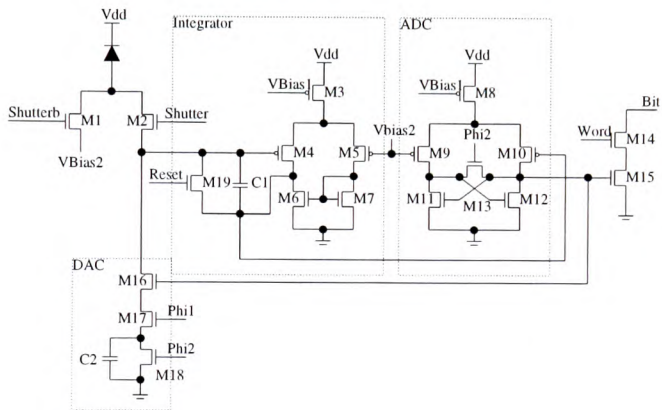


Figure 6.11: *A pixel-level $\Sigma - \Delta$ ADC schematic.*

by

$$L = 2^{\frac{SNR-5.2dB}{9}} \tag{6.13}$$

where SNR is the required signal-to-noise ratio [48]. Fixed-pattern noise is limited by the DAC matching to about 1%. In order to improve the fill-factor, a quantizer and DAC were multiplexed between four pixels, yielding a pixel size of $11 \times 11\mu m^2$, and a fill-factor of 30% in a $0.5\mu m$ process. If fixed-pattern noise was reduced by an order of magnitude and decimation was carried out on-chip, pixel-level sigma-delta modulation would be a possible conversion architecture for imagers.

6.8 Semi-parallel and serial converter strategies

Semi-parallel and serial converters are considered together because the same converter architectures are possible for each of them. The remainder of this chapter discusses the basic operation of selected converters, before deriving an estimate for power consumption; discussing matching requirements, examples of previously fabricated converters and finally concluding by suggesting which converter architectures are most suitable for on-chip integration.

In order to simplify the discussion, the following assumptions are made:

1. The pixel array is square, containing $n \times n$ pixels, where $100 \leq n \leq 4000$.
2. Conversion is to N-bits, where $6 \leq N \leq 12$.
3. The input range is $1V$.
4. The frame rate is 30 frames *per* second.
5. For ease of layout, m is limited so that a maximum of two comparators are integrated *per* column.
6. Memory power consumption is not considered because the integrated on-chip digital-signal processing will determine the required memory depth, and, hence, memory power consumption. However, a serial converter is likely to require less memory than a parallel approach.
7. Digital power consumption is not considered, because it is hard to quantify. However, there may be considerable variation in the digital processing required, for example, a single-slope converter outputs a digital word, whilst a flash converter outputs a thermometer code, which must be bubble corrected before conversion to a binary word.
8. Auto-zeroing is not considered, therefore, there is likely to be a factor-of-two increase in comparator bias current for high-resolution converters if comparator offset is critical.
9. A row time is used for sampling, followed by a row time for conversion; this provides a lower bound for power consumption since the sampling and conversion time are maximized. Further, the assumption avoids the need to optimize the relative sampling and conversion time for each architecture.

6.9 The flash converter

6.9.1 Operation

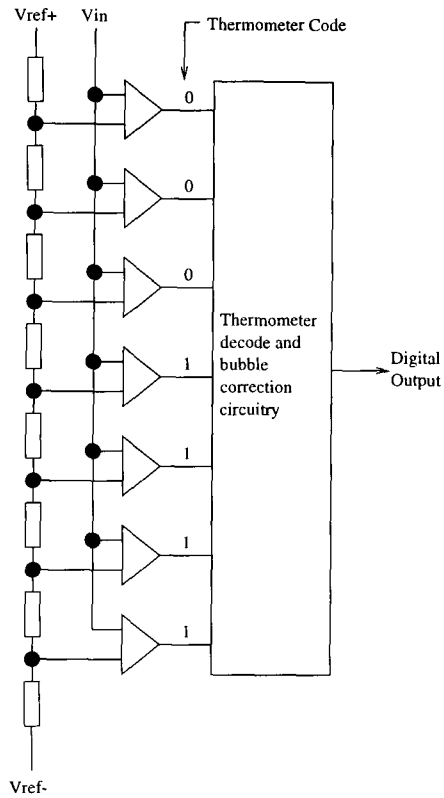


Figure 6.12: *A 3-bit flash converter.*

The flash converter uses a brute-force approach to perform conversion in a single clock period. Figure 6.12 shows the operation of a basic flash converter: an input signal is simultaneously compared to 2^N reference voltages using 2^N comparators. A thermometer code is output from the comparator bank, which must then be converted to binary data. Flash converters are most suitable for low-resolution converters because power consumption, area and input capacitance increase exponentially with resolution.

Semi-parallel integration on an imaging array is limited by the area requirement. A sensible limit to integration is two comparators *per* column, which allows a full column pitch for layout, if alternate converters are placed at opposite ends of the pixel array. Therefore, the minimum number of columns that a 6- and 12-bit converter is multiplexed between is 32 and 512 columns, respectively.

6.9.2 Power consumption

Two cases are considered, a serial converter and a semi-parallel converter, which is multiplexed between the minimum number of columns for the given resolution. Estimates for the current required to charge the converter input capacitance, generate a reference and bias the comparators are derived. This section concludes by considering how non-idealities affect the integration of a flash converter with an image sensor and whether a serial or semi-parallel converter is most appropriate.

6.9.2.1 Reference generation

Power consumption is calculated assuming that a common resistor ladder generates reference voltages for the entire array. In practice, because of the required number of signal lines, it may be easier to provide a separate reference for each converter, however, this would introduce a further source of fixed-pattern noise.

If auto-zeroing is not applied, the comparator inputs remain fixed to the resistor ladder, therefore, after initial setup, capacitance is not charged through the ladder. Consequently, the resistor value can be optimized to improve matching and reduce current consumption without the need to realize a given time constant. For example, if a unit resistor value of R is chosen as a compromise between area, power consumption and matching, the reference current, I_{ref} is given by

$$I_{ref} = \frac{V_{ref}}{R \times 2^N} \tag{6.14}$$

where R is, typically $1k\Omega$. Equation 6.14 shows that the reference current is independent of the array size and decreases with increase in resolution. However, in practice, a total resistance can be chosen to make the reference current insignificant at any resolution.

6.9.2.2 Input capacitance

Each sampled pixel value must be multiplexed to the converter in turn. A passive charge-sharing scheme would introduce a significant reduction in input signal, because of the large input capacitance. Therefore, a buffer must be used. The minimum value of current required is

determined by the buffer slew-rate and is given by

$$I = C\frac{\Delta V}{\Delta t} = \frac{n}{m} \times 2^N C_{in} \times \frac{nfm\Delta V}{\eta} = \frac{n^2 f 2^N C_{in}(N)\Delta V}{\eta} \tag{6.15}$$

where η is the proportion of the clock period that is allowed for charging the input capacitance. Note that, in order to reduce the comparator offset voltage, transistor area and, consequently, the input capacitance, $C_{in}(N)$, will increase with N.

6.9.2.3 Comparator

A total of 2^N comparators are required for each of the $\frac{n}{m}$ converters, therefore, provided that the comparator performance is not slew-rate limited, the total comparator current, I_{bw}, is given by

$$I_{bw} = \frac{n}{m} \times 2^N \times \frac{1}{2\beta}\left(\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}}\right)^2 = \frac{n}{m} \times 2^N \times \frac{1}{2\beta}\left(\frac{C_L \Delta V_{out}}{\frac{\eta}{nfm} \times \frac{1}{2^{N+1}}}\right)^2 \tag{6.16}$$

Rearranging Equation 6.16 yields

$$I_{bw} = \frac{n^3 f^2 m 2^{3N+1}}{\beta} \times \left(\frac{C_L \Delta V_{out}}{\eta}\right)^2 \tag{6.17}$$

If the comparator is slew-rate limited, the total current, I_{sr}, is given by

$$I_{sr} = \frac{n}{m} \times 2^N \times \frac{C_L \Delta V_{out}}{T_{dec}} = n^2 f 2^N \times \frac{C_L \Delta V_{out}}{\eta} \tag{6.18}$$

Considering Equations 6.17 and 6.18 shows that as the array size and resolution is increased the minimum comparator current will be dominated by the bandwidth limit given in Equation 6.17. If a single converter is used, *i.e.* when $m = n$, the total current increases with n^4, rather than n^3 when parallel converters are used. Therefore, as array size is increased, it becomes increasingly beneficial to use $\frac{n}{m}$ converters in parallel. Conversely, if the comparator is slew-rate limited, the comparator bias current is independent of m.

6.9.2.4 A discussion of power consumption for the flash converter

The estimates for power consumption derived in Equations 6.14 to 6.18 are used to plot the total power consumption for 6-, 8-, and 10-bit resolution; semi-parallel and serial converters

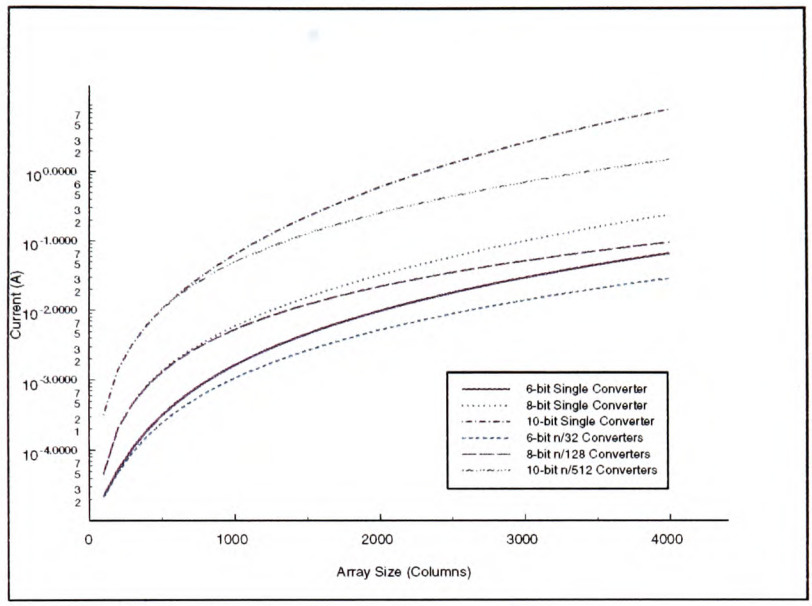


Figure 6.13: *A comparison of total bias current for flash converters at 6-,8-, and 10-Bit resolution using a semi-parallel and serial approach.*

in Figure 6.13. Power consumption increases more significantly between 8- and 10-bit than 6- and 8-bit resolution because, as shown in Figure 6.15, the comparator current, which varies with 2^{3N+1}, is dominant at 10-bit resolution, whilst sampling and input-capacitance-charging current dominates at lower resolutions.

Power consumption is not critical in choosing between a serial and semi-parallel approach for a 6-bit resolution converter for array sizes below 3000×3000. The relatively small saving in bias current, shown in Figure 6.14, is realized because the comparator is slew-rate limited and, therefore, identical for a serial or semi-parallel approach. A design choice, between a semi-parallel and serial approach, can be determined by area, introduced fixed-pattern noise and the noise introduced by capacitive coupling whilst buffering the analogue signal from a column to the serial converter. With careful design, at 6-bit resolution, the coupled noise and introduced fixed-pattern noise should be less than the random noise level, therefore, a serial approach is more attractive. At 10-bit resolution, power consumption is the critical issue. Further, the estimates shown in 6.15 are conservative because an auto-zeroing phase is not included in the calculation. Therefore, with the possible exception of a single 10-bit converter, for an array size of about 500×500, the integration of a 10-bit flash converter is impractical due to excessive

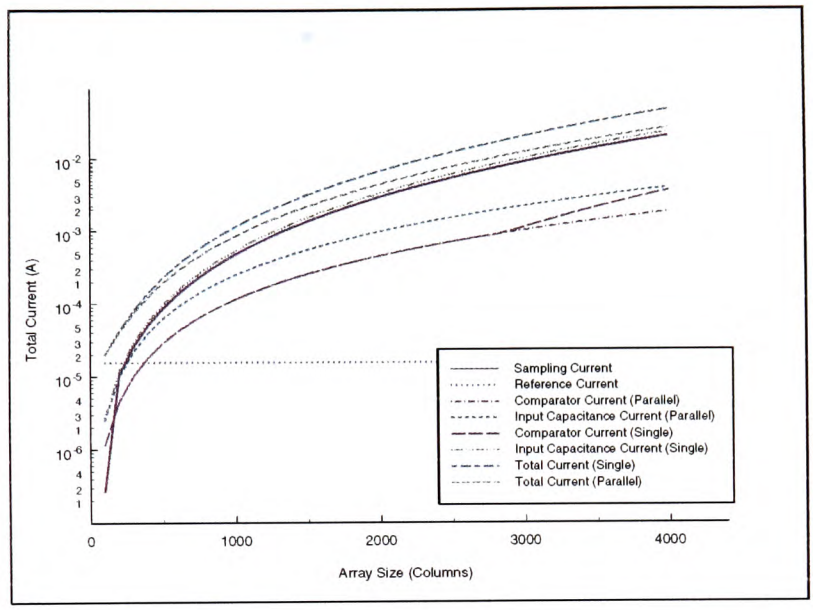


Figure 6.14: *The total comparator, reference and input capacitance bias currents required for a serial and semi-parallel, 6-bit flash converter. Note that as the array size is increased above* 3000×3000 *pixels, the comparator bias current is no longer slew-rate limited. This can be seen clearly as a change in gradient of the comparator bias current.*

power consumption.

6.9.3 Mismatch and offset

Equation 6.17 states that as array size and resolution is increased, a comparator gain must increase, whilst the decision time is reduced. A further limit to comparator performance is that the input offset must be less than a single LSB. Hence, the comparator limits the resolution and throughput of a flash converter. If comparator offset is greater than $\frac{1}{2}$-LSB, or a comparator is not functional, so-called bubbles can appear in the thermometer code. Bubbles result in two or more 1-0 transitions in the comparator output, therefore, to obtain a meaningful output, digital correction is required [131, 132].

The resistor reference ladder introduces non-linearity to the converter transfer function because of the mismatch between unit resistance values. Consequently, multiple reference ladders introduce fixed-pattern noise. A common reference ladder, however, requires 2^N analogue signal

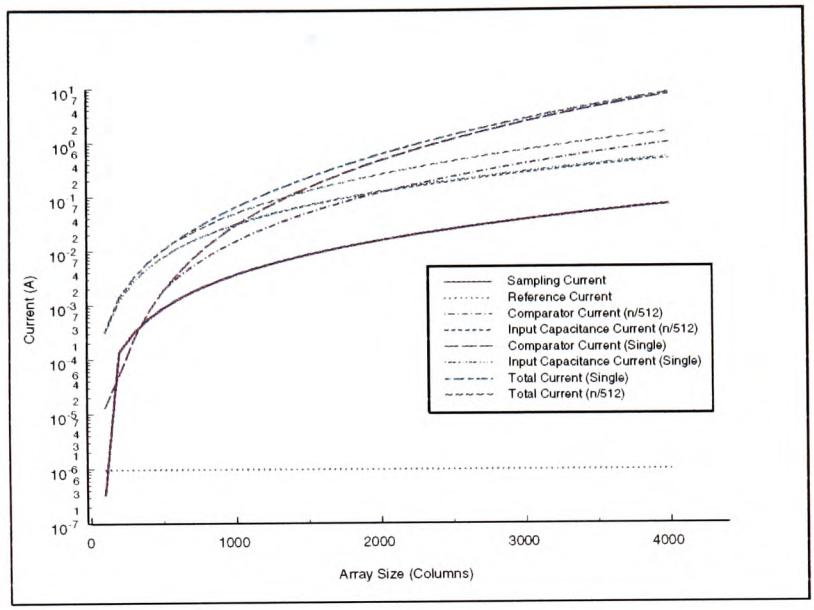


Figure 6.15: *The total, comparator, reference and input capacitance bias currents required for a serial and semi-parallel, 10-bit flash converter.*

wires. Therefore, practically, a reference ladder is required for each converter and the maximum introduced fixed-pattern noise must be less than 1-LSB.

6.10 Two-stage flash conversion

6.10.1 Operation

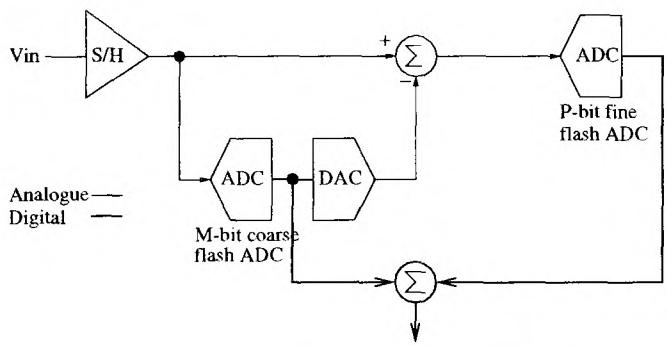


Figure 6.16: *A two-stage flash converter.*

Discussion of the flash converter showed that at 10-bit resolution, power consumption was dominated by the 2^N comparators. Several techniques have been proposed to reduce the required number of comparators:

- Coarse and fine conversion is performed in consecutive clock periods. As shown in Figure 6.16, a M-bit flash converter determines the M-most significant bits, and a DAC is used to subtract the quantized signal from the input signal. A second P-bit converter is used to determine the least significant bits from the residue [131]. Assuming that a single row time is used for conversion, both comparator banks must meet the same offset and gain criteria as a full-flash converter, whilst the decision time is halved. Therefore, the power consumption *per* comparator is greater than in a flash architecture, but the total power consumption and area is reduced.

- A further reduction in power, at the expense of data latency, can be achieved if the output of the coarse conversion is sampled and two row-times are used for the conversion [125].

- If interstage gain is used, the settling requirements of the fine comparator bank are relaxed, because the minimum over-drive signal is increased. Further, this technique can be used to achieve up to 14-bit resolution [127].

- An alternative technique is to process the fine and coarse conversions in parallel using a folding technique. Figure 6.17 shows the principle of a folding converter: a folding circuit is used to subtract the unknown most significant bits from the input signal, the fine conversion is performed on the output from the folding circuit in parallel to the coarse conversion. If the power consumed by an ideal folding circuit is ignored, the reduction in bias current is identical to the 2-stage flash conversion with inter-stage sampling [133, 134]. However, the delay introduced by the folding circuit reduces the maximum settling time for the fine converter stage, increasing the power consumption. Further, the folding stage will consume significant power and introduce fixed-pattern noise in a semi-parallel converter. Therefore, the use of inter-stage sampling is optimum for a two-stage flash converter.

There are two additional advantages of a two-step architecture over a full flash converter:

- Reduced input capacitance, which yields a further power saving.

- The two-step converter can be multiplexed between fewer columns, therefore, the comparator settling time can be increased. For example, if a comparator from each bank is laid out in a single column, a 10-bit converter is shared between 32 columns, rather than 512 for a full flash converter.

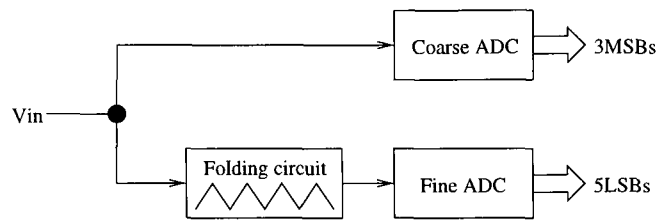


Figure 6.17: *A block diagram of a folding ADC.*

6.10.2 Power consumption

Power consumption is calculated assuming that $M = P = \frac{N}{2}$ and that a simple two-stage flash converter architecture is used, without interstage gain or sampling.

6.10.2.1 Reference generation

The input reference for the first stage remains fixed, however, the result from the first stage is used to determine which portion of the resistor ladder is used to provide the second stage reference voltages. Consequently, the minimum current is determined by the time taken to charge the input capacitance of the fine converter bank through the resistor ladder. A worst case estimate for the minimum reference current, I_{ref} is given by

$$I_{ref} = \frac{f_{ck} V_{ref} C_p N \ln(2)}{4} = \frac{\frac{n}{m} \times \frac{mnf}{\eta} V_{ref} 2^{\frac{N}{2}} C_{in}(N) \times N \ln(2)}{4} \tag{6.19}$$

rearranging yields

$$I_{ref} = \frac{n^2 f}{\eta} V_{ref} 2^{\frac{N}{2}-2} N \ln(2) C_{in}(N) \tag{6.20}$$

6.10.2.2 Input capacitance

The current required to charge the input capacitance of the two banks of comparators is given by,

$$I = 2 \times \frac{n}{m} \times 2^{\frac{N}{2}} C_{in}(N) \Delta V \times \frac{2nfm}{\eta} = 2^{\frac{N}{2}+2} \frac{n^2 f}{\eta} C_{in}(N) \Delta V \tag{6.21}$$

where η is the proportion of the clock period used to charge both banks of input capacitance.

6.10.2.3 Comparators

Assuming that the comparator banks are bandwidth limited, the minimum bias current is given by

$$I = \frac{n}{m} \times 2 \times \frac{2^{\frac{N}{2}}}{2\beta} \times (\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}})^2 = \frac{n}{m} \times 2 \times \frac{2^{\frac{N}{2}}}{2\beta} \times (C_L \Delta V_{out} \times \frac{2nfm}{\eta} \times 2^{N+1})^2 \tag{6.22}$$

rearranging yields,

$$I = 2^{\frac{5N+8}{2}} \times \frac{n^3 m f^2}{\beta} \times \left(\frac{C_L \Delta V_{out}}{\eta}\right)^2 \tag{6.23}$$

Like the flash converter, at low resolution or small array sizes, the comparator current is slew-rate, rather than bandwidth, limited. Under these conditions, the minimum bias current is given by

$$I = \frac{n}{m} \times 2 \times 2^{\frac{N}{2}} C_L \times \frac{V_{out}}{\frac{\eta}{2nfm}} = 2^{\frac{N+4}{2}} \times \frac{n^2 f C_L V_{out}}{\eta} \tag{6.24}$$

The reduction in comparator bias current achieved by using a 2-stage flash converter, under the condition of bandwidth limiting, is calculated to be a factor of $2^{\frac{N-6}{2}}$, using Equations 6.17 and 6.23. Similarly, if the comparator is slew-rate limited, Equations 6.18 and 6.24 show that the power saving factor is $2^{\frac{N-4}{2}}$.

6.10.2.4 A discussion of power consumption for a 2-step flash converter

Figure 6.19 shows that, at 10-bit resolution, for array sizes larger than 300×300, serial converter power consumption is dominated by the comparator bias current. If a semi-parallel approach is

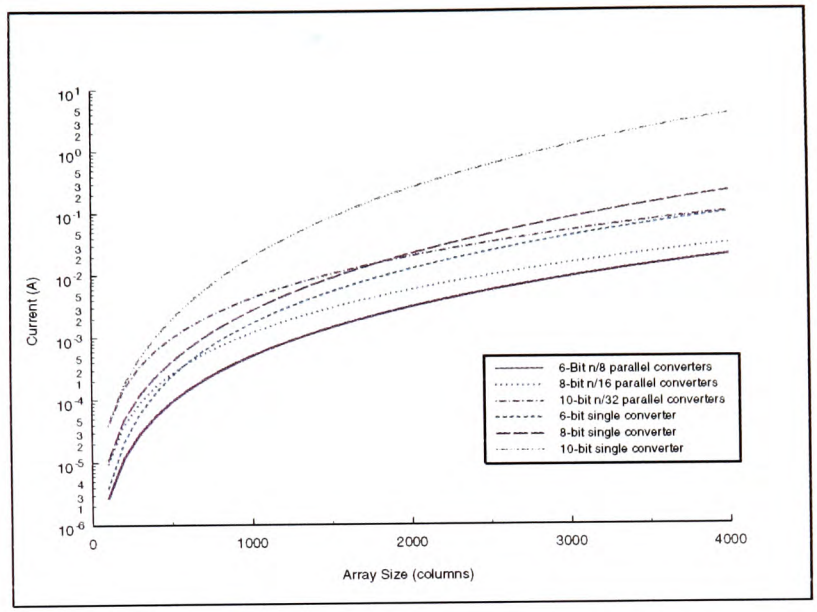


Figure 6.18: *A comparison of bias current for a two-step flash converter.*

used, comparator current is insignificant compared to the input-capacitance-charging and reference current. Figure 6.18 shows that the reduction in comparator bias and input-capacitance-charging current make the semi-parallel strategy more attractive than the serial approach for array sizes larger than 300×300.

Unlike the full-flash converter, a 10-bit semi-parallel converter is practical. The reduction in m possible with the two-step flash architecture, produces significant reductions in power over the single converter, as shown in Figure 6.18.

6.10.3 Mismatch

Unfortunately, the flash converter mismatch tolerances are not improved by the standard two-step architecture. However, if inter-stage gain is used the fine conversion mismatch limit is increased. Similarly, the mismatch tolerance of the coarse comparator bank can be improved if the input range of the fine converter is increased by using extra converters.

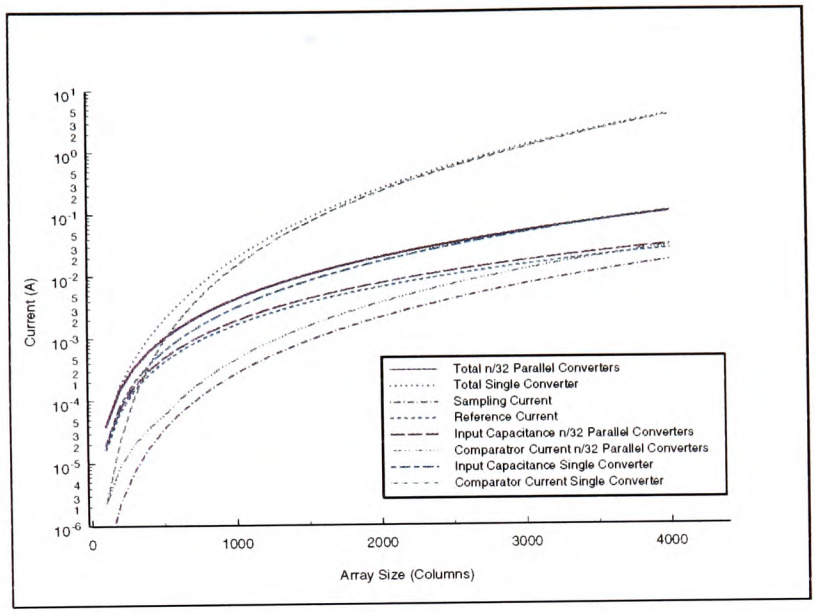


Figure 6.19: *The required bias current for a 10-bit two-step flash converter.*

6.11 The pipelined converter

The pipeline converter is formed by extending the two-step flash architecture to a greater number of stages. Each stage converts the B most significant bits of the residue from the preceding stage. Maloberti concludes that pipeline converters are the best choice for low-power, medium-resolution converters, with the proviso that the introduced data latency is acceptable [123], which it is for area image sensors.

A pipeline stage, for example, as shown in Figure 6.20, has a transfer function of the form

$$V_{out} = G(V_{in} - V_{DAC}) \tag{6.25}$$

where V_{DAC} is the output from the DAC and the stage gain, G, is given by

$$G = \left(1 + \frac{C_s}{C_F}\right) \times \left(1 - e^{-\frac{t}{\tau}}\right) \times \frac{1}{1 + \frac{1}{Af_b}} \tag{6.26}$$

where the first term is the voltage gain term; the exponential term describes the settling time of a single pole amplifier; the third term is related to the finite amplifier gain, A, and f_b is the

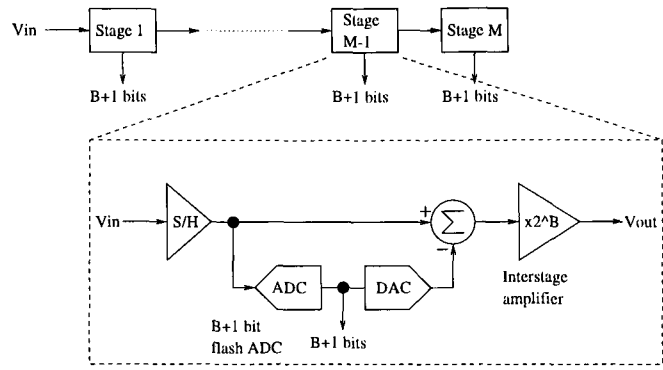


Figure 6.20: *A typical pipeline architecture.*

feedback factor, which is defined as the ratio of the feedback capacitance to the total capacitance seen at the input to the amplifier. Each term in Equation 6.26 contributes to the gain error, $\frac{\Delta G}{G}$, which is given by [125]

$$\frac{\Delta G}{G} = \frac{G_{ideal} - G_{actual}}{G} = \frac{1}{2^B}\left(2^B - \left(1 + \frac{C_s}{C_F}\right)\left(1 - e^{-\frac{t}{\tau}}\right)\left(\frac{1}{1 + \frac{1}{Af_b}}\right)\right) \tag{6.27}$$

In order to achieve N-bit resolution, the combined gain term should be less than a least-significant bit. Consequently, the gain error term elements can be bounded [125]:

The amplifier gain, A, should satisfy

$$A > 2^{N-B} \times \frac{2^B C + C_{in}}{C} \tag{6.28}$$

and the settling time, T_{settle} should be such that

$$T_{settle} > N\tau \ln(2) \tag{6.29}$$

where $\tau = \frac{C_L}{g_m} \times \frac{1}{f_b}$ where g_m is the transconductance of the input transistor and C_L is the load capacitance.

In a pipeline architecture, because of the interstage gain, the noise, mismatch and settling requirements become less stringent along the pipeline. Therefore, an optimum pipeline converter is designed with progressively lower performance, or reduced power, amplifiers [125]. The power estimate presented in this section, however, presumes identical stages for simplicity.

Further power savings of 25 to 40% have been achieved by sharing the amplifier output stage between adjacent stages and using a common-mode feedback amplifier as a pre-amplifier for the comparator [135].

6.11.1 Power consumption

The power consumption estimate assumes that a dynamic flash converter is used and that the DAC is performed using a switched capacitor array. Therefore, the power consumption is dominated by the amplifier bias and input-capacitance-charging currents [125]. The minimum number of columns that a pipeline converter is multiplexed between is four to allow sufficient area for amplifier layout.

6.11.1.1 Charging the input capacitance

A current, I_C, is required to charge the input capacitance of the first stage of the pipeline. The input capacitance of subsequent stages is charged by the output buffer of the preceding stage and is considered as part of the output capacitance. I_C is given by

$$I_C = \frac{n}{m} \times C_{in} \times \Delta V_{out} \times \frac{nfm}{\eta} = \frac{n^2 f C_{in} \Delta V_{out}}{\eta} \tag{6.30}$$

6.11.1.2 The amplifier

If the amplifier is bandwidth limited, the minimum required bias current, I_{bw}, is given by

$$I_{bw} = \frac{n}{m} \times \frac{N}{B} \times \frac{1}{2\beta} \left(\frac{NC_L \ln(2)}{f_b T_{dec}} \right)^2 = \frac{n^3 m N^3 f^2}{2B\beta} \left(\frac{C_L \ln(2)}{f_b \eta} \right)^2 \tag{6.31}$$

Comparing Equation 6.23 and 6.31 shows that the required amplifier bias current is proportional to N^3 for a pipeline converter, whereas it increases with $2^{\frac{5N+8}{2}}$ using a two-step flash converter. Therefore, the pipeline architecture will be more power efficient as converter resolution increases. If the amplifier is slew-rate limited, the bias current, I_{sr}, is given by

$$I_{sr} = \frac{n}{m} \times \frac{N}{B} \times \frac{nfm}{\eta} \times C_L \Delta V_{out} = \frac{n^2 f N}{B\eta} C_L \Delta V_{out} \tag{6.32}$$

Under the assumption of slew-rate limiting, the bias current is proportional to converter resolution, which scales less quickly than the $2^{\frac{N+4}{2}}$ relationship of the two-step flash converter for

the given resolution range.

6.11.2 Total power consumption

At 12-bit resolution, as shown in Figure 6.22, the amplifier bias current is dominant for both semi-parallel and serial converters. However, because the amplifier is bandwidth limited, a semi-parallel strategy yields a significant current saving of one order of magnitude at a 1000 $\times$ 1000 array, increasing to three orders of magnitude at 4000 $\times$ 4000 pixels.

The amplifier current of a 6-bit serial converter is slew-rate limited for array sizes below 1500 $\times$ 1500, therefore, it is identical for a semi-parallel or serial approach. Serial converter power consumption is dominated by the input-capacitance-charging current at these resolutions. Therefore, as shown in Figure 6.23, a semi-parallel strategy yields a power saving of an order of magnitude.

In conclusion, other than for small array sizes, where the input capacitance of the serial converter is similar to that of the semi-parallel converter, a semi-parallel approach gives a significant saving over the serial converter.

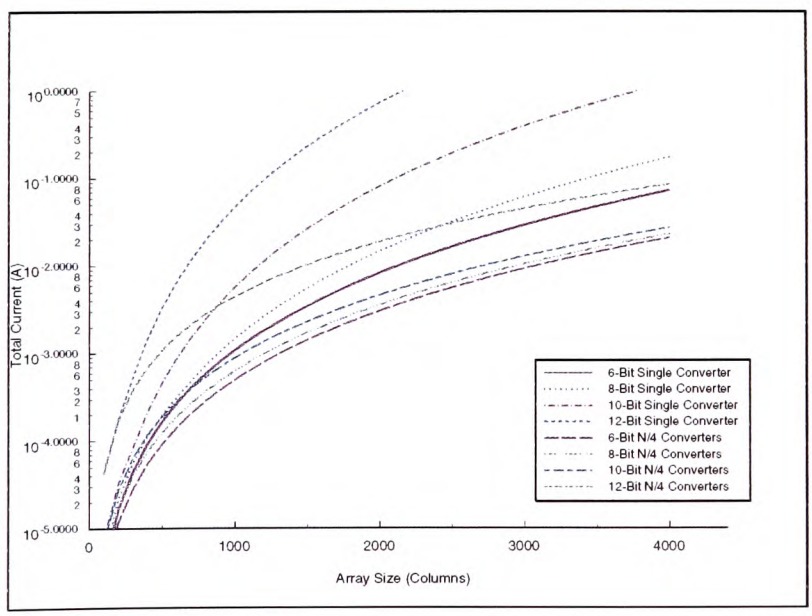


Figure 6.21: *The minimum bias current for a pipeline converter at chosen resolutions.*

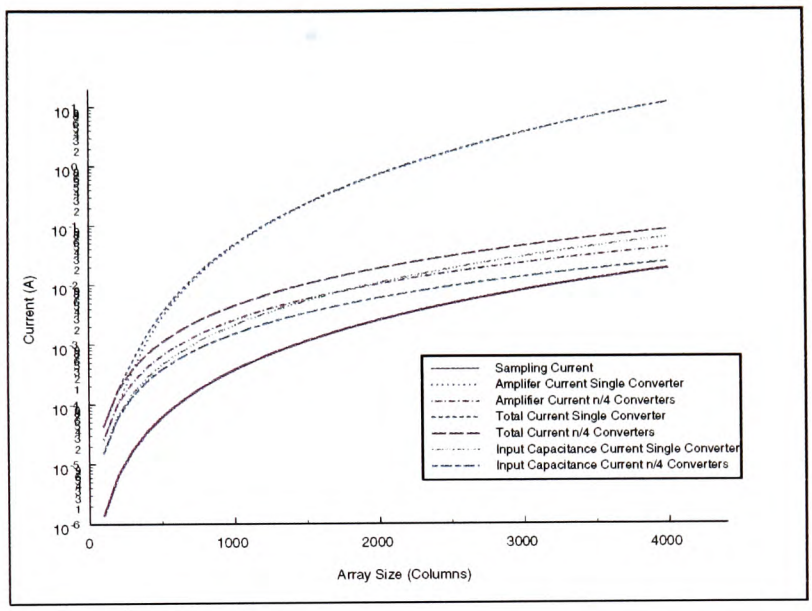


Figure 6.22: *The minimum bias current for a 12-bit pipeline converter.*

6.11.3 Mismatch

In addition to the amplifier gain and bandwidth requirements presented previously, each stage in the pipeline must satisfy the mismatch requirement of a flash converter with resolution $N - (i-1)B$, where i is the stage number.

6.12 The algorithmic (cyclic) converter

An algorithmic converter is a pipelined converter implemented so that a single stage is used repeatedly. The converter must, therefore, satisfy the most stringent requirements of the MSB pipeline stage. Further, a conversion must take place in a single clock period, rather than the $\frac{N}{B}$ clock periods for a pipeline converter. Consequently, unless the amplifier is slew-rate limited, the algorithmic converter is less power efficient than a pipeline converter. Its primary advantage over a pipeline architecture is that a cyclic converter consumes less area [136]. Further to the advantage of the cyclic converter, by reducing the number of conversion cycles, the converter can produce a reduced resolution, increased frame-rate image.

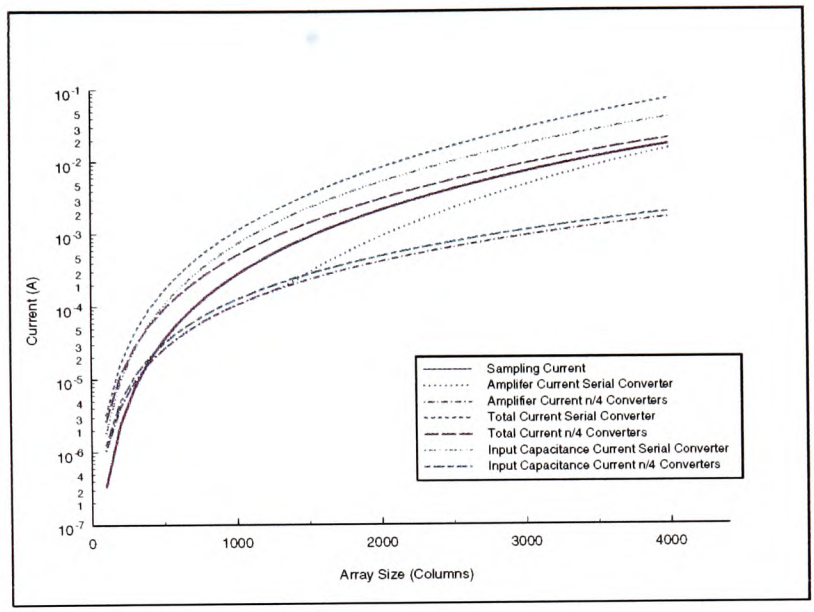


Figure 6.23: *The minimum bias current for a 6-bit pipeline architecture.*

6.12.1 Power consumption

Due to the similarity between the architectures, the estimate for power consumption is similar to the pipeline converter, however, for completeness the formulae are included below.

The amplifier bias current, I_{bw} under the assumption of bandwidth limiting, is given by

$$I_{bw} = \frac{n}{m} \times \frac{1}{2\beta} \left(\frac{NC_L \ln(2)}{f_b \frac{\eta B}{nfmN}} \right)^2 = \frac{n^3 f^2 m N^4}{2\beta} \left(\frac{C_L \ln(2)}{\eta B f_b} \right)^2 \tag{6.33}$$

A consequence of the cyclic use of a single stage is that the settling time is inversely proportional to the total resolution, N. The total bias current, therefore, increases with N^4 rather than N^3 for a pipeline converter. Under the condition of slew-rate limiting, the bias current, I_{sr} is given by

$$I_{sr} = \frac{n}{m} \times C_L \times \Delta V_{out} \times \frac{nfmN}{\eta B} = \frac{n^2 f N}{\eta B} C_L \Delta V_{out} \tag{6.34}$$

which is identical to Equation 6.32, the amplifier bias current for a pipelined converter. The input capacitance current is identical to the pipeline converter, and is given by Equation 6.30.

Therefore, if the amplifier is slew-rate limited, a cyclic converter is preferable to a pipeline architecture because of the reduced component count.

6.12.1.1 Total power consumption

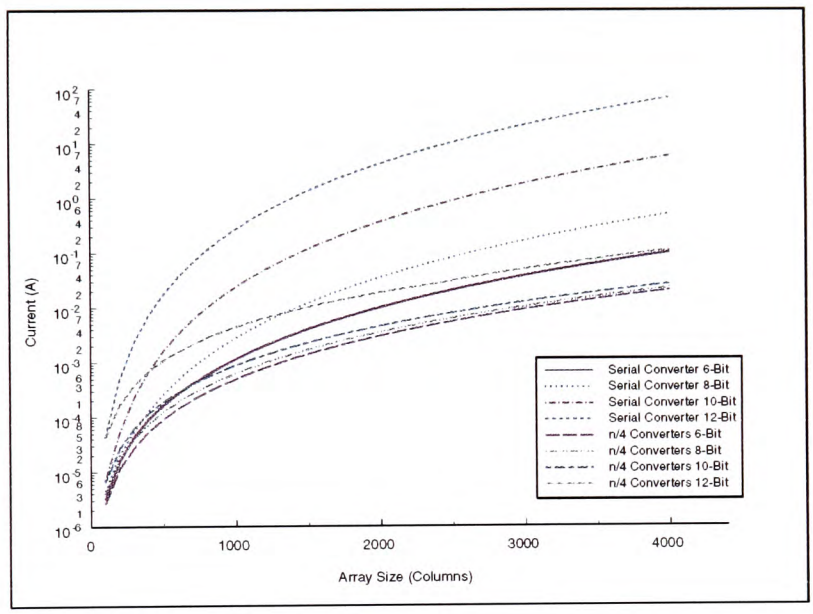


Figure 6.24: *Total bias current for a serial and semi-parallel cyclic converter at various resolutions.*

Figure 6.24 shows that, for array sizes over 500×500 and at resolution greater than 6-bit, the cyclic converter is more than an order-of-magnitude more power efficient when used in a semi-parallel, rather than serial, architecture. Further, Figure 6.25 shows that, above 6-bit resolution, a serial pipeline converter offers a substantial power saving over the serial cyclic converter. However, if a semi-parallel approach is chosen, Figure 6.26 shows that, other than for array sizes greater than 3000×3000 at 12-bit resolution, the cyclic converter consumes the same current as the pipeline converter. Therefore, a cyclic converter is preferred for a semi-parallel converter because of the reduced component count.

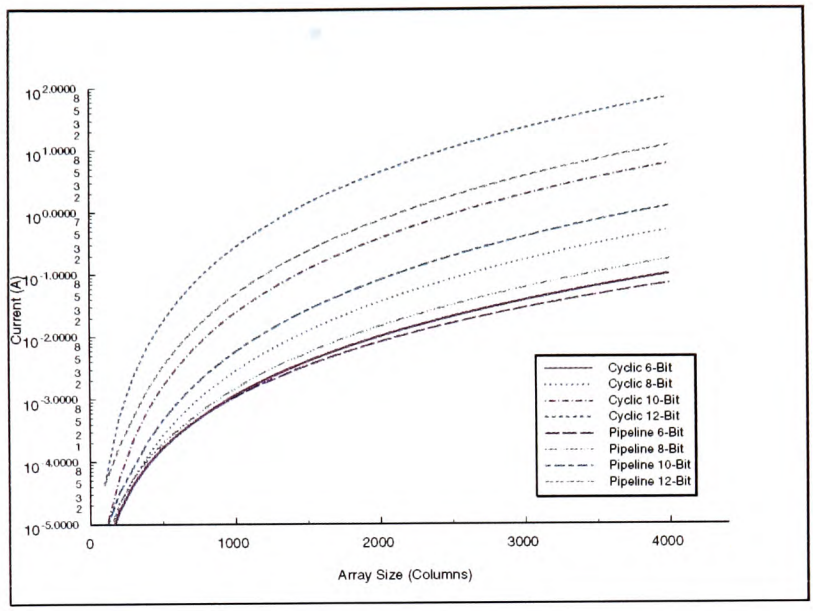


Figure 6.25: *The total bias current required for a serial cyclic and pipeline converter at chosen resolutions.*

6.13 Ramp or integrating converters

A ramp converter can be operated in single-, dual- or triple-slope mode depending upon the input applied to the comparator. This section describes the operation of the single-slope converter before deriving an estimate for the required bias current.

6.13.1 The single-slope converter

A conversion cycle begins by reseting the counter, enabling write to the N-bit register and setting the reference voltage to the input range minimum. The input signal is then sampled onto the positive input of the comparator. Initialization is now complete and the conversion process begins by concurrently starting the counter and ramping the reference voltage, V_{rcf}. The reference voltage is ramped at a rate such that it reaches the input range maximum when the counter reaches full-scale. Providing that the input signal lies within the allowed input range, at some point during conversion, the reference voltage will exceed the input voltage, forcing the comparator to change state. This output signal latches the counter value into the register. The value stored in the register is a measure of the time taken for the reference value

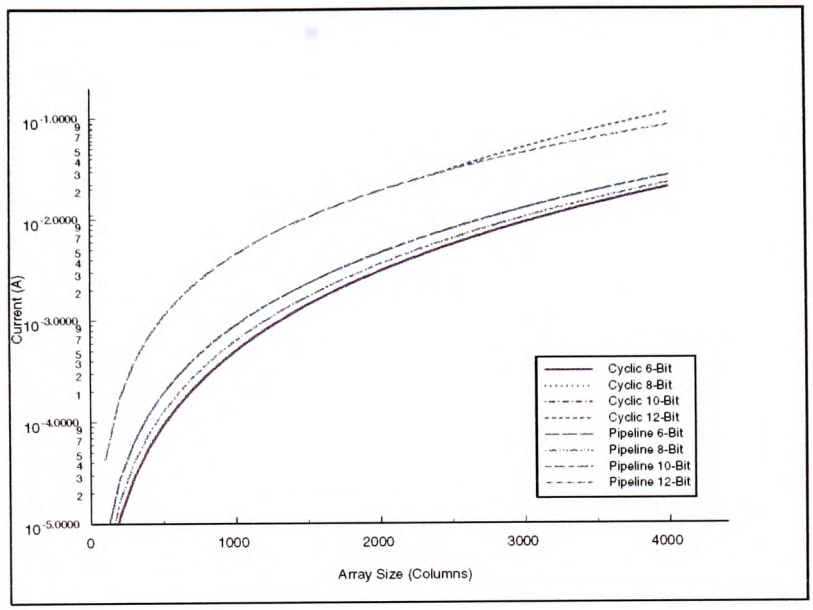


Figure 6.26: *The total bias current required for a semi-parallel (n/4) cyclic and pipeline converter at chosen resolutions.*

to exceed the input value, and assuming the ramp is linear, is proportional to the input signal voltage [124]. Expressed mathematically,

$$\frac{V_{in} - V_{in(min)}}{V_{infs}} = \frac{C}{2^N} \tag{6.35}$$

where $V_{in(min)}$ is the initial reference voltage; V_{infs} is the input full-scale and C is the latched counter value.

A well-known disadvantage of the single-slope technique is that the conversion process takes 2^N clock cycles. Therefore, only a semi-parallel architecture is considered. An advantage of the single-slope converter is that the counter and reference generator can be shared between the individual converters and, consequently, only an N-bit register, simple logic and a comparator are integrated *per* m columns. The minimum value of m, therefore, is 1.

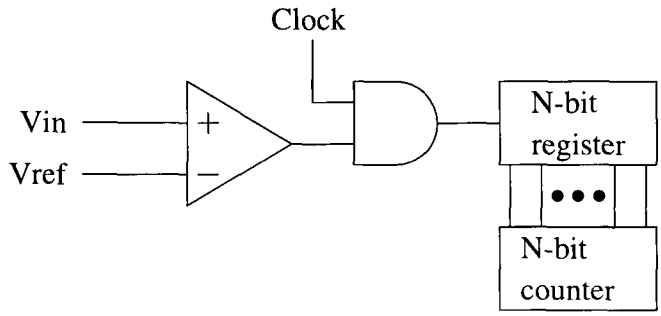


Figure 6.27: *The architecture of a ramp converter.*

6.13.2 Power consumption

The comparator, ramp generator, counter and memory all consume current. For simplicity, the memory power consumption is assumed to be independent of converter type, therefore, it is ignored in the following power estimate.

6.13.2.1 Ramp

The reference voltage must be applied to the all comparators simultaneously, therefore, the minimum required current is given by

$$I = C\frac{\Delta V}{\Delta t} = nC_{sample}\Delta V \times \frac{nf}{\eta} \tag{6.36}$$

6.13.2.2 Counter

As the array size increases, the counter capacitive load increases, therefore, the output drivers consume increased current and dominate the counter current. Consequently, only the buffer current required to drive a capacitance, $C = n \times N \times C_{mem}$, is considered. Assuming that the buffer does not consume quiescent current, the worst-case current, required to charge the load capacitance when all bits change simultaneously, is given by

$$I = CV_{dd}f = nNC_{mem} \times V_{dd} \times \frac{nf2^N}{\eta} \tag{6.37}$$

6.13.2.3 Comparator

If the comparator is bandwidth limited, and the decision time is equivalent to the time taken for the reference voltage to increase by a LSB, the minimum required bias current, I_{bw}, is given by

$$I_{bw} = n \times \frac{1}{2\beta}\left(\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}}\right)^2 = \frac{n^3 f^2 2^{4N+1}}{\beta}\left(\frac{C_L \Delta V_{out}}{\eta}\right)^2 \tag{6.38}$$

Alternatively, under slew-rate limiting, the minimum bias current, I_{sr} is given by

$$I_{sr} = n \times C_L \frac{\Delta V_{out}}{T_{dec}} = \frac{n^2 f 2^N}{\eta} C_L \Delta V_{out} \tag{6.39}$$

6.13.3 Total power consumption

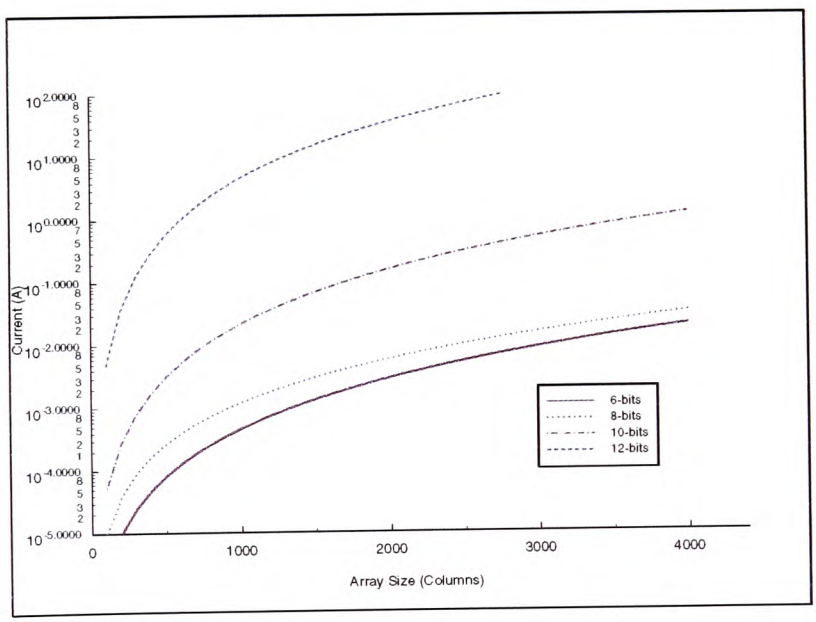


Figure 6.28: *Minimum bias current for a semi-parallel, single-slope converter at 6-, 8-, 10- and 12-bit resolution.*

Figure 6.28 shows that a 10-bit single-slope converter consumes an order of magnitude more current than an 8-bit converter. A further two orders of magnitude of current are required to increase the resolution to 12-bits. This increase is due to the exponential rise in comparator current, which is caused by the factor of four reduction in both the minimum input signal and the decision time between 8- and 10-bit, and 10- and 12-bit, resolution converters. Figure 6.30

shows that, at 12-bit resolution, the comparator current is two orders of magnitude greater than the counter current, which in turn is an order of magnitude greater than the sampling current. For a 6-bit converter, the sampling current is dominant. However, both the comparator and

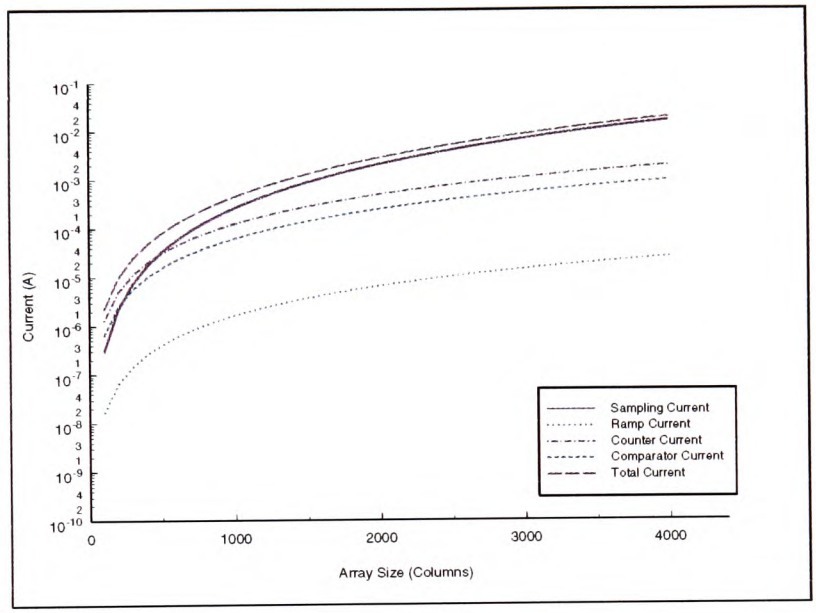


Figure 6.29: *Power consumption for a semi-parallel, 6-bit, single-slope converter.*

counter currents are significant, in particular, at small array sizes.

6.13.4 Fixed-pattern noise

If the signal delay across the array is negligible in comparison with the clock period, the common ramp and counter should not introduce fixed-pattern noise. However, Figure A.1 shows that RC-delay can be comparable to a typical system clock of 50nS. Consequently, a fixed-pattern noise due to signal delay may be introduced. If the ramp and the clock are driven from the same side(s) of the array this effect is mitigated.

The comparator introduces fixed-pattern noise due to input offset and mismatch in bias current and parasitic capacitances. Fortunately, these variations are not signal dependent, therefore, a constant fixed-pattern noise is associated with each column. It is possible to reduce the offset mismatch by performing an auto-zero phase, however, the conversion time would be reduced leading to an increase in power consumption. Further, the variation in comparator decision

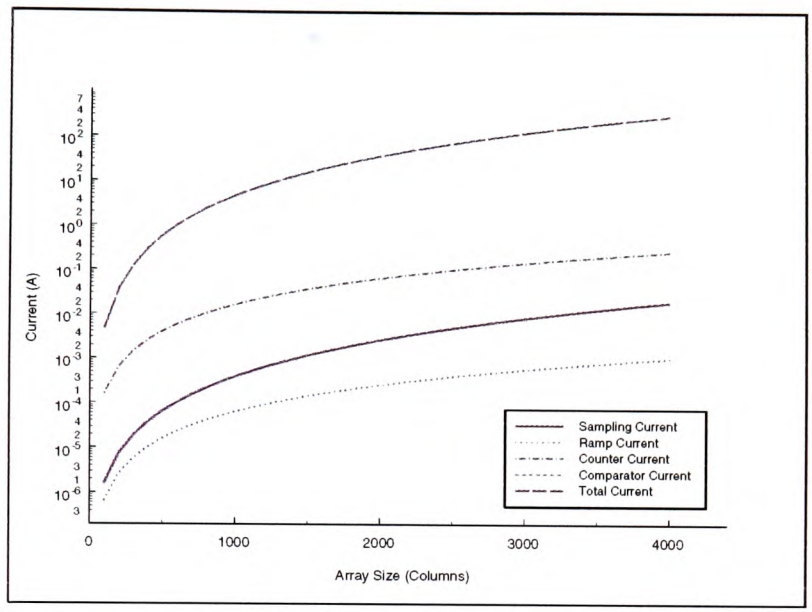


Figure 6.30: *Power consumption for a semi-parallel, 10-bit, single-slope converter.*

time caused by bias current and parasitic capacitance variation would not be cancelled by the auto-zeroing technique. Therefore, it is preferable to digitally subtract a column offset, which can be performed as dark reference.

6.13.5 A power efficient single-slope converter

As previously observed, the power consumption of a single-slope converter at 10- and 12-bit resolution is dominated by the comparator, with the counter making a significant contribution. Both of these contributions must be substantially reduced if the single-slope converter is to be used at 10- or 12-bit resolution.

6.13.5.1 Reduced power counter

The counter buffer power consumption can be decreased, for a given load capacitance, by reducing the transition frequency or limiting the clock-swing. Whether a reduction in clock-swing is possible is dependent upon the memory structure, discussion of which is deferred to Section 7.4.3. A reduction in the clock transition frequency is possible using a Gray code

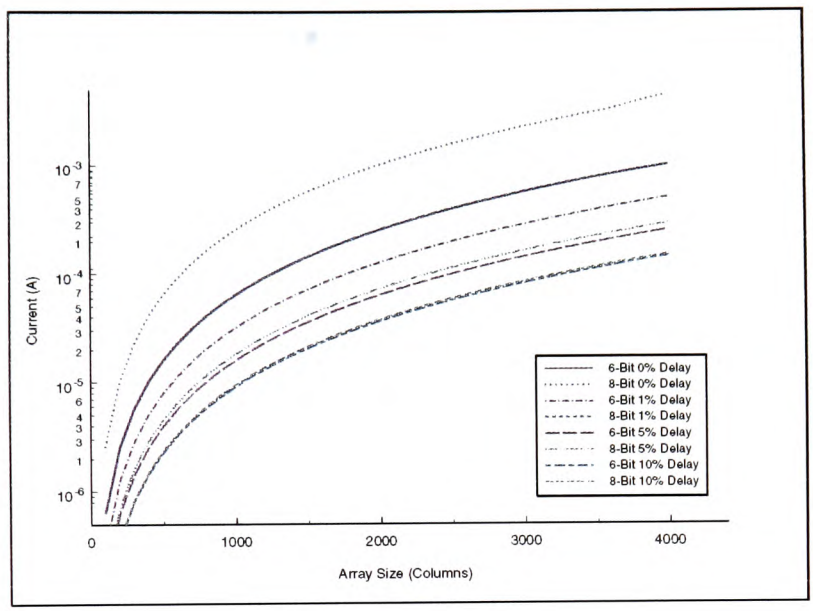


Figure 6.31: *A graph to show the reduction in comparator bias current with allowed delay for a 6- and 8-bit single-slope converter.*

counter, which is characterized by a single bit transition *per* clock cycle. A further benefit of Gray code is that latching errors are limited to a single LSB [137].

6.13.5.2 Reduced power comparator

Under the assumption of bandwidth limiting, the minimum bias current for a comparator is given by Equation 6.7, which is repeated below

$$I_{bias} = \frac{1}{2\beta} \times \left(\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}} \right)^2 \tag{6.40}$$

If β is chosen to optimize the analogue performance of the input pair and C_L and ΔV_{out} are minimized, the power consumption can be reduced by either increasing the decision time, T_{dec}, or the minimum input voltage, $V_{in(min)}$.

Jed Hurwitz (a VLSI Vision employee) has suggested that the decision time can be increased to N clock periods. The increase in decision time causes an offset of N-LSBs to the digital output, which, can be subtracted in the same operation as fixed-pattern noise removal in the

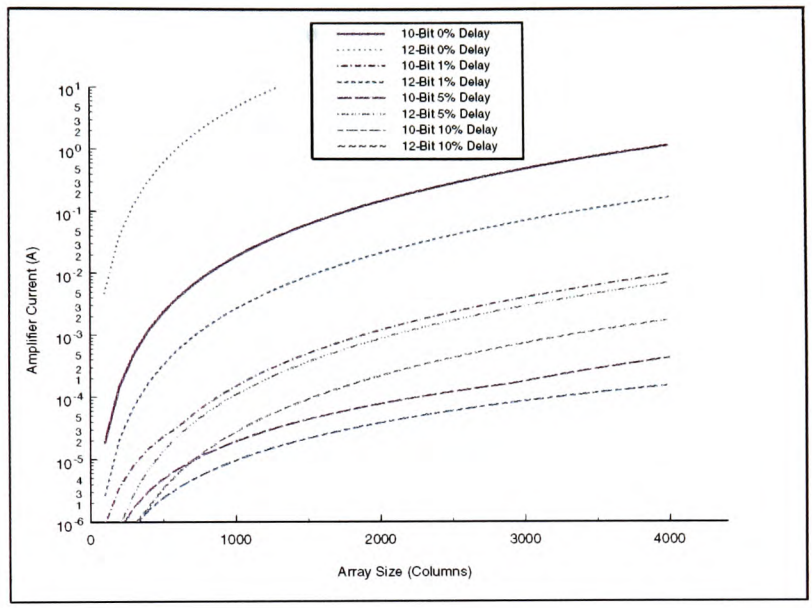


Figure 6.32: *A graph to show the reduction in comparator bias current with allowed delay for a 10- and 12-bit single-slope converter.*

digital domain. Figures 6.31 and 6.32 show the variation in minimum comparator bias current as the decision time is increased by a given percentage of the total conversion time. If a delay of 1% of the conversion time is acceptable the comparator current is reduced by 2, 3 orders of magnitude at 10- and 12-bit resolution, respectively. The increased power reduction at higher resolution is because a fixed time rather than number of clock cycles delay is assumed. In practice, the introduced delay, or conversely minimum bias current, will be less than that shown in Figures 6.31 and 6.32 because the reference voltage increases during the extended decision time. Therefore, the effective minimum input voltage is increased.

Figure 6.33 compares the total bias current required for chosen 10-bit converters. It shows that the reduction in power consumption due to a Gray-code counter and 1% delay result in the sampling current being dominant. Further, the low-power single-slope converter consumes approximately the same power as the cyclic converter, which, of the standard converters considered, consumes the least current.

An alternative method of increasing the clock period is to use a scheme similar to the triple slope converter. A triple-slope architecture begins quantization using a fast ramp to perform a

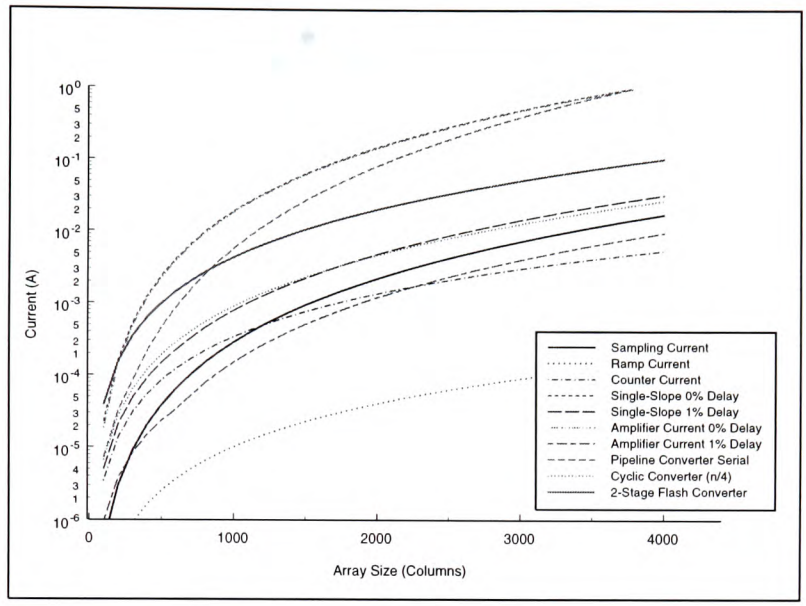


Figure 6.33: *A comparison of a 10-bit single-slope converter bias current and chosen architectures.*

coarse conversion. The fine conversion is then limited to a fraction of the input range [124]. If the coarse and fine conversion cycles quantize an equal number of bits, the total number of clock cycles required is reduced from 2^N to $2^{\frac{N}{2}+1}$, which is a factor of 32 at 12-bit resolution, if the clock periods in both conversion cycles are equal. Note that, if a common ramp is to be used, the coarse conversion value must be subtracted from the input value before the fine conversion can proceed.

Other possible methods to perform the coarse conversion include:

- A low-resolution flash converter, which has the benefit of increasing the fine conversion time. Further, if a cascade comparator is used within the ramp converter, the individual amplifiers could be used to perform a 2-bit flash conversion.
- If charge crosstalk between pixels is significant, adjacent pixel values can be used to predict the input signal value, allowing conversion over a reduced input range.

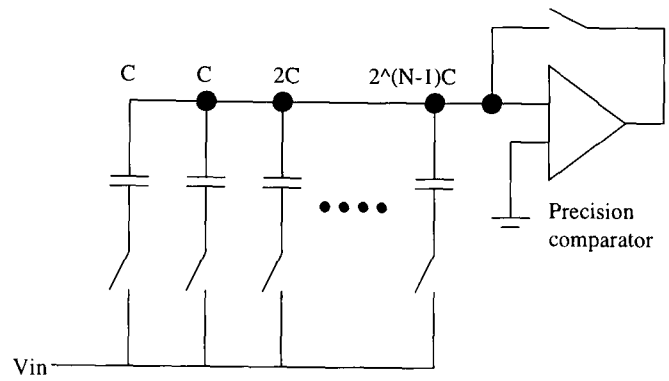


Figure 6.34: *A successive approximation converter*

6.14 Successive approximation converter

The successive approximation converter is a promising candidate for low power conversion because it comprises a single precision comparator and a C-DAC. Conversion is performed in N clock periods. During the first period, the input is compared to a reference voltage equivalent to half the input range. If the input is greater than the reference voltage, the most-significant bit is set to one and the next reference voltage is equal to the three-quarter point of the input range, otherwise, the MSB is set to zero and the quarter reference voltage is used. In a similar manner, an additional bit is determined every clock period until the N-bit word is complete.

The achievable throughput is limited because the capacitor array must settle to its full accuracy during each clock period. Further, the capacitor array must be carefully matched, limiting the maximum resolution to 8-bits without calibration.

6.14.1 Power consumption

6.14.1.1 Comparator

The comparator decision time is given by, $\frac{\eta}{nfmN}$, therefore, under the assumption of bandwidth limiting, the bias current, I_{bw} is given by

$$I_{bw} = \frac{n}{m}\frac{1}{2\beta} \times \left(\frac{C_L \Delta V_{out}}{T_{dec} V_{in(min)}}\right)^2 = \frac{n^3 f^2 N^2 m 2^{2N+1}}{\beta}\left(\frac{C_L \Delta V_{out}}{\eta}\right)^2 \tag{6.41}$$

and if it is slew-rate limited by

$$I_{sr} = \frac{n}{m} \times C_L \times \frac{nfmN}{\eta} = \frac{n^2 fN}{m\eta} C_L \Delta V_{out} \tag{6.42}$$

6.14.1.2 Reference generation

The minimum reference current is given by

$$I = \frac{12kT2^{N+1} f_{ck}}{V_{infs}} = \frac{3kT2^{N+3} nfmN}{\eta} \tag{6.43}$$

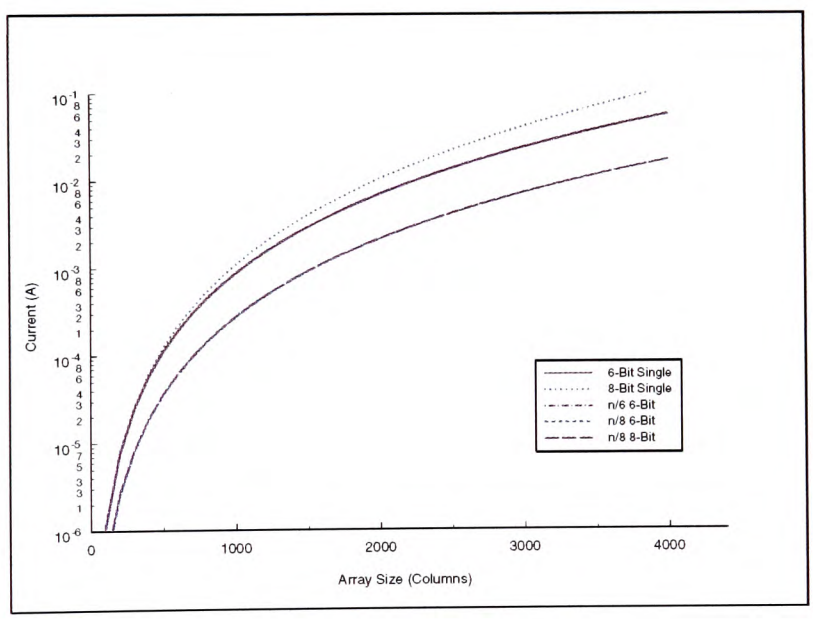


Figure 6.35: *Minimum bias current for semi-parallel and serial, successive-approximation converters at 6- and 8-bit resolution.*

6.14.2 Total bias current

At 8-bit resolution, Figure 6.36 shows that, the total bias current for a semi-parallel converter is dominated by the sampling current. The comparator and input capacitance current are significant for a serial converter, therefore, the semi-parallel converter offers a significant power reduction, as shown in Figure, 6.35. Further, because sampling current does not significantly

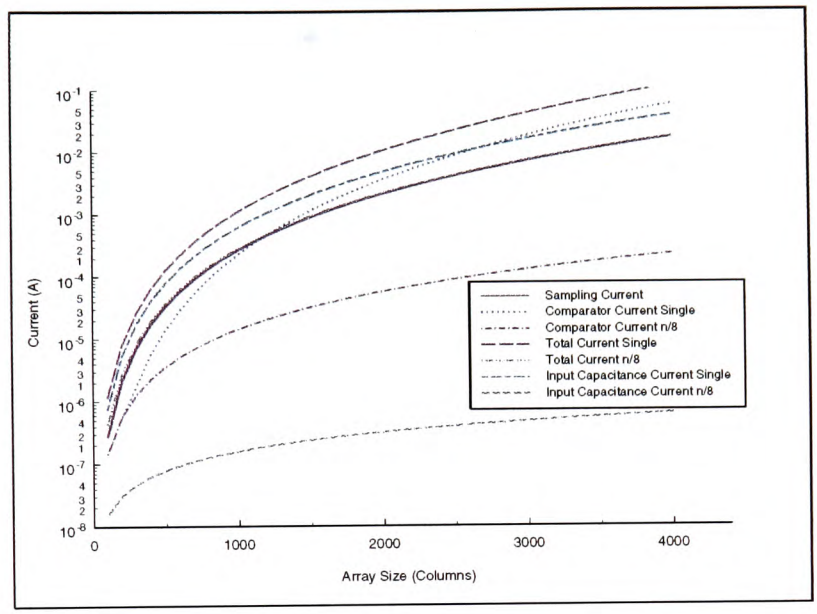


Figure 6.36: *The required bias current at 8-bit resolution.*

increase between 6- and 8-bit resolution, the 8-bit semi-parallel converter consumes a comparable current to the 6-bit converter.

6.15 The $\Sigma - \Delta$ converter

Nyquist rate converters, such as those presented previously, use high-precision analogue circuits, which are vulnerable to noise and interference, to quantize an input signal. An alternative approach is to use an oversampling converter, which uses simple, relatively high-tolerance analogue circuits with fast digital processing to quantize a signal. In principle, oversampling converters are well suited to integration, because the CMOS process is designed for fast-digital processing, rather than high-precision analogue circuits [7].

An oversampling, or $\Sigma - \Delta$ converter comprises a $\Sigma - \Delta$ modulator, which quantizes the input signal at the oversampling frequency, and a decimator, which converts the output of the modulator to digital words at the (lower) output frequency. The oversampling ratio, OSR, is

defined as

$$OSR = \frac{f_s}{2f_o} \tag{6.44}$$

where f_s is the (over)sampling frequency and f_o is the signal bandwidth or, equivalently, $2f_o$ is the Nyquist frequency of the input signal.

6.15.1 The $\Sigma - \Delta$ modulator[7]

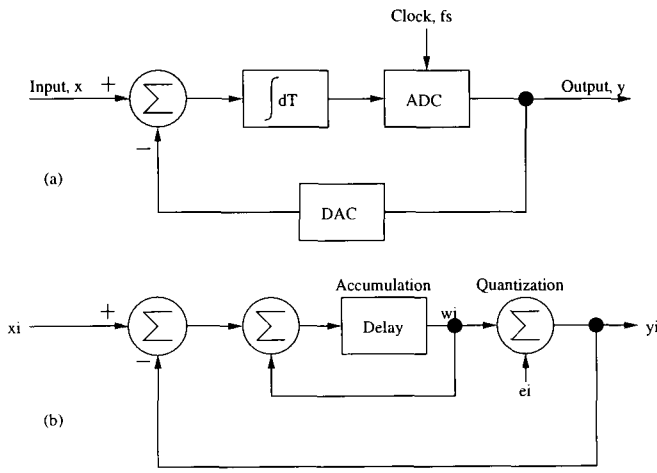


Figure 6.37: *(a) A block diagram of a $\Sigma - \Delta$ modulator and (b) its sampled data equivalent circuit.*

Two characteristics describe a $\Sigma - \Delta$ modulator, the order, or number of feedback loops, and the number of bits in the feedback loop. For example, a first-order, one-bit sigma-delta modulator is shown in Figure 6.37. The feedback loop forces the average output value of the quantizer to track the average input value, such that the difference equation of the modulator is given by

$$y_i = x_{i-1} + (e_i - e_{i-1}) \tag{6.45}$$

Equation 6.45 shows that the output quantization error is the difference of two successive quantized errors, e_i and e_{i-1}. This has the effect of placing the quantization error energy outside the signal band, reducing the in-band quantization noise, $\bar{n}_o^2$, to [7]

$$\bar{n}_o^2 = e_{rms}^2 \frac{\pi^2}{3}\left(\frac{2f_o}{f_s}\right)^3 = e_{rms}^2 \frac{\pi^2}{3OSR^3} \tag{6.46}$$

Consequently, each doubling of the oversampling ratio reduces the in-band quantization noise by 9dB, which is equivalent to an extra 1.5-bits of resolution. A second-order modulator uses a second feedback loop to more accurately estimate the quantization error, thus achieving a 15dB, or 2.5- bits of resolution, reduction in the in-band quantization noise for each doubling of the oversampling frequency.

6.15.2 Decimation [7]

The modulator output is a series of bits, produced at the oversampling frequency. Decimation must convert the bit stream to output words at the Nyquist frequency. Unfortunately, the modulator output contains modulation noise, circuit noise and out-of-band components that must be filtered to achieve the performance given by Equation 6.46. A simple filter is capable of removing the quantization noise, however, an abrupt low-pass filter is required to remove out-of-band signal. In order to reduce the filter complexity, modulation is often carried out in two-stages, as shown in Figure 6.38. In this example the decimator outputs words at four times the Nyquist

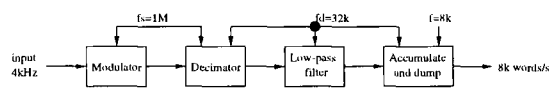


Figure 6.38: *The block diagram for a two-stage decimator.*

rate, which are low-pass filtered before conversion to words at the Nyquist rate. The decimator includes a low-pass filter to remove modulator noise, leaving the intermediate-frequency low-pass filter to remove out-of-band signal components. Ideally, the decimator should have transfer-function zeros at multiples of its output frequency, f_D, to prevent noise folding into the signal band. A suitable decimator, the accumulate-and-dump circuit, is shown in Figure 6.39. Operation is as follows:

1. The register contents are summed with the input signal.

2. If C_D is low the result is written back to memory, otherwise, the result is divided by N, which is given below, and output to the next stage.

$$N = \frac{f_s}{f_D} \tag{6.47}$$

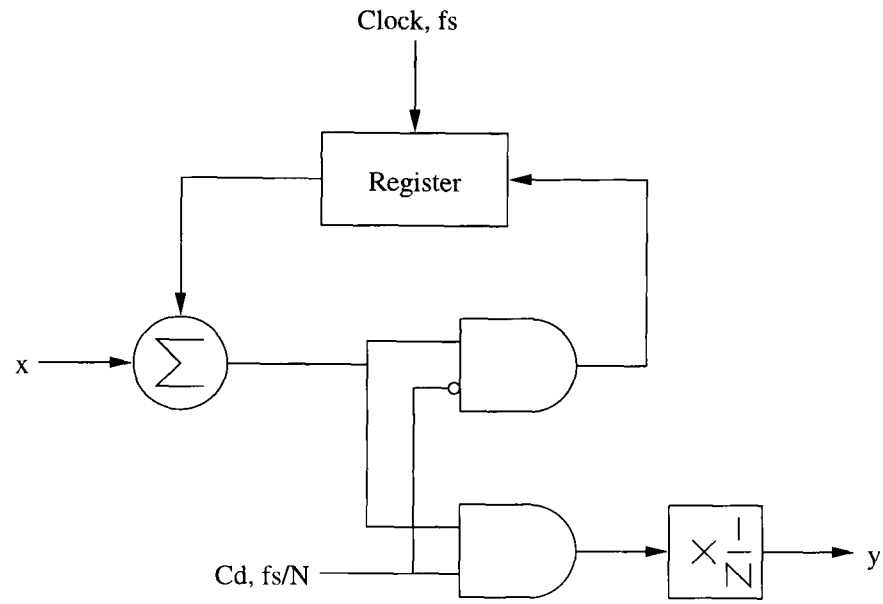


Figure 6.39: *The block diagram for an accumulate-and-dump circuit.*

The difference equation of the circuit is given by

$$y_k = \frac{1}{N} \sum_{i=N(k-1)}^{Nk-1} x_i \tag{6.48}$$

which has the transfer function

$$H(e^{j\omega t}) = \frac{sinc(\pi f N \tau)}{sinc(\pi f \tau)} \tag{6.49}$$

where $\tau = \frac{1}{f}$. Equation 6.49 shows that the transfer function has zeros at multiples of f_D, and, hence, the accumulate-and-dump circuit is a suitable decimator.

6.15.3 Integration of a $\Sigma - \Delta$ converter on an image-sensor chip.

In order to minimize the oversampling frequency, a modulator is integrated *per* column. Previous image sensors have performed decimation on-chip, using a simple averaging circuit in the column [128], and off-chip [48]. Therefore, both strategies are considered here.

An N-bit, Nyquist-rate, 1V input-range, converter produces a signal-to-quantization-noise ratio,

$\frac{n_o}{\Delta}$ given by

$$\frac{n_o}{\Delta} = \frac{1}{\sqrt{3}} \times \frac{1}{2^{N+1}} \tag{6.50}$$

Unfortunately, the quantization noise figure depends on the decimation technique used. Two cases are considered, ideal decimation, and decimation using simple averaging over the Nyquist interval, which can be calculated using a counter and is, therefore, relatively simple to implement. The required oversampling ratio for an accumulate-and-dump decimator will be similar to that using an ideal modulator [7]. The oversampling ratio required to achieve N-bit resolution is obtained by equating the signal-to-in-band-quantization-noise ratio with Equation 6.50, which yields:

For an ideal first-order modulator,

$$OSR > \left(\frac{\sqrt{3}}{\pi 2^N}\right)^{-\frac{2}{3}} \tag{6.51}$$

For a first-order modulator, using a counter to decimate,

$$OSR > \frac{1}{2^{N+\frac{1}{2}}} \tag{6.52}$$

For an ideal second-order modulator,

$$OSR = \left(\frac{\sqrt{5}}{\pi^2 2^N}\right)^{-\frac{2}{5}} \tag{6.53}$$

Equations 6.51 to 6.53 are evaluated for chosen resolutions in Table 6.1 and the corresponding sampling frequency for an $n \times n$ imager is shown in Figure 6.40.

Architecture	8-bit	10-bit	12-bit	14-bit	16-bit
Ideal First-Order	60	151	381	959	2418
First-Order with Counter	362	1448	5792	23170	92682
Ideal Second-Order	17	29	50	88	153

Table 6.1: *The required oversampling ratio for chosen converter architectures at the given resolutions.*

Figure 6.40 shows that, even at 8-bit resolution and small array sizes, the sampling frequency

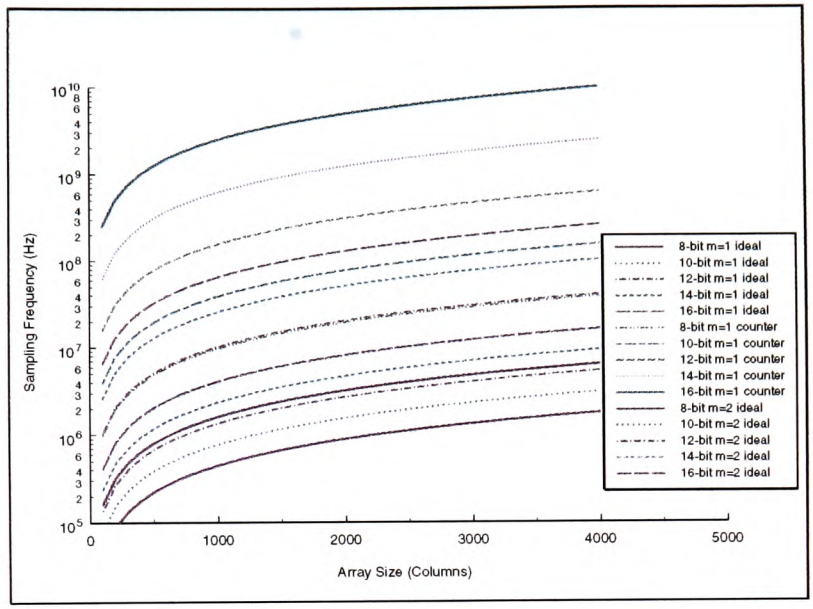


Figure 6.40: *The minimum sampling frequency to achieve 8-, 10, 12-, 14- and 16-bit conversion using an m-order modulator. Note that the ideal graphs represent a ideal modulator with an ideal decimator; the counter lines are for an ideal modulator with a simple mean decimator.*

for a first-order modulator using a counter as a demodulator is several MHz. This is too high to provide a power-efficient conversion solution and is, therefore, disregarded.

Off-chip decimation requires the modulator outputs to be driven off-chip. The resulting digital signal needs to be driven at $\frac{n}{m} \times f_s$Hz, where m is the number of pins used. Clearly, this is impractical for the image-array sizes under consideration.

Table 6.1 shows that second-order modulation results in significantly lower sampling ratios than a first-order converter. However, this advantage is obtained at the expense of increased circuit complexity and matching requirements. Further to the disadvantage of second-order modulators, a more complicated decimation technique is required [7]. Consequently, the second-order modulator is not suitable for focal-plane integration.

The remaining architecture is the first-order modulator with accumulate-and-dump decimator. Fowler has shown that it is possible to integrate a first-order modulator at pixel level [48], therefore, semi-parallel integration should be relatively easy. The decimation circuit is composed of

simple logic blocks, a register and an adder. Whether the decimator is integrable is dependent on the required memory, M_b, which is given in bits by

$$M_b = \log_2(N) + b \tag{6.54}$$

where b is the modulator-output word length and $N = \frac{f_s}{f_D}$. If f_D is chosen for optimum signal-to-in-band-quantization-noise ratio, the memory requirement for chosen resolutions is given in Table 6.2. Integration of sufficient memory would be possible for the given resolutions,

Architecture	8-bit	10-bit	12-bit	14-bit	16-bit
Ideal First-Order	15	38	95	240	604

Table 6.2: *The accumulate-and-dump memory required for a first-order modulator for the given resolutions.*

however, the digital noise generated and power consumed during the read-write process at the oversampling frequency makes this architecture unattractive.

In addition to the previously mentioned problems, the $\Sigma - \Delta$ memory must be reset at the start of each pixel reading. Consequently, there is a transient effect to consider: does the oversampling ratio have to increase further to attain a given resolution? At present, this problem is ignored, because there are sufficient other reasons to disregard the $\Sigma - \Delta$ converter.

In conclusion, unless a low-power, simple, yet near-ideal decimation technique is found, $\Sigma - \Delta$ converters are unsuitable for focal-plane integration.

6.16 Charge-to-digital conversion

Prior to analogue-to-digital conversion, CCD and active-pixel image sensors convert the photocurrent generated, discrete-time, charge-domain signal to a continuous-time, voltage-domain signal. The charge-to-voltage transformation introduces non-linearity and does not preserve the zero-levels. At the expense of doubling the system bandwidth, a zero-level can be re-established using correlated-double sampling, however, the non-linearity is more difficult to remove.

Unfortunately, the charge-to-voltage transformation is fundamental to the operation of an active pixel. However, in a CCD system, the signal remains in the charge-domain until the off-chip amplifier. Traditionally, CCD system analogue-to-digital conversion is performed off-chip,

consequently, high-bandwidth buffers are placed in the signal-path, which introduces noise and increases non-linearity. Further, considerable design time must be spent to ensure that the off-chip environment does not introduce significant noise into the analogue-signal path. An on-chip charge-to-digital converter could, therefore, significantly reduce system-power and improve performance. Such an architecture is discussed in Section 4.9 [122].

6.17 Comparison of converters

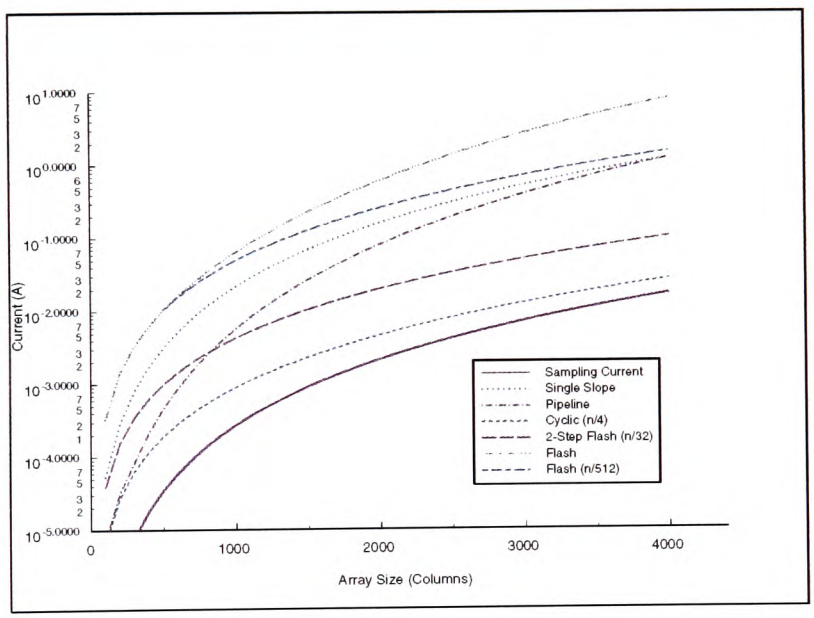


Figure 6.41: *A comparison of chosen converter architectures at 10-bit resolution.*

Figures 6.41 to 6.43 show a comparison of chosen converter architectures at 10-, 8-, and 6-bit resolution, respectively.

For array sizes greater than 500×500, a serial converter consumes significantly more power than multiplexed converters, which are, consequently preferred. Further at these array sizes, the required bias current is so large that an off-chip solution should be considered in preference to a serial converter. Although an off-chip converter would lead to an increase in system power-consumption, it would greatly reduce on-chip power-consumption and noise generation.

At 6- and 8-bit resolution, the most power-efficient architecture is a successive-approximation

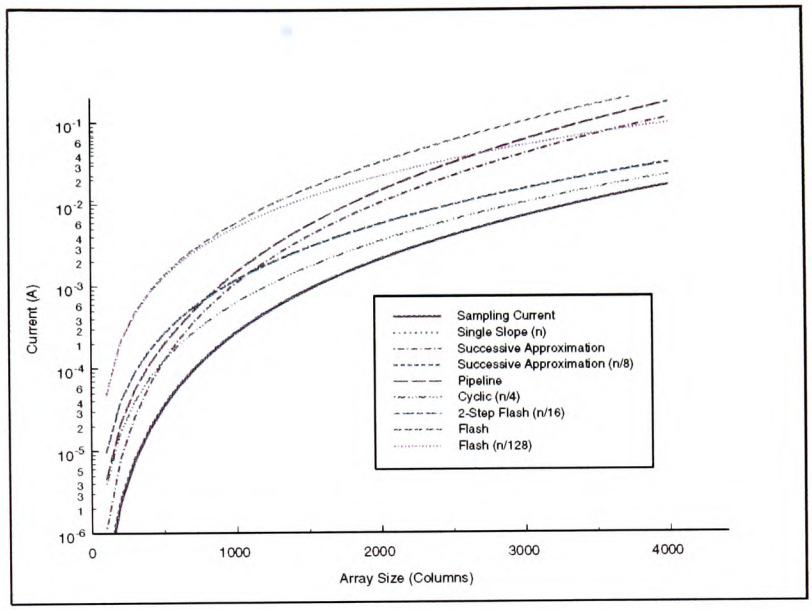


Figure 6.42: *A comparison of the minimum bias current for chosen converters at 8-bit resolution.*

converter multiplexed between the minimum number of columns, which is assumed to be 8 in this analysis. For this architecture, the dominant current is the sampling current, therefore, on-chip integration of such a converter yields the benefits described previously and mitigates the disadvantage in increased image-sensor-chip power consumption. Further, the relatively few clock signals required should not introduce excessive digital noise. The single-slope converter, two-step flash and cyclic-converters multiplexed between the minimum number of columns may be worth considering at these resolutions.

At 10-bit resolution, the sampling current is not dominant. Further, on-chip power-consumption is increased by an order of magnitude by an on focal-plane converter. The maximally parallel cyclic, pipeline and two-step converters should be considered with an off-chip converter to determine the optimum solution at 10-bit resolution.

6.18 Integrated converters from the literature

The most popular converter architecture for integration has been the *per* column single-slope converter [13, 137, 138]. Jansson reports that 8-bit performance was successfully achieved for

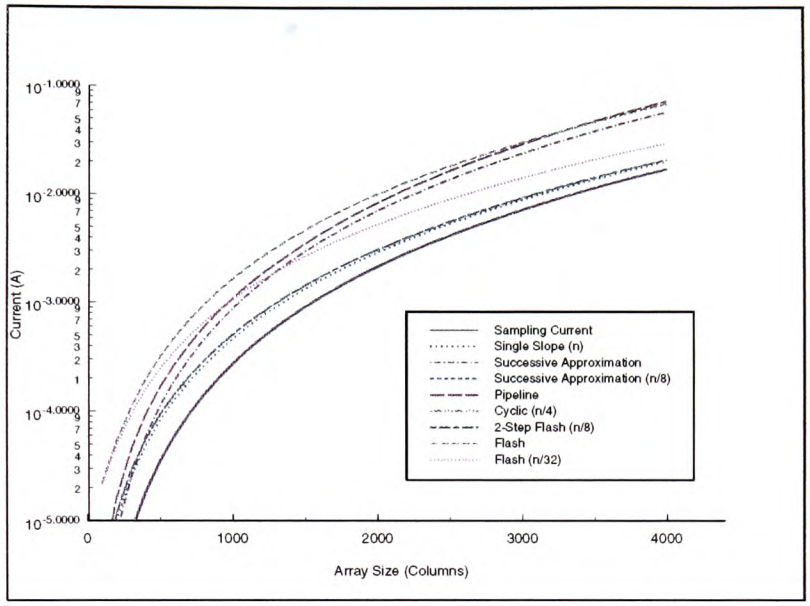


Figure 6.43: *A comparison of minimum bias current for chosen converter architectures at 6-bit resolution.*

a 256×256 image sensor [13] and Torelli experimented with a converter multiplexed between four columns, but found that power-consumption was significantly increased [138]. Interestingly, Torelli concluded that a serial 3-stage flash converter offered power savings over the two single-slope converters and multiplexed successive-approximation converter on test. If the three-stage flash converter was slew-rate limited, and more power efficient than a two-stage flash converter, this result agrees with the presented estimates. However, the successive-approximation result is in direct contradiction to the presented results. Further, the successive approximation converter performed to only 6-bits of resolution and contributed $-38dB$ of fixed-pattern noise, compared to $-40dB$ for the single-slope converter in the same test and $-53dB$ in [13]. Unfortunately, the source of the fixed-pattern noise and random noise that limited the resolution, is not discussed in [138], nor was sufficient information given to determine why the power consumption was so great. However, it is surmised that the reference generation was not accurate enough to achieve 8-bit resolution. Certainly, 8-bit resolution should be possible with this architecture.

Perhaps surprisingly, given the discussion in Section 6.15, considerable effort has been made to integrate a $\Sigma - \Delta$ converter on-chip. Fowler integrated a pixel-level modulator and per-

formed modulation off-chip, concluding that on-chip decimation required too much memory or bandwidth [48]. Mendis used a column integrated modulator and ripple counter as a decimator, however, experimental results were not presented. Therefore, it is difficult to conclude whether using a counter as a decimator is a suitable technique for small array-sizes where the oversampling frequency is not as problematic.

6.19 Conclusion

An on-chip converter is attractive in terms of reducing system power. However, this is at the expense of increasing the image-sensor power consumption and introducing digital noise to the sensor chip. The increase in power is greater as resolution is increased, making integration less practical. Conversely, the need for a quiet off-chip environment is more critical as resolution is increased. Therefore, a practical limit to converter resolution for video-rate imagers, with pixel arrays greater than 500×500, is 8-bit. Below which resolution, the successive-approximation converter offers a power-efficient quantization solution.

A reduced bias current single-slope converter was presented, the design, implementation and results from a fabricated converter using this technique are presented in Chapter 7. A further suggestion, using two sets of sampling capacitors has the potential of significantly reducing chip power consumption. Unfortunately, this technique was not incorporated into the design of *Ginger Dancer*.

Chapter 7
The design of, and results from, the test chip *Ginger Dancer*

7.1 Overview

The previous chapters have highlighted a number of important issues for future-generation CMOS image sensors, namely:

1. **low-voltage operation,** which will be necessary for compatibility with future-generation processes and advantageous to reduce power consumption for portable applications.

2. **improved signal-to-noise ratio.** In order to compete successfully with a CCD-based sensor, it is important to improve the low-light imaging performance. Equivalently, the present level of dark current must be suppressed and the signal-to-noise ratio should be improved.

3. **the integration of on-chip signal processing.** Perhaps the most significant advantage of the CMOS sensor, is the ability to integrate signal processing with the image sensor. In Chapter 6, it was concluded that the power consumption of the integrated processing must be minimized to avoid the deterioration of imaging performance.

4. **the minimisation of coupling from digital to analogue sections of the chip.** Experimental results from the literature, for example Smith [60], have indicated that sensor performance can be limited by digital noise coupling to the analogue chip blocks. In the presented design, steps are taken to minimise the generation of digital noise.

5. **compatibility with future-generation processes.** To date, published studies of the effects of scaling on the CMOS imager have been theoretical. Consequently, it is desirable to fabricate the design on a deep-submicron process and to fully characterize the pixels.

This chapter presents the design of the test chip *Ginger Dancer*[1], which is used to experimentally validate some of the conclusions from previous chapters. *Ginger Dancer* comprises an array of single-slope analogue-to-digital converters and a separate pixel array, along with readout and signal-generation circuits. After a discussion of the general design principles, the design and experimental results from the pixel array are presented in Section 7.3 and from the converter array in Section 7.4.

7.2 The design principles

7.2.1 Choice of process

Ideally, the process would have the following characteristics:

- **be at the $0.35\mu m$ generation or beyond.** Current state-of-the-art CMOS imagers are fabricated on $0.5\mu m$ processes. Therefore, to study the effects of process scaling, a $0.35\mu m$ process or, preferably, a $0.25\mu m$ process is required.
- **allow low-threshold-voltage transistors.** As processes are scaled, the performance of current pixel architectures will be severely limited by the reduction in supply voltage. In order to mitigate this effect, low-threshold-voltage transistors can be used for critical transistors, for example, the pixel-reset transistor. However, the consequent increase in voltage swing is at the expense of increased leakage current. Experiments are needed to quantify whether this increase in leakage current is acceptable.
- **> 3 metal layers.** Two metal layers severely limit the layout of a CMOS image sensor. In an array structure, two metal layers are often required to route signals. Consequently, there is no extra layer for shielding. Further, a third extra layer would ease the layout of structures within the severely limited column pitch. If more than three layers are available, it is likely that the extra layers will not benefit pixel layout, but may reduce pixel sensitivity by reducing the light intensity at the pixel surface. Methods of incorporating extra metal layers without reducing pixel performance need investigating.

For financial reasons, it was decided to use Europractice silicon. Unfortunately, at the time of chip design, the most advanced process with an available analogue design kit was the Mietec

[1]The name, *Ginger Dancer*, is not symbolic or meaningful.

$0.7\mu m$ process. Therefore, this process was chosen for the design. The choice of process was not ideal because:

- it is an earlier generation process than used for state-of-the-art CMOS imagers. Hence, it is not possible to study the effect of scaling on imager performance.
- it is a two-metal, single-poly process. Therefore, shielding is limited and some structures will increase in size, for example, the SRAM cell.
- low-threshold-voltage transistors were not available. Consequently, the increase in leakage through the reset transistor can not be studied.

7.2.2 General design principles

With the exception of the pixel array and drivers, which require a 3V supply, the chip was designed to be operable from 2V supplies. The threshold voltage of 0.8V on the $0.7\mu m$ Alcatel-Mietec process required low-voltage design techniques to achieve this supply voltage. Analogue-to-digital conversion was chosen as an important example of the integration of signal processing on an imaging chip. For successful integration, the converter circuitry was designed to be low power and digital noise generation was reduced through the use of novel circuit structures.

Although the test chip array is only 32 columns wide, the converter and readout circuits are designed to operate at the frequency required for a 1000×1000 pixel array at 30 frames *per* second. Despite the analysis presented in Section 2.7.3, which indicated that the active pixel sensor could achieve a maximum resolution of 10-bits, a 12-bit converter is integrated on-chip. This should allow improved characterization of the column-to-column fixed-pattern noise introduced by the converters and exploration of the limits of performance.

7.3 Pixels

The pixel array section of the chip, shown in Figure 7.1, comprises an array of pixels, digital address circuitry, an output multiplexer, a sampling capacitor and a differential output buffer. Each of these is described before the experimental results from the pixel array are presented.

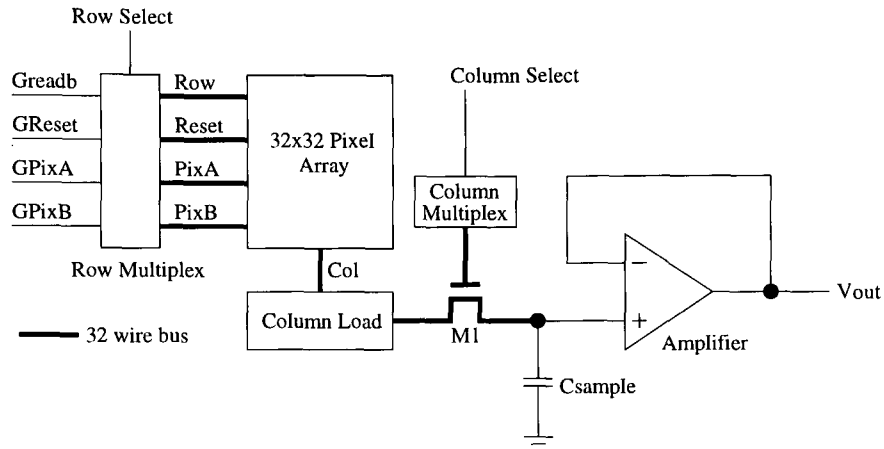


Figure 7.1: *The pixel array and support circuitry.*

7.3.1 The pixel cell

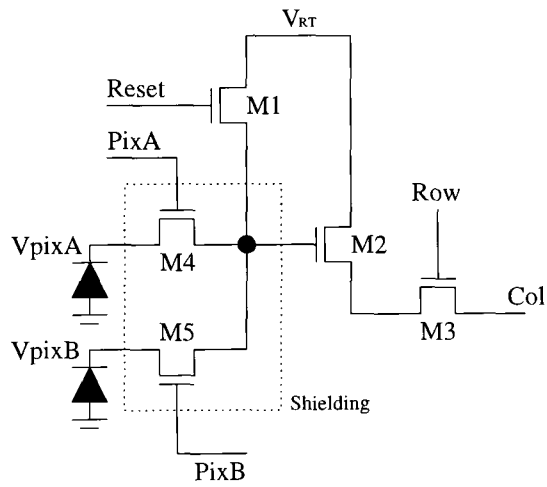


Figure 7.2: *The active-pixel cell.*

The pixel, shown in Figure 7.2, is designed to be addressed flexibly so that the following four modes of operation can be validated.

1. **A single active pixel.** In this mode of operation, as shown in Figure 7.3, *PixA* and *PixB* are held high to link the two diode diffusions; thus, creating a single active pixel.

2. **A double active pixel.** In this mode of operation, which is described in Section 2.6.2, two pixels from adjacent columns share an in-pixel source follower.

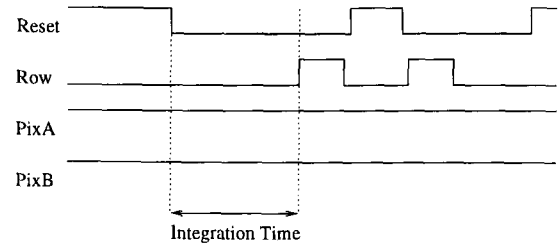


Figure 7.3: *A timing diagram for the pixel in standard-active-pixel mode.*

3. **As a shuttered pixel.** This configuration is used to investigate the effect of charge leakage from the storage node, which is the gate of the in-pixel source follower.

4. **Reduced-reset-noise pixel.** In this mode of operation, the shutter mode of operation is used to store the reset value for correlated-double sampling, as discussed in Section 2.6.3.

During pixel design, three steps were taken to improve pixel performance:

- in order to reduce mismatch, the pixel transistors are increased from minimum size to $\frac{1.5\mu m}{1\mu m}$.
- in an effort to reduce fixed-pattern noise, the A and B pixels were laid out as symmetrically as possible.
- metal 1 and metal 2 were used as a light shield to reduce the rate of discharge from the sampling capacitance.

The double-active-pixel and shuttered-pixel modes of operation are described in the next two sections.

7.3.1.1 Double-active-pixel mode

Comparison of Figures 7.4 and 7.3 shows that the operation of the double-active pixel differs from that of the standard-active pixel because the reset sample is performed before the signal sample. This allows correlated-double sampling to suppress the $\frac{kT}{C}$ noise introduced during the reset operation immediately prior to *PixA* and *PixB* going high.

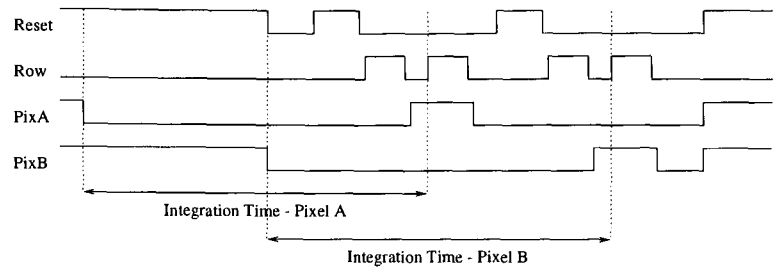


Figure 7.4: *A timing diagram for the pixel in double-active-pixel mode.*

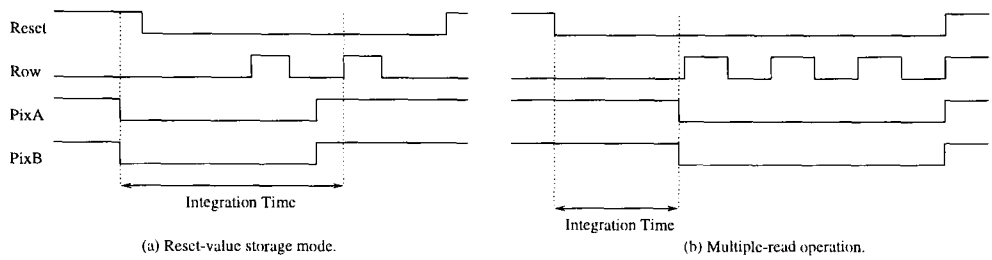


Figure 7.5: *A timing diagram for the pixel in (a) Reset-storage mode and (b) Multiple-read mode.*

7.3.1.2 Shuttered-pixel mode

The shuttered mode of operation can be used to store the current pixel value for future reference, for example, in image-processing it would allow multiple reads of a pixel value or a difference-of-frames operation to be carried out[69]. The storage capacitance is partly comprised of diffusion capacitance, therefore, the stored value will decay due to charge crosstalk from neighbouring pixels and thermally generated charge. If this mode of operation is used, correlated-double sampling can not be performed by reseting the pixel after reading the signal, because the pixel value must be maintained for future reference. Therefore, a pixel offset must be stored in a frame-memory.

The sampling capacitance comprises both diffusion and gate-oxide parasitic capacitances and must, therefore, be shielded from light. On the test-chip, a combination of metal 1 and 2 was used to shield the two pass transistors and the sampling capacitance.

7.3.2 Experimental results from the pixel array

Since the chosen process is several generations old, the optical properties are not particularly interesting. Therefore, the primary aim of the following experiments is to determine which of the suggested modes of pixel operation are feasible. Equivalently, the level of fixed-pattern noise must be determined for each mode of operation. Further, to validate the two shuttered pixel modes of operation, the rate of decay of the sampled pixel voltage must be determined.

Note that throughout the experimental results, two types of voltages are given: fixed-pattern noise and an average value. The average value is simply the arithmetic mean of all the samples taken. Fixed-pattern noise is assumed to be the maximum spread in values taken — a more rigorous definition would be to fit the observed data to a normal distribution and use, for example, the 7σ points to define the fixed-pattern noise (see Appendix E). However, the precise value of fixed-pattern noise is not important, what is significant is whether it is sufficiently large to need to be cancelled before usable images can be obtained.

7.3.2.1 Decay of voltage from sampling capacitance

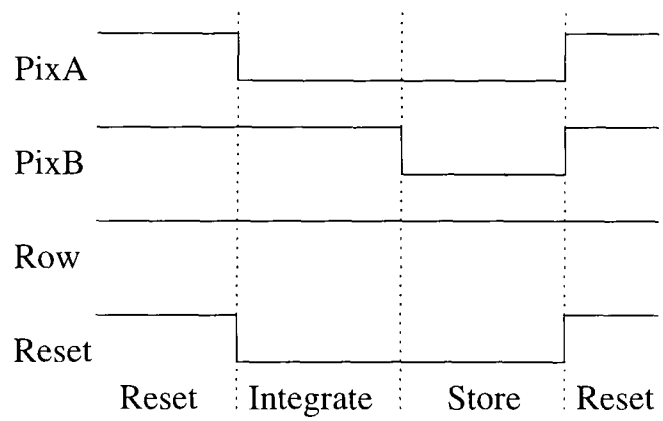


Figure 7.6: *A timing diagram showing the signals used to determine the discharge rate of the sampling capacitance.*

For the shuttered pixel mode to be viable, the decay in stored value must be small relative to the discharge of the pixel over a frame-time, which is typically $\frac{1}{30}s$. An initial experiment was performed, using the timing waveforms shown in Figure 7.6, to determine the rate of discharge of the pixel capacitance. In order to determine the discharge rate, a single pixel output was monitored during a reset-integrate-store cycle. In order to limit the pixel discharge to lie within

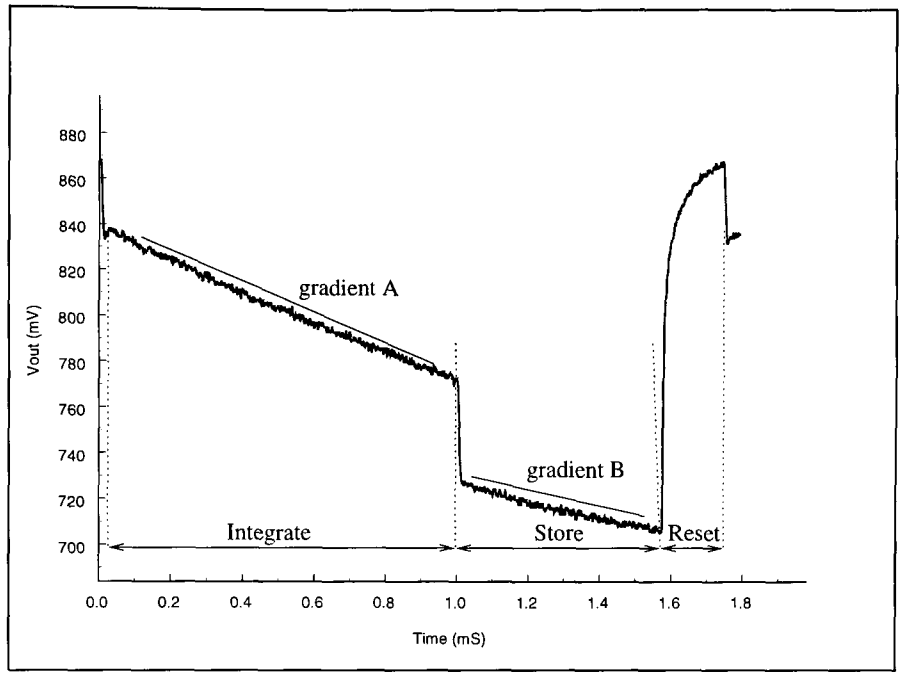


Figure 7.7: *The pixel output voltage during illuminated shuttered pixel operation.*

the limited voltage swing (approximately 0.5V at 3V supply) of the pixel, the integration and storage times were chosen to be $1ms$ and $0.5ms$. By repeating the experiment using shielding over the sensor array, the dark current contribution for both the sampling capacitance and pixel was determined.

A typical output trace is shown in Figure 7.7, which clearly shows the discharge of the pixel and sampling capacitance. The sampling operation is non-ideal because the sampled value decays and the sampled value is less than the pixel value due to capacitive coupling through the parasitic gate-drain capacitance, which comprises the sampling transistor overlap capacitance and interconnect capacitance. If it is assumed that capacitive coupling introduces a fixed offset, the sampling operation is still viable provided that the rate of discharge of the sampling capacitance, gradient B in Figure 7.7 is small compared to the pixel discharge rate (gradient A). Unfortunately, under illumination, the average discharge rate of the sampling capacitance, $(37.1Vs^{-1})$ was found to be comparable to the average pixel discharge rate, $(68.4Vs^{-1})$.

The above experiment was repeated using shielding over the image sensor. Discharge was,

therefore, dominated by dark current. In this experiment, the pixel and sampling capacitances discharged at $17.6mVs^{-1}$ and $30.8mVs^{-1}$, respectively. This is equivalent to a pixel dark current of 0.26fA and sampling capacitance dark current of 0.22fA.

A number of conclusions are drawn from this experiment:

1. The shuttered mode of operation is impractical because the sampling capacitance voltage decays at a similar rate to the pixel voltage. This could be for one of two reasons, but more probably a combination of both:

   (a) Photogenerated charge diffused from the neighbouring pixels and discharged the diffusion capacitance at the sampling node.

   (b) The light-shield did not sufficiently attenuate the incident light.

   In order to determine which of these two effects dominate, the above experiment should be repeated in a temperature cabinet over the temperature range $-30^{o}C$ to $70^{o}C$. Since discharge due to illumination is (to a good approximation) independent of temperature and the diffusion length of photogenerated charge increases with temperature, the variation of sampling capacitance discharge rate with temperature can be used to identify the dominant cause. Note that care must be taken to account for the reduction in thermally generated dark current as temperature is lowered.

   Summarising: the discharge of the sampling capacitance is too great for the shuttered pixel mode to be viable.

2. Equation 2.36 shows that if the shutter operation is to be used to store the pixel reset value, the discharge of the sampling capacitance must be small compared to the pixel discharge. The results above show that this is not the case, therefore, the reduced-reset-noise pixel is not practical due to attenuation of the signal at the pixel.

3. The non-illuminated discharge of the pixel and sampling capacitance correspond to a dark current density of $0.27nAcm^{-2}$ and $0.72nAcm^{-2}$, respectively. For a standard active pixel, assuming that the pixel fully discharges, this level of dark current would limit the achievable resolution to 9-bits if the integration time was equal to the frame time, at 30Hz. However, if we assume an order-of-magnitude variation in scene illumination, 0.5% of the signal from a dark pixel is due to dark current, and for a two-order-of magnitude variation 5% of the dark pixel signal is due to dark current.

The relatively large dark current exhibited by the sampling capacitance compared to the pixel capacitance warrants further investigation. It is surmised that this could be due to:

- the perimeter-to-capacitance ratio of the pixel and capacitance, which are $2.1\mu m/fF$ and $4.5\mu m/fF$, respectively.
- the shape of the diffusions, for example, corners may increase dark current.
- the proximity of neighbouring components — the sampling capacitance is surrounded by four transistors, while most of the pixel perimeter is bordered by interconnect.
- leakage through the reset transistor.

In order to determine the dominant effects, a test-chip should be fabricated using different pixel layouts. In particular, rounded and jagged pixels should be used and transistors should be placed at different distances from the pixel diffusion. In order to determine the effect of leakage through the reset transistor, pixels should be fabricated using a variety of transistor lengths — leakage current will decrease as transistor length increases.

7.3.2.2 Noise and averaging

The output data from the chip included a random noise component of $5mV$ peak-to-peak. In order to suppress this noise, the recorded data was averaged over a number of samples taken at 10Mhz on a 2GHz oscilloscope. This noise figure is an order of magnitude greater than expected. Improved decoupling and a custom printed circuit board with probe grounds closer to the output pins should improve this noise figure.

7.3.2.3 Fixed-pattern noise introduced by the shutter transistor

The sampling operation is non-ideal because of the introduced $\frac{kT}{C}$ noise due to the sampling transistor channel charge and capacitive coupling through the gate-drain-overlap capacitance. In order to quantify these two effects, the clock waveforms shown in Figure 7.8 are applied to repeatedly sample the pixel voltage. A typical output trace is shown in Figure 7.9, the repeatedly sampled values are $\Delta V + \bar{v}_{\frac{kT}{C}}$ less than the pixel value, where ΔV is due to capacitive coupling and is constant for a given pixel and $\bar{v}_{\frac{kT}{C}}$ is a noise voltage, primarily caused by $\frac{kT}{C}$ noise from the sampling transistor channel charge. Two quantities are of interest:

1. the variation of ΔV across the array.

2. the magnitude of $\bar{v}_{\frac{kT}{C}}$

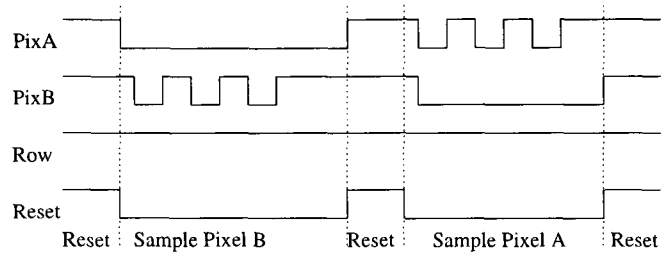


Figure 7.8: *A timing diagram for the pixel in double-active-pixel mode*

Noise Source	Average Value (mV)	Output Voltage Noise (mV)
$\frac{kT}{C}$ noise	NA	1.0
Capacitive Coupling PixelB	63.7	5.1
Capacitive Coupling PixelA	48.7	5.7

Table 7.1: *Output noise due to the sampling operation.*

Two output traces from this experiment are shown in Figures 7.9 and 7.10 and the levels of $\frac{kT}{C}$ and fixed-pattern noise are given in Table 7.1. Three conclusions can be drawn from this experiment:

1. The variation in sampling level for a single pixel, which was on average 1.0mV, agrees reasonably with the calculated value for $\frac{kT}{C}$ noise, which is given by

$$\bar{v}_{\frac{kT}{C}} = \frac{\sqrt{kTC_{ox}W_4L_4}}{C_{sample}} \times A_o = \frac{\sqrt{kT \times 2.44f \times 1.5 \times 1}}{7.1f} \times 0.9 = 0.5mV \qquad (7.1)$$

   where A_o is the voltage gain from the pixel to the chip pad.

2. The fixed-pattern noise introduced by the gate-drain-overlap capacitance is an average of 5.4mV and would limit the achievable resolution to 6 bits for a 1V voltage swing. This fixed-pattern noise is due to variation in the gate-drain parasitic capacitance. It would be possible to cancel this fixed-pattern noise using correlated-double sampling, provided that both the reset and signal values are sampled onto the in-pixel capacitance.

3. The average value of output voltage change due to capacitive coupling through the overlap capacitance was 63.7mV for the B pixels and 48.7mV for the A pixels. Therefore, the

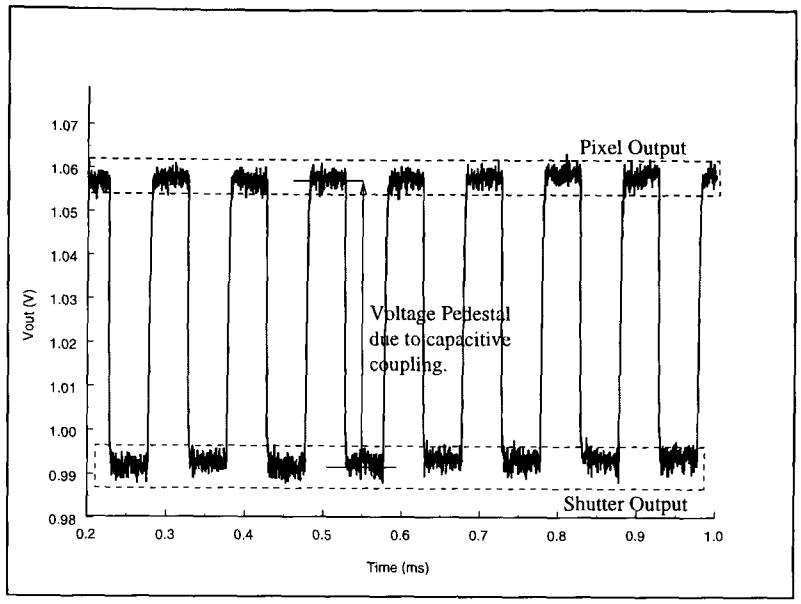


Figure 7.9: *An output trace from a shuttered pixel undergoing repeated sampling.*

fixed-pattern noise introduced by the double active pixel would limit resolution to 5 bits, which is unacceptable for most applications. This difference can be explained by considering Figure 7.11: the *PixA* interconnect runs along the top of the pixel cell in metal 2, while the *PixB* interconnect runs along the bottom of the cell, also in metal 2. In order to reach the gate of the sampling transistor, the *PixB* interconnect must travel vertically up through the cell, overlapping the sampling capacitance. Therefore, the parasitic capacitance between *PixB* and the sampling capacitance is greater than that between *PixA* and the sampling capacitance. Consequently, the voltage step due to capacitive coupling is larger for the B pixels than the A pixels.

This form of fixed-pattern noise can be cancelled using correlated-double sampling. For the double active pixel, a separate reset value must be used for the A and B pixels.

7.3.2.4 Pixel-offsets

Figure 7.12 shows a graph of the output signal from sampled pixels across a chip. The data was obtained by reading the output voltage from a pixel held in reset. Across the chip, the maximum and minimum output signals were 0.97700 V and 0.92995 V. This is equivalent

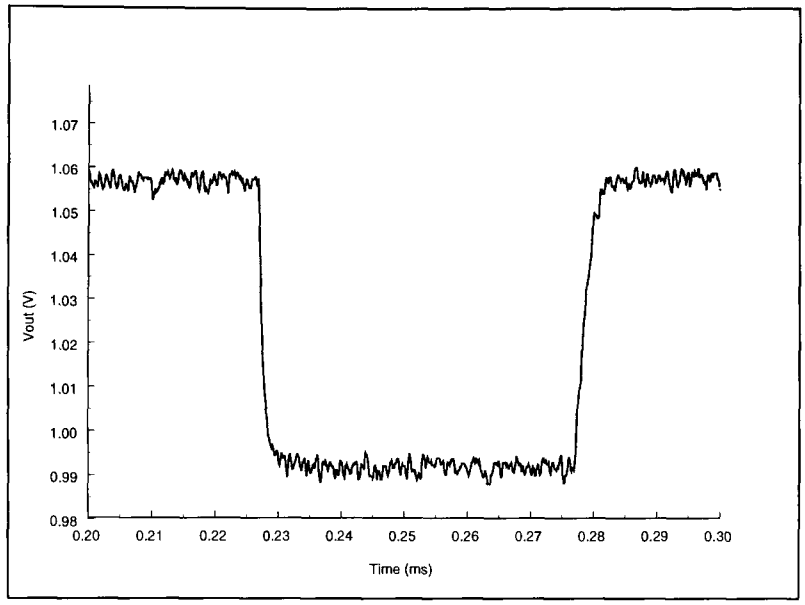


Figure 7.10: *An enlarge output trace from a shuttered pixel showing a sampling operation.*

to a fixed-pattern noise of 47 mV. However, interpretation of Figure 7.12 shows that most of the extreme values lie around the perimeter of the array. If the outside rows and columns are ignored, the fixed-pattern noise is reduced to 34.6 mV. This result shows the benefit of including dummy pixels around the edge of an array. As expected, these values are substantially higher than those predicted by matching data. However, 34.6mV is substantially less than 0.3V which is the difference between the maximum and minimum threshold voltages given in the process data sheet. Therefore, this result is sensible.

7.4 The single-slope converter

In chapter 6, a low-power mode of operation for the single-slope converter was described whereby the comparator decision time was increased at the expense of adding a fixed offset to the output data. This section describes the realization of the design and results from the test chip. Initially, the constituent parts of the converter, namely, the comparator, ramp generator, counter, N-bit register and readout circuits, are described in turn.

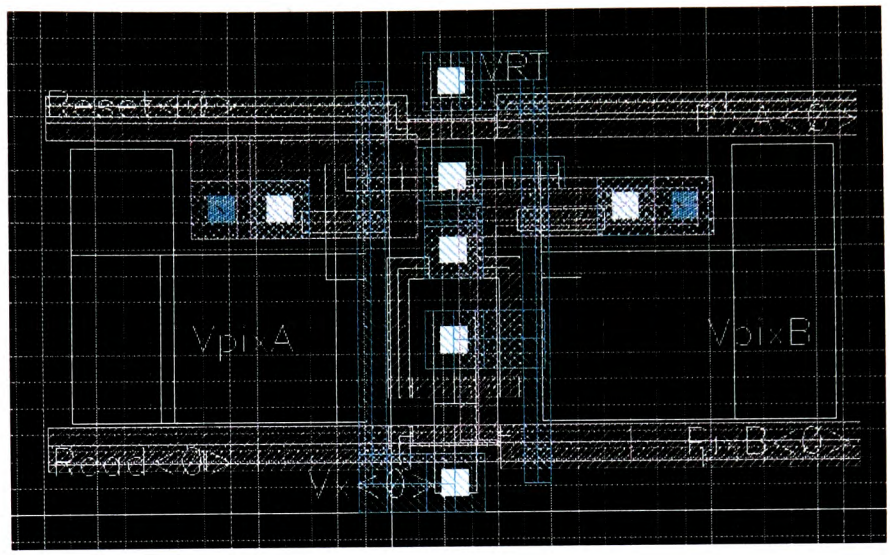


Figure 7.11: *The layout of the active pixel. Note that each grid square is* $1 \times 1\mu m^2$ *and that the colour key is: yellow – polysilicon; pink – metal2; cyan – metal1; white – contact; green – via; transparent with white outline – n-diffusion.*

7.4.1 The comparator

The discussion in Section 6.3 concluded that, for power efficient comparator design, a dynamic latch should be used to generate CMOS levels. In order to overcome the input offset of the latch, a pre-amplifier is needed. For a single comparator, a clocked latch, such as that presented by Yin can be used to achieve low-power operation[139]. However, this scheme is unattractive for a single-slope converter because the latch would need to be reset every clock-cycle during the conversion cycle. This results in $2^N - 2$ unnecessary output transitions, which introduce digital noise. This situation is exacerbated as the array size increases and $\frac{n}{m}$ comparators simultaneously switch. Therefore, a cross-coupled NAND gate latch is used to generate CMOS levels from the output of the amplifier cascade. The latch makes two transitions *per* conversion: once during initialization and again when the pre-amplifier output changes from positive to negative.

A four-amplifier cascade was chosen for the pre-amplifier as a trade-off between area and decision time (as discussed in Section 6.3). In order to improve the power-supply rejection, a fully-differential amplifier was chosen for each of the elements of the cascade. Most realizations of a fully-differential amplifier are unsuitable for layout within the limited column pitch because the common-mode feedback circuit is both too complicated and consumes too much

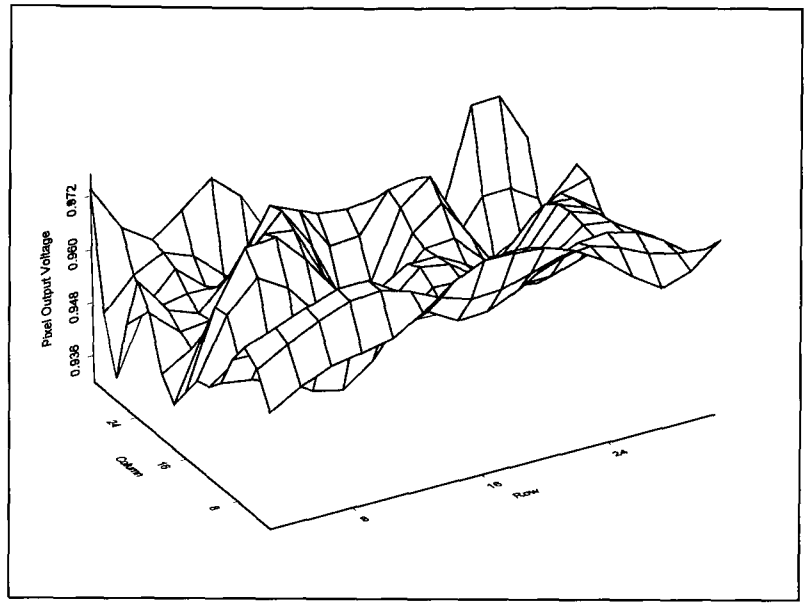


Figure 7.12: *The variation in output voltage across the pixel array for a constant input voltage.*

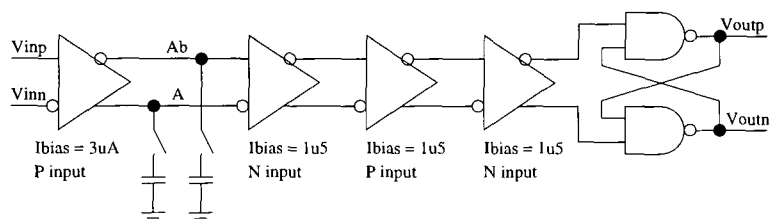


Figure 7.13: *The column comparator, which comprises a cascade of four fully-differential amplifiers followed by a pair of cross-coupled NAND gates.*

power. The amplifier shown in Figure 7.14 uses two transistors, M_7 and M_8, operated in the linear region to provide this function. This configuration was selected because:

1. The common-mode feedback circuit does not consume extra power.
2. The common-mode feedback circuit is simple and, therefore, is suitable for layout within the limited space of a pixel pitch.
3. Unlike the diode-loaded differential pair, which shares the above two advantages, the gain of the stage is of the order $g_m \times r_{ds}$.

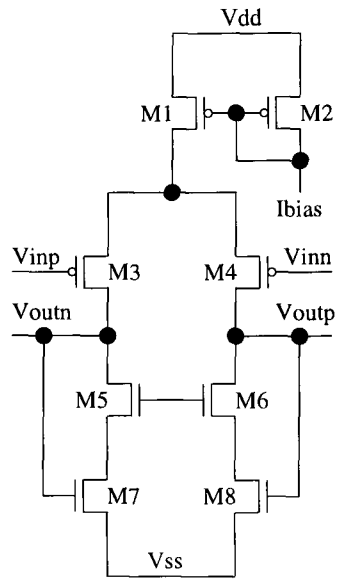


Figure 7.14: *A fully-differential amplifier.*

For ease of layout and to improve analogue performance, the amplifier was laid out over two pixel pitches.

7.4.2 The ramp generator

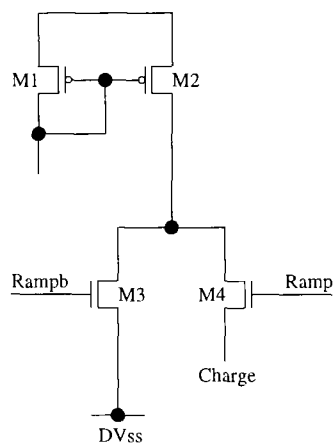


Figure 7.15: *The ramp generator.*

For simplicity, the ramp function was generated using a current source to charge the sampling capacitance at the signal input to the comparator array. During the conversion cycle, *Ramp* is held high and an ideally constant current charges the comparator input capacitance, yielding a

continuous-time ramp. This reduces the generated digital noise compared to a stepped ramp. The two disadvantages of this ramp are that it is not differential and it introduces non-linearity because:

- the output resistance of the current source is finite, therefore, the charging current will be dependent on the ramp voltage. In this design, this problem was exacerbated because a simple current mirror was used to enable low-voltage operation.
- the sampling capacitances, which are the gate-channel capacitances of NMOS transistors fabricated in an n-well, are non-linear.

If the non-linearity introduced is unacceptable, the ramp function could be generated using the counter output to drive a digital-to-analogue converter.

7.4.3 The SRAM array and support circuitry

The 32×12 SRAM array is supported by read and write digital circuitry, a counter, which provides the input data for the array and readout circuitry. Each of the subcircuits is discussed in turn.

7.4.3.1 The SRAM cell

The discussion in Appendix C.1 compares SRAM and DRAM cells and concludes that, in general, SRAM is more suitable than DRAM for integration on an image-sensor chip because of the need for a refresh operation in a DRAM cell. Further, in the specific case of a single-slope converter, the memory input capacitance must be charged 2^N times per conversion. Therefore, it is important to minimize the memory input capacitance. In a DRAM cell, the input capacitance is dominated by the storage capacitance, which must be large so that leakage currents do not discharge it too rapidly. Consequently, for this application an SRAM cell is preferred to a DRAM cell.

For low-voltage operation and to allow fabrication on a standard CMOS process, the 6-transistor cell is preferred over the resistive-load cell. However, the 6-transistor cell suffers from a relatively large input capacitance, which comprises the gate capacitance of the two non-minimum size transistors and the diffusion capacitances of the access transistor. In order to reduce the

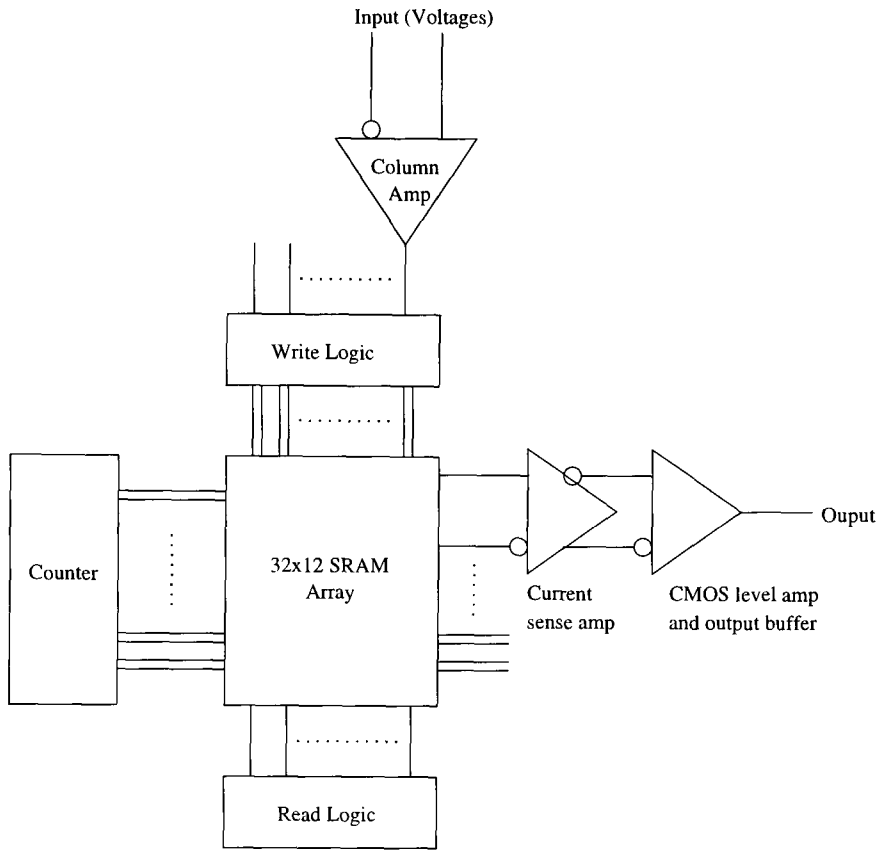


Figure 7.16: *The SRAM array and support circuitry.*

input capacitance, a novel pseudo-static cell, shown in Figure 7.17, is proposed. In this cell, the output structure is separate from the input devices. Therefore, the input devices do not have to be sized to preserve the static-noise margin, hence, the input capacitance is reduced to the gate capacitance of a single minimum-sized transistor and the diffusion capacitance associated with the access transistor. Further to the advantage of the proposed cell:

- The input transistors amplify the signal on the V_{inn} and V_{inp} buses, therefore, a reduced voltage swing counter can be used. This was not implemented in the design because the use of a Gray code counter mitigated the advantage and also made the design of a power-efficient reduced-voltage driver more difficult.
- A current-mode output scheme is used to reduce the voltage swing on the output buses and, consequently, reduce the dynamic power consumption (see Section A.4).
- Ideally, the cell sinks a quiescent current from the supply. Note that this quiescent current

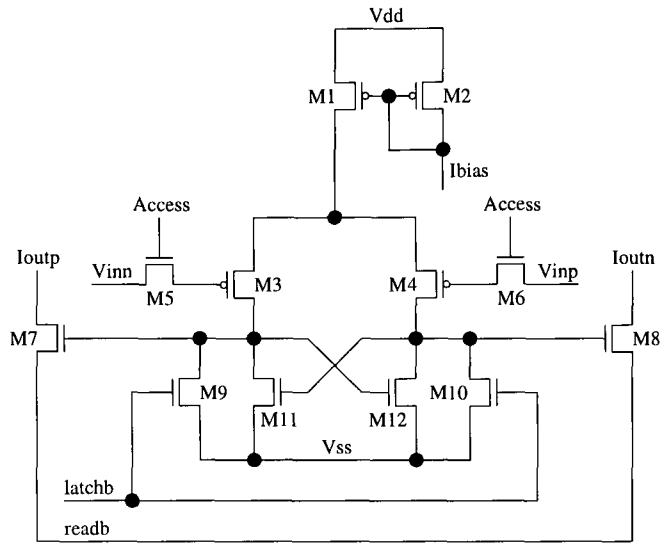


Figure 7.17: *A differential-pair-based pseudo-static memory cell.*

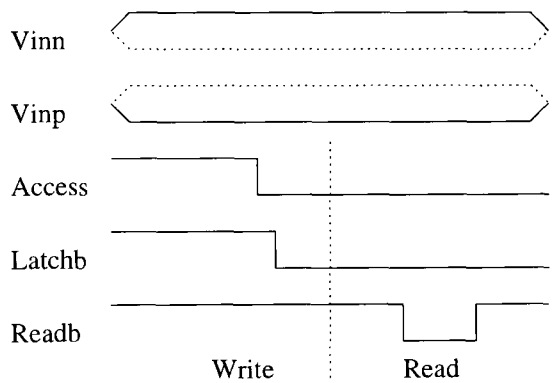


Figure 7.18: *The timing diagram for the memory cell shown in Figure 7.17.*

can be small because the time between the write and read operations is relatively large. On the test chip, the quiescent current was $0.2\mu A$ *per* cell, or $2.4\mu A$ *per* column, which is 25% of the column current budget.

There are two major disadvantages of this cell over a standard CMOS SRAM cell:

1. In a two-layer-metal technology, the cell size is three times larger than a standard six-transistor SRAM cell. If more interconnect layers were available, this disadvantage would be reduced to twice the area of a conventional cell.

2. The proposed cell consumes a bias current of $0.2\mu A$, where as a standard SRAM cell

does not consume quiescent current. However, for a 1000×1000 pixel array operating at 30 frames *per* second the increase in quiescent power is comparable to the dynamic power saving due to the reduction in input capacitance.

The timing diagram for the pseudo-static cell is shown in Figure 7.18. After the comparator has changed states, two signals are sent to the SRAM cell, *Access* and *latchb*. Once *Access* falls, the values of V_{inn} and V_{inp} are dynamically stored on the gate capacitances of the differential pair input transistors. Provided that the difference in stored voltages is sufficient, the tail current will flow down one branch of the differential pair through one of the latch transistors, M_9 and M_{10} in Figure 7.17. When *latchb* falls, the cross-coupled NMOS transistors M_{11} and M_{12} quickly amplify the differential current signal and the cell enters the storage mode.

There are two methods of balancing a cross-coupled NMOS pair, in the proposed circuit, shown in Figure 7.17, two transistors M_9 and M_{10} are used to conduct the differential current during the balance cycle. An alternative scheme is to use a single transistor between the gates of transistors M_{11} and M_{12}. In the first scheme, at the beginning of the amplification phase, gate nodes of the two NMOS transistors are below the transistor threshold voltages, therefore, the cross-coupled transistors can not conduct the differential current, which charges the parasitic drain capacitances at a rate proportional to the branch current. Presuming that there is a differential current, one of the drain nodes will charge more quickly than the other and the positive feedback will act to discharge the drain node at the lower potential, which in turn acts to reduce the drain-source current of the other NMOS transistor . . . . In the second scheme, at the beginning of the amplification phase, there is a voltage difference between the gate nodes of transistors M_{11} and M_{12} caused by the voltage drop across the pass transistor. This voltage is quickly amplified by the positive feedback loop. There is little to choose between the two schemes: the first has a developed differential current, the second a differential voltage. Perhaps, the chosen scheme is less prone to error. However, the primary advantage of the chosen scheme is that the latch transistors have their source grounded, therefore, a $2V$ gate voltage is sufficient.

During storage, the dynamically stored values on the gates of the input transistors can discharge due to leakage through the source diffusions of the Access transistors. Only n-type diffusion is present, therefore, the voltage on these nodes will decrease, thus, increasing the gate-source voltage of the PMOS access transistors. Therefore, it is important that the gain of the feedback is sufficient to retain the stored data *i.e.* the transconductance of the NMOS devices must be greater than the PMOS devices. In the present design, the output transistors can source current

during the storage phase, for larger array sizes it would be better to include a read transistor, similar to that in an active pixel cell to prevent output current during the storage phase.

In order to read the stored data, *readb* is pulsed low and a differential output current is sunk from the bitlines I_{outn} and I_{outp}.

7.4.3.2 The Counter

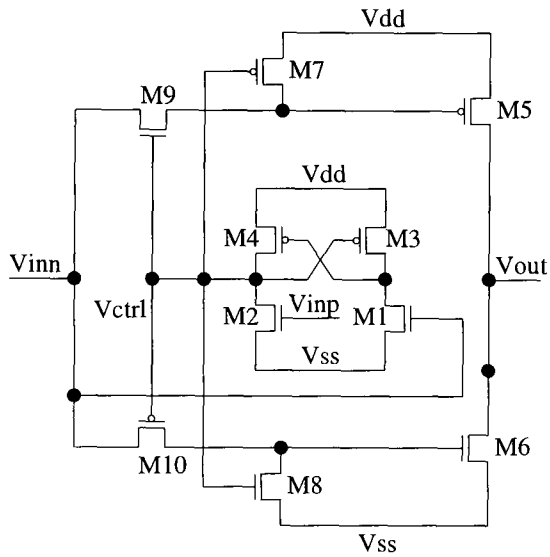


Figure 7.19: *A single-ended clock driver.*

It is assumed that the array size is large enough so that the digital noise generated by the counter is insignificant compared to that generated by the clock drivers, which charge the SRAM input buses. Therefore, there was no effort to reduce the digital noise introduced by the counter circuitry. In this design, a synchronous counter was used instead of a ripple counter, because the counter resolution was too great for a ripple counter in the given conversion time [140]. The output of the counter is converted from binary to Gray code using a series of N XNOR gates [141].

A reduced slew-rate limited driver, shown in Figure 7.19 is used to reduce the digital noise generated by the bus drivers. Operation is similar to the bus driver described in Section A.3.2. However, the voltage-sensing circuit, M_{1-4}, has been modified to:

- sense a differential input voltage.

- allow the driver to output CMOS levels.

7.4.4 Readout circuitry

The readout circuitry comprises a cascade of:

- **a current-sense amplifier,** which converts a differential current to a differential voltage.
- **a return-to-zero amplifier,** which amplifies the differential voltage to CMOS levels.
- **a d-type flip-flop,** which stores the data until it is ready for output.
- **a pad driver,** which is based on the counter output driver, shown in Figure 7.19.

Operation of the current-sense and return-to-zero amplifiers are described in the next two sections.

7.4.4.1 The current-sense amplifier

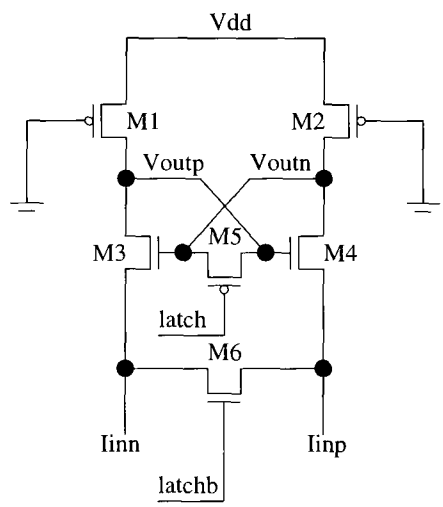


Figure 7.20: *The current-sense amplifier.*

The amplifier is adapted from the one presented in [39] and described in Section A.4. It was necessary to make two alterations to the original design. Firstly, in order to work at low supply voltages the cross-coupled inverter pair is replaced by a pseudo-nmos pair. Secondly, the column select transistors are removed and each amplifier feeds a voltage amplifier and buffer, which drive the CMOS level voltage signals off-chip.

7.4.4.2 The return-to-zero amplifier

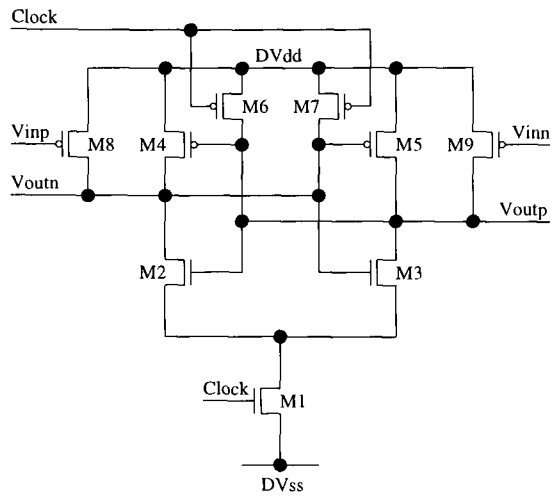


Figure 7.21: *A dynamic amplifier, which uses positive feedback to generate CMOS levels after Spalding [37].*

Unlike the latch at the output of the comparator pre-amplifier, this latch is operated at a specific time during the readout cycle. Therefore, a clocked latch can be used without introducing excessive digital noise. The latch, shown in Figure 7.21 is copied from Spalding [37] and comprises a pair of cross-coupled inverters, $M_{2,4}$ and $M_{3,5}$ with source follower input transistors, $M_{8,9}$. Operation is in two phases: balance and amplify. In the balance phase, clock is low, therefore, no current flows through the latch and the gates of the cross-coupled inverters are tied to Vdd. When clock goes high, the cross-coupled inverters are in an unstable condition (both inputs and outputs are high) and so quickly move to a stable condition, which is determined by the input voltages.

7.4.5 Experimental results

The primary aim of the experiments on the ADC section of the chip is to characterize the fixed-pattern noise. There are two possible types of fixed-pattern noise:

1. **signal dependent fixed-pattern noise,** which would limit the achievable converter resolution.

2. **constant fixed-pattern noise,** which can be subtracted in the digital domain and, provided that it is not an excessive proportion of the signal swing, does not limit converter perform-

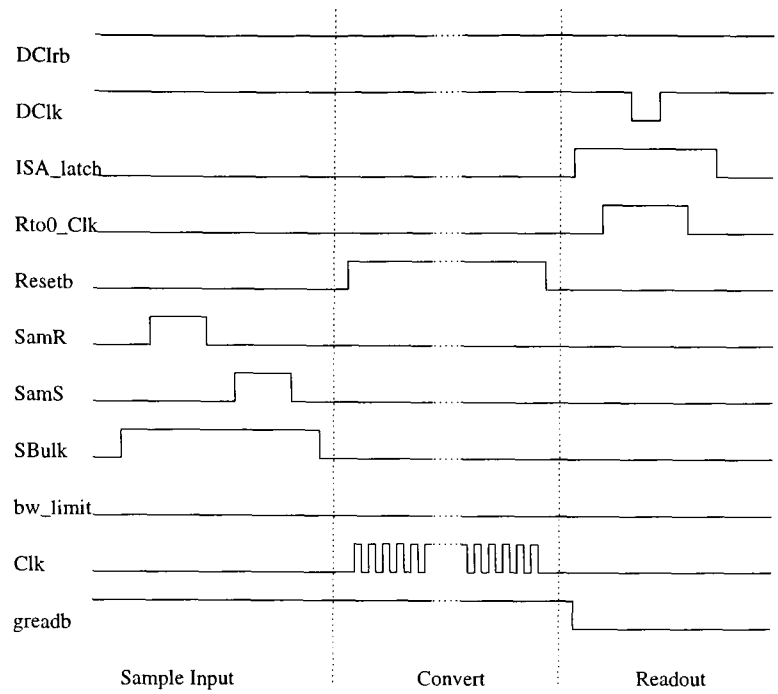


Figure 7.22: *A timing diagram for the single-slope converter array*

ance.

In order to quantify the above two effects, the single-slope converters are used to digitize a series of analogue signals which cover the entire input range of the converter. The input signals are common to the entire converter array, therefore, any difference in the output is due to fixed-pattern noise.

As shown in Figure 7.22, three phases are need to characterize the converters: sampling the input signal, conversion and readout. During the sampling phase, off-chip generated voltages are sampled onto the converter negative and positive inputs. When *Resetb* falls, the conversion process begins, delayed versions of the *Resetb* signal are generated on-chip to prepare the RAM to receive data and to start the counter. The output signals are monitored using a data analyser.

The observed digital outputs were independent of the analogue input values and ramp voltages. Further, they were independent of the selected converter. Therefore, it was concluded that the digital data was the result of offsets within the output cascade. In order to investigate further, clock signals were systematically removed from the output cascade and the output data was observed. Table 7.2 shows the results of holding clock signals constant. From these results,

Signal	Expected Result	Observed Result
DClk = 1	output remains constant	output remains same
Rto0-Clk = 0	output = 000000000000	output = 000000000000
ISA-latch = 0	output determined by offset in Rto0-amp	output remains same

Table 7.2: *The effect of removing clock signals from the output cascade. Note that "output remains same" is used to mean that the output is identical whether the signal is removed or not and is, typically, 011110011000*

it is concluded that the return-to-zero amplifier and all subsequent circuitry *i.e.* the latch and pad driver are functioning correctly. Further, the latch is a single-stage from the counter, which combined with the fact that simulation of digital circuits is likely to be more reliable than analogue circuits, is used to surmise that the counter is operational.

Since the output is unchanged if the current-sense amplifier is held in balance (ISA-latch = 0), the output data must be due to offsets within the return-to-zero amplifier. Consequently, the current-sense amplifier is not amplifying the input signal. The most likely reason for this is that the input signal is not differential. Equivalently, the output current from the SRAM cell is not sufficient to cause the current-sense amplifier to switch. It is possible that the SRAM cell is functioning correctly, but the differential current is small compared to the bias current flowing in the output buses. To verify this, the bus bias must be altered by changing the voltage on the gates of the two bias transistors. Unfortunately, these are tied to V_{dd} in the present design and, therefore, must be bonded to an output pad using focussed-ion-beam milling and deposition to perform this experiment, which, due to time constraints, is left to future work. A further possible cause of error is that the RAM cell may not store data successfully. In the storage mode, one of the gates of the cross-coupled NMOS transistors will tend to push the bias current source out of saturation and eventually cut it off, therefore, it is effectively a DRAM cell, which can discharge due to leakage currents. Although the dark current values calculated in Section 7.3.2.1 are insufficient to discharge the storage nodes, the relative isolation of the diffusion could increase the discharge rate. This would be difficult to investigate because any focussed-ion-beam deposition would greatly increase the capacitance of the storage nodes and the operation would be altered.

Unfortunately, despite extensive simulation, the analogue-to-digital converter section of the chip did not output meaningful data. The chip layout was such that there were no intermediate

outputs between the comparator input and pad outputs so it is difficult to determine the exact failure mode. However, a number of lessons can be learnt:

1. It is important to add outputs/inputs at intermediate stages of a cascade of circuits to allow trouble-shooting of new circuit topologies.
2. It can be more important to get an operational circuit than one that is optimized for the given task.

7.5 Conclusion

A number of novel circuit structures have been presented and evaluated.

- On the given process, using the gate-capacitance of the source follower transistor to store pixel data is not practical due to the rapid voltage decay. If an analogue in-pixel memory element is required, the percentage of the sampling capacitance that is composed of diffusion would have to be reduced from the present value of 60% to a few percent. This is not practical without using a specialized process that includes area-efficient capacitor structures.
- Variation in the interconnect capacitance introduced fixed-pattern noise to the double active pixel structure. This fixed-pattern noise can be cancelled using correlated-double sampling. However, in this case, the sampling capacitance reset noise is not cancelled. For practical values of the sampling capacitance, this $\frac{kT}{C}$ noise would limit the achievable pixel resolution to 8-bits, which may be unsuitable for some applications.

Chapter 8
Conclusions

8.1 Overview

The final chapter summarises the conclusions that have been presented throughout this work. In the next section, a review of this work is presented. In Section 8.3 the potential advantages of a CMOS sensor over a CCD-based imager, which were presented in Section 1.2 are reviewed in light of this research. The remaining two sections reiterate the salient issues raised through the theoretical and practical work, respectively.

8.2 Summary

In Chapter 2, a review of pixel architectures concluded that:

- The simplicity of the passive pixel results in the largest fill-factor and voltage swing. Therefore, for a given pixel pitch, the passive pixel yields the largest saturation charge, which was four times larger than that of the active pixel. This results in the best noise performance, for the pixels under consideration, sufficient for 11-bit resolution. However, the discussion of the readout structures showed that the charge-sensing readout scheme limited the achievable resolution. This is most severe as array size increases. Therefore, passive pixels are most suitable for array sizes below 250×250 pixels and low-resolution sensors (6-bits and below).

- At larger array sizes, the active pixel is preferred. While the pixel performance is inferior to the passive pixel, the readout scheme does not significantly reduce the overall achievable performance level. A significant disadvantage of the active pixel structure is that correlated-double sampling is required to suppress fixed-pattern noise caused by threshold variation of the source-follower transistor.

- The photogate pixel is unattractive because of absorption of short-wavelength light in the polysilicon electrode. This could be improved using a hybrid process, which allowed the

integration of a CCD pixel (a photogate pixel can be thought of as a single pixel CCD sensor).

- Capacitive pixels suffer from a restricted voltage swing at the pixel, which limits the achievable signal-to-noise ratio. A further disadvantage of capacitive pixels is that the *Reset* signal may need non-CMOS voltage levels. This would result in static power dissipation.

Two specific suggestions have been made to improve the performance of CMOS pixels:

1. increasing the area-to-perimeter ratio of the pixel. Since the depletion reaches the semiconductor surface at the pixel perimeter, where surface states dramatically increase thermally generated diffusion current, a careful choice of pixel shape will help to reduce dark current.
2. using non-minimum sized transistors to reduce the variation in threshold voltage and, hence increase the available voltage swing. Other advantages of increasing the size of pixel transistors are:
   - the flicker noise contribution, which is inversely proportional to transistor area is reduced.
   - the pixel capacitance is increased without increasing dark current. Consequently, provided that the pixel capacitance is fully discharged, the signal-to-noise ratio will improve.
   - if the length of the reset transistor is increased, any leakage current through the transistor will be reduced.

Further, three novel pixels were suggested:

1. an active pixel where the V_{RT} signal was provided by the *Reset* and *Read* signals. The increase in load on the driver transistors will limit the use of this active pixel to small array sizes.
2. a multiplexed pixel, where the in-pixel source follower is shared between neighbouring pixels. Experimental validation of this structure conclude that it is feasible provided that correlated-double sampling is used in such a way as to suppress the fixed-pattern noise due to variations in the gate-drain interconnect capacitance.

3. a timing scheme for a shuttered pixel to use the shutter to store the pixel reset value.

The CCD image sensor was studied to investigate where CMOS image sensing could benefit from the development of CCD imagers. An example of this is the use of post-fabrication processing, which is common to both CCD and CMOS sensors. Perhaps, the most significant area for development is in pixel technology. A CCD sensor uses buried photodiodes and biasing to reduce dark current. If CMOS sensors are to match CCD systems in low-light level imaging, research is needed to create a hybrid process with low dark current pixels. However, whether this is economically viable remains to be seen. It may be more beneficial to exploit markets where either the illumination level is controlled or low-resolution images are acceptable. In which case, present CMOS imager performance is acceptable.

A number of developments, which erode some of the traditional advantages of the CMOS sensor were discussed, namely:

- it is now possible to economically add CMOS capability to a CCD process. However, the achieved gate-length is too long for the integration of large-scale digital processing.
- a low-voltage CCD process was outlined. In this planar process, boron implants are used to reduce the inter-electrode potential barriers. Using this technology, a 1.8V clock swing achieved a sufficient charge-transfer efficiency for medium-to-large pixel arrays.
- a charge-to-digital converter was discussed as an example of image processing using CCD elements.

Whether these development are transfered from the research bench to the market place will depend on the relative value of the solid-state imaging markets. For example, the requirement for longer battery life in the camcorder market could drive the development of low-voltage CCD systems and the integration of charge-domain signal processing.

Until recently, the use of a standard CMOS process has not reduced image performance. However the continued scaling of the digital CMOS process could degrade image performance due to:

- increased dark current as tunnelling currents may dominate thermally-generated dark current beyond the $0.18\mu m$ generation.
- the reduction in supply voltage will severely limit the operation of present pixel architectures.

- silicide layers are relatively opaque and, hence, must be blocked around the pixel sites.
- increased number of metal layers may pose problem for sensor arrays. For example, all the layers may have to be included across the array.
- shallower vertical dimensions will cause a blue shift in the spectral response.
- silicon-on-insulator technology may be unsuitable for sensor design.

There are a number of less significant advantages to moving to new technologies:

- stackable contacts and finer lithography will result in an increase in pixel fill-factor for a given pixel pitch.
- increased capacitance *per* unit area will tend to improve the signal-to-noise ratio of a standard pixel.

Summarizing, there are numerous problems that must be addressed before scaled processes can be used for CMOS image sensing. Indeed, it may be that it is not beneficial to use technologies beyond the $0.5\mu m$ process. Certainly, the development of CCD technology will yield more benefit to imagers than the evolution of the standard CMOS process. It is expected that to address viewed imaging markets hybrid CMOS processes must be developed. However, $0.5\mu m$ technology should be adequate for markets where image quality is not the paramount criterion, for example, where large-scale digital signal processing is integrated with the pixel array.

In Chapter 6, power consumption estimates were derived for selected converter architectures and for the functions required for quantization. As array sizes increase, it was shown that the power required to charge the column capacitance and drive digital output buffers would become prohibitively high. For example, for a 1000×1000 pixel imager, the two functions could consume 100mW. In order to reduce the sampling current, a novel technique was proposed where two sets of sampling capacitances were used in order that the sampling time was maximized and, hence, power consumption was minimized. If the digital output buffer power consumption is too high, two options exist:

1. analogue-to-digital conversion can be performed off-chip, resulting in a two-orders-of-magnitude reduction in power consumption for a 1000×1000 pixel image sensor. However

the reduction in sensor chip power consumption is at the expense of increased system power and increased system design complexity to maintain a quiet off-chip environment.

2. the output voltage swing can be reduced. However, this is only an option for custom applications — for a multipurpose chip, CMOS levels are required.

Experimental work is needed in this area to compare the image degradation due to increased sensor-chip power consumption and digital noise with the increase in noise coupled to an extended analogue signal path.

If it is decided to integrate a converter with the sensor array, the power consumption analysis showed that:

- below 500×500 pixels at 8-bit resolution, a serial converter was preferred to a semi-parallel approach because the power consumption was similar, yet the area required for a serial converter is much smaller. At 10-bit resolution, a semi-parallel approach became more attractive at smaller array sizes (250×250 pixels) and at 6-bit resolution at larger sizes (2000×2000 pixels).
- for 6- and 8-bit resolution converters, the successive-approximation converter multiplexed between the minimum number of columns, was most power efficient.
- at 10-bit resolution the cyclic, pipeline and 2-step flash converters multiplexed between the minimum number of columns were the most power-efficient converters .

In addition to the above recommendations, a low-power mode of operating the single-slope converter was described. By increasing the permitted decision time, the comparator bias current was reduced at the expense of a fixed offset. This converter was incorporated into the design of the test chip, *Ginger Dancer*.

In the analysis in Chapter 6 the two extremes of multiplexing were considered: serial conversion or a semi-parallel converter shared between the minimum number of columns. For some converters, an optimum solution may lie between these two extremes. The analysis showed that there is no power advantage gained by increasing multiplexing beyond the point where amplifiers are slew-rate (rather than bandwidth) limited. Indeed, for a given converter, the optimum parallelism for power and area is likely to be at the cross-over between bandwidth and slew-

rate limiting. For this reason, it is unlikely that a pixel-level converter will ever be the optimum power solution.

A test chip comprising an array of multipurpose active pixels and single-slope converters was fabricated and tested. The multiplexed pixel was shown to be a feasible architecture provided that the fixed-pattern noise introduced by variations in the gate-drain overlap capacitance was suppressed using correlated-double sampling. However, in this mode, the $\frac{KT}{C}$ noise due to the sampling transistor channel charge was not suppressed. In order to mitigate this effect a larger sampling capacitance could be used. However, this would reverse the fill-factor benefit of using this pixel. Perhaps the simplicity of the standard active and passive pixels will be a sufficient benefit to stop the wide-spread adoption of alternative pixel structures.

Evaluation of the shuttered pixel showed that the sampling capacitance discharge too rapidly for this mode of operation to be viable. If a pixel memory is required, further experimentation with capacitor structures and improved shielding is required. However, an off-focal plane memory is likely to be a more attractive solution.

Unfortunately, the design did not allow individual elements to be tested. For example, it was unclear whether the RAM cell or current-sense amplifier was not functioning. In order to determine this, expensive alterations must be made using focussed-ion-beam milling and deposition. This could have been avoided if the initial circuit had been designed with testing in mind. This was exacerbated by the inclusion of so many untried circuits on a single chip. For example, it may well have been better to use library cells for the memory array. Two circuit techniques which show promise were not evaluated on *Ginger Dancer*— the no-V_{RT} pixel and using two sets of sampling capacitors. As array sizes increase, two sets of sampling capacitors will yield a significant power saving. Therefore, it is important to evaluate the level of fixed-pattern noise and capacitive coupling which may be introduced by this technique.

8.3 A review of the advantages of the CMOS sensor over a CCD imaging system

In Section 1.2, a number of possible advantages of CMOS image sensors over CCD-based imaging systems were highlighted. These are evaluated in turn:

- **Standard process.** The cost advantages of using a standard process are reduced if ex-

pensive post-fabrication treatment, such as the addition of colour filters and micro-lens arrays, is needed. However, in the future, this advantage is likely to be lessened still further because:

1. In order to compete with CCD sensors it is necessary to suppress dark current. This will necessitate a move away from a standard process to one allowing buried photodiodes.
2. Technologies beyond the $0.18\mu m$ process are predicted to have a supply voltage of 1.8V. Without aggressive threshold voltage scaling, this will be insufficient to operate an active pixel. Consequently, unless new pixel architectures are designed, the standard process will no longer be suitable for the manufacture of CMOS sensors.

- **Power.** The present day power advantage of a CMOS image sensor over a CCD imaging system will be eroded because:

  1. High-voltage clocks will no longer be required to maintain charge-transfer efficiency.
  2. While single-chip CCD imagers are unlikely, two-chip systems are possible. For large array sizes, power consumption may prohibit a single-chip CMOS imager. Therefore, power consumption will be similar for a large-array size imager in both CMOS and CCD technologies. At medium and small array sizes, below 500×500 pixels a significant power advantage will remain, unless a single-chip CCD sensor is produced.

  In practice, sensor power may not be a crucial issue. In a digital camera, the memory elements and shutter motor use sufficient power to mitigate any sensor power saving. Further, if a flash unit is required on a CMOS camera, while not on a CCD camera, any power saving is further eroded.

- **Size.** For complete camera systems, CMOS sensors will retain a size advantage at medium and small array sizes. However, for applications such as a dental probe, where size is a critical design criterion, a CCD sensor chip can be manufactured on the probe head, while the processing chips are located at the receiving unit.

- **Design resources.** It remains true that design in CMOS is supported by developed cell libraries and simulation tools.

- **Addressable pixels.** CCD image sensors continue to output serial data, while CMOS sensors can be addressed randomly. Further, it is possible to produce CMOS pixels that can be read in continuous time, for example, the logarithmic pixel.
- **On-chip integration of signal-processing.** Large-scale integration of signal-processing is not feasible on present CCD-CMOS processes. Therefore, CMOS sensors can benefit from a considerable advantage, particularly at small to medium array sizes where the chip power consumption is not prohibitive. In the future this advantage could be eroded if there is sufficient market demand for such sensors, however, some advantage is likely to remain, provided that CMOS sensors continue to use near to state-of-the-art processes.

The primary advantage of CCD sensors remain because of two factors:

1. CMOS pixels are subject to $\frac{kT}{C}$ noise, which can be cancelled using a frame memory.
2. High dark current, which limits the signal-to-noise ratio and, thus, reduces the camera sensitivity. Process steps can be taken to improve this situation, however, this is at the cost of moving away from a standard process.

However, two developments could improve the sensitivity of a CMOS sensor: a low-threshold voltage transistor and a reduced-dark-current pixel.

Considering the above points, there are clearly some applications, such as the Gameboy camera, where a CMOS sensor provides benefits over a CCD system. As array size and required resolution increase, CCD systems become more attractive. The other area where a CMOS sensors can compete at an advantage over CCD systems is if signal processing can be integrated on-chip. For example, a 6 to 8-bit analogue-to-digital converter on a small-to-medium imaging array would be better implemented as a CMOS sensor, provided that the camera product was for use in well-lit environments.

8.4 Recommendations from theoretical considerations

If the performance of CMOS imagers is to improve, it is critical that reduced dark current pixels are fabricated. This will mean a departure from standard processes and, hence, an increase in cost. Whether this is economically viable remains to be seen. However, there is likely to be a

split within the CMOS sensor products between high-resolution medium-to-large array sensors on hybrid processes and low-resolution, small array size sensors incorporating significant signal processing on a non-state-of-the-art industry-standard process. It has been argued that for large sensor arrays, power consumption and crosstalk will make the integration of significant processing unattractive and, therefore, two chip sensors solutions will dominate. If this is so, this market is likely to be dominated by CCD sensors.

At present, the passive pixel has been generally disregarded because of its poor signal-to-noise ratio. However, this work has shown that, for small arrays, the passive pixel can give an improved signal-to-noise ratio over an active-pixel sensor.

8.5 Recommendations from practical work

Testing *Ginger Dancer* highlighted a number of important issues:

- The shape and/or environment of a pixel can strongly influence the dark current level. It was hypothesised that the area-to-perimeter ratio for a pixel should be maximized to reduce the effect of surface state and, hence, reduce dark current.
- Capacitance discharge rendered the shuttered-pixel mode impractical. Further experiments are required to determine whether this discharge was due to the photogeneration of charge at the sampling capacitance or the crosstalk of charge from neighbouring pixels.
- The routing of extra signals to a pixel leads to difficulties in layout and an increase in fixed-pattern noise due to capacitive coupling. While it is possible to suppress some of this fixed-pattern noise using correlated double-sampling, it is probably best practice to use the simplest pixel structures possible *i.e.* the passive pixel for small arrays and low-resolution sensors, otherwise the simple active pixel.

8.6 A final thought.

From the preceding discussion it is clear that the CMOS image sensor offers considerable advantages over CCD imaging systems where considerable image processing can be integrated with the pixel array. As array sizes increase, this advantage is reduced due to the increase in

chip power consumption and generated digital noise, which causes image deterioration. Further, CCD systems are likely to become more integrated until only two chips are required to provide the same functionality as the CMOS sensor chip. While this will lead to an increase in system power consumption, it may produce higher quality images due to the dedicated processes used for the sensing and processing chip. Further, the two chip solution may be more flexible than a single chip solution.

In a study such as this, it is relatively easy to argue what is the best solution technically. However, history has shown that other factors may be more important in determining market success. For example, in the dominance of Intel processors and Microsoft software or the adoption of VHS as the video standard. For similar reasons, I believe that momentum of companies like Sony will allow CCD based systems to continue to dominate the camcorder and digital camera markets.

Appendix A
Driving interconnect lines

A.1 Overview

As imager array size is increased, the signals for pixel and column amplifier operation must be driven on increasingly capacitive bit-lines. In some cases, for example, the pixel reset signal, line-drivers must be used, which leads to increased power dissipation. Other signals, such as the output from a pixel or an SRAM are driven by near-minimum-sized transistors, which may provide insufficient current as the bit-line capacitance is increased [8]. A possible solution is to reduce the voltage swing, for example, by current-mode operation. A further benefit of this approach is a reduction in generated digital noise [8].

As a bit-line length is increased, the signal-propagation delay may become significant compared to the system clock. The next section presents the formulae derived by Seevinck that can be used to estimate the transmission line delay [8].

A.2 Transmission line delay [8]

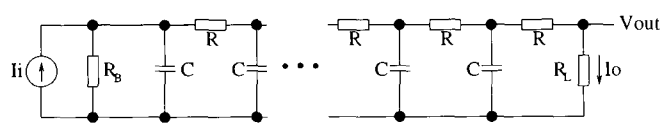


Figure A.1: *The distributed RC transmission line model for interconnect lines.*

The delay along a transmission line, relative to the input signal, δt, is given by

$$\delta t = \frac{R_T C_T}{2} \times \frac{R_B + \frac{R_T}{3} + R_L}{R_B + R_T + R_L} + R_B C_T \times \frac{R_L}{R_B + R_T + R_L} \tag{A.1}$$

where R_T and C_T are the total line capacitance and resistance, respectively. Equation A.1 shows that the transmission line delay can be reduced by minimizing R_B, the case with an ECL driver, or R_L the case with a current-mode signal. For voltage mode signals, where

$R_L \gg R_B, R_T$, the delay is given by

$$\delta t_v = \frac{R_T C_T}{2} \times (1 + \frac{2R_B}{R_T}) \tag{A.2}$$

If $R_B > R_T$, which is usually the case for CMOS circuits, the delay will be much larger than the intrinsic line delay, $\frac{R_T C_T}{2}$. For current-mode operation, the output resistance is low, ideally zero, and Equation A.1 reduces to

$$\delta t_i = \frac{R_T C_T}{2} \times (\frac{R_B + \frac{R_T}{3}}{R_B + R_T}) \tag{A.3}$$

This is approximately an order of magnitude less than the voltage-mode delay for a typical SRAM memory. Figure A.2 shows the delay versus load resistance for a memory line across a

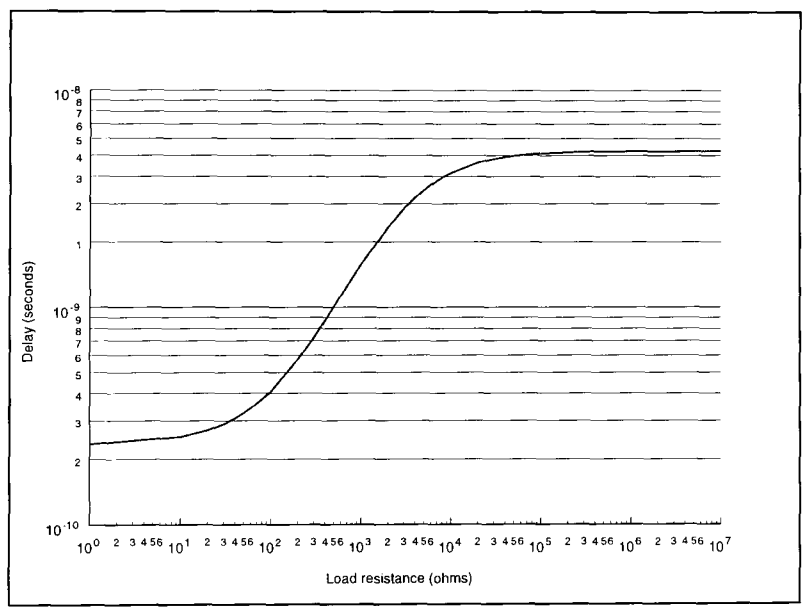


Figure A.2: *Modelled transmission line delay.*

1000 columns of $10\mu m$ pitch assuming a total capacitance of $2pF$ and resistance of 250Ω with a driver resistance of $2.5k\Omega$. If the load resistance is greater than $1K\Omega$, the transmission line delay is of the same order as a typical system clock, and must, therefore, be considered in the design of imagers.

A.3 Voltage-mode drivers

In Section A.2, it was argued that current-mode operation was preferable to voltage-mode in terms of delay and digital noise. However, some signals must be voltage-mode, for example, off-chip digital signals and the pixel reset signal. These two cases will be considered in the remainder of this section.

A.3.1 Driving signals off-chip

The connections between the power pads of an integrated circuit and the board can be modelled as a serial inductance, shunt capacitance and serial resistance. The bond-wire inductance can cause voltage spikes on the supply line. If the total capacitance seen by the driver is $50pF$, and the signal rise-time is $2nS$, the required charging current, I is given by

$$I = C \times \frac{dV}{dT} = 50pF \times \frac{5V}{2ns} = 125mA \tag{A.4}$$

The current variation caused by the charging current produces a voltage drop, V, over any serial inductance, for example, if the bond-wire inductance has a value of $10nH$, the voltage drop is given by

$$V = L \times \frac{dI}{dt} = 10nH \times \frac{125mA}{2nS} = 0.625V \tag{A.5}$$

In order to minimize this voltage drop, the slew-rate must be controlled, for example, by using two driving transistors, the second of which is switched on when the output reaches a given level [142].

A.3.2 The reset signal

The most effective means of reducing the digital noise associated with a voltage-mode driver is to reduce the output swing. In the case of the reset signal, the output must reach V_{dd}, however, it is not necessary for the output to fall to V_{ss}. Indeed, Reset is often held above V_{ss} to provide blooming protection.

The reduced-swing clock driver, shown in Figure A.3, uses a fast-voltage-sense translator as positive feedback to adjust the output voltage and limit the output swing to 1V [143]. Operation

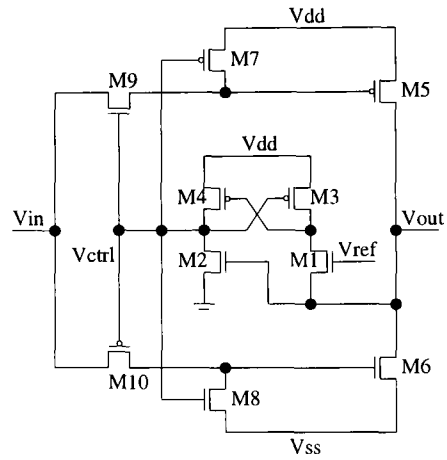


Figure A.3: *A schematic of a reduced-swing driver.*

is described for a low to high transition at the input. Initially the output is high, therefore, V_{ctrl} is low and the input signal is passed to the NMOS output driver, M_6, which starts to discharge the output node when the input makes a low-to-high transition. When $V_{out} < V_{ref} - V_{out}$ the voltage sense translator switches state and V_{ctrl} goes high turning M_{10} off and also discharging the gate of the driver transistor, M_6 via M_8. Provided that the output node has not fully discharged this implements a reduced swing driver. The swing range can be controlled by altering V_{ref}. Note that the short-circuit current is eliminated since both drivers are not on at the same time. Also the output node is dynamic, so bus restorers may be needed. A further advantage of this circuit is that it limits slew-rate. The output transistors are turned on through the RC circuit formed by the pass transistors, $M_{9,10}$ and the driving transistor gate capacitance. The turn-off time is determined by the size of transistors $M_{7,8}$ and the capacitance at the gate node of the driver transistors.

A.4 Current-mode drivers

The basis of operation for a current-mode amplifier is to provide a virtual short circuit to input currents. Such a circuit, the current conveyer, is shown in Figure A.4. It is, essentially, a differential current buffer. The resistances, R, are bitline loads that bias the lines near V_{dd}. In order to provide a virtual short circuit, the gate-source voltages of transistors $M_{5,1}$ and $M_{4,6}$ are summed so that each gate-source voltage pair contains one transistor from each side of the differential circuit. Therefore, to first order, the line voltages remain equal.

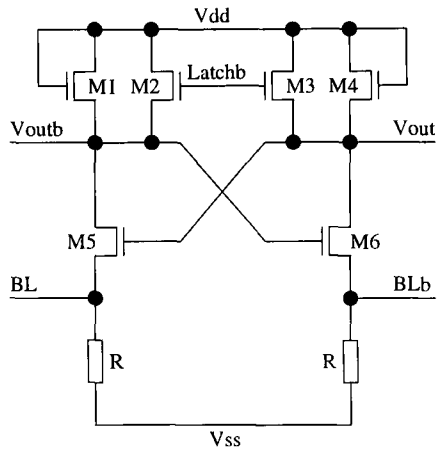


Figure A.4: *The current conveyer after Seng [38].*

In order to decrease the decision time of a current to voltage amplifier, the highly-capacitive sense nodes are distinct from where the sense amplifier signal is developed [39]. Blalock de-

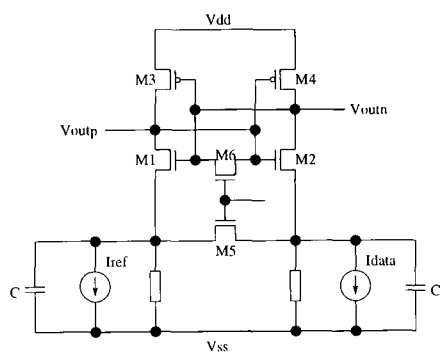


Figure A.5: *A current-sense amplifier after Blalock [39].*

veloped such an amplifier, which is shown in Figure A.5. Operation is in two phases: precharge and signal amplification. During precharge M_5 and M_6 force the bit-lines and amplifier outputs to equal potentials respectively. The amplifier is balanced in this state, therefore, equal current flow through the branches $M_1 - M_3$ and $M_2 - M_4$. Consequently, half the differential input current, $\Delta I = I_{data} - I_{ref}$ must flow through M_5. The amplification stage commences when transistors M_5 and M_6 are switched off. M_1 must then source the current that previously flowed through M_5, therefore, V_{outn} increases. Similarly, the reduction in current through M_2 forces a reduction in V_{outp}. This initial trajectory for the voltage difference is quickly amplified to full-scale by positive feedback [39]. Unfortunately, the bit-lines are discharged during the amplification stage, because no current flows through the latch.

A.5 Conclusion

A number of issues associated with the driving of large capacitances have been discussed in this chapter. Firstly, it was shown that the delay in driving a bit-line is significant for a 1000-column CMOS imager. Possible driving circuits for voltage-mode signals and amplifier circuits for current-mode signals were presented. These circuits are developed and included in the *Ginger Dancer* chip.

Appendix B
Noise

B.1 Overview

A noise signal has random amplitude and phase. Its mean value over time is zero, therefore, it is described in terms of power. This section describes the different noise mechanisms [79, 144] before giving the noise models used for the devices considered in this thesis.

B.2 Noise sources

Noise sources are given in terms of a spectral density, which gives the noise power *per* unit frequency, measured in Hertz. Unless otherwise stated, noise sources are uncorrelated, hence, the total spectral density is the sum of the individual densities. The rms noise current over a frequency range, $f_1 < f < f_2$, is calculated by integrating the spectral noise density:

$$\bar{i}^2 = \int_{f_1}^{f_2} \sum_{j=1}^{n} S_{ij} df \tag{B.1}$$

B.2.1 Thermal noise

Thermal noise is caused by the random, thermally excited, vibration of the charge carriers in a conductor. It is present independently of any current flowing. In a conductor of resistance R, thermal noise is modelled by a shunt current generator with a spectral density, S_{iR}, given by

$$S_{iR} = \frac{4kT}{R} \tag{B.2}$$

Equation B.2 states that the thermal noise spectral density is independent of frequency, which is often described as a white noise spectrum.

B.2.2 Shot noise

Shot noise is a white noise source associated with direct current flow in diodes and transistors. It is caused by individual carriers flowing over a potential barrier, for example, associated with the $p-n$ junction in a diode. Device current is composed of a large number of random independent current pulses, which are individual carriers crossing the junction. The transition of carriers across a $p-n$ junction is a random event that is dependent on the carrier having sufficient energy to overcome the junction potential barrier. Shot noise is the fluctuation in the number of carriers crossing the junction. The spectral density, S_{is}, of shot noise is given by

$$S_{is} = 2qI \tag{B.3}$$

It has been shown that the sum of the reverse and forward current shot noise is equivalent to device thermal noise[145].

B.2.3 Flicker or $\frac{1}{f}$ noise

This is a type of noise that is found in all active devices and that is always associated with the flow of direct current. As the name suggests, the spectral density of $\frac{1}{f}$ noise increases without bound as frequency decreases. Flicker noise displays a spectral density of the form:

$$S_{if} = \frac{KI^a}{f^b} \tag{B.4}$$

where K is a device dependent constant; $0.5 < a < 2$ and $b \approx 1$.

B.2.4 Noise due to sampling

There are two noise sources introduced by sampling [146]. Namely, $\frac{kT}{C}$ noise and partition noise. $\frac{kT}{C}$ noise is the sampled thermal noise generated by the sampling transistor. Partition noise is generated when the sampling transistor is turned off. On turn-off, initially, the channel charge transport mechanism is dominated by self-induced drift. However, as the carrier concentration drops, self-induced fields reduce to the order of thermal fields and the dominant transport mechanism changes to thermal fields. Thermal diffusion is a stochastic process, therefore, it generates noise. The total root-mean-square noise voltage, $\bar{v}_n$, introduced by sampling

is given by

$$\bar{v}^2 = \frac{kT}{C_s} + \frac{2kT}{\pi^2 WLC_{ox}} \tag{B.5}$$

where C_s is the sampling capacitance and WLC_{ox} is the MOSFET channel capacitance.

B.3 Noise models

B.3.1 Diode

Both flicker and shot noise are present in a diode. In forward bias the shot noise component of the forward and reverse currents must be summed. Only diodes in reverse bias are considered in this text, in which case the total noise spectral density, S_i is given by

$$S_i = 2qI_{DS} + \frac{KI_{DS}^a}{f} \tag{B.6}$$

B.3.2 MOSFET

If parasitic resistances are ignored, (which contribute thermal noise) the noise generated in a MOSFET is due to channel thermal and flicker noise. In the subthreshold region, thermal noise can also be considered to be shot noise.

B.3.2.1 Thermal noise: saturation region

Thermal noise is modelled by a spectral density, S_{iRS}, given by

$$S_{iRS} = \frac{8}{3}kTg_m(1 + \frac{1}{g_{mb}}) = \frac{8}{3}kT \times (1 + \frac{1}{g_{mb}}) \times (\mu C_{ox}\frac{W}{L}\Delta V_{GS}) \tag{B.7}$$

When referred to the input of the transistor the noise current spectral density is divided by the square of the transistor small-signal transconductance to yield an equivalent noise voltage spectral density, S_{Veq}, which is given by

$$S_{Veq} = \frac{8}{3}\frac{kT}{g_m}(1 + \frac{1}{g_{mb}}) = \frac{8}{3}kT \times \frac{1 + \frac{1}{g_{mb}}}{\mu C_{ox}\frac{W}{L}\Delta V_{GS}} \tag{B.8}$$

B.3.2.2 Thermal noise: linear region

In the linear region the thermal-noise-spectral density is given by

$$S_{iR} = 4kTg_{ds} = 4kT\mu C_{ox}\frac{W}{L}\Delta V_{GS} \tag{B.9}$$

which, when referred to the input of the transistor, is equivalent to a voltage spectral density given by

$$S_{Veq} = 4kT \times \frac{g_{ds}}{g_m^2} = 4kT\frac{\Delta V_{GS}}{\mu C_{ox}\frac{W}{L}V_{DS}^2} \tag{B.10}$$

B.3.2.3 Thermal noise: subthreshold region

It has been shown [145] that the thermal noise present in the drain current of a MOSFET operating in the subthreshold region is modelled by a spectral density, S_{iR}, given by

$$S_{iR} = 2qI_{sat}(1 + e^{-\frac{V_{ds}}{U_T}}) \tag{B.11}$$

where $I_{sat} = I_o e^{\frac{nV_G - V_S}{U_T}}$ and corresponds to the saturation current at the given gate voltage. This value gradually increases, to twice this value, as the device enters the linear mode of subthreshold operation, ($V_{ds} < 5U_T$), and the shot current from the drain becomes increasingly significant.

The gate referred voltage noise spectral density is given by

$$S_{Veq} = \frac{2qU_T^2}{n^2 I_{sat}}(1 + e^{-\frac{V_{ds}}{U_T}}) \tag{B.12}$$

B.3.2.4 Flicker noise

Flicker noise is explained by the carrier-density-fluctuation model, which describes the variation in the channel free carrier concentration. The variation is due to the capture and release of carriers by traps. There is a different bias dependency in the n- and p-channel devices: little bias dependency is shown in NMOS devices, whilst the flicker noise in PMOS devices increases as the subthreshold region is entered from strong inversion. For simplicity this effect is ignored,

the following formula is used to calculate flicker noise for MOSFETs in all regions of operation

$$S_{if} = \frac{K_F I_{DS}^a}{C_{ox} L^2 f} \tag{B.13}$$

which referred to the input of the transistor, yields a voltage spectral density given by

$$S_{Veq} = \frac{K_F}{2 f \mu C_{ox}^2 W L} \tag{B.14}$$

Equation B.14 shows that then flicker noise is inversely proportional to channel area, due to the averaging of the number of recombination centres as channel area increases [147].

Appendix C
Memory Cells

C.1 Overview

There are two generic types of memory cells:

1. **DRAM.** A DRAM cell uses an isolated capacitor to store the data value.
2. **SRAM.** A SRAM cell uses a positive feedback loop to store data. If the stored value is corrupted, the feedback loop will reassert the correct value.

This appendix considers the suitability of SRAM and DRAM for integration on an image-sensor chip.

C.2 DRAM cells

A DRAM cell and associated readout mechanism is shown in Figure C.1. Readout operation is as follows:

1. the sense-lines, D and $\bar{D}$ are precharged to $\frac{V_{dd}}{2}$.
2. the column-sense amplifier is enabled, the column is selected and the precharge circuit is disabled.
3. the memory cell is accessed. The stored charge causes a change in potential on column D. A differential amplifier is used to amplify the column voltage difference to CMOS levels.
4. if required, the column sense-amplifier is used to rewrite the memory contents to the DRAM cell. Note that this consumes considerable power because the column amplifier must drive the highly capacitive column-sense lines.

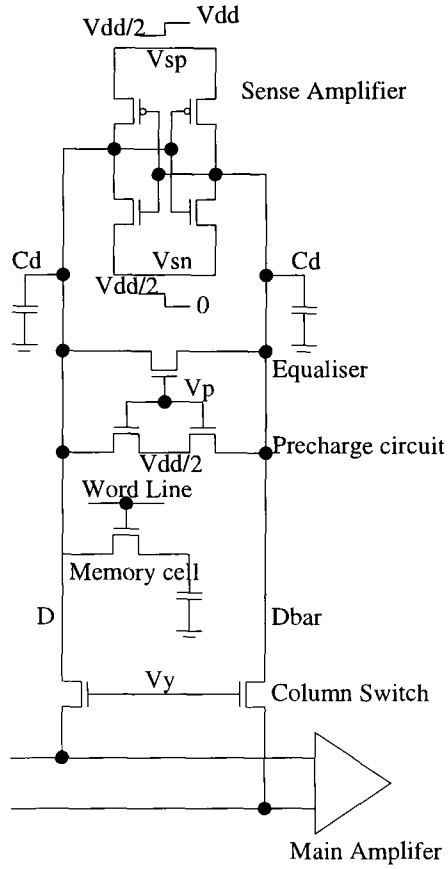


Figure C.1: *DRAM readout circuitry.*

The disadvantages of a DRAM cell are[148]:

- like the passive pixel cell, the readout charge causes a small voltage change on the sense lines. Consequently, in a mixed-signal environment, the readout process is susceptible to crosstalk.
- true differential operation is not possible, though two independent cells could be used in a pseudo-differential scheme.
- readout is destructive.
- a refresh operation may be required to prevent a stored one discharging below the column amplifier threshold.
- additional processing may be required to realize sufficient capacitance within the pixel pitch.

- photo-induced or thermal leakage currents may corrupt stored data.

C.3 SRAM cells

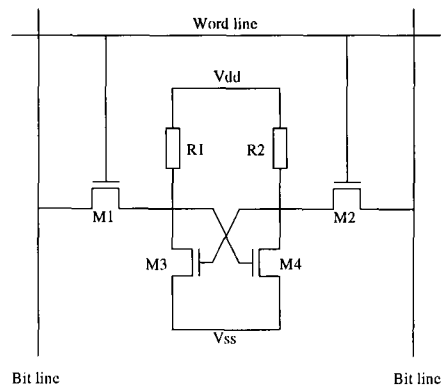


Figure C.2: *A resistive-load SRAM cell.*

Figure C.2 shows the high-resistance load SRAM memory cell, which is commonly used in memory chips. Polysilicon resistances R_1 and R_2 supply current to pull up nodes N_1 and N_2. Using multiple polysilicon technology, the resistances can be formed over transistors, thus, saving cell area. In a standard CMOS process, if a highly-resistive layer is not available, the 6-transistor cell, shown in Figure C.3 is used instead. An advantage of the 6T cell is that the

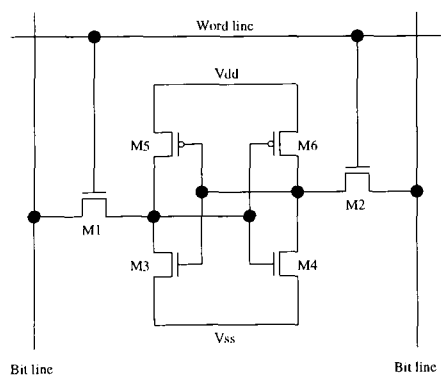


Figure C.3: *A six-transistor, PMOS-load SRAM cell.*

PMOS transistor reduces the leakage current. Therefore, the NMOS threshold voltage can be reduced without greatly increasing static power dissipation.

The significant disadvantages of an SRAM cell are:

1. **Size.** a SRAM cell contains 6 or more elements, which as discussed in Section C.3.1 are not minimum size. Whereas, a DRAM cell contains two elements.

2. **digital noise.** The SRAM cell is a cascade of two inverters, which generate switching noise. For example, Schults reported that a 512×15 embedded SRAM generates $\frac{dI}{dt} = 8.2mAns^{-1}$ at $3.3V$ [149], which, given a bond-wire inductance of $10nH$, causes a power supply disturbance of $0.1V$.

The SRAM cell is preferable to the DRAM cell for low-voltage, low-power operation because, during the storage phase, there is a wide voltage margin against external noise [150]. For example, at $3V$ supply, a one stored in a DRAM cell will be $2V$ and must not discharge below $1.5V$ if a half-supply-voltage precharge scheme is used.

C.3.1 Static noise margin [9]

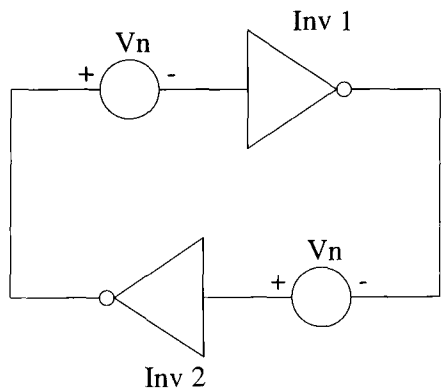


Figure C.4: *A flip-flop comprised of two inverter. Static noise voltage sources, V_n, are included.*

During a read access, the bit lines are precharged and effectively shunt the load elements. This reduces the gain of the two inverters making the cell more susceptible to noise. The static noise margin of the cell is defined as the maximum noise value, V_n, that can be tolerated by the flip-flop, which comprises the inverters formed by Transistors M_{3-6} in Figure C.4, before changing states. The static-noise margin for a six-transistor cell is given by

$$SNM_{6T} = V_T - \left(\frac{1}{k+1}\right)\left\{\frac{V_{dd} - \frac{2r+1}{r+1}V_t}{1 + \frac{r}{k(r+1)}} - \frac{V_{dd} - 2V_T}{1 + k\frac{r}{q} + \sqrt{\frac{r}{q}(1 + 2k + \frac{r}{q}k^2)}}\right\} \quad \text{(C.1)}$$

where $r = \frac{\beta_{3,4}}{\beta_{1,2}}$; $q = \frac{\beta_{5,6}}{\beta_{1,2}}$ and $k = \left(\frac{r}{r+1}\right)\left\{\sqrt{\frac{r+1}{r+1-\frac{V_{dd}-V_T}{V_{dd}-\frac{V_T}{r+1}}}}-1\right\}$. The static-noise margin depends on β ratios, V_{dd} and V_T, but not the absolute value of the transistor transconductances. To maintain a positive static-noise margin, there is a minimum supply voltage that the cell can operate at, which for the 6T-cell is about $2V_T$ [151].

C.4 Conclusion

The basic properties of the SRAM and DRAM cells have been discussed. It has been argued that the SRAM cell is preferable to the DRAM cell in a low-voltage mixed-signal environment. However, if the supply voltage is reduced to about $2V_T$ the SRAM cell will no longer function. With a suitable precharge scheme, the DRAM cell will operate provided that the write-read interval is sufficiently small.

Appendix D
Correlated Double Sampling

D.1 Overview

Correlated-double sampling was introduced by White to eliminate $\frac{kT}{C}$ noise and suppress $\frac{1}{f}$ noise from the floating-diffusion output amplifier in CCD sensors [40]. A typical block diagram

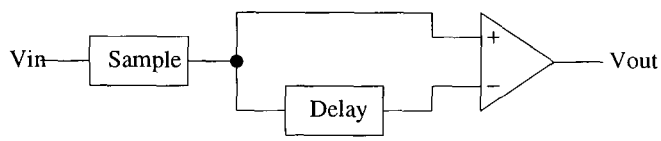


Figure D.1: *The correlated-double sampling operation.*

for a CDS operation is shown in Figure D.1. The CDS operation samples a signal twice, once at time t and then again at a time $t + \Delta t$. In a CCD sensor the CDS operation is performed on the output amplifier. The first sample is taken after the floating-diffusion node has been reset to V_{RT}. A second sample is taken after the charge packet has been dumped on the charge-sensing node. The difference between the two samples is due to the sensed charge packet and random noise. Recently, the technique has been applied to CMOS active-pixel sensors to suppress fixed-pattern and $\frac{1}{f}$ noise.

D.2 A mathematical description of CDS applied to a CCD output amplifier

Numerous attempts have been made to derive the spectral response of reset noise observed in CCD charge-detection circuits. In 1974, White presented a simple analysis which concluded that the CDS transfer function was given by [40]

$$T(s) = T_o \frac{1 - e^{-s\tau}}{1 + \frac{s}{\omega_o}} \tag{D.1}$$

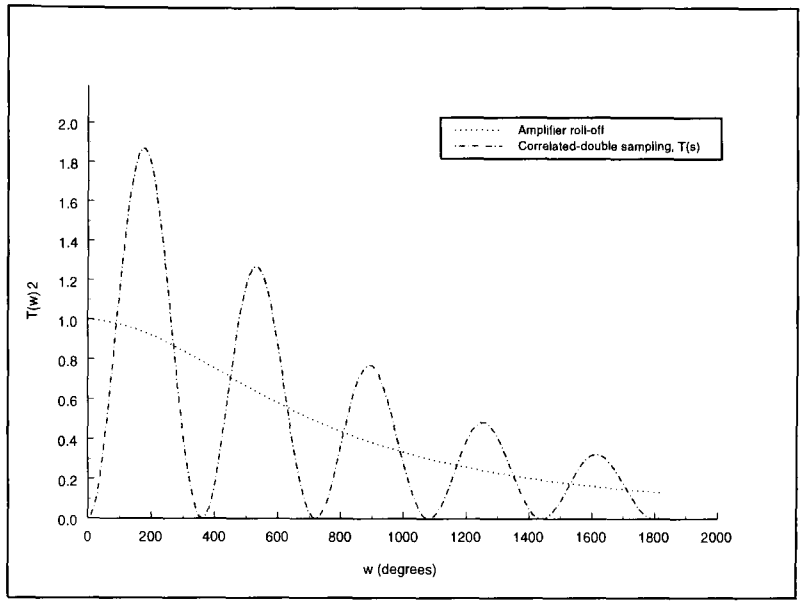


Figure D.2: *Filter characteristic of correlated-double sampling with* $\tau = \frac{T}{2}$ *after White [40].*

where T_o is the DC signal gain; τ is the time delay between the end of the reset signal and the end of the sample pulse and ω_o is the bandwidth of the amplifier. Equation D.1 is plotted in Figure D.2. It can be seen that at multiples of τ there are zeros introduced into the transfer function which suppress noise. The most significant zero is at $f = 0$ because this cancels any DC term, including offsets and the sampled reset value. This zero also serves to suppress $\frac{1}{f}$ noise. The zeros at other frequencies act to shape the output noise spectrum but are not considered further.

While the analysis presented by White is useful to understand the basic operation of correlated-double sampling, it does not consider a number of significant points. Namely, it is assumed that there is no correlation between consecutive voltage levels after the completion of reset and the effect of sampling is ignored[152]. A more rigorous analysis has been presented by Hynecek in two correspondences [152, 153]. The function given by Hynecek for the noise-power spectral density measured at the output of the amplifier is

$$V_n^2(f) = |H_a(2\pi f)|^2 A_o^2 \left[V_g^2 + 4\pi S_o \left(\frac{S_c(2\pi f)}{S_o} \right) \right] \tag{D.2}$$

where $|H_a(2\pi f)|$ is the normalized frequency response of the amplifier; A_o is the DC gain of

the amplifier; V_g represents the noise generated in the amplifier; $S_o = \frac{1}{\pi}kTR$ where R is the source resistance and S_c is given by

$$S_c(\omega) = \frac{1}{\pi}\left(\frac{kT}{C}\right)\left[\frac{(1-\zeta)\omega_f}{\omega_f^2+\omega^2} + \frac{1}{2}\tau\zeta^2\frac{\sin\left(\frac{\omega\delta}{2}\right)}{\frac{\omega\delta}{2}}\right] \tag{D.3}$$

where $\zeta = \frac{\delta}{\tau}$ is the duty cycle of the reset complement and ω_f is the bandwidth of low-pass filter formed by the sampling capacitance and the source resistance. Using Equation D.3 the amplifier bandwidth and reset duty cycle can be varied to optimise the system noise performance.

D.3 CDS applied to an active-pixel CMOS sensor.

In an active pixel sensor, the CDS operation is applied to cancel fixed-pattern noise arising from offsets within the pixel cell and sometimes to cancel column-to-column fixed-pattern noise caused by amplifier offsets. The fundamental difference between CDS performed on an active pixel and a CCD output amplifier is caused by the integration time. Since the integration time is often longer than the time allowed to read the data from one row of pixels, the reset value must be stored in memory elements during the integration time. Alternatively, the reset value can be sampled immediately after the signal value. These two options are discussed in the next two Sections.

D.3.1 True correlated-double sampling

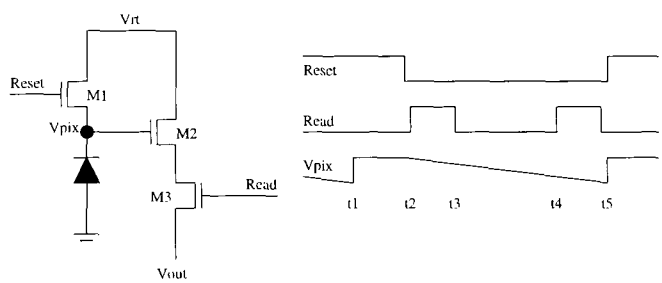


Figure D.3: *An active pixel and the signals applied to perform true correlated-double sampling.*

In true correlated-double sampling, the pixel output is sampled immediately after the reset operation at the beginning of the integration period (the Reset value) and again at the end of the integration period (the Signal value). This method of operation is non-ideal because:

- The integration time varies and can be up to a frame time, therefore, memory elements are required to store the reset value until the signal value can be read.
- The suppression of $\frac{1}{f}$ noise is controlled by the product $\tau\omega_f$ where τ is the time between samples and ω_f is the amplifier bandwidth. This product effectively determines the degree of correlation between the two samples. The integration time can be comparatively long, therefore, the suppression of $\frac{1}{f}$ noise is reduced.

D.3.2 Common correlated-double sampling

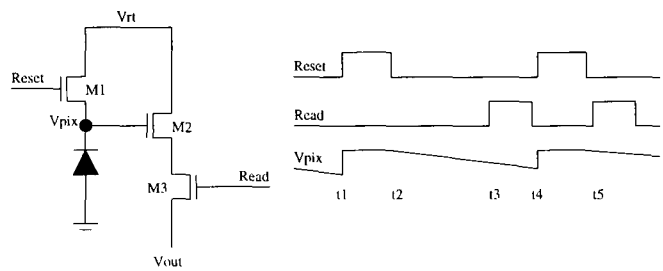


Figure D.4: *An active pixel and the signals applied to perform correlated-double sampling.*

In most active pixel sensors, to avoid the need for a frame memory, correlated-double sampling is performed as shown in Figure D.4. Under this scheme, the pixel is reset twice each frame: once before integration and again after the signal has been read. The disadvantage of this mode of operation is that the reset level in the Signal and Reset samples is uncorrelated. Therefore, $\frac{kT}{C}$ noise is not suppressed. However, fixed-pattern noise within the pixel is cancelled.

Appendix E
Matching and fixed-pattern noise

E.1 Overview

Mismatch is defined as a time-independent random variation in a physical parameter of identically designed devices. Classic examples of the effect of mismatch include: amplifier input offset and variation in the gain of a current mirror. In CMOS imagers, mismatch causes fixed-pattern noise, which is a systematic variation in the image. For example, amplifier offset can cause a column-to-column fixed-pattern noise that results in image stripes. Pixel-to-pixel fixed-pattern noise, for example, caused by threshold-voltage variation, can cause a speckled image effect.

Appendix D describes a method for removing fixed-pattern noise, the remainder of this chapter discusses the effects of mismatch.

E.2 Mismatch

CMOS camera design is limited by three different variation types:

1. **local mismatch**, which is the variation of a component parameter with reference to an adjacent, identically designed component.
2. **cross-chip mismatch**, for example, caused by an oxide thickness gradient, leads to a variation in a parameter across the chip.
3. **inter-chip mismatch** leads to so-called fast and slow chips. Such variations can either be across the wafer or between batches.

Unlike good analogue design, where the ratio of matched devices determines the achievable performance, CMOS image sensors are limited by the variation in the parameter values of distant, unmatched, often minimum sized, transistors.

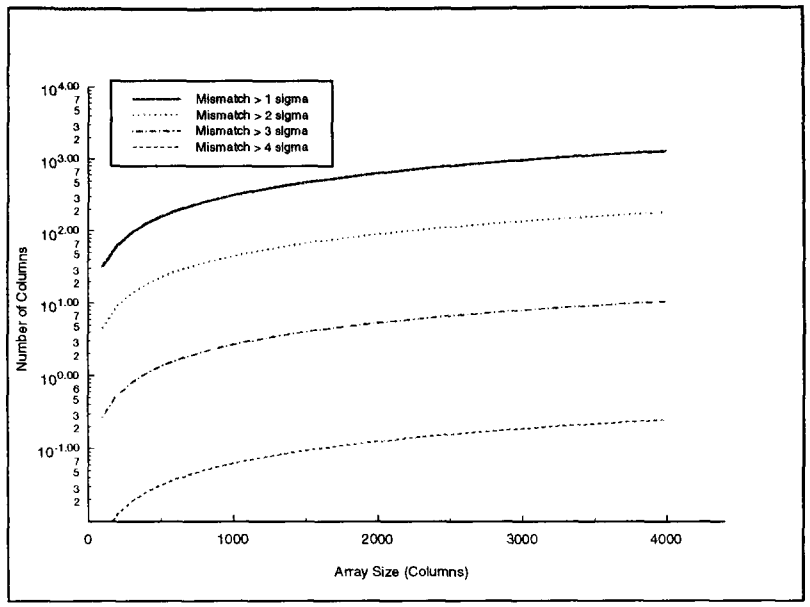


Figure E.1: *The number of columns that, on average, exhibit a variation of greater than the given number of standard deviations from the mean value.*

E.2.1 Local mismatch

The mismatch between matched devices is given in terms of the standard deviation of the matching distribution. In order to determine the mismatch that must be accounted for in the sensor design, it is useful to consider Figures E.1 and E.2, which show the average number of columns and pixels that exhibit a variation greater than the given number of standard deviations for an array size of $n \times n$ pixels. Assuming that the devices are well matched and that the array size is 1000×1000, on average, a tenth of chips will have a column with a mismatch greater than four standard deviations (4σ) and each chip will have a pixel with a mismatch of 5σ. A sensible design estimate would be to assume a column mismatch of 6σ and a pixel mismatch of 7σ. In most pixel architectures, transistors are not matched, and therefore the above analysis does not apply. With good design, column characteristics should depend on matching and the limits detailed above apply.

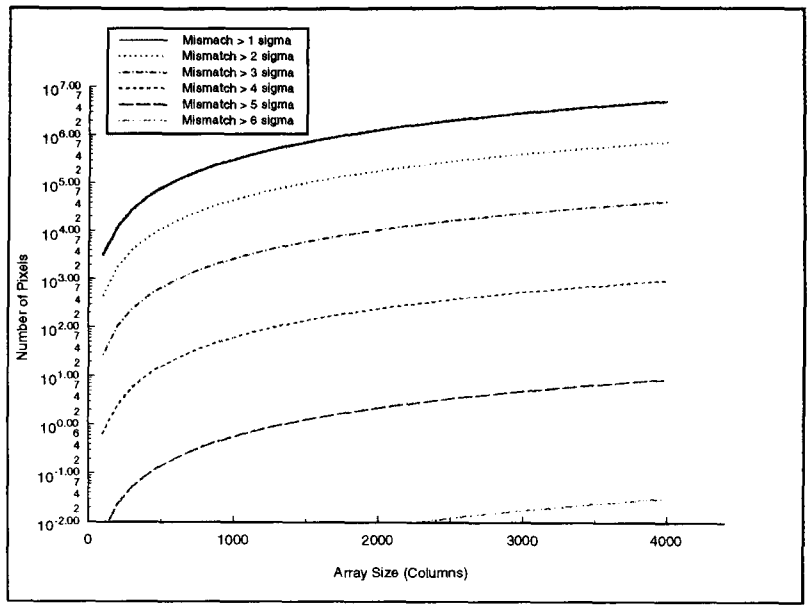


Figure E.2: *The number of pixels that, on average, exhibit a variation of greater than the given number of standard deviations from the mean value.*

E.2.1.1 Threshold voltage mismatch

The threshold voltage variation for near minimum sized devices is discussed in Section 5.2.3.1, and for devices sized to optimize analogue performance in the next section. Two important observations are that:

1. threshold voltage variation is not effected by rotation, unlike the transconductance factor [154].

2. if the source is not tied to the same potential as the substrate, the threshold voltage mismatch is increased due to variations in substrate doping [155].

E.2.1.2 Current mismatch

A current mirror gain shows variation due to mismatch in the threshold voltage, V_T, and transistor transconductance, β. Mismatch in V_T accounts for variation in channel charge and in the gate-oxide capacitance *per* unit area. Variations in dimensions, channel mobility and gate-oxide capacitance cause a mismatch in β. Therefore, there is some correlation in the mismatches,

which can be shown to be negligible [156].

The variance of the threshold voltage mismatch is inversely proportional to transistor area, whilst, the transconductance variance $\frac{\sigma_\beta^2}{\bar{\beta}^2}$, has a more complex relationship with transistor dimensions, given by[156]

$$\frac{\sigma_\beta^2}{\bar{\beta}^2} = A \times \frac{1}{\bar{L}\bar{W}} + B(\frac{1}{\bar{L}^2} + \frac{1}{\bar{W}^2}) \tag{E.1}$$

Equation E.1 shows that the transconductance mismatch decreases with gate area.

In the saturation region, the current mismatch of a current mirror is given by

$$\frac{\sigma_I^2}{\bar{I}^2} = \frac{\sigma_K^2}{\bar{K}^2} + 4\frac{\sigma_{VT}^2}{(V_{GS} - \bar{V}_T)^2} \tag{E.2}$$

The study by Kadaba [156], based on a $3\mu m$ process, concluded that the threshold voltage mismatch dominated for $V_{GS} - V_T < 0.5V$, therefore, 0.5V is commonly used as the gate-source over-drive voltage [56]. Figure E.3 shows that this is too conservative for the $0.7\mu m$ process, due to the improvement in threshold voltage matching. Figure E.4 shows the total current mismatch and the transconductance and threshold voltage contribution for a $2\mu A$ current mirror, with a fixed gate length of $5\mu m$. It shows that, provided $V_{GS} - V_T > 0.05V$, the gate-source over-drive voltage can be chosen as a compromise between limiting the output voltage range of the current mirror and transistor size, without noticeably affecting matching. If a 6σ mismatch and good matching is assumed, Figure E.4 implies that, with an appropriate choice of transistor size, current mismatch can be limited to approximately $1 - 2\%$.

E.2.2 Cross- and Inter-chip mismatch

If transistors are not matched, the absolute value of the threshold voltage, rather than the difference between two threshold voltages, is the limiting design factor. For example, the variation in pixel source follower threshold voltage, is defined by the maximum threshold voltage range for the given transistor size. The range of values increases as the size of transistor is reduced, the worst case being for a minimum size transistor, which in the Mietec $0.7\mu m$ process has a nominal threshold voltage of 0.8V, but the worst case threshold voltage is 1V [41].

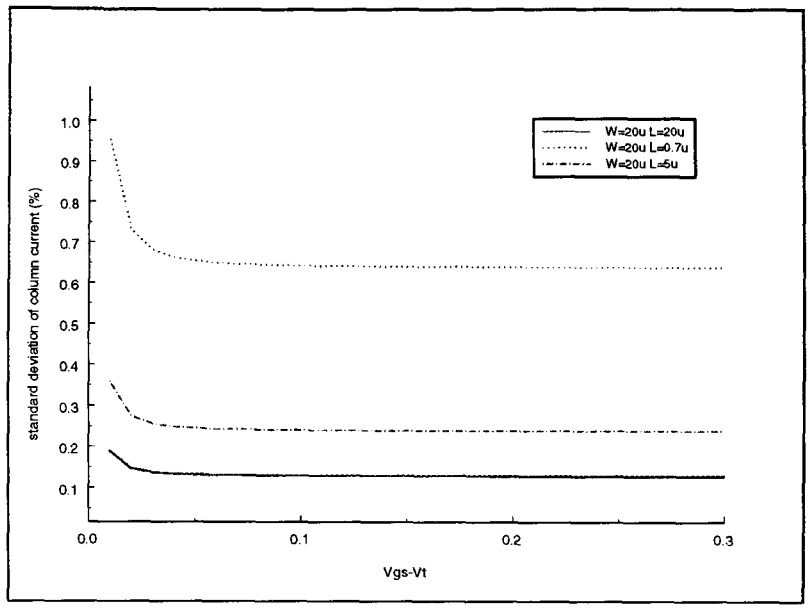


Figure E.3: *The standard deviation of percentage current mismatch for three current mirrors as $V_{GS} - V_T$ is varied[41].*

E.3 Common-mode-rejection ratio

An important design consequence of mismatch is that the common-mode-rejection ratio of differential circuits is decreased. For example, the ideally infinite common-mode-rejection ratio, $CMRR$, of the differential pair shown in Figure E.5 is reduced to [56]

$$CMRR = \frac{2g_{m1}R_B}{\frac{2\Delta V_T}{V_{GS}-V_T} + \frac{\Delta R_L}{R_L} + \frac{\Delta \beta_n}{\beta_n}} \tag{E.3}$$

where ΔX represents the mismatch between the two matched parameters, X, which can be taken as the 6σ value for column mismatch. Equation E.3 shows that the common-mode-rejection ratio can be improved by better matching or increasing either the transconductance of the input pair or the output resistance, R_B, of the current source.

E.4 Conclusion

Variations in physical parameters cause transistor mismatch, which limits analogue circuit design. For a pair of matched devices, the standard deviation of mismatch in threshold voltage

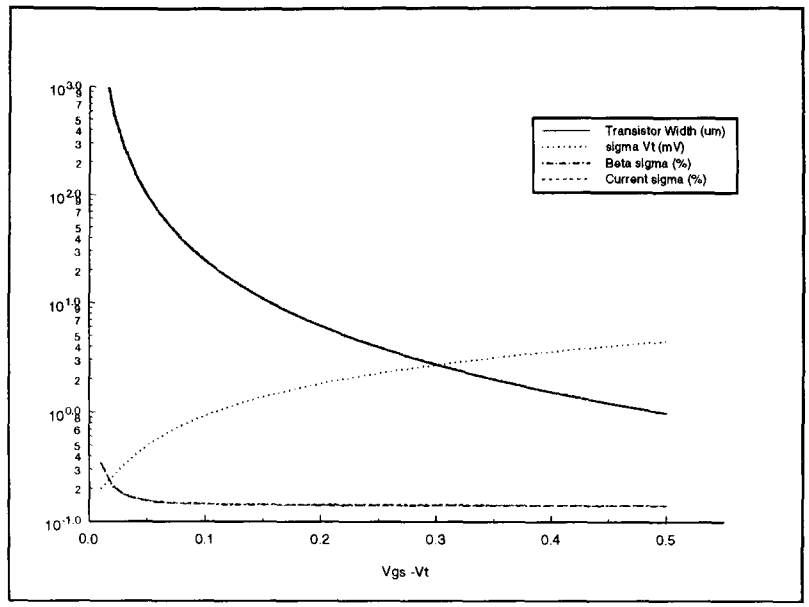


Figure E.4: *The standard deviation of the current, threshold voltage, and transconductance mismatch for a* $2\mu A$ *current mirror with* $L = 5\mu m$ *[41].*

and transconductance can be calculated. The total mismatch that the design must tolerate can be estimated depending on the number of matched transistor pairs. If the transistors are not matched, the design allowance must be increased to accommodate the maximum possible variation in a parameter. The common-mode-rejection ratio of a differential pair was presented as an example of mismatch adversely affecting analogue circuit performance.

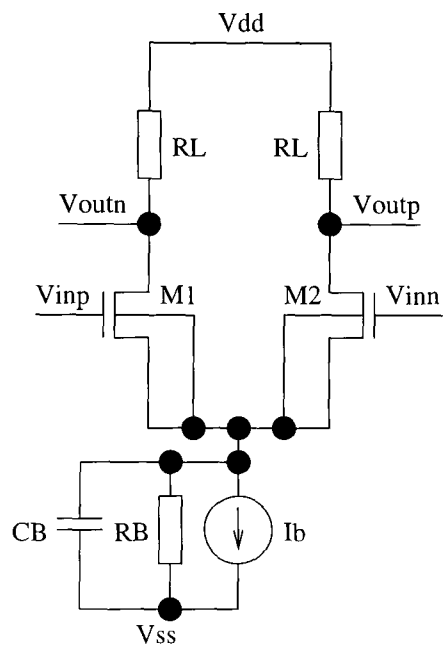


Figure E.5: *A resistive-load differential pair.*

Appendix F
Crosstalk

F.1 Overview

A possible advantage of a CMOS imager over a CCD imaging system is the ability to integrate on-chip digital logic. However, such a mixed-mode circuit can suffer from a reduction in analogue performance due to crosstalk. The trend towards high-frequency, high-resolution and low-voltage analogue circuitry integrated with complex, high-speed digital circuitry, exacerbates this problem. Consequently, the resolution of such mixed-mode circuits can be limited by the inability of the analogue circuitry to adequately reject the generated high-frequency noise. For example, a state-of-the-art imager, which comprises 25,000 digital gates, 14,300 SRAM bits and 400,000 analogue transistors [60], can experience performance degradation due to supply-borne crosstalk [78] and digital-to-analogue coupling [23].

This appendix discusses the source of digital noise and the methods of coupling to analogue circuits. Section F.5 outlines methods for the reduction of crosstalk, and evaluates the effectiveness of each method.

F.2 The cause of crosstalk

The basis of electrical interference is noise generation caused by fast current variations from digital gates or non-differential analogue circuits, which result in voltage drops over bond-wire and package pin inductances. The consequent noisy power supply, may disturb analogue circuits. Furthermore, if noise is injected into the substrate it can disturb even distant analogue circuits, limiting the achievable circuit precision [157–159].

A common source of digital noise is the buffer circuits required to drive large capacitances, for example, bus lines and off-chip circuitry. Such driving circuits often operate at high-frequencies and consume a large portion of the power budget [160]. One possible buffer circuit, the CMOS inverter, is discussed in the next section.

F.2.1 The CMOS inverter

A CMOS inverter consumes negligible power in steady-state. However, during a transition a significant current flows to charge the load capacitance and an unwanted short-circuit current can also flow. It has been shown that, for a well-designed inverter, the short-circuit power consumption is negligible [159]. However, a short-circuit current will cause a sharp increase in bias current, and, therefore, contribute significantly to power-supply-borne noise.

Veendrick has shown that for an unloaded, symmetrical inverter the short-circuit power dissipation, P_{short}, is given by

$$P_{short} = \frac{\beta}{12}(V_{dd} - 2V_T)^3 \frac{\tau}{T} \tag{F.1}$$

where τ is the 0 to 100% rise-time of the linearized input signal, and T is the period of the signal [160]. In order to reduce this power consumption and, therefore, the rate of current increase, input rise and fall times should be less than the output rise and fall times [160]. This is because a fast input transition can switch off the load transistor before the output has moved sufficiently to allow it to conduct significant current.

Further, increasing the output signal rise-time reduces the capacitive charging current. In conclusion, the output signal rise-time should be maximized.

F.3 The generation and communication of crosstalk

F.3.1 Supply-borne crosstalk

The rate of change of bias current causes a voltage drop over bond-wire and track inductances. Consequently, the on-chip power supply voltage is subject to variation, which can interfere with circuit operation. For example, the drain-substrate parasitic diode can be forward biased, which results in the injection of current into the substrate.

F.3.2 Capacitive coupling

When a digital signal line passes close to, or crosses, an analogue component or signal, the mutual parasitic capacitance can couple a fraction of the digital signal to the analogue component. To reduce this effect, the analogue and digital lines should be separated, ideally with a

grounded wire and crossing should be avoided [161]. However, this is impractical in an array, where signals must be routed both horizontally and vertically.

A parasitic capacitance between a node and the substrate can couple noise into the substrate. The affect of injected or coupled charge when is has reached the substrate is dependent on the process type.

F.3.3 Substrate

As discussed in the following two subsections, coupling characteristics depend on whether the process is based on an epitaxial or lightly-doped substrate.

F.3.3.1 Epitaxial substrate

If a circuit is fabricated on an epitaxial process, noise coupling is independent of circuit separation, provided that the separation distance is greater than four-times the epitaxial layer depth, which, for example, is typically $30\mu m$ for a $2\mu m$ process. This is because a majority of injected current flows vertically down to the low-resistance substrate, through the substrate and then vertically through the epitaxial layer to the substrate contact [158]. Therefore, the bulk can be regarded as a single node and noise injected into the bulk will spread throughout the entire chip.

F.3.3.2 Lightly-doped substrate

A lightly doped substrate forces current to flow close to the semiconductor surface. Consequently, the resistance between two contacts increases almost linearly with distance and the physical separation of circuits is an effective means of reducing crosstalk [158].

In order to use a lightly doped substrate for a CMOS imager, substrate contacts would need to be included in the pixel array to collect the photocurrent. A contact and bias line must be integrated in each group of four pixels, otherwise, pixel-to-pixel fixed-pattern noise would be increased. The consequent reduction in pixel fill-factor is approximately 10% for a minimum sized pixel. This increase in fill-factor results in epitaxial processes being favoured for CMOS imagers.

F.4 The effect of crosstalk

F.4.1 Single-ended analogue circuit.

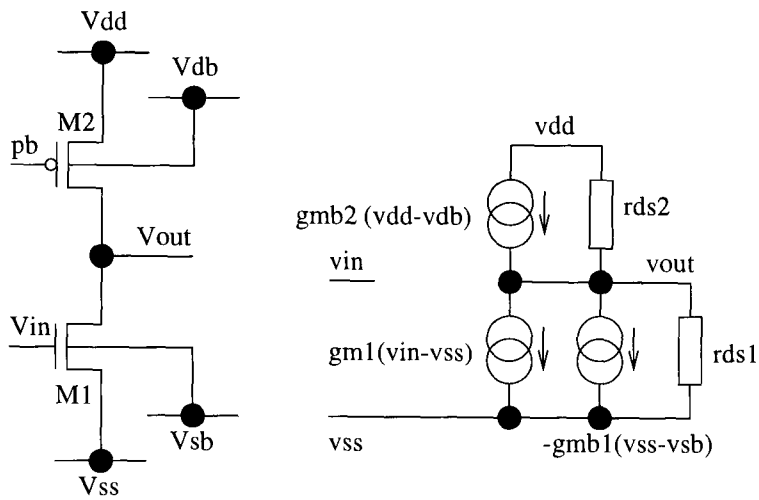


Figure F.1: *A common-source transistor stage and small-signal equivalent circuit.*

A typical non-differential transistor stage is shown in Figure F.1. The transistor stage is sensitive to signals on the three power supply lines, as well at the input node. If the load bias line, *pb*, is sufficiently well decoupled to V_{dd}, the small-signal output voltage, v_{out}, is given by

$$v_{out} = \frac{1}{g_{ds1} + g_{ds2}} \times (-g_{m1}v_{in} + (g_{m1} + g_{mb1})v_{ss} - g_{mb1}v_{sb} - g_{mb2}v_{db} + (g_{ds2} + g_{mb2})v_{dd}) \tag{F.2}$$

Equation F.2 shows that noise on the negative supply, V_{ss}, is indistinguishable from the input signal. Further, substrate and positive supply noise is amplified by approximately a tenth of the input gain. Consequently, non-differential circuits must be used with quiet supply lines, in particular, the substrate voltage must be equal to the negative supply, which must be very quiet. In the case of a PMOS input transistor, the results are reversed, *i.e.* the positive supply becomes more critical than the negative supply.

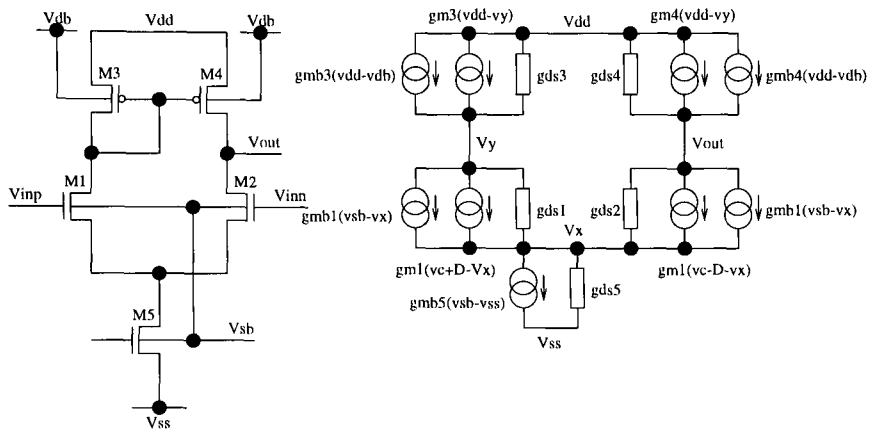


Figure F.2: *A single-ended differential pair and equivalent small-signal circuit.*

F.4.2 Single-ended differential stage

The small-signal output voltage of a differential pair, v_{out}, can be shown to be given by

$$
\begin{aligned}
v_{out} = & \frac{1}{(g_{m3}+g_{ds3})((g_{ds4}+g_{ds2})(g_1+g_{ds5})+g_2g_{ds4}))+g_{ds1}(g_{ds4}(g_1+g_{ds5})+g_{ds2}g_{ds5})+g_{m4}g_1g_{ds2}} \times \\
& \{\Delta(g_{m4}+g_{m3}+g_{ds3})(g_{m1}(g_{mb2}+g_{ds2})+g_{m2}(g_{mb1}+g_{ds1})) \\
& +g_{ds5}(g_{m1}g_{m4}+g_{m2}(g_{m3}+g_{ds3}+g_{ds1})) \\
& v_c(g_{m4}+g_{m3}+g_{ds3})(g_{m1}(g_{mb2}+g_{ds2})-g_{m2}(g_{mb1}+g_{ds1})) \\
& +g_{ds5}(g_{m1}g_{m4}-g_{m2}(g_{m3}+g_{ds3}+g_{ds1})) \\
& v_{sb}((g_{m4}+g_{m3}+g_{ds3})(g_2g_{mb1}-g_1g_{mb2})+g_{ds5}(g_{m4}g_{mb1}-g_{mb2}(g_{m3}+g_{ds3}+g_{ds1})) \\
& +g_{mb5}(g_2(g_{m3}+g_{ds3}+g_{ds1})-g_1g_{m4})) \\
& v_{db}(g_{ds1}(g_{mb3}g_2-g_{mb4}g_1)-(g_1+g_2+g_{ds5})(g_{m4}g_{mb3}-g_{mb4}(g_{m3}+g_{ds3}+g_{ds1}))) \\
& v_{ss}(g_1g_{m4}-g_2(g_{m3}+g_{ds3}+g_{ds1}))(g_{ds5}-g_{gmb5}) \\
& v_{dd}((g_4(g_{m3}+g_{ds3}+g_{ds1})-g_{m4}g_3)(g_1+g_2+g_{ds5})+g_{ds1}(g_3g_2-g_4g_1))\}
\end{aligned}
\tag{F.3}
$$

where $g_x = g_{mx} + g_{mbx} + g_{dsx}$. Equation F.3 states that the suppression of common-mode voltages and noise on the supply line is dependent on matching. For example, terms such as $g_{m1}(g_{mb2} + g_{ds2}) - g_{m2}(g_{mb1} + g_{ds1})$ are zero for a matched pair. However, because the differential pair is asymmetric, a term $g_{m1}g_{m4} - g_{m2}(g_{m3} + g_{ds3} + g_{ds1})$ is present, which is non-zero for a matched device. In order to improve the rejection of common-mode noise, it is important that the individual device output conductances, g_{dsx}, which is given below [56], are

small. This requires that device channel lengths are increased.

$$g_{ds} = \frac{I_{DS}}{V_E L} \tag{F.4}$$

The substrate transconductance terms, g_{mbx}, are less well matched than the transconductance terms and, therefore, can adversely affect the rejection of common-mode signals. Consequently, the bulk reference should be the local analogue ground.

Similar observations apply for fully-differential analogue circuits. The analysis is omitted here, but the significant difference would be that all terms are symmetrical, hence, common-mode rejection is improved.

F.5 Reduction of crosstalk

Digital noise is proportional to the number of active gates. Therefore, to reduce the digital noise at source, the number of gates should be minimized and asynchronous timing should be used to reduced the number of concurrently switching gates. After the digital gate count has been minimized, the other techniques discussed in this section can be used to reduce the effect of coupling.

F.5.1 Reduction of power-supply

An effective method of reducing digital noise is to reduce the power supply. Experimentally, Keiko has shown that coupled digital noise is reduced by a factor of five if the power supply is reduced from 5 to 4 V, and further halved if reduced to 2.5V [162]. However, the reduction in power supply from 4 to 2.5V will, approximately, halve the achievable analogue input and output range, consequently, the reduction in digital noise does not result in improved analogue performance.

F.5.1.1 Guard rings

A guard ring is a continuous native diffusion that surrounds a circuit. It provides a return path for injected currents, that otherwise would contribute to crosstalk. Isolation is more effective in a lightly doped substrate, where current flow is close to the surface. In such cases, a p^+ guard-

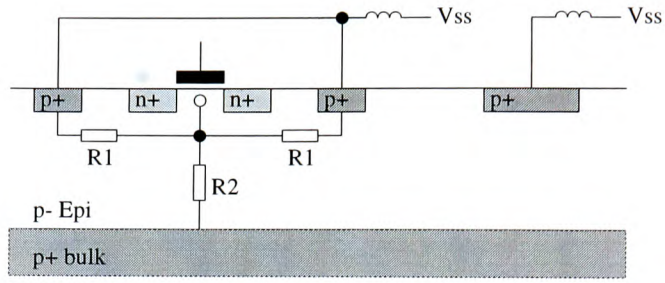


Figure F.3: *A process cross-section showing a guard ring biased using a dedicated package pin.*

ring diffusion can reduce the switching noise by an order of magnitude. Further improvements in isolation can be achieved using an n-well guard diffusion to force current to flow through the bulk, effectively increasing the isolation distance [158].

On an epitaxial substrate, the guard ring must be close to the source of the noise to be effective. For example, placed at $6\mu m$, a guard ring, with a dedicated pin reduced noise by 20%. However, if the substrate contact was used to bias the guard ring, coupling increased by a similar amount [157]. Figure F.3 shows the parasitic resistances associated with an epitaxial substrate and guard ring. If the guard ring is to be effective, the resistance R_1 must be less than R_2. This is equivalent to placing the guard ring closer to the noise source than the epitaxial layer depth [157].

F.5.2 Reducing the effect of bond-wire

An effective way of reducing supply-borne coupling is to decrease the inductance between the substrate and power supply using multiple package pins to reduce the bond-wire inductance. Both the peak-to-peak noise and settling time of noise is reduced [158].

The on-chip power-to-ground impedance is a parallel combination of the on-chip capacitance $C_{decoup} + C_{cir} + C_{par}$ and the bond-wire inductance. At high-frequencies this forms a resonant circuit, which can exhibit peaking. A resistor, added in series with the bond-wire, reduces peaking but the voltage drop is unacceptable for low-voltage applications. Ingels proposes a parallel RLC circuit to limit peaking, without reducing the available power supply [157].

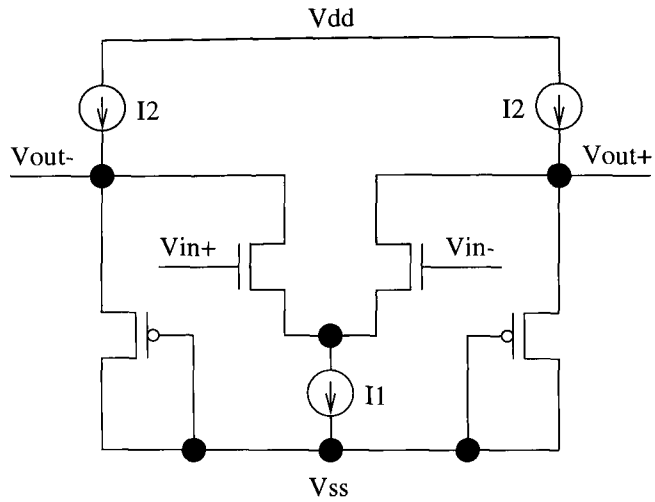


Figure F.4: *A folded-source coupled logic circuit.*

F.5.3 Differential digital logic

Alternative logic architectures to CMOS have been proposed to reduce the switching noise at the expense of increased quiescent current. For example, the circuit shown in Figure F.4, which is a folded-source coupled logic (FSCL) circuit, reduces digital switching noise by a factor of 30 to 300. A further disadvantage of FSCL is that it consumes double the area of a CMOS gate. However, synchronized differential signals are available, which can mitigate the increase in area. The power-delay product is similar to a CMOS gate because of the reduced logic swing which is defined by the values of I_1, I_2 and the transconductance of the load transistors [159].

F.6 Conclusion

If digital circuitry is to be integrated with a CMOS imager, the effect of crosstalk must be evaluated and limited. This chapter showed a number of methods of reducing crosstalk, the most important being using a fully-differential analogue architecture, reducing the digital noise at source and reducing the crosstalk mechanisms, for example, by using guard rings and separation on a lightly-doped substrate.

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