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Impedance Matching and DC-DC Converter Designs for Tunable Radio Frequency Based Mobile Telecommunication Systems

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Declaration

I hereby declare that this thesis has been composed by myself and that except where stated, the work contained is my own. I also declare that the work contained in this thesis has not been submitted for any other degree or professional qualification except as specified.

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Yan Chiew Wong

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Abstract

Tunability and adaptability for radio frequency (RF) front-ends are highly desirable because they not only enhance functionality and performance but also reduce the circuit size and cost. This thesis presents a number of novel design strategies in DC-DC converters, impedance networks and adaptive algorithms for tunable and adaptable RF based mobile telecommunication systems. Specifically, the studies are divided into three major directions: (a) high voltage switch controller based DC-DC converters for RF switch actuation; (b) impedance network designs for impedance transformation of RF switches; and (c) adaptive algorithms for determining the required impedance states at the RF switches.

In the first stage, two-phase step-up switched-capacitor (SC) DC-DC converters are explored. The SC converter has a simple control method and a reduced physical volume. The research investigations started with the linear and the non-linear voltage gain topologies. The non-linear voltage gain topology provides a higher voltage gain in a smaller number of stages compared to the linear voltage gain topology. Amongst the non-linear voltage gain topologies, a Fibonacci SC converter has been identified as having lower losses and a higher conversion ratio compared to other topologies. However, the implementation of a high voltage (HV) gain Fibonacci SC converter is complex due to the requirement of widely different gate voltages for the transistors in the Fibonacci converter. Gate driving strategies have been proposed that only require a few auxiliary transistors in order to provide the required boosted voltages for switching the transistors on and off. This technique reduces the design complexity and increases the reliability of the HV Fibonacci SC converter.

For the linear voltage gain topology, a high performance complementary-metal-oxide-semiconductor (CMOS) based SC DC-DC converter has been proposed in this work. The HV SC DC-DC converter has been designed in low voltage (LV) transistors technology in order to achieve higher voltage gain. Adaptive biasing circuits have been proposed to eliminate the leakage current, hence avoiding latch-up which normally occurs with low voltage transistors when they are used in a high voltage design. Thus, the SC DC-DC converter achieves more than 25% higher boosted voltage compared to converters that use HV transistors. The proposed design provides a 40% power reduction through the charge recycling circuit that reduces the effect of non-ideality in integrated HV capacitors. Moreover, the SC DC-DC converter achieves a 45% smaller area than the conventional converter through optimising the design parameters.

In the second stage, the impedance network designs for transforming the impedance of RF switches to the maximum achievable impedance tuning region are investigated. The maximum achievable tuning region is bounded by the fundamental properties of the selected impedance network topology and by the tunable values of the RF switches that are variable over a limited range. A novel design technique has been proposed in order to achieve the maximum impedance tuning region, through identifying the optimum electrical distance between the RF switches at the impedance network. By varying the electrical distance between the RF switches, high impedance tuning regions are achieved across multi frequency standards. This technique reduces the cost and the insertion loss of an impedance network as the required number of RF switches is reduced. The prototype demonstrates high impedance coverages at LTE (700MHz), GSM (900MHz) and GPS (1575MHz).

Integration of a tunable impedance network with an antenna for frequency-agility at the RF front-end has also been discussed in this work. The integrated system enlarges the bandwidth of a patch antenna by four times the original bandwidth and also improves the antenna return loss. The prototype achieves frequency-agility from 700MHz to 3GHz. This work demonstrates that a single transceiver with multi frequency standards can be realised by using a tunable impedance network.

In the final stage, improvement to an adaptive algorithm for determining the impedance states at the RF switches has been proposed. The work has resulted in one more novel design techniques which reduce the search time in the algorithm, thus minimising the risk of data loss during the impedance tuning process. The approach reduces the search time by more than an order of magnitude by exploiting the relationships among the mass spring's coefficient values derived from the impedance network parameters, thereby significantly reducing the convergence time of the algorithm. The algorithm with the proposed technique converges in less than half of the computational time compared to the conventional approach, hence significantly improving the search time of the algorithm.

The design strategies proposed in this work contribute towards the realisation of tunable and adaptable RF based mobile telecommunication systems.

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List of Acronyms and Abbreviations

AMS	=	AustriaMicroSystem
B	=	Susceptance
BMS	=	Basic mass spring
BST	=	Barium Strontium Titanate
C	=	Charge storage capacitor
C_L	=	Output load capacitor
CMOS	=	Complementary metal-oxide-semiconductor
C_P	=	Parasitic capacitance
CPM	=	POLY1-MET1-MET2-MET3
CPOLY	=	POLY1-POLY2
C_{OX}	=	Gate oxide transistor
C_{OUT}	=	Output capacitor
C_{Store}	=	Charge storage capacitor
CV	=	Capacitance-voltage
CWPM	=	DNTUB-MET1-MET2-MET3
d(n)	=	Desired impedance
DC	=	Direct current
DCMS	=	Derivative-corrective mass spring
$D_{i,t+1}^{N}$	=	Displacement of the spring
e(n)	=	Error signal
EMI	=	Electromagnetic interference
f	=	Clock frequency
f_d	=	Design frequency
FET	=	Field-effect transistor
FOM	=	Overall antenna figure of merit
G	=	Antenna gain
GA	=	Genetic algorithm
GaAs	=	Gallium Arsenide
g_{ext}	=	External random force
G_L	=	Conductance
GPS	=	Global Positioning System

GSM	=	Global System for Mobile Communications
HV	=	High voltage
IC	=	Integrated circuit
I_D	=	DC drain current
I_L	=	Output current
k	=	Stiffness of the spring
K_{ox}	=	Relative permittivity of silicon dioxide
L	=	Length of the transistor
LDO	=	Low-Dropout regulator
LMS	=	Least Mean Square
L_{OC}	=	Open-circuited stub
L_{SC}	=	Short-circuited stub
LTE	=	Long-term evolution
LV	=	Low voltage
MEMS	=	Miro-electro-mechannical-systems
MOS	=	Metal-oxide-semiconductor
MS	=	Mass spring
N	=	Number of stages
N_A	=	Doping concentration
nMOS	=	N type metal-oxide-semiconductor
NPN	=	A bipolar transistor with a layer of P-doped between two N-doped layers
PNP	=	A bipolar transistor with a layer of N-doped between two P-doped layers
pMOS	=	P-type metal-oxide-semiconductor
q	=	Charge of an electron
Q-factor	=	Quality factor
RF	=	Radio frequency
SC	=	Switched- capacitor
SEM	=	Scanning electron microscope
SiC	=	Silicon Carbide
SMA	=	surface-mount assembly
SOI	=	Silicon-on-insulator
SOS	=	Silicon-on-sapphire
SP	=	Series-parallel
S/H	=	Sample and hold

T	=	Antenna noise temperature
V_{B_S}	=	Bulk to substrate voltage
VCLK1	=	Voltage at clock 1
VCLK2	=	Voltage at clock 2
V_{DB_MAX}	=	Maximum technology allowable drain to bulk voltage
VDD	=	Power supply
VDS	=	Drain to source voltage
V_{DS_MAX}	=	Maximum technology allowable drain to source voltage
V_{GS_eff}	=	Effective gate to source voltage
V_{GS_MAX}	=	Maximum technology allowable gate to source voltage
V_{LS}	=	Voltage supply at the level shifter
VLSI	=	Very large scale or integration
$V_{i,t+1}^{N}$	=	Next step velocity
V_{out}	=	Output voltage
V_{SB_MAX}	=	Maximum technology allowable source to bulk voltage
VSWR	=	Voltage standing wave ratio
V_{TH}	=	Threshold voltage
V_{TH0}	=	V_{TH} with zero V_{SB}
W	=	Width of the transistor
w(n)	=	Weighting factor
Y_0	=	Nominal system admittance
Z_{in}	=	Input impedance
Z_{Load}	=	Load impedance
Z_0	=	Nominal system impedance
α	=	Alpha
β	=	Beta
ε_{si}	=	Permittivity of silicon
ε_{ox}	=	Oxide permittivity
$\Delta\lambda$	=	Electrical distance between the RF switches
g_m	=	Transconductance
$\lambda/4$	=	Quarter wavelength
η	=	Efficiency
r	=	Vicious damping coefficient
r_{ds}	=	On-resistance in the transistor
Γ	=	Reflection coefficient

t_{ox}	=	Gate oxide thickness
$2\phi_F$	=	Surface potential
μ_n	=	Mobility of electrons near the silicon surface
γ	=	Body effect parameter

Chapter 1: Introduction

1.1 Motivation for the Tunable RF based Mobile Telecommunication Systems

Radio frequency (RF) circuits with tunable and adaptable functions propose a wide range of possibilities and attract significant interest especially in the field of mobile telecommunication systems. Tunable and adaptable RF based mobile telecommunication systems not only enhance their functionality and performance but also reduce the circuit size and cost. In general, RF front-end circuits can be designed to adapt to different types of operating conditions, such as multi frequency bands, variable transmit power levels, antennas in mismatch conditions and a fluctuating operating environment, which are discussed as follows.

1.1.1 Multi Frequency Bands

Over the past 10 years, the mobile industry has evolved at a rapid pace, which increases both the requirements and the capabilities of the RF front-end in order to support a multi frequencies wireless connection. Wireless communication has expanded from a single mode, triple-band 2G system in the year 2000, to a triple-mode, 9-band high speed data capable system by the year 2010 [1]. The trend continues with the rapid deployment of 4G LTE

systems with new modes and operating bands. The operation of multi-mode and multi-band is usually supported by multiple stacked transceiver units [2], as shown in Figure 1.1. Each of units is optimised for a single frequency band. Employment of multiple transceiver units is costly due to component duplication and large components count, which are undesirable for mobile applications. For the front-end to be able to support the continuing evolution, tunable RF technology is one of the promising solutions [1, 2]. Figure 1.2 shows that the tunable RF system reconfigures for multi-mode standards in a single transceiver unit rather than duplicating mode-specific transceiver units for each new standard. In tunable RF system, RF main components such as filters or duplexers, power amplifiers and antenna impedance matching network have to be reconfigured to cater for multi-mode standard operating requirements [3]. For instance, tunability in filter provides spectral diversity and increases efficiency [4]; Tunability in duplexer improves adjustable isolation [5]; Tunability in power amplifiers provides variable transmit power levels for multi frequency operations [6]; Tunability in impedance matching network provides required susceptance for antenna to compensate for changes such as frequency and the detuning effects that occur due to the user's head and hand. As a result, the whole tunable RF system increases the reuse of components and lower material costs, resulting in space saving and cost efficiency.

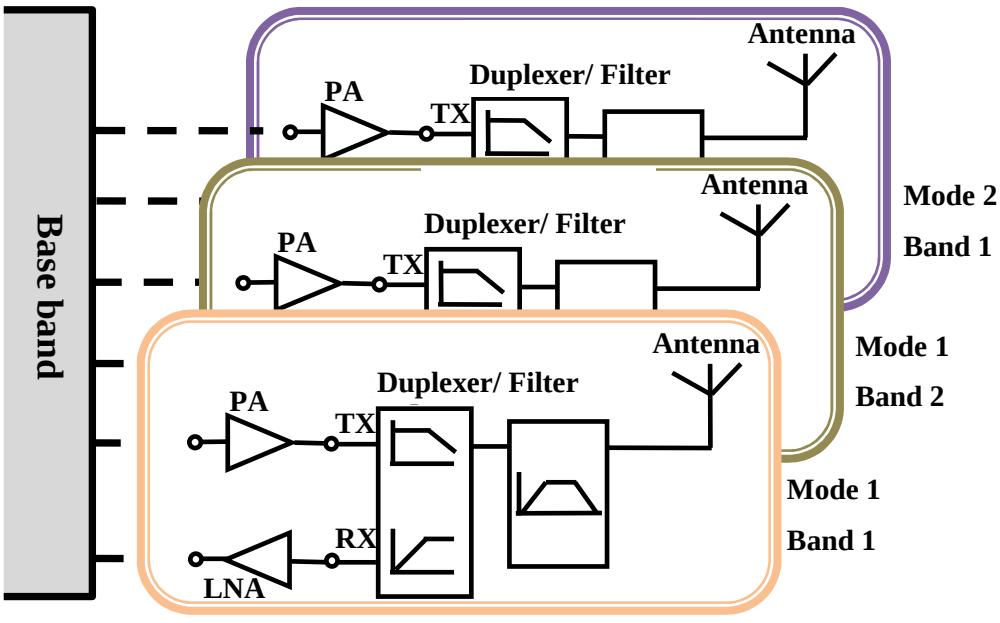


Figure 1.1: Multiple transceiver units employed for multi-mode and multi-band operations

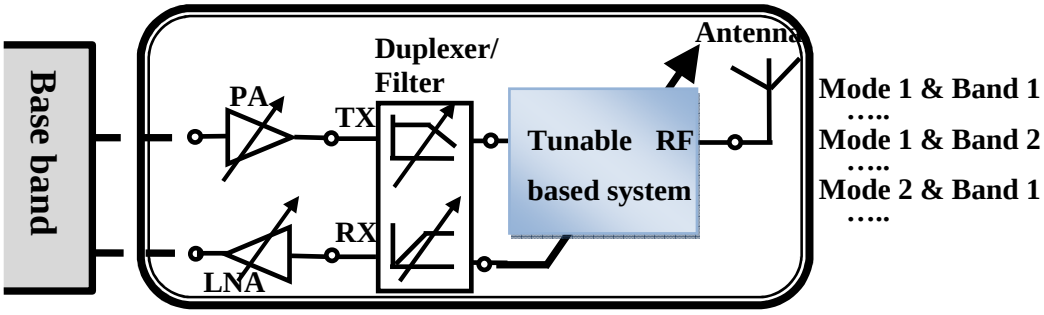


Figure 1.2: Tunable RF based system reduces the size of multi-mode and multi-band transceiver

1.1.2 Variable Transmit Power Level

On the other hand, tunable RF technology also improves the power efficiency in RF front-ends. Transmit power levels in mobile devices depend on the distance to the communicating base stations. By adjusting the biasing voltage or current [7, 8] or load impedance [6, 9, 10] of the power amplifier at the RF front-ends, according to the optimum operating power level, overall power efficiency can be considerably improved.

1.1.3 Antenna in Mismatch Conditions

Tunability for RF front-end helps in relaxing antenna design process. Antennas used in mobile devices are preferable small in size. However, most of the small size antennas are narrow bandwidth which is easily detuned by a slight handling error or a fluctuating operating environment. A detuned antenna will have an operating frequency that is shifted from its design frequency. This causes a high voltage standing wave ratio (VSWR) and a large power reflection. Some of the antennas for mobile devices are developed with a maximum VSWR of 3.5 which have an equivalent loss of 1.6 dB or 30 percent of the reflected power at the antenna [11]. Tunable RF circuits allow a considerable extension of the operational bandwidth of mobile device antennas [12, 13]. With tunable RF circuitries, the operational frequency [14-16] and radiation pattern [17] of an antenna can even be reconfigured. These significantly relax the tight constraints in designing the antennas.

1.1.4 Fluctuating Operating Environment

Adaptability in RF front-end improves the link quality by maintaining low VSWR in operating environment through spontaneously tuning the impedance to counteract the sudden impedance change in a user fluctuating operating environment. This situation mostly occurs in the miniaturised antenna of a mobile terminal [18]. The impedance of miniaturised antennas tends to shift with simple human ergonomics in operating conditions [19, 20].

Previous researchers have analysed the performance of mobile antennas influenced by a user's head, hand and shoulder [21-25]. For example, how the phone is held by the hand can have an impact on antenna performance, as shown in Figure 1.3 [24]. Similarly, how the phone is stored (in a pocket or briefcase, for example) can also negatively impact the matching of the antenna impedance. Due to the fact that every model of a device is different, interference from the user's hand and head is undefined a priori. This creates a significant problem to mobile users such as phone call drop, bad link quality and fast drain off of battery power.

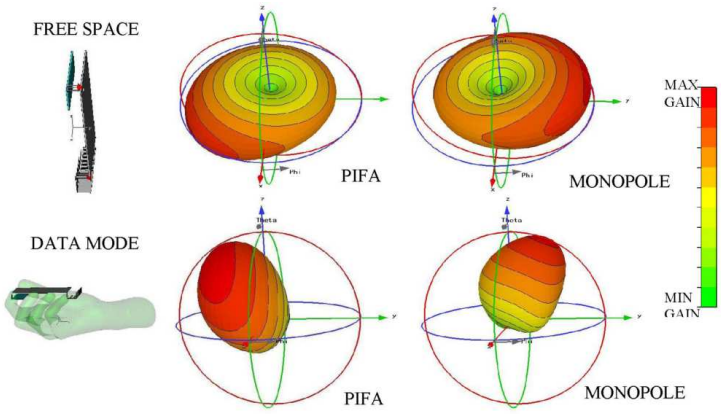


Figure 1.3: Effect of human hand (in data mode position) to the antenna gain patterns at 881.5MHz frequency [24]

For this reason, adaptability in the RF circuit is needed in order to improve the link quality by reducing the user's impact on antenna in mobile devices, as shown in Figure 1.4. The adaptive RF circuit corrects the impedance mismatch and preserves the maximum radiated power [7, 26-29]. By reducing the reflected power, the battery life of mobile devices is extended and the communication performance of mobile device is enhanced.

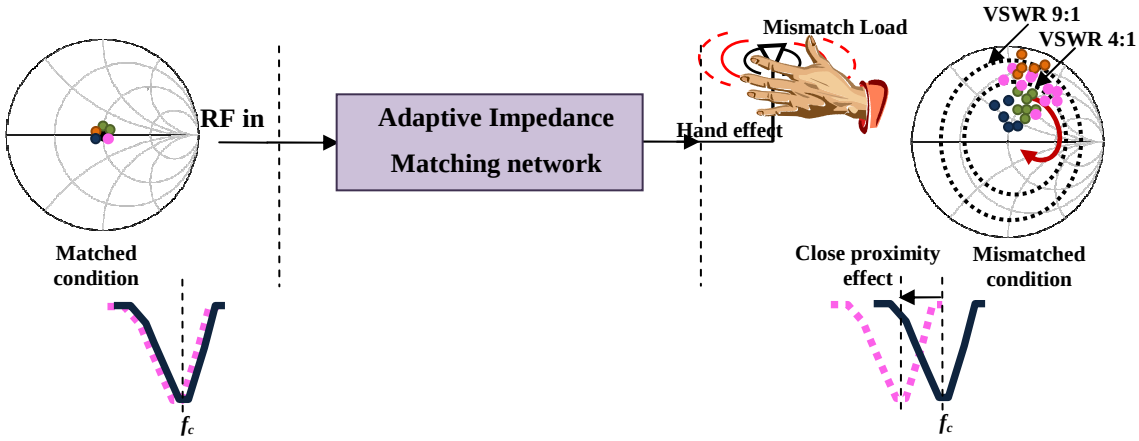


Figure 1.4: Adaptability in an RF circuit corrects the antenna impedance mismatch that is caused by the effect of close proximity with a human hand

1.2 Research Investigation

Introducing tunability or adaptability to the RF front-end provides great benefits but carries also losses and complexity by having additional functional blocks. Thus, research attentions are required to optimise these functional blocks in order to minimise the additional losses. Several key areas require research attentions such as RF switches design, controller, processor, impedance network designs and detector. Specifically, this thesis focuses on control circuitries, impedance network designs and adaptive algorithms for RF switches, aiming at the realisation of high performance mobile telecommunication systems. The study is divided into three distinct topics: (a) high voltage switch controller based on DC-DC converters for the RF switches actuation, (b) impedance network designs for impedance transformation of the RF switches, and (c) adaptive algorithms to determine the required impedance state at the RF switches for compensating the impedance variation of an antenna, as depicted in Figure 1.5.

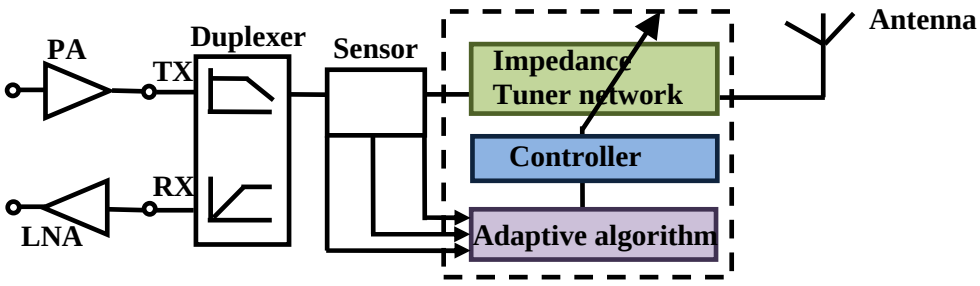


Figure 1.5: Research areas (in the dashed block) covered in this thesis

1.2.1 High Voltage Switch Controller based on DC-DC Converters for RF Switch Actuation

In the first stage, high voltage (HV) switch controller for RF switches actuation will be explored. Most of the RF switches, in particular RF Micro-Electro-Mechanical-Systems (MEMS) devices, require biasing voltages which are significantly higher than the supply voltage. Thus, a DC-DC converter will be developed as an HV switch controller for biasing the RF switches. The DC-DC converter has to meet several specifications such as high output voltage, small size, low power consumption and linearity.

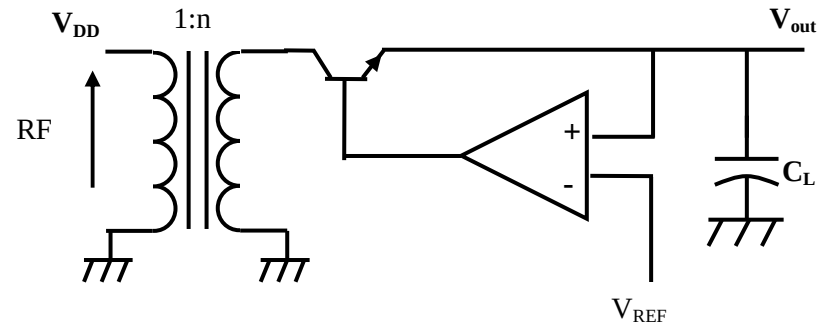
In general, three topologies can be implemented for the DC-DC converter. They are linear regulators, inductive based converters and switched-capacitor (SC) DC-DC converters, as shown in Figure 1.6 (a), (b) and (c) respectively.

Linear regulators or low-dropout regulators (LDO) are a mature technology but they are not preferable in scenarios where the dropout voltage between the input and output is very large. This will dramatically reduce the efficiency of the LDO [30].

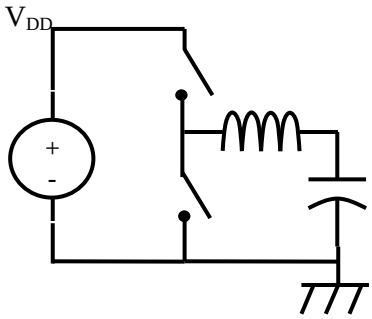
The SC DC-DC converters have several advantageous properties, which include a simple control method and a reduced physical volume [31-34]. They also have less electromagnetic interference (EMI), low cost and high power density for the design. The SC converter output voltage is determined by the converter topology and has good no-load voltage regulation [35]. This is ideally suited for battery-operated applications with power management, where the converter must operate at an almost zero load.

Inductive based switching converters provide high efficiency and flexible power conversions. However, the inductive based converters require either technologically intensive integrated inductors (i.e. non- production CMOS) or bulky off-chip inductors, and suffer from severe electromagnetic interference noise [30, 36]. Furthermore, the switching components (i.e. transistors) in the inductive based converters have to sustain the full voltage difference and the peak current of the converter. This high voltage rating requirement is difficult to fulfil by current state of the art CMOS technology. In contrast, for a linear SC DC-DC converter, the required rating of the transistors is relatively small. Furthermore, the SC DC-DC converter requires only capacitors and switches. Thus, these make the SC DC-DC converter feasible for integration. Comparative analyses in [30, 37] conclude that the SC DC-DC converter has strong advantages with respect to both switch utilisation and high

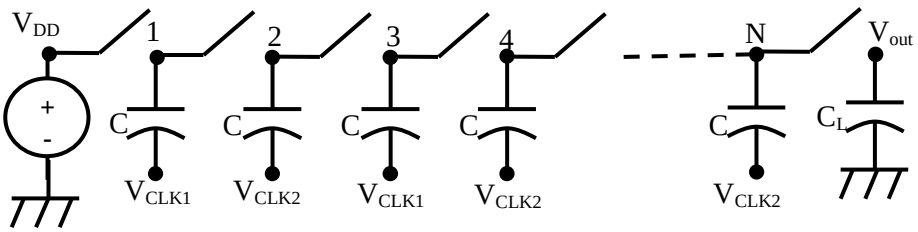
energy densities of capacitors versus inductors. These show that the SC converter is evidently a promising candidate for this application.



(a)



(b)



(c)

Figure 1.6: Topologies of DC-DC converter (a) linear regulator (b) inductor based converter (c) switched capacitor converter

Historically, SC converters have been used in integrated circuits to provide programmable voltages to memories, but have been limited to low powers (<100mW). Dickson et al. [38] has provided a detailed analysis and conducted a number of experimental

measurements of a MOS diode-connect SC converter built in very large scale integration (VLSI) technology. Improvements to SC DC-DC converters have been performed and discussed in [37, 39-45]. Palumbo [39, 42] presents a design methodology based on an optimum number of stages for a particular voltage gain. Tanzawa provides a detailed dynamic analysis in [43] and an optimisation technique to maximise the output current in a minimum circuit area in [40]. In [37, 41, 44, 45], Seeman presents a simpler optimization technique for the switches and capacitances in SC converters on various topologies. Previous research works have focused on different topologies [46, 47], mathematical models [48], low voltage operation [49], load properties [42] to the improvement in power and area considerations [31, 40, 50]. Little effort has gone into designing and optimizing HV SC DC-DC converter for RF switches. More details of the design and optimisation of the linear and the nonlinear voltage gain based on two-phase SC DC-DC converter topologies will be presented in Chapters 2 and 3.

1.2.2 Impedance Network Designs for Impedance Transformation of RF Switches

In the second stage, tunable impedance network designs will be investigated. The tunable impedance networks are evolved from the fixed impedance networks that have been used for precisely correcting the mismatch to the desired impedance. The impedance of the fixed network cannot be changed after implementation. To be reconfigured, RF switches need to be included in the impedance network. The impedance network designs transform the impedance of the RF switches to a range of impedance tuning region which depends on their applications. Impedance networks have been applied in antenna load tuning [51-54], antenna impedance matching [13, 19, 28, 55-58], tunable filters [13, 59] and tunable power amplifier [8, 10, 60, 61].

For mobile applications, tunable impedance network designs require more stringent specifications, such as wide impedance coverage, a lesser number of RF switches, impedance network topology with small circuit size and losses, and less complexity in the biasing circuit.

In general, RF switches could function as ohmic contact switches or tunable capacitive switches. It depends on the internal design structures of the RF components which

will not be covered in this thesis. For simplicity, both ohmic contact switches and tunable capacitive switches are named as RF switches in this thesis.

Impedance networks can function as discrete tuning or continuous tuning approaches, which are discussed as follows.

1.2.2.1 Discrete Tuning

The discrete tuning approach utilises a combination of RF switches with a number of discrete capacitors. The discrete tuning approach delivers a precise range of capacitance values through a digital switching control circuit. An example of the impedance network topology utilising a total of 14 MEMS capacitive switches in a 6-bit configuration is shown in Figure 1.7 [62].

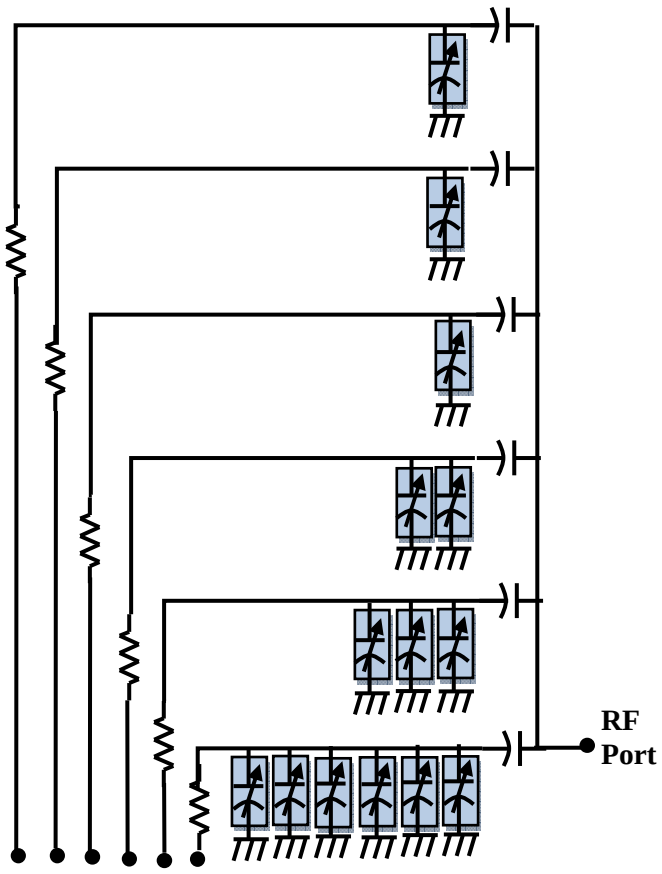


Figure 1.7: An example of discrete tuning approach which utilises a total of 14 RF switches in a 6-bit configuration

1.2.2.2 Continuous Tuning

The continuous tuning approach utilises variable capacitive RF switches in the impedance network. The main advantage of the continuous tuning is a simpler control circuit in biasing the switches. A significantly fewer number of tunable RF switches are needed compared to a discrete tuning approach for approximately the same size of impedance tuning region. The impedance and electrical length of the stubs are reconfigured by varying the tunable components, as shown in Figure 1.8.

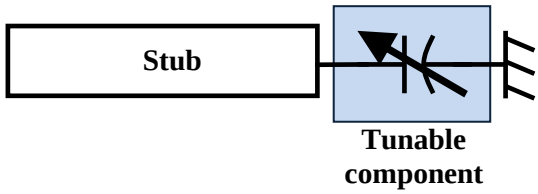


Figure 1.8: An example of continuous tuning approach which utilises an RF switch in a tunable matching stub

For multi frequency standards, the discrete tuning approach demonstrates a larger impedance tuning region compared to a continuous tuning approach. However, a discrete tuning approach utilises a large number of RF switches which require a very complex control circuitry for biasing the RF switches. These also increase the size of the overall impedance network which is undesirable in mobile telecommunication applications.

Even though a continuous tuning approach appears as to have a reduced number of RF switches and is less complex in its control circuitry implementation, the limited tuning ratio in the RF switches restrain the achievable impedance tuning region. More details of the design and development of tunable impedance networks will be presented in Chapter 4. Integration of the tunable impedance network with an antenna will be discussed in Chapter 5.

1.2.3 Adaptive Algorithms for Determining the Required Impedance States at the RF Switches

In the final stage, adaptive algorithms will be used to determine the required impedance stage at the RF switches based on different levels of antenna impedance mismatch.

Impedance states at RF switches in the impedance network will be sought by the adaptive algorithm in order to provide a complex conjugate match solution, corresponding with the mismatch antenna load. In general, adaptive algorithms are broadly divided into functional and deterministic types, which are described as follows.

1.2.3.1 Functional Approach

The first approach includes functional algorithms that commonly use the detected information for direct control of tunable RF switches in a sequence that converges within the acceptable limits defined by the VSWR. This approach utilises control circuitries such as analog and digital circuits [63], two nested control loops [64], two cascaded control loops [28, 65] and a closed-loop mixed-signal matching state search circuit [26], for the generation of the timing signals. This approach requires detection of the complex value of impedances, admittances, or reflection coefficients. This algorithm requires no initial knowledge of antenna impedance or network values. Instead, the network components are set to some initial, or default setting and adjusted by an iterative algorithm [26, 66]. Through a sample and hold (S/H) process, the present value will be compared to the one stored in the S/H at each iteration. If the present value is better than the previous value, the present value will be stored and vice versa. After scanning all possible impedance values sequentially, the value stored in the system represents the optimum state. The most significant drawback of functional tuning algorithms is that they require many iterations before a satisfactory matched condition is reached [66]. The tuning process will cause amplitude and phase modulation of the signal radiated. Thus, long tuning times might increase the risk of corrupting the data transfer in mobile applications.

1.2.3.2 Deterministic Approach

The second tuning method includes deterministic algorithms that make use of searching and optimization [28]. This method aims to minimise the duration of the tuning cycle. There are two ways to obtain the impedance values. The impedance values could be stored in lookup tables or trial-and-error by the adaptive algorithm [67].

By solely using lookup tables, all potential tuning stages of RF switches need to be pre-calculated from the antenna feed point for each frequency band. A one-step algorithm which makes use of a lookup table with the S-parameter data of each setting of the matching

network, obtained from calibration or a reference design, has been used in previous research work [65]. For antenna operating at multi frequency standards, the impedance network requires a very large set of tuning data. Generating this tuning data would require an unfeasibly large number of calculation times as an initialization procedure for the adaptive algorithm [66]. Large data storage is also a limitation in mobile applications.

To reduce the size of the data storage, trial-and-error adaptive algorithms could be used. However, this comes with a trade-off in tolerable search time and the search time will be drastically increased in a multi frequency standards environment which has a relatively large search space. In addition, due to the non-linear correlation of the RF switches in an impedance network, some of the adaptive algorithms such as least mean squares (LMS), steepest gradient [68], simulated annealing [69], and fuzzy [70] are able to search either the real or imaginary part of the impedance but not both parts simultaneously. To correct both real and imaginary parts of the impedance, researchers applied a specific Genetic Algorithm (GA) [67, 71-73]. However, GAs are computationally very expensive and exhibit slow convergence speeds. Other adaptive algorithms such as Hooke and Jeeves's algorithm [55], Powell Algorithm [55] and the nearest neighbour search algorithm [74] strongly depend on an initial starting point and are difficult to search for an optimum state. A fast convergence analytical algorithm was proposed in [75] but it is an impedance network specific algorithm and difficult to extend to other network topologies.

For these reasons, a fast and robust adaptive algorithm with less computational resources is needed to calculate the required impedance tuning stage at the RF switches for compensating the impedance variation of an antenna. In particular, design considerations for the adaptive algorithm include search capability, computational resources and convergence speed. More details for the design of an adaptive algorithm for tunable RF switches in mobile applications will be presented in Chapter 6.

Figure 1.9 summarises the area and challenges to be addressed in the thesis.

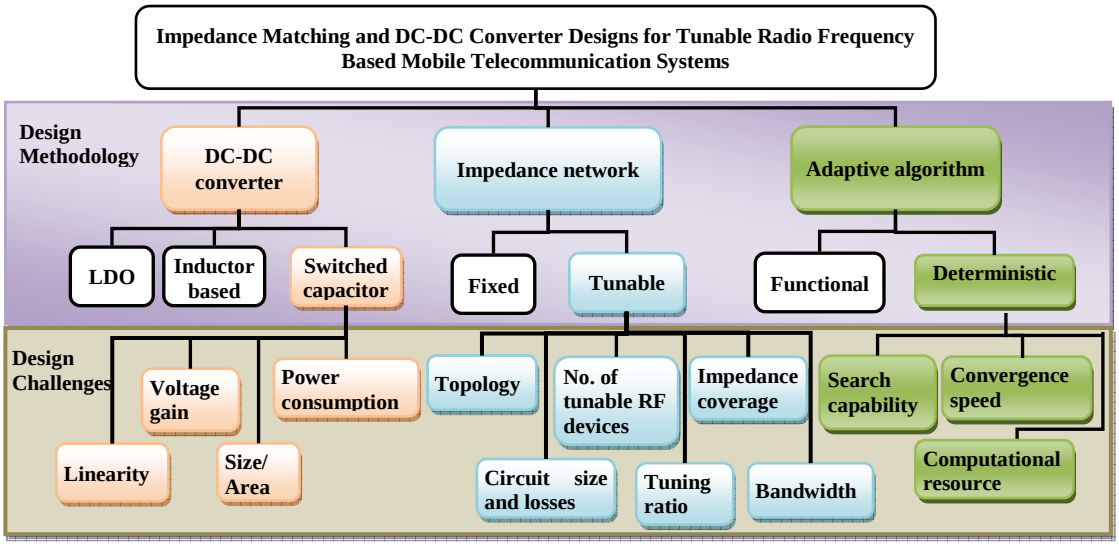


Figure 1.9: The overview of the research structure (the highlighted boxes are the research areas)

1.3 Overview of Thesis

The thesis is divided into seven chapters. In this chapter, the need for a tunable RF mobile system and the roles of the DC-DC converters, the tunable impedance networks and the adaptive algorithms in mobile telecommunication systems have been outlined.

Chapter 2 provides a review of the topology and proposes design techniques to address the implementation difficulties in high voltage two-phase SC DC-DC converters. The properties of the key components in the topologies are analysed. A Fibonacci SC converter has been identified as having the lowest voltage loss per gain compared to other topologies. However, implementation of a high voltage Fibonacci converter is difficult because it requires a wide range of voltage rating of the components and the associated reliability issues. Gate driving techniques have been proposed in order to address the implementation difficulties and reduce the design complexity.

Chapter 3 presents the design techniques for an integrated HV SC DC-DC converter. The design parameters are analysed and synthesised in order to reduce the die area of the proposed SC DC-DC converter. The adaptive biasing circuits have been proposed in this chapter for avoiding latch-up, which normally occurs with low voltage transistors when they

are used in a high voltage design. A charge recycling circuit is introduced to reduce the power consumption due to the effect of non-ideality in integrated HV capacitors. Reliability issues in the design have also been addressed in this chapter.

Chapter 4 not only provides a review of the impedance network's topologies and the RF switches technology, but also proposes a design technique to increase the impedance tuning region within the limits of available tuning ranges in RF switches.

Chapter 5 presents the integration of a wideband tunable impedance network with an antenna for a multi-band RF front-end. The design considers multi-section impedance networks, radial stub and tuning trajectory to achieve wide bandwidth performance. The integrated system improves the antenna's performance after realisation. It also corrects the antenna impedance mismatch due to manufacturing errors, relaxing the antenna design process.

Chapter 6 presents a novel technique to reduce the search time by exploiting the relationships among the mass spring's coefficient values derived from the impedance network parameters, thereby significantly reducing the convergence time of the algorithm. The proposed algorithm has faster convergence speed and is more robust than the existing algorithms, i.e. Least Mean Square (LMS) and Genetic Algorithm (GA). To operate in multi frequency standards, the proposed algorithm has been customised from the perspective of topology, operating bands and VSWR, thus reducing the search space in the algorithm.

Chapter 7 concludes the research investigations and suggests future work.

1.4 Publications Arising from This Research

In the course of this research, the following journals and conference papers have been published:

1. **Y.C. Wong**, N.H. Noordin, A.O. El-Rayis, N. Haridas, A.T. Erdogan, and T. Arslan, "An evaluation of 2-phase charge pump topologies with charge transfer switches for green mobile technology," *IEEE International Symposium on Industrial Electronics* (ISIE2011), pp. 136-140, 2011.

2. **Y.C. Wong,** W. Zhou, A.O. El-Rayis, N. Haridas, A.T. Erdogan, and T. Arslan, "Practical design strategy for two-phase step up DC-DC Fibonacci Switched-Capacitor

converter," *20th European Conference on Circuit Theory and Design (ECCTD)*, pp. 817-820, 2011.

3. **Y.C. Wong**, T. Arslan, A.T. Erdogan, N. Haridas, and A.O. El-Rayis, "Speedy Derivative-Corrective Mass Spring Algorithm for Adaptive Impedance Matching Networks," *Electronics Letters*, vol. 48, pp. 653-655, 2012.

4. **Y.C. Wong**, T. Arslan, and A.T. Erdogan, "Reconfigurable Wideband RF Impedance Transformer Integrated with an Antenna for Multi-band Wireless Devices," *Loughborough Antennas & Propagation Conference*, pp. 1-5, 2012.

5. **Y.C. Wong**, T. Arslan "An Adaptive Impedance Matching Network for Smart Antenna Systems" *University of Edinburgh Postgraduate Research Conference*, 2012.

6. N.H. Noordin, **Y.C. Wong**, A.T. Erdogan, and T. Arslan, "Meandered inverted-F antenna for MIMO mobile devices," *Loughborough Antennas and Propagation Conference (LAPC)*, pp. 1-4, 2012.

7. **Y.C. Wong**, T. Arslan, A.T. Erdogan, and A.O. El-Rayis, "Efficient Ultra-high-voltage controller-based complementary-metal-oxide-semiconductor switched-capacitor DC-DC converter for radio-frequency micro-electro-mechanical systems switch actuation," *IET Circuits, Devices & Systems*, vol. 7, pp. 59-73, 2013.

8. **Y.C. Wong**, T. Arslan, and A.O. El-Rayis, "Adaptive Impedance Tuning Network Using Genetic Algorithm: ITuneGA" Accepted by *NASA/ESA Conference on Adaptive Hardware and Systems (AHS-2013)*, 2013.

1.5 Summary

This thesis proposes a tunable and adaptable RF based mobile telecommunication system, where particular attention is given to:

i. High voltage switch controller based on DC-DC converters for RF switch actuation
ii. Impedance network designs for impedance transformation of RF switches
iii. Adaptive algorithms for determining the required impedance states at the RF switches for compensating the impedance variation of an antenna

Chapter 2:
High Voltage Switch Controller based Two-phase Step-up SC DC-DC Converter

2.1 Introduction

This chapter presents topologies of high voltage (HV) SC DC-DC converters and proposes design strategies for switching the SC converter. Research investigation begins with the topologies of two-phase step-up SC DC-DC converters developed in the past and the associated practical considerations. Three SC converters are selected for analysis in steady and dynamic states. From the analysis, the Fibonacci SC converter demonstrates the highest performance among the other topologies for mobile applications. However, the implementation of an HV gain Fibonacci SC converter is complex due to the requirement of widely different gate voltages for the transistors in the Fibonacci converter. Gate driving strategies, that only require few auxiliary transistors in order to provide the required boosted voltages for switching the transistors on and off, are proposed. Finally, the Fibonacci SC converter is optimised and implemented in discrete technology.

2.2 Topologies of Two-phase Step-up SC DC-DC Converter

The topology of the SC DC-DC converters can be broadly classified into linear and non-linear voltage gain converters.

2.2.1 Linear Voltage Gain Topology

The linear voltage gain topology generates the required high voltages through cascade connection of a suitable number of identical stages (*N*) to give an output voltage equal to $(N+1)*V_{DD}$ [76]. The ratio between the output voltage and the input voltage is the conversion ratio of the converter. The three mostly used linear voltage gain topologies i.e. the Dickson, the bootstrap, and the interleave structures are presented as follows.

2.2.1.1 The Dickson SC Converter

Dickson demonstrated for the first time the integrated realisation of an SC converter in 1976 [38]. This topology is similar to the Crockcroft and Walton topology proposed in 1932, which was adopted in discrete implementations [77]. The Dickson SC converter was firstly designed with diodes rather than transistors, as shown in Figure 2.1. However, isolated diodes were not available for integrated implementation. Thus, the Dickson converter was further developed by replacing the diodes with MOS transistors. The MOS transistors are in diode-connected style, as shown in Figure 2.2.

The main advantage of the Dickson converter is it does not need a clock signal in switching the transistors. However, the disadvantage of this topology is the high threshold voltage drop as it has weak gate biasing voltages associated with the diode-connected MOS transistors [78]. The gate biasing voltage in the Dickson converter is the voltage differences between the drain and the source of the transistors. In higher stages, the gate biasing voltages become less efficient in switching on the transistors because of body effect, as shown in (2.1). Increasing the body effect will increase the threshold voltage of the transistors in the

converter, see (2.2). The performance of this topology is degraded at higher conversion ratios when the number of stages increased. This significantly reduces the SC converter's output voltage and efficiency.

$$\gamma = (t_{ox} / \varepsilon_{ox})\sqrt{2q\varepsilon_{si} N_A} \tag{2.1}$$

where γ is the body effect parameter, t_{ox} is gate oxide thickness, ε_{ox} is oxide permittivity, ε_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of an electron.

$$V_{TH} = V_{TH0} + \gamma.(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}) \tag{2.2}$$

where V_{TH} is the threshold voltage, V_{SB} is the source-bulk potential, V_{TH0} is the V_{TH} with zero V_{SB} and $2\phi_F$ is the surface potential.

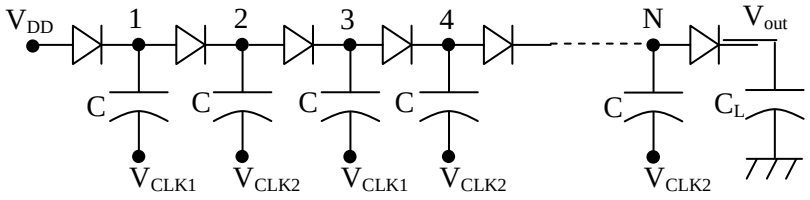


Figure 2.1: Dickson SC DC-DC converter with discrete diodes

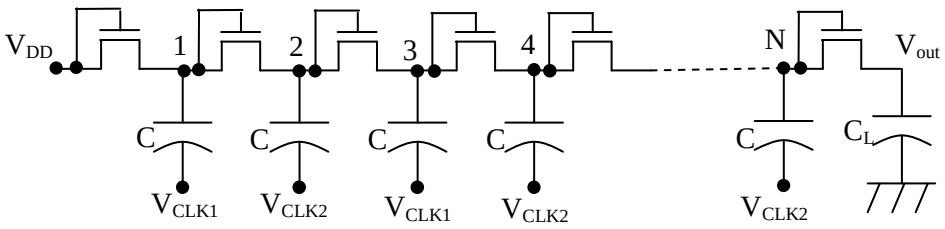


Figure 2.2: Dickson SC DC-DC converter with MOS diode connected

2.2.1.2 The Bootstrap SC Converter

A topology of a bootstrap SC converter was presented in [79, 80], as shown in Figure 2.3. In this topology, the voltages at the MOS transistor's terminals are higher than the power supply (V_{DD}). Consequently, a gate voltage with a magnitude of $2*V_{DD}$ is needed to switch on the MOS transistors. In addition, this topology requires four phases of clock signals for

implementation, which is complex in control circuitry. This topology has been enhanced by using a static backward control method to simplify the transistor control circuitry [49]. However, the method required an additional high voltage clock generator at the output stage of the converter, which increased the overall power consumption and the complexity of the design.

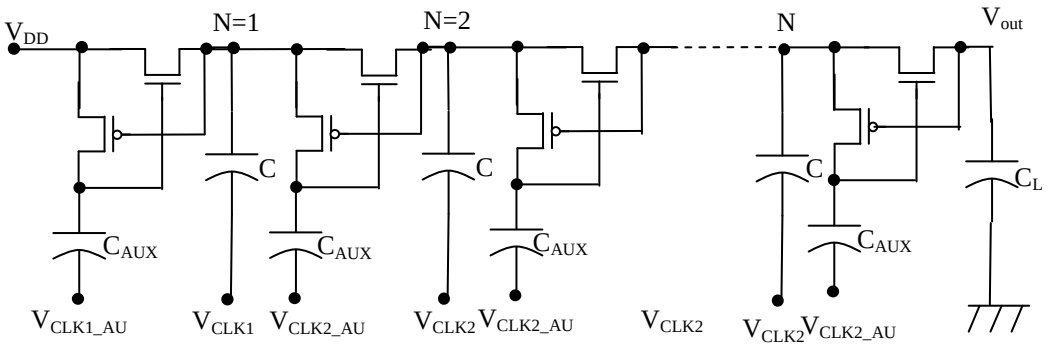


Figure 2.3: Bootstrap SC DC-DC converter

2.2.1.3 The Interleave Structure SC Converter

The interleave structure SC converter was originally proposed by [81, 82] and is shown in Figure 2.4. This topology of the SC converter is able to reduce the output ripple by using the same total capacitance. Unlike the bootstrap SC converter, the interleave structure requires only a two-phase clock and a simple design approach. More details of this topology will be discussed in Chapter 3.

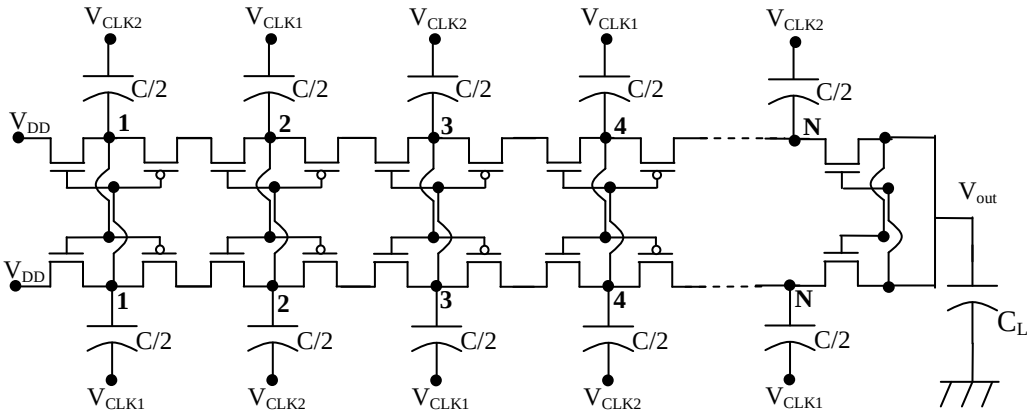


Figure 2.4: Interleave structure SC DC-DC converter

2.2.2 Nonlinear Voltage Gain Topology

For the nonlinear voltage gain topology, it shows the advantages of achieving higher conversion ratios by using fewer numbers of switches and capacitors. The three mostly used nonlinear voltage gain topologies, i.e. the series-parallel (SP), the voltage doubler and the Fibonacci structures are presented as follows.

2.2.2.1 The Series-Parallel SC Converter

The series-parallel (SP) converter was first proposed by [77], as shown in Figure 2.5. Recently, this topology has been modified by [83]. The SP converter is parallel charging all the capacitors to the V_{DD} during the first clock phase and discharging through a series connected capacitors during the second clock phase. However, the SP converter is constituted of parasitic capacitances, which affects its performance more than the other topologies. In addition, the switches implementation in the SP converter is another critical issue to be considered [39].

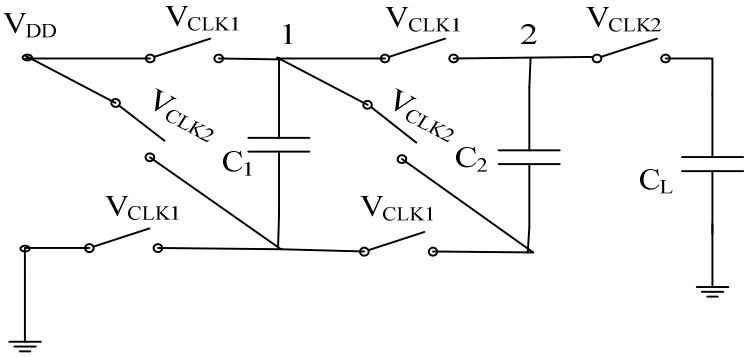


Figure 2.5: Series-parallel SC DC-DC converter

2.2.2.2 The Voltage Doubler SC Converter

The voltage doubler with a multi-phase clock was proposed by Oota et. al. [84]. This SC converter achieves the maximum voltage gain of 2^N using N+1 capacitors and 3N+1 switches by 2N phases of clock signals. The N is the number of stages in the voltage doubler converter. In the later stages of development, this exponential gain topology has been improved by using a two-phase clock [85-88].

The voltage doubler topology consists of a pair of cross-connected nMOS and pMOS transistors for charging the capacitors and transferring the charges between stages, as shown in Figure 2.6. This topology is considered to give higher efficiency when compared to the Dickson converter [31, 47, 76]. In addition, the topology shows the advantage of operating with a high switching frequency. In a high switching frequency, the topology of the voltage doubler allows the use of low voltage transistors and small capacitors [9]. Thus, it achieves a smaller die area [89] and higher efficiency [47, 90]. However, the cross-coupled structure in the voltage doubler exhibits a few serious drawbacks such as substantial switching noise caused by a large voltage ripple due to a sudden load change [91].

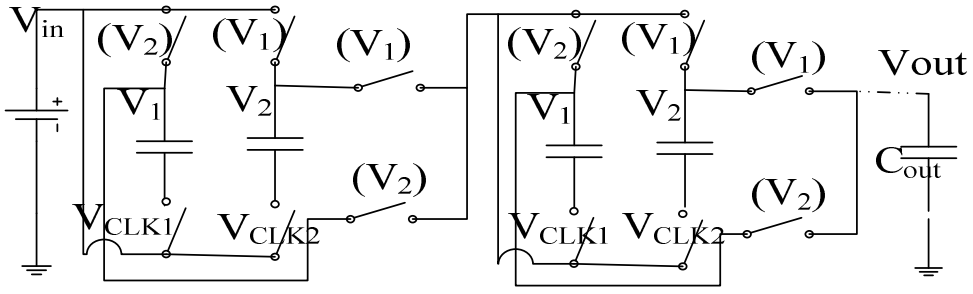


Figure 2.6: Voltage doubler SC DC-DC converter

2.2.2.3 The Fibonnacci SC Converter

Ueno et. al. proposed the Fibonnaci SC converter whose maximum attainable voltage gain is given by the number of stages of approximately 1.16exp(0.483N) [92]. The topology of the Fibonacci SC DC-DC converter is shown in Figure 2.7. Makowski carries out a systematic investigation and analysis into this topology [46, 93-96]. This gain is the maximum conversion ratio that can be attained from a two-phase SC DC-DC converter by using *N-1* capacitors. Theoretically, the conversion ratios can be ranged from 1, 2, 3, 5, 8, 13, 21, and so on. However, the implementation of the Fibonacci SC converter is limited by the technology considered [41, 97]. To maintain the voltage gain multiplication per stage, this topology requires a high amplitude of clock signal (V_{CLK}) i.e. *0V* to $F_{(N+1)}*V_{in}$. Thus, high voltage transistors must be used in this topology to avoid transistors' gate oxide break down.

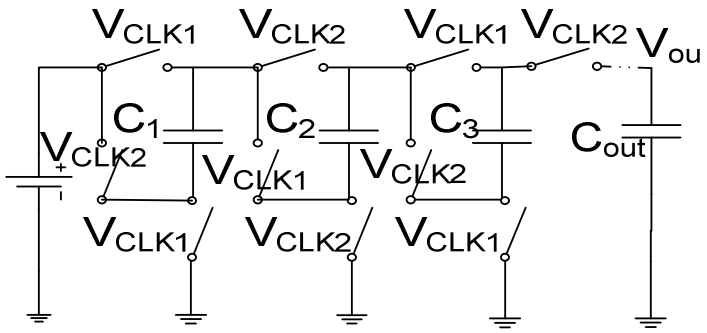


Figure 2.7: Fibonacci SC DC-DC converter

2.3 Evaluation of Key Components in the SC Converter

To achieve optimum performance of the SC converter, the key components of the converter, i.e. charge storage capacitors and charge transfer transistors, are analysed as follows.

2.3.1 Charge Storage Capacitors

The quality of the charge storage capacitor in the converter is mostly determined by its parasitic capacitance (C_P). The losses due to C_P result by a factor of α from its bottom plate, and β from its top plate of charging capacitors [42]. The factor α is generally more than one order of magnitude higher than that of the factor β. In [2], α was obtained by measuring the ratio of the parasitic capacitance of the bottom plate of the charging capacitor and the charging capacitor itself, as described by (2.3); In [42], α was derived through measurements of the input and output current. More generally, α represents a term which links the loss to the total capacitance of the SC converter that appeared in real converter after realisation. The parameter α is technology dependent and varies between 0.1 in capacitors for LV applications and 0.4 for HV applications [98].

$$\alpha = C_p / C \tag{2.3}$$

where C and C_P are the charging and parasitic capacitance per stage

Several types of capacitors have been summarised based on their parasitic capacitance, the efficiency (η) and the maximum voltage rating, as shown in Table 2.1. The charge storage capacitor with double poly technology has the smallest parasitic capacitance at about 5%, thus achieving the highest η of the converter. A thin oxide capacitor provides about 5-15% parasitic capacitances, but have a higher capacitance per area compared to the double poly capacitor [76]. Poly-metal capacitors show a moderate parasitic capacitance and also the η. External capacitors demonstrate a superior quality compared to the integrated capacitors by having a very low parasitic capacitance with α between 0.1-0.2 percent.

Besides the parasitic capacitance, the maximum voltage rating is another important constraint for the capacitor used in a high voltage (HV) SC converter. More details on the

effect of different types of capacitors to the converter and a technique to compensate the effect of the parasitic capacitance will be discussed in Chapter 3.

Table 2.1: Types of Capacitors

Types of capacitors	α	maximum η (%)	Maximum voltage rating (V)	References
Poly-metal	0.2- 0.5	50- 75	Medium	[76, 90]
Thin oxide	0.05 – 0.15	68 - 80	Low	[76]
Double poly	0.05	80	Low	[76, 90, 99]
External	0.002	70- 95.6	High	[76, 100, 101]

2.3.2 Charge Transfer Transistors

Transistors, as the charge transfer switch, are used to pass the charges to the next stage and also block the charges from leakage. The transistors operate in a linear region to transfer the high volume of charges with a small on-resistance [95, 102]. Otherwise, the transistors are in a cut-off region to block the charges from leakage. Figure 2.8 shows the current- voltage (IV) characteristic of an n type MOSFET transistor based on an AMS 0.35µm model [103]. In a cut-off region, there is no conduction between drain and source or only a sub-threshold current that is an exponential function of gate source voltage flow; in a linear region, the transistor operates like a resistor, controlled by the gate voltage relative to both the source and drain voltages. A MOSFET transistor typically used as voltage controlled current source in a saturation region. In order for a MOSFET to work efficient as a switch, the operating region of the transistor should be towards the left-side of the load line (smaller R_{DS} or on resistance in the transistor) which is the linear region of the IV characteristic curve, as shown in Figure 2.8.

NMOS and pMOS transistors can be used in the design of an SC DC-DC converter. An nMOS transistor can be switched off by applying a gate voltage of *0V* or effective gate to source voltage (V_{GS_eff}) smaller than the V_{TH} [102, 104]. To fully switch on the nMOS transistor, the V_{GS_eff} of the nMOS has to be higher than the voltage at the subsequent stage [76, 102, 105]. If the voltage difference between two subsequent stages is large, it is difficult

to switch on a charge transfer switch that uses an nMOS transistor. This situation normally happens in non-linear voltage gain topologies.

For a pMOS transistor, it can be easily switched on by having $V_{GS\_eff} \leq 0V$. However, it has difficulty in completely switching off. The design of the converter has to consider the bulk of the pMOS to avoid leakage currents from the drain or the source to the substrate [49, 102, 105, 106].

To achieve satisfactory performance of the SC converter, effective transistor gate driving strategy is needed. More design approaches will be discussed in Section 2.5.

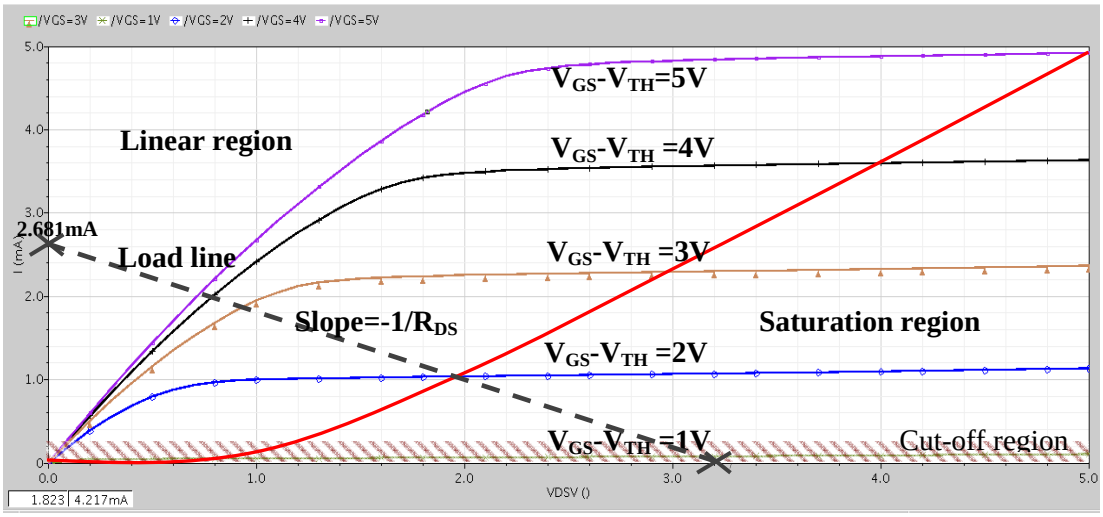


Figure 2.8: I-V characteristic curve of a transistor

2.4 Analysis of the SC Converters

Based on the presented topologies, three SC converters are selected for analysis. The topologies are the Dickson, the voltage doubler and the Fibonacci. The analysis is performed in steady and dynamic states, as follows.

2.4.1 Steady State

In a steady-state, on-resistance of the transistors plays a significant role in determining the efficiency of the converter. The on-resistance is influenced by the amplitude of the switching

clock, the sizing of the transistor and the technology considered, as shown in (2.4). The required amplitude of V_{CLK} depends on the converter's topologies. For the Dickson and the voltage doubler, V_{CLK} varies from V_{DD} to $2*V_{DD}$. While for the Fibonacci's topology, the V_{CLK} swings between V_{DD} to $F_{(N+1)}*V_{DD}$ [95, 107]. The Dickson converter uses N+1 nMOS transistors. The total on-resistance of the Dickson converter is shown by (2.5). The topology of the voltage doubler requires the highest number of transistors with *2N* of nMOS and *2N* of pMOS transistors. The total on-resistance for the voltage doubler is shown by (2.6). The Fibonacci converter requires *N* numbers of nMOS and *2N+1* pMOS transistors and its total on-resistance is shown by (2.7). Based on equations (2.4)-(2.7), these show that in order to achieve lower on-resistance in the converter, larger width of the transistors and higher V_{GS_eff} should be used.

$$r_{ds} = 1/g_{ds} = \partial I_D / \partial V_{DS} = 2L/[\lambda \mu_n C_{OX} W (V_{GS\_eff}) * V_{DS} - \frac{(V_{DS})^2}{2}] \tag{2.4}$$

where r_{ds} is the on-resistance in transistor, g_{ds} is the transconductance, ∂I_D and ∂V_{DS} are the differential of the drain current and the drain to source voltage, L and W are the length and the width of the transistor, V_{GS_eff} is the effective gate to source voltage, C_{OX} is the gate oxide of the transistor, λ is the output impedance constant and μ_n is the mobility of electrons.

$$R_{on\_Dikson} = \sum_{i=1}^{N+1} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni}) * V_{DS} - \frac{(V_{DS})^2}{2}} \tag{2.5}$$

$$R_{on\_Doubler} = \sum_{i=1}^{2N} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni}) * V_{DS} - \frac{(V_{DS})^2}{2}} + \sum_{i=1}^{2N} \frac{2L_{pi}}{\lambda_n \mu_p C_{oxp} W_{pi} (V_{GS\_effpi}) * V_{DS} - \frac{(V_{DS})^2}{2}} \tag{2.6}$$

$$R_{on\_Fibonnaci} = \sum_{i=1}^{N} \frac{2L_{ni}}{\lambda_n \mu_n C_{oxn} W_{ni} (V_{GS\_effni}) * V_{DS} - \frac{(V_{DS})^2}{2}} + \sum_{i=1}^{2N+1} \frac{2L_{pi}}{\lambda_n \mu_p C_{oxp} W_p (V_{GS\_effpi}) * V_{DS} - \frac{(V_{DS})^2}{2}} \tag{2.7}$$

where R_{on} is the total on-resistance, V_{GS_effni} and V_{GS_effpi} are the effective gate to source voltages applied to i_{th} of nMOS and pMOS respectively in the N number of stages of SC converter, λ_n is the output impedance constant, $\mu_{n/p}$ is the mobility of electrons/hole, $C_{oxn/p}$, $L_{n/pi}$, $W_{n/pi}$ are the gate oxide capacitance, the length and the width for i_{th} of nMOS and pMOS respectively.

2.4.1.1 Simulation Results

The three SC DC-DC converter topologies were simulated in Advanced Design System (ADS) 2009 based on 0.35µm CMOS technology. To have an equal comparison, all converters were simulated on their best performance setting. Width of nMOS and pMOS, charge storage capacitances (C) and output capacitance (C_{out}) were sized at their respective optimum values based on previous research works [31, 47, 95, 108]. While the length of nMOS and pMOS were set to slightly higher than the minimum channel length i.e. 0.5µm. Three of the converters were driving the same output load. Thus, the output currents were fixed and the voltages will be evaluated. The converters were switched on and off by two non-overlapping V_{CLK1} *and* V_{CLK2} with V_{DD} of 3.7V. The measurements of the voltage drop across respective transistors were performed in a steady state, where the dynamic loss can be neglected.

In a steady state, the transistors in the topologies of the Dickson, the voltage doubler and the Fibonacci are equivalent to the on-resistance, as illustrated in Figure 2.9, Figure 2.10, and Figure 2.11 respectively. The on-resistance in nMOS and pMOS are represented by the RN and the RP, respectively. Approximately similar numbers of transistors were used in the converters to have a comparative analysis of the losses by the components in the topologies.

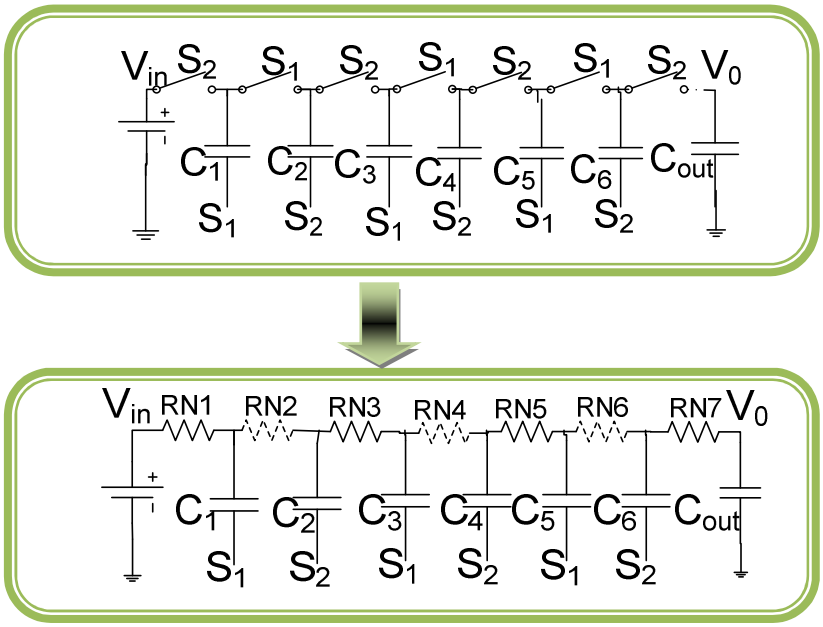


Figure 2.9: Illustration of transistors in a Dickson SC DC-DC converter in a steady state

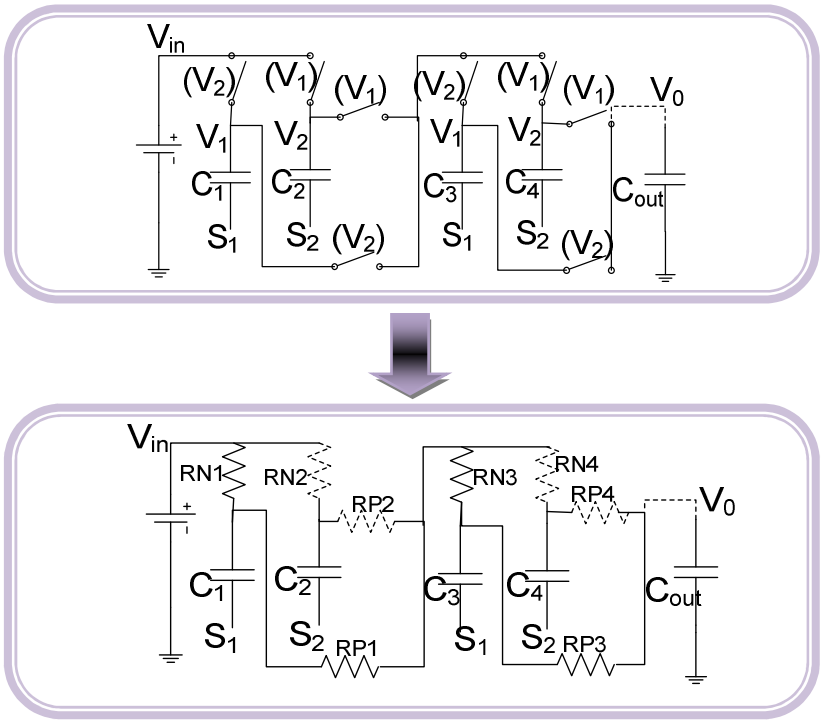


Figure 2.10: Illustration of transistors in a voltage doubler SC DC-DC converter in a steady state

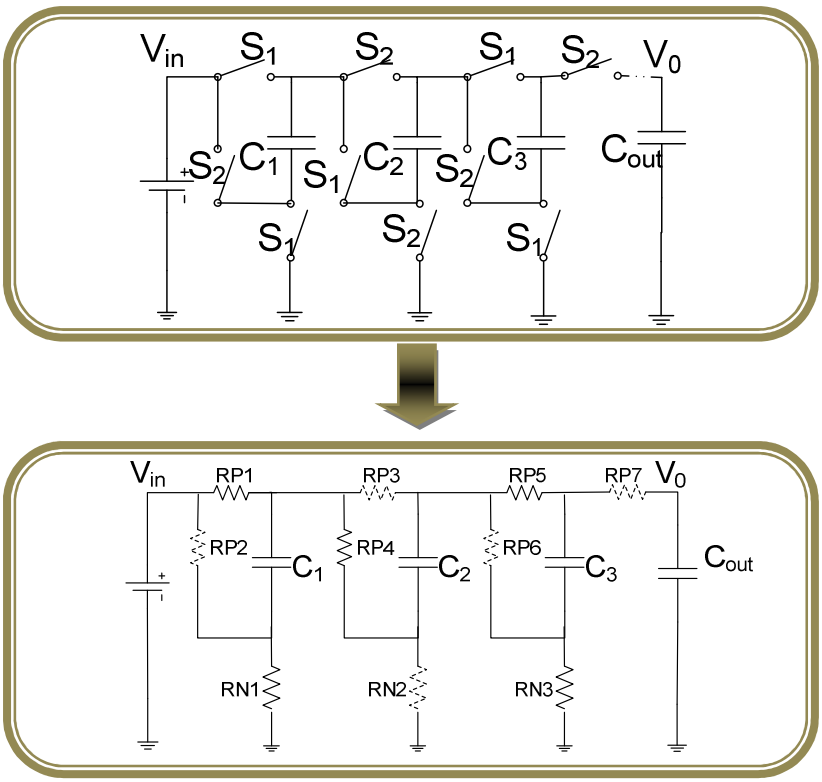


Figure 2.11: Illustration of transistors in a Fibonacci SC DC-DC converter in a steady state

Figure 2.12 shows the simulation results of the total resistive voltage drop due to on-resistance in transistors for three different converters' topologies. All of the converters' topologies have half of their total on-resistance operated in each clock cycle. Generally, nMOS transistors show higher on-resistance compared to pMOS transistors. The Dickson topology, which uses all nMOS transistors, shows the highest total resistive voltage drop. The output voltage of the Dickson converter has been reduced by a factor of $(N+1)*V_{TH}$ which contributed by the threshold voltage (V_{TH}) in the forward biased MOS diode-connected transistors. The voltage doubler shows a moderate on-resistance with a weaker $V_{GS,eff}$. The Fibonacci topology has the lowest on-resistance with its high V_{GS_eff} and a large width over length (W/L) ratio. The simulation results are aligned with the derived equations in (2.5)-(2.7) that higher V_{GS_eff} and wider W reduce the on-resistance in the converters.

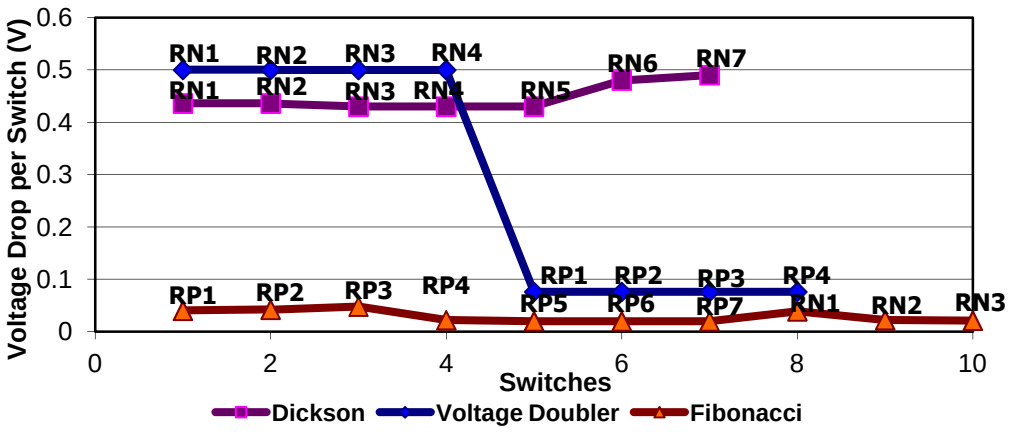


Figure 2.12: Total resistive voltage drop in the SC DC-DC converters at a steady state

2.4.2 Dynamic State

In a dynamic state, the main charge loss in transistors is due to the gate capacitances and the drain or the source to the bulk capacitances, as shown in (2.8) and (2.9).

$$Q_{OX} = C_{ox} V_{GS\_eff} (W_{n/p} L_{n/p}) \tag{2.8}$$

$$Q_{S/DB} = C_j V_{GS\_eff} W_{n/p} L_{n/p} + 2C_{jSW} V_{GS\_eff} \ (W_{n/p} + L_{n/p}) \tag{2.9}$$

where Q_{OX} and $Q_{S/DB}$ are the charges consumed by gate oxide and drain/source to bulk capacitances respectively, $W_{n/p}$ and $L_{n/p}$ are the width and the length of nMOS and pMOS transistors, C_{OX} is the gate oxide capacitance, C_j and C_{jsw} are the junction capacitances

Since same value of $L_{n/p}$ was used in the converters and $L_{n/p}$ is much smaller than $W_{n/p}$, thus $L_{n/p}$ was eliminated from (2.9). The total charge loss per switch is obtained by summing (2.8) and (2.9), as shown by (2.10).

$$Q_{Loss} \approx [C_{ox} L_{n/p} + C_j W_{n/p} L_{n/p} + 2C_{jsw}] W_{n/p} V_{GS\_eff} \tag{2.10}$$

By excluding $L_{n/p}$, C_j, C_{jsw} and C_{ox} parameters which depend on the technology considered, the remaining variables are $W_{n/p}$ and V_{GS_eff}. The total charge loss in transistors is proportional to $W_{n/p}$ and V_{GS_eff} in a dynamic state.

2.4.2.1 Simulation Results

Figure 2.13 shows that the Dickson and the voltage doubler have lower dynamic charge losses in the transistors. Low V_{GS_eff} and narrow widths of the transistors are the reasons for the low dynamic charge losses. The Fibonacci converter uses a higher V_{GS_eff} and a greater width of the transistors to accommodate the high volume of charge transfer per clock cycle. Thus, higher charge is consumed by the transistors in the Fibonacci topology at a dynamic state when compared with the other topologies, as seen in Figure 2.13.

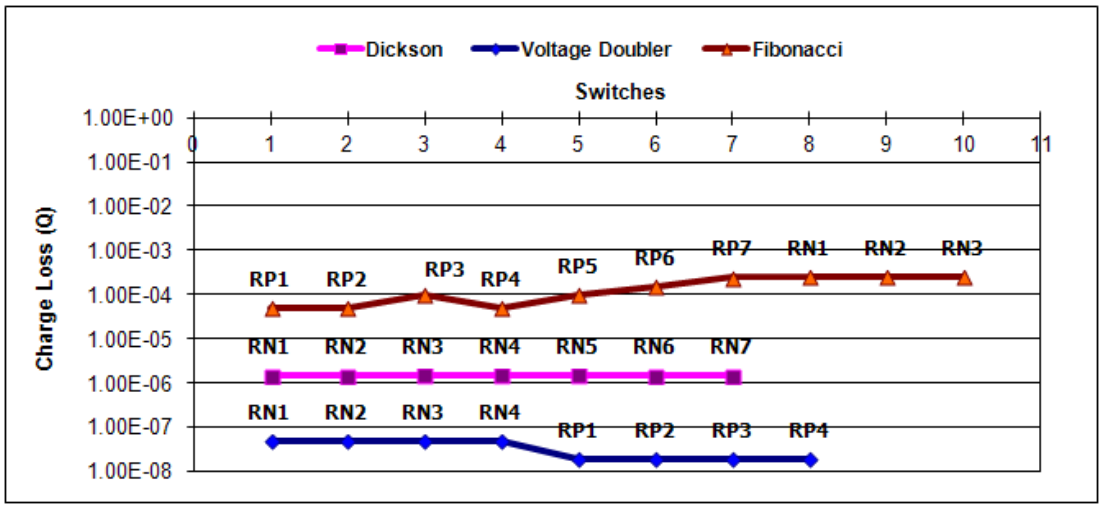


Figure 2.13: Total charge loss in the SC DC-DC converters at a dynamic state

2.4.3 Comparisons

Simulation results have been summarised and evaluated from the perspective of total voltage loss, as shown in Figure 2.14. Simulation results suggest that lower on- resistance at a steady state can be obtained by using higher V_{GS_eff} and *W/L* ratio. However, larger W/L ratio of the transistor will cause a higher charge loss in a dynamic state.

The Dickson and the voltage doubler converters have higher voltage loss per gain compared to the Fibonacci converter. The Dickson converter with MOS-diode connected structure has a weak V_{GS_eff} which results in a high on-resistance in the transistors in a steady state. A better performance of the Dickson topology can be achieved by introducing a proper gate driving technique to improve the conductivity of the transistors in the converter [31].

The voltage doubler also shows a moderate to high on-resistance with a weaker $V_{GS,eff}$. Auxiliary transistors can be used in the voltage doubler to increase the V_{GS_eff} from V_{DD} - 2*V_{DD} to 0 – 2*V_{DD} to improve the conductance of the converter [76]. Generally, the voltage doubler operates at higher frequencies compared to the Dickson and the Fibonacci topologies. The voltage doubler has been designed with the operating frequency as high as 150MHz in previous research work [47]. In this high operating frequency, high parasitic capacitance loss is another issue to be considered.

The Fibonacci SC converter exhibits the lowest voltage drop per gain and thus, achieves the highest voltage conversion ratio. The Fibonacci SC converter shows a very small on-resistance in the transistor with its high V_{GS_eff} and a large width of the transistors. However, this high V_{GS_eff} and a large width of the transistors cause the Fibonnaci to be the converter with the highest dynamic charge loss in the transistors. Even though the Fibonacci topology shows a higher dynamic loss, the resulted voltage loss from the dynamic state is relatively low compared to the steady state. In addition, the Fibonacci converter works in the hundreds of kHz frequency, which has less parasitic capacitance loss [95, 102].

The Fibonacci SC topology demonstrates the highest voltage efficiency with the lowest voltage drop compared to other topologies. It also achieves the highest gain with the minimum number of capacitors among the three topologies. In the next section, the design strategies for switching the Fibonacci SC converter will be presented.

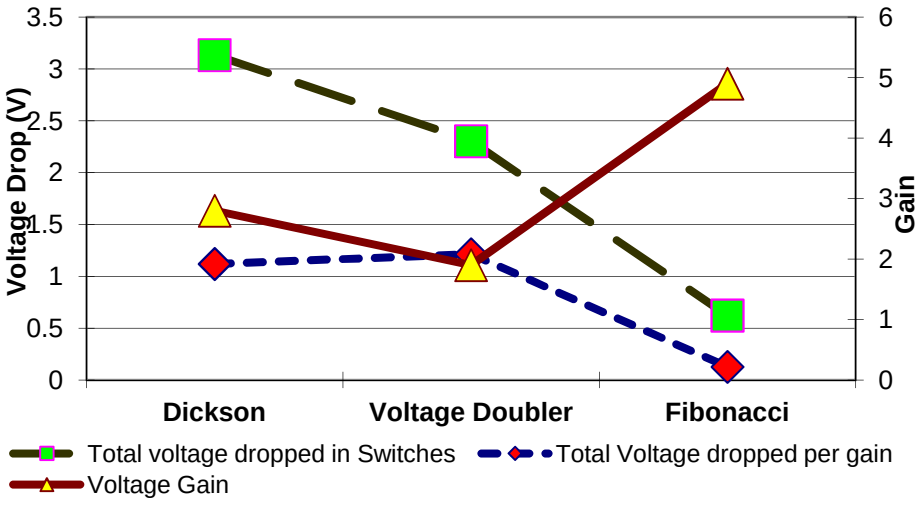


Figure 2.14 Comparison of total voltage drop versus voltage conversion gain amongst the SC DC-DC converters

2.5 Transistor Gate Driving Techniques

The effective transistor gate driving techniques are essential to ensure that the transistors work in linear or cut-off region while being switched on and off, respectively. Most of the previous works are based on pure topology aspects to characterise the Fibonacci SC converters [46, 93, 94, 102, 109]. They treat transistors as ideal switches in their analysis. Some gate driving strategies have bee proposed but limited to low and medium voltage gain and required more clock phases for the implementation [95, 102, 107].

The proposed design strategies which provide the effective gate voltages to the Fibonacci topology and consider also the reliability of the technologies used in implementation are shown in Figure 2.15 and Figure 2.16. When the clock 1 (CLK1) is HIGH, a boosted signal is obtained at output port *P2* which follows CLK1, but has a higher magnitude. Similarly, *P1* follows CLK2 which is non-overlapped version of CLK1. These boosted signals (*P1* and *P2*) are used to trigger the transistors to switch on or off, to form the alternating charges flow across the capacitors for phase 1 and phase 2, as shown in Figure 2.15. By connecting the source and bulk of pMOS transistors to the highest terminal of each stage, this can effectively reduce the leakage current to substrate.

Most of the switches are pMOS based transistors as they provide higher efficiency in charge transfer process compared to nMOS based transistors in this design. NMOS transistors are used for the switches located near the ground terminal, as shown in Figure 2.15. When the bulk terminals of nMOS transistors are connected to the ground terminal, the body effect of nMOS transistors can be eliminated which increases the overall voltage gain per stage.

Figure 2.15 demonstrates the implementation of a step-up Fibonacci converter for low to medium voltage conversions. A diode is placed between V_{DD} and the level shifter to provide an initial voltage for starting up the level shifter. When the output voltage is higher than V_{DD}, the diode will be turned off. The output voltage (V_{out}) of the Fibonacci converter can be directly fed to the level shifter for a higher clock magnitude. By switching *P1* and *P2* voltages between 0V and $F_{(N+1)}*V_{DD}$, a sufficient voltage level can be obtained for switching off the pMOS transistors. To switch on the nMOS transistors, a voltage of V_{DD} is enough when the source and bulk terminals of nMOS transistors are connected to the ground. Both pMOS and nMOS transistors can be easily switched on and off by using 0V respectively.

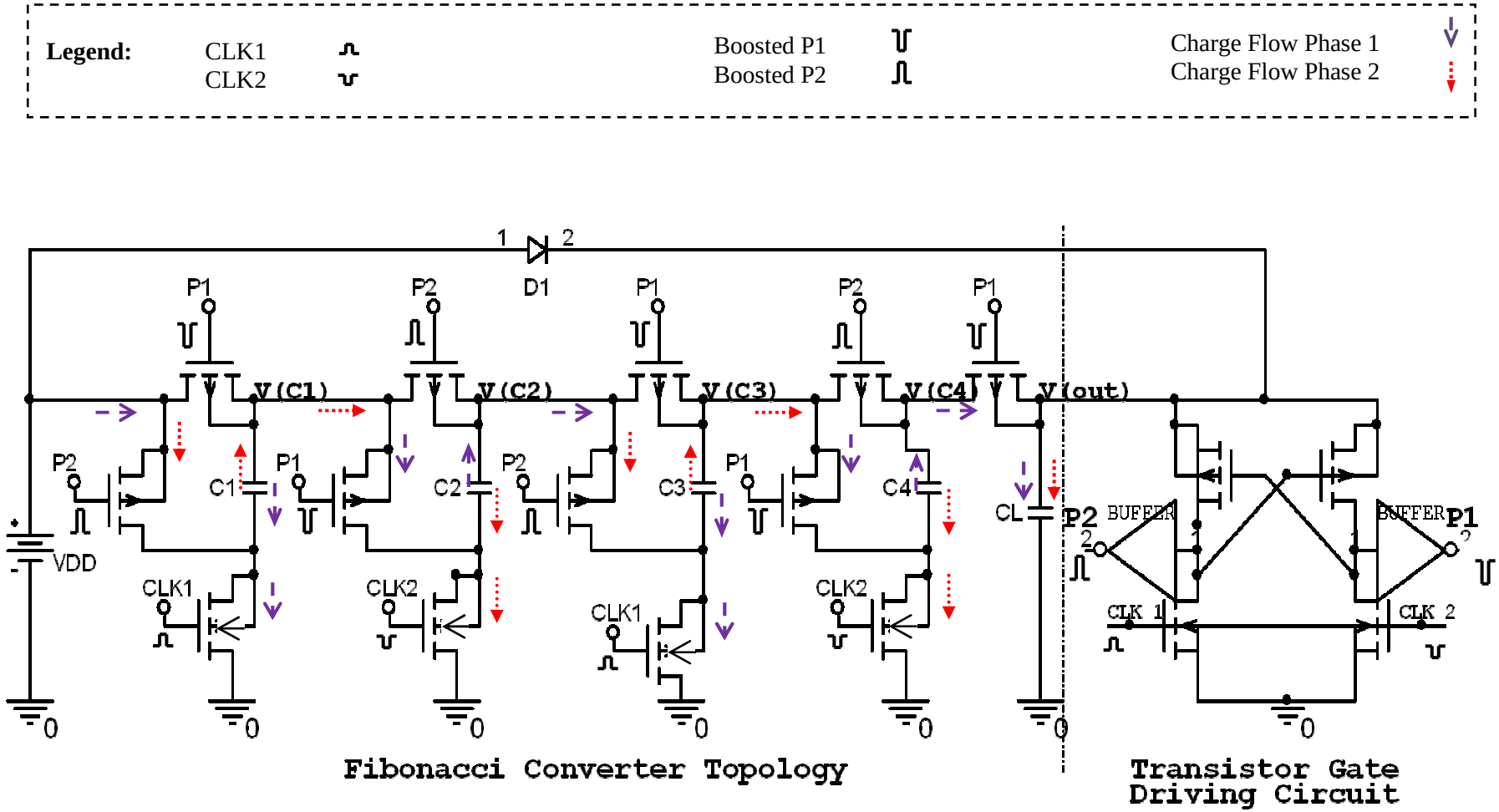


Figure 2.15: Effective gate driving technique for a low to medium voltage conversion gain Fibonacci SC DC-DC converter

This gate control technique is quite straightforward, since these transistors will not face the risk of exceeding their technology maximum limits of gate source voltage (V_{GS_MAX}) and drain source voltage (V_{DS_MAX}). High voltage thick oxide transistors are used with this topology to avoid transistor gate oxide breakdown.

For a high voltage conversion, auxiliary transistors have to be used to boost the voltage at each stage or cell based on the developed reference voltage from other nodes. It is not appropriate to direct switching the gate voltage of the transistors between 0V and $F_{(n+1)}*V_{DD}$. The gate of the transistors will suffer from breakdown with high voltage level stresses at V_{GS}. For instance, a V_{GS} voltage of – 29.6V needs to be held by transistors in an 8X Fibonacci converter with a 3.7V of V_{DD}.

The gate driving approach in this nonlinear topology is different from the linear topology such as the Dickson converter. In the linear topology, CLK1 and CLK2 are able to access each cell node, thus an initial voltage can be pumped through the capacitors in parallel. Previous researcher proposed a backward control which uses the already established high voltage to control the transistors of the previous stage for biasing the linear topology [49]. However, this approach is not suitable for the Fibonacci converter, where clock phases are not directly attached to the capacitors. In the Fibonacci converter, all capacitors are flying capacitors, which mean both end terminals of the capacitors are connected with transistors rather than fixed at supply or ground terminal, as shown in Figure 2.16.

For this reason, a forward control technique is proposed for the Fibonacci converter. As shown in Figure 2.16, each cell of the converter consists of three main transistors. Each transistor needs to be able to turn on and off at the designated clock phases to allow charges to be pushed to the next stage, and block charges from leaking to the previous stage or ground. An example of driving the three main transistors in the fourth stage of the Fibonacci converter has been used to illustrate the proposed technique.

For instance, by using the previous cell node voltage, e.g. V(C2), as the source voltage and the current cell voltage, V(C4), as the drain voltage for auxiliary inverters, the transistor, MP1_4, can be turned on by V(C2) and turned off by V(C4), as shown in Figure 2.16. For the middle transistor, MP2_4, a gate drive circuit is also needed to generate a boosted voltage for switching MP2_4 on and off at the designated clock phases. Therefore, the drain of MP2_4 is connected to the drain of MN1_4 while the source port of MN1_4 is grounded. For the high voltage conversion Fibonacci converter, the voltage at the drain of

MN1_4 in the higher stages will sustain some voltage levels rather than being grounded, due to an increasing volume of charge trapped in the capacitors. Therefore, for long cascaded stages of the Fibonacci converter, there will be a voltage present at V(C4_0), as shown in Figure 2.16. It is easier to switch on and off the charge transfer switch by using an nMOS rather than a pMOS. Thus, MP2_4 have been replaced by an nMOS (MN2_4), which will be switched on and off by a level shifter (AP2_4 and AN2_4). The MN2_4 can be turned on by V(C4) and turned off by V(C4_0). By using the reference voltage for switching the transistors, it will not exceed the technological limits of V_{DS_MAX} and V_{GS_MAX} of the transistors. For the bottom nMOS transistors, MN1_4, with its ground reference terminal, a voltage level of 0V and V_{DD} is enough to turn the transistor off and on.

For long cascaded stages of the Fibonacci converter, a combination of level shifter and the proposed forward control technique can be used. A level shifter can be used to provide the required voltage levels for the transistors at the first, second and third cells, as shown in Figure 2.16. For the fourth and higher stages of cells, the forward control technique can be used, for effectively driving the transistors. The voltage supply (V_{LS}) of the level shifter has to be connected to the internal cell node rather than the output voltage of the converter in order to avoid the breakdown of the transistors. By doing this, the number of auxiliary transistors can be reduced and the transistors remain operating within the specification margins.

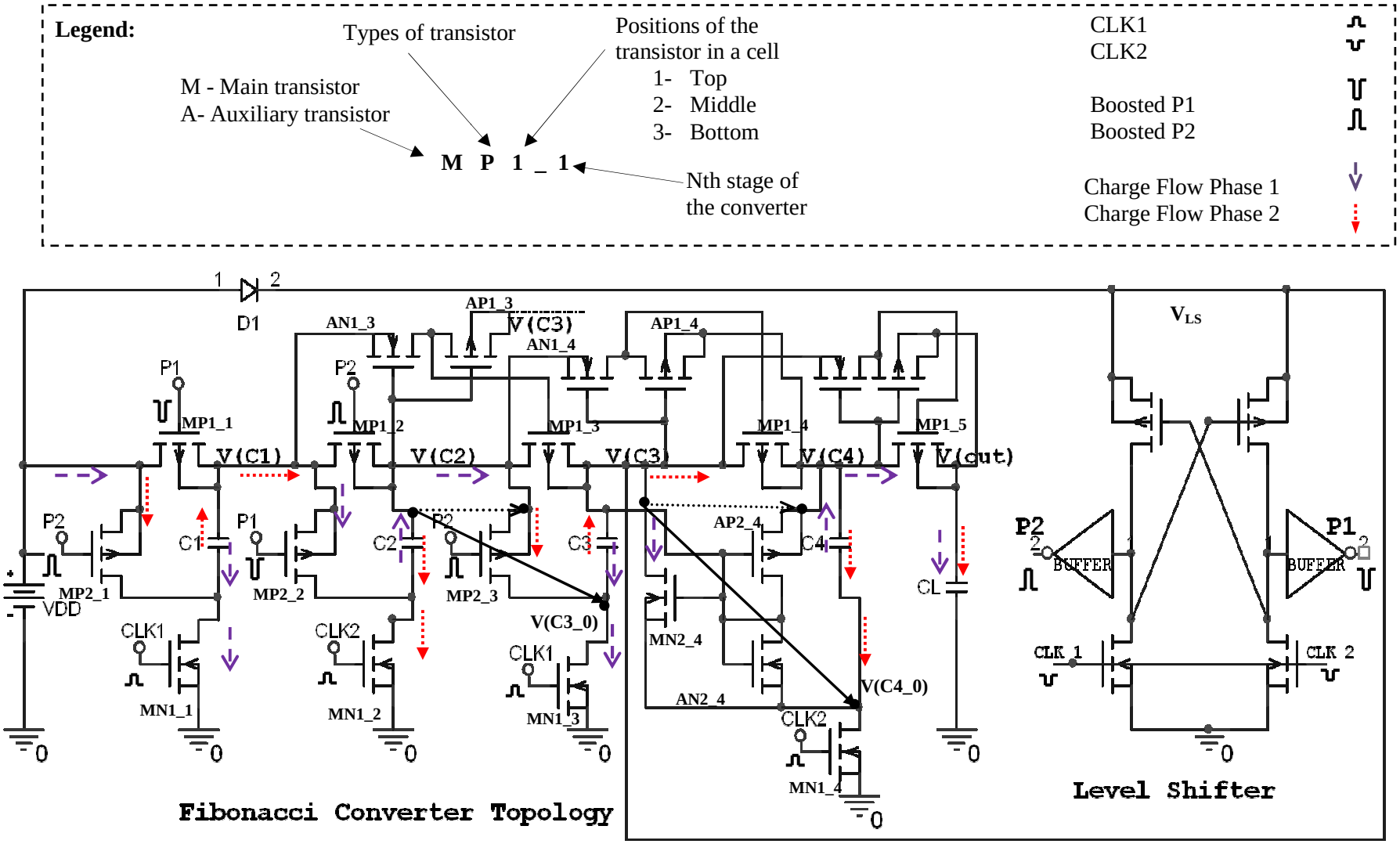


Figure 2.16: Effective gate driving technique for a long cascaded high voltage conversion gain Fibonacci SC DC-DC converter

2.5.1 Optimisation of the Fibonacci Topology

The Fibonacci topology can be optimized based on capacitors or transistors. By optimizing these two elements, slow and fast switching limits of a converter can be determined. Capacitors in the Fibonacci converter do not carry the same DC voltages. The voltages in capacitors follow the Fibonacci sequence [93]. By using the charge balance model (2.11), the size of the charge storage capacitor (C_{Store}) should be arranged in reverse order of the Fibonnaci sequence, as shown in Figure 2.17. The largest capacitor should be placed next to V_{DD} and the smallest next to output load capacitor (C_L).

$$C = Q/V \tag{2.11}$$

The optimization can also target the sizes of transistors. Using too large transistors will increase the parasitic loss; conversely, small size switches are not able to accommodate sufficient amount of charge, which results to a lower output voltage for a particular frequency. Sizes of the transistors should follow the multiplier (q), as shown in Figure 2.17.

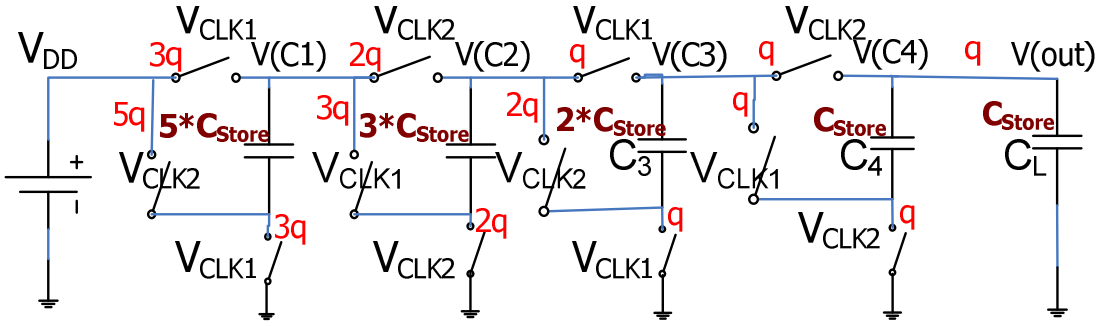


Figure 2.17: Charge flow and optimisation in the Fibonacci SC DC-DC converter

2.5.2 Simulation Results

To demonstrate the effectiveness of the proposed gate driving techniques, the Fibonacci SC converter, as shown in Figure 2.16, is designed and simulated using AMS 0.35µm technology. A V_{DD} of 3.7V was supplied to the converter. The length of the transistors was set to 1µm while the width of the transistors followed the multiplier (*q*) sequence with minimum of 1000µm. Capacitor (C_{Store}) was set to the market available size, 33nF. Non-overlapping clock signals, V_{CLK1} and V_{CLK2}, were generated for switching the converter to avoid charge leakage from short circuit path. A high voltage transistor device model with V_{GS_MAX} and V_{DS_MAX} of 20V was chosen for the simulation of this converter.

The simulation results demonstrate the effectiveness of the proposed gate driving techniques for the Fibonacci SC converter, providing a conversion efficiency (η) of up to 88%. The transistors can be turned on and off at the designated clock phases and without exceeding their transistor technology limits, as shown in Figure 2.18. The magnitudes of V_{CLK1} and V_{CLK2} swing from 0V to 3.7V, while the magnitudes of P1 and P2 swing from 0V to 10.3V. Both switching signals remain within the V_{GS_MAX} of the transistors. Similarly, V_{DS_MAX} of the transistors is kept within the transistor technology limits. For example, V_{DS} of transistor MP1_2 is determined by the voltage difference between V(C1) and V(C2) which is less than 20V, as shown in Figure 2.16. Slow and fast switching limits of the converter are also demonstrated. A faster rise-up time can be obtained by multiplying the capacitors with the reverse of the Fibonacci sequence. Whereas, using same size capacitors lead to an output with a longer rise-up time, as shown in Figure 2.19.

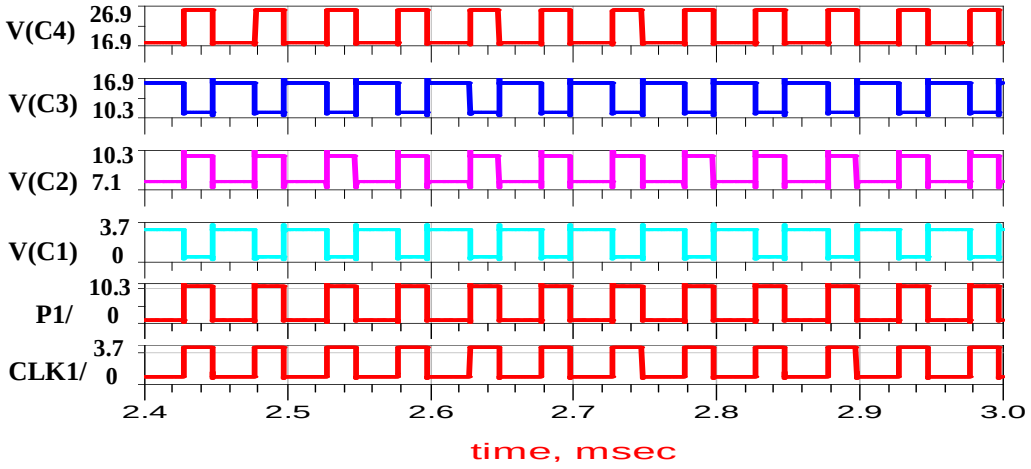


Figure 2.18: The internal node voltage levels for the *8X* Fibonacci SC DC-DC converter

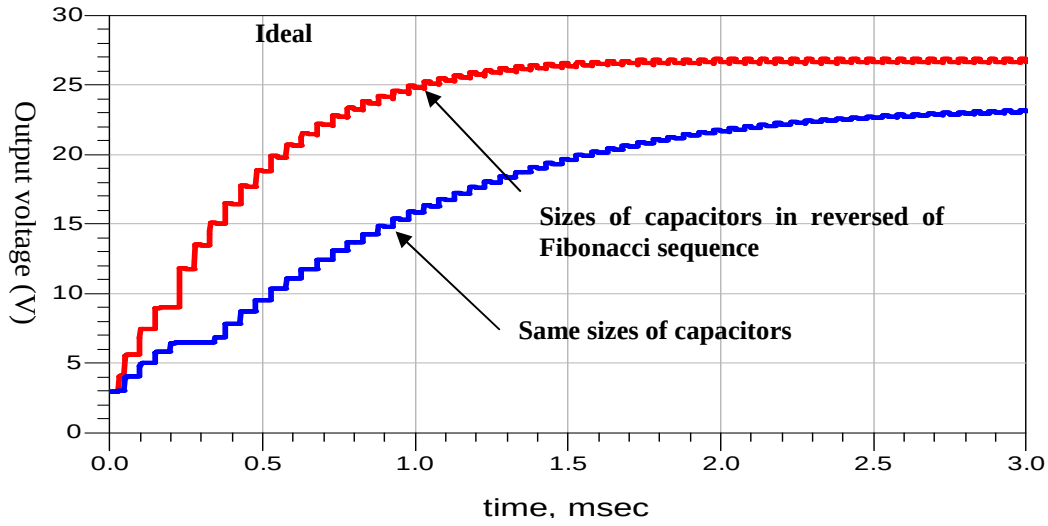
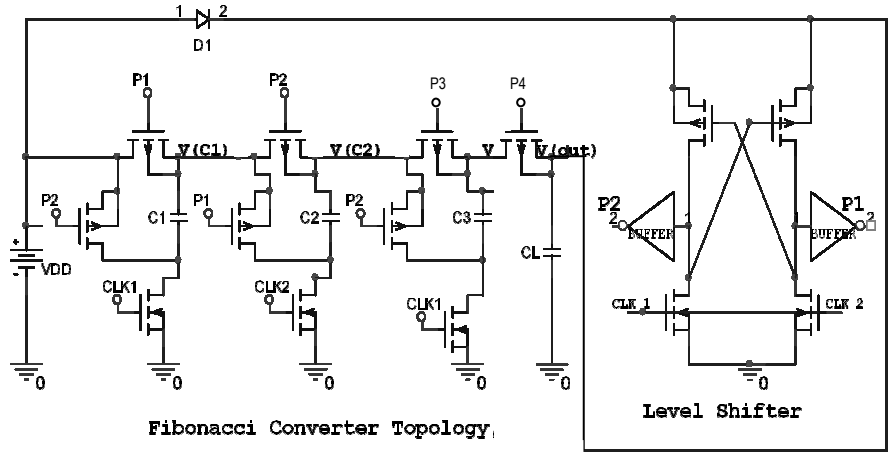


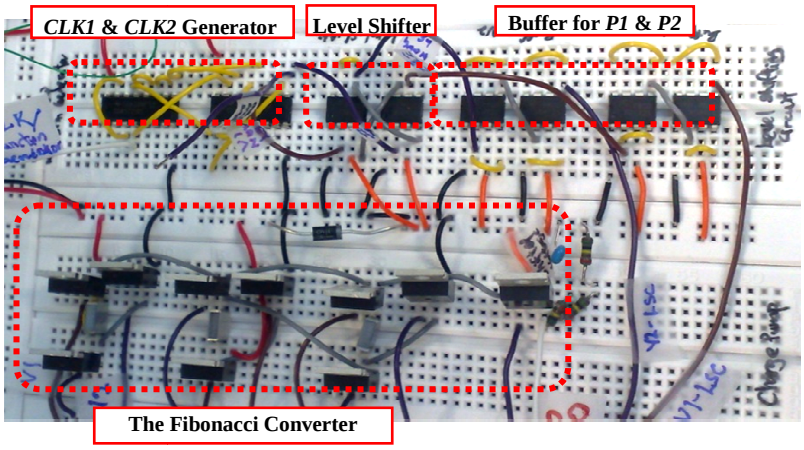
Figure 2.19: The simulated output voltages for the *8X* Fibonacci SC DC-DC converter

2.5.3 Verification

The *5X* Fibonacci SC converter has been realised by using discrete components, as shown in Figure 2.20. Ceramic capacitors, which have a low equivalent series resistance (*ESR*), have been used in the prototype. A function generator was used to generate the input non-overlapped clock signals *CLK1* & *CLK2*. Figure 2.21 show the prototype provides a voltage conversion efficiency η of 72%. The slightly discrepancy is due to the higher V_{TH} in the discrete transistors and also the non-ideality in CLK1 and CLK2.



(a)



(b)

Figure 2.20: The fabricated 5X Fibonacci SC DC-DC converter by discrete components (a) circuit diagram (b) prototype

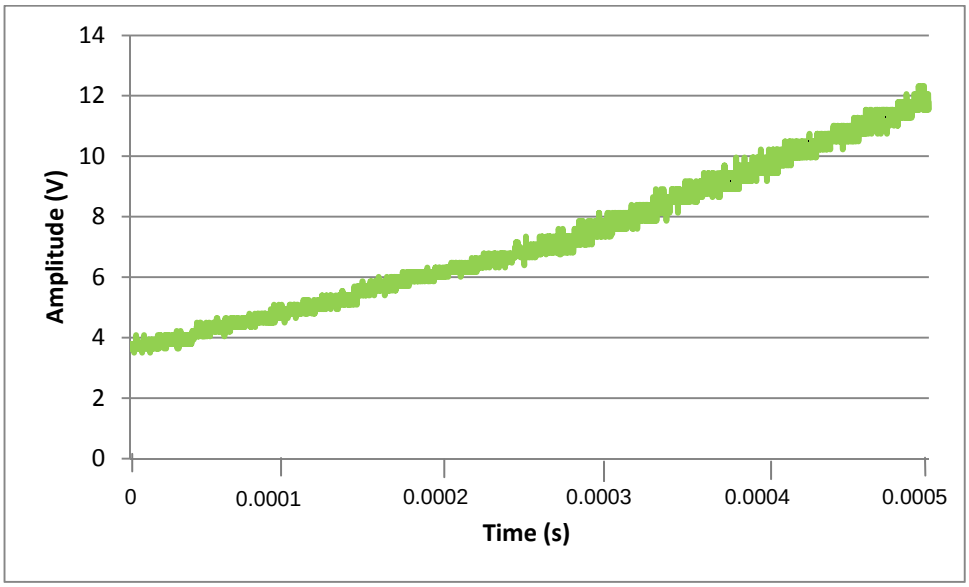


Figure 2.21: Measurement result of the SC DC-DC converter

2.6 Discussion

Generally, nonlinear voltage gain SC converters are adopted for discrete implementations. They have been seldom used in integrated circuit (IC) implementations, since it was considered inefficient for this use [39]. Only recently, a few nonlinear voltage gain SC converters were developed in an IC environment, but their designs were either low voltage gain design [110, 111] or using off-the-shelf components [76]. Thus, with the limited current state-of-art IC technology, discrete technology is still the best for nonlinear voltage gain topology implementation [40].

Due to voltage differences between stages of the Fibonacci converter being high, thus higher voltage ripple is observed at the output of the converter. A large output capacitor has to be used to compensate the voltage ripple. This is not an issue for discrete capacitors which have a high capacitance per area and a low stray capacitance. A significantly smaller prototype area can be achieved by using transistors and capacitors in surface-mount assembly (SMA) packaging.

To consider the nonlinear HV SC converter for IC technology at a future stage of development, two main factors need to be considered. First, the transistors have to be selected within the high voltage rating limits. Second, the capacitors have to choose from a high capacitance per area and a high voltage rating limit in order to minimise the area and achieve high reliability.

2.7 Summary

Topologies of two-phase SC DC-DC converters, as controllers for tunable RF devices, have been discussed in this chapter. These include the Dickson, the Bootstrap and the interleave topologies for linear voltage gain topologies; for non-linear voltage gain topologies, they have the series-parallel, the voltage doubler and the Fibonacci topologies. The properties of the main components in an SC converter, which are capacitors and transistors, have also been analysed in order to identify the parameters that influence the performance of the converter. Losses in the topologies have been compared in steady and dynamic states. From the comparison, the Fibonacci SC converter has been identified as having the lowest voltage loss per gain compared to other topologies. This topology also shows the advantages of using a lesser number of capacitors, which results in a high conversion ratio. However, the implementation is complex for a high voltage gain Fibonacci SC converter because of the requirement for a widely different gate voltage for the transistors in the Fibonacci converter. For this reason, two gate driving techniques for implementing the Fibonacci SC converter for both low and high step-up conversion ratios have been proposed in this chapter. The proposed gate driving techniques only require a few auxiliary transistors in order to provide the required boosted voltages for switching the transistors on and off. As a result, the proposed gate driving techniques reduce the design complexity and increase the reliability of the Fibonacci SC converter. The sizes of the transistors and the capacitors of the converter have also been optimised for a higher switching speed. The simulation results verify the proposed techniques. A prototype of the Fibonacci converter has also been fabricated. Good agreement has been achieved between the measured and simulation results. Figure 2.22 summaries the areas and the challenges presented in this chapter. In the next chapter, the design of linear voltage gain topology in integrated technology will be discussed.

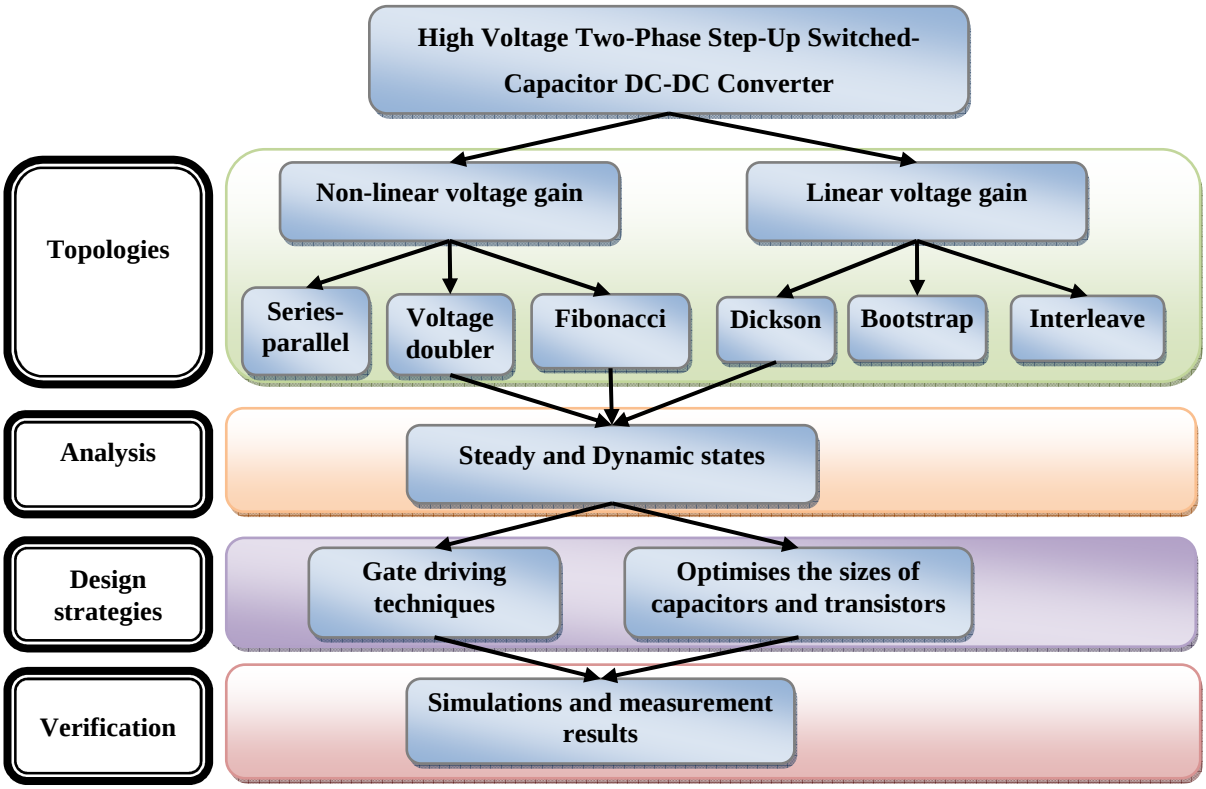


Figure 2.22: Summary of the areas and the challenges addressed in Chapter 2

Chapter 3:
High Voltage Switch Controller based CMOS SC DC-DC Converter

3.1 Introduction

Design of a non-linear voltage gain converter based on discrete technology has been presented in Chapter 2. This chapter presents design and development of an integrated two-phase HV SC DC-DC converter. Novel design techniques for a higher output voltage and lower power consumption in a smaller die area are proposed. The design of the HV SC DC-DC converter is based on low voltage (LV) transistors in order to achieve higher voltage conversion. However, it is very challenging to design HV converter using low voltage transistors in CMOS technology. Two inter and final stages adaptive biasing circuits are proposed to eliminate the leakage current, hence avoiding very high current peaks flowing to the substrate. Through the proposed design techniques, the SC DC-DC converter achieves higher boosted voltage compared to converters that use HV transistors. In addition, the design parameters of the SC DC-DC converter have been analysed and optimised. The effect of parasitic capacitance in high voltage capacitor has also been identified and reduced by the charge recycling circuit. Thus, these significantly reduce the die area and the power consumption of the proposed SC DC-DC converter. The proposed HV SC DC-DC converter has been benchmarked, taking into consideration previous research works in the literature.

3.2 High Voltage Switch Controller based CMOS SC DC-DC Converter

There are several types of topologies for SC converters such as linear voltage gain [38, 49], doubler voltage gain [47, 89, 90], and Fibonacci voltage gain [46, 97], as have been discussed in Chapter 2. When implemented in CMOS technology, the linear voltage gain shows the best performance among these topologies [40]. Previous research in linear voltage gain SC converters is targeted at non-volatile memory where the focus of the research is on LV operation and high output currents [47, 49, 50, 78, 98, 106]. However, these design merits are not suitable for an HV SC DC-DC converter targeted at RF switches, in particular RF MEMS applications. Most commercially available SC DC-DC converters are limited to maximum output voltages between 12V and 15V. To achieve higher output voltages, bulky and costly solutions based on external discrete components tend to be used. This chapter presents a complete design, analysis and synthesis of an integrated HV SC DC-DC converter for low power consumption and small die area in CMOS technology.

RF MEMS switches require an actuation voltage in the range of 0V to 30V which is provided by a customised SC DC-DC converter design. The area of the SC converter has to be small for the integration with the RF MEMS in a single package. To reduce the output ripple and gate oxide stress, an interleave structure linear voltage gain SC converter topology [78, 106] is applied. The initial design of this converter is for an LV converter application [78, 106]. In this work, an HV SC converter based on the enhanced LV interleave topology is proposed.

3.3 Operation of High Voltage SC DC-DC Converter

The design of the enhanced LV interleave topology begins with the operation of the converter, as shown in Figure 3.1. Each stage of the SC converter is composed of an nMOS transistor (NM), a pMOS transistor (PM), and a charging capacitor (C). The second row has the same topology as the first row. Clock 1 (*CLK1*) and clock 2 (*CLK2*) are non-overlapped clocks. When *CLK1* is HIGH, a boosted signal (*P1*) is obtained at the source terminal (*S*) of the transistors, as shown in Figure 3.1. The waveform of *P1* follows *CLK1*, while *P2* follows *CLK2*. These boosted signals (*P1* and *P2*) are used to trigger the MOS transistors to

switch on or off, to form the alternating charge flow across the capacitors for phase 1 and phase 2. For instance, *P1* is HIGH when *CLK1* in the 1st stage of the SC converter is HIGH. HIGH *P1* will switch on NM_{21} and switch off PM_{21} in the 2nd row of the SC converter. Similarly, when CLK2 in the 2nd row is LOW, it will switch off NM_{11} and switch on PM_{11}. The off state of PM_{21} and NM_{11} will block the charge from going back to the previous stage, while the on state of PM_{11} and NM_{21} will pass the charge to the next stage. *P1* and *P2* in this interleave structure provide effective gate switching potentials for boosting up the charge. Different biasing techniques to control the n-type potential (V_{B_N}) and the p-type potential (V_{B_P}), and the bulk-substrate potential (V_{B_S}) of the transistors in inter and final stages are discussed in the next section.

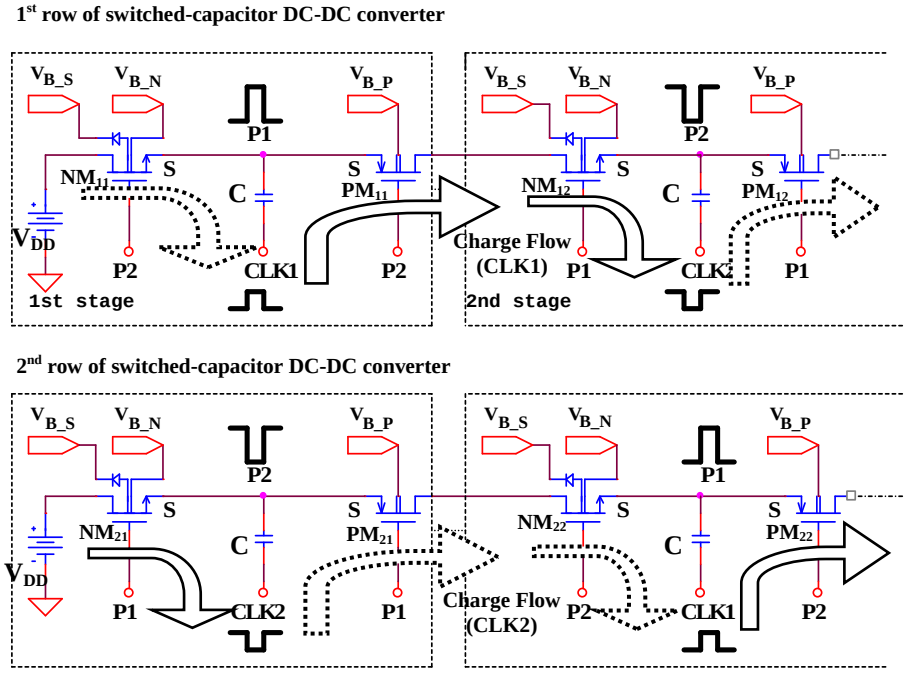


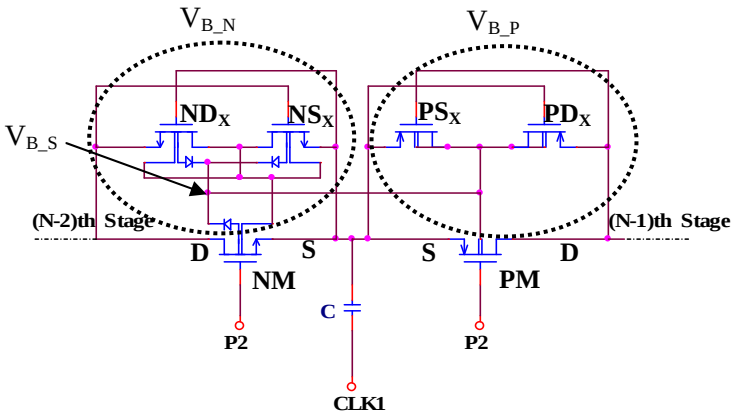
Figure 3.1: Interleave structure linear voltage gain SC DC-DC converter

3.4 Design of High Voltage SC DC-DC Converter

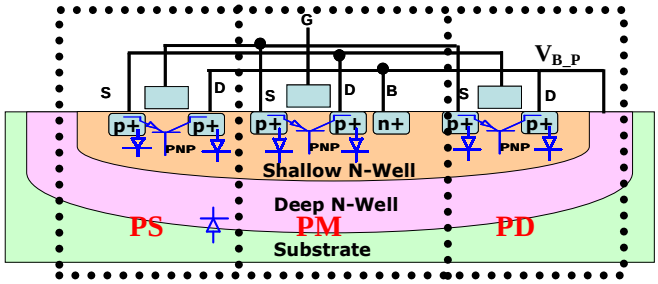
The bulk potential of the transistors needs to be properly biased when LV transistors are employed in an HV design in order to avoid circuit latch-up and break-down. In [78], the bulk of nMOS and pMOS transistors are recommended to be connected to their source. Improvements in operating pMOS transistors are recommended in [106], but the designs are still limited to LV applications only. In this work, two adaptive bulk biasing circuits for inter and final stages of the SC DC-DC converter are proposed. Through the proposed adaptive bulk biasing techniques, the leakage current is eliminated. Thus, the reliability of the SC converter for high output voltage using low voltage transistor technology is assured.

3.4.1 Adaptive Bulk Biasing Circuit

The proposed inter stage adaptive bulk biasing circuits for pMOS and nMOS LV transistors are shown in Figure 3.2(a). In the case of a small conversion ratio SC converter, the bulk of the nMOS transistors (V_{B_N}) was grounded. However, for a larger conversion ratio SC converter, if V_{B_N} is still at zero potential, not only it will increase its bulk effect significantly but also may cause the transistor to break down when the potentials between the drain-bulk, source-bulk and gate-bulk are greater than the technology specific voltage limits. Thus, two auxiliary nMOS transistors (ND_X and NS_X) are used to adaptively set the V_{B_N} to the lowest potential between its drain (D) and source (S) in every stage, as shown in Figure 3.2(a). For instance, when the potential of the drain of nMOS is higher than its source, NS_X becomes forward-biased, and sets the V_{B_N} approximately to nMOS's source potential. On the other hand, when the potential of the drain of nMOS is lower than its source, NDx sets the V_{B_N} to nMOS's drain potential. By having this adaptive bulk biasing circuit, the V_{B_N} will always be at the lowest potential and within the technology limit. Similarly but in an opposite way, two auxiliary transistors (PS_X and PD_X) are used to set the bulk voltage of pMOS (V_{B_P}) to the highest between its drain and source, as shown in Figure 3.2(a). Through the proposed biasing circuit, the source-bulk voltage in each stage of the SC converter no longer increases. Thus, the threshold voltage (V_{TH}) remains almost constant even with a large number of stages.



(a)



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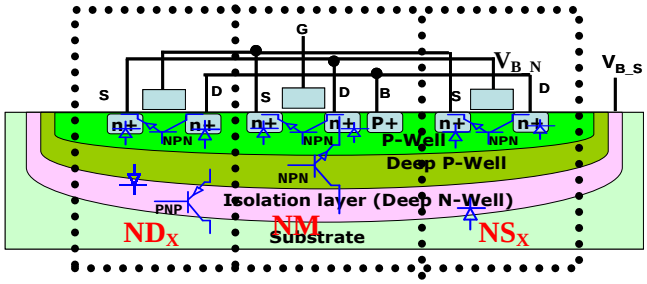


(c)

Figure 3.2: Single stage of the SC DC-DC converter with adaptive bulk biasing circuit (a) schematic, (b) the equivalent cross-section in floating pMOS LV transistors, and (c) the equivalent cross-section in floating nMOS LV transistors with parasitic elements

The cross-section views of two types of transistors (PM and NM) in a single stage SC DC-DC converter are illustrated in Figure 3.2 (b) and (c). In this design, the conventional substrate-based (standard) LV transistor is replaced by a floating LV transistor. The substrate-based LV transistor generates substrate noise and collects substrate current [103].

The floating LV transistor has an additional isolation layer, which is not found in standard transistors, is to cater for the technology allowable limit between bulk-substrate from 7V to 50V. In addition, the floating LV transistor is more robust against substrate noise. The floating LV transistor is available for all HV process options. The process option used in this design is the 0.35µm 50V CMOS Design Kit. The area penalty for the floating LV transistor is negligible.

The PM is a floating pMOS LV transistor with deep and shallow N-wells on p-type substrate, as shown in Figure 3.2 (b). The deep N-well is the isolation layer. The shallow N-well is the bulk of the PM. Both N-wells have to be biased with the highest potential (V_{B_P}) to avoid switching on the junction diode and further triggering the parasitic PNP bipolar transistor as shown in Figure 3.2 (b). Thus, this illustrates the importance of two auxiliary transistors (PD and PS) laid on both sides to bias the bulk and substrate of PM to the highest potential to ensure that no leakage current is drawn to the substrate.

Figure 3.2 (c) shows the cross-section view of a single floating nMOS LV transistor biased by two auxiliary transistors (ND_X and NS_X). This additional isolation layer will be biased by the substrate potential (V_{B_S}) which is obtained from the V_{B_P} as shown in Figure 3.2 (a). For the bulk biasing in the nMOS, it is similar to the pMOS but in an opposite way. The bulk of the nMOS has to be biased to the relatively lowest potential through ND_X and NS_X to avoid switching on the parasitic NPN transistor.

Through this adaptive biasing technique, the HV SC converter can be prevented from latch-up, which guarantees the reliability of the HV SC converter design using LV transistors. The work presented here is not limited to floating LV transistors and can be extended to other standard/substrate-based LV transistors by ensuring the targeted output voltage of the design is within the technology allowable limits of the transistor models.

3.4.2 Output Stage of the SC DC-DC Converter

The proposed adaptive biasing circuit for the output stage of the converter has been carefully designed to accommodate the voltage ripples when driving the variable capacitive MEMS load, as shown in Figure 3.3. The bulk of the PM at the final stage of the converter is biased by the voltage that is slightly higher than the V_{out} (V_{B_F}), as shown in Figure 3.3. The V_{B_F} can be obtained by complementing the two boosted voltages (V_{XC1} and V_{XC2}). These boosted voltages are obtained from V_{X1} and V_{X2} that are connected to the output node (V_{out}) through two small auxiliary transistors (M_{AUX}) and capacitors (C_{AUX}), as shown in Figure 3.3. The V_{XC1} and V_{XC2} can be obtained through the transistor (M_{CX}) and a serial large resistor (R_X). The magnitudes of V_{XC1} and V_{XC2} are slightly higher than V_{out} and P_1 or P_2, but within technology allowable limit of the transistors. By complementing the V_{XC1} and V_{XC2} through the adaptive output reference, a rather linear V_{B_F} can be obtained. By using this output stage biasing circuit, the SC converter can directly be connected to RF MEMS switches without adding a large output capacitance to compensate the ripple due to the variable capacitive load. By avoiding the large output capacitance, the proposed design demonstrates a smaller die area and a faster rise time.

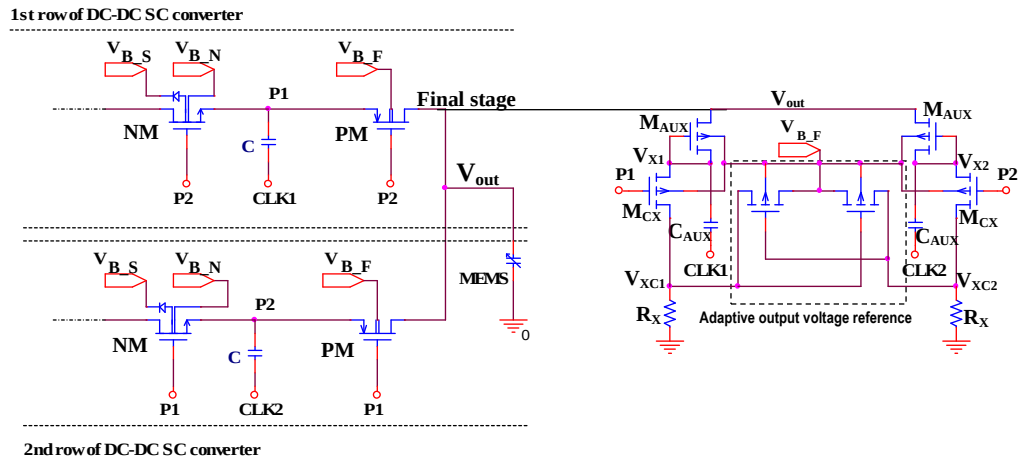


Figure 3.3: Output stage of the SC DC-DC converter with an adaptive output stage biasing circuit

3.5 Analysis of the Design Parameters of High Voltage SC DC-DC Converter

3.5.1 Voltage Gain Efficiency

The main components of an SC DC-DC converter are the transistors and the capacitors. The first integrated SC DC-DC converter was introduced in [38]. For an ideal *N* stage SC DC-DC converter with ideal transistors and capacitors driven by a clock frequency *f*, the output voltage (V_{out_IDEAL}) can be expressed as in (3.1).

$$V_{out\_IDEAL} = (N+1).V_{DD} - \frac{N.I_L}{f.C} \tag{3.1}$$

where *N* is the number of stages, V_{DD} is the supply voltage, I_L is the output current, *C* is the charging capacitance per stage, and *f* is the switching frequency of the SC DC-DC converter.

The output voltage of an ideal SC DC-DC converter operating at 25MHz with supply voltage of 3.3V is illustrated in Figure 3.4. The output voltage (V_{out}) increases with the number of stages (*N*) but decreases with the current (I_L) drawn from the converter. The bigger size of the charging capacitor (*C*) exhibits a higher load driving capability which is able to draw more current without significantly degrading the output voltage of the converter. Capacitors are the components which consume the most design area in CMOS technology. For the 0.35µm *AMS* technology, the density of the capacitance in an HV environment is at least three times less than the capacitance in an LV environment. For instance, the densities of the HV capacitances are 0.127fF/µm^2 in CPM structure (POLY1-MET1-MET2-MET3) and 0.246fF/µm^2 in CWPM structure (DNTUB-MET1-MET2-MET3) [103]. On the contrary, the density of the LV capacitance is 0.86fF/µm^2 in CPOLY structure (POLY1-POLY2) [103]. In other words, the area of the converter for an HV is significantly larger than an LV design. Since the SC converter requires a very low output current in actuating RF MEMS, small charging capacitors are used, resulting in significantly reduce die area.

For the SC converter with a linear conversion ratio, which exhibits a similar charge multiplier coefficient at each stage, equal size of charging capacitors are used in every stage. Capacitance optimisation, as in previous research work [45, 97, 112], is not suitable for this

linear conversion ratio SC converter. By having an equal charging capacitor in every stage, the driving capability for a defined amount of capacitance is made optimum [42].

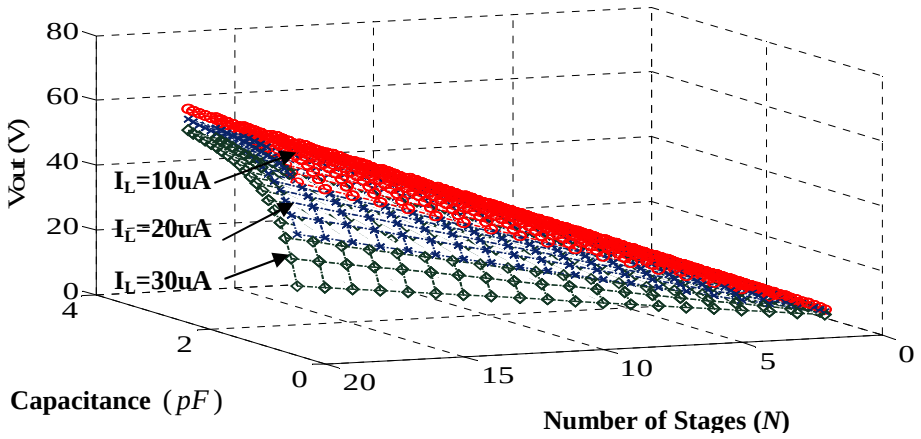


Figure 3.4: Output voltage of an ideal SC converter (without loss) operating at 25MHz for up to 20 number of stages (*N*), and three different output currents (I_L)

3.5.2 Power Consumption

Power consumption is critical in mobile devices. Thus, it is highly desirable to reduce the power consumption in the SC DC-DC converter. The power consumption of the converter can be determined by (3.2). Since V_{DD} is fixed, the input current, I_{power}, is the parameter to be minimised.

$$P_{power} = I_{power} . V_{DD} \tag{3.2}$$

where I_{power} is the average input current and V_{DD} is the voltage supply

In a steady state, the SC converter has a current consumption (ΔI_{steady_state}) which depends on the amount of the output current (I_L) and the number of stages (N) as shown by the first term in (3.3) [42]. In a dynamic state, the current consumption ($\Delta I_{Dynamic\_state}$) depends on frequency, N and parasitic capacitance (C_P), as shown by the second term in (3.3). More analysis of C_P will be presented in the Section 3.5.3.

$$\begin{aligned} I_{power} &= \Delta I_{steady\_state} + \Delta I_{Dynamic\_state} \\ I_{power} &= (N+1).I_L + N.C_P.f.V_{DD} \end{aligned} \tag{3.3}$$

where I_{power} is the average input current, ΔI_{steady_state} is the steady state current consumption, and $\Delta I_{Dynamic\_state}$ is the dynamic current consumption

3.5.3 SC DC-DC Converter with Losses

The performance of the SC DC-DC converter is degraded by the parasitic effects of the transistors and the charging capacitor. The parasitic effects include the non-ideality in the charging capacitors (C_P) and the threshold voltage (V_{TH}) in MOS transistors as given by (3.4) [38]. The losses due to C_P result by a factor of α from its bottom plate, and β from its top plate of charging capacitors [42]. The factor α is generally more than one order of magnitude higher than that of the factor β, so focus will be on α. The parameter α is technology dependent and varies between 0.1 in capacitors for LV applications and 0.4 for HV applications [98]. Techniques to minimise the effects of these parasitic losses will be presented in Section 3.6.

$$V_{out} = [(\frac{N.C}{C+C_P}) + 1].V_{DD} - (N+1).V_{TH} - \frac{N.I_L}{(C+C_P).f} \tag{3.4}$$

where N is the number of stages, V_{DD} is the power supply, I_L is the output current, V_{TH} is the threshold voltage of the switches, and f is the switching frequency of the SC DC-DC converter

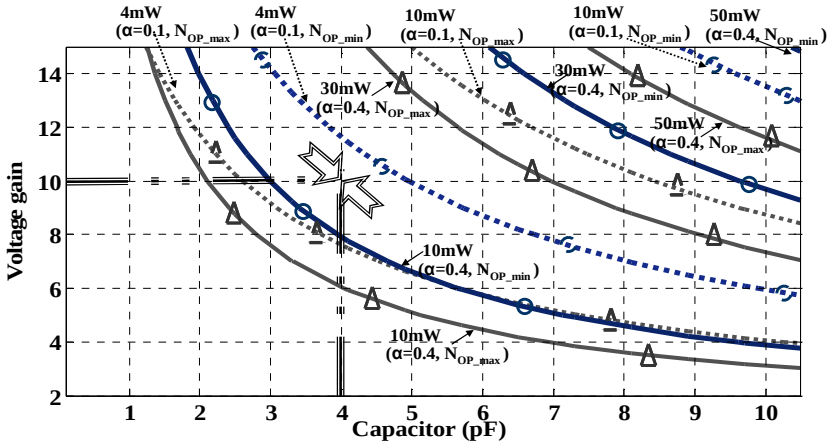
3.5.4 Optimisation of the Design Parameters

As shown by (3.3), the parameter N plays a significant role in optimising the power consumption. The power consumption can be reduced by optimising the number of stages based on derivation from output current (I_L). By minimising I_L, the optimum number of stages (N_{OP}) can be derived as given by (3.5) [42]. For an SC converter with maximised I_L (3.6) [40], significantly higher power is consumed for a similar voltage gain compared to (3.5)[42], as shown in Figure 3.5(a). The difference in power consumption at higher voltage gains is considerable. Higher degree of non-ideality in the HV capacitor shows higher power consumption compared to the LV capacitor which has a smaller α parameter. For instance,

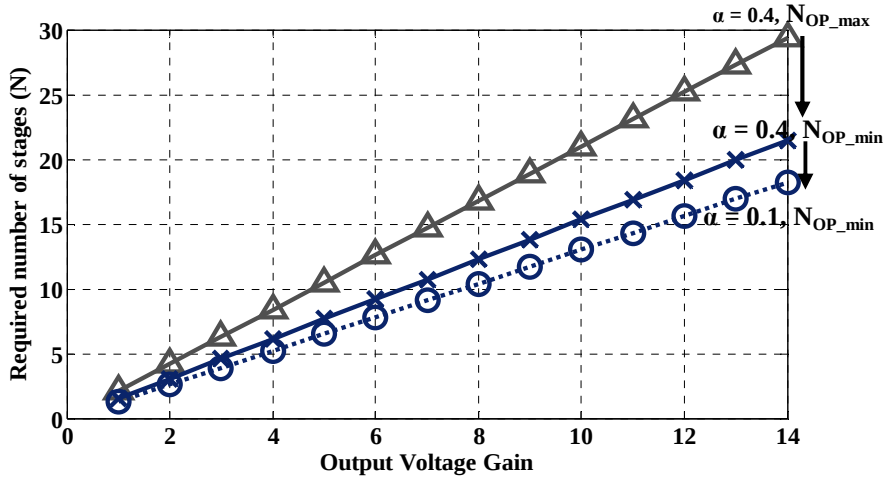
for a voltage gain of 10 using 4pF per stage, the SC converter consumes more than 10mW compared to 3mW by having α = 0.4 and α = 0.1 respectively.

$$N_{op\_\min} = (1+\sqrt{\frac{\alpha}{1+\alpha}}).(\frac{V_{out}}{V_{DD}}-1) \tag{3.5}$$

$$N_{op\_\max} = 2.(1+\beta).(\frac{V_{out}}{V_{DD}}-1) \tag{3.6}$$



(a)



(b)

Figure 3.5: Comparison of power consumption and voltage gain by minimising I_L (O) and maximising I_L (Δ) design (a) Power consumption of an SC converter with parasitic capacitance losses of α = 0.1 (dotted line) and α = 0.4 (solid line) and β = 0.05, threshold voltage V_{TH} = 0.7V (b) Required number of stages based on different voltage gains

Figure 3.5(b) shows the required number of stages for a particular voltage gain given by (3.5) and (3.6). For a particular voltage gain, the SC converter with α = 0.4 and β = 0.05 for maximising the I_L, requires 37% more stages compared to the SC converter for minimizing the I_L. Besides that, by having a lower α, the required number of stages for a particular voltage gain can be further reduced, as shown in Fig. 6(b). To reduce the effect of non-ideality in HV capacitors, a charge recycling technique which significantly improves the power consumption of the SC converter will be presented in Section 3.6.2.

3.5.5 Design Example

To better understand the use of the analysis presented, consider an SC converter for generating a 30V voltage with a very small output current of 10μA and an input voltage of 3.3V. Assuming parameter α = 0.4, the optimum number of stages is obtained as being 13, given by (3.5). Based on (3.6), the required number of stages increases to 17 if more output current is needed. There is a trade-off for the selection of the switching frequency. Smaller charging capacitors can be used for a higher switching frequency. However, a higher switching frequency will increase unwanted RF noise to the system. For a switching frequency of 25MHz, the charging capacitor per stage is about 0.32pF based on (3.1). Equation (3.4) is rewritten versus N_{OP} as given by (3.7). The loss in transistors that was neglected in the derivation of (3.5) in [18] has now been considered by (3.7) for more accurately predicting the output performance of the SC converter. A similar or slightly lower output voltage that defined in (3.5) will be obtained by (3.7) by having a negligible loss from the transistors.

$$V_{out} = (N_{OP} + 1).V_{DD} - (N_{OP} + 1).V_{TH} - \frac{N_{OP}.I_L}{C.f} \tag{3.7}$$

Based on the presented analysis, the design area of the SC converter for high voltage gain and power efficiency in a small size has been identified and developed as shown in Figure 3.6. In summary, the number of stages of the SC converter depends on the required voltage gain and the technological parameter α, which gives the degree of non-ideality of the capacitor for a given technology. The size of charging capacitors is independent of the number of stages, but it depends on the required current capability of the converter. For an SC converter targeted at RF MEMS applications, a smaller charging capacitor, e.g. 1pF rather than 5pF, can be used without affecting the output voltage, as shown in Figure 3.6.

The presented analysis and synthesis on the SC converter enable the design of a high voltage gain and low power consumption CMOS controller for RF MEMS switches in a small die area.

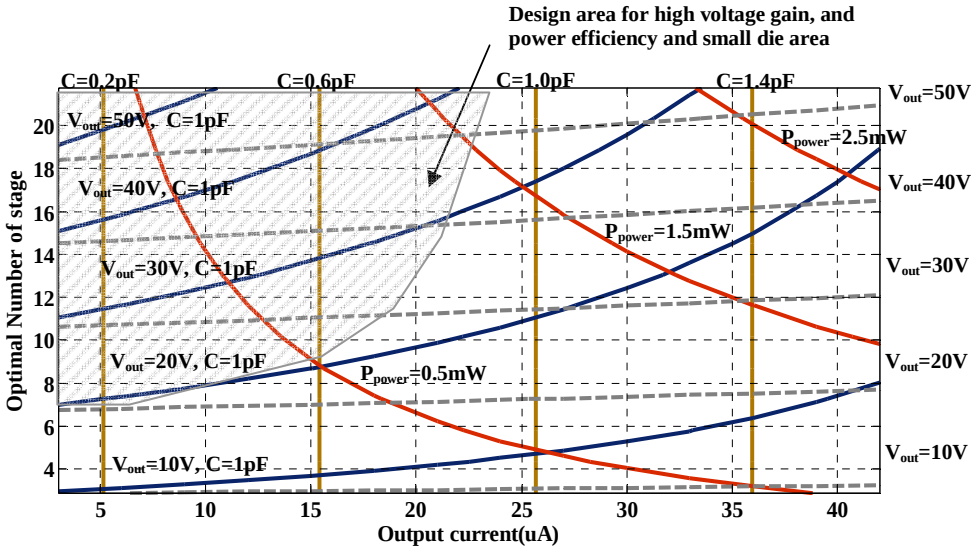


Figure 3.6: Design area of an SC DC-DC converter with an operating frequency of f = 25 MHz, with the assumption that parasitic capacitance loss of α =0.4, and a constant threshold voltage of 0.7V from the transistors

3.6 Improvement to the Performance of High Voltage SC DC-DC Converter

In this section, two effective techniques are proposed in order to improve the performance of the HV SC DC-DC converter in terms of voltage gain efficiency and power consumption.

3.6.1 Improving the Voltage Gain Efficiency

3.6.1.1 Reducing the Threshold Voltage of the Transistors

Improvement of the voltage gain efficiency of the SC DC-DC converter can be achieved by using LV transistors as charge transfer switches. The maximum technology allowable for source-bulk potential (V_{SB_MAX}) or drain-bulk potential (V_{DB_MAX}) in an LV transistor is less than 5V. Thus, the adaptive biasing circuits as presented in previous section are required to maintain the V_{SB} and V_{DB} within the limit. For HV transistors (thin and thick gate oxide HV

models), the V_{SB_MAX} or the V_{DB_MAX} is 50V. The bulk of the HV transistors can directly be connected to the highest node of the converter, which is the V_{out} in this case, without the need of the adaptive biasing circuits. Although a simpler circuit can be obtained by using the HV transistors, the bulk effect due to the increment of V_{SB} as shown by (3.8) [104] can no longer be ignored in this case. This bulk effect will seriously diminish the output voltage of the SC converter. Thus, a lower boosted voltage is obtained by using HV transistors. The performance of the SC converter is poorer when using the thick oxide compared to the thin oxide HV transistors with reduced current drive in the transistors. The effect of thin and thick HV transistors on the performance of the SC converter will be verified in Section 3.7.

$$V_{TH} = V_{TH0} + \gamma.(\sqrt{|V_{SB} + 2\phi_F|} - \sqrt{|2\phi_F|}) \tag{3.8}$$

where V_{SB} is the source-bulk potential, V_{TH0} is the V_{TH} with zero V_{SB} and $2\phi_F$ is the surface potential. $\gamma = (t_{ox}/\varepsilon_{ox})\sqrt{2q\varepsilon_{si}N_A}$ is the body effect parameter, t_{ox} is gate oxide thickness, ε_{ox} is oxide permittivity, ε_{si} is the permittivity of silicon, N_A is a doping concentration, q is the charge of an electron.

3.6.1.2 Increasing the Transconductance of the Transistors

The transconductance (g_m) of the transistors is proportional to the effective gate-to-source voltage (V_{GS_EFF}) as shown in (3.9). Hence, high voltage gain efficiency has dictated the use of high V_{GS_EFF}. The V_{GS_EFF} is decreasing over the stages in the SC converter. This is especially obvious if using linear MOS diode-connected structure [38, 42, 113]. Weak V_{GS_EFF} causes the transistors not able to be turned on fully, thus a higher on-resistance in the transistors and eventually a smaller charge will pass to the next stage. The interleave structure of the SC converter constantly provides a high V_{GS_EFF} over stages. This is crucial for designing the SC converter with a large number of stages for a high voltage gain.

$$g_m = \partial(\frac{I_D}{V_{GS}}) = \frac{W}{L}\mu_n\frac{K_{ox}\varepsilon_0}{t_{ox}}(V_{GS} - V_{TH}) = \frac{W}{L}\mu_n\frac{K_{ox}\varepsilon_0}{t_{ox}}V_{GS\_EFF} \tag{3.9}$$

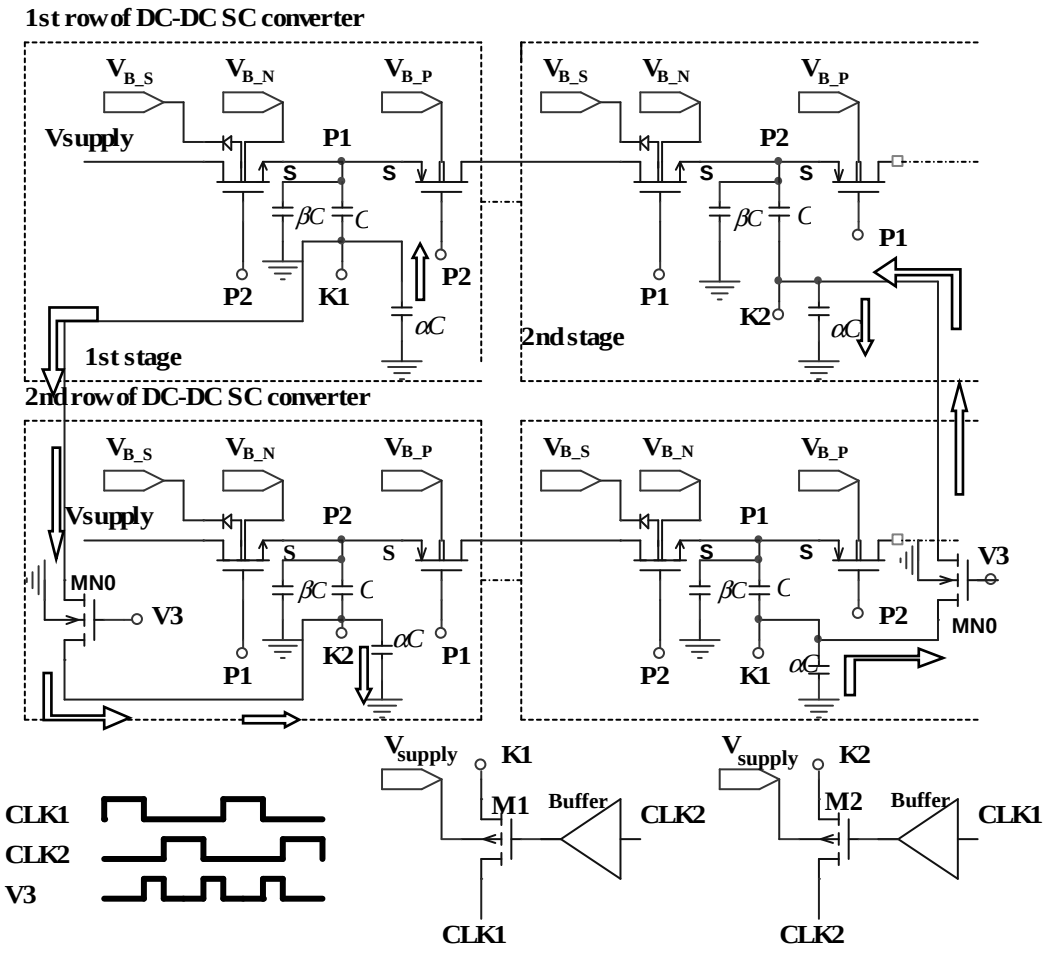
where I_D is the DC drain current, V_{GS_EFF} is the effective gate-to-source voltage, which is the difference between gate-to-source voltage and the threshold voltage (i.e. $V_{GS} - V_{TH}$), K_{ox} is the relative permittivity of silicon dioxide and t_{ox} is the thickness of the gate oxide, ε_o is permittivity of free space (equal to 8.854 X 10^{-12} F/m), W/L is the width and length ratio of the transistor and μ_n is the mobility of electrons near the silicon surface.

3.6.2 Reducing the Power Consumption in Parasitic Capacitance

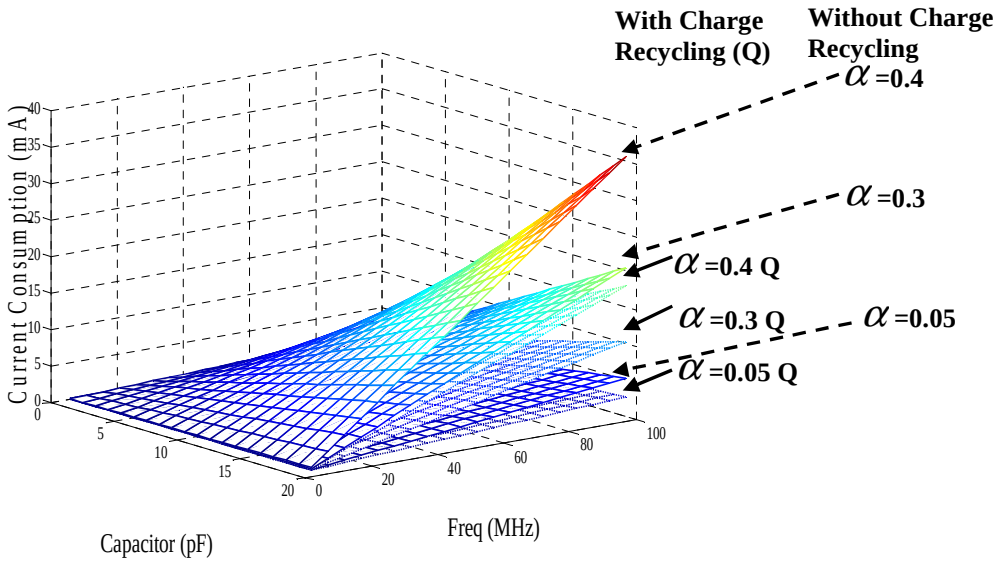
Charge recycling technique shows a significant improvement on the current consumption of the SC DC-DC converter with low output current [114]. This technique is suitable for the CMOS controller for RF MEMS switch which has low loading characteristic. The non-ideality in the integrated-circuit capacitor is high in the current state of art CMOS technology especially for HV capacitors. The parasitic parameter (α) can be up to 0.4 in an HV capacitor for the technology considered [98]. A charge recycling circuit is designed for this HV SC converter as presented in Figure 3.7(a). An nMOS (MN0) is used as a switch to connect the parasitic capacitance between the first and second rows of the SC converter in every stage. The MN0 only operates at a very short period (V3) as shown in Figure 3.7(a). Exceeding the defined period of V3 leads to a leakage of the current to ground through the MN0 and eventually more current is drawn from the input supply. The V3 signal is developed through a NOR gate connected between CLK1 and CLK2 to ensure the non-overlap among these signals. For the clocking circuitries (CLK1 and CLK2), PMOS transistors (M1 and M2) are used before the charging capacitors (C). As CLK1 is high and CLK2 is low, M1 is switched on and M2 is switched off. The charging capacitor and also the parasitic capacitance (αC) in the SC converter are charged to VDD by CLK1. As both M1 and M2 are switched off, the charges trapped in the parasitic capacitance by CLK1 in the 1st row of the converter are recycled through MN0 to the parasitic capacitance in the 2nd row of the converter at CLK2. This equalises the potential at both parasitic capacitances to VDD/2 before CLK2 goes high. Thus, the amount of charge drawn from the power supply for charging the parasitic capacitances is half the amount needed compared to without the charge recycling circuit. Ideally, this technique reduces the dynamic current consumption ($\Delta I_{Dynamic\_state}$) to half, as by (3.10) which is rewritten from (3.3). Figure 3.7(b) demonstrates the effect of the charge recycling technique on the current consumption of the SC converter.

$$I_{power_Q} = \Delta I_{steady\_state} + \frac{\Delta I_{Dynamic\_state}}{2} = (N+1).I_L + \frac{N.C_P.f.V_{DD}}{2} \tag{3.10}$$

where N is the number of stages, V_{DD} is the power supply, I_L is the output current, C and C_P ($C_P = \alpha C$) are the charging and parasitic capacitance per stage, V_{TH} is the threshold voltage of the transistors, and *f* is the switching frequency



(a)



(b)

Figure 3.7: Charge recycling technique in the SC DC-DC converter (a) circuit diagram for the implementation (b) Comparison of the current consumption with and without the charge recycling technique

3.7 Verification of the Improved Performance High Voltage SC DC-DC Converter

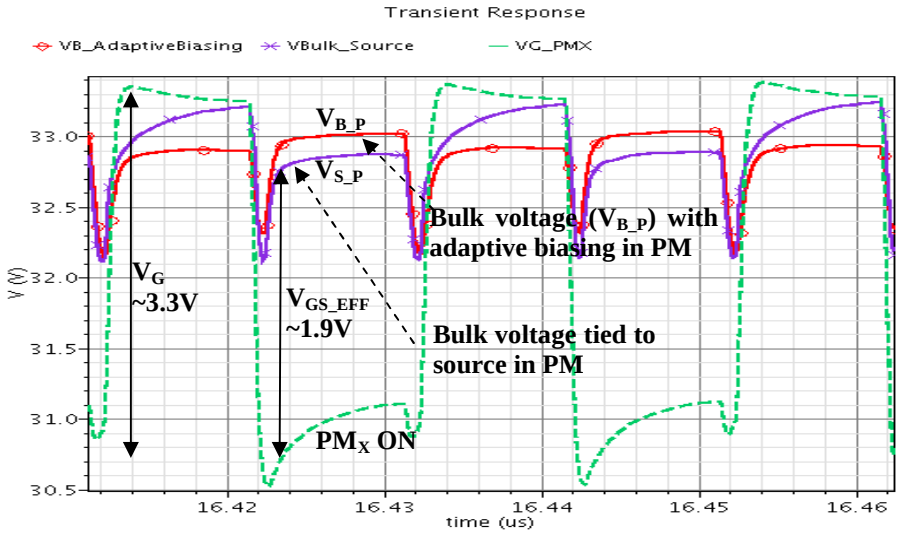
To demonstrate the effectiveness of the proposed design techniques, the HV SC DC-DC converter with a 15-stage, as presented in Figure 3.1, is simulated in the 0.35μm *AMS* technology. A V_{DD} of 3.3V was supplied to the converter. The width of the pMOS transistors was set to the ratio of 2.5 to the width of the nMOS transistors in the SC converter. Since a high output voltage of 40V with a low output current are required, the charging capacitor (*C*) was set to 0.467pF per stage per capacitor according to (3.5) and (3.1). Non-overlapping clock signals, CLK1 and CLK2, were generated for switching the converter to avoid charge leakage from short circuit paths. A floating 3.3V LV transistor model, as presented in Section 3.4.1, was chosen for the SC converter. The technology allowable voltage limit (V_{GS_MAX} and V_{DS_MAX}) of the transistors is 5V.

In this simulation, the effectiveness of the proposed adaptive biasing circuit for the inter- and the final stages in the interleave structure of the SC DC-DC converter are demonstrated. The interleave structure of the SC converter provides a constantly effective V_{GS_EFF} for switching on and off the transistors (PM and NM) as shown in Figure 3.8(a) and (b). The V_{GS_EFF} is within the technology voltage limit of the transistor (< 5V). Thus, there is no HV overstress on the gate oxide of the devices. This V_{GS_EFF} is crucial in the SC converter with a large number of stages.

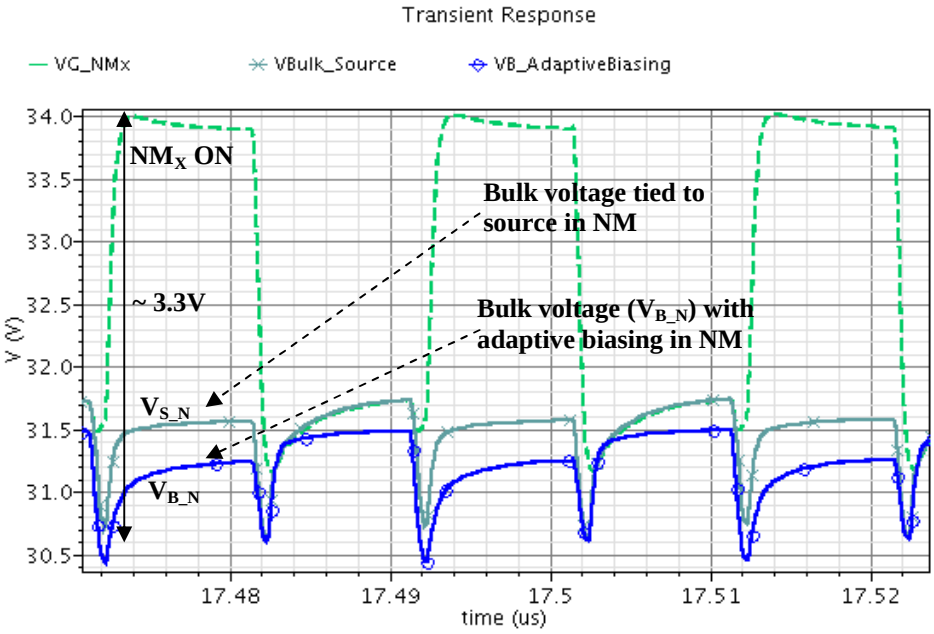
Through the inter- stage adaptive biasing circuit, the bulk of the PM (V_{B_P}) is always higher than its source (V_{S_P}) as shown in Figure 3.8(a). This eliminates the leakage current to the substrate as shown in Figure 3.9(a). Similarly, the bulk of the NM with adaptive biasing (V_{B_N}) is always lower than its source (V_{S_N}) as shown in Figure 3.8(b). Figure 3.9(b) compares the leakage current in the transistors with and without using the adaptive bulk biasing. A very high current peak is flowing to the substrate through the parasitic vertical bipolar in the transistor which without using the adaptive bulk biasing circuit.

Figure 3.10(a) shows the voltages at the output stage of the SC DC-DC converter. The bulks of the pMOS (V_{B_F}) from two rows of the SC converter are biased at the highest potentials using the proposed final stage adaptive biasing circuit compared to their sources (*P1* and *P2*) and the drain i.e. V_{out} in this case as shown in Figure 3.10. Hence, there is no

leakage current in the NM and the PM at the final stage when driving a variable capacitive MEMS load. This eliminates the SC converter from latch-up.

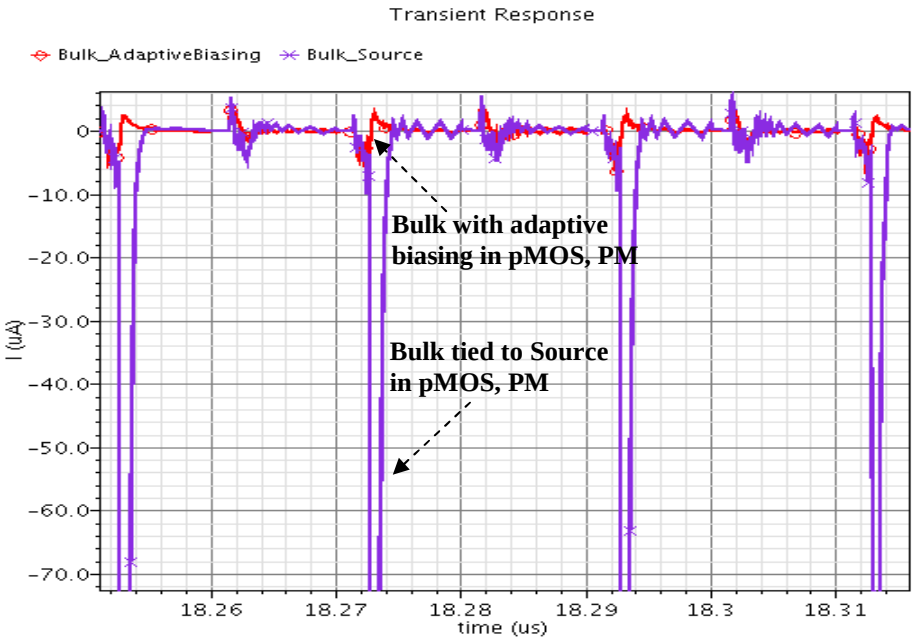


(a)

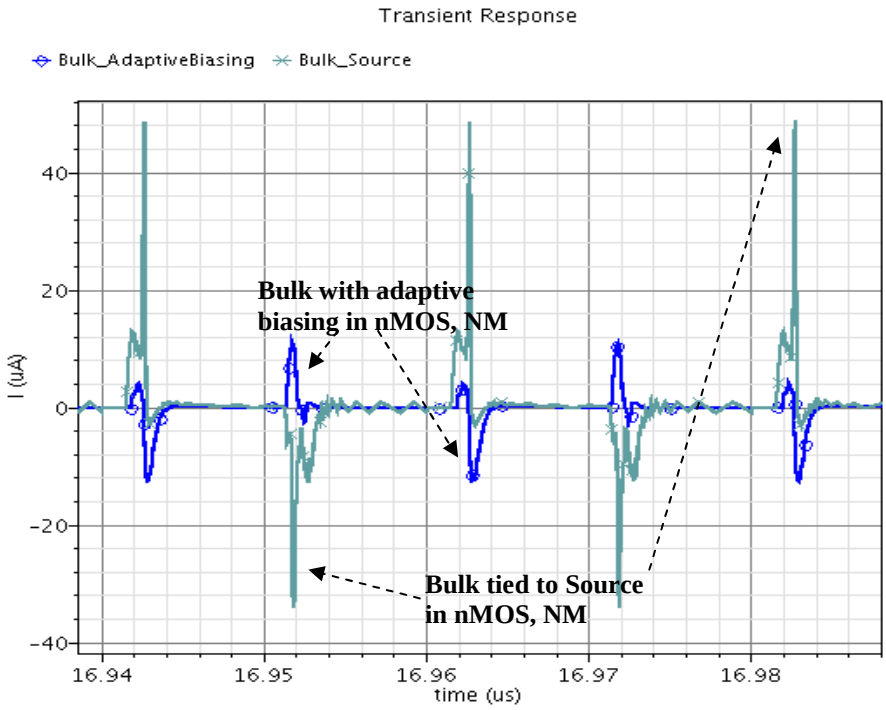


(b)

Figure 3.8: Simulation results of the proposed SC DC-DC converter show (a) bulk voltage in PM (V_{B_P}) that uses the inter stage adaptive biasing circuit is always higher than its source to switch off the vertical parasitic bipolar in PM, (b) bulk voltage in NM (V_{B_N}) that uses the inter stage adaptive biasing circuit is always lower than its source to switch off the vertical parasitic bipolar in NM



(a)



(b)

Figure 3.9: Simulation results of the proposed SC DC-DC converter show (a) no leakage current in PM that uses the adaptive biasing circuit compared to the PM's bulk tied to its source (which have very high current peaks flowing to the substrate) and, (b) no leakage current in NM that uses the adaptive biasing circuit compared to the NM's bulk tied to its source (which have very high current peaks flowing to the substrate)

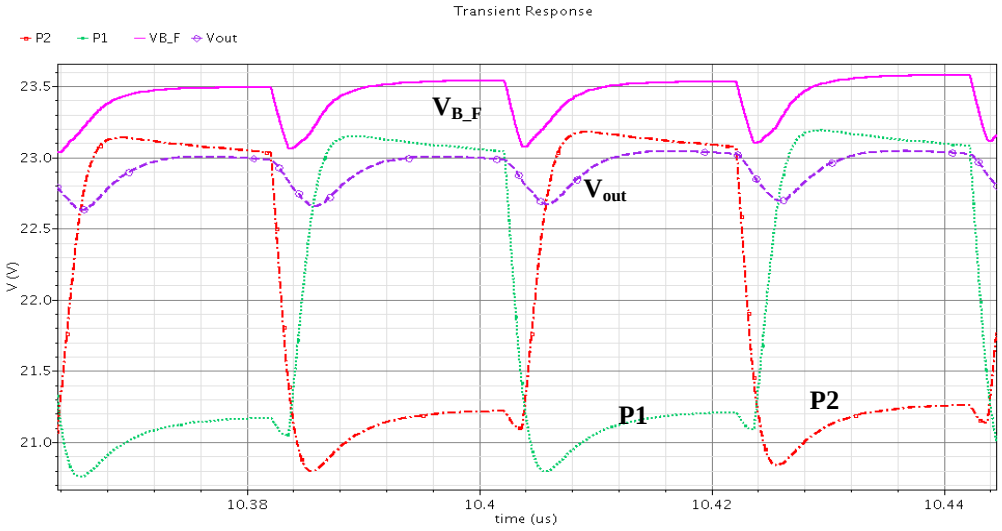


Figure 3.10: Bulk voltage at the output stage (V_{B_F}) of the proposed SC DC-DC converter that uses the final stage adaptive biasing circuit is always higher than the output voltage, *P1* and *P2* to prevent the converter from latch-up

Figure 3.11 shows the output voltage ripple from the post layout simulation of the converter. By complementing the voltage waveforms from the 1st and the 2nd rows of the interleave structure of the SC converter, the ripple at the output node is reduced significantly from V_{DD} to about 0.5V.

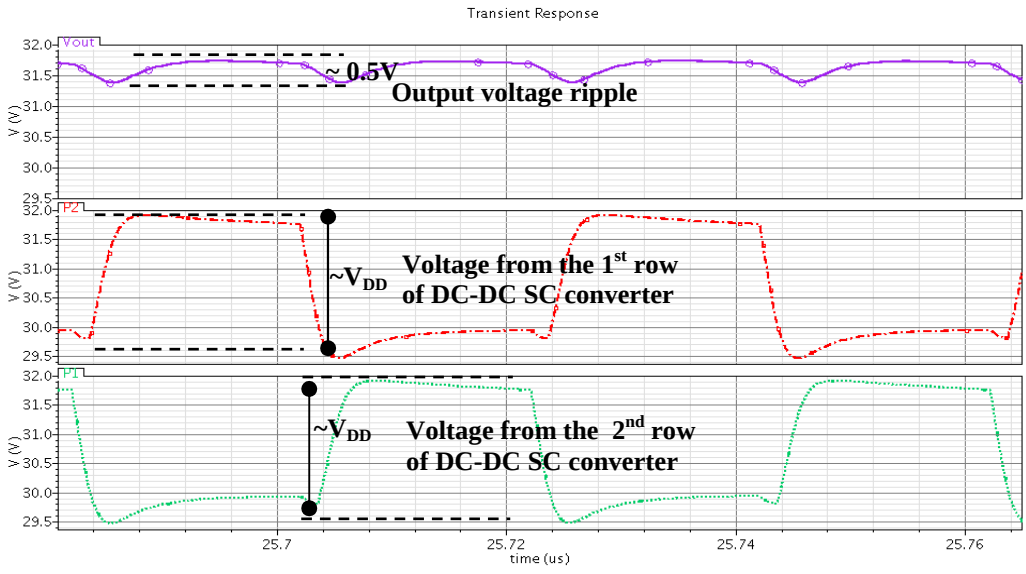
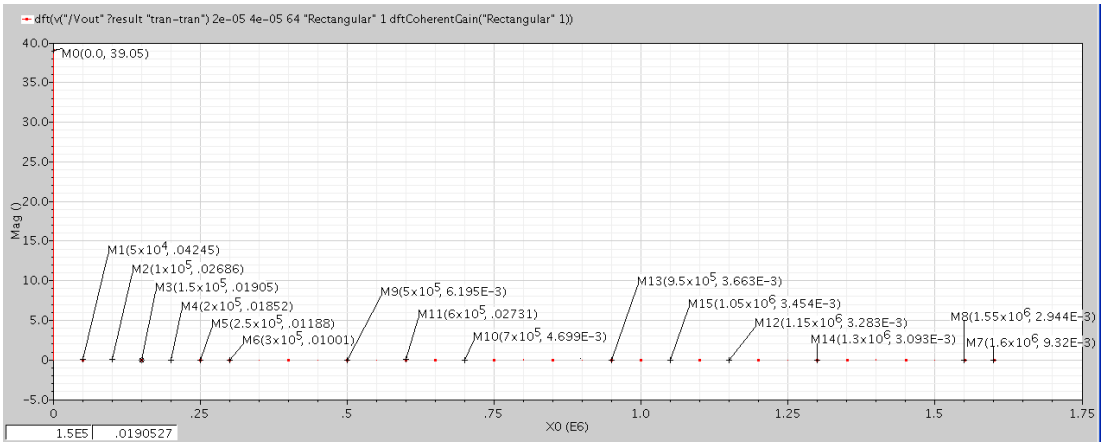
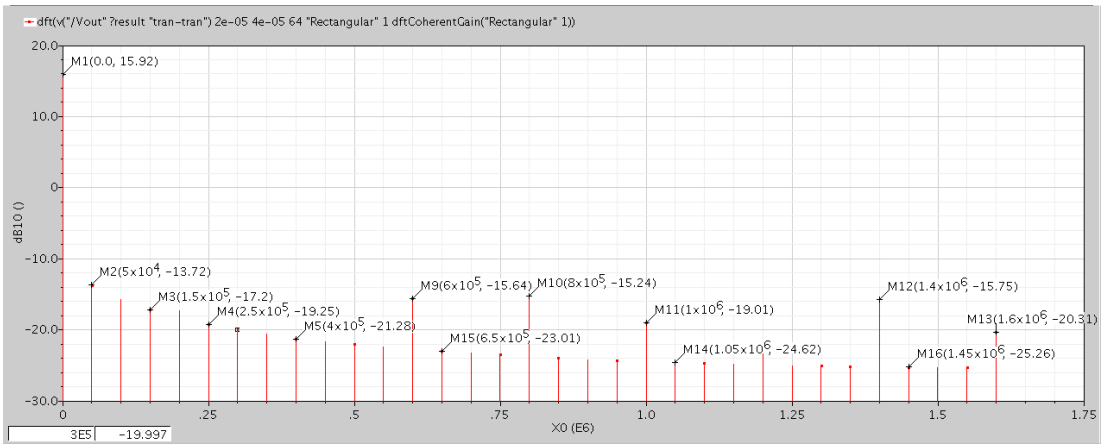


Figure 3.11: The SC converter achieves small ripples at the output voltage through complementing the internal node voltages from the 1st and the 2nd rows of the SC DC-DC converter

Figure 3.12(a) and (b) show the output voltage ripple and its harmonic in the form of voltage magnitude and power respectively. The first harmonic happens at 0.05MHz with -13.72dB or 0.042V over the DC component 39.05V. This shows the effectiveness of the proposed techniques that successfully suppress the interference to a low level.



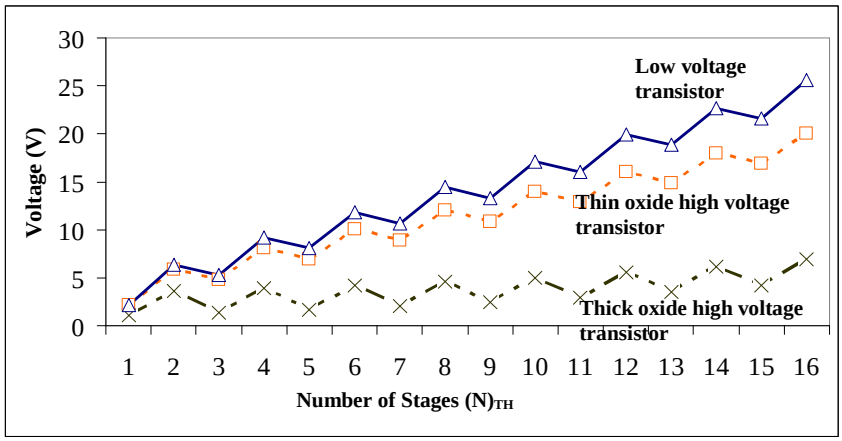
(a)



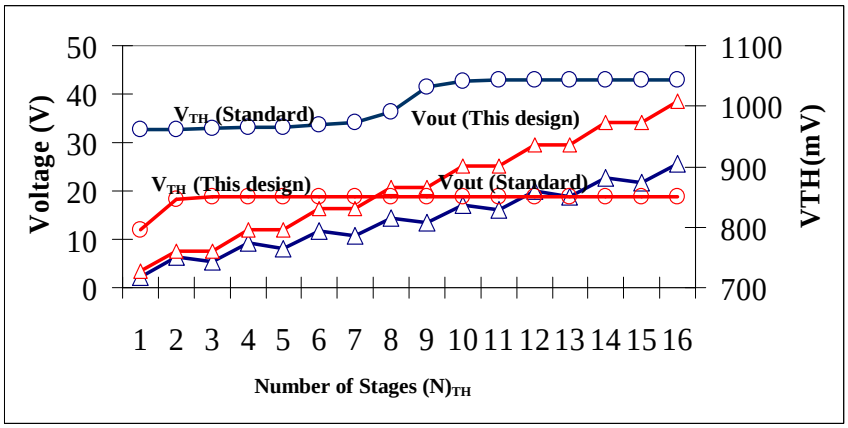
(b)

Figure 3.12: The output voltage ripple and its harmonic in (a) magnitude and (b) dB10

The improvement to the voltage gain of the SC DC-DC converter using LV transistors compared to HV transistors is demonstrated in Figure 3.13(a). More than 25% of boosted voltage is obtained by using the LV transistors compared to the HV transistors based on same number of stages. The voltage gain of the SC converter is worse by using the thick gate oxide HV transistors. This is due to the reduced transconductance in the thick gate oxide HV transistors compared to the thin gate oxide HV transistors. The curves in Figure 3.13(a) are not monotonic functions of N unlike (3.1) due to charging and discharging processes in the SC converter. For instance, while the even stages of the SC converter are charging, the odd stages are discharging. Thus, relatively higher voltages are obtained in the even stages, as shown in Figure 3.13(a). The differences of voltages between stages are less than 5V which complied with the technology allowable voltage limit.



(a)



(b)

Figure 3.13: Simulation results of the SC DC-DC converter with improved voltage gain through (a) LV transistors and (b) low V_{TH} in transistors

Figure 3.13(b) shows the improvement to the voltage gain through reducing the V_{TH} in the transistors. V_{TH0} is a device parameter with zero V_{SB}. Increasing of V_{SB} in standard MOS diode-connected converter over stages affects the V_{TH} as described by (3.8). Higher V_{TH} in the transistors reduces the voltage gain of the standard MOS diode-connected converter as shown in Figure 3.13(b). A nearly constant V_{TH} is achieved by the SC converter with adaptive biasing circuit. Moreover, the interleave structure of the SC converter provides an effective V_{GS_EFF}, thus demonstrates a higher output voltage in the transistors as shown in Figure 3.13(b).

Improvement to the power consumption of the SC DC-DC converter through the charge recycling technique is presented in Figure 3.14. The charge was recycled between the bottom plate of parasitic capacitors through an nMOS (MN0) as described in Figure 3.7(a). The MN0 operates at a small period of non-overlapping regions of *CLK1* and *CLK2*. A 400 μA of current is recycled between the parasitic capacitors, thus reducing the current drawn from the input supply (I_{power}) as shown in Figure 3.14. The saving of the current is slightly less than 50% (in ideal case) due to the losses in the additional gate and current leakage during the circuit operation.

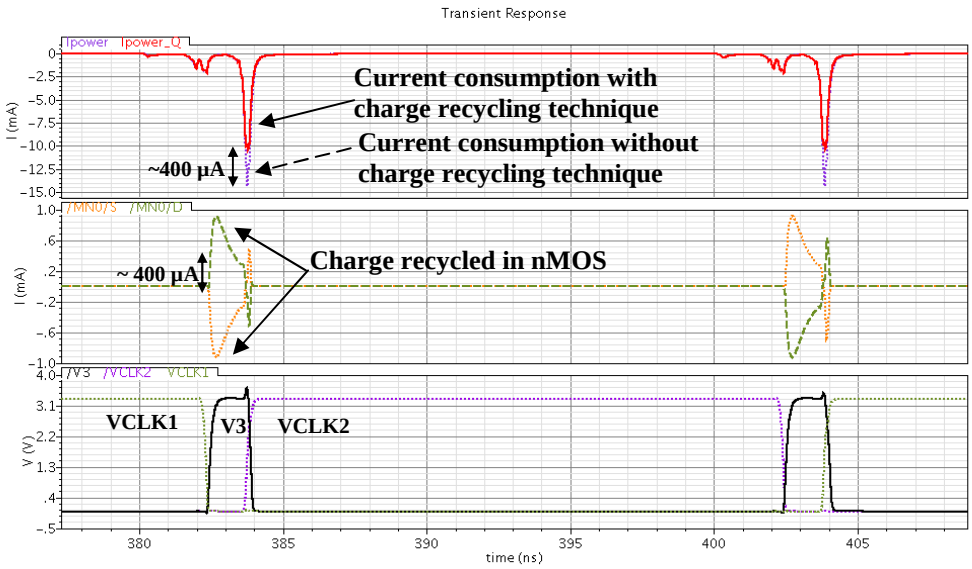
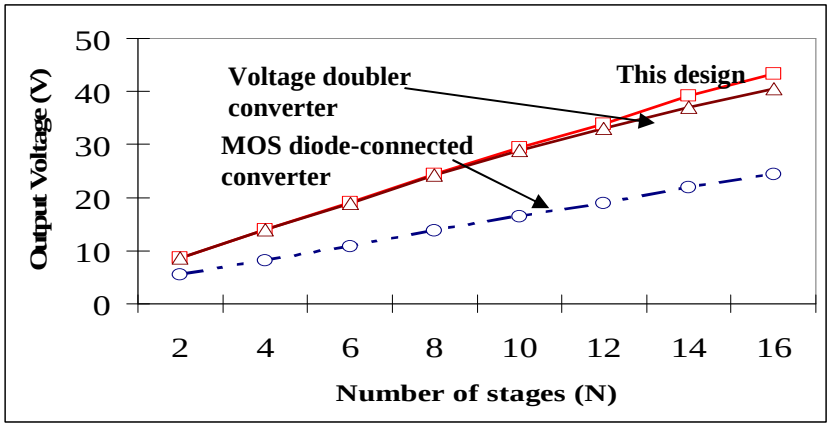
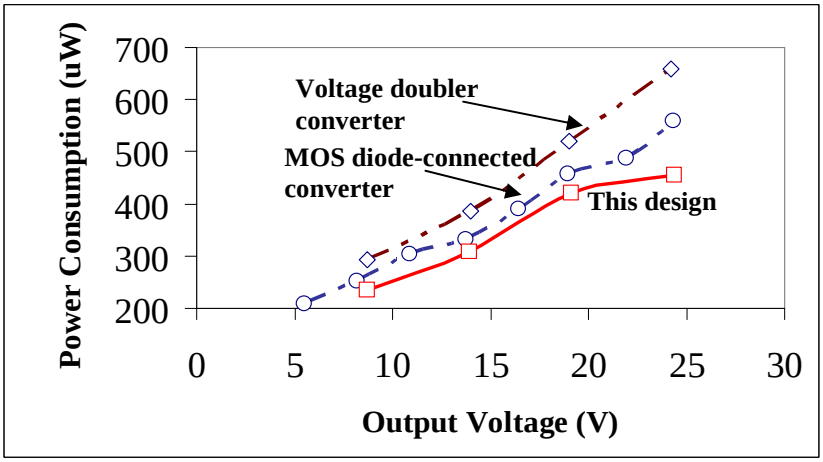


Figure 3.14: Charges in parasitic capacitors are recycled to reduce the current consumption, I_{power} through an optimized nMOS, MN0 operating at period of V3

Figure 3.15(a) and (b) show the performance of the improved HV SC DC-DC converter in this design compared to other converter's topologies. By reducing the V_{TH} and increasing transconductance of the transistors through the adaptive biasing circuits and the effective V_{GS_EFF},, the SC converter shows a higher magnitude of output voltage compared to the standard MOS diode-connected converter and the voltage doubler converter, as shown in Figure 3.15(a). The power consumption is also significantly reduced compared to the other two topologies, by eliminating the leakage current and introducing the charge recycling circuit, as shown in Figure 3.15(b).



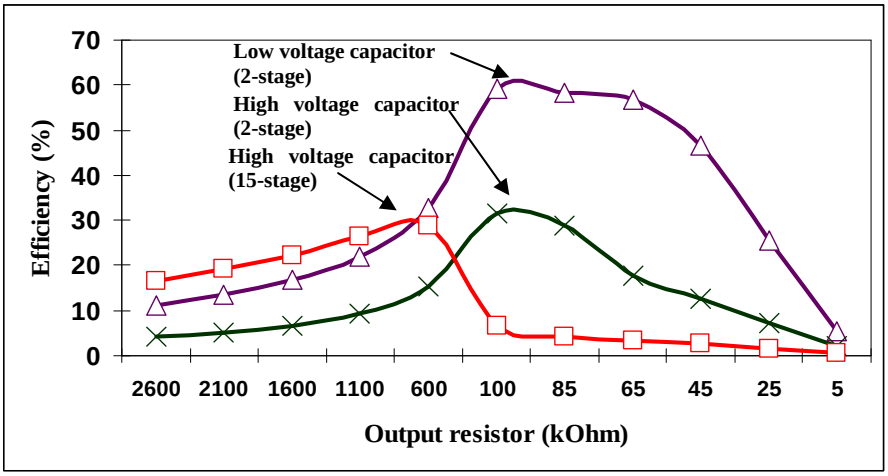
(a)



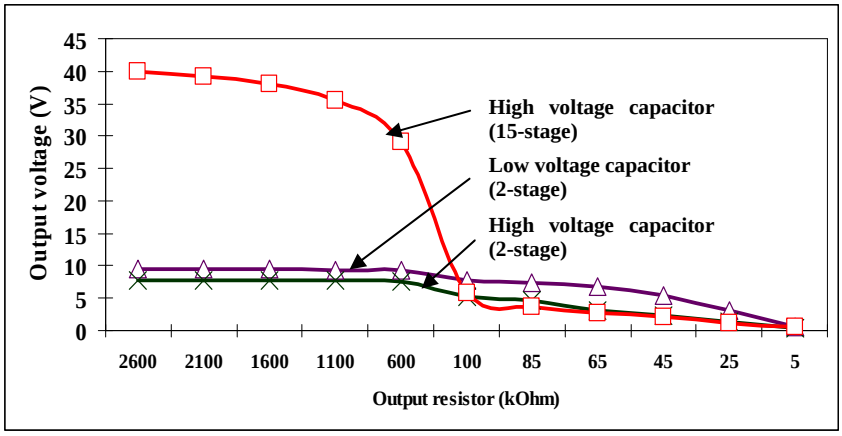
(b)

Figure 3.15: Simulation results of the improved HV SC DC-DC converter compared with the standard MOS diode-connected converter and the voltage doubler converter, with 0.935pF per stage at 25MHz, in terms of a) output voltage and b) power consumption

The power efficiency (η) of the improved SC DC-DC converter is presented in Figure 3.16(a). Figure 3.16 (b) shows the output voltage of the SC converter based on different charging capacitors' technologies. The SC converter is customised for RF MEMS applications with high output voltage and low output current, thus a large output resistor was used in these simulations. The maximum efficiency of a two-stage SC converter is up to 60% by using LV capacitors (CPOLY) and reduces nearly to half by using HV capacitors (CWPM). Generally, the efficiency will be significantly reduced by having higher stages as demonstrated in previous research works [42, 47]. In this work, by using presented design strategies, the maximum efficiency of the converter for a 15-stage is only slightly reduced compared to a 2-stage converter.



(a)



(b)

Figure 3.16: A 2-stage and a 15-stage SC DC-DC converters using HV capacitors compare with a 2-stage SC converter using LV capacitors in terms of (a) efficiency and (b) output voltage

3.8 Implementations

3.8.1 Layout of Floating Low Voltage Transistors

The layout for an HV design using CMOS technology is complex and not as straightforward as for an LV design [103]. Figure 3.17 demonstrates the layout of the SC DC-DC converter in a single stage using floating LV transistors (as presented in Section 3.4). The floating LV transistors are surrounded by an isolation layer as shown in Figure 3.17. This isolation layer enables the LV transistors in an HV environment and further enhances the performance of the transistors from the substrate noise. A guard ring is drawn between the HV blocks in the layout of the SC converter. The guard ring collects the electrons emitted from a forward biased junction in the transistors and current noise from the nearby digital circuitry. The guard ring consists of a combination of shallow and deep p-wells, including a p-type diffusion ring with metal contacts. The metal contacts of the guard ring are connected directly to the substrate through a wide piece of metal layer to reduce substrate resistance. The substrate resistance is designed to be as low as possible to avoid parasitic bipolar effects and parasitic field transistors. Through a proper layout drawing, it eliminates latch up in the LV transistors in the HV design and achieves high reliability in the SC converter.

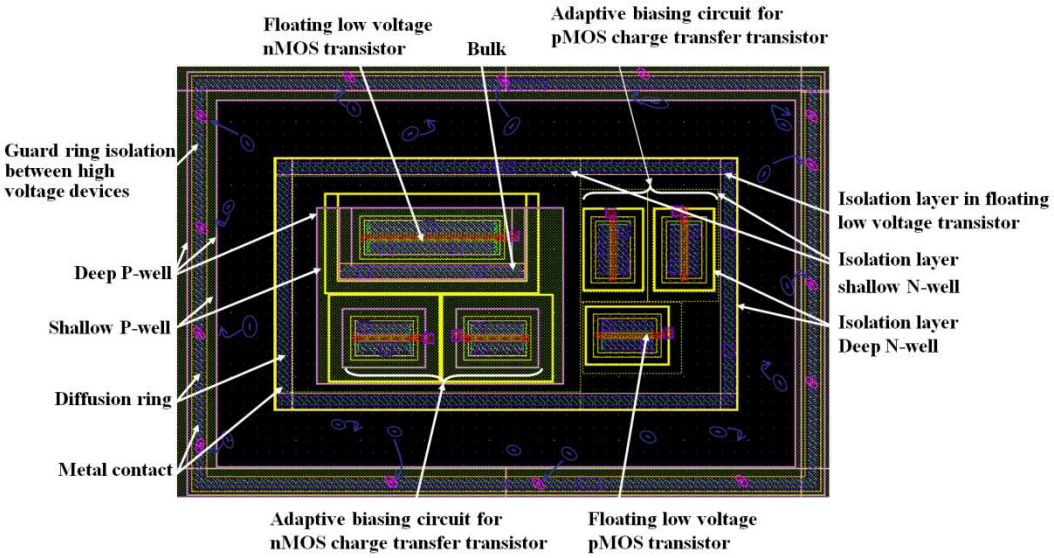


Figure 3.17: Layout of the enhanced interleave structure HV SC DC-DC converter in a single stage

3.8.2 Layout of SC DC-DC Converters

The layouts of the improved HV SC DC-DC converter and standard MOS diode-connected converter, each providing an output voltage of approximately 40V, are shown in Figure 3.18. The MOS diode-connected converter requires a 38% increase in the number of stages compared to the HV SC converter, due to the weak V_{GS_EFF} and low transconductance in the transistors. Thus, the die area is only a 0.2176mm^2, which is 45% smaller than the area of the standard MOS diode-connected converter. Figure 3.18 also shows that HV capacitors dominate the largest areas of the layouts, as identified by our analysis.

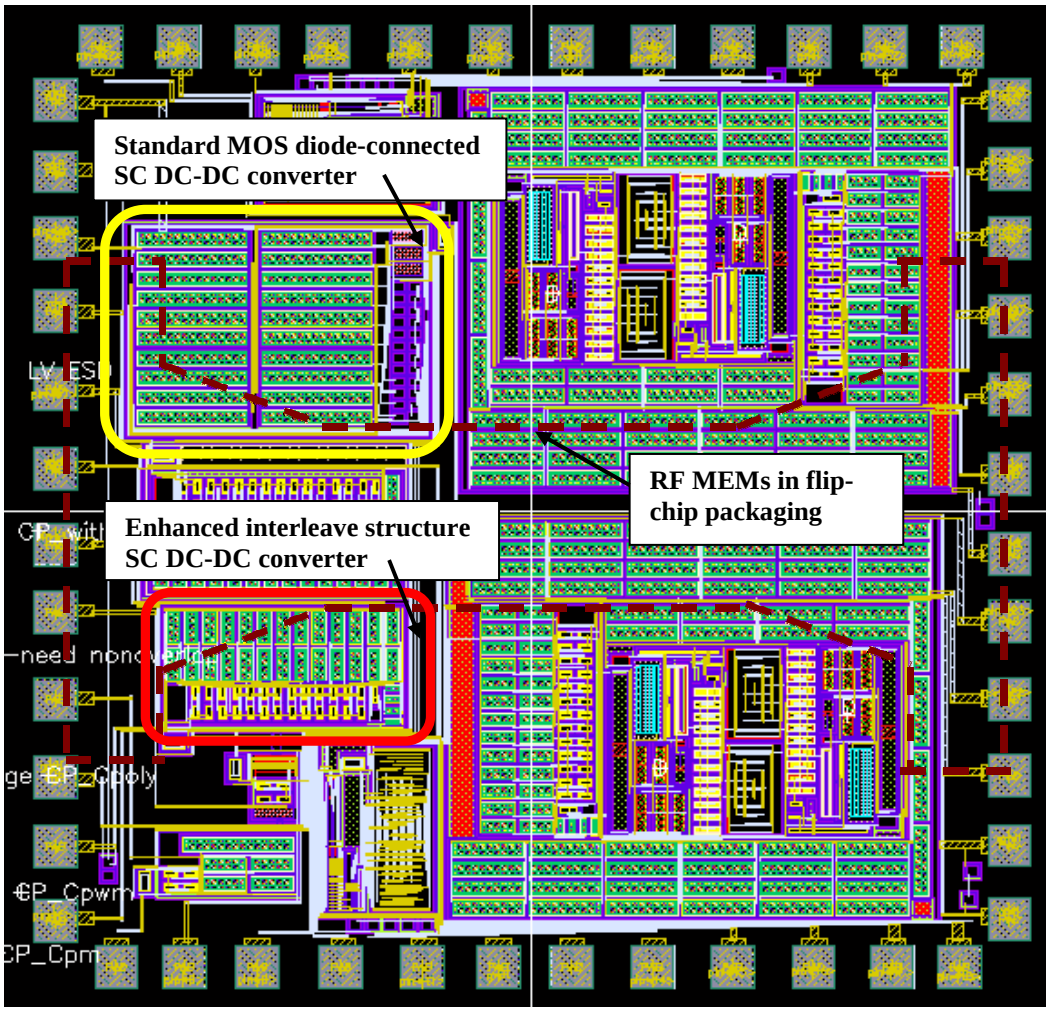


Figure 3.18: Layout of the enhanced interleave structure HV SC DC-DC converter in fabrication ready pad frame (with the effective area of 0.2176 mm^2 surrounded by the red colour line) compares with the standard MOS diode-connected converter that has the effective area of 0.3924mm^2 (surrounded by the yellow colour line)

3.9 Benchmarking

The figures of merit for the improved HV SC DC-DC converter have been compared with a number of other research works in the literature, as tabulated in Table 3.1. The HV SC DC-DC converter shows the lowest power consumption, the highest voltage gain and the least ripple of output voltage, even with a very small output capacitor. Furthermore, the die area in this design is small compared to previous research works. This validates the effectiveness of the proposed design strategies for a high output voltage, low power consumption and a small size CMOS controller for RF MEMS applications.

Table 3.1: Summary of the design parameters and merits of performance on two-phase SC DC-DC converter

Design parameters & merits of performance	**This design**	**[49]**	**[47]**	**[106]**	**[90]**	**[113]**	**[99]**	**[50]**	**[97]**
Technology (µm)	0.35	0.8	0.18	0.35	0.8	0.18	0.7	0.35	0.35
Number of stages	15	4	5	2	16	16	5	4	8
Capacitance per stage (*pF*)	0.936	15	2.5	23	1	5.4	NA	6.67	Reverse Fibonacci sequence (5,3,2,1)*(33x1E3)
Capacitive load (*pF*)	1	30	30	NA	28	27	NA	30	33x1E3
Oscillator frequency (*MHz*)	25	5	100	25	10	75	NA	100	0.01
Voltage gain	14	3.23	5.61	2.42	10	12.33	5.4	4.611	7
Ripple (ΔV/Vout) (%)	0.367	NA	16.4	0.6	0.8	1.1	NA	NA	4.3
Output current (µA)	20	10	350	26	50	14.86	NA	400	NA
Current consumption (µA)	249.3	NA	NA	1600	NA	NA	2800	NA	NA
Effective area (mm^2)	0.2176	NA	NA	0.7888	0.33	0.72	NA	NA	NA
Proposed solutions	1. The HV design is based on an LV interleave structure 2. A small ripple (0.367%) is achieved by using a small output capacitor (1pF) 3. A 15-stage converter is developed for a 40V output voltage 4. LV transistors are used in the HV design for a higher voltage gain 5. Latch up of LV transistors in an HV design is avoided through the proposed adaptive biasing circuits and the HV layout drawing 6. Charge recycling circuit is proposed to reduce the power consumption which is due to the non-ideality in HV capacitors 7. The charging capacitors have been optimised to reduce die area ($0.2176mm^2$) and power consumption (822.6µW)	1. Linear structure was used in an LV operation through the internal boosted voltage 2. A large output capacitor (30pF) was used to reduce the ripple	1. Voltage doubler structure was used to generate large output current through a high frequency 2. A 5-stage converter was developed for a 10V output voltage	1. Interleave structure was used 2. The design was a 2-stage converter for the output of 6.7V and 26µA	1. Voltage doubler structure was used 2. Voltage gain of 10 was achieved through a 16-stage of the converter 3. Two designs were developed based on LV and HV capacitors. The design which used HV capacitors consumed significant die area compared to the design using LV capacitors	1. Linear structure was used 2. A high output voltage (14.8V) was generated by a 1.2V supply through a large number of stages (16) 3. Large output capacitor (27pF) was used to reduce the ripple (1.1%)	1. Hybrid structure was used through cascoding the two linear structures 2. Medium output voltage from the 1st converter was used for pumping the 2nd converter	1. Linear structure was used 2. Positive and negative output voltages were generated through a complex clocking circuit 3. A 4-stage converter was developed for an output voltage of 8V and a large output current of 400µA	1. Fibonacci structure was used 2. Size of capacitors was optimised based on a reverse Fibonacci sequence 3. Large capacitors were used in the design
Applications	RF MEMS	Flash-EEPROM	Flash- EEPROM	Antenna controller	NA	RF MEMS	RF MEMS	Flash memory	RF MEMS

NA- Not available

3.10 Measurement Results

The fabricated SC DC-DC converter using 0.35 µm AMS technology on a die is shown in. The SC DC-DC converter has been verified experimentally. High clock frequency waveform has been generated using ARM Cortex-M3 processor for this purpose. Figure 3.20(a) shows the testing set up of the fabricated chip with the ARM processor. The measurement probe has been set to 10X position for high frequency measurement. Figure 3.20(b) shows the generated square-wave clock signal with the frequency of 22MHz. The 2-stage and the 15-stage SC DC-DC converters have been measured with the output of 8.53V and 31.5V, as shown in Figure 3.21(a) and (b) respectively. Both of the SC converters achieve very low output ripples. The power consumption has been measured based on the voltage dropped across a series resistor with a known value [115, 116]. The measured power consumptions are approximately 167 µW and 530µW with a zero output current for the 2-stage and the 15-stage SC converters.

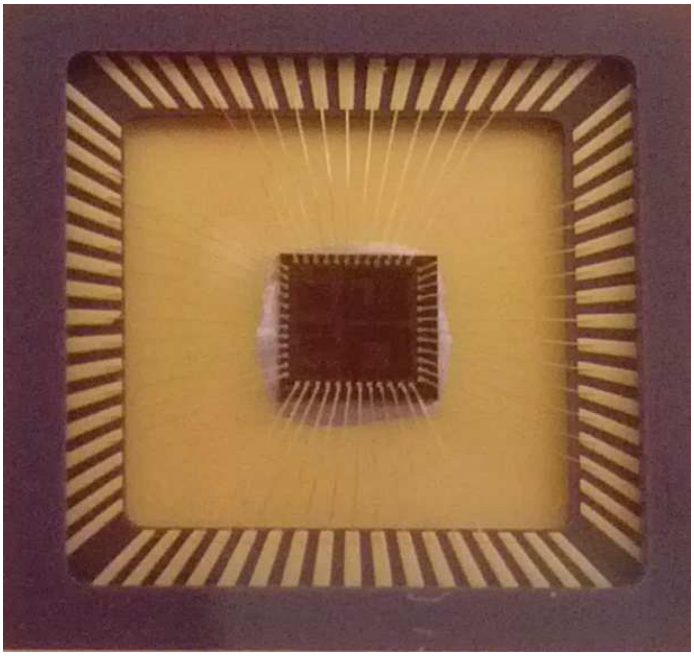
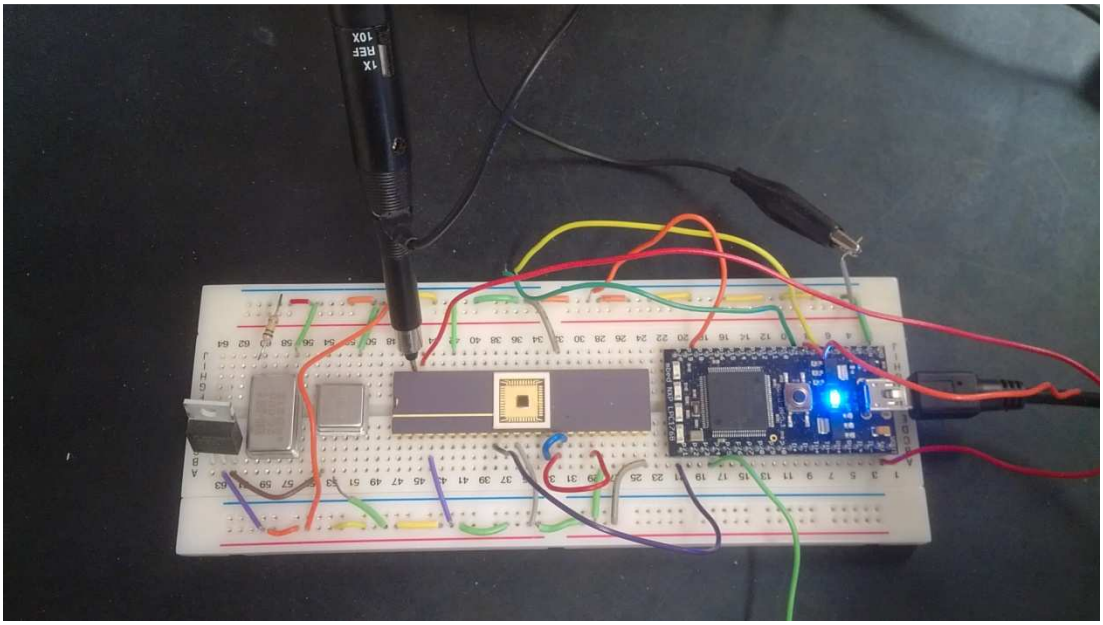
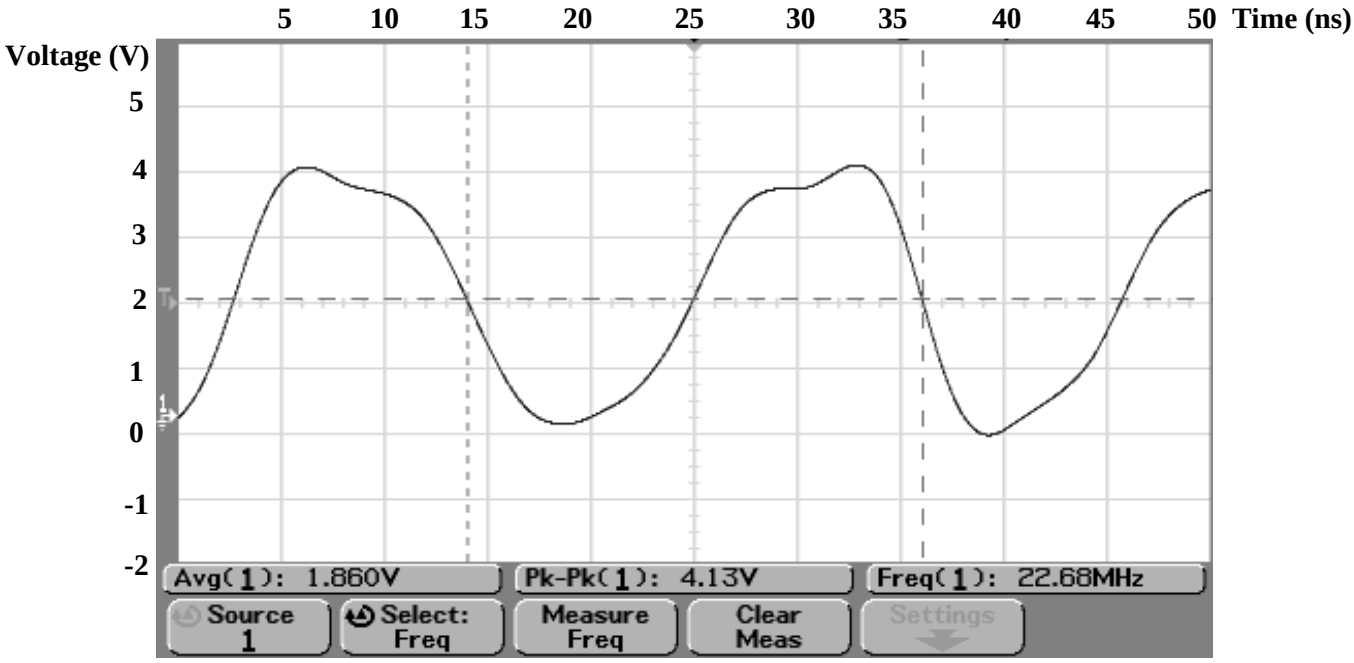


Figure 3.19: The fabricated SC DC-DC converter on a die

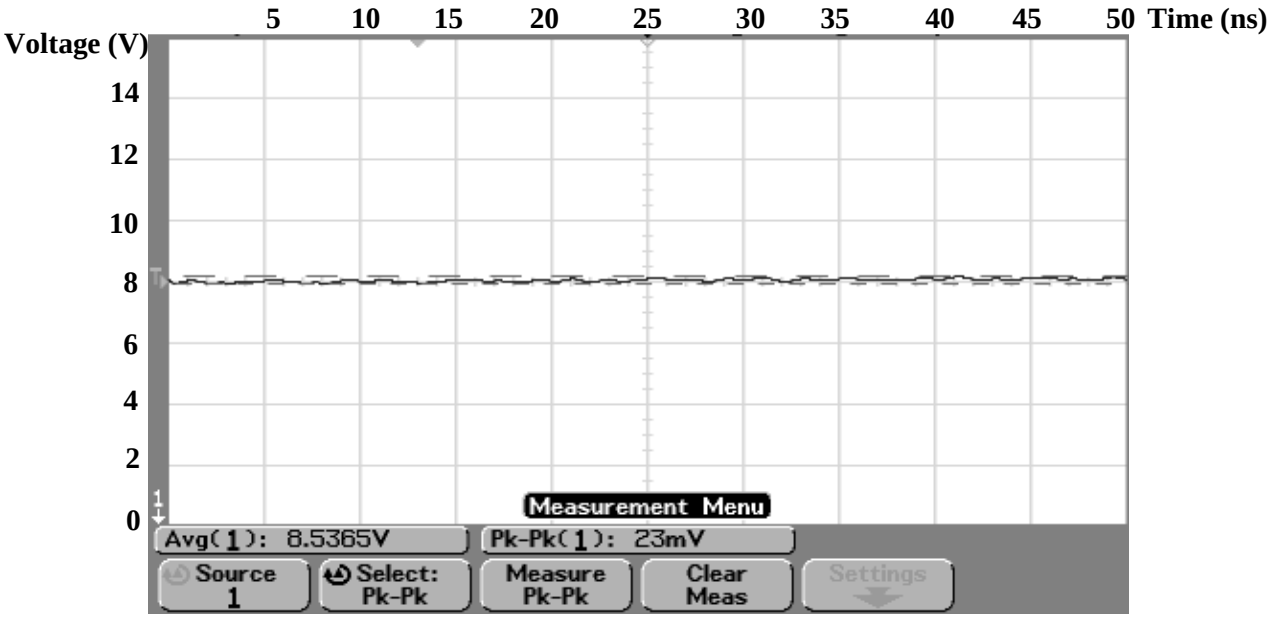


(a)

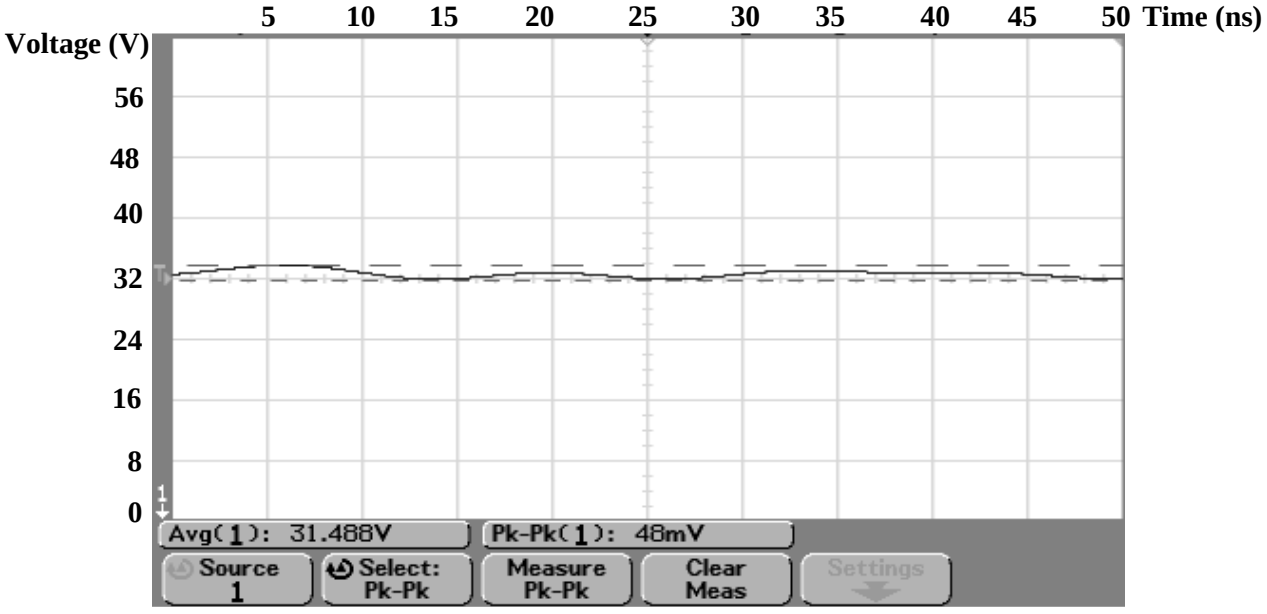


(b)

Figure 3.20: The fabricated SC DC-DC converter (a) in the testing set up environment and, (b) the generated 22MHz square ware clock signal by the ARM processor



(a)



(b)

Figure 3.21: Measured output voltages (a) at 8.53V for 2-stage (with voltage ripple of 23mV) and, (b) at 31.49V for 15-stage (with voltage ripple of 48mV) based on the 22MHz frequency

3.11 Discussion

By using a clock frequency of 22MHz rather than the design frequency 50MHz, the chip has been fully functioned but with a slight reduced output voltage and power consumption as expected. The smaller the clock frequency, the lower the output voltage and power consumption in the converter. This chip demonstrates that the proposed techniques have been successfully avoided the latch-up in the low voltage transistors that used in high voltage design.

In the future stage of development, the SC converter can be integrated with RF switches through flip chip technology, as suggested in Section 7.3.1. The output voltage of the SC converter can also be reconfigured through varying the clock frequency or assisted by auxiliary circuitries, as depicted in Appendix I.

3.12 Summary

The HV SC DC-DC converter has been designed in LV transistors technology in order to achieve high voltage conversion. Adaptive biasing circuits have been proposed to eliminate very high current peaks flowing to the substrate. The proposed adaptive biasing circuits successfully eliminate the leakage current, hence avoiding latch-up which normally occurs with low voltage transistors when they are used in a high voltage design. The use of LV transistors improves the transconductance and reduces the threshold voltage drop. Thus, a higher output voltage (more than 25%) is achieved compared to using high voltage transistors. The output voltage demonstrated also high linearity with very low ripples. The design parameters for the SC DC-DC converter, as an RF switch controller, have also been analysed and synthesised. A low loading effect of the SC DC-DC converter has been identified which allows the capacitors' size and the number of stages to be optimised. Thus, this significantly reduces the die area and the power consumption of the proposed SC DC-DC converter. To reduce the effect of parasitic capacitance in high voltage capacitors, the proposed charge recycling circuit reuses the charge and achieves a power saving of more than 40%. The proposed HV SC DC-DC converter has been benchmarked against previous research and shown to have the smallest die area with a higher output voltage. Figure 3.22 summarises the areas and the challenges addressed in this chapter. In the next chapter, impedance network designs for impedance transformation of the RF switches will be presented.

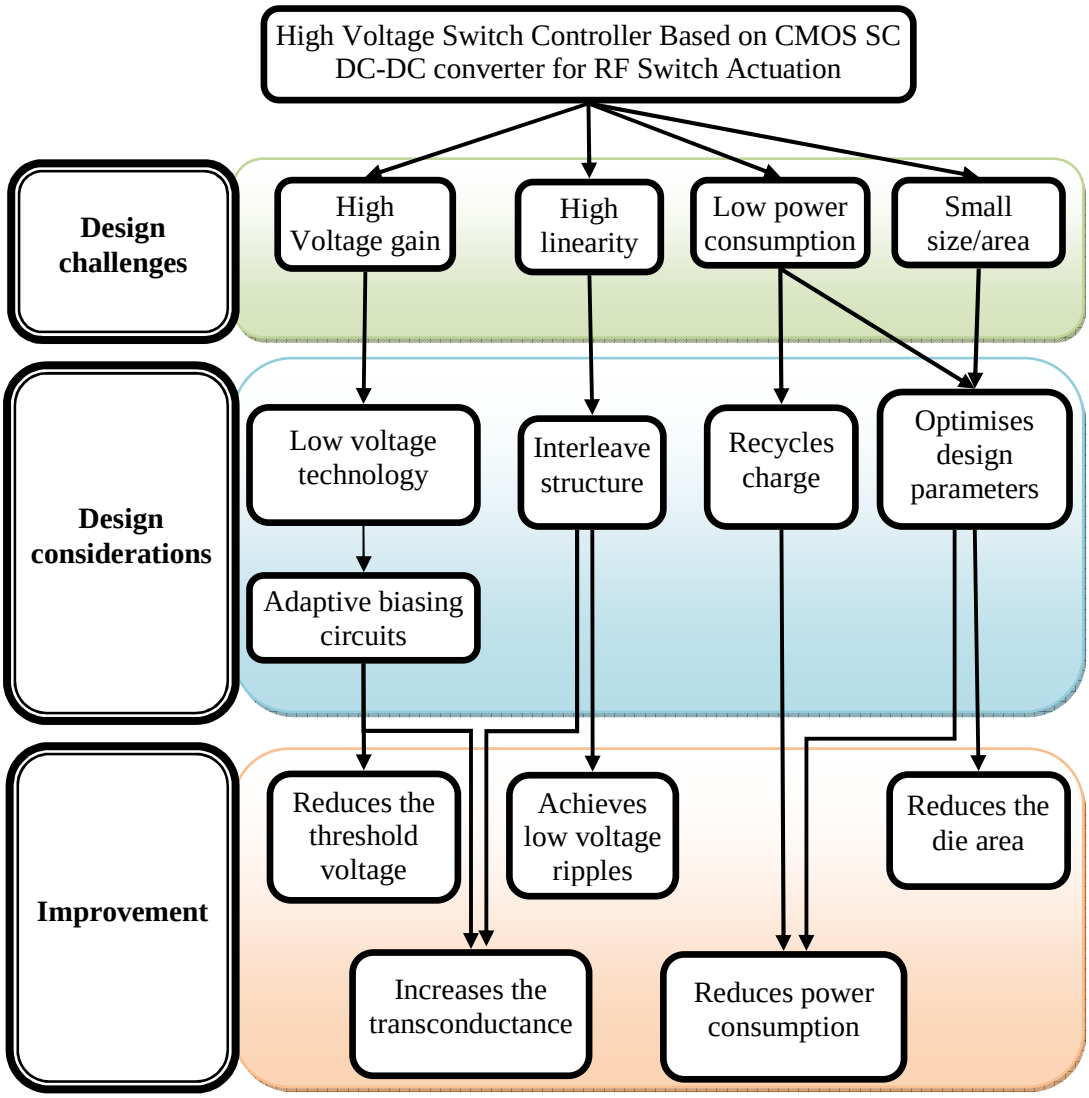


Figure 3.22: Summary of the areas and the challenges addressed in Chapter 3

Chapter 4: Tunable Impedance Network Designs for RF Switches Impedance Transformation

4.1 Introduction

A high voltage switch controller based on an SC DC-DC converter for RF switch actuation has been presented in Chapter 3. This chapter describes microstrip-based impedance network designs for impedance transformation of RF switches. Research investigation begins with the topologies of the impedance networks developed in the past and the associated practical considerations. An impedance transformation technique is presented to improve the area and reduce the losses in the impedance network through transforming the unrealisable to the realisable one. The technologies of the RF switches in the impedance network, which are semiconductors, Barium Strontium Titanate (BST) and Micro Electro-Mechanical Systems (MEMS), are compared and analysed. From the analysis, a large number of RF switches tend to be used in impedance networks in order to achieve large impedance coverage at multi-operating frequencies. However, this increases the losses, sizes and also the implementation complexity of an impedance network. For this reason, a design technique is proposed in order to achieve a wide impedance coverage with a reduced number of RF switches.

4.2 Impedance Network Topologies

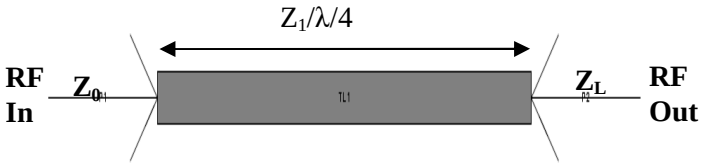
4.2.1 Real Impedance Matching

An impedance network may be realised by inserting a section of a quarter-wave (λ/4) transmission line with a characteristic impedance of Z_1, as by (4.1). The reflection coefficient can be determined by (4.2)[117]. A λ/4 impedance matching is the simplest impedance network that consists of a length of transmission line in the size of a λ/4 wavelength. The λ/4 impedance matching is designed in momentum ADS 2009, as presented in Figure 4.1(a). The λ/4 transmission line provides a perfect match at only a single frequency, as shown in Figure 4.1(b). Furthermore, a stand alone λ/4 transmission line can only match real load impedances. To match complex load impedance, the mismatched load needs to be transformed to a real impedance before applying this type of impedance network. An appropriate length of transmission line between the load and the λ/4 impedance network, or an appropriate series or shunt reactive stub can be used to transform a complex load impedance to a real impedance. However, these techniques will usually alter the frequency dependency of the equivalent load, which often has the effect of reducing the bandwidth of the match [118].

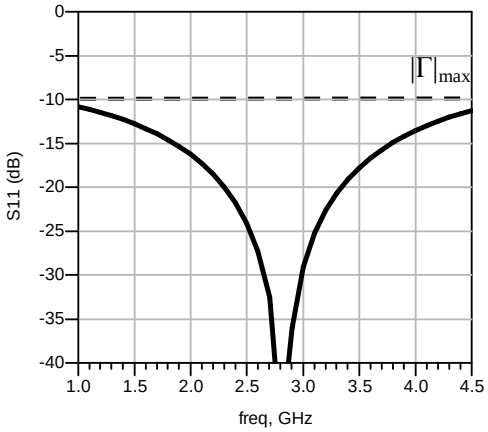
$$Z_1 = \sqrt{Z_0 Z_L} \tag{4.1}$$

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0 + j2t\sqrt{Z_0 Z_L}} \tag{4.2}$$

where Z_1 is the impedance characteristic of a λ/4 transmission line placed between nominal system impedance Z_0 and the antenna load impedance Z_L, t is tan βl and $\beta l = 90^0$. The reflection coefficient Γ is used to measure the degree of mismatch between the Z_0 and Z_L.



(a)



(b)

Figure 4.1: A quarter-wave impedance matching in (a) layout view and (b) its characteristic

A broadband design may be obtained by cascading multiple λ/4 transmission line sections and gradually varying their characteristic impedance on the line sections, as shown in Figure 4.2(a). By assuming all Z_n increase or decrease monotonically across the transmission line, the partial reflection coefficients at each junction can be defined by (4.3)-(4.6). The overall reflection coefficient can be approximated by (4.7) [119]. This approach reduces the reflection coefficient on the line at desired frequency bands, as shown in Figure 4.2(b). The design approaches of a multi-section transmission line can be based on Binomial or Chebyshev technique. A maximum reflection coefficient (or a maximum VSWR) that can be tolerated in the frequency bands will be specified during the design process. Figure 4.3 shows an example of a fabricated multi-section Binomial impedance network to transform 100 Ω into 50 Ω [56]. However, the fabricated impedance network is too large to be practical especially for mobile telecommunication systems. The length of the transformer is greater than λ/2 (β_L>Π) or approaching full length to minimize the mismatch [119].

$$\Gamma_1=\frac{Z_1-Z_0}{Z_1+Z_0} \tag{4.3}$$

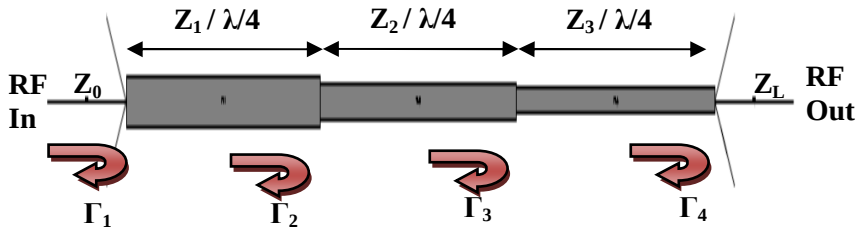
$$\Gamma_2=\frac{Z_2-Z_1}{Z_2+Z_1} \tag{4.4}$$

$$\Gamma_3=\frac{Z_3-Z_2}{Z_3+Z_2} \tag{4.5}$$

$$\Gamma_4=\frac{Z_L-Z_3}{Z_L+Z_3} \tag{4.6}$$

$$\Gamma(\theta)= \Gamma_0+ \Gamma_1 e^{-2j\theta}+ \Gamma_2 e^{-4j\theta}+ \Gamma_3 e^{-6j\theta}+ \Gamma_4 e^{-8j\theta} \tag{4.7}$$

where $\Gamma(\theta)$ is reflection coefficient response as a function of frequency (θ), $e^{-nj\theta}$ is the phase delay when the incident wave travels up and down the line that consists of n sections



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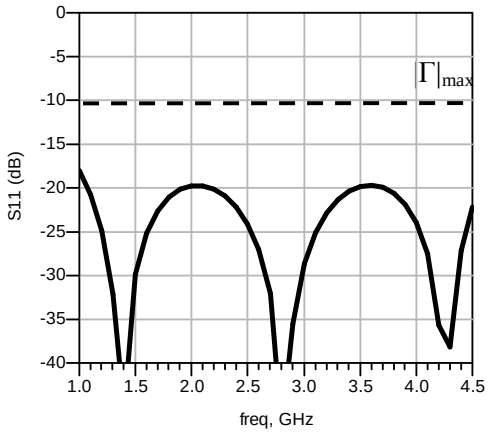
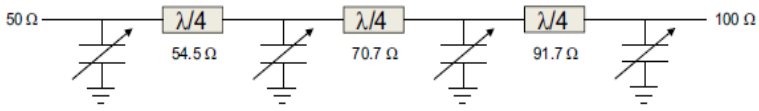
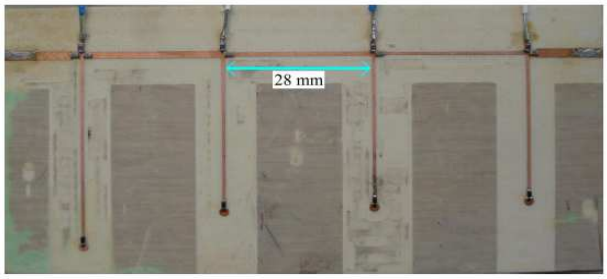


(b)

Figure 4.2: A multi-section impedance network in (a) layout view and (b) its characteristic



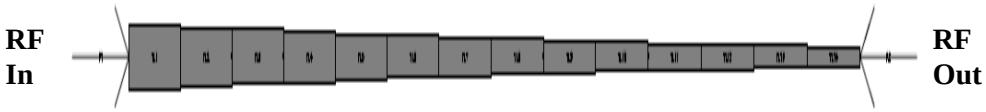
(a)



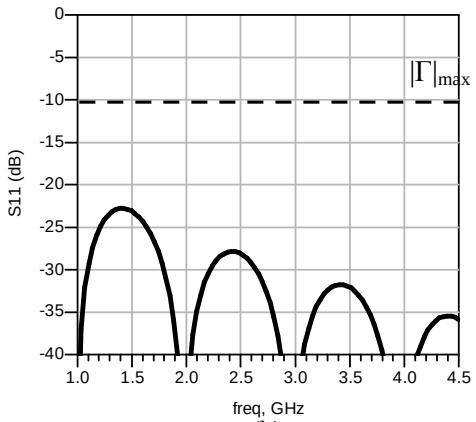
(b)

Figure 4.3: A Binomial multi-section impedance network to transform from 50 Ω and 100 Ω in (a) schematic view and (b) prototype [56]

As the number of discrete sections increases, the step changes in characteristic impedance between the sections become smaller. Thus, with a limit of an infinite number of sections, a continuously tapered line further reduces the reflection coefficient compared to the multi-section transmission line. Instead of discrete sections, the line is continuously tapered as shown in Figure 4.4(a). Lower reflection coefficient |Γ| is obtained in the taper, as shown in Figure 4.4(b). However, the taper also occupied a large layout area with the length of the taper about ½ to 2 of wavelength in order to reduce the mismatch [119]. A continuous tapered line can be based on the exponential, triangular or Klopfenstein approach [120].



(a)



(b)

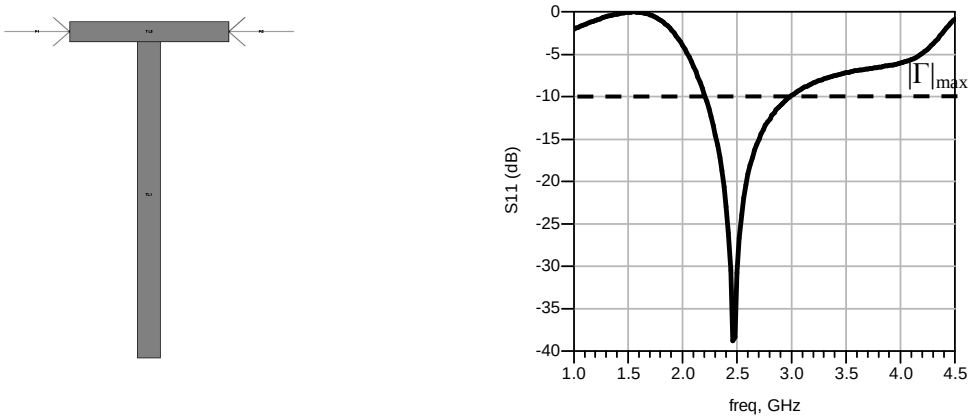
Figure 4.4: A continuous tapered line in (a) layout view and (b) its characteristic

4.2.2 Complex Impedance Matching

For complex impedance matching, matching stubs and lumped elements can be used. These are described as follows.

4.2.2.1 Matching Stub

Matching stubs are widely used to match a complex load impedance to the system impedance. They consist of shorted or opened stubs and are connected in parallel with the main transmission line at a distance from the load. The distance corrects the real part of the complex impedance. The parallel stub provides the required susceptance to cancel the load susceptance. A single matching stub and its characteristic are shown in Figure 4.5(a) and (b). If more mismatch loads are to be matched, double or triple stubs may be used. Triple stubs have a higher degree of freedom in the design to correct impedance mismatch.



(a) (b)

Figure 4.5: Single matching stub in (a) layout view and (b) its characteristic

4.2.2.2 Matching Lumped Elements

Matching stubs will occupy a large area at lower RF frequencies. To achieve a smaller size impedance network, lumped reactive components may be used for matching at lower RF frequencies [121]. Generally, the matching lumped elements consist of L-, π- or T- type topologies, as shown in Figure 4.6(a), (b) and (c). The impedance networks use only reactive elements i.e. inductors or capacitors, to correct any load impedance. The changes of the impedance due to series or parallel connected inductors and capacitors can be observed based on the trajectories on the Smith chart, as shown in Figure 4.6(d). The L-type matching

network can match any mismatch load, but its bandwidth and quality factor are fixed uniquely by the values of the antenna load and system impedances [118]. The π-and T- type impedance networks have an extra degree of freedom that they are able to control the bandwidth at the matched condition. One of the advantages of the T-type network is that it often results in more practical values for the circuit elements; however, the T-type network tends to have more losses [57].

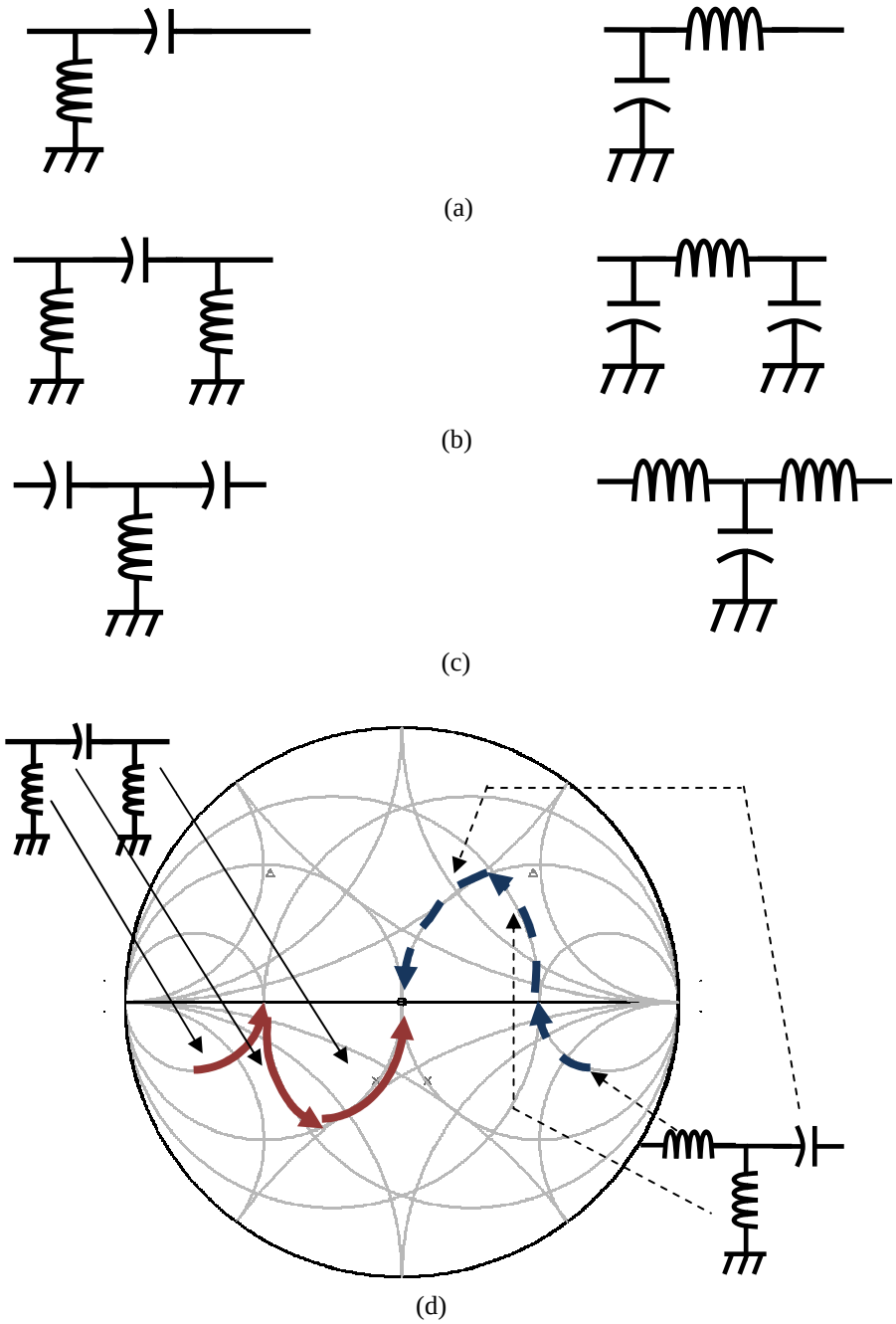


Figure 4.6: Matching lumped elements with (a) L-network, (b) *Pi*-network, (c) T-network and (d) the trajectories of series and parallel inductors and capacitors on the Smith chart

4.3 Optimisation of Impedance Network Topologies

Most of the impedance networks have inductors in their topologies, as in previous research work [28, 55, 122]. Small values of inductance are realised either by coplanar waveguide or bondwires implemented using silicon-on-glass technology [7, 123]. Large inductance can be obtained in a spiral microstrip inductor or a lumped element inductor.

The spiral microstrip inductor requires a number of turns using the narrowness of the track to obtain a large inductance value. This leads to a significant series resistance and skin effect which limit the quality factor (Q) of the inductor. The large inductance results in more losses, which leads to a spurious resonance that limits the maximum operating frequency [119].

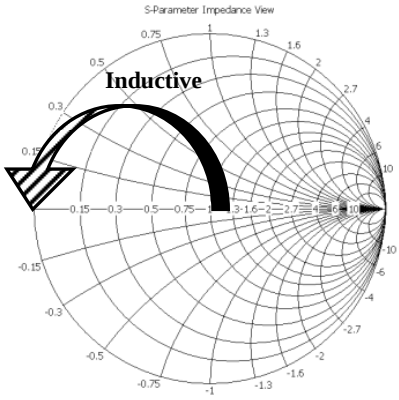
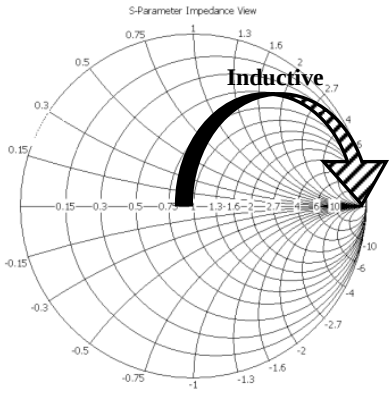
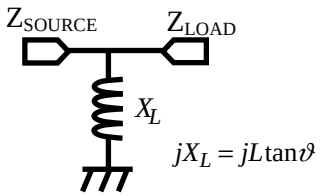
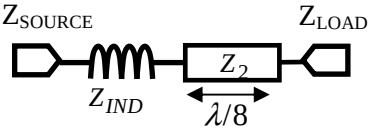
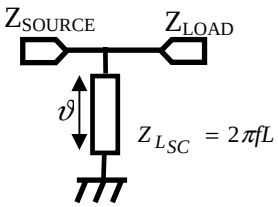
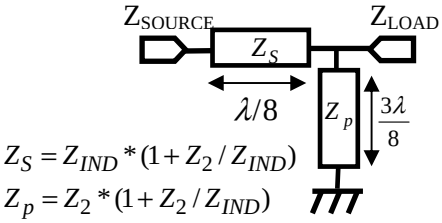
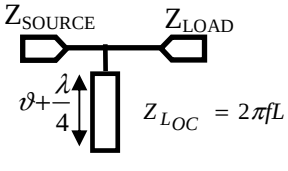
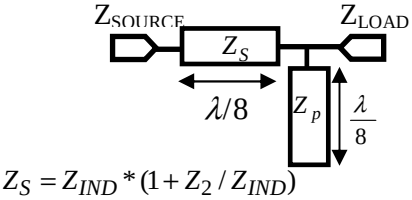
For the lumped element inductors, they also contribute significant losses to the impedance network, as reported in [7, 16, 28, 57, 124]. The loss by the components used in the impedance network was even up to -11dB [13]. Furthermore, the inductors may be prohibited in certain applications due to their power handling constraints [122].

To have a more practical impedance network topology, the impedance network has to transform from an unrealisable to a realisable one. The inductor will be replaced with a matching open-circuited stub (L_{OC}) or a short-circuited stub (L_{SC}). Techniques to transform between the L_{OC} and the L_{SC} will also be presented as follows.

4.3.1 Techniques for Impedance Transformation

To exclude an inductor from the impedance network topology, the reactance of the inductor can be transformed to an approximate lossless microstrip matching stub through Richard's transformation [119], as shown in Table 4.1. The inductor, which is connected in either series or parallel to the RF path, can be transformed to an L_{OC} or an L_{SC}. Table 4.1 shows the trajectory of the parallel and the serial connected inductors on the Smith chart.

Table 4.1: Impedance transformation

	Impedance Transformation of Parallel Inductor	**Impedance Transformation of Serial Inductor**
Smith Chart		
Lump Component		
Short-Circuited Stub (L_{SC})		
Open-Circuited Stub (L_{OC})		

i. Parallel Connected Inductor

For a parallel connected inductor, the increase of inductance moved in an anti-clock wise direction on the Smith chart. Similar trajectories on the Smith chart can be obtained by using the L_{SC} or the L_{OC} to replace the parallel inductor, as shown in Table 4.1.

ii. Series Connected Inductor

For a series connected inductor, the increase of inductance moved in a clock wise direction on the Smith chart. Kuroda's identities can be used in order to transform the series inductor to a λ/8 long L_{OC} or a 3λ/8 long L_{SC}. The λ/8 long transmission line was used for simplicity in the hand calculation.

iii. Interchanges between the L_{SC} and the L_{OC}

To transform between the L_{SC} and the L_{OC}, an additional λ/4 wavelength can be added. An L_{SC} can be converted to an L_{OC} by having an additional λ/4 wavelength, thus $L_{SC} = L_{OC} \pm 90^0$. For an L_{SC} shorter than λ/4, the stub has an inductive reactance and moves to the upper hemisphere of the Smith chart. The length and the impedance characteristic of the L_{SC} are adjusted for the required inductance of the circuit. Similarly, by having an additional λ/4 wavelength, the L_{OC} changes the sign of its reactance from capacitive to inductive. In fact, the L_{OC} is preferable in a microstrip circuit since it is easier to be fabricated compared to the L_{SC}, which requires a via hole through the substrate to the ground plane.

4.4 Tunable Impedance Network

The fixed impedance networks are not able to change the impedance to correct the additional mismatch once implemented [118, 119]. Thus, to dynamically correct the impedance mismatch, a tunable impedance network is needed. The performance of the tunable impedance network is strongly influenced by the considered RF switches technologies. The RF switches technologies have to meet demanding requirements such as linearity, insertion loss and tuning range. Several RF switches technologies are currently being utilised in the impedance networks applications. There are conventional technologies such as semiconductor technology, as well as newer technologies such as Gallium Arsenide (GaAs), Barium Strontium Titanate (BST) and Micro Electro-Mechanical Systems (MEMS), which will be discussed in the following sections.

4.4.1 Semiconductor

Semiconductor- based RF switches are widely used because of their easy availability as tuning elements in RF frequencies and their relatively ease in developing a prototype. Semiconductor-based varactor diodes have been used in much of the earlier work for impedance tuning applications [13, 125, 126]. The semiconductor varactor diodes are usually made of silicon-on-sapphire (SOS) [127], silicon-on-insulator (SOI) [128] or Gallium Arsenide (GaAs).

4.4.1.1 Silicon

The semiconductor varactor diodes fabricated using silicon-on-sapphire (SOS), or silicon-on-insulator (SOI) are low in cost and cheap to process. Silicon possesses a much higher hole mobility, allowing the fabrication of a higher speed P-channel FET, which are required for a CMOS digital circuit. Thus, the digital interface can be integrated directly onto silicon switches, achieving a compact module or system. A moderate amount of dc power by P-I-N diodes (3-10mV per P-I-N diode) and virtually no dc power by Field-Effect transistor (FET)-based varactor diodes have been reported in previous research work [125]. However, the performance of the silicon based RF switches is significantly degraded at higher frequencies.

4.4.1.2 Gallium Arsenide

The semiconductor varactor diodes, fabricated using Gallium Arsenide (GaAs) j-PHEMT, are able to operate at higher frequencies compared to silicon technology. Furthermore, the GaAs varactor diodes are relatively insensitive to heat owing to their wide bandgap. In addition, the GaAs varactor diodes tend to have less noise than silicon varactor diodes, especially at higher frequencies. However, the GaAs technology lacks a fast digital circuit structure as in the silicon technology. A separate digital controller is required for switching the GaAs varactor diodes which increases the power consumption and complicates the design implementation.

4.4.1.3 Performance

Varactor diodes have an inherent tradeoff between on-resistance and off-capacitance. Figure 4.7 shows the circuit model of a varactor [129]. Datasheet of the varactor has been included in Appendix III. The on-resistance affects the quality factor (Q) of the device, while the off-capacitance increases the parasitic loading due to the off branches. For reasonable performance, semiconductor switches fabricated using either GaAs j-PHEMT, SOS, or SOI are integrated with Metal-Insulator-Metal (MIM) capacitors. For an overall capacitance ratio of 5:1 together with associated MIM capacitor losses and parasitic, this leads to an effective Q in the maximum capacitance state at 1 GHz of 25 to 50. For impedance matching applications, and for antennas with relatively low VSWR, this moderate Q for the switched capacitor solution may yield acceptable performance.

For high power applications, voltages as high as 40 to 100 V are encountered due to the high VSWR encountered in antennas. In many cases, the breakdown voltage of the transistors and/or capacitors will not meet the power handling requirements and must be stacked, increasing the insertion loss and cost/size accordingly [1]. The insertion losses are around 5dB at 19GHz [126] and 15dB at 35GHz in the filter designs [130]. In [13], the insertion loss is about 11dB at 4.8GHz in the triple-stub impedance network design. Recent research work has improved the doping techniques and reduced the losses to 3dB at 1.4GHz in the double-stub impedance network based on Silicon Carbide (SiC) varactors [131].

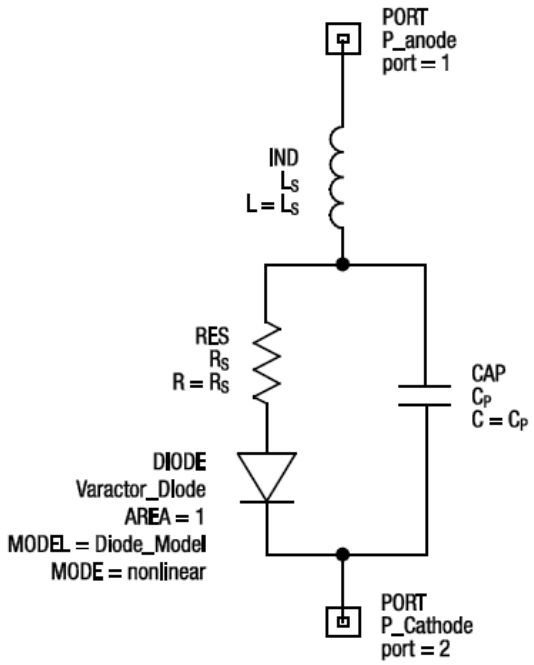


Figure 4.7: SPICE model of a varactor

4.4.1.4 Availability

There is a relatively large variety of commercial products from semiconductor based technologies. The firms that produce semiconductor switches for RF applications are Skyworks [129], Infineon [132], Avago Technologies [133], Texas Instrument [134], etc.

4.4.2 Barium Strontium Titanate

Barium Strontium Titanate (BST) is a notable ferroelectric material. BST based capacitive RF switches can be varied with a controlled voltage, thus achieving a continuous tuning. When the controlled voltage is near zero, the unit cells in the crystal lattice are easily polarised leading to the peak dielectric constant in the capacitive RF switches. Thus, a large tuning value is achieved. As a higher controlled voltage is applied, the resulting polarisation reduces the sensitivity to an additional field, which lowers the effective dielectric constant in BST based capacitive RF switches. This inherent nonlinear behaviour is used to build variable capacitive RF switches that are controlled by applied voltages. Lower losses are

possible in BST switches than those available from semiconductor switches, leading to an expanded range of applications for BST based capacitive RF switches. However, the key limitations in BST based RF switches are low tuning ratio, thermal stability issues and marginal linearity. Typically, the BST switch exhibits a 3:1 tuning ratio. The low tuning ratio is intentionally limited to provide a stable operation and a reasonable linearity. A fabricated BST based RF switch is shown in Figure 4.8[135].

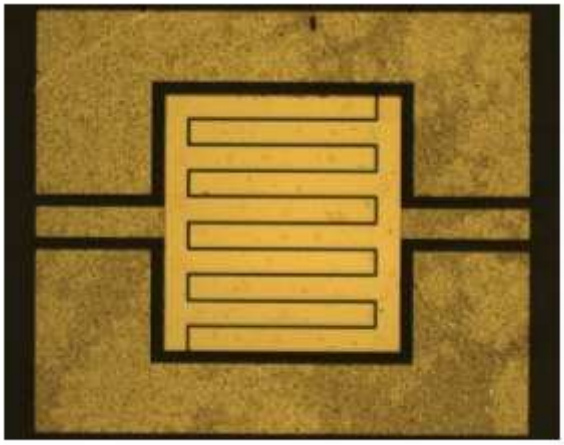


Figure 4.8: BST interdigital capacitive electrodes RF switches with five finger pairs [135]

4.4.2.1 Performance

BST based capacitive RF switches have been used in tunable impedance networks [136, 137]. Research work shows that the insertion loss for the impedance network with all biasing voltages from 0 to 18V is below 0.3dB [137]. The impedance network based on an all-pass topology also achieves an insertion loss of less than 5dB [136]. However, the effective tuning ranges are limited to a factor of 2 [137] and 3.2 [136] because of the forward biasing and the breakdown constraints of BST technology.

4.4.2.2 Availability

Paratek Microwave provides a BST-based material (ParaScan) for tunable RF applications [138, 139].

4.4.3 Micro Electro-Mechanical Systems

Recent work in tunable impedance networks has involved with RF MEMS switches. RF MEMS switches are surface-micro-machined devices which use a mechanical movement for an electrical change in the RF transmission-line. They are designed to operate at RF to mm-wave frequencies (0.1 to 100 GHz). They are composed of a thin metal membrane which can be electro-statically actuated to the RF line using a high DC voltage.

RF MEMS switches can be designed by different mechanical structures. For instance, an ohmic RF MEMS switch could be operated by establishing the electrical connection through the beam that was deflected by a voltage between the gate and the source electrodes, as shown in Figure 4.9 [140]. The free end of the beam contacts the drain and completes an electrical path between the drain and the source. Another type of capacitive RF MEMS switch operates by varying its capacitance through adjusting the position of the membrane up or down, as shown in Figure 4.10 [141, 142].

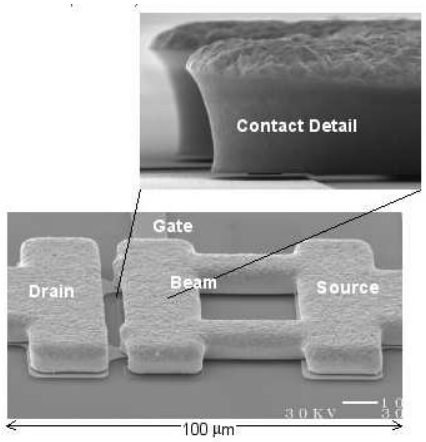


Figure 4.9: Scanning Electron Microscope (SEM) micrograph of ohmic RF MEMS switching technologies for discrete tuning approach [140]

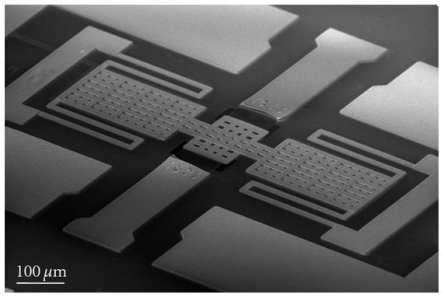


Figure 4.10: SEM micrograph of capacitive RF MEMS switching technologies for continuous tuning approach [141]

4.4.3.1 Performance

RF MEMS switches are inherently low loss and are able to handle power with high linearity. The first planar double stub impedance network using RF MEMS switches was developed at 20GHz [143]. In the same year, two types of impedance networks have been developed. The first achieves an insertion loss of 4-7dB at 29GHz (two capacitive RF MEMS switches) and the second achieves 4-12dB at 30GHz (12 ohmic RF MEMS switches) [144]. In [145], the impedance network using eight elements RF MEMS switches reduces the loss by consuming only a total of 0.5dB loss at 4-12GHz, but slightly increases to 1.5dB at 18GHz. The loss is further reduced for an impedance network with six elements RF MEMS switches with an insertion loss better than 0.6dB from 6 to 18GHz [146].

RF MEMS switches achieve better RF performance compared to semiconductor and BST based technologies. The RF path in the RF MEMS switches is through a metal trace with virtually no frequency response on it, thus achieving a higher quality factor (Q) and linearity compared to semiconductor-based technologies. Also, the DC voltage is physically separated from the RF path; thus, the voltage handling is high. However, as a mechanical device, there exists an aging effect which eventually will cause device failure, related to wearing out. Recent RF lifetime tests of RF MEMS switch have been carried out. Approximately 500 million cycles has been achieved for hot switching before experiencing intermittent sticks; cold switching reliability test has exceeded 10^{10} cycles with the current applied only during switch closure [147]. Relevant RF lifetime datasheets have been enclosed into appendix. Furthermore, RF MEMS switches require high DC control voltages to prevent self-actuation and maintain linearity. More discussion on the DC control voltages have been presented in Chapters 2 and 3.

4.4.3.2 Availability

Due to the ability of RF MEMS switches in high power handling with low loss and high linearity, a lot of firms have recently developed RF MEMS switches. There are six firms with sampling ohmic RF MEMS switches. California-based WiSpry Inc. is offering RF MEMS for high-volume mobile applications [148-150]. On another front, U.S. firms Analog Devices Inc.[151], Radant Technologies Inc. [152] and XCOM Wireless Inc.[153], are in cooperation with relay manufacturer Teledyne Technologies Inc. as well as Japanese supplier Omron Corp., and are targeting high-end applications for testing and

instrumentation, such as automatic test equipment (ATE) and RF test [154]. US start-ups Radant MEMS [140] and MEMtronics [155] focus on defence applications. Fewer companies deal with capacitive RF MEMS switches. Japan's TDK-Epcos [156], US-based Cavendish Kinetics [157] and Scotland-based Sofant Technologies [142, 158] are offering capacitive MEMS for mobile applications.

4.4.4 Comparison

A general summary of the strengths and weaknesses of RF switch technologies is shown in Table 4.2 [1, 56]. Q is defined as the ratio of energy stored in a component to the energy dissipated by the component. The tuning ratio is the range of the variable capacitive ratio with the applied voltage.

Table 4.2: Comparison of operating performances in RF switches technologies

	Semiconductor technologies	**Barium Strontium Titanate**	**Micro Electro-Mechanical Systems**
Quality factor (Q)	Medium	Medium	High
Tuning ratio	High (for low Q) Low (for high Q)	Low	High
Power handling	Low	Medium	High
Linearity	Medium	Medium	High
Switching cycles	High	High	Medium
Cost	Low	Medium	Medium
Reliability	Low	High	Medium

A comparison of capacitance-voltage (CV) curves in RF switch technologies is also presented in Figure 4.11. The capacitances of the semiconductor switches (SMV1235, SMV1232, SMV1247 from Skyworks [159] and BB833 from Infineon [132]) and BST switch [56] decrease with applied voltages. The capacitance of the RF MEMS switch (EPCOS [160]) increases with the applied voltages. RF MEMS switch shows a larger capacitance tuning range compared to the semiconductor switches and the BST switch.

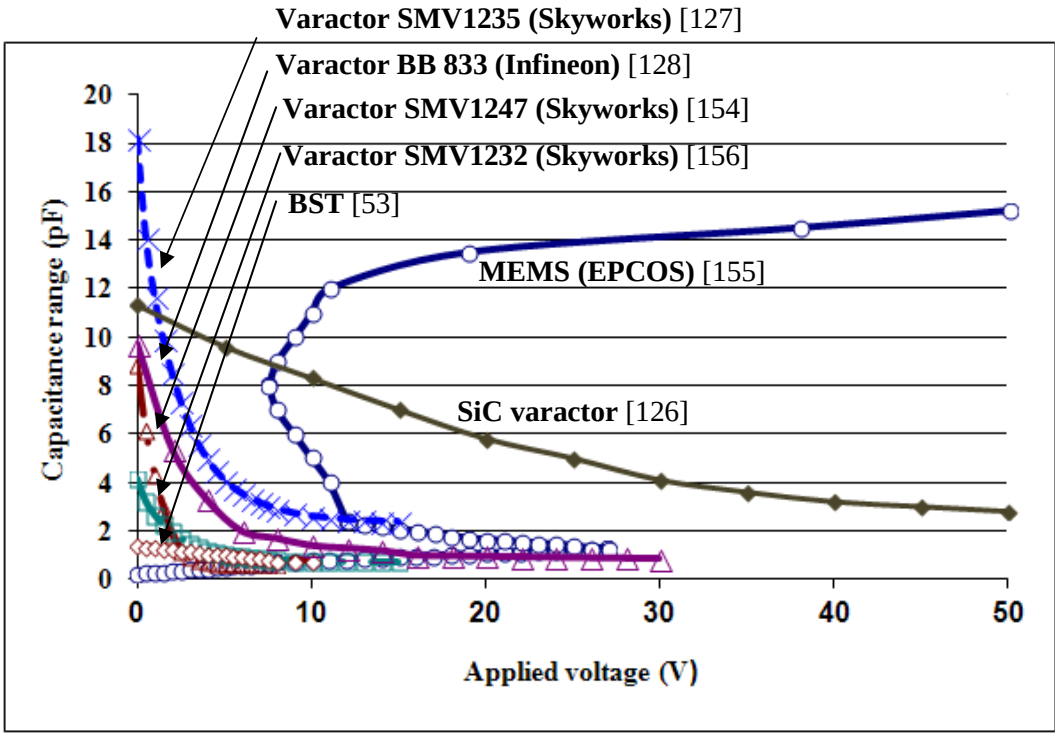


Figure 4.11: Comparison of capacitance-voltage (CV) curves for a selection of RF switches technologies

4.5 Tunable Impedance Networks with Wide Impedance Coverage

Most of the impedance networks use a large number of RF switches for wide impedance coverage. For instance, the single stub impedance network that developed in [58] uses four RF switches on the shorted t-lines stub and six RF switches on the transmission line in order to achieve impedance coverage from 20GHz to 50GHz. The double stubs impedance network that developed in [162] and [144] use eight RF switches for impedance coverage from 10GHz to 20GHz [162], and 12 RF switches for impedance coverage from 29GHz to 32GHz [144]. The triple stubs impedance network that reported in [163] use eleven RF switches in order to produce 2^{11} different impedances for 75GHz to 100GHz.

These impedance networks provide, in general, very good impedance coverage, but they use a large number of RF switches in the designs which suffer from expensive packaging and cost. This, on the other hand, increases insertion loss caused by a large number of RF switches. Complexity also increases dramatically in the control circuitry and the impedance searching algorithm which deals with a large number of RF switches.

In this work, a design strategy is proposed to achieve wide impedance coverage with a lesser number of RF switches in the impedance network.

4.6 Impedance Network Design Technique

A typical *Pi*- network, with two RF switches, connected to an antenna is shown in Figure 4.12. The antenna load (Z_{Load}) is modelled by an inductor in series with a resistance which represents all possible radiation and loss resistances and a parallel capacitance. The spreading of the impedance values across the Smith chart indicates the impedance tuning region of the network. An example of the trajectories of two RF switches (C_1 and C_2) in a *Pi*-network, as shown in Figure 4.13.

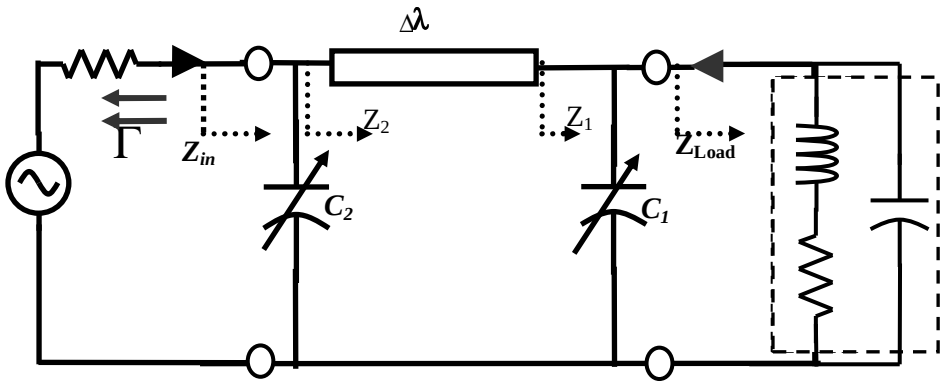


Figure 4.12: A *Pi*-network with related network parameters

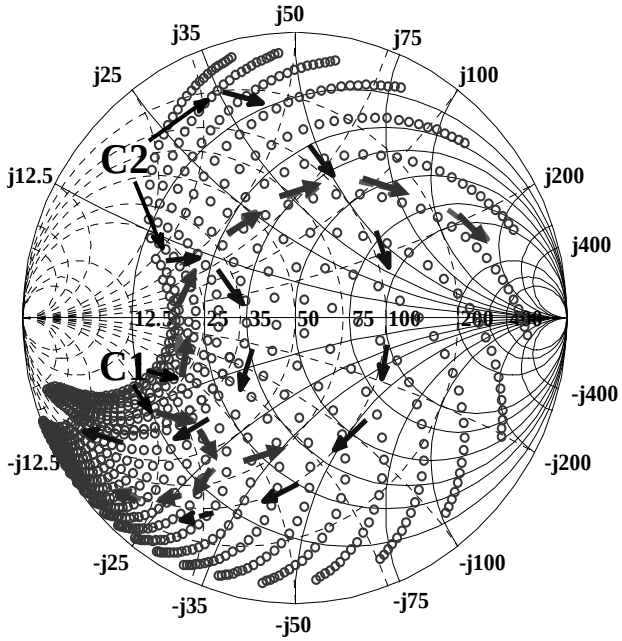


Figure 4.13: Simulated impedance coverage (lossless) of a sample *Pi*-network. The arrows indicate the directions of increase for C_1 and C_2 from 1pF to 37pF.

4.6.1 In Consideration of Topology

One of the disadvantages of the *Pi*-network topology is that it cannot achieve full impedance coverage [119]. The design parameter that determines the unachievable range will be the electrical distance between the two tuning components ($\Delta\lambda$), as shown in Figure 4.12. The unachievable region can be minimised by making the $\Delta\lambda$ very small or very close to a multiple of $\lambda/2$. However, as the $\Delta\lambda$ approaches zero (or $\lambda/2$), the circuit becomes more frequency sensitive and implementation difficulties arise. By assuming a $\Delta\lambda=36^0$, the impedance network can determine the achievable minimum real part of the impedance as 17.3 Ω or 0.058 mho by (4.8) [119].

$$0 \le G_L \le \frac{Y_0}{\sin^2 \Delta\lambda} \tag{4.8}$$

where G_L is conductance (a reverse of resistance), Y_0 is the nominal system admittance and $\Delta\lambda$ is the distance between RF switches

Once the distance between the tunable components was chosen, the susceptances of each stub can be determined by (4.9) and (4.10)[119].

$$B_1 = -B_L + \frac{Y_0 \pm \sqrt{(1+t^2)G_L Y_0 - {G_L}^2 t^2}}{t} \tag{4.9}$$

$$B_2 = \frac{\pm Y_0 \sqrt{Y_0 G_L (1+t^2) - {G_L}^2 t^2} + G_L Y_0}{G_L t} \tag{4.10}$$

where G_L and B_L are the real and imaginary parts of the load admittance respectively, and $t=tan(\Delta\lambda)$.

The required susceptances for the impedance network with the $\Delta\lambda=36^0$ can be calculated as shown in Table 4.3. In order to achieve the impedance tuning regions for $20\Omega<R_{LOAD}<80\Omega$ and $-150\Omega < X_{LOAD} <150\ \Omega$ at three operating standards which are LTE, GSM and GPS, a tuning range of 3.07pF to 43pF in RF switches is required.

Table 4.3: Calculation of the required susceptances for the stubs and equivalent capacitances to match the non 50Ω impedance loads to 50Ω with a $\Delta\lambda=36^0$ at different operating standards

Load Impedance Z_{Load} (Ohm)	**Stubs**	**Susceptance B (mho)**	**Capacitance (pF)**		
			LTE (700MHz)	**GSM (900MHz)**	**GPS (1.575GHz)**
20+j*0	1	0.04739	10.77	8.38	4.19
	2	0.03547	8.06	6.27	3.14
80+j*0	1	0.05135	11.67	9.08	4.54
	2	0.06564	14.92	11.61	5.80
20-j*150	1	0.02803	6.37	4.96	2.48
	2	0.18912	43.00	33.44	16.72
20+j*150	1	0.04113	9.35	7.27	3.64
	2	0.18912	43.00	33.44	16.72
80-j*150	1	0.03469	7.89	6.13	3.07
	2	0.11677	26.55	20.65	10.33
80+j*150	1	0.04507	10.25	7.97	3.99
	2	0.11678	26.55	20.65	10.33

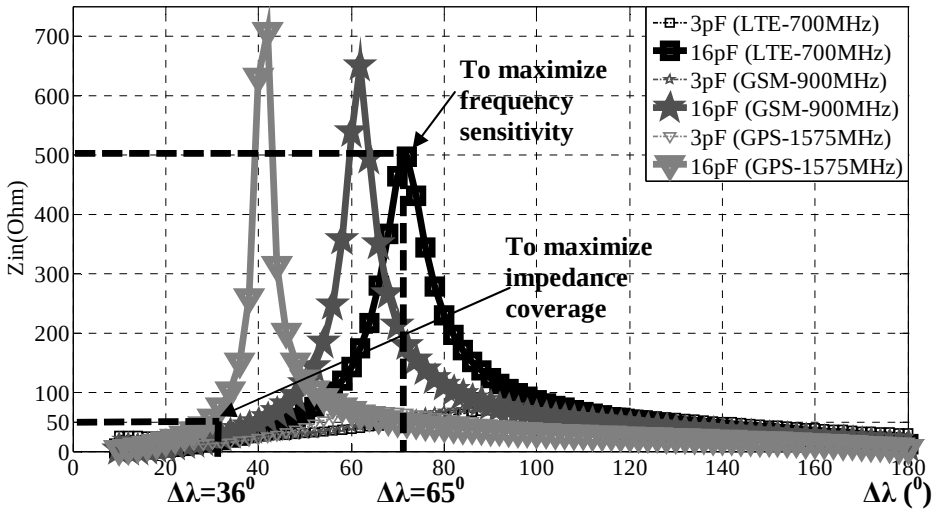
4.6.2 In Consideration of Maximum Impedance Coverage

The effects of $\Delta\lambda$ to the sensitivity and the magnitude of input impedance (Z_{in}) at the *Pi*-network are demonstrated in Figure 4.14(a). The simulations are performed by varying the $\Delta\lambda$ at three operating frequencies in order to observe the changes of the magnitude of Z_{in}. Simulations have been performed using Advanced Design Systems (ADS 2009) based on a 1.6 mm-FR4 substrate with a dielectric constant of 4.55.

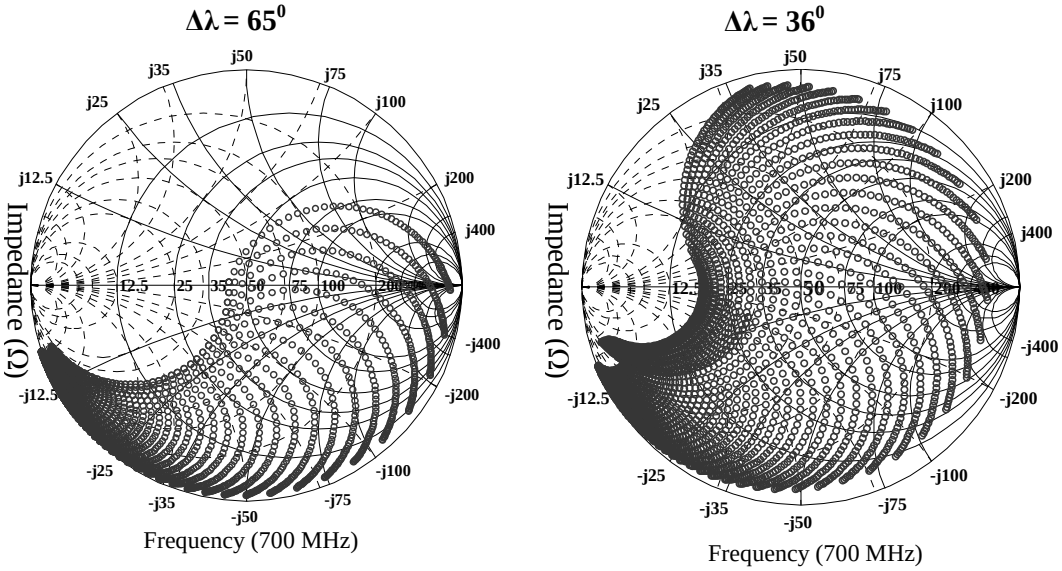
In Figure 4.14(a), a $\Delta\lambda$ of 65^0 achieves the maximum frequency sensitivity in the impedance network at LTE operating standard. A significant change to the magnitude of Z_{in} by slightly varying the $\Delta\lambda$ is observed at Figure 4.14(a). However, with the distance of $\Delta\lambda=65^0$, the input impedance is about 500Ω, which is too large for this design application. In contrast, by selecting the $\Delta\lambda$ approximates to 36^0, Z_{in} varies around $\pm 50\,\Omega$. This range of impedance is suitable for compensating the impedance variation at the antenna load in mobile applications.

The $\Delta\lambda$ for maximum impedance coverage is approximately around 36^0 for other operating standards. By identifying the $\Delta\lambda$ for maximum impedance coverage, the capability of the impedance network in impedance matching is significantly increased.

Figure 4.14(b) shows the simulated impedance coverage at LTE standard in the Smith chart based on ideal tuning components (without loss) for $\Delta\lambda$ at 36^0 and 65^0, respectively. Nearly 80% of the coverage in the Smith chart is achieved by using $\Delta\lambda=36^0$, compared to $\Delta\lambda=65^0$ which acquires less than 50% of the coverage.



(a)



(b)

Figure 4.14: Technique in choosing the electrical length of the series transmission line (Δλ) based on tuning range and operating frequency. (a) Magnitude of the input impedances for different electrical length of the series transmission line using capacitor values of C_1=[1pF, 37pF] and C_2=[1pF, 37pF], and (b) the impedance coverage in the Smith chart at $\Delta\lambda=36^0$ and $\Delta\lambda=65^0$ (lossless)

4.7 Verifications

An impedance network with a reconfigurable Δλ is designed as shown in Figure 4.15. The Δλ will be reconfigured to three operating frequencies in this experiment's work. Only two RF switches (C_1 and C_2) were employed in the impedance network. For the simplicity of biasing circuits, the series inductors have been simplified with serial transmission lines. The Δλ between C_1 and C_2 is adjusted by using an additional stage switching component (C_W), to have an additional electrical reactance for different frequencies.

The impedance network is first designed at GPS frequency. The C_W will be set to 0.95976pF to achieve Δλ=36º at GSM frequency. When turning to LTE frequency, C_W will be set to 1.5873pF to provide the additional electrical distance between C_1 and C_2, thus maintaining an equivalent Δλ=36º between C_1 and C_2.

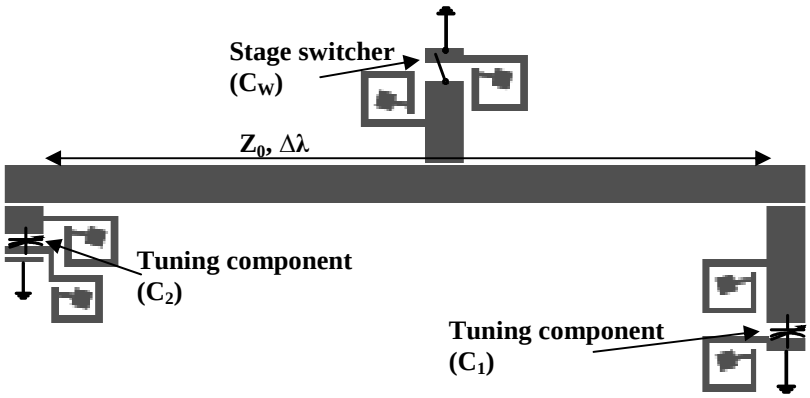


Figure 4.15: Layout of the Δλ reconfigurable *Pi*-network

4.8 Prototyping

The photograph of the prototype impedance network, fabricated on a FR-4 with a dielectric constant of 4.3 and thickness of 1.6mm, is presented in Figure 4.16. Two commercially available varactor diodes were used as the tuning elements with the hyper-abrupt junction capacitance range of 2.03pF to 37.35pF [164]. A varactor diode was used as the C_W for adjusting the $\Delta\lambda$ [159]. The varactor diodes were biased by three biasing voltages (V_B) which individually had a variable voltage from 0V to 8V.

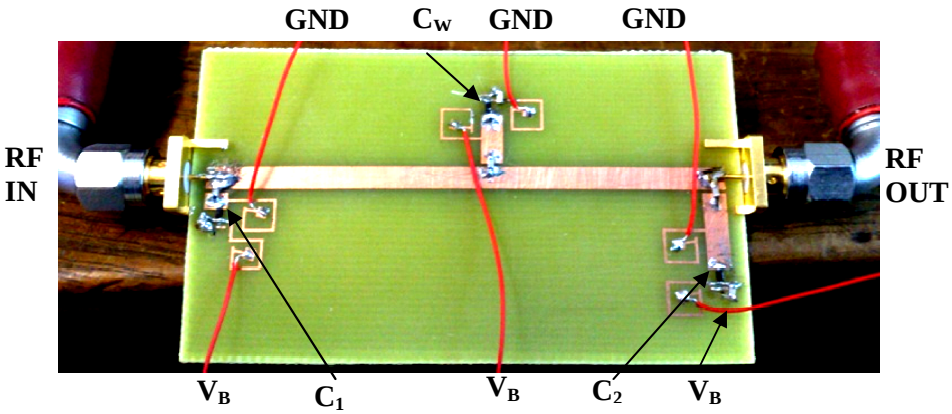
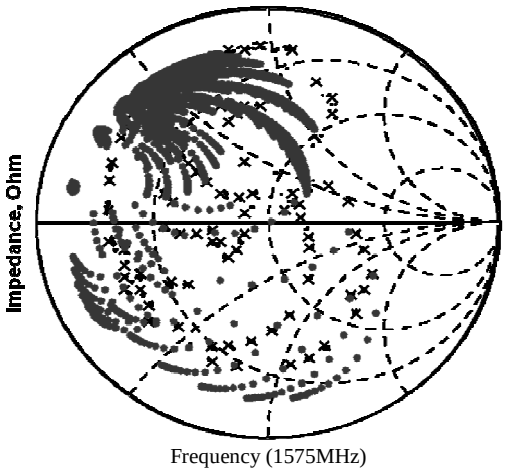
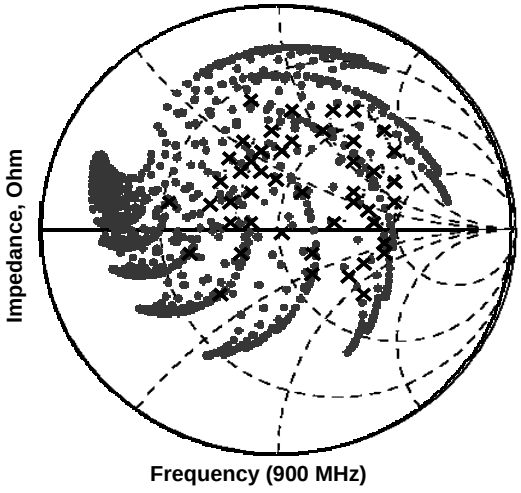


Figure 4.16: The fabricated $\Delta\lambda$ reconfigurable *Pi*-network to achieve high impedance coverage at multi frequency standards

The impedance network was tested using a network analyzer (HP 8753A). The impedance coverage for three operating frequencies were measured and compared with the simulated results, as shown in Figure 4.17. Even with the limited capacitance range available from the tuning components, a wide tuning range for different frequencies are achieved through adjusting the electrical distance. A good agreement between the measurement and the simulation results is found. The measured impedance coverage is slightly reduced compared to the simulations because of the losses of the transmission line, resolution of the tuning components and the handling processes. The uneven distribution of the impedance coverage in the Smith chart is because of the hyper-abrupt junction tuning varactors, which have a low and inconsistent tuning resolution across the tuning range. The insertion loss of the tuner is about 2 dB as shown in Figure 4.18. The slightly high insertion loss is because of the low quality factor and limited tuning values available in the semiconductor hyper-abrupt junction tuning varactors.



(a)



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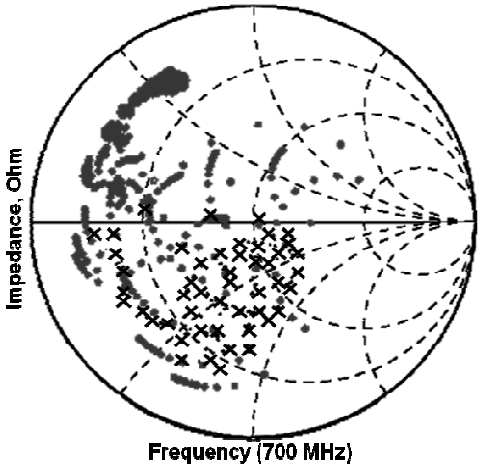


(c)

Figure 4.17: Simulated (O) and measured (X) range of impedance coverage at (a) GPS (1575 MHz) (b) GSM (900 MHz), and (c) LTE (700 MHz)

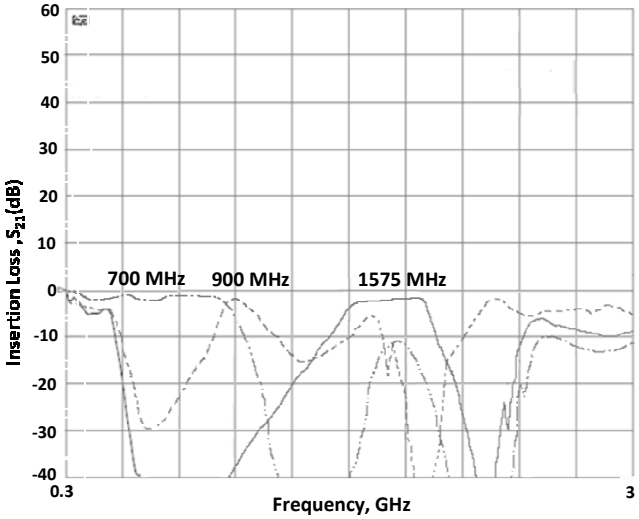


Figure 4.18: Insertion loss of the *Pi*-network at 1575 MHz, 900 MHz and 700 MHz

4.9 Discussions

Employing a large number of RF switches improves the impedance coverage, as demonstrated in pervious research works. However, complexity of the biasing circuit and losses in the system are proportional to the number of RF switches in the impedance network. A large number of RF switches increases losses and size to the systems. Thus, an impedance network with a reduced number of RF switches is proposed.

By identifying the $\Delta\lambda$ for maximum impedance coverage, the impedance network achieves a wide impedance tuning region in the Smith chart. To maintain the $\Delta\lambda$ for maximum impedance coverage at different operating frequencies, the design technique is proposed which is based on adding a T-network as an approximate conversion of a short lossless transmission line to the impedance network. To cover a larger range of frequency standards, multiple T-networks may be used to give a more accurate result. The series transmission line at the T-network could be replaced by two J-inverters and a tunable capacitor [55, 122] as an approximation for a tunable inductor or an electronically tunable transmission line. This makes the prototype exactly similar to the proposed structure, further improving the impedance coverage. The coverage of impedance matching can also be further improved by using a higher range of tuning components.

The proposed technique is not limited to the presented topology and operating frequencies. By using a similar procedure as described, more frequency standards could be covered in a single impedance network, significantly reducing the number of RF switches in the impedance network.

Introducing tunability to the RF front-end provides great benefits but carries also losses in the impedance network. Commercially available varactor diodes have been used as the tuning elements in the prototype to validate the design approach. The drawback with varactor diodes is the effect it has on the overall losses with the structure – where the tuning range is the most, the losses are larger [4]. The impedance network consists of series and parallel elements such as varactor diode itself, DC blocking capacitors, substrate resistance, wire bonding/soldering. For parallel elements of the impedance network, the loss equals the ratio between its parallel element's susceptance and load conductance, and for series elements, it equals the ratio between its series element's reactance and load resistance. To achieve minimum insertion loss, the susceptance of the parallel elements and the reactance of the series elements must be small. Hence, the insertion loss can be improved by selecting the desired impedance transformation trajectories, as well as on the component values used to achieve that transformation [28, 165].

4.10 Summary

Topologies of microstrip-based impedance networks have been discussed in this chapter. These include λ/4 transmission lines and continuously tapered lines for real impedance matching; for complex impedance matching, they have matching stub- and lumped elements-based impedance networks. A technique to transform between the matching stub and the lumped elements through Richard's transformation has also been presented, in order to reduce the size and losses in the impedance network. Technologies of RF switches have been analysed and broadly divided into semiconductor, Barium Strontium Titanate (BST) and Micro Electro-Mechanical Systems (MEMS). The properties of the RF switches are compared in terms of losses, tuning range and RF performance. RF performance depends on the technology considered; tuning range can be increased at the expense of a large number of RF switches, which increase losses and design complexity. For this reason, a design technique has been proposed in order to reduce the number of RF switches through identifying the electrical distance for the maximum impedance coverage. Through reconfiguring the electrical distance, the maximum impedance coverage has been achieved at multi-operating frequencies. The proposed technique has been verified by both simulations and real measurements. Figure 4.19 summarises the areas and the challenges addressed in this chapter. In the next chapter, multi-band performance in the integrated system based on a tunable impedance network and an antenna will be presented.

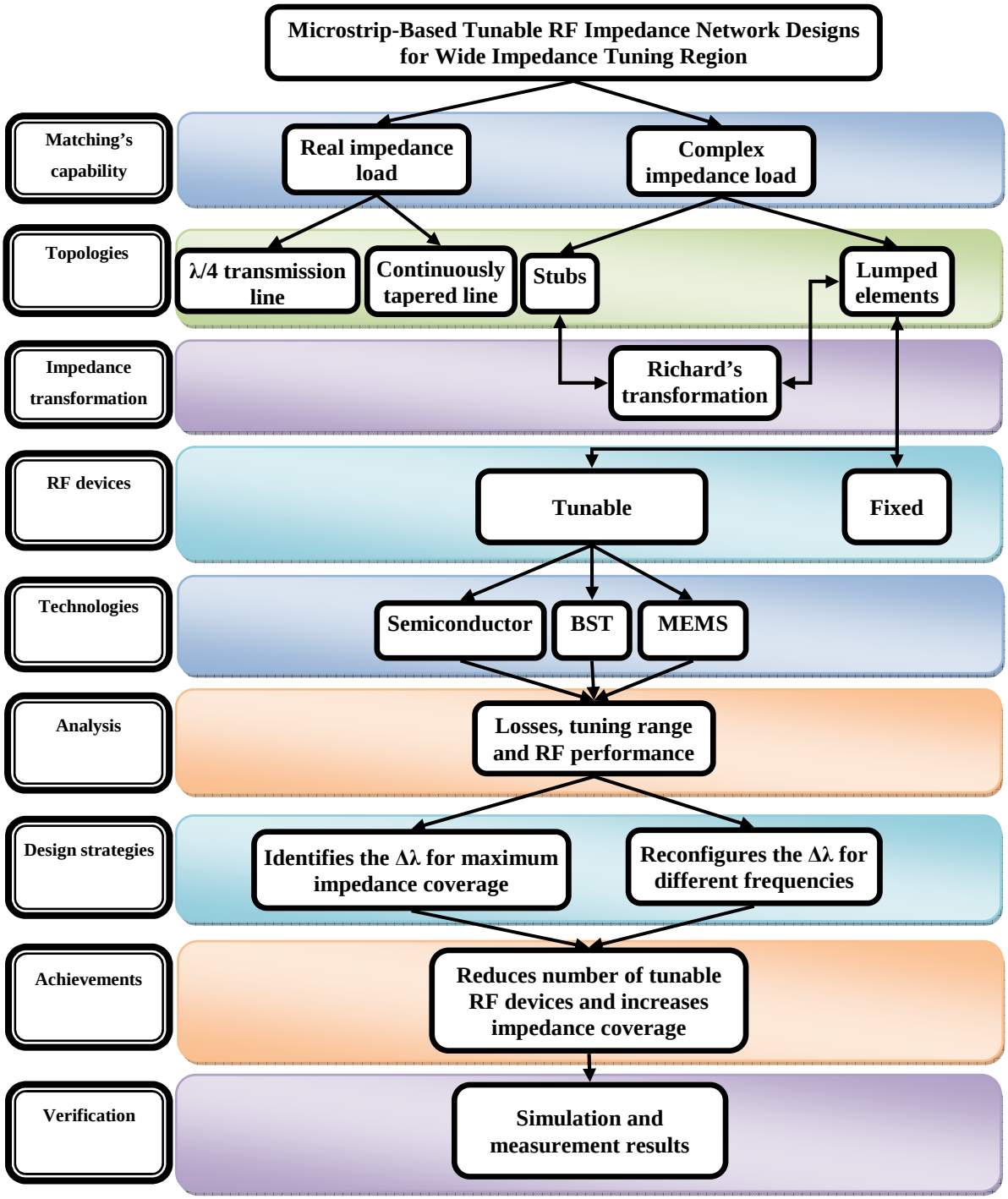


Figure 4.19: Summary of the areas and the challenges addressed in Chapter 4

Chapter 5: Tunable Impedance Network Integrated with an Antenna for Multi-band Wireless Devices

5.1 Introduction

This chapter describes the development and the integration of a wideband impedance network with an antenna for frequency-agility at the RF front-end. The wideband impedance network allows a considerable extension of the operational bandwidth of mobile device antennas. Several methods including a multi-section transmission line, radial stubs and tuning steps are presented in order to increase the operational bandwidth of the impedance network. The presented impedance network is optimised to allow convenient implementation of the necessary dc control lines, RF choke and DC blocking capacitor to control the tuning components. The integrated system re-tunes the antenna's performance after realisation, enabling multi-band performance in the integrated system. It also corrects the antenna impedance mismatch due to manufacturing errors, relaxing the antenna design process.

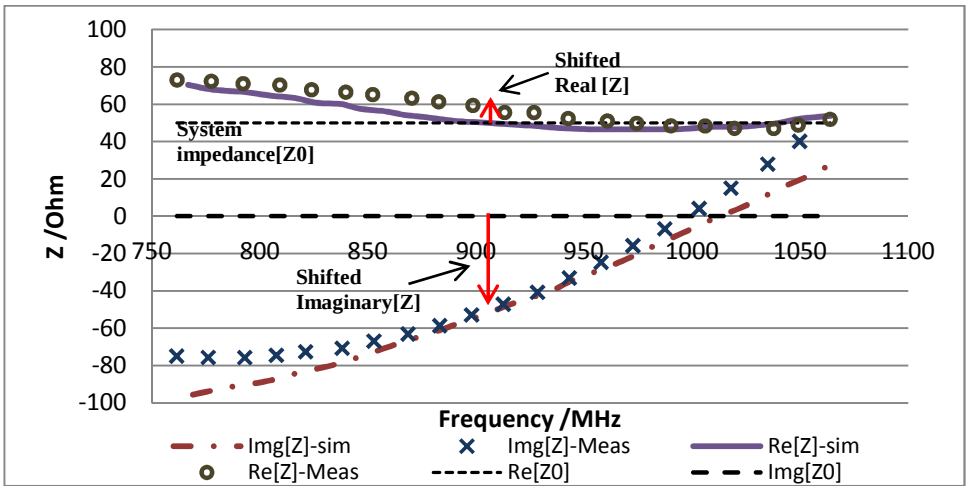
5.2 Antennas for Multi-standard RF Front-end

The bandwidth of an RF front-end is controlled by the input impedance of the antennas or by the impedance matching between devices at the RF front-end. This imposes severe design constraints as the antenna must both be an efficient radiator to free space, yet provide an appropriate impedance match to the RF front-end circuits.

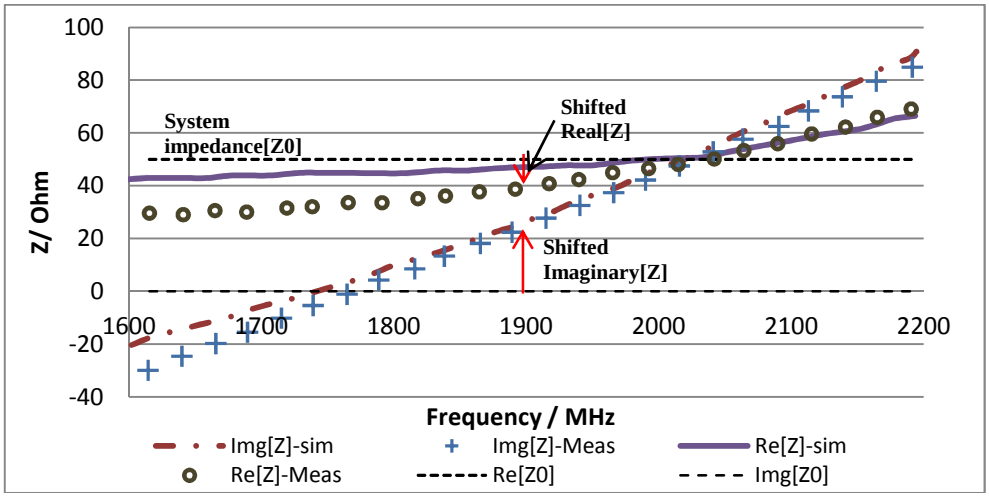
5.2.1 Antenna in Mobile Devices

To achieve a large bandwidth, an electrically large size of antenna tends to be used. However, in mobile telecommunication applications, a small size antenna is preferable with the limited space available. However, a small size antenna has input impedance that is easily detuned by the surrounding objects, due to its narrow bandwidth characteristic [1-3].

For instance, in close proximity to the user, the input impedance of a λ/4 monopole antenna mounted on a mobile phone was shifted to about 10% in the operating frequencies of 914MHz and 1890MHz, as shown in Figure 5.1(a) and (b) respectively [166].



(a)



(b)

Figure 5.1: Effect on a λ/4 monopole antenna in close proximity to the user, causing a shift in the antenna input impedance from its nominal value (Z_0) at (a) 914MHz and (b) 1890MHz operating frequencies [166]

Figure 5.2 compares the performance of the monopole helical antenna in free space and in close proximity to a human phantom [68]. The human phantom is located at a distance of 2.5cm from the antenna. The impedance of the antenna was changed significantly by the human phantom, changing the resonant frequency of the antenna away from the desired frequency of 160MHz. The VSWR was increased from 1 to about 6.

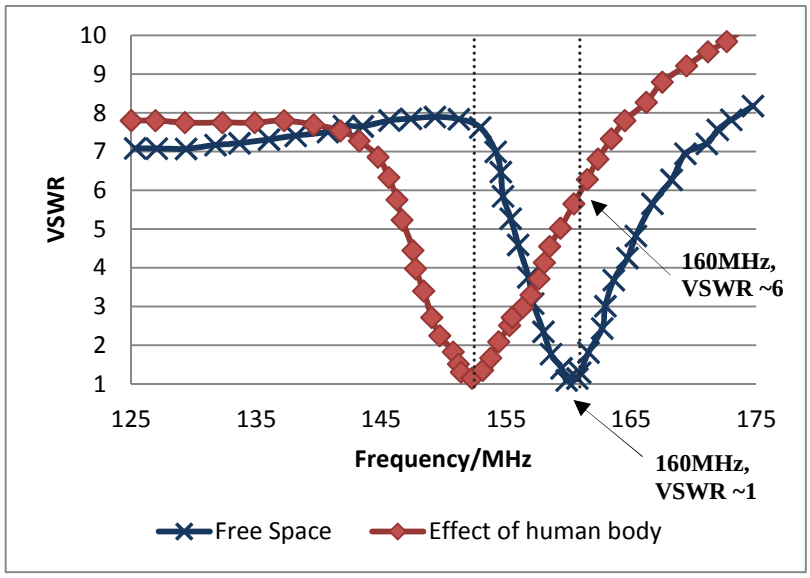


Figure 5.2: Effect of a monopole helical antenna in close proximity to the human body, causing a change in the resonant frequency of the antenna away from the desired frequency at 160MHz [68]

The performance of the antenna is also affected by surrounding objects. Figure 5.3 shows S_{11} of a microstrip patch antenna in free space and in close proximity with a metal sheet [167]. The effect of the metal plate severely disturbs the antenna performance. The resonant frequency was increased by 30MHz from 1516MHz to 1546MHz and the reflected power was increased as much as 13dB, from -14dB to -1dB, at the original resonant frequency (1516MHz).

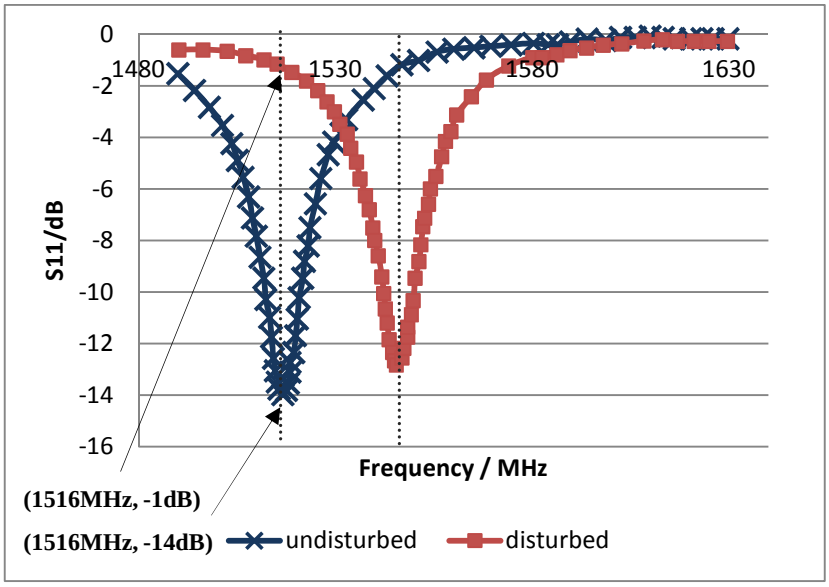


Figure 5.3: Effect of a microstrip patch antenna in close proximity with a metal sheet shifts the resonant frequency of the antenna and increases the reflected power [167]

5.2.2 Design of Wideband Antennas by using Switchable Impedance Networks

Small size antennas are bandwidth limited, while wideband antennas are typically electrically large. An alternate solution is integrating the small size antenna with an impedance network to achieve wide bandwidth performance. Some realisations in designing wideband antennas using switchable impedance networks have been published, but not many. In [16], a switchable impedance network was used to achieve four discrete frequencies from 470MHz to 770MHz for a meandered monopole antenna. In [124], a short dipole antenna with a frequency range from 250MHz to 400MHz was achieved by using a fixed impedance network. A switchable impedance network has also been proposed in [14], corresponding to different working modes of the mobile communication terminal. However, both fixed and switchable impedance networks achieve limited tuning steps and cannot further optimise the performance of the antenna after realisation. Substantial impedance variations might happen because of manufacturing errors, handling uncertainty or even during operating conditions.

To achieve a multi-band RF front-end system, a tunable impedance network is one of the preferable solutions [7, 26-29]. The tunable impedance network is integrated with the antenna to achieve a good return loss for a wide range of operating frequencies; the integrated system is also able to cater for mismatches of the antenna impedance due to the interference with other RF devices or in user-operating environments. Thus, this increases the capability of the RF front-end and improves the link quality by reducing the user's impact on the antenna.

5.3 Design of a Wide Bandwidth Frequency-Agility Impedance Network

To achieve a wide bandwidth impedance network, the design can be based on a multi-section transmission line, matching stub and tuning trajectory, which are discussed as follows.

5.3.1 Multi-section Transmission Line

The bandwidth of an impedance network can be visualised by the Q-factor circle. Figure 5.4 shows the Q-factor circles on the Smith chart. The higher the impedance mismatch level, the bigger the Q-factor circle to be matched. However, to match the high impedance mismatch which has a high Q-factor, the bandwidth of an impedance network becomes narrow. Thus, to maintain the large bandwidth of the impedance network, multiple sections of transmission lines can be cascaded in order to reduce the overall Q-factor to be matched.

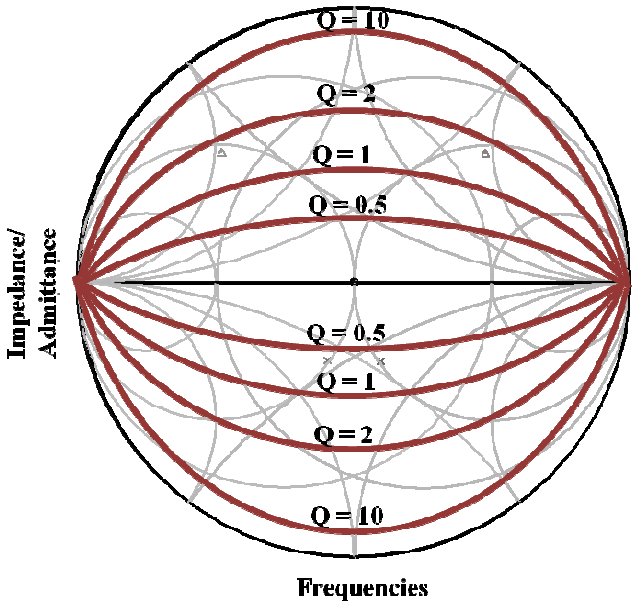


Figure 5.4: Bandwidth of the impedance network depends on the level of mismatch load and could be estimated by constant-Q lines on the Smith chart

For instance, to match a highly mismatched load (9.9+j14)Ω back to system impedance 50Ω, a *Pi*-network could be used, as shown in Figure 5.5(a). The single *Pi*-network with two RF switches achieves a minimum Q-factor of 0.6, as shown in Figure 5.6. The overall Q-factor could be reduced from 0.6 to 0.4 by using two sections of *Pi*-network, as shown in Figure 5.5(b). Thus, by cascading multiple sections of impedance networks, a lower Q-factor and a wider bandwidth can be achieved.

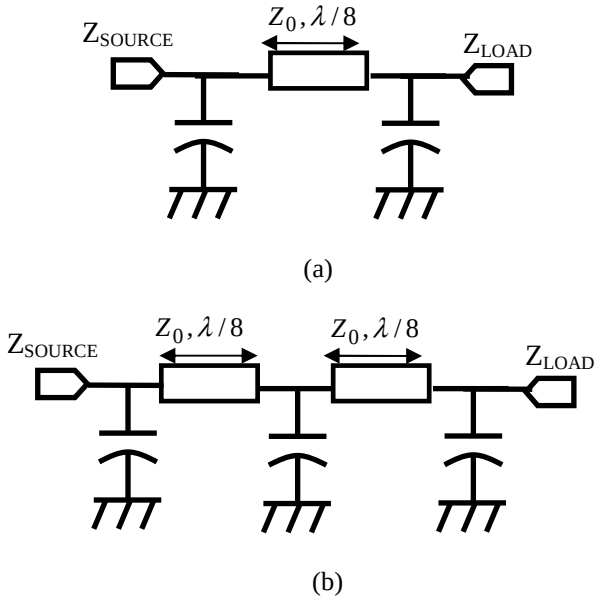


Figure 5.5: Impedance networks based on (a) a single *Pi*-network, and (b) two *Pi*-networks

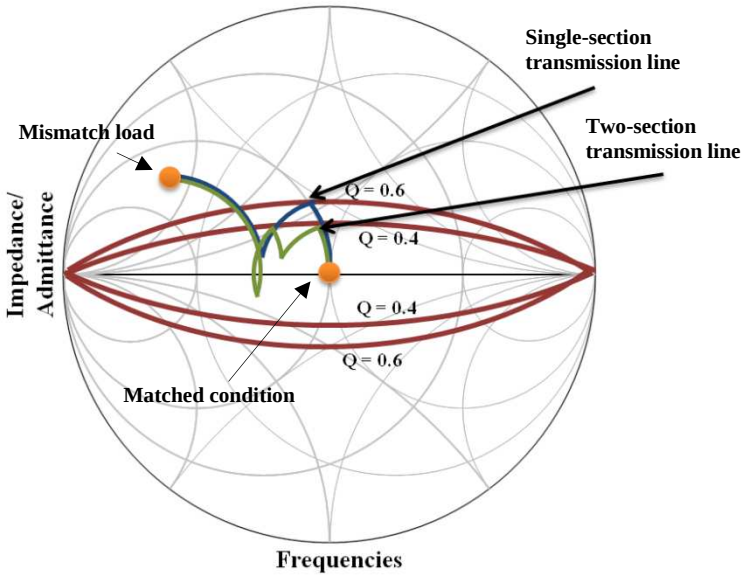


Figure 5.6: The impedance network based on two *Pi*-networks achieves a smaller Q factor (Q = 0.4) compared to a single *Pi*-network (Q = 0.6)

5.3.2 Radial Stub

A microstrip λ/4 linear stub, either short- or open-circuited, can be used to achieve impedance transformation. A short-circuited stub requires grounding the stub to the substrate through a via hole, which creates difficulties in fabrication. By having an additional λ/4 wavelength, a short-circuited stub can be realised by an open-circuited stub, but it provides a narrow bandwidth characteristic. In order to have a wider bandwidth, a radial stub is used in place of a linear stub. The bandwidth of the radial stub depends on the physical width of the stub. At the connection point, the width of the radial stub should be small; whilst at the open end, the width of the radial stub should be wide. A round shape should be given at the open end to reduce charge accumulating at the rectangular corner. Moreover, when cascaded with high impedance quarter-wavelength transmission lines, the radial stub can provide an effective decoupling network for other RF active components. Procedures for designing the radial stub can be found in [168, 169].

The radial stub has a broader bandwidth to tolerate fabrication errors but it occupies a larger board area, especially at lower frequencies. In this work, to reduce the board area, a zigzag linear stub is used to connect to a radial stub. The zigzag radial stub was optimised by considering the physical dimensions, the parasitic effects of biasing circuits, and the tuning components. The opening angle of the radial stub has also been reduced from 90^0 to 30^0. The radial stub with 30^0 opening angle achieves smaller area compared to radial stubs and wider bandwidth compared to linear stub, as shown in Figure 5.7 (ideal case).

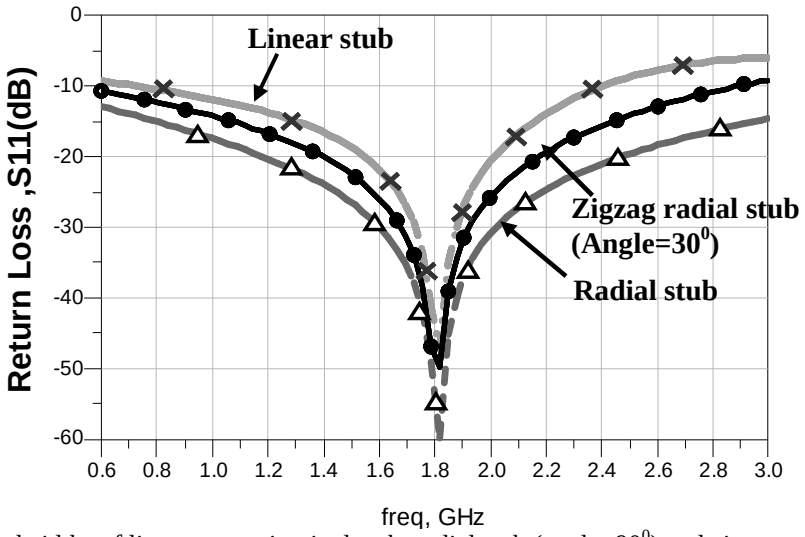


Figure 5.7: Bandwidths of linear open-circuited stub, radial stub (angle=90^0) and zigzag radial stub (angle=30^0)

The impedance network is targeted to a wide bandwidth, in particular for three operating frequencies, i.e. LTE (700 MHz), GSM (1.8 GHz), and WIFI (2.45 GHz). The RF switches are integrated with the zigzag radial stubs. With the electrical tunable stubs, increasing the reverse bias voltage leads to a decrease in the capacitance (*C*) in RF switches, effectively shortening the stub length (*L*) and changing the effective impedance of the stub, as shown in (5.1)[119].

$$L = [\frac{1}{2\pi} \arctan(2\pi . f . C . Z_0)] . \lambda \tag{5.1}$$

where *L* is the length of the stub, *C* is the capacitance in RF switches and Z_0 is the nominal system impedance

Simulations have been performed using Advanced Design Systems (ADS 2009) based on a 1.6 mm-FR4 substrate with a dielectric constant of 4.55. By varying the RF switches from 2pF to 16pF, it enables compensating a change in frequency caused by the impedance mismatch either due to a poor fabrication process or under user-operating fluctuating conditions, as shown in Figure 5.8. With the limited tuning range (2pF to 16pF), the impedance network covers tuning regions of $20\Omega<R_{LOAD}<80\Omega$ and $-150\Omega< X_{LOAD}<150\Omega$ for GSM and WIFI operating standards, and $40\Omega<R_{LOAD}<80\Omega$ and $-50\Omega <X_{LOAD}<50\ \Omega$ for LTE standard. The coverage of impedance matching can be further improved by using a higher tuning ratio of RF switches.

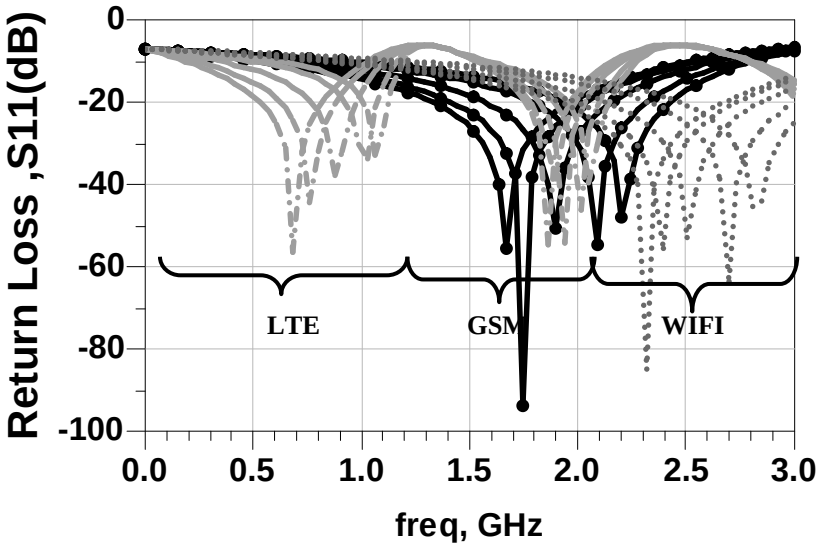
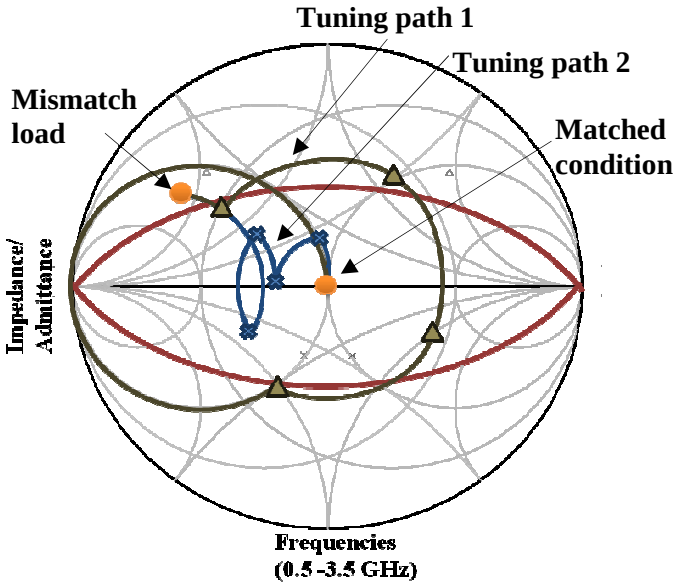


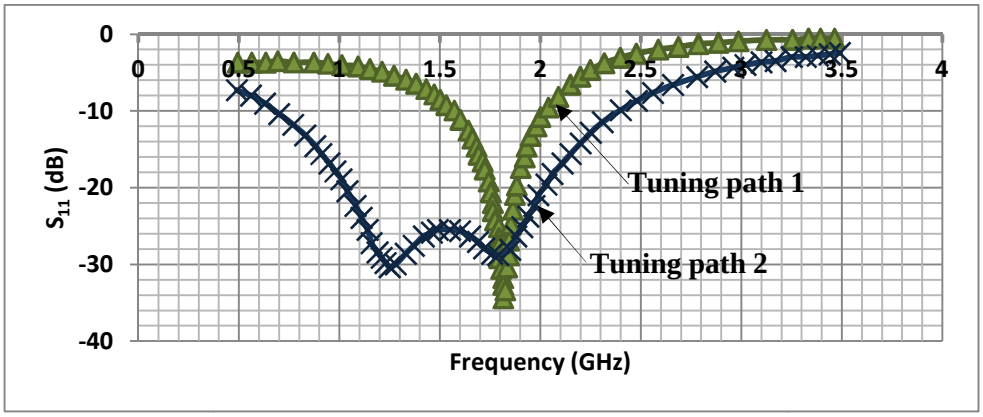
Figure 5.8: Frequency agility of the impedance network at LTE, GSM and WIFI

5.3.3 Tuning Trajectory

Proper tuning steps also increase the impedance network's bandwidth. Figure 5.9(a) shows two different trajectories in the Smith chart for tuning a mismatch load back to 50Ω (centre of the Smith chart). The bandwidths of the tuning network with two sets of tuning trajectories are illustrated in a linear graph, as shown in Figure 5.9(b). The closer the impedance tuning trajectory comes to the edge of the Smith chart, the narrower the bandwidth. Maximum bandwidth for a given impedance network can be obtained by keeping the trajectories short and away from the edges of the Smith chart. In addition, the trajectories of the impedance network should be close to the real axis of the Smith chart and inside of the lower Q regions.



(a)



(b)

Figure 5.9: The matching network with (a) the trajectories of impedance network in a Smith chart and (b) the corresponding return loss

5.4 Optimization and Implementation

The design of the impedance network is referred to as the 50-50 design since the source and the antenna load impedance (Z_L) are both set to 50Ω. The impedances of the radial stubs and the interconnection lines are determined based on the frequencies of interest. To convert the design to microstrip layout, the design is modified to account for the added varactor capacitance. Eventually, the design is optimised to obtain the final lengths and widths for all sections of the impedance network. Practical parameters such as microstrip vias, pads of the varactor, gap, etc. are included in the optimisation process.

5.4.1 Layout of the Wideband Impedance Network

The geometry of the proposed microstrip impedance network is shown in Figure 5.10. The layout of the impedance network is etched on a sheet of FR-4 printed circuit board (thickness, h=1.6mm and relative dielectric constant, ε_r = 4.3).

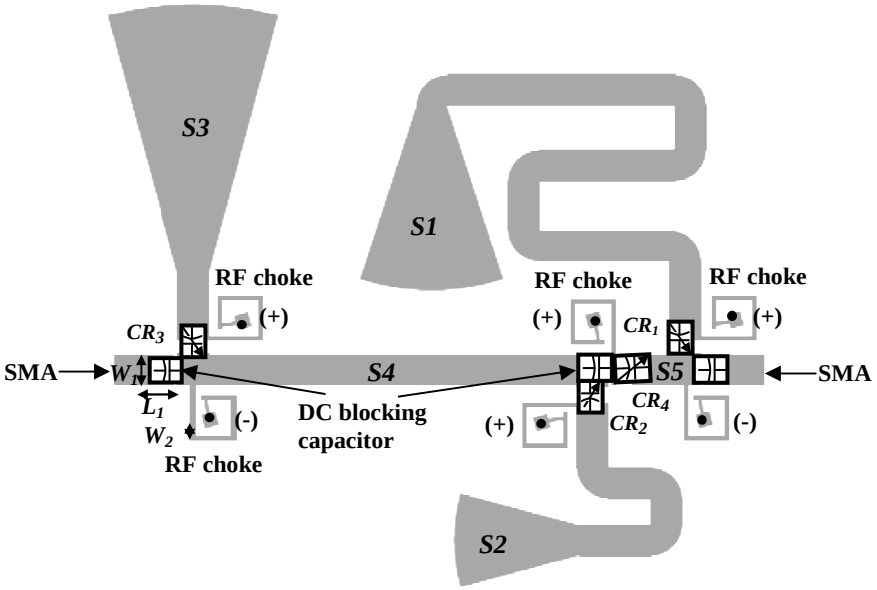


Figure 5.10: Layout of the impedance network for LTE, GSM and WIFI operating standards

Three radial stubs (*S1*, *S2* and *S3*) are designed based on their respective operating frequencies at LTE, GSM and WIFI to allow for the matching at 700 MHz, 1.8 GHz and 2.45 GHz frequencies. The length and the width of the insets are determined by the size of the semiconductor varactor (W_1 x L_1). To control the operating frequency of the impedance

network, three varactors (CR_1, CR_2 and CR_3) are inserted between the branches of the radial stubs and the main transmission line. The fourth varactor (C$R4$) is inserted at the main transmission line to adjust the electrical length of the impedance network.

5.4.2 Controlling the RF Switches

Semiconductor varactors are used in this work as they are low cost and available in the market. Skyworks hyper-abrupt junction tuning varactors have been used in this work [159]. To control the varactor, six dc biasing circuits are designed. The biasing circuit consists of dc blocking capacitors and RF chokes, as shown in Figure 5.11. For the varactor in on-state ($V_F>0V$), the equivalent circuit is represented by a variable capacitor and a parasitic resistor, R=3Ω, while for the varactor in off-state ($V_F=0V$), the equivalent circuit is represented by a parasitic capacitor, C=0.64pF.

Four biasing lines are used for supplying dc forward biasing voltages (V_F) to varactor 1, 2, 3 and 4. Two dc grounding lines are connected to each stub (*S4* and *S5*), which drains the dc current from the varactor 1, 2, 3 and 4 to ground.

Three dc blocking capacitors of C=220pF are chosen to isolate the dc current from RF paths. This value of dc blocking capacitor represents a “near short circuit” condition in RF operating environment. For instance, the impedance value of the blocking capacitor at 700MHz is Z_C = -j(1/wC) = -j1Ω, whereas at 2.45GHz is Z_C = -j0.29Ω. Thus, RF signals are able to pass through the dc blocking capacitors with little loss or nearly no reflection.

The RF choke inductor isolates RF signals from flowing into the dc path, therefore, a very thin but within fabrication resolution (W_2 = *0.4 mm*, $L=\lambda/4$) square spiral microstrip inductor was used. By using this microstrip printed inductor, the use of bulky off-chip RF choke inductors can be eliminated. At the end of the quarter-wavelength in the square spiral inductor, a dc forward biasing voltage (V_F) is connected for controlling the varactor. The V_F varies from *0V* to *8V*, supplying capacitance proportional from 37pF to 0.6pF.

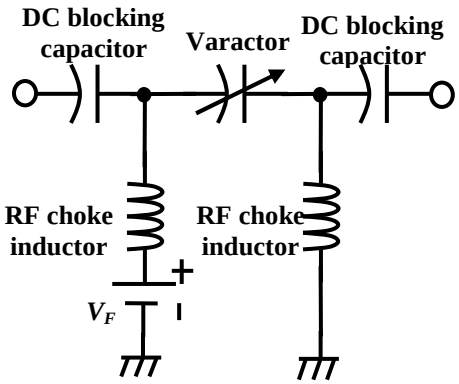


Figure 5.11: The configuration in semiconductor based varactor biasing circuit

5.5 Verification

The photograph of the prototype impedance network, fabricated on a FR-4 with a dielectric constant of 4.3 and the thickness of 1.6mm, is shown in Figure 5.12. Commercially available hyper abrupt junction tuning varactors were used as the tuning elements [164].

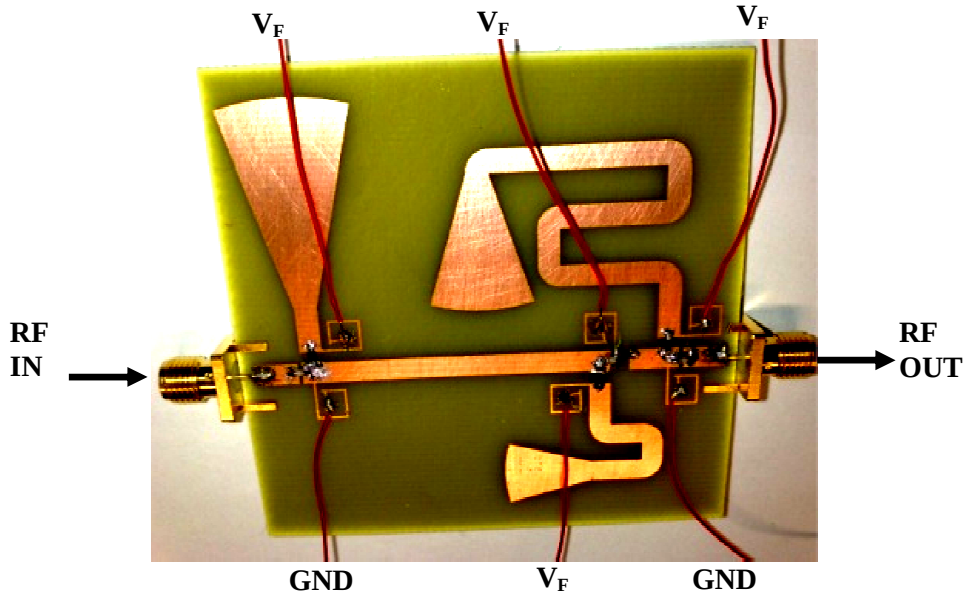
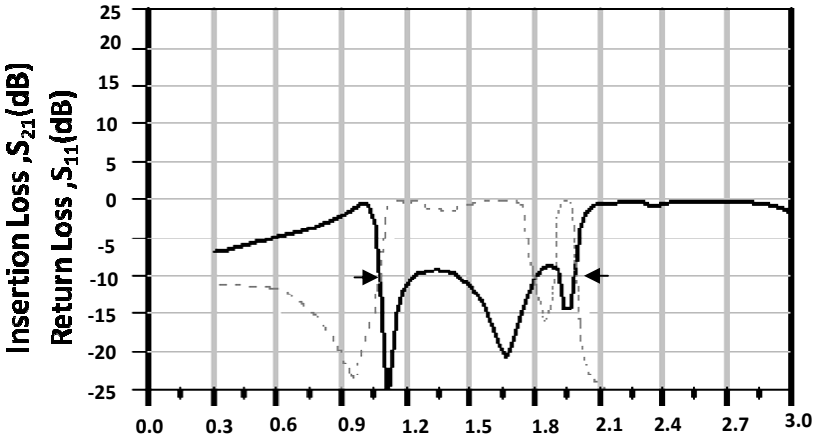
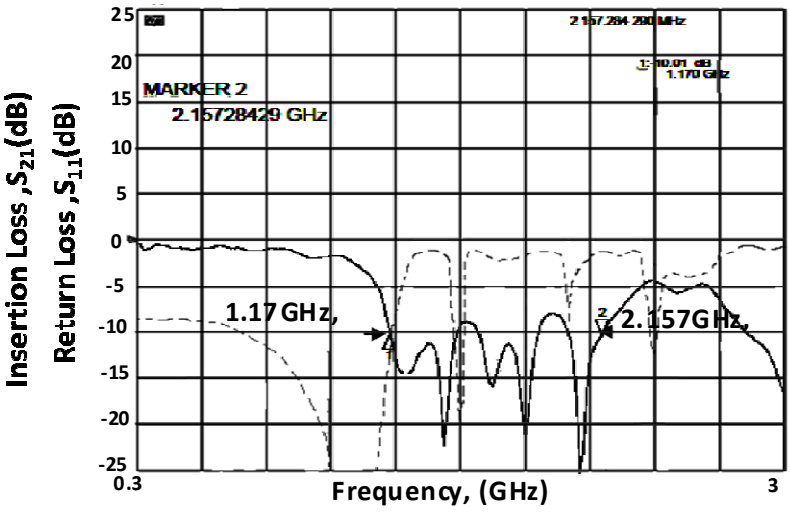


Figure 5.12: Prototype of the impedance network with frequency-reconfigurable capability

The prototype was tested using a network analyzer (HP 8753A). The measurement result of the impedance network exhibits a wide bandwidth (>1GHz) as presented in Figure 5.13. The insertion loss of the tuner is about 2 dB. The slightly high insertion loss is because of the tuning elements - hyper-abrupt junction tuning varactors which have a low and inconsistent tuning resolution across the tuning range. The tuning values in the varactor change in exponential rather than linear form. Thus, not all the tuning value is available for the desired optimum performance. A slight discrepancy between the measurement and the simulation is due to the handling of the power supply wires, which are not considered during the design and optimization stages.



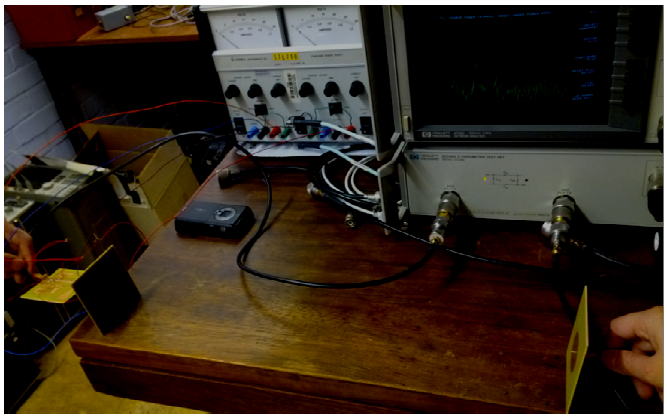
(a)



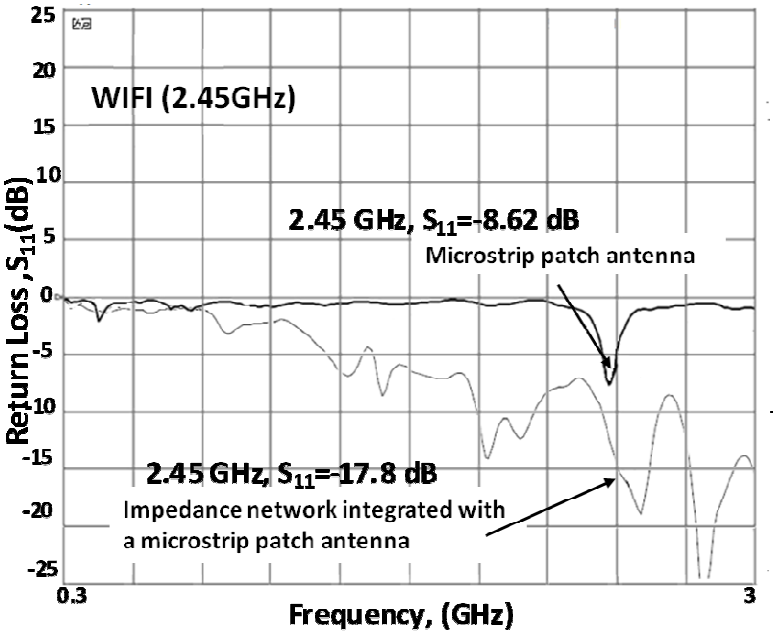
(b)

Figure 5.13: Results of the wideband impedance network in (a) simulation and (b) measurement

In this experiment, the frequency responses of antenna with and without matching network have been demonstrated, as shown in Figure 5.14(a). Two identical microstrip circular patch antennas with operating frequency of 2.45GHz have been used in this experiment. Two antennas have been set apart at a fixed distance. Measurement results have been captured for antenna with and without matching network, as shown in Figure 5.14(b). By using the impedance network, a better return loss of 18dB is achieved at 2.45GHz compared to the original 9dB. Integration of the impedance network with the antenna significantly increases the bandwidth to more than 1000MHz, from the original bandwidth of 250MHz, by having S11 most of the time below -10dB, as shown in Figure 5.14(b).



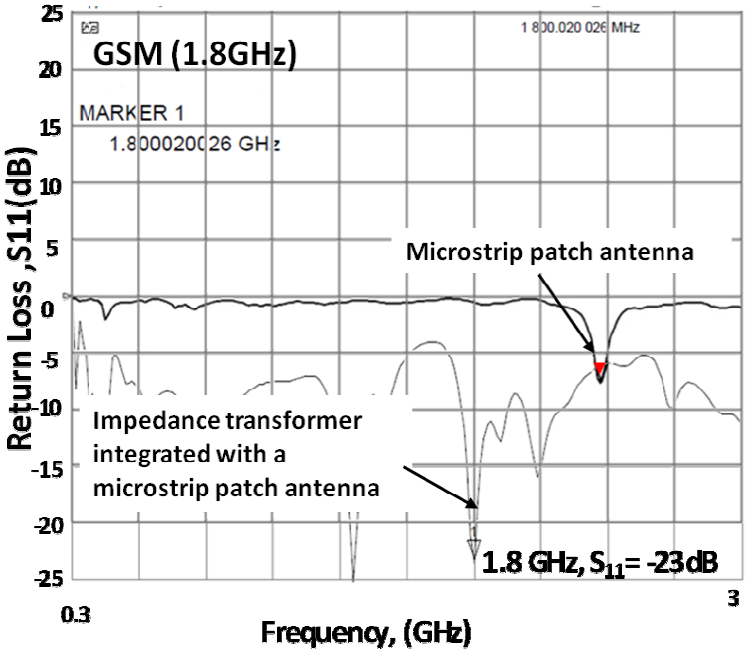
(a)



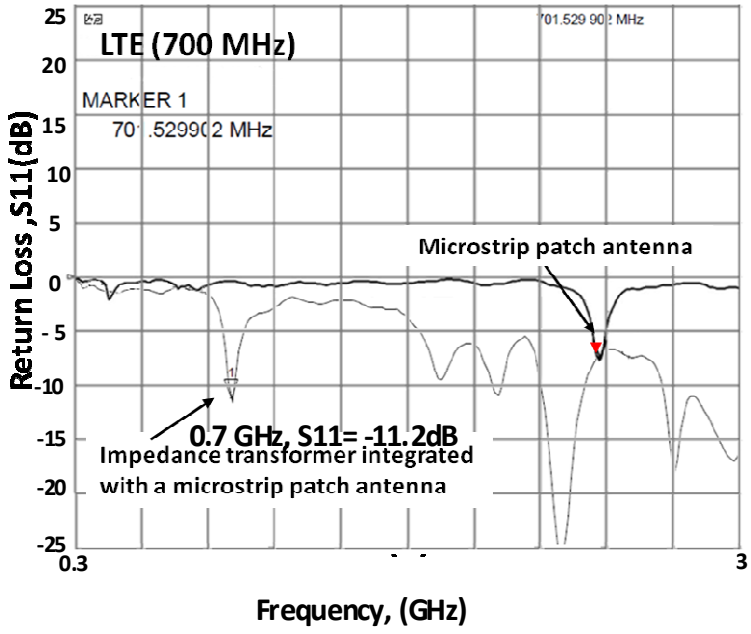
(b)

Figure 5.14: Integrated system of the impedance network with a simple microstrip antenna in (a) experimental setup and (b) measurement result at 2.45GHz

Integration of the antenna with the impedance network enables it to operate in ultra wideband frequencies, from 2.45GHz, 1.8GHz to 700MHz, as shown in Figure 5.15(a) and (b).



(a)



(b)

Figure 5.15: Measured results of the integrated system at (a) 1.8GHz, and (b) 700 MHz

Due to the limited experimental setup, the transmission responses of the antennas with and without the impedance network have only been demonstrated at operating frequency of 2.45GHz. The experiment was deliberately tested the integrated system at the highest design frequency to capture the highest losses in the impedance network. From the experiment, even though the impedance network carries losses to the integrated system, it still improves the transmission response in overall as shown in Figure 5.16.

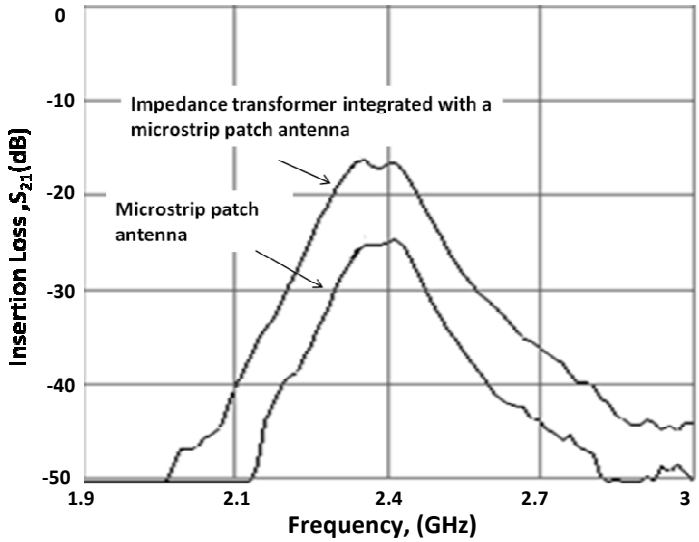


Figure 5.16: Insertion loss of the antenna and the integrated system

5.6 Discussions

Smaller bandwidths are achieved for frequencies other than 2.45GHz. For instance, the integrated design has return losses of 23dB at 1.8GHz and 11dB at 700MHz. This is due to the impedance of the antenna that deviates from 50Ω at frequencies other than the primary design frequency (2.45GHz). A better performance of the integrated design can be achieved by using a measured input impedance of the antenna rather than the 50-50 design in developing the impedance network.

Insertion loss is defined as a ratio between dissipated power in the matching network and power delivered to the load [165]. For parallel elements of the impedance network, this power ratio equals the ratio between its loss and load conductance, and for series elements, it equals the ratio between its loss and load resistance. The losses are contributed by equivalent series resistance in the varactors, DC blocking capacitors, substrate resistance, wire

bonding/soldering and etc.. To achieve minimum insertion loss, the susceptance of the parallel elements and the reactance of the series elements must be small. Hence, the insertion loss can be improved by selecting the desired impedance transformation trajectories, as well as on the component values used to achieve that transformation [28].

5.7 Summary

An integrated system to achieve multi-frequency standards in a single RF front-end has been presented in this chapter. The integrated system is based on a tunable wide bandwidth impedance network integrated with a simple antenna. The tunable wideband impedance network has been designed based on zigzag radial stubs, which have a smaller area compared to radial stubs and a wider bandwidth compared to linear stubs. The tuning of the impedance network increases the bandwidth by using the shortest trajectories within the lower Q circles in the Smith chart. Integration of the tunable impedance network with a simple patch antenna significantly improves the antenna's bandwidth up to 1GHz (4 times original) and achieves a better return loss of 18dB. Furthermore, the design operates for frequencies ranging from 700MHz to 3GHz, covering most of the widely used mobile telecommunication operating frequencies. The results demonstrate that many different frequency standards could be achieved in one circuit. This avoids multiple mode-specific transceiver units for different standards on a single device. Figure 5.17 summarises the areas and the challenges addressed in this chapter. In the next chapter, adaptive algorithms to search for the required impedance state at the RF switches in the impedance network, based on different degrees of impedance mismatch, will be presented.

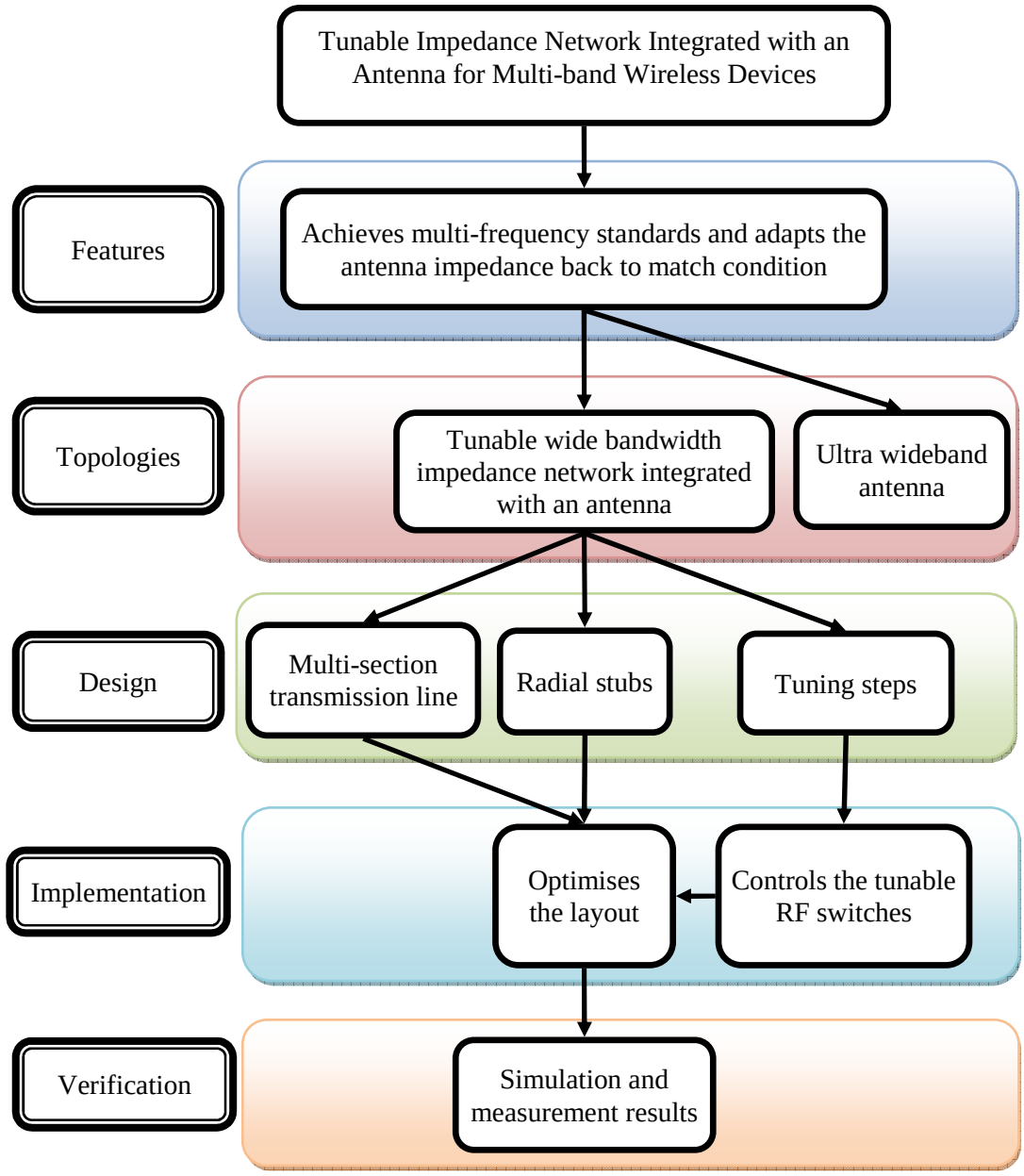


Figure 5.17: Summary of the areas and the challenges addressed in Chapter 5

Chapter 6: Adaptive Algorithms for Tunable RF Impedance Networks

6.1 Introduction

Impedance network designs for impedance transformation of RF switches to improve antenna performance and achieve multi frequency standards have been presented in Chapter 5. This chapter presents adaptive algorithms to determine the required tuning stage at the RF switches based on different levels of antenna impedance mismatch. It is highly desirable to reduce the search time in order to minimise the risk of data loss during the impedance tuning process. Existing algorithms are either difficult to reach convergence for a complex number or exhibit high computational resources which are intolerable for mobile applications. Presented here is a novel technique to reduce the search time by more than an order of magnitude by exploiting the relationships among the mass spring's coefficient values derived from the matching network parameters, thereby significantly reducing the convergence time of the algorithm. The search area of the algorithm is further reduced by the proposed adaptive boundary technique, achieving a faster convergence rate and higher impedance coverage.

6.2 Adaptive Algorithms

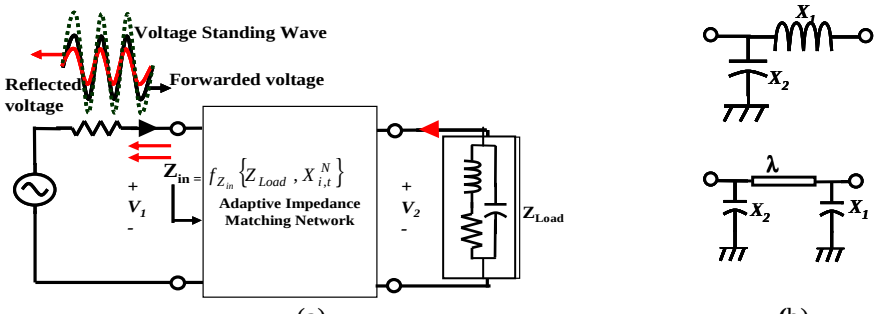
Linear correlation or stochastic methods based adaptive algorithms are commonly used in impedance matching networks [52, 67, 72, 73, 165, 170-174].

6.2.1 Linear Correlation Method

Linear correlation methods, such as least mean square (LMS), were reported to search the antenna impedance [165, 170, 173]. LMS has been used for matching the real [170] or imaginary [165] parts of the antenna impedance. LMS uses a gradient based method of steepest decent, in searching for the matched impedance tuning values. LMS is designed to match either the real or imaginary part of the impedance but not both parts simultaneously due to the non-linear correlation of the RF switches in the impedance networks.

6.2.1.1 Formation of the Susceptance Matrix

The impedance network transforms the impedance of RF switches to a tuning region to compensate the impedance mismatch between the RF front-end and antenna load, as shown in Figure 6.1a. Tuneable impedance networks are mostly based on *LC*- or *Pi*-networks, as shown in Figure 6.1b. RF switches (X_i) could be an array of capacitors or inductors. These tunable capacitors or inductors generate the required impedance, as given by (6.1). Depending on the topology of the impedance networks, the impedance transformation of the RF switches can be obtained by applying (6.2) and (6.3) alternately. The equations (6.1) - (6.3) apply to all types of transmission line, including coaxial cable, microstrip and metal waveguides.



(a) (b)

Figure 6.1: Block diagram of an adaptive impedance network (a) impedance network parameters (b) impedance network topologies: *LC*-network and *Pi*-network

$$Z_{Tune[1\ldots N]} = 1/(2*\pi*f*C_{[1\ldots N]}) \text{ or } Z_{Tune[1\ldots N]} = 2*\pi*f*L_{[1\ldots N]} \tag{6.1}$$

$$Z_{TP} = Z_L \,//\, Z_{Tunei} \tag{6.2}$$

$$Z_{TS} = Z_0 \frac{Z_{TP} + j(Z_0 t_i)}{Z_0 + jZ_{TP} t_i} \quad \text{where } t_i = \tan \Delta\lambda_i \tag{6.3}$$

Voltage Standing Wave Ratio (VSWR) is used as a measure of impedance mismatch based on the reflection coefficient (Γ), as shown by (6.4) [119]. The mismatch between the load (Z_{Load}) and the nominal system impedance (Z_0) decides the Γ. By introducing the impedance network, it provides the required impedance for matching the Z_0, thus reducing the Γ. The input impedance of the impedance network (Z_{in}) is a function of the Z_{Load}, the Z_0, the array of N elements RF switches parameters ($X_{i,t}^N$), and the distance between the RF switches in radian (t_i), as illustrated in (6.5). In this work, the Z_{in} is used to determine the level of mismatches in the system, as shown in (6.6). The Γ is a complex number. The magnitude of Γ determines the VSWR, as by (6.7) [119].

$$\Gamma = \frac{Z_{Load} - Z_0}{Z_{Load} + Z_0} \tag{6.4}$$

$$Z_{in} = f\left\{Z_{Load}, X_{i,t}^N, Z_0, t_i\right\} \tag{6.5}$$

$$\Gamma = \frac{f_{Z_{in}}\left\{Z_{Load}, X_{i,t}^N, Z_0, t_i\right\} - Z_0}{f_{Z_{in}}\left\{Z_{Load}, X_{i,t}^N, Z_0, t_i\right\} + Z_0} \tag{6.6}$$

$$VSWR = \frac{1+|\Gamma|}{1-|\Gamma|} \geq 1 \tag{6.7}$$

6.2.1.2 The Process of LMS

The process of LMS is shown in Figure 6.2. The input for the algorithm is based on a combination of impedance detectors such as VSWR detector, phase detector and etc.. The detection of VSWR only provides the levels of mismatch. However, a particular value of VSWR can arise from an infinite number of impedance values. Thus, VSWR information alone does not give sufficient information to select the components for the impedance matching network. An additional of phase detector has to be included in order to obtain the complex impedance value. The impedance load data is an assumption that the complex impedance value can be approximated from the impedance detectors such as VSWR detector and phase detector.

Assuming an impedance detector provides the antenna impedance value (Z_{Load}), the error signal (*e(n)*) is generated by comparing the Z_{in} with the desired system impedance (i.e. 50 Ω). The (*e(n)*) is generated over *n* iterations using (6.8), as plotted in Figure 6.3(a). A smaller *e(n)* is obtained when the real part of Z_{in} moves towards 50Ω while the imaginary part of Z_{in} moves towards zero, as shown in Figure 6.3 (b). Over the iterations, the weight factor (*w*) is updated by *e(n)*, as by (6.9). The *w* calculates the required tuning values at the RF switches. The tuning values need to be properly defined to avoid exceeding its boundary. The step size (μ) of the algorithm is considered with the trade-off in convergence rate and accuracy. For example, by using a large step size of μ leads to fast convergence but less accuracy.

$$e(n) = d(n) - Z_{in}(n) \tag{6.8}$$

$$\vec{w}(n+1) = \vec{w}(n) + \mu.e(n).\vec{u}(n) \tag{6.9}$$

where *e(n)* is the error signal, *d(n)* is the desired impedance, $Z_{in}(n)$ is the input impedance, *w(n)* is the weighting factor and μ is step size

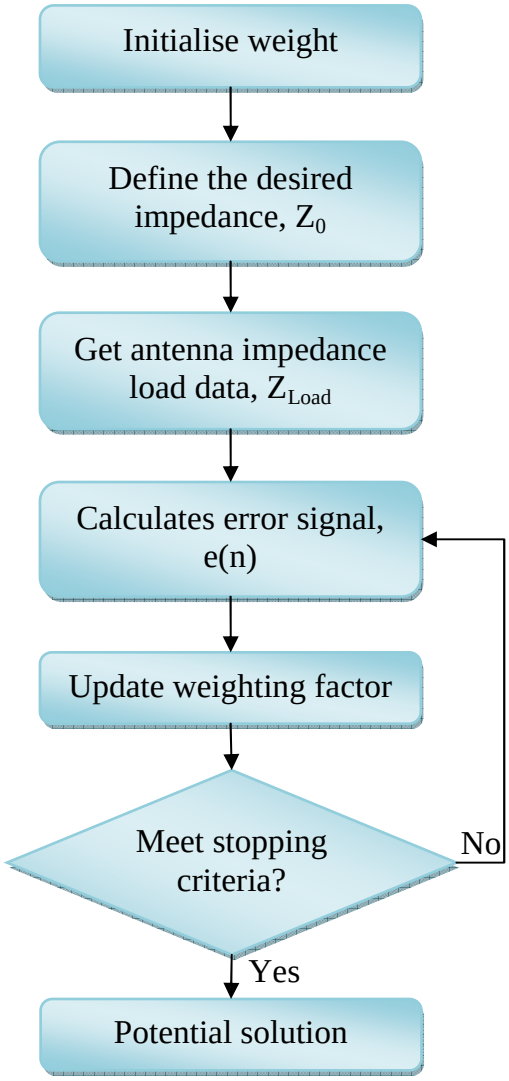
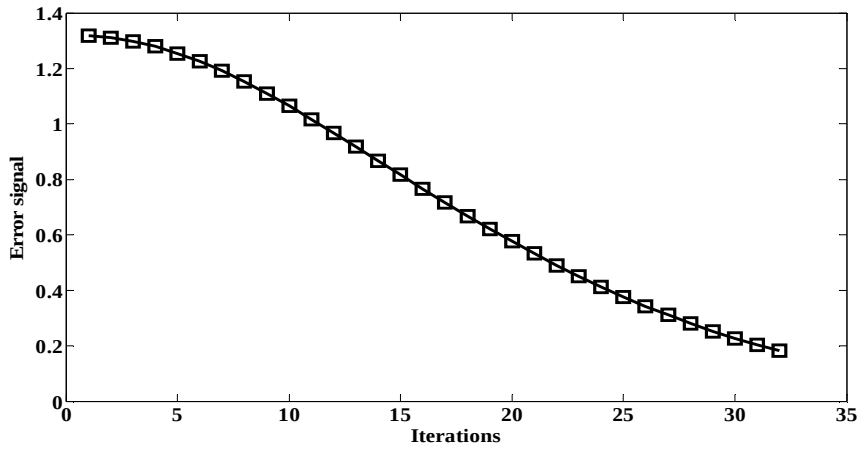
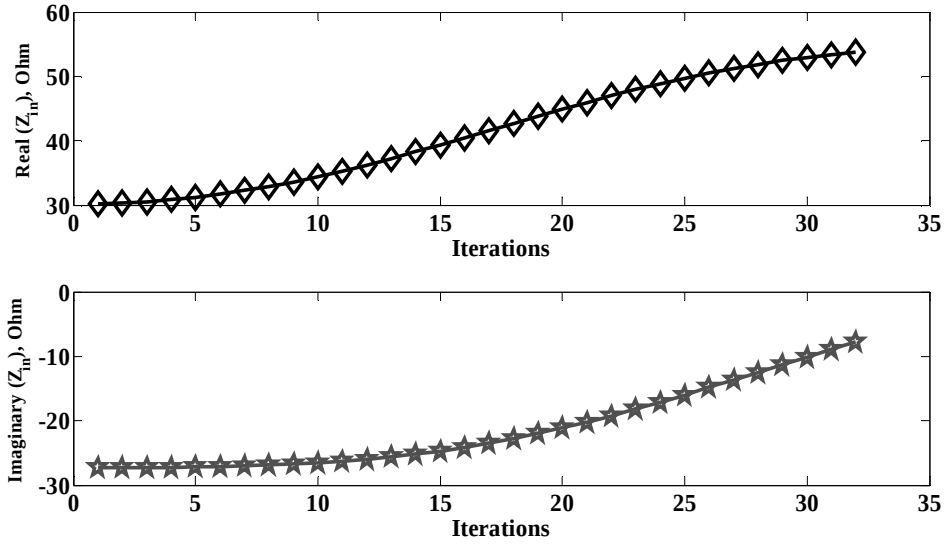


Figure 6.2: LMS process flow



(a)



(b)

Figure 6.3: Convergence of LMS based on (a) error signals and (b) the real and imaginary of input impedances over number of iterations

6.2.1.3 Simulation Results

The effectiveness of the developed adaptive algorithm has been demonstrated for a sample *Pi*-network with two RF switches placed at the electrical distance of 30^0. The mismatch antenna load was assumed having a value of 50+j*15.6. The algorithm stops as soon as the user-defined threshold for *e(n)* is reached (e.g., $|e(n)|<1$) or the maximum number of iterations (i.e., 100) is exceeded. The evaluation criteria of the algorithm could also be the transmitting power or transducer gain [175].

Figure 6.4 shows the Z_{in} before and after applying the algorithm in the Smith chart. Two tuning values are generated (C_1=1.436pF and C_2=5.3851pF) for matching the Z_{in} toward the 50Ω in less than 21ms, as shown in Figure 6.5.

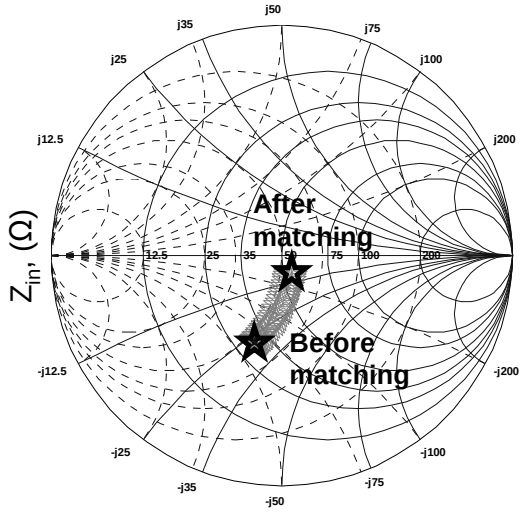


Figure 6.4: Convergence of LMS based on complex impedances in a Smith chart

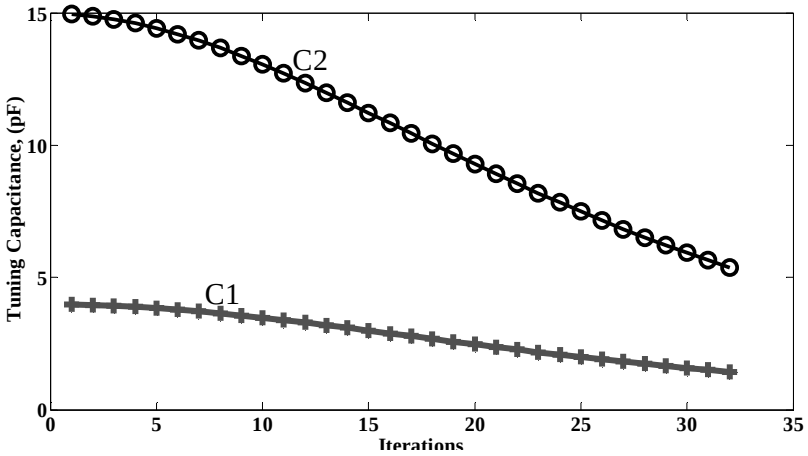


Figure 6.5: Tuning elements C_1 and C_2 over number of iterations

Due to the nature of the highly non-linear correlation in complex impedance, an adaptive impedance network based on LMS algorithm is limited to correct either the real or imaginary part of the Z_{Load}. Furthermore, the linear methods require a large number of tuning steps for a small increment value. In a strong mismatch condition, larger increment values can be used to reduce the convergence time. However, with a larger step size, the algorithm might be trapped at a local optimum or converge to non-optimum solutions.

Recent work in tunable impedance networks has involved a large number of RF switches [58, 144, 162, 163]. For instance, an impedance network based on a single stub with four RF switches on the stub and six RF switches on the transmission line has been used [58], whereas eight RF switches have been used in [162]. Some impedance networks had even been designed using 11 to 12 RF switches [144, 163]. To search potential complex impedance solutions for a large number of RF switches, a random global search method is required.

6.2.2 Stochastic Method

Stochastic methods, such as the Genetic Algorithm (GA) have been proven to be a very powerful search method for many application areas. The GA works on an encoding of the parameter set and searches globally within a population. The GA has learning capability, and does not require function derivatives. They thus fit to the nature of the tuning problem. To correct both real and reactive mismatches, researchers applied a specific GA [67, 72, 73, 171, 174].

The GA uses a stochastic method in searching for matched impedance tuning values. The algorithm mimics the metaphor of natural biological evolution. At each generation, new sets of approximations are created by the process of selecting individuals according to their level of fitness in the problem domain and breeding them together using operators borrowed from natural genetics. This process creates a population of individuals that are better suited to the environment than the population that it was created from, just as in natural adaptation. The process of the GA is presented in Figure 6.6.

Each chromosome would be assigned a fitness value through a customised fitness function. The fitness value drives the selection towards more fit individuals to be mated

together during the reproduction phase. New chromosomes will be produced in the next generation through the GA's operators such as crossover and mutation. Newly generated chromosomes will be evaluated by the fitness function and the process continues through subsequent generations. The average performance of individuals in a population is expected to increase, as good individuals are preserved and bred with one another and the less fit individuals die out.

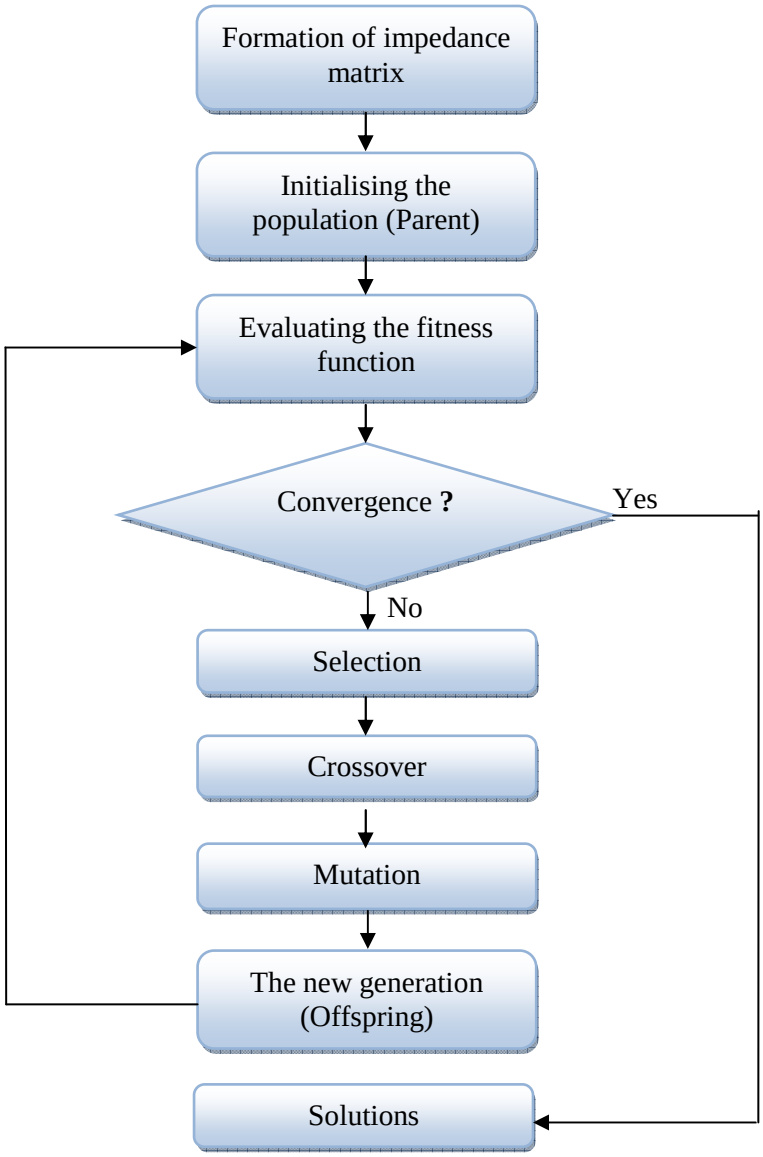


Figure 6.6: GA process flow

6.2.2.1 Population

Before proceeding with the GA, the formation of the impedance matrix based on RF switches (X_i) is needed. The impedance matrix consists of chromosomes in *N* number, as shown in Figure 6.7(a). A higher number of *N* increases convergence speed but requires more computational resources. The chromosome is an array of RF switches, as shown in Figure 6.7(b). The chromosome can be encoded in binary or real code. These chromosomes are arranged such that the X_i values can be uniquely mapped onto the decision variable domain.

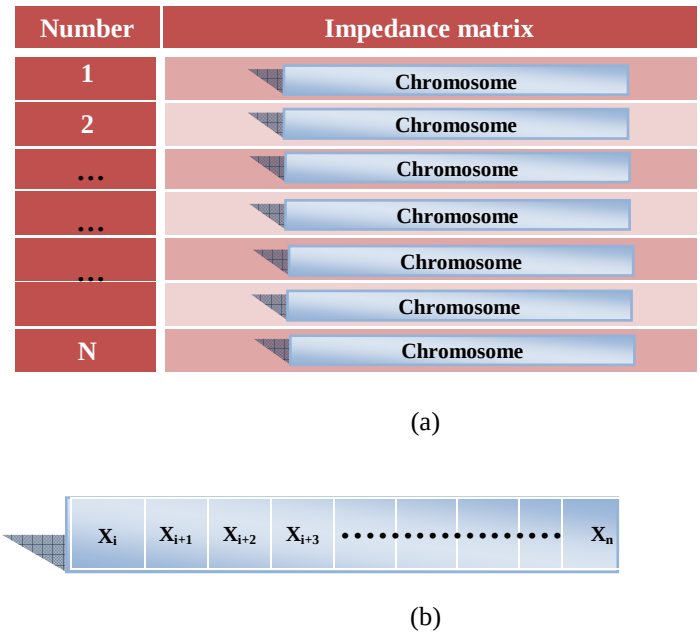


Figure 6.7: Population of the GA with (a) the formation of the impedance matrix and (b) the arrangement of RF switches in a chromosome structure

6.2.2.2 Fitness Value

Fitness function in the GA (*Fit*) evaluates the performance of a chromosome based on the VSWR value. The VSWR value is an indicator for the degree of impedance mismatch. A weighting factor is used to improve the searching efficiency of the developed GA in complex impedance domain by (6.10).

$$Fit = f\{VSWR\} * W_{i,t+1}^{N} \tag{6.10}$$

where $W^{N}_{i,t+1}$ is a scaling factor that is inversely proportional to the VSWR, *i* is the number of RF switches in the impedance network, *t* is the number of chromosomes in the population and *N* is the number of iterations.

6.2.2.3 GA's Operators

Parents are selected for the next generation based on their scaled values from the fitness scaling function. Crossover combines two individuals (as parents) to form a new individual (as child) for the next generation. Children are created between the lines containing the two parents. The mutation function makes small random changes to the children in the population, which provides genetic diversity and enables the genetic algorithm to search a broader area. The direction of changes is adaptively generated with respect to the last successful generation.

6.2.2.4 Simulation Results

The effectiveness of the developed adaptive algorithm based on GA has been demonstrated for a sample *Pi*-network with a wavelength ($\Delta\lambda_i$) of 30^0 between two RF switches. The mismatch load was assumed as an antenna load of 90-j*160. The working frequency is at 2.45GHz. 100 chromosomes are used in the simulation. The algorithm stops as soon as the user-defined threshold for *Fit(n)* is reached (e.g., $|Fit(n)| \leq 1.1$) or the maximum number of iterations (i.e., 1000) is exceeded. Figure 6.8 shows Z_{in} before and after applying the GA in the Smith chart.

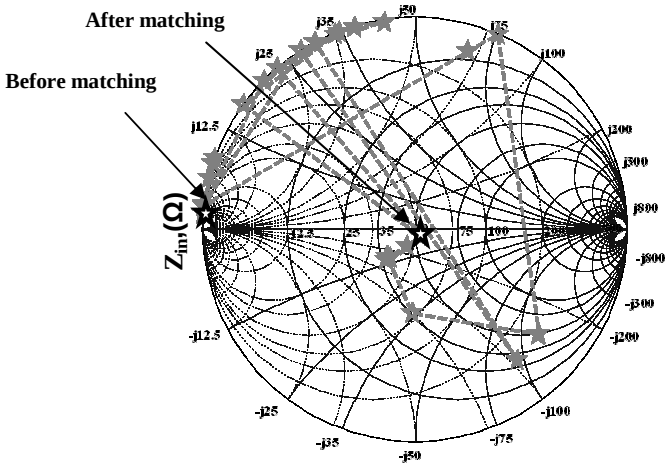


Figure 6.8: Convergence of GA based on complex input impedances in the Smith chart

The developed GA has also been tested with the *Pi*-network with four RF switches. Convergence of the GA based on real and imaginary parts of the input impedance over a number of iterations is presented in Figure 6.9. The real part of the input impedance is moved towards 50 Ω while the imaginary part of the input impedance is moved towards 0 Ω. This value of the input impedance is closely matched with system impedance (Z_0 = 50 Ω), thus significantly reducing the reflected power. The variations of tuning values in the four RF switches over iterations are presented, as shown in Figure 6.10.

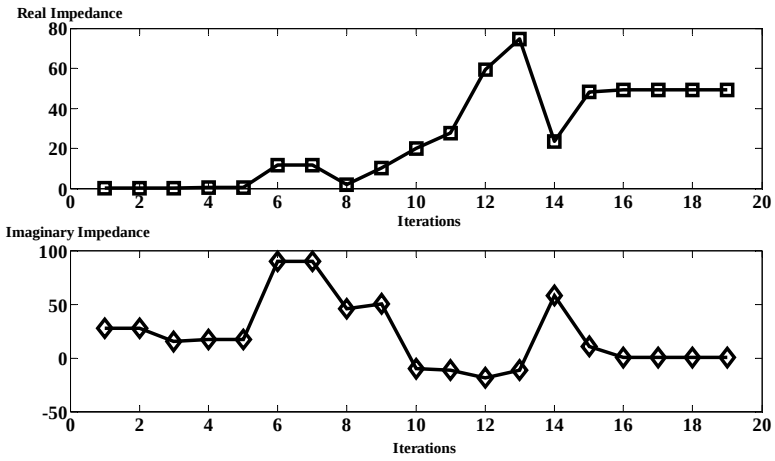


Figure 6.9: Convergence of the GA based on real and imaginary parts of input impedances over number of iterations

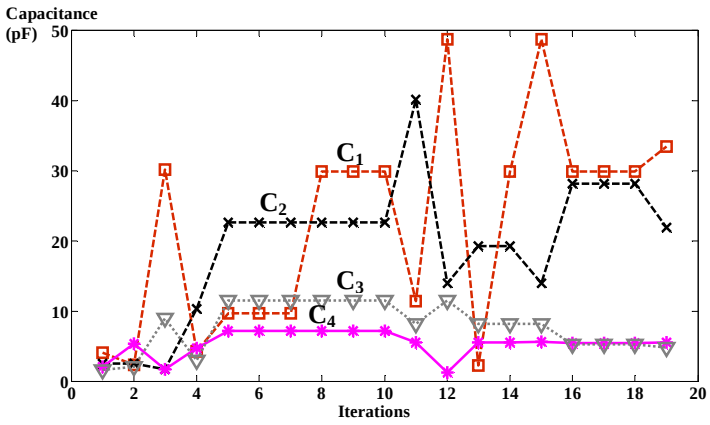


Figure 6.10: Tuning elements C_1, C_2, C_3 and C_4 over number of iterations

However, the convergence time of the GA is strongly affected by the population size. Figure 6.11 shows distributions of GA in 1000 times Monte Carlo simulations based on four RF switches in *Pi*-network for Z_{Load} of 183.7+j*258. Four different sizes of population have been tested i.e. 5, 10, 50 and 100 chromosomes. Simulation results show that the required number of iterations for a population size of 5 is significant longer compared to a population size of 100.

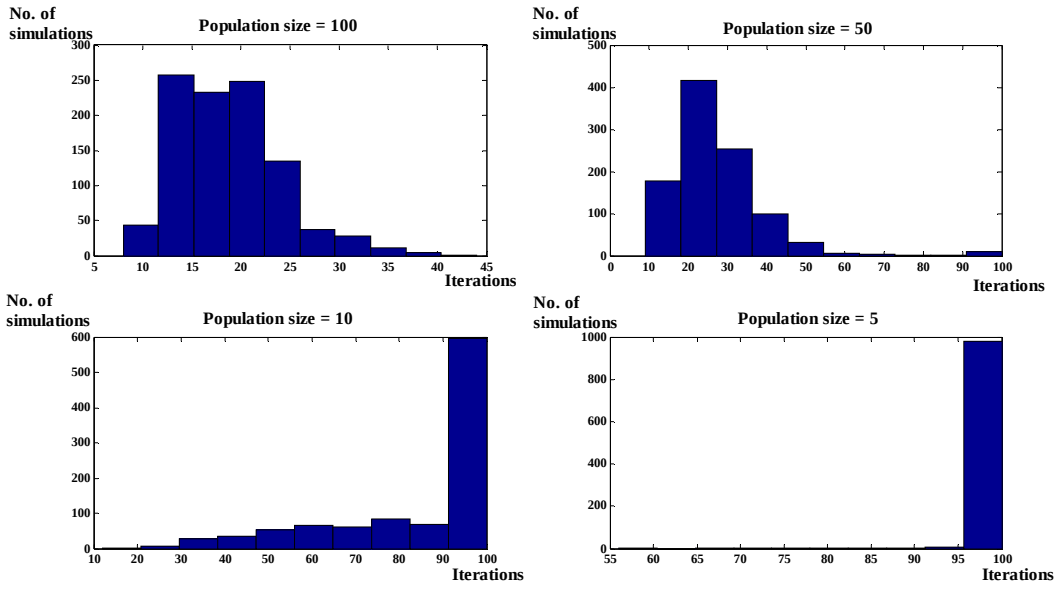


Figure 6.11: The required number of iterations of a GA for population sizes of 5, 10, 50 and 100 in 1000 times Monte Carlo simulations in a four tunable elements impedance network

In Time Division Multiple Access (TDMA), data stream divided into frames and frames divided into time slots. Time slots contain data with a guard period if needed for synchronisation. The tuning approach can potentially exploit the guard time between the time slots of the transmitted and received signal in a typical TDMA system. In a GSM system, the signal waveform frame comprises 1250 symbol or bit periods, divided into 8 time slots of 156.25 symbol periods. Each TDMA slot has fixed 152.25 symbol periods for traffic data, control data, etc., and 4 bit periods for dynamic time alignment. During these 4 bit periods, the radio system can lower the PA output power level (to prevent the excessive reflected power from destroying the PA) and perform the impedance tuning [26].

The tuning process will cause amplitude and phase modulation of the signal radiated as matching network component values are changed, so transmitted data may be corrupted if tuning occurs during transmission. Therefore it is desirable to perform tuning during limited idle periods, or at least minimise loss of data by minimising the duration of the tuning process [52, 176].

In the following section, a novel speedy Derivative-Corrective Mass Spring (DCMS) algorithm has been proposed for adaptive impedance matching networks. The performance of the proposed algorithm is evaluated by simulations, demonstrating a shorter convergence time compared to the GA and better accuracy compared to LMS based methods.

6.2.3 Derivative-Corrective Mass Spring Algorithm

The evolution of the proposed DCMS algorithm is governed by the fundamental second-order numerical differential method for a basic mass spring (BMS) [177]. The force exerted by the spring (F) is proportional to the stiffness of the spring (k) and the vicious damping coefficient (r), as shown by (6.11). Applying a finite-difference approximation for the BMS in (6.11), and incorporating the related network parameters in (6.4) and (6.7), the next step velocity ($V_{i,t+1}^{N}$) and the displacement ($D_{i,t+1}^{N}$) of the spring are derived, as shown by (6.12) and (6.13).

$$F = m.a = m.(\frac{V_{i,t+1}^{N} - V_{i,t}^{N}}{dt}) = m.d(\frac{D_{i,t+1}^{N} - D_{i,t}^{N}}{dt}) = -k.D - r.V \tag{6.11}$$

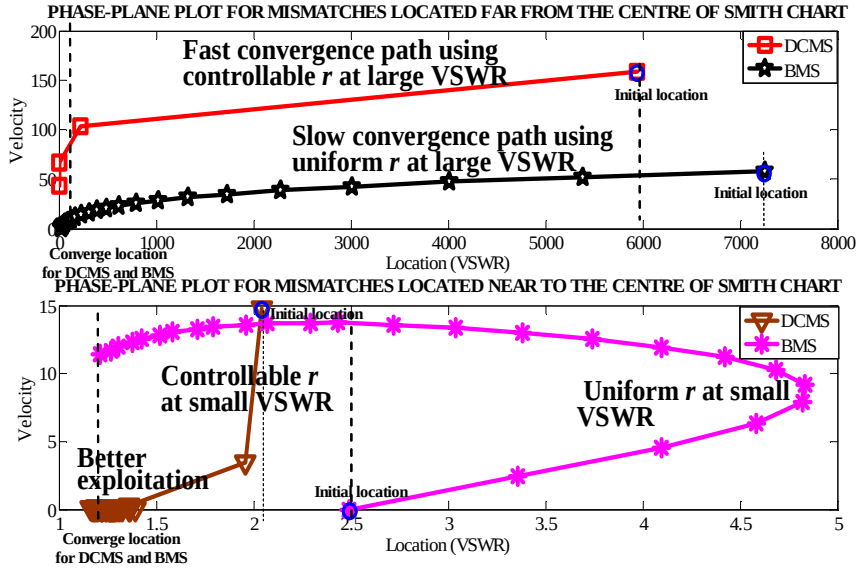
$$V_{i,t+1}^{N} = \frac{-k.D_{i,t}^{N}}{m} + (1 - \frac{f\{VSWR\}}{m}).V_{i,t}^{N} = -k.g_{ext}.D_{i,t}^{N} + (1 - r.g_{ext}).V_{i,t}^{N} \tag{6.12}$$

$$D_{i,t+1}^{N} = (1 - \frac{k}{m}).D_{i,t}^{N} + (1 - \frac{f\{VSWR\}}{m}).V_{i,t}^{N} = (1 - k.g_{ext}).D_{i,t}^{N} + (1 - r.g_{ext}).V_{i,t}^{N} \tag{6.13}$$

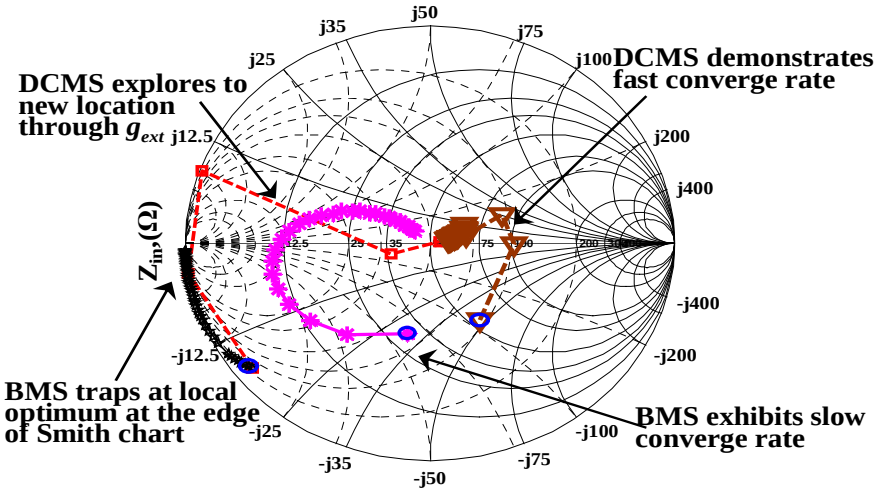
In the BMS algorithm, a uniform r is used. However, in the proposed DCMS algorithm, parameter r is controlled by the VSWR while the VSWR is determined by Γ and Z_{in}, which are derived from the current displacement ($D_{i,t}^{N}$). Z_{in}, which is closer to the coordinate of the Smith chart, has lower VSWR; while Z_{in}, which is far from the centre of the Smith chart, exhibits higher VSWR. The parameter r is incorporated with $V_{i,t+1}^{N}$ and $D_{i,t+1}^{N}$, as shown in (6.12) and (6.13). A higher velocity is imposed on individuals which are located far from the centre of the Smith chart, as shown in Figure 6.12a. Whereas, the velocity decays towards the centre of the Smith chart, making the individuals exploiting their current locations better. This enhances the convergence speed of the DCMS significantly compared to the BMS, as shown in Figure 6.12a.

The BMS will always be trapped in local optimum when the mismatch impedance is located at the edge of the Smith chart, as shown in Figure 6.12b. For the proposed DCMS, an external random force ($0< g_{ext} <1$) is applied to re-tune the direction of convergence when the individuals go out of user-defined boundaries (e.g., $|imag(Z_{in})|>100\Omega$) or the potential tuning parameters are invalid ($X_{i,t}^{N} <0$). This external force in the DCMS circumvents the

limitation of the numerical method which is sensitive to the initial values and enables better extrapolation to its neighbourhood.



(a)

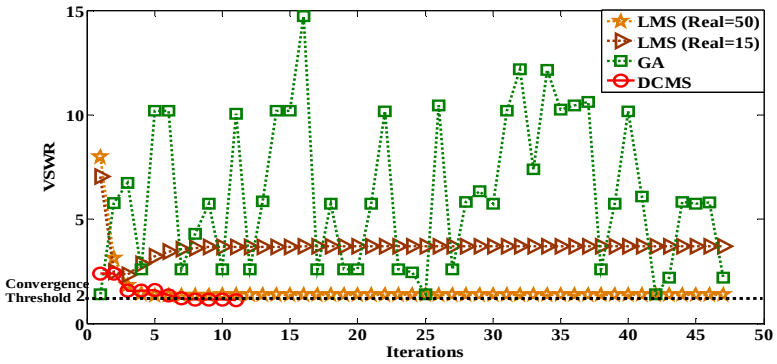


(b)

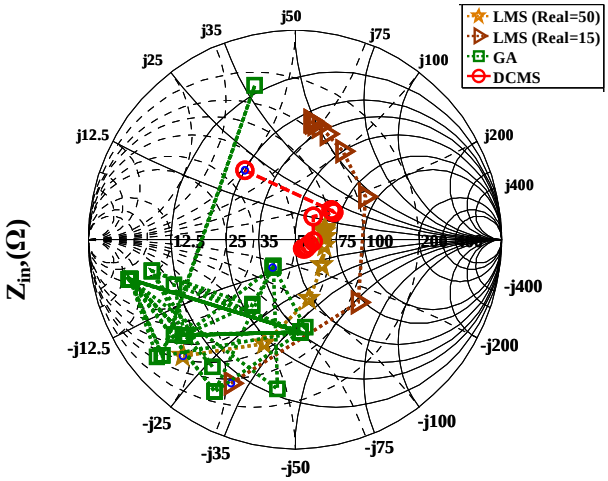
Figure 6.12: Comparison of the proposed DCMS with BMS for different mismatches based on (a) velocities and current locations of the individuals in phase-plane plot, and (b) complex input impedances (Z_{in}) in Smith chart

6.2.3.1 Simulation Results

The DCMS algorithm was tested with two topologies, i.e. *LC*- and *Pi*-network. The algorithm stops as soon as a user-defined threshold for the VSWR is reached (e.g., VSWR<2) or the maximum number of iterations (48) is exceeded. The results show that the DCMS outperforms both the LMS and the GA with its very fast convergence speed and high accuracy, see Figure 6.13a and b. The LMS shows a moderate convergence speed compared to the DCMS owing to its constant step size. However, the LMS is unable to converge when both real and imaginary parts are involved in the tuning process, as shown in Table 6.1. The GA and the DCMS have close average convergence rates, although the GA's convergence rate could be improved further by allowing longer simulation time and increasing the number of chromosomes. However, the GA has the longest average CPU time, which is more than 40 times slower compared to the DCMS.



(a)



(b)

Figure 6.13: Convergence of LMS, GA and DCMS based on (a) VSWR over number of iterations, and (b) complex input impedances (Z_{in}) in a Smith chart

Table 6.1: The average VSWR and CPU time for DCMS, LMS and GA in 1000 runs based on *LC*- and *Pi*- network for mismatches involving both real and imaginary part of Z_{Load} (15+j15.6) and solely the imaginary part of Z_{Load} (50+j15.6)

ADAPTIVE ALGORITHM	**Imp. Network**	**ELEMENTS IN Z_{LOAD} TO BE CORRECTED**	**AVERAGE VSWR**	**CPU TIME (ms)**	**COMMENTS**
DCMS	*LC*	REAL & IMAGINARY	1.7643	2.9	Fast and good convergence rate
		IMAGINARY ONLY	1.2134	2.8	
	Pi	REAL & IMAGINARY	1.4561	12.4	
		IMAGINARY ONLY	1.2053	13.1	
LMS	*LC*	REAL & IMAGINARY	6.3731	16.4	Unable to converge (VSWR>2) for the mismatches involving both real and imaginary parts
		IMAGINARY ONLY	1.4539	18.9	
	Pi	REAL & IMAGINARY	3.6866	20.4	
		IMAGINARY ONLY	1.0979	20.3	
GA	*LC*	REAL & IMAGINARY	1.3258	539.7	Slow CPU time
		IMAGINARY ONLY	1.0879	536.9	
	Pi	REAL & IMAGINARY	1.3921	544.6	
		IMAGINARY ONLY	1.2028	556.8	

6.3 Summary

This chapter has presented linear and stochastic based adaptive algorithms for determining the required impedance states at the RF switches. LMS (a linear based algorithm) is fast in speed but it is limited to match either real or imaginary parts of the complex impedance. The GA (a stochastic algorithm) is robust in searching for potential complex impedance solutions but it requires very expensive computational time. For this reason, a novel Derivative-Corrective Mass Spring (DCMS) algorithm which has faster convergence speed and is more robust than existing algorithms, i.e. the LMS and the GA, has been proposed. The proposed DCMS algorithm can intelligently increase diversity and escape from local optimum traps, enabling it to converge to solutions faster. Moreover, it can adaptively determine the next step velocities and displacements, which significantly reduce the number of searching steps required. In the second part, the DCMS is customised for implementation in the impedance network. A novel design technique through reconfiguring the boundaries of the search area has been proposed. It is based on the impedance network's topology, operating band and VSWR value. The searching space has been significantly reduced through identifying the required minimum and maximum ranges of the individuals. This significantly enhances the convergence rate and reduces computational resources. The reduction in search time is very important for reducing the risk of data loss and achieving better link quality for next generation mobile applications. Figure 6.14 summarises the areas and the challenges addressed in this chapter. The next chapter concludes the research investigation and suggests future work.

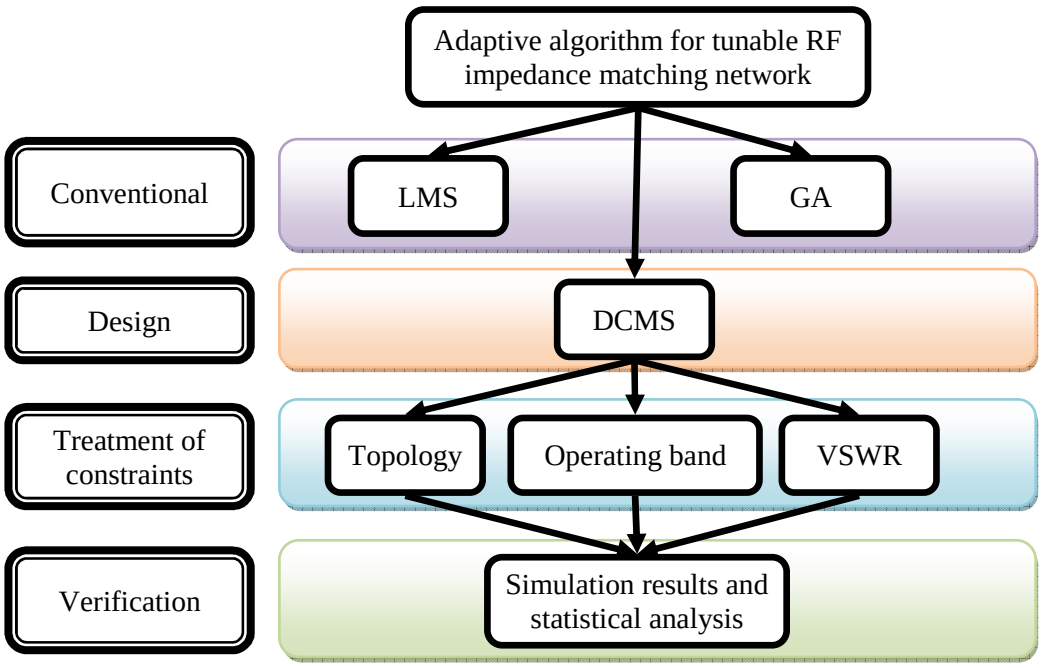


Figure 6.14: Summary of the areas and the challenges addressed in Chapter 6

Chapter 7: Conclusions

7.1 Summary and Conclusions

This thesis covers the research studies of DC-DC converters, impedance networks and adaptive algorithms for RF switches in order to achieve tunable and adaptable RF based mobile telecommunication systems. Specifically, the studies are divided into three major directions: (a) high voltage switch controller based on SC DC-DC converters for RF switch actuation, (b) impedance network designs for impedance transformation of RF switches, and (c) adaptive algorithms to calculate the required impedance at the RF switches for compensating the impedance variation of an antenna.

To achieve satisfactory RF switch performance, it is often necessary to have an actuating circuitry to generate high DC voltages for RF switch actuation with low power consumption. From the study, the RF switch controller based on an SC DC-DC converter demonstrates a promising topology due to its high energy density and ease in integration. In particular, due to its simpler switching circuitry, two-phase SC DC-DC converters have been investigated. Topologies of the SC DC-DC converter have been compared and the performance in steady and dynamic states have been analysed in Chapter 2. From the comparison, a Fibonacci converter (a non-linear voltage gain topology) demonstrates that it has the lowest voltage drop and the highest voltage gain by using the minimum number of components. Transistor gate driving strategies have been proposed to make the Fibonacci converter feasible for implementation. It was shown that the proposed gate driving

techniques reduce the design complexity and increase the reliability of the Fibonacci SC converter. A voltage conversion efficiency of 72% has been achieved by the prototype in discrete technology as mentioned in Chapter 2.

In Chapter 3, a linear voltage gain topology of the SC converter has been designed and developed in a CMOS integrated circuit environment. The design is based on the enhanced low voltage interleave structure. Two novel adaptive biasing circuits have been proposed in order to eliminate the leakage current, hence avoiding latch-up which normally occurs with low voltage transistors when they are used in high voltage design. The design parameters for the SC converter have been analysed and optimised. This includes the capacitor's size and the number of stages, which have significant effects to the die area and the power consumption of the converter. The effects of transistors' threshold voltage drop and parasitic capacitances have also been reduced for a higher voltage gain and lower power consumption. Through the proposed design techniques, the SC DC-DC converter achieves more than 25% higher boosted voltage compared to converters that use high voltage transistors. The proposed design reduces the power consumption by 40% through the charge recycling circuit that minimises the effect of non-ideality in high voltage capacitors. Moreover, the proposed SC DC-DC converter achieves a 45% smaller area than the conventional converter. Measurement results validate the proposed design strategies.

The second aspect of the research focuses on the design and development of an impedance network. An impedance network is designed to transform the RF switches to a range of impedance tuning regions, which are suitable for compensating the impedance variation of an antenna. The larger the impedance tuning region, the higher the ability of impedance network to correct antenna impedance mismatches. However, the maximum achievable impedance tuning region is bounded by the fundamental properties of the selected impedance network topology and by the tunable values of the RF switches that are variable over a limited range. A novel design technique for achieving the maximum achievable impedance tuning region at different operating frequencies, through identifying the frequency sensitivity of the impedance network, has been proposed in Chapter 4. By reconfiguring the electrical distance between two RF switches, wide impedance tuning regions are achieved across different frequencies. This technique reduces the cost and the insertion loss of an impedance network as the required number of RF switches is reduced. The prototype demonstrates high impedance coverages at LTE (700MHz), GSM (900MHz) and GPS (1575MHz).

Integration of a tunable impedance network with an antenna for frequency-agility at the RF front-end has been discussed in Chapter 5. An impedance network with zigzag radial stubs, which have a wider bandwidth compared to a linear stub but smaller area compared to radial stubs, have been designed and developed. The tuning of the impedance network has been designed based on the trajectories of the RF switches and the Q circle on a Smith chart in order to achieve a larger bandwidth. The integration of the tunable impedance network enlarges the bandwidth of a patch antenna by 1GHz (four times the original bandwidth). In the integrated system, the patch antenna also achieves a better return loss of 18dB. The design reconfigures for a wide range of frequency bands, ranging from 700MHz to 3GHz. This work demonstrates that a single transceiver with multi frequency ability can be realised by using a tunable impedance network.

Another aspect of the research focuses on the design and development of an adaptive algorithm. The adaptive algorithm calculates the required biasing state at the RF switches for compensating the impedance variation of an antenna based on the degree of impedance mismatch. It is highly desirable to reduce the search time in order to minimise the risk of data loss during the impedance tuning process. Existing algorithms are either difficult to converge for a complex number or exhibit high computational resource that are intolerable for mobile application. For this reason, a novel Derivative-Corrective Mass Spring (DCMS) algorithm which has faster convergence speed and is more robust than existing algorithms, i.e. the LMS and the GA, has been proposed in Chapter 6. The proposed DCMS algorithm increases the diversity intelligently and escapes from local optimum traps, which results in a faster convergence rate. Moreover, it can adaptively determine the next step velocities and displacements, which significantly reduce the required number of searching steps. For multi frequency standards, a novel design technique based on a flexible search area has also been proposed. The design technique reduces the searching space of the DCMS algorithm by identifying the required minimum and maximum ranges of the tuning elements. The computational speed is doubled with the adaptive boundary technique compared to the conventional approach. This work demonstrates that the proposed adaptive algorithm successfully reduces the search time, thus reducing the risk of data loss, which is very important in mobile applications.

7.2 Summary of Contributions

This section summarises the areas and the challenges in designing tunable RF based mobile telecommunication systems that have been addressed in this thesis. In particular, the research areas include DC-DC converters, impedance networks and adaptive algorithms, which are discussed as follows.

7.2.1 Design of a High Voltage Switch Controller based on SC DC-DC Converters for RF Switch Actuation

In this work, the design of the switch controller for the RF switch actuation is required to meet several stringent specifications, such as high voltage level, small size, low power consumption and linearity. The research investigation has been started with the linear and the non-linear voltage gain topologies.

7.2.1.1 Non-linear Voltage Gain SC Converter

The main contribution of this section is the design of gate driving strategies that only require few auxiliary transistors, hence reducing design complexity and increasing reliability in the implementation of a nonlinear voltage gain SC converter. The details of the research work are as follows.

a. Research investigation into the nonlinear voltage gain SC converters

   From the study, the non-linear voltage gain converter topology provides higher voltage gain in a smaller number of stages compared to the linear voltage gain topology. Among the non-linear voltage gain topology, the Fibonacci SC converter has been identified as having the lowest voltage loss per gain compared to other topologies. This topology also shows the advantages of using a fewer number of capacitors which result in a high conversion ratio. However, the implementation of a high voltage gain Fibonacci SC converter is complex due to the requirement of a widely different gate voltage for the transistors in the Fibonacci converter.

b. Design of gate driving techniques

   For this reason, two gate driving techniques for implementing the Fibonacci SC converter for both low and high step-up conversion ratios have been proposed in this work. The proposed gate driving techniques only require a few auxiliary transistors in order to provide the required boosted voltages for switching the transistors on and off. This results in a reduced design complexity and increased reliability of the Fibonacci SC converter.

c. Design optimisation and linearity improvement

   The sizes of the transistors and the capacitors of the converter have also been optimised for a higher switching speed. To achieve linearity, a large output capacitor has been suggested to compensate for the high voltage ripple due to a large voltage difference between the stages of the Fibonacci converter.

d. Implementation considerations for an HV switch controller using discrete technology

   For the non-linear voltage gain converter implementation, discrete or hybrid technology is the best solution with a high capacitance per area and high voltage rating limit of the components. A discrete prototype has been demonstrated in this work, verifying the proposed techniques.

7.2.1.2 Linear Voltage Gain SC Converter

The main contribution of this section is the design of a high performance CMOS based linear voltage gain SC DC-DC converter for high output voltage, low power consumption and small die area. The details of the research work are as follows.

a. Research investigation into the linear voltage gain SC converters

   For the linear voltage gain topology, it is best implemented in CMOS technology. In this work, the design parameters for a high performance CMOS based SC DC-DC converter has been analysed and synthesised.

b. Design optimisation and linearity improvement

A low loading effect of the SC DC-DC converter has been identified which allows the size of the capacitors and its stages to be optimised. Thus, this significantly reduces the die area and the power consumption of the proposed SC DC-DC converter. In addition, a power saving of more than 40% is achieved through the proposed charge recycling circuit that reduces the effect of non-ideality in high voltage capacitors.

The proposed design also demonstrates a high linearity performance where very small ripples have been observed at the output voltage, through complementing the internal node voltages from the 1st and the 2nd rows of the SC DC-DC converter.

c. Design of adaptive bulk biasing techniques

In order to further improve the performance of the SC DC-DC converter, low voltage transistors have been chosen for the implementation in the high voltage SC converter. Inter- and final- stages adaptive biasing circuits have been proposed to eliminate the leakage current, hence avoiding very high current peaks flowing to the substrate. A higher output voltage (more than 25%) is achieved with the proposed technique compared to using high voltage transistors.

d. Implementation considerations for an HV switch controller in integrated technology

The layout for an HV design using CMOS technology is complex and not as straightforward as for an LV design. The layout of the SC DC-DC converter has been surrounded with several isolation layers which enables the LV transistors in an HV environment and further enhances the performance of the transistors from the substrate noise. The design has been fabricated in AMS 0.35µm technology. The measurement results verify the proposed techniques.

7.2.2 Impedance Network Designs for Impedance Transformation of RF Switches

In this work, the impedance network has been designed to transform the RF switches to a range of impedance tuning region which is suitable for compensating the impedance variation of an antenna. A design technique has been proposed to increase the impedance tuning region through identifying the optimum electrical distance between the RF switches in the impedance network, and maintain the high impedance tuning region across multiple frequency standards through varying the electrical distance. Research investigations have been performed into the impedance network designs, including impedance network topology, impedance network losses, circuit size, tunable RF technology, impedance coverage and the integrated system. The details of the research work are as follows.

a. Research investigation into the impedance network topologies

   From the studies, topologies based on a λ/4 transmission line or a taper show the limitation in impedance tuning that only covers a real impedance region. Whereas, topologies based on a stub or lumped elements impedance networks demonstrate complex impedance tuning ability.

b. Optimises impedance network to reduce losses and circuit size

   Optimisation to the impedance network has also been performed. Conventional impedance network topology consists of bulky and high loss components such as inductors, which are unfit for mobile applications. Techniques to replace these unwanted components (such as inductors) to stub line or capacitive RF switches, which have a higher quality factor and easier integration features, have been presented. Thus, the size and the losses in the impedance network are reduced based on this optimisation technique.

c. Research study on the technology of RF switches

   RF performance depends on the RF switches technology considered. Technologies of RF switches such as semiconductor, BST, and MEMS have been studied and analysed in this work. The properties of the RF switches are compared in terms of losses, tuning range and RF performance. From the comparison, impedance coverage

can be increased at the expense of a large number of RF switches, which increase losses and design complexity.

d. Design of high impedance coverage technique

   For this reason, a design technique has been proposed in order to reduce the number of the RF switches through identifying the electrical distance between RF switches for the maximum impedance coverage. By varying the electrical distance, the maximum impedance coverage has been achieved at multi-operating frequencies.

7.2.2.1 Integrated System Designs for Multi Frequency Standards

In this work, the development and the integration of a wideband impedance network with an antenna for frequency-agility at RF front-end have been performed, which are discussed as follows.

a. Research study on the wide bandwidth impedance networks

   The wideband impedance network allows a considerable extension of the operational bandwidth of mobile device antennas. Several methods including multi-section transmission lines, radial stubs and tuning steps are discussed in order to increase the operational bandwidth of the impedance network.

b. Implementation considerations for an impedance network integrated with an antenna

   The presented impedance network is optimised to allow convenient implementation of the necessary dc control lines, RF choke and DC blocking capacitor to control the tuning components. The integrated system improves the antenna's bandwidth and achieves a better return loss. The integrated system reconfigures from 700MHz to 3GHz, covering most of the widely used mobile telecommunication operating frequencies. The results demonstrate that many different frequency standards could be achieved in one circuit. This avoids duplicating mode-specific transceiver units for multi frequency standards on a single device.

7.2.3 Adaptive Algorithm for Determining the Required Impedance States at the RF Switches

In the final stage, adaptive algorithms have been investigated to calculate the required impedance states at the RF switches. A design technique has been proposed to reduce the search time by more than an order of magnitude by exploiting the relationships among the mass spring's coefficient values derived from the impedance network parameters, thereby significantly reducing the convergence time of the algorithm. The research investigation has been started with linear correlation and stochastic approaches. The details of the research work are as follows.

a. Research investigation into the linear correlation approach

   From the study, linear correlation approaches, such as least mean square (LMS), have been applied in searching the antenna impedance. LMS is fast in reaching convergence. However, LMS is limited in searching for either the real or the imaginary part of the impedance but not both parts simultaneously due to the non-linear correlation in complex impedance. With an increasing number of RF switches in the impedance network, searching using LMS will be more difficult.

b. Research investigation into the stochastic approach

   For the stochastic approach, the Genetic Algorithm (GA) has been investigated. The GA has been designed and well fit into this problem domain. However, analysis shows that the GA converges in reverse correlation to population size. Large population sizes require high computational costs, which are not preferable for mobile applications. By using a small population, a long convergence time is required. A long convergence time might increase the risk of data loss, as transmitted data may be corrupted if tuning happens during transmission. Therefore, it is desirable to perform tuning during very limited idle periods in order to minimise the risk of data loss.

c. The design of a speedy adaptive algorithm for mobile applications

   For this reason, a speedy adaptive algorithm has been proposed which can adaptively determine the next step velocities and displacements, significantly reducing the number of searching steps required. The proposed algorithm reduces the search time

by more than an order of magnitude by exploiting the relationships among the mass spring's coefficient values derived from the impedance network parameters, thereby significantly reducing the convergence time of the algorithm.

A summary review of the areas and the challenges addressed in the thesis is concluded in Figure 7.1.

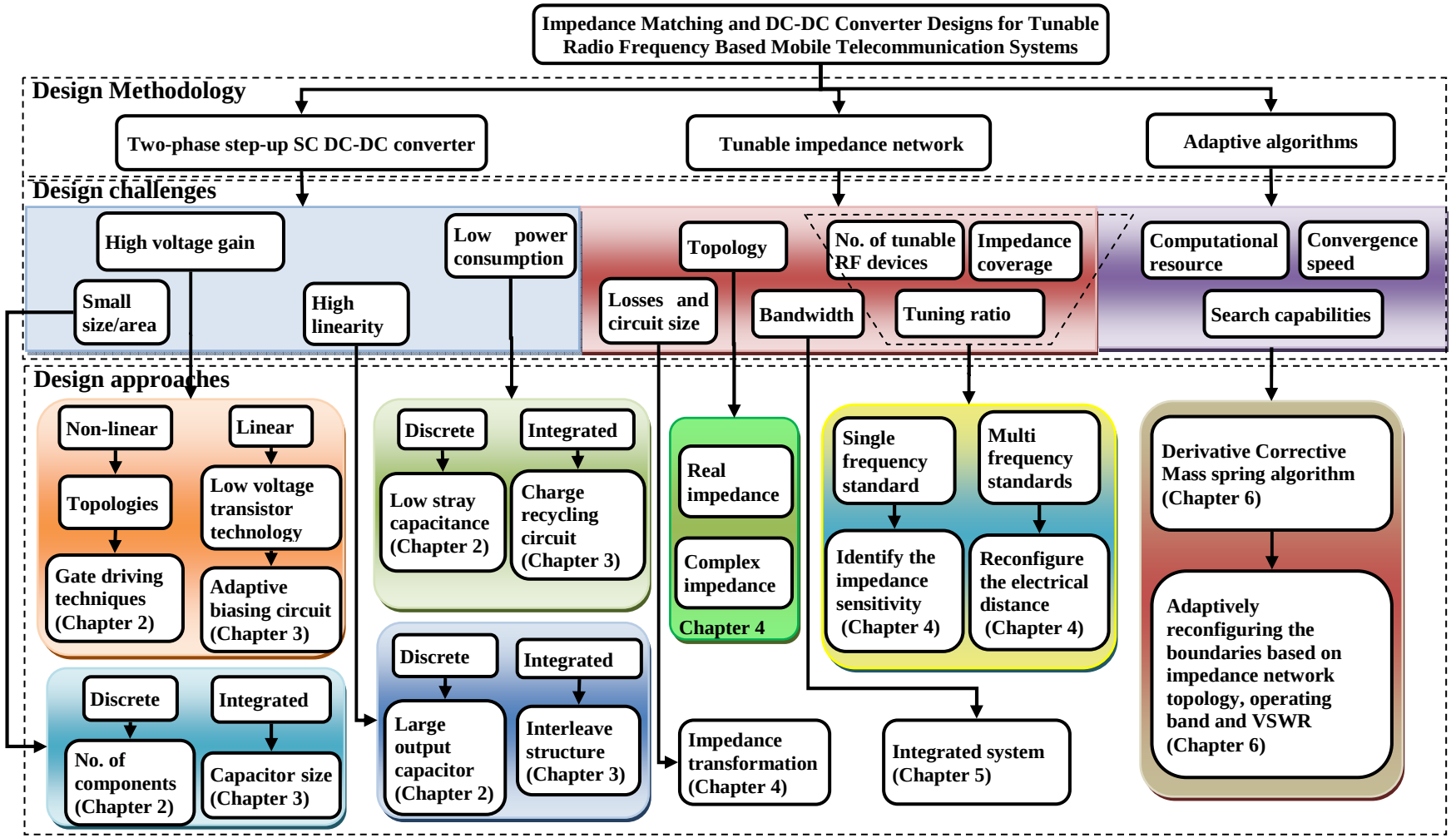


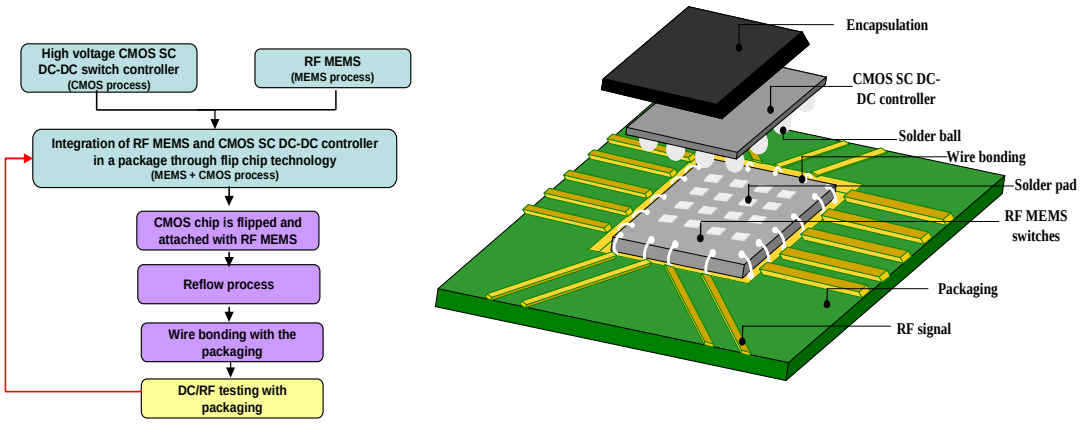
Figure 7.1: The areas and the challenges addressed in the thesis

7.3 Future Work

The following are possible topics for further investigation:

7.3.1 High Voltage Switch Controller based on SC DC-DC Converters for RF Switch Actuation

In this work, one future direction would be integrating the proposed HV SC DC-DC converters with RF switches through flip chip technology. The dimensions of the HV SC DC-DC converter have been customised to match exactly with the RF switches to comply with the flip chip technique. Figure 7.2(a) shows the process flow for the integration of RF switches with the HV SC converter in a single package. Figure 7.2(b) illustrates the integrated system underneath the encapsulation. Through the single package integration, high voltage exposure on the system board can be avoided. Moreover, this eliminates the need for electrostatic discharge (ESD) network capacitors, which significantly reduces 20pF to 30pF capacitances at input/output (IO) pads. This will result in a much smaller packaging than traditional carrier based packaging both in area and height. The short wires in the flip chip technology will greatly reduce inductance and allow higher frequency operations. This is crucial for RF applications.



(a) (b)

Figure 7.2: System integration between an RF MEMS switch and the CMOS SC DC-DC converter in (a) process flow and (b) package level integration through flip chip technology

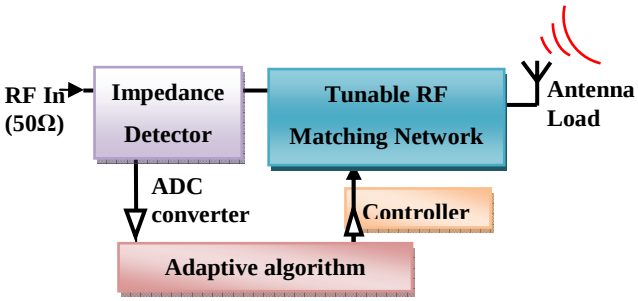
7.3.2 Impedance Network Designs for Impedance Transformation of RF Switches

In this work, commercially available varactors were used as the tuning elements in the prototype to validate the design approach. The varactors are cheap and easily available but low in power handling. This limits the prototype in functioning as both receiver and transmitter. To achieve higher power handling capability, especially for the antenna used in transmission, the work presented here can be extended to capacitive RF MEMS switches. RF switches based on MEMS technology demonstrate lower insertion loss and higher power handling features compared to other technologies.

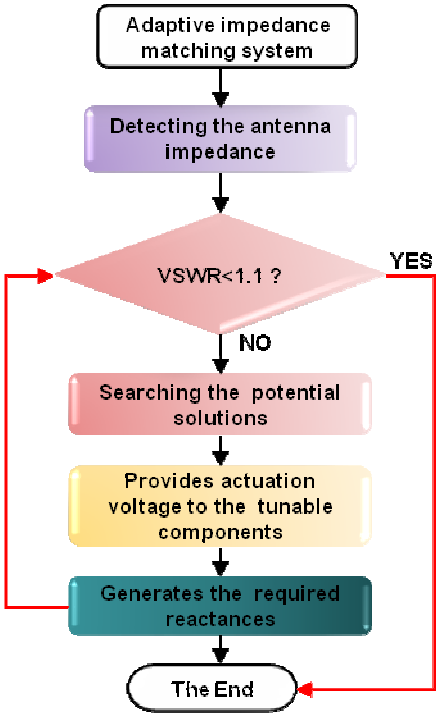
Another future direction would be developing the proposed impedance networks with the RF switches at the same platform to achieve smaller size and lower reflection loss.

7.3.3 Adaptive Algorithms for Determining the Required Impedance States at the RF Switches

For the adaptive algorithm, one future direction could be to embed the proposed DCMS algorithm in a processor and integrate it with a tunable impedance network. Figure 7.3 (a) shows the simplified block diagram of an adaptive integration system. The adaptive system obtains the actual impedance value in real time through an impedance detector. The degree of mismatch can be obtained through off-the-shelf components e.g. AD8303[178]. The impedance mismatch can also be obtained through performing two subsequent detections, with a second set of tuning values, assuming the Z_{Load} has remained constant, the load impedance may be derived [69]. The adaptive algorithm will search for potential solutions based on the degree of the mismatch. The solutions will be fed to a controller, which provides high voltage for actuating the RF switches in the impedance network. This process will be repeated until a match condition is reached, as shown in Figure 7.3(b).



(a)



(b)

Figure 7.3: Integrating the adaptive algorithm to the tunable impedance matching system in (a) block diagram, and (b) flow chart

7.3.4 Final Comments

Implementation of an impedance matching network can be accomplished using a variety of methods.

The impedance network can be designed together with the antenna which can maximise the performance of the particular antenna [167]. The impedance network can also be designed as the 50-50 designs by assuming the source and antenna impedance are both at 50Ω, as in this work. The earlier approach will obtain the best antenna tuning performance but a longer design process with severe design constraints. The later is simpler in design and generic that can easily apply to any model with the antenna impedance at 50Ω.

Similarly, the tuning can be performed by using single [167] or multiple tuning elements (this work). Single varactor tuning shows simple control mechanism however has significantly limited tuning resolutions and low impedance coverage on Smith chart. Pi- and T-network, require multiple tuning elements, show higher tuning resolutions compared to single varactor tuning. Pi-and T-network also show an extra degree of freedom that is able to control the bandwidth at the matched condition. These advantages are achieved at the expense of higher complexity in the biasing circuits as well as in the adaptive algorithm.

There is a trade-off between performance and complexity which is up to the designer choices and also the priority in the design requirements.

7.4 Conclusion

In conclusion, Figure 7.4 summarises the research contributions towards the realisation of tunable RF based mobile telecommunication systems. Research study addressed the challenges in the areas of DC-DC converters, impedance networks and adaptive algorithms for RF switches in order to achieve multi frequency bands RF front-ends, aiming at the realisation of high performance mobile telecommunication systems.

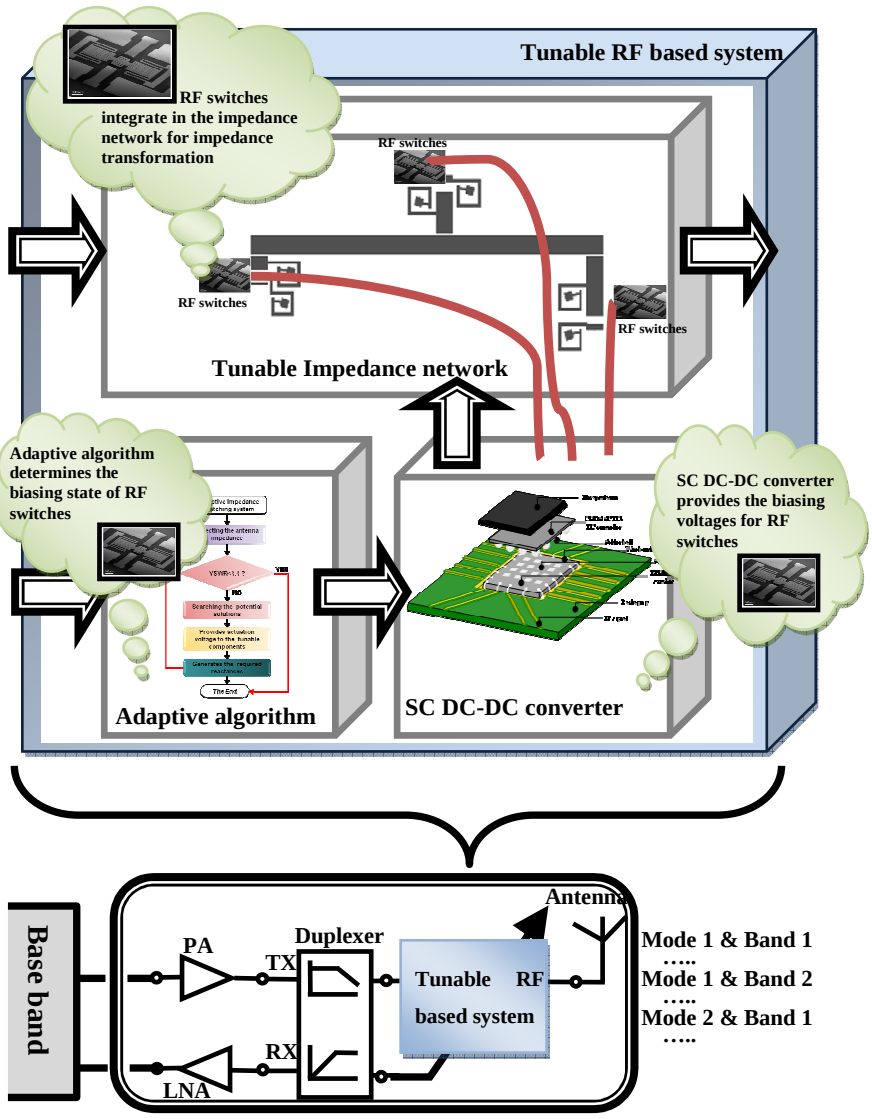


Figure 7.4: Contributions of the proposed functional blocks towards the realisation of tunable RF based mobile telecommunication systems, aimed at the realisation of high performance mobile telecommunication systems

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Appendix I:

Transistor Device characteristics

FAIRCHILD
SEMICONDUCTOR TM

September 1997

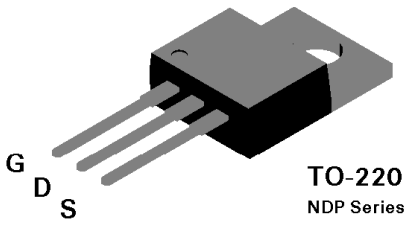
NDP6020P / NDB6020P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

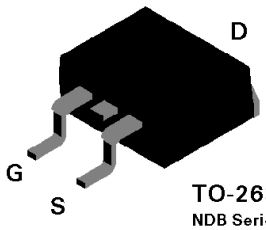
These logic level P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

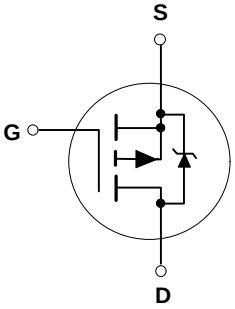
- -24 A, -20 V. $R_{DS(ON)}$ = 0.05 Ω @ V_{GS}= -4.5 V.
  $R_{DS(ON)}$ = 0.07Ω @ V_{GS}= -2.7 V.
  $R_{DS(ON)}$ = 0.075 Ω @ V_{GS}= -2.5 V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6020P	NDB6020P	Units
V_{DSS}	Drain-Source Voltage	-20		V
V_{GSS}	Gate-Source Voltage - Continuous	±8		V
I_D	Drain Current - Continuous	-24		A
	- Pulsed	-70		
P_D	Total Power Dissipation @ T_C = 25°C	60		W
	Derate above 25°C	0.4		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.7	-1	V
		T_J = 125°C	-0.3	-0.56	-0.7	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -12 A		0.041	0.05	Ω
		T_J = 125°C		0.06	0.08	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -2.7 V, I_D = -10 A		0.059	0.07	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -2.5 V, I_D = -10 A		0.064	0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-24			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -12 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1590		pF
C_{oss}	Output Capacitance			725		pF
C_{rss}	Reverse Transfer Capacitance			215		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -20 V, I_D = -3 A, V_{GS} = -5 V, R_{GEN} = 6 Ω		15	30	nS
t_r	Turn - On Rise Time			27	60	nS
$t_{D(off)}$	Turn - Off Delay Time			120	250	nS
t_f	Turn - Off Fall Time			70	150	nS
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -24 A, V_{GS} = -5 V		25	35	nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			10		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-24	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-80	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -12 A (Note 1)		-1.1	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -24 A, dI_F/dt = 100 A/µs		60		ns
I_{rr}	Reverse Recovery Current			-1.7		A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

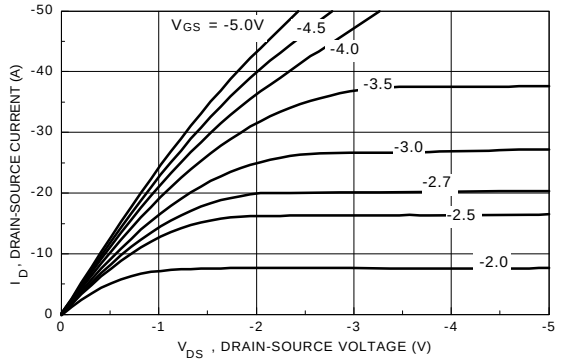


Figure 1. On-Region Characteristics.

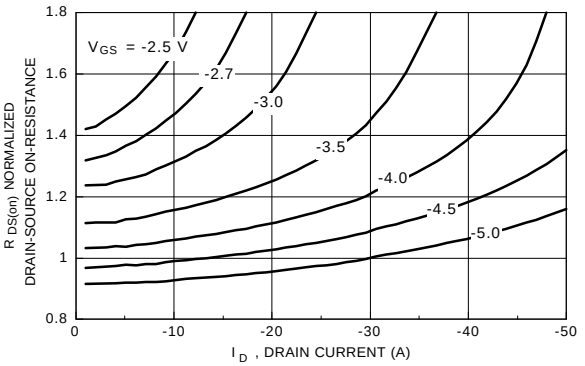


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

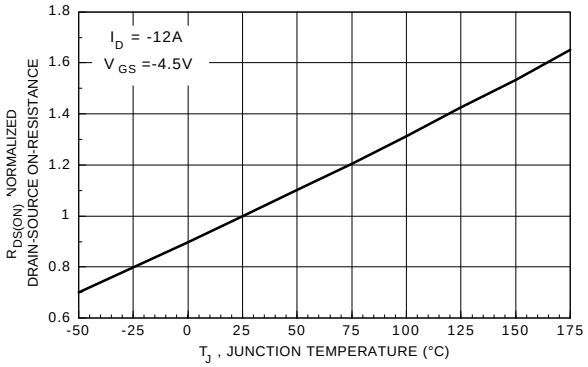


Figure 3. On-Resistance Variation with Temperature.

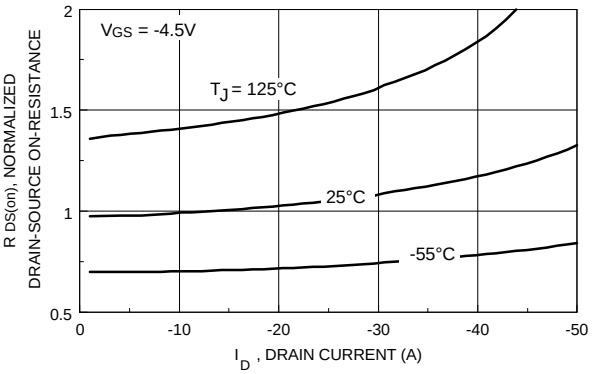


Figure 4. On-Resistance Variation with Drain Current and Temperature.

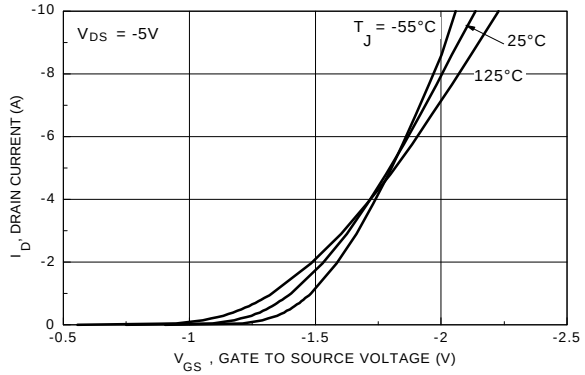


Figure 5. Transfer Characteristics.

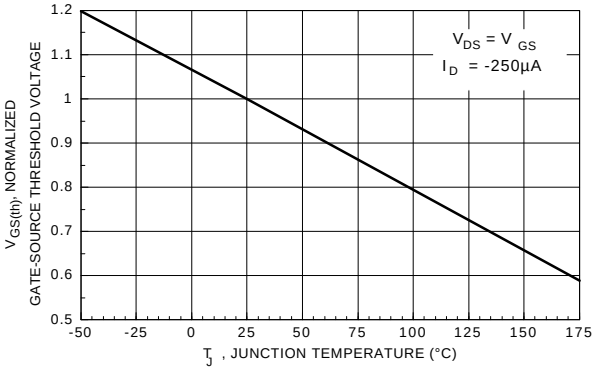


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

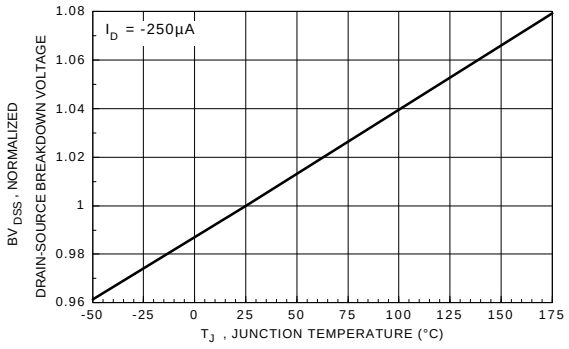


Figure 7. Breakdown Voltage Variation with Temperature.

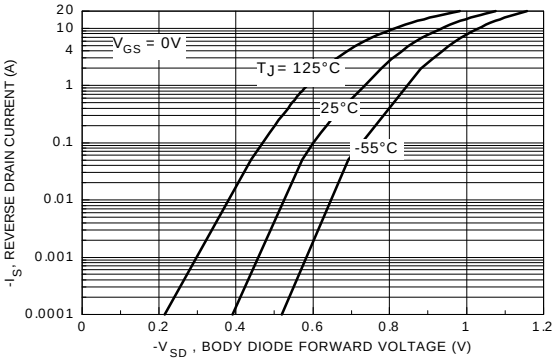


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

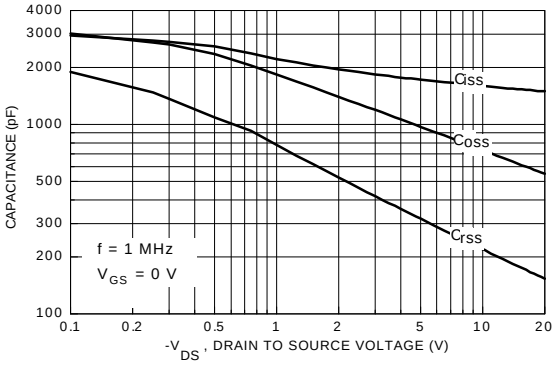


Figure 9. Capacitance Characteristics.

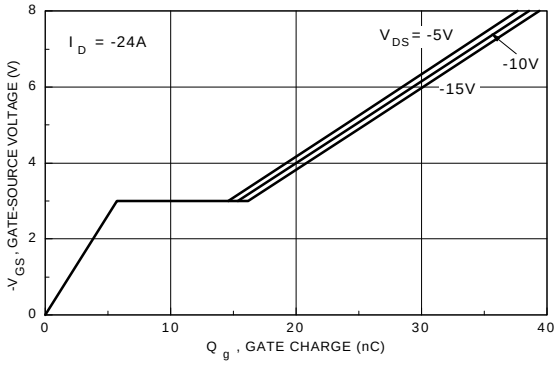


Figure 10. Gate Charge Characteristics.

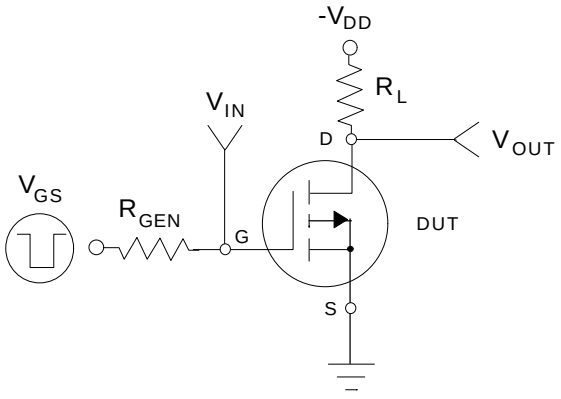


Figure 11. Switching Test Circuit.

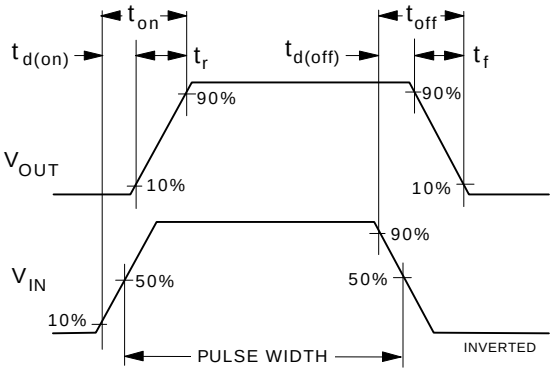


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

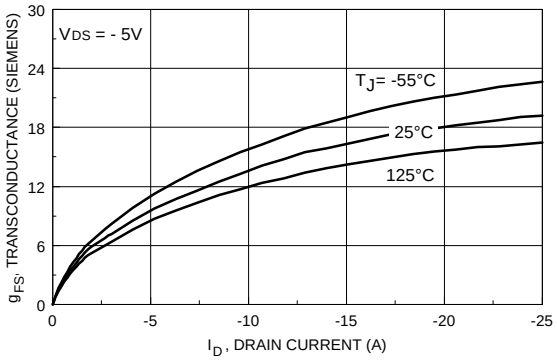


Figure 13. Transconductance Variation with Drain Current and Temperature.

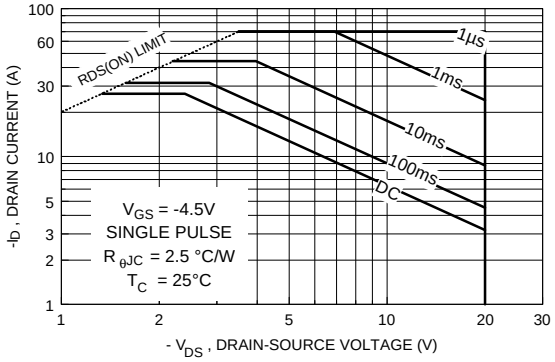


Figure 14. Maximum Safe Operating Area.

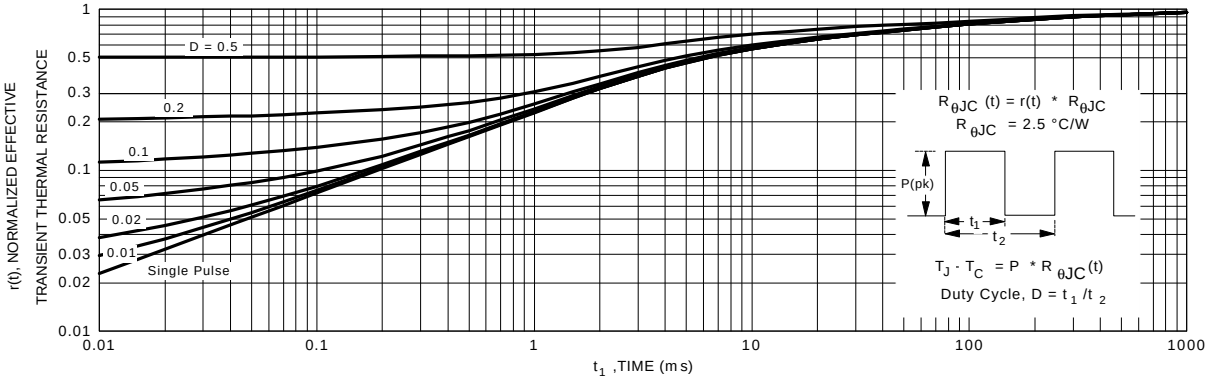


Figure 15. Transient Thermal Response Curve.

International
IOR Rectifier

PD - 95089A

IRLR3802PbF
IRLU3802PbF

HEXFET® Power MOSFET

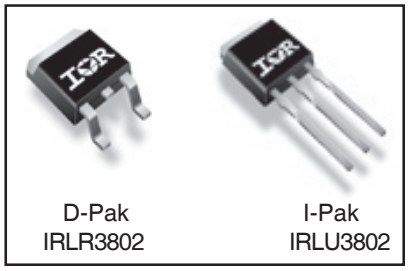
V_{DSS}	$R_{DS(on)}$ max	Q_g
12V	8.5mΩ	27nC

Applications

- High Frequency 3.3V and 5V input Point-of-Load Synchronous Buck Converters
- Power Management for Netcom, Computing and Portable Applications.
- Lead-Free

Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current



D-Pak IRLR3802 | I-Pak IRLU3802

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	84 ④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 4.5V	60④	
I_{DM}	Pulsed Drain Current①	320	
P_D @T_C = 25°C	Maximum Power Dissipation	88	W
P_D @T_C = 100°C	Maximum Power Dissipation	44	W
	Linear Derating Factor	0.59	mW/°C
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.7	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	——	40	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Notes ① through ④ are on page 9

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	12	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.009	—	V/°C	Reference to 25°C, I_D = 1mA ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.5	8.5	mΩ	V_{GS} = 4.5V, I_D = 15A ③
		—	—	30		V_{GS} = 2.8V, I_D = 12A
$V_{GS(th)}$	Gate Threshold Voltage	0.6	—	1.9	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-3.2	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	µA	V_{DS} = 9.6V, V_{GS} = 0V
		—	—	250		V_{DS} = 9.6V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -12V
g_{fs}	Forward Transconductance	31	—	—	S	V_{DS} = 6.0V, I_D = 12A
Q_g	Total Gate Charge	—	27	41		
Q_{gs1}	Pre-Vth Gate-Source Charge	—	3.6	—		V_{DS} = 6.0V
Q_{gs2}	Post-Vth Gate-Source Charge	—	2.0	—		V_{GS} = 5.0V
Q_{gd}	Gate-to-Drain Charge	—	10	—	nC	I_D = 6.0A
Q_{godr}	Gate Charge Overdrive	—	11	—		See Fig.16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	12	—		
Q_{oss}	Output Charge	—	28	—	nC	V_{DS} = 10V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	11	—		V_{DD} = 6.0V, V_{GS} = 4.5V③
t_r	Rise Time	—	14	—	ns	I_D = 12A
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		Clamped Inductive Load
t_f	Fall Time	—	17	—		
C_{iss}	Input Capacitance	—	2490	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	2150	—	pF	V_{DS} = 6.0V
C_{rss}	Reverse Transfer Capacitance	—	530	—		f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	300	mJ
I_{AR}	Avalanche Current①	—	20	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	84④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	320		
V_{SD}	Diode Forward Voltage	—	0.81	1.2	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V ③
		—	0.65	—		T_J = 125°C, I_S = 12A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	52	78	ns	T_J = 25°C, I_F = 12A, V_R=20V
Q_{rr}	Reverse Recovery Charge	—	54	81	nC	di/dt = 100A/µs ③
t_{rr}	Reverse Recovery Time	—	50	75	ns	T_J = 125°C, I_F = 12A, V_R=20V
Q_{rr}	Reverse Recovery Charge	—	50	75	nC	di/dt = 100A/µs ③

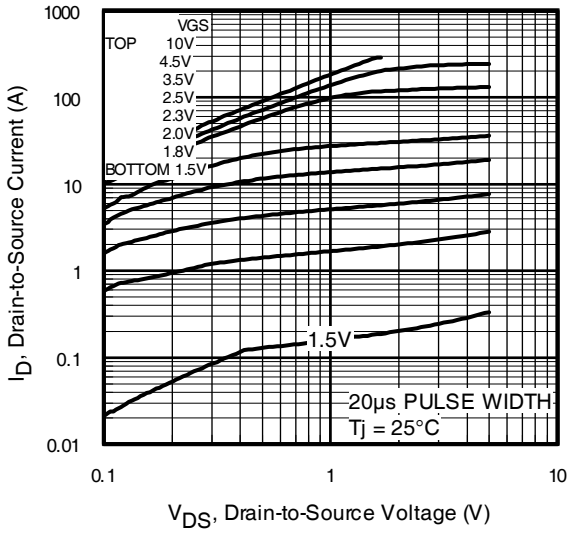


Fig 1. Typical Output Characteristics

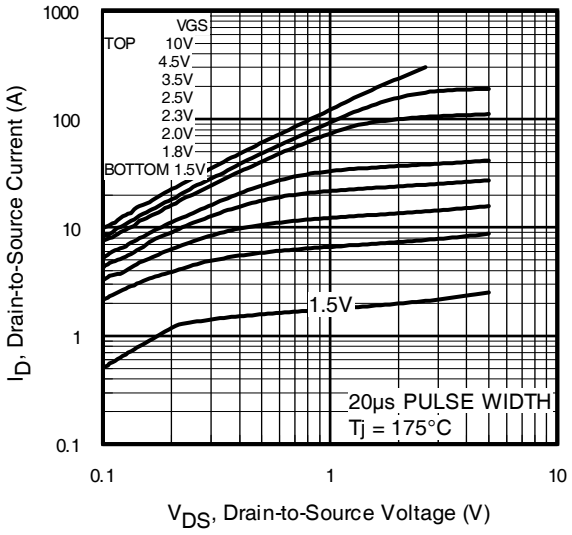


Fig 2. Typical Output Characteristics

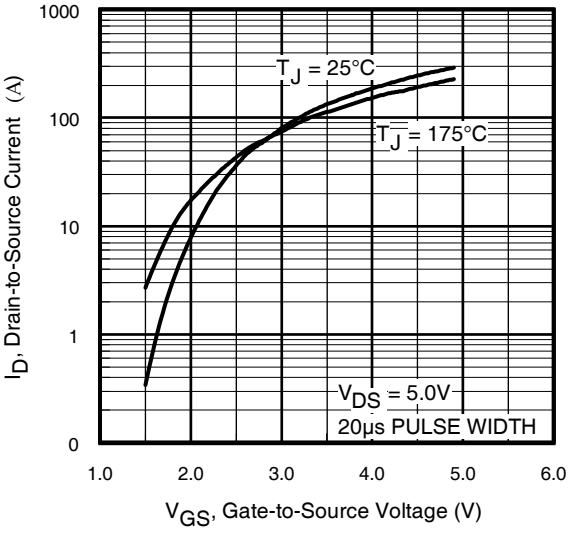


Fig 3. Typical Transfer Characteristics

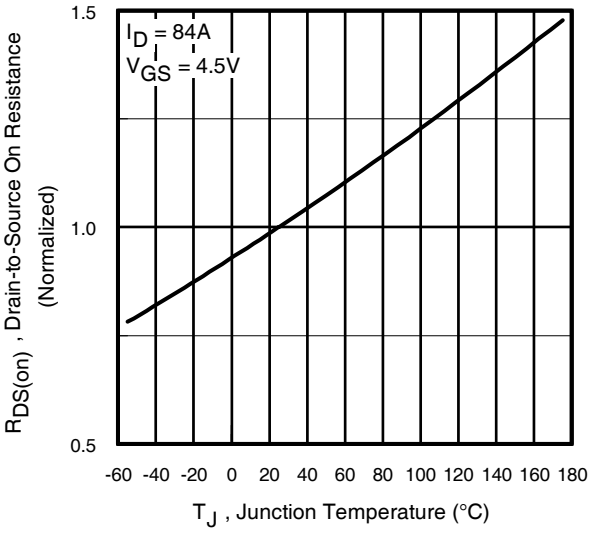


Fig 4. Normalized On-Resistance Vs. Temperature

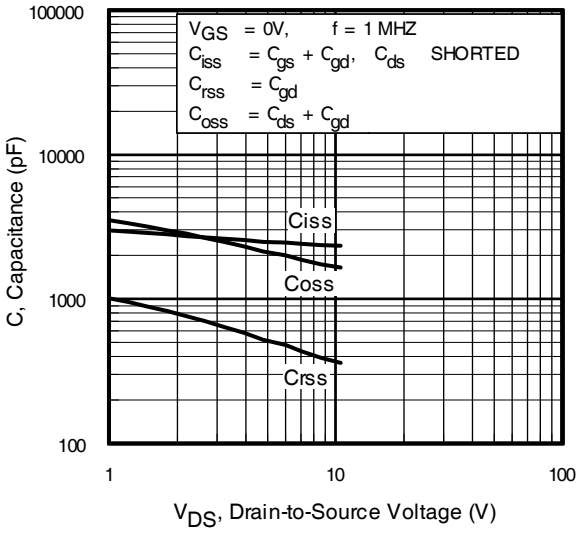


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

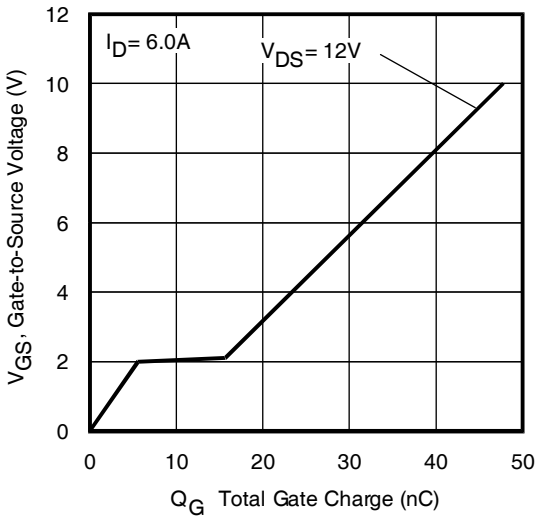


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

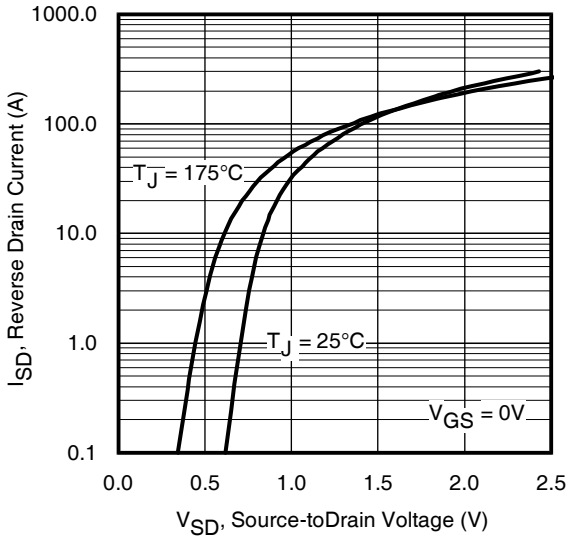


Fig 7. Typical Source-Drain Diode Forward Voltage

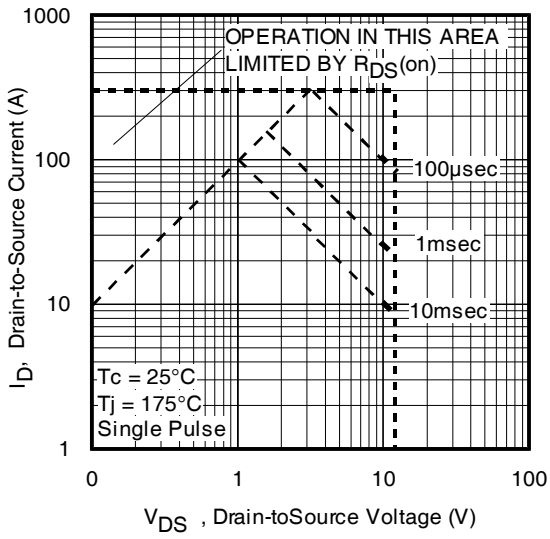


Fig 8. Maximum Safe Operating Area

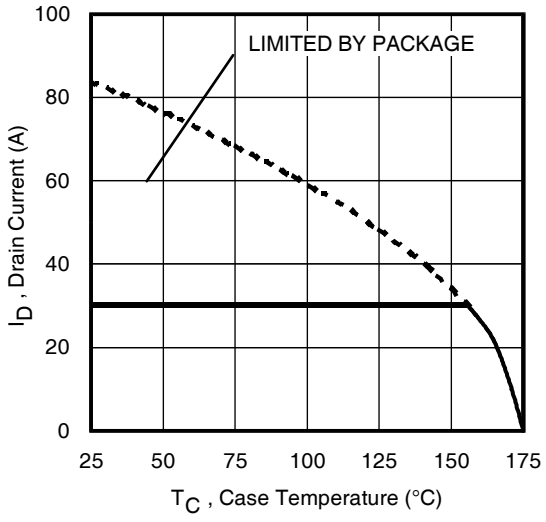


Fig 9. Maximum Drain Current Vs. Case Temperature

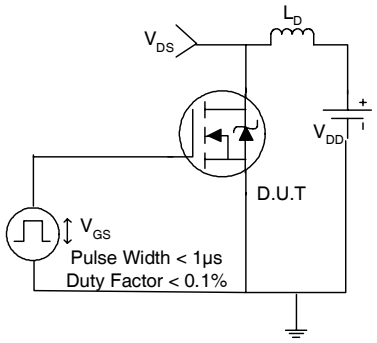


Fig 10a. Switching Time Test Circuit

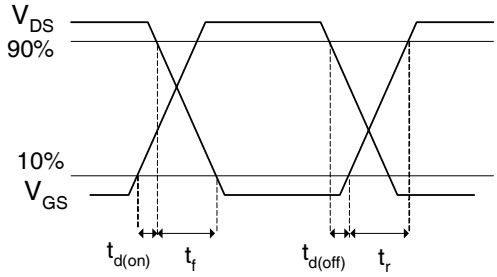


Fig 10b. Switching Time Waveforms

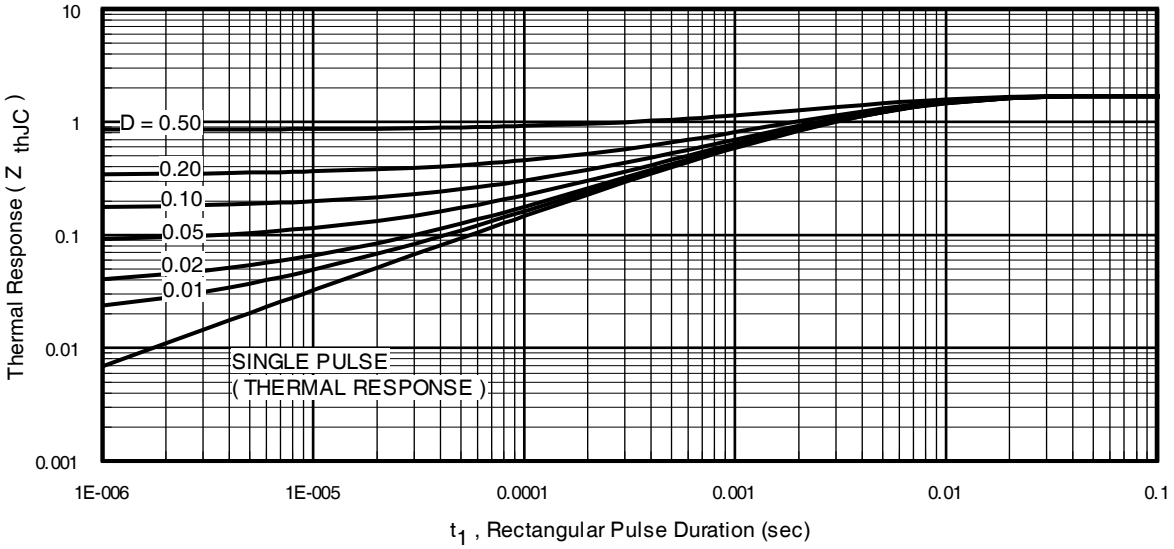


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

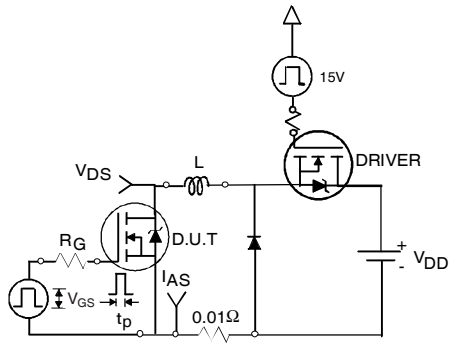


Fig 12a. Unclamped Inductive Test Circuit

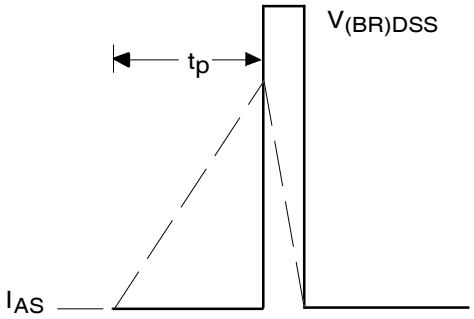


Fig 12b. Unclamped Inductive Waveforms

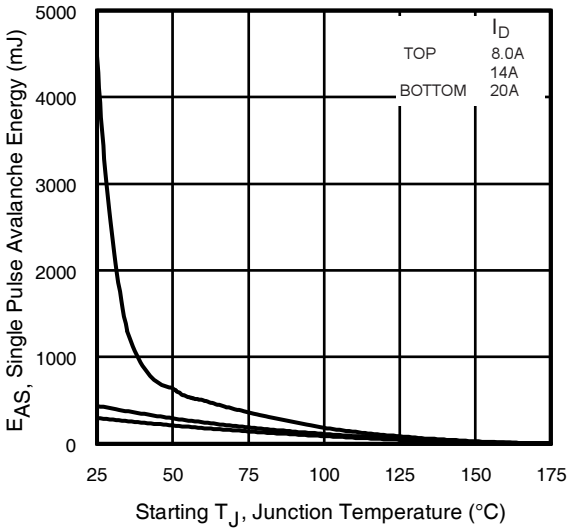


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

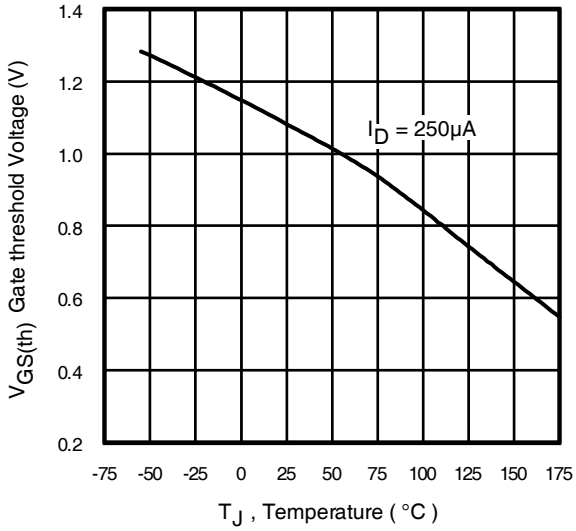


Fig 13. Threshold Voltage Vs. Temperature

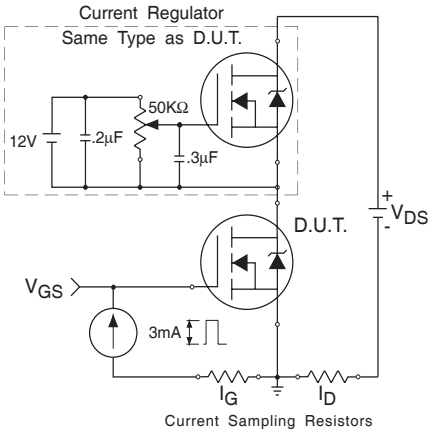


Fig 14. Gate Charge Test Circuit

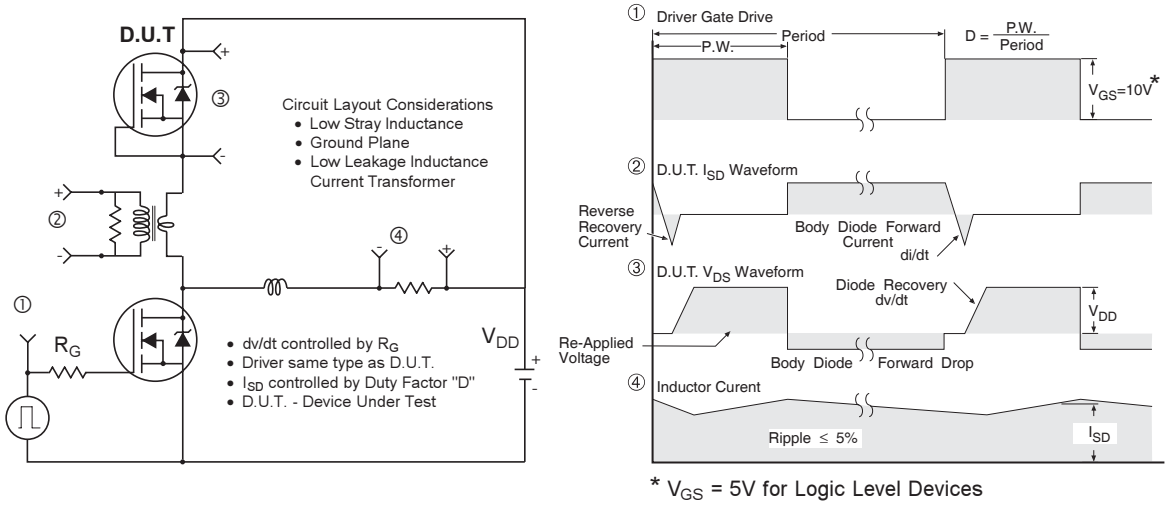


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

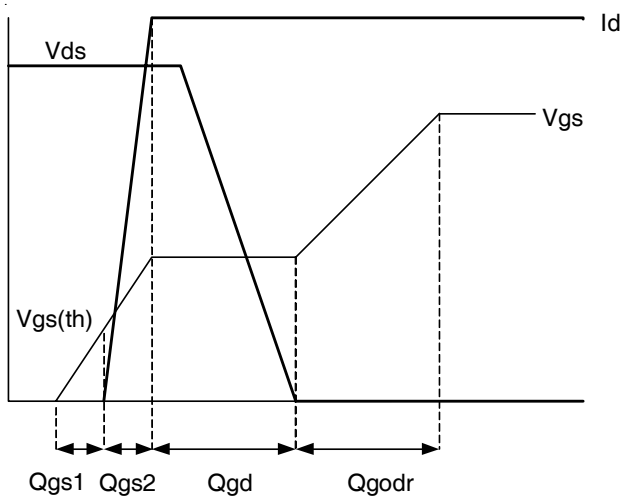
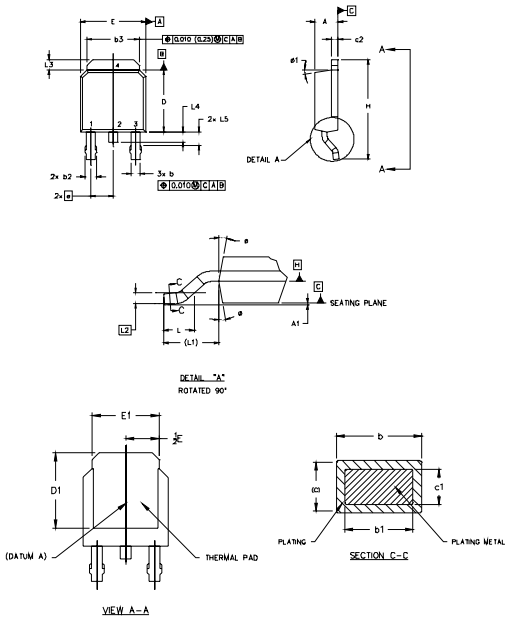


Fig 16. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0 LEAD DIMENSION UNCONTROLLED IN L5.
4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.78	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170		4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.061 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

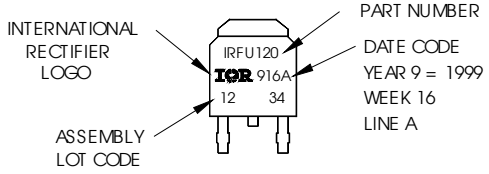
HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

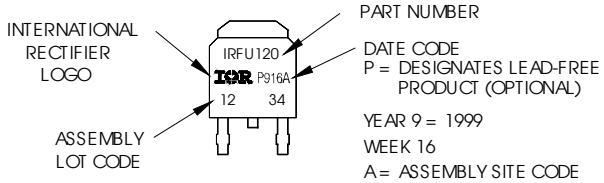
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

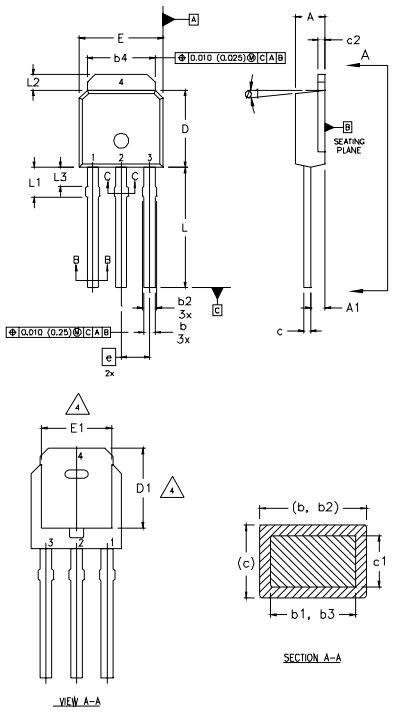


OR



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5. LEAD DIMENSION UNCONTROLLED IN L3.
6. DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7. OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8. CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	-	0.205	-	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	-	0.170	-	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

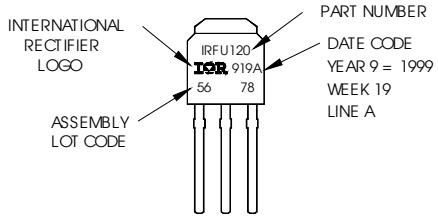
HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

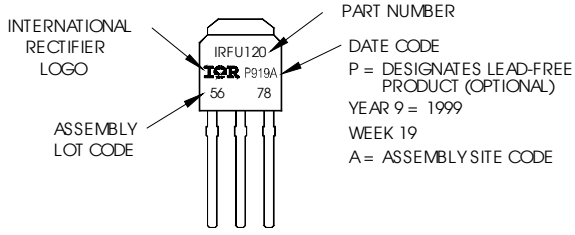
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"



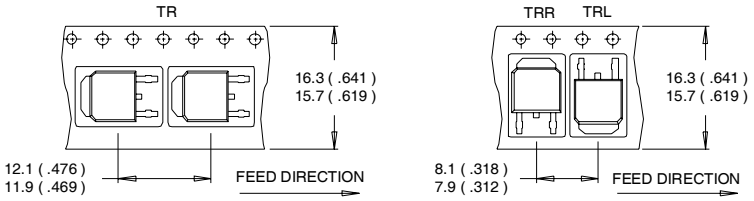
OR



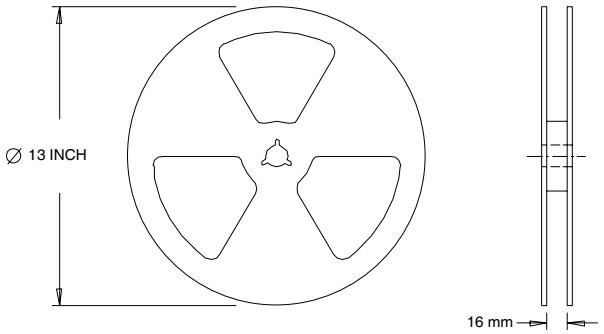
International
IOR Rectifier

D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.4mH R_G = 25Ω, I_{AS} = 20A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrialmarket.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.12/04

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/

Appendix II:

Reconfigurable HV Controller based SC DC-DC Converter

The block diagram of the reconfigurable controller based SC DC-DC converter is shown in Figure 1. The overall functional blocks of the reconfigurable controller basically consists of an SC DC-DC converter, a digital-analog-converter (DAC) and an amplifier. The amplifier will be controlled by the DAC, which converts a digital input to an analog output. The amplifier functions as a level shifter to magnify the input based on a voltage reference. The voltage reference is provided by the SC DC-DC converter.

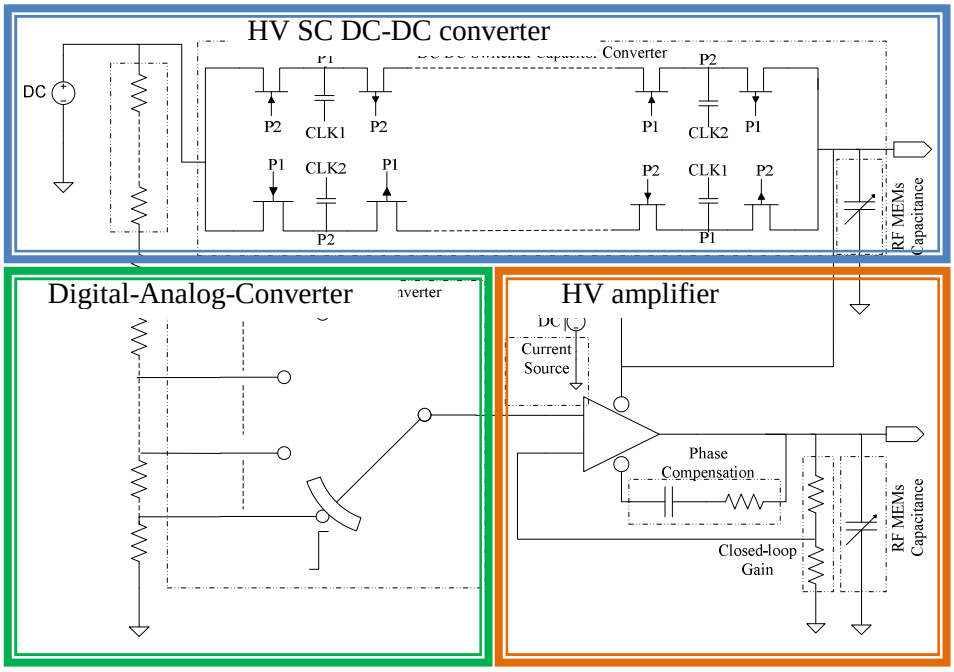


Figure 1: Structure of the reconfigurable controller based SC DC-DC converter

The reconfigurable controller based on the SC DC-DC converter has been simulated at the post layout level using a 0.35 µm CMOS technology with a supply voltage of 3.3 V. Figure 2 shows the post layout simulation of the controller. The SC DC-DC converter maintains a nearly constant high output voltage level to support the amplifier for variable output voltages. The overall current consumption is 2.2mA, giving a dissipated power of 7.26mW.

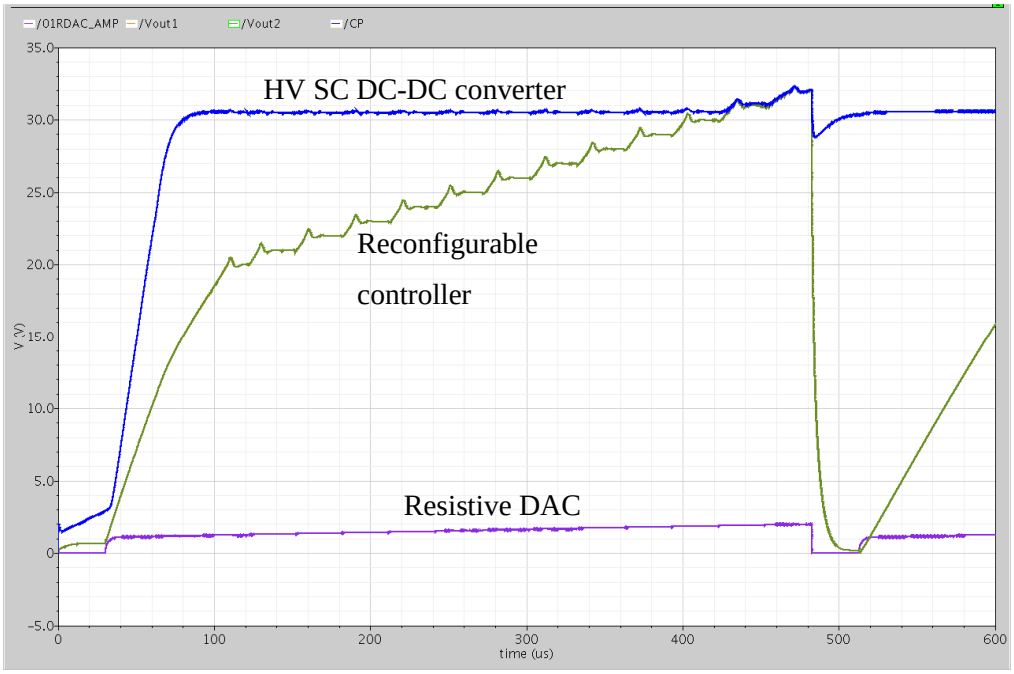


Figure 2: Post layout simulation to the reconfigurable controller based on high voltage SC DC-DC converter

Appendix III:

Data sheet of semiconductor hyper abrupt junction tuning varactors

DATA SHEET

SMV123x Series: Hyperabrupt Junction Tuning Varactors

Applications

- Low tuning voltage VCOs
- High-Q resonators in wireless system VCOs
- High-volume commercial systems

Features

- High capacitance ratio
- Low series resistance for low phase noise
- Packages rated MSL1, 260 °C per JEDEC J-STD-020

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The SMV123x series of silicon hyperabrupt junction varactor diodes are designed for use in Voltage Controlled Oscillators (VCOs) with a low tuning voltage operation. The low resistance of these varactors makes them appropriate for high-Q resonators in wireless system VCOs to frequencies over 2.5 GHz. This family of varactors is characterized for capacitance and resistance over temperature.

Table 1 describes the various packages and markings of the SMV123x varactors.

Table 1. Packaging and Marking

					
Single	Single	Single	Common Cathode	Common Anode	Common Cathode
SC-79 Green™	SOD-323 Green™	SOT-23	SOT-23	SC-70	SC-70
					SMV1231-074 Marking: JA3
SMV1231-079LF Marking: Cathode	**SMV1231-011LF** Marking: KA				**SMV1231-074LF** Green™ Marking: KA3
					SMV1232-074 Marking: CC3
SMV1232-079LF Marking: Cathode	**SMV1232-011LF** Marking: HC				**SMV1232-074LF** Green™ Marking: HC3
		SMV1233-001 Marking: VP1	**SMV1233-004** Marking: VP3		**SMV1233-074** Marking: VP3
SMV1233-079LF Marking: Cathode	♦ **SMV1233-011LF** Marking: DP	**SMV1233-001LF** Green™ Marking: DP1	**SMV1233-004LF** Green™ Marking: DP3		**SMV1233-074LF** Green™ Marking: DP3
		SMV1234-001 Marking: VQ1	**SMV1234-004** Marking: VQ3	**SMV1234-073** Marking: VQ9	
SMV1234-079LF Marking: Cathode	♦ **SMV1234-011LF** Marking: DQ	**SMV1234-001LF** Green™ Marking: DQ1	**SMV1234-004LF** Green™ Marking: DQ3	**SMV1234-073LF** Green™ Marking: DQ9	
		SMV1235-001 Marking: VR1	**SMV1235-004** Marking: VR3		**SMV1235-074** Marking: VR3
SMV1235-079LF Marking: Cathode	**SMV1235-011LF** Marking: DR	**SMV1235-001LF** Green™ Marking: DR1	**SMV1235-004LF** Green™ Marking: DR3		**SMV1235-074LF** Green™ Marking: DR3
		SMV1236-001 Marking: AQ1	**SMV1236-004** Marking: AQ3		**SMV1236-074** Marking: AQ3
♦ **SMV1236-079LF** Marking: Cathode	**SMV1236-011LF** Marking: EQ	**SMV1236-001LF** Green™ Marking: EQ1	**SMV1236-004LF** Green™ Marking: EQ3		**SMV1236-074LF** Green™ Marking: EQ3
		SMV1237-001 Marking: VT1			
		SMV1237-001LF Green™ Marking: DT1			
Ls = 0.7 nH	Ls = 1.5 nH	Ls = 1.5 nH	Ls = 1.5 nH	Ls = 1.4 nH	Ls = 1.4 nH

The Pb-free symbol or "LF" in the part number denotes a lead-free, RoHS-compliant package unless otherwise noted as Green™. Tin/lead (Sn/Pb) packaging is not recommended for new designs.

Innovation to Go™
Select Linear Products (indicated by ♦) now available for purchase online.

Electrical and Mechanical Specifications

The absolute maximum ratings of the SMV123x varactors are provided in Table 2. Electrical specifications are provided in Table 3. Typical capacitance values are listed in Table 4. Typical performance characteristics of the SMV123x varactors are illustrated in Figures 1 through 4.

The SPICE model for the SMV123x varactors is shown in Figure 5 and the associated model parameters are provided in Table 5.

Package dimensions are shown in Figures 6 to 12 (even numbers), and tape and reel dimensions are provided in Figures 7 to 13 (odd numbers).

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SMV123x series of varactors are rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. They can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

Table 2. SMV123x Absolute Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Units
Reverse voltage	V_R			15	V
Forward current	I_F			20	mA
Power dissipation	P_{DIS}			250	mW
Operating temperature	T_{OP}	–55		+125	°C
Storage temperature	T_{STG}	–55		+150	°C

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times. The SMV123x varactors are Class 1B Human Body Model (HBM) ESD devices.*

Table 3. SMV123x Electrical Specifications (Note 1)
(T_{OP} = 25 °C, Unless Otherwise Noted)

Part Number	C_T @ 1 V (pF)		C_T @ 3 V (pF)	C_T @ 6 V (pF)	$\frac{C_T \text{ @ 1 V}}{C_T \text{ @ 3 V}}$ (Ratio)		$\frac{C_T \text{ @ 1 V}}{C_T \text{ @ 6 V}}$ (Ratio)		R_S @ 3 V, 500 MHz (Ω)
	Min.	Max.	Typ.	Typ.	Min.	Max	Min.	Max.	Typ.
SMV1231	1.43	1.72	0.97	0.61	1.5	1.8	2.5	2.8	2.90
SMV1232	2.34	2.86	1.50	0.94	1.5	1.9	2.6	3.3	1.50
SMV1233	3.00	3.60	1.80	1.10	1.5	1.9	2.6	3.3	1.20
SMV1234	5.85	7.15	3.60	2.00	1.6	2.0	2.8	3.4	0.80
SMV1235	10.35	12.65	6.40	3.60	1.6	2.0	2.9	3.4	0.60
SMV1236	15.50	18.50	9.20	5.30	1.6	2.0	3.0	3.5	0.50
SMV1237	45.00	54.00	26.90	14.40	1.6	2.0	3.0	3.5	0.40

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Tested with -079 package.

Reverse voltage V_R (I_R = 10 µA) = 15 V minimum
Reverse current I_R (V_R = 12 V) = 20 nA maximum

Table 4. Capacitance vs Reverse Voltage

V_R (V)	C_T (pF)						
	SMV1231	SMV1232	SMV1233	SMV1234	SMV1235	SMV1236	SMV1237
0	2.35	4.15	5.08	9.63	18.22	26.75	71.82
0.5	1.87	3.22	3.95	7.53	14.12	20.61	56.10
1.0	1.58	2.67	3.28	6.28	11.67	17.02	46.89
1.5	1.40	2.28	2.80	5.39	9.91	14.38	40.33
2.0	1.22	1.97	2.41	4.68	8.52	12.29	35.13
2.5	1.09	1.72	2.09	4.09	7.36	10.56	30.71
3.0	0.970	1.51	1.82	3.58	6.40	9.16	26.87
3.5	0.882	1.35	1.62	3.15	5.62	8.04	23.57
4.0	0.794	1.22	1.45	2.81	4.99	7.19	20.83
4.5	0.732	1.13	1.33	2.54	4.50	6.53	18.62
5.0	0.683	1.05	1.24	2.32	4.11	6.01	16.87
5.5	0.648	0.99	1.16	2.15	3.80	5.61	15.48
6.0	0.613	0.94	1.10	2.02	3.55	5.28	14.36
6.5	0.590	0.90	1.05	1.90	3.34	5.02	13.46
7.0	0.567	0.86	1.01	1.80	3.17	4.81	12.72
7.5	0.551	0.84	0.98	1.72	3.03	4.64	12.11
8.0	0.534	0.81	0.96	1.65	2.91	4.49	11.61
9.0	0.512	0.78	0.92	1.55	2.73	4.28	10.87
10.0	0.497	0.76	0.90	1.47	2.61	4.13	10.38
11.0	0.492	0.75	0.88	1.42	2.53	4.02	10.06
12.0	0.487	0.74	0.87	1.38	2.47	3.95	9.84
13.0	0.480	0.73	0.86	1.35	2.43	3.89	9.68
14.0	0.472	0.73	0.85	1.33	2.40	3.84	9.56
15.0	0.466	0.72	0.84	1.32	2.38	3.80	9.47

Typical Performance Characteristics

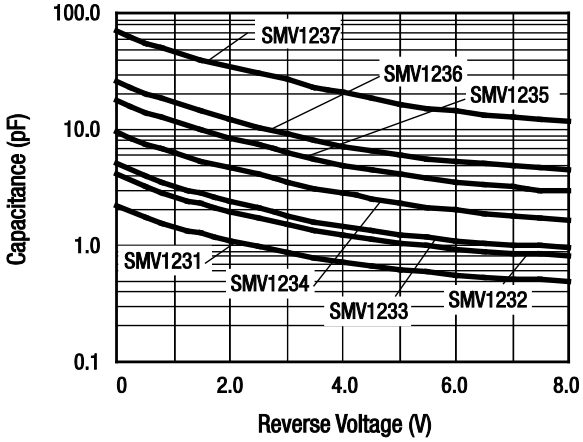


Figure 1. Capacitance vs Reverse Voltage

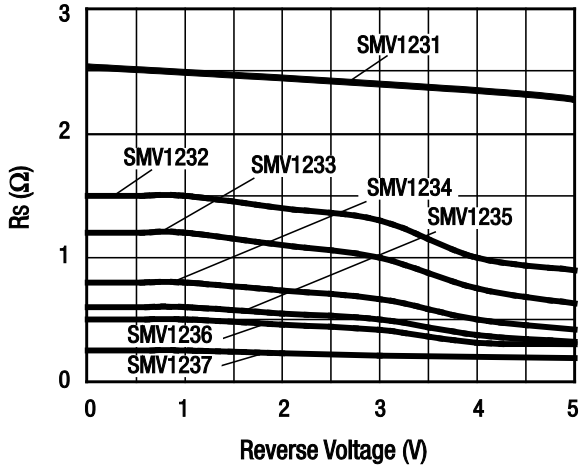


Figure 2. Series Resistance vs Reverse Voltage @ 500 MHz

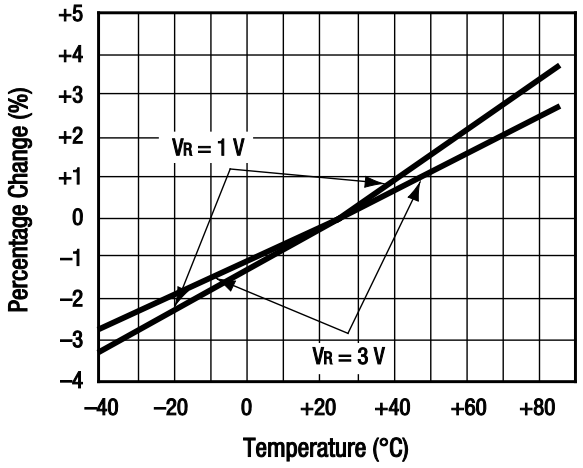


Figure 3. Relative Capacitance Change vs Temperature

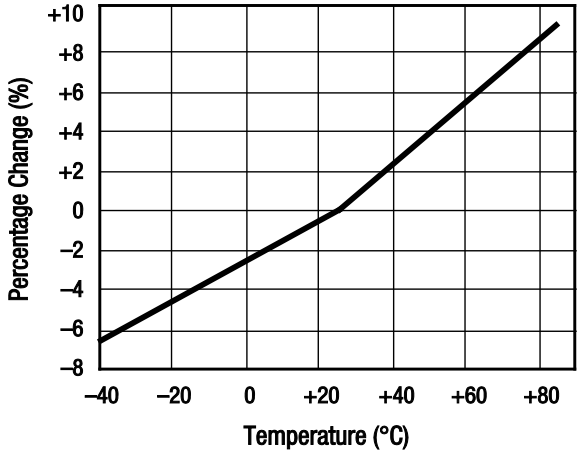


Figure 4. Relative Series Resistance Change vs Temperature @ 500 MHz

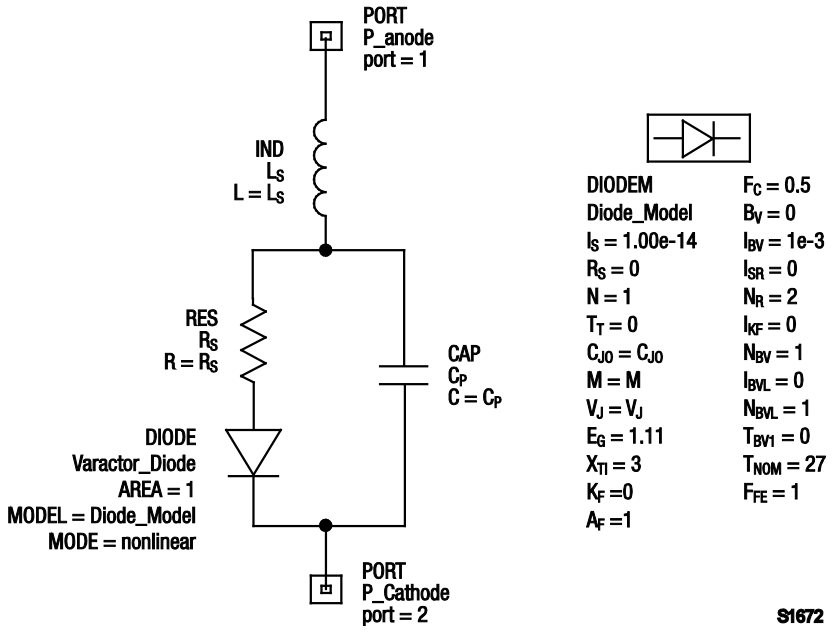


Figure 5. SPICE Model

Table 5. SPICE Model Parameters

Part Number	C_{J0} (pF)	V_J (V)	M	C_P (pF)	R_S (Ω)
SMV1231	1.88	10.13	4.999	0.44	2.50
SMV1232	3.43	8.36	4.690	0.68	1.50
SMV1233	4.21	11.87	6.430	0.81	1.20
SMV1234	8.36	7.95	3.960	1.15	0.80
SMV1235	15.85	8.78	4.570	2.15	0.60
SMV1236	22.89	9.62	5.230	3.59	0.50
SMV1237	61.40	14.51	6.780	8.90	0.25

Values extracted from measured performance.
For package inductance (L_S), refer to Table 1.
For more details, refer to the Skyworks Application Note, *Varactor SPICE Model for Approved RF VCO Applications*, document number 200315.

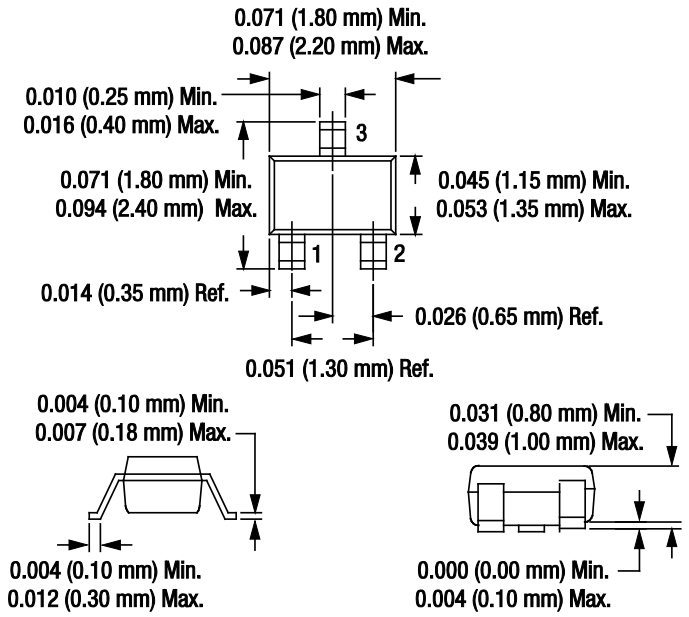
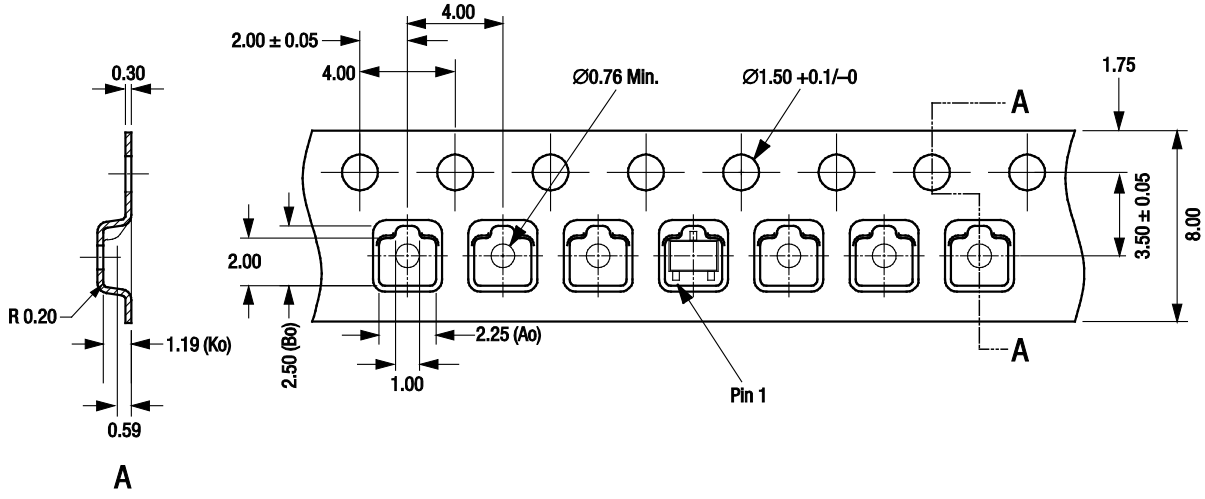


Figure 6. SC-70 Package Dimensions



Notes:
1. *Carrier tape: black conductive polystyrene bakeable material at 125 °C.*
2. *Cover tape material: transparent conductive PSA.*
3. *Cover tape size: 5.40 mm width.*
4. *ESD surface resistivity is ≥1 x 10^4 and approx. ≤1 x 10^9 Ohms/square per EIA, JEDEC TNR Specification.*
5. *All measurements are in millimeters.*

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Figure 7. SC-70 Tape and Reel Dimensions

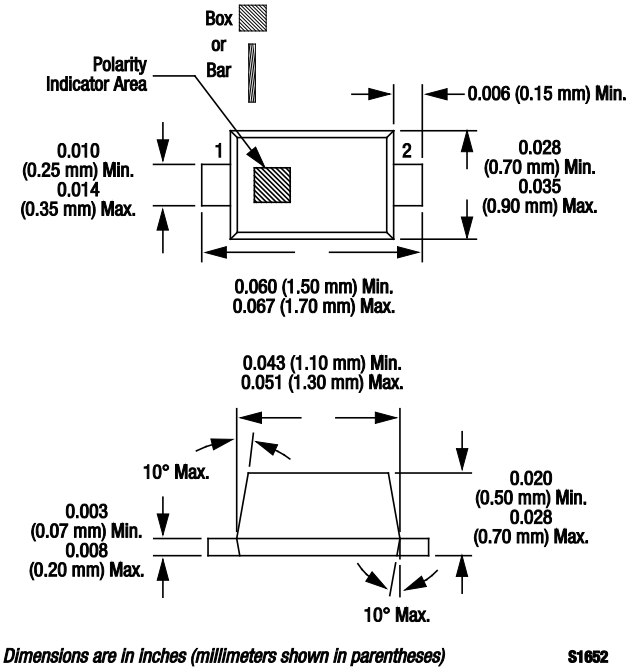


Figure 8. SC-79 Package Dimensions

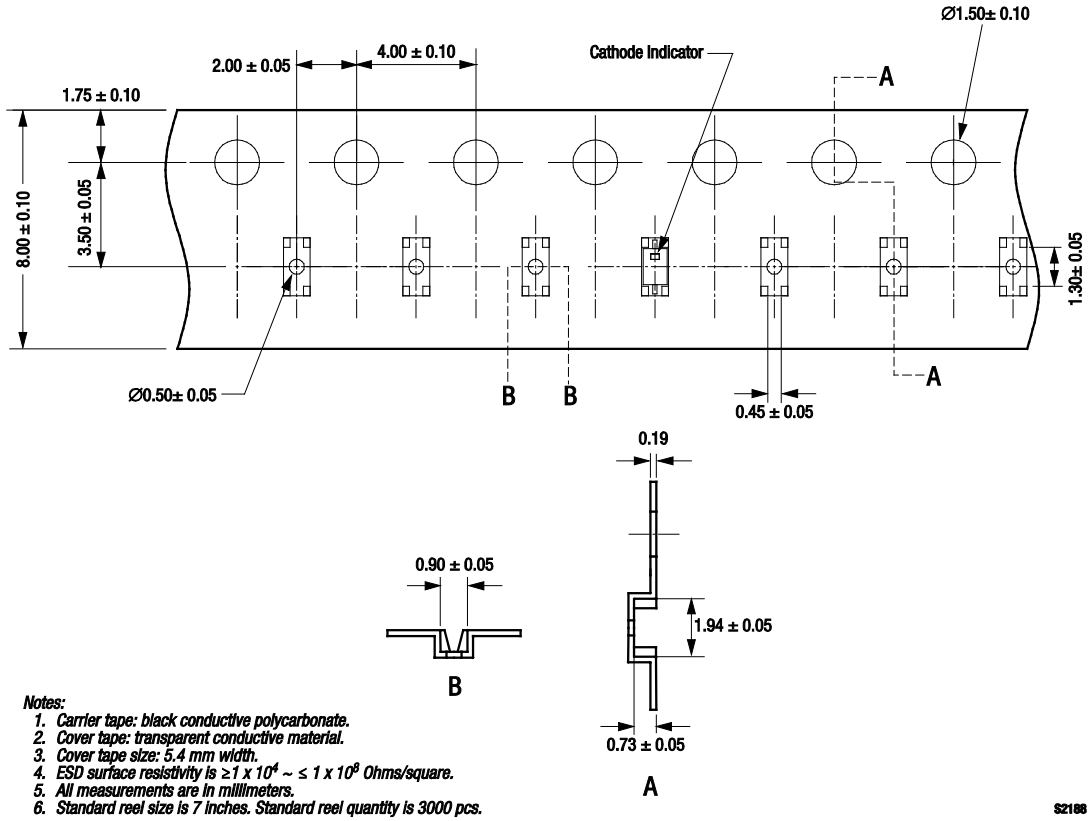


Figure 9. SC-79 Tape and Reel Dimensions

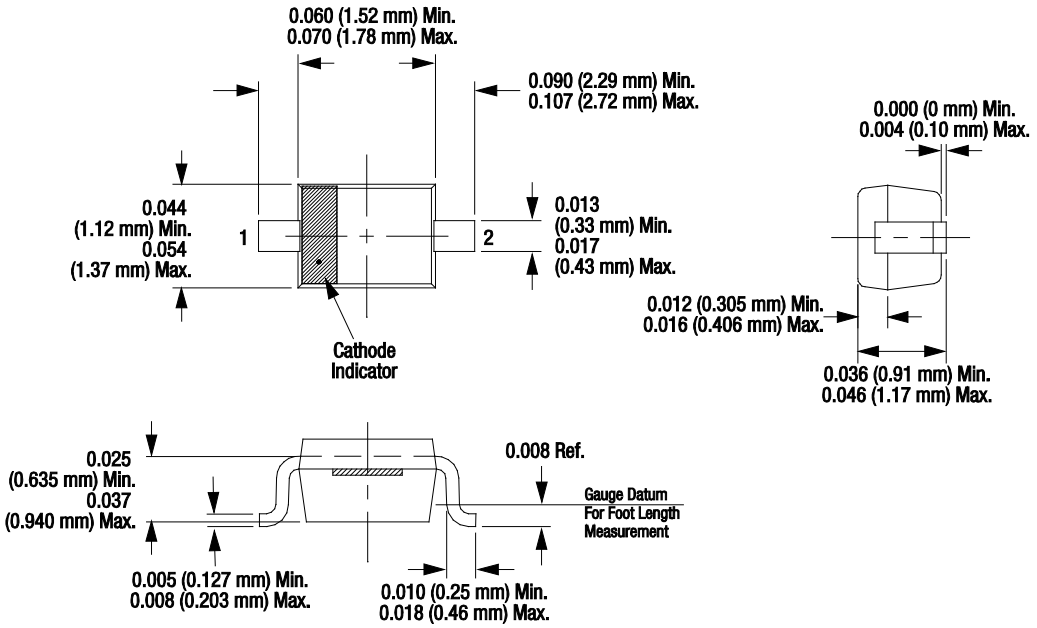
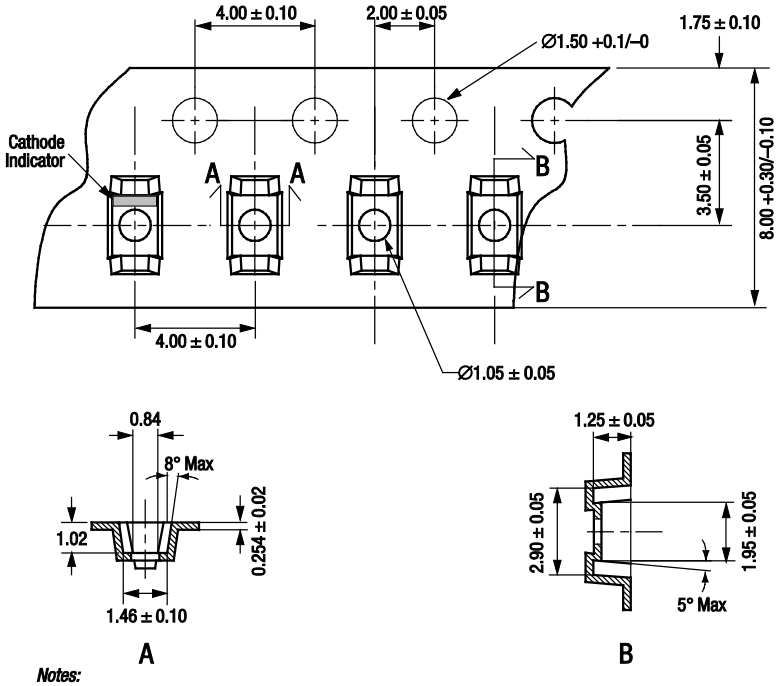


Figure 10. SOD-323 Package Dimensions



Notes:

1. *Carrier tape: black conductive polycarbonate or polystyrene.*
2. *Cover tape: transparent conductive material.*
3. *Cover tape size: 5.5 mm width.*
4. *ESD surface resistivity is ≥1 x 10^5 ~ ≤ 1 x 10^{11} Ohms/square.*
5. *10 sprocket hole pitch cumulative tolerance: ±0.20 mm.*
6. *Ao and Bo measured on plane 0.30 mm above bottom of the pocket.*
7. *All measurements are in millimeters.*
8. *Standard reel size is 7 inches. Standard reel quantity is 3000 pcs.*

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Figure 11. SOD-323 Tape and Reel Dimensions

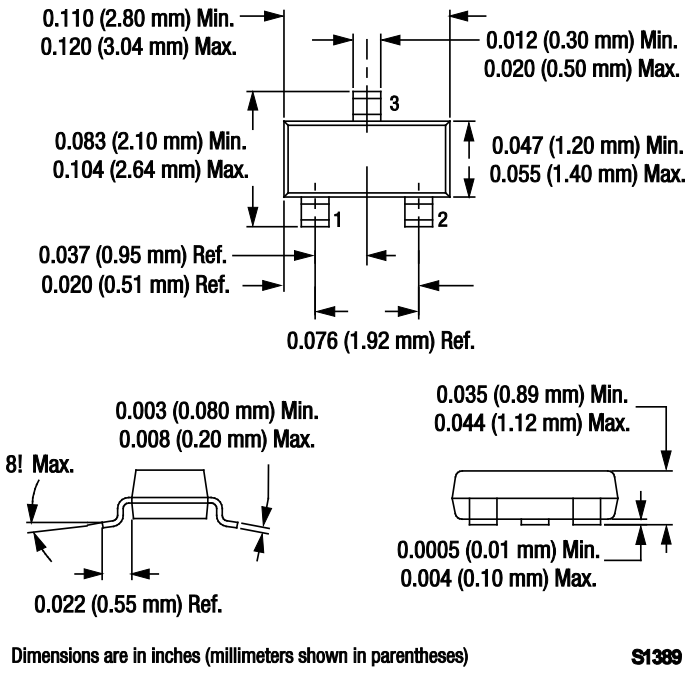


Figure 12. SOT-23 Package Dimensions

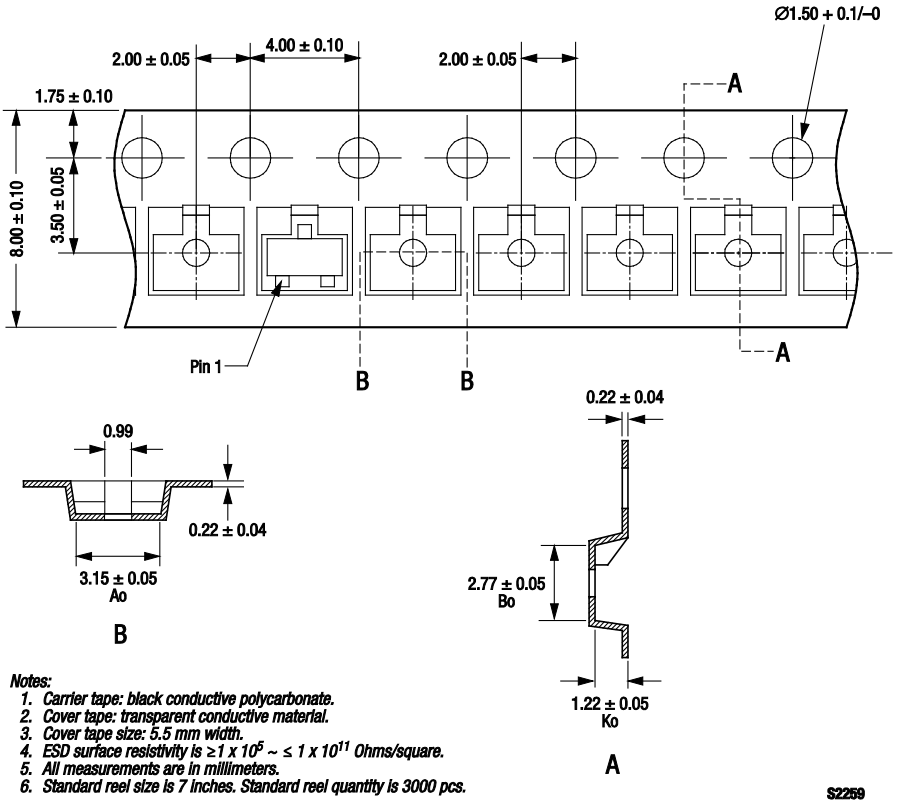
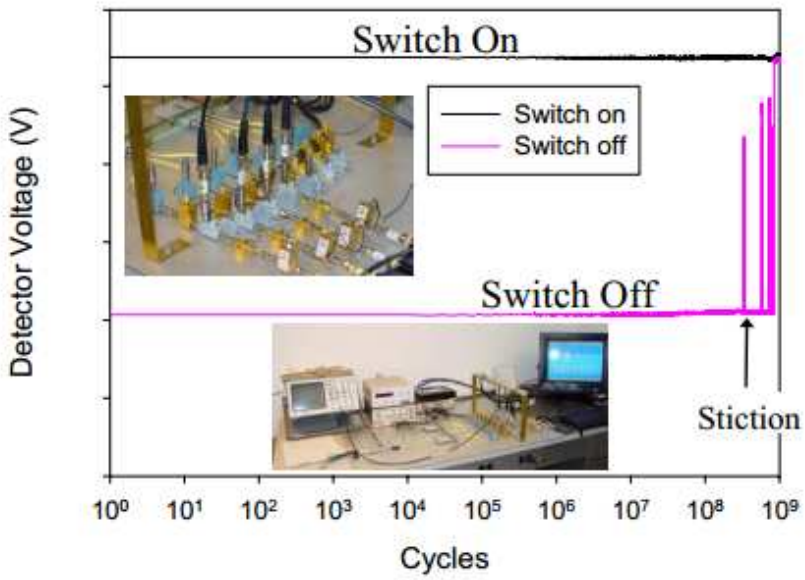


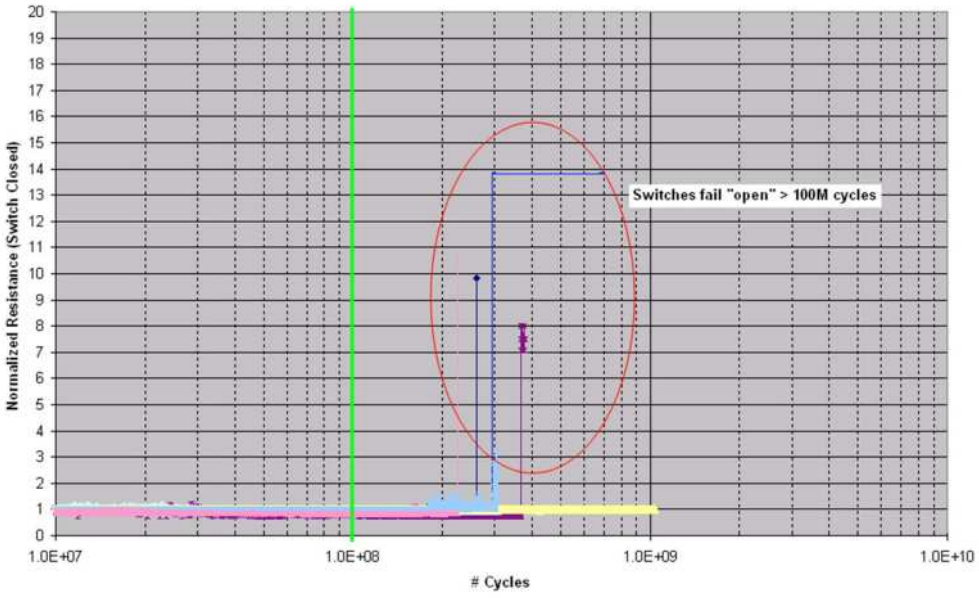
Figure 13. SOT-23 Tape and Reel Dimensions

Appendix IV:

RF life time testing of RF MEMS switches



RF lifetime testing at 10GHz for RADANT 8-MEMS switch with 11 dBm of input power. Stable contact resistance is seen over the life of the switch. Intermittent sticks start to appear at approximately 500 million cycles [147].



Hot switching testing of RFMD MEMS switch with 0dBm achieves 117 million cycles before failed [160].