
THE UNIVERSITY
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# Harmonic Modelling and Characterisation of Modern Power Electronic Devices in Low Voltage Networks

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# Abstract

Although the overall levels of harmonics in modern power supply systems are in most of the practical cases still below the prescribed tolerance limits and thresholds (e.g. these stipulated in [IEC 61000-3-2 and 61000-3-12]), the sources of harmonics are constantly increasing in numbers and are expected to increase even more in the future. Some of the examples of modern non-linear power electronic (PE) devices that are expected to be employed on a much wider scale in LV networks in the future include: light-emitting diode (LED) lamps, switched-mode power supplies (SMPS'), electric vehicle battery chargers (EVBCs) and photovoltaic inverters (PVIs), which are all analysed in this thesis.

The thesis first reviews the conventional harmonic analysis methods, investigating their applicability to modern PE devices. After that, the two most widely used forms of harmonic models, i.e. component-based models (CBMs) and frequency-domain models (FDMs), are applied for modelling of the four abovementioned types of modern PE devices and their models are fully validated by measurements. The thesis next investigates the impact of supply voltage conditions and operating modes (e.g. low vs high operating powers) on the device characteristics and performance, using both measurements and developed CBMs and FDMs. The obtained results confirm that both supply conditions and operating modes have an impact on the characteristics of most of the considered PE devices, which is taken into account in the developed models and demonstrated on a number of case studies.

As the next contribution, the thesis proposes new indices for the evaluation of current waveform distortions, allowing for a separate analysis of contributions of low and high frequency harmonics and interharmonics to the total waveform distortion of PE devices. As the modern PE devices are normally based on high-frequency switching converters or inverters, the impact of circuit topologies and control algorithms on their harmonic emission characteristics and performance is also investigated. Special attention is given to the operation of PE devices at low powers, when there is a significant increase of current waveform distortion, a substantial decrease of efficiency

and power factors and when input ac current might lose its periodicity with the supply voltage frequency. This is analysed in detail for SMPS', resulting in the proposal of a new methodology ("operating cycle based method") for evaluating overall performance of PE devices across the entire range of operating powers.

Finally, a novel and simple hybrid harmonic modelling technique, allowing for the use of both time-domain and frequency-domain models in the same simulation environment, is proposed and illustrated on the selected case studies. This is accompanied with a frequency-domain aggregation approach, which is applied in the thesis to investigate the impact of increasing numbers of different types of modern PE devices on the LV network. The implementation of the developed hybrid harmonic modelling approach and frequency-domain aggregation technique is demonstrated on the example of a typical (UK) urban generic LV distribution network and used for the analysis of different deployment levels of EVs and PVIs. The presented harmonic modelling framework for individual PE devices and, particularly, for their aggregate models, fills the gap in the existing literature on harmonic modelling and characterisation of modern PE devices, which is important for the correct evaluation of their harmonic interactions and analysis of the impact of their large-scale deployment on the overall network performance.

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# Declaration

I declare that this thesis was composed by myself, that the work contained herein is my own except where explicitly stated otherwise in the text, and that this work has not been submitted for any other degree or professional qualification except as specified.

Xiao Xu

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# Acronyms and abbreviations

| | |
|---|---|
| ac | Alternating current |
| ADC | Analog-to-digital |
| ADMD | After diversity maximum demand |
| a-PFC | Active power factor correction |
| CBM | Component-based model |
| CC | Constant current |
| CCCV | Constant-current constant-voltage |
| CCR | Constant current regulator |
| CCSM | Constant (harmonic) current source model |
| CC-StrongNeg | Constant current-strong negative |
| CF | Crest factor |
| CFL | Compact fluorescent lamp |
| CHNM | Coupled harmonic Norton model |
| CI | Constant impedance |
| CI (Neg) | Constant impedance (negative) |
| CP | Constant power |
| CP-StrongNeg | Constant power-strong negative |
| CV | Constant voltage |
| dc | Direct current |
| DFT | Discrete Fourier transform |
| DG | Distributed generation |
| DHNM | Decoupled harmonic Norton model |
| EHV | Extra high voltage |
| EMI | Electromagnetic interference |

| | |
|---|---|
| EMT | Electromagnetic transient |
| FB | Full-bridge |
| EV | Electric vehicle |
| EVBC | Electric vehicle battery charger |
| FDM | Frequency-domain model |
| FDS | Frequency-domain simulation |
| FFT | Fast Fourier Transform |
| HAM | Harmonic admittance matrix |
| $HAM_{\%}$ | Harmonic admittance matrix in percentage |
| $HAM_{N}$ | Norton harmonic admittance matrix |
| $HAM_{N\_\%}$ | Norton harmonic admittance matrix in percentage |
| HF | High frequency |
| HFM | Harmonic fingerprint model |
| HV | High voltage |
| IGBT | Insulated-gate bipolar transistor |
| IHA | Iterative harmonic analysis |
| InC | Incremental conductance |
| LED | Light-emitting diode |
| LF | Low frequency |
| LV | Low voltage |
| MC | Monte Carlo |
| MOSFET | Metal-oxide-semiconductor field-effect transistor |
| MOV | Metal-oxide varistor |
| MPP | Maximum power point |
| MPPT | Maximum power point tracking |
| MV | Medium voltage |

| | |
|---|---|
| no-PFC | Without power factor correction |
| PC | Personal computer |
| PCC | Point of common coupling |
| PDF | Probability density function |
| PE | Power electronic |
| PFC | Power factor correction |
| PI | Proportional Integral |
| PMF | Probability mass function |
| P&O | Perturb and observe |
| p-PFC | Passive power factor correction |
| PQ | Power quality |
| PR | Proportional Resonant |
| pu | Per-unit |
| PV | Photovoltaics |
| PVI | Photovoltaic inverter |
| PWM | Pulse width modulation |
| SCR | Silicon controlled rectifier |
| SMPS | Switched-mode power supply |
| SoC | State of charge |
| StrongPos | Strong positive |
| TDM | Time-domain model |
| TDS | Time-domain simulation |
| RTM | Regression tree model |
| VUF | Voltage unbalance factor |

# Nomenclature

| | |
|---|---|
| $C_{dc}$ | dc-link capacitor |
| $D$ | Duty ratio |
| $D_I$ | Current distortion power |
| $D_V$ | Voltage distortion power |
| $E_{range}$ | Range uncertainty |
| $E_{reading}$ | Reading uncertainty |
| $f$ | Frequency |
| $F_{AA}$ | Aging acceleration factor |
| $FF$ | Fundamental factor |
| $F_{HL}$ | Harmonic loss factor for winding eddy currents |
| $F_{HL\text{-}STR}$ | Harmonic loss factor for the other stray losses |
| $h$ | Harmonic order |
| $h_{max}$ | Maximum harmonic order considered |
| $i_{ac}$ | Instantaneous ac current |
| $I_{dc}$ | dc component of input ac current |
| $I_{dc,eq}$ | Equivalent dc constant current |
| $i_{dc\text{-}5}$ | Instantaneous current at 5 V dc output of PC-SMPS |
| $i_{dc\text{-}12}$ | Instantaneous current at 12 V dc output of PC-SMPS |
| $I_f$ | Diode forward current |
| $I_{f\text{-}spec}$ | Spectrum component of input ac current at frequency $f$ |
| $I_h$ | The rms value of individual current harmonic of order $h$ |
| $I_H$ | The rms value of the sum of all considered current harmonics |
| $I_{isg,h}$ | Subgroup interharmonic current of order $h$ |
| $\hat{I}_{L,lower}$ | Peak value for the lower boundary of the inductor current |

| | |
|---|---|
| $\hat{I}_{L,upper}$ | Peak value for the upper boundary of the inductor current |
| $I_{max}$ | Maximum permissible current |
| $I_{MPP}$ | Maximum power point current of PV panels |
| $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$ | Fundamental and harmonic components of ac current |
| $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\%}$ | Current harmonic spectrum |
| $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{N}}$ | Norton current source |
| $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{1pu}}$ | $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$ of device under ideal supply condition |
| $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\%\_\boldsymbol{1pu}}$ | Current harmonic spectrum of device under ideal supply condition |
| $i_{pv}$ | Instantaneous output current of PV array |
| $I_{req}$ | Regulated current value |
| $I_{rated}$ | The rms value of the rated current |
| $I_s$ | Reverse saturation current of LED |
| $I_{sg,h}$ | Subgroup harmonic current of order *h* |
| $I_{tot}$ | Total operating current |
| $I_1$ | The rms value of fundamental component of ac current |
| $I_{1\text{-}rms}$ | rms value of the current on the transformer primary side |
| $\bar{I}^1$ | Fundamental component of ac current |
| $\bar{I}^1_{1pu}$ | $\bar{I}^1$ of device under ideal supply condition |
| $\bar{I}^1_{Tot}$ | Fundamental component of total current |
| $I_{2\text{-}rms}$ | rms value of the current on the transformer secondary side |
| $I_{2\text{-}h}$ | *h*-order current harmonic at the transformer secondary side |
| $I_{2\text{-}R}$ | Rated current at the transformer secondary side |
| $K_P$ | Proportional gain term |
| $K_I$ | Integral gain term |
| $L_{in}$ | Input-side inductance |

| | |
|---|---|
| $n$ | Maximum considered harmonic order in FDMs |
| $N$ | Nonactive power |
| $n_p$ | Exponential model coefficient for active power |
| $n_q$ | Exponential model coefficient for reactive power |
| $P$ | Active power |
| $P_{DC}$ | Ohmic loss |
| $P_{dc,eq}$ | Equivalent dc constant power |
| $P_{DC\text{-}R}$ | Ohmic loss under rated conditions |
| $P_{EC}$ | Eddy current loss |
| $P_{EC\text{-}R}$ | Eddy current loss under rated conditions |
| $PF$ | Power factor |
| $PF_d$ | Distortion power factor |
| $PF_1$ | Displacement power factor |
| $P_H$ | Harmonic active power |
| $P_{in,ac}$ | Input ac active power of PE device |
| $P_{in,H}$ | Total harmonic active power at the input ac side of PE device |
| $P_{in,1}$ | Fundamental active power at the input ac side of PE device |
| $P_{LL}$ | Load losses |
| $P_{LL\text{-}R}$ | Load losses under rated conditions |
| $P_{NL}$ | Non-load losses |
| $P_{NL\text{-}R}$ | Non-load losses under rated conditions |
| $P_{OSL}$ | Other stray loss |
| $P_{OSL\text{-}R}$ | Other stray loss under rated conditions |
| $p_{pv}$ | Instantaneous power output of PV array |
| $P_T$ | Transformer total power losses |
| $P_0$ | Active power at nominal 1 p.u. supply voltage $V_0$ |

| | |
|---|---|
| $P_1$ | Fundamental active power |
| $q$ | Electron charge ($1.602e^{-19}$ Coulombs) |
| $Q$ | Reactive power |
| $Q_H$ | Harmonic reactive power |
| $Q_0$ | Reactive power at nominal 1 p.u. supply voltage $V_0$ |
| $Q_1$ | Fundamental reactive power |
| $R_{batt}$ | Battery resistance |
| $R_{DC}$ | dc resistance of all windings |
| $R_{eq}$ | Equivalent resistance |
| $R_{in}$ | Input-side resistance |
| $R_{on}$ | Series intrinsic resistance of LED |
| $R_p$ | Parallel parasitic resistance |
| $S$ | Apparent power |
| $S_H$ | Harmonic apparent power |
| $S_{in,ac}$ | Input ac apparent power of PE device |
| $S_{in,1}$ | Fundamental apparent power at the input ac side of PE device |
| $S_1$ | Fundamental apparent power |
| $TDC$ | Total distortion content |
| $TDD$ | Total demand distortion |
| $TDD_{sg}$ | Subgroup total demand distortion |
| $THC$ | Total harmonic current |
| $THCS$ | Subgroup total harmonic current |
| $THD_I$ | Total current harmonic distortion |
| $THD_V$ | Total voltage harmonic distortion |
| $THDS_I$ | Subgroup total harmonic distortion of current |
| $THDS_V$ | Subgroup total harmonic distortion of voltage |

| | |
|---|---|
| $THF_{LF}$ | Total LF harmonic factor |
| $TH\&IHC_{HF}$ | Total high-frequency harmonic and interharmonc current |
| $TH\&IHD_{I,HF}$ | Total high-frequency harmonic and interharmonc distortion |
| $TIHDS_I$ | Subgroup total interharmonic distortion of current |
| $TIHDS_V$ | Subgroup total interharmonic distortion of voltage |
| $TNHDF$ | Total non-(LF)-harmonic distortion factor |
| $TSHCS$ | Subgroup total subharmonic current |
| $TSHDS_I$ | Subgroup total subharmonic distortion of current |
| $TSHDS_V$ | Subgroup total subharmonic distortion of voltage |
| $v_{ac}$ | Instantaneous ac voltage |
| $v_{dc}$ | Instantaneous dc-link voltage |
| $v_{dc\text{-}5}$ | Instantaneous voltage at 5 V dc output of PC-SMPS |
| $v_{dc\text{-}12}$ | Instantaneous voltage at 12 V dc output of PC-SMPS |
| $V_{dc}$ | dc component of input ac voltage |
| $V_f$ | Diode forward voltage |
| $V_h$ | The rms value of individual voltage harmonic of order *h* |
| $V_H$ | The rms value of the sum of all considered voltage harmonics |
| $V_{h,limit}$ | Individual voltage harmonic limit specified in EN50160 |
| $V_{MPP}$ | Maximum power point voltage of PV panels |
| $\overline{\boldsymbol{V}}^{\boldsymbol{H}}$ | Fundamental and harmonic components of ac voltage |
| $\overline{\boldsymbol{V}}^{\boldsymbol{H}}_{\%}$ | Voltage harmonic spectrum |
| $V_{on}$ | Conduction voltage of LED diode |
| $v_{pv}$ | Instantaneous output voltage of PV array |
| $V_{ref}$ | Reference voltage |
| $V_{th}$ | Threshold voltage of the CCR regulation |
| $V_1$ | The rms value of the sum of all considered voltage harmonics |

| | |
|---|---|
| $\bar{V}^1$ | Fundamental component of ac voltage |
| $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}$ | HAM |
| $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\%}$ | HAM in percentage |
| $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\boldsymbol{N}}$ | Paralleled connected $HAM_N$ |
| $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\boldsymbol{N,dia}}$ | Diagonal elements of $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\boldsymbol{N}}$ |
| $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\boldsymbol{N}\_\%}$ | $HAM_N$ in percentage |
| $\theta_A$ | Ambient temperature |
| $\theta_g$ | Hottest-spot conductor rise over top-oil temperature |
| $\theta_{g\text{-}R}$ | Rated value of hottest-spot conductor rise over top-oil temperature |
| $\theta_h$ | Phase angle difference between $V_h$ and $I_h$ |
| $\theta_H$ | Hottest-spot temperature |
| $\theta_{TO}$ | Top-oil-rise over ambient temperature |
| $\theta_{TO\text{-}R}$ | Rated value of top-oil-rise over ambient temperature |
| $\omega_0$ | Resonant frequency |
| $\omega_c$ | Bandwidth around $\omega_0$ |
| $\eta$ | Efficiency |
| $\eta_1$ | Fundamental efficiency |

# Chapter 1
# Introduction

Although power system harmonics exist since the early stage of ac system, the problems utility and customers facing are changing with the advance of science and technology. Initially, the main harmonic issue is the third-order current harmonic emitted from ferromagnetic loads like the saturated iron of transformers. After that, arcing devices like the electrical arc furnaces came into the picture and became one of the main harmonic sources in the grid. The booming emergence of power electronic devices like personal computers and variable speed drives starts from the 1970s and 1980s, which bring about new harmonic issues like interharmonics and high-frequency harmonics to the grid [1]. Accordingly, the power system will normally face with different harmonic issues whenever the popularity of new electric or electronic devices appears, implying that the power system harmonic studies require to be up-to-date in order to provide corresponding harmonic mitigation solutions as well as the proper adjustment of harmonic-related standards and regulations.

With the wide applications of semiconductor devices like IGBTs, MOSFETs and SCRs in the past decades, highly diversified switched-mode converter and inverter topologies have been proposed, contributing to the improved performance of traditional power electronic (PE) devices. For example, the early-stage LED lamps, computer switched-mode power supplies (SMPS') and electric vehicle battery chargers (EVBCs) normally use the single-phase full-wave rectifiers (with smoothing capacitor) as the front-end circuits, and are featured by low power factor, high current harmonic emission and bulky dc link capacitor [2]. To improve the device performance and meet the strict power quality (PQ) requirements from the newly enforced standards, traditional full-wave rectifiers with smoothing capacitor have been gradually replaced by a variety of high-frequency switched-mode converters, resulting in the change of harmonic characteristics of PE devices. To ensure the present system operate flawlessly with the increasing and diversified harmonic sources in the future, utilities have to correctively assess the cumulative harmonic impact of modern PE

devices on the grid and the effectiveness of the harmonic mitigation solutions, on the premise of fully evaluating the harmonic modelling and characterisation of the modern PE devices.

## 1.1 The need for harmonic modelling of modern PE devices

Modern PE devices seen in LV work network vary from low power applications like LED lamps, to medium power applications like desktop PC-SMPS' and to high power applications like EVBCs, photovoltaic inverters (PVIs) and residential wind turbines, with respect to the after diversity maximum demand (ADMD) of a typical EU household which is around 2 kW [3]. Most of those devices are connected to the grid via various high-frequency switch-mode converter or inverter based circuits to achieve the ac to dc or dc to ac power conversion, where the harmonics will be generated and injected into the grid. One important feature of modern PE devices is that their harmonic characteristics are not only determined by their circuit topologies and corresponding control algorithms, but also affected by the working mode (or operating power) and the non-ideal supply conditions. Evaluating the harmonic impact of modern PE devices without properly taking into account those influencing factors, will make the obtained results questionable. Unfortunately, applying constant current source model with fixed harmonic magnitudes and phase angles for assessing the cumulative harmonic impact of PE devices is still the common practice in existing literature (e.g. [4][5]) and software (e.g. OpenDSS [6] and DigSILENT [7]).

To solve that issue, it is necessary to fully investigate the harmonic characterisation of modern PE devices under comprehensive working conditions and develop proper harmonic models which can be applied for investigating their cumulative harmonic impact on the grid.

## 1.2 Research objectives and scope

The main research objective is to develop suitable models capable of accurately representing the harmonic characteristics of modern PE devices under practical network conditions. To select proper harmonic modelling techniques, the investigation of the harmonic characteristics of modern PE devices under different supply conditions and operating modes is required and will be achieved by comprehensive laboratory

tests in this thesis. In addition, modern PE devices are normally based on high-frequency converters or inverters, and may produce harmonics, subharmonics and interharmonics at different working conditions, requiring the selection and development of appropriate harmonic analysis approaches and indices.

Based on the analysis results of the harmonic characteristics of the selected modern PE devices, both component-based models (CBMs) and frequency-domain models (FDMs) will be developed, with the model accuracy fully validated with measurements. As different harmonic model forms might be applied to different PE devices, network harmonic analysis methods of using different harmonic model forms under the same simulation environment have to be proposed. To investigate the impact of large-scale deployment of PE devices on the LV networks, developing aggregate harmonic models for multiple devices is one of the natural extensions of the proposed works.

The specific research objectives are defined as:

- To review the typical harmonic modelling techniques applicable to PE devices.
- To develop harmonic models for modern PE devices in LV networks.
- To investigate the characteristics and performance of considered modern PE devices under different supply conditions and operating powers or modes.
- To evaluate the applicability of existing harmonic analysis approaches and indices for evaluating the characteristics and performance of PE devices under nonsinusoidal conditions, as well as giving suggestions for improvement.
- To propose proper network harmonic analysis methodologies for using different harmonic model forms under the same simulation environment.
- To propose generalised harmonic aggregation approaches.

The scope and boundaries of the research are defined as:

- The research focuses on the rapidly growing PE devices found in LV networks, including LED lamps, SMPS', EVBCs and residential-scale PVIs.
- The characteristics and performance of PE devices operating at the ideal supply condition (i.e. sinusoidal supply voltage with magnitude of 1 p.u. and zero

source impedance) with rated power are used as the reference for evaluating the impact of non-ideal supply conditions.

- For the laboratory tests of PE devices considered in the thesis, the change of supply conditions refers to the combinations of different supply voltage magnitudes, waveform distortions and source impedances. Specifically, the supply voltage magnitude is adjusted from 0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u., considering the fact that typical supply voltage variations are within ±10% of the nominal voltage (230 V). Regarding the applied supply voltage waveforms, three representative waveforms are applied, which are a) ideally sinusoidal waveform (WF1), b) "flat-top" distorted waveform (WF2, representing the typical residential LV network), c) "pointed-top" distorted voltage waveform (WF3, representing typical industrial LV networks), with their time-domain waveform shape and corresponding harmonic spectrums illustrated in Figure 1.1. Finally, two difference source impedance values are applied separately: ZS1=0 (ignoring the negligible impedance of the connection cables between power supply and tested PE devices) and ZS2=(0.4+0.25j) Ω, representing maximum expected impedance in LV networks (e.g. this value is exceeded for only about 2% of LV customers in the UK). The laboratory testing of PE devices under considered supply conditions can provide preliminary results on the sensitivity of electrical characteristics of PE devices to the non-ideal supply conditions, even though the practical grid conditions may vary from the considered combinations.

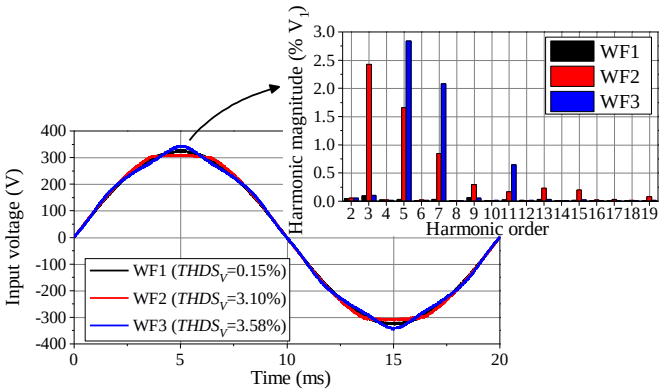



**Figure 1.1:** Illustration of the three different voltage waveforms applied in laboratory tests of considered PE devices in the thesis.

## 1.3 Main contributions of the thesis

The main results of the work have been presented in three journal papers [8] [9] [10] and 14 international conference papers [11][12][13][14][15][16][17][18][19][20][21][22][23] [24] (the full list of publications are given in Appendix A). The main contributions and related publications are summarised as the following points:

- The characteristics and performance of residential LED lamps are investigated through comprehensive laboratory tests. From these tests, 28 different lamps, being classified into four different types with the general circuit topology for each type, have been fully discussed [11]. Based on the operating principles of different circuit topologies, the generalised harmonic modelling approach for each type LED lamps is given and validated with measurements, followed by the discussion of the model aggregation approaches. The work provides preliminary results for investigating the cumulative impact of LED lamps on LV networks, as well as the other research areas like the assessment of LED lamp flicker performance with respect to the presented classification.
- The impact of three main types of power factor correction (PFC) circuits (i.e. no PFC, passive PFC and active PFC) on the characteristics and performance of SMPS' are evaluated through laboratory tests of six different desktop PC-SMPS' operating under different supply conditions and powers [12].
- The impact of lost periodicity on the efficiency and current waveform distortion is evaluated on two of the tested SMPS'. Special attention is given to the appropriate measurement and calculation procedures for evaluating changes in waveform distortion, efficiency and power factors of SMPS' when lost periodicity happens. Instead of using the standardised 200 ms time window, the time window length should be adjusted according to the effective periodicities of voltage and current waveform under specific operating conditions, which is in order to achieve the correct performance evaluation when lost periodicity happens. In addition, the operating cycle based performance indicators are also proposed to assess the performance of SMPS' operating over entire power range [9][13].

- Both CBMs and FDMs are developed for the three main SMPS types, which are capable of accurately representing the ac current waveform distortions different supply conditions and operating powers.
- The characteristics and performance of 19 different EVBCs are evaluated when the EVs are under Level 2 charging with different supply conditions. A classification of tested EVBCs is performed based on their voltage dependency of active power and fundamental reactive power, with the relevant exponential model coefficients also provided [14].
- A full circuit component-based EVBC model is developed to represent the change of ac current for EV under Level 2 charging with different supply conditions. The developed model also takes into account the fact that the EV charging transfers from constant current (CC) mode to constant voltage (CV) mode when the EV battery is charged up to 80%-90% of the battery's full state of charge (SoC). Due to the high computational requirements and the long simulation time of the full circuit model, its back-end circuit part is replaced by a variable resistance and the corresponding equivalent circuit model is obtained. Both full circuit model and equivalent circuit model are fully validated with measurements [15]. In addition, the performance differences between CBMs and FDMs are detailedly discussed on the case of EVBC modelling [16].
- The characteristics and performance of residential PVIs are investigated based on the laboratory testing of three different PVIs [17]. In particular, the change of harmonic current emission and efficiency under a combination of different supply conditions and operating powers is analysed.
- Detailed CBMs are developed for both single-phase and three-phase PVIs, with the model accuracy validated with measurements.
- FDMs are developed for three tested PVIs, and are capable of accurately representing the harmonic emission of PVIs under comprehensive working conditions [18]. In addition, a novel modelling approach is proposed to significantly reduce the number of tests required for modelling the harmonic characteristics of power-dependent PE devices, followed by the discussion of aggregate FDMs [19].

- The impact of supply conditions and operating powers on the harmonic and efficiency characteristics of SMPS', EVBCs and PVIs is fully investigate based on both simulation results and measurement data [8][10][20]. In addition, new waveform distortion indices are proposed to describe the power-dependent harmonic characteristics of modern PE devices, and are illustrated on SMPS', EVBCs and PVIs [8].
- Hybrid harmonic modelling approaches are proposed to allow the use of different harmonic model forms under time-domain or frequency-domain simulation environment, and are illustrated on the evaluation of the harmonic interaction of EVs and CFLs [21].
- The harmonic impacts of different deployment scales of EVs and/or PVs on the urban generic distribution network, are investigated by applying the hybrid modelling approach (using FDMs in a time-domain simulator).

In further collaborations with colleagues and other professors, the results are not included in the thesis, but are given in [22][23][24].

## 1.4 Thesis structure

This thesis consists of eight chapters, with the additional materials provided in the appendices. A brief summary of each chapter is given below:

**Chapter 1**

The introduction chapter first briefly reviews the history of harmonics in power systems and relates the change of harmonic issues with the proliferation of new electrical or electronic devices, emphasizing the necessity of evaluating the harmonic characteristics of modern PE devices. After that, the research objectives and scopes are clearly defined, as well as the main contributions of the thesis.

**Chapter 2**

Chapter 2 investigates the conventional harmonic analysis methods. It starts with an introduction of the typical harmonic analysis algorithms, followed by a discussion of the commonly used definitions, symbols and indices under nonsinusoidal condition. After that, the commonly used harmonic standards for both power system and

equipment are introduced. This chapter also discusses the internal and external causes of harmonic current emissions of PE devices, as well as the potential adverse effects of harmonics on LV networks. For the last two sections of the chapter, the typical harmonic modelling techniques and network harmonic analysis methods are investigated.

**Chapter 3**

Chapter 3 focuses on the harmonic modelling and characterisation of LED lamps. It first reviews the circuit topologies of residential LED lamps and points out that the harmonic current emission of LED lamps is directly affected by the circuit topology applied. After that, the comprehensive laboratory testing of 28 different residential LED lamps is introduced, with the basic information and results discussed. On the basis of the commonalities of their general operating principles and typical circuit topologies, tested LED lamps are classified into four different types, with the impact of different supply conditions on the change of electrical characteristics and presented classification also investigated. The final part of this chapter presents the generalised modelling approach for each type of LED lamps, with the component-based modelling approach applied for the Type A-C LED lamps and the frequency-domain modelling approach applied for Type D LED lamps. *Publications from this chapter:[11]*.

**Chapter 4**

Chapter 4 investigates the harmonic modelling and characterisation of the three main types of PC-SMPS' regarding the applied power factor control (PFC) circuits-without PFC (no-PFC), with passive PFC (p-PFC) and with active PFC (a-PFC). It first discusses the comprehensive laboratory testing results of six different desktop PC-SMPS', with the impact of different supply conditions and operating powers also taken into account. Special attention is given to the lost periodicity phenomenon observed from two of the tested SMPS' when they are operating at low or very low powers, and the corresponding impact on the device efficiency and current waveform. When lost periodicity occurs, the accuracy of indices, being calculated by using the recommended 200 ms window length from existing standards, is also analysed. After that, operating cycle based performance evaluation methodology is proposed and

demonstrated on the SMPS' with lost periodicity phenomenon. The final part of this chapter is on the harmonic modelling of SMPS', with the developed CBMs and FDMs discussed and validated with measurements. *Publications from this chapter: [8][9][10][12][13][20]*.

**Chapter 5**

Chapter 5 is on the harmonic modelling and characterisation of on-board EVBCs. It starts with the laboratory testing results of 19 different on-board EVBCs, with the basic information and results disclosed. After that, the impact of supply conditions on the characteristics and performance of EVBCs are fully investigated. The main focus of this chapter is the component-based modelling of an on-board unidirectional single-phase EVBCs under Level 2 charging which is currently the predominant EV charging approach in EU. Based on the relationship between instantaneous dc-link voltage and dc-link current, the developed full circuit model is simplified as an equivalent circuit model, with the accuracy of the two models fully validated with measurements. In addition, the developed FDM for the same EVBC is also discussed and compared with CBM in a simple but realistic LV network simulation, in terms of the difficulty, development effort and accuracy. *Publications from this chapter: [8][10][14][15][16][20]*.

**Chapter 6**

Chapter 6 investigates the harmonic modelling and characterisation of residential-scale PVIs. It starts with an introduction of the general circuit topologies and controls of PVIs, focusing on discussing the features and functionalities of main circuit parts. After that, the laboratory testing results of three different residential-scale PVIs operating under a combination of different supply conditions and operating powers, are analysed in terms of their current harmonic emission characteristics. The main part of this chapter is on the harmonic modelling of PVIs, where both CBMs and FDMs are developed and validated with measurements. Moreover, two harmonic admittance matrix (HAM) modification based FDMs are proposed and compared with the measurement-based FDMs, followed by the discussion of their frequency-domain aggregation approaches. *Publications from this chapter: [8][10][17][18][19][20]*.

**Chapter 7**

This chapter is about the evaluation of hybrid modelling techniques for the purpose of implementing different forms of harmonic models under the same harmonic network modelling environment. It starts with a brief introduction of various harmonic modelling techniques based on a case study of EVBC modelling. After that, two hybrid harmonic modelling approaches are proposed and compared on a simple network study with both CBMs and FDMs connected. To further demonstrate the effectiveness of the hybrid modelling approach, hybrid modelling using time-domain simulation is applied to investigate the harmonic interactions between various numbers of EVs and CFLs, based on a simple test network. The final part of this chapter investigates the harmonic impact of different deployment scales of EVs and/or PVs on the urban generic distribution network, by applying the hybrid modelling approach (using FDMs in a time-domain simulator). *Publications from this chapter: [21]*.

**Chapter 8**

The last chapter reviews the main findings of the research as well as the contributions to the harmonic modelling area. The limitations of the research and recommendations for the further improvement and extension of work are also discussed.

**Appendices**

Additional results and information which are not given in the main body of the thesis are provided in the appendices.

# Chapter 2

# Harmonic analysis methods

## 2.1 Introduction

This chapter starts with a detailed discussion of the conventional waveform distortion indices and other electric power quantities under nonsinusoidal conditions, followed by an introduction of two proposed waveform distortion indices for evaluating the contributions of LF harmonics and all other distortions to the total waveform distortion. After that, the most widely used harmonic standards for both power system and PE devices are introduced. This chapter also discusses the internal and external causes of harmonic current emissions of PE devices, as well as the potential adverse effects of harmonics on LV networks (especially the impact on distribution transformers). For the last two sections of the chapter, the harmonic modelling techniques and network harmonic analysis methods are investigated, giving the basis for the development of CBMs and FDMs for modern PE devices in the followed chapters.

## 2.2 Definitions, symbols and indices under nonsinusoidal condition

This section reviews the most widely used harmonic analysis tools and indices applied for nonlinear loads, which lays the basis for investigating the characteristics and performance of modern PE devices operating under nonsinusoidal supply voltage.

### 2.2.1 Harmonic analysis algorithms

Till now, numerous harmonic analysis algorithms have been proposed for evaluating the spectral contents of voltage and current waveforms measured in the power system, including discrete Fourier transform (DFT) or its fast implementation algorithm, named fast Fourier Transform (FFT) [25][26], wavelet transform [27][28], Hilbert-Huang transform [29][30], probabilistic neutral network [31][32], etc. However, among all those tools, DFT/FFT is still the most widely used tool for the commercial PQ analysers and is also the reference spectral analysis tool in the IEC 61000-4-7 [33], due to its easy implementation and low computational burdens as opposed to the others

[25]. As DFT/FFT algorithms assume the analysed signal is periodic, it requires the time window length to be the integer numbers of the period of the analysed signal, which is hard to strictly obey in practical applications and may result in issues like picket fence effects and spectrum leakage. Therefore, a variety of modified DFT/FFT based algorithms have been proposed to improve the accuracy and applicability of DFT/FFT, including short-time Fourier Transform [34], windowed interpolation FFT [35], etc. In existing IEC 61000 series and IEEE harmonic related standards, conventional FFT is still used as the reference tool for harmonic analysis and is also applied as the default signal processing tool in this thesis.

### 2.2.2 Definitions, symbols and indices

In this subsection, the standardised definition, measurement and calculation approaches for waveform distortion indices and other general electric power quantities under nonsinusoidal conditions will be discussed first, followed by an introduction of proposed waveform distortion indices for evaluating the contributions of low frequency (LF) harmonic and all other distortions to the total waveform distortion.

#### Standardised waveform distortion indices and electric power quantities under nonsinusoidal conditions

The most important standard defines the waveform distortion indices is IEC 61000-4-7 [33], with the detailed testing and measurement procedures given in IEC 61000-4-30 [36]. With respect to the definitions of general electric power quantities under nonsinusoidal condition, IEEE Std. 1459 plays a key role [37]. The indices applied for describing voltage and current waveform distortion normally refer to total harmonic distortion (*THD*), total harmonic current (*THC*) and total demand distortion (*TDD*) with their definitions given in (2.1)-(2.3).

$$THD_Y = \frac{Y_H}{Y_1} = \frac{\sqrt{\sum_{h=2}^{h_{max}} Y_h^2}}{Y_1} \times 100\% \tag{2.1}$$

$$THC = I_H = \sqrt{\sum_{h=2}^{h_{max}} I_h^2} \tag{2.2}$$

$$TDD = \frac{I_H}{I_{rated}} = \frac{\sqrt{\sum_{h=2}^{h_{max}} I_h^2}}{I_{rated}} \times 100\% \tag{2.3}$$

where: the symbol $Y$ is replaced by the symbol $I$ for currents and the symbol $U$ for voltages; $h_{max}$ is 40 for IEC 61000 series and is 50 for IEEE Standards; $I_H$ and $I_h$ are

the rms value of the sum of all considered current harmonics and the rms value of individual current harmonic respectively; $I_{rated}$ is the rms value of the rated current.

Both IEC 61000 series and IEEE harmonic related standards use DFT/FFT as the default spectral analysis tool which is theoretically only applicable to stationary signals whose spectral contents do not vary with time. However, the actual measured voltage and current waveforms are normally featured by varying spectral contents (i.e. the change of spectral component frequencies and/or magnitudes) and the existence of interhamornic components, resulting in spectrum leakage issue and hence reduced accuracy of the spectrum analysis results. To alleviate the impact of spectrum leakage on the accuracy of harmonic analysis, a harmonic and interharmoic subgrouping scheme is proposed in IEC 61000-4-7 [33]. Specifically, the rectangular window width applied for the analysed signal has to be 10 (for 50 Hz system) or 12 (for 60 Hz system) fundamental periods, leading to a 5 Hz frequency resolution (i.e. the frequency separation of the spectral components) [33]. If all the spectral components of the analysed signal (assuming it is stationary) have their frequencies to be integer multiples of 5 Hz, all spectral components can be correctly represented by the FFT results without having the spectral leakage issue.

Considering the fact that the spectral contents of analysed signal are typically not pre-known, the compromised subgrouping approach is applied in IEC 61000-4-7 for the evaluation of harmonics and interhamonics, and is defined by (2.4) and (2.5) [33]. As shown in Figure 2.1, the two adjacent spectral components of *h* order harmonic are grouped together with this harmonic to form a subgroup harmonic while the spectral components between two harmonics (except the spectral components directly adjacent to the harmonics) are grouped together to form a subgroup interharmonic. By applying the subgroup harmonics to (2.1)-(2.3), the corresponding subgroup total harmonic distortion of voltage and current ($THDS_V$ and $THDS_I$), subgroup total interharmonic distortion of voltage and current ($TIHDS_V$ and $TIHDS_I$), subgroup total subharmonic distortion of voltage and current ($TSHDS_V$ and $TSHDS_I$), subgroup total harmonic current (*THCS*), subgroup total interharmonic current (*TIHCS*), subgroup total subharmonic current (*TSHCS*), and subgroup total demand distortion ($TDD_{sg}$) can be obtained, as given in (2.6)-(2.12).

$$Y_{sg,h} = \sum_{N-1}^{N+1} Y_{C,(N\times h)+k}^2 \quad (2.4)$$

$$Y_{isg,h} = \sum_{k=2}^{N-2} Y_{C,(N\times h)+k}^2 \quad (2.5)$$

$$THDS_Y = \frac{\sqrt{\sum_{h=2}^{hmax} Y_{sg,h}^2}}{Y_{sg,1}} \times 100\% \quad (2.6)$$

$$TIHDS_Y = \frac{\sqrt{\sum_{h=1}^{hmax} Y_{isg,h}^2}}{Y_{sg,1}} \times 100\% \quad (2.7)$$

$$TSHDS_Y = \frac{\sqrt{\sum_{h=0}^{1} Y_{isg,h}^2}}{Y_{sg,1}} \times 100\% \quad (2.8)$$

$$THCS_Y = \sqrt{\sum_{h=2}^{hmax} Y_{sg,h}^2} \quad (2.9)$$

$$TIHCS_Y = \sqrt{\sum_{h=1}^{hmax} Y_{isg,h}^2} \quad (2.10)$$

$$TSHCS_Y = \sqrt{\sum_{h=0}^{1} Y_{isg,h}^2} \quad (2.11)$$

$$TDD_{sg} = \frac{\sqrt{\sum_{h=2}^{hmax} I_{sg,h}^2}}{I_{rated}} \times 100\% \quad (2.12)$$

where: the symbol *Y* is replaced by the symbol *V* for voltage and is replaced by the symbol *I* for current; $Y_{sg,h}$ is the subgroup harmonic of order *h* while $Y_{isg,h}$ is the subgroup interharmonic between order *h* and (*h*+1); $Y_{C,(N\times h)+k}$ is the spectral components calculated by using FFT with *N* equals 10 for 50 Hz system and equals 12 for 60 Hz system.

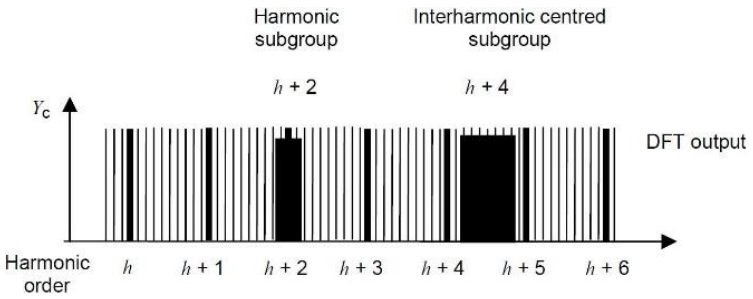



**Figure 2.1:** Illustration of the harmonic and interharmonic subgrouping approach in IEC 61000-4-7 [33].

Apart from the harmonic evaluation indices, conventional electric power quantities may also have different definitions under nonsinusoidal conditions, which are critical for the correct evaluation the electrical characteristics of modern PE devices. The key electric power indices given in [37] includes apparent, active and reactive power, and

power factors under nonsinusoidal conditions, and will be fully analysed in the following.

As shown in (2.13) and (2.14), the apparent power, *S*, is directly correlated to the voltage and current waveform distortion which is represented by $THD_V$ and $THD_I$ respectively. With increasing voltage and current waveform distortion, *S* will increase correspondingly. By dividing *S* into different parts as in (2.15), it is noticed that *S* consists of four different parts including the fundamental apparent power ($S_1$), the current distortion power ($D_I$), the voltage distortion power ($D_V$) and the harmonic apparent power ($S_H$), where the latter three are caused by voltage and/or current distortions. The mathematical expressions of $D_I$, $D_V$ and $S_H$ can also be rewritten as a multiple of $S_1$, $THD_I$ and $THD_V$ as in (2.16)-(2.18), indicating that they are not negligible parts when the voltage and current waveforms are highly distorted.

$$Y_H^2 = \sum_{h\neq 1} Y_h^2 = Y^2 - Y_1^2 \tag{2.13}$$

$$S^2 = V^2 I^2 = (V_1^2 + V_H^2)(I_1^2 + I_H^2) = S_1^2(1 + THD_V^2)(1 + THD_I^2) \tag{2.14}$$

$$S^2 = V^2 I^2 = (V_1^2 + V_H^2)(I_1^2 + I_H^2) =$$
$$= V_1^2 I_1^2 + V_1^2 I_H^2 + V_H^2 I_1^2 + V_H^2 I_H^2 = S_1^2 + D_I^2 + D_V^2 + S_H^2 \tag{2.15}$$

$$D_I^2 = V_1^2 I_H^2 = V_1^2 I_1^2 THD_I^2 = S_1^2 THD_I^2 \tag{2.16}$$

$$D_V^2 = V_H^2 I_1^2 = V_1^2 I_1^2 THD_V^2 = S_1^2 THD_V^2 \tag{2.17}$$

$$S_H^2 = V_H^2 I_H^2 = V_1^2 I_1^2 THD_V^2 THD_I^2 = S_1^2 THD_V^2 THD_I^2 \tag{2.18}$$

where: *Y* is replaced by *V* for voltage and is replaced by *I* for current; $Y_h$ is the rms value of individual harmonic while $Y_H$ and $Y_1$ are the rms value of all considered harmonics and the rms value of fundamental component respectively; *V* and *I* are the rms value of voltage and current respectively.

The definitions of active power (*P*) and reactive power (*Q*) are given in (2.19) and (2.20) respectively, with *P* divided into fundamental active power ($P_1$) and harmonic active power ($P_H$) and with *Q* divided into fundamental reactive power ($Q_1$) and harmonic reactive power ($Q_H$). To investigate the relationships among $S_H$, $P_H$ and $Q_H$, $S_H$ is further divided into $P_H$, $Q_H$ and distortion power, $D_{VI}$, as in (2.21). By replacing $S_H$ in (2.15) with (2.21), $S^2$ can be represented as the sum of $P^2$, $Q^2$ and the square of total distortion power, $D^2$, as shown in (2.22). In addition, the root sum square of $Q^2$ and $D^2$ is called nonactive power, *N*, in IEEE Std. 1459 [37]. From the above distortion,

it is noticed that the nonsinusoidal condition has direct impact on the calculation of electric power quantities, which will further affect the calculations of other relevant derived indices like power factors and efficiencies. For example, the calculation of power factor, *PF*, under nonsinusoidal condition equals to the product of displacement power factor, $PF_1$, and distortion power factor, $PF_d$, in (2.23), with $PF_1$ representing the conventional power factor under sinusoidal condition and with $PF_d$ representing the impact of voltage and current waveform distortion on *PF* (higher voltage and current waveform distortion results in lower $PF_d$ value). In conclusion, the correlations between voltage and current waveform distortion and the electric power quantities indicate that the existence of harmonics has direct impact on the electrical characteristics of PE devices and hence the power system operation.

$$P = V_1 I_1 cos\theta_1 + \sum_{h\neq 1}(V_h I_h cos\theta_h) = P_1 + P_H \tag{2.19}$$

$$Q = V_1 I_1 sin\theta_1 + \sum_{h\neq 1}(V_h I_h sin\theta_h) = Q_1 + Q_H \tag{2.20}$$

$$S_H^2 = V_H^2 I_H^2 = (\sum_{h1\neq 1} V_{h1}^2)(\sum_{h2\neq 1} I_{h2}^2) = \sum_{\substack{h1\neq 1 \\ h1=h2}} V_{h1}^2 I_{h2}^2 + \sum_{\substack{h1\neq 1 \\ h1\neq h2}} V_{h1}^2 I_{h2}^2 =$$

$$= (\sum_{\substack{h1\neq 1 \\ h1=h2}} V_{h1}^2 I_{h2}^2 cos^2\theta_h + \sum_{\substack{h1\neq 1 \\ h1=h2}} V_{h1}^2 I_{h2}^2 sin^2\theta_h) + (\sum_{\substack{h1\neq 1 \\ h1\neq h2}} V_{h1}^2 I_{h2}^2) =$$

$$= (P_H^2 + Q_H^2) + D_{VI}^2 \tag{2.21}$$

$$S^2 = S_1^2 + D_I^2 + D_V^2 + S_H^2 = (P_1^2 + Q_1^2) + D_I^2 + D_V^2 + P_H^2 + Q_H^2 + D_{VI}^2 =$$

$$= (P_1^2 + P_H^2) + (Q_1^2 + Q_H^2) + (D_I^2 + D_V^2 + D_{VI}^2) =$$

$$= P^2 + Q^2 + D^2 = P^2 + N^2 \tag{2.22}$$

$$PF = \frac{P}{S} = \frac{P_1 + P_H}{S_1\sqrt{(1+THD_V^2)(1+THD_I^2)}} = \frac{\frac{P_1}{S_1} + \frac{P_H}{S_1}}{\sqrt{(1+THD_V^2)(1+THD_I^2)}} =$$

$$= \frac{PF_1(1+\frac{P_H}{P_1})}{\sqrt{(1+THD_V^2)(1+THD_I^2)}} = PF_1 PF_d \tag{2.23}$$

where: *Y* is replaced by *V* for voltage and is replaced by *I* for current; $Y_h$ is the rms value of individual harmonic of order *h* while $Y_H$ and $Y_1$ are the rms value of all considered harmonics and the rms value of fundamental component respectively; *V* and *I* are the rms value of voltage and current respectively, and *h1* and *h2* are the harmonic orders.

**Waveform distortion indices for assessing the contributions of LF harmonics and all other distortions to the total waveform distortion**

Based on the definitions of $THD_I$, *THC* and *TDD* in (2.1)-(2.3), it is noticed that *THC* and *TDD* are linked by a constant factor ($100/I_{rated}$), and they represent the total harmonic contents either in absolute values or in percentage of $I_{rated}$, without indicating the correlation between the harmonic contents and fundamental component. Accordingly, when the PE device is not operating at its rated current, the corresponding *THC* and *TDD* values cannot well represent the extent of actual current waveform distortion. By contrast, $THD_I$ represents the harmonic contents in percentage of the fundamental component, without indicating the absolute values of harmonic contents. Accordingly, *THC*, *TDD* and $THD_I$ allow performing harmonic analysis from two different perspectives. *THC* and *TDD* allow the analysis of the impact of harmonic emissions of PE devices on the voltage and current harmonic levels in the network (i.e. network perspective) for evaluating the contribution of PE devices to the total harmonic distortion. $THD_I$ allows the analysis of the harmonic characteristics of an individual PE device (i.e. equipment perspective), indicating how the device's harmonic currents change in relation to the fundamental current, which is important for evaluating the performance of PE device.

However, *THC*, *TDD* and $THD_I$ only take into account the current harmonics of integer orders (up to $40^{th}$ and $50^{th}$ order for IEC standard and IEEE standard respectively, representing LF harmonics), without considering the other types or causes of waveform distortion like the subharmonics, interharmonics and high-frequency (HF) harmonics which might be present in the case of modern PE devices. Accordingly, to evaluate the contributions of those non-harmonic and HF harmonic distortion to the total operating current of PE devices, the fundamental factor, *FF*, and total distortion content, *TDC*, are proposed in [38] with the definitions given in (2.24) and (2.25) respectively. It is noticed that *FF* evaluates the fundamental current component, $I_1$, in percentage of the total operating current, $I_{tot}$, while *TDC* assesses the total distortion content, $I_{non\_fund}$, as a percentage of $I_{tot}$. In order to separate the LF harmonics and non-LF-harmonics from $I_{non\_fund}$, two new indices are proposed. One is the total LF harmonic factor, $THF_{LF}$, representing the LF harmonics as a ratio of $I_{tot}$ in (2.26). The other one is the total non-(LF)-harmonic distortion factor, *TNHDF*, describing the non-

(LF)-harmonic distortion as a ratio of $I_{tot}$ in (2.27). These two indices not only accompany the previously introduced *TDC* and *FF* indices, but extend their application as well. In particular, $THF_{LF}$ and *TNHDF* make a further distinguish between the LF harmonics and all other distortions, where is particularly important for the evaluation of harmonic characteristics of modern PE devices, for which LF harmonics might not be the most significant part of the total waveform distortion.

$$FF = \frac{I_1}{I_{tot}} \tag{2.24}$$

$$TDC = \frac{I_{non\_fund}}{I_{tot}} = \frac{\sqrt{I_{tot}^2 - I_1^2}}{I_{tot}} = \sqrt{1 - FF^2} \tag{2.25}$$

$$THF_{LF} = \frac{THC}{I_{tot}} = \frac{THD_I \cdot FF}{100} \tag{2.26}$$

$$TNHDF = \frac{I_{non\_harm}}{I_{tot}} = \frac{\sqrt{I_{tot}^2 - I_1^2 - THC^2}}{I_{tot}} = \sqrt{1 - FF^2 \cdot (1 + (THD_I/100)^2)} \tag{2.27}$$

where: $I_{non\_harm}$ is the rms values of non-LF-harmonic (non-fundamental) distortion current.

## 2.3 Harmonic standards

Depending on the regulating objectives, the harmonic standards can be divided into two types-the harmonic standards for the equipment and the harmonic standards for the power system. For the former one, the harmonic standards limit the maximum individual current harmonic emission for devices operating under ideal supply condition with its typical working mode, while for the latter one, the harmonic standards restrict the maximum individual voltage harmonics and *THD* value at supply terminals and the point of common coupling (PCC). The key harmonic related standards refer to IEEE Std 519 [39], EN 50160 [40], IEC TR 61000-3-6 [41], IEC 61000-3-2 [42], IEC 61000-3-12 [43], IEEE Std 1547 [44], and IEC TR 3-15 [45], with the first three defining the harmonic limits for power systems at different voltage levels and with the last four specifying the harmonic emission limits for different types of equipment.

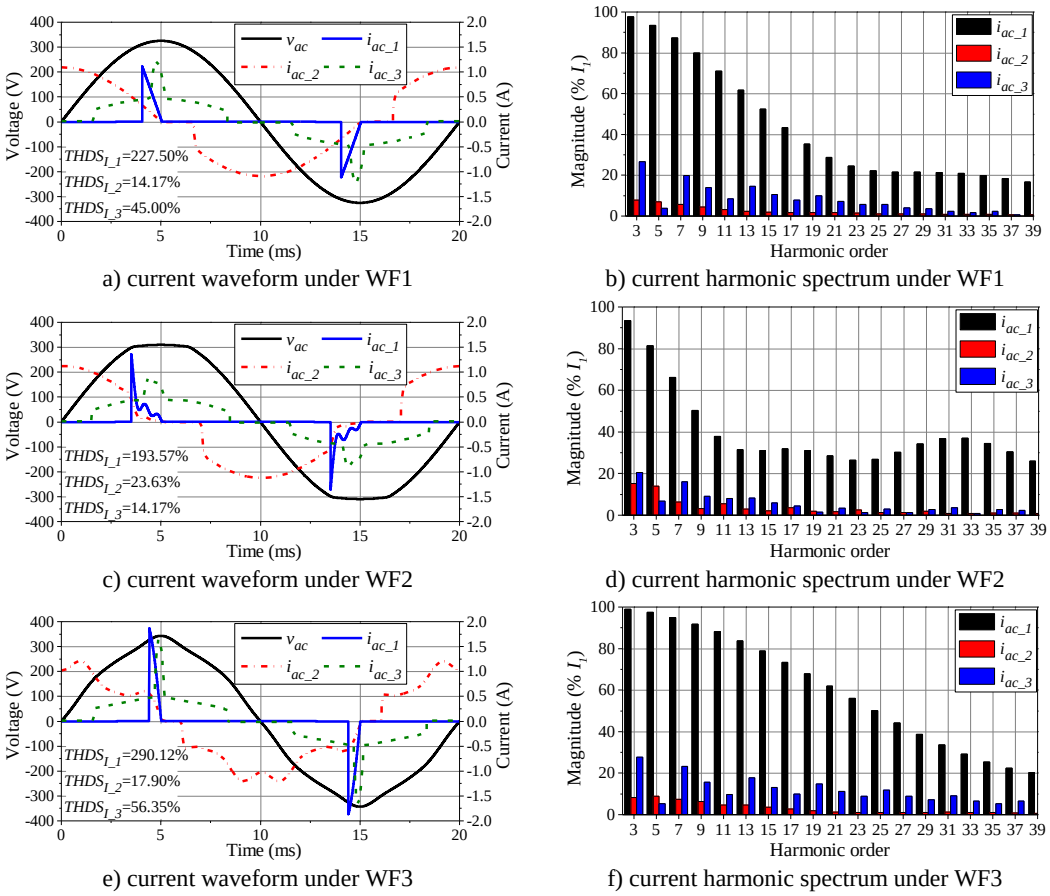
Specifically, IEEE Std 519 not only provides individual voltage harmonic limits and $THD_V$ limits for networks at different voltage ranges, but also specifies the individual current harmonics limits and the *TDD* limits at PCC point. Accordingly, IEEE Std 519

can also be applied for assessing the current harmonic emission compliance of different equipment. Standard EN 50160 specifies the limits for individual voltage harmonics at supply terminals for LV, MV and HV networks separately, while IEC TR 61000-3-6 outlines the indicative values of the planning levels for individual voltage harmonics in MV, HV and EHV power systems. It is worth noting that the planning levels for individual voltage harmonics are applied for system design, and should have some margins with respect to the compatibility levels (i.e. the planning level values are equal to or less than the corresponding compatibility values) [41]. Regarding the current harmonic regulation for individual equipment, IEC 61000-3-2 defines the limits for LV equipment with rated current below 16 A while IEC 61000-3-12 defines the limits for LV equipment with rated current higher than 16 A and below 75 A. Finally, IEC TR 61000-3-15 provides the individual current harmonics limits for DG in LV network with rated current up to 75 A while the individual current harmonic limits given in IEEE Std 1547 have the same values with limits ($I_{SC}/I_L$<20) in IEEE Std 519 for general electric equipment. The above standards or technical reports will be used for evaluating the harmonic emission compliance of the different types of PE devices in the thesis.

## 2.4 Causes of harmonic current emission of PE devices

The causes of current harmonic emission for PE devices can be generally divided into two types-internal causes and external causes. The internal causes refer to the circuit topologies and control strategies applied to PE devices, which determines the way of current drawn from the grid, while the external causes refer to the non-ideal supply conditions. The combined effect of internal causes and external causes determines the harmonic characteristics of PE devices. When the PE device is under sinusoidal supply voltage, the nonlinear behaviours of its font-end converter may result in distorted current waveform drawn from the grid, which also can be interpreted as the injection of low-order current harmonics to the grid. When the current harmonics propagate in the gird and flow through the gird impedance, harmonic voltage drops across the impedance will occur and distort the supply voltage waveform for the PE device. Depending on the internal circuit applied, PE devices may have distinctive ac current waveform shapes even they are within the same device category. For example, Figure 2.2(a) illustrates the time-domain current waveforms of three different passive front-

end converters, which are the full-wave rectifier circuit, capacitive dropper circuit and the valley-fill circuit, with the corresponding current harmonic spectrums given in Figure 2.2(b). The observed distinctive current waveform shapes and harmonic spectrums suggest that the internal circuit topologies of PE devices have a direct impact on the waveform distortion characteristics of their input ac current.




a) current waveform under WF1

b) current harmonic spectrum under WF1

c) current waveform under WF2

d) current harmonic spectrum under WF2

e) current waveform under WF3

f) current harmonic spectrum under WF3

**Figure 2.2:** The time-domain ac current waveforms and corresponding harmonic spectrums for the three circuits under different voltage waveforms (WF1-3).

When the PE devices are operating under distorted supply voltage waveform, their front-end converters and corresponding control circuits may have different sensitivities and responses (e.g. the change of firing angle and the detection of zero-crossing point) to the supply voltage distortions, resulting in the change of current waveform shapes. For example, it is observed in Figure 2.2(c)-2.2(f) that the ac current of the three front-end circuits exhibit different waveform distortions and harmonic spectrums when two distinctive distorted supply voltage waveforms are applied. In conclusion, the investigation of the current harmonic emission characteristics of

modern PE devices has to take into account both the internal causes and the external causes, which is the prerequisite of developing accurate harmonic models for them.

## 2.5 Impact of harmonics on LV networks

High-levels of harmonics propagating in LV networks not only increase the total power loses, but also affect the normal operation of network equipment and grid-connected customer devices, with the typical negative effects summarised below:

a) Generators: The presence of generators under voltage and current harmonics will result in the increased machine heating and temperature due to the increase of iron and copper losses which are frequency-dependent and increase with the increasing harmonics [46]. Therefore, to ensure the lifetime of the generators supplying nonlinear loads, generators require to be de-rated.

b) Power cables: The power cable losses, $I^2R$, are dissipated as a form of heat, and are determined by both the line current and the effective resistance. On the one hand, current harmonics flowing through the cable will increase the total rms current. On the other hand, harmonics amplify the existing skin effect and proximity effect, which will increase the effective resistance of power cables and hence the power losses.

c) Motors: As part of the iron losses for ac motors, the hysteresis and eddy current losses are frequency-dependent and will generally increase with the increasing frequency. Therefore, voltage harmonics will bring about extra iron losses for the motors with increasing working temperature. In addition, when negative sequence harmonics (i.e. harmonic order is $3k$-1, $k$ is positive integer) exist, the rotating direction of the created magnetic field is opposite to the one produced by fundamental frequency, resulting in the torsional oscillations of the motor shaft [46].

d) Overcurrent protective devices: Conventional protective installations applied in LV network are normally designed to protect against overcurrent, without considering the impact of harmonics [47]. The existence of current harmonics results in the overestimation of current value, which mag trip the device operating at normal current. In addition, the overcurrent protection circuit is typically implemented by using circuit

breakers or fuses with thermal releases which might be tripped due to the extra heating from excessive current harmonics [47].

e) PE devices: As discussed in Section 2.4, the current harmonic emission of PE devices is generally affected by the distortion characteristics of the supply voltage, which will not only bring about additional harmonic power losses, but also decrease the true power factor (according to (2.6)-(2.16)). Accordingly, reduced PQ performance can be expected for PE devices operating under distorted supply voltage.

f) Transformers: As distribution transformer is the key component of LV networks, the presence of voltage and current harmonics may result in a series of negative effects on the transformer operation and hence its lifetime. For example, current harmonics circulating in transformer windings will increase the stray losses and bring about extra heating, as well as aggravating the laminated core vibrations, resulting in the lifetime reduction. Moreover, European distribution network is typically the three-phase four-wire system, with the delta-wye configuration for the distribution transformer. For a balanced system with purely sinusoidal voltage and current waveforms, the line currents for the three phase will cancel out at the neutral line (i.e. the vector sum equals zero). When there is zero sequence current harmonics (i.e. triplen current harmonics) in the secondary winding, those harmonics will add cumulatively instead of cancelling out, causing the increased temperature of the neutral conductor of the transformer secondary winding. The zero sequence current harmonics will also circulate in the delta primary winding with extra heating.

In order to further investigate the impact of harmonics on transformers, the calculation procedure of transformer harmonic power loses, operation temperature increase and the reduced lifetime defined in [48][49] will be fully discussed. Specifically, the transformers total power losses, $P_T$, consist of non-load losses, $P_{NL}$, and load losses, $P_{LL}$, as indicated in (2.28). $P_{NL}$ is the losses due to voltage excitation or magnetization of the core when there is no loads connected, and is related to the voltage harmonics only (as $P_{NL}$ is independent of supplying load) [50]. Considering the fact that the supply voltage distortion is typically below 5% and $P_{NL}$ is insensitive to supply voltage distortion (e.g. a voltage distortion with $THD_V$ equals 10% only increases $P_{NL}$ from

687.7 W to 691.2 W in [51]). Therefore, $P_{NL}$ can be assumed constant at its rated value irrespective of the voltage harmonics.

$$P_T = P_{NL} + P_{LL} \tag{2.28}$$

In terms of $P_{LL}$, it is further divided into three different parts which are Ohmic loss, $P_{DC}$, eddy current loss, $P_{EC}$, and other stray loss, $P_{OSL}$, as shown in (2.29), and all the three parts are directly related to the current harmonics. The sum of $P_{EC}$ and $P_{OSL}$ is called total stray loss, $P_{TSL}$. The mathematical expressions of $P_{DC}$, $P_{EC}$ and $P_{OSL}$ under non-sinusoidal condition are represented by (2.30), (2.31) and (2.32) respectively, according to [48]. In addition, To quantify the impact of current harmonics on $P_{EC}$ and $P_{OSL}$, the harmonic loss factor for winding eddy currents, $F_{HL}$, and the harmonic loss factor for the other stray losses, $F_{HL\text{-}STR}$, are multiplied to the eddy current loss under rated conditions, $P_{EC\text{-}R}$, and the other stray loss under rated conditions, $P_{OSL\text{-}R}$, respectively, with their definitions given in (2.31) and (2.32). It is noticed that $F_{HL}$ and $F_{HL\text{-}STR}$ only equal one when the current is purely sinusoidal, and will be greater than one when the current is distorted. The higher current harmonic contents of specified harmonic orders, the larger $F_{HL}$ and $F_{HL\text{-}STR}$ will be (and hence the larger $P_{EC}$ and $P_{OSL}$). The calculation of $P_{LL}$, $P_{DC}$, $P_{EC}$ and $P_{OSL}$ under rated conditions (i.e. $P_{LL\text{-}R}$, $P_{DC\text{-}R}$, $P_{EC\text{-}R}$ and $P_{OSL\text{-}R}$) is given in (2.33)-(2.36). To maintain the normal life of the transformer, the maximum permissible current under specific current harmonic spectrum, $I_{max}$, can be calculated in per-unit of the rated current as given in (2.37).

$$P_{LL} = P_{DC} + P_{TSL} = P_{DC} + P_{EC} + P_{OSL} \tag{2.29}$$

$$P_{DC} = k_1 \times (I_{1-rms}^2 R_1 + I_{2-rms}^2 R_2) \tag{2.30}$$

$$P_{EC} = P_{EC-R} \times \frac{\sum_{h=1}^{hmax}(I_h^2 h^2)}{I^2} = P_{EC-R} \times \frac{\sum_{h=1}^{hmax}(I_h^2 h^2)}{\sum_{h=1}^{hmax} I_h^2} = P_{EC-R} \times F_{HL} \tag{2.31}$$

$$P_{OSL} = P_{OSL-R} \times \frac{\sum_{h=1}^{hmax}(I_h^2 h^{0.8})}{I^2} = P_{OSL-R} \times \frac{\sum_{h=1}^{hmax}(I_h^2 h^{0.8})}{\sum_{h=1}^{hmax} I_h^2} = P_{OSL-R} \times F_{HL-STR} \tag{2.32}$$

$$P_{LL-R} = P_{DC-R} + P_{TSL-R} = P_{DC-R} + P_{EC-R} + P_{OSL-R} \tag{2.33}$$

$$P_{DC-R} = k_1 \times (I_{1-R}^2 R_1 + I_{2-R}^2 R_2) \tag{2.34}$$

$$P_{EC-R} = k_2 \times P_{TSL-R} \tag{2.35}$$

$$P_{OSL-R} = (1 - k_2) \times P_{TSL-R} \tag{2.36}$$

$$I_{max}(pu) = \sqrt{\frac{P_{LL-R}(pu)}{1+F_{HL}P_{EC-R}(pu)+F_{HL-STR}P_{OSL-R}(pu)}} \tag{2.37}$$

where: $R_{DC}$ is the dc resistance of all windings; $I_{1\text{-}rms}$ and $I_{2\text{-}rms}$ are the transformer primary side current and secondary side current while $I_{1\text{-}R}$ and $I_{2\text{-}R}$ are their rated values; $I_h$ is the harmonic current of order $h$; $h_{max}$ is the maximum harmonic order considered; $k_1$ is a constant number, and is 1.0 and 1.5 for single-phase and three-phase transformer respectively; $k_2$ is the ratio of $P_{EC\text{-}R}$ to $P_{TSL\text{-}R}$, and is 0.33 and 0.67 for liquid-filled transformer and dry type transformer respectively; the per-unit base for $P_{LL\text{-}R}$, $P_{EC\text{-}R}$ and $P_{OSL\text{-}R}$ in (2.37) is $P_{DC\text{-}R}$;

With the transformer consistently operating under nonsinusoidal conditions, the excessive power losses due to harmonics will increase the winding temperature, and hence accelerate the deterioration of the winding insulation materials, resulting in reduced lifetime of the transformer [52][53]. To quantify the impact of harmonics on the increase of winding temperature and the resulted loss of life for the transformer, the hottest-spot temperature, $\theta_H$, and the aging acceleration factor, $F_{AA}$, are introduced in [48] and [49] respectively, with the definitions given in (2.38)-(2.41). Specifically, $\theta_H$ is equal to the sum of the top-oil-rise over ambient temperature, $\theta_{TO}$, the hottest-spot conductor rise over top-oil temperature, $\theta_g$, and the ambient temperature, $\theta_A$. The remaining life of the transformer is the winding insulation life divided by $F_{AA}$ [49]. The transformer is operating in the safe zone when $F_{AA}$ is below one [49][54]. In addition, K-factor is proposed in [55] and [56] to describe the capability of transformer withstanding current harmonics, with the definition given in (2.42). By comparing the definition of $F_{HL}$ in (2.31) with that of K-factor, it is noted that $F_{HL}$ describes the weighted current harmonic contents with respect to the actual rms value of the current on the secondary side ($I_{2\text{-}rms}$), while K-factor describes the weighted current harmonics with respected to the rated current on the secondary side ($I_{2\text{-}R}$). As indicated in (2.43), $F_{HL}$ and K-factor can be linked by a constant factor, $I_{2-R}^2/I_{2-rms}^2$, implying that $F_{HL}$ only equals K-factor when $I_{2\text{-}rms}$ equals $I_{2\text{-}R}$. When the transformer is not highly loaded with respect to its power rating, it can be expected that $F_{HL}$ will be apparently larger

than the K-factor as the transformer secondary-side current will be much smaller than its rated value.

$$\theta_{TO} = \theta_{TO-R} \times \left(\frac{P_{LL}+P_{NL}}{P_{LL-R}+P_{NL}}\right)^{0.8} \quad (2.38)$$

$$\theta_g = \theta_{g-R} \times \left(\frac{P_{LL}(pu)}{P_{LL-R}(pu)}\right)^{0.8} = \theta_{g-R} \times \left(\frac{1+F_{HL}\times P_{EC-R}(pu)}{1+P_{EC-R}(pu)}\right)^{0.8} \quad (2.39)$$

$$\theta_H = \theta_{TO} + \theta_g + \theta_A \quad (2.40)$$

$$F_{AA} = \exp\left(\frac{15000}{383} - \frac{15000}{\theta_H+273}\right) \quad (2.41)$$

$$K - factor = \frac{1}{I_R^2}\sum_{h=1}^{h_{max}}(I_h^2 \times h^2) \quad (2.42)$$

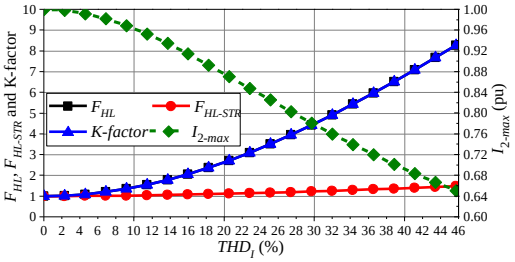
$$F_{HL} = \frac{I_{2-R}^2}{\sum_{h=1}^{h_{max}} I_{2-h}^2} \times K - factor = \frac{I_{2-R}^2}{I_{2-rms}^2} \times K - factor \quad (2.43)$$

where: $\theta_{TO\text{-}R}$ is the rated value of top-oil-rise over ambient temperature while $\theta_{g\text{-}R}$ is the rated value of hottest-spot conductor rise over top-oil temperature; $I_R$ is the rms fundamental current under rated frequency and rated load conditions; $I_{2\text{-}h}$ and $I_{2\text{-}R}$ are the *h*-order current harmonic and the rated current at the transformer secondary side respectively, with *h* and $h_{max}$ representing the harmonic order and the maximum considered harmonic order respectively; the per-unit base for (2.39) is $P_{DC\text{-}R}$.

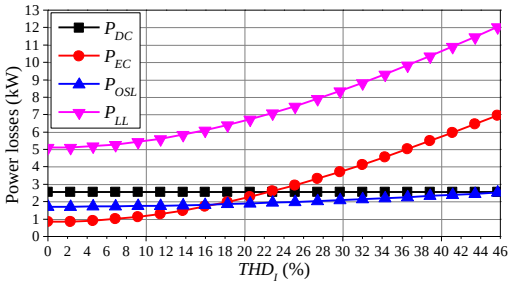
To demonstrate the actual impact of harmonics on the power losses, temperature increase and derating of the transformer, a 500 kVA distribution transformer (oil-filled, delta-wye connection) with $P_{NL\text{-}R}$ and $P_{LL\text{-}R}$ equal to 680 W and 5100 W respectively, is used as an example. The dc resistance of the primary winding is lumped to the secondary side, with the secondary dc resistance, $R_2$, equals to 3.264 mΩ. Based on the transformer power rating, and the nominal phase-to-phase voltages on the primary and secondary sides (11 kV and 400 V), rated line current on the primary and secondary sides, $I_{1\text{-}R}$ and $I_{2\text{-}R}$, can be obtained, equalling 26.24 A and 721.69 A respectively. According to (2.34)-(2.36), the calculated $P_{DC\text{-}R}$, $P_{EC\text{-}R}$ and $P_{OSL\text{-}R}$ are equal to 2550 W, 841.5 W and 1708.5 W respectively. Based on the above information, and the current harmonics on the transformer secondary side, the $F_{HL}$, $F_{HL\text{-}STR}$, $P_{DC}$, $P_{EC}$, $P_{OSL}$ and $P_{LL}$ can be calculated with (2.29)-(2.36). Here, it is assumed that $\theta_{TO\text{-}R}$, $\theta_{g\text{-}R}$ and $\theta_A$ are 65°C, 5°C and 35°C respectively, with a reference winding insulation

life of 30 years. In terms of the loading conditions of the transformer, it is assumed that the reference harmonic spectrum of the supply current on the secondary side follows the 1/*h* rule (i.e. $I_h/I_1=1/h$) which is conventionally used for estimating the harmonic pollution of nonlinear loads [57]. To further investigate the impact of the extent of transformer secondary current waveform distortion on the considered indices calculation, a series of harmonic spectrums ($3^{rd}$ to $19^{th}$ odd order harmonics considered) are created by adjusting the harmonic contents from 0 to $I_1/h$ with a step of $I_1/h\times\%5$, with the rms value of resultant current maintained at $I_{2\text{-}R}$.

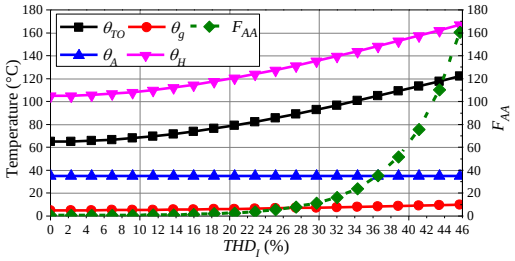
By applying (2.28)-(2.43), the impact of different levels of secondary-side current distortion on the specified transformer can be quantified in terms of the harmonic loss factors, transformer derating K-factor, maximum permissible secondary-side current ($I_{2\text{-}max}$), power losses, operating temperature increase and $F_{AA}$, as illustrated in Figure 2.3. It is observed from Figure 2.3(a) that $F_{HL}$ increases much more rapidly than $F_{HL\text{-}STR}$ with the increase of $THD_I$, implying that the winding eddy-current loss, $P_{EC}$, is more sensitive to the current distortion than the other stray loss, $P_{OSL}$, as shown in Figure 3.2(b). It is also noticed from Figure 3.2(a) that $I_{2\text{-}max}$ almost linearly decreases with the increase of $THD_I$ while the opposite trend is observed for the K-factor, suggesting the derating of the transformer is required when the current distortion is high. Regarding the impact of current on the transformer operating temperature, it is observed from Figure 2.3(c) that the hottest-spot temperature, $\theta_H$, is mainly determined by the top-oil-rise over ambient temperature, $\theta_{TO}$, which increases rapidly with the increasing $THD_I$, while the hottest-spot conductor rise over top-oil temperature, $\theta_g$, only accounts for a small portion of $\theta_H$ and its impact on the $\theta_H$ is negligible.




a) $F_{HL}$, $F_{HL\text{-}STR}$, K-factor and $I_{2\text{-}max}$




b) Power losses




c) Temperature and $F_{AA}$

**Figure 2.3:** The considered performance indicators for the distribution transformer with different current distortion levels on the secondary side.

## 2.6 Harmonic modelling techniques

Due to the increasing penetration of modern PE devices (like EVBCs and PVIs) into LV networks, it is essential to evaluate their large deployment impact on the voltage and current distortions of the network and the effectiveness of existing harmonic mitigation approaches applied, which requires suitable models to correctly represent the harmonic characteristics of PE devices under practical network conditions. The selection of harmonic load modelling approach has a direct impact on the harmonic analysis of power system, and is mainly determined by the information and measurement data available for the modelled device, the network study objective and its compatibility with the network simulators.

Typical harmonic modelling techniques can be classified into two types: time-domain modelling and frequency-domain modelling. Time domain models (TDMs) are usually derived from circuit-based, or component-based representations of the modelled equipment, allowing to correlate derived models with the physical characteristics and structure of the modelled equipment directly [16][21]. Frequency-domain models (FDMs) rely on measurements only, without the need of knowledge on the exact circuit topology and control algorithms of modelled device. As CBM and FDM are the two most widely used model forms for representing the harmonic characteristics of nonlinear loads, both CBMs and FDMs will be applied to the considered modern PE devices in this thesis, with their main features and implementation approaches discussed in the following subsections.

### 2.6.1 Component-based modelling

For the CBMs, they require accurate representation of the main electrical/electronic circuits of the modelled PE devices. A well-developed CBM can retain the main

electrical characteristics (e.g. harmonic emission characteristics, the voltage dependency of active and reactive power) of modelled PE devices operating under different working modes and supply conditions, and can be easily transformed to other model forms according to the requirement of specific network study. Considering the fact that PE device manufacturers rarely disclose their circuit design information and the device inspection requires the opening-up of the housing, the practical implementation of CBMs is complicated, especially for PE devices with sophisticated circuits (e.g. EVBCs and PVIs).

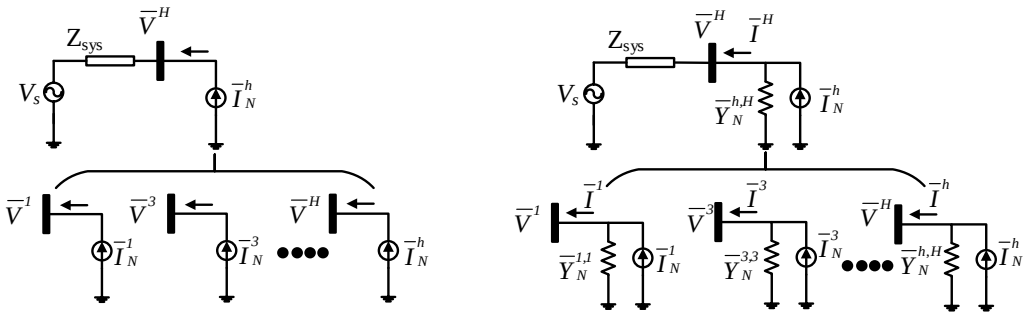
To solve that issue, the approach applied in the thesis is to estimate the general circuit topologies and main component parameter values from a few sets of measurements, with the implementation difficulty mainly determined by the circuit complexity of the modelled device. As the front-end converter or inverter circuits of PE devices are the main conversion stage between ac power form and dc power form, their circuit topologies have direct impact on the current harmonic characteristics of modelled devices, and can be divided into three different types depending on the applied power factor correction (PFC) circuits, which are PE devices without PFC (no-PFC), PE devices with passive PFC (p-PFC) and PE devices with active PFC (a-PFC). For PE devices with no-PFC or with p-PFC, their simple circuit topologies and component parameter values can be easily obtained from the measurement, due to their distinctive current waveform shapes. For example, the ac current of the uncontrolled full-wave rectifier with smoothing capacitor, is characterised by a pulse-like waveform shape. The generalised approach of developing CBM for PE devices with no-PFC or with p-PFC will be demonstrated on the case of LED lamp modelling in Chapter 3.

Regarding the modern PE devices equipped with a-PFC circuits, developing CBM for them becomes complicated especially when the information on the circuit topologies of modelled devices are not available. In addition, the circuit topology estimation approach applied for PE devices with no-PFC or with p-PFC is inappropriate for PE devices with a-PFC, which is not only because of the lack of features for their ac current waveform, but also due to the great diversity of the a-PFC based converter topologies and corresponding control strategies. The approach for developing CBM PE devices with a-PFC in this thesis is summarised as the following steps: a) figure

out the typical circuit topology within the category of modelled device; b) apply different a-PFC control strategies to the selected circuit topology and find out the one having closest ac current waveform distortion (or harmonic components) with the measurements; c) adjust the circuit parameter values to further improve the mode accuracy. This approach is used for developing CBMs for SMPS', EVBCs and PVIs in this thesis.

### 2.6.2 Frequency-domain modelling

Depending on whether the voltage dependency of current harmonics is taken into account and how it is considered in the model, conventional FDMs include constant (harmonic) current source models (CCSMs), decoupled and coupled harmonic Norton models (DHNMs and CHNMs respectively), and the harmonic fingerprint models (HFMs), with their physical circuit representation illustrated in Figure 2.4 [58]. Specifically, CCSMs are a series of parallel connected harmonic current sources, with the harmonic magnitudes and phase angles pre-defined. DHNMs and CHNMs are represented in the form of Norton equivalent circuit with a current source in parallel with a Norton harmonic admittance matrix ($HAM_N$) representing the impact of voltage fundamental component and harmonics on the current fundamental component and harmonics. Unlike CHNMs, HFMs directly link voltage and current fundamental components and harmonics with a (coupled) harmonic admittance matrix (HAM).



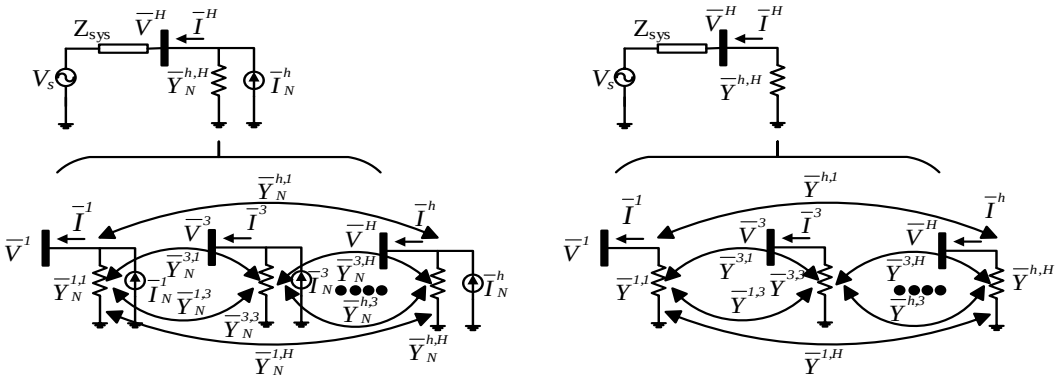



**Figure 2.4:** The physical circuit representation of the four FDMs.

**CCSMs**

For the CCSMs, fixed current harmonic spectrum is applied without considering the impact of supply voltage conditions, with the harmonic magnitudes and phase angles either obtained from the device manufacturer or measured from the field or laboratory tests. Considering the fact that the harmonic emission of PE devices is affected by a variety of factors including supply voltage distortions, voltage magnitude deviations, the source impedance connected, the operating power or mode of the device, etc., using fixed harmonic spectrum cannot well represent the actual harmonic emission of PE devices working under non-ideal supply conditions or different operating powers. Accordingly, CCSMs are normally applied when there the comprehensive laboratory tests for the modelled device are not accessible or infeasible (e.g. large PV plant), or when the harmonic emission of the modelled device is less sensitive to the change of supply conditions and operating powers. The information on the typical current harmonics of the modelled device are either provided by the manufacturer or obtained from the field tests. Due to the ease of use, CCSM is still the most widely used model form for representing the current harmonic emission of PE devices in existing literatures (e.g. [59][60][61]), and is the default model form for the network harmonic analysis simulator of commercial software (e.g. OpenDSS [6] and DlgSILENT [7]).

**DHNMs and CHNMs**

To take into account the impact of supply voltage conditions on current harmonics, DHNMs and CHNMs were proposed with the basic mathematical expression given in

(2.44), where the $\bar{\boldsymbol{I}}_{\boldsymbol{N}}^{\boldsymbol{h}}$ and $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h,H}}$ represent the Norton current source and the paralleled connected Norton harmonic admittance matrix ($HAM_N$) respectively. The only difference between DHNMs and CHNMs is that DHNMs neglect the coupling between voltage and current harmonics of different orders while it is taken into account by CHNMs. Accordingly, the off-diagonal elements of $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h,H}}$equal zero for DHNMs.

$$\begin{bmatrix} \bar{I}^1 \\ \bar{I}^2 \\ \bar{I}^3 \\ \vdots \\ \bar{I}^n \end{bmatrix} = \begin{bmatrix} \bar{I}_N^1 \\ \bar{I}_N^2 \\ \bar{I}_N^3 \\ \vdots \\ \bar{I}_N^n \end{bmatrix} + \begin{bmatrix} \bar{Y}_N^{1,1} & \bar{Y}_N^{1,2} & \bar{Y}_N^{1,3} & \dots & \bar{Y}_N^{1,n} \\ \bar{Y}_N^{2,1} & \bar{Y}_N^{2,2} & \bar{Y}_N^{2,3} & \dots & \bar{Y}_N^{2,n} \\ \bar{Y}_N^{3,1} & \bar{Y}_N^{3,2} & \bar{Y}_N^{3,3} & \dots & \bar{Y}_N^{3,n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_N^{n,1} & \bar{Y}_N^{n,2} & \bar{Y}_N^{n,3} & \dots & \bar{Y}_N^{n,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}^1 \\ \bar{V}^2 \\ \bar{V}^3 \\ \vdots \\ \bar{V}^n \end{bmatrix} \quad (2.44)$$

where: $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$ and $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ are the fundamental and harmonic components of ac current, and the fundamental and harmonic components of ac voltage, respectively, for *h*, *H*= 1, 2,⋯, *n*, where *n* is the maximum considered harmonic order (19in this paper); $\bar{\boldsymbol{I}}_{\boldsymbol{N}}^{\boldsymbol{h}}$ is the harmonic Norton current. $\bar{Y}_N^{k,j}$ represents the influence of *j* order voltage harmonic (*j*=1 refers to fundamental voltage component) on the *k* order current harmonic (*k*=1 refers to fundamental current component).

For DHNMs, the two unknown variable vectors ($\bar{\boldsymbol{I}}_{\boldsymbol{N}}^{\boldsymbol{h}}$ and the diagonal elements of $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h,H}}$, $\bar{\boldsymbol{Y}}_{\boldsymbol{N,dia}}^{\boldsymbol{h,H}}$, in (2.44) can be solved through two different measurements (measurements with different supply voltage distortions), which can be easily obtained from laboratory or field tests. DHNMs were initially applied for the modelling of distribution feeder (e.g. [62][63][64]), where the change of supply voltage waveform is normally achieved by the switching of a shunt capacitor, a shunt impedance or a parallel transformer as illustrated in Figure 2.5. As the model parameters can be directly calculated from the two sets of measurements with different supply voltage waveforms, the selection of the supply voltage waveform distortions has a direct impact on the model parameter values, and the use of different measurement sets may result in totally different model parameter values, making the accuracy and reliability of obtained model questionable [64]. Additionally, DHNMs are not suitable for modelling highly nonlinear system or equipment (e.g. uncontrolled full-wave rectifier based circuit), for which an apparent coupling exits between voltage and current harmonics of different orders.

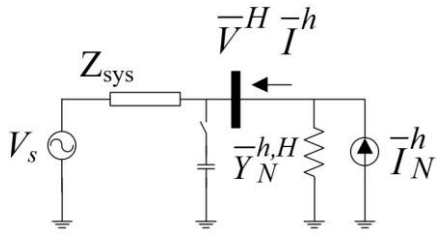


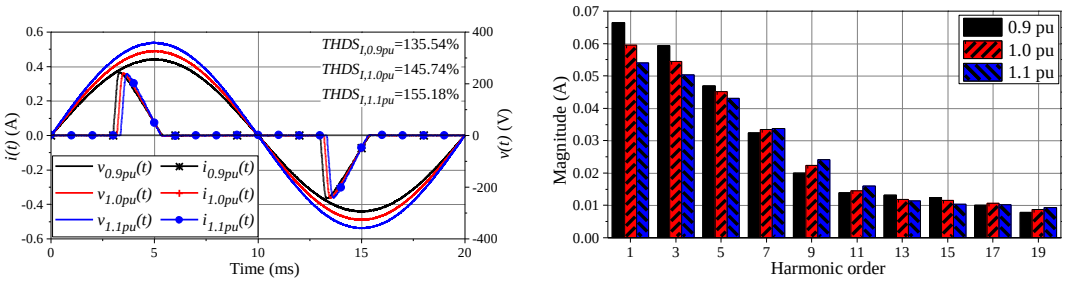

**Figure 2.5:** The practical implementation approach of DHNMs for a distribution feeder.

Unlike DHNMs, CHNMs also take into account the off-diagonal elements of $HAM_N$, representing the impact of voltage harmonics on the current harmonics of different orders. It is noticed that when the equipment input ac voltage is sinusoidal, (2.44) can be rewritten as (2.45). The current harmonics of device under ideal supply condition (i.e. $\bar{V}^1$ in (2.45) equals 230 V or 1 p.u.), $\boldsymbol{\bar{I}_{1pu}^h}$, can be represented by (2.46). Assuming $\boldsymbol{\bar{I}_{1pu}^h}$ of the equipment is pre-known, (2.46) minus (2.45) is equal to (2.47). It is noted from (2.47) that the first column of $HAM_N$, $\boldsymbol{\bar{Y}_N^{h,1}}$, represents the impact of off-nominal $\bar{V}^1$ on the $\boldsymbol{\bar{I}^h}$. For example, by observing the time-domain current waveforms and corresponding current harmonics of a LED lamp under sinusoidal supply voltage with different voltage magnitudes in Figure 2.6, it is noticed that the increase of $\bar{V}^1$ results in the decrease of fundamental current and certain current harmonics (e.g. 3th, 5th, 13th, and 15th harmonics) and the increase of 7th, 9th, 11th and 19th current harmonics. CHNMs have been widely applied for modelling PE devices (e.g. [16][21][65][66]).

$$\begin{bmatrix}\bar{I}^1\\ \bar{I}^2\\ \bar{I}^3\\ \vdots\\ \bar{I}^n\end{bmatrix} = \begin{bmatrix}\bar{I}_N^1\\ \bar{I}_N^2\\ \bar{I}_N^3\\ \vdots\\ \bar{I}_N^n\end{bmatrix} + \bar{V}^1 \begin{bmatrix}\bar{Y}_N^{1,1}\\ \bar{Y}_N^{2,1}\\ \bar{Y}_N^{3,1}\\ \vdots\\ \bar{Y}_N^{n,1}\end{bmatrix} \tag{2.45}$$

$$\begin{bmatrix}\bar{I}_{1pu}^1\\ \bar{I}_{1pu}^2\\ \bar{I}_{1pu}^3\\ \vdots\\ \bar{I}_{1pu}^n\end{bmatrix} = \begin{bmatrix}\bar{I}_N^1\\ \bar{I}_N^2\\ \bar{I}_N^3\\ \vdots\\ \bar{I}_N^n\end{bmatrix} + \bar{V}_{1pu}^1 \begin{bmatrix}\bar{Y}_N^{1,1}\\ \bar{Y}_N^{2,1}\\ \bar{Y}_N^{3,1}\\ \vdots\\ \bar{Y}_N^{n,1}\end{bmatrix} \tag{2.46}$$

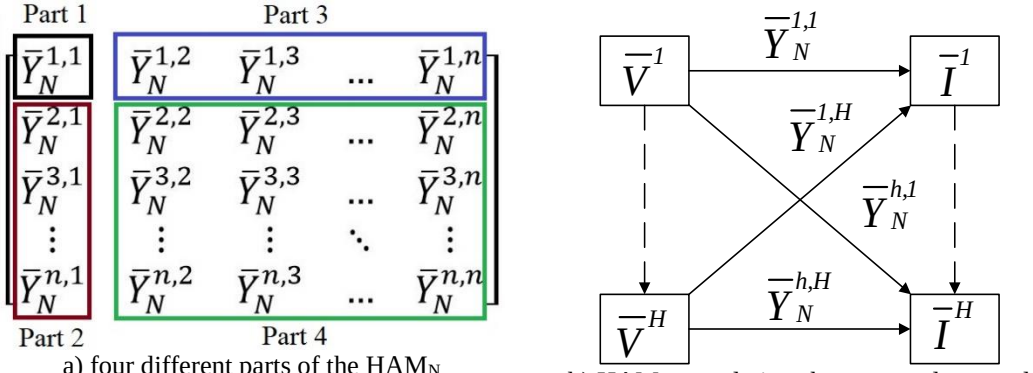
$$\begin{bmatrix}\bar{I}^1\\ \bar{I}^2\\ \bar{I}^3\\ \vdots\\ \bar{I}^h\end{bmatrix} = \begin{bmatrix}\bar{I}_{1pu}^1\\ \bar{I}_{1pu}^2\\ \bar{I}_{1pu}^3\\ \vdots\\ \bar{I}_{1pu}^n\end{bmatrix} + (\bar{V}^1 - \bar{V}_{1pu}^1) \begin{bmatrix}\bar{Y}_N^{1,1}\\ \bar{Y}_N^{2,1}\\ \bar{Y}_N^{3,1}\\ \vdots\\ \bar{Y}_N^{n,1}\end{bmatrix} \tag{2.47}$$




a) time-domain waveforms b) frequency-domain current harmonics

**Figure 2.6:** The time-domain waveform and corresponding current harmonics of a LED lamp under sinusoidal supply voltage with magnitudes of 0.9-1.1 p.u.

To further investigate the correlations between voltage and current fundamental components and harmonics, the $HAM_N$ is divided into four parts as illustrated in Figure 2.7. Specifically, Part 1, $\bar{Y}_N^{1,1}$, represents the impact of $\bar{V}^1$ on $\bar{I}^1$; Part 2, $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h},\boldsymbol{1}}$, represents the impact of $\bar{V}^1$ on the $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$; Part 3, $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{1},\boldsymbol{H}}$, represents the impact of $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ on $\bar{I}^1$; Part 4, $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h},\boldsymbol{H}}$, represents the impact of $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ on $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$. The calculation approach of each part will be discussed separately in the following.




a) four different parts of the $HAM_N$ b) $HAM_N$ correlations between voltage and current harmonics

**Figure 2.7:** Dependencies between voltage and current harmonics in $HAM_N$.

*a) Part 1 and Part 3: the impact of $\bar{V}^1$ and $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ on $\bar{I}^1$*

By extracting the first row of (2.44), Part 1 and Part 3 can be given by (2.48). From (2.48), it is noticed that Part 1 and Part 3 are represented by the former part, (2.49), and the later part, (2.50), respectively.

$$\bar{I}^1 = (\bar{I}_N^1 + \bar{Y}_N^{1,1}\bar{V}^1) + \begin{bmatrix}\bar{Y}_N^{1,2} & \bar{Y}_N^{1,3} & \dots & \bar{Y}_N^{1,n}\end{bmatrix} \times \begin{bmatrix}\bar{V}^2 \\ \bar{V}^3 \\ \vdots \\ \bar{V}^n\end{bmatrix} \tag{2.48}$$

$$\bar{I}_{P1}^1 = \bar{I}_N^1 + \bar{Y}_N^{1,1}\bar{V}^1 = f(\bar{V}^1) \tag{2.49}$$

$$\bar{I}_{P2}^{1} = \begin{bmatrix} \bar{Y}_N^{1,2} & \bar{Y}_N^{1,3} & \dots & \bar{Y}_N^{1,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}^2 \\ \bar{V}^3 \\ \vdots \\ \bar{V}^n \end{bmatrix} \tag{2.50}$$

To solve Part 1, ac current waveforms measured at sinusoidal supply voltage with different magnitudes are required, and the correlation between $\bar{I}^1$and $\bar{V}^1$ can be easily obtained through curve fitting (when supply voltage is sinusoidal, $\bar{I}_{P1}^{1}$ equals $\bar{I}^1$ with $\bar{I}_{P2}^{1}$ equals zero). As the correlation between $\bar{I}^1$and $\bar{V}^1$ for modern PE devices may not be linear relationship (e.g. a 2nd-degree polynomial relationship can be expected for a constant impedance load), the linear formulation used in (2.49) may not be able to accurately represent the dependency of $\bar{I}^1$on $\bar{V}^1$ for modelled device. Accordingly, $\bar{I}^1$ can be represented as a function of $\bar{V}^1$(i.e. $f(\bar{V}^1)$), where the selection of function form is determined by the observed relationship between $\bar{I}^1$ and $\bar{V}^1$ for the modelled device. In terms of Part 2 represented by (2.50), it can be solved from the individual voltage harmonic tests which are tests under sinusoidal supply voltage superimposed with individual voltage harmonic with varying harmonic magnitudes and phase angles. Assuming there are *k* different tests for *H* order voltage harmonic with different harmonic magnitudes and phase angles, Part 3 for any two of the *k* testes (test *k1* and *k2*) can be represented by (2.51) and (2.52) respectively, and the element $\bar{Y}_N^{1,H}$ can be calculated by using (2.52) minus (2.51). Hence, there will be (*k*-1) $\bar{Y}_N^{1,H}$ values for individual *H* order voltage harmonic. Here, the average value of the (*k*-1) $\bar{Y}_N^{1,H}$ values will be applied in the final model.

$$\bar{I}_{k1}^{1} = f(\bar{V}_{k1}^{1}) + \bar{Y}_N^{1,H} \times \bar{V}_{k1}^{H} \tag{2.51}$$

$$\bar{I}_{k2}^{1} = f(\bar{V}_{k2}^{1}) + \bar{Y}_N^{1,H} \times \bar{V}_{k2}^{H} \tag{2.52}$$

$$\bar{I}_{k2}^{1} - \bar{I}_{k1}^{1} = f(\bar{V}_{k2}^{1}) - f(\bar{V}_{k1}^{1}) + \bar{Y}_N^{1,H} \times (\bar{V}_{k2}^{H} - \bar{V}_{k1}^{H}) \tag{2.53}$$

*b) Part 2: the impact of $\bar{V}^1$on $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$*

When the modelled device is tested under sinusoidal supply voltage, (2.44) is simplified as (2.45). To separate Part 1 from (2.45), the current harmonics are expressed in percentage of the fundamental component and (2.54) can be obtained. $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,1}}$ in (2.54) represents the impact of fundamental voltage component, $\bar{V}^1$, on the current harmonic spectrum, $\bar{\boldsymbol{I}}_{\boldsymbol{\%}}^{\boldsymbol{h}}$.

$$\begin{bmatrix} \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{n} \end{bmatrix} = \begin{bmatrix} \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \bar{V}^{1} \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} \\ \bar{Y}_{N\_\%}^{3,1} \\ \vdots \\ \bar{Y}_{N\_\%}^{n,1} \end{bmatrix} \tag{2.54}$$

Again, assuming there are *k* testes for sinusoidal supply voltage with different voltage magnitudes, and *k1* and *k2* are the two of the n tests (corresponds to (2.55) and (2.56) respectively), $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,1}}$ can be easily obtained from (2.57) which equals (2.56) minus (2.55). As there will be (*k*-1) sets of $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,1}}$ values for n tests, their average values are applied in the final model.

$$\begin{bmatrix} \bar{I}_{\%\_k1}^{2} \\ \bar{I}_{\%\_k1}^{3} \\ \vdots \\ \bar{I}_{\%\_k1}^{n} \end{bmatrix} = \begin{bmatrix} \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \bar{V}_{k1}^{1} \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} \\ \bar{Y}_{N\_\%}^{3,1} \\ \vdots \\ \bar{Y}_{N\_\%}^{n,1} \end{bmatrix} \tag{2.55}$$

$$\begin{bmatrix} \bar{I}_{\%\_k2}^{2} \\ \bar{I}_{\%\_k2}^{3} \\ \vdots \\ \bar{I}_{\%\_k2}^{n} \end{bmatrix} = \begin{bmatrix} \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \bar{V}_{k2}^{1} \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} \\ \bar{Y}_{N\_\%}^{3,1} \\ \vdots \\ \bar{Y}_{N\_\%}^{n,1} \end{bmatrix} \tag{2.56}$$

$$\begin{bmatrix} \bar{I}_{\%\_k2}^{2} - \bar{I}_{\%\_k1}^{2} \\ \bar{I}_{\%\_k2}^{3} - \bar{I}_{\%\_k1}^{3} \\ \vdots \\ \bar{I}_{\%\_k2}^{n} - \bar{I}_{\%\_k1}^{n} \end{bmatrix} = (\bar{V}_{k2}^{1} - \bar{V}_{k1}^{1}) \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} \\ \bar{Y}_{N\_\%}^{3,1} \\ \vdots \\ \bar{Y}_{N\_\%}^{n,1} \end{bmatrix} \tag{2.57}$$

*c) Part 4: the impact of* $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ *on* $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$

To separate Part 4 from Part 1-3, (2.44) is expressed in the percentage of fundamental voltage and current components as shown in (2.58). As the first row of (2.58) is independent of the other rows, removing the first row from (2.58) will result in (2.59). Reorganising (2.59) will obtain (2.60) where content between the brackets represents the current harmonic spectrum under ideal supply condition, $\bar{\boldsymbol{I}}_{\boldsymbol{\%\_1pu}}^{\boldsymbol{h}}$, as in (2.61).

$$\begin{bmatrix} 1 \\ \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{n} \end{bmatrix} = \begin{bmatrix} 1 \\ \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \begin{bmatrix} \bar{Y}_{N\_\%}^{1,1} & \bar{Y}_{N\_\%}^{1,2} & \bar{Y}_{N\_\%}^{1,3} & \cdots & \bar{Y}_{N\_\%}^{1,n} \\ \bar{Y}_{N\_\%}^{2,1} & \bar{Y}_{N\_\%}^{2,2} & \bar{Y}_{N\_\%}^{2,3} & \cdots & \bar{Y}_{N\_\%}^{2,n} \\ \bar{Y}_{N\_\%}^{3,1} & \bar{Y}_{N\_\%}^{3,2} & \bar{Y}_{N\_\%}^{3,3} & \cdots & \bar{Y}_{N\_\%}^{3,n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_{N\_\%}^{n,1} & \bar{Y}_{N\_\%}^{n,2} & \bar{Y}_{N\_\%}^{n,3} & \cdots & \bar{Y}_{N\_\%}^{n,n} \end{bmatrix} \times \begin{bmatrix} 1 \\ \bar{V}_{\%}^{2} \\ \bar{V}_{\%}^{3} \\ \vdots \\ \bar{V}_{\%}^{n} \end{bmatrix} \tag{2.58}$$

$$\begin{bmatrix} \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{n} \end{bmatrix} = \begin{bmatrix} \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} & \bar{Y}_{N\_\%}^{2,2} & \bar{Y}_{N\_\%}^{2,3} & \cdots & \bar{Y}_{N\_\%}^{2,n} \\ \bar{Y}_{N\_\%}^{3,1} & \bar{Y}_{N\_\%}^{3,2} & \bar{Y}_{N\_\%}^{3,3} & \cdots & \bar{Y}_{N\_\%}^{3,n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_{N\_\%}^{n,1} & \bar{Y}_{N\_\%}^{n,2} & \bar{Y}_{N\_\%}^{n,3} & \cdots & \bar{Y}_{N\_\%}^{n,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}_{\%}^{2} \\ \bar{V}_{\%}^{3} \\ \vdots \\ \bar{V}_{\%}^{n} \end{bmatrix} \tag{2.59}$$

$$\begin{bmatrix} \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{n} \end{bmatrix} = \left( \begin{bmatrix} \bar{I}_{N\_\%}^{2} \\ \bar{I}_{N\_\%}^{3} \\ \vdots \\ \bar{I}_{N\_\%}^{n} \end{bmatrix} + \begin{bmatrix} \bar{Y}_{N\_\%}^{2,1} \\ \bar{Y}_{N\_\%}^{3,1} \\ \vdots \\ \bar{Y}_{N\_\%}^{n,1} \end{bmatrix} \right) + \begin{bmatrix} \bar{Y}_{N\_\%}^{2,2} & \bar{Y}_{N\_\%}^{2,3} & \cdots & \bar{Y}_{N\_\%}^{2,n} \\ \bar{Y}_{N\_\%}^{3,2} & \bar{Y}_{N\_\%}^{3,3} & \cdots & \bar{Y}_{N\_\%}^{3,n} \\ \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_{N\_\%}^{n,2} & \bar{Y}_{N\_\%}^{n,3} & \cdots & \bar{Y}_{N\_\%}^{n,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}_{\%}^{2} \\ \bar{V}_{\%}^{3} \\ \vdots \\ \bar{V}_{\%}^{n} \end{bmatrix} \tag{2.60}$$

$$\begin{bmatrix} \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{n} \end{bmatrix} = \begin{bmatrix} \bar{I}_{\%\_1pu}^{2} \\ \bar{I}_{\%\_1pu}^{3} \\ \vdots \\ \bar{I}_{\%\_1pu}^{n} \end{bmatrix} + \begin{bmatrix} \bar{Y}_{N\_\%}^{2,2} & \bar{Y}_{N\_\%}^{2,3} & \cdots & \bar{Y}_{N\_\%}^{2,n} \\ \bar{Y}_{N\_\%}^{3,2} & \bar{Y}_{N\_\%}^{3,3} & \cdots & \bar{Y}_{N\_\%}^{3,n} \\ \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_{N\_\%}^{n,2} & \bar{Y}_{N\_\%}^{n,3} & \cdots & \bar{Y}_{N\_\%}^{n,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}_{\%}^{2} \\ \bar{V}_{\%}^{3} \\ \vdots \\ \bar{V}_{\%}^{n} \end{bmatrix} \tag{2.61}$$

Assuming $\bar{\boldsymbol{I}}_{\%\_1pu}^{\boldsymbol{h}}$ is pre-known (either obtained from laboratory measurement or provided by manufacturer), solving (2.61) needs at least (*n*-1) different measurements with different supply voltage distortions (to avoid singular matrix). Each row of the Norton harmonic admittance matrix in percentage ($HAM_{N\_\%}$) can be solved by (2.62).

$$\begin{bmatrix} \bar{I}_{\%\_1}^{h} \\ \bar{I}_{\%\_2}^{h} \\ \vdots \\ \bar{I}_{\%\_(n-1)}^{h} \end{bmatrix} = \begin{bmatrix} \bar{I}_{\%\_1pu}^{h} \\ \bar{I}_{\%\_1pu}^{h} \\ \vdots \\ \bar{I}_{\%\_1pu}^{h} \end{bmatrix} + \begin{bmatrix} \bar{V}_{\%\_1}^{2} & \bar{V}_{\%\_1}^{3} & \bar{V}_{\%\_1}^{4} & \cdots & \bar{V}_{\%\_1}^{n} \\ \bar{V}_{\%\_2}^{2} & \bar{V}_{\%\_2}^{3} & \bar{V}_{\%\_2}^{4} & \cdots & \bar{V}_{\%\_2}^{n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{V}_{\%\_(n-1)}^{2} & \bar{V}_{\%\_(n-1)}^{3} & \bar{V}_{\%\_(n-1)}^{4} & \cdots & \bar{V}_{\%\_(n-1)}^{n} \end{bmatrix} \times \begin{bmatrix} \bar{Y}_{N\_\%}^{h,2} \\ \bar{Y}_{N\_\%}^{h,3} \\ \vdots \\ \bar{Y}_{N\_\%}^{h,n} \end{bmatrix} \tag{2.62}$$

When there are (*n*-1) individual voltage harmonic tests at order *H* with a combination of different magnitudes and phase angles, (2.62) can be rewritten as (2.63) to represent the relationship between *h* order current harmonic, $\bar{I}_{\%}^{h}$, and *H* order voltage harmonic $\bar{V}_{\%}^{H}$, and there will be (*n*-1) $\bar{Y}_{N\_\%}^{h,H}$ values, with their average value applied in the final model. In addition, $\bar{Y}_{N\_\%}^{h,H}$ and $\bar{Y}_{N}^{h,H}$ are linked by a constant factor, $\bar{V}^{1}/\bar{I}^{1}$, as indicated in (2.64).

$$\begin{bmatrix} \bar{I}_{\%\_1}^{h} \\ \bar{I}_{\%\_2}^{h} \\ \vdots \\ \bar{I}_{\%\_(n-1)}^{h} \end{bmatrix} = \begin{bmatrix} \bar{I}_{\%\_1pu}^{h} \\ \bar{I}_{\%\_1pu}^{h} \\ \vdots \\ \bar{I}_{\%\_1pu}^{h} \end{bmatrix} + \begin{bmatrix} \bar{V}_{\%\_1}^{H} \\ \bar{V}_{\%\_2}^{H} \\ \vdots \\ \bar{V}_{\%\_(n-1)}^{H} \end{bmatrix} \times \bar{Y}_{N\_\%}^{h,H} \tag{2.63}$$

$$\bar{Y}_{N\_\%}^{h,H} = \frac{\Delta \bar{I}_{\%}^{h}}{\Delta \bar{V}_{\%}^{H}} = \frac{\Delta \bar{I}^{h}/\bar{I}^{1}}{\Delta \bar{V}^{H}/\bar{V}^{1}} = \bar{Y}_{N}^{h,H} \times \frac{\bar{V}^{1}}{\bar{I}^{1}} \tag{2.64}$$

Based on the above discussion, the required measurements as inputs for developing CHNMs are : a) measurement of device operating under ideal supply condition (for obtaining $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\%\_\boldsymbol{1pu}}$) b) measurement of device operating under sinusoidal supply voltage with different voltage magnitudes (for obtaining Part 1: $\bar{Y}_N^{1,1}$ and Part 2: $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h,1}}$); c) measurement of device operating under sinusoidal supply voltage superimposed with individual voltage harmonics with varying voltage magnitudes and phase angles, and the rms magnitude of distorted supply voltage is maintained at 1 p.u. (for obtaining Part 3: $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{1,H}}$ and Part 4: $\bar{\boldsymbol{Y}}_{\boldsymbol{N}}^{\boldsymbol{h,H}}$);

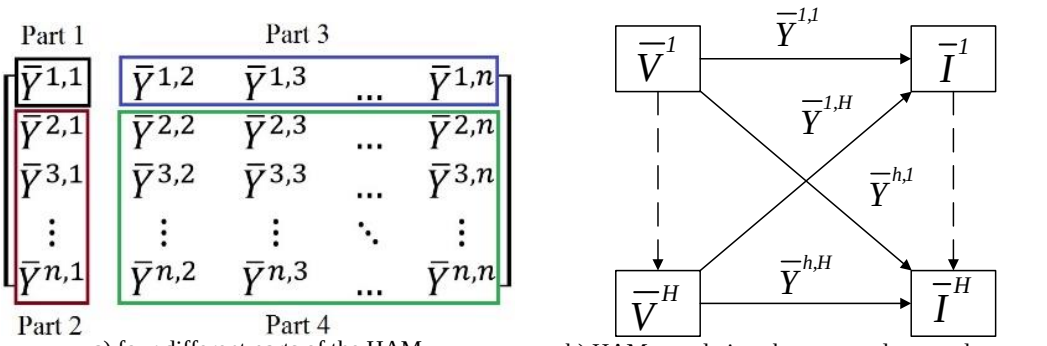
**HFMs**

As opposed to CHNMs and DHNMs, HFMs neglect the parallel connected current source as shown in Figure 2.4(d), with its basic mathematical formulation given in (2.65). The application of HFMs for nonlinear loads has been seen in existing literatures (e.g. [67][68][69]).

$$\begin{bmatrix} \bar{I}^1 \\ \bar{I}^2 \\ \bar{I}^3 \\ \vdots \\ \bar{I}^n \end{bmatrix} = \begin{bmatrix} \bar{Y}^{1,1} & \bar{Y}^{1,2} & \bar{Y}^{1,3} & \dots & \bar{Y}^{1,n} \\ \bar{Y}^{2,1} & \bar{Y}^{2,2} & \bar{Y}^{2,3} & \dots & \bar{Y}^{2,n} \\ \bar{Y}^{3,1} & \bar{Y}^{3,2} & \bar{Y}^{3,3} & \dots & \bar{Y}^{3,n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \bar{Y}^{n,1} & \bar{Y}^{n,2} & \bar{Y}^{n,3} & \dots & \bar{Y}^{n,n} \end{bmatrix} \times \begin{bmatrix} \bar{V}^1 \\ \bar{V}^2 \\ \bar{V}^3 \\ \vdots \\ \bar{V}^n \end{bmatrix} \tag{2.65}$$

where: $\bar{I}^h$, $\bar{V}^H$ denote fundamental and harmonic components of equipment input ac current, and fundamental and harmonic components of ac supply voltage, respectively, for $h$, $H$ = 1, 2, …, $n$, where $n$ is the maximum considered harmonic order (19 in the thesis). All mutual dependencies are represented by HAM elements, $\bar{Y}^{h,H}$.

Similar with CHNMs, HAM in (2.65) can also be divided into four parts as shown in Figure 2.8. Specifically, Part 1 is one admittance, $\bar{Y}^{1,1}$, representing the impact of $\bar{V}^1$ on one part of total fundamental current, $\bar{I}_A^1$; Part 2 is a column-matrix, $\bar{\boldsymbol{Y}}^{\boldsymbol{h,1}}$, representing the impact of on one part of the total harmonic currents with all considered orders, $\bar{\boldsymbol{I}}_{\boldsymbol{A}}^{\boldsymbol{h}}$; Part 3 is a row-matrix, $\bar{\boldsymbol{Y}}^{\boldsymbol{1,H}}$, representing the impact of $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ on the other part of total fundamental current, $\bar{I}_B^1$; Part 4 is a matrix, $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}$, representing the impact of $\bar{\boldsymbol{V}}^{\boldsymbol{H}}$ on the other part of the total harmonic currents with all considered orders, $\bar{\boldsymbol{I}}_{\boldsymbol{B}}^{\boldsymbol{h}}$. It is noticed that the total fundamental and harmonic currents ($\bar{I}_{Tot}^1$ and $\bar{\boldsymbol{I}}_{\boldsymbol{Tot}}^{\boldsymbol{h}}$) are divided into two parts-$\bar{I}_A^1$ and $\bar{I}_B^1$ for $\bar{I}_{Tot}^1$ and $\bar{\boldsymbol{I}}_{\boldsymbol{A}}^{\boldsymbol{h}}$ and $\bar{\boldsymbol{I}}_{\boldsymbol{B}}^{\boldsymbol{h}}$ for $\bar{\boldsymbol{I}}_{\boldsymbol{Tot}}^{\boldsymbol{h}}$, represented by (2.66). This is the basis for the modified HFM proposed in Chapter 6.




a) four different parts of the HAM

b) HAM correlations between voltage and current harmonics

**Figure 2.8:** Dependencies between voltage and current harmonics in HAM.

$$\begin{bmatrix} \bar{I}^1_{Tot} \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{Tot}} \end{bmatrix} = \begin{bmatrix} \bar{I}^1 \\ \bar{I}^2 \\ \bar{I}^3 \\ \vdots \\ \bar{I}^n \end{bmatrix} = \bar{V}^1 \begin{bmatrix} \bar{Y}^{1,1} \\ \bar{Y}^{2,1} \\ \bar{Y}^{3,1} \\ \vdots \\ \bar{Y}^{n,1} \end{bmatrix} + \bar{\boldsymbol{V}}^{\boldsymbol{H}} \begin{bmatrix} \bar{Y}^{1,2} & \bar{Y}^{1,3} & \dots & \bar{Y}^{1,n} \\ \bar{Y}^{2,2} & \bar{Y}^{2,3} & \dots & \bar{Y}^{2,n} \\ \bar{Y}^{3,2} & \bar{Y}^{3,3} & \dots & \bar{Y}^{3,n} \\ \vdots & \vdots & \ddots & \vdots \\ \bar{Y}^{n,2} & \bar{Y}^{n,3} & \dots & \bar{Y}^{n,n} \end{bmatrix} = \begin{bmatrix} \bar{I}^1_A \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{A}} \end{bmatrix} + \begin{bmatrix} \bar{I}^1_B \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{B}} \end{bmatrix} \quad (2.66)$$

In addition, (2.66) can also be normalized by representing $\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{Tot}}$ and $\bar{V}^H$ in percentage of $\bar{I}^1_{Tot}$ and $\bar{V}^1$ respectively, as indicated in (2.67), with the elements $\bar{Y}^{h,H}$ of HAM normalized into $\bar{Y}^{h,H}_{\%}$ of HAM% by using (2.68).

$$\begin{bmatrix} \bar{I}^1_{\%\_Tot} \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{\%\_Tot}} \end{bmatrix} = \begin{bmatrix} \bar{I}^1_{\%} \\ \bar{I}^2_{\%} \\ \bar{I}^3_{\%} \\ \vdots \\ \bar{I}^h_{\%} \end{bmatrix} = \bar{V}^1_{\%} \begin{bmatrix} \bar{Y}^{1,1}_{\%} \\ \bar{Y}^{2,1}_{\%} \\ \bar{Y}^{3,1}_{\%} \\ \vdots \\ \bar{Y}^{h,1}_{\%} \end{bmatrix} + \bar{V}^H_{\%} \begin{bmatrix} \bar{Y}^{1,2}_{\%} & \bar{Y}^{1,3}_{\%} & \dots & \bar{Y}^{1,H}_{\%} \\ \bar{Y}^{2,2}_{\%} & \bar{Y}^{2,3}_{\%} & \dots & \bar{Y}^{2,H}_{\%} \\ \bar{Y}^{3,2}_{\%} & \bar{Y}^{3,3}_{\%} & \dots & \bar{Y}^{3,H}_{\%} \\ \vdots & \vdots & \ddots & \vdots \\ \bar{Y}^{h,2}_{\%} & \bar{Y}^{h,3}_{\%} & \dots & \bar{Y}^{h,H}_{\%} \end{bmatrix} = \begin{bmatrix} \bar{I}^1_{\%\_A} \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{\%\_A}} \end{bmatrix} + \begin{bmatrix} \bar{I}^1_{\%\_B} \\ \bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{\%\_B}} \end{bmatrix} \quad (2.67)$$

$$\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}} = \frac{\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{Tot}}}{\bar{\boldsymbol{V}}^{\boldsymbol{H}}} = \frac{\bar{\boldsymbol{I}}^{\boldsymbol{h}}_{\boldsymbol{\%\_Tot}}}{\bar{\boldsymbol{V}}^{\boldsymbol{H}}_{\%}} \times \frac{\bar{\boldsymbol{I}}^{\boldsymbol{1}}_{\boldsymbol{Tot}}}{\bar{\boldsymbol{V}}^{\boldsymbol{1}}} = \bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\%} \times \frac{\bar{\boldsymbol{I}}^{\boldsymbol{1}}_{\boldsymbol{Tot}}}{\bar{\boldsymbol{V}}^{\boldsymbol{1}}} \quad (2.68)$$

The calculation of the HAM in (2.65) is illustrated as follows: when the supply voltage is sinusoidal, (2.65) turns into (2.69) where $\bar{\boldsymbol{Y}}^{\boldsymbol{h,1}}$ can be directly calculated from the measurement. Although the variation of $\bar{V}^1$ may result in different $\bar{\boldsymbol{I}}^{\boldsymbol{h}}$ and hence different $\bar{\boldsymbol{Y}}^{\boldsymbol{h,1}}$, $\bar{\boldsymbol{Y}}^{\boldsymbol{h,1}}$ is calculated from the measurement under ideal supply condition with 1 p.u. voltage magnitude, as shown in (2.70). When the modelled device is under individual voltage harmonic tests at order *H*, (2.66) turns into (2.71), where each column of HAM%, $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}$, can be easily calculated from the corresponding measurements.

$$\begin{bmatrix} \bar{I}^1 \\ \bar{I}^2 \\ \bar{I}^3 \\ \vdots \\ \bar{I}^n \end{bmatrix} = \bar{V}^1 \begin{bmatrix} \bar{Y}^{1,1} \\ \bar{Y}^{2,1} \\ \bar{Y}^{3,1} \\ \vdots \\ \bar{Y}^{n,1} \end{bmatrix} \tag{2.69}$$

$$\begin{bmatrix} \bar{Y}^{1,1} \\ \bar{Y}^{2,1} \\ \bar{Y}^{3,1} \\ \vdots \\ \bar{Y}^{n,1} \end{bmatrix} = \begin{bmatrix} \bar{I}^1_{1pu} \\ \bar{I}^2_{1pu} \\ \bar{I}^3_{1pu} \\ \vdots \\ \bar{I}^n_{1pu} \end{bmatrix} / \bar{V}^1_{1pu} \tag{2.70}$$

$$\begin{bmatrix} \bar{I}^1 \\ \bar{I}^2 \\ \bar{I}^3 \\ \vdots \\ \bar{I}^n \end{bmatrix} = \bar{V}^1 \begin{bmatrix} \bar{Y}^{1,1} \\ \bar{Y}^{2,1} \\ \bar{Y}^{3,1} \\ \vdots \\ \bar{Y}^{n,1} \end{bmatrix} + \bar{V}^H \begin{bmatrix} \bar{Y}^{1,H} \\ \bar{Y}^{2,H} \\ \bar{Y}^{3,H} \\ \vdots \\ \bar{Y}^{n,H} \end{bmatrix} = \frac{\bar{V}^1}{\bar{V}^1_{1pu}} \begin{bmatrix} \bar{I}^1_{1pu} \\ \bar{I}^2_{1pu} \\ \bar{I}^3_{1pu} \\ \vdots \\ \bar{I}^n_{1pu} \end{bmatrix} + \bar{V}^H \begin{bmatrix} \bar{Y}^{1,H} \\ \bar{Y}^{2,H} \\ \bar{Y}^{3,H} \\ \vdots \\ \bar{Y}^{n,H} \end{bmatrix} \tag{2.71}$$

## 2.7 Network harmonic analysis techniques

Typical network harmonic analysis techniques include: a) direct current injection (or frequency scan), b) harmonic power flow, c) iterative harmonic analysis (IHA), and d) time-domain simulation (TDS) [45][70]. The first three approaches perform network harmonic analysis in the frequency domain with the last one in the time-domain simulation. Based on the technique selected, compatible harmonic models should be applied.

Specifically, the direct current injection approach is applied to investigate the frequency response of the network, by injecting one per-unit harmonic current at specified frequency into the bus of interest [71][72]. As the harmonic voltage at the bus is equal to the injected harmonic current multiplied by the harmonic impedance, it is able to obtain the harmonic impedance based on the measured harmonic voltage. Since the direct current injection approach can provide a picture of the network harmonic impedance, it is normally applied to detect the potential voltage distortions and resonances [71].

With respect to the harmonic power flow technique, it solves harmonic voltages and currents at different frequencies simultaneously by using Newton-type algorithms

[72]. This approach fully takes into account the harmonic cross-coupling effects, resulting in significant computational burdens, especially for the complex network with high orders of harmonics considered. As opposed to harmonic power flow technique, the IHA approach represents the nonlinear loads with their typical current harmonic spectrums. The approach starts with using an estimated supply voltage (e.g. sinusoidal supply voltage with a magnitude of 1 p.u.) to obtain the harmonic currents which in turn, will be applied to achieve the updated harmonic voltages. The updated harmonic voltages will be used to obtain the more accurate current harmonics. The iterative approach stops once the voltage and current variations are within the predefined tolerance limits.

In terms of the TDS, it is a generalised approach which runs the time-domain simulation until a steady-state is reached. For example, by connecting developed CBMs of different types of PE devices to the network model, it is able to investigate their harmonic impact on the voltage and current waveform distortions at different buses.

## 2.8 Chapter conclusions

This chapter first fully discusses the key definitions, symbols and indices for quantifying voltage and current waveform distortions and other general electric power quantities under nonsinusoidal condition, followed by an introduction of the two proposed waveform distortion indices for assessing the contributions of LF harmonics and all other distortions to the total waveform distortion. Those indices will be applied for investigating the harmonic characteristics and performance of considered PE devices in the thesis. After that, the harmonic related standards for limiting the maximum allowed harmonic currents of PE devices are introduced. Moreover, the causes of harmonic current emission of PE devices are classified into internal and external causes, referring to the impact of circuit topologies of PE device and the impact of supply conditions respectively. It turns out that it is important to take into account both internal and external causes when developing harmonic models for modern PE devices.

This chapter also discusses the potential adverse impact of harmonics on LV networks, with the main focus on the impact of harmonics on the power losses, winding temperature and lifetime of distribution transformer. The main part of this chapter is given to the discussion of conventional harmonic modelling techniques and their detailed implementation approaches that will be applied for the harmonic modelling of considered PE devices in the later chapters. Finally, the typical network harmonic analysis techniques are briefly introduced.

# Chapter 3

# Harmonic modelling and characterisation of LED lamps

## 3.1 Introduction

Due to the inherent advantages like low power consumption, high luminous efficiency and long lifetime [73], LED lamps are expected to gradually increase its penetration into LV networks in the next decades, which may have an impact on the network operation. For example, on the one hand, replacing conventional incandescent (IND) lamps or compact fluorescent (CFL) lamps with LED lamps in large numbers will decrease the total power demand for lighting which occupies around 20% of the electricity consumption worldwide [74]. On the other hand, as a type of nonlinear loads, LED lamps will inject harmonics to the grid. Although it is not an issue for a single device, the accumulated harmonic currents from the large-scale adoption of LED lamps may still affect the proper operation of the distribution networks.

As the light output of LEDs are sensitive to the variation of junction temperature, the forward voltage and forward current [75], most of the publications on LED lamps focus on developing novel LED driver circuits with improved performance (e.g. higher circuit efficiency, accurate regulation of LED driving current, high power factor and low harmonic current) and lower costs [73][76][77], and the improved lamp fixture with better thermal performance [78][79]. Only a few papers partially investigate the harmonic emission of LED lamps [80][81][82], and the LED lamp modelling approach for the purpose of network harmonic analysis [83][84]. For example, the harmonic emission of a variety of LED lamps was discussed in [82], without considering the impact of non-ideal supply conditions (e.g. supply voltage distortion with varying magnitudes). In [83], the LED lamp modelling was investigated based on the full-wave rectifier (with smoothing capacitor) circuit topology, without considering the high diversity of LED driver circuits. To fill the gap in existing literature, this chapter will fully investigate the electrical characteristics of residential LED lamps through laboratory testing under different supply conditions. Based on the features of measured

electrical characteristics, the general circuit topologies of tested LED lamps can be obtained and modelled for the network integration studies. The structure of the chapter is as follows: Section 3.2 will introduce the typical driver circuits for LED lamps. Section 3.3 will present the laboratory testing results of residential LED lamps, and the derived classification with corresponding driver circuit topologies. The general modelling approach for each type of driver circuit is given in Section 3.4, with the model accuracy fully validated by measurements. Based on the power dependency of the model parameter values, the generalised model for each type driver circuit topology is developed, which facilitates the next step of model aggregation.

## 3.2 Typical LED driver circuit topologies

The mathematical expressions of the forward voltage and forward current of a LED chip can be represented by (3.1), as indicated in [85], with the corresponding $I_f$-$V_f$ curve illustrated in Figure 3.1 (the black solid line). When LED is operating at its high forward voltage and current region, (3.1) can be simplified to a linear formulation given in (3.2), with the $I_f$-$V_f$ curve (the red solid line) and the electrical model illustrated in Figure 3.1 and Figure 3.2 respectively [85][86].

$$I_f = I_s[\exp\left(\frac{q \cdot V_f}{n \cdot k \cdot T}\right) - 1] \tag{3.1}$$

$$V_f = V_{on} + R_{on} \cdot I_f \tag{3.2}$$

where: $V_f$ and $I_f$ are the diode forward voltage and forward current respectively; $I_s$ is the reverse saturation current; $q$ is the electron charge ($1.602e^{-19}$ Coulombs); n is the ideality factor (equals 1 for perfect diode); $k$ is Boltzmann constant ($1.381e^{-23}$ J/K); $T$ is the operating of the LED; $V_{on}$ is the conduction voltage of LED diode and $R_{on}$ is the series intrinsic resistance of LED.

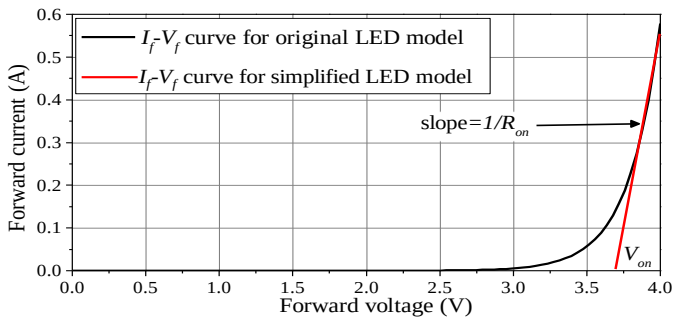



**Figure 3.1:** The $I_f$-$V_f$ curve for both original and simplified LED model.

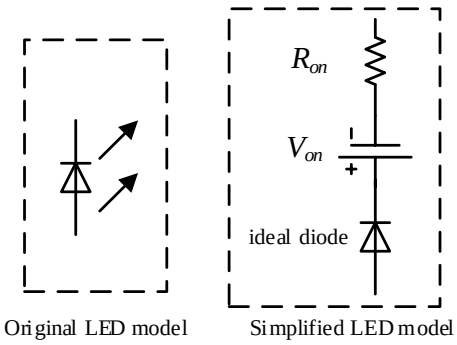



**Figure 3.2:** The simplified electrical model for LED.

As illustrated in Figure 3.1, the LED forward current is very sensitive to its forward voltage, and a slight change of forward voltage will result in a significant variation of forward current and consequently an apparent variation of luminous intensity. Accordingly, the proper design of LED driver circuit should ensure that the forward current is rather constant at the proper working value. Depending on the existence of high-frequency switches, LED driver topologies can be first classified into passive LED drivers and switched-mode LED drivers. For the passive LED drivers, they do not have active switches (excluding the switches used for linear regulator or overvoltage protection circuit), gate drivers, controllers and related power supplies, but consist of passive components including resistors, inductors, capacitors, diodes, transformers, et al. [87]. To provide suitable dc voltage for the LED string, the scaling-down of the mains supply voltage is typically achieved by the input-side transformer, inductor or capacitor for the passive LED drivers. Although the passive LED drivers are easy to design, they have the inherent disadvantages of low efficiency, bulky dc-link capacitor, and the fluctuation of LED forward voltage or forward current with the change of mains supply condition (e.g. varying voltage magnitudes and voltage waveform distortions). In terms of the switched-mode LED drivers, high-frequency switches are applied to achieve active control of the LED forward voltage and current, as well as providing the flexibility of incorporating a variety of functionalities like power factor correction, dimming, circuit fault protecting and thermal tracking [87][88]. In the following subsections, both passive and switched-mode LED drivers will be discussed separately with their typical representative circuit topologies.

### 3.2.1 Passive LED driver circuits

The typical representatives of passive LED driver circuits include the following types: a) step-down transformer based circuit, b) inductive voltage dropper with dc-link capacitor or valley-fill circuit, c) capacitive voltage dropper circuit, d) constant current regulator (CCR) straight circuit. In the following, the working principles and characterised ac side voltage and current waveforms for the five types of passive LED drivers will be analysed based on the corresponding Matlab/Simulink models. In the developed models, the LED string is represented by its simplified circuit model (corresponds to Figure 3.2) with $V_{on}$ and $R_{on}$ equalling 18.24 V and 4.62 Ω respectively.

**Step-down transformer based circuit**

As shown in Figure 3.3, the step-down transformer based circuit use a step-down transformer to drop the mains supply voltage to a value that is required for the LED string. The dc-link capacitor $C_1$ should be sufficiently large to regulate the output voltage ripples within an acceptable range, and the resistor $R_1$ is applied to limit the current fed to the LED string. The typical grid-side voltage and current waveforms of a Matlab/Simulink model for the passive type-a driver are illustrated in Figure 3.4(a), with the corresponding frequency-domain current harmonic magnitudes given in Figure 3.4(b). For the Matlab/Simulink model, $C_1$ and $R_1$ are 4700 μF and 10 Ω respectively, and the step-down transformer is modelled as ideal transformer with negligible transformer leakage. The simulated forward voltage and forward current for the LED string are 21.2 V (with ±0.19 V variation) and 0.65 A (with ±0.04 A variation) respectively. It is observed that the grid-side current is featured with a pulse-like waveform which is rich in harmonics.

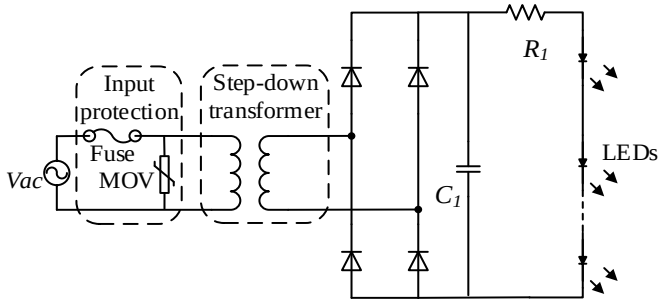
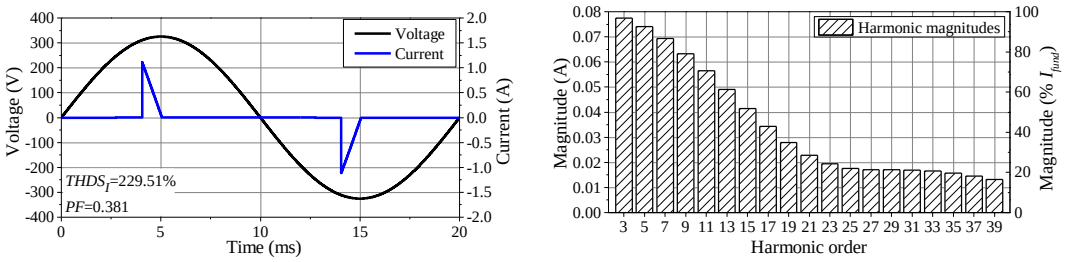



**Figure 3.3:** The circuit schematic for the step-down transformer based LED driver.




a) grid-side voltage and current b) current harmonic spectrum

**Figure 3.4:** Simulated grid-side voltage and current waveforms for the step-down transformer based LED driver, as well as the current harmonic spectrum.

**Inductive dropper with dc-link capacitor or valley-fill circuit**

As shown in Figure 3.5, the inductive dropper circuit uses a large inductor ($L_1$) on the input ac side to scale down the mains voltage [87][88][89]. Additionally, inductor $L_1$ can smooth the grid-side current, and consequently alleviate the harmonic emission from LED lamps. The large inductor $L_2$ is applied to convert the dc-link voltage source to a current source before feeding to the LED string [89]. The dc-link capacitor $C_1$ can be replaced with a typical valley-fill circuit as illustrated in Figure 3.5. The gird-side voltage and current waveforms of a Matlab/Simulink model for the inductive dropper LED driver are illustrated in Figure 3.6(a), with the frequency-domain current harmonics magnitudes given in Figure 3.6(b). For the Matlab/Simulink model, $L_1$, $L_2$ and $C_1$ equal 1.06 H, 1 H and 40 µF respectively while $C_2$ and $C_3$ are both equal to 20 µF. The simulated forward voltage and forward current for the LED string are 21.2 V (with ±0.14 V variation) and 0.65 A (with ±0.03 A variation) respectively. Although this kind of circuit has grid-side current close to sinusoidal, the *PF* is very low (around 0.1), suggesting that the whole circuit is highly inductive (the reactive power demand is much higher than the active power demand). The poor *PF* of this circuit can be slightly improved (due to the large inductor $L_1$) by adding a capacitor in parallel with the mains supply [89].

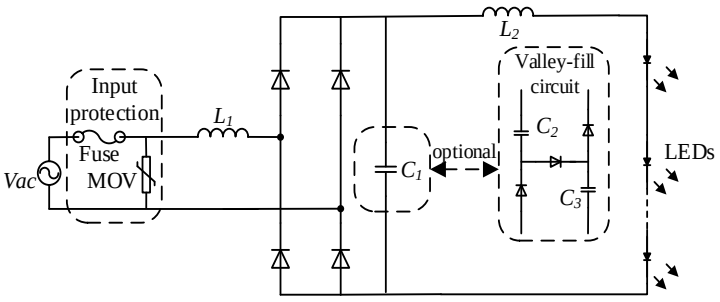
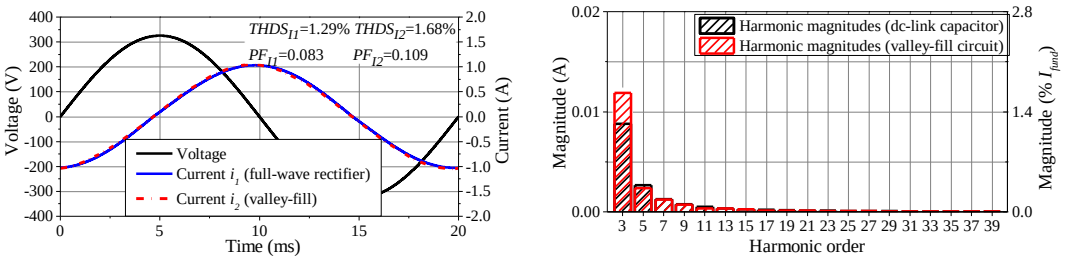



**Figure 3.5:** The circuit schematic for the inductive dropper LED driver.




a) grid-side voltage and current b) current harmonic spectrum

**Figure 3.6:** Simulated grid-side voltage and current waveforms for the inductive dropper LED driver, as well as the current harmonic spectrum.

### Capacitive dropper circuit

The generalised circuit schematic of the capacitive dropper circuit is shown in Figure 3.7, consisting of an input protection circuit, capacitors $C_1$ and $C_2$, resistors $R_1$ and $R_2$, a Zener diode $D_z$ and a full-wave rectifier. Compared with the inductive voltage dropper circuit which uses the grid-side inductor to scale down the mains supply voltage, the voltage step-down for the capacitive voltage dropper circuit is achieved by the grid-side capacitor (Capacitor $C_1$ in Figure 3.7) which also limits the maximum current fed to the LED string. Resistor $R_1$ is used to discharge the capacitor $C_1$ when the mains supply is turned off while resistor $R_2$ is applied to limit the high inrush current when the lamp is turned on.

This kind of circuit is only suitable for low-power applications, as the voltage and current fed to the LED string are affected by the variation of supply conditions (e.g. the voltage magnitude fluctuation). The grid-side voltage and current waveforms of the Matlab/Simulink model for a capacitive dropper LED driver are illustrated in Figure 3.8(a), with the frequency-domain current harmonic magnitudes shown in Figure 3.8(b). For the circuit parameter values of the Matlab/Simulink model, $C_1$ and $C_2$ are equal to 10.7 µF and 4700 µF respectively while $R_1$ and $R_2$ are equal to 470 kΩ and 5 Ω respectively. The simulated forward voltage and forward current for the LED string are 21.2 V (with ±0.18 V variation) and 0.65 A (with ±0.04 A variation) respectively. It is noticed from Figure 3.8(a) that the circuit is highly capacitive with a very low *PF* (around 0.1), implying that the reactive power injection is much higher than the active power consumption. In terms of the harmonic emission, the capacitive dropper circuit has relatively low harmonic emission as shown in Figure 3.8(b).

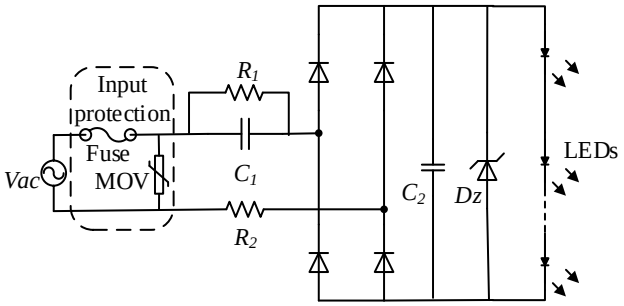
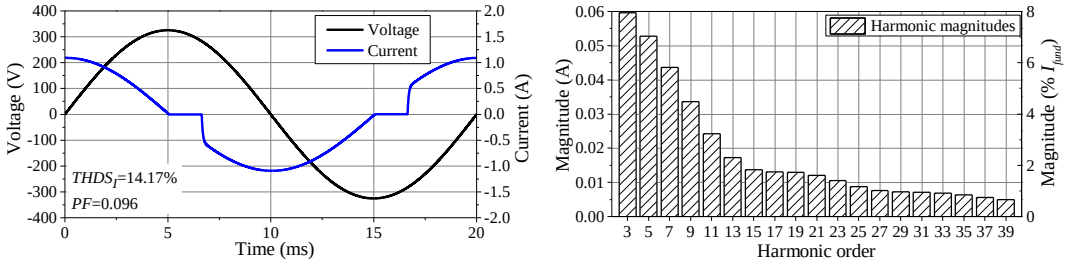



**Figure 3.7:** The circuit schematic for the capacitive dropper LED driver.




a) grid-side voltage and current b) current harmonic spectrum

**Figure 3.8:** Simulated grid-side voltage and current waveforms for the capacitive dropper LED driver, as well as the current harmonic spectrum.

**CCR straight circuit**

The typical circuit schematic of a CCR straight LED driver is shown in Figure 3.9, consisting of a input protection circuit, an EMI filter, a full-wave rectifier, a CCR and the associated overvoltage protection (OVP) circuit. As a key component for this kind of driver, CCR is a type of self-biased transistor, and is able to maintain the flowing-through current (i.e. CCR current) constant over a wide voltage range [90][91]. The CCR current will increase rapidly before the voltage across CCR enters into the current regulation voltage range, for which the CCR current will remain constant, as required by the LED string [90]. In order to avoid the potential damage due to overvoltage, an OVP circuit is usually integrated into the driver and gets activated once the voltage across CCR exceeds its threshold value. Figure 3.9 shows one of the typical OVP circuits, with more details given in [91]. Besides the application in the straight circuit shown in Figure 3.9, CCR can also be applied to other types of circuit topologies like the capacitive dropper circuit and the a-PFC based converters [90]. The grid-side voltage and current waveforms of the Matlab/Simulink model for a CCR straight LED driver are illustrated in Figure 3.10(a), with the frequency-domain current harmonic magnitudes given in Figure 3.10(b). It is observed that the grid-side current is

characterised by a square shape, which is in phase with the grid voltage and low in harmonic emission.

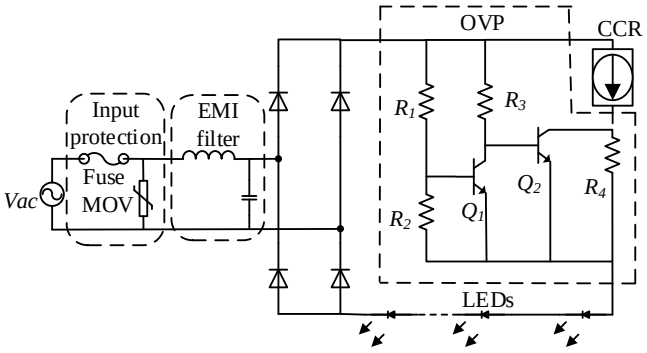
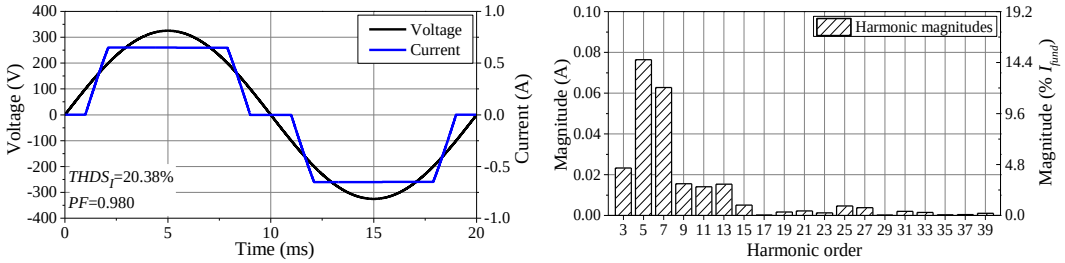



**Figure 3.9:** The circuit schematic for the CCR straight LED driver.




a) grid-side voltage and current b) current harmonic spectrum

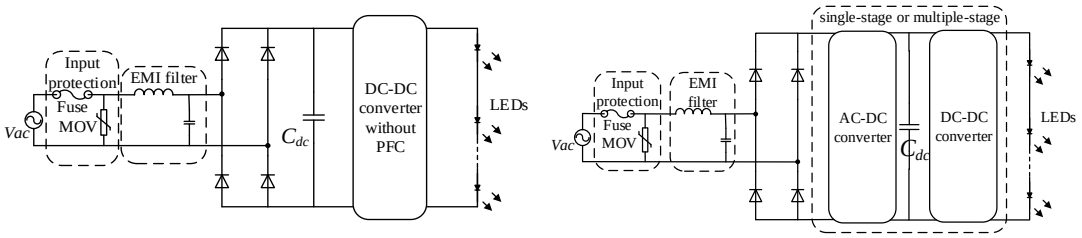
**Figure 3.10:** Simulated grid-side voltage and current waveforms for the CCR straight LED driver, as well as the current harmonic spectrum.

## 3.2.2 Switched-mode LED driver circuits

Depending on the location of the storage capacitor, the circuit topologies of the switched-mode LED drivers can be divided into two types, as illustrated in Figure 3.11 [88]. For the Type 1 switched-mode LED driver circuits, the storage capacitor, $C_{dc}$, is located at low-frequency side (i.e. grid frequency) and is directly connected in parallel with the uncontrolled full-wave rectifier, resulting in a pulse-like input ac current waveform which is similar with the one in Figure 3.4(a). As shown in Figure 3.11(a), Type 1 switched-mode LED driver circuits consist of input protection (e.g. fuse and metal-oxide varistor, MOV), input EMI filter (e.g. L-C circuit), an uncontrolled full-wave rectifier, a storage capacitor $C_{dc}$ and a switching DC-DC converter. The DC-DC switching converter (do not have PFC functionality) is applied to scale down the mains supply voltage, as well as regulating the voltage and current fed to the LED string.

For the Type 2 switched-mode LED driver circuits, the storage capacitor, $C_{dc}$, is located at the high-frequency side after the AC-DC converter, resulting in a less distorted input ac current and improved *PF* as opposed to the Type 1 switched-mode LED driver circuits. As the AC-DC converter topologies and the corresponding control algorithms are high in diversity, it is difficult to specify the generalised working principles and related electrical characteristics of switched-mode LED lamps.

Depending on whether the input AC-DC converter and output DC-DC converter are integrated into the one-stage regulation circuit, Type 2 switched-mode LED driver circuits can be further divided into the single-stage and multiple-stage sub-types. Typical single-stage converters for LED lamps include buck, buck-boost, SEPIC, flyback, half-bridge, push-pull converters and other types of converters [88]. In the multi-stage LED drivers, the AC-DC converter provides both regulation of the input ac current and pre-regulation of the output dc voltage, while one or more subsequent DC-DC converters help to precisely regulate dc voltage and current, as in e.g., constant current mode of operation, when constant current is supplied to the LED string over wider ranges of supply voltage variations. As opposed to single-stage drivers, multi-stage drivers require more power electronic components, and therefore increased cost and complexity of the circuit design to ensure high efficiency. Accordingly, multi-stage LED driver circuits are normally applied in high-power LED applications (e.g. for LED spotlights), where the cost is less of an issue [88] and power losses inside the LED lamp are minimized by optimising design and circuit configuration for the specific LED string length.




a) Type 1 b) Type 2

**Figure 3.11:** The two circuit topologies for the switched-mode LED driver circuits.

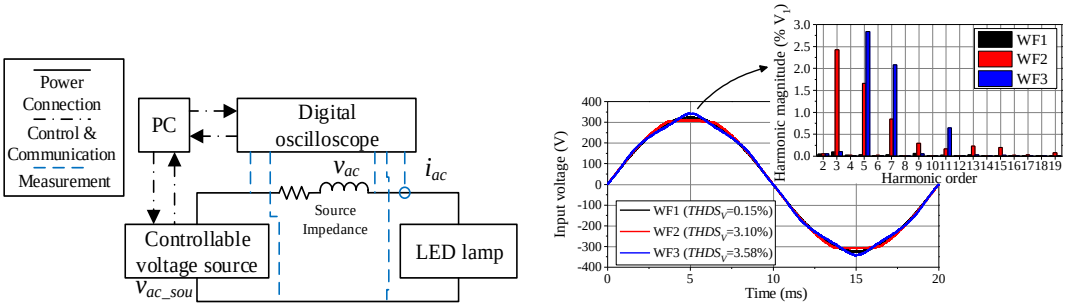
## 3.3 Laboratory testing of residential LED lamps

This section presents the comprehensive testing results of 28 different LED lamps from 13 different European manufacturers, with the rated power, $P_{rated}$, ranging from 3 W to 25 W. The upper limit of 25 W is selected due to a simple fact that most of the LED lamps for residential applications are with $P_{rated}$ below 25 W, and as [42] stipulates harmonic limits for only discharge-type lighting equipment (e.g. CFLs) with $P_{rated}$ lower than 25 W [42] (denoted as "Class C" in [42]). In this section, the harmonic limits for the discharge-type lighting equipment in [42] (denoted as "Class C" limits), will be applied to evaluate the harmonic compliance of tested LED lamps. Based on the features of input ac current waveforms and the distribution characteristics of the electric power quantities (e.g. *PF*, $PF_1$, $THDS_I$, etc.) under ideal supply condition, tested LED lamps will be classified into different types, with their general driver circuit topologies being discussed. The obtained classification will be validated by the voltage dependency of the electrical characteristics of tested LED lamps under comprehensive supply conditions.

### 3.3.1 Test set-up

The experimental set-up for testing LED lamps is illustrated in Figure 3.12(a), consisting of a fully controllable ac voltage source (used to emulate different voltage distortion as shown in Figure 3.12(b)), a control PC, a digital oscilloscope for data acquisition (500 kSa/s). The three voltage waveforms applied in the tests are: a) ideally sinusoidal waveform, b) "flat-top" distorted waveform (WF2, representing the typical residential LV network), c) "pointed-top" distorted voltage waveform (WF3, representing typical industrial LV networks), Figure 3.12(b). The rms voltage magnitude is varied from 0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u., and two source impedance values are applied separately: ZS1=0 and ZS2=(0.4+0.25j) Ω, representing maximum expected impedance in LV networks (e.g. this value is exceeded for only about 2% of LV customers in the UK) [92]. The ZS2 value is often denoted as "flicker" impedance. The basic data on the 28 tested LED lamps are tabulated in Table 3.1, which not only lists the nameplate information (e.g. brand, luminous flux, colour temperature, etc), but also discloses the measured electrical characteristics under ideal supply condition, using calculation equations from [33][37][93]. The last column

evaluates the compliance with [42]. Although 7 of 28 tested lamps are dimmable, dimmers are not applied in the tests.




a) experimental set-up b) different supply voltage waveforms

**Figure 3.12:** The general experimental set-up for testing LED lamps, as well as the three supply voltage waveforms applied.

**Table 3.1:** Basic information on the tested LED lamps.

| No. | Nameplate Data | | | | | Measured and Calculated Values | | | | | | | | | Comply. with [42] (Y/N) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | *Brand* | $P_{rated}$ (W) | *Luminous flux (lm)* | *Color Temp. (K)* | *Dimmable (Y/N)* | *P* (W) | $Q_1$ (VAr) | *PF* | $PF_1$ | $PF_d$ | $THDS_I$ (% of $I_1$) | *THCS* (mA) | $TH\&IHD_{I,HF}$ (% of $I_1$) | $TH\&IHC_{HF}$ (mA) | |
| 1 | B1 | 3 | 200 | 6500 | No | 2.76 | -1.64 | 0.41 | 0.86 | 0.48 | 183.90 | 25.60 | 22.09 | 3.07 | No |
| 2 | B2 | 5.5 | 470 | 2700 | No | 4.95 | -1.98 | 0.54 | 0.93 | 0.58 | 139.13 | 32.25 | 19.70 | 4.57 | No |
| 3 | B2 | 6 | 470 | 2700 | No | 6.02 | -2.26 | 0.53 | 0.94 | 0.56 | 143.79 | 40.12 | 17.51 | 4.89 | No |
| 4 | B3 | 8 | 470 | 2700 | No | 7.33 | -2.95 | 0.54 | 0.93 | 0.58 | 137.87 | 47.55 | 19.75 | 6.81 | No |
| 5 | B2 | 8 | 806 | 2700 | No | 7.64 | -2.52 | 0.53 | 0.95 | 0.56 | 148.12 | 51.82 | 9.67 | 3.38 | No |
| 6 | B4 | 9.5 | 806 | 2700 | No | 8.99 | -4.09 | 0.56 | 0.91 | 0.62 | 128.53 | 55.18 | 16.93 | 7.27 | No |
| 7 | B2 | 9.5 | 806 | 2700 | Yes | 9.32 | -4.89 | 0.60 | 0.89 | 0.67 | 106.49 | 48.67 | 15.27 | 6.98 | Yes |
| 8 | B2 | 11 | 1055 | 2700 | No | 10.2 | -3.00 | 0.51 | 0.96 | 0.53 | 157.12 | 72.57 | 12.23 | 5.65 | No |
| 9 | B5 | 12 | 1010 | 2700 | No | 10.9 | -3.14 | 0.48 | 0.96 | 0.50 | 171.02 | 84.87 | 25.93 | 12.87 | No |
| 10 | B6 | 15 | 1350 | 2700 | No | 11.7 | -2.80 | 0.43 | 0.97 | 0.44 | 197.61 | 103.8 | 43.15 | 22.67 | No |
| 11 | B2 | 13 | 1521 | 2700 | No | 13.0 | -4.29 | 0.54 | 0.95 | 0.57 | 145.74 | 86.73 | 10.54 | 6.27 | No |
| 12 | B1 | 5 | 400 | 6500 | No | 4.47 | -9.09 | 0.39 | 0.44 | 0.89 | 49.20 | 21.60 | 10.26 | 4.51 | Yes |
| 13 | B7 | 9 | 806 | 3000 | No | 9.42 | -9.39 | 0.57 | 0.71 | 0.80 | 73.00 | 42.22 | 12.35 | 7.14 | Yes |
| 14 | B8 | 10 | 950 | 6500 | No | 10.4 | -12.38 | 0.56 | 0.64 | 0.88 | 57.43 | 40.37 | 7.60 | 5.34 | Yes |
| 15 | B8 | 18 | 1700 | 6500 | No | 17.2 | -31.54 | 0.44 | 0.48 | 0.92 | 43.18 | 67.45 | 5.91 | 9.24 | Yes |
| 16 | B8 | 20 | 1880 | 6500 | No | 19.5 | -29.72 | 0.49 | 0.55 | 0.89 | 49.08 | 75.82 | 6.29 | 9.72 | Yes |
| 17 | B8 | 25 | 2250 | 6500 | No | 22.8 | -22.99 | 0.59 | 0.70 | 0.84 | 64.19 | 90.29 | 6.61 | 9.29 | Yes |
| 18 | B9 | 8 | 1010 | 2700 | Yes | 5.11 | -0.02 | 0.88 | 1.00 | 0.88 | 53.61 | 11.90 | 4.25 | 0.94 | Yes |
| 19 | B10 | 15 | 1150 | 3000 | Yes | 13.3 | -0.06 | 0.96 | 1.00 | 0.96 | 27.71 | 16.13 | 2.05 | 1.19 | Yes |
| 20 | B11 | 6.7 | 490 | 2700 | Yes | 6.94 | -1.95 | 0.91 | 0.96 | 0.95 | 32.98 | 10.32 | 4.08 | 1.28 | Yes |
| 21 | B4 | 7 | 470 | 2700 | No | 7.41 | -2.87 | 0.92 | 0.93 | 0.99 | 10.10 | 3.48 | 9.48 | 3.27 | Yes |
| 22 | B12 | 9 | 806 | 2700 | Yes | 8.47 | -6.01 | 0.70 | 0.82 | 0.85 | 58.71 | 26.49 | 12.86 | 5.80 | No |
| 23 | B1 | 10 | 806 | 6500 | No | 9.22 | -3.33 | 0.93 | 0.94 | 0.99 | 16.79 | 7.14 | 6.37 | 2.71 | Yes |
| 24 | B13 | 15 | 1500 | 6000 | No | 11.9 | -2.35 | 0.66 | 0.98 | 0.67 | 21.54 | 11.43 | 53.94 | 28.61 | Yes |
| 25 | B11 | 11. | 810 | 2700 | Yes | 12.1 | -3.54 | 0.95 | 0.96 | 0.99 | 12.18 | 6.69 | 6.83 | 3.75 | Yes |
| 26 | B1 | 13 | 1055 | 6500 | No | 12.2 | -4.12 | 0.93 | 0.95 | 0.98 | 19.09 | 10.67 | 5.55 | 3.10 | Yes |
| 27 | B7 | 14 | 1055 | 3000 | Yes | 12.9 | -3.05 | 0.93 | 0.97 | 0.96 | 32.28 | 18.57 | 2.42 | 1.39 | Yes |
| 28 | B8 | 15 | 1390 | 6500 | No | 15.8 | -4.66 | 0.95 | 0.96 | 0.99 | 15.94 | 11.47 | 5.42 | 3.90 | Yes |

Note: *PF*, $PF_1$, $PF_d$ are true, displacement, distortion power factors, *P* is active power, $Q_1$ is fundamental reactive power, *THCS*/$THDS_I$ are total subgroup low frequency (LF) harmonic current/distortion, $TH\&IHC_{HF}$/$TH\&IHD_{I,HF}$ are total high frequency (HF) harmonic and interharmonic current/distortion (up to 9 kHz).

### 3.3.2 Classification of tested LED lamps

In Table 3.1, big variations of $PF$ (0.39-0.96), $PF_1$ (0.44-1), $PF_d$ (0.44-0.99), $THDS_I$ (10.1%-197.61%) and $TH\&IHD_{I,HF}$ (2.05%-53.94%) values are observed among the tested LED lamps. However, similarities of certain electrical characteristics are also noticed among some of the tested LED lamps. For example, when plotting $PF$, $PF_1$ and $THDS_I$ given in Table 3.1 together as in Figure 3.13, it is noticed that LED1-11 are characterized by low $PF$ (0.41-0.60), high $PF_1$ (0.86-0.97) and very high $THDS_I$ (above 100%), while LEDs 12-17 are featured with low $PF$ (0.39-0.59), low $PF_1$ (0.44-0.7, hence high $Q_1$) and relatively low $THDS_I$ (43.18%-73%)). LED18-19 have highest $PF_1$ (unity) as opposed to the others, with relatively low $THDS_I$ (27.71% and 53.61% respectively). LED20-28 have further improved electrical characteristics with high $PF$ (close to 1, except LED22, 24) and very low $THDS_I$ (around 10%-20%, except LED20, 22 and 27). Accordingly, tested LED lamps are classified into four types as listed in Table 3.2, as well as the ranges of $PF$, $PF_1$, $PF_d$ and $THDS_I$, and $TH\&IHD_{I,HF}$ for each type.

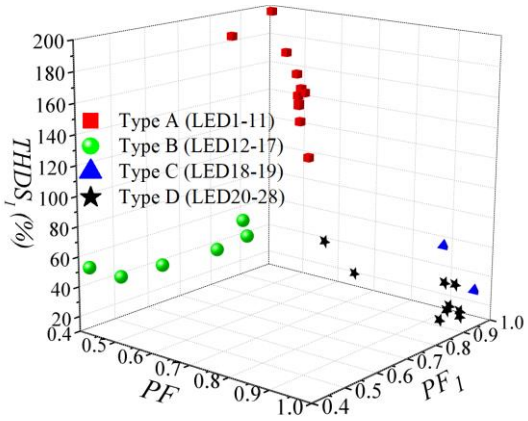



**Figure 3.13:** Grouping of tested LED lamps according to their calculated $PF$, $PF_1$ and $THDS_I$ (under ideal supply condition).

**Table 3.2:** Classification of tested LED lamps based on $PF$, $PF_1$, $PF_d$, $THDS_I$ and $TH\&IHD_{I,HF}$ (under ideal supply condition).

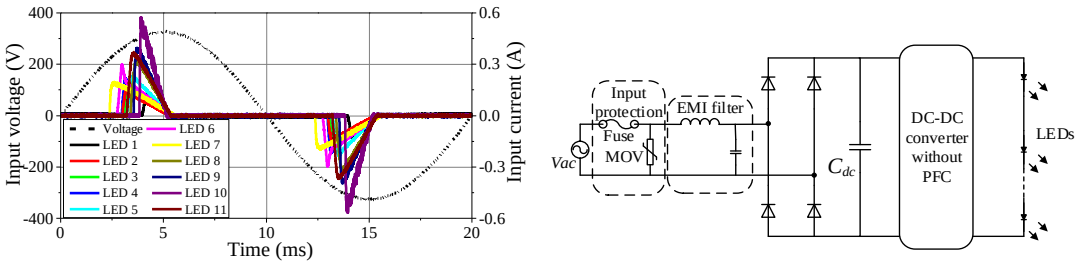
| LED Type | $PF$ | $PF_1$ | $PF_d$ | $THDS_I$ (%) | $TH\&IHD_{I,HF}$ (%) |
|---|---|---|---|---|---|
| **A (LED1-11)** | 0.41-0.60 | 0.86-0.97 | 0.44-0.67 | 106.49-197.61 | 9.67-43.15 |
| **B (LED12-17)** | 0.39-0.59 | 0.44-0.71 | 0.80-0.92 | 43.18-73 | 5.91-12.35 |
| **C (LED18-19)** | 0.88-0.96 | 1.00 | 0.88-0.96 | 27.71-53.61 | 2.05-4.25 |
| **D (LED20-28)** | 0.70-0.95 | 0.82-0.98 | 0.67-0.99 | 10.10-58.71 | 2.42-53.94 |

Due to the distinctive input current waveform shapes among for each type LED lamps, their general circuit topologies can be obtained and will be discussed separately in the following.

**Type A: full-wave rectifier with smoothing capacitor and DC-DC converter circuit (without PFC)**

As shown in Figure 3.14(a), Type A LED lamps (LED1-11 in Table 3.1) are featured with a pulse-like current waveform shape with the conduction time being around ¼ of the input voltage period (conducts around the peak area of input voltage waveform), resulting in high $PF_1$, high $THDS_I$ and low $PF$. The input current waveform shape suggests that the AC-DC conversion stage for Type A LED lamps is made up of an uncontrolled full-wave rectifier followed by a large smoothing capacitor. The general circuit topology for Type A LED lamps is shown in Figure 3.14(b), and belongs to the Type 1 switched-mode LED driver circuits discussed in Section 3.2.2.

As shown in Table 3.1, almost all Type A LED lamps violate the harmonic emission limits in [42], except LED7 which has the longest conduction period as shown in Figure 3.14(a). The pulse-like current waveform with short conduction period makes Type A LED lamps have much higher harmonic emission than the other three types.



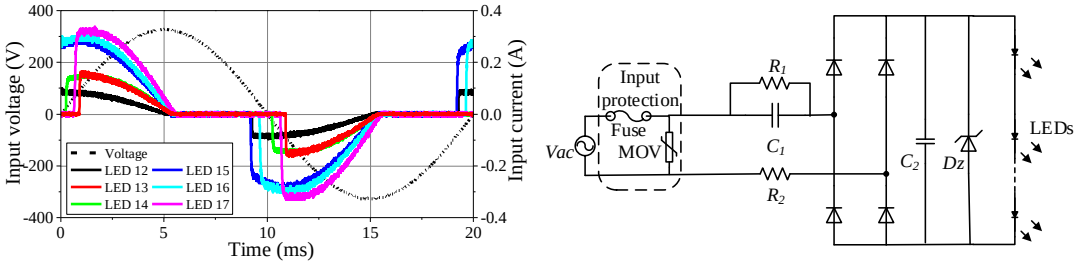

a) input voltage and current waveforms b) general circuit topology

**Figure 3.14:** Input voltage and current waveforms (under ideal supply condition) of Type A LED lamps and their general circuit topology.

**Type B: capacitive dropper circuit**

As shown in Figure 3.15, the input current of type B LED lamps (LED12-17 in Table 3.1) starts to conduct around the zero-crossing point of input voltage waveform until reaching its peak point, resulting in a highly capacitive circuit with low $PF_1$ (0.44-0.7). Compared with Type A LED lamps, the conduction time increases to around half of the input voltage period, contributing to relatively low $THDS_I$ (43.18%-73%) and $TH\&IHD_{I,HF}$ (5.91%-12.35%), high $PF_d$ (0.8-0.92), and hence good compliance with

[42]. The combined effect of high $PF_d$ and low $PF_1$ does not improve the $PF$ of Type B LED lamps with respect to that of Type A. The general circuit topology is illustrated in Figure 3.15(b), and has been analysed in Section 3.2.1.

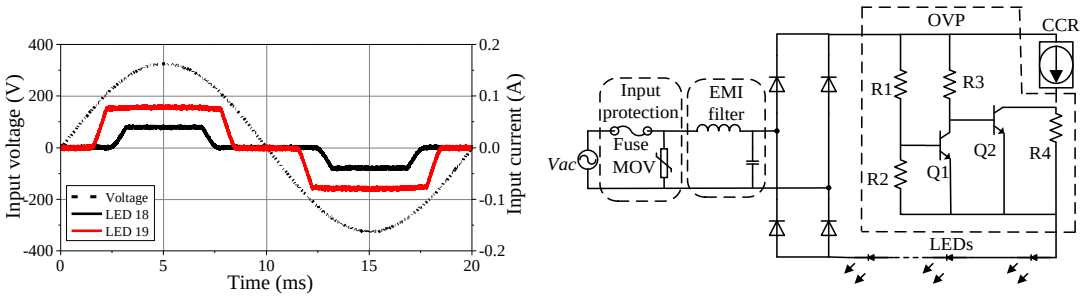



a) input voltage and current waveforms b) general circuit topology

**Figure 3.15:** Input voltage and current waveforms (under ideal supply condition) of Type B LED lamps and their general circuit topology.

**Type C: CCR straight circuit**

Unlike the other three type LED lamps, Type C LED lamps (LED18-19 in Table 3.1) are characterised by square-shaped input current waveform, as illustrated in Figure 3.16(a), due to the applied constant current regulator (CCR). The general circuit topology is given in Figure 3.16(b), consisting of an input protection circuit, input EMI filter, an uncontrolled full-wave rectifier, the OVP circuit and the CCR. The working principles of each circuit part has been discussed in Section 3.2.1 and will not be repeated here. The harmonic emission of Type C LED lamps is relatively low (27.71%-53.61% for $THDS_I$ and 2.05%-4.25% $TH\&IHD_{I,HF}$) and can easily comply with limits specified in [42].

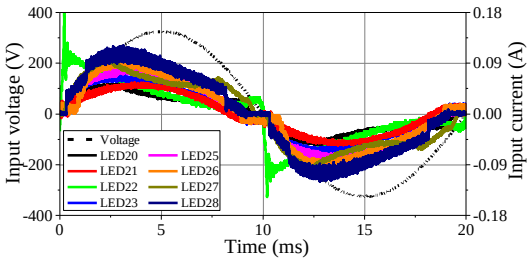



a) input voltage and current waveforms b) different supply voltage waveforms

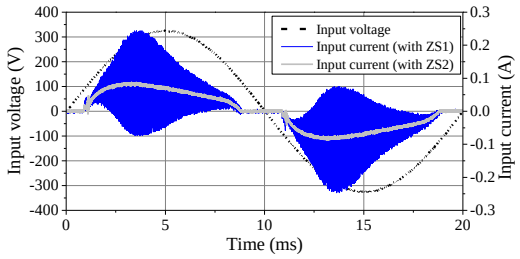
**Figure 3.16:** Input voltage and current waveforms (under ideal supply condition) of Type C LED lamps and their general circuit topology.

**Type D: switch-mode driver circuit (with a-PFC)**

As opposed to the other three types, the input current waveform of Type D LED lamps (LED20-28 in Table 3.1 except LED24) almost conducts the whole input voltage period (except the small dead zone around the zero-crossing of input voltage) and is in phase with the input voltage, as illustrated in Figure 3.17(a), which is attributed to the applied a-PFC circuit. Unlike LED20-23 & LED25-28 working at continuous conduction mode (CCM), LED24 works at discontinuous conduction mode (DCM), resulting in significant emission of high frequency (around 190 kHz) current harmonics, as shown in Figure 3.17(b). Although Type D LED lamps can be further divided to different groups depending on the a-PFC converter and control circuit applied, it is difficult to figure out their circuit topologies merely from the input current waveform shape (due to lack of features) and hence sub-classification is not taken into account. The general circuit topology and working principles have been discussed in Section 3.2.2 (corresponds to the Type 2 switched-mode LED driver circuits).




a) voltage and current waveforms (LED20-23, 25-28)




b) voltage and current waveforms (LED24)

**Figure 3.17:** Input voltage and current waveforms (under ideal supply condition) of Type D LED lamps.

## 3.3.3 Impact of supply conditions on the electrical characteristics of LED lamps

To further evaluate the validity of the proposed classification in Section 3.2, the impact of different supply conditions on the electrical characteristics (*PF*, $PF_1$, $PF_d$, $THDS_I$ and $TH\&IHD_{I,HF}$) of the four type LED lamps are fully analysed in this section. The change of supply conditions refers to a combination of three different supply voltage waveforms, five voltage magnitudes and two source impedance as described in Section 3.3.1. The impact of varying supply conditions on the electrical characteristics of tested LED lamps are illustrated in Figures 3.18-3.21. In Figures 3.18-3.21, *P*, $Q_1$, $THDS_I$ and $TH\&IHD_{I,HF}$ are normalized with respect to the nominal values in Table

3.1 while *PF*, $PF_1$ and $PF_d$ are given in actual values for different supply voltage conditions under ZS1. As ZS2 mainly affects the high-frequency harmonic emission from the observation of testes, $TH\&IHD_{I,HF}$ under ZS2 are also shown in order to compare with the value under ZS1. The black, red and blue colour correspond to WF1, WF2 and WF3, respectively, while the arrow represents the change of indices from 0.9 p.u. to 1.1 p.u. supply voltage magnitude. In addition, the supply voltage dependency of indices is further represented by the exponential fitting coefficient, $k_{exp}$, which is calculated by applying the exponential fitting function (in the form of $P_{pu}=V_{pu}^{kexp}$) to the indices values at five voltage magnitudes (from 0.9 p.u to 1.1 p.u. with a step of 0.05 p.u.). Specifically, a close to zero $k_{exp}$ indicates that the considered electric indices are insensitive to the change of voltage magnitudes, while a $k_{exp}$ equalling one suggests the indices increase linearly with the increasing voltage magnitudes. The higher $k_{exp}$ refers to the stronger voltage magnitude dependency of indices. In addition, a negative $k_{exp}$ indicates a reverse relationship between indices and voltage magnitudes. The impact of varying supply conditions on the electrical characteristics of tested LED lamps will be discussed separately in the following.

**Changes in active power, *P***

It is observed from Figure 3.18 that the supply conditions have negligible impact on *P* of Type A LED lamps (except LED7), and *P* is maintained constant around 1 p.u. *P* of LED7 increases with the increasing voltage magnitudes, with a slight decrease under WF2 and a slight increase under WF3. Type B LED lamps have a strongest positive dependency of *P* on supply voltage magnitudes ($k_{exp}$ is between 2 and 3 for WF1-3), where *P* decreases under WF2 and increases under WF3. For Type C LED lamps, the increase of supply voltage magnitudes results in an increase of *P*, while WF2 and WF3 have negligible impacts on *P*. For Type D LED lamps, *P* is either independent of supply voltage magnitudes (LED23-24, 26, 28 with $k_{exp}$ between 0.5 and 1), or shows a weak dependency (LED20-22, 25, 27 with $k_{exp}$ close to 0), while voltage distortion has negligible impact, except on LED21, for which *P* slightly increases under WF2 and slightly decreases under WF3. The above changes are consistent for LED lamps in each type/class.

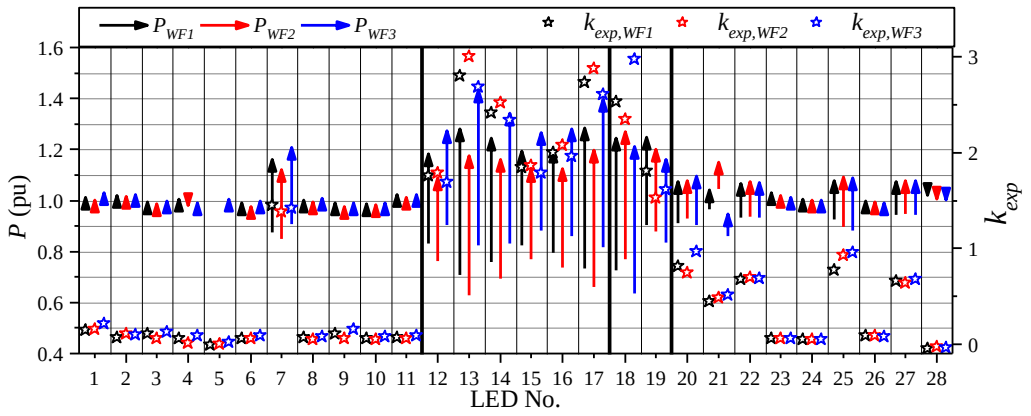



**Figure 3.18:** The impact of varying supply conditions on active power, *P* (at ZS1).

**Changes in fundamental reactive power, $Q_1$**

As shown in Figure 3.19, $Q_1$ of Type A LED lamps is more sensitive to voltage waveform distortions as opposed to the change of voltage magnitudes, with an apparent increase under WF2 and a significant decrease under WF3. For Type B LED lamps except LED7, the increase of supply voltage magnitudes result in s significant increase of $Q_1$ ($k_{exp}$ is above 2), with voltage distortion having little impacts. For Type C LED lamps, there is no obvious relationship between supply conditions and $Q_1$, considering the fact that their $Q_1$ is negligible because of unity $PF_1$. For type D LED lamps, an exponential relationship exists between $Q_1$ and supply voltage magnitudes ($k_{exp}$ is around 2), and voltage distortion has negligible impact on $Q_1$. The above changes are consistent for LED lamps in each type/class.

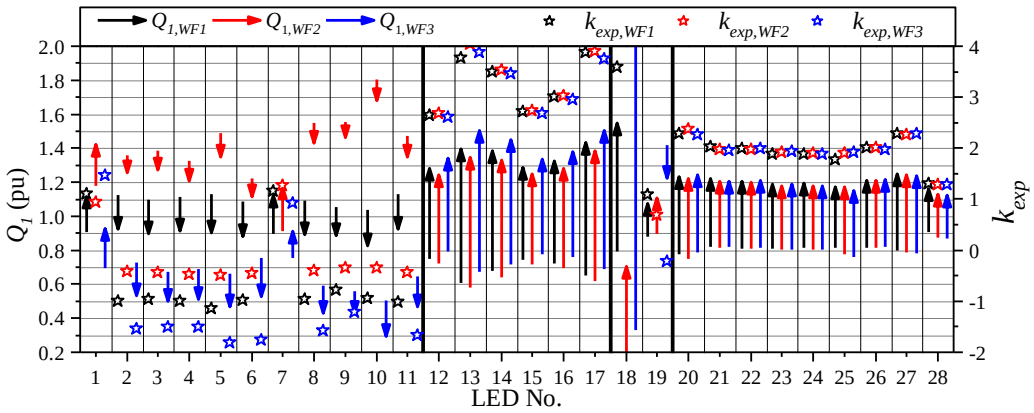
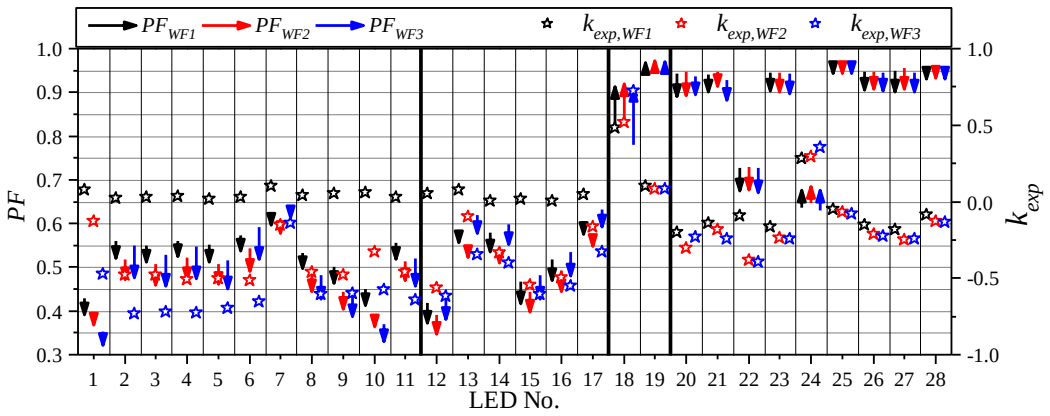


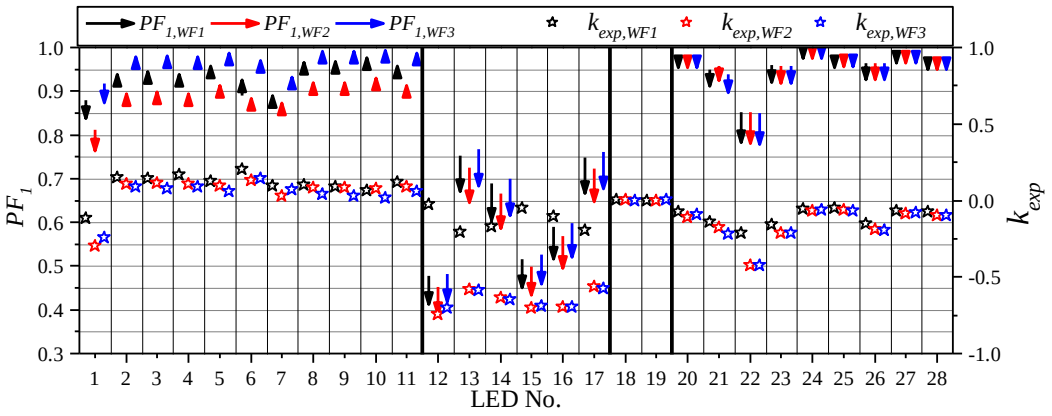

**Figure 3.19:** The impact of varying supply conditions on the fundamental reactive power, $Q_1$ (at ZS1).

**Changes in power factors (*PF*, $PF_1$ and $PF_d$)**

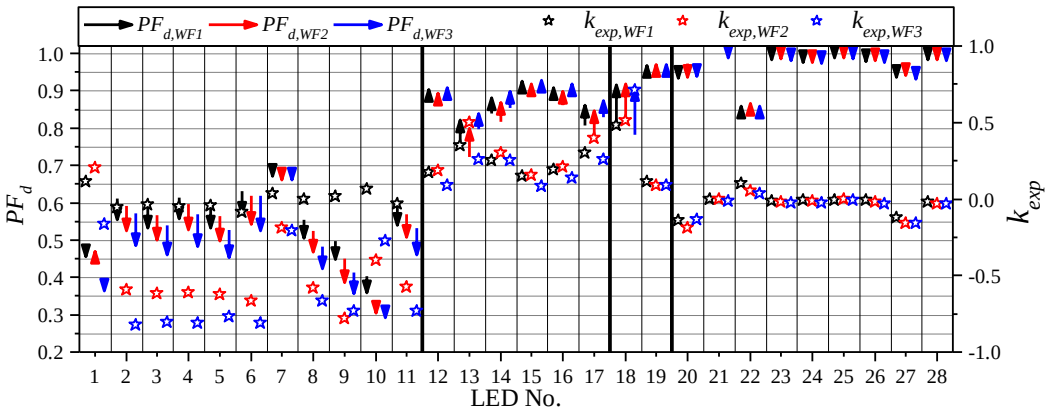
The changes in power factors for tested LED lamps under different supply conditions are illustrated in Figure 3.20. For Types A, B and D LED lamps, increasing supply voltage magnitude results in a slight decrease of *PF*, while the opposite trend is observed for Type D LED lamps. In terms of the impact of voltage distortion, *PF* of Type A LED lamps slightly decreases under WF2 and WF3, while *PF* of Type B LED lamps slightly increases under WF3 and slightly decreases under WF2. For Types C and D LED lamps, supply voltage distortion has negligible impact on the *PF* values. For Types A and B LED lamps, $PF_1$ will increase under WF3 and decrease under WF2, with $PF_1$ of Type B LED lamps being more sensitive to the varying supply voltage magnitudes (increasing magnitude leads to decreasing $PF_1$, with $k_{exp}$ being around 0.7 under WF2 and WF3). $PF_1$ of Type C LED lamps is around 1 for all supply conditions ($k_{exp}$ equals 0), while $PF_1$ of Type D LED lamps is also insensitive to changes of supply voltage conditions (except LED22 with the $PF_1$ slightly decreases with the increasing voltage magnitudes). The changes of $PF_d$ for Types A, C and D LED lamps are similar to their *PF* changes, while for Type B LED lamps, $PF_d$ is greater than *PF* and $PF_1$ and follows the changes of voltage magnitudes, exhibiting slightly decrease under WF2 and slightly increase under WF3. Except Type A LED lamps under WF2 and WF3 whose $PF_d$ slightly decreases with the increasing voltage magnitudes, $PF_d$ of Type B, C and D LED lamps are almost under varying supply conditions with $k_{exp}$ close to 0. The above changes are consistent for LED lamps in each type/class.




a) *PF*




b) $PF_1$

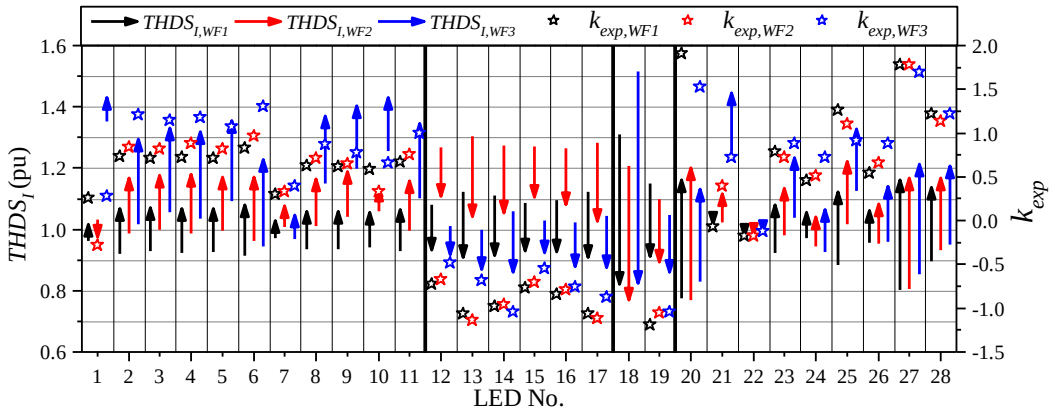



c) $PF_d$

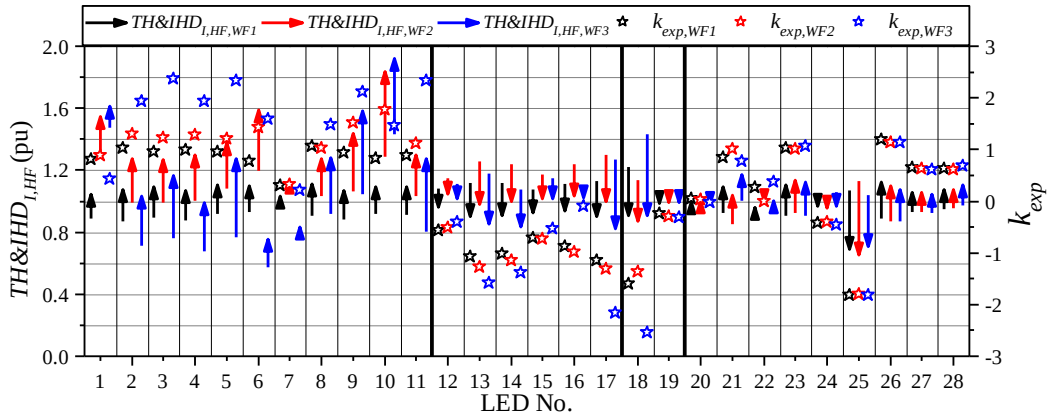
**Figure 3.20:** The impact of varying supply conditions on the power factors, *PF*, $PF_1$ and $PF_d$ (at ZS1).

**Changes in LF and HF harmonic emission ($THDS_I$ and $TH\&IHD_{I,HF}$)**

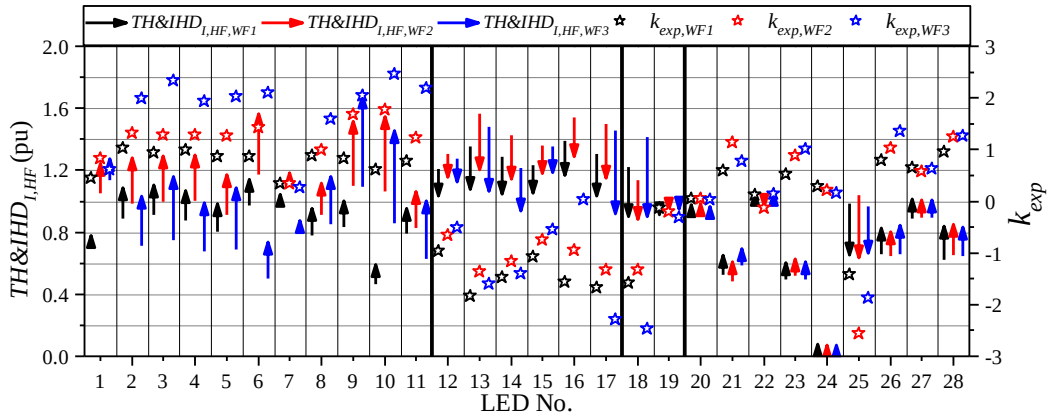
The changes in LF and HF harmonics emission for tested LED lamps under different supply conditions are illustrated in Figure 3.21. For Types A and D LED lamps, the increase of supply voltage magnitudes generally leads to an increase of $THDS_I$ and $TH\&IHD_{I,HF}$ (positive $k_{exp}$ is observed), while the opposite trend is observed for Types B and C LED lamps (negative $k_{exp}$ is observed). In terms of the impact of voltage distortion, it varies significantly among different lamp types: for some lamps, it is more pronounced for WF3, while for the others, it is more pronounced for WF2. Accordingly, it can be generally concluded that the changes in LF and HF current waveform distortion of tested lamps are less consistent than previously discussed changes in active/reactive power demands and three power factor values. The impact of source impedance on HF waveform distortion is noticeable and can be followed from the results in the last two plots of Figure 3.21.




a) $THDS_I$ (at ZS1)




b) $TH\&IHD_{I,HF}$ (at ZS1)




c) $TH\&IHD_{I,HF}$ (at ZS2)

**Figure 3.21:** The impact of varying supply conditions on the power factors, $THDS_I$ (at ZS1) and $TH\&IHD_{I,HF}$ (at both ZS1 and ZS2).

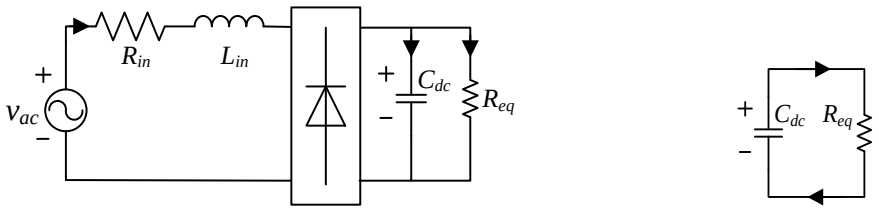
From the above discussion, it turns out that the supply voltage dependency of the electrical characteristics of tested LED lamps follows the presented classification, implying that it is possible to develop generalised models for each type LED lamps and will be discussed in the next section in detail.

## 3.4 Modelling of residential LED lamps

Based on the classification of tested LED lamps given in the last section, this section will introduce generalised modelling approach for each type. With the proposed approaches, the model circuit parameter values can be easily obtained from the measurements, with the model accuracy fully validated by measurements under different supply voltage conditions. Based on the distribution characteristics of parameter values for each type circuit topology, the generic model can be obtained, and can be directly applied for developing the corresponding aggregate model. In the following, the modelling approaches of the four type LED drivers will be discussed separately.

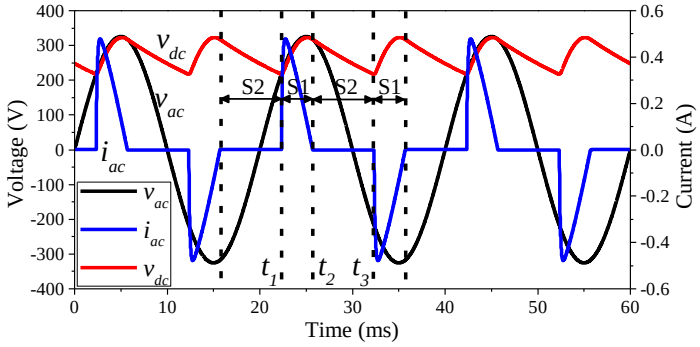
### 3.4.1 Type A LED lamps

The generalised circuit model for Type A LED lamps is shown in Figure 3.22(a), consisting of the input side resistor, $R_{in}$, the input side filter, $L_{in}$, the dc-link capacitor $C_{in}$, and the equivalent resistance, $R_{eq}$, for the followed DC-DC converters and LED strings. It has two different working states, which are the capacitor charging state S1 and the capacitor discharging state S2, as illustrated in Figure 3.22(a) and Figure 3.22(b) respectively. For the capacitor charging state S1, both $C_{dc}$ and $R_{eq}$ get the current supply from the mains supply, while for the capacitor discharging state S2, no current flow on the input ac side and $C_{dc}$ is discharging though the resistor $R_{eq}$ (forms a RC discharging circuit). By observing the input ac voltage and current ($v_{ac}$ and $i_{ac}$), and the dc-link voltage waveforms ($v_{dc}$) of a typical type A LED lamp shown in Figure 3.23, the two working modes can be clearly reflected from the input ac current waveform shape, implying the possibility of estimating the model circuit parameter values from the synchronized input ac voltage and current waveforms. In order to achieve that objective, establishing the mathematical relationship between the model circuit parameter values and the input ac voltage and current waveforms is required, with the derivation process given in the following.

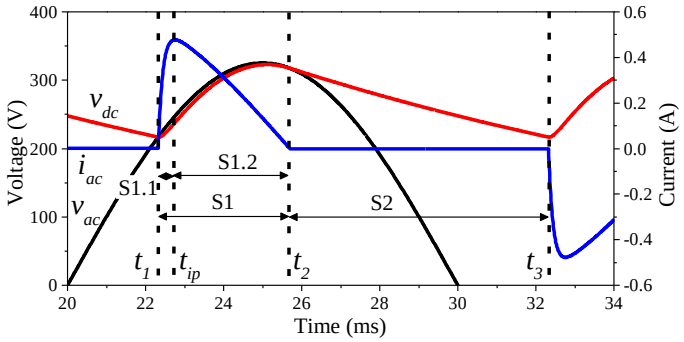



a) S1 b) S2

**Figure 3.22:** The two working states for the generalised circuit model of the Type A LED driver.




a) input ac voltage and current, and dc-link voltage




b) zooming-part

**Figure 3.23:** The input ac side voltage and current waveforms and dc-link voltage waveforms for a Type A LED lamp.

*a) Capacitor charging state S1 ($t_1 \leq t < t_2$)*

Based on the Kirchhoff's laws, (3.1) and (3.2) can be obtained for the capacitor charging state S1.

$$i_{ac} = C_{dc}\frac{dv_{dc}}{dt} + \frac{v_{dc}}{R_{eq}} \tag{3.1}$$

$$v_{ac} = i_{ac}R_{in} + L_{in}\frac{di_{ac}}{dt} + v_{dc} \tag{3.2}$$

*b) Capacitor discharging state S2 ($t_2 \leq t < t_3$)*

By applying the Kirchhoff's laws to the circuit under capacitor discharging state S2, (3.3) and (3.4) can be obtained. By integrating (3.4) from the time interval, [$t_2$, $t_3$], (3.5) is obtained.

$$i_{ac} = 0 \tag{3.3}$$

$$\frac{v_{dc}}{R_{eq}} = -C_{dc}\frac{dv_{dc}}{dt} \tag{3.4}$$

$$\int_{t_2}^{t_3} v_{dc}\, dt = R_{eq}C_{dc}(v_{dc}(t_2) - v_{dc}(t_3)) \tag{3.5}$$

As the time period of the dc-link voltage equals T/2 (T is the period of mains supply), $v_{dc}(t_3)$ equals $v_{dc}(t_1)$. Hence, (3.5) is equivalent to (3.6).

$$\int_{t_2}^{t_3} v_{dc}\, dt = R_{eq}C_{dc}(v_{dc}(t_2) - v_{dc}(t_1)) \tag{3.6}$$

When capacitor $C_{dc}$ starts to discharge through resistor $R_{eq}$, the relationships among the capacitor voltage level $v_{dc}$, discharging time $t_{dis}$ and $R_{eq}C_{dc}$ value are illustrated in Figure 3.24, according to (3.7).

$$\frac{v_{dc}}{v_{dc}(t_2)} = e^{-t_{dis}/(R_{eq}C_{dc})} \tag{3.7}$$

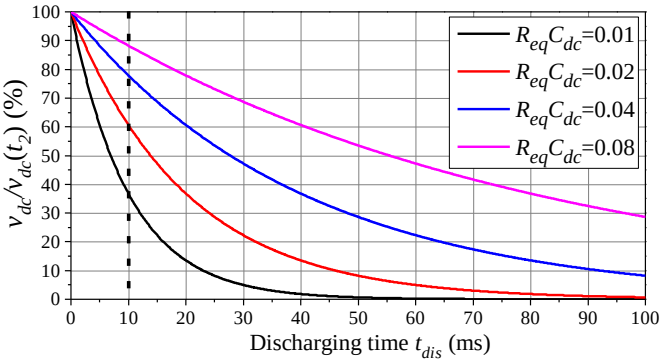



**Figure 3.24:** The relationships among the capacitor voltage level $v_{dc}$, discharging time $t_{dis}$ and $R_{eq}C_{dc}$ value.

As each discharging duration is less than 10 ms, the discharging curve can be approximately treated as linear curve (as illustrated in Figure 3.24), suggesting that (3.6) can be further simplified as (3.8).

$$R_{eq}C_{dc} = \frac{(v_{dc}(t_1)+v_{dc}(t_2))(t_1-t_2+T/2)}{2(v_{dc}(t_2)-v_{dc}(t_1))} \tag{3.8}$$

As time $t_1$ and $t_3$ are the transition points between the charging and discharging of capacitor, $v_{dc}(t_1)$ and $v_{dc}(t_2)$ are equal to $v_{ac}(t_1)$ and $v_{ac}(t_2)$ respectively, and hence, equation (3.8) can be replaced by equation (3.9), based on which, $R_{eq}C_{dc}$ can be directly obtained from the input ac voltage and current waveforms.

$$R_{eq}C_{dc} = \frac{(v_{ac}(t_1)+v_{ac}(t_2))(t_1-t_2+T/2)}{2(v_{ac}(t_2)-v_{ac}(t_1))} \quad (3.9)$$

For the charging state S1, integrating (3.1) from the time interval, [$t_1$, $t_2$], will obtain (3.10). By substituting (3.9) into (3.10), (3.11) is obtained. In addition, by integrating (3.2) from the time interval, [$t_1$, $t_2$], (3.12) will be obtained. Adding (3.11) and (3.12) together will obtain (3.13).

$$R_{eq}\int_{t_1}^{t_2} i_{ac}dt = R_{eq}C_{dc}\big(v_{ac}(t_2) - v_{ac}(t_1)\big) + \int_{t_1}^{t_2} v_{dc}dt \quad (3.10)$$

$$R_{eq}\int_{t_1}^{t_2} i_{ac}dt = \big(v_{ac}(t_1) + v_{ac}(t_2)\big)(t_1 - t_2 + T/2) + \int_{t_1}^{t_2} v_{dc}dt \quad (3.11)$$

$$R_{in}\int_{t_1}^{t_2} i_{ac}dt = \int_{t_1}^{t_2} v_{ac}dt - \int_{t_1}^{t_2} v_{dc}dt \quad (3.12)$$

$$R_{in} + R_{eq} = \frac{(v_{ac}(t_1)+v_{ac}(t_2))\left(t_1-t_2+\frac{T}{2}\right)+\int_{t_1}^{t_2} v_{ac}dt}{\int_{t_1}^{t_2} i_{ac}dt} \quad (3.13)$$

It is noticed from (3.13) that ($R_{in}$+$R_{eq}$) can be easily obtained from the input ac voltage and current waveforms. In order to derive the mathematical expressions on inductor $L_{in}$, (3.2) is integrated from the time interval, [$t_{ip}$, $t_2$] ($t_{ip}$ is the time where the peak of $i_{ac}$ is reached), resulting in (3.14).

$$L_{in} = \frac{R_{in}\int_{t_{ip}}^{t_2} i_{ac}dt+\int_{t_{ip}}^{t_2} v_{dc}dt-\int_{t_{ip}}^{t_2} v_{ac}dt}{i_{ac}(t_{ip})} \approx \frac{R_{in}\int_{t_{ip}}^{t_2} i_{ac}dt+V_{dc}(t_2-t_{ip})-\int_{t_{ip}}^{t_2} v_{ac}dt}{i_{ac}(t_{ip})} \quad (3.14)$$

where $V_{dc}$ is the average dc-link voltage, which is estimated from (3.15).

$$V_{dc} \approx (v_{dc,max} + v_{dc,min})/2 \approx (v_{ac,max} + v_{ac}(t_1))/2 \quad (3.15)$$

In order to obtain the parameter values of $R_{in}$, $L_{in}$, $C_{dc}$ and $R_{eq}$ from (3.9), (3.13), and (3.14), an initial estimation of one of the four parameter values is required. By ignoring the little power losses due to $R_{in}$ and diode conduction, the initial value of $R_{eq}$ can be estimated from (3.16), with the initial values of $R_{in}$, $L_{in}$ and $C_{dc}$ obtained correspondingly from (3.9), (3.13) and (3.14).

$$R_{eq} = \frac{V_{dc}^2}{P_{dc}} \approx \frac{V_{dc}^2}{P_{ac}} \quad (3.16)$$

$R_{in}$ (or $R_{eq}$) is adjusted according to the difference ($i_{ac\_diff}$) between measured peak current and simulated peak current. Specifically, when $i_{ac\_diff}$ is positive, $R_{in}$ should be

reduced (corresponds to an increase of $R_{eq}$), and the $R_{in}$ should be increased if $i_{ac\_diff}$ is negative (corresponds to a decrease of $R_{eq}$). For each time $R_{in}$ is adjusted, $L_{in}$, $C_{dc}$ and $R_{eq}$ are updated correspondingly according to (3.9), (3.13) and (3.14). The flowchart for adjusting the circuit parameter values is given in Figure 3.25. Once the absolute value of $i_{ac\_diff}$ is less than 0.5% of the peak value of $i_{ac}$, or $R_{in}$ is below 1 **Ω**, the iteration process is ended, with the final set of parameter values provided.

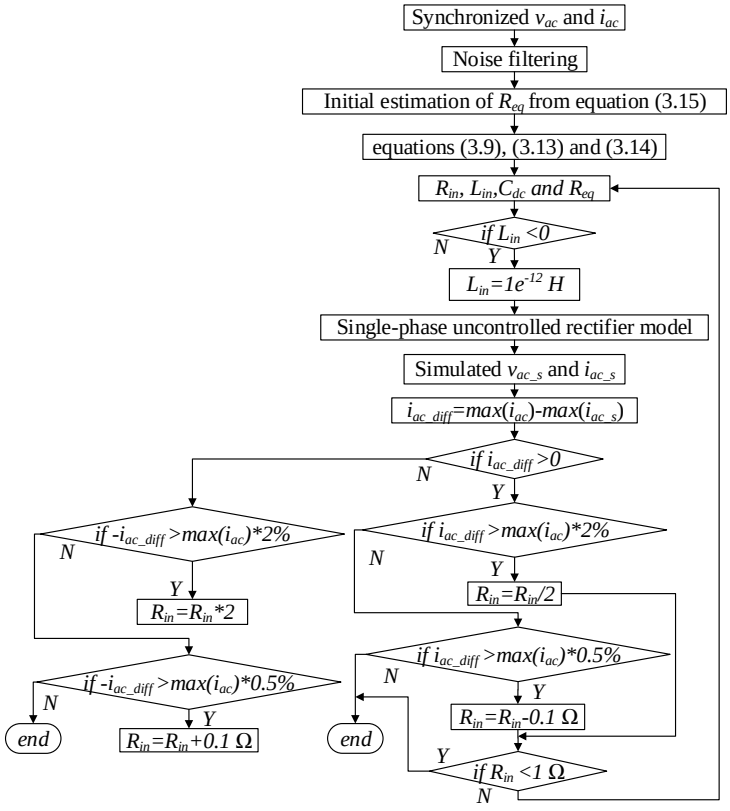



**Figure 3.25:** The flowchart for obtaining circuit parameter values for Type A LED lamps.

After the circuit parameter values have been obtained from synchronised input ac voltage and current waveforms under ideal supply condition, the next step is to obtain $R_{eq}$ values at different supply voltage magnitudes in order to take into account the voltage dependency of the circuit. The process for adjusting $R_{eq}$ at different supply voltage magnitudes is rather straightforward, and is illustrated by the flowchart given in Figure 3.26, for which the adjusting criteria is the input active power difference ($P_{ac\_diff}$) between the measurement ($P_{ac\_mea}$) and the simulation results ($P_{ac\_sim}$). Once $P_{ac\_diff}$ is less than 1% of $P_{ac\_mea}$, the iteration process is ended.

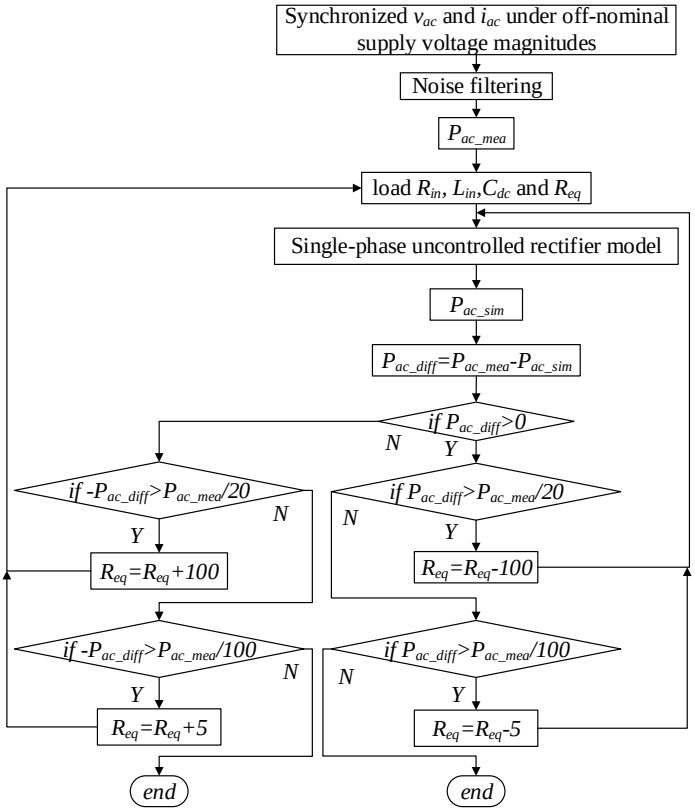



**Figure 3.26:** The flowchart for obtaining $R_{eq}$ under off-nominal voltage magnitudes.

By applying the flowcharts in Figure 3.25 and Figure 3.26 to the measured input ac voltage and current waveforms of Type A LED lamps (LED1-11) tested under sinusoidal supply voltage with different voltage magnitudes, their model parameter values (corresponds to Figure 3.22(a)) can be easily obtained, and are tabulated in Table 3.3. For the type A circuit based model, the relationship between $R_{eq}$ and $V_{ac}$ can be achieved through proper curve fitting based on the obtained values in Table 3.3, and the change of $R_{eq}$ with respect to $V_{ac}$ can be modelled as a controllable current source in Matlab/Simulink.

**Table 3.3:** The main circuit parameter values of the model in Figure 3.22(a).

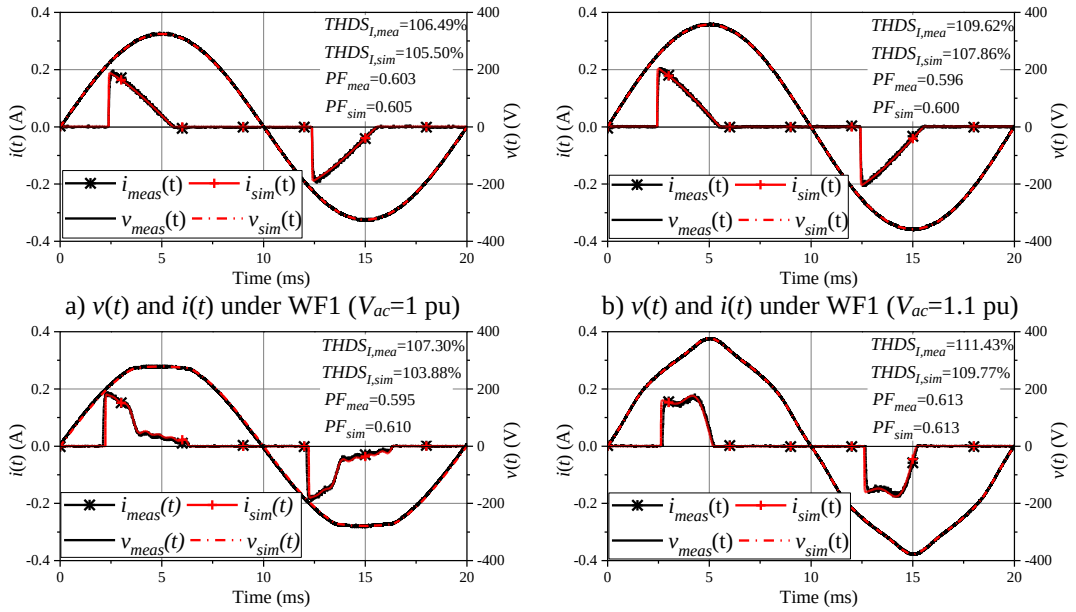
| LED No. | $R_{in}$ (Ω) | $L_{in}$ (H) | $C_{dc}$ (μF) | $R_{eq}$ (Ω) | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | $V_{ac\text{-}0.9pu}$ | $V_{ac\text{-}0.95pu}$ | $V_{ac\text{-}1pu}$ | $V_{ac\text{-}1.05pu}$ | $V_{ac\text{-}1.1pu}$ |
| **1** | 9.389 | $1e^{-12}$ | 4.23 | 29709.46 | 33544.4 | 36234.4 | 39794.4 | 43054.4 |
| **2** | 2 | $1e^{-12}$ | 2.17 | 14189.85 | 16029.8 | 17689.8 | 19649.8 | 21839.8 |
| **3** | 2 | $1e^{-12}$ | 2.90 | 11939.45 | 13509.4 | 14959.4 | 16464.4 | 18229.4 |
| **4** | 2 | $1e^{-12}$ | 3.02 | 9475.335 | 10815.3 | 11875.3 | 13300.3 | 14640.3 |
| **5** | 15.02 | $1e^{-12}$ | 4.54 | 9723.287 | 10968.2 | 11883.2 | 13463.2 | 14953.2 |
| **6** | 2 | $3e^{-5}$ | 2.81 | 7241.748 | 8246.74 | 9291.74 | 10241.7 | 11416.7 |
| **7** | 4 | $1e^{-12}$ | 2.20 | 7801.27 | 8126.27 | 8391.27 | 8536.27 | 8861.27 |
| **8** | 12.86 | $1e^{-12}$ | 6.90 | 7461.66 | 8406.66 | 9171.66 | 10201.6 | 11246.6 |
| **9** | 5.564 | $1e^{-12}$ | 8.72 | 7051.657 | 7931.65 | 8686.65 | 9566.65 | 10501.6 |
| **10** | 1.046 | $1e^{-12}$ | 1.39 | 6816.552 | 7626.55 | 8356.55 | 9206.55 | 10121.5 |
| **11** | 13.54 | $1e^{-12}$ | 7.05 | 5657.309 | 6387.30 | 7052.30 | 7772.30 | 8602.30 |

As the efficiency of the full-wave rectifier based circuit is high (the power losses are mainly due to $R_{in}$ and the conduction losses of diodes), the voltage dependency of active and reactive power for the model circuit is determined by the voltage dependency of the power consumption on $R_{eq}$. It is observed from Figure 3.18 that LED1-6 and LED8-9 are constant power load and LED7 is constant current load. Therefore, an alternative way to represent the dc power consumption of the model is to replace $R_{eq}$ in Table 3.3 as constant power load (for LED1-6 and LED8-9) or constant current load (for LED7), with the dc active power ($P_{dc\text{-}eq}$) or current values ($I_{dc\text{-}eq}$) listed in Table 3.4. The constant dc output power or the constant dc output current is implemented in the model through the controllable current source.

**Table 3.4:** Equivalent dc constant power or constant current for the model.

| LED No. | $P_{dc\text{-}eq}$ (W) | $I_{dc\text{-}eq}$ (A) |
|---|---|---|
| LED1 | 2.75 | / |
| LED2 | 4.95 | / |
| LED3 | 5.999 | / |
| LED4 | 7.32 | / |
| LED5 | 7.58 | / |
| LED6 | 8.98 | / |
| LED7 | / | 0.0335 |
| LED8 | 10.1 | / |
| LED9 | 10.92 | / |
| LED10 | 11.75 | / |
| LED11 | 12.893 | / |

To validate the accuracy of developed models, both time-domain current waveforms and calculated indices (including $P$, $Q_1$, $PF$, $PF_1$, $PF_d$ and $THDS_I$) are compared between simulation and measurement for Type A LED lamps tested under different supply conditions. To save space, the time-domain current waveform comparison between simulation and measurement is demonstrated on LED7 under different supply conditions, with the comparison results shown in Figure 3.27. In terms of the comparison of calculated indices, the differences between simulation and measurement are represented as percentage of indices calculated from measurement, with the minimum and maximum percentage differences for LED1-11 tested under a combination of different input voltage waveforms (WF1-3) and different input voltage magnitudes (0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u.), tabulated in Table 3.5. It is observed from Figure 3.27 and Table 3.5 that the proposed generalised model with the parameter values in Table 3.3 and Table 3.4 can well represent the electrical characteristics of Type A LED lamps (LED1-11). Regarding the deviation of indices between simulation and measurement, the maximum percentage difference is within 5% for all indices except the *%P* for LED12 which is slightly higher than 5%.




a) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1 pu)

b) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1.1 pu)

c) $v(t)$ and $i(t)$ under WF2 ($V_{ac}$=0.9 pu)

d) $v(t)$ and $i(t)$ under WF3 ($V_{ac}$=1.1 pu)

**Figure 3.27:** Comparison between measured and simulated voltage and current waveforms for LED7 under different supply conditions.

**Table 3.5:** Minimum and maximum percentage difference between simulation and measurement for Type A LED lamps tested under different supply conditions.

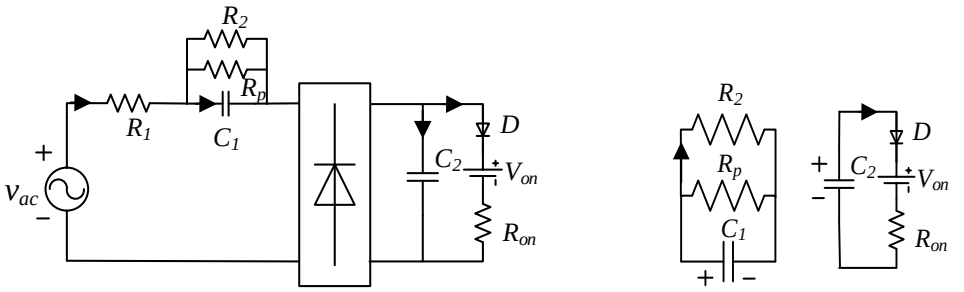
| No. | % $P$ | % $Q_1$ | % $PF$ | % $PF_1$ | % $PF_d$ | % $THDS_I$ |
|---|---|---|---|---|---|---|
| **1** | 0.49 | -1.54 | 0.66 | -0.48 | 0.21 | -0.44 |
| | 10.47 | 15.34 | 6.98 | -2.12 | 8.87 | -14.71 |
| **2** | 0.85 | 0.86 | 0.13 | 0.00 | -0.36 | 0.05 |
| | 10.25 | 25.75 | 1.88 | 2.24 | 1.70 | -3.18 |
| **3** | -0.25 | -0.50 | 0.07 | -0.09 | 0.60 | 0.11 |
| | 10.70 | 29.89 | -1.40 | 1.98 | 1.52 | -3.27 |
| **4** | 0.45 | -0.60 | -0.01 | -0.09 | 0.19 | -1.38 |
| | 12.01 | 35.18 | 3.53 | 2.02 | 4.68 | -7.36 |
| **5** | 0.84 | 0.05 | -1.68 | 0.07 | -1.29 | 1.23 |
| | 11.94 | 29.02 | -3.05 | 1.43 | -3.77 | 4.58 |
| **6** | -0.64 | -0.70 | 2.34 | -0.09 | 2.86 | -5.99 |
| | 9.36 | 34.53 | 7.30 | 2.63 | 5.94 | -9.56 |
| **7** | -0.46 | 0.48 | 0.01 | 0.02 | 0.04 | -0.21 |
| | 3.00 | 9.03 | 2.83 | 1.30 | 1.68 | -4.07 |
| **8** | 0.85 | -1.55 | -0.11 | 0.04 | 0.00 | -0.41 |
| | 10.51 | 31.37 | -1.37 | 1.13 | -1.41 | 1.79 |
| **9** | 0.49 | 0.86 | 0.03 | -0.03 | 0.10 | -0.13 |
| | 12.29 | 30.79 | 4.16 | 1.35 | 3.88 | -5.04 |
| **10** | 0.40 | 0.93 | 0.22 | -0.13 | 0.35 | -0.68 |
| | 12.49 | 34.78 | 6.88 | 0.87 | 6.25 | -8.46 |
| **11** | 0.11 | 0.45 | 0.04 | -0.04 | -0.22 | 0.12 |
| | 10.63 | 28.76 | 1.03 | 1.39 | 1.47 | -2.17 |

### 3.4.2 Type B LED lamps

The CBM developed for Type B LED lamps is illustrated in Figure 3.28(a), consisting of resistors $R_1$, $R_2$, $R_p$ and $R_{on}$, capacitors $C_1$, $C_2$, a full wave rectifier, ideal diode $D$ and constant dc voltage source $V_{on}$. As stated in Section 3.2.1, resistor $R_1$ is for limiting the high inrush current when the lamp is turned up while resistor $R_2$ is used to discharge capacitor $C_1$ when the lamp is turned off. The scaling-down of mains supply voltage is achieved by capacitor $C_1$ with its parallel parasitic resistance $R_p$ which has an impact on the zero crossing position of input current $i_{ac}$ at time $t_2$. Specifically, when $R_p$ is infinite large, $t_2$ is when the peak of supply voltage waveform $v_{ac}$ achieved, while smaller $R_p$ makes $i_{ac}(t_2)$ slightly shift to the left with respect to the position where the peak of $v_{ac}$ is located (i.e. the discharging of $C_1$ starts before $v_{ac}$ reaches its peak value). The LED string is modelled as an ideal diode $D$, with constant dc voltage source $V_{on}$ and LED intrinsic resistance $R_{on}$ connected in series.

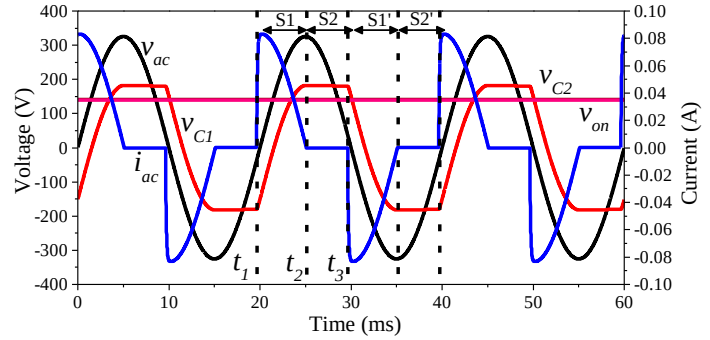
As shown in Figure 3.28, the circuit has two working states: the capacitor $C_1$ charging state S1 and the capacitor $C_1$ discharging state S2, which can be reflected from the relationships among input ac voltage and current waveforms, dc link voltage waveform illustrated in Figure 3.29. During the capacitor $C_1$ charging state ($t_1 \leqslant t < t_2$), capacitor $C_1$ gets charged and the current fed to LED string is from the mains supply, while during the capacitor $C_1$ discharging state ($t_1 \leqslant t < t_2$), capacitor $C_1$ gets discharged across the paralleled connected resistor $R_2$ which is typically around 470 kΩ.

The charging and discharging duration of capacitor $C_2$ is determined by its size with respect to capacitor $C_1$. Specifically, if capacitor $C_2$ is relatively small (e.g. close to $C_1$), its charging and discharging will be completed in the state S1 only and no current will be fed to the LED string during state S2, while for relatively large $C_2$ (e.g. $1000 \times C_1$), the discharging of capacitor $C_2$ will extend to state S2, and the current fed to the LED array will be continuous. At time $t_3$ when the input voltage becomes negative, capacitor $C_1$ charges in an opposite direction as opposed to time $t_1$ and its voltage starts to decrease. It is noticed from Figure 3.28 and Figure 3.29 that the two working modes of the circuit are well reflected from the input current waveform shape, implying the possibility of estimating circuit parameter meter values from the input voltage and current waveforms. Therefore, the next step is to establish the mathematical relationships among circuit parameters, and the input voltage and current waveforms, with the derivation process fully discussed in the following.

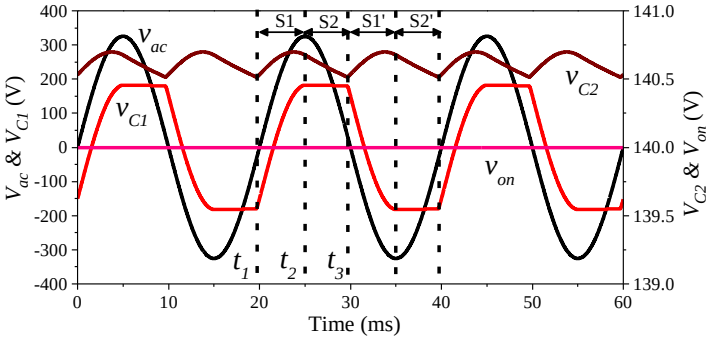



a) S1 (Capacitor C1 charging) b) S2 (Capacitor C1 discharging)

**Figure 3.28:** The two working states for the generalised circuit model of Type B LED driver.




a) input ac voltage and current, and dc-link voltage




b) zooming-part

**Figure 3.29:** The input ac side voltage and current waveforms and dc-link voltage waveforms for a Type B LED lamp.

By applying the Kirchhoff's laws to the circuit under capacitor charging state S1 ($t_1 \leqslant t < t_2$), (3.17) and (3.18) are obtained. As the current flowing through resistor $R_2$ is much smaller than the current flowing through capacitor $C_1$, (3.18) can be simplified as (3.19). Integrating (3.17) and (3.18) from the time interval, [$t_1$, $t_2$], will obtain (3.20) and (3.21) respectively.

$$i_{ac} = i_{dc} + i_{LED} \approx i_{C1} = C_1 \frac{dv_{C1}}{dt} \tag{3.17}$$

$$v_{ac} = i_{ac}R_1 + v_{C1} + v_{C2} \approx i_{ac}R_1 + \frac{1}{C_1}\int i_{ac}\,dt + v_{on} \tag{3.18}$$

$$v_{ac} = i_{ac}R_1 + v_{C1} + v_{C2} \approx i_{ac}R_1 + \frac{1}{C_1}\int i_{C1}\,dt + v_{on} \tag{3.19}$$

$$C_1 \approx \frac{\int_{t_1}^{t_2} i_{ac}dt}{v_{C_1}(t_2) - v_{C_1}(t_1)} \approx \frac{\int_{t_1}^{t_2} i_{ac}dt}{2v_{C_1}(t_2)} \approx \frac{\int_{t_1}^{t_2} i_{ac}dt}{2(v_{ac,max} - V_{on})} \tag{3.20}$$

$$V_{on} \approx \left(\int_{t_1}^{t_2} v_{ac}\,dt - R_1 \int_{t_1}^{t_2} i_{ac}\,dt\right)/(t_2 - t_1) \tag{3.21}$$

For the other circuit parameters including $R_1$, $C_2$, $R_p$, $R_{on}$, as their impact on the input current waveform shape is less apparent than the impact of $C_1$ and $V_{on}$ on the input ac

current, the initial estimation of those parameters is: $R_1$ equals 20 Ω, $R_p$ equals 9 kΩ, while $C_2$ and $R_{on}$ are obtained from (3.22) and (3.23) respectively.

$$C_2 = 10C_1 \tag{3.22}$$

$$R_{on} = \frac{nR_{LED}}{m} = \frac{V_{on}R_{LED}}{mV_{LED}} \tag{3.23}$$

where: m is the number of strings in the LED array (m is assumed to be 1); n is the number of LED chips in each string; $R_{LED}$ and $V_{LED}$ are the series intrinsic resistance and the conduction voltage of a single LED diode respectively (assumed to be 0.77 Ω and 3.04 V respectively in the model).

The flowchart for adjusting the circuit parameter values is given in Figure 3.30. The parameter adjustment process is divided into two stages, where the first stage is adjusting $V_{on}$ based on the *THD* difference ($THD_{iac\_diff}$) between measured and simulated input current waveforms ($THD_{iac\_mea}$ and $THD_{iac\_sim}$ respectively), and the second stage is adjusting $C_1$ according to the rms value difference ($I_{iac\_diff}$) between measured and simulated input current ($I_{iac\_mea}$ and $I_{iac\_sim}$ respectively). Specifically, $V_{on}$ will be increased if $THD_{iac\_diff}$ is positive and will be decreased if $THD_{iac\_diff}$ is negative, while $C_1$ will be increased if $I_{iac\_diff}$ is positive and will be decreased if $I_{iac\_diff}$ is negative. Once the absolute value of $THD_{iac\_diff}$ is less than 1% of $THD_{iac\_mea}$ and the absolute value of $I_{iac\_diff}$ is less than 1% of $I_{iac\_mea}$, the iteration process is ended, with the final set of parameter values provided. In order to further improve the matching between simulated and measured input current waveforms, parameter values of $R_1$, $P_p$ and $C_2$ can be further slightly adjusted according to their insignificant impacts on the input current waveform shape. By applying the flowchart in Figure 3.30 to the measured voltage and current waveforms of LED12-17 tested under sinusoidal supply voltage with different voltage magnitudes, their component-based model parameter values (corresponds to Figure 3.28(a)) can be easily obtained, and are tabulated in Table 3.6. As the model with parameter values in Table 3.3 can well represent the simulated current waveforms under other supply voltage magnitudes, there is no need to adjust the dc-side power consumption (i.e. $V_{on}$ and $R_{on}$ for the LED array) under different supply voltage magnitudes as did for Type A LED lamps.

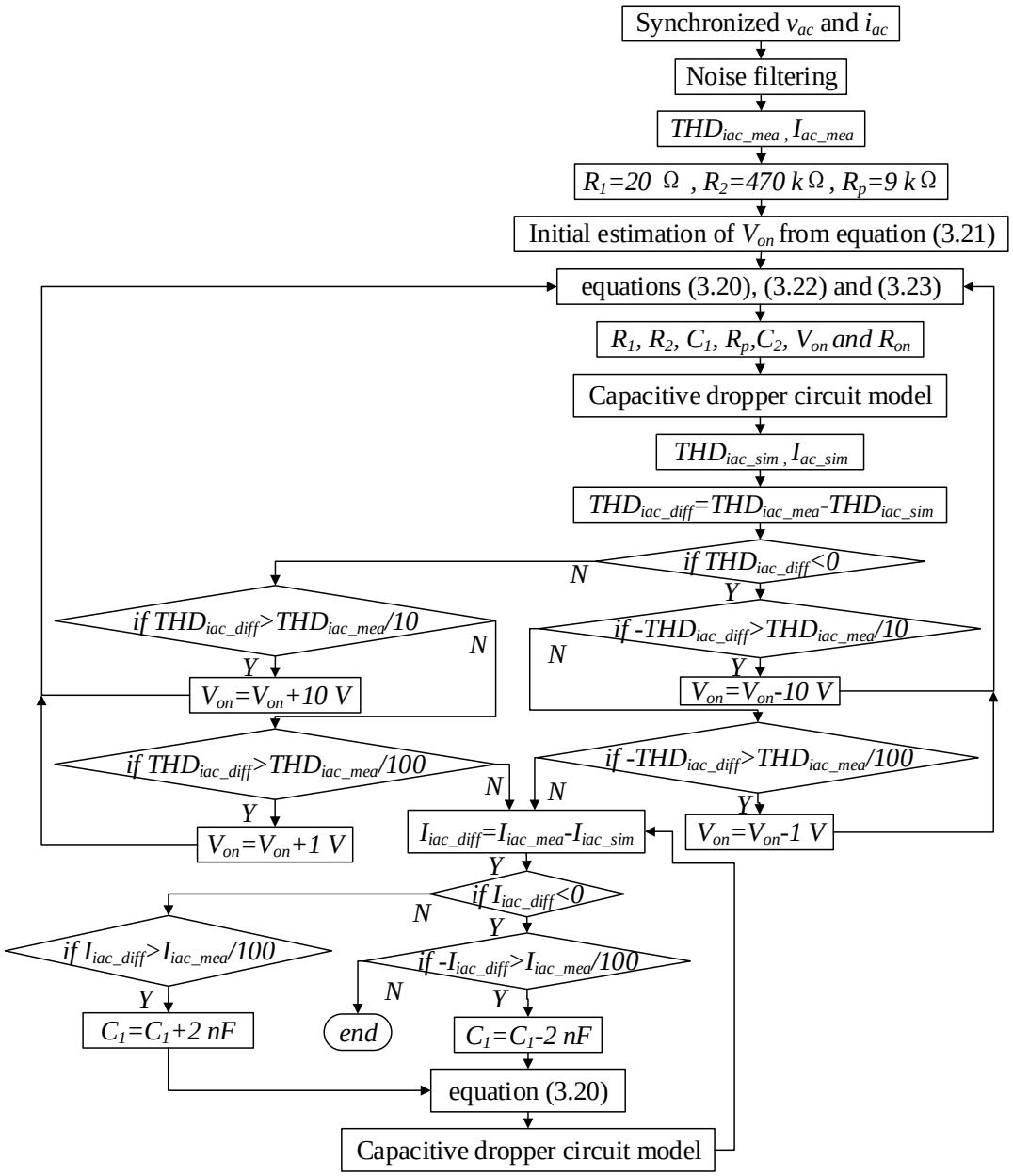
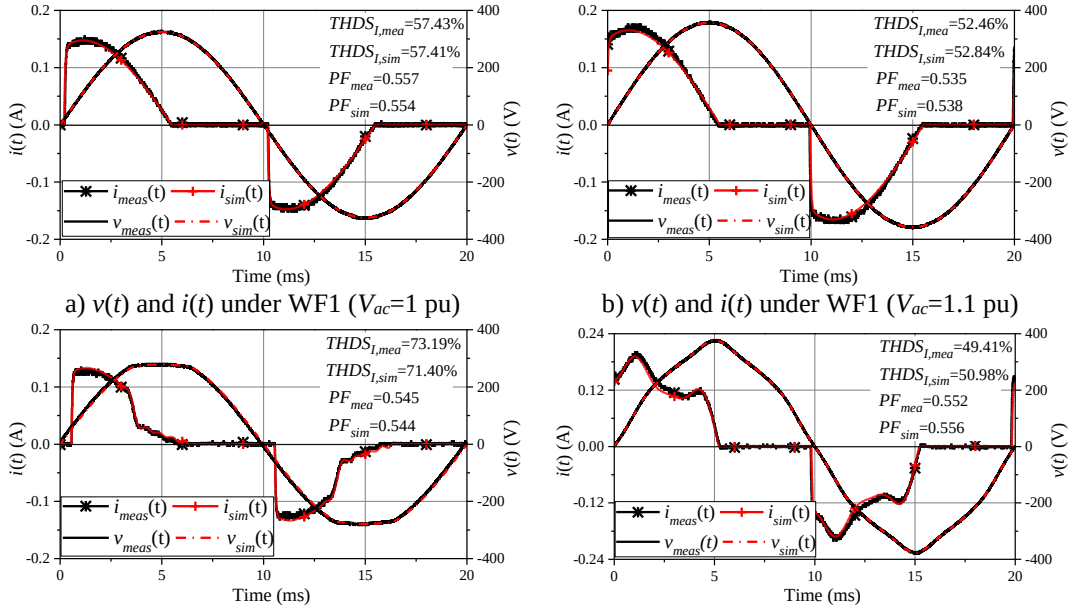



**Figure 3.30:** The flowchart for obtaining circuit parameter values from measured input voltage and current waveforms.

**Table 3.6:** The main circuit parameter values of the model in Figure 3.28(a).

| No. | $R_1$ (Ω) | $R_2$ (kΩ) | $C_1$ (µF) | $C_2$ (µF) | $V_{on}$ (V) | $R_{on}$ (Ω) | $R_p$ (kΩ) |
|---|---|---|---|---|---|---|---|
| **12** | 20 | 470 | 0.841 | 100 | 121.65 | 30.81 | $1e^7$ |
| **13** | 10 | 470 | 1.76 | 50 | 188.82 | 47.83 | 10 |
| **14** | 30 | 470 | 1.63 | 16.3 | 145.97 | 36.97 | 9 |
| **15** | 20 | 470 | 2.92 | 29.2 | 105.52 | 26.73 | 9 |
| **16** | 20 | 470 | 3.14 | 20 | 123.68 | 31.33 | 9 |
| **17** | 22 | 470 | 3.82 | 30 | 167.20 | 42.35 | 4 |

To validate the accuracy of developed models, both time-domain current waveforms and calculated indices (including $P$, $Q_1$, $PF$, $PF_1$, $PF_d$ and $THDS_I$) are compared between simulation and measurement for LED lamps tested under different supply conditions. To save space, the time-domain current waveform comparison between simulation and measurement is demonstrated on LED14 under different supply conditions, with the comparison results shown in Figure 3.31. Regarding the comparison of calculated indices, The minimum and maximum percentage differences of indices calculated for Type B LED lamps under a combination of different input voltage waveforms (WF1-3) and different input voltage magnitudes (0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u.), are tabulated in Table 3.7. It is observed from Figure 3.31 and Table 3.7 that the proposed generalised model with the parameter values in Table 3.6 can well represent the electrical characteristics of Type B LED lamps. For the deviation of indices between simulation and measurement, the maximum percentage difference is within 5% for all indices except the $\%P$ for LED12 which is slightly higher than 5%.




a) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1 pu)

b) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1.1 pu)

c) $v(t)$ and $i(t)$ under WF2 ($V_{ac}$=0.9 pu)

d) $v(t)$ and $i(t)$ under WF3 ($V_{ac}$=1.1 pu)

**Figure 3.31:** Comparison between measured and simulated voltage and current waveforms for LED14 under different supply conditions.

**Table 3.7:** Minimum and maximum percentage difference between simulation and measurement for Type B LED lamps tested under different supply conditions.

| No. | % $P$ | % $Q_1$ | % $PF$ | % $PF_1$ | % $PF_d$ | % $THDS_I$ |
|---|---|---|---|---|---|---|
| **12** | -2.42 | 0.03 | -0.86 | -0.71 | -0.01 | 1.20 |
| | -5.26 | -2.54 | -4.54 | -4.38 | -0.85 | 4.32 |
| **13** | -0.17 | -1.54 | -0.11 | 0.19 | -0.51 | 1.52 |
| | -1.28 | -3.00 | -1.11 | 1.01 | -1.95 | 4.23 |
| **14** | -0.02 | 0.19 | -0.04 | -0.01 | -0.03 | -0.04 |
| | 3.27 | 5.61 | 1.88 | -1.83 | 0.89 | 3.18 |
| **15** | 0.13 | 0.36 | 0.28 | 0.35 | -0.06 | 0.17 |
| | 1.96 | -2.34 | 3.00 | 3.17 | -0.16 | 1.46 |
| **16** | -1.27 | 0.19 | -0.55 | -0.57 | 0.01 | -0.07 |
| | -3.55 | 2.86 | -2.67 | -3.00 | 0.34 | -0.90 |
| **17** | 0.05 | -0.07 | 0.04 | 0.00 | -0.02 | 0.03 |
| | -3.53 | 4.64 | 1.03 | -1.18 | 1.04 | -2.52 |

### 3.4.3 Type C LED lamps

For Type C LED lamps, their current waveform shape is mainly determined by the voltage dependency of CCR circuit which are represented by a voltage controlled current source in Matlab/Simulink as illustrated in Figure 3.32. As shown in Figure 3.32, the model is rather simple, consisting of a full-wave rectifier, a voltage controlled current source, an ideal diode and a constant dc voltage source (the voltage drop across $R_{on}$ is included in the voltage controlled current source and hence, $R_{on}$ is not included in the model). According to the input current waveform shape illustrated in Figure 3.33, the operation of the circuit can be divided into three states: for the pre-conduction state S1 ($t_1 \leqslant t < t_2$), $v_{ac}$ is smaller than $V_{on}$ and hence the circuit is not conducted; for the conduction and pre-regulation state S2 ($t_2 \leqslant t < t_3$), a linear relationship can be assumed between $i_{ac}$ and $v_{ac}$; for the regulation state S3 ($t_3 \leqslant t < t_4$), $i_{ac}$ is almost constant due to the current regulation of CCR.

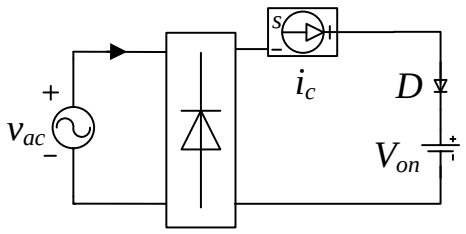



**Figure 3.32:** The generalized circuit model of Type C LED driver.

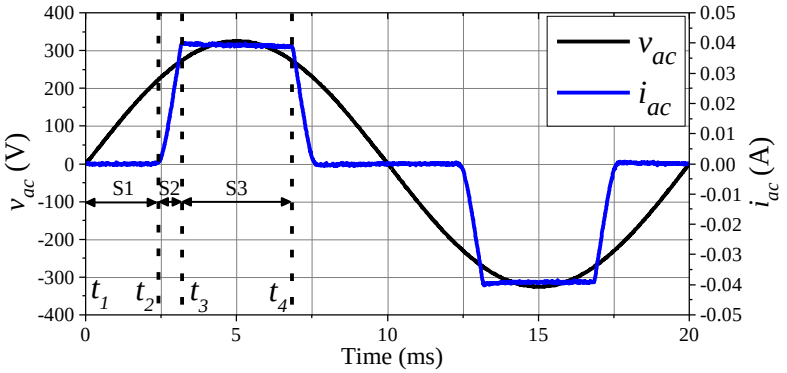



**Figure 3.33:** The input voltage and current waveforms for a Type C LED lamp.

To obtain the circuit parameter values ($i_c$ and $V_{on}$), (3.24) to (3.30) are applied to measured input voltage and current of LED18-19 tested under ideal supply condition, without any iterations required. By applying (3.24) to (3.30) to the measured input voltage and current for LED18-19 tested under ideal supply condition, the obtained circuit parameter parameters are tabulated in Table 3.8. As the model with parameter values in Table 3.8 can well represent the simulated current waveforms under other supply voltage magnitudes, there is no need to adjust the dc-side power consumption (i.e. $V_{on}$ for the LED array) under different supply voltage magnitudes as did for Type A LED lamps.

$$V_{on} = v_{ac}(t_2) \tag{3.24}$$

$$V_{th} = v_{ac}(t_3) \tag{3.25}$$

$$I_{req} = mean(i_{ac}(t_3 : t_4)) \tag{3.26}$$

$$R_{eq} = (V_{th} - V_{on})/I_c \tag{3.27}$$

$$i_{c,t1\sim t2} = 0 \tag{3.28}$$

$$i_{c,t2\sim t3} = (V_{rec} - V_{on})/R_{eq} \tag{3.29}$$

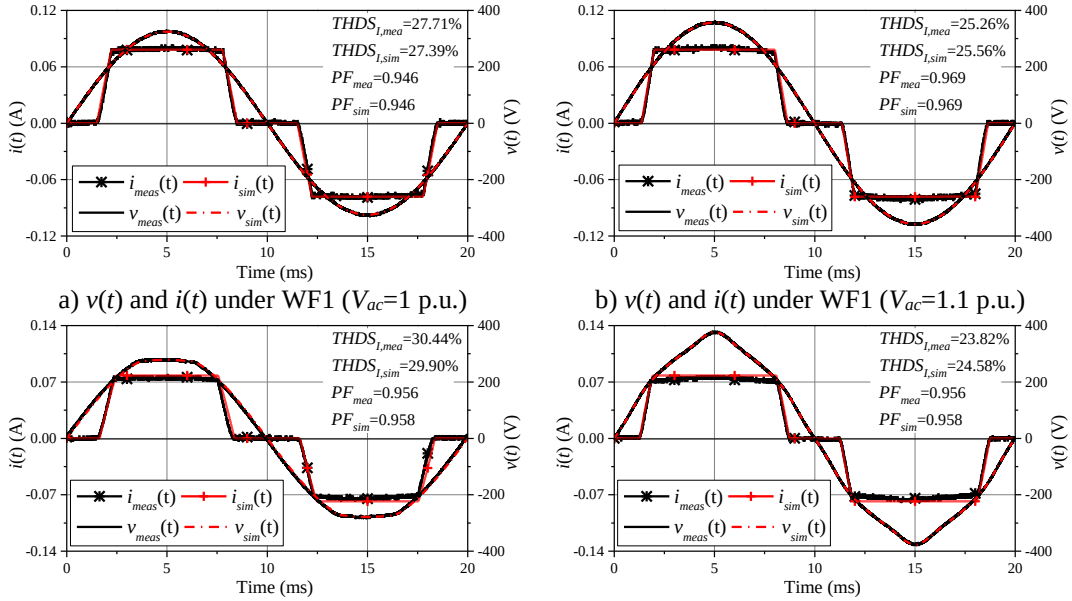
$$i_{c,t3\sim t4} = I_{req} \tag{3.30}$$

where: $V_{on}$ is the conduction voltage of the LED array; $V_{th}$ is the threshold voltage of the CCR regulation state S3; $I_{req}$ is the regulated current value; $R_{eq}$ is the equivalent resistance for the conduction and pre-regulation state S2; $i_{c,t1\sim t2}$, $i_c$,$t_{2\sim t3}$ and $i_{c,t3\sim t4}$ are the input ac current at state S1, S2 and S3 respectively.

**Table 3.8:** The main circuit parameter values of the model in Figure 3.32.

| LED No. | $V_{on}$ (V) | $R_{eq}$ (Ω) | $I_{req}$ (mA) | $V_{th}$ (V) |
|---|---|---|---|---|
| **18** | 221.19 | 1346.89 | 39.29 | 274.11 |
| **19** | 147.86 | 788.88 | 78.16 | 209.53 |

To validate the accuracy of developed model, both time-domain current waveforms and calculated indices are compared between simulation and measurement for Type C LED lamps tested under different supply conditions. The time-domain current waveform comparison between simulation and measurement is demonstrated on LED19, with the comparison results shown in Figure 3.34. Regarding the comparison of calculated indices, the minimum and maximum percentage differences for Type C LED lamps tested a combination of different input voltage waveforms (WF1-3) and different input voltage magnitudes (0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u.), are tabulated in Table 3.9. It is observed from Figure 3.34 and Table 3.9 that the proposed simple model with the parameter values in Table 3.9 can well represent the electrical characteristics of Type C LED lamps (the big percentage difference for $Q_1$ is not an issue due to the small absolute value of $Q_1$ and the near unity $PF_1$).




a) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1 p.u.)

b) $v(t)$ and $i(t)$ under WF1 ($V_{ac}$=1.1 p.u.)

c) $v(t)$ and $i(t)$ under WF2 ($V_{ac}$=0.9 p.u.)

d) $v(t)$ and $i(t)$ under WF3 ($V_{ac}$=1.1 p.u.)

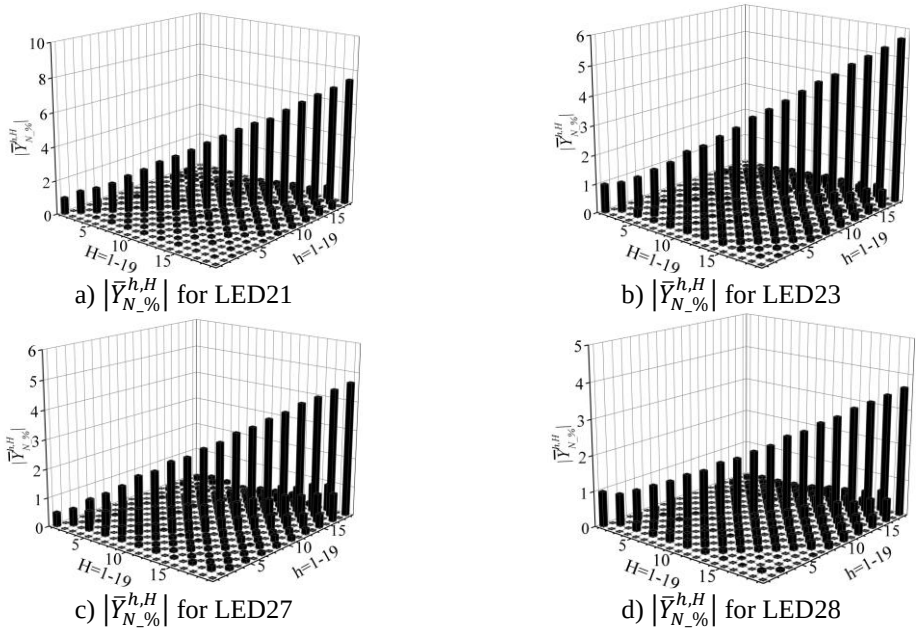
**Figure 3.34:** Comparison between measured and simulated voltage and current waveforms for LED19 under different supply conditions.

**Table 3.9:** Minimum and maximum percentage difference between simulation and measurement for Type C LED lamps tested under different supply conditions.

| No. | *% P* | *% $Q_1$* | *% PF* | *% $PF_1$* | *% $PF_d$* | *% $THDS_I$* |
|---|---|---|---|---|---|---|
| **18** | 1.01 | -58.76 | 0.96 | 0.00 | 0.96 | -5.55 |
| | 5.18 | -150.62 | 3.29 | 0.00 | 3.29 | -8.54 |
| **19** | -0.12 | -94.01 | 0.03 | 0.00 | 0.03 | 0.00 |
| | 7.65 | -97.76 | 0.28 | 0.00 | 0.28 | 3.19 |

## 3.4.4 Type D LED lamps

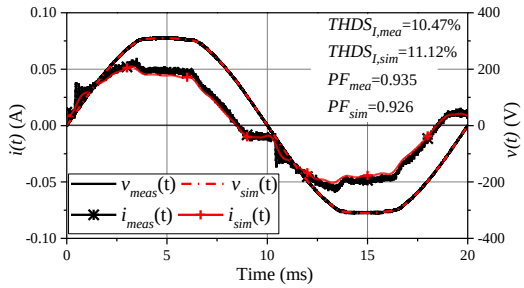
As Type D LED lamps are based on switched-mode driver circuits which are high in circuit diversity, building a generalised circuit model for them is infeasible, and hence frequency-domain modelling is applied, by using the development procedure of CHNMs given in Chapter 2. The obtained $HAM_{N\_\%}$ of Type D LED lamps is shown in Figure 3.35, by taking LED21, LED23, LED27 and LED28 for example. It turns out that diagonal elements are dominant in $HAM_{N\_\%}$, suggesting that the current harmonics of Type D LED lamps are mainly determined by voltage harmonics of the same order. In addition, the diagonal matrix elements magnitudes gradually increase with the increasing harmonic orders. The corresponding input current waveform and indices comparison between simulation and measurement are given in Figure 3.36 and Table 3.10, and both of them indicate that good model accuracy is achieved.



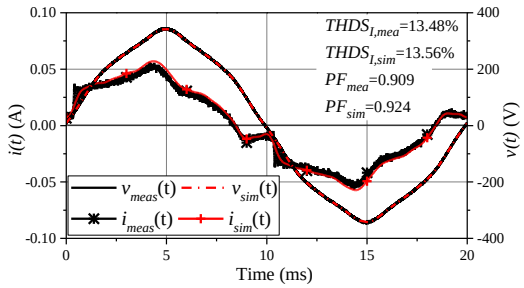

a) $|\bar{Y}_{N\_\%}^{h,H}|$ for LED21 b) $|\bar{Y}_{N\_\%}^{h,H}|$ for LED23

c) $|\bar{Y}_{N\_\%}^{h,H}|$ for LED27 d) $|\bar{Y}_{N\_\%}^{h,H}|$ for LED28

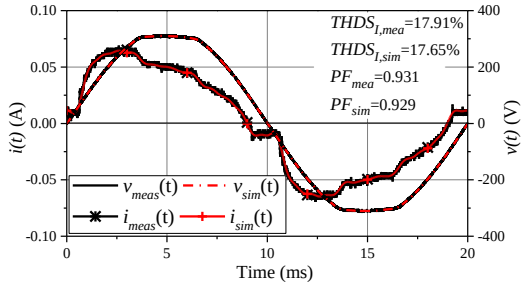
**Figure 3.35:** $|\bar{Y}_N|$ obtained from laboratory individual harmonic tests for LED21, LED23, LED27 and LED28.



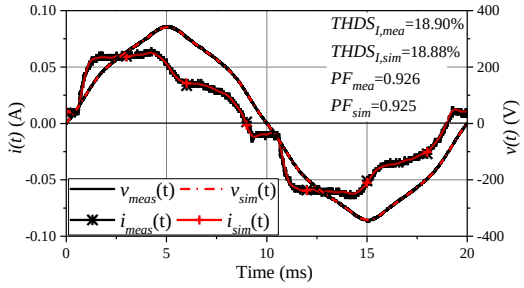

a) voltage and current waveform for LED21 under WF2, ZS2



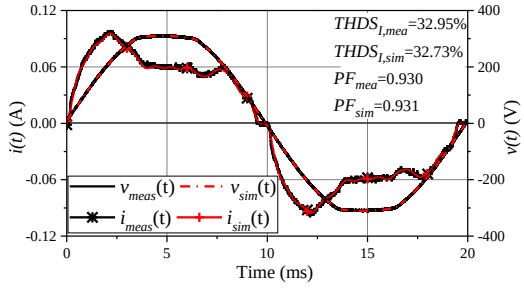

b) voltage and current waveform for LED21 under WF3, ZS2



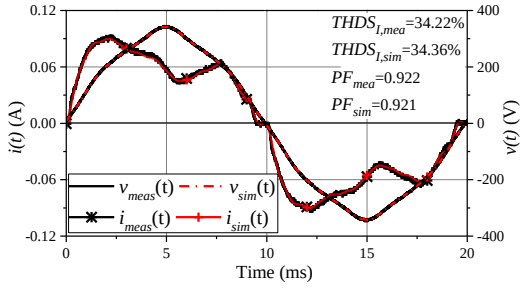

c) voltage and current waveform for LED23 under WF2, ZS2



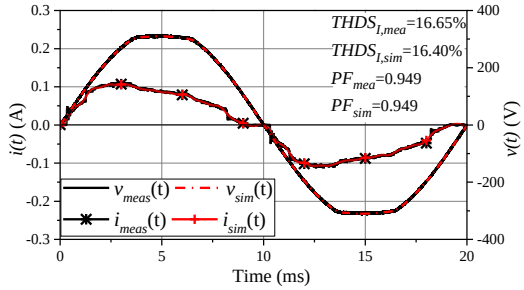

d) voltage and current waveform for LED23 under WF3, ZS2



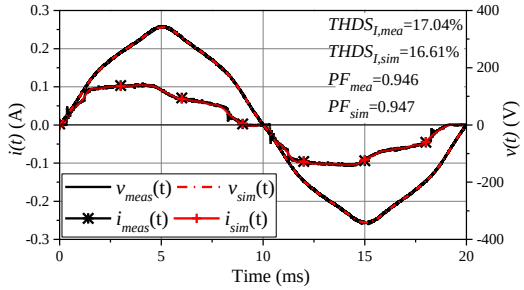

e) voltage and current waveform for LED27 under WF2, ZS2




f) voltage and current waveform for LED27 under WF3, ZS2




g) voltage and current waveform for LED28 under WF2, ZS2




h) voltage and current waveform for LED28 under WF2, ZS2

**Figure 3.36:** Comparison between measured and simulated grid-side current waveforms for LED21 operating under different supply conditions.

**Table 3.10:** Minimum and maximum percentage difference between simulation and measurement for Type D LED lamps tested under different supply conditions.

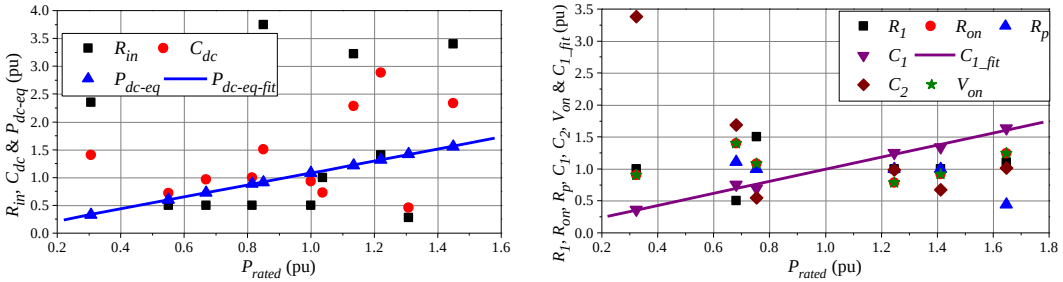
| No. | *% P* | *% $Q_1$* | *% PF* | *% $PF_1$* | *% $PF_d$* | *% $THDS_I$* |
|---|---|---|---|---|---|---|
| **21** | 0.00 | 0.00 | 0.49 | 0.00 | 0.34 | -0.06 |
| | 12.08 | 0.56 | 2.49 | 1.69 | 0.78 | 7.80 |
| **23** | 0.00 | 0.00 | 0.14 | 0.00 | 0.13 | -0.29 |
| | 1.27 | 0.57 | 0.54 | 0.17 | 0.37 | -2.31 |
| **27** | 0.00 | 0.00 | -0.06 | 0.00 | -0.05 | 0.98 |
| | -0.83 | 1.28 | -0.46 | -0.12 | -0.36 | 4.61 |
| **28** | 0.00 | 0.00 | 0.19 | 0.00 | 0.30 | -0.31 |
| | 1.05 | 3.08 | 0.42 | -0.14 | 0.44 | -4.57 |

### 3.4.5 Aggregate models of LED lamps

With the developed individual load models for all four types of LED lamps, the following step is to select appropriate model aggregation approach in order to investigate the cumulative impact of each type LED lamps on LV networks. In this section, the generic model for each type LED lamp will be developed first, which will be used for the development of aggregate model of the specific type of LED lamps. For Type A-C LED lamps with specified circuit topologies, their generic model can be obtained by evaluating the correlations between main circuit parameter values and $P_{rated}$. With the generic model developed for each Type LED lamps (Type A-C), their corresponding aggregate model can be easily derived. Unlike Type A-C LED lamps, the aggregation of Type D LED lamps should be done in frequency domain, due to their high circuit diversity. The frequency-domain aggregation will be fully analysed in Chapter 6 and hence not discussed here.

Specifically, based on the power ($P_{rated}$) dependency of circuit parameter values illustrated in Figure 3.37 and the corresponding (linear) correlation coefficients between the circuit parameter values and $P_{rated}$ for Type A-B LED lamps listed in Table 3.11, it turns out that only $P_{dc\text{-}eq}$ (for Type A) and $C_1$ (for Type B) have a linear dependency of $P_{rated}$ while no obvious correlations are observed between the other circuit parameter values and $P_{rated}$. As there are only two tested lamps within the Type C group, a linear fitting is applied between their circuit parameter values and the corresponding $P_{rated}$ values. The obtained linear fitting coefficients (in the form of $aP_{rated}+b$) for Type A-C LED lamps are tabulated in Table 3.12, where all the

parameter values are expressed in p.u. with respect to their median values of the specified group, as listed in Table 3.13. For the circuit parameter values which do not have linear dependency of $P_{rated}$ (i.e. those parameters which are not listed in Table 3.12), their corresponding median values of the specified group are used as the circuit parameter values for their generic model.




a) the $P_{rated}$ dependency circuit parameter values for Type A LED lamps

b) the $P_{rated}$ dependency circuit parameter values for Type B LED lamps

**Figure 3.37:** Comparison between measured and simulated grid-side current.

**Table 3.11:** The correlation coefficients between main circuit parameter values and $P_{rated}$ for Type A-B LED lamps.

| **Type A** | $R_{in}$ | $C_{dc}$ | $P_{dc-eq}$ | | | |
|---|---|---|---|---|---|---|
| | 0.17 | 0.39 | 1.00 | | | |
| **Type B** | $R_1$ | $C_1$ | $C_2$ | $V_{on}$ | $R_{on}$ | $R_p$ |
| | 0.12 | 1.00 | -0.70 | -0.03 | -0.03 | -0.67 |

**Table 3.12:** The linear fitting coefficients between circuit parameter values (p.u. values) and $P_{rated}$ (p.u.) for Type A-C LED lamps.

| **Type A** | | $P_{dc-eq}$ | **Type B** | | $C_1$ |
|---|---|---|---|---|---|
| | **a** | 1.076 | | **a** | 0.943 |
| | **b** | 0.004 | | **b** | 0.052 |
| **Type C** | | $V_{on}$ | $R_{eq}$ | $I_{req}$ | $V_{th}$ |
| | **a** | -0.444 | -0.584 | 0.739 | -0.298 |
| | **b** | 1.444 | 1.584 | 0.261 | 1.298 |

**Table 3.13:** The median circuit parameter values for Type A-C LED lamps.

| **Type A** | $P_{rated}$ (W) | $R_{in}$ (Ω) | $C_{dc}$ (µF) | $P_{dc-eq}$ (W) | | | |
|---|---|---|---|---|---|---|---|
| | 8.99 | 4.00 | 3.02 | 8.28 | | | |
| **Type B** | $P_{rated}$ (W) | $R_1$ (Ω) | $C_1$ (µF) | $C2$ (µF) | $V_{on}$ (V) | $R_{on}$ (Ω) | $R_p$ (Ω) |
| | 13.835 | 20.00 | 2.34 | 29.60 | 134.83 | 34.15 | 9 |
| **Type C** | $P_{rated}$ (W) | $V_{on}$ (V) | $R_{eq}$ (Ω) | $I_{req}$ (mA) | $V_{th}$ (V) | | |
| | 9.25 | 184.53 | 1067.90 | 58.73 | 241.82 | | |

Once the generic model is obtained, the aggregate model for each type LED lamps can be easily obtained. Specifically, the aggregate Type A LED lamps with their total aggregate active power on the ac side equalling $P_{rated,a}$, have its aggregate circuit parameter values given by (3.31-3.33). For example, the simulated current waveform of the aggregate model of 100 generic Type A LED lamp models with $P_{rated}$ of individual lamp equal to the median value in Table 3.13, is illustrated in Figure 3.38(a), which turns out to be the same with the sum of ac current waveforms of all the individual lamps, indicating the correctness of the provided aggregation approach.

$$R_{in,a} = R_{in,g}/P_{rated,a}(pu) \tag{3.31}$$

$$C_{dc,a} = C_{dc,g} \times P_{rated,a}(pu) \tag{3.32}$$

$$P_{dc-eq,a} = P_{dc-eq,g} \times P_{rated,a}(pu) \tag{3.33}$$

where: $P_{rated,a}$(pu) is the ac aggregate active power in per units with respect to the corresponding median value given in Table 3.13; $R_{in,a}$, $C_{dc,a}$ and $P_{dc\text{-}eq,a}$ are the aggregate model parameter values while $R_{in,g}$, $C_{dc,g}$ and $P_{dc\text{-}eq,g}$ are the generic model parameter values.

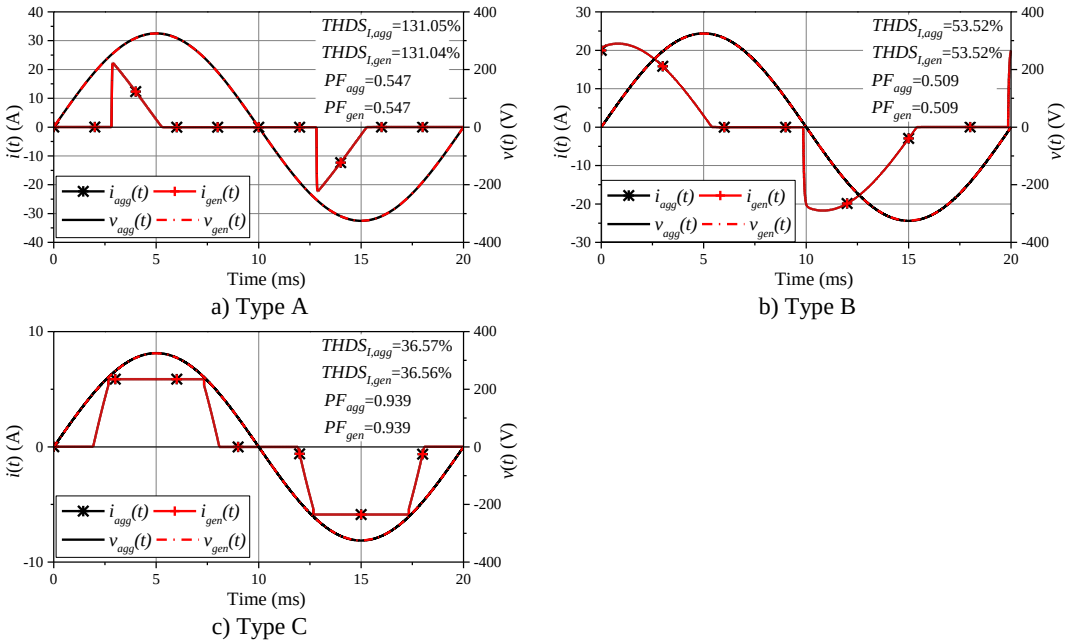



**Figure 3.38:** The comparison between current waveform of the aggregate model and the sum of current waveform of 100 individual generic models with $P_{rated}$ equal to the median value given in Table 3.8.

Similarly, for the aggregate load model of Type B LED lamps with total aggregate active power equalling $P_{rated,a}$, the relation between the aggregate and generic model parameter values are indicated in (3.34-3.40). Again, to demonstrate the correctness of the proposed aggregation approach, the simulated current waveform of the aggregate model of 100 generic Type B LED lamp models with $P_{rated}$ of individual lamp equal to the median value in Table 3.13, is illustrated in Figure 3.38(b), which turns out to be the same with the sum of ac current waveforms of all the individual lamps.

$$R_{1,a} = R_{1,g}/P_{rated,a}(pu) \tag{3.34}$$

$$R_{2,a} = R_{2,g}/P_{rated,a}(pu) \tag{3.35}$$

$$R_{p,a} = R_{p,g}/P_{rated,a}(pu) \tag{3.36}$$

$$C_{1,a} = C_{1,g} \times P_{rated,a}(pu) \tag{3.37}$$

$$C_{2,a} = C_{2,g} \times P_{rated,a}(pu) \tag{3.38}$$

$$V_{on,a} = V_{on,g} \tag{3.39}$$

$$R_{on,a} = R_{on,g}/P_{rated,a}(pu) \tag{3.40}$$

where: $R_{1,a}$, $R_{2,a}$, $R_{p,a}$, $C_{1,a}$, $C_{2,a}$, $V_{on,a}$ and $R_{on,a}$ are the aggregate model parameter values while $R_{1,g}$, $R_{2,g}$, $R_{p,g}$, $C_{1,g}$, $C_{2,g}$, $V_{on,g}$ and $R_{on,g}$ are the generic model parameter values.

With respect to the aggregate model of Type C LED lamps, the relation between the aggregate and generic model parameter values are indicated in (3.41-3.44). The simulated current waveform of the aggregate model of 100 generic Type C LED lamp models with $P_{rated}$ of individual lamp equal to the median value in Table 3.13, is illustrated in Figure 3.38(c), which is the same with the sum of ac current waveforms of all the individual lamps.

$$V_{on,a} = V_{on,g} \tag{3.41}$$

$$R_{eq,a} = R_{eq,g}/P_{rated,a}(pu) \tag{3.42}$$

$$I_{req,a} = I_{req,g} \times P_{rated,a}(pu) \tag{3.43}$$

$$V_{th,a} = V_{th,g} \tag{3.44}$$

where: $V_{on,a}$, $R_{eq,a}$, $I_{req,a}$ and $V_{th,a}$ are the aggregate model parameter values while $V_{on,g}$, $R_{eq,g}$, $I_{req,g}$ and $V_{th,g}$ are the generic model parameter values.

## 3.5 Chapter conclusions

The chapter starts with a detailed review of the typical LED driver circuits, with their general working principles and current waveform distortion characteristics fully discussed, implying that the harmonic characteristics of LED lamps are closely related to the applied circuit topologies. After that, the comprehensive laboratory testing results of 28 different residential LED lamps are discussed, with the main focus given to the impact of supply conditions on the performance and electrical characteristics of tested lamps. As the current waveform distortion features and electric power quantities of certain tested LED lamps exhibit similar supply voltage dependency, the tested lamps are classified into four types, with their general circuit topologies discussed. Based on the derived relationships between the time-domain current waveform and the circuit parameters of general circuit topologies, the generalised modelling approach is proposed for each type LED lamps, with the accuracy of developed models fully validated.

With the developed models for individual LED lamps, the correlation between the circuit parameter values and the rated operating power, $P_{rated}$, is investigated and applied for developing the generic and further aggregate model for each type LED lamps. All those results can be easily applied for investigating the impact of large-scale residential LED lamps on LV networks. The proposed generalised component-based modelling approach can also be applied to other types of PE devices with passive front-end circuits (e.g. SMPS' with no-PFC and with p-PFC), with only a few numbers of tests and measurements required.

# Chapter 4

# Harmonic modelling and characterisation of SMPS'

## 4.1 Introduction

As one of the typical PE devices in both residential and commercial load sectors, computer SMPS' are gradually increasing the penetration into the LV networks. For example, it is reported in [94][95] that the percentage of households with desktop PCs in the UK has increased from ~13% in 1985 to ~85% in 2014, while the percentage of individuals using computers on a daily basis increased from ~45% in 2006 to ~72% in 2015, as illustrated Figure 4.1. Accordingly, the continuously increasing numbers of SMPS' require careful evaluation of their performance and potential PQ impact on LV networks.

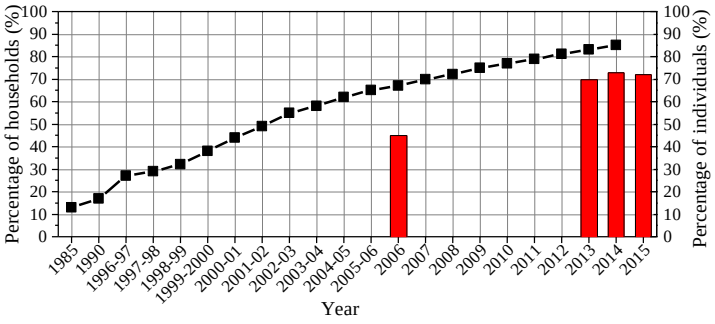



**Figure 4.1:** Percentage of households with desktop computers in the United Kingdom from 1985 to 2014 and percentage of individuals using computers daily in 2006, 2013-15.

Although the classification of SMPS' can be performed according to different criteria like the application (e.g. laptop, desktop or server), the circuit topologies (e.g. isolated or non-isolated topologies), the power flow direction (unidirectional or bidirectional), etc., the considered desktop PC-SMPS' are classified into three general types based on the applied PFC circuits: a) without PFC (no-PFC), b) with passive PFC (p-PFC) and c) with active PFC (a-PFC) [96]. Specifically, SMPS' with no-PFC are based on the uncontrolled full-wave rectifier followed by a large storage capacitor, while SMPS' with p-PFC usually connect a bulky inductor between the full-wave rectifier and the storage capacitor. Considering the fact that SMPS' with rated power above 75 W has to comply with the current harmonic emission requirements for "Class D" equipment

defined in [42], the majority of commercial desktop PC-SMPS' are equipped with either p-PFC or a-PFC while SMPS' with no-PFC are rarely seen on the market, but still can be found as demonstrated in this chapter. In terms of SMPS' with a-PFC, the bulky inductor used in SMPS' with p-PFC is replaced with an a-PFC based converter with its control circuit. The increasing penetration of SMPS' with a-PFC into the market is also driven by certain energy certifications scheme such as "Energy Star" and "80 PLUS", [97]-[98], which have stringent efficiency and power factor requirements that cannot be easily achieved by SMPS' with p-PFC. As opposed to SMPS' with no-PFC and with p-PFC, SMPS' with a-PFC can better regulate the output voltage of the dc-link capacitor with less voltage fluctuation, which will facilitate the design of the followed DC-DC conversion stages [99]. As SMPS' with a-PFC feature a high circuit diversity, it is also important to investigate the impact of different a-PFC circuits on the operational performance of SMPS' and their PQ impact on the grid, which is demonstrated on three SMPS' with different a-PFC strategies in this chapter.

The existing literature on the efficiency and PQ aspects of SMPS' only considered limited operating powers of SMPS' working under sinusoidal supply condition. For example, the efficiency and harmonic emission of a computer SMPS with no-PFC are measured and discussed in [100], by decomposing the overall efficiency into efficiencies of different sections of the circuit. However, the results given are for SMPS operating at 24% rated power ($P_{rated}$) without further investigating the change of efficiency and harmonic emission over the whole power range. In practice, the power consumption of SMPS' during normal operation mostly varies in range from 20%-60% of $P_{rated}$ [101]-[102], depending on the use of specific PC application or the performed activity [103]. In addition, most of the previous works (e.g. [104][105][106]) concentrate on SMPS' with no-PFC or with p-PFC, without comparing their performance with SMPS' with a-PFC. Finally, the related harmonic emission regulation standards (e.g. [42]) for SMPS' requires the tests performed under ideal supply condition only (i.e. ideally sinusoidal supply voltage with magnitude of 1 p.u. and no source impedance connected), which normally cannot represent the harmonic emission characteristics of SMPS' operating under real network scenarios which are typically featured by supply voltage distortion, magnitude deviation, three-phase unbalance, etc.

In this chapter, six commercial desktop SMPS' are selected as the typical representatives of the three main types of SMPS' based on the PFC circuits applied (with no-PFC, with p-PFC and with a-PFC), with their efficiency and PQ performance for the whole operating power range and under both purely sinusoidal and distorted supply voltages fully investigated.

## 4.2 Laboratory testing of SMPS'

This section starts with an introduction of the laboratory testing set-up of SMPS', as well as the basic information of the six SMPS'. After that, the power dependency of input current waveform distortion for the tested SMPS' operating under the whole power range is discussed, which is the basis for analysing the impact of supply conditions on the characteristics and performance of SMPS' in the next section.

### 4.2.1 Test set-up and analytical framework

**Test set-up**

The fully automated test set-up is configured as shown in Figure 4.2, consisting of a fully controllable voltage source, a control PC, a data acquisition system (i.e. ADC system), voltage and current probes and two variable resistances for adjusting the operating power of SMPS' at 12 V and 5 V dc outputs (3.3 V output is ignored due to its relatively small power output as opposed to the 12 V and 5 V outputs).

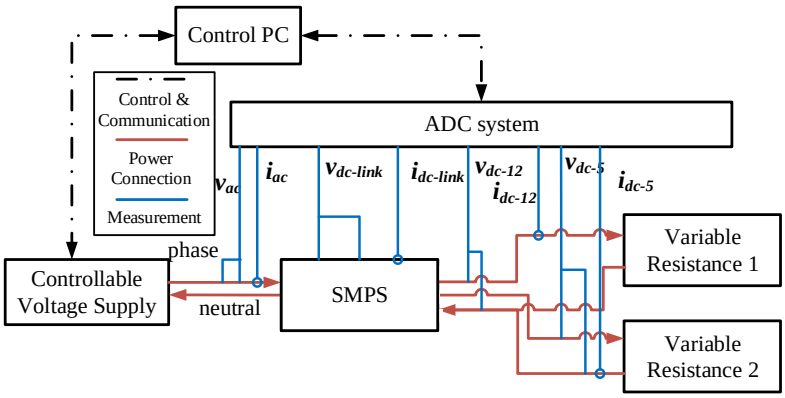



**Figure 4.2:** A fully automated SMPS test set-up.

Considering the fact that the operating power of SMPS' can vary significantly with the change of specific applications, the operating powers of six considered PC-SMPS' are (approximately) adjusted at the following values: 100%, 75%, 50%, 25%, 15%, 10%, 5% and 1% of $P_{rated}$. The six selected SMPS' are first tested under ideal supply

condition (i.e. purely sinusoidal supply voltage with a magnitude of 1 p.u.), using as the reference case. Afterwards, to investigate the sensitivity of the efficiency and PQ performance of tested SMPS' to the individual voltage harmonics as well as providing the essential measurement data required for the development of FDMs in the later sections, the individual voltage harmonic tests are performed, for which the individual voltage harmonic is superimposed to the sinusoidal supply voltage with the resultant voltage magnitude maintained at 1 p.u.

Specifically, the considered individual voltage harmonic orders are from 2$^{nd}$ to 25$^{th}$ (both even and odd orders), with a combination of stepwise changes of voltage harmonic magnitudes and phase angles. For each individual voltage harmonic order, the phase angle is adjusted from 0° to 330° in steps of 30°, with respect to the zero crossing of fundamental component, while the harmonic magnitude is adjusted as 0.5x$V_{h,limit}$, 1x$V_{h,limit}$ and 2x$V_{h,limit}$ (and 5% $V_1$ if 2x$V_{h,limit}$ is lower than 5% $V_1$) where $V_{h,limit}$ is the corresponding limit value from [40] and 5% $V_1$ is the maximum limit from [39] for the worst case conditions (i.e. the lowest short circuit ratio). According to the above discussion, the applied test sequence for each of the selected SMPS' operating under specified power is made up of 1093 tests (1x ideally sinusoidal supply voltage; 19x individual harmonic distorted voltages with 4x harmonic magnitudes and 5x individual harmonic distorted voltages with 3x harmonic magnitudes; and 12x harmonic phase angles).

**Analytical framework**

The indices applied for evaluating the efficiency and PQ performance of tested SMPS' include efficiency ($\eta$), fundamental efficiency ($\eta_1$), true power factor ($PF$), displacement power factor ($PF_1$), total harmonic active power at the input ac side ($P_{in,H}$), total subgroup current harmonic distortion ($THDS_I$), and total current harmonic and interharmonic distortion for the high-frequency range 2-150 kHz ($TH\&IHD_{I,HF}$), with the calculation procedure based on [8][33][37][93]. Indices are calculated by using the 200 ms time window which is recommended in [33] for spectral analysis (the sampling frequency is around 300 kSa/s), with the applied equations represented by (4.1-4.9).

$$P_{in,ac} = \frac{1}{kT}\int_{\tau}^{\tau+kT} p_{in,ac}\,dt = \frac{1}{kT}\int_{\tau}^{\tau+kT} v_{ac} i_{ac}\,dt \quad (4.1)$$

$$P_{in,1} = V_1 I_1 cos\Theta_1 \quad (4.2)$$

$$P_{in,H} = V_0 I_0 + \sum_{h\neq 1} V_h I_h cos\Theta_h = P_{in-ac} - P_{in,1} \quad (4.3)$$

$$\eta = \frac{P_{out,dc}}{P_{in,ac}} \times 100 \quad (4.4)$$

$$\eta_1 = \frac{P_{out,dc}}{P_{in,1}} \times 100\% \quad (4.5)$$

$$PF = \frac{P_{in,ac}}{S_{in,ac}} = \frac{P_{in,ac}}{V_{ac} I_{ac}} \quad (4.6)$$

$$PF_1 = cos\Theta_1 \quad (4.7)$$

$$THDS_I = \sqrt{\sum_{h=2}^{40} (\frac{I_{sg,h}}{I_{sg,1}})^2} \quad (4.8)$$

$$TH\&IHD_{I,HF} = \sqrt{\sum_{f=2kHz+5Hz}^{f=150kHz} (\frac{I_f}{I_{sg,1}})^2} \quad (4.9)$$

where: $v_{ac}$ and $i_{ac}$ are the instantaneous time-domain voltage and current waveforms respectively while $V_1$ and $I_1$ are the rms value of the fundamental voltage and current components respectively; $\tau$, $T$ and $k$ are the moment when the measurement starts, period and positive integer number, respectively; the phase angle difference between the fundamental voltage and current is represented by $\Theta_1$ while the phase angle difference between voltage harmonic and current harmonic of order h is denoted as $\Theta_h$; the input ac active power and its fundamental component are represented by $P_{in,ac}$ and $P_{in,1}$ respectively while input harmonic active power is denoted as $P_{in,H}$; $V_0$ and $I_0$ are the dc component of input voltage and current respectively while $V_h$ and $I_h$ are the voltage harmonic and current harmonic of order h respectively; $I_{sg,1}$ and $I_{sg,h}$ are the subgroup fundamental current component and the subgroup current harmonic of order $h$ respectively; the spectrum component (rms value from the FFT decomposition) of input ac current at frequency $f$ is represented by $I_{f\text{-}spec}$.

### 4.2.2 Basic information and results of tested SMPS'

The six tested SMPS' are for commercial desktop PC applications, with their PFC types and rated power output tabulated in Table 4.1. The input ac current waveforms

of tested SMPS' operating under different powers with ideally sinusoidal supply voltage are illustrated in Figure 4.3.

**Table 4.1:** Basic information of six tested SMPS'.

| | **SMPS1** | **SMPS2** | **SMPS 3** | **SMPS 4** | **SMPS 5** | **SMPS 6** |
|---|---|---|---|---|---|---|
| **PFC Type** | no-PFC | p-PFC | p-PFC | a-PFC | a-PFC | a-PFC |
| ***P*$_{rated}$ (W)** | 280 | 320 | 400 | 400 | 400 | 350 |

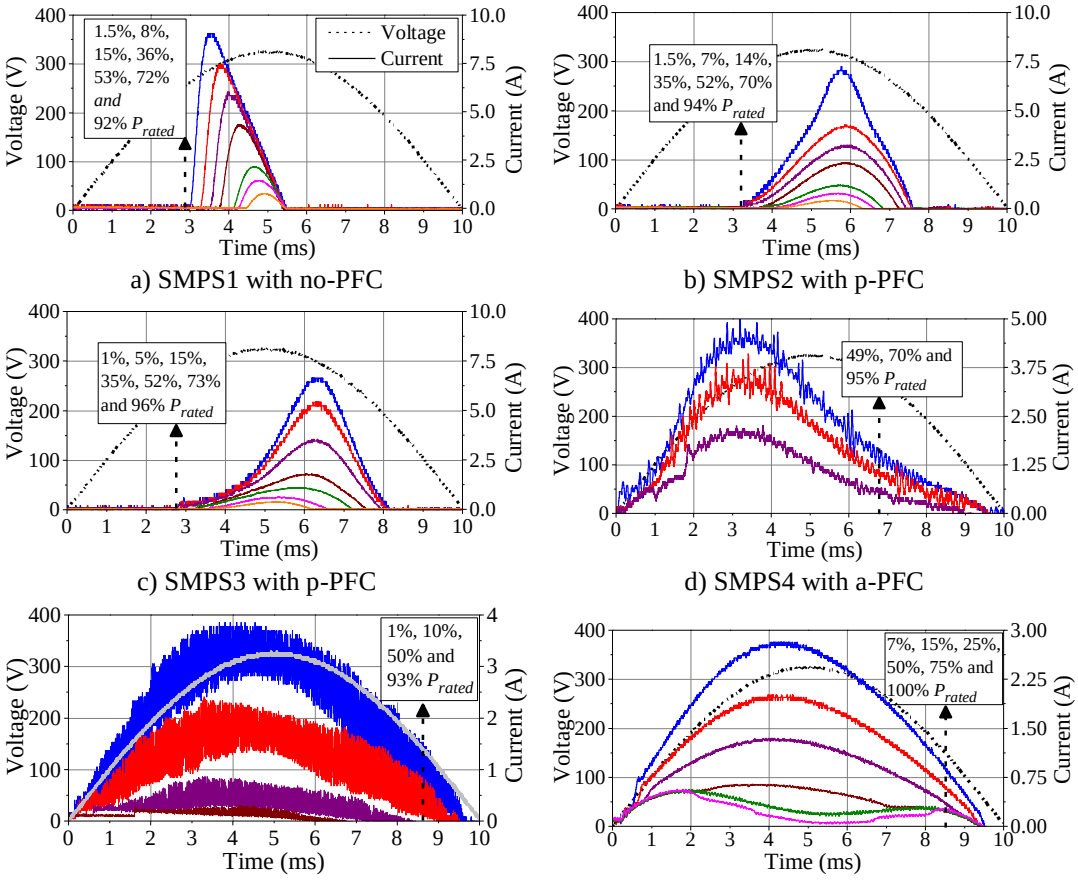



**Figure 4.3:** Input half-cycle ac voltage and current waveforms for six tested SMPS' operating at different power levels for ideally sinusoidal supply voltage.

It is observed from Figure 4.3 that the input ac current waveforms of SMPS1 with no-PFC and SMPS2-3 with p-PFC do not significantly change with the decrease of operating power, maintaining a discontinuous pulse-like waveform shape with the current conduction time gradually decreasing with the reducing powers. As opposed to SMPS' with no-PFC or p-PFC, SMPS' with a-PFC have continuous input ac current waveform, but distinctive waveform features depending on the specific a-PFC circuit applied. Specifically, the input current waveform of SMPS5 and SMPS6 is more close

to sinusoidal waveform shape than SMPS4 for the high-power range (i.e. above 50% $P_{rated}$), even though the input current of SMPS5 is superimposed with high-frequency harmonics. In addition, the input current waveforms of SMPS' with a-PFC exhibit strong power dependency which is represented by the apparent change of waveform shape, especially for the low power (e.g. 10%-30% $P_{rated}$) and very low power (below 10% $P_{rated}$) operating ranges. What's even worse, the input current waveforms of SMPS4 and SMPS6 become highly distorted and loss the 20 ms periodicity when the operating power drops below 49% $P_{rated}$ and 7% $P_{rated}$ for SMPS4 and SMPS6 respectively, resulting in significantly increased emission of subharmonics, interhamronics and dc component. For example, it is observed from Figure 4.4 that the period of input current changes from 20 ms to 60 ms, and correspondingly an apparently increase of subharmonic (e.g. at 50/3 Hz) and interharmonics (e.g. at 250/3 Hz and 350/3 Hz) is seen in the harmonic spectrum.

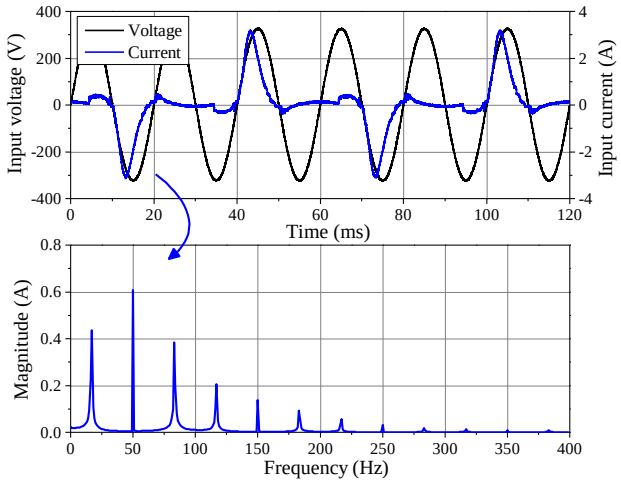



**Figure 4.4:** Instantaneous input ac voltage and current waveforms for SMPS4 operating at 25% of $P_{rated}$ under sinusoidal supply voltage.

## 4.3 Impact of supply conditions on the characteristics and performance of SMPS'

In this section, the impact of individual voltage harmonics on the efficiency and PQ performance of six tested SMPS' with different PFC circuits will be investigated, based on the indices defined in Section 4.2.1.

### 4.3.1 Total and fundamental efficiencies

It is noticed from (4.3-4.5) that the harmonic power, $P_{in,H}$, is directly related with the fundamental efficiency, $\eta_1$, and the total efficiency, $\eta$. Specially, when $P_{in,H}$ is positive, SMPS' consume harmonic active power from the grid, making $\eta_1$ higher than $\eta$. On the opposite, SMPS' inject harmonic active power to the grid when $P_{in,H}$ is negative, making $\eta_1$ less than $\eta$. For example, Figure 4.5 shows the $P_{in,H}$, $\eta$ and $\eta_1$ for SMPS1 operating under $P_{rated}$ with 3rd harmonic of different magnitudes and phase angles. It is observed from Figure 4.5 that $P_{in,H}$ is affected by both the magnitudes and phase angles of 3rd voltage harmonic, resulting in corresponding changes of $\eta$ and $\eta_1$ (more apparent for $\eta_1$).

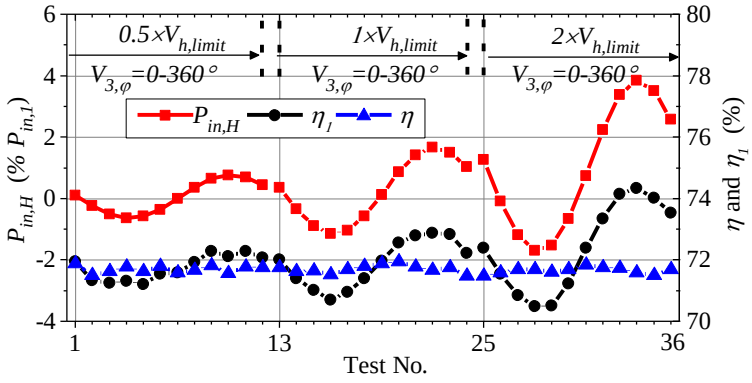
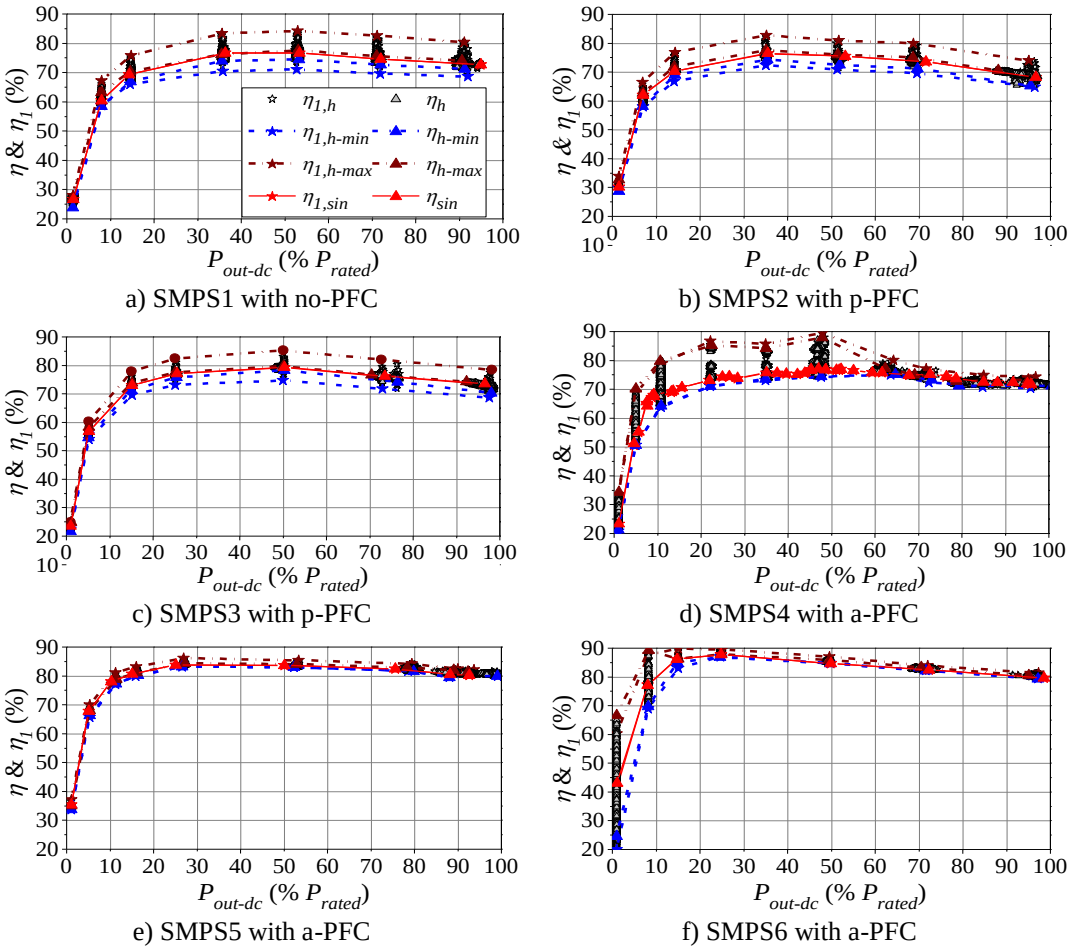



**Figure 4.5:** The $P_{in,H}$, $\eta$ and $\eta_1$ for SMPS1 operating under $P_{rated}$ and distorted supply voltage with 3rd harmonic of different magnitudes and phase angles.

The obtained $\eta$ and $\eta_1$ of six tested SMPS' operating under both sinusoidal and distorted supply voltage with different individual harmonic contents (as given in Section 4.2,1), are illustrated in Figure 4.6. Specifically, the individual symbols represent the indices values under individual voltage harmonic tests while the dash line and the dash dot line refer to the minimum and maximum indices values among all individual voltage harmonic tests respectively. The indices value under sinusoidal supply voltage is represented by the solid line. It turns out that SMPS1 with no-PFC (Figure 4.6(a)) and SMPS2-3 with p-PFC (Figure 4.6(b)-4.6(c)) have similar curves for the whole operating range and distorted supply conditions, where an apparent variation of $\eta_1$ is seen as opposed to $\eta$ which is almost the same with the corresponding value under ideal supply condition. In terms of SMPS4-6 with a-PFC, $\eta$ and $\eta_1$ curves of SMPS5 almost overlap, and are less sensitive to the different distorted supply

conditions. For SMPS4 and SMPS6, $\eta$ have similar values with $\eta_1$ until the operating power drops below certain points (around 49% $P_{rated}$ and 7% $P_{rated}$ for SMPS4 and SMPS6 respectively). After that, significant variation of $\eta$ and $\eta_1$ is seen with the change of distorted supply conditions. It should be noted that $\eta$ and $\eta_1$ of SMPS' operating under sinusoidal supply condition (denoted by $\eta_{sin}$ and $\eta_{1,sin}$ respectively) are exactly the same as $P_{in,H}$ equals zero, irrespective of the actual current harmonic emission of SMPS'.




a) SMPS1 with no-PFC

b) SMPS2 with p-PFC

c) SMPS3 with p-PFC

d) SMPS4 with a-PFC

e) SMPS5 with a-PFC

f) SMPS6 with a-PFC

**Figure 4.6:** Efficiencies ($\eta$ and $\eta_1$) of six tested SMPS' at different operating powers and under both sinusoidal and distorted voltage supply conditions.

In addition, when SMPS' are operating under their main power range (i.e. 20%-100% $P_{rated}$), it is observed from Figure 4.6 that SMPS' with no-PFC and with p-PFC have their efficiencies ($\eta$ and $\eta_1$) around 70%-80% while SMPS' with a-PFC achieves higher efficiencies which are around 80%-90% (except for SMPS4 with efficiencies at 70%-80%), suggesting that integrating a-PFC circuits into the design of SMPS' cannot ensure a high overall efficiency which is also determined by the specific a-PFC

algorithms applied and the efficiency of the followed DC-DC converter. When SMPS' are operating at low power range (below 20% $P_{rated}$), the efficiencies for all the six tested SMPS' significantly decrease with the reducing power, which is mainly resulted from the increased switching losses [107].

For the efficiencies obtained under distorted supply voltage with different individual harmonic contents, their maximum and minimum values at different powers are indicated with dash-dotted lines (for $\eta_{1,h\text{-}min}$ and $\eta_{1,h\text{-}max}$) and dashed lines (for $\eta_{h\text{-}min}$ and $\eta_{h\text{-}max}$), as illustrated in Figure 4.6. As opposed to the variations of $\eta_h$, the variations of $\eta_{1,h}$ are more apparent, particularly for SMPS' with no-PFC and with p-PFC. Additionally, when the lost periodicity happens for the input ac current waveforms of SMPS4 and SMPS6 when their operating powers drops below certain points, significant variations of $\eta_{1,h}$ and $\eta_h$ are observed, implying the improper operation of a-PFC circuits at lower power has a strong impact on the efficiencies of SMPS'.

### 4.3.2 True and displacement power factors

As shown in (4.10), the true power factor, *PF*, quantifies the ratio of active power to the total apparent power supplied to the load by the utility, and can be rewritten as the product of displacement power factor, $PF_1$, and the distortion power factor, $PF_d$.

$$PF = \frac{P_{in,ac}}{S_{in,ac}} = \frac{P_{in,1}+P_{in,H}}{S_{in,1}\sqrt{(1+THD_V^2)(1+THD_I^2)}} =$$

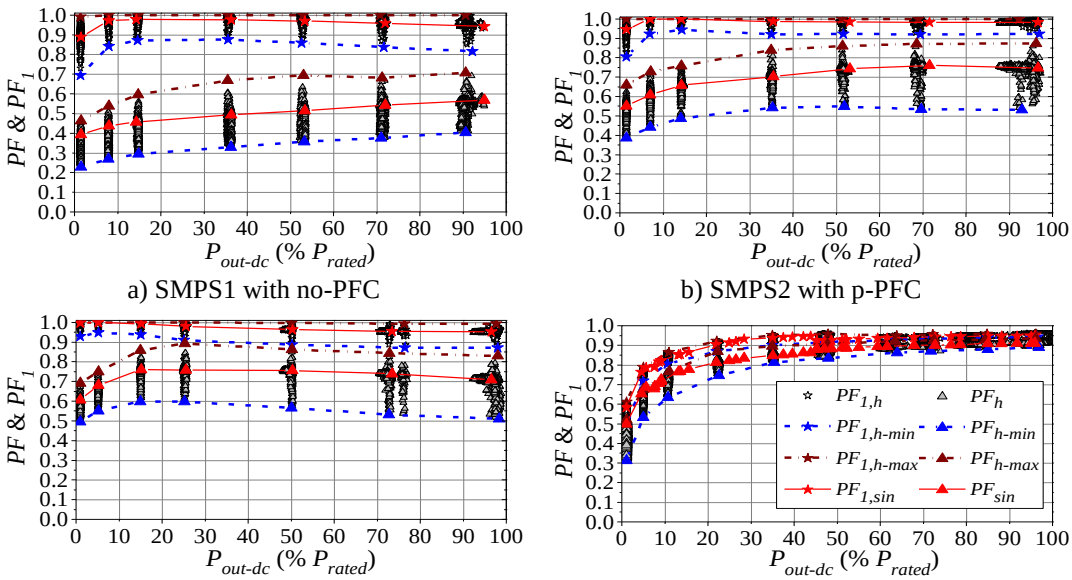
$$= \frac{\frac{P_{in,1}}{S_{in,1}}+\frac{P_{in,H}}{S_{in,1}}}{\sqrt{(1+THD_V^2)(1+THD_I^2)}} = \frac{PF_1(1+\frac{P_{in,H}}{P_{in,1}})}{\sqrt{(1+THD_V^2)(1+THD_I^2)}} = PF_1 PF_d \qquad (4.10)$$

where: $P_{in,ac}$, $S_{in,ac}$, $P_{in,1}$, $P_{in,H}$, $S_{in,1}$ are the input ac active power, input ac apparent power, input fundamental active power, input harmonic active power and input fundamental apparent power respectively; $THD_V$ and $THD_I$ are the waveform distortion of input voltage and current respectively.

It is observed from (4.2) and (4.10) that $PF_1$ represents the ratio of fundamental active power to the fundamental apparent power and is equal to the cosine of the phase angle difference between fundamental voltage component and fundamental current component, while $PF_d$ quantifies the impact of harmonic active power and the presence

of supply voltage and current waveform distortion on the *PF*. Due to the fact that $THD_V$ of supply voltages in LV networks are typically below 5% and $P_{in,H}$ is relatively small as opposed to $P_{in,1}$, $PF_d$ is mainly determined by the $THD_I$ of supply current with an inverse relationship (i.e. the high $THD_I$, the lower $PF_d$ and hence lower *PF*).

The calculated *PF* and $PF_1$ of the six tested SMPS' are illustrated in Figure 4.7 (using the same figure plot as in Figure 4.6), with the minimum and maximum values under considered distorted supply conditions for specific operating power indicated by dash lines ($PF_{I,h\text{-}min}$ and $PF_{I,h\text{-}min}$) and dash-dotted lines ($PF_{I,h\text{-}max}$ and $PF_{h\text{-}max}$) respectively ($PF_d$ is not given as it equals the ratio of *PF* to $PF_1$). It is observed that the *PF* curves (the curves for the calculated minimum and maximum values under individual voltage harmonics, as well as the curves under sinusoidal supply voltage) are lower than the corresponding $PF_1$ curves for all the six tested SMPS' operating under the whole power range. In addition, the difference between *PF* and $PF_1$ is more apparent for SMPS' with no-PFC and with p-PFC than SMPS' with a-PFC, which is due to the higher current waveform distortion of SMPS' with no-PFC and with p-PFC.

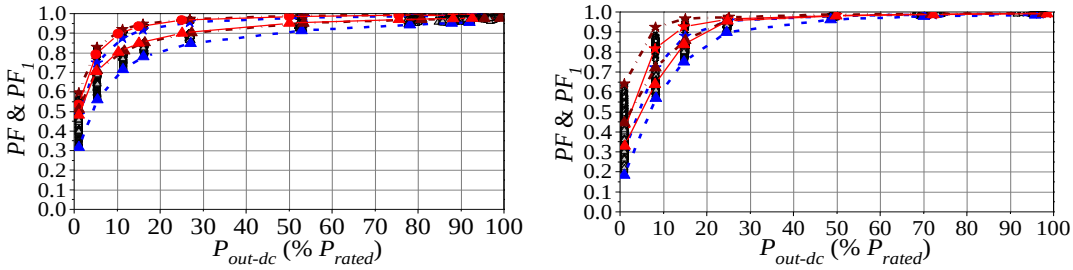



a) SMPS1 with no-PFC

b) SMPS2 with p-PFC

c) SMPS3 with p-PFC

d) SMPS4 with a-PFC




e) SMPS5 with a-PFC f) SMPS6 with a-PFC

**Figure 4.7:** Power factors (*PF* and $PF_1$) of six tested SMPS' at different operating powers and under both sinusoidal and distorted voltage supply conditions.

It is also observed from Figure 4.7 that the $PF_1$ values of SMPS' with no-PFC and with p-PFC are close to unity for the whole operating power range, while the $PF_1$ values of SMPS' with a-PFC significantly decrease when the operating power drops below 20% $P_{rated}$, implying a deterioration of performance. Moreover, the variations of *PF* and $PF_1$ for SMPS' with no-PFC and with p-PFC are more apparent than that for SMPS' with a-PFC (but still noticeable variations). The variations of *PF* and $PF_1$ for SMPS' with a-PFC become stronger with the decrease of operating powers, especially for the lower power range.

### 4.3.3 Harmonic and HF current waveform distortions

The calculated $THDS_I$ and $TH\&IHD_{I,HF}$ values for six tested SMPS' are illustrated in Figure 4.8 (using the same figure plot as in Figure 4.6). It turns out that SMPS' with no-PFC and with p-PFC have much larger $THDS_I$ values than SMPS' with a-PFC when they are operating under sinusoidal supply voltage, suggesting that equipping SMPS' with a-PFC circuits achieves an improved regulation of the input ac current waveform. However, variations of $THDS_I$ are seen for all tested SMPS' operating under distorted supply voltage conditions (i.e. individual voltage harmonics), and are more pronounced for SMPS' with no-PFC and with p-PFC at all operating powers as opposed to the variations of $THDS_I$ for SMPS' with a-PFC. In addition, the variations of $THDS_I$ for SMPS' with no-PFC and with p-PFC is less sensitive to the change of operating powers as opposed to SMPS' with a-PFC, for which the variations increase with the reducing operating powers.

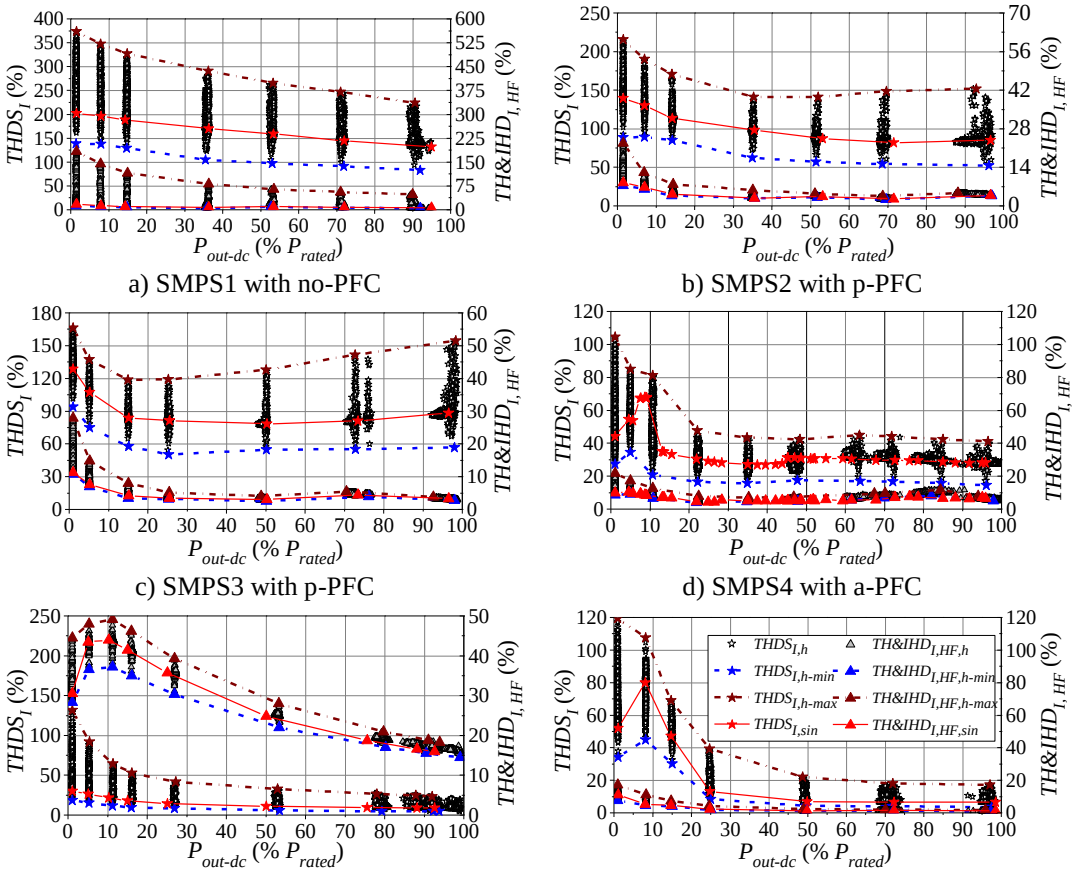



**Figure 4.8:** Harmonic and current waveform distortions ($THDS_I$ and $TH\&IHD_{I,HF}$) of six tested SMPS' at different powers with both sinusoidal and distorted voltage supply conditions.

It is also noticed that the $THDS_{I,sin}$ curves are located between the $THDS_{I,h\text{-}min}$ and $THDS_{I,h\text{-}max}$ curves, implying that individual voltage harmonics may either aggravate or alleviate the supply current distortion depending on their phase angles (hence highlighting the importance of phase angles in the analysis).

With respect to the high-frequency (above 2 kHz) harmonic and interharmonic supply current distortion represented by $TH\&IHD_{I,HF}$, it is found that $TH\&IHD_{I,HF}$ values for all the tested SMPS' are relatively low compared with $THDS_I$ values, indicating that the supply current distortion is mainly determined by low-order ($2^{nd}$-$40^{th}$) harmonics. Except for SMPS5 with its $TH\&IHD_{I,HF}$ values above 10%, all the other five SMPS' have their $TH\&IHD_{I,HF}$ values below 10% for their main operating power ranges (above 20% $P_{rated}$). With respect to the $TH\&IHD_{I,HF}$ values under distorted supply voltage conditions, $TH\&IHD_{I,HF}$ values generally exhibit small variations for most of the test SMPS' except for SMPS1, for which a relatively strong variation is seen.

The main finding from the above discussions can be summarised as the following points:

a) a higher total efficiency (around 80%-90%) is achieved by SMPS' with a-PFC (except SMPS4) as opposed to the total efficiency (around 70%-80%) of SMPS' with no-PFC and with p-PFC for the operating powers above 20% of $P_{rated}$;

b) the specified individual voltage harmonic distortions have negligible impacts on the total efficiency curves of all tested SMPS';

c) greater variations of the fundamental efficiency curves are seen for SMPS' with no-PFC or p-PFC than SMPS' with a-PFC;

d) close to unity $PF_1$ is achieved by all tested SMPS' operating at high power ranges, while higher $PF$ is obtained by SMPS with a-PFC than SMPS with no-PFC and with p-PFC for both sinusoidal and distorted voltage supply;

e) due to the input current regulation of a-PFC circuits, SMPS' with a-PFC achieve much smaller $THDS_I$ than SMPS' with no-PFC and p-PFC;

f) performance of all SMPS' deteriorates in terms of $\eta$, $PF$ and harmonic emission) when the operating powers drop below certain points;

g) SMPS' with a-PFC may fail to maintain the close-to-sinusoidal waveform shape for the input current at low (SMPS4) and very low (SMPS6) powers, which is manifested by significantly distorted currents and lost periodicity.

All in all, it turns out that even though SMPS' with a-PFC achieve better efficiency and PQ performance than SMPS' with no-PFC and with p-PFC at high powers, their harmonic, subharmonic and interhamonic current emission may significantly increase at low or very low powers, highlighting the importance of the comprehensive assessment of the possible impacts of SMPS' with different PFC types on both existing networks and future "smart grids".

## 4.4 Harmonic modelling of SMPS'

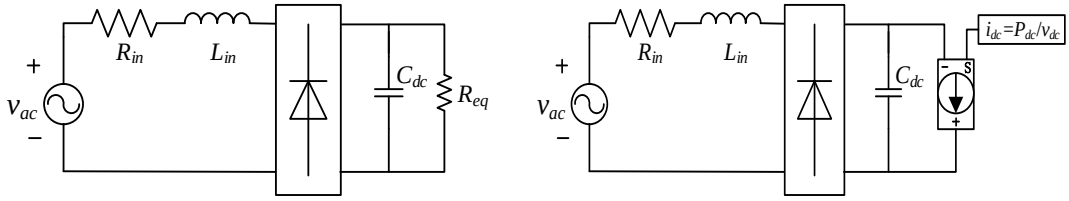
This section focuses on the harmonic modelling of the three main SMPS types, which is demonstrated on SMPS1 (with no-PFC), SMPS2 (with p-PFC) and SMPS4 (with a-PFC). The development procedure of CBMs and FDMs for the three main SMPS types will be discussed, with the model accuracy fully validated with measurements.

### 4.4.1 Component-based modelling

In this subsection, the component-based modelling methodology for the three main SMPS types will be demonstrated on SMPS1 (with no-PFC), SMPS2 (with p-PFC) and SMPS4 (with a-PFC) respectively, with the simulation results fully validated with measurements.

**Component-based modelling of SMPS1 (with no-PFC)**

As the PQ performance of SMPS1 with no-PFC is mainly determined by its front-end circuit which is based on the full-wave rectifier with smoothing capacitor, the circuit parameter estimation approach applied for Type A LED lamps, can also be used for the component based modelling of SMPS1. Specifically, by applying the flowchart in Figure 3.25 of Chapter 3 to the typical current waveform of SMPS1 measured under rated operating power with ideal supply condition (i.e. ideally sinusoidal supply voltage with a magnitude of 1 p.u.), the main circuit parameter values-$R_{in}$, $L_{in}$, $C_{dc}$ and $R_{eq}$ marked in Figure 4.9(a) can be easily obtained (the whole back-end circuit after the dc-link capacitor is represented with the equivalent resistance $R_{eq}$). To take into the account the voltage dependency of the circuit and the change of operating powers, $R_{eq}$ should be adjusted correspondingly by using the approach given in Figure 3.26 of Chapter 3. The derived circuit parameter values-$R_{in}$, $L_{in}$, $C_{dc}$, are equal to 1.2 Ω, 0 H and 171.03 μF respectively, with the change of $R_{eq}$ under combinations of different operating powers and supply voltage magnitudes illustrated in Figure 4.10.




a) back-end circuit is represented by $R_{eq}$

b) back-end circuit is represented by $P_{dc}$ (implemented as controllable current source $i_{dc}$)

**Figure 4.9:** The component based model schematic for SMPS1 with two different representation forms for the back-end circuit.

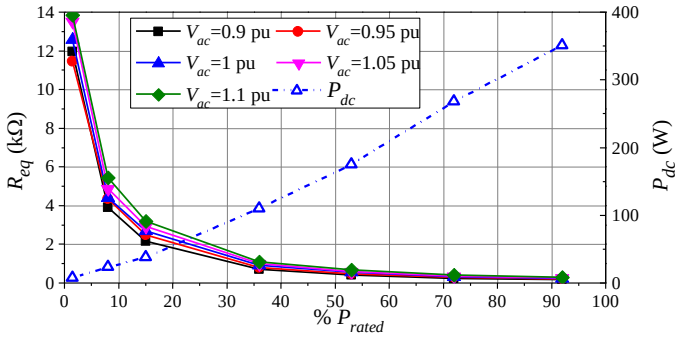


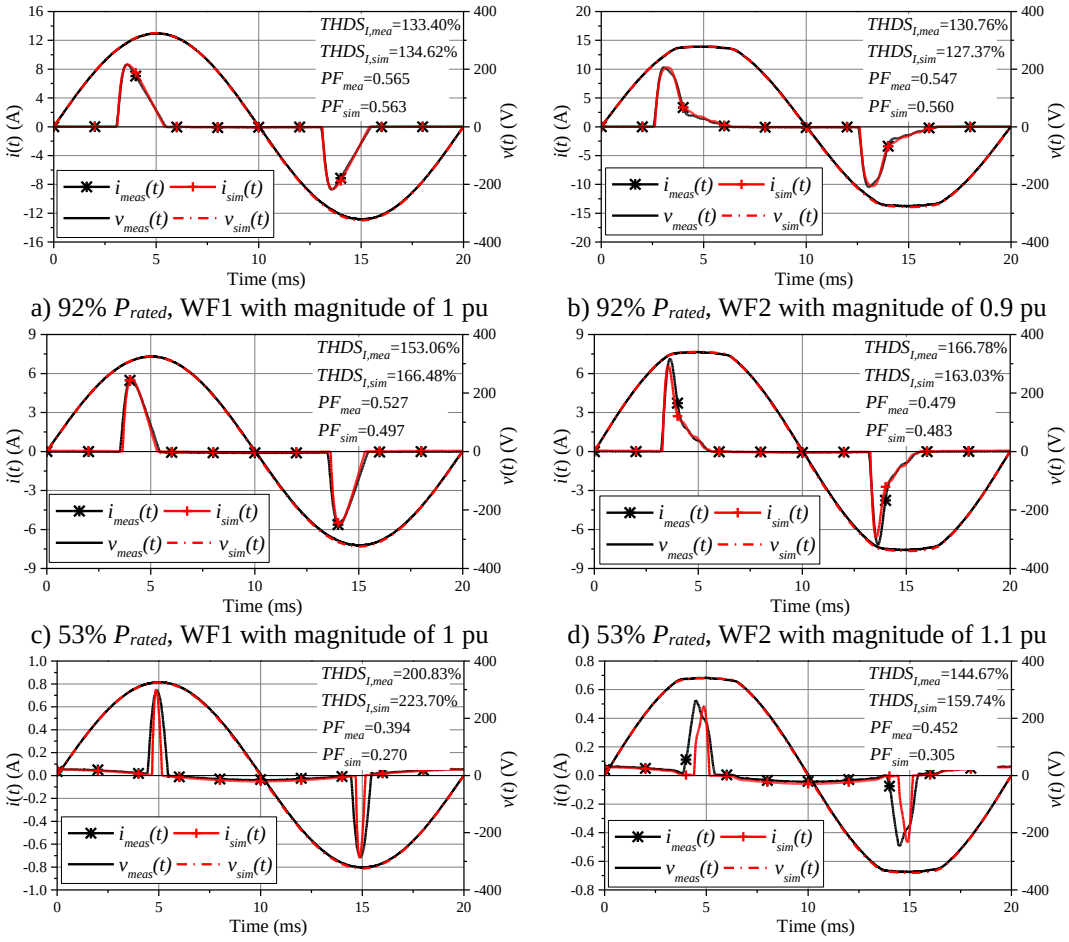

**Figure 4.10:** The obtained $R_{eq}$ values (corresponds to Figure 4.9(a)) under combinations of different supply voltage magnitudes and operating powers, and the corresponding $P_{dc}$ values (corresponds to Figure 4.9(b)).

As the power losses on the full-wave rectifier is negligible, the voltage dependency of active and reactive power for the model is determined by the voltage dependency of the power consumption on $R_{eq}$. As the exponential load model coefficient, $n_p$, for SMPS1 at different power levels is close to zero (as given in Table 4.2), SMPS1 at specific power can be regarded as constant power load type which is independent of the change of supply voltage magnitudes. It should be noted that the constant power load type refers to the voltage dependency of power for SMPS operating at specific power level while the actual power consumption of SMPS will still fluctuate in a wide range, depending on the running applications. Therefore, the equivalent resistance, $R_{eq}$, can be replaced by a "constant" power term, $P_{dc}$, which is implemented as controllable current source in Matlab/Simulink (as illustrated in Figure 4.9(b)). The value of $P_{dc}$ at specific power level can be easily calculated from $\bar{V}_{dc,sim}^2/R_{eq,1pu}$, where $\bar{V}_{dc,sim}$ is the average value of the simulated dc-link voltage under corresponding $R_{eq,1pu}$ value (i.e. the $R_{eq}$ curve in Figure 4.10 when $V_{ac}$=1 p.u.).

**Table 4.2:** The exponential load model coefficients for SMPS1.

| (% $P_{rated}$) | 1.5 | 8 | 15 | 36 | 53 | 72 | 92 |
|---|---|---|---|---|---|---|---|
| $n_p$ | 0.53 | 0.30 | 0.24 | 0.05 | -0.05 | -0.03 | -0.06 |
| $n_q$ | 1.60 | 0.55 | 0.22 | -0.62 | -1.64 | -1.20 | -1.84 |

Based on the obtained circuit parameter values as well as the $P_{dc}$ values given in Figure 4.10, the accuracy of the developed CBM can be validated by comparing the time-domain simulated current waveform with the measurement data for SMPS1 operating under different supply conditions together with different operating powers, as illustrated in Figure 4.11. It turns out the developed CBM can accurately reproduce the input ac current waveform of SMPS1 for its whole power range under both ideal and non-ideal supply conditions.




a) 92% $P_{rated}$, WF1 with magnitude of 1 pu

b) 92% $P_{rated}$, WF2 with magnitude of 0.9 pu

c) 53% $P_{rated}$, WF1 with magnitude of 1 pu

d) 53% $P_{rated}$, WF2 with magnitude of 1.1 pu

e) 1.5% $P_{rated}$, WF1 with magnitude of 1 pu

f) 1.5% $P_{rated}$, WF2 with magnitude of 1.1 pu

**Figure 4.11:** The comparison between simulated and measured time-domain input ac current waveform for SMPS1 operating under combinations of different powers and supply conditions.

**Component-based modelling of SMPS2 (with p-PFC)**

For SMPS2 with p-PFC, the same circuit topology in Figure 4.9 can be applied, with the inductor $L_{in}$ representing the p-PFC. For SMPS1, $L_{in}$ is close to zero and can be negligible while for SMPS2, $L_{in}$ has relatively large value. By applying the same modelling procedure, the circuit parameters for the CBM of SMPS2 can be easily

derived, with $R_{in}$, $L_{in}$, $C_{dc}$ equal to 1 Ω, 14.1 mH and 138.24 μF respectively and the change of $R_{eq}$ under combinations of different operating powers and supply voltage magnitudes illustrated in Figure 4.12.

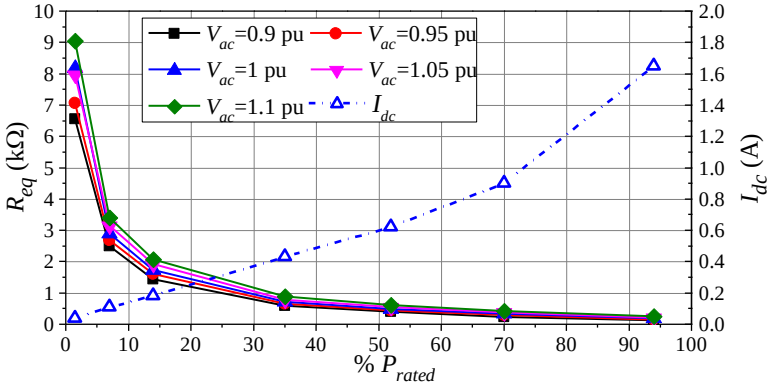
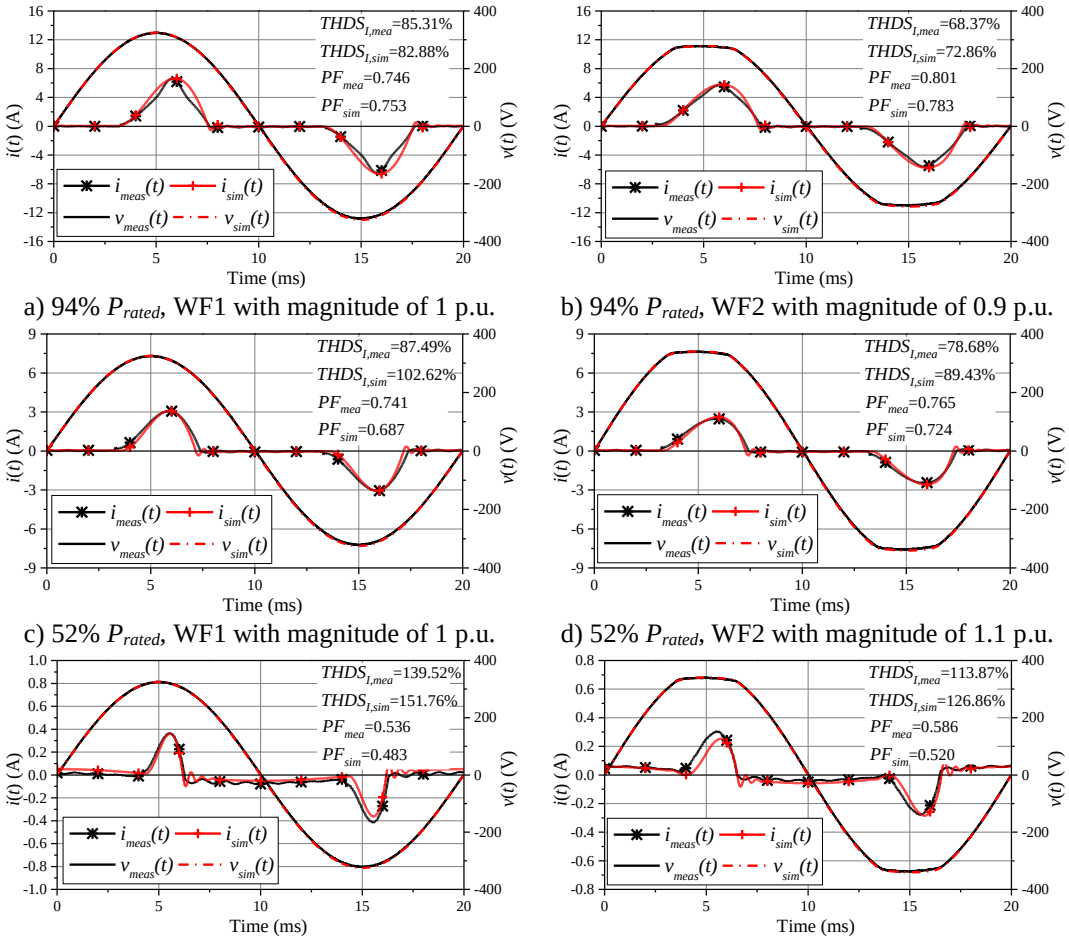



**Figure 4.12:** The obtained $R_{eq}$ values under combinations of different supply voltage magnitudes and operating powers, and the corresponding $I_{dc}$ values.

Similar with SMSP1, the representation of the back-end circuit can be either represented by $R_{eq}$ or other forms like constant power or constant current load which is determined by the supply voltage dependency of the modelled device. For the case of SMPS2, it turns out that SMPS2 belongs to constant current load type (i.e. $n_p$ close to 1) according to its exponential load model coefficients listed in Table 4.3. As the power losses of the full-wave rectifier is negligible, the supply voltage dependency of the power demand of the back-end circuit can be regarded as the same with the whole device. Accordingly, the back-end circuit can be represented by constant current source $I_{dc}$, with its values under different powers illustrated in Figure 4.12. With the obtained circuit parameter values, the model accuracy is validated by comparing the simulated input ac current waveform with the measurement for SMPS2 operating under different powers combined with different supply conditions, as shown in Figure 4.13. Again, a good accuracy is achieved by the developed CBM for SMPS2.

**Table 4.3:** The exponential load model coefficients for SMPS2.

| **(% $P_{rated}$)** | 1.5 | 7 | 14 | 35 | 52 | 70 | 94 |
|---|---|---|---|---|---|---|---|
| $n_p$ | 1.01 | 1.00 | 1.00 | 1.00 | 1.00 | 1.01 | 1.00 |
| $n_q$ | 0.54 | 0.33 | 0.16 | -0.01 | -0.03 | -0.26 | -0.11 |




a) 94% $P_{rated}$, WF1 with magnitude of 1 p.u.

b) 94% $P_{rated}$, WF2 with magnitude of 0.9 p.u.

c) 52% $P_{rated}$, WF1 with magnitude of 1 p.u.

d) 52% $P_{rated}$, WF2 with magnitude of 1.1 p.u.

e) 1.5% $P_{rated}$, WF1 with magnitude of 1 p.u.

f) 1.5% $P_{rated}$, WF2 with magnitude of 1.1 p.u.

**Figure 4.13:** The comparison between simulated and measured time-domain input ac current waveform for SMPS2 operating under combinations of different powers and supply conditions.

**Component-based modelling of SMPS4 (with a-PFC)**

Unlike SMPS1-3 which use simple p-PFC or have no PFC, SMPS4 is equipped with boost converter based a-PFC, resulting in a less distorted input ac current waveform. Due to the lack of features for the input ac current waveform, the generalised modelling approach for SMPS' with no-PFC and with p-PFC cannot be applied to SMPS' with a-PFC. Instead, the component-based modelling of SMPS' with a-PFC requires accurate representation of the equipped a-PFC based converter and its control circuits. The circuit schematic of the CBM developed for SMPS4 is illustrated in Figure 4.14, consisting of an input EMI filter, standard diode bridge rectifier (DBR) and boost converter based a-PFC circuit. Specifically, the EMI filter is a balanced "T filter" for suppressing high-frequency harmonics, followed by an uncontrolled single-phase DBR. After the DBR, a small input capacitor is connected in parallel with the function

of stabilising the input voltage in accordance with the peak current requirement of the SMPS [108]. The power dependency and supply voltage dependency of the current waveform distortion characteristics of SMPS4 is mainly determined by the boost converter based a-PFC circuit which regulates both the dc-link output voltage and the inductor current (and hence the input ac current).

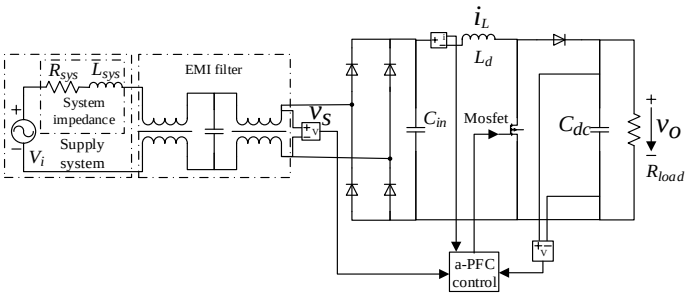



**Figure 4.14:** The schematic of the developed CBM for SMPS4.

The corresponding a-PFC control circuit is illustrated in Figure 4.15, and is based on the average current mode control, consisting of an inner current loop and an outer voltage loop. For the outer voltage loop, the sensed dc-link voltage is scaled down and then compared with the reference value, with the voltage difference supplied to the voltage controller $G_v(s)$, providing the reference magnitude for the inductor current $i_L$. By scaling down the input voltage waveform, a haversine function is obtained and multiplied with the output of the voltage controller to provide the reference waveform for the inductor current. After that, the scaled inductor current is compared with its reference waveform, with the difference fed to the current controller, $G_i(s)$. Finally, the output of the current controller is compared with a high-frequency sawtooth signal to generate the PWM control signal for the boost converter switch. The circuit parameter values of the developed CBM for SMPS4 are listed in Table 4.4. By comparing the simulated input ac current waveform with the measurement for SMPS4 operating under different powers and supply conditions as illustrated in Figure 4.16, it turns out that developed CBM is capable of accurately representing the power and supply voltage dependency of the waveform distortion characteristics of SMPS4.

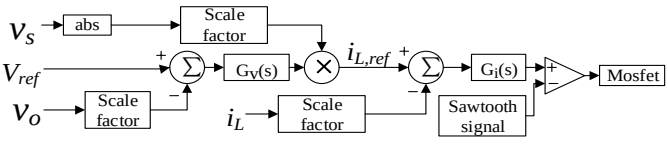
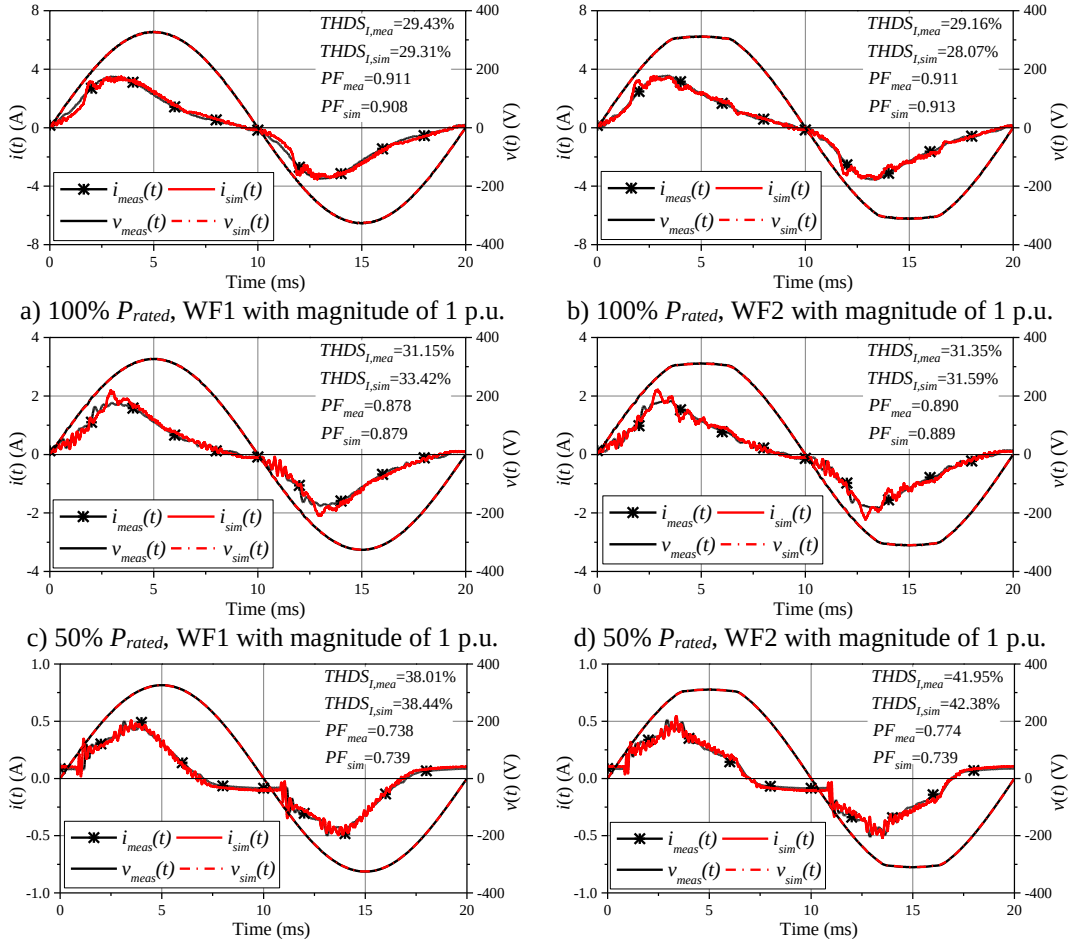


**Figure 4.15:** The block diagram of a-PFC circuit applied to the SMPS4 model.

**Table 4.4:** The circuit parameter values of the developed CBM for SMPS4.

| SMPS4 | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| **Power stage** | | | **Voltage control loop** | | | **Voltage scale factor** | **Current control loop** | | |
| $C_{in}$ (µF) | $L$ (µH) | $C_{DC}$ (µF) | **Scale factor** | $V_{ref}$ (V) | $G_V(s)$ | | **Scale factor** | $G_I(s)$ | $K_{PWM}$ |
| 1.1 | 780 | 460 | 1/400 | 2.5 | $24/(1.8\cdot10^{-3}s+1)$ | 1/325 | 0.4 | $6.5\cdot10^{3}(2\cdot10^{-5}s+1)/(10^{-6}s^{2}+s)$ | 0.25 |




a) 100% $P_{rated}$, WF1 with magnitude of 1 p.u.

b) 100% $P_{rated}$, WF2 with magnitude of 1 p.u.

c) 50% $P_{rated}$, WF1 with magnitude of 1 p.u.

d) 50% $P_{rated}$, WF2 with magnitude of 1 p.u.

e) 10% $P_{rated}$, WF1 with magnitude of 1 p.u.

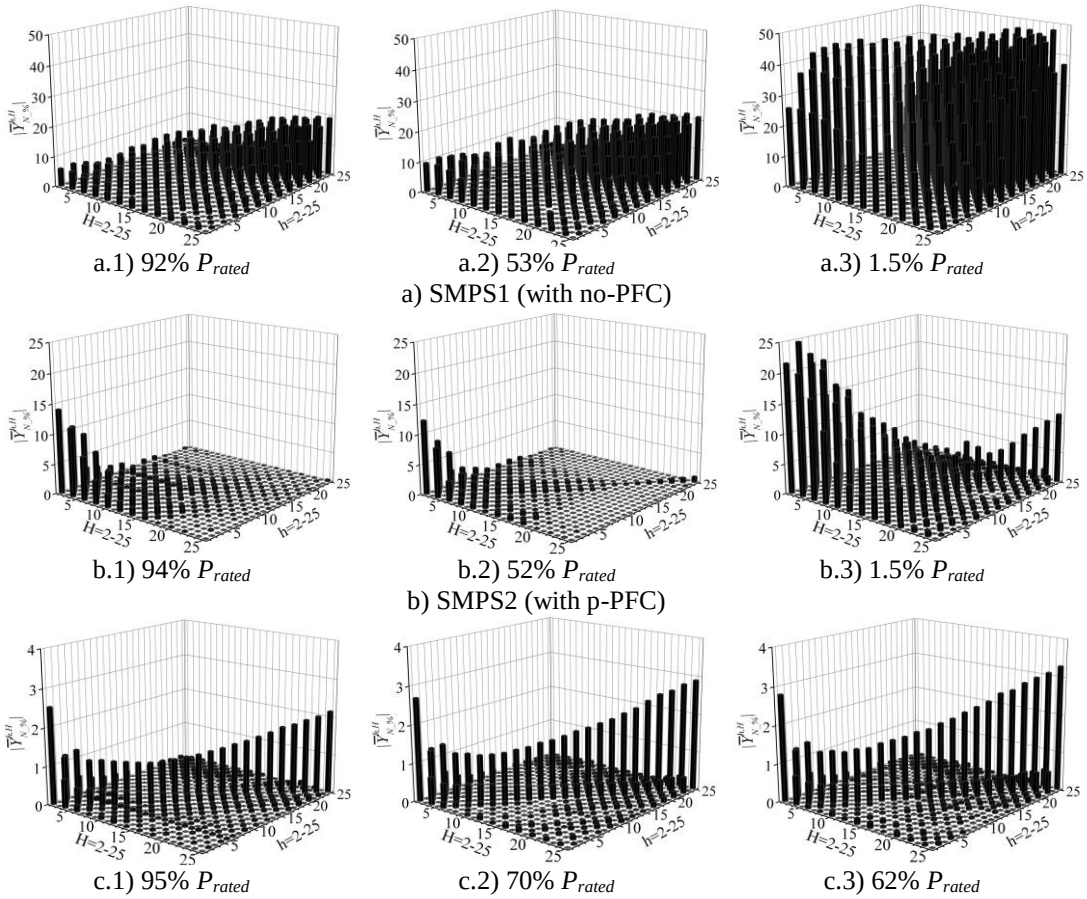
f) 10% $P_{rated}$, WF2 with magnitude of 1 p.u.

**Figure 4.16:** The comparison between simulated and measured time-domain input ac current waveform for SMPS4 operating under combinations of different powers and supply conditions.

## 4.4.2 Frequency-domain modelling

Based on the component-based modelling methodologies demonstrated on the three main SMPS types, it is noticed that the modelling approach will vary with the PFC

types. In addition, developing CBMs for SMPS' with a-PFC is more complex than for SMPS' with no-PFC and with p-PFC, due to the requirement of accurate representation of actual a-PFC circuits applied to the modelled device. Unlike component-based modelling, the frequency-domain modelling is a generalised approach for representing the harmonic emission characteristics of PE devices, regardless of their actual circuit topologies. By applying the frequency-domain modelling approaches discussed in Chapter 2 to the measurement data of individual harmonic tests given in Section 4.2, the FDMs for SMPS1-6 can be easily obtained. In this section, the development of FDMs for the three main SMPS types will be demonstrated on SMPS1, 2 and 4, with developed CHNMs fully validated. Specifically, the individual voltage and current harmonics are first extracted from the individual voltage harmonic tests for SMPS operating at specific power level (as given in Section 4.2.1), and then used as the input data for the development of CHNM. The obtained Norton harmonic admittance matrix in percentage, $HAM_{N\_\%}$ for tested SMPS' operating at different powers are illustrated in Figure 4.17.




a.1) 92% $P_{rated}$ a.2) 53% $P_{rated}$ a.3) 1.5% $P_{rated}$

a) SMPS1 (with no-PFC)

b.1) 94% $P_{rated}$ b.2) 52% $P_{rated}$ b.3) 1.5% $P_{rated}$

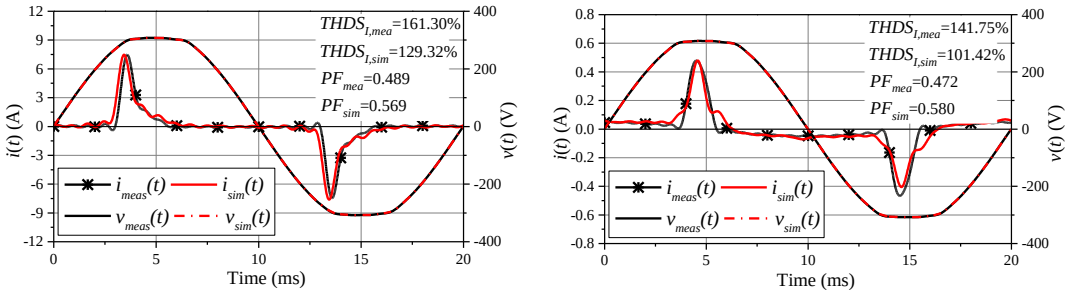
b) SMPS2 (with p-PFC)

c.1) 95% $P_{rated}$ c.2) 70% $P_{rated}$ c.3) 62% $P_{rated}$

c) SMPS4 (with a-PFC)

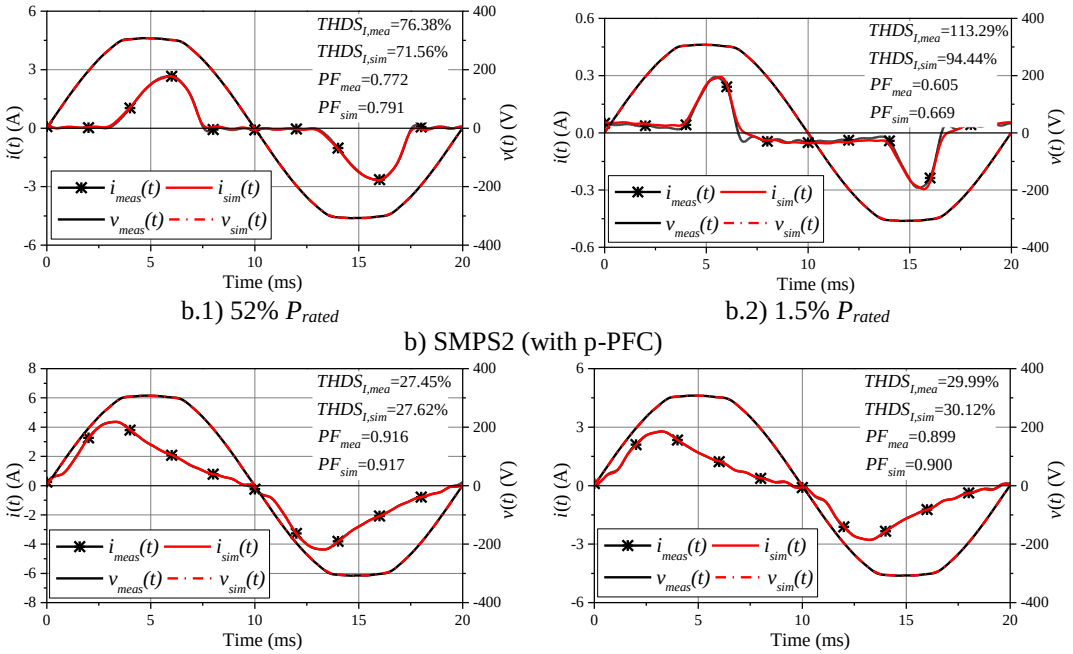
**Figure 4.17:** The obtained $|HAM_{N\_\%}|$ for tested SMPS' operating at different powers.

It is observed from Figure 4.17 that the power dependency of $HAM_{N\_\%}$ have different characteristics among the three main SMPS types. For SMPS with no-PFC (SMPS1), the individual current harmonics are not only determined by the individual voltage harmonics of the same order, but affected by the individual voltage harmonics of different orders as well. In addition, the voltage harmonic dependency of current harmonics will become stronger (i.e. larger element magnitudes of $|HAM_{N\_\%}|$) with the decrease of power. For SMPS' with p-PFC (SMPS2), it is noticed that the coupling between voltage and current harmonics of different orders is not as strong as SMPS' with no-PFC, especially when the operating power is high. For SMPS' with a-PFC (SMPS4), the individual current harmonics are mainly determined by the voltage harmonics the of same order (represented by the dominant diagonal elements of $|HAM_{N\_\%}|$), and the dependency becomes stronger with decrease of operating power. To validate the accuracy of the developed FDMs, the comparison between simulated and measured input ac current waveform under WF2 distorted supply voltage is illustrated in Figure 4.18 (the comparison under WF3 supply voltage waveform is given in the Appendix A). It is observed that the developed CHNMs can well represent the power dependency and supply voltage dependency of the ac current distortion characteristics of considered SMPS'. In addition, it is noticed that CHNMs achieve better accuracy for SMPS' with a-PFC than for SMPS' with no-PFC and with p-PFC. It is because the conventional FDMs assume linear relationships between voltage and current harmonics which might not be true for highly nonlinear PE devices (e.g. SMPS' with no-PFC and with p-PFC).




a.1) 53% $P_{rated}$ a.2) 1.5% $P_{rated}$

a) SMPS1 (with no-PFC)




b.1) 52% $P_{rated}$ b.2) 1.5% $P_{rated}$

b) SMPS2 (with p-PFC)

d.1) 95% $P_{rated}$ d.2) 62% $P_{rated}$

c) SMPS4 (with a-PFC)

**Figure 4.18:** The comparison between measured and simulated (CHNMs) input ac current waveforms for tested SMPS' operating at different powers with WF2 distorted supply voltage (magnitude equals 1 p.u.).

## 4.5 Operating Cycle Performance, Lost Periodicity and Waveform Distortion of SMPS'

This section focuses on investigating the performance of desktop SMPS' across their whole operating range, especially when lost periodicity happens. As mentioned in Section 4.3, two of the tested SMPS' with a-PFC circuits (SMPS4 and SMPS6) exhibit lost periodicity phenomenon when their operating powers drop to certain values, resulting in significant non-harmonic (subharmonic and interharmonic) current distortions and the deterioration of the performance (a substantial decrease of operational power factors and efficiency). Therefore, appropriate measurement and calculation procedures should be applied to evaluate the overall efficiency and PQ performance of SMPS' under specified operating cycles, which is the main focus in this section.

### 4.5.1 Introduction on current performance evaluation methods for SMPS'

The current recommendations for the performance evaluation of SMPS' generally suggest several test points for SMPS' operating at different power levels, in order to

take into account the power dependency of performance [8][12]. For example, the two main SMPS efficiency certifications requires the performance to be evaluated at four discrete operating powers (10, 20, 50 and 100 % of rated power, $P_{rated}$) [97][98], while [102] considers three discrete operating powers only (20, 50 and 100 % of $P_{rated}$). On the other hand, the regulations for the power factor in [102] and the harmonic limits in [42] only consider SMPS' operating at $P_{rated}$. It turns out that none of the above regulations or legislations take into account the actual time duration for SMPS' operating at each discrete power level, i.e. the SMPS operating cycle.

As another type of power-dependent modern PE devices, PVIs exhibit strong power variations and therefore, a "weighted efficiency" for the performance evaluation of PVIs is suggested in [109][110] based on the typical operating cycle of PVIs (i.e. the predetermined time durations at specified discrete operating powers). However, the operating cycle based weighting approach has not been applied to the SMPS performance evaluation, and might be of particular importance in terms of the efforts on reducing energy consumption in stand-by and low-power modes. For example, the efficiency evaluation in [111] takes into account the 'off', 'sleep' and 'idle' modes with corresponding operating powers typically below 10% $P_{rated}$ [2], for which a substantial performance deterioration is observed for SMPS' and other PE devices [8][10][12][13][93]. What's even worse is that the input ac currents of some of the tested SMPS' lose the 20 ms periodicity when the operating power is low or very low, highlighting the importance of selecting appropriate measurement and calculation procedures. Although a variety of approaches (e.g. [112][113][114]) have been proposed for evaluating PQ indices under nonstationary and aperiodic waveforms, they are not always compatible with the framework in [33].

In order to fully evaluate the power dependency of the overall efficiency and PQ performance of SMPS', a novel testing and evaluation methodology is proposed in this section with the entire operating cycle of SMPS' taken in account. The developed measurement framework extends the testing results given in Section 4.3 by taking into account the impact of test set-up uncertainties on the calculated indices, as well as providing further tests results and a more detailed analysis of the efficiency and PQ performance of the tested SMPS'. After that, the overall performance evaluation

methodology and its application will be presented on one tested SMPS combined with different operating cycle data, in order to demonstrate its applicability for both PMF and PDF operating cycle representations. The proposed methodology is fully compatible with the standard evaluation framework in [33], and can be easily applied for the other types of power-dependent PE devices with their own operating cycles.

### 4.5.2 Representation of PC-SMPS operating cycle

Traditionally, the specifications provided by manufacturers are for SMPS' operating at rated power, while their actual operating powers in practical applications may vary significantly (mostly between 20%-60% $P_{rated}$ [101][102]), depending on the specific running tasks. This is denoted as a "PC operating cycle", with an example of a desktop PC in a commercial office setting illustrated in Figure 4.8 [102]. Specifically, four discrete operating power levels (100%, 50%, 20% and 10% of $P_{rated}$) are considered in the example operating cycle, representing four general types of activities with different power demands, together with the time duration of each activity within one typical working day for a PC in a commercial office [9]. Potential power variations at the four discrete power levels are also indicated in Figure 4.19 as: a) 2%-10% $P_{rated}$, very low power mode (stand-by or idling), b) 10%-30% $P_{rated}$, low power mode (non-demanding text processing, internet browsing), c) 30%-70% $P_{rated}$, medium power mode (typical office tasks, read/write operations), and d) 70%- 100% $P_{rated}$, high power mode (streaming, complex simulations) [9].

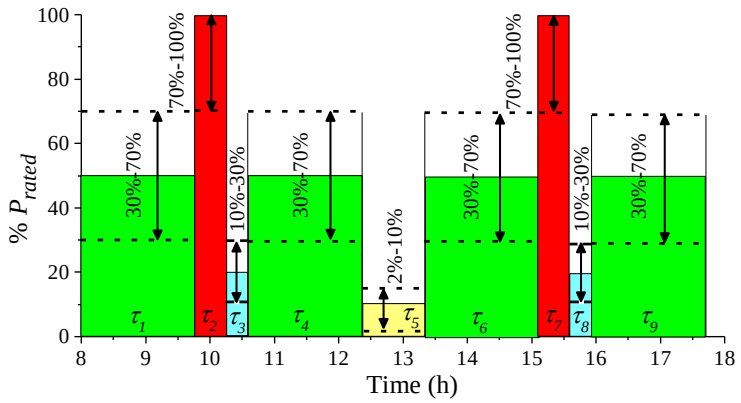



**Figure 4.19:** Example of a PC operating cycle in a commercial office setting; bar plot represents discrete values [102], dash lines indicate ranges [2].

As the operating cycle can be specified in PMF or PDF form, PMF in Figure 4.20 is converted to PDF by discretising the specified four power ranges into a series of

individual power levels from 2% to 100% $P_{rated}$ with a 1% $P_{rated}$ interval [9]. A normal distribution is assumed for the discrete powers within each power range with a coverage probability of 99.7% (three-sigma rule), and the sum of their PDF values equal to corresponding percentages of total duration, as illustrated in Figure 4.9 [9]. The final weighting coefficients (i.e. % of total PC working duration) of the four discrete powers (corresponding to PMF) or four operating ranges (corresponding to PDF) are tabulated in Table 4.5 [9]. It should be noted that the approach applied for the conversion from PMF to PDF is a simple normal distribution based discretisation, and any other suitable conversion methods can also be used, which is not the focus of the studies in this section. Although the actual PC operating cycles will vary within different PC users, the specification of different operating cycles (theoretical or measured) does not affect the generality of presented overall performance evaluation methodology.

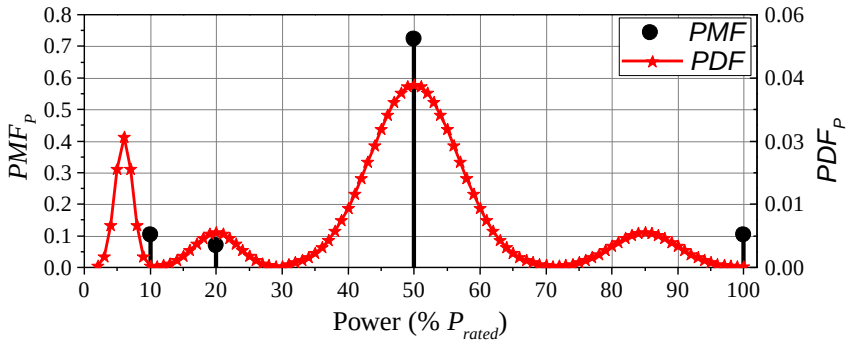



**Figure 4.20:** Probability mass and density functions for Figure 4.8.

**Table 4.5:** Example data for PC operating cycle used for analysis.

| PC Operating State | % of $P_{rated}$ | Duration (hours) | % of Total Duration | | |
|---|---|---|---|---|---|
| ***Four Discrete Powers*** | | | | | |
| **Full load** | 100 | 1 | 10.34% | | |
| **Typical load** | 50 | 7 | 72.41% | | |
| **Light load** | 20 | 0.67 | 6.91% | | |
| **Low load** | 10 | 1 | 10.34% | | |
| ***Ranges of Operating Powers*** | | | | ***Normal Distribution*** | |
| | | | | $\mu$ | $3\sigma$ |
| **High Power Range** | 70-100 | 1 | 10.34% | 85 | 15 |
| **Medium Power Range** | 30-70 | 7 | 72.41% | 50 | 20 |
| **Low Power Range** | 10-30 | 0.67 | 6.91% | 20 | 10 |
| **Very Low Power Range** | 2-10 | 1 | 10.34% | 6 | 4 |

### 4.5.3 Methodology for evaluating operating cycle performance and PQ indices

The efficiencies and PQ indices of PC-SMPS' analysed in this section include total efficiency $\eta$, fundamental efficiency $\eta_1$, true, displacement and distortion power factors *PF*, $PF_1$ and $PF_d$, total subgroup current harmonic distortion $THDS_I$ and total subgroup harmonic current *THCS* (for harmonic subgroup orders 2-40), total subgroup current interharmonic distortion $TIHDS_I$ and total subgroup interharmonic current *TIHCS*, (for interharmonic subgroup orders 0-40) and the dc component. The reference harmonic and interharmonic measurement methods and the related parameter selections (e.g. target uncertainty and window length) are taken from [33] and [36], with the metrics for distortion power calculation indicated in [37].

The operating cycle *T* is formed by a sequence of discrete intervals $\tau$. The operating power level $P^{(j)}$ at power demand *j* of a SMPS will have a cumulative duration $\tau^{(j)} = \sum_i \tau_i$, with $\tau_i$: $P = P^{(j)}$, so total duration of the operating cycle is: $T = \sum_{j=1}^{N_P} \tau^{(j)}$, where $N_P$ is total number of different operating powers, $P^{(j)}$. The generic frequency of occurrence of $N_P$ at different power levels $P^{(j)}$ is $f^{(j)} = \tau^{(j)}/ T$, and each $P^{(j)}$ will have cumulative duration $\tau^{(j)}$ and frequency of occurrence $f^{(j)}$ [9].

**Single operating power scenario**

For SMPS operating at given power $P(j)$ of the operating cycle, the total and fundamental efficiencies and related ac and dc side active powers can be calculated from (4.11-4.15) [9].

$$\eta_P^{(j)} = P_{dc}^{(j)} / P_{ac}^{(j)} \tag{4.11}$$

$$\eta_{P1}^{(j)} = P_{dc}^{(j)} / P_{ac,1}^{(j)} \tag{4.12}$$

$$P_{dc}^{(j)} = \frac{1}{N^{(j)}} \sum_{m=1}^{M} \sum_{n=1}^{N^{(j)}} v_{dc,m}(n) i_{dc,m}(n) \tag{4.13}$$

$$P_{ac}^{(j)} = \frac{1}{N^{(j)}} \sum_{n=1}^{N^{(j)}} v_{ac}(n) i_{ac}(n) \tag{4.14}$$

$$P_{ac,1}^{(j)} = \frac{1}{N^{(j)}} \sum_{n=1}^{N^{(j)}} v_{ac,1}(n) i_{ac,1}(n) \tag{4.15}$$

where: $v_{ac}$ and $i_{ac}$ are the sampled instantaneous ac voltage and current, with fundamental components represented by $v_{ac,1}$ and $i_{ac,1}$ repsecitvely, while $v_{dc,m}$, $i_{dc,m}$ are

the sampled instantaneous dc voltage and current at dc output level $m$ of total $M$ dc output levels, over the observation period $\tau^{(j)}$ constituted by $N^{(j)}$ samples equal to $\tau^{(j)} f_s$, where $f_s$ is the sampling frequency.

For the calculation of operating power factors and PQ indices, (4.16)-(4.18) are applied while for the calculation of waveform distortion indices, (4.19)-(4.22) are used.

$$PF^{(j)} = P_{ac}^{(j)} / S_{ac}^{(j)} \tag{4.16}$$

$$PF_1^{(j)} = P_{ac,1}^{(j)} / S_{ac,1}^{(j)} \tag{4.17}$$

$$PF_d^{(j)} = PF^{(j)} / PF_1^{(j)} \tag{4.18}$$

$$THDS_I^{(j)} = \frac{\sqrt{\sum_{h=2}^{40} I_{sg,h}^2}}{I_{sg,1}} \tag{4.19}$$

$$THCS^{(j)} = \sqrt{\sum_{h=2}^{40} I_{sg,h}^2} \tag{4.20}$$

$$TIHDS_I^{(j)} = \frac{\sqrt{\sum_{h=0}^{40} I_{isg,h}^2}}{I_{sg,1}} \tag{4.21}$$

$$TIHCS^{(j)} = \sqrt{\sum_{h=0}^{40} I_{isg,h}^2} \tag{4.22}$$

where: $S_{ac}^{(j)} = V_{ac}^{(j)} I_{ac}^{(j)}$, $V_{ac}^{(j)}$ and $I_{ac}^{(j)}$ represent the rms values of the input ac voltage and ac current respectively, and $S_{ac,1}^{(j)} = V_{ac,1}^{(j)} I_{ac,1}^{(j)}$, represent the corresponding fundamental components; $I_{sg,h}$ and $I_{isg,h}$ are harmonic and interharmonic subgroups respectively according to [33].

**Entire operating cycle scenario**

For any given PC operating cycle, indices for the single operating power $P^{(j)}$ defined by (4.11-4.22) can be associated with the corresponding cumulative duration $\tau^{(j)}$ and frequency of occurrence $f^{(j)}$. It is also useful to apply "energy efficiency" for the efficiency calculation as defined in (4.23-4.24).

$$\eta_E = \frac{\sum_{j=1}^{N_P} \left(P_{dc}^{(j)}\right).\tau^{(j)}}{\sum_{j=1}^{N_P} P_{ac}^{(j)} \tau^{(j)}} = \frac{E_{dc}}{E_{ac}} \tag{4.23}$$

$$\eta_{E1} = \frac{\sum_{j=1}^{N_P}\left(P_{dc}^{(j)}\right)\cdot\tau^{(j)}}{\sum_{j=1}^{N_P} P_{ac,1}^{(j)}\tau^{(j)}} = \frac{E_{dc}}{E_{ac,1}} \tag{4.24}$$

where: $E_{(.)}$ represents the total energy consumed at power $P_{(.)}$ with a duration of $\tau_{(.)}$ by a customer using PC running ranges of specific activities and tasks.

In terms of the calculation of the operating power factors, mean quantities can be applied [9]. [Note: Energy billing in some countries, e.g. Italy, applies (4.24), while standard [37] recommends (4.25)-(4.27)]:

$$\overline{PF} = \frac{\sum_{j=1}^{N_P} P_{ac}^{(j)}\tau^{(j)}}{\sum_{j=1}^{N_P} S_{ac}^{(j)}\tau^{(j)}} \tag{4.25}$$

$$\overline{PF}_1 = \frac{\sum_{j=1}^{N_P} P_{ac}^{(j)}\tau^{(j)}}{\sum_{j=1}^{N_P} S_{ac,1}^{(j)}\tau^{(j)}} \tag{4.26}$$

$$\overline{PF}_d = \frac{\overline{PF}}{\overline{PF_1}} \tag{4.27}$$

The harmonic magnitude, $I_h^{(j)}$, is applied to represent harmonics at each operating power $P^{(j)}$. To show the variations of harmonic and interhamronic currents for SMPS' operating at different powers $P^{(J)}$, the obtained harmonic and interharmonic currents are expressed in the form of two matroids-[$P^{(J)}$, $h$, $I_{sg,h}$] and [$P^{(J)}$, $h$, $I_{isg,h}$] (the dimension for each matroid is $N_P$ x $N_h$ x $N_{Ih}$, with $N_P$, $N_h$ and $N_{Ih}$ representing the number of operating power levels, the number of harmonic or interharmonic orders and the number of discrete consecutive classes in which measured values of currents are discretized) respectively [9]. Therefore, 2x41 PMFs are obtained for harmonic and interharmonic subgroup, including dc and fundamental components, and from which, the relevant statistical characteristics (maximum, mean, mode and 95$^{th}$ percentile values) for each PMF can be extracted by using (4.28)-(4.31) respectively. The obtained statistical values can be directly applied for evaluating the overall efficiencies and PQ performance of a PE device over its entire operating cycle (see (4.32) and (4.33) in Section 4.5.6).

$$\hat{I}_{sg,h} = \max_j I_{sg,h}^{(j)}, \tag{4.28}$$

$$\mu_{I_{sg,h}} = \sum_{j=1}^{N_P} I_{sg,h}^{(j)} \cdot f^{(j)}, \tag{4.29}$$

$$v_{I_{sg,h}} = I_{sg,h}^{(j^*)}: j^* \rightarrow \max_j f^{(j)}, \tag{4.30}$$

$$I_{sg,h,95\%} = I_{sg,h}^{(j^*)}: j^* \rightarrow \sum_j f^{(j)} \geq 95\%., \tag{4.31}$$

### 4.5.4 Testing and measurement framework

**Test set-up**

The test set-up is same with the one illustrated in Figure 4.2, with the dc operating power (at +12 V and +5 V dc outputs) of SMPS' gradually adjusted from 1% $P_{rated}$ to 100% $P_{rated}$. Although continuous fluctuation may be seen for the dc power output in practical applications, the dc power was controlled with negligible variation during the tests. All recordings are synchronized by the data acquisition system with a sampling rate of 1 MSa/s.

**Supply voltage waveforms applied in tests**

In the tests, there different supply voltage waveforms (denoted as WF1, WF2 and WF3) are applied in the tests, with WF1 referring to the ideally sinusoidal supply voltage (as a reference), and WF2 and WF3 representing two distorted supply voltage waveforms found in LV networks, as illustrated in Figure 4.21.

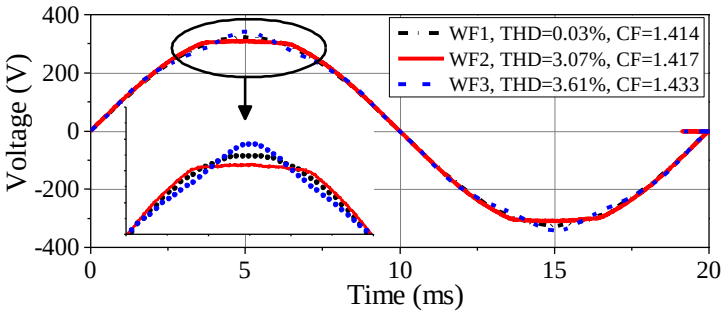



**Figure 4.21:** The three voltage waveforms used in tests (CF denotes crest factor).

**Evaluation of measurement accuracy and uncertainties**

In order to evaluate the measurement accuracy and uncertainties, the approach proposed in [9][10] was applied. Specifically, the accuracy and uncertainty evaluation begins with the manufacturer standard uncertainties of the test instruments as tabulated in Table 4.6. By assuming the errors for each instrument are uniformly distributed, the Monte Carlo (MC) trials can be performed to investigate the error distribution characteristics of the calculated indices.

**Table 4.6:** Standard uncertainties (manufacturers' datasheets) [9].

| Measurement | Equipment | $E_{reading}$ | $E_{range}$ |
|---|---|---|---|
| $v_{ac}$ | Differential probe | ±2% | / |
| $i_{ac}$ | Current probe | ±0.5% | / |
| $v_{dc\text{-}12}$ | Differential probe | ±2% | / |
| $i_{dc\text{-}12}$ | Current probe | ±1% | ±2mA |
| $v_{dc\text{-}5}$ | Differential probe | ±2% | / |
| $i_{dc\text{-}5}$ | Current probe | ±1% | ±2mA |
| **Data acquisition** | ADC system | ±0.03% | dc: ±0.02%±2 mV<br>ac: ±0.02% |
| $E_{reading}$, $E_{range}$: reading and range uncertainty; ADC system range: ±100 V. | | | |

For investigating the impact of measurement uncertainty on the error distribution characteristics of the calculated indices, reference sinusoidal input ac voltage and current waveforms are used ($v_{ac}$ and $i_{ac}$), with their rms magnitudes equal to 230 V and 2.182 A respectively, corresponding to a reference power of $P_{ac,ref}$=500 W. In addition, the current waveform lags five degrees ($5^o$) with respect to the voltage. The reference dc voltage and current values for $v_{dc\text{-}12}$, $v_{dc\text{-}5}$, $i_{dc\text{-}12}$, $i_{dc\text{-}5}$ are set to be 12 V, 5 V, 25 A, and 20 A, respectively, corresponding to the total reference dc power of $P_{dc,ref}$ = 400 W. The reference efficiency is selected at 80%, i.e. the efficiency for SMPS operating at $P_{rated}$. Apart from the operating power at $P_{rated}$, the error distribution characteristics were evaluated at 100%, 70%, 50%, 30%, 10% and 2% of $P_{rated}$, with where the reference values for the ac and dc side voltage and current waveforms scaled-down from the corresponding values at 100% of $P_{rated}$ (assuming the efficiency is maintained constant at 80%). By performing 50000 MC trials, histograms of the ac power deviation ($\Delta P_{ac}/P_{ac,ref}$), dc power deviation ($\Delta P_{dc}/P_{dc,ref}$), efficiency and fundamental efficiency deviation ($\Delta\eta/\eta_{ref}$ and $\Delta\eta_1/\eta_{1,ref}$ respectively) can be obtained, with the results at $P_{rated}$ illustrated in Figure 4.22 [9].

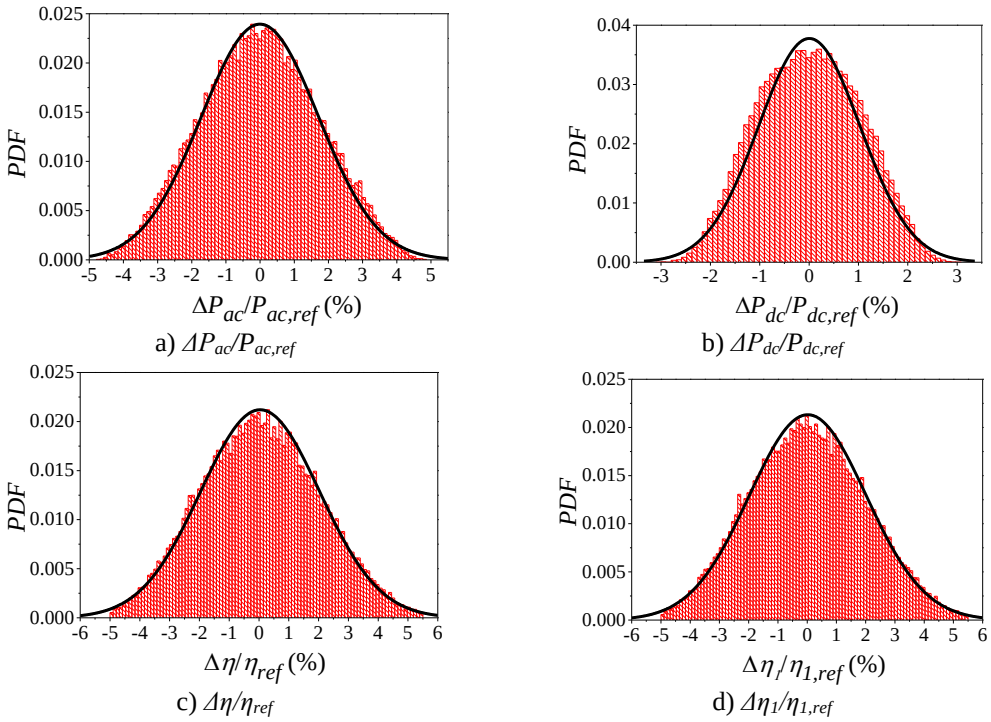



**Figure 4.22:** Histogram and fitted normal distributions for: ac power deviation, dc power deviation, efficiency and fundamental efficiency deviation, for SMPS with $P_{dc,ref}$ = 400 W.

The complete expanded uncertainty values (coverage factor 3) for assessing the measurement precision at different power levels are tabulated in Table 4.7. For the accuracy, the cumulative effect of the available measurement equipment uncertainties are comparable with the requirements from [36], and are, therefore, considered acceptable, particularly as the probabilities of operation at lower powers in the considered PC-SMPS operating cycle are low, so a larger uncertainty observed for SMPS operating at these powers does not affect the presented results.

**Table 4.7:** Expanded uncertainties (coverage factor 3) at different power levels.

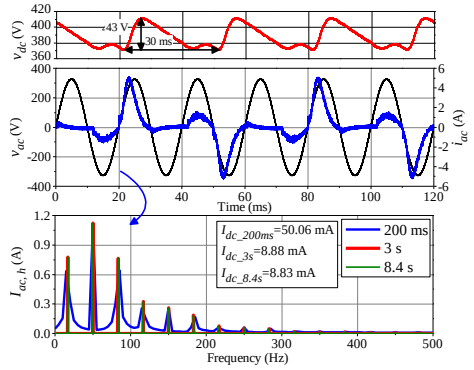
| % $P_{rated}$ | Expanded Uncertainty in % | | | |
|---|---|---|---|---|
| | $\Delta P_{ac}/P_{ac,ref}$ (%) | $\Delta P_{dc}/P_{dc,ref}$ (%) | $\Delta\eta/\eta_{ref}$ (%) | $\Delta\eta_1/\eta_{1,ref}$ (%) |
| ***70-100*** | [5.41, 5.15] | [3.11, 3.09] | [6.25, 5.99] | [6.25, 6.00] |
| ***50-70*** | [5.86, 5.41] | [3.10, 3.11] | [6.62, 6.25] | [6.62, 6.25] |
| ***30-50*** | [7.23, 5.86] | [3.15, 3.10] | [7.90, 6.62] | [7.91, 6.62] |
| ***10-30*** | [16.66, 7.23] | [3.40, 3.15] | [17.13, 7.90] | [17.13, 7.91] |
| ***2-10*** | [79.90, 16.66] | [7.07, 3.40] | [95.14, 17.13] | [95.16, 17.13] |

## 4.5.5 Measurement results

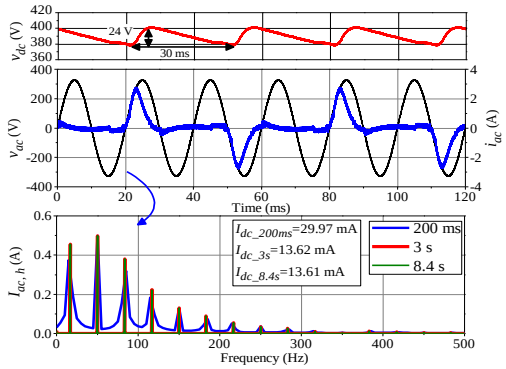
In this section, the lost periodicity phenomenon of SMPS4 ($P_{rated}$=400 W) and SMPS6 ($P_{rated}$=350 W) will be fully discussed.

**Lost periodicity in PC-SMPS applications**

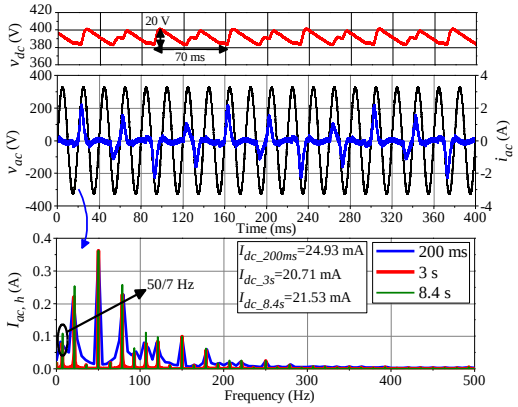
Standards [33][36] requires that the time window applied for (inter)harmonic evaluation should be 10 fundamental periods in 50 Hz supply systems and 12 periods in 60 Hz supply systems. When lost periodicity happens on SMPS4 and SMPS6, the obtained current (inter)harmonic spectra for 200 ms window length are compared with the results for 3 s (recommended in [36]) and 8.4 s windows (suggested in this section) are illustrated in Figure 4.23 and Figure 4.24. The results for 3 s and 8.4 s windows are obtained from the squared average values 15 and 42 consecutive individual 200 ms windows, according to [36]. The main reason for selecting 8.4 s window length is that it corresponds to 420 fundamental periods in 50 Hz supply systems (504 periods in 60 Hz supply systems), which allows for integer factorization of 420 and 504 periods by most of the pairs from the series {1, 2, 3, 4, 5, 6, 7} and hence ensure correct results being obtained for all combinations of voltage and current periods from that series.



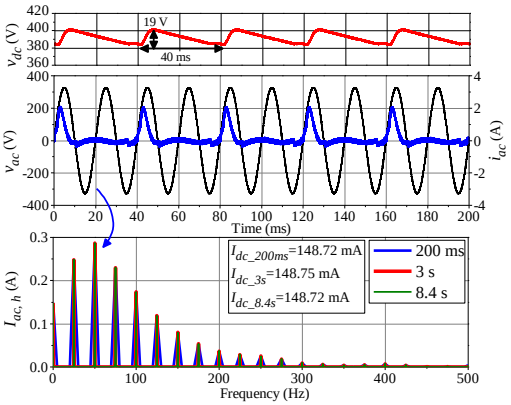

a) 50% $P_{rated}$ (lost periodicity: triple-period, or period-3 current)




b) 20% $P_{rated}$ (lost periodicity: triple-period, or period-3 current)

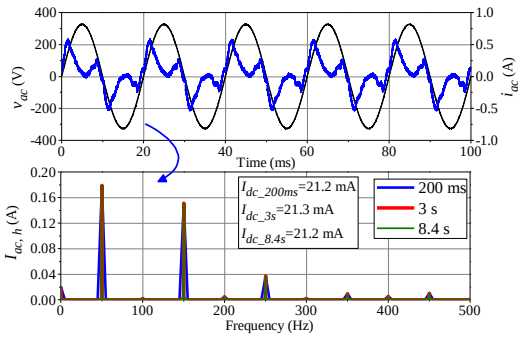



c) 14% $P_{rated}$ (lost periodicity: septuple-period, or period-7 current)

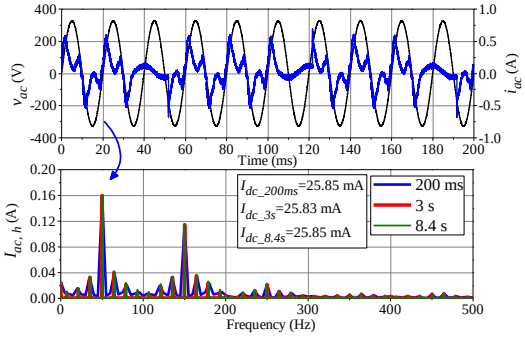



d) 10% $P_{rated}$ (lost periodicity: double-period, or period-2 current)

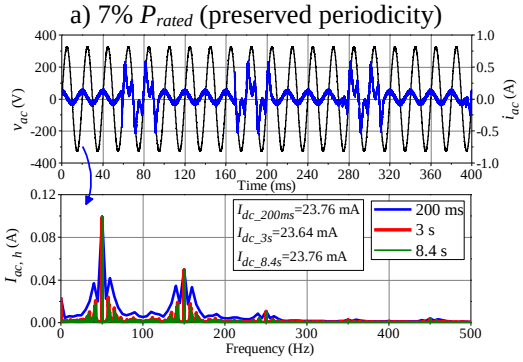
**Figure 4.23:** The illustration of the lost periodicity phenomena, SMPS4.




a) 7% $P_{rated}$ (preserved periodicity)




b) 6% $P_{rated}$ (lost periodicity: period-7 current)




c) 2% $P_{rated}$ (lost periodicity: quasi-aperiodic current)

**Figure 4.24:** The illustration of the lost periodicity phenomena, SMPS6.

**Discussion of lost periodicity results**

When the operating power of SMPS4 is above 50% $P_{rated}$, the input ac current, $i_{ac}$, can maintain the same 20 ms period with the input ac voltage, $v_{ac}$, while the dc-link voltage is characterised by a 100 Hz voltage ripple (corresponding to a 10 ms period). However, when the operating power of SMPS4 starts to drop below 50% $P_{rated}$, the lost periodicity phenomenon occurs, which is represented by the change of $i_{ac}$ period from 20 ms to 60 ms (period-tripling, or period-3), as shown in Figure 4.23(a) and 4.23(b), while the discharging time of the dc link voltage also increases, resulting a dc-link voltage period of 30 ms. When period-3 occurs, it can be expected that the use of 200 ms window length will result in three possible different current waveform samples within 10 consecutive periods of 200 ms window, and will produce an error in 50 Hz supply systems. However, this is not an issue for the 60 Hz systems, as the $v_{ac}$ has period of 50/3 ms and period-tripling of $i_{ac}$ corresponds to the period of 50 ms, i.e. in exactly 12 voltage and 4 current periods in 200 ms window.

The period septupling (period-7) is observed for SMPS4 when its operating power drops to around 14% $P_{rated}$ as illustrated in Figure 4.23(c), where the discharging time of $v_{dc}$ further increases and is featured with a period of 70 ms. In addition, it is noticed

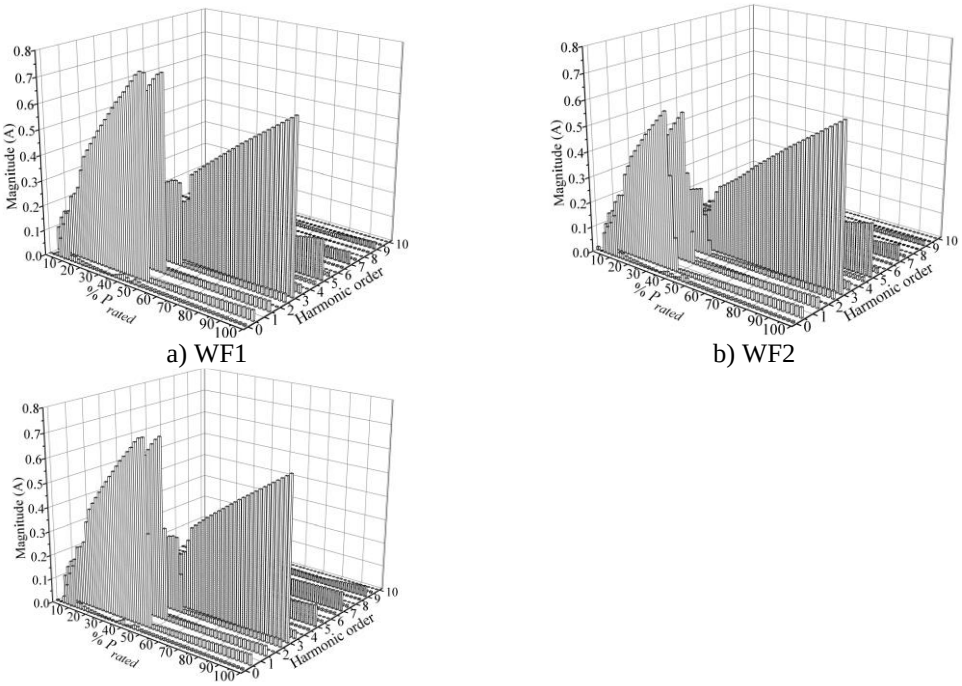
that the 50/7 component (marked with a circle in Figure 4.23(c)) cannot be accurately captured by the 200 ms and 3 s windows, which justified the use of 8.4 s window. If the operating power of SMPS4 further drops to around 10% $P_{rated}$, the period doubling (or period-2) occurs, with the period of $i_{ac}$ and $v_{dc}$ changed to 40 ms, as demonstrated in Figure 4.23(d).

When SMPS4 is operating at very low power mode (e.g. below 3% $P_{rated}$), a completely lost periodicity of input ac current ("chaotic operation" [13]) happens. For the dc current component, it turns out that a very high dc component (around 150 mA) is observed when period-doubling happens (Figure 4.23(d)), which is of concern, as it result in serious issues like transformer saturation, or malfunction of protection. In terms of SMPS6, its $i_{ac}$ becomes heavily distorted when the operating power drops to around 7% $P_{rated}$ (Figure 4.24(a)), followed by the occurrence of period-septupling if the power further drops (Figure 4.24(b)). Finally, a quasi-aperiodic operation happens for SMPS6 operating at very low power (Figure 4.24(c)).

As demonstrated in Figure 4.23 and 4.24, significant subharmonic, interharmonic and dc component emission are observed when lost periodicity happens, which are not fully captured with a 200 ms window. In addition, it is observed from Figure 4.23(a) and 4.23(b) that the period-tripling results in a strong emission of 50/3 Hz subharmonic and its odd multiple interharmonics (250/3 Hz, 350/3 Hz,...), while the period-doubling brings about the 50/2 Hz subharmonic and its odd multiple interharmonics (150/2 Hz, 250/3 Hz,…). In terms of the period-septupling shown in Figure 4.23(c) and 4.24(b), a 50/7 subharmonic is observed, together with its odd multiple sub/inter harmonics.

**Evaluation of SMPS performance for sinusoidal and distorted voltage supply**

Figure 4.25 further evaluates the impact of lost periodicity on the dc current component, subgroup current subharmonics, interharmonics and harmonics (up to the $10^{th}$ order) for SMPS4 operating under the whole power range combined with three different supply voltage waveforms WF1-3. The 8.4 s window length is used here to avoid potential problems with spectral leakage especially when lost periodicity happens. It is observed from Figure 4.25 that dc component, subharmonics and $2^{nd}$ harmonic significantly increase and become the dominant components in the spectrum, when the operating power reduces to around 50% of $P_{rated}$.




a) WF1 b) WF2

c) WF3

**Figure 4.25:** The dc component, current harmonic, subharrmonic and interharmonic magnitudes for SMPS4 (8.4 s window).

When the operating power is between 50% and 100% $P_{rated}$, the 3rd and 5th harmonics are the dominant components, which gradually decrease with reducing power. Moreover, a distinctive step change in waveform distortion is observed when the operating power is at 50% $P_{rated}$ and lost periodicity starts to occur. It is also noticed that the supply voltage distortions (WF2 and WF3) have only a small impact on the dc component, subharmonic, inerharmonic and harmonic emission of SMPS4, as illustrated in Figure 4.25(b) and 4.25(c).

**Evaluation of SMPS operating cycle performance**

To investigate if the 200 ms window suggested in [33] can be applied for correct calculation and evaluation of SMPS' performance, the calculated efficiencies, true power factor, and harmonic distortion indices for SMPS4 operating at the whole power range with WF1-3 by using the three different window lengths are given in Figure 4.26. The combined standard uncertainty bounds are represented by the error bars in Figure 4.26(a) and 4.26(b), but are not shown in Figures 4.26(c)-4.26(f) as they are very small (less than 1%).

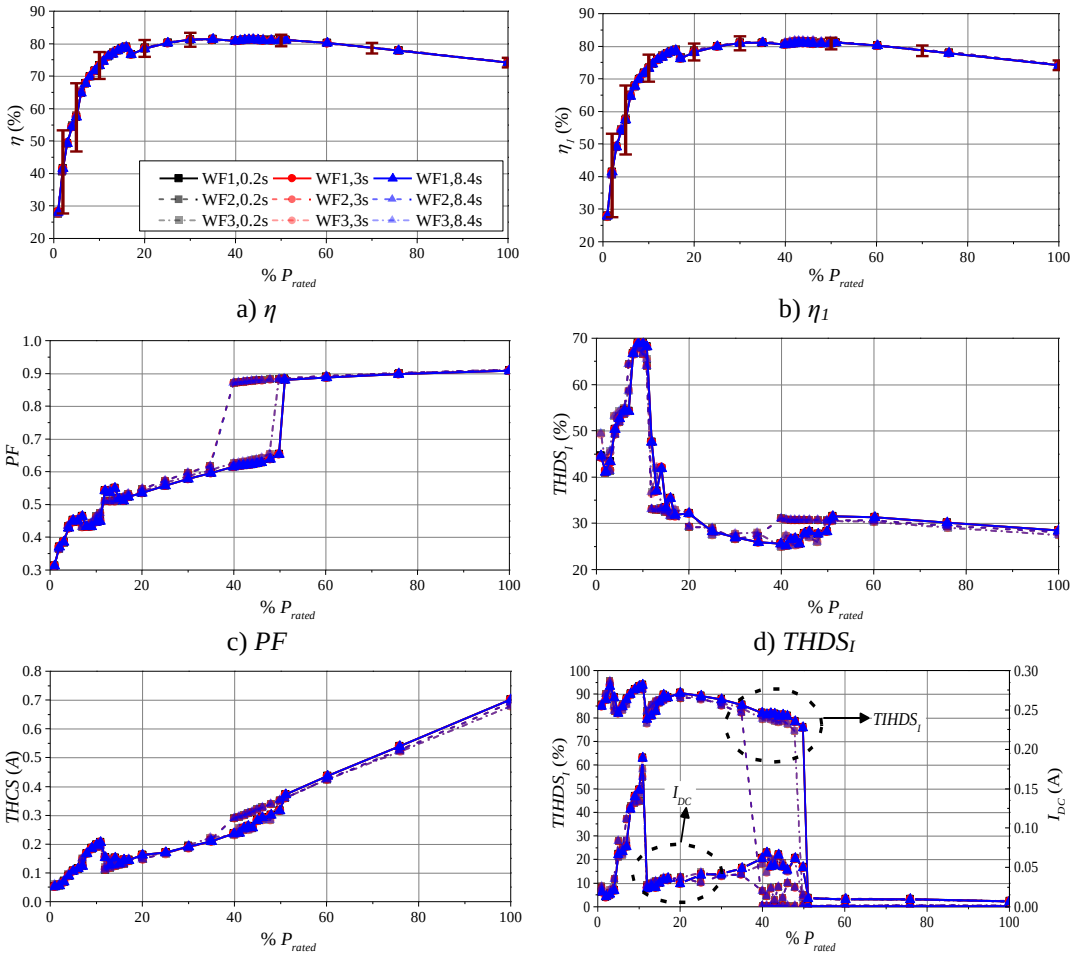



**Figure 4.26:** Performance indicators and PQ indices with standard uncertainty bounds obtained from 200 ms, 3 s and 8.4 s time windows (SMPS4).

As shown in Figure 4.26, a step change is seen for *PF*, $TIHDS_I$ and $I_{DC}$ values at around 50% $P_{rated}$, together with a rapid decrease of $\eta$ and $\eta_1$ and increase of $THDS_I$ values when the operating power is below 20% $P_{rated}$, implying that the SMPS performance evaluation based on several fixed operating powers may not be able to accurately represent the device's actual performance over its entire operating cycle. The minimum and maximum percentage differences among individual 200 ms and 3 s windows with respect to the results for 8.4 s window are listed in Table 4.8 and from which significant differences are observed for 200 ms window with reduced differences for 2 s window, demonstrating the importance of selecting a suitable window length.

**Table 4.8:** Difference (in %) of 200 ms and 3s from 8.4 s window.

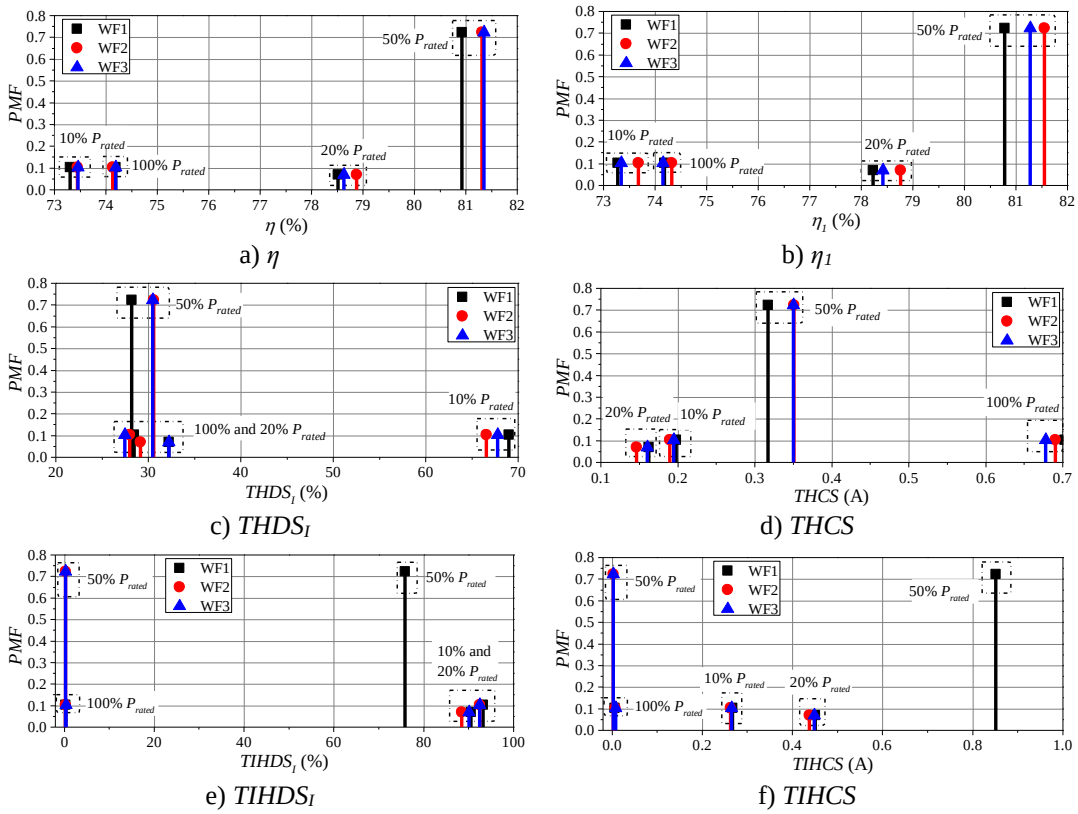
| Window | $\eta$ | $\eta_1$ | $PF$ | $PF_1$ | $PF_d$ | $THDS_I$ | $THCS$ | $TIHDS_I$ | $TIHCS$ | $I_{dc}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| **200ms** | -20 | -21 | -17 | -10 | -10 | -45 | -47 | -27 | -27 | $-1E^2$ |
| | 25 | 22 | 17 | 11 | 15 | 46 | 57 | 32 | 31 | $2E^3$ |
| **3s** | -1.0 | -1.3 | -2.5 | -0.9 | -1.9 | -4.6 | -5.3 | -3.8 | -3.7 | -9.2 |
| | 2.0 | 1.8 | 2.7 | 0.6 | 2.2 | 4.8 | 5.5 | 4.0 | 3.9 | $1E^3$ |

### 4.5.6 Results for SMPS operating cycle performance

Although the results for SMPS4 performance in Figure 4.26 provide detailed information on the changes of efficiencies and PQ performance over the entire power range, they are not capable of indicating the overall operating cycle performance. For that purpose, the results on efficiencies and PQ performance for SMPS at specific operating power levels can be combined with the corresponding frequency of occurrence data. In this section, the PMF and PDF data in Figure 4.20 will be applied to demonstrate the proposed overall operating cycle performance evaluation methodology.

**Operating cycle performance: discrete operating powers and normally distributed ranges of operating powers**

The PMFs and PDFs for SMPS4 operating cycle based efficiencies and PQ performance under WF1-3 are shown in Figure 4.27 and Figure 4.28. In terms of the operating cycle performance under discrete operating powers in Figure 4.27, it is observed that highest $\eta$ and $\eta_1$ values are achieved for SMPS operating at 50% $P_{rated}$, with lower $\eta$ and $\eta_1$ at 10% and 100% $P_{rated}$. $THDS_I$ has very close values at 20%, 50% and 100% $P_{rated}$, with highest value achieved at 10% $P_{rated}$, while $THCS$ values generally decrease with reducing power, except at very low power, where $THCS$ slightly increases. $TIHDS_I$ and $TIHCS$ have close to zero values until lost periodicity happens, when they increase significantly. The highest probability for all indices at 50% $P_{rated}$, corresponding to PMFs in Figure 4.20. In addition, the efficiencies and PQ performance of SMPS4 are insensitive to the considered supply voltage distortions (WF2 and WF3).

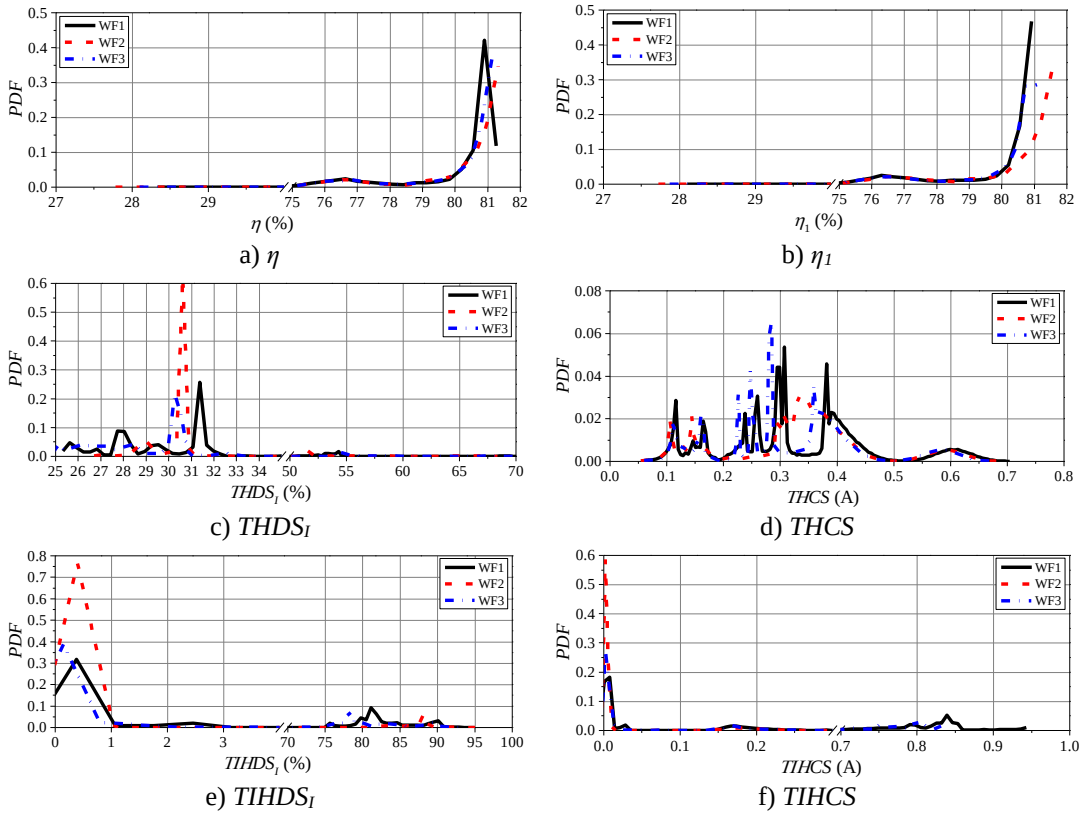



a) $\eta$ b) $\eta_1$

c) $THDS_I$ d) $THCS$

e) $TIHDS_I$ f) $TIHCS$

**Figure 4.27:** Operating cycle performance of SMPS4 for WF1-3 and for operating cycle represented with discrete powers (PMF) in Figure 4.20.




a) $\eta$ b) $\eta_1$

c) $THDS_I$ d) $THCS$

e) $TIHDS_I$ f) $TIHCS$

**Figure 4.28:** Operating cycle performance of SMPS4 for WF1-3 and for operating cycle represented with ranges of normally distributed powers (PDF) in Figure 4.20.

For the operating cycle performance under normally distributed operating powers in Figure 4.28, it turns out that $\eta$ and $\eta_1$ generally increase with increasing power, with an almost linear decrease seen for *THCS* with reducing power. $THDS_I$ is relatively constant at high powers and apparently increase at very lower powers. For $TIHDS_I$ and *TIHCS*, a step change is seen for them when lost periodicity happens. Same with Figure 4.27, highest probability for all indices is achieved at around 50% $P_{rated}$.

**Operating cycle performance: weighted indices**

According to the PMFs and PDFs of the two operating cycles specified in Figure 4.20, and the indices values calculated using 8.4 window at different power levels in Figure 4.26, the overall efficiencies and PQ indices are calculated and tabulated in Table 4.9, with the calculation procedure illustrated for the weighted true power factor ($PF_\mu$) in (4.32) and (4.33) for discrete operating powers and operating cycle with the ranges of normally distributed powers, respectively. $k_{Pk}$ refers to the frequency of occurrence for four discrete powers in (4.32) and refer to the frequency of occurrence for normally distributed power ranges in (4.33) (derived from the PDF curve in Figure 4.20). It should be noted that (4.32) and (4.33) are equivalent to (4.29).

$$PF_\mu = k_{P10}PF_{P10} + k_{P20}PF_{P20} + k_{P50}PF_{P50} + k_{P100}PF_{P100} \quad (4.32)$$

$$PF_\mu = \sum_{k=1}^{100} k_{Pk}PF_{Pk} \quad (4.33)$$

where: $k_{P10}$, $k_{P20}$, $k_{P50}$ and $k_{P100}$ are the weighting coefficients from Table 4.2, and $PF_{P10}$, $PF_{P20}$, $PF_{P50}$, and $PF_{P100}$ are the measured *PF* at the four corresponding operating powers. $k_{Pk}$ and $PF_{Pk}$ are the weighting coefficients and measured *PF* under normally distributed power ranges.

**Table 4.9:** Operating cycle based efficiencies and PQ performance indicators for SMPS4.

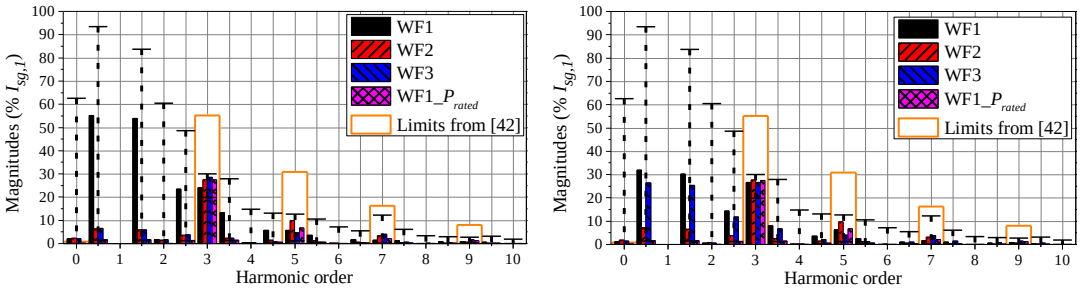
| | $I_{dc,\mu}$ (mA) | $\eta_\mu$ (%) | $\eta_1$, (%) | $PF_w$ | $PF_{1,\mu}$ | $PF_{d,\mu}$ | $THDS_{I,\mu}$ (%) | $THCS_\mu$ (A) | $TSHDS_{I,\mu}$ (%) | $TSHCS_\mu$ (mA) | $TIHDS_{I,\mu}$ (%) | $TIHCS_\mu$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***Discrete Operating Powers*** | | | | | | | | | | | | |
| **WF1** | 54 | 79 | 79 | 0.65 | 0.94 | 0.69 | 33 | 0.33 | 64 | 607 | 71 | 680 |
| **WF2** | 28 | 80 | 80 | 0.82 | 0.92 | 0.89 | 33 | 0.36 | 15 | 55 | 16 | 60 |
| **WF3** | 26 | 80 | 80 | 0.82 | 0.92 | 0.89 | 34 | 0.36 | 15 | 57 | 16 | 61 |
| ***Ranges of Normally Distributed Operating Powers*** | | | | | | | | | | | | |
| **WF1** | 35 | 78 | 78 | 0.72 | 0.92 | 0.78 | 32 | 0.33 | 42 | 333 | 46 | 360 |
| **WF2** | 24 | 78 | 79 | 0.81 | 0.91 | 0.88 | 33 | 0.34 | 16 | 61 | 17 | 67 |
| **WF3** | 32 | 78 | 78 | 0.74 | 0.92 | 0.80 | 32 | 0.32 | 37 | 276 | 40 | 297 |

By comparing the weighted efficiencies and PQ performance indices in Table 4.9 with the corresponding indices values at rated power given in Table 4.10, noticeable differences are observed for most of the indices, especially the power factors, the dc current and interharmonic/subharmonic emission. In addition, very close values are achieved for the two operating cycles (Table 4.9).

**Table 4.10:** Efficiencies and PQ performance indicators of SMPS4 at $P_{rated}$.

| WF | $I_{dc}$ (mA) | $\eta$ (%) | $\eta_1$, (%) | $PF$ | $PF_1$ | $PF_d$ | $THDS_I$ (%) | $THCS$ (A) | $TSHDS_I$ (%) | $TSHCS$ (mA) | $TIHDS_I$ (%) | $TIHCS$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **1** | 7.1 | 74 | 74 | 0.91 | 0.95 | 0.96 | 29 | 0.70 | 0.06 | 1.6 | 0.26 | 6.3 |
| **2** | 6.6 | 74 | 74 | 0.91 | 0.95 | 0.96 | 28 | 0.69 | 0.07 | 1.6 | 0.29 | 7.1 |
| **3** | 6.7 | 74 | 74 | 0.91 | 0.95 | 0.96 | 27 | 0.68 | 0.08 | 1.9 | 0.29 | 7.1 |

Finally, Figure 4.29 compares the operating cycle based magnitudes of current harmonic spectra of SMPS4 with the corresponding values for SMPS4 operating at $P_{rated}$, and with the maximum and minimum values observed from all test points (i.e. all operating powers and voltage waveforms). Again, clearly visible differences are observed and weighted subharmonic and interharmonic magnitudes are much higher than the corresponding values at $P_{rated}$. The existing limits indicated in [42] are also indicated in Figure 4.29. All the above findings suggest that the operating cycle based performance evaluation methodology can better represent the actual or expected SMPS performance than the performance indicators specified at $P_{rated}$, and could be considered as a part of standard device assessment procedures.




a) discrete operating powers

b) ranges of normally distributed operating powers

**Figure 4.29:** The weighted current harmonic spectra of SMPS4 for WF1-3, where the whisker plot shows the range of values measured during the tests.

## 4.6 Chapter conclusions

Based on the comprehensive laboratory testing results of the six PC-SMPS' with different PFC types, it turns out that although SMPS' with a-PFC normally have better PQ performance than SMPS' with no-PFC and with p-PFC when operating at high power mode, their harmonic, interharmonic and subharmonic current emission may significantly increase at low power operating mode if a-PFC circuit is not properly designed. In addition, two of the tested SMPS' cannot maintain the 20 ms periodicity of the input ac current when they are operating at low or very powers, resulting in a significant increase of PC-SMPS' current waveform distortion, at harmonic and interharmonic frequencies, and a substantial decrease of efficiency and power factors. It is also pointed out that applying the standardised 200 ms time window when lost periodicity occurs, can result in inaccurate calculation of indices, and the time window length should be adjusted based on the periodicity of the input ac current of SMPS' at different powers.

Regarding the harmonic modelling of SMPS', both CBMs and FDMs are developed for the three main SMPS types by using SMPS1, SMPS2 and SMPS4 as example. It turns out that the developed models can accurately represent the harmonic characteristics of SMPS' operating under different powers and supply conditions.

To take into account the impact of operating powers on the PQ performance evaluation of SMPS', the operating cycle based performance evaluation methodology is proposed and demonstrated on selected SMPS'. The proposed approach can be easily applied for the analysis of other types of PE devices that operate with variable powers. For example, a similar case of lost periodicity phenomena has been reported for PV inverter in [33] and the authors are currently considering applying the presented methodology for a more comprehensive assessment of the entire operating cycle performance of PV inverters. In this context, the presented analysis and results provides a new perspective for assessing performance of PE devices and contributes to the ongoing efforts at international level aimed at developing comprehensive and standardised testing procedures for operational and PQ performance evaluation.

# Chapter 5

# Harmonic modelling and characterisation of EVBCs

## 5.1 Introduction

Due to the combined effects of reduced electric vehicle (EV) costs, high fossil fuel prices and various incentives aimed at reducing CO2 and other GHG emission, the number of EVs in road transportation sector is steadily increasing currently. Practically all modern EVs have an on-board charger, with typical rated powers ranging from few to tens kWs. Most of on-board electric vehicle battery chargers (EVBCs) are designed as single-phase devices, but some also allow for three-phase connection, while few are designed with two single-phase chargers and can use two phases. Due to their relatively high installed powers, it is important to assess the impact of an increasing number of EVBCs on the performance of both low voltage (LV) and medium voltage (MV) networks (e.g. [115][116][117][118]).

Technical and technology developments over the recent decades led to significant changes in the design, characteristics and performance of modern EVBCs. Commercial EVBCs from the early 1980s used uncontrollable and passive power electronic (PE) circuits, resulting in a high total current harmonic distortion ($THD_I$) of around 60%-70%, low power factors and inability to regulate battery voltage and current for optimal charging performance and lifetime maintenance [119][120]. Sophisticated controls and complex PE circuits of modern EVBCs provide improved performance and controllability, typically achieved through a better regulation of voltages and currents at both input ac-side and output dc-side. Accordingly, modern EVBCs feature an input AC-DC converter, equipped with active power factor control (a-PFC) PE circuit, which regulates input ac current to have (an almost) sinusoidal shape with near unity power factor and ensures compliance with relevant harmonic emission limits, [42][43][121]. This is confirmed in some of recent studies evaluating PQ and harmonic emission of modern EVBCs, e.g. [122], showing that their $THD_I$ values at rated current and for undistorted AC supply voltage are typically lower than 10%-15%.

With the technology change of EVBCs, their large-scale penetration impacts on the operation of existing grid may be different, which is the closely related to the PQ performance of connected EVBCs. Depending on the PQ performance of modelled EVBC and the approach of representing EVBC in the grid, the obtained network study results might be completely different. For example, a study in [115] suggested that uncontrolled charging of EVs with a relatively low (10%) penetration might increase peak demands by up to 18%. On the other hand, a study in [116] suggested that connection of a number of different types of EVBCs could result in significant harmonic cancellation, which is beneficial to the distribution network operation. Accordingly, appropriate EVBC models should be used in related system operation and planning studies, in order to correctly represent their steady-state and harmonic power flow characteristics. For example, the voltage dependency of active and reactive power demands of EVBCs is particularly important for the general assessment of network voltage profiles and power flows, as well as for assessing EVBC's potential for conservation voltage reduction. In addition, the cumulative current harmonic emission of large-scale grid-connected EVBCs may deteriorate the supply voltage waveform and hence affected the normal operation of other grid-connected PE devices.

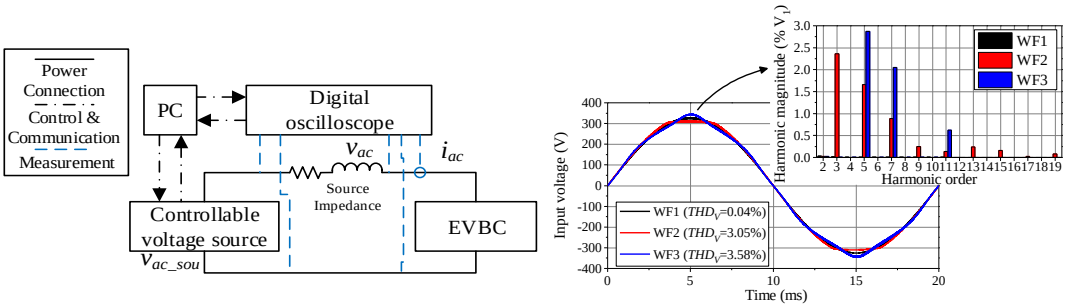
This chapter first analyses the laboratory testing results of 19 different EVBCs, with the characteristics and performance of EVBCs tested under different supply conditions fully discussed. After that, both CBM and FDM are developed for the selected EVBC, with the model accuracy fully validated. The last part of this chapter compares the performance differences between developed CBM and FDM with their advantages and disadvantages for evaluating the performance of individual devices and for their interactions in network simulations summarised.

## 5.2 Laboratory testing of EVBCs

This section introduces the test set-up for the 19 different commercial EVs and discusses their general electrical characteristics and performance under "Level 2" charging, which will be used as the reference for investigating the impact of non-ideal supply conditions on the considered electric power quantities of EVBCs in the next section.

### 5.2.1 Test set-up and analytical framework

A general set-up for testing various EVBCs at three different universities consists of a fully controllable three-phase power source with programmable voltage waveforms and source impedances, a measurement block with 1 MHz sampling rate and a PC for processing of obtained test data, as shown in Figure 5.1(a). Tested EVBCs were connected to the power source using appropriate 1-phase or 3-phase connectors for "Level 2" charging. The AC supply voltage and current waveforms were captured for EVBCs operating in "constant current" (CC) charging mode, or both CC charging mode and "constant voltage" (CV) charging mode.




a) experimental set-up b) different supply voltage waveforms

**Figure 5.1:** The experimental set-up and the supply voltage waveforms applied.

The supply condition for the tested EVBCs is a combination of different supply voltage waveforms, magnitudes and source impendences as tabulated in Table 5.1. Specifically, the applied three voltage waveforms are: a) ideally sinusoidal waveform (denoted as "WF1"), b) flat-top waveform (representing the LV network with a large number of residential customers, denoted as "WF2"), c) pointed-top waveform (representing the LV network with a large number of industrial customers, denoted as "WF3"). The supply voltage magnitudes of test voltage waveforms were varied in the range of 0.9 p.u. to 1.1 p.u., with a step of 0.05 p.u., in order to acknowledge for allowed and typically present supply voltage magnitude variations in LV networks, [40]. In addition, both zero source impedance (ZS1) and flicker (i.e. maximum) source impedance (ZS2) are applied between the power supply and tested EVBCs, representing the minimum possible source impedance which is close to zero (considering the charging cable impedance is small enough to be ignored), and the maximum source impedance in the LV distribution network to represent a weak gird respectively. All the EVBCs were tested under CC charging mode, with some of them

tested under CV charging mode as well. The electrical characteristics evaluated for tested EVBCs include $P$, $Q_1$, $PF$, $PF_1$, $PF_d$, $THDS_I$ and $THCS$, by using the calculation approaches defined in Chapter 2.

**Table 5.1:** Test parameter values.

| Test Parameter | Values | Test Points |
|---|---|---|
| **Source impedance (Ω)** | ZS1~0, ZS2 = 0.4+j0.25 | 2 |
| **Type of voltage waveform** | WF1, WF2, WF3 | 3 |
| **Voltage supply magnitude (pu)** | 0.9, 0.95, 1, 1.05, 1.1 | 5 |

### 5.2.2 Basic information and results of tested EVBCs

The basic information on the 19 tested EVBCs and the measured values on the general electrical characteristics (including $P$, $Q_1$, $PF$, $PF_1$, $PF_d$ and $THDS_I$) for EVBCs operating under ideal supply condition are listed in Table 5.2, which does not provide any information on both EV and EVBC manufacturers and models. Nevertheless, the test sample of 19 different on-board EVBCs from this chapter effectively represents the majority of the EVs currently available in the commercial EU market. In addition, the data provided in Table 5.1 is for EVs under "Level 2" charging (208 V-240 V single-phase, or 360 V-415 V three-phase, ac supply, with the input ac charging current up to 80 A), considering the fact that "Level 2" charging is currently the predominant charging approach in EU.

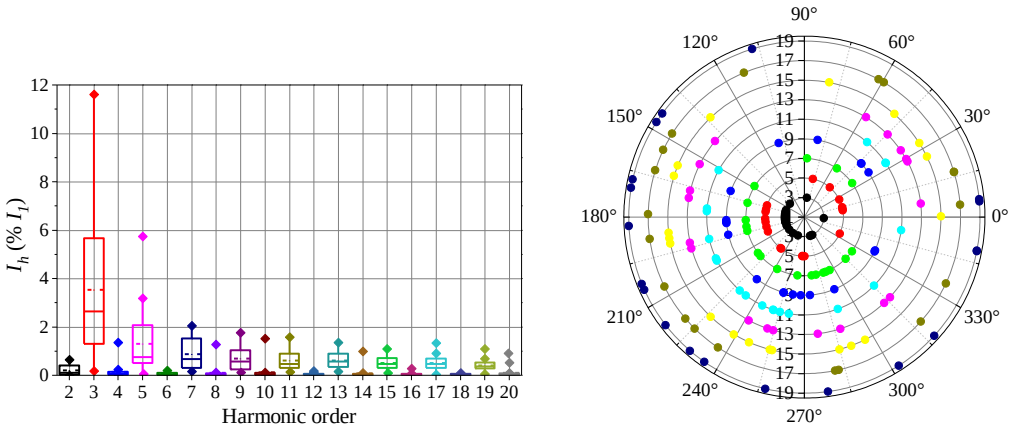
It is also noticed from Table 5.2 that all tested EVs (except EV10) are equipped with Li-ion battery featured with constant current (CC)-constant voltage (CV) charging mode. Specifically, when the battery state of charge (SoC) is below 80%-90% of the full battery capacity, EV is under CC charging mode, where the charging power is maintained constant (assuming the supply voltage condition does not change during the charging period). If EV is further charged, it will enter into CV charging mode, where the charging power will gradually decrease with the increase of charging time (or battery SoC). As the CC charging mode is the dominant period for EV charging and the nameplate charging power refers to EV under CC charging, information given in Table 5.2 are for EV under CC charging mode (with ideal supply condition).

**Table 5.2:** Basic information on the tested EVBCs

| No. | Nameplate values | | | | | Measured values | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Charging characteristics | | | Battery | | Electrical characteristics | | | | | |
| | Tested phases | $P_{rated}$ (kW) | Max $I_{charge}$ (A) | Types | Ratings (kWh) | *P* (kW) | $Q_1$ (kVAr) | *PF* | $PF_1$ | $THDS_I$ (%) | *THCS* (A) |
| **1** | 1ph | 7.7 | 32 | Li-ion | 32 | 6.407 | 0.137 | 0.998 | 1.000 | 3.159 | 0.874 |
| **2** | 1ph | 7.4 | 32 | Li-ion | 22 | 7.118 | 0.138 | 0.999 | 1.000 | 4.310 | 1.335 |
| **3** | 1ph | 3.3 | 16 | Li-ion | 14.5 | 3.181 | -0.181 | 0.995 | 0.998 | 7.698 | 1.067 |
| **4** | 1ph | 3.3 | 16 | Li-ion | 8.8 | 3.455 | -0.412 | 0.993 | 0.993 | 2.521 | 0.382 |
| **5** | 3ph | 6.1 | 13 | Li-ion | 36 | 3.299 | -0.157 | 0.998 | 0.999 | 2.741 | 0.389 |
| **6** | 1ph | 3.3 | 16 | Li-ion | 24 | 3.615 | -0.484 | 0.984 | 0.991 | 11.693 | 1.855 |
| **7** | 1ph | 3.3 | 16 | Li-ion | 22 | 3.567 | -0.048 | 0.998 | 1.000 | 4.852 | 0.753 |
| **8** | 1ph | 7.2 | 16 | Li-ion | 18.7 | 3.517 | -0.319 | 0.995 | 0.996 | 2.620 | 0.402 |
| **9** | 1ph | 3.3 | 16 | Li-ion | 4.4 | 2.208 | -0.110 | 0.998 | 0.999 | 3.077 | 0.296 |
| **10** | 1ph | 2.75 | 16 | NiCd | 14 | 2.988 | -0.276 | 0.993 | 0.996 | 7.256 | 0.947 |
| **11** | 1ph | 3.3 | 16 | Li-ion | 22 | 3.501 | -0.260 | 0.997 | 0.997 | 3.046 | 0.464 |
| **12** | 3ph | 7.4/22 | 32 | Li-ion | 22 | 6.900 | -1.470 | 0.974 | 0.978 | 7.384 | 2.259 |
| **13** | 3ph | 3.3/22 | 16/32 | Li-ion | 17.6 | 3.705 | -0.203 | 0.998 | 0.998 | 1.380 | 0.223 |
| **14** | 3ph | 10/20 | 40/80 | Li-ion | 85 | 5.852 | -0.988 | 0.985 | 0.986 | 5.235 | 1.352 |
| **15** | 1ph | 16.8 | 80 | Li-ion | 56 | 6.412 | -1.601 | 0.969 | 0.970 | 5.773 | 1.659 |
| **16** | 1ph | 3.3 | 16 | Li-ion | 12 | 2.190 | -0.123 | 0.998 | 0.998 | 1.704 | 0.162 |
| **17** | 1ph | 3.3 | 16 | Li-ion | 23 | 2.074 | -0.011 | 0.998 | 1.000 | 5.627 | 0.507 |
| **18** | 1ph | 3.7 | 16 | Li-ion | 11.2 | 2.890 | 0.073 | 0.999 | 1.000 | 3.083 | 0.388 |
| **19** | 1ph | 3.3 | 16 | Li-ion | 16 | 3.371 | -0.110 | 0.997 | 0.999 | 7.129 | 1.044 |

As shown in Table 5.2, EVBC5, and EVBC12-14 are tested with three-phase charging connection while the other EVBCs are tested with single-phase charging connection. For the single-phase charging connection, it can be easily accessible at residential houses with no-dedicated socket while the three-phase charging connection requires dedicated charging infrastructure. It is also noticed from Table 5.2 that the rated charging power of most of the tested EVBCs are higher than the after diversity maximum demand (ADMD) of a typical UK household which is between 1.5 kW and 2.5 kW [3], suggesting high penetration level of EVBCs will indeed increase the total power demand of existing LV network. Apart from the nameplate values, measured electrical characteristics including *P*, $Q_1$, *PF*, $PF_1$, $THDS_I$ and *THCS* are also listed in Table 5.2, giving a general evaluation of the PQ performance of tested EVBCs. It turns out that all tested EVBCs have near unity *PF*, with relatively low $THDS_I$ value (except EVBC6, all other EVBCs have their $THDS_I$ value below 10%).

In addition, the distribution characteristics of individual current harmonic magnitudes (in a percentage of fundamental components) and phase angles ($2^{nd}$ to $20^{th}$ odd orders) of tested EVBCs under ideal supply condition are illustrated in Figure 5.2. For the box plot in Figure 5.2(a), the lower boundary and upper boundary represent the $25^{th}$ percentile and $75^{th}$ percentile respectively while the solid line and dash line inside the box refers to the median and mean values respectively, with the outliers represented by filled symbols. It is observed that the considered odd order current harmonic magnitudes gradually decreases with the increase of harmonic orders, while the even order current harmonics have negligible magnitudes. In addition, almost all tested EVBCs have their individual current harmonic magnitudes below 10% of their fundamental currents, $I_1$. As the even order current harmonics have negligible magnitudes as opposed to odd order current harmonics, only the phase angles of odd order current harmonics are given in Figure 5.2(b) (refer to the fundamental voltage phase angle which is set at zero), for which a decentralized distribution is observed. It suggests that apparent harmonic cancellation can be achieved when different EV models are connected to the same charging point (e.g. a car park with EV charging capability).




a) box plot of individual current harmonic magnitudes

b) phase angle distribution of $3^{rd}$-$19^{th}$ odd order current

**Figure 5.2:** The distribution characteristics of $2^{nd}$-$20^{th}$ individual current harmonics of 19 tested EVBCs (CC mode) operating under ideal supply condition.

## 5.3 Impact of supply conditions on the characteristics and performance of EVBCs

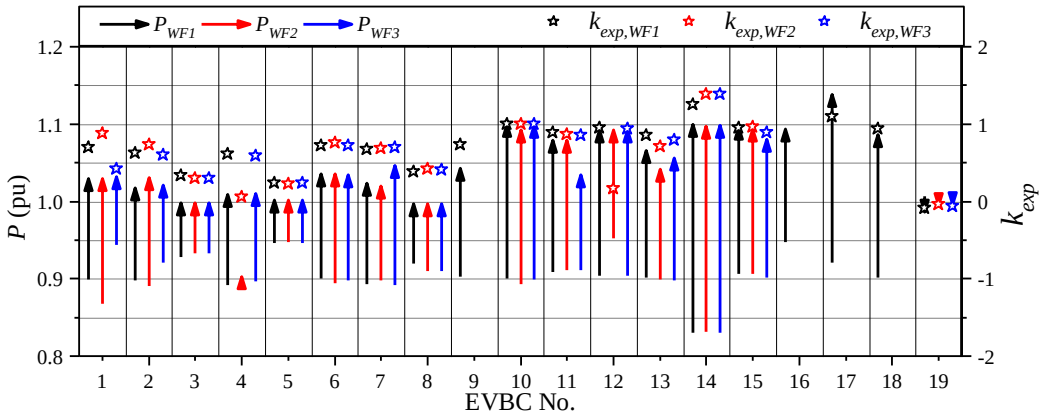
In order to develop suitable models to accurately represent the electrical behaviour of tested EVBCs under practical gird conditions, it is necessary to investigate how the

electrical characteristics of tested EVBCs vary under different supply condition (i.e. a combination of different supply voltage magnitudes, waveform distortion, and source impedances), which is done through comprehensive laboratory testing. In this section, the impact of varying supply conditions on the electrical characteristics of all 19 EVBCs will be fully investigated.

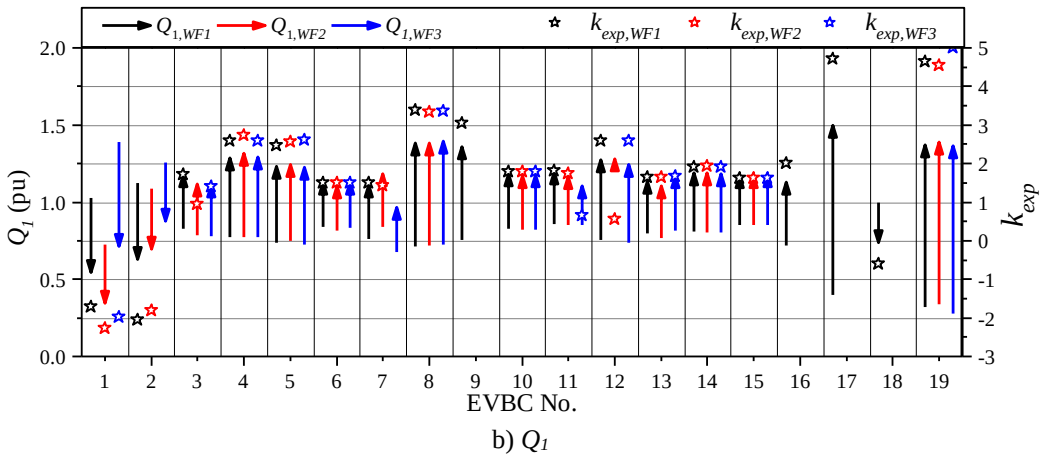
### 5.3.1 Impact of supply voltage conditions on the power consumption

The overview of active power, $P$ and fundamental reactive power, $Q_1$ of all tested EVBCs (CC mode) operating under a combination of different supply voltage waveforms (WF1-3) and voltage magnitudes (0.9-1.1 p.u. with a step of 0.05 p.u.) with ZS1 is shown in Figure 5.3, where the arrow represents the change of indices from 0.9 p.u. to 1.1 p.u. supply voltage magnitude with the black, red and blue colour correspond to WF1, WF2 and WF3, respectively. In addition, the voltage magnitude dependency of indices is further represented by the exponential fitting coefficient, $k_{exp}$, which is calculated by applying the exponential fitting (in the form of $P_{pu}=V_{pu}^{kexp}$) to the indices values at five voltage magnitudes (from 0.9 p.u to 1.1 p.u. with a step of 0.05 p.u.). The higher absolute value of $k_{exp}$ represents a stronger voltage magnitude dependency of indices. It should be noted that EVBC9 and EVBC16-18 are tested under WF1 only, and $P$ and $Q_1$ are given in per-unit values by using their measured nominal values in Table 5.2 as the bases.

It is observed from Figure 5.3 that $P$ of tested EVBCs almost linearly increases with the increasing supply voltage magnitudes ($k_{exp}$ close to 1), and is insensitive to the considered supply voltage distortions. EVBCs 1, 2, and 18 have their $Q_1$ reduced with the increasing voltage magnitudes while all the other EVBCs have the opposite trend.




a) $P$




b) $Q_1$

**Figure 5.3:** Overview of $P$ (p.u.) and $Q_1$ (p.u.) of tested EVBCs (CC mode) for different supply voltage conditions and ZS1.

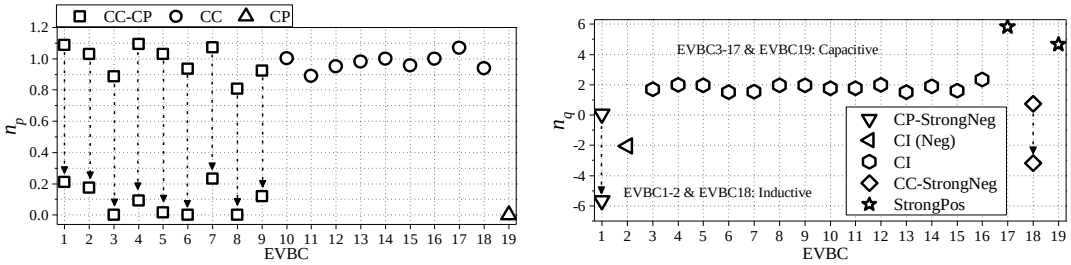
According to the laboratory testing results on the voltage dependent characteristics of $P$ and $Q_1$, it turns out that some of the tested EVBCs will have completely different $P$-$V$ or $Q_1$-$V$ relationships once the supply voltage surpasses 1 p.u. (0.95 p.u. for EVBC5 and 1.05 p.u. for EVBC6). The composite (or piecewise) $P$-$V$ and $Q_1$-$V$ relationships deserve special attention when developing EVBC models for network study purpose. In order to more accurately investigate that issue, a general classification of tested EVBCs is introduced in this section, based on the voltage-dependent changes of measured active and fundamental reactive power demands (under WF1, ZS1). This classification is done in accordance with the commonly used formulation of steady state "exponential load model", in which changes of active and reactive power demands with the voltage are expressed as:

$$P = P_0(V/V_0)^{n_p} \tag{5.1}$$

$$Q = Q_0(V/V_0)^{n_q} \tag{5.2}$$

where: $P$, $Q$ are active and reactive power demands at supply voltage $V$; $V_0$ is nominal (1 p.u.) voltage; $P_0$, $Q_0$ are active and reactive powers at nominal 1 p.u. supply voltage $V_0$; $n_p$, $n_q$ are exponential model coefficients for active and reactive power, respectively. The values of $n_p$ and $n_q$ equal, or close to 0, 1 and 2 represent load model characteristics known as "constant power" (CP), "constant current" (CC) and "constant impedance" (CI) load, respectively.

The obtained exponential load model coefficients of tested EVBCs are illustrated in Figure 5.4. As some of the tested EVBCs exhibit different *P*-*V* or $Q_1$-*V* relationships once the supply voltage exceeds $V_0$ (1.0 p.u. for EVBC1-4 and EVBC7-19, 0.95 p.u. and 1.05 p.u. for EVBC5 and EVBC6 respectively), the exponential model coefficients are dived into two parts ($V \leq V_0$ and $V > V_0$). According to the similarities of the *P*-*V* and $Q_1$-*V* dependency among tested EVBCs, it is able to classify all tested EVBCs into different types.




a) exponential load model coefficients for active power, $n_p$

b) exponential load model coefficients for fundamental reactive power, $n_q$

**Figure 5.4:** The exponential load model coefficients of tested EVBCs (StrongNeg and StrongPos correspond to "strong negative" and "strong positive" characteristics, respectively).

As shown in Figure 5.4, EVBC1-9 have "composite" active power demand (*P*-*V*) characteristics, i.e. they will transfer from a CC load type ($n_p$ values are around 1) to a constant power (CP) load type (np values are around 0) when the supply voltage magnitude exceeds a certain value. Accordingly, they are denoted as a "constant current-constant power" (CC-CP) active power load type. EVBC10-18 are classified as a CC active power load type, as their $n_p$ values are around 1 for the considered range of supply voltage magnitude variation, while EVBC19 with $n_p \sim 0$ is classified as a CP active power load type. The change of *P*-*V* relationship for EVBC1-9 is possibly because the maximum allowed charging power predefined in the control circuits of on-board EV charger is reached when supply voltage exceed certain value. Accordingly, the charger starts to regulate the charging power rather than maintaining a constant charging current.

Although $Q_1$ is relatively small as opposed to *P* (demonstrated by near unity *PF* given in Table 5.2), tested EVBCs can also be divided into different groups according to the $n_q$ values. It is observed from Figure 5.4(b) that EVBC1 has a "composite" fundamental reactive power demand characteristic ($Q_1$-*V*), as its $n_q$ value shifts from

0.053 to -5.66 when the supply voltage magnitude exceeds 1 p.u. Accordingly, EVBC1 is classified as a "constant power-strong negative (CP-StrongNeg)" reactive power load type. EVBC2 (represented has $n_q$~-2, and its $Q_1$-$V$ characteristic is classified as a "constant impedance (negative)", CI (Neg) load type. EVBC3-17 have $n_q$ values around 2, and they are classified as a "constant impedance" (CI) load type regarding their fundamental reactive power demand characteristics. For EVBC17 and EVBC19, their $n_q$ values are 5.8 and 4.65 respectively, denoting that their $Q_1$-$V$ characteristic has a strong positive relationship, and is therefore classified as a "strong positive (StrongPos)" reactive power load type. For EVBC18, its $n_q$ value transfers from 0.74 to -3.2 when the input voltage magnitude is greater than 1.0 p.u., and hence, it is classified as a "constant current-strong negative", CC-StrongNeg load type. The above classification of the tested EVBCs is illustrated in more detail in Figure 5.5.

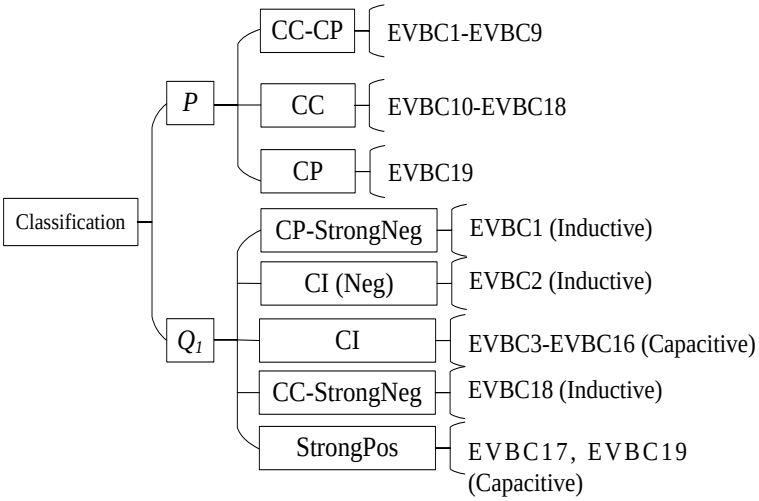
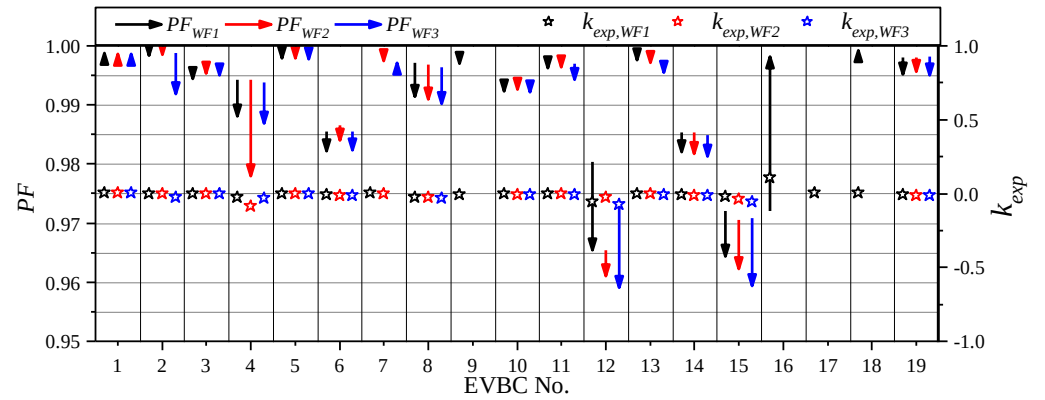


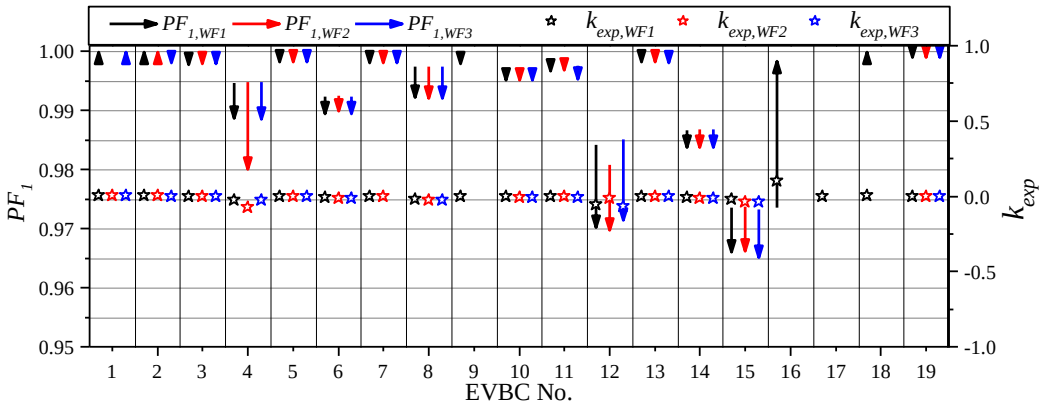

**Figure 5.5:** Classification of the tested EVBCs based on $P$-$V$ and $Q_1$-$V$ characteristics.

## 5.3.2 Impact of supply voltage conditions on the power factors

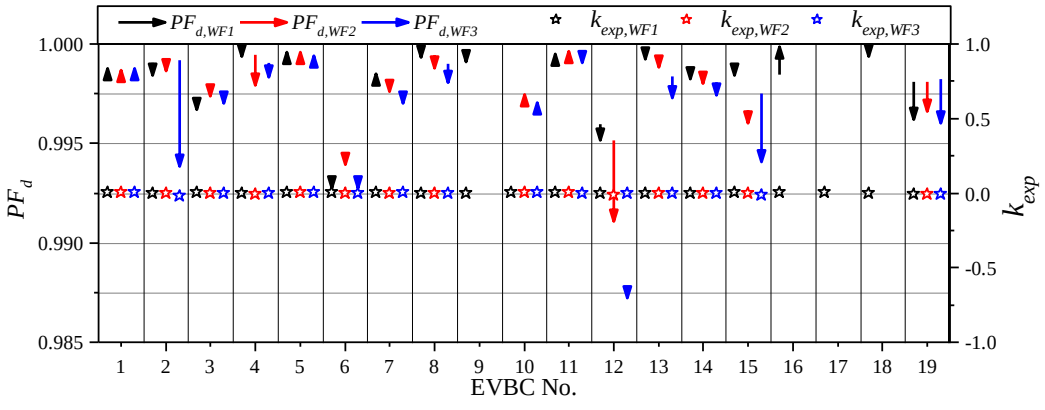
The supply voltage dependency of power factors of tested EVBCs is illustrated in Figure 5.6. It is noticed that $PF$, $PF_1$ and $PF_d$ achieve near unity values under all considered supply voltage conditions, and are insensitive to the supply voltage distortion and magnitude deviations ($k_{exp}$ equals 1). In addition, $PF$ and $PF_1$ either stay constant (e.g. EVBC1-3 and EVBC 7) or gradually decrease (e.g. EVBC4, 6 and 12) with the increase of voltage magnitudes, while $PF_d$ is insensitive to both supply voltage distortion and magnitude variations ($k_{exp}$ equals 1).




a) *PF*




b) $PF_1$




c) $PF_d$

**Figure 5.6:** Overview of *PF*, $PF_1$ and $PF_d$ of tested EVBCs (CC mode) for different supply voltage conditions and ZS1.

### 5.3.3 Impact of supply voltage conditions on the current distortions

The impact of different supply voltage conditions on the current waveform distortions ($THDS_I$ and *THCS*) is illustrated in Figure 5.7. It turns out that for most of the tested EVBCs (e.g. EVBC1 and EVBC3), their $THDS_I$ and *THCS* values are insensitive to the voltage magnitude variation ($k_{exp}$ is around 1), but slightly decrease under WF2 and increase under WF3. A few of the tested EVBCs like EVBC4, EVBC8 and

EVBC13 have their current waveform distortion apparently aggravated under distorted supply voltage, especially under WF3.

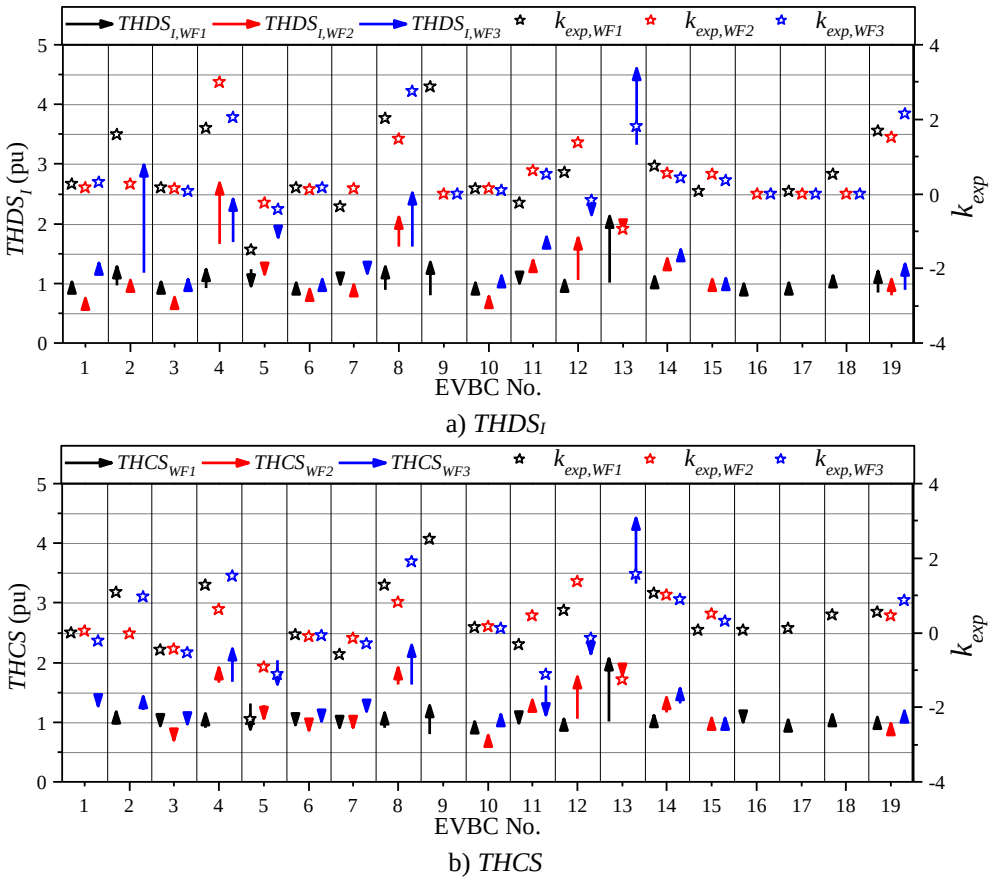



**Figure 5.7:** Overview of $THDS_I$ and $THCS$ of tested EVBCs (CC mode) for different supply voltage conditions and ZS1.

### 5.3.4 Impact of source impedance

In this part, the impact of source impedance on the electrical characteristics is demonstrated on EVBC2, EVBC6, EVBC8 and EVBC10 which are tested under the flicker source impedance, ZS2. The comparison between indices under ZS1 and indices under ZS2 for EVBCs operating under WF2-3 supply voltage waveforms with a magnitude of 1 p.u., is shown in Figure 5.8. In addition, $P$, $Q_1$ and $THDS_I$ are given in p.u. by using their corresponding values in Table 5.2 as the bases. It is observed that $P$ and $Q_1$ slightly decrease under ZS2 for the four EVBCs (except for EVBC2 whose $Q_1$ slightly increases under ZS2). The power factors ($PF$, $PF_1$ and $PF_d$) are insensitive to the change of source impedance. For the current waveform distortion, increased $THDS_I$ values are seen under ZS2.

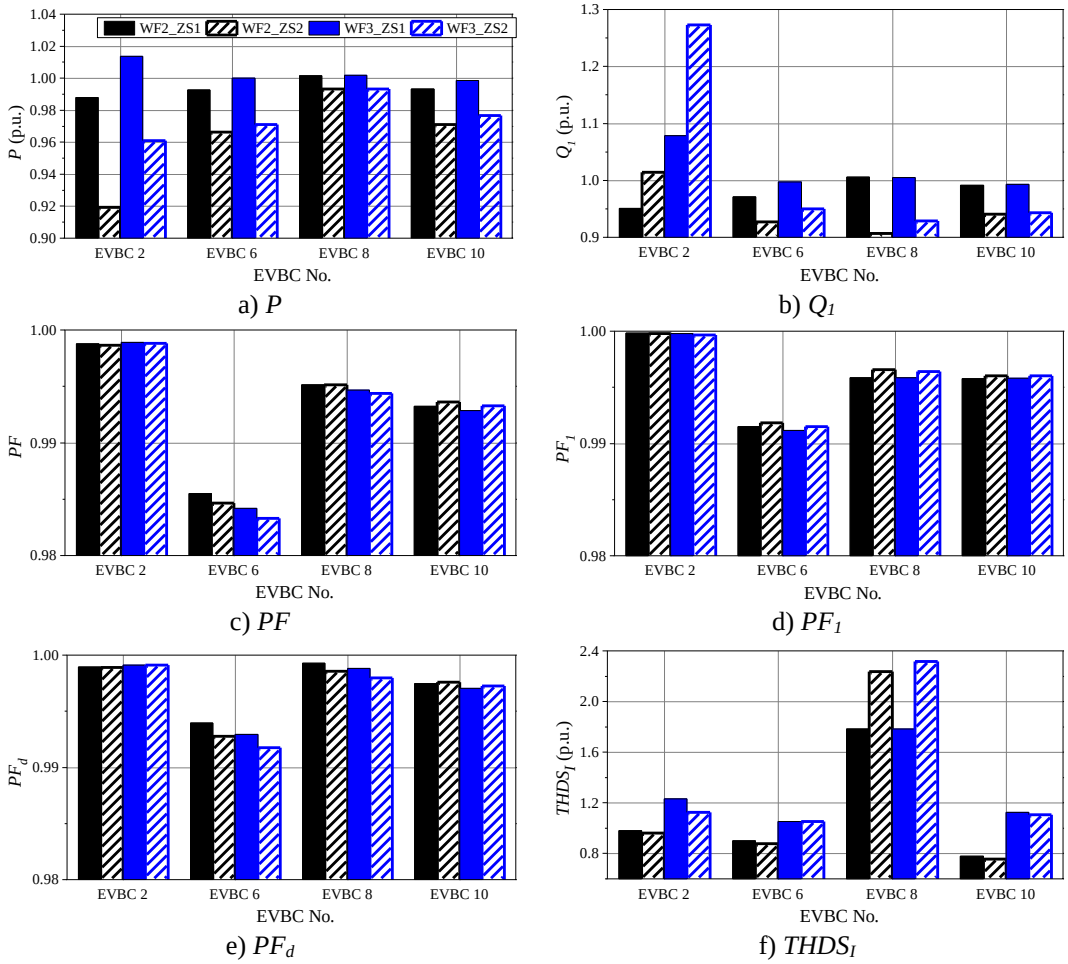
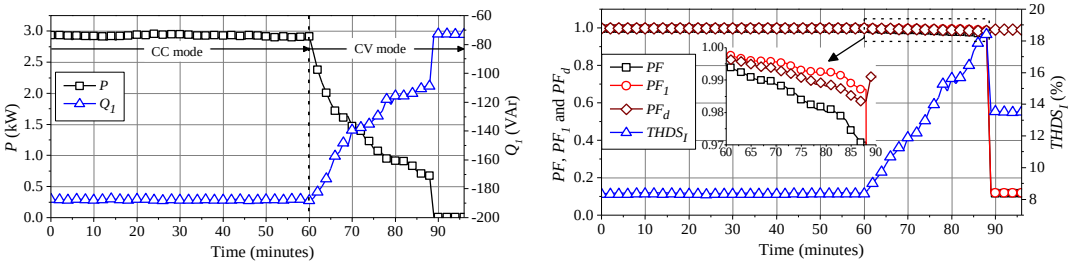



**Figure 5.8:** The calculated indices values under ZS1-2 (with WF2-3 and a supply voltage magnitude of 1 p.u.).

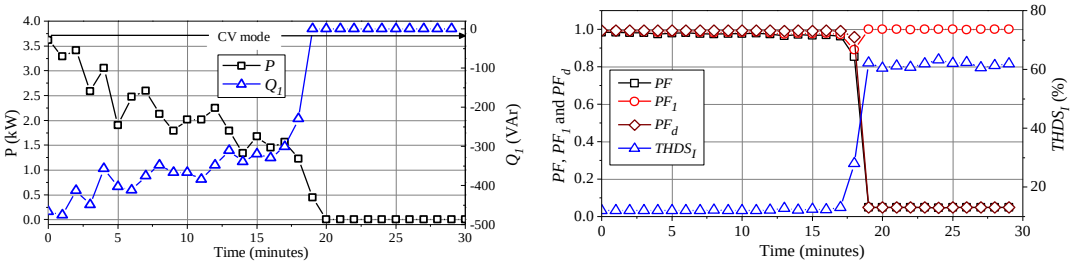
### 5.3.5 Impact of CV charging mode on the general electrical characteristics

Among the 19 tested EVBCs, EVBC3, EVBC6 and EVBC8 are tested under CV charging mode, with the change of their electrical characteristics during CV mode charging period demonstrated in Figures 5.9-5.11. It is observed that the considered electrical characteristics are almost constant when EVBCs are under CC mode while keep changing with the charging time when EVBCs are under CV mode. Specifically, both $P$ and $Q_1$ start to decrease with charging time once EVBCs enter into the CV mode, together with increase of $THDS_I$. The power factors ($PF$, $PF_1$ and $PF_d$) are still close to unity until the operating power drops to very low values (close to zero).



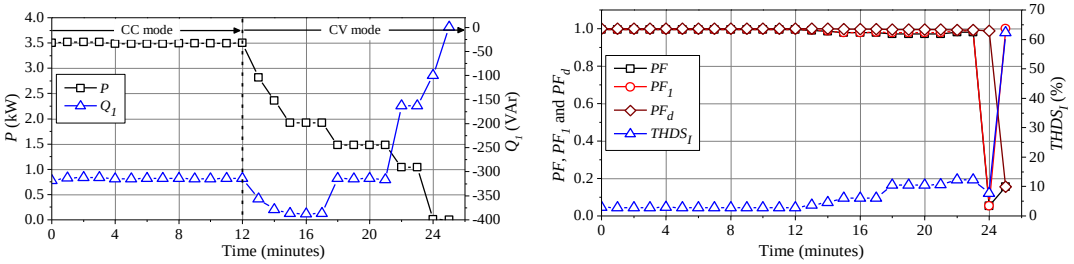

a) $P$ and $Q_1$ b) $PF$, $PF_1$ and $PF_d$

**Figure 5.9:** The change of general electrical characteristics with charging time for EVBC3 transferring from CC mode to CV mode (under ideal supply condition).




a) $P$ and $Q_1$ b) $PF$, $PF_1$ and $PF_d$

**Figure 5.10:** The change of general electrical characteristics with charging time for EVBC6 transferring from CC mode to CV mode (under ideal supply condition).

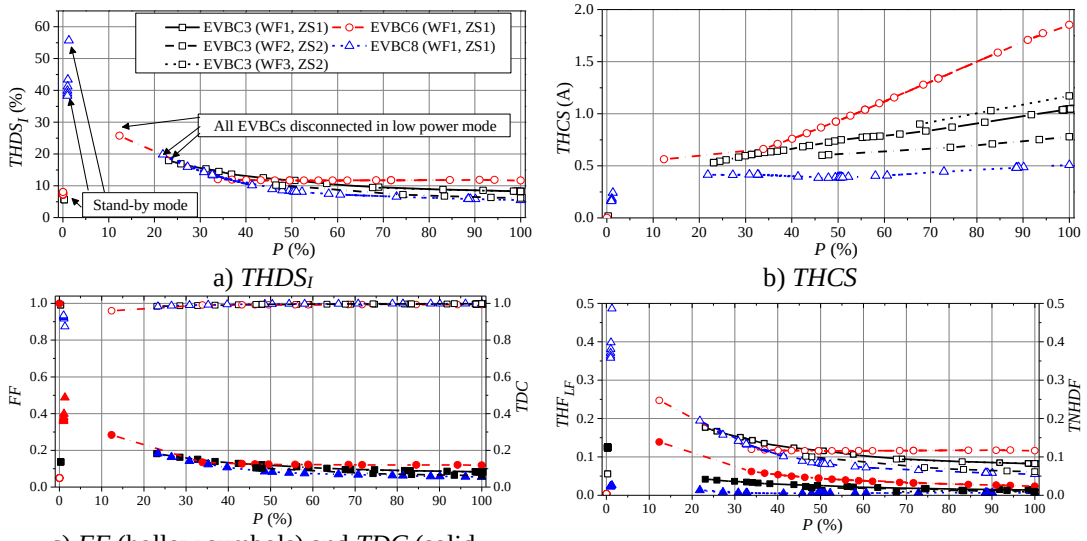



a) $P$ and $Q_1$ b) $PF$, $PF_1$ and $PF_d$

**Figure 5.11:** The change of general electrical characteristics with charging time for EVBC8 transferring from CC mode to CV mode (under ideal supply condition).

Figures 5.9-5.11 suggest that transferring from CC mode to CV mode mainly affects the power consumption and input ac current waveform distortion. Accordingly, the change of current waveform distortion under CV mode can be regarded as its power dependency characteristics, with the waveform distortion indices ($THDS_I$, $THCS$, $FF$, $TDC$, $THF_{LF}$ and $TNHDF$) over the whole power ranges of the three tested EVBCs illustrated in Figure 5.12. It is observed that the $THDS_I$ values of all three EVBCs gradually increase with the decrease of operating powers and reach the maximum values at very low operating power (around 1% $P_{rated}$). The maximum $THDS_I$ values occur when EVBCs are operating at "stand-by" mode, i.e. when charging is finished but the EVBC is still connected to the supply [8]. However, this is not considered

further due to the negligible power demands (and hence negligible current magnitudes).




a) $THDS_I$ b) *THCS*

c) *FF* (hollow symbols) and *TDC* (solid symbols)

d) $THF_{LF}$ (hollow symbols) and *TNHDF* (solid symbols)

**Figure 5.12:** The power dependency characteristics of current waveform distortion indices for three EVBCs under CV mode.

Regarding the *THCS* values in Figure 5.12(b), EVBC3 and EVBC6 have their *THCS* values steadily decrease with reduced powers, while an initial reduction of *THCS* is observed for EVBC8, followed by a slight increase of *THCS* below 40% $P_{rated}$. Figure 5.12(c) shows that the contribution of the fundamental current (represented by *FF* introduced in Chapter 2) of the tested EVBCs is somewhat reduced in (very) low power mode, with limited contribution of non-fundamental currents (represented by *TDC* introduced in Chapter 2). In addition, it is noticed from Figure 5.12(d) that LF harmonics (represented by $THF_{LF}$) are the main contributor to the total waveform distortion, due to the relatively low values of *TNHDF* ($THF_{LF}$ and *TNHDF* are introduced in Chapter 2).

## 5.4 Harmonic modelling of EVBC

To study the impact of large-scale deployment of EVs on power flows and PQ, accurate EVBC models are required. Depending on the type of charger and purpose of modelling, a variety of different EVBC models have been proposed in existing literature, and can be generally divided into three types: CBMs [123][124][125][126], FDMs [127][128][129], constant power load [130][131]. Only the first two model

forms are able to represent the harmonic characteristics of EVBCs, while constant power load is applied for general power flow studies. In addition, existing literature on EVBC modelling mainly focus on the development of novel EVBCs (e.g. [125][126]) and the presented models generally not capable of representing the characteristics and performance of existing commercial EVBCs. To address the above issue, this chapter presents both the CBM and FDM of selected single-phase unidirectional on-board EVBC currently available on the EU domestic market, with the model accuracy fully validated with measurement. This chapter extends the EVBC modelling work presented in [116], with the objective of producing suitable models for evaluating the impact of the increased penetration of EVs on low voltage (LV) and medium voltage (MV) networks.

### 5.4.1 Component-based modelling

As an important component of the EV, the characteristics and performance of EVBC are closed related to the battery life, charging modes, conditions and durations. EVBCs can be classified into different types based on serval factors including the charging location (on-board and off-board), the charging voltage and current (single-phase, three-phase or dc charging) and the power flow directions (unidirectional or bidirectional). It is obvious that characteristics and performance of EVBCs vary among different types while this chapter concentrates on the single-phase unidirectional on-board chargers. Although EVBCs are gradually increasing the penetration into the grid, there is still no dedicated harmonic limits specified in [121], which instead recommends the harmonic limits for Class A equipment defined in [42]. Accordingly, EVBCs are normally equipped with a-PFC circuit, not only for their harmonic suppressions, but also for the control of reactive power demands. However, considering the fact that the LV residential networks are typically featured by supply voltage distortion which may have an effect on the control of the a-PFC circuit, the current harmonic emission characteristics of PE devices may vary under different supply voltage distortion [132], highlighting the importance of including the a-PFC circuit in the correct modelling of EVBCs. In the following, the detailed CBM development procedure for selected EVBC will be discussed, followed by the validation of model accuracy with measurement.

**Full circuit EVBC model of CC mode**

As a complex power electronic circuit, the main components of typical single-phase unidirectional EVBC include EMI filter, standard diode bridge rectifier (DBR), an AC-DC converter (e.g. boost converter) with its control circuit, a DC-DC full-bridge converter with its PWM control, as illustrated in Figure 5.13. Specifically, the EMI filter is to filter the high-frequency harmonics of the supply current while the DBR is to rectify the ac voltage to dc. Although there are a variety of a-PFC based AC-DC converters like buck, boost, buck-boost, cúk, flyback or forward converters, the boost converter based a-PFC topology with inductor current operating at continuous conduction mode (CCM) is still the most widely used a-PFC strategy [133][134], and is implemented in the developed CBM for selected EVBC in this chapter.

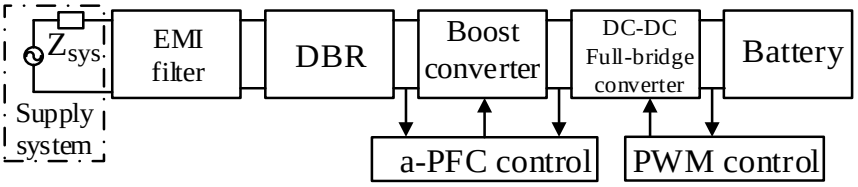



**Figure 5.13:** Main components of a single-phase unidirectional EVBC.

The schematic of the developed full circuit CBM of selected single-phase unidirectional EVBC is illustrated in Figure 5.14, consisting of the front-end circuit (the system impedance, EMI filter and boost converter and its control) and the back-end circuit (the DC-DC full-bridge converter with the battery charging control). The functionalities of the main components will be discussed separately in the following.

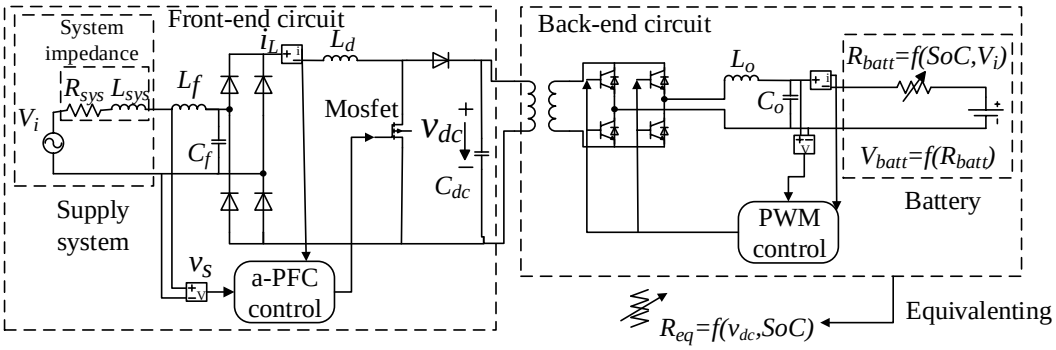



**Figure 5.14:** The schematic of the developed full circuit CBM of a single-phase unidirectional EVBC circuit.

*1) Front-end AC-DC converter and a-PFC control:*

For the developed component based EVBC model, the a-PFC circuit is implemented on a boost converter. The conventional a-PFC control techniques include average current control, peak current control and sinusoidal or fixed-band current control, and normally consist of an inner current loop and outer voltage loop. The inner current loop is to regulate the inductor current (and hence the input ac current) within the defined upper and/or lower boundaries, through the high-frequency switching behaviour of the switches of the a-PFC based converter. The outer voltage loop is to maintain the dc-link voltage at a specified value, as well as providing the magnitude for the reference inductor current (i.e. the amplified dc voltage error in the outer voltage loop).

The block diagram of the a-PFC control circuit applied to the developed full circuit CBM is illustrated in Figure 5.15. Unlike traditional current control circuit where the reference magnitude for the inductor current or input ac current is obtained from the amplified dc-link voltage error, the outer voltage loop is neglected in the applied modified peak current control and the reference magnitude of input current is obtained from the mathematical relationship between the input ac voltage and input ac current from the measurement as shown in (5.3). Regarding the reference inductor current waveform shape, as the measured time-domain input current waveform shape is similar with the supply voltage waveform under different supply voltage distortions, the reference waveform shape for the inductor current can be achieved by the scaling-down of input voltage waveform, while the reference magnitudes for the upper boundary and lower boundary of the inductor current can be obtained by (5.4) and (5.5) respectively.

$$I_{AC,rms,ref} = \begin{cases} 3.50e^{-4}V_{AC,rms}^2 - 0.142V_{AC,rms} + 28.78, & 183.81V \le V_{AC,rms} < 218.24V \\ -0.051V_{AC,rms} + 25.51, & 218.24V \le V_{AC,rms} \le 275.74V \end{cases} \quad (5.3)$$

$$\hat{I}_{L.upper} = \left(\frac{\hat{V}_{AC}}{V_{AC,rms}} + 0.105\right) I_{AC,rms,ref} \quad (5.4)$$

$$\hat{I}_{L.lower} = 0.6\hat{I}_{L.upper} \quad (5.5)$$

where: $I_{AC,rms,ref}$ and $V_{AC,rms}$ are the reference rms value of the input ac current and the measured input current respectively while $\hat{V}_{AC}$, $\hat{I}_{L,upper}$ and $\hat{I}_{L,lower}$ are peak values of

the upper boundary and the lower boundary for the inductor current; $i_{L,ref}$ is the reference inductor current; $\frac{\hat{V}_{AC}}{V_{AC,rms}}$ is the crest factor of $v_{ac}$.

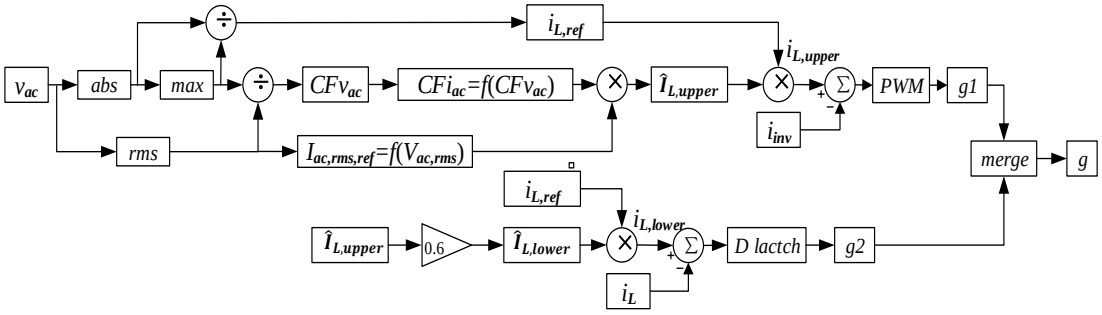



**Figure 5.15:** The block diagram of the developed a-PFC control circuit for the boost converter in Figure 5.14.

As shown in Figure 5.15, besides the upper boundary ($i_{L,upper}$) used in a conventional peak current control, a lower boundary ($i_{L,lower}$) for the inductor current is also added to the modified peak current control. When the inductor current is less than its lower boundary value, the boost converter is switched on until the inductor current increases above the lower boundary. When the inductor current is higher than its lower boundary value, the difference between the inductor current and its upper boundary is compared with a ramp signal to generate pulse width modulation (PWM) control for the boost converter switch. The switching frequency of the boost converter is set at 35.8 kHz, which is equal to the frequency of the ramp signal. By comparing the simulated current harmonics of the modified peak current and the other three considered a-PFC control circuit (i.e. the average current control, the peak current control and the hysteresis control) with the measured current harmonics under ideally sinusoidal supply voltage given in Figure 5.16, it turns out that the applied modified peak current control circuit can better represent the current harmonic characteristics as opposed to the other three a-PFC control circuits, in terms of the total subgroup harmonic distortion ($THDS_I$) and harmonic magnitudes/phase angles.

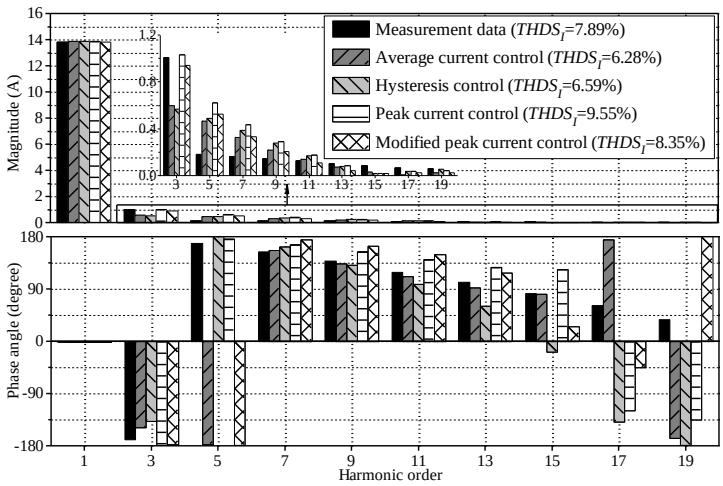



**Figure 5.16:** Comparison of input ac current harmonic magnitudes, phase angle and $THDS_I$ values between measurements and considered a-PFC circuits.

*2) High-frequency transformer:*

To ensure a safety and better control of the voltage and current supplied to the battery via the back-end DC-DC converter, a high-frequency transformer is used in the CBM to achieve the galvanic isolation.

*3) Back-end DC-DC full-bridge converter with battery charging control:*

As the battery packs used for commercial EVs are normally Lithium-ion batteries which are featured by constant-current constant-voltage (CCCV) charging mode. Specifically, when the battery' state of charge (SoC) is below 80%-90% of its full state value, the charging current fed to the battery is maintained constant at its reference value while the charging voltage gradually increases until it reaches its reference value (CC mode). Once the battery voltage reaches its reference value, it will be kept constant with a graduate decrease of the battery current (CV mode). It is observed during the testing of EVs, the CC charging mode plays a key role in EV battery charging as opposed to the CC charging mode which normally lasts around a few to several tens of minutes.

Figure 5.17 shows the control circuit of the DC-DC full-bridge converter in the developed EVBC model, where the reference values for the battery current and voltage are set at 6.5 A ($I_{batt,ref}$) and 360 V ($V_{batt,ref}$) respectively according to the actual measurement data of the battery voltage ($v_{batt}$) and current ($i_{batt}$) shown in Figure 5.18. By comparing the amplified voltage and current errors with the ramp signal (frequency

is 35.8 kHz), the PWM signal for controlling the switching behaviour of the four transistors of the DC-DC full bridge converter is obtained.

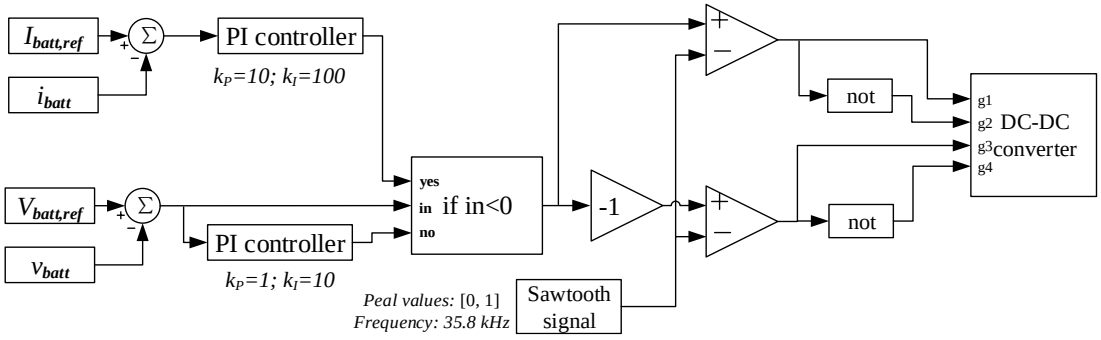



**Figure 5.17:** The control circuit of the DC-DC full-bridge converter.

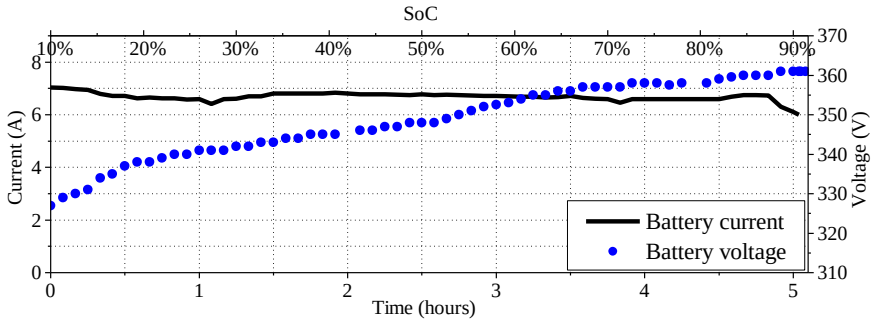



**Figure 5.18:** Measured battery voltage and current for EVBC charging under 1 p.u. sinusoidal input ac voltage.

*4) Battery:*

To correctly evaluate the performance of the developed EVBC model, it is necessary to accurately represent the EV battery in the model, which is expressed as a function of battery charging time (i.e. SoC) and voltage magnitude of the input ac voltage magnitude (i.e. $V_i$), as given in (5.6). The mathematical expression between the battery resistance and battery charging time can be directly obtained from the measurements of the charging voltage and current for the EV battery, which turns out to be approximately linear, Figure 5.19. In addition, it should be noted that the equivalent battery resistance decreases with the reducing input ac voltage magnitude, as shown in Figure 5.19 and (5.6).

$$R_{batt} = \begin{cases} 6.47SoC + 60.66V_i - 9.84, & 0.80 \leq V_{i,pu} \leq 1.0 \\ 6.47SoC - 48.39V_i^2 + 112.12V_i - 14.84 & 1.0 < V_{i,pu} \leq 1.20 \end{cases} \quad (5.6)$$

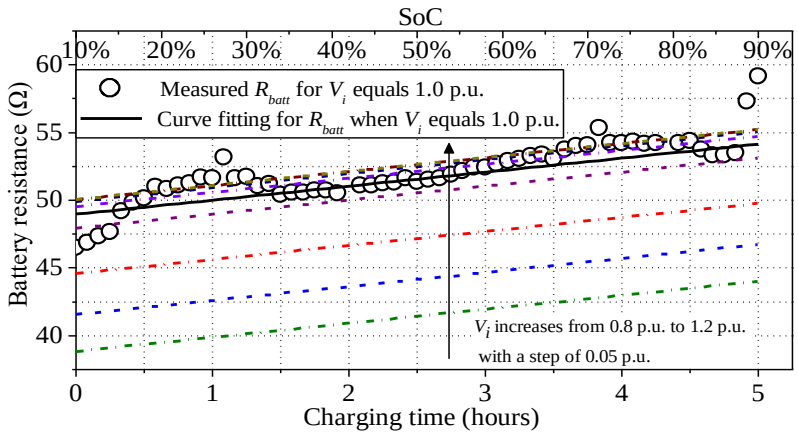



**Figure 5.19:** Measured battery resistance during CC charging mode.

As illustrated in Figure 5.19, the increase of $R_{batt}$ with the increasing $V_i$, is much faster when $V_i$ is below 0.95 p.u. than $V_i$ is above 0.95 p.u., implying the necessity of dividing the relationship between $R_{batt}$ and $V_i$ into two operations, as indicated in (5.6). It is because the tested EVBC turns from the constant current load type to the constant power load type when the $V_i$ is above 0.95-1 p.u., indicating that $R_{batt}$ will increase linearly with the increase of $V_i$ when it is below 0.95-1 p.u. and will remain approximately constant when $V_i$ is above 0.95-1 p.u. (assuming constant power conversion efficiencies for different $V_i$ values).

**Equivalent circuit EVBC model of CC mode**

As the full circuit EVBC model requires the modelling of relatively complex electronic circuits and the high computational burdens result in relatively long simulation times, an equivalent circuit EVBC model is proposed in this section with the back-end circuit represented by an analytical expression for the equivalent time-variable resistance, $R_{eq}$, as illustrated in Figure 5.14. Specifically, $R_{eq}$ is calculated by dividing the instantaneous dc-link voltage with the dc-link current from the full circuit EVBC model simulated under a combination of different battery SoC (increase from 26% to 90% with a step of 16%) and different input voltage magnitudes (increase from 0.8 p.u. to 1.2 p.u. with a step of 0.05 p.u.), as shown in Figure 5.20. It is observed that $R_{eq}$ almost linearly increase with the increasing dc-link voltage, $v_{dc}$, and its general equation can be easily obtained through curve fitting as given in (5.7).

$$R_{eq} = (0.013SoC + 0.117)v_{dc} + 0.216SoC^2 + 0.0845SoC + 0.268 \qquad (5.7)$$

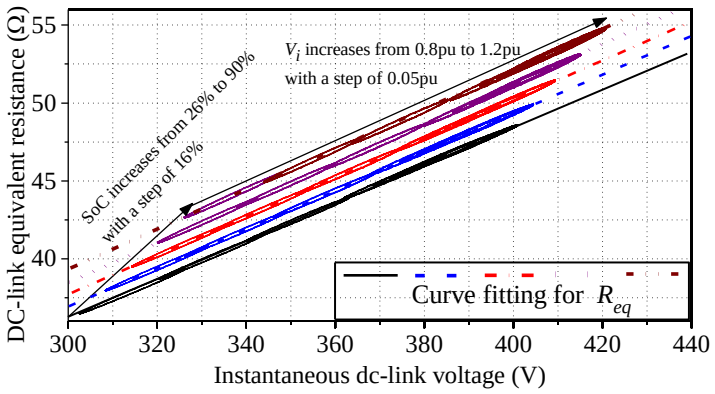
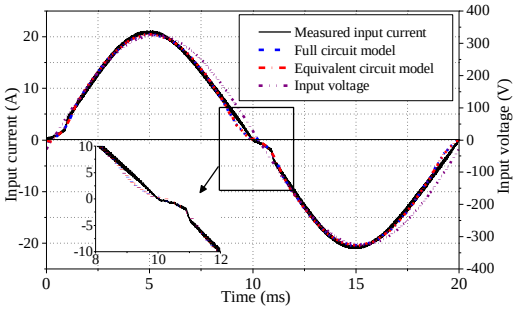



**Figure 5.20:** The relationship between the equivalent resistance ($R_{eq}$) and dc-link voltage ($v_0$) under 0.8-1.2 p.u. sinusoidal input ac voltage.

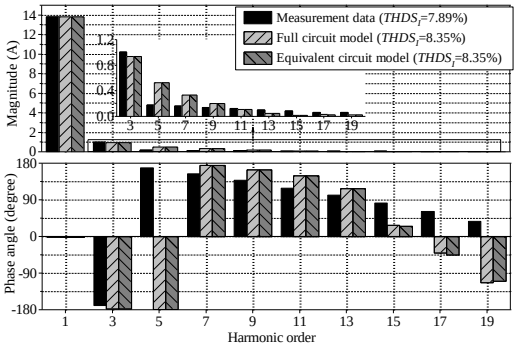
**Validation of the full circuit and equivalent circuit EVBC models of CC mode**

In this subsection, the developed full circuit and equivalent circuit EVBC models will be validated by comparing the simulation results with the measurement data of selected EVBC. Here, the simulated input ac current is compared with the measured one in both time-domain and frequency-domain under a combination of different input voltage distortion and voltage magnitudes. Specifically, three supply voltage waveforms are considered, including ideally sinusoidal, "flat-top" and "pointed-top" waveforms as defined in Section 5.2, with the voltage magnitude adjusted from 0.8 p.u. to 1.2 p.u. with a step of 0.05 p.u.

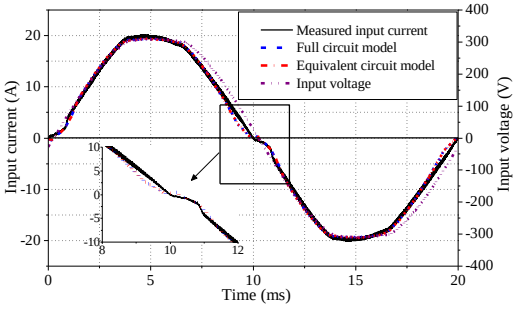
Figure 5.21 compares the simulated input ac current of the two models with the measured one under the three considered voltage waveforms with the magnitude of 1 p.u. It turns out that both the full circuit model and the equivalent circuit model can sufficiently accurately represent the input ac current waveform distortion of modelled EVBC operating under comprehensive supply conditions. To further validate the model, the simulated voltage-dependency of selected electrical characteristics including active power ($P$), fundamental reactive power ($Q_1$), true power factor ($PF$), displacement power factor ($PF_1$), distortion power factor ($PF_d$) and total subgroup current harmonic distortion ($THDS_I$), is compared with the measured one for voltage range of 0.8 p.u. to 1.2 p.u., as illustrated in Figure 5.22. Again, a good matching is achieved between the simulation results of the two models and the measurement data.



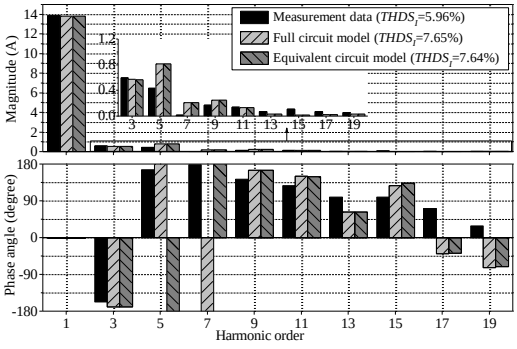

a) instantaneous input current waveforms under WF1



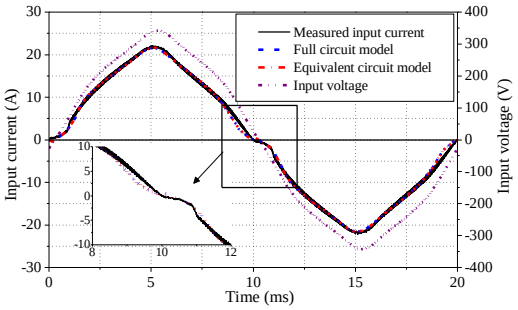

b) input current harmonics under WF1



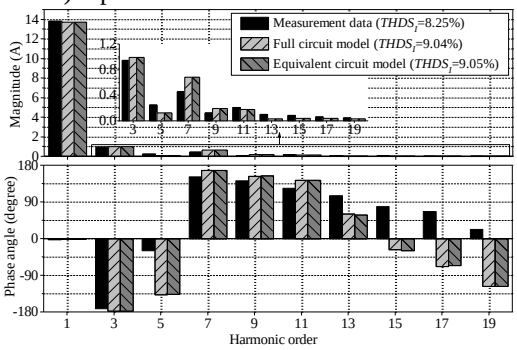

c) instantaneous input current waveforms under WF2




d) input current harmonics under WF2

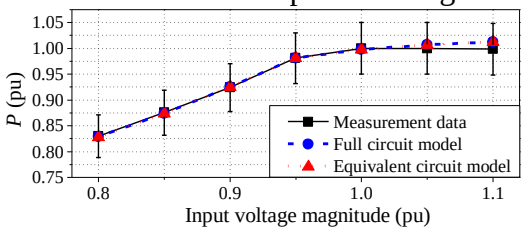



e) instantaneous input current waveforms under WF3

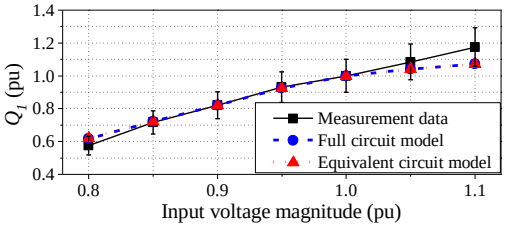



f) input current harmonics under WF3

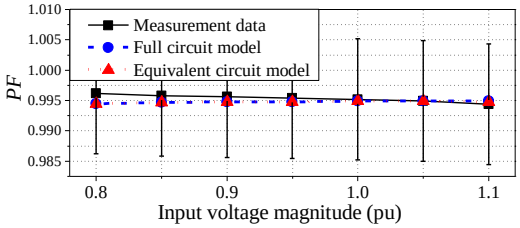
**Figure 5.21:** Comparison of measured and simulated input ac currents for the three considered input ac voltage waveforms with magnitude of 1 p.u.



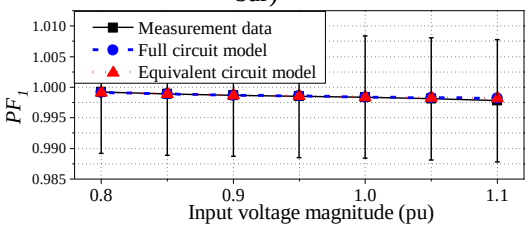

a) active power (with 5% error bar)



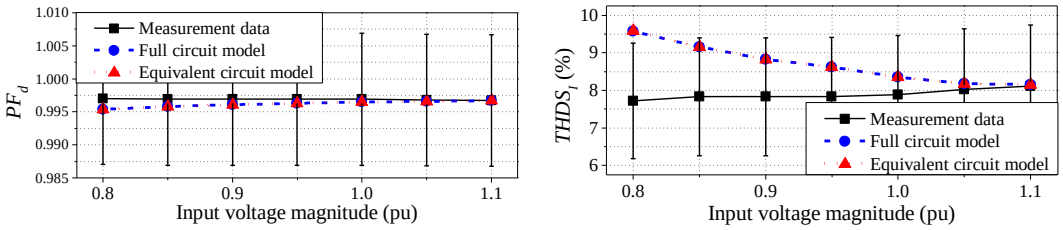

b) fundamental reactive power (with 10% error bar)




c) true power factor (with 1% error bar)




d) displacement power factor (with 1% error bar)




e) distortion power factor (with 1% error bar)

f) total current harmonic distortion (with 20% error bar)

**Figure 5.22:** Comparison of selected electrical characteristics derived from measurement and simulation data (for 0.8 p.u. to 1.1 p.u. sinusoidal input voltages).

**EVBC model of CV mode**

As CC mode charging is the main charging period of the whole CCCV charging process, the EVBC model of CV mode will only be briefly discussed in this section. The only difference between EVBC model of CC mode and EVBC model of CV mode is the slight adjustment of the a-PFC control circuit. Specifically, the peak values for the upper boundary and lower boundary of the inductor current ($\hat{I}_{L,upper}$and $\hat{I}_{L,lower}$) are not only determined by the rms value of supply voltage magnitude ($V_{AC,rms}$), but also affected by the EVBC operating power ($P\%$) which gradually decreases with the increase of battery SoC of EV at CV charging mode, as illustrated in Figure 5.23. The relationship among $V_{AC,rms}$, $P\%$, $\hat{I}_{L,upper}$and $\hat{I}_{L,lower}$ is represented by (5.8-5.10). The corresponding power dependency of battery resistance is illustrated in Figure 5.24 and is implemented in the full circuit EVBC model through a lookup table approach.

$$I_{AC,rms,ref} = 3.33e^{-4}V_{AC,rms}^2 - 0.186V_{AC,rms} + 0.126P + 25.24 \quad (5.8)$$

$$\hat{I}_{L,upper} = (\frac{\hat{V}_{AC.upper}}{V_{AC,rms}} + 0.174) \times I_{AC,rms,ref} \quad (5.9)$$

$$\hat{I}_{L,upper} = 0.55\hat{I}_{L,upper} \quad (5.10)$$

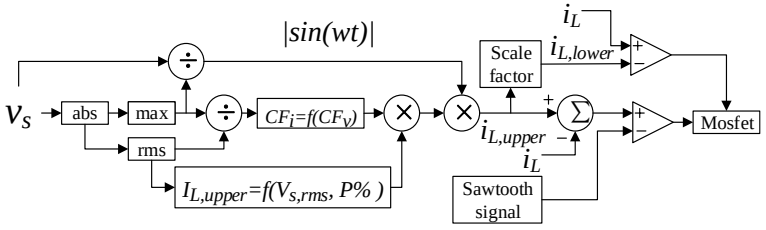



**Figure 5.23:** The block diagram of a-PFC control applied to the EVBC model of CV mode ($CF_v$ and $CF_i$ refer to the crest factor of voltage and current waveform respectively).

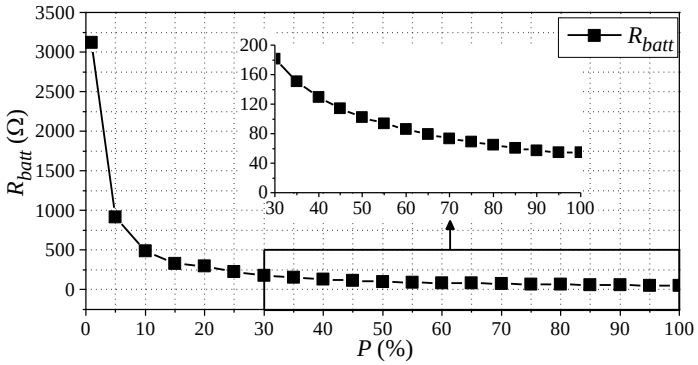
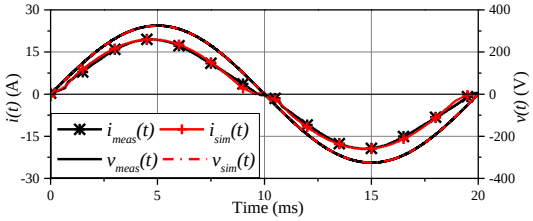
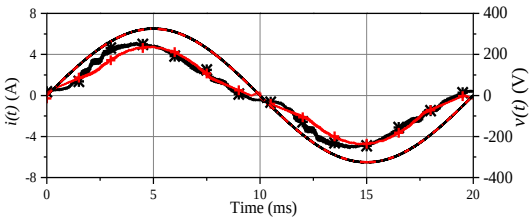



**Figure 5.24:** The power dependency of the battery resistance, $R_{batt}$, for EV of CV mode.

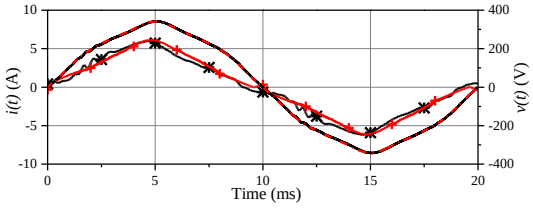
By applying the modified a-PFC control circuit and the adjusted $R_{batt}$ at different power levels, the full circuit EVBC model of CV mode can be obtained, with the comparison of input ac current waveform between measurement and simulation results illustrated in Figure 5.25. It is observed from Figure 5.25 that the developed EVBC model of CV mode is able to correctly represent the power-dependent waveform distortion characteristics of CV mode EVBC under different supply conditions.




a) input ac voltage, *v(t)*, and current, *i(t)*, at 100% $P_{rated}$ under WF1 and ZS1




b) input ac voltage, *v(t)*, and current, *i(t)*, at 25% $P_{rated}$ under WF1 and ZS1

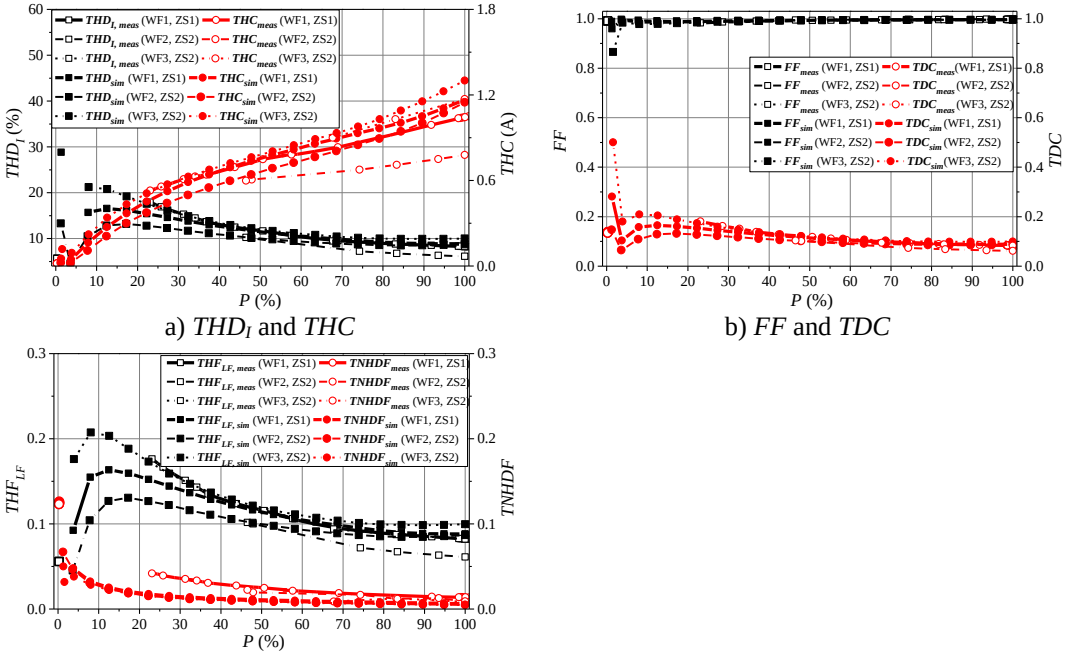



c) input ac voltage, *v(t)*, and current, *i(t)*, at 25% $P_{rated}$ under WF3 and ZS2

**Figure 5.25:** The comparison of time-domain input ac voltage and current waveforms between measurement ("meas") and simulation ("sim") results for EVBC model of CV mode.

To further investigate the accuracy of the developed EVBC model of CV mode, the waveform distortion indices including $THD_I$, *THC*, *FF*, *TDC*, $THF_{LF}$ and *TNHDF* are compared between the measurement and simulation results under a combination of different supply conditions and operating powers, as illustrated in Figure 5.26. It turns

out that the developed EVBC model of CV mode can indeed well represent the current harmonic emission characteristic of the selected EV for its whole CV charging period.




a) $THD_I$ and $THC$ b) $FF$ and $TDC$

c) $THF_{LF}$ and $TNHDF$

**Figure 5.26:** Comparison of measured ("meas", hollow symbols) and simulated ("sim", solid symbols) waveform distortion indices (including $THD_I$, $THC$, $FF$, $TDC$, $THF_{LF}$ and $TNHDF$) for EVBC of CV mode.

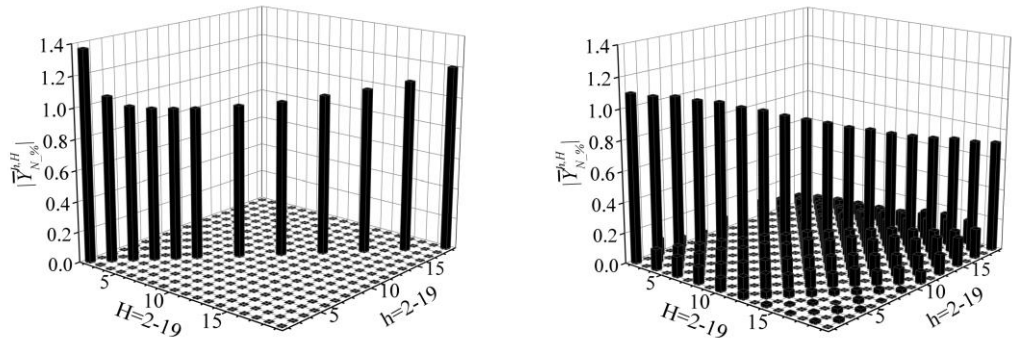
## 5.4.2 Frequency-domain modelling

For EVBC operating at CC mode, the input ac power remains constant at its rated charging power (i.e. does not change with the battery SoC), while for EVBC operating at CV mode, the input ac power will gradually decrease from the rated charging power to the cut-off value (e.g. 5% $P_{rated}$). Accordingly, the FDM is developed separately for EVBC of CC mode and EVBC of CV mode. Here, the FDM for EVBC refers to the CHNM introduced in Chapter 2.

### FDM for EVBC of CC mode

Similar with the development of FDMs for LEDs and SMPS' in Chapters 3-4, the development of FDM for EVBC is also based on the individual voltage harmonic tests, referring to sinusoidal supply voltage superimposed with individual voltage harmonic with varying magnitudes and phase angles. The considered voltage harmonic orders are 3$^{rd}$-19$^{th}$ odd order harmonics and 2$^{nd}$-6$^{th}$ even order harmonics. For each individual voltage harmonic order, the phase angle is adjusted from 0° to 330° in steps of 30°,

with respect to the zero crossing of fundamental component, while the harmonic magnitude is adjusted from 0.1x$V_{h,limit}$ to 1.2x$V_{h,limit}$ in steps of 0.1x$V_{h,limit}$, where $V_{h,limit}$ is the corresponding limit value from [40]. Accordingly, for each individual voltage harmonic, there would be 144 different tests. By applying the model development procedure given in Chapter 2, the CHNM for EVBC of CC mode can be easily obtained, with the corresponding $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,H}}$ indicated in Figure 5.27(a). Alternatively, the CHNM can be obtained by applying simulated individual voltage harmonic tests to the developed CBM given in Section 5.4.1, with the obtained $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,H}}$ illustrated in Figure 5.27(b) ($8^{th}$-$18^{th}$ even order harmonics are also taken into account). By comparing Figure 5.27(a) with Figure 5.27(b), it turns out that $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,H}}$ obtained from measurement and $\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,H}}$ obtained from CBM have very close values, especially for the diagonal elements.

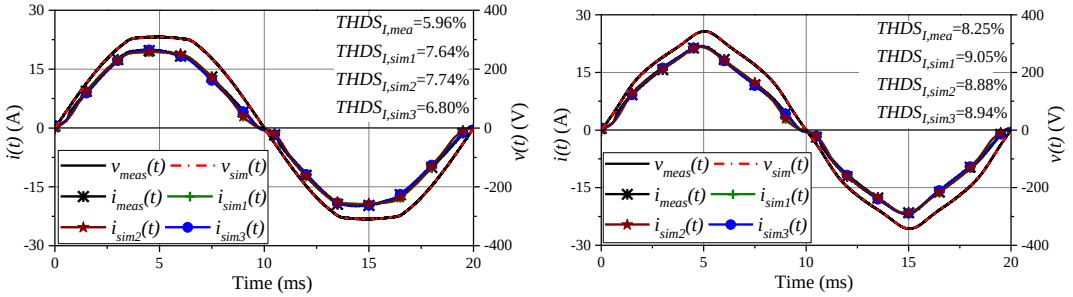



a) $|\bar{\boldsymbol{Y}}_{\boldsymbol{N_\%}}^{\boldsymbol{h,H}}|$obtained from laboratory individual harmonic tests

b) $|\bar{\boldsymbol{Y}}_{\boldsymbol{N_\%}}^{\boldsymbol{h,H}}|$obtained from component-based EVBC model (at CC charging mode)

**Figure 5.27:** Comparison of $|\bar{\boldsymbol{Y}}_{\boldsymbol{N\_\%}}^{\boldsymbol{h,H}}|$ obtained from the laboratory individual harmonic tests (EVBC of CC mode) and the component-based EVBC model of CC mode.

The comparison of the time-domain input ac current waveform among measurement (denoted as "mea"), simulation results by using CBM, CBM derived FDM, and measurement derived FDM (denoted as "sim1", "sim2" and "sim3" respectively) are illustrated in Figure 5.28. It turns out that all the three models can well represent the current waveform distortion characteristics for EVBC operating at CC mode with comprehensive supply conditions.

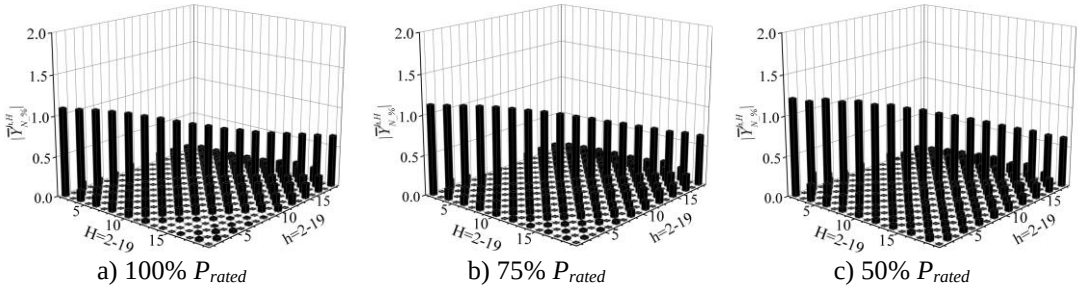



a) $v(t)$ and $i(t)$ at WF2, ZS2 b) $v(t)$ and $i(t)$ at WF3, ZS2

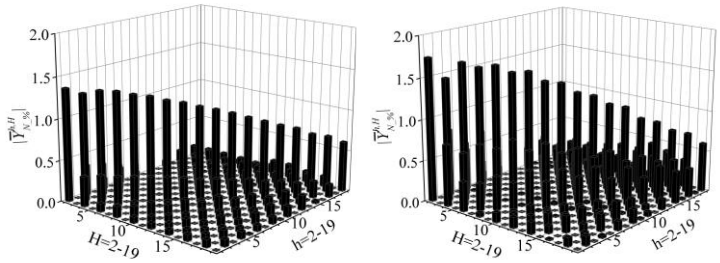
**Figure 5.28:** Comparison between measured and simulated grid-side current waveforms from different models for EVBC operating at CC mode.

**FDM for EVBC of CV mode**

When EVBC is operating at CV mode, the input current waveform distortion will vary with the decrease of operating power, as illustrated in Figure 5.26. Accordingly, the FDM for EVBC of CV mode has to be developed at different power levels, in order to take into account the power dependency of input current distortion. Considering the fact that the operating power gradually decreases with the increase of battery SoC for EV under CV charging mode, it is infeasible to perform individual voltage harmonic tests with the EVBC operating power maintained at a constant value. Accordingly, simulated individual voltage harmonic tests are performed to the developed CBM for EVBC of CV mode, with the obtained $\bar{\boldsymbol{Y}}_{\boldsymbol{N}\_\%}^{\boldsymbol{h,H}}$ at different powers illustrated in Figure 5.29. It turns out that the diagonal elements of $|\bar{\boldsymbol{Y}}_{\boldsymbol{N}\_\%}^{\boldsymbol{h,H}}|$ have the highest magnitudes, implying that individual current harmonics are mainly determined by the individual voltage harmonics of the same order. In addition, the magnitudes of the matrix elements gradually increase with the decrease of the operating power. To validate the accuracy of developed model, the comparison of time-domain current waveforms among measurements, simulation results by using CBM and CBM derived FDM is illustrated Figure 5.30. Again, good accuracy is achieved by all the models.

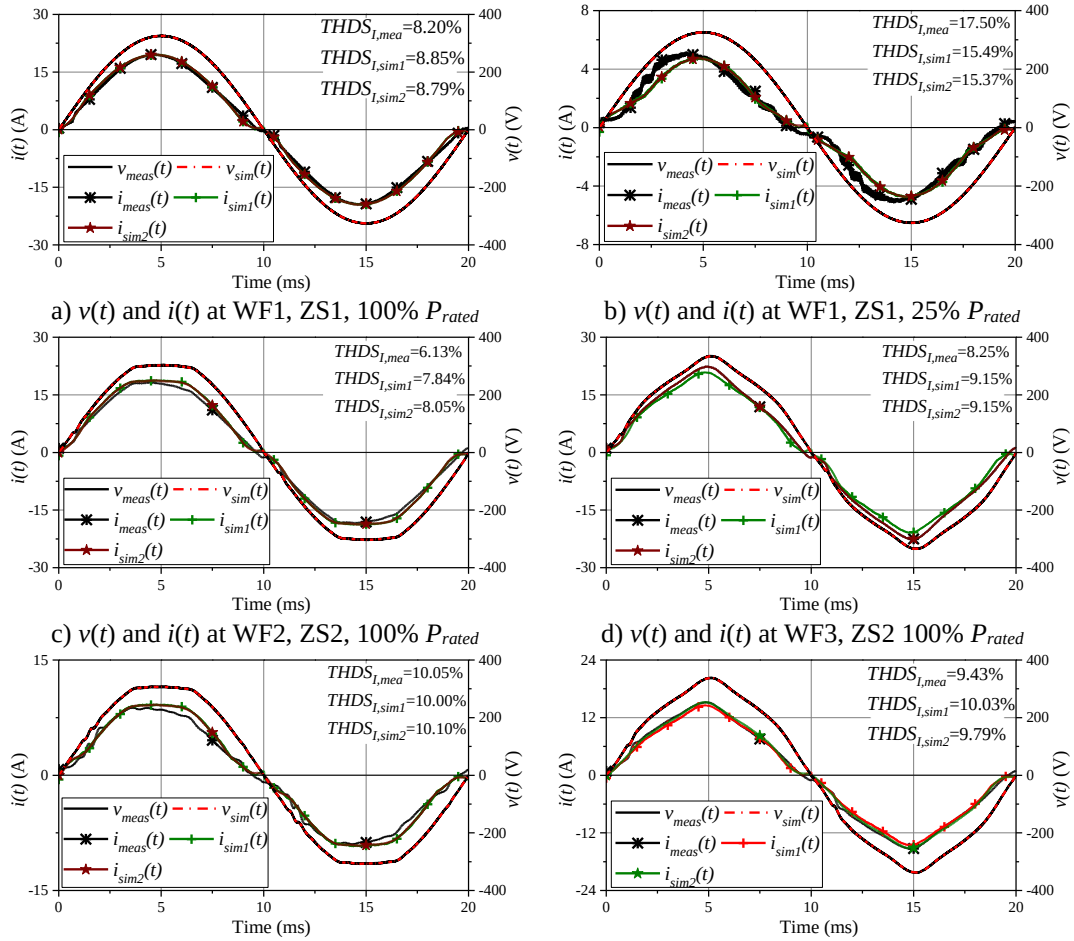



a) 100% $P_{rated}$ b) 75% $P_{rated}$ c) 50% $P_{rated}$




d) 25% $P_{rated}$ e) 10% $P_{rated}$

**Figure 5.29:** $|\overline{Y}^{h,H}_{N\_\%}|$ obtained from the component-based EVBC model of CV mode with different % $P_{rated}$.




a) $v(t)$ and $i(t)$ at WF1, ZS1, 100% $P_{rated}$ b) $v(t)$ and $i(t)$ at WF1, ZS1, 25% $P_{rated}$

c) $v(t)$ and $i(t)$ at WF2, ZS2, 100% $P_{rated}$ d) $v(t)$ and $i(t)$ at WF3, ZS2 100% $P_{rated}$

e) $v(t)$ and $i(t)$ at WF2, ZS2, 50% $P_{rated}$ f) $v(t)$ and $i(t)$ at WF3, ZS2, 70% $P_{rated}$

**Figure 5.30:** Comparison between measured and simulated grid-side current waveforms from different models for EVBC of CV mode.

## 5.5 Comparison between CBMs and FDMs in the case of EVBC harmonic modelling

As CBMs and FDMs are the two dominant harmonic modelling approached for modern PE devices, their characteristics and performance will be further discussed in the case of EVBC modelling. As mentioned in Section 5.4, CBMs require a detailed prior knowledge on the circuit topologies, related control circuits and the functionality

of the main circuit parts, while FDMs represent the harmonic emission of the modelled device via an assumed or postulated model with the model parameters directly obtained from predefined measurements. The difference of the input data requirement between CBMs and FDMs will result in their distinctive applicability and performance, which will be fully discussed in the following.

### 5.5.1 Required input information

**CBMs for EVBC**

According to the literature review on EVBC modelling (e.g. [133], [134]), it turns out that a typical circuit topology of an on-board, Level 2, unidirectional EVBC has an a-PFC based boost converter as the front-end circuit, which is modelled for operation in a continuous conduction mode with modified peak current control in this chapter. For the back-end circuit, a full-bridge DC-DC converter is implemented to the developed EVBC model, regulating the charging voltage and current fed to the battery. The corresponding CBM of EVBC features a relatively complex and sophisticated electrical/electronic and control circuit, as represented by the circuit schematic shown in Figure 5.14.

In general, developing CBM for EVBC does not rely on extensive measurements, but need detailed information on the applied circuit topology and the corresponding control circuits. Preferably, this kind of information can be provided by the EV charger manufacturer. Another option is to perform a thorough inspection of the actual EV charger circuits, with the obtained data on the main circuit components and connections transferred to the simulation environment. However, detailed circuit inspection of EVBC circuit may still not be able to know the actual settings of certain non-user-settable control parameters which are typically packaged inside chips. To solve that issue, a series of dedicated, but typically not too extensive measurements can be performed to estimate those control parameters.

For the purpose of finely tuning the model as well as the final model validation, some measurements (e.g. the time-domain input ac voltage and current waveforms) of the modelled EVBC are required. Furthermore, as the EV battery is directly connected with EVBC, the electrical behaviours of the battery during the whole charging process should also be taken into account for correctly evaluating the performance of

developed EVBC. Although the majority of commercial EVs are equipped with Li-ion batteries, the electrical characteristics of EV batteries normally vary within different battery manufacturers. Accordingly, the development of an accurate EVBC requires a proper representation of the battery, which essentially relies on measurements.

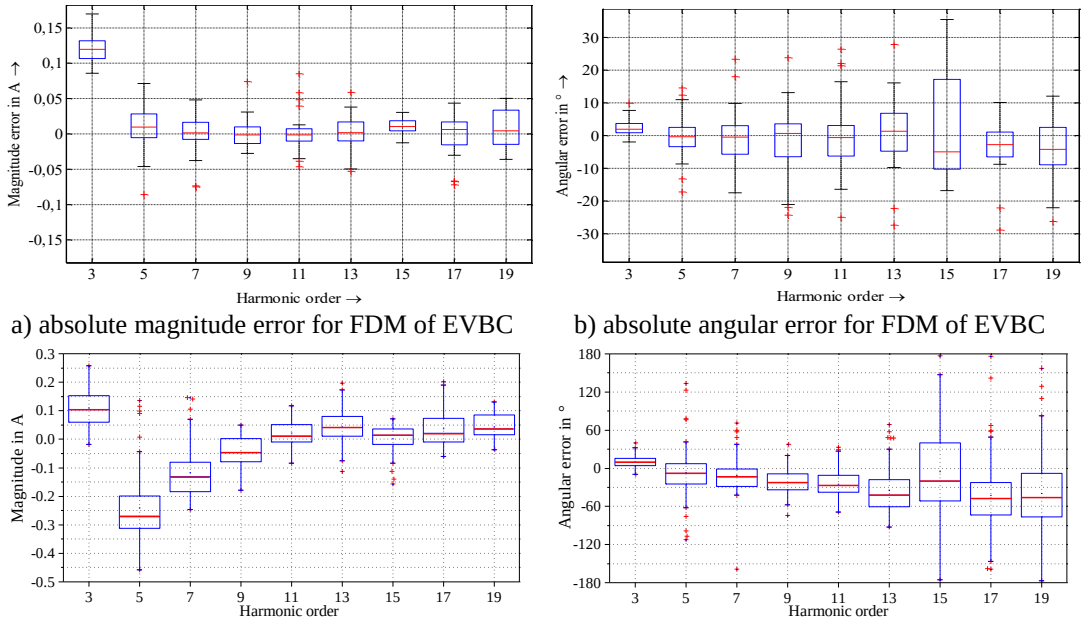
**FDMs for EVBC**

FDMs generally do not require the circuit information of the modelled device and treat the device as a "black box". However, for devices having multiple operating modes or states, information on those operating states can improve the model development efficiency by reducing the numbers of total required tests and measurements. All the tests can be fully automated without any user interactions. The characterization process for modelled devices is modularized and is made up of modules for investigating the device response to different supply conditions, including unbalance, magnitude of supply voltage, LV and HF harmonic distortions, etc.

For the FDMs for EVBC given in Section 5.4.2, the LF harmonic distortion module consists of around 2,000 individual measurement points with different harmonic contents of the supply voltage. Firstly, to obtain the reference current harmonic spectrum of modelled device, a single measurement is performed for the device operating under ideal supply condition (i.e. ideally sinusoidal supply voltage with a magnitude of 1 p.u.). Secondly, to investigate the voltage harmonic dependency of current harmonics of the same and different orders, a harmonic fingerprint analysis is performed, where each individual harmonic voltage is stepwise changed in magnitude and phase angle. Thirdly, the voltage band test is performed to obtain the fundamental voltage dependency of current harmonics, where the supply voltage is purely sinusoidal with a stepwise adjustment of voltage magnitude. With the above measurements, it is able to easily obtain the parameter values of FDM. Typically, FDMs only take into account LF harmonics (e.g. up to $20^{th}$ order in the developed FDMs for EVBC).

### 5.5.2 Comparison of single models

In this section, the performance comparison between CBMs and FDMs (measurement derived CHNM) is demonstrated on the case of EVBC modelling, based on the model accuracy under 50 randomly selected voltage waveforms with different voltage harmonic spectrums. Specifically, the CBM and FDM for EVBC of CC mode in Section 5.4 are applied with 50 different voltage waveforms containing multiple LF harmonics (e.g. the most common orders 3 and 5). For each of the 50 tests, the simulated current harmonics of CBM and FDM are compared with the corresponding measured current harmonics, with the absolute magnitude error and the absolute angular error illustrated in Figure 5.31 and several statistical indices tabulated in Table 5.3. For the boxplot, the blue rectangles mark the 25$^{th}$ and 75$^{th}$ percentiles, while the 50$^{th}$ percentile (i.e. the median) is represented by the red bars in the box. The lower and upper black bars mark the 5$^{th}$ and 95$^{th}$ percentiles respectively, with the outliers indicated by the red crosses. The comparison of time-domain and frequency-domain input ac current for one selected voltage waveform is shown in Figure 5.32. It turns out both FDM and CBM are capable of accurately representing the voltage harmonic dependency of current harmonics in the case of EVBC modelling, while FDM has relatively better accuracy as opposed to CBM.



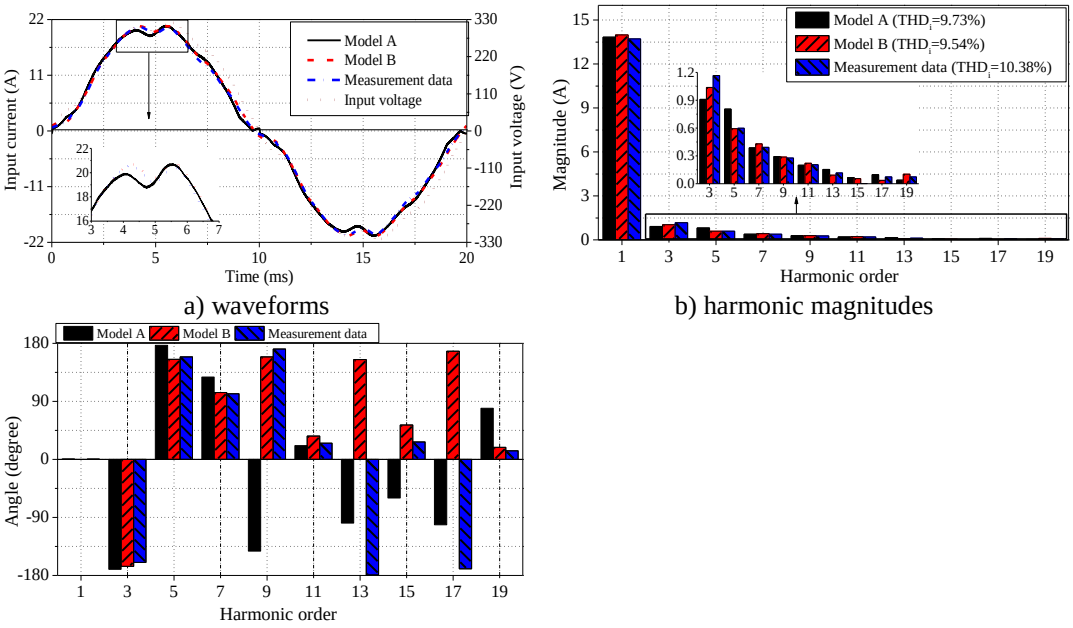

a) absolute magnitude error for FDM of EVBC b) absolute angular error for FDM of EVBC

c) absolute magnitude error for CBM of EVBC d) absolute angular error for CBM of EVBC

**Figure 5.31:** Comparison of the absolute magnitude error and the absolute angular error between FDM and CBM for EVBC of CC mode.

**Table 5.3:** The minimum, maximum, median and 90th percentile values of the absolute magnitude error and the absolute angular error for FDM and CBM of EVBC under CC mode (Model A and B refer to CBM and FDM respectively).

| | | Min | Max | Median | 90th percentile |
|---|---|---|---|---|---|
| $THD_I$ (%) | **Model A** | 0.03 | 1.49 | 0.38 | 1.11 |
| | **Model B** | 0.23 | 1.11 | 0.69 | 0.89 |
| **H3_mag (A)** | **Model A** | 0.00 | 0.26 | 0.10 | 0.23 |
| | **Model B** | 0.06 | 0.20 | 0.12 | 0.16 |
| **H3_ang (°)** | **Model A** | 0.46 | 32.20 | 9.86 | 17.30 |
| | **Model B** | 0.05 | 9.44 | 2.20 | 4.82 |
| **H5_mag (A)** | **Model A** | 0.01 | 0.46 | 0.26 | 0.40 |
| | **Model B** | 0.00 | 0.08 | 0.02 | 0.04 |
| **H5_ang (°)** | **Model A** | 0.04 | 146.82 | 17.68 | 86.87 |
| | **Model B** | 0.08 | 52.70 | 2.99 | 12.38 |




a) waveforms

b) harmonic magnitudes

c) harmonic phase angles

**Figure 5.32:** Comparison of time and frequency domain model characteristics for one selected voltage waveform (Model A and B refer to CBM and FDM respectively).

## 5.5.3 Comparison for multiple model instances

To compare the performance of the FDM and CBM for network harmonic analysis, a simple but realistic network model is used, as shown in Figure 5.33. It is a simplified LV network model and is made up of a voltage source representing the 11 kV MV network, a 11 kV to 400 V delta-wye distribution transformer with rated power of 200 kVA (Dyn5; uk=6%) and two buses (A and B) connected by Cable 1 (200m of 4x150mm²) and Cable 2 (100m of 4x50mm²). In addition, the MV network has a short

circuit power of 113 MVA at 79°, corresponding to a source impedance of (0.205+1.046j) Ω. To reflect the background distortions in typical UK and German LV networks, a typical value for the 5$^{th}$ harmonic (2% of the fundamental component with a phase angle of 30°) is superimposed to the ideal supply voltage source at 11 kV. As shown in Figure 5.33, 10 houses and 2 EVs are connected to each phase of Bus A and Bus B respectively, for investigating the impact EV charging on the resulting voltage and current distortions, as well as the harmonic interaction between EVs and houses.

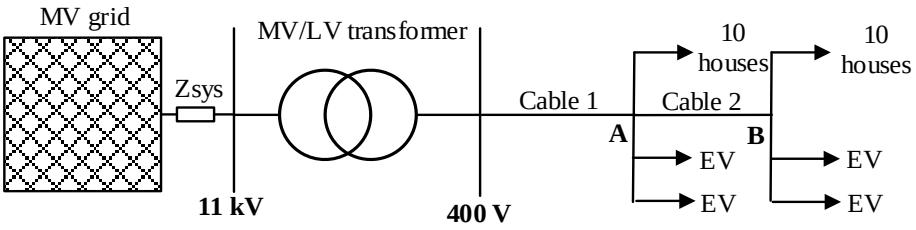



**Figure 5.33:** Configuration of the test grid.

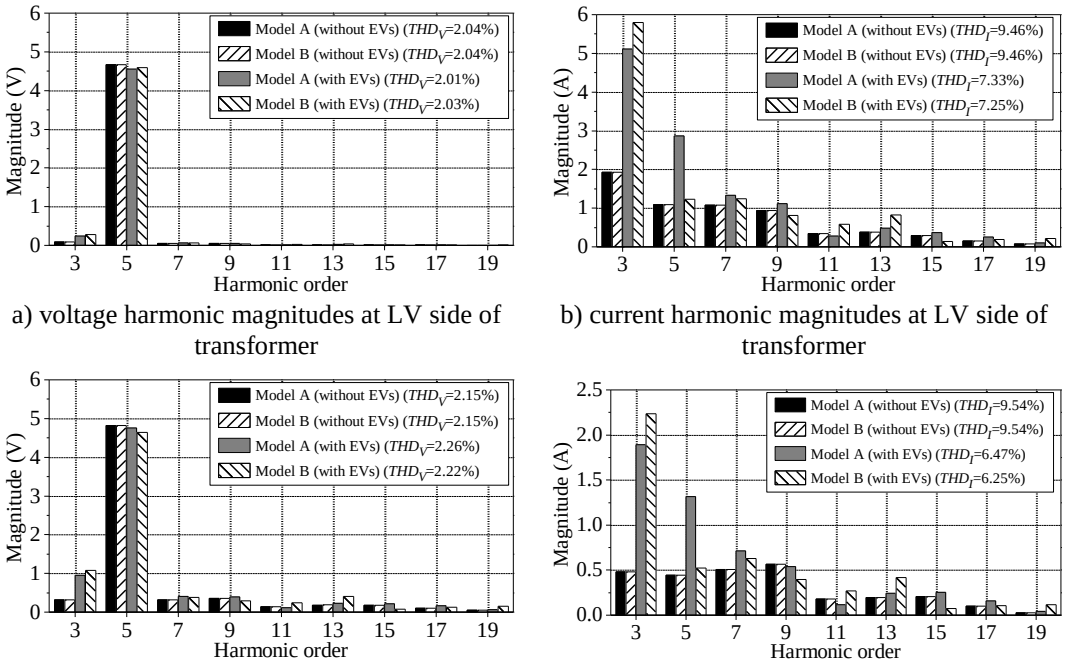
The network is implemented in Matlab/Simulink with houses represented by constant current source with fixed harmonic spectrum and EVs represented by CBM and FDM developed in Section 5.4 respectively. The current harmonics of the lumped 10 houses at Bus A and Bus B are different, with the harmonic magnitudes and phase angles tabulated in tabulated in Table 5.4.

**Table 5.4:** The current harmonic spectrum of the lumped 10 houses at Bus A and Bus B respectively.

| | **Order** | **1** | **3** | **5** | **7** | **9** | **11** | **13** | **15** | **17** | **19** |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Magnitude (A)** | **Bus A** | 17.52 | 1.57 | 0.72 | 0.58 | 0.41 | 0.17 | 0.18 | 0.08 | 0.05 | 0.05 |
| | **Bus B** | 11.13 | 0.48 | 0.45 | 0.51 | 0.56 | 0.18 | 0.19 | 0.21 | 0.10 | 0.03 |
| **Angle (°C)** | **Bus A** | -0.18 | 172.51 | -59.98 | 85.39 | -76.52 | 78.68 | 146.50 | -46.48 | -2.32 | -157.14 |
| | **Bus B** | -8.89 | 124.44 | -15.92 | 99.46 | -47.25 | 60.27 | 145.98 | -52.25 | 2.83 | -177.88 |

The simulation times required to reach steady state by using CBM for EVBC and FDM for EVBC are 960 seconds and 4 seconds respectively, with the obtained voltage and current harmonic magnitudes at the LV side of transformer and Bus B illustrated in Figure 5.34. It turns out that both CBM and FDM for EVBC have very close simulation results, in terms of the voltage and current waveform distortions (represented by $THD_V$ and $THD_I$ respectively) at the transformer secondary side and Bus B. In terms of considered individual voltage and current harmonics, a good matching is achieved

between CBM and FDM while CBM results in higher 5$^{th}$ current harmonic as opposed to FDM.




a) voltage harmonic magnitudes at LV side of transformer

b) current harmonic magnitudes at LV side of transformer

c) voltage harmonic magnitudes at Bus B

d) current harmonic magnitudes at Bus B

**Figure 5.34:** The voltage and current harmonics magnitudes at LV side of transformer and Bus B (Model A and B refer to CBM and FDM for EVBC respectively).

## 5.5.4 Summary

Based on the above discussion and analysis, it shows that both CBMs and FDMs have their own strengths and weaknesses, which is summarised in the following for providing a broad guideline for the selection of proper harmonic modelling approaches.

*Harmonic coverage:* FDMs normally only cover the specified harmonic orders without taking into account other non-harmonic distortions (e.g. interharmonics and subharmonics) and high frequency harmonics. However, properly designed CBMs should be able to well represent all kinds of distortions of the modelled device.

*Input data:* CBMs require a priori knowledge of the circuit topologies and the main circuit parameter values which are typically difficult to obtain, while FDMs do not require the detailed circuit information, but rely on extensive measurements.

*Development time:* The development time for CBM is mainly determined by two factors including the complexity of the circuit for the modelled device and the availability of the information on the circuit details. For PE devices with simple circuit topologies (e.g. full-wave rectifier based CFL), their CBMs can be easily obtained due to their simple working principles (as discussed in Chapter 3). Considering the fact that modern PE devices (e.g. EVBCs and PVIs) are typically based on switched-mode converters and/or inverters which have complex circuit topologies and control algorithms, the development of CBMs normally takes more time than the development of FDMs, especially when the information on detailed circuits of the modelled device is not well known. For the development of FDMs, time is mainly spent on the individual harmonic tests and measurements for correctly assessing the voltage harmonic dependency of current harmonics. Once all the required measurements are obtained, the model parameter values for FDM can be easily derived.

*Accuracy:* The accuracy of CBMs is mainly determined by the availability of information on the circuits and main component parameter values. If all details are known, the develop CBMs will be able to capture most of the electrical characteristics of modelled PE devices under comprehensive working conditions, which is normally difficult to be achieved by FDMs. For FDMs, the model accuracy is not only determined by the reproducibility of the measurements, but also affected by the mathematical model form selected for FDMs. As typical FDMs refer to CHNMs or HFMs which assume the linear relationships between voltage and current harmonics, FDMs may not be suitable for PE devices whose current harmonics have highly nonlinear voltage harmonic dependency (e.g. CFL with a pulse-like input ac current).

*Simulation time:* As FDMs are based on RMS-based frequency-domain simulation and do not require the simulation of instantaneous current and voltages as CBMs do (typically as a part of an electro-magnetic transient simulator), the simulation time for FDMs is significantly less than CBMs.

*General applicability:* Due to the relatively high computation burdens and long simulation time of CBMs, direct application of CBMs for large-scale network simulation is infeasible. As properly developed CBMs should be able to capture the main electrical characteristics of modelled PE devices, they can be easily transferred

to different model forms (e.g. static ZIP and exponential models, FDMs) based on the specific network study objective. For FDMs, they are mainly applied for network harmonic analysis, and their application is limited to the harmonic orders specified in the model.

## 5.6 Chapter conclusions

This chapter starts with a discussion of the laboratory testing results 19 different on-board EVBCs operating under comprehensive supply conditions, with special attention given to the impact of varying supplying conditions on the harmonic emission and other general electric power quantities of tested EVBCs. It turns out that the considered electrical characteristics are quite diversified among tested EVBCs, and exhibit different supply voltage dependencies, implying that the impact of EV charging on the grid operation is closely related to the type of EVBCs. After that, both CBM and FDM are developed for the selected EVBC with both CC charging mode and CV charging taken into account.

To further compare the difference between CBM and FDM, the performance of developed CBM and FDM are investigated based on both 50 random tests and a simple but realistic LV network simulation. It turns out that the performance difference between CBM and FDM is mainly determined by the information available on the circuit of modelled EVBC. As EVBC normally has sophisticated circuits and controls which are difficult to be obtained, FDM is a better option for representing the harmonic emissions of EVBC as opposed to CBM, without requiring the detailed circuit information. Regarding the model accuracy, the accuracy of CBM is determined by how accurate the actual EVBC circuit is represented, while the accuracy of FDM is determined by the measurement error as well as the mathematical model formulation applied. The presented experimental and analytical results provide important information that could be directly used for investigating the impact of large-scale deployment of EVBCs on the operation of existing networks and future “smart grids”.

# Chapter 6

# Harmonic modelling and characterisation of PVIs

## 6.1 Introduction

As a type of renewable energy resources, solar energy is an ideal alternative energy supply for the electricity generation. Depending on whether the PV systems are grid-connected, they can be classified into two types: grid-connected (or utility interactive) PV systems and standalone PV systems [135]. As the grid-connected systems require less maintenance and are more cost-effective as opposed to standalone PV systems which are typically equipped with energy storage systems, grid-connected PV systems attract most of the public attention [136]. As opposed to standalone PV systems using batteries, more than 99% of the installed PV capacity is occupied by grid-connected PV systems [137]. Due to the combined effects of PV module cost reduction, economic incentives and policy support, grid-connected PV systems in the EU is accelerating its penetration into the grid in the recent years [17][138]. For example, the total installed capacity of PV systems in Germany is over 30 GW, while in the UK, it has increased from a few hundred MWs in 2010 to over 8 GW in 2015, with a projected growth to 10-13 GW by 2020 [138]. As a consequence, PV systems are widely connected to both transmission and distribution networks. The rated power of the grid-connected PV systems can vary from a hundred watts to several megawatts [139]. For the LV grid connections, residential-scale PV systems are typically installed on the rooftops of the buildings, with peak rated power up to 5-6 kW for the single-phase connections and 10-15 kW for the three-phase connections [140]. In this chapter, both the single-phase and three-phase residential-scale PV systems will be analysed.

With the cost reduction of residential-scale (below 10 kW) PV inverters (PVIs), their increasing penetration into LV networks of Europe is observed in the last decade. However, the distributed connection of large numbers of PVIs will change the conventional radial configuration of LV networks, resulting in increased complexity of the network operation [141]. Consequently, investigating the PQ impact of PVIs on LV networks has obtained great concern recently. For example, as the output power of

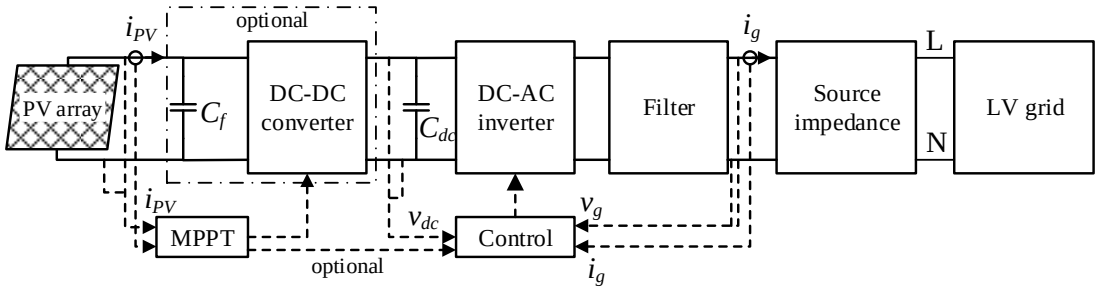
PVIs fed into the grid is not controlled and mainly determined by the instantaneous power absorbed by the connected PV panels from the sunlight, it may result in voltage flicker issue at the point of connection (PCC) [142][143]. Moreover, the randomly distributed single-phase PVI among the customers of the LV distribution network may aggravate the already existing voltage imbalance issue, resulting in a series of problems like no-characteristic harmonic emission from nonlinear loads, and improper network control systems [144]. Among all the possible PQ issues due to PVI connection, the investigation of current harmonic emission characteristics of PVIs under different operation conditions is the main concern in this chapter, and will be discussed based on the laboratory measurements of three commercial residential-scale PVIs.

Due to the working principle of grid-connected inverters, PVIs will emit current harmonics inherently. However, their current harmonic emission characteristics are affected by a series of factors which can be generally divided into two types-internal factors and external factors which are introduced in Chapter 2. Internal factors include the inverter topologies and the corresponding control strategies while the external factors mainly refer to the power level absorbed from the PV panels (i.e. the operating power of the inverters) and the supply conditions (referring to the supply grid impedance, supply voltage magnitude and waveform distortion) [145][146][147]. Accordingly, investigating the harmonic characteristics of PVIs not only require a deep understanding of the working principles of PVIs (can be achieved by the component-based modelling of PVIs), but also need detailed assessment of the impact of supply conditions and device operating powers on the harmonic emission of PVIs (can be achieved through proper laboratory testing). After fully understanding the harmonic emission characteristics of PVIs, it will be able to develop appropriate PVI models (both CBMs and FDMs) based on the laboratory tests and measurements of selected commercial PVIs. With the developed individual FDMs for several commercial PVIs, the frequency-domain aggregation approach is proposed in the last part of this chapter in order to investigate their large-scale deployment impact on the grid.

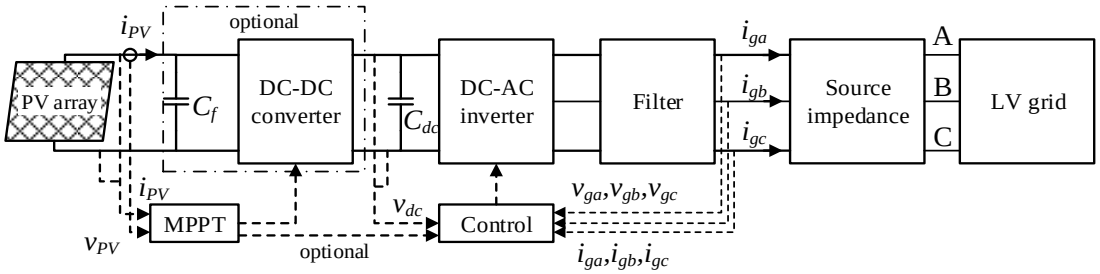
## 6.2 General circuit topologies and control of PVIs

In general, PVI topologies can be classified into different types based on the different criteria. For example, according to the existence of transformer (either HF transformer on the dc side or the line frequency transformer on the ac side), PVIs can be divided into isolated and non-isolated topologies [148]. Compared with the non-isolated PVIs, isolated PVIs have the advantage of providing galvanic isolation between the PV array and the grid, as well as avoiding dc current injection to the grid [149]. However, the addition of transformer will increase the cost, size and power losses of PVIs [149][150]. Accordingly, non-isolated PVIs can achieve lighter weight, smaller size, reduced cost and improved efficiency as opposed to isolated PVIs. For the residential-scale PVIs where the cost is a concern, transformerless PVIs are a better choice. Additionally, according to the existence of DC-DC converters between the PV array and the DC-AC inverter, PVIs can be divided into single-stage topology and multiple-stage (typically two-stage) topologies [151]. For the single-stage PVI, maximum power point tracking (MPPT) function is directly implemented on the DC-AC inverter while for the two-stage PVI, MPPT function is achieved by the DC-DC converters. Compared with the two-stage PVI, single-stage PVI is more reliable and cost-effective, even though it requires minimum voltage limits for the PV array (to avoid over-modulation of the DC-AC inverter) and larger dc-link capacitor (to suppress the dc-link voltage ripples) [151].

Typical transformerless PVI circuit configuration is illustrated in Figure 6.1, consisting of a PV array voltage output capacitor filter $C_f$, a DC-DC converter (optional), a dc-link capacitor $C_{dc}$, a DC-AC inverter and the output grid-side filter. In the following, the working principles of the main circuit parts will be fully analysed, as it is the basis for developing accurate circuit based PVI models in the next stage.




a) general configuration of single-phase transformerless PVI

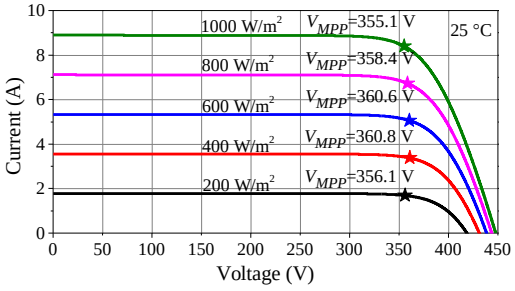



b) general configuration of three-phase transformerless PVI

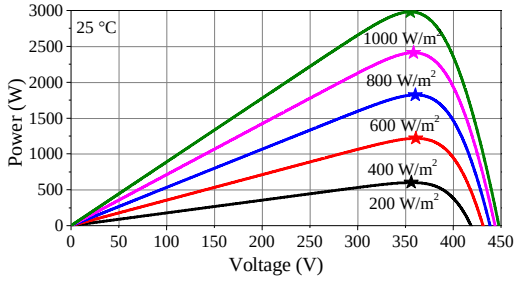
**Figure 6.1:** General circuit configuration of single-phase and three-phase PVIs.

## 6.2.1 DC-DC converter with MPPT function

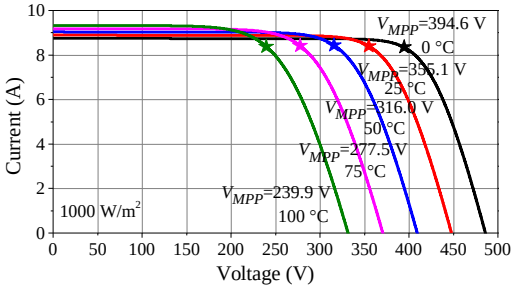
In order to achieve the maximum power output from the PV array operating at specific solar irradiance and ambient temperature, the voltage and current output from the PV array have to be continuously monitored by the MPPT controller which in turn maintains the voltage level of the PV array at $V_{mpp}$. An example illustrating the *I-V* and *P-V* relationship of a commercial PV array (consists of 10 series-connected PV modules with maximum power of 300 W for each module) is given in Figure 6.2. As shown in Figure 6.2, unique maximum power point (MPP) exists on the *I-V* and *P-V* curves where the highest power harvest is achieved, although its exact location on the curves varies with the change of sun irradiance and/or cell temperature.



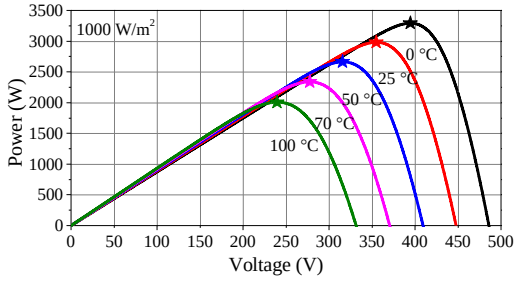

a) *I-V* characteristics of the PV array (200-1000 W/m², 25 °C)




b) *P-V* characteristics of the PV array (200-1000 W/m², 25 °C)




c) *I-V* characteristics of the PV array (0-100 °C, 1000 W/m²)




d) *P-V* characteristics of the PV array (0-100 °C, 1000 W/m²)

**Figure 6.2:** The *I-V* and *P-V* characteristics of a commercial PV array under different sun irradiance (in W/m2) and cell temperature (in °C).

According to the unique *I-V* and *P-V* characteristics of PV array, a variety of MPPT algorithms have been proposed, including constant voltage method [152][153], open-circuit voltage method [154][155][156], short-circuit current method [156][157], perturb and observe (P&O) method [158][159][160], incremental conductance (InC) method [160][161][162], fuzzy logic control method [163][164], Neural network method [165][166], et al. Among all those techniques, only the P&O method and the InC method are the two most widely used approaches for MPPT [167]. They can be implemented either on the DC-DC converter or directly on the DC-AC inverter as illustrated in Figure 6.1. In the following subsections, the working principles of the P&O MPPT and InC MPPT will be introduced, with their implementation approaches demonstrated on the boost converter modelling (with the two MPPT approaches applied separately) in Matlab/Simulink.

**P&O MPPT method and its implementation approach**

The flowchart of the P&O MPPT algorithm is illustrated in Figure 6.3. The main concept behind this approach is to perturb the voltage output of the PV array according to the observation of the change of PV array power output [160]. Specifically, the PV array power output $p_{pv}(t)$ at time $t$ is calculated from the monitored output voltage $v_{pv}(t)$ and current $i_{pv}(t)$ of the PV array. If $p_{pv}(t)$ equals $p_{pv}(t\text{-}t_s)$ which is the PV array power output at the last sample time, $v_{pv}(t)$ is at the MPP position (i.e. $v_{pv}(t)$ equals $V_{MPP}$). If both $p_{pv}(t)$ and $v_{pv}(t\text{-}t_s)$ are larger than their last sampled values, $v_{pv}(t)$ is in the left part region of the *P-V* curve (with respect to the MPP), and is moving right towards MPP, suggesting that the increasing trend of $v_{pv}$ should be maintained. If $p_{pv}(t)$ is larger than $p_{pv}(t\text{-}t_s)$ and $v_{pv}(t)$ is smaller than $v_{pv}(t\text{-}t_s)$, $v_{pv}(t)$ is in the right part region of the *P-V* curve, and is moving left towards MPP, implying $v_{pv}$ should keep the decreasing trend. On the other hand, if $p_{pv}(t)$ and $v_{pv}(t)$ are smaller than their last sampled values, $v_{pv}(t)$ is in the left part region of the *P-V* curve (with respect to the MPP), and is moving left away from MPP, suggesting that $v_{pv}$ should be perturbed to an opposite trend (i.e. increase $v_{pv}$). If $p_{pv}(t)$ is smaller than $p_{pv}(t\text{-}t_s)$ and $v_{pv}(t)$ is larger than $v_{pv}(t\text{-}t_s)$, $v_{pv}(t)$ is in the right part region of the *P-V* curve, and is moving right away from MPP, implying $v_{pv}$ should be decreased. The whole process is illustrated in Figure 6.4. In addition, When the MPPT is implemented on the boost converter, the increase of $v_{pv}$ is achieved

by the decrease of duty ratio ($D$) of the switch and the decrease of $v_{pv}$ is achieved by the increase of $D$, considering that fact that $v_{pv}$ equals $(1\text{-}D)v_{dc}$.

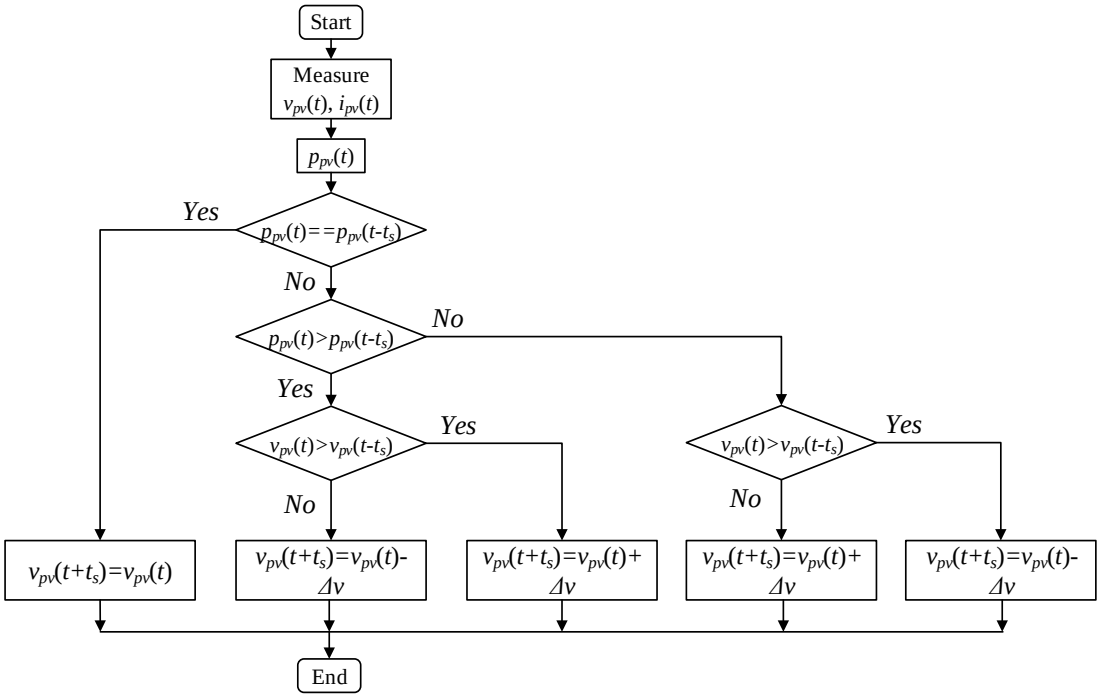



**Figure 6.3:** The flowchart of the P&O MPPT algorithm.

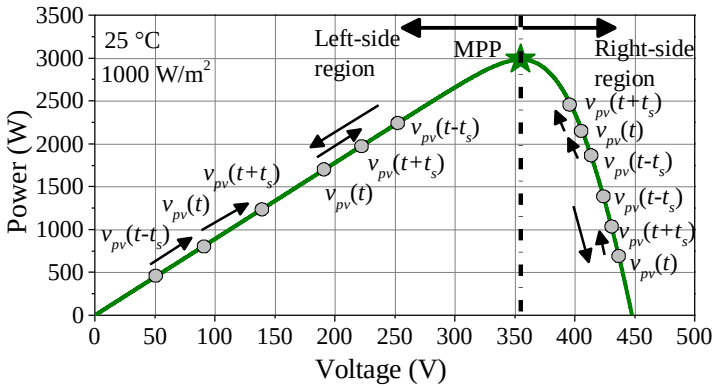



**Figure 6.4:** Illustration of the P&O MPPT algorithm on the *P-V* curve.

In order to implement the P&O MPPT effectively, the algorithm in Figure 6.3 can be equivalent to the form shown in Figure 6.5, with the implementation approach demonstrated on the boost converter modelling in Matlab/Simulink. The circuit schematic of the MPPT based boost converter model and the corresponding block diagram of the implementation of P&O MPPT approach are shown in Figure 6.6 with the key circuit parameter values given in Table 6.1.

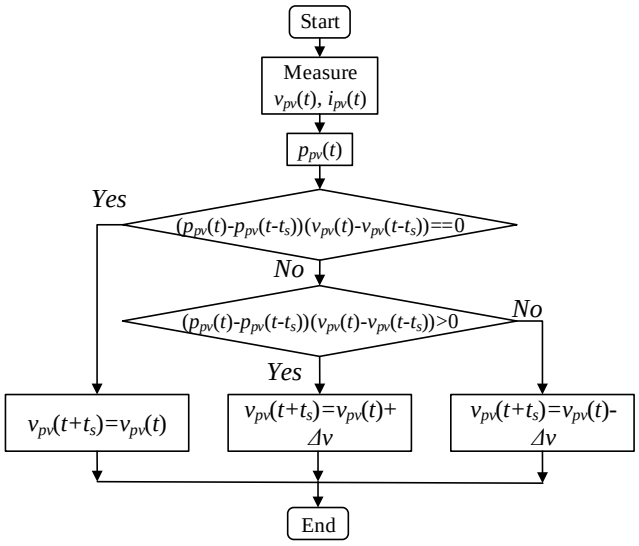
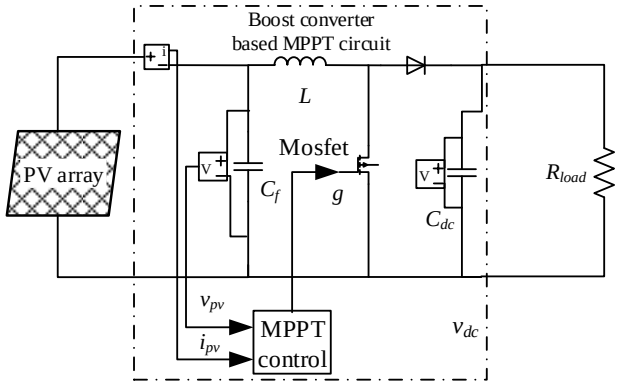
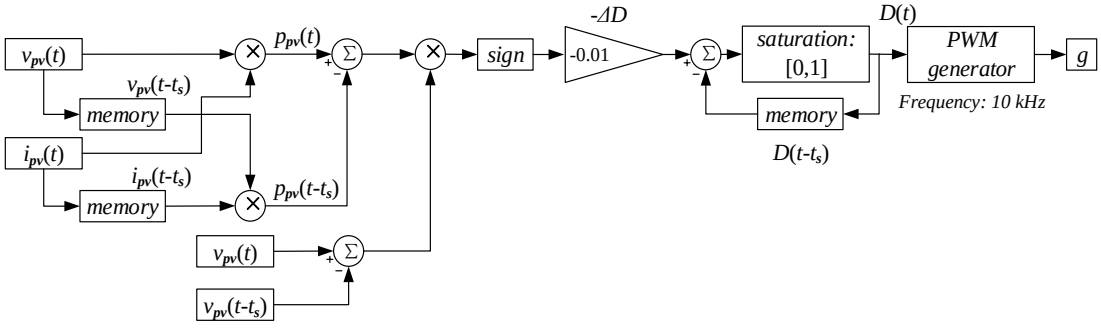



**Figure 6.5:** The simplified flowchart of the P&O MPPT algorithm with respect to Figure 6.3.




a) the circuit schematic of the MPPT based boost converter model




b) the block diagram of the implementation of the P&O MPPT approach on a boost converter

**Figure 6.6:** The boost converter model with P&O MPPT implemented.

**Table 6.1:** The main parameter values of the boost converter shown in Figure 6.6.

| $C_f$ (µF) | $L$ (mH) | $C_{dc}$ (µF) | $R_{load}$ (Ω) | $\Delta D$ | $f_{sw}$ (kHz) |
|---|---|---|---|---|---|
| 5500 | 9 | 2200 | 100 | 0.001 | 10 |

When the PV array is at 1000 W/m$^2$ and 25 °C cell temperature (open-circuit voltage and short-circuit current are 447.8 V and 8.83 A respectively, voltage and current at MPP are 355.1 V and 8.4 A respectively with the maximum power output equals 2983 W), the performance of the P&O MPPT implemented on a boost converter is illustrated by the *I-V* curve of PV array in Figure 6.7. It is observed that the P&O MPPT takes around 0.42 s to reach the MPP position (no initial charging for $C_f$ and $C_{dc}$), with 3.56 V voltage (1% $V_{MPP}$) and 0.085 A current ripple (0.96% $i_{MPP}$).

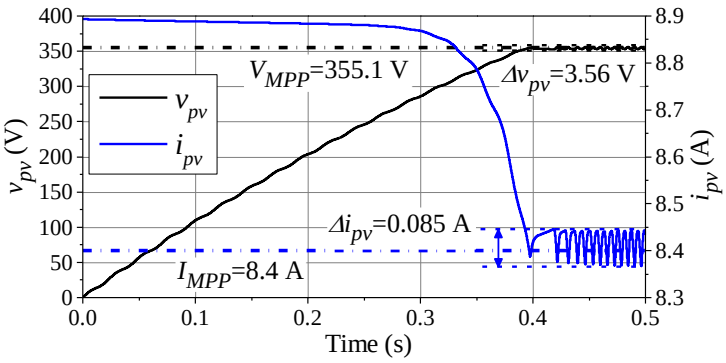



**Figure 6.7:** The *I-V* curve of the P&O MPPT implemented on a boost converter.

**InC MPPT method and its implementation approach**

The flowchart of the InC MPPT algorithm is illustrated in Figure 6.8. The main concept behind this approach is to perturb the voltage output of the PV array according to the slope change of *P-V* curve. Specifically, when the $v_{pv}$ is in the left-side region of the *P-V* curve shown in Figure 6.4, $dp_{pv}/dv_{pv}$ is positive, while $dp_{pv}/dv_{pv}$ becomes negative when $v_{pv}$ is in the right-side region of the *P-V* curve. $v_{pv}$ reaches the MPP position when $dp_{pv}/dv_{pv}$ equals zero. Since $dp_{pv}/dv_{pv}$ is equivalent to $i_{pv}+v_{pv}(di_{pv}/dv_{pv})$, the comparison between $dp_{pv}/dv_{pv}$ and zero can be simplified as the comparison between $di_{pv}/dv_{pv}$ and - $i_{pv}$ /$v_{pv}$ as shown in Figure 6.8.

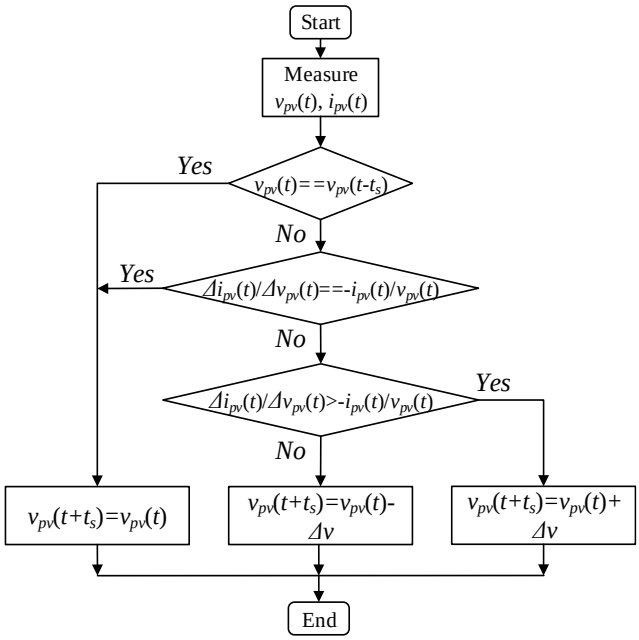
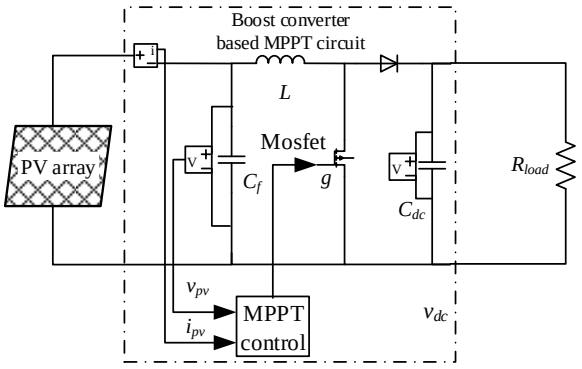
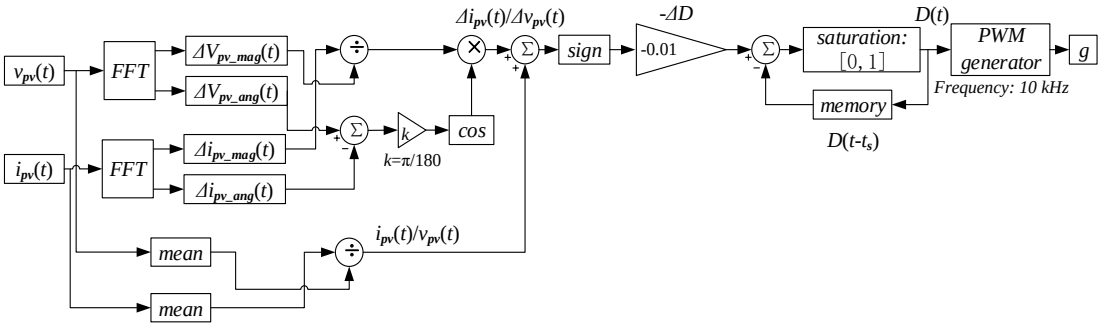



**Figure 6.8:** The flowchart of the InC MPPT algorithm.

The implementation approach of the InC MPPT is demonstrated on a boost converter model as shown in Figure 6.9, with the same circuit parameter values given in Table 6.1 and the same PV array. The performance of the InC MPPT implemented on a boost converter is illustrated by the *I-V* curve of PV array in Figure 6.10. It turns out that the InC MPPT has slightly better performance compared with the P&O MPPT due to the slightly shorter time to reach MPP and less PV voltage and current variation (summarized in Table 6.2).




a) the circuit schematic of the MPPT based boost converter model




b) the block diagram of the implementation of the InC MPPT approach on a boost converter

**Figure 6.9:** The boost converter model with InC MPPT implemented.

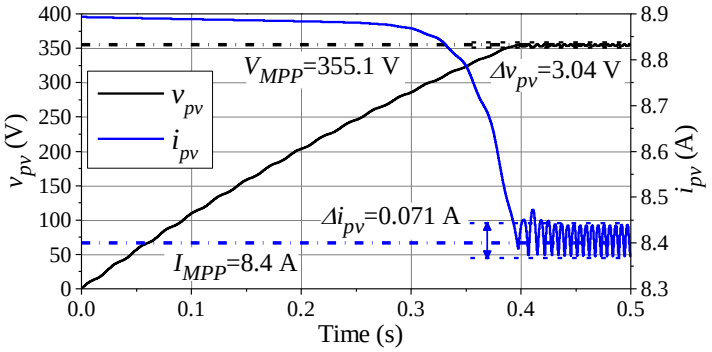



**Figure 6.10:** The *I-V* curve of the P&O MPPT implemented on a boost converter.

**Table 6.2:** Performance comparison between the P&O MPPT and the InC MPPT when implemented on the same boost converter with parameter values in Table 6.1.

| | **P&O MPPT** | **InC MPPT** |
|---|---|---|
| $t_{fMPP}$ **(s)** | 0.42 | 0.4 |
| $\Delta v_{pv,MPP}$ **(V)** | 3.56 | 3.04 |
| $\Delta i_{pv,MPP}$ **(A)** | 0.085 | 0.071 |

## 6.2.2 DC-AC inverter with its control circuits

Although there are a variety of DC-AC inverters have been proposed for PVIs including full-bridge (or H-bridge) inverter, half-bridge inverter, H5 inverter, HERIC inverter, NPC inverter, et al., the full-bridge (FB) inverter is still the most widely used inverter topology for both single-phase and three-phase gird connections [137][140]. Accordingly, only FB inverter is considered in this section, with the main focus given to the different types of control circuits which have direct impact on the harmonic emission of the whole PVI system.

Depending on whether the grid-side control objective is inverter output voltage or inverter control current, the control strategies of FB inverter can be generally divided into voltage control mode and current control mode, and both of these two modes are widely seen in commercial PVIs [168][169]. For the voltage control mode, the PWM

technique is applied to the FB inverter with the objective of regulating the output voltage waveform close to the reference waveform. The voltage control mode FB inverter is seen as a voltage source from the grid side, where the output current is determined by the grid condition. For the current control mode, the PWM technique is applied to the FB inverter with the objective of regulating the output current close to its reference, and hence this type of inverter is seen as a current source from the grid side, with the output voltage determined by the grid condition. Compared with voltage control mode FB inverter, the fault short-circuit current of the current mode FB inverter is much lower than that of its counterpart [169]. However, voltage mode FB inverter has the inherent advantage of supporting off-grid operation which is typically not supported by current mode FB inverter [169].

Although the FB inverter can be either single-phase or three-phase, the way of implementing of voltage control or current control is quite similar, and hence only the single-phase FB inverter is discussed in this section with the aid of circuit simulation in Matlab/Simulink.

**Single-phase FB inverter with the corresponding control circuits**

For the single-phase FB inverter, both stationary-frame control and rotating-frame control can be applied. As the majority of residential-scale PVI requires unity power factor without considering the reactive power support functionality, simple stationary-frame control can be applied. Hence, only stationary-frame control is considered in this part.

*a) Voltage control mode FB inverter*

For the voltage control mode of single-phase FB PVI, dual loop control strategy is typically applied, with the outer current control loop providing feedback for the inner voltage control loop. As the inner voltage loop is rather straightforward with the function of generating PWM control signals based on the reference inverter output voltage provided by the outer current loop, the harmonic emission characteristics of the voltage control mode FB inverter are mainly determined by the outer current loop which affects the distortion level of the reference inverter output voltage. Hence, only the outer current loop is considered here. For the PV application, PI control and PR

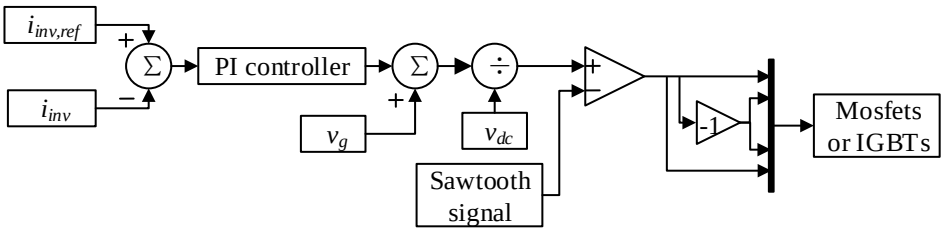
control are the most common used outer current control loops, with their transfer function represented by (6.1) and (6.2) respectively.

$$G_{PI}(s) = K_P + K_I/s \tag{6.1}$$

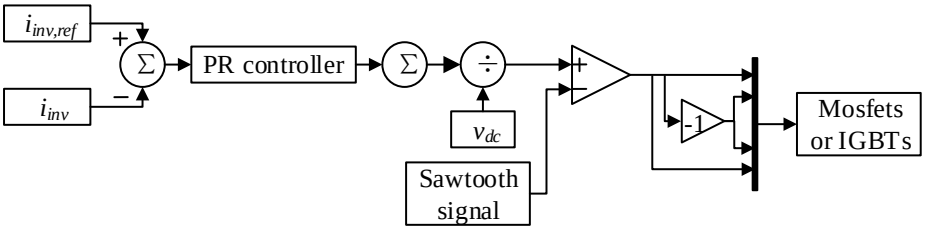
$$G_{PR}(s) = K_P + K_I \frac{2\omega_c s}{s^2+2\omega_c s+\omega_0^2} \tag{6.2}$$

where: $K_P$ and $K_I$ are proportional gain term and integral gain tern respectively. $\omega_0$ and $\omega_c$ are the resonant frequency (should equals to the grid frequency, i.e. 314 rad/s) and the bandwidth around $\omega_0$, respectively.

The block diagram of implementing PI and PR controller in the voltage control mode FB inverter is given in Figure 6.11. As illustrated in Figure 6.11, since PI controller is not capable of tracking sinusoidal reference without steady error, the grid voltage is added to the output of the PI controller to improve the dynamic response of the controller, which is not required for the PR controller [170]. For the PR controller, the integral term $K_I$ only works at frequency very close to $\omega_c$, it is able to track a sinusoidal reference with negligible steady state error [170][171].




a) the block diagram of implementing PI controller in the voltage control mode FB inverter

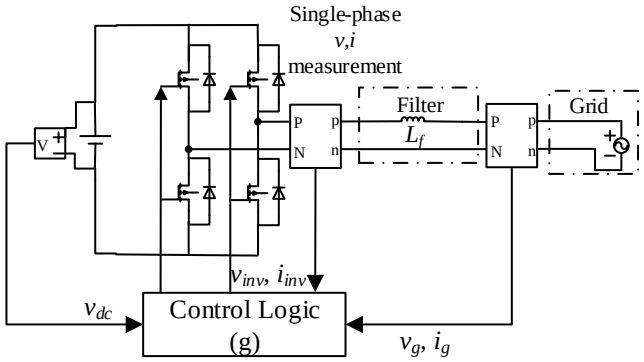



b) the block diagram of implementing of PR controller in the voltage control mode FB inverter

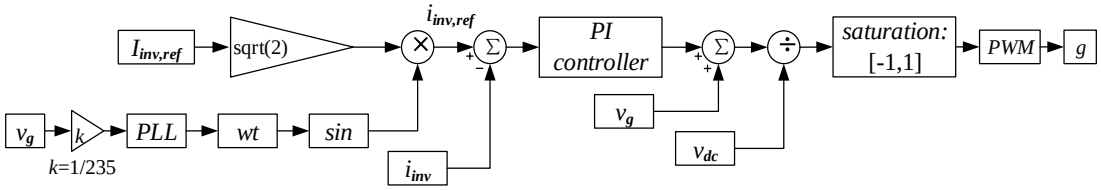
**Figure 6.11:** The block diagram of the implantation of PI and PR controller in the voltage control mode FB inverter.

In order to further compare the performance of PI controller and PR controller in the context of voltage centrode mode FB inverter, their circuit schematic and block diagrams are shown in Figure 6.12, with the main circuit parameter values tabulated

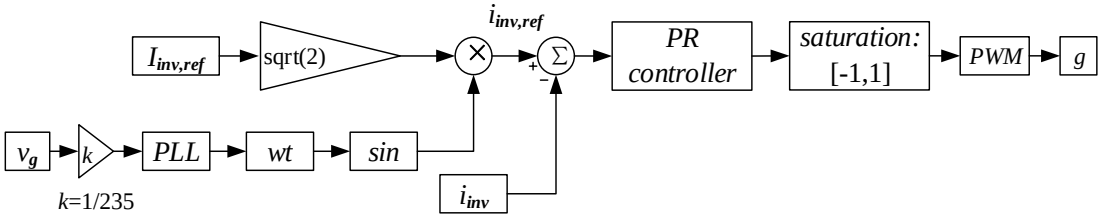
in Table 6.3. As shown in Figure 6.12, the input of the FB inverter is represented by a constant dc source ($v_{dc}$=360 V), and the grid voltage is a sinusoidal voltage frequency with the rms magnitude of 230 V and the frequency of 50 Hz. As the voltage output of the FB inverter should be less than its input to avoid over modulation, a saturation block is applied to limit the modulation index within -1 and 1, shown in Figure 6.12. Additionally, the control signal for the four switches (Mosfets or IGBTs) is generated by the sinusoidal PWM approach, with the frequency of the carrier signal (a sawtooth signal) selected at 10 kHz which is the typical switching frequency of the FB inverter. The grid-side filter is represented by the typical L filter.




a) the circuit schematic of the voltage control mode FB inverter




b) implementation of PI controller in voltage control mode FB inverter



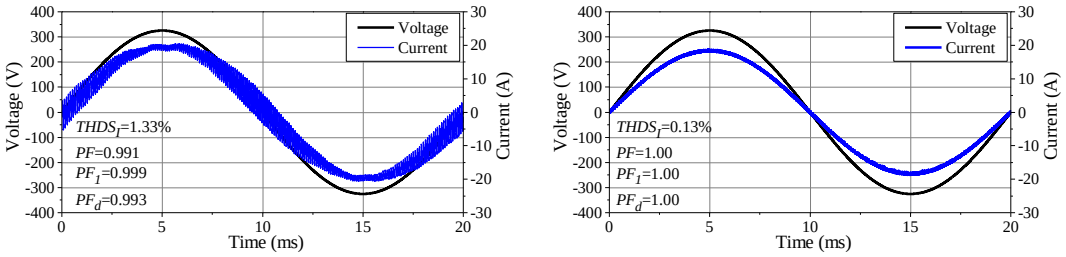

c) implementation of PR controller in voltage control mode FB inverter

**Figure 6.12:** Implementation of the PI controller and PR controller in the FB inverter model.

**Table 6.3:** The main circuit parameter values of the models shown in Figure 6.12.

| $v_{dc}$ (V) | $L_f$ (mH) | Sawtooth signal | | $K_P$ | | $K_I$ | |
|---|---|---|---|---|---|---|---|
| | | Amplitude | Frequency | PI | PR | PI | PR |
| 360 | 2 | 1 | 10 kHz | 4 | 6.8 | 2100 | 90 |

The performance comparison between PI controller and PR controller applied to the voltage control mode FB inverter is illustrated by the grid side voltage and current waveforms in Figure 6.13. It turns out that the PR controller has better performance as opposed to PI controller in terms of $THDS_I$, $PF$, $PF_1$ and $PF_d$, when applied to the voltage control mode FB inverter.

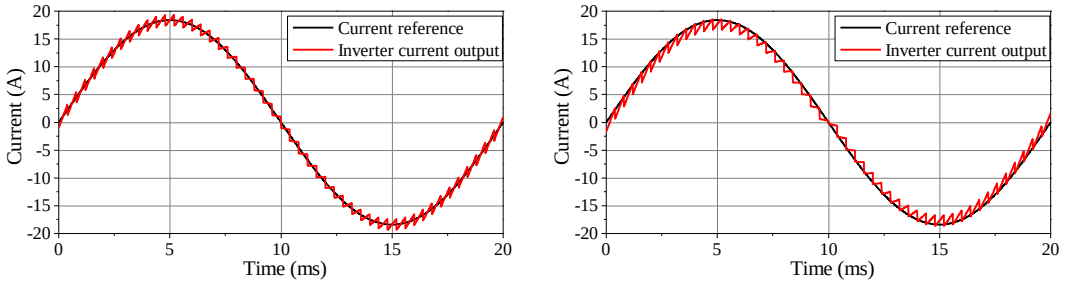



a) PI controller b) PR controller

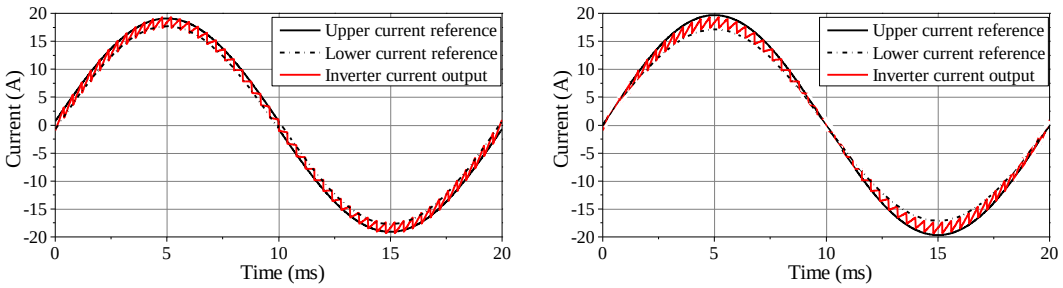
**Figure 6.13:** The grid side voltage and current waveform for voltage control mode FB inverter with PI controller and PR controller respectively.

*b) Current control mode FB inverter*

Similar with voltage control mode FB inverter, the dual loop control strategy is also normally applied to the current control mode FB, with the outer dc-link voltage loop providing the feedback for the inner current loop. By monitoring the change of dc-link voltage, the output current of the FB inverter is adjusted. As the outer voltage loop only provides the reference magnitude for the inner current loop, the harmonic emission characteristics of the current control mode FB inverter is mainly determined by the current control strategies used in the inner current loop. The typical control strategies applied to the inner current loop are average current control, peak current control, and hysteresis current control (both fixed band and sinusoidal band), shown in Figure 6.14.



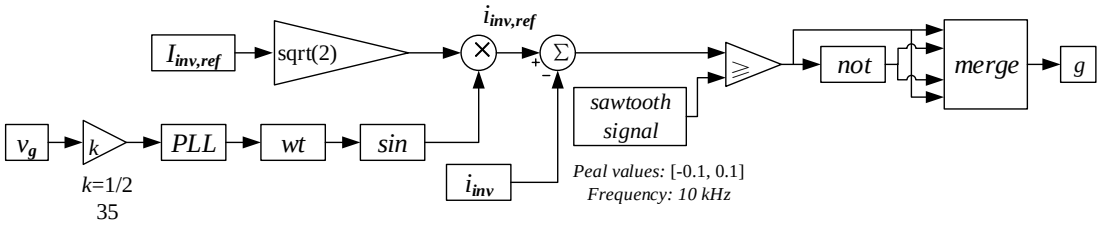

a) average current control b) peak current control



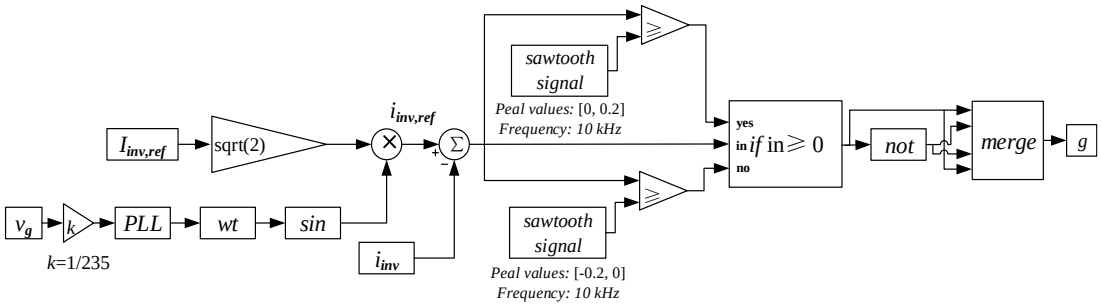

c) hysteresis current control (fixed band) d) hysteresis current control (sinusoidal band)

**Figure 6.14:** The relationship between reference current and inverter current output for average current control, peak current control and hysteresis current control.

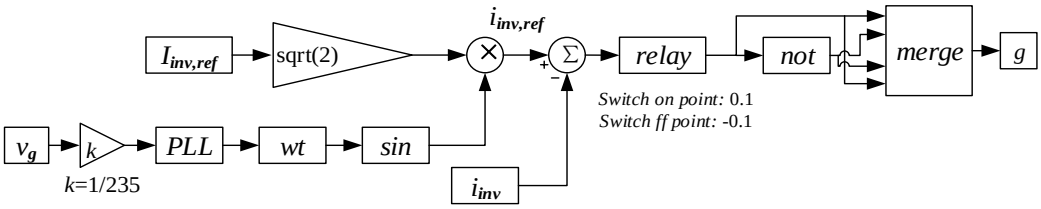
The implementing approach of the above current control strategies are demonstrated on the FB inverter model in Matlab/Simulink. The inverter model circuit schematic is the same with one shown in Figure 6.12(a), with the block diagram of the control circuits given in Figure 6.15. By observing the way of generating PWM signals in Figure 6.15, it is found that both average current control and peak current have a fixed switching frequency (same with the frequency of applied sawtooth signal) while the hysteresis current control (both fixed and sinusoidal band) has a varying frequency (as no carrier signal is applied). For the hysteresis current control, the switching frequency of the FB inverter varies over a wide range and is determined by the hysteresis band, the sampling frequency, the system and load parameter values, making the design of the grid-side filter more complicated as opposed to the average current control and peak current control [172].



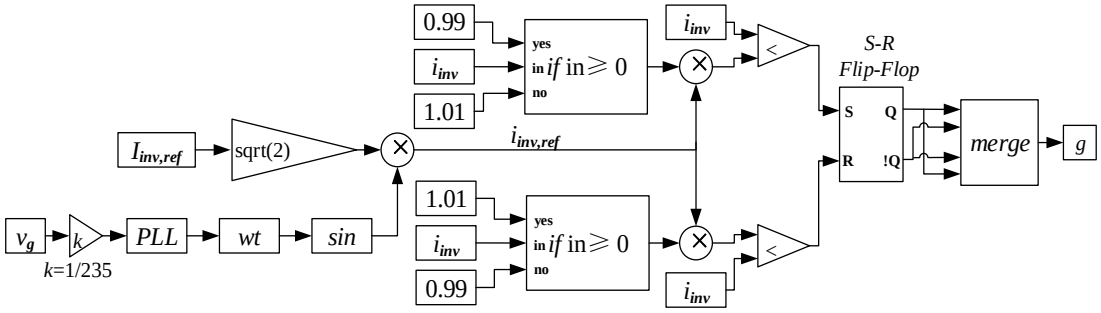

a) implementation of average current control the current control mode FB inverter




b) implementation of peak current control in the current control mode FB inverter



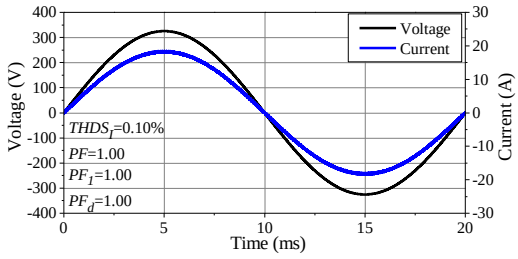

c) implementation of hysteresis current control (fixed band) in the current control mode FB inverter



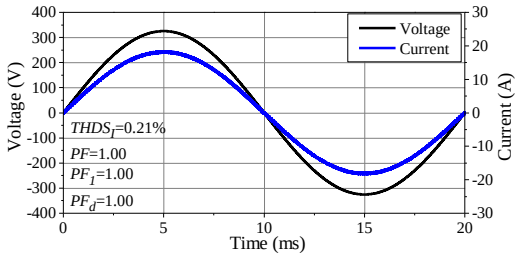

d) implementation of hysteresis current control (sinusoidal band) in the current control mode FB inverter

**Figure 6.15:** Implementation of different current control strategies in the current control mode FB inverter.

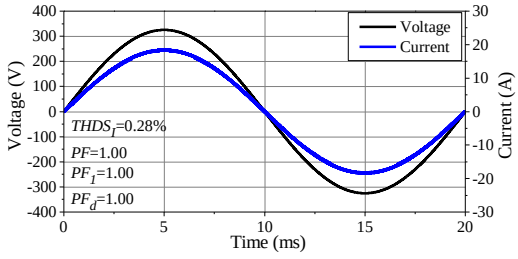
The comparison of the inverter current output among different current control strategies is illustrated in Figure 6.16. It is observed that different control strategies indeed have impact on the current harmonic emission (reflected from the $THDS_I$ values). The $THDS_I$ values for all the four control strategies are small due to the application of purely sinusoidal output current reference, high switching frequency or small hysteresis band.



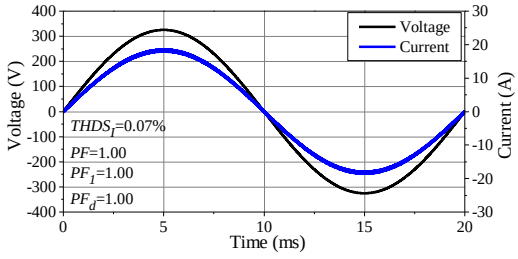

a) average current control




b) peak current control




c) hysteresis current control (fixed band)




d) hysteresis current control (sinusoidal band)

**Figure 6.16:** The grid side voltage and current waveform for current control mode FB inverter with different current control strategies.

### 6.2.3 Grid-side filter

There are three main types of gird-side filters that are widely applied to PVIs, which are L, LC and LCL filters as illustrated in Figure 6.17 (a)-(c) [173]. Among all these three types filters, the first-order L filter is the simplest one, but can only effectively attenuate the high-frequency harmonics emitted from the inverter switches, due to its constant attenuation rate (20 dB/decade) over the whole frequency range [174]. Compared with the L filter, LC filter is a second-order filter and has better performance with an attenuation rate of 40 dB/decade [173]. In terms of the LCL filter, it can achieve a 60 dB/decade attenuation rate when the frequency higher than its resonant frequency, allowing the FB inverter operating at a relatively low switching frequency [173]. The transfer function of ideal L, LC and LCL filter are described in (6.3-6.5), with the resonant frequency $f_{res}$ of ideal LC and LCL filter given in (6.6) and (6.7) respectively. When using LC and LCL filters, the selection of component parameter values should ensure that $f_{res}$ is not too close to the grid frequency $f_g$ (e.g. $f_{res} \geq 10\ f_g$), but still below the switching frequency $f_{sw}$ of the inverter (e.g. $f_{res} \leq 0.5\ f_{sw}$) [175]. The typical switching frequency of PV inverters is around 10 to 20 kHz [176][177].

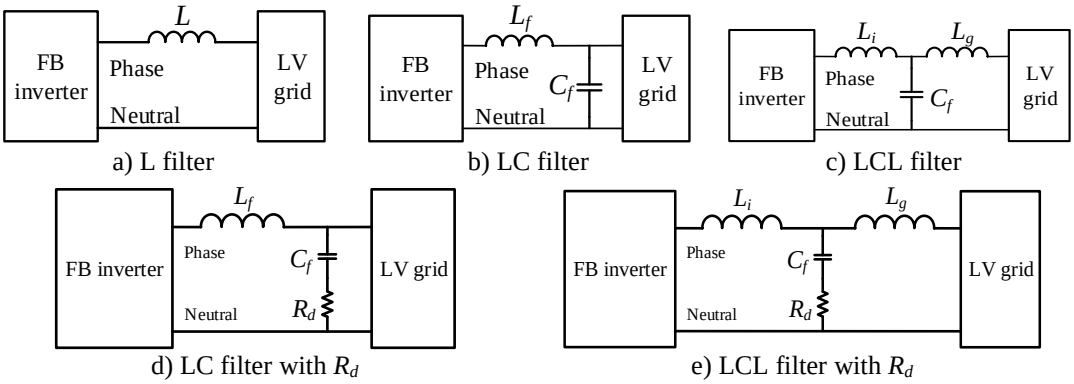



**Figure 6.17:** The three main grid-side filters for PVI (using single-phase PVI as an example).

$$G_L(s) = \frac{v_g(s)}{v_{inv}(s)} = \frac{1}{Ls} \tag{6.3}$$

$$G_{LC}(s) = \frac{v_g(s)}{v_{inv}(s)} = \frac{1}{L_f C_f s^2 + 1} \tag{6.4}$$

$$H_{LCL}(s) = \frac{i_g(s)}{v_{inv}(s)} = \frac{1}{L_i L_g C_f s^3 + (L_i + L_g)s} \tag{6.5}$$

$$f_{LC,res}(s) = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{6.6}$$

$$f_{LCL,res}(s) = \frac{1}{2\pi}\sqrt{\frac{L_i+L_g}{L_i L_g C_f}} \tag{6.7}$$

The bode plot of three ideal L, LC and LCL filters is given in Figure 6.18 (a)-(c). It is noticed that a very high gain is achieved at the resonant frequency of LC and LCL filters, making the whole PVI system vulnerable to oscillations. Hence, proper damping is required at the resonant frequency, with either passive or active damping approaches. The simplest way is to add a small resistor $R_d$ in series with the filter capacitor $C_f$ [178] (as shown in Figure 6.17 (d)-(e)), where the transfer function of LC and LCL filters become equation (6.8) and (6.9) respectively.

$$G_{LC\_Rd}(s) = \frac{v_g(s)}{v_{inv}(s)} = \frac{R_d C_f s+1}{L_f C_f s^2+R_d C_f s+1} \tag{6.8}$$

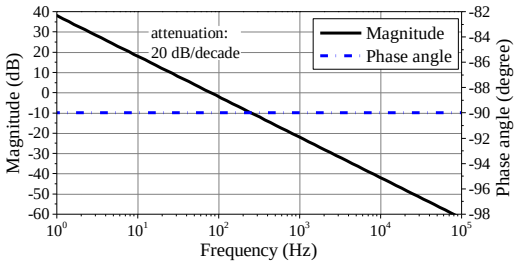
$$H_{LCL\_Rd}(s) = \frac{i_g(s)}{v_{inv}(s)} = \frac{R_d C_f s+1}{L_i L_g C_f s^3+(L_i+L_g)R_d C_f s^2+(L_i+L_g)s} \tag{6.9}$$

As indicated in (6.10) and (6.11), the $R_d$ value is generally selected as one third of the capacitor impedance at $f_{res}$, in order to avoid high damping losses across $R_d$ [175][178].

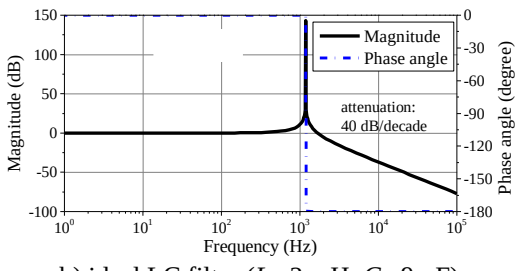
$$R_{d\_LC} = \frac{1}{3}\sqrt{\frac{L_f}{C_f}} \tag{6.10}$$

$$R_{d\_LCL} = \frac{1}{3}\sqrt{\frac{L_i L_g}{(L_i+L_g)C_f}} \tag{6.11}$$

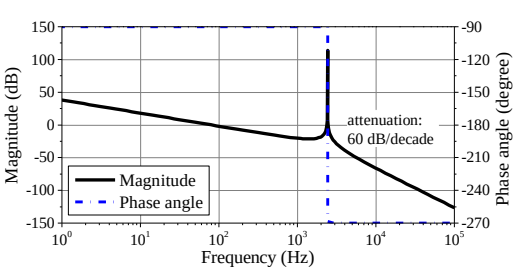
For the ideal LC and LCL filters in Figure 6.18(b)-(c), the calculated $R_d$ values (according to (6.10) and (6.11)) are 4.969 Ω and 2.434 Ω respectively, with the bode plot given in Figure 6.18(d). It is observed that the series connected $R_d$ sufficiently reduce the resonance peak, without affecting the resonant frequency and the attenuation rate. Therefore, the damped LC and LCL filters are more preferred in the PV applications.



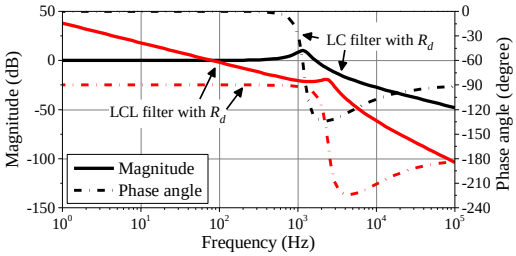

a) ideal L filter ($L$=2 mH)




b) ideal LC filter ($L_f$=2 mH, $C_f$=9 μF)




c) ideal LCL filter ($L_i$=1.2 mH, $C_f$=9 μF, $L_g$=0.8 mH)

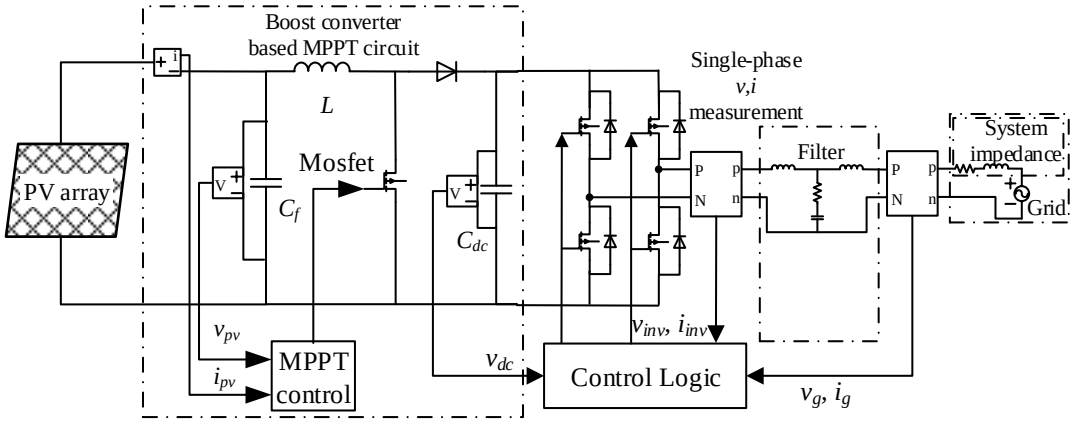



d) LC and LCL filters with $R_d$ ($R_d$ is 4.969 Ω and 2.434 Ω for LC and LCL filters respectively)

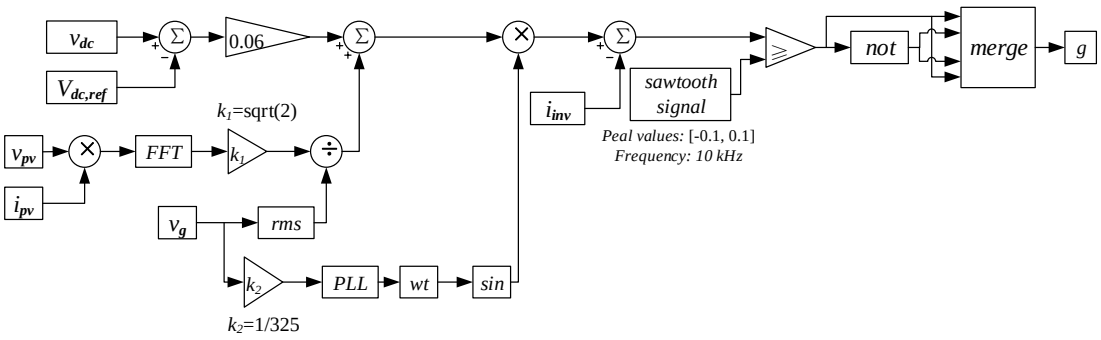
**Figure 6.18:** The bode plots of L, LC and LCL filters.

## 6.2.4 Full PVI system circuit

With all the main circuit components discussed in the previous sections, this section will briefly discuss the working principles of the whole PVI system by assembling all the circuit parts together. Here, a 3 kW generalised PVI model is built in Matlab/Simulink, consisting of the InC MPPT based boost converter, single-phase current control mode FB inverter (average current control), and damped LCL model. The circuit parameter values are the same with the circuit parts discussed in previous sections, with the circuit schematic and corresponding control diagram illustrated in Figure 6.19 (the InC MPPT control is not shown as it is given in section 6.2.1). The simulated grid-side voltage and current waveform, PV array voltage and current output are shown in Figure 6.20, implying that the PVI model developed by combing the main circuit parts works properly. This work will facilitate the next-step work of developing component-based PVI model from the measurement data.

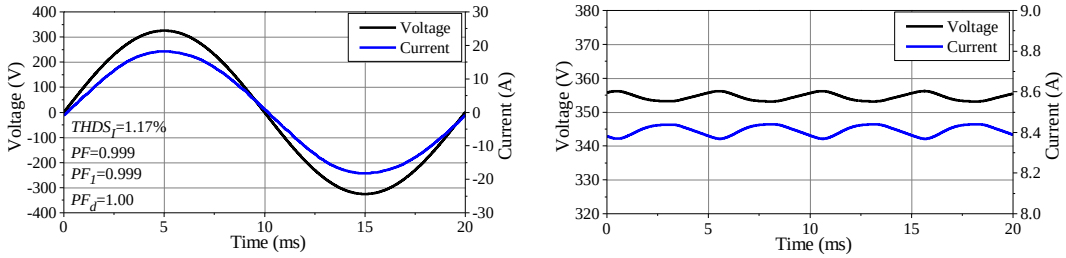



a) the circuit schematic of the single-phase PVI model




b) the block diagram of the average current control for the FB inverter ($V_{dc,ref}$=545 V)

**Figure 6.19:** The circuit schematic of full PVI model in Matlab/Simulink.




a) grid side voltage and current b) PV array output voltage and current

**Figure 6.20:** Simulated grid side voltage and current, PV array output and current.

## 6.3 Harmonic emission of residential-scale PVIs

In this section, the measured harmonic emission characteristics of three residential-scale PVIs will be fully discussed, with the basic information of tested PVIs given in Table 6.4. This section is structured as follow: Section 6.3.1 will briefly introduce the test set-up, with the applied harmonic evaluation framework and related harmonic emission standards of PVIs given in Section 6.3.2. Section 6.3.3 will give the harmonic evaluation results of tested PVIs.

**Table 6.4:** The basic information of three tested PVIs.

| Inverter | PVI-A | PVI-B | PVI-C |
|---|---|---|---|
| **Technology** | Transformerless | HF-transformer | LF-transformer |
| **Rated power (kVA)** | 4.6 | 10 | 4.6 |
| **Phase connection** | Single-phase | Three-phase | Single-phase |
| **Rated/Reference current (A)** | 20 | 14.5 | 20 |

### 6.3.1 Test set-up

A fully automated test-bed (with accuracies better than 5%, 2% and 1% for individual harmonic magnitudes higher than 50 mA, 100 mA and 200 mA, respectively) is used

for all presented measurements. It consists of a 1 MS/s acquisition system and a controllable three-phase power source with three voltage waveforms used in tests: sinusoidal, WF1, "flat-top", WF2, and "pointed-top", WF3, emulating typical "background distortions" in LV grids, [179]. In the tests, source impedance was either adjusted to be as low as possible, $Z_S$~0 (ZS1), representing the impedance of the cable connecting tested PE device to the power source, or as "maximum expected source impedance" (at 90% LV supply points, [92]), ZS2. In addition, the operating power of PVIs is gradually reduced from 100% $P_{rated}$ to 5% $P_{rated}$.

### 6.3.2 Harmonic evaluation framework and related standards

The typical way of evaluating the current harmonic emission from gird connected PVI includes individual current harmonics and total harmonic emission/demand distortion. According to the calculation methods for harmonic measurements defined in [33], a time window of ten fundamental periods in 50 Hz systems (corresponds to 200 ms) is applied for the measurement data processing, as well as a 150-cycle (3 s) time aggregation interval suggested in [36]. The application of 200 ms time window results in a frequency resolution of 5 Hz, which can alleviate spectrum leakage to some extend as opposed to the harmonic calculation from the one fundamental period of measurements. In order to further take into account the spectrum leakage or interharmonic emission due to the variations of the amplitude and/or phase angle of the fundamental component and/or of the harmonic components, the spectral components directly adjacent to the considered harmonic are grouped together to the harmonic which is called harmonic subgroup [33]. The individual subgroup harmonic emission of PVI in the function of operating power, is calculated based on equation (6.12).

$$I_{sg,h}(P) = \sqrt{\sum_{k=-1}^{1}\left[I_{C,(N\cdot h+k)}(P)\right]^2} \tag{6.12}$$

where: $I_{sg,h}$ is the subgroup harmonic of order h which positive integers; $N$ is the number of fundamental periods within the calculation time window which 10 for the 50 Hz supply system; $I_{c,k}$ is the rms value of the k-th spectrum component calculated from the 200 ms time window (k is positive integers).

As the recording length of the each testing point is 10 s, the individual subgroup harmonics are calculated by using the non-overlapping 200 ms time window, from which the very short time (3 s) harmonic values can be obtained and updated every 200 ms. Within the aggregation time intervals, the minimum, average (arithmetic average for the 200 ms window and average rms for the 3 s window) and maximum values can be obtained from the calculated individual subgroup harmonics and the very short time harmonics.

With the calculation of individual subgroup harmonics and the very short time harmonics, it is possible to evaluate the current waveform distortion at different operating power of the device, based on indices including the total (subgroup) harmonic current distortion, $THDS_I(P)$, total (subgroup) harmonic current, $THC_{sg}(P)$ and total demand distortion, $TDD_{sg}(P)$, with their calculation equations given in (6.13-6.15).

$$THC_{sg}(P) = \sqrt{\sum_{h=2}^{H}\left[I_{sg,h}(P)\right]^2} \tag{6.13}$$

$$THDS_I(P) = \frac{100}{I_{sg,1}(P)}\sqrt{\sum_{h=2}^{H}\left[I_{sg,h}(P)\right]^2} = \frac{THC_{sg}(P)}{I_{sg,1}(P)} \times 100 \tag{6.14}$$

$$TDD_{sg}(P) = \frac{100}{I_{rated}}\sqrt{\sum_{h=2}^{H}\left[I_{sg,h}(P)\right]^2} = \frac{THC_{sg}(P)}{I_{rated}} \times 100 \tag{6.15}$$

where: $I_{sg,1}$(P) and $I_{rated}$ are the subgroup harmonic current at fundamental frequency and the rated current respectively.

Technical Report IEC TR 61000-3-15 [45] and Standards IEEE Std. 519 [39], IEC 61000-3-2 [42], IEC 61000-3-12 [43] give emission limits for individual current harmonics of power electronic equipment (Table 6.5) either in absolute values, or in percentage of equipment rated current (denoted as "reference current"), with [39] specifying *TDD* limits and [43] specifying *THC* limits. $THD_I$ limits are not given, as this will require to specify equipment fundamental current, while standards focus on harmonics. Different criteria are used for limits in [39][42][43][45]: single-phase or three-phase equipment connections, voltage levels and strengths of the supply system. The IEC standards [42][43] are generally intended for passive power electronic equipment (i.e. for power-consuming loads), but can be applied to PVIs connected to

the LV network. Limits in [45], for example, are the same as in [43], while [39] suggests to apply the strictest limits for loads to power generating equipment.

For assessing PVI-B (with $I_{rated}$<16 A), limits from [45] and [42] are used ([45] is a non-mandatory Technical Report), while limits from Table 6.5 in [43] are used for PVI-A and PVI-C (16 A< $I_{rated}$ <75 A) for the "worst case conditions" (i.e. the lowest value of short circuit power at the point of common coupling, PCC); Standards [42] and [43] give limits assuming non-distorted supply conditions, but this is rarely found in actual networks. Finally, limits in [39] for power generating equipment are used for all three PVIs, assuming unity power factor (which was also adjusted during the tests).

**Table 6.5:** Harmonic emission limits applied to tested PVIs.

| Harmonics | Harmonic Emission Limits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | IEC 61000-3-2 [42] [a] | | IEC 61000-3-12 [43] [b] | | IEC TR 61000-3-15 [45] [c] | | IEEE Std. 519 [39] [d] | |
| | PVI-B | | PVI-A & PVI-C | | All three PVIs | | All three PVIs | |
| | Order | $I_h$ | Order | $I_h$ | Order | $I_h$ [b] | Order | $I_h$ |
| | ***h*** | **[*A*]** | ***h*** | **[% $I_{rated}$]**[c] | ***h*** | **[% $I_{rated}$]**[c] | ***h*** | **[% $I_{rated}$]**[c] |
| **Odd** | 3 | 2.3 | 3 | 21.6 | 3 | 21.6 | 3-9 | 4 |
| | 5 | 1.14 | 5 | 10.7 | 5 | 10.7 | 11-15 | 2 |
| | 7 | 0.77 | 7 | 7.2 | 7 | 7.2 | 17-21 | 1.5 |
| | 9 | 0.4 | 9 | 3.8 | 9 | 3.8 | 23-33 | 0.6 |
| | 11 | 0.33 | 11 | 3.1 | 11 | 3.1 | 35-49 | 0.3 |
| | 13 | 0.21 | 13 | 2 | 13 | 2 | | |
| | 15-39 | 2.25/*h* | / | / | 15-39 | 1 | | |
| **Even** | 2 | 1.08 | 2-12 | 16/*h* | 2-40 | 1 | 2-10 | 1 |
| | 4 | 0.43 | | | | | 12-16 | 0.5 |
| | 6 | 0.3 | | | | | 18-22 | 0.375 |
| | 8-40 | 1.84/*h* | | | | | 24-34 | 0.15 |
| | | | | | | | 36-50 | 0.075 |
| ***TDD*** | / | | 23% [c] | | / | | 5% | |
| Notes: [a] for Class A equipment; [b] Table 2 for single-phase equipment and for short circuit ratio=33; [c] for $P_{rated}$>600 W; [d] Table 2 for short circuit ratio≤20. | | | | | | | | |

## 6.3.3 Harmonic emission of tested PVIs

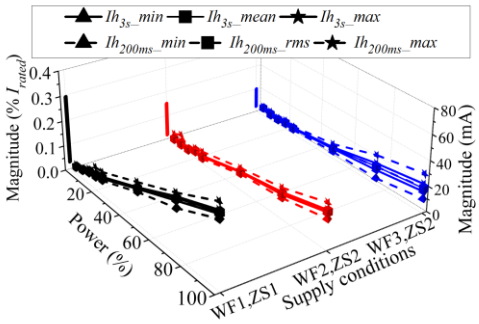
In this section, the measured harmonic emission characteristics of the three PVIs under a combination of different supply conditions and operating power are fully discussed.

### Harmonic emission of PVI-A

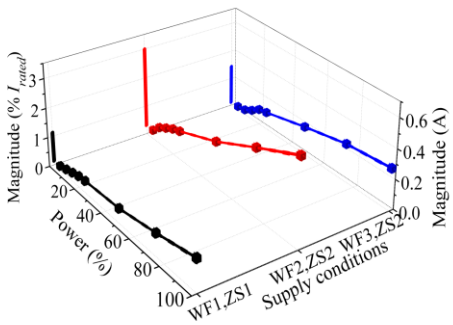
The individual harmonic subgroups of order 2-7, the $THDS_I$ and $TDD_{sg}$ under different supply conditions and different operating powers are illustrated in Figure 6.21. The values in Figure 6.21 are calculated by using both 200 ms time window and 3 s time window, with the derived minimum, average and maximum values applied to illustrate

the variation of calculated indices values under different time windows. The observations from Figure 6.21 are summarized as follows:

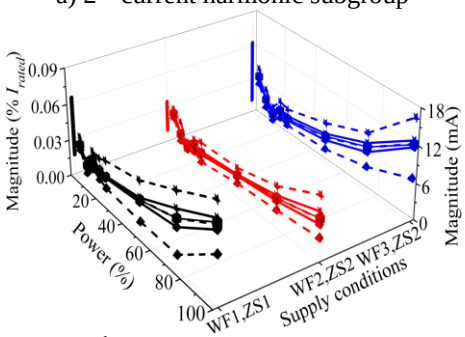
a) all calculated indices show changes with operating powers and supply conditions;
b) the 3rd harmonic is dominant among the order of 2 to 7; the 2nd harmonic has comparable magnitude as opposed to 5th and 7th harmonics under WF1, ZS1;
c) the odd harmonics increase their emission under non-ideal supply conditions (WF2/WF3, ZS2) compared with their values under ideal condition (WF1, ZS1);
d) most harmonics decrease their emission with the decreasing operating power, while 4th and 6th harmonics increase their emission under very low operating power;
e) nonideal supply conditions have strong impacts on the considered harmonics, except 4th and 6th;
f) all individual harmonics are below the limits in the related standards;
g) $THDS_I$ increases around 60 times in the very low power;
h) WF2 with dominant 3rd harmonic increases the 3rd current harmonic emission, while WF3 with dominant 5th harmonic increases the 5th current harmonic emission;
i) $TDD_{sg}$ does not violate the limits in related standards, but is close to the limits in [39].
j) the switching frequency of PVI-A is around 16 kHz and is insensitive to the change of supply conditions and operating powers.



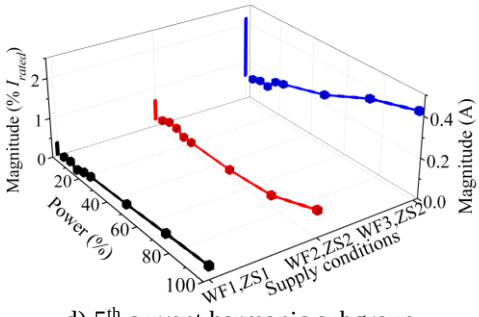
a) 2nd current harmonic subgroup



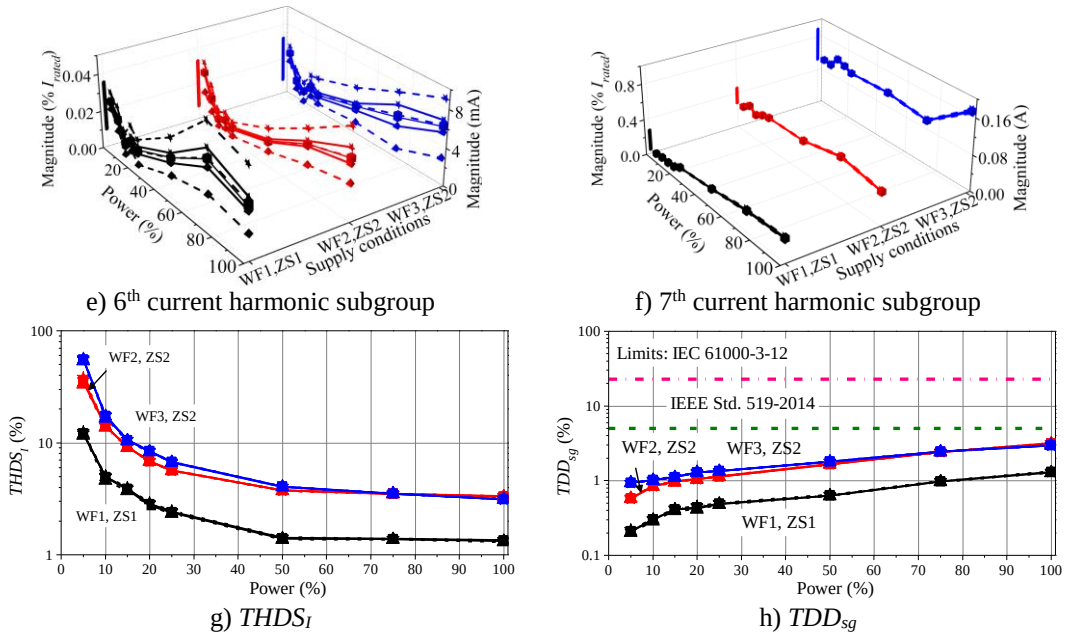
b) 3rd current harmonic subgroup



c) 4th current harmonic subgroup



d) 5th current harmonic subgroup




e) 6th current harmonic subgroup

f) 7th current harmonic subgroup

g) $THDS_I$

h) $TDD_{sg}$

**Figure 6.21:** Individual current harmonic subgroups, $THDS_I$ and $TDD_{sg}$ ($THC_{sg}$ in % of rated current) for PVI-A.

**Harmonic emission of PVI-B**

The individual harmonic emission of order 2-7, $THDS_I$ and $TDD_{sg}$ for PVI-B under different supply conditions and operating powers are given in Figure 6.22. The main findings are concluded as follow:

a) different supply conditions have apparent impacts on the odd harmonic emission, but have little impacts on the even harmonic emission;

b) the odd harmonic emission is alleviated with the decrease of operating power;

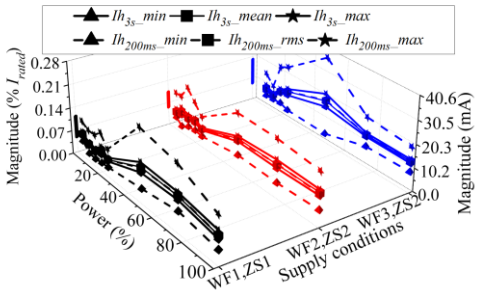
c) both *TDDsg* and individual harmonic emission under ideal supply condition (WF1, ZS1) are below the limits in related standards;

d) nonideal supply conditions have a strong impact on the odd harmonic emission: 3rd, 5th and 7th current harmonics violate the limits in [39], while 5th and 7th current harmonics violate the limits in all three standards under WF3, ZS2 for the whole operating power range or only the low power operating range;

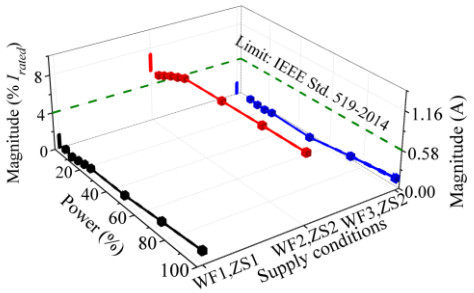
e) the increased harmonic emission under nonideal supply conditions (WF2/WF3, ZS2) violates the $TDD_{sg}$ limits in [39], for the whole operating power range.

f) the switching frequency of PVI-B is around 20 kHz and is insensitive to the change of supply conditions and operating powers.

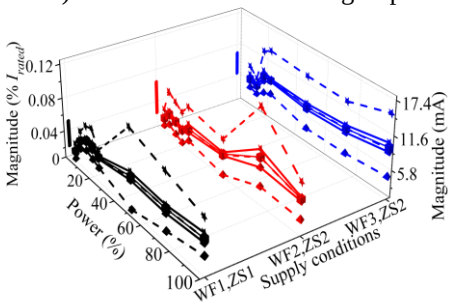
As opposed to PVI-A, PVI-B is much more sensitive to the background waveform distortion (WF2/WF3) and the source impedance (ZS2), with their $THDS_I$ and $TDD_{sg}$ values increase by approximately 600 times and 10 times respectively with respect to their values under ideal supply condition (WF1, ZS1). Although the odd harmonics under WF2/WF3, ZS2 violate the limits in the three standards, only [45] considers the background voltage waveform distortion and off-nominal operating power, while the limits in [42] and [39] require the device tested under ideal supply condition (WF1, ZS1) with nominal operating power. Finally, the increased harmonic emission under nonideal supply conditions suggest that the $THD_I$ values specified by the manufacturers for device tested under ideal supply condition and rated operating power, cannot represent the actual harmonic emission level of the device connecting to the LV networks.



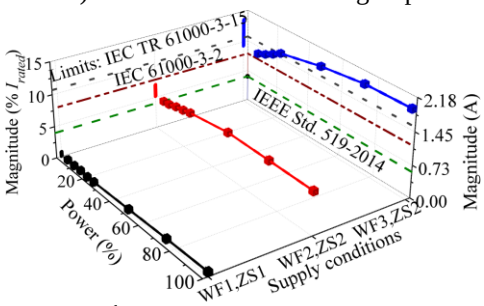

a) 2nd current harmonic subgroup



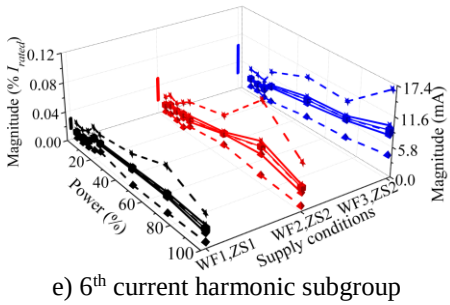

b) 3rd current harmonic subgroup



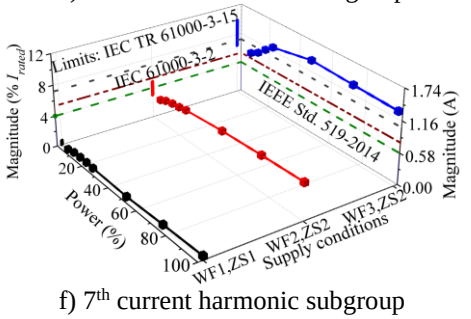

c) 4th current harmonic subgroup



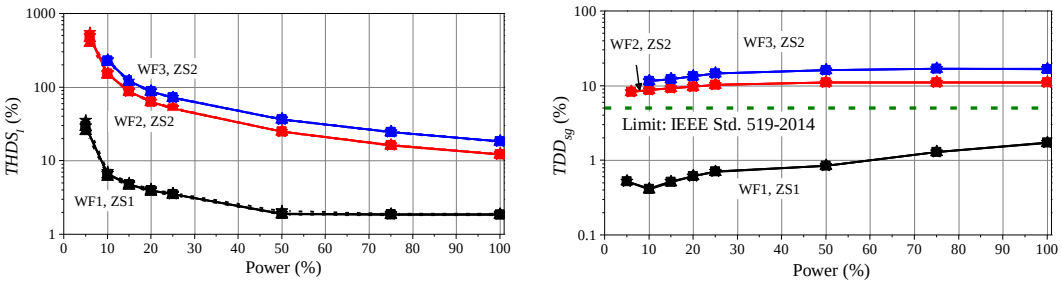

d) 5th current harmonic subgroup




e) 6th current harmonic subgroup




f) 7th current harmonic subgroup




g) $THDS_I$ h) $TDD_{sg}$

**Figure 6.22:** Individual current harmonic subgroups, $THDS_I$ and $TDD_{sg}$ ($THC_{sg}$ in % of rated current) for PVI-B (phase A).

**Harmonic emission of PVI-C**

The individual harmonic emission of order 2-7, $THDS_I$ and $TDD_{sg}$ for PVI-C under different supply conditions and operating powers are given in Figure 6.23. The main findings are concluded as follow:

a) as opposed to PVI-A and PVI-B, PVI-C has increased even current harmonic emission;

b) even harmonics remain more or less constant for the main operating power range (30%-100% $P_{rated}$), with a slight increase in low power mode (below 30% $P_{rated}$);

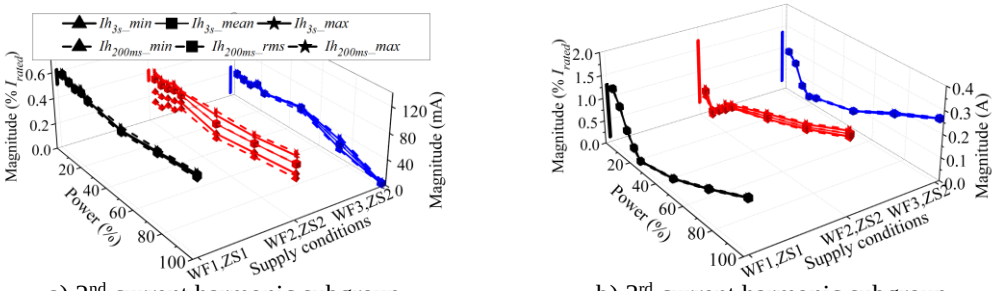
c) non-ideal supply conditions (WF2/WF3, ZS2) result in to an reduction of even harmonic emission, but increase the odd harmonic emission;

d) the impact of nonideal supply conditions is small for 3rd harmonic;

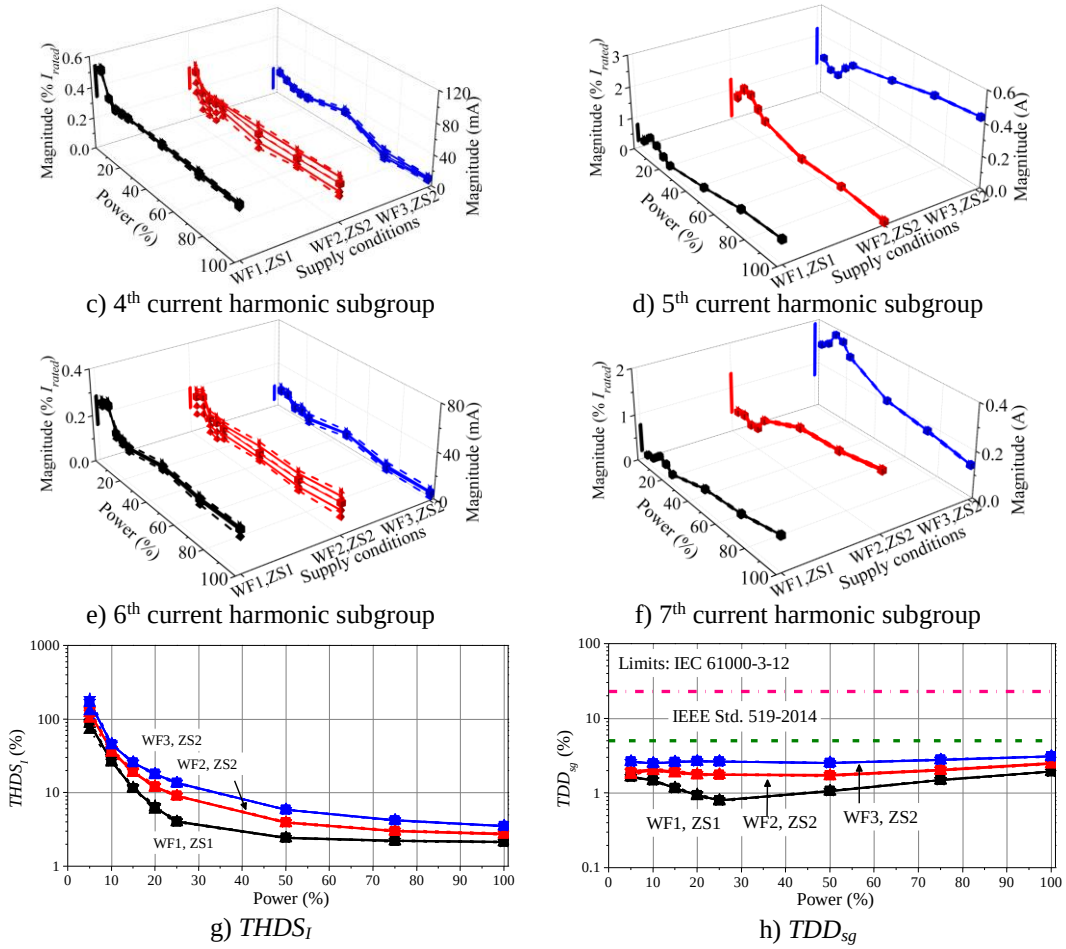
e) 3rd and 7th harmonics under very low operating power are very close to, or higher than their values at nominal operating power;

f) both individual harmonics and $TDD_{sg}$ are below the limits in related standards under all testing conditions.

g) the switching frequency of PVI-C is around 16 kHz and is insensitive to the change of supply conditions and operating powers.




a) 2nd current harmonic subgroup b) 3rd current harmonic subgroup




c) 4th current harmonic subgroup

d) 5th current harmonic subgroup

e) 6th current harmonic subgroup

f) 7th current harmonic subgroup

g) $THDS_I$

h) $TDD_{sg}$

**Figure 6.23:** Individual current harmonic subgroups, $THDS_I$ and $TDD_{sg}$ ($THC_{sg}$ in % of rated current) for PVI-C.

## 6.4 Modelling of PVIs

The model format considered in this section includes both CBM and FDM, which will be applied to selected PVIs, with the model accuracy fully validated with measurements.

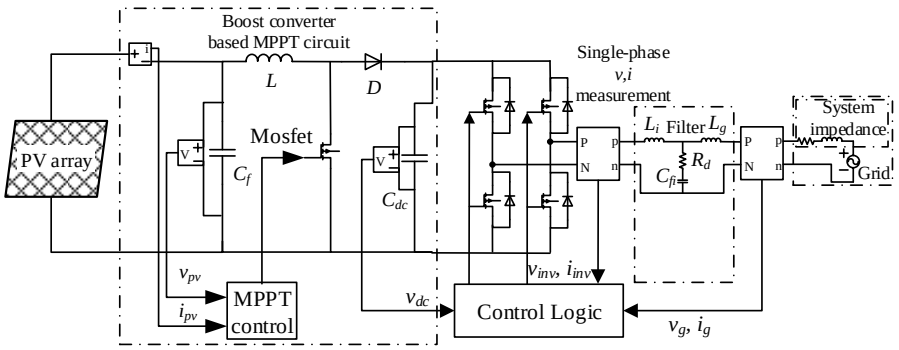
### 6.4.1 Component-based modelling

In this part, the development procedure of CBMs for PVIs will be demonstrated on the single-phase PVI-A and the three-phase PVI-B which are introduced in Section 6.3.

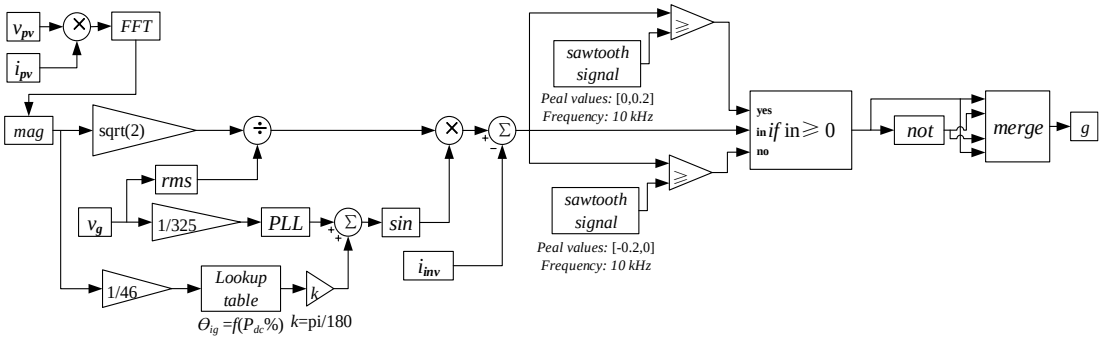
*a) Component-based modelling of PVI-A*

Considering the fact that it is typically difficult to get access to the detailed circuit design information of PVIs, the developed component-based PVI-A model is based on the typical residential-scale PVI circuit topology which is based on the single-stage single-phase transformerlesss FB inverter circuit. As the current control scheme is

more preferred than the voltage control scheme in the grid-connected PVI, current control scheme is applied to the CBM [137]. By comparing the four typical current control strategies in Section 6.2.2 and the three grid-side filters discussed in Section 6.2.3, the peak current control FB inverter with the grid-side LCL filter can achieve the best matching between the simulated and the measured grid-side current, and hence will be used in the CBM for PVI-A. The circuit schematic of the full circuit PVI-A model and the block diagram of the control logic are given in Figure 6.24.




a) the circuit schematic of the single-phase PVI-A model

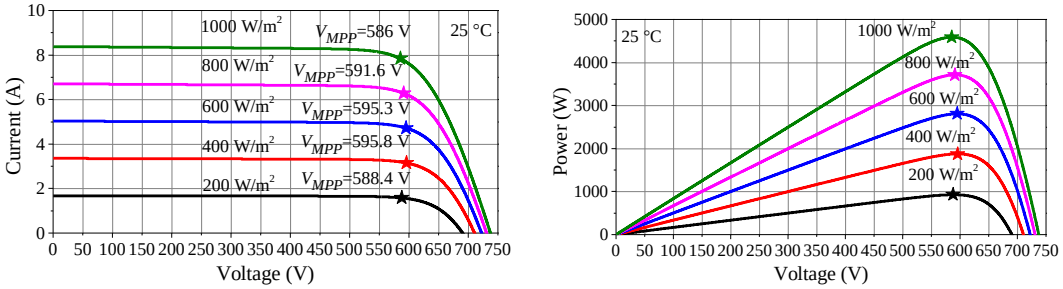



b) the block diagram of the peak current control for the FB inverter

**Figure 6.24:** The schematic of the developed full circuit PVI-A model.

As illustrated in Figure 6.24, it is a two-stage single-phase PV inverter where the first stage is the boost converter based MPPT circuit and the second stage is FB inverter and corresponding control circuits. The modelled PV array consists of 20 PV modules connected in series (maximum power output at 1000 W/m$^2$ and 25 °C is 4.6 kW), with its typical *I-V* and *P-V* characteristics illustrated in Figure 6.25. In terms of the MPPT circuit and control, it is implemented on a boost converter with the InC MPPT approach introduced in Section 6.2.1. As the parameter values for the boost converter and corresponding MPPT control is the same with those given in Table 6.1 and Figure 6.9, the MPPT control circuits are not shown in Figure 6.24. The block diagram of the

control circuit for the FB inverter is further illustrated in Figure 6.26. Specifically, the amplitude of the inverter reference output current is obtained from the PV array power output $P_{pv}$ and the rms value of grid supply voltage $v_g$, while the reference output current phase angle $\theta_{ig}$ with respect to $v_g$ is determined by $P_{pv}$. By comparing the difference between the inverter reference current output and the actual current output with a high-frequency low-amplitude sawtooth signal, the PWM control signals for the four switches of the FB inverter are easily obtained. The main circuit parameter values are tabulated in Table 6.6. The simulated gird-side voltage and current waveforms, PV array output voltage and current waveforms of the full circuit PVI-A model operating under different supply conditions with different operating powers (from 10% to 100% $P_{rated}$) are illustrated in Figure 6.27. It is noticed from Figure 6.27 that a good matching achieved between measured and simulated gird-side current waveforms, and the PV array voltage and current outputs are maintained around the predefined MPPT point (in Figure 6.25), suggesting the developed full circuit PVI model can accurately representing the general electrical characteristics of PVI-A.




a) *I-V* characteristics of the PV array (200-1000 W/m², 25 °C)

b) *P-V* characteristics of the PV array (200-1000 W/m², 25 °C)

**Figure 6.25:** The *I-V* and *P-V* characteristics of the modelled PV array under different sun irradiance (in W/m²).

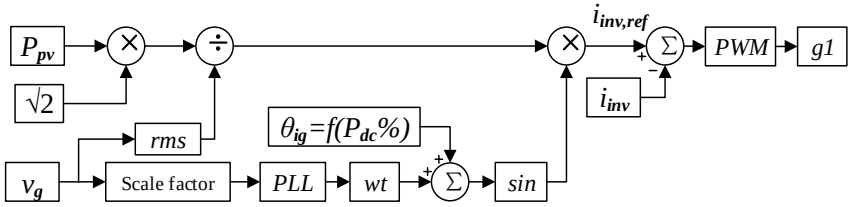
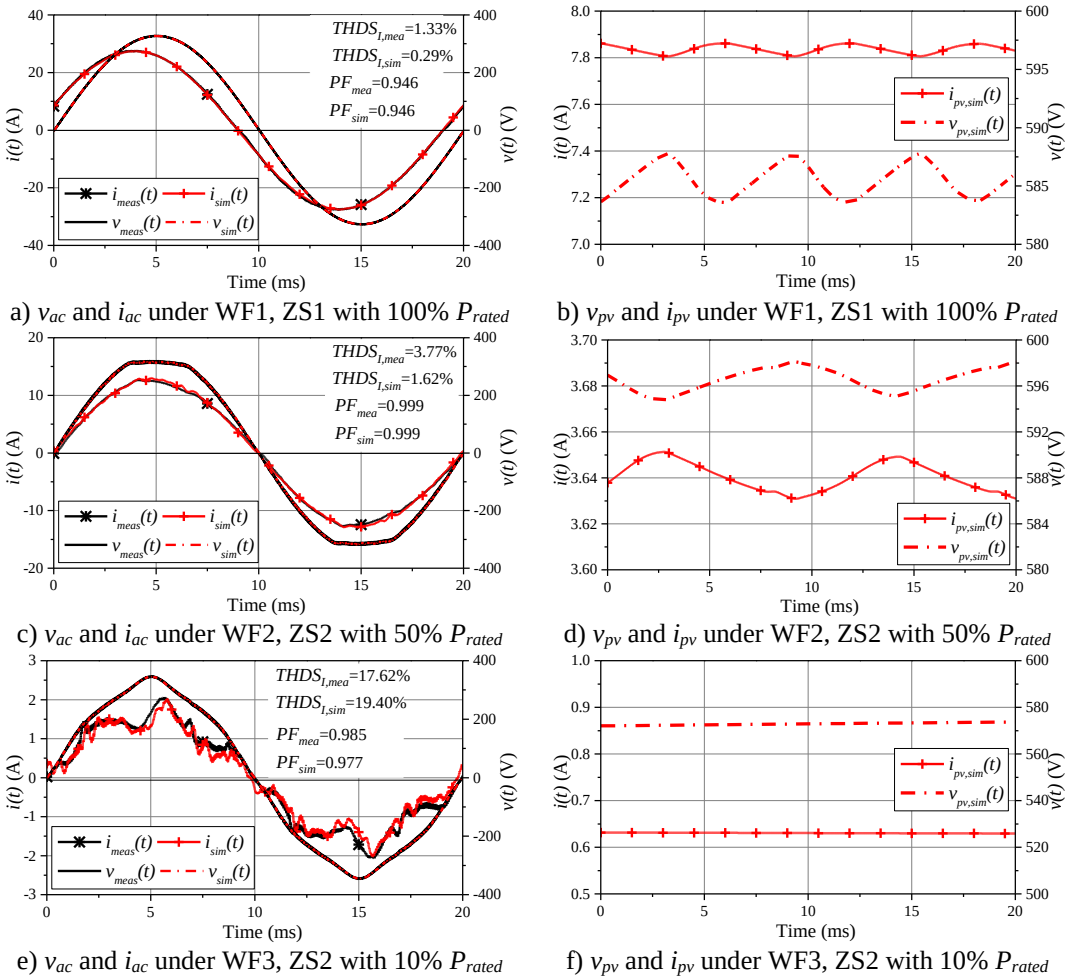



**Figure 6.26:** The block diagram of the peak current control applied to the full circuit PVI-A model.

**Table 6.6:** The main circuit parameter values of the full circuit PVI-A model.

| $C_{dc}$ (μF) | $L_i$ (mH) | $L_g$ (mH) | $C_{fi}$ (μF) | $R_d$ (Ω) | Sawtooth signal | |
|---|---|---|---|---|---|---|
| | | | | | Amplitude | Frequency |
| 2200 | 1.2 | 0.8 | 11 | 4 | 0.2 | 16 kHz |




a) $v_{ac}$ and $i_{ac}$ under WF1, ZS1 with 100% $P_{rated}$

b) $v_{pv}$ and $i_{pv}$ under WF1, ZS1 with 100% $P_{rated}$

c) $v_{ac}$ and $i_{ac}$ under WF2, ZS2 with 50% $P_{rated}$

d) $v_{pv}$ and $i_{pv}$ under WF2, ZS2 with 50% $P_{rated}$

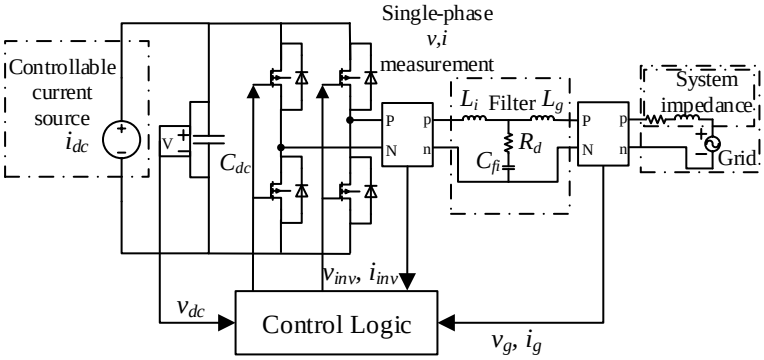
e) $v_{ac}$ and $i_{ac}$ under WF3, ZS2 with 10% $P_{rated}$

f) $v_{pv}$ and $i_{pv}$ under WF3, ZS2 with 10% $P_{rated}$

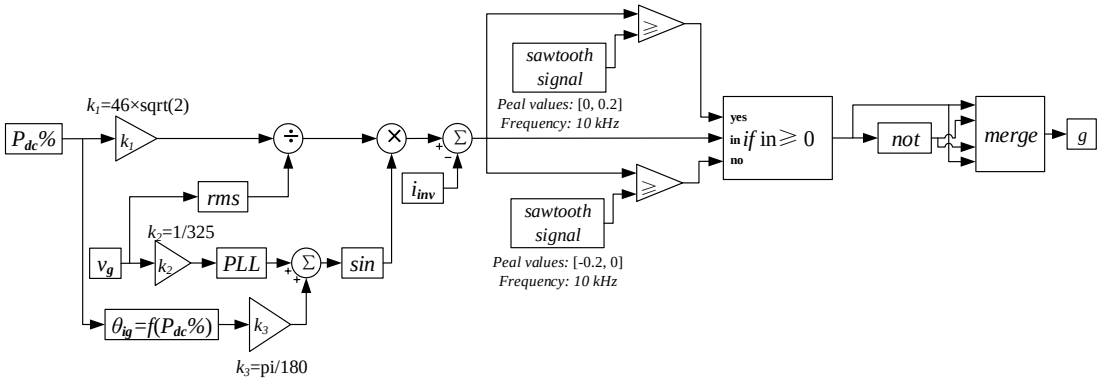
**Figure 6.27:** Simulated grid-side voltage and current, PV array voltage and current output of the full circuit PVI-A model under different supply conditions and powers.

As the general electrical characteristics of PVI is mainly determined by the DC-AC conversion part (i.e. the FB inverter with its control circuits), the full circuit model can be simplified by replacing the PV array and the MPPT circuits with a controllable current source, and the corresponding circuit schematic given in Figure 6.28. The output of the controllable current source is determined by the dc-link voltage and the power level. The neglecting of MPPT circuits will contribute to reduced simulation time, while the simplified circuit model is still able to accurately represent the

measured electrical characteristics of PVI-A, which is desirable for the further network analysis purpose.



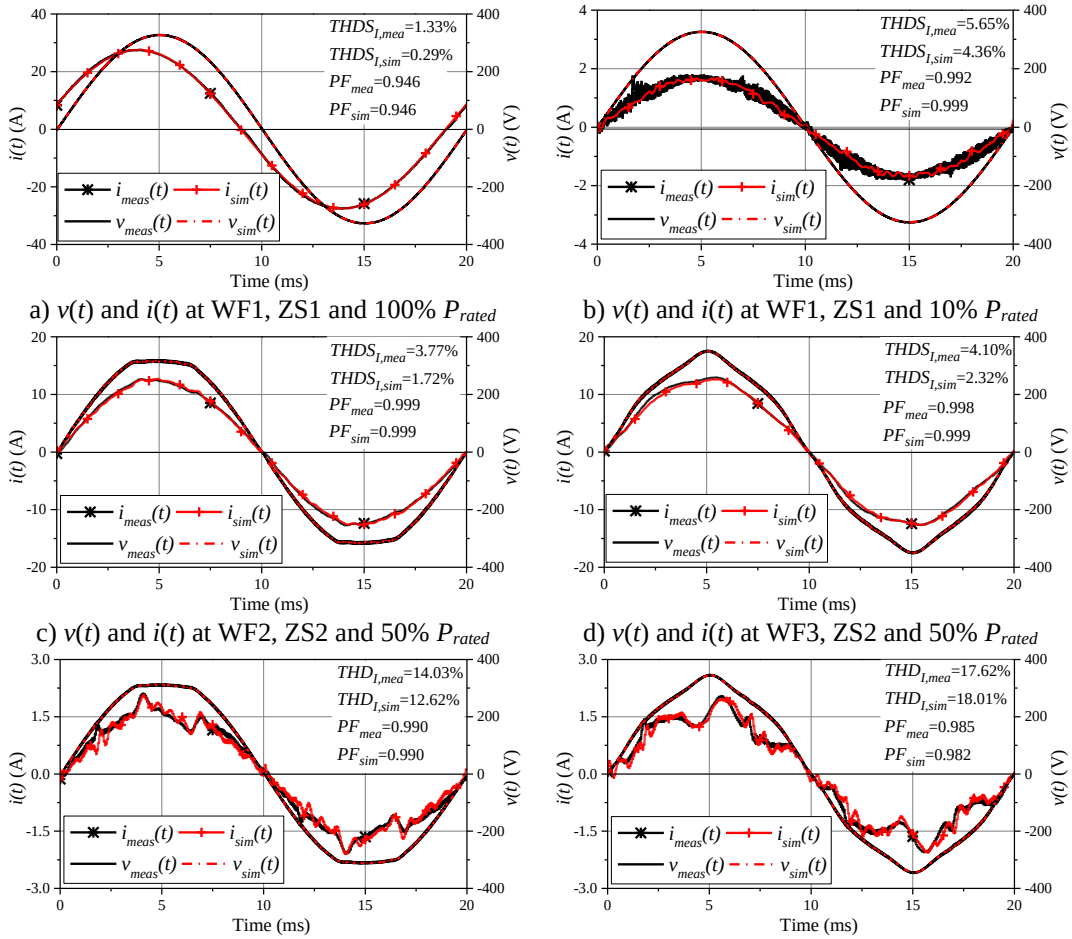

a) the circuit schematic of the simplified PVI-A model




b) the block diagram of the peak current control for the FB inverter

**Figure 6.28:** The schematic of the developed simplified component-based PVI-A model.

In order to evaluate the accuracy of the simplified component-based PVI-A model, the simulated and measured grid voltage and current waveforms are compared under different supply conditions (a combination of different supply waveform distortion and source impedance) and different operating powers as shown in Figure 6.29. It turns out that the developed simplified CBM is capable of accurately representing the grid-side current waveform distortion for PVI-A operating under all considered supply conditions and operating powers.




a) $v(t)$ and $i(t)$ at WF1, ZS1 and 100% $P_{rated}$

b) $v(t)$ and $i(t)$ at WF1, ZS1 and 10% $P_{rated}$

c) $v(t)$ and $i(t)$ at WF2, ZS2 and 50% $P_{rated}$

d) $v(t)$ and $i(t)$ at WF3, ZS2 and 50% $P_{rated}$

e) $v(t)$ and $i(t)$ at WF2, ZS2 and 10% $P_{rated}$

f) $v(t)$ and $i(t)$ at WF3, ZS2 and 10% $P_{rated}$

**Figure 6.28:** Comparison between measured and simulated (by using simplified CBM) grid-side voltage and current waveforms for PVI-A under different supply conditions and powers.

*b) Component-based modelling of PVI-B*

For the three-phase PVI-B, the circuit schematic of developed CBM in Matlab/Simulink is shown in Figure 6.30, with the corresponding block diagram of the control circuit illustrated in Figure 6.31. Specifically, the developed model is based on the voltage control mode (using PR controller) three-phase FB inverter, with the damped LC filter as the grid-side filter. As illustrated in Figure 6.31, the control circuit can be divided into two parts-three-phase grid synchronization part and the grid voltage control part. For the grid synchronization part, the instantaneous ac supply voltage waveform is detected and applied with the *abc* to *dq* transformation as input into a PLL for providing the synchronized reference frame into the closed loop control.

The grid voltage control consists of an outer current control (with the reference for the grid current magnitude achieved by a PI controller that is applied to the dc-link voltage) and an inner voltage control (with the reference for the grid voltage magnitude achieved by a PR controller that is applied to the grid current in the αβ frame). The final output of the control circuit is the scaled three-phase reference voltage waveforms for the average-model based FB inverter. The main circuit parameter values are tabulated in Table 6.7.

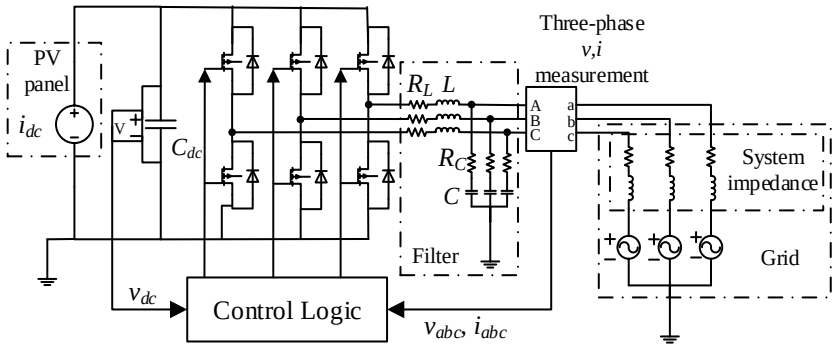



**Figure 6.29:** The schematic of the developed component-based PVI-B model.

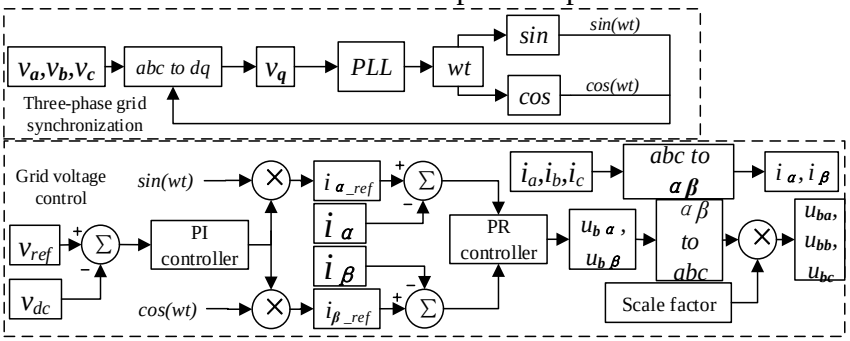


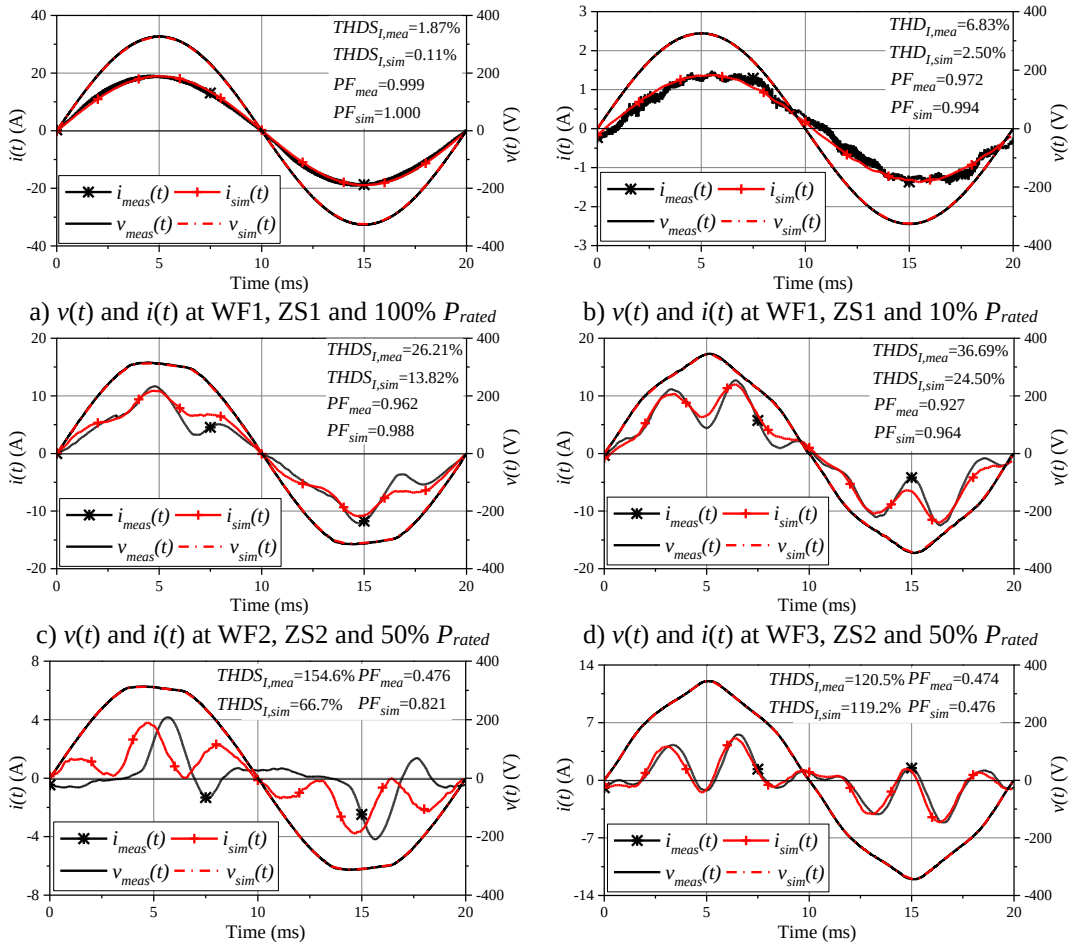

**Figure 6.30:** The block diagram of the control circuit of the PVI-B model.

**Table 6.7:** The main circuit parameter values of the component-based PVI-B model.

| **Input filter** | | | | **dc-link** | | **dc-link voltage PI controller** | | **Current PR controller** | | |
|---|---|---|---|---|---|---|---|---|---|---|
| ***L*** **(mH)** | $R_L$ **(Ω)** | ***C*** **(μF)** | $R_C$ **(Ω)** | $C_{dc}$ **(uF)** | $V_{dc}$ **(V)** | $K_P$ | $K_I$ **(s$^{-1}$)** | $K_P$ | $K_I$ **(s$^{-1}$)** | $\omega_C$ **(s$^{-1}$)** |
| 0.85 | 0.35 | 12 | 0.5 | 600 | 690 | 1.1 | 1 | 4 | 90 | 20 |

To evaluate the accuracy of the developed model, the simulated grid-side voltage and current waveforms are compared under different supply conditions, as shown in Figure 6.32. It is observed that although there is a small mismatch between simulated and measured current waveforms under certain testing points (e.g. Figure 6.32(e)), the

general current waveform characteristics are still well represented by the developed model.




a) $v(t)$ and $i(t)$ at WF1, ZS1 and 100% $P_{rated}$

b) $v(t)$ and $i(t)$ at WF1, ZS1 and 10% $P_{rated}$

c) $v(t)$ and $i(t)$ at WF2, ZS2 and 50% $P_{rated}$

d) $v(t)$ and $i(t)$ at WF3, ZS2 and 50% $P_{rated}$

e) $v(t)$ and $i(t)$ at WF2, ZS2 and 10% $P_{rated}$

f) $v(t)$ and $i(t)$ at WF3, ZS2 and 10% $P_{rated}$

**Figure 6.31:** Comparison between measured and simulated grid-side voltage and current waveforms for PVI-B under different supply conditions and powers.

## 6.4.2 Frequency-domain modelling

In this section, the FDMs for the three tested PVIs (PVI-A, PVI-B and PVI-C in Section 6.2) will be developed and discussed. In this section, the FDM refers to the HFM introduced in Chapter 2. In addition, PVIs are nonlinear power electronic devices with their current harmonic emission affected by both the operating power and the supply conditions [17][181][182]. Therefore, HFMs for PVIs requires to be developed at different operating powers in order to well represent the harmonic emission characteristics under the whole power range, which is typically achieved by individual voltage harmonic tests at considered powers. Accordingly, this section will first discuss the developed HFMs obtained from the individual voltage harmonic tests for

three PVIs operating at different power levels. After that, a novel approach of developing HFMs for PVIs is proposed and fully validated, which can significantly reduce the number of measurements required.

The comprehensive laboratory tests are performed for the single-phase PVI-A and PVI-C operating in the power range from 100% $P_{rated}$ down to 10% $P_{rated}$ with a step of 10% $P_{rated}$, and the three-phase PVI-B operating in the power range from 50% $P_{rated}$ down to 5% $P_{rated}$ with a step of 5% $P_{rated}$. At each power level, the considered voltage harmonic orders are 2, 4 and 6 (even orders) and 3, 5, 7, 9, 11, 13, 15, 17 and 19 (odd orders), with magnitudes varying from 0.1 of the corresponding limits, $V_{h,limit}$, in [40] to 1.2× $V_{h,limit}$, with a step of 0.1 $V_{h,limit}$, while the harmonic phase angles is varied from 0° to 360° in a step of 30°. During the individual harmonic tests, the rms value of the resultant supply voltage is maintained at 1 p.u. (230 V) and no source impedance was connected (except a small impedance of the connecting cables), according to the requirement given in [183]. Although maintaining the resultant supply voltage at 1 p.u. will make the fundamental component less than 1 p.u., the effect of individual voltage harmonic on the reduction of fundamental component is small enough to be ignored. For example, a 1 p.u. resultant voltage with an individual harmonic magnitude equalling to 6% $V_1$ (the maximum $V_{h,limit}$ given in [40]), have its $V_1$ equals to 0.9982 pu (229.59 V), suggesting that it is still reasonable to assume $V_1$ is maintained constant at 1 p.u. during the tests.

In addition to the individual harmonic tests, three different voltage waveform were also applied to three PVIs operating at the considered power levels, which are purely sinusoidal waveform WF1, "flat-top" waveform WF2 and "pointed-top" waveform WF3 with the same harmonic contents as given in previous chapters. The resultant voltage magnitude is adjusted from 0.9 p.u. to 1.1 p.u. with a step of 0.05 p.u.

**HAM% calculated from measurements**

The HFM development procedure is already fully discussed in Chapter 2 and is not repeated here. The obtained diagonal elements of HAM% at different power levels are illustrated in Figure 6.33, with the corresponding off-diagonal elements given in appendix A.1. As the magnitudes of off-diagonal elements are much smaller as opposed to those of diagonal elements, only diagonal elements will be discussed here.

The main observations from Figure 6.33 are: a) the diagonal elements of HAM% are strongly power dependent, which is more pronounced for PVI-B, b) the magnitudes of the diagonal elements (except the element at fundamental frequency whose magnitude is fixed at 1) apparently increase with the decrease of operating power, implying that the voltage waveform distortion has greater impacts on the current waveform distortion at low power, c) an approximate linear relationship can be observed among $\bar{\boldsymbol{Y}}_{\%}^{h,H}$ at different powers.

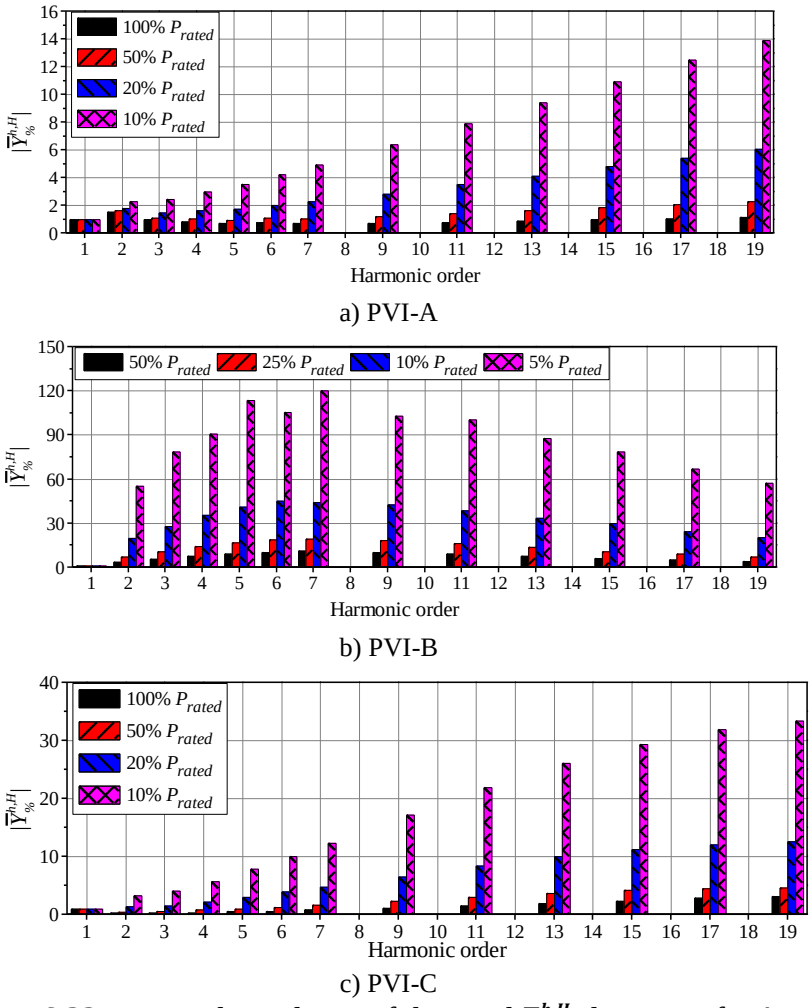



**Figure 6.32:** Power-dependency of diagonal $\bar{\boldsymbol{Y}}_{\%}^{h,H}$ elements of HAM%.

### *THD*-based approaches for HAM% estimation

Although $\bar{\boldsymbol{Y}}_{\%}^{h,H}$ have distinctive values under different power levels, the similarities among the $\bar{\boldsymbol{Y}}_{\%}^{h,H}$ distribution characteristics of different powers suggest that it is possible to estimate the HAM% at other power levels based on HAM% at reference power level (e.g. $P_{rated}$), which can avoid the troublesome individual voltage harmonic

tests and improve the practical applications of HFMs. The proposed approach for estimating HAM% at any power level, i.e. HAM%(P) is based on the following assumptions: 1) measurements of the individual harmonic tests are available for equipment operating at one power level (e.g. $P_{rated}$), in order to obtain the corresponding reference HAM%_ref. 2) measurements of device operating at the reference power level with ideally sinusoidal voltage and with sinusoidal voltage superimposed with combined voltage harmonics (e.g. WF2 and WF3) are available, in order to obtain $THDS_{I\_ref\_A}$ and $THDS_{I\_ref\_B}$ respectively. 3) part 2 of HAM%(P), i.e. $\bar{\boldsymbol{Y}}_{\%}^{h,1}(P)$, is assumed to be proportional to the part 2 of HAM%_ref, $\bar{\boldsymbol{Y}}_{\%\_ref}^{h,1}(P)$ while part 3 and part 4 of HAM%_ref, i.e. $\bar{\boldsymbol{Y}}_{\%}^{h,H}(P)$, is assumed to be proportional to the part 3 and part 4 of HAM%_ref, $\bar{\boldsymbol{Y}}_{\%\_ref}^{h,H}$, as shown in (6.16) and (6.17) respectively (the four parts of HAM% are indicated in (6.18) with more details given in Chapter 2). 4) measurements of device operating at considered power level with sinusoidal supply voltage and with sinusoidal supply voltage superimposed with combined voltage harmonics are available, in order to obtain $k_{THD\_A}$ and $k_{THD\_B}$ respectively.

$$\bar{\boldsymbol{Y}}_{\%}^{\boldsymbol{h,1}}(P) = k_{THD\_A}(P) \times \bar{\boldsymbol{Y}}_{\%\_\boldsymbol{ref}}^{\boldsymbol{h,1}} \tag{6.16}$$

$$\bar{\boldsymbol{Y}}_{\%}^{\boldsymbol{h,H}}(P) = k_{THD\_B}(P) \times \bar{\boldsymbol{Y}}_{\%\_\boldsymbol{ref}}^{\boldsymbol{h,H}} \tag{6.17}$$

$$\begin{bmatrix} \bar{I}_{\%\_Tot}^{1} \\ \bar{\boldsymbol{I}}_{\%\_\boldsymbol{Tot}}^{\boldsymbol{h}} \end{bmatrix} = \begin{bmatrix} \bar{I}_{\%}^{1} \\ \bar{I}_{\%}^{2} \\ \bar{I}_{\%}^{3} \\ \vdots \\ \bar{I}_{\%}^{h} \end{bmatrix} = \bar{V}_{\%}^{1} \begin{bmatrix} \bar{Y}_{\%}^{1,1} \\ \bar{Y}_{\%}^{2,1} \\ \bar{Y}_{\%}^{3,1} \\ \vdots \\ \bar{Y}_{\%}^{h,1} \end{bmatrix} + \bar{\boldsymbol{V}}^{\boldsymbol{H}} \begin{bmatrix} \bar{Y}_{\%}^{1,2} & \bar{Y}_{\%}^{1,3} & \dots & \bar{Y}_{\%}^{1,H} \\ \bar{Y}_{\%}^{2,2} & \bar{Y}_{\%}^{2,3} & \dots & \bar{Y}_{\%}^{2,H} \\ \bar{Y}_{\%}^{3,2} & \bar{Y}_{\%}^{3,3} & \dots & \bar{Y}_{\%}^{3,H} \\ \vdots & \vdots & \ddots & \vdots \\ \bar{Y}_{\%}^{h,2} & \bar{Y}_{\%}^{h,3} & \dots & \bar{Y}_{\%}^{h,H} \end{bmatrix} = \begin{bmatrix} \bar{I}_{\%\_A}^{1} \\ \bar{\boldsymbol{I}}_{\%\_\boldsymbol{A}}^{\boldsymbol{h}} \end{bmatrix} + \begin{bmatrix} \bar{I}_{\%\_B}^{1} \\ \bar{\boldsymbol{I}}_{\%\_\boldsymbol{B}}^{\boldsymbol{h}} \end{bmatrix} \tag{6.18}$$

where: the linear relationship between $\bar{\boldsymbol{Y}}_{\%}^{\boldsymbol{h,1}}(P)$ and $\bar{\boldsymbol{Y}}_{\%\_\boldsymbol{ref}}^{\boldsymbol{h,1}}$ is represented by $k_{THD\_A}$ and the linear relationship between $\bar{\boldsymbol{Y}}_{\%}^{\boldsymbol{h,H}}(P)$ and $\bar{\boldsymbol{Y}}_{\%\_\boldsymbol{ref}}^{\boldsymbol{h,H}}$ is represented by $k_{THD\_B}$ respectively; the Part 1 to Part 4 of HAM% are represented by black, red, blue and green rectangles respectively.

The estimation of $k_{THD\_A}$ and $k_{THD\_B}$ could be done in two different approaches, depending on the measurements available. In the following, all the three approaches will be discussed, with obtained coefficients and the estimated HAM%(P) compared

with each other. After that, the simulated time domain current waveform will be compared with the measured one to validate the proposed approach.

*a) HAM$_{\%}$(P) modification using only operation power*

In addition to the previous four basic assumptions, this approach requires the pre measurement data of device operating at ideally sinusoidal supply voltage, WF1, and the two typical distorted supply voltage found in LV network, WF2 and WF3, over the whole power range. This allows to obtain two corresponding three sets of values of $THDS_{I\_WF1}(P)$, $THDS_{I\_WF2}(P)$ and $THDS_{I\_WF3}(P)$, from which values of and $THDS_{I\_A}(P)$ and $THDS_{I\_B}(P)$ at operating power $P$ are calculated as:

$$THDS_{I\_A}(P) = THDS_{I\_WF1}(P) \tag{6.19}$$

$$THDS_{I\_B}(P) = \left(\frac{THDS_{I\_WF2}(P)+THDS_{I\_WF3}(P)}{2}\right) - THDS_{I\_A}(P) \tag{6.20}$$

Coefficients $k_{THD\_A}(P)$ and $k_{THD\_B}(P)$ will be directly calculated from the ratio of $THDS_{I\_A}(P)$ and $THDS_{I\_B}(P)$ to their corresponding reference values as shown in (6.21) and (6.22). With the obtained $k_{THD\_A}(P)$ and $k_{THD\_B}(P)$ over the whole power range, it is able to find corresponding coefficient values at any operating power by using a lookup table approach.

$$k_{THD\_A}(P) = THDS_{I\_A}(P)/THDS_{I\_ref\_A} \tag{6.21}$$

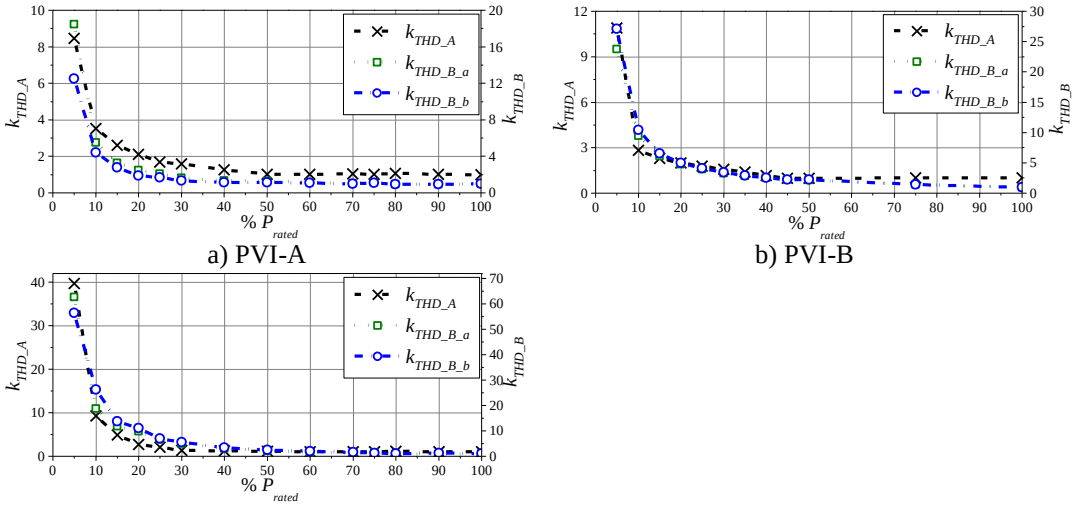
$$k_{THD\_B}(P) = THDS_{I\_B}(P)/THDS_{I\_ref\_B} \tag{6.22}$$

*b) HAM$_{\%}$(P) modification using actual THDS$_I$ value for PVI operating at specific power with any distorted supply voltage.*

If actual $THDS_I$ value is available for equipment operating at specific power $P$ and for any given distorted supply voltage supply conditions, e.g. from the field measurement, this can be used for a direct calculation of the coefficient $k_{THD\_B}(P)$, while the calculation of coefficient $k_{THD\_A}(P)$ is the same with approach a (i.e. determined from the tests with ideally sinusoidal supply voltage). If the available actual measured value is denoted as $THDS_{I\_actual}(P)$, $k_{THD\_B}(P)$ can be calculated as (6.23) instead of (6.22) in approach a. In the case here, it is assumed that $THDS_{I\_actual}(P)$ is obtained from measurement under WF2 and therefore, $THDS_{I\_actual}(P)$ equals $THDS_{I\_WF2}(P)$.

$$k_{THD\_B}(P) = (THDS_{I_{actual}}(P) - THDS_{I_A})/THDS_{I\_ref\_B} \quad (6.23)$$

The obtained coefficients $k_{THD\_A}(P)$ and $k_{THD\_B}(P)$ of using the two approaches (denoted as $k_{THD\_B\_a}$ and $k_{THD\_B\_b}$ for approach a and b respectively) for the three PVIs are illustrated in Figure 6.34, where $HAM_{\%\_ref}$ is available for PVI-A and PVI-C operating at 100% $P_{rated}$ and PVI-B operating at 50% $P_{rated}$. It is observed that the selection of the approaches result in different values of $k_{THD\_B}(P)$, especially the low power range (below 10% $P_{rated}$).



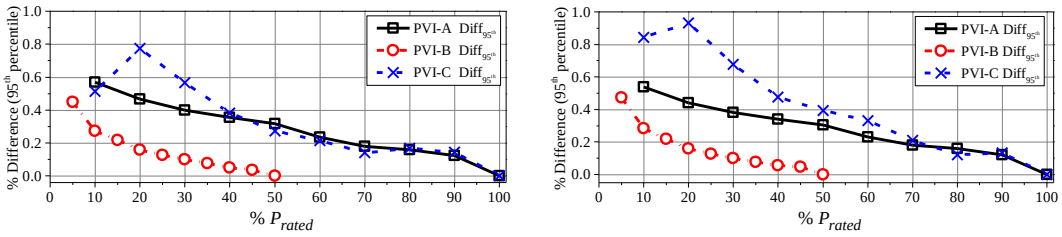

a) PVI-A b) PVI-B

c) PVI-C

**Figure 6.33:** Illustration of calculated coefficients $k_{THD\_A}(P)$ and $k_{THD\_B}(P)$, based on power-dependent changes of $THDS_{I\_A}(P)$ and $THDS_{I\_B}(P)$, respectively.

To evaluate the accuracy of the proposed approaches for $HAM_{\%\_ref}$ estimation, the estimated values of $HAM_{\%\_est}(P)$ elements, $\bar{\boldsymbol{Y}}^{h,H}_{\%\_est}(P)$, are compared with the values obtained in measurements, i.e. with $HAM_{\%\_meas}(P)$ calculated from a full set of HFM measurements at each considered operating power $P$, giving corresponding elements $\bar{\boldsymbol{Y}}^{h,H}_{\%\_meas}(P)$. Figure 6.35 illustrates that 95$^{th}$ percentile values of relative differences between $\bar{\boldsymbol{Y}}^{h,H}_{\%\_est}(P)$ and $\bar{\boldsymbol{Y}}^{h,H}_{\%\_meas}(P)$ for all three PVIs under their entire operating power range are small, based on (6.24).

$$DIFF_{95^{th}}(P) = \left(\frac{|\bar{Y}^{h,H}_{\%est}(P) - \bar{Y}^{h,H}_{\%meas}(P)|}{\sum_{H=1}^{n}\sum_{h=1}^{n}|\bar{Y}^{h,H}_{\%meas}(P)|}\right)_{95^{th}} \times 100\% \quad (6.24)$$



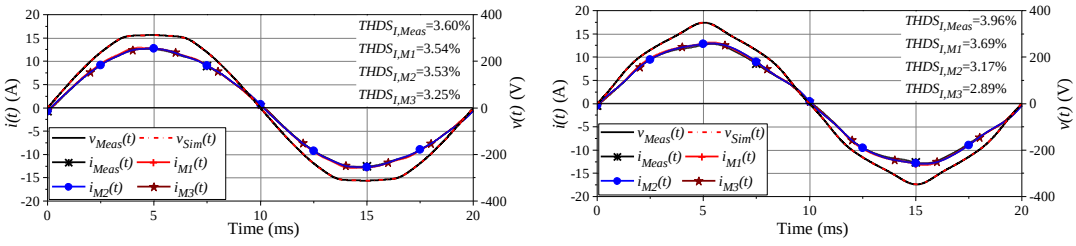

a) approach a b) approach b

**Figure 6.34:** The 95th percentile values of relative differences between $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\%\_\boldsymbol{est}}(\boldsymbol{P})$ and $\bar{\boldsymbol{Y}}^{\boldsymbol{h,H}}_{\%\_\boldsymbol{meas}}(\boldsymbol{P})$ (for both approach a and approach b).

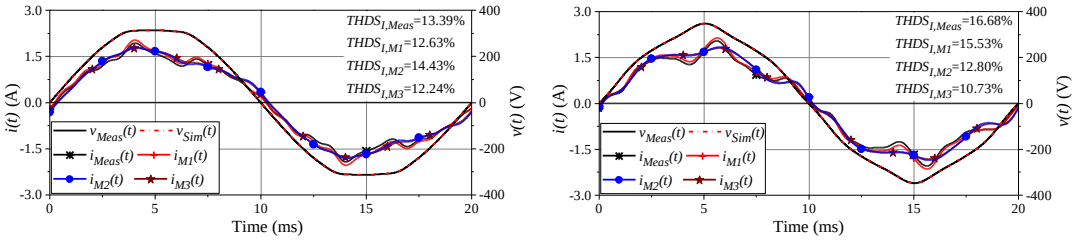
**Time-domain validation of HFMs**

In order to assess the accuracy of developed HFMs for three PVIs, the simulated time-domain current waveforms are compared with the measurements for WF2 and WF3 distorted supply voltage, as illustrated in Figures 6.36-6.38. The notations used in the figures are defied as follows: measured instantaneous voltage and current waveforms, $v(t)$ and $i(t)$, and the relevant $THDS_I$ are denoted with a subscript "Meas"; " ; $i(t)$ and its $THDS_I$ values reconstructed from measurement-based HFMs at specific operating power are denoted as "M1"; $i(t)$ and its $THDS_I$ values reconstructed from the modified HFM using only PVI operating power are denoted as "M2"; $i(t)$ and its $THDS_I$ values reconstructed from the modified HFM using actual $THDS_I$ value at specific PVI operating power are denoted as "M3".

It is observed from Figures 6.36-6.38 that all the three HFMs can well represent the current waveform distortion at different operating powers, demonstrating the accuracy of the proposed HAM%(P) modification approaches which can also be easily applied to other power-dependent PE devices with similar characteristics.

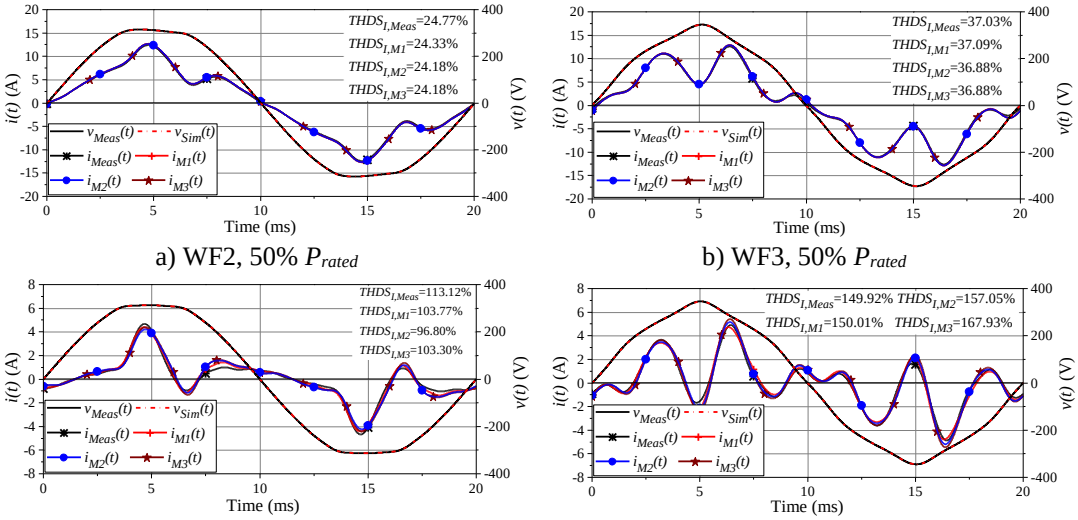



a) WF2, 50% $P_{rated}$ b) WF3, 50% $P_{rated}$




c) WF2, 10% $P_{rated}$ d) WF3, 10% $P_{rated}$

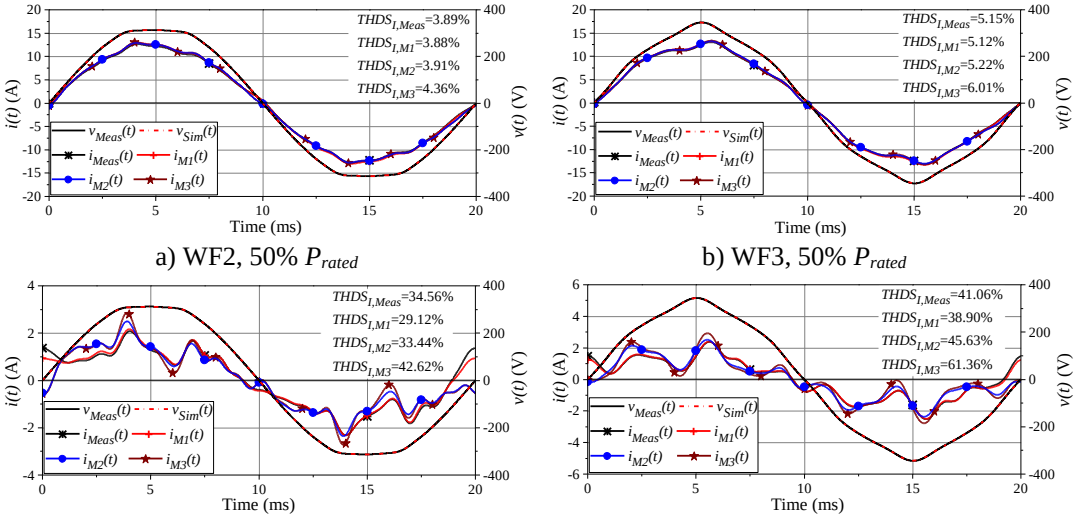
**Figure 6.35:** Comparison of measured and reconstructed instantaneous current waveforms from different HFMs for PVI-A.




a) WF2, 50% $P_{rated}$ b) WF3, 50% $P_{rated}$

c) WF2, 10% $P_{rated}$ d) WF3, 10% $P_{rated}$

**Figure 6.36:** Comparison of measured and reconstructed instantaneous current waveforms from different HFMs for PVI-B.




a) WF2, 50% $P_{rated}$ b) WF3, 50% $P_{rated}$

c) WF2, 10% $P_{rated}$ d) WF3, 10% $P_{rated}$

**Figure 6.37:** Comparison of measured and reconstructed instantaneous current waveforms from different HFMs for PVI-C.

## 6.5 Aggregate harmonic fingerprint models

In this part, the operation of parallel-connected PVI units will be further analysed and evaluated, investigating whether the correct aggregate HFM can be obtained from their individual HFMs, by summing-up the corresponding HAM elements. This part compares the results for the aggregate HFMs obtained using individual HFMs from measurement-based and two proposed approaches with modified HAMs, which are illustrated using an example of two parallel-connected PVIs that are also analysed in Section 6.4.2.

The main objective of this part is to answer the following question: If individual HFMs are available for two or more parallel-connected power electronic devices, how accurate is an aggregate HFM obtained by summing-up corresponding HAM elements from their individual HFMs. The analysis is illustrated using an example of two parallel-connected PVIs operating at same or different powers, where summing (i.e. superposition) of HAM elements of individual HFMs is performed for four different types of individual HFMs (two are obtained in measurements and two are based on the modifications presented in Section 6.4.2). These four sets of aggregate HFM-results are compared with the aggregate HFM obtained in direct measurements with two PVIs operating together, which is used as a reference model for the validation.

### 6.5.1 Measurement-based aggregate HFMs

A measurement-based aggregate HFM of two or more parallel-connected devices can be obtained in the same way as their individual HFMs. In the considered case of two parallel-connected PVIs, the same experimental set-up described and used in Section 6.4.2 for obtaining their individual measurement-based HFMs is also used to obtain their measurement-based aggregate HFM, with only one significant difference: two PV emulators are used and connected to two different PVIs, in order to adjust selected combinations of their operating powers. Furthermore, both PVIs are connected in parallel to a controllable three-phase power source, as one of the two PVIs is a three-phase unit. The basic experimental setup with marked relevant voltages and currents is illustrated in Figure 6.39, while further details can be found in [146][182][183].

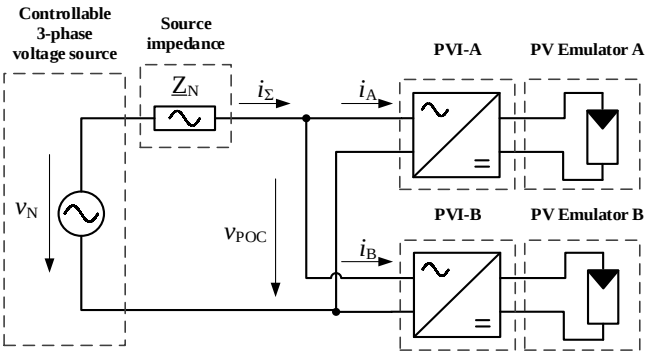



**Figure 6.38:** Measurement setup.

The two tested PVIs, marked as "PVI-A" and "PVI-B" in accordance to the notation used in Section 6.4.2, are measured when operating individually and when operating in parallel, using the same test procedure described in Section 6.4.2 (regarding considered harmonic orders, adjusted operating powers, rms voltage magnitudes, etc.). Based on these measurements, the corresponding individual HFMs, with related HAMs, are obtained for PVI-A operating in the range from 100% of $P_{rated}$ down to 10% of $P_{rated}$ with a step of 10% of $P_{rated}$ and for PVI-B from 50% to 5% of $P_{rated}$, with a 5% step, as well as variations of rms voltage magnitudes in the range from 0.9 pu to 1.1 pu. Regarding the measurements of the two parallel-connected PVIs, the tested combinations of operating powers of PVI-A and PVI-B connected together are listed in Table 6.8.

**Table 6.8:** Tested operating powers for parallel-connected PVIs.

| **Case Identifier (P1&P2)** | **Operating Power (in % of $P_{rated}$)** | |
|---|---|---|
| | ***PVI-A (P1)*** | ***PVI-B (P2)*** |
| **Case 10&10** | 10 % | 10 % |
| **Case 10&50** | 10 % | 50 % |
| **Case 50&10** | 50 % | 10 % |
| **Case 50&50** | 50 % | 50 % |

In order to provide a clear distinction based on notation applied in Part 1 paper, the *measurement-based individual* HFMs and corresponding HAM elements, obtained for PVI-A and PVI-B operating at specific powers P1 and P2, are denoted as "M1": $HFM_{M1\_PVI\text{-}A}(P1)$, $HAM_{\%\_M1\_PVI\text{-}A}(P1)$ and $\underline{Y}^{h,H}_{\%\_M1\_PVI-A}(P1)$ for PVI-A, and $HFM_{M1\_PVI\text{-}B}(P2)$, $HAM_{\%\_M1\_PVI\text{-}B}(P2)$ and $\underline{Y}^{h,H}_{\%_{M1_{PVI}}-B}(P2)$ for PVI-B.

The *measurement-based aggregate* HFMs and corresponding HAM elements are marked with the additional subscript "Agg", corresponding to two following types of *measurement based aggregate* HFMs obtained by:

1. Direct measurements of parallel-connected PVI-A and PVI-B, operating at powers P1 and P2, denoted as "Ma" values: $HFM_{Agg\_Ma}$(P1&P2), $HAM_{\%\_Agg\_Ma}$(P1&P2) and $\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2)$, and

2. Summing-up Y-elements of two individual measurement-based HFMs for PVI-A and PVI-B, operating at powers P1 and P2, denoted as "M1" values: $HFM_{Agg\_M1}$(P1&P2), $HAM_{\%\_Agg\_M1}$(P1&P2) and $\underline{Y}^{h,H}_{\%\_Agg\_M1}(P1\&P2)$.

The calculation (summing-up) of $HAM_{\%\_Agg\_M1}$(P1&P2) elements from $HAM_{\%\_M1\_PVI\text{-}A}$(P1) and $HAM_{\%\_M1\_PVI\text{-}B}$(P2) elements is performed using:

$$\underline{Y}^{h,H}_{\%_{Agg}\ \ M1}(P1\&P2)\frac{\bar{I}^1_{Tot}(P1\&P2)}{\bar{V}^1} =$$

$$= \underline{Y}^{h,H}_{\%\_M1\_PVI-A}(P1)\frac{\bar{I}^1_{PV-A}(P1)}{\bar{V}^1} + \underline{Y}^{h,H}_{\%\_M1\_PVI-B}(P2)\frac{\bar{I}^1_{PV-B}(P2)}{\bar{V}^1} \qquad (6.25)$$

where normalized values are obtained from absolute values using the corresponding fundamental input ac currents, $\bar{I}^1_{PVI-A}(P1)$, for PVI-A at power P1, $\bar{I}^1_{PVI-B}(P2)$, for PVI-B at power P2, $\bar{I}^1_{Tot}(P1\&P2)$, for PVI-A and PVI-B connected in parallel and operating at P1 and P2, respectively.

## 6.5.2 Aggregate HFMs based on two HAM modifications

The two HAM modifications presented in Section 6.4.2 allow to obtain two corresponding HFMs for individual PVIs with a significant reduction of required measurements, [18]. Both modifications use only one "reference HAM", multiplied by two coefficients calculated from power-dependent changes of PVIs total subgroup current harmonic distortion, $THDS_I$. This simplifies representation of power-dependent changes of PVIs harmonic characteristics, as the two related coefficients can be either prepared in advance and used as a "look-up table" (the first modification), or calculated from the actual $THDS_I$ value for a PVI operating at specific power and under specific voltage supply condition (the second modification). In that way, two

proposed modifications allow for a simple but correct representation of PVIs harmonic characteristics for the entire range of their operating powers and for different voltage supply conditions, which is crucial for evaluating aggregate impact of a large number of PVIs.

Following the same notation applied in Section 6.4.2, the two *modification-based individual* HFMs and corresponding HAM elements for PVI-A and PVI-B operating at powers P1 and P2 are denoted as "M2" and "M3" values, i.e. as: $HFM_{M2\_PVI\text{-}A}(P1)$, $HAM_{\%\_M2\_PVI\text{-}A}(P1)$ and $\underline{Y}^{h,H}_{\%\_M2\_PVI-A}(P1)$, and also $HFM_{M3\_PVI\text{-}A}(P1)$, $HAM_{\%\_M3\_PVI\text{-}A}(P1)$ and $\underline{Y}^{h,H}_{M3_{PVI}-A}(P1)$for PVI-A, as well as $HFM_{M2\_PVI\text{-}B}(P2)$, $HAM_{\%\_M2\_PVI\text{-}B}(P2)$ and $\underline{Y}^{h,H}_{\%_{M2_{PVI}}-B}(P2)$, and $HFM_{M3\_PVI\text{-}B}(P2)$, $HAM_{\%\_M3\_PVI\text{-}B}(P2)$ and $\underline{Y}^{h,H}_{M3\_PVI-B}(P2)$ for PVI-B.

The *modification-based aggregate* HFMs and corresponding HAM elements are again marked with the additional subscript "Agg", this time corresponding to the two following types of *modification-based* aggregate HFMs obtained by:

1. Summing-up Y-elements of two individual modification-based HFMs related to modification M2 for PVI-A and PVI-B, operating at powers P1 and P2, denoted as "M2" values: $HFM_{Agg\_M2}(P1\&P2)$, $HAM_{\%\_Agg\_M2}(P1\&P2)$ and $\underline{Y}^{h,H}_{\%\_Agg\_M2}(P1\&P2)$, and

2. Summing-up Y-elements of two individual modification-based HFMs related to modification M3 for PVI-A and PVI-B, operating at powers P1 and P2, denoted as "M3" values: $HFM_{Agg\_M3}(P1\&P2)$, $HAM_{\%\_Agg\_M3}(P1\&P2)$ and $\underline{Y}^{h,H}_{\%\_Agg\_M3}(P1\&P2)$.

The calculation (summing-up) of $HAM_{\%\_Agg\_M2}(P1\&P2)$ elements from $HAM_{\%\_M2\_PVI\text{-}A}(P1)$ and $HAM_{\%\_M2\_PVI\text{-}B}(P2)$ is performed using:

$$\underline{Y}^{h,H}_{\%_{Agg_{M2}}}(P1\&P2)\frac{\bar{I}^1_{Tot}(P1\&P2)}{\bar{V}^1}$$

$$= \underline{Y}^{h,H}_{\%\_M2\_PVI-A}(P1)\frac{\bar{I}^1_A(P1)}{\bar{V}^1} + \underline{Y}^{h,H}_{\%\_M2\_PVI-B}(P2)\frac{\bar{I}^1_B(P2)}{\bar{V}^1} \qquad (6.26)$$

while calculation (summing-up) of $HAM_{\%\_Agg\_M3}$(P1&P2) elements from $HAM_{\%\_M3\_PVI\text{-}A}$(P1) and $HAM_{\%\_M3\_PVI\text{-}B}$(P2) is performed using:

$$\underline{Y}^{h,H}_{\%Agg_{M3}}(P1\&P2)\frac{\bar{I}^1_{Tot}(P1\&P2)}{\bar{V}^1}$$

$$= \underline{Y}^{h,H}_{\%\_M3\_PVI-A}(P1)\frac{\bar{I}^1_A(P1)}{\bar{V}^1} + \underline{Y}^{h,H}_{\%\_M3\_PVI-B}(P2)\frac{\bar{I}^1_B(P2)}{\bar{V}^1} \quad (6.27)$$

where again absolute values are calculated from normalized values using the corresponding fundamental currents.

## 6.5.3 One fixed-power measurement-based aggregate HFM

An additional case is introduced to check the errors when only one measurement-based aggregate HFM, obtained for the fixed operating powers of two individually measured PVIs, is used for representing power-dependent changes of their aggregate harmonic characteristics. Although any pair of operating power levels can be used for this comparison, in this paper PVI-A and PVI-B are adjusted to both operate at 50% of their rated powers, i.e. at the middle of their operating ranges. The corresponding *measurement based aggregate* HFM is obtained by summing-up individual HAMs of PVI-A and PVI-B, and is denoted as "M4": $HFM_{Agg\_M4}$(50&50), $HAM_{\%\_Agg\_M4}$(50&50) and $\underline{Y}^{h,H}_{\%Agg_{M4}}(50\&50)$. This HFM corresponds to one of measurement-based aggregate HFMs already available from "M1" aggregate HFMs (Case 50&50).

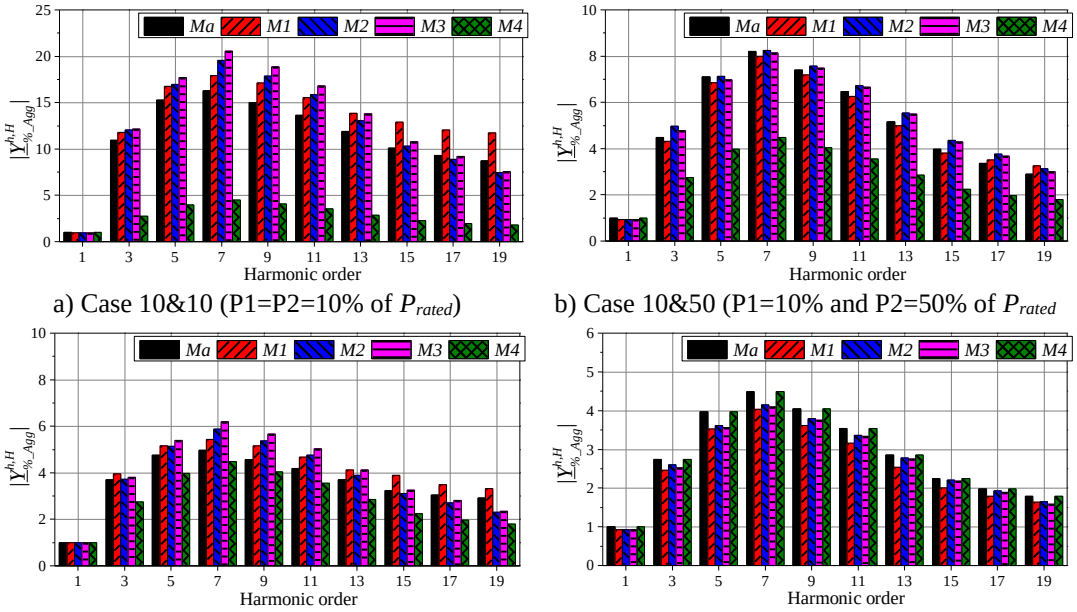
## 6.5.4 Comparison of different aggregate HFMs

This section compares results for five different aggregate $HFM_{Agg}$, denoted as "Ma", "M1", "M2", "M3" and "M4" based on the nomenclature described in the previous section. The reference model is $HFM_{Agg\_Ma}$, i.e. aggregate HFM obtained in direct measurements of two parallel-connected PVIs operating at specific combination of powers.

### Comparison of Magnitudes of $HAM_{\%\_Agg}$ Elements

The comparison of five different $HAM_{\%\_Agg}$(P1&P2) is performed for only diagonal elements, $\underline{Y}^{h,H}_{\%\_Agg}(P1\&P2)$, *h=H*, as off-diagonal elements are small. The results are illustrated in Figure 6.40, where up to a five-fold increase in values of

$HAM_{\%\_Agg}$ elements can be observed when parallel-connected PVIs transfer from medium operating powers (Case 50&50) to very low operating powers (Case 10&10).




a) Case 10&10 (P1=P2=10% of $P_{rated}$) b) Case 10&50 (P1=10% and P2=50% of $P_{rated}$

c) Case 50&10 (P1=50% and P2=10% of $P_{rated}$) d) Case 50&50 (P1=P2=50% of $P_{rated}$)

**Figure 6.39:** Power-dependency of diagonal elements of different $HAM_{\%\_Agg}$.

### Relative Differences of $HAM_{\%\_Agg}$ Elements

In order to assess the accuracy of the different aggregate HFMs, the 95$^{th}$ percentile values of the relative differences between the $HAM_{\%\_Agg}$ (P1&P2) elements for models "M1", "M2","M3" and "M4" and "Ma" model values (obtained in direct measurements with parallel-connected PVIs) are calculated with (6.28), (6.29), (6.30) and (6.31), respectively, and listed in Table 6.9.

$$DIFF_{95^{th}\_M1}(P1\&P2) = \left(\frac{|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2) - \underline{Y}^{h,H}_{\%\_Agg\_M1}(P1\&P2)|}{\sum_{H=1}^{n}\sum_{h=1}^{n}|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2)|}\right)_{95th} \times 100\% \qquad (6.28)$$

$$DIFF_{95^{th}\_M2}(P1\&P2) = \left(\frac{|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2) - \underline{Y}^{h,H}_{\%\_Agg\_M2}(P1\&P2)|}{\sum_{H=1}^{n}\sum_{h=1}^{n}|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2)|}\right)_{95th} \times 100\% \qquad (6.29)$$

$$DIFF_{95^{th}\_M3}(P1\&P2) = \left(\frac{|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2) - \underline{Y}^{h,H}_{\%\_Agg\_M3}(P1\&P2)|}{\sum_{H=1}^{n}\sum_{h=1}^{n}|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2)|}\right)_{95th} \times 100\% \qquad (6.30)$$

$$DIFF_{95^{th}\_M4}(P1\&P2) = \left(\frac{|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2) - \underline{Y}^{h,H}_{\%\_Agg\_M4}(P1\&P2)|}{\sum_{H=1}^{n}\sum_{h=1}^{n}|\underline{Y}^{h,H}_{\%\_Agg\_Ma}(P1\&P2)|}\right)_{95th} \times 100\% \qquad (6.31)$$

**Table 6.9:** The 95th percentile values of relative differences between M1-M4 $HAM_{\%\_Agg}$ elements and Ma $HAM_{\%\_Agg}$. elements.

| Case | $\boldsymbol{DIFF_{95th\_M1}(P1\&P2)}$, $\boldsymbol{DIFF_{95th\_M2}(P1\&P2)}$, $\boldsymbol{DIFF_{95th\_M3}(P1\&P2)}$ and $\boldsymbol{DIFF_{95th\_M4}(P1\&P2)}$ in % | | | |
|---|---|---|---|---|
| | **M1** | **M2** | **M3** | **M4** |
| **Case 10&10** | 2.51 | 2.87 | 3.57 | 6.01 |
| **Case 10&50** | 0.92 | 0.65 | 0.50 | 2.81 |
| **Case 50&10** | 1.40 | 2.97 | 3.54 | 2.28 |
| **Case 50&50** | 0.77 | 0.77 | 0.96 | 0 |

## 6.5.5 Time- and frequency-domain validation

This section provides the results of the comparisons of all considered aggregate $HFM_{Agg}$ in both time-domain (by comparing the reconstructed instantaneous current waveforms with the measured ones) and in frequency-domain (by comparing the calculated harmonic magnitudes and phase angles with the measured ones).

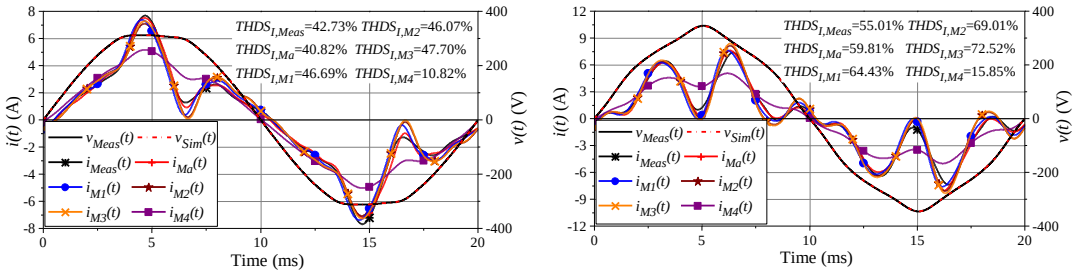
**Comparison of time-domain current waveforms**

This part compares reconstructed instantaneous current waveforms with measured instantaneous current waveforms for two parallel-connected PVIs operating at different powers and supplied with voltage waveforms WF2 and WF3 (Section 6.4.2 provides description of used waveforms). The notation is following nomenclature from Section 6.4.2 and descriptions from Section 6.5.4: measured instantaneous voltage waveforms, *v(t)*, and instantaneous current waveforms, *i(t)*, and related $THDS_I$ values are denoted with a subscript "Meas"; *i(t)* and related $THDS_I$ values reconstructed from aggregate HFM obtained in direct measurements with two parallel-connected PVIs operating at corresponding operating powers are denoted as "Ma"; *i(t)* and related $THDS_I$ values reconstructed from the aggregate HFM obtained by summing-up two individual HAMs, obtained in separate measurements of each PVI operating at corresponding powers, are denoted as "M1"; *i(t)* and related $THDS_I$ values reconstructed from the aggregate HFM obtained by summing-up two individual HAMs, obtained by applying the first modification (i.e. based on only operating powers of PVIs, as described in Section 6.4.2) are denoted as "M2"; "; *i(t)* and related $THDS_I$ values reconstructed from the aggregate HFM obtained by summing-up two individual HAMs, obtained by applying the second modification (i.e. based on

operating powers and $THDS_I$ values of PVIs, as described in Part 1 paper ) are denoted as “M3”; and *i(t)* and related $THDS_I$ values reconstructed from aggregate HFM obtained by summing-up two individual HAMs of both PVIs operating at fixed power of 50% of their rated powers are denoted as “M4”.

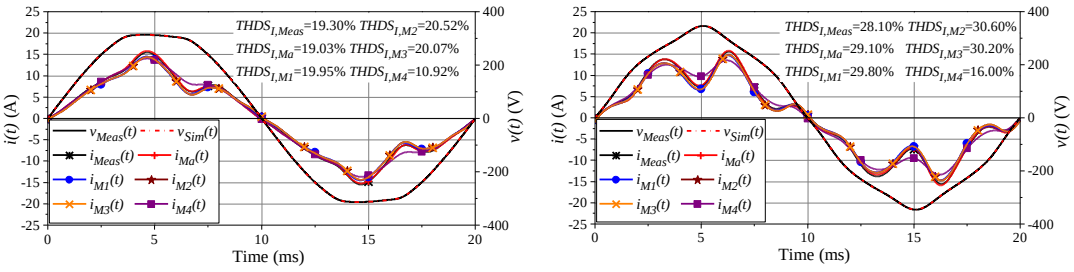
The results for time-domain comparison are given in Figures. 6.41-6.44, demonstrating, as expected, excellent accuracy of measurement-based aggregate HFMs, assuming they are obtained for the correct PVIs operating powers (results for Ma and M1). If, however, measurement-based aggregate HFM is obtained for one fixed operating power of PVIs and used for modelling operation of PVIs at other operating powers (results for M4), this will result in a fixed instantaneous current waveform, which will introduce errors at other powers.

The results in Figures. 6.41-6.44 also demonstrate a very good accuracy of modification-based aggregate HFMs, obtained by summing-up the corresponding HAM elements from the two individual HFMs. Further to results in Section 6.4.2, this confirms that the proposed approach is not only correct for modelling of aggregated PVIs power-dependent harmonic characteristics, but can also correctly represent overall behavior of aggregated PVIs.



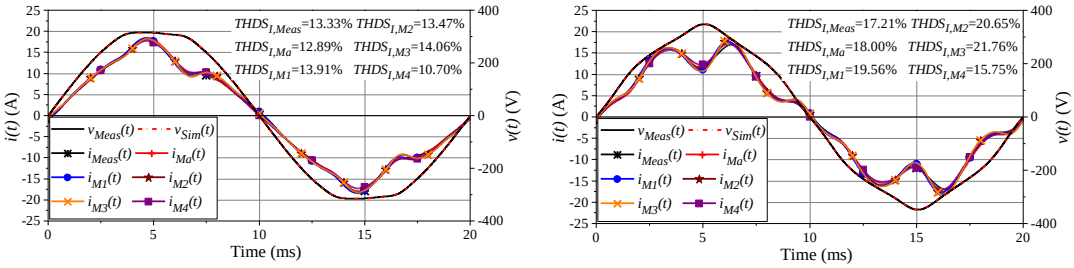

a) WF2 b) WF3

**Figure 6.40:** Time-domain comparison (Case 10&10).



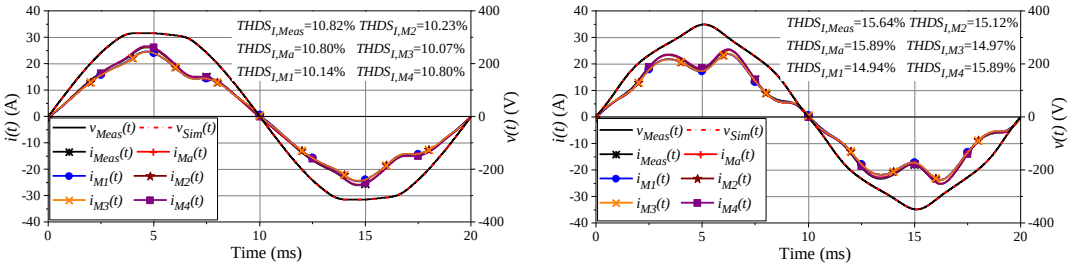

a) WF2 b) WF3

**Figure 6.41:** Time-domain comparison (Case 10&50).




a) WF2 b) WF3

**Figure 6.42:** Time-domain comparison (Case 50&10).

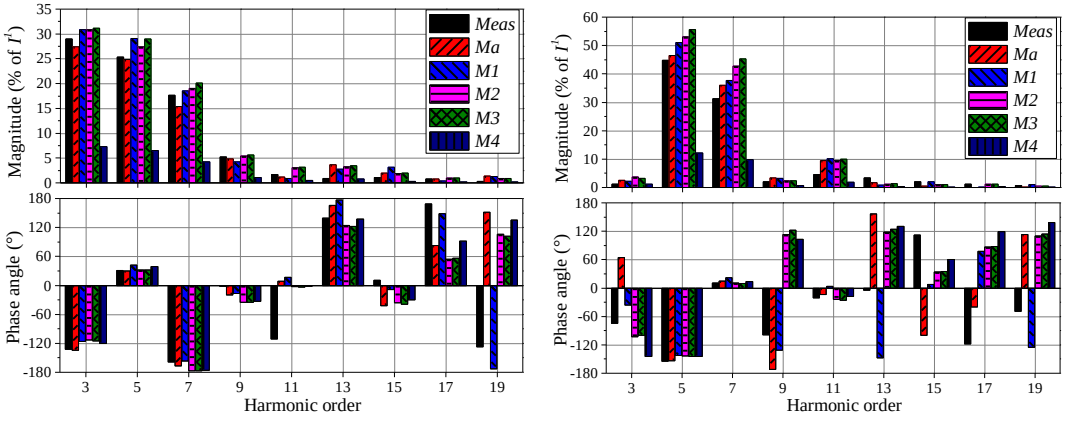



a) WF2 b) WF3

**Figure 6.43:** Time-domain comparison (Case 50&50).

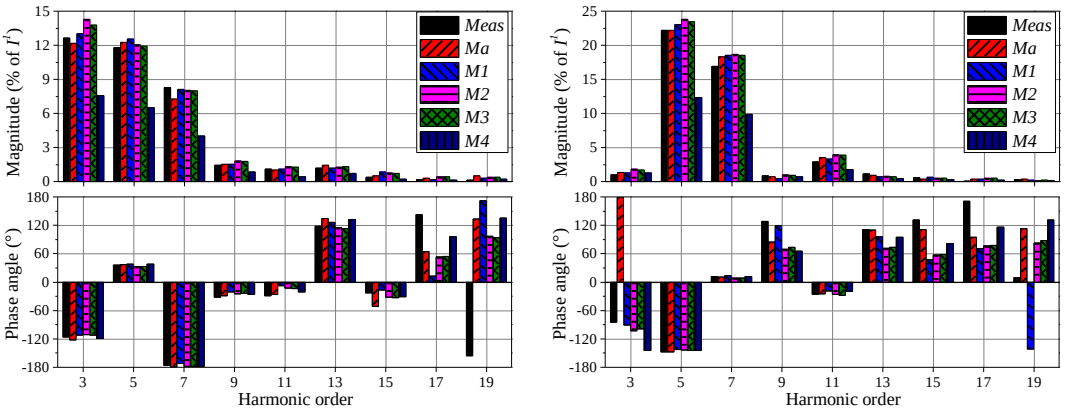
### Comparison of frequency-domain current harmonics

This part compares the results for harmonic magnitudes and phase angles obtained by the considered aggregate HFMs with the corresponding measured results obtained for two parallel-connected PVIs operating at different powers and supplied with voltage waveforms WF2 and WF3. These results, shown in Figures. 6.45-6.48, confirm conclusions drawn from the time-domain validation.



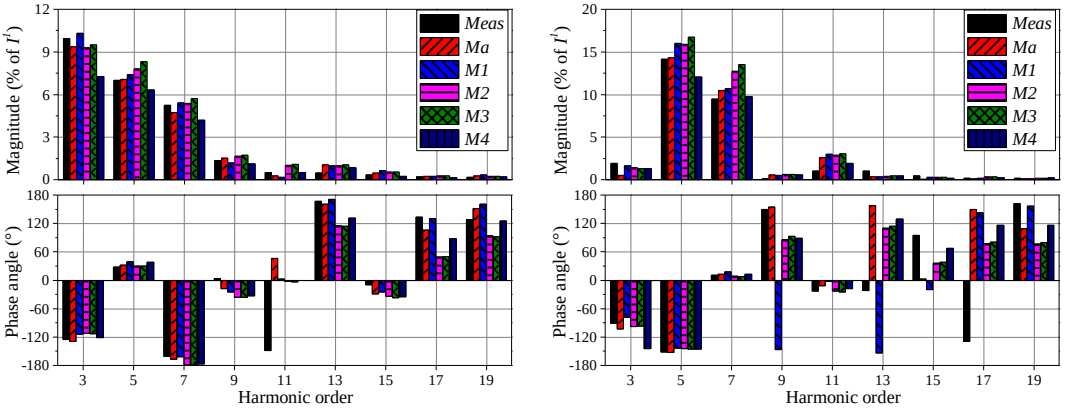

a) WF2 b) WF3

**Figure 6.44:** Frequency-domain comparison (Case 10&10).



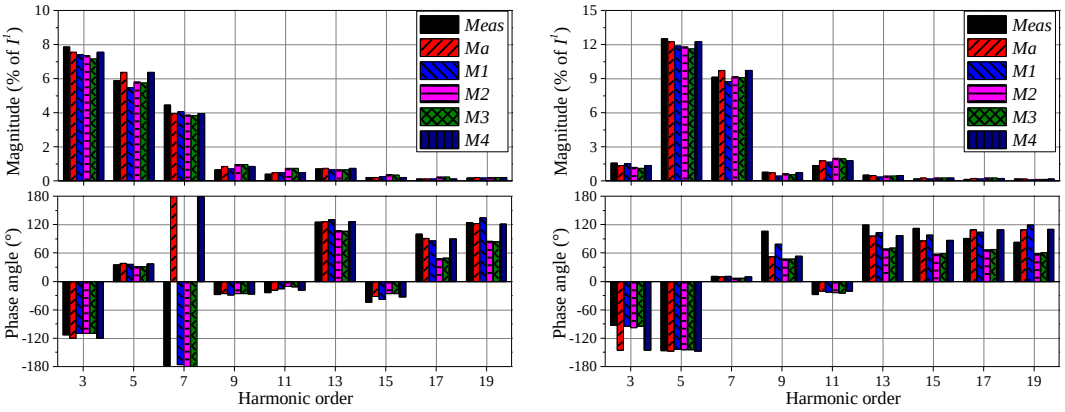

a) WF2 b) WF3

**Figure 6.45:** Frequency-domain comparison (Case 10&50).




a) WF2 b) WF3

**Figure 6.46:** Frequency-domain comparison (Case 50&10).




a) WF2 b) WF3

**Figure 6.47:** Frequency-domain comparison (Case 50&50).

Based on the time- and frequency-domain comparison results, the main conclusions with respect to the considered case of two parallel-connected PVIs, are:

- Summing-up of HAM elements of individual HFMs seems to be an appropriate way to derive aggregate HFM from individual HFMs, but achieved accuracy of the aggregate HFM depends on how accurate are individual HFMs;

- Measurement-based aggregate HFM, obtained in direct measurements of two parallel-connected PVIs (denoted as "Ma" values), are the most accurate;

- Measurement-based aggregate HFMs, obtained by summing-up HAM elements of two individual PVIs (denoted as "M1" values), require to perform full HFM measurements and obtain individual HFMs for exact (or close) operating powers of two PVIs, as otherwise significant errors might be introduced. This is demonstrated by the errors introduced when $HFM_{Agg\_M4}$(50&50) (denoted as "M4") is used to model parallel-connected PVI-A and PVI-B operating at 10% of their rated powers (Case 10&10);

Two modification-based aggregate HFMs (denoted as "M2" and "M3") provide a very good accuracy with much reduced number of required measurements for deriving individual power-dependent HFMs and, therefore, provide additional benefits for simple and accurate modelling of a large number of parallel-connected PVIs, as they essentially require only information about their operating powers.

## 6.6 Chapter conclusions

This chapter first investigates the general circuit topologies of residential-scale PVIs, with the functions of the main circuit parts and corresponding control algorithms discussed based on simulation. It turns out that the harmonic emission characteristics of PVIs are closely related to applied circuits, which are referring to the internal factors in the thesis. In addition, the laboratory testing results of three PVIs in Section 6.3 indicate that the harmonic characteristics are also affected by the operating powers (determined by the solar radiations) and supply conditions, which are referring to external factors. By fully taking into account both the internal factors and external factors, both CBMs and FDMs are developed for selected PVIs, with the model accuracy validated with measurements. In addition, modified frequency-domain modelling approaches are proposed, which can significantly reduce the number of tests required as the input for the FDM with competitive accuracy as opposed to the

measurement-based FDM. The proposed approaches will facilitate the practical implementation of FDMs.

As PVIs have sophisticated circuits which are quite diversified among different manufacturers, it is infeasible to develop the time-domain aggregation model for PVIs. Instead, the frequency-domain aggregation approach should be applied as they have generalised model form which is irrespective the actual circuit topology of the modelled device. The frequency-domain aggregation approach is fully discussed in last part of this chapter, and is demonstrated on two of the tested PVIs. It turns out that the proposed aggregation approach can indeed accurately represent the harmonic interactions among different PVIs.

# Chapter 7

# Evaluation of hybrid harmonic modelling techniques

## 7.1 Introduction

Currently, the majority of the grid-connected PE devices have only simple circuit topologies without PFC or with only p-PFC, and their CBMs can be easily developed with a good representation of their harmonic emission characteristics. However, it can be expected that increasing numbers of modern PE devices (like EVBCs and PVIs) will be connected to the grid. Considering the fact that most of modern PE devices are based on switched-mode converters or inverters having sophisticated controls, the difficulty of developing CBMs for them significantly increase, and FDMs are more preferred for them as opposed to CBMs. Accordingly, depending on the circuit complexity and the harmonic emission characteristics of modelled, different harmonic modelling techniques may be applied to different types of PE devices, requiring hybrid harmonic modelling approach to be proposed for allowing the implementation of different harmonic model forms under the same simulation environment.

This chapter will first briefly review the typical harmonic modelling techniques for modern PE devices, with the comparison of their performance demonstrated on the EVBC modelling. After that, hybrid harmonic modelling approaches using time-domain simulation (TDS) and using frequency-domain simulation (FDS) are proposed and demonstrated on a simple network case study. As the hybrid harmonic modelling using FDS may have convergence problems on weak or poorly damped networks, it can be expected that hybrid harmonic modelling using TDS is more preferred on complex network studies with the co-simulation of multiple harmonic model forms. To further investigate the feasibility of hybrid harmonic modelling using TDS on evaluating the harmonic interactions among different types of PE devices, the network case study in Section 7.3 is extended by varying numbers of connected EVs and CFLs. The last part of this chapter further demonstrates the applicability of the hybrid harmonic modelling approach using TDS on the urban generic LV distribution network model with varying numbers of EVs and/or PVs connected.

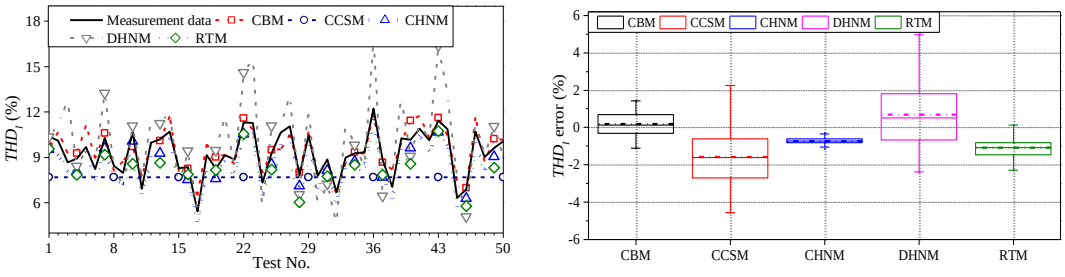
## 7.2 Typical harmonic modelling techniques

Typical harmonic modelling techniques can be divided into three different types which are a) time-domain models b) frequency-domain models and c) other analytical or mathematical models. The former two has been discussed in Chapter 2 while the "other models" refer to harmonic source models excluding CBM and FDM. These modelling techniques are quite diversified and are not as widely used for representing the current harmonic emission of modern PE devices as CBM and FDM. For example, an EVBC model based on PID controller is proposed in [184], while the regression tree model (RTM) given by (7.2) is developed and validated with the measurement data in [185].

$$v(t) = f(v(t-1), \cdots, v(t-n_v), i(t-1), \cdots, i(t-n_i)) \qquad (7.1)$$

where: $v(t)$ and $i(t)$ are the sampled input voltage and current waveforms respectively, while $n_v$ and $n_i$ are the maximum voltage and current lags respectively; $f(.)$ is nonlinear function, which is obtained by using tree partitioning for RTM [185].

For comparing the accuracy of the main harmonic source modelling techniques, CBM, RTM, CCSM, CHNM and DHNM were developed for one tested EVBC which is a 3.2 kW, single-phase, Level 2, on-board charger from an EV available on the EU market. In tests, the EVBC was operating at CC charging mode, supplied with 50 pre-set voltage waveforms with different harmonic spectrum. A comparison of the $THD_I$ values between measured and simulated input current with different modelling techniques is illustrated in Figure 7.1(a), and a box plot is given in Figure 7.1(b) to show the variation of $THD_I$ difference. The box plot is defined by 25$^{th}$ and 75$^{th}$ percentiles, while the solid and dash-dot lines inside the box represent 50$^{th}$ percentile and mean value respectively, with the upper and lower whiskers represent the 95$^{th}$ percentile and 5$^{th}$ percentile respectively.




a) measured and simulated $THD_I$ values b) whisker-box plot for $THD_I$ errors

**Figure 7.1:** Comparison of different modelling techniques applied to a tested EVBC.

It is observed from Figure 7.1 that CBM and CHNM achieve better accuracy than the other methods, implying that they should be given priority when choosing appropriate harmonic modelling techniques for the tested EVBC. In terms of the other three models, CCSM returns a constant $THD_I$ value while DHNM introduces a big variation of errors because of neglecting the interaction between voltage and current harmonics of different orders. Although RTM has relatively low $THD_I$ error when applied to the tested EVBC, it is a less conventional model for the integration in network analysis environments.

## 7.3 Hybrid harmonic modelling approaches

Typical network harmonic analysis techniques include: a) direct current injection (or frequency scan), b) harmonic power flow, c) iterative harmonic analysis (IHA), and d) time domain simulation (TDS) [8]. The first three approaches perform network harmonic analysis in the frequency domain with the last one in the time domain simulation. Based on the technique selected, compatible harmonic models should be applied. Among the four approaches, only IHA and TDS allow different forms of harmonic models of the loads and network components to be implemented in a hybrid modelling environment [186]. As the harmonic model form should be selected according to the harmonic emission characteristics of modelled equipment and using the same harmonic model form for all the devices connected to the network is not an appropriate solution, implementation of the hybrid modelling approach is very important for investigating the harmonic interaction among different types of PE devices connected to the same network, and is expected to increase the accuracy and confidence of the obtained network harmonic analysis results. Therefore, this section will focus on discussing the implementation approach for IHA and TDS, with different forms of harmonic models applied.

### 7.3.1 Network case study

As shown in Figure 7.2, a simple test network is applied to demonstrate the implementation approach and compare the difference between IHA and TDS. The network consists of a LV source, $V_{BG}$, modelled as a "flat-top" distorted supply voltage waveform, representing the typical "background" distortion in residential LV grids, a source impedance $Z_{sys}$ of (0.4+j0.25) Ω, representing the maximum expected source

impedance of phase and neutral conductors in LV networks (at 90 % LV supply points [92]) and a point of common coupling (PCC) where all harmonic models are connected. Here, three different types of harmonic loads are connected, which are 10 households (HHs), two EV chargers of the same type (as introduced in Section 7.2) and 50 different CFLs. HHs, EVs and CFLs are modelled by CCSM, CHNM and HCBM respectively.

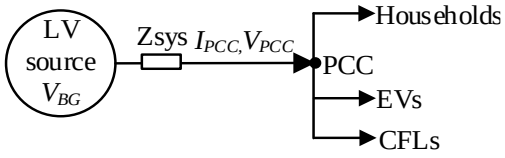



**Figure 7.2:** A simple test network used for the analysis.

The development of CHNM for EVBC is presented in Chapter 5, while the CBM for CFL is illustrated in Figure 7.3, with more details on its development given in [2]. The sample population of 50 CFLs is generated by probabilistic variation of the parameter values of the generic CFL CBM, presented in Table 7.1, with the rated power ranging between 5-25 W, representing the typical residential CFLs. The aggregate current harmonics of 10 HHs are obtained from the measurements in a LV distribution network, with the spectrum shown in Figure 7.4. The fundamental current component is 17.52 A∠0.18° and is not shown in the figure.

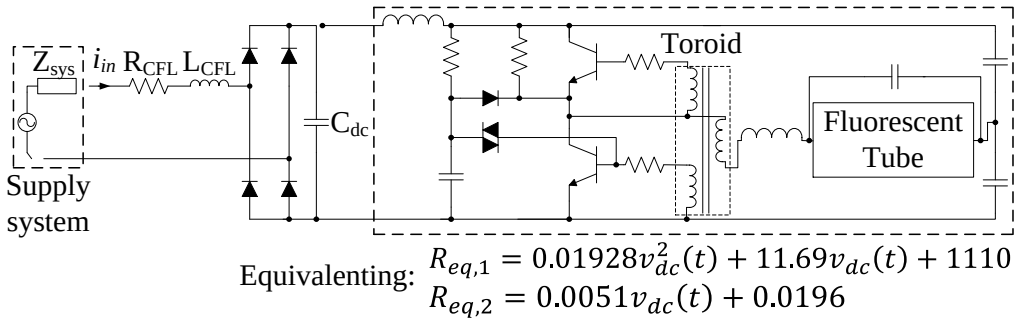



**Figure 7.3:** CBM of CFL with self-oscillating ballast (the circuit after the dc-link capacitor is replaced by varying equivalent resistance for the charging and discharging states) [2].

**Table 7.1:** CBM generic CFL model parameter values [2].

| Model Parameter | Generic value (p.u.) | Distribution of values | Range of values (p.u.) |
|---|---|---|---|
| $R_{CFL, pu}$ | 2.16 x 10-3 | Uniform | [1.95x10-3, 2.38x10-3] |
| $X_{Cdc, pu}$ | 0.25 | Normal | $\mu = 0.25$, $\sigma = 2.98$ |
| $P_{CFT}$ | 1 | Uniform | [0.8, 1.02] |
| $X_{LCFL, pu}$ | 3.92 x 10-5 | Constant | / |
| Note: All values are in per-unit of CFL rated power and voltage. $R_{CFL}$ and $X_{LCFL}$ represent the input resistance and inductance respectively, $X_{Cdc}$ and $P_{CFT}$ represent the dc side capacitance and tube rated power. | | | |

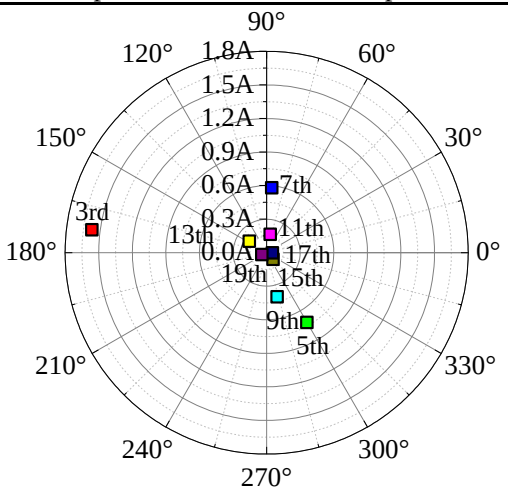



**Figure 7.4:** Current harmonics of 10 HHs measured in LV distribution network.

### 7.3.2 The application of FDM and CBM in frequency-domain simulation

With reference to Figure 7.2, the application of different types of the models (CHNM, CCSM and CBM) in a frequency-domain simulation using IHA is implemented as a hybrid modelling environment using the following steps [21]:

1. Initialise a 1 p.u. ideally sinusoidal supply voltage at $V_{PCC}$ to all connected HCBMs, CHNMs and CCSMs, and the supply voltage is specified in frequency domain for HNM and CCSM and in time domain for CBM.

2. Extract one-cycle inputs voltage and current waveforms from the steady-state simulation results of CBM, and apply fast/discrete Fourier transform (FFT/DFT) to obtain corresponding voltage and current harmonics.

3. Sum complex current harmonics from all models connected to the PCC to obtain $I_{PCC}$.

4. Calculate the harmonic voltage drop across the harmonic source impedance of the same order to update $V_{PCC}$ by subtracting harmonic voltage drop from the $V_{BG}$ in the frequency domain.

5. Apply new value of $V_{PCC}$ in Step 2 and repeat Steps 2-5 until no obvious variations are observed for the *THD* of $V_{PCC}$ or $I_{PCC}$, in accordance to the selected convergence criterion, i.e. the maximum difference of *THD* of $V_{PCC}$ between two successive iterations is below the set threshold value (0.3% in the presented simulation results).

### 7.3.3 The application of FDM and CBM in time-domain Simulation

In order to incorporate CHNM and CCSM in a time-domain simulation, time-domain input voltage waveform has to be processed by FFT to obtain complex voltage harmonics as inputs for CHNM and CCSM, with complex current harmonics as outputs. The current harmonics will be represented as a series of parallel connected voltage-controlled current sources in the time-domain simulator. With reference to Figure 7.2, the following steps are used to implement the hybrid modelling environment in a time-domain simulator [21]:

1. Initialise controllable current sources for representing CHNM and CCSM to their predefined values (e.g. the current harmonic emission under ideal supply condition) and run the time-domain simulation until the first full-cycle waveform of $V_{PCC}$ is available for performing FFT.

2. Apply FFT to the voltage waveform at PCC, and the obtained complex voltage harmonics will be used as inputs to CHNM and CCSM.

3. Calculate current harmonics from CHNM and CCSM.

4. Complex current harmonics obtained from Step 3 are represented as voltage-controlled current sources in the time-domain simulator.

5. Obtain the new one-cycle time-domain voltage waveform at PCC in the next time-step of simulations (sliding one-cycle window) and apply it to Step 2.

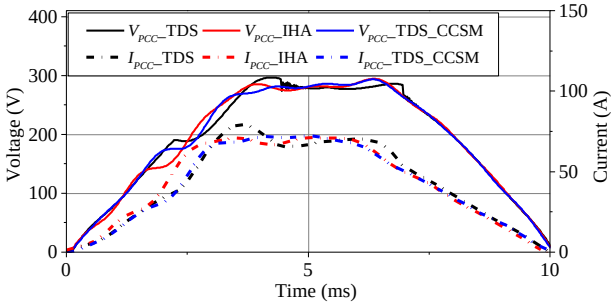
In this case, the convergence criterion of reaching steady-state operating conditions in the time-domain simulator is equivalent to the specification in the frequency-domain simulator.

### 7.3.4 Comparison of the hybrid modelling approaches

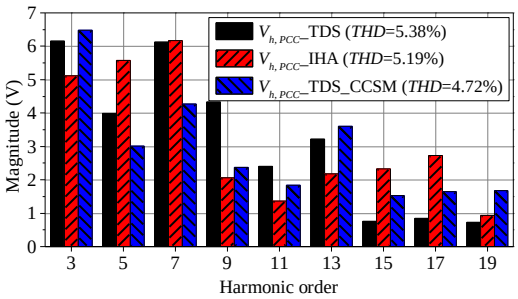
The comparison of the test network simulation results between the two hybrid modelling approaches (using IHA and TDS) is illustrated in Figure 7.5. Considering the fact that the CCSM is still the most widely used harmonic modelling technique for network harmonic analysis, the results when all CBMs and CHNMs are replaced by their corresponding CCSMs are used as the reference case shown in Figure 7.5 [21].

It is observed from Figure 7.5 that $THD_I$ at PCC has higher value by using TDS and has lower value by using IHA with respect to the reference case. This phenomenon is mainly due to the existence of highly nonlinear CFL loads which are characterized by a pulse-like current waveform and is clearly visible in the increasing part of a half-cycle current waveform in Figure 7.5(a) [21]. When the 50 CFLs start to conduct, an apparent distortion of the supply voltage waveform at PCC is noticed, and is captured differently for TDS and IHA. Specifically, IHA cannot respond to the fast changes in the current waveform, which are inherently maintained in the solver of the partial differential equations which characterize the time-domain analysis. The result is a noticeable shift in the conduction period of supply current waveform and hence the voltage waveform distortion at PCC, which will affect the harmonic emission characteristics of EVBCs connected to PCC [21].

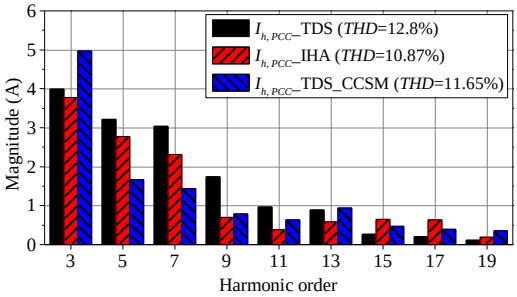
One issue related to the IHA approach is the existence of convergence problem when the test network is weak or poorly damped, or when resonances occur, which can be solved by applying the reactance compensation (e.g. [187]). There is no such issue when using TDS, implying that TDS would be preferred for hybrid modelling approach where both FDM and CBM are connected. Finally, both IHA and TDS are able to take into account the supply voltage dependency of the harmonic emission characteristics of PE devices, making them more suitable for different types of network harmonic analysis as opposed to the conventional approach (i.e. representing nonlinear devices with constant harmonic current sources).




a) half-cycle voltage and current waveforms at PCC




b) comparison of voltage harmonics at PCC




c) comparison of current harmonics at PCC

**Figure 7.5:** Comparison of the results for the application of two hybrid modelling approaches (using IHA and TDS) and CCSM in TDS.

## 7.4 Hybrid modelling using TDS: analysis of harmonic interactions between EVs and CFLs

In this section, the feasibility of implementing FDM for EVBC and CBM for CFLs in a hybrid modelling approach based on TDS is further illustrated on the same test network shown in Figure 7.2, with varying numbers of EVBCs and CFLs connected to PCC. Specifically, the number of CFLs connected to the PCC was varied from 0 to 50 (increase by 5 for every simulation), while the number of connected EVBCs was varied from 0 to 5 (increase by 1 for every simulation), with the source impedance adjusted between zero (ZS1) and the maximum expected value specified in [92] (ZS2).

The network study results are represented by the *THD* values of $I_{PCC}$ and $V_{PCC}$ shown in Figure 7.6, as wells as the 3rd, 5th, 7th and 9th individual current harmonics at PCC given in Figure 7.7.

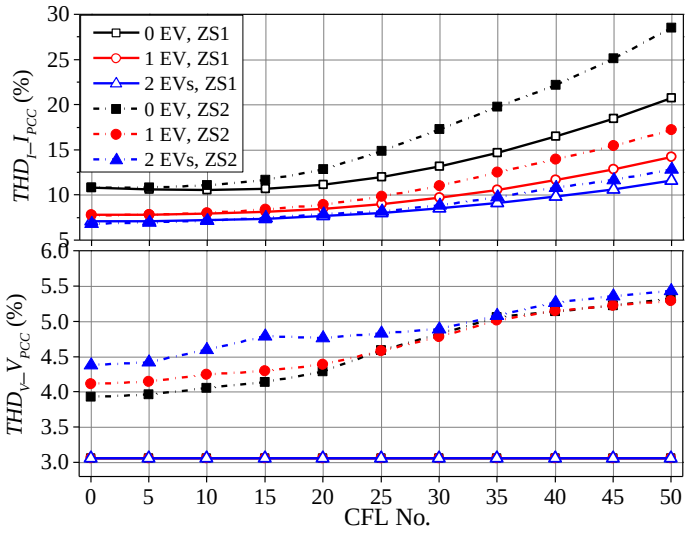
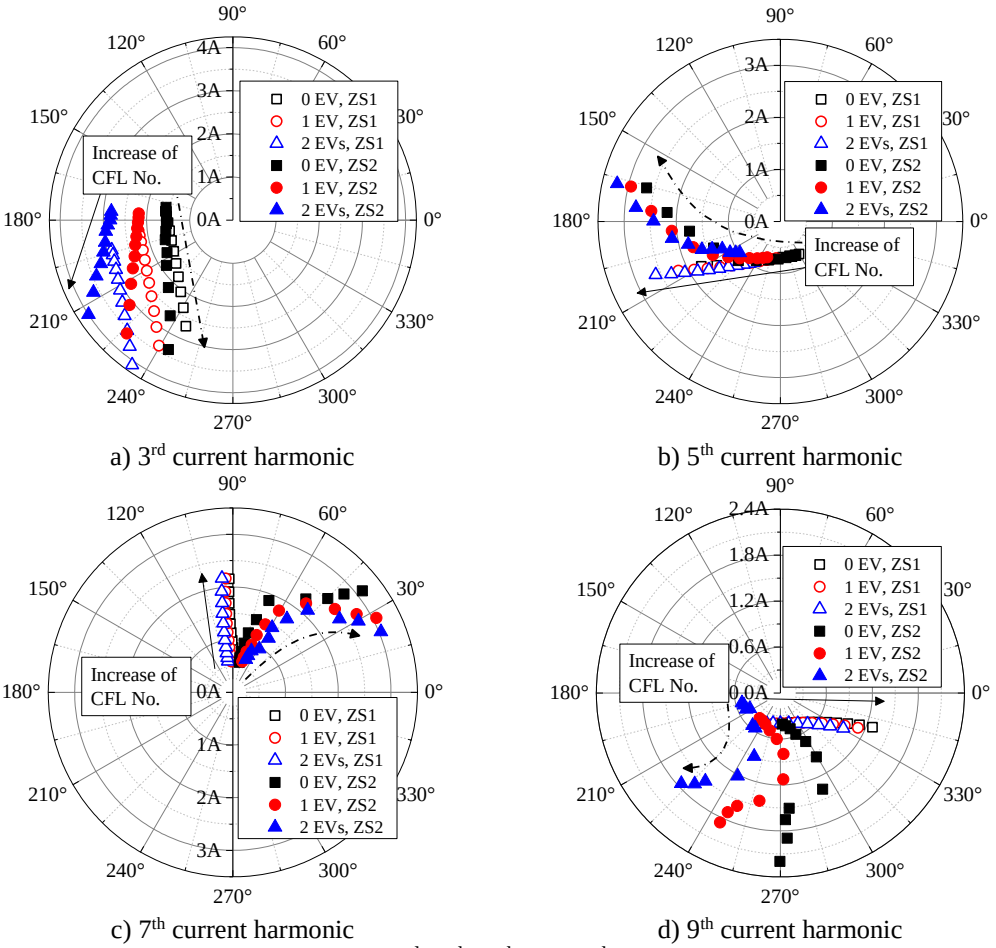



**Figure 7.6:** The *THD* values for $I_{PCC}$ and $V_{PCC}$.




a) 3rd current harmonic

b) 5th current harmonic

c) 7th current harmonic

d) 9th current harmonic

**Figure 7.7:** The distribution of 3rd, 5th, 7th and 9th current harmonics at PCC under different loading and supply conditions.

As shown in Figure 7.6, the $THD_v\_V_{PCC}$ is independent of the number of EVBCs and CFLs connected, which is because the interaction between loads and the grid relies on the source impedance. Under both ZS1 and ZS2, the increasing number of connected CFLs will result in the deterioration of the current waveform distortion at PCC, and distortion is more severe under ZS2. The increasing number of connected EVBCs could alleviate the current waveform distortion at PCC, which is due to the harmonic cancellation between EVBCs and CFLs. For the voltage waveform distortion at PCC with ZS2, it increases mildly with the increasing number of CFL and EVBCs. After the source impedance value changes from ZS1 to ZS2, the voltage and current waveform distortion at PCC both increase.

With respect to the 3rd, 5th, 7th and 9th current harmonics of $I_{PCC}$ shown in Figure 7.7, the increase of connected CFL number will result in higher magnitudes of all considered harmonics, while the increasing number of EVBCs will lead to an increased magnitude of the 3rd magnitude with negligible impacts on the 5th, 7th and 9th harmonic magnitudes. Additionally, the increased number of connected EVBCs results in a anticlockwise phase angle shift of the 5th current harmonic and a clockwise phase angle shift for the 3rd, 7th and 9th current harmonics.

In terms of the impacts of ZS2 on the considered individual current harmonics at PCC, ZS2 has very little impacts on the 3rd and 5th harmonic magnitude, but will apparently increases the magnitudes of 7th and 9th current harmonics especially when CFLs are connected in large numbers. Moreover, ZS2 leads to a stronger clockwise phase angle shift of all the considered individual harmonics. This case study gives an example of applying the hybrid harmonic modelling approach to investigate the changes of harmonic emission with varying numbers and types of the connected PE devices, which is very important for predicting the harmonic emission impacts of the further highly diversified PE devices on power network, as well as helping the planning and operational strategies for the anticipated changes in the structure and characteristics of the connected PE devices.

## 7.5 Case study: impact of EVs and PVs on the urban generic LV distribution network

In this section, the hybrid harmonic modelling using TDS is applied to the urban generic LV distribution network for investigating the impact of different deployment scales of EVs and PVs on the supply voltage and current distortion as well as the distribution transformer operation.

### 7.5.1 Case study details

The LV network model provided in Figure 7.8 corresponds to the UK urban generic LV distribution network with an 11/0.4 kV delta-wye transformer having a power rating of 500 kVA. The loads connected to the network are represented by 19 house clusters (H1 to H19) with 190 single-phase residential households, as shown in Figure 7.8. The detailed information on the network model and the household phase connection is provided in Appendix B. To evaluate the harmonic impact of EV home charging and residential-scale PVs on the LV network, four different deployment scales are assumed and are represented by "Case A" to "Case D" in Figure 7.8, with the house clusters having EVs and/or PVs connected, marked by green arrows. Specifically, Case A has EVs and/or PVs connected at H15 only while Case B has EVs and/or PVs connected at H13 and H15. The house clusters selected for the connection of EVs and/or PVs for Case C is H1, H13, H15 and H18 while it is H1, H2, H8, H10, H13, H15, H16 and H18 for Case D. For each case, three different scenarios are considered: 1) only EVs are connected; 2) only PVs are connected; and 3) both EVs and PVs are connected. For Case A to Case C, it is assumed that each house of the selected house clusters have one EV and/or PV connected at the same phase while for Case D, two of the houses on each phase of the selected house clusters, are equipped with EVs and/or PVs (with each house having one EV and/or PV).

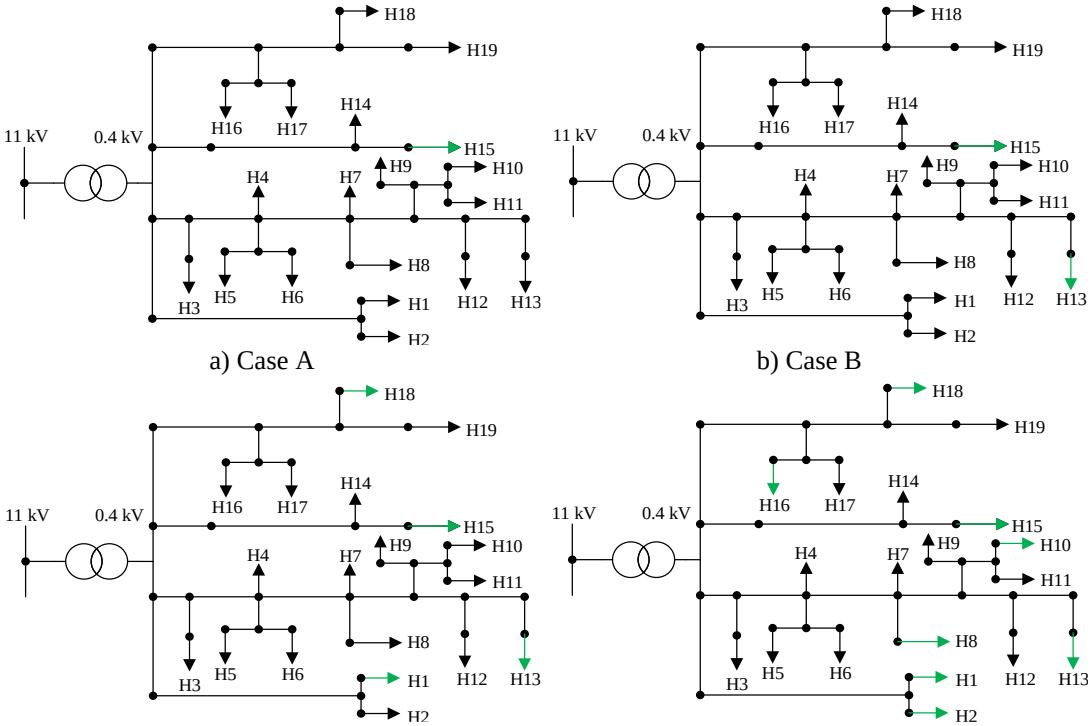



**Figure 7.8:** Four different deployment cases for EVs and/or PVs connected to the urban generic LV distribution network.

The current harmonic emission of individual household is represented by constant current source model, with the fundamental current harmonic, 3rd, 5th and 7th current harmonics assumed to be 4.35 A∠0°, 0.435 A∠-160°, 0.305 A∠-45°and 0.131 A∠30° respectively (corresponds to 10%, 7% and 3% $I_1$ for 3rd, 5th and 7th current harmonics respectively) with respect to the zero phase angle of supply voltage. The values for 3rd and 5th current harmonic are defined according to the household current harmonic emission survey in [188], while the value for 7th current harmonic is randomly selected. As the 3rd, 5th and 7th current harmonics are the dominant harmonic orders for a typical household, the other current harmonic orders are not considered here. In addition, the power consumption of individual household is 1 kW under ideal supply condition, with the total power consumption for the 190 houses equal to 190 kW. The network study results without the connection of EVs and PVIs are used as the reference case.

The current harmonic of individual EV is represented by the CHNM developed in Chapter 5 for EV under single phase home charging (belongs to Level 2 charging) with CC charging mode. In terms of the current emission of residential-scale (rooftop) PVIs, it is represented by the (measurement based) HFM developed for PVI-A in Chapter 6.

As the power consumption for EV under CC charging mode is almost constant, it can be regarded as the power-independent load. However, for PV whose power consumption changes significantly with the varying solar radiation on the PV panels, it is necessary to take into account the impact of operating power on the current harmonic emission. Accordingly, for the scenario of only PVs connected and the scenario of both EVs and PVs connected, the operating power of PVs is adjusted at three different power levels which are 10% $P_{rated}$, 50% $P_{rated}$ and $P_{rated}$. As the main purpose of the case study is to demonstrate the applicability of the hybrid harmonic modelling using TDS for complex network with different forms of harmonic models for modern PE devices connected, it is assumed that all the individual houses, EVs and PVs at different connection points are exactly the same (i.e. same type with the same operating power or mode). In addition, when multiple devices are connected to the same terminal point, aggregate FDM obtained from the arithmetic summing-up of individual FDMs is applied (as demonstrated in Chapter 6). The discussion of network study results for each case will be given in the next section.

### 7.5.2 Case study results

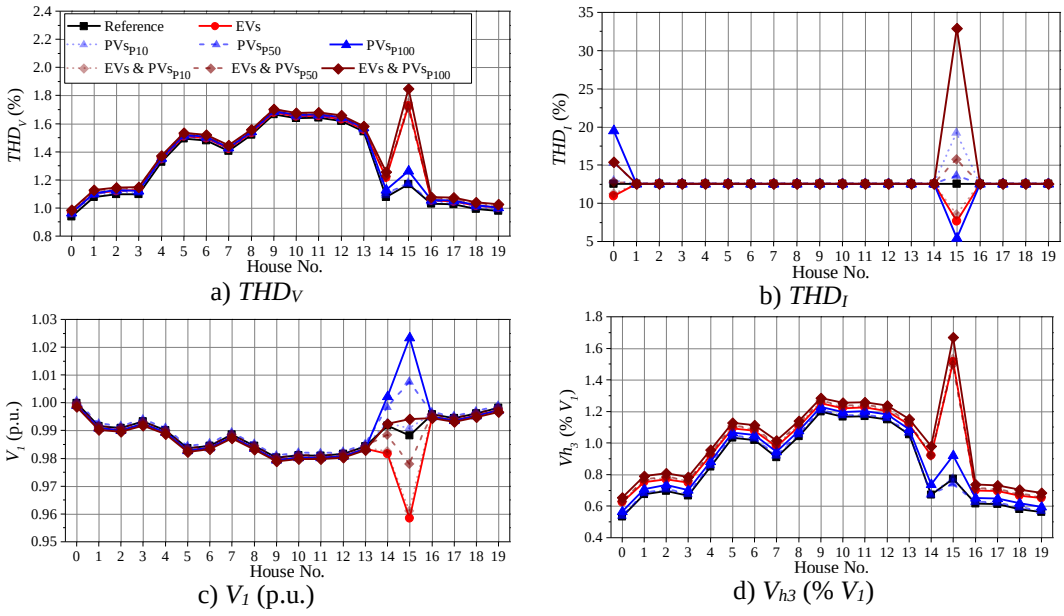
In this section, the network study results will be discussed individually for each case. As the network is well three-phase balanced for the reference case (the maximum voltage unbalance factor, *VUF*, for the 19 house clusters is 0.05%), and the EVs and PVs are evenly distributed on each phase of the selected house clusters, only the simulation results of phase A will be analysed. In addition, as the FDMs developed for EVs and PVs only consider the harmonic orders up to 20, only 2$^{nd}$ to 20$^{th}$ order harmonics are taken into account in the $THD_V$ and $THD_I$ calculations.

**Case A: EVs and/or PVs connected to H15 only**

Figure 7.9 illustrates the $THD_V$, $THD_I$, $V_1$, $V_3$, $V_5$ and $V_7$ of H1-H19 and the LV side (marked as "H0" in the figures) of the distribution transformer under different scenarios of EV and/or PV connections, with the values under the reference case (i.e. only houses) marked by the black lines. It is noticed that the connection of EVs, or both EVs and PVs at H15 only aggravate the supply voltage distortion locally, with very little impacts on the other house clusters, while the connection of PVs only slightly increase the $THD_V$ at H15 for PVs operating at $P_{rated}$. That is because the

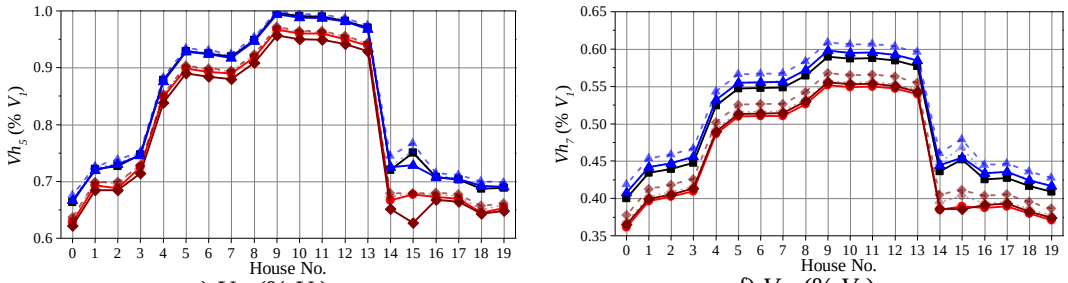
connection of EVs, or both EVs and PVs apparently increase the 3rd harmonic content of the supply voltage (almost three times the reference case), even though the 5th and 7th voltage harmonic contents slightly decrease with respect to the reference case. When only PVs are connected to H15, $V_1$ at H15 is above 1 p.u. when the operating power of PVs is above 50% $P_{rated}$, implying a power injection into the grid. The increase of $V_1$ at H15 not only slightly improves the voltage level of nearby house cluster H14, but also alleviates the supply voltage distortion of H15, making the $THD_V$ value close to the reference case.

In terms of the supply current distortion at H15 shown in Figure 7.10, lower $THD_I$ value is achieved for the scenarios of only EV connection, only PV (at 100% $P_{rated}$) connection, and both EV and PV (at 10% $P_{rated}$) connection. That is because for all the three scenarios, the supply current is dominated by the ac current of either EVs or PVs which are less distorted as opposed to the current waveform of the houses, illustrated in Figure 7.10(a) and Figure 7.10(c). On the other hand, when both EVs and PVs (at 100% $P_{rated}$) are connected at H15, the total power consumption of houses and EV charging is almost equal to the power supplied by the PVs, resulting in a very low value of the fundamental component of the supply current and hence high waveform distortion, as illustrated in Figure 7.10(b) and Figure 7.10(d). Similarly, the partial power consumption of houses supplied by PVs operating at 10% $P_{rated}$ also slightly increases the supply current distortion (Figure 7.10(b)).



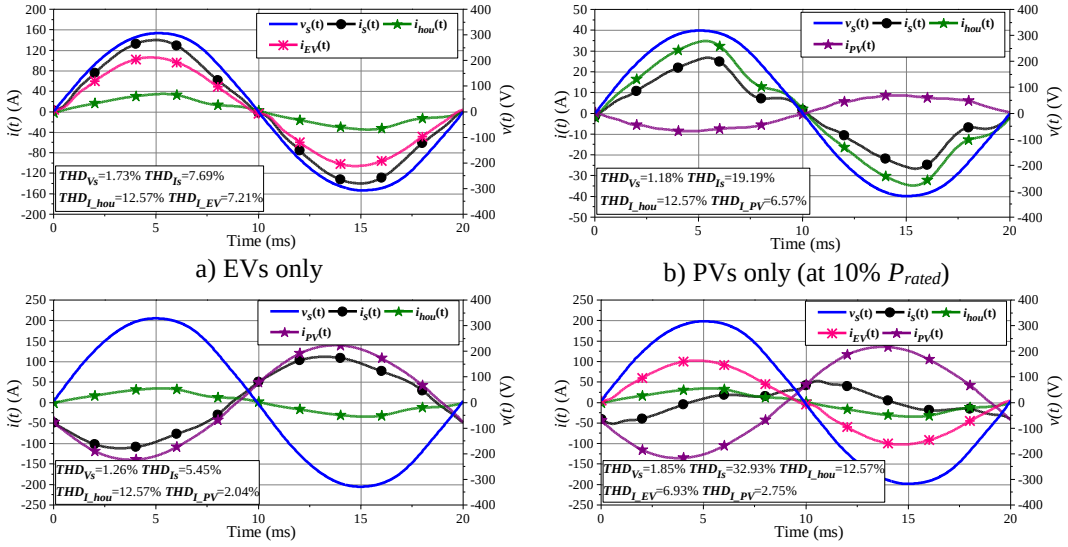

a) $THD_V$ b) $THD_I$

c) $V_1$ (p.u.) d) $V_{h3}$ (% $V_1$)




e) $V_{h5}$ (% $V_1$) f) $V_{h7}$ (% $V_1$)

**Figure 7.9:** The $THD_V$, $THD_I$, $V_1$, $V_3$, $V_5$ and $V_7$ at different house clusters for Case A with different EV and/or PV connection scenarios.




a) EVs only b) PVs only (at 10% $P_{rated}$)

c) PVs only (at 100% $P_{rated}$) d) EVs & PVs (at 100% $P_{rated}$)

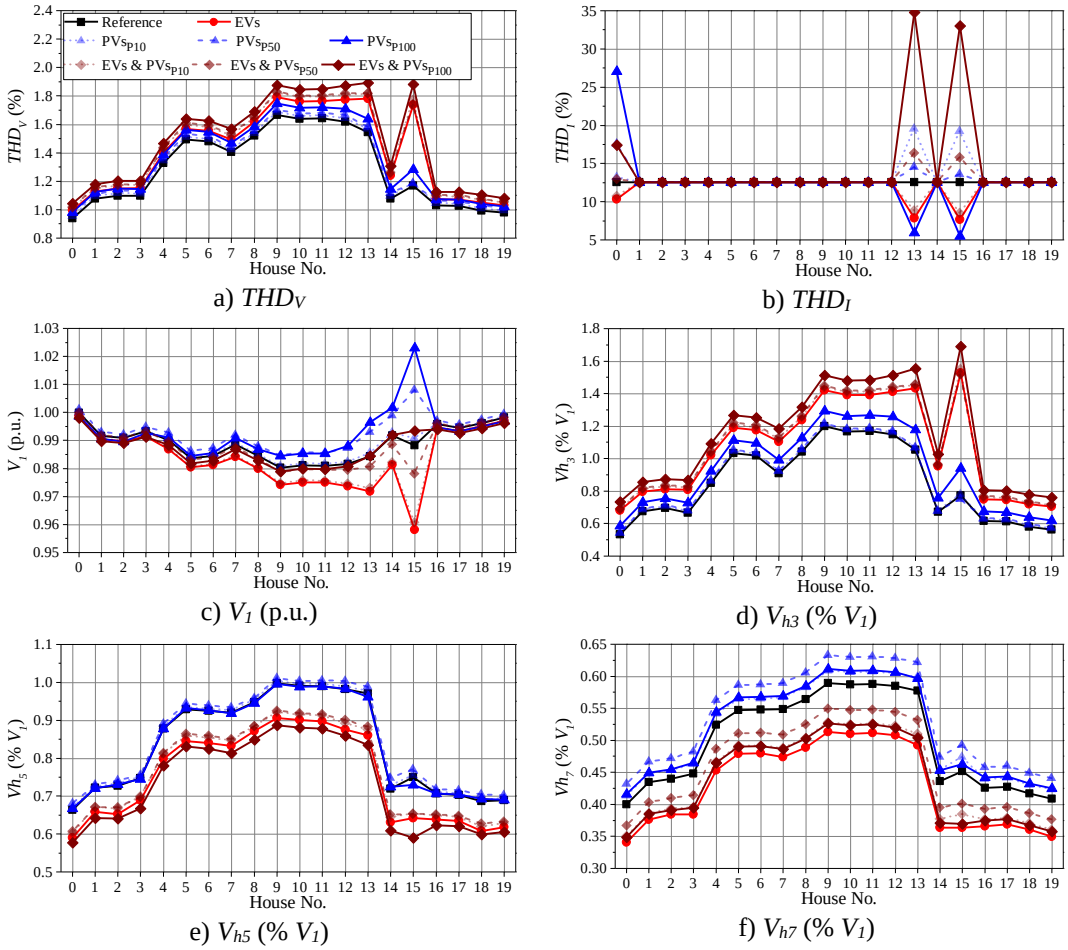
**Figure 7.10:** The simulated time-domain voltage and current waveforms at H15 for Case A with selected EV and/or PV connection scenarios.

**Case B: EVs and/or PVs connected to H13 and H15**

For Case B, EVs and/or PVs are connected to both H13 and H15. It is observed from Figure 7.11(a) that the supply voltage distortion at H13 and H15 is aggravated by the connection of only EVs, or both EVs and PVs. The $THD_V$ values at other house clusters without the connection of EVs and PVs also slightly increase, especially for H9-H12 which are close to H15. For $V_1$, $Vh_3$, $Vh_5$ and $Vh_7$ under different scenarios, their distribution patterns over different house clusters are similar with the corresponding curves in Case A.

As the supply voltage and current distortion at H15 are almost the same with Case A, only the time-domain supply voltage and current waveforms at H13 are shown in Figure 7.12. It turns out that the voltage and current waveform distortions at H13 of

Case B are similar with the waveform distortions at H15 of Case A, suggesting that the same analysis for Figure 7.10 also applies to Figure 7.12.

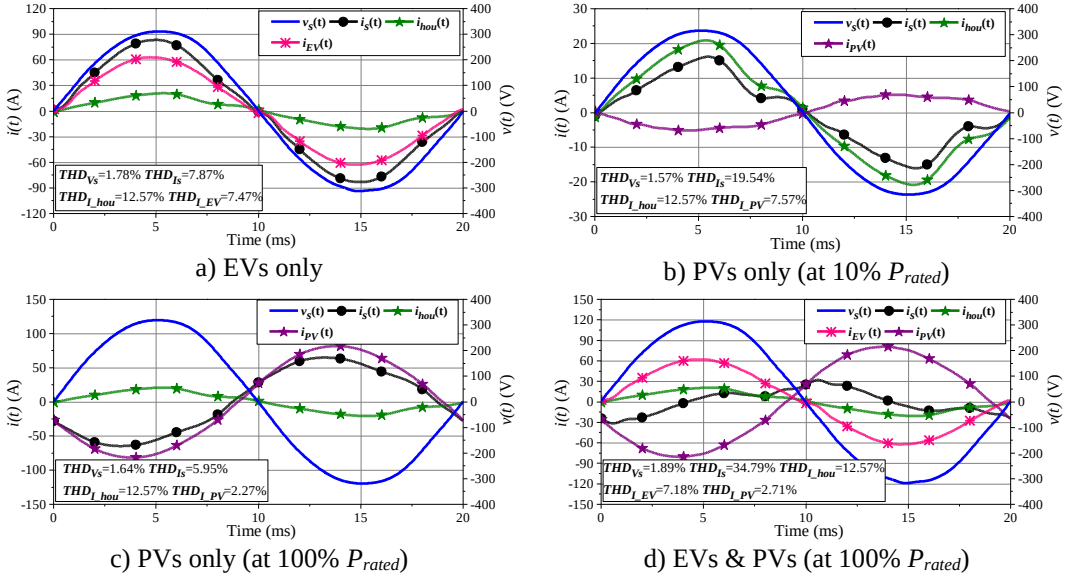



a) $THD_V$ b) $THD_I$

c) $V_1$ (p.u.) d) $V_{h3}$ (% $V_1$)

e) $V_{h5}$ (% $V_1$) f) $V_{h7}$ (% $V_1$)

**Figure 7.11:** The $THD_V$, $THD_I$, $V_1$, $V_3$, $V_5$ and $V_7$ at different house clusters for Case B with different EV and/or PV connection scenarios.




a) EVs only b) PVs only (at 10% $P_{rated}$)

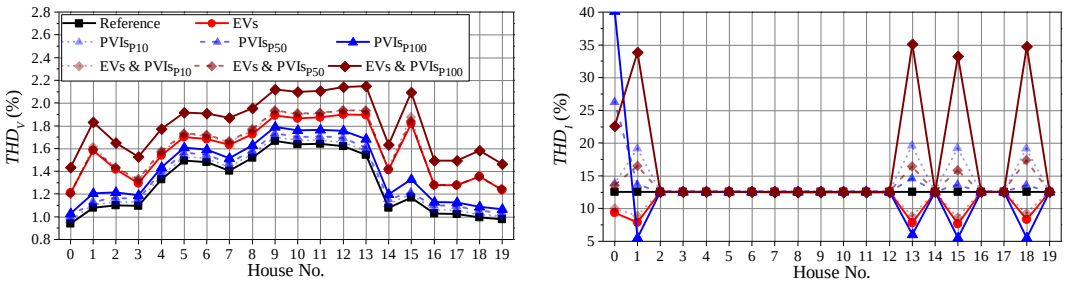
c) PVs only (at 100% $P_{rated}$) d) EVs & PVs (at 100% $P_{rated}$)

**Figure 7.12:** The simulated time-domain voltage and current waveforms at H13 for Case B with selected EV and/or PV connection scenarios.

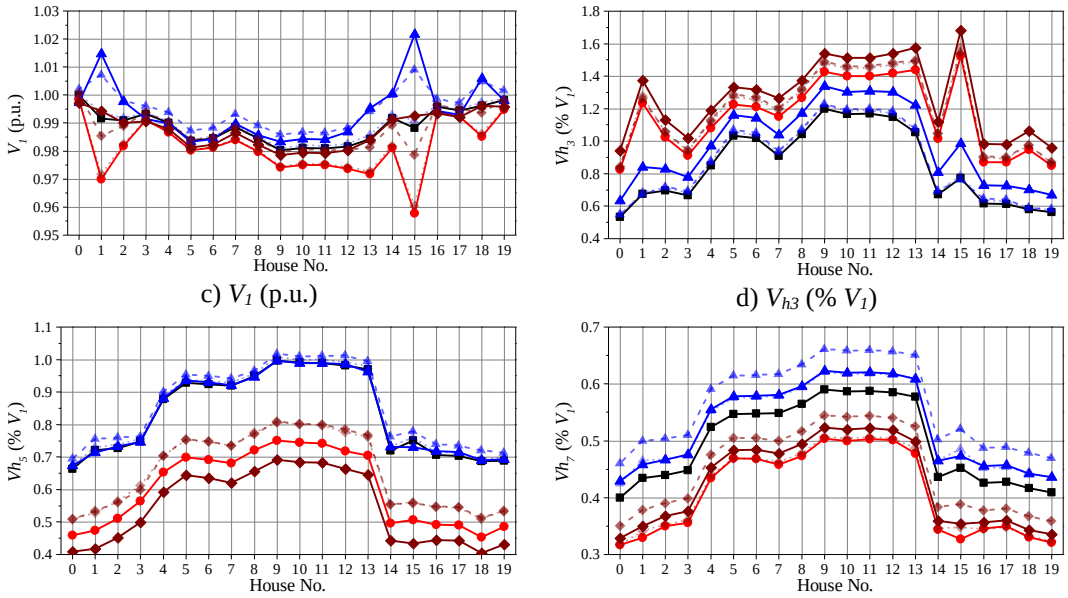
**Case C: EVs and/or PVs connected to H1, H13, H15 and H18**

As shown in Figure 7.13, when the connection points for EVs and/or PVs extend from H13, H15 to H1, H13, H15 and H18, the supply voltage distortion is further aggravated not only for the four house clusters, but also for all the other house clusters without EV and PV connection, especially for the scenarios of only EV connection, and both EV and PV connection. Regarding $V_1$, the connection of EVs decreases $V_1$ locally, and an opposite trend is observed for the connection of PVs. However, when both EVs and PVs (at 100% $P_{rated}$) are connected, $V_1$ at different house clusters is very close to $V_1$ for the reference case, implying that the power consumption required by the EV charging is mainly provided by the power generation from PVs. For the 3rd, 5th and 7th voltage harmonics, $Vh_3$ increases under all the scenarios, while the connection of EVs or both EVs and PVs contributes a reduction of $V_{h5}$ and $V_{h7}$. When only PVIs are connected, the $THD_V$ at all house clusters only slightly increases with the increase of operating powers of PVs, which is mainly attributed to the increase of $Vh_3$ and $Vh_7$.

For the supply current waveform distortion at house clusters with EV and/or PV connection, the same phenomenon for Case A and Case B is observed, as shown in Figure 7.14(b). In short, the connection of EVs or PVs (at 100% $P_{rated}$) or both EVs and PVs (at 10% $P_{rated}$) alleviates the supply current distortion with respect to the reference case, while the connection of both EVs and PVs (at 100% $P_{rated}$) apparently increases the supply current distortion, and the reason for that is given in the discussion of Case A. In terms of the current waveform distortion on the transformer secondary side, the connection of PVs only (at 50% or 100% $P_{rated}$) or the connection both EVs and PVs (at 100% $P_{rated}$) results in an obvious increase of $THD_I$ with respect to the reference case, as shown in Figure 7.14(b).



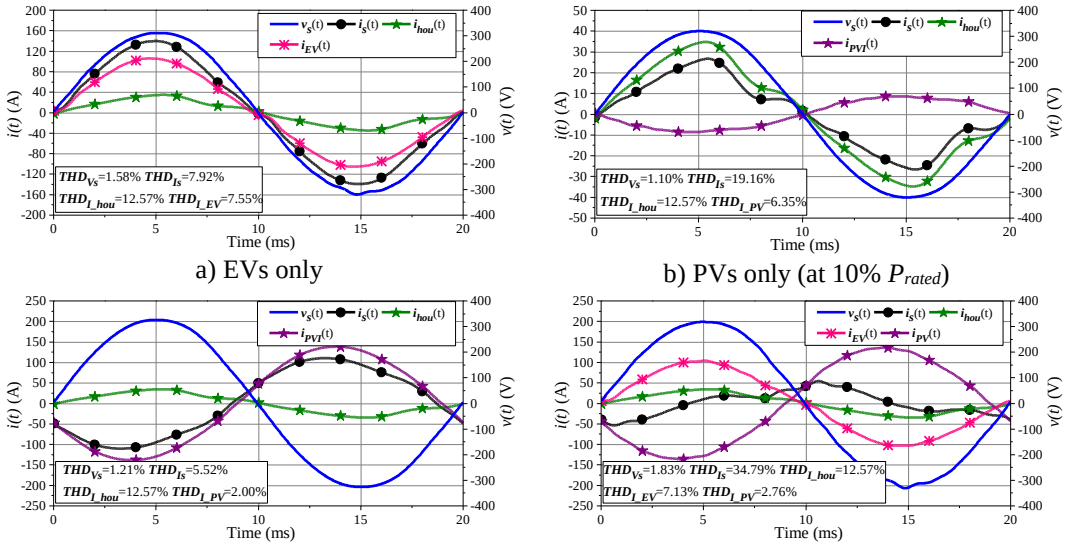

a) $THD_V$ b) $THD_I$




c) $V_1$ (p.u.) d) $V_{h3}$ (% $V_1$)

e) $V_{h5}$ (% $V_1$) f) $V_{h7}$ (% $V_1$)

**Figure 7.13:** The $THD_V$, $THD_I$, $V_1$, $V_3$, $V_5$ and $V_7$ at different house clusters for Case C with different EV and/or PV connection scenarios.




a) EVs only b) PVs only (at 10% $P_{rated}$)

c) PVs only (at 100% $P_{rated}$) d) EVs & PVs (at 100% $P_{rated}$)

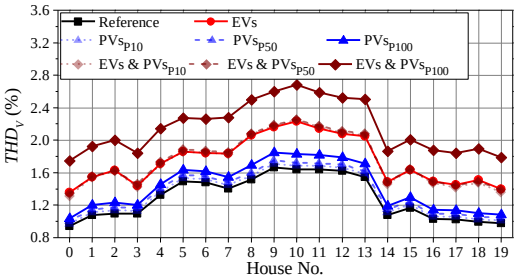
**Figure 7.14:** The simulated time-domain voltage and current waveforms at H1 for Case C with selected EV and/or PV connection scenarios.

**Case D: EVs and/or PVs connected to H1, H2, H8, H10, H13, H15, H16 and H18**

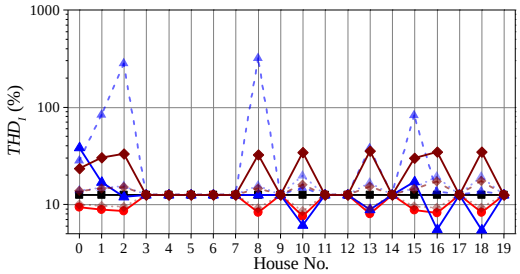
For Case D, EVs and/or PVs are connected to two of the houses on each phase of H1, H2, H8, H10, H13, H15 and H16 (each house has one EV and/or PV connected). Similar to Case C, the $THD_V$ values at all house clusters obviously increase when only EVs or both EVs and PVs are connected. For the impact of different scenarios on the fundamental voltage $V_1$, it is noticed from Figure 7.15(c) that the connection of EVs only will slightly decrease $V_1$ while the connection of PVs only (at 50% or 100% $P_{rated}$)

brings about an increase of $V_1$. It is also noticed that the connection of both EVs and PVs (at 100% $P_{rated}$) has negligible impacts on the $V_1$ at all house clusters, which is because the power demand of EV charging is locally supplied by the power generation from the PVIs. In terms of the 3rd, 5th and 7th low order voltage harmonics, their general trend under different scenarios is similar with Case C. Specifically, $V_{h3}$ increases under all scenarios (expect the connection of PVs only (at 10% $P_{rated}$)). For the $V_{h5}$, the connection of EVs only or both EVs and PVs can apparently reduce $V_{h5}$ while the connection of PVs only has the same $V_{h5}$ level with the reference case. With respect to $V_{h7}$, the connection of EVs only or both EVs and PVs result in a decrease of $V_{h7}$ while the connection of PVs increases $V_{h7}$, as shown in Figure 7.15(e).

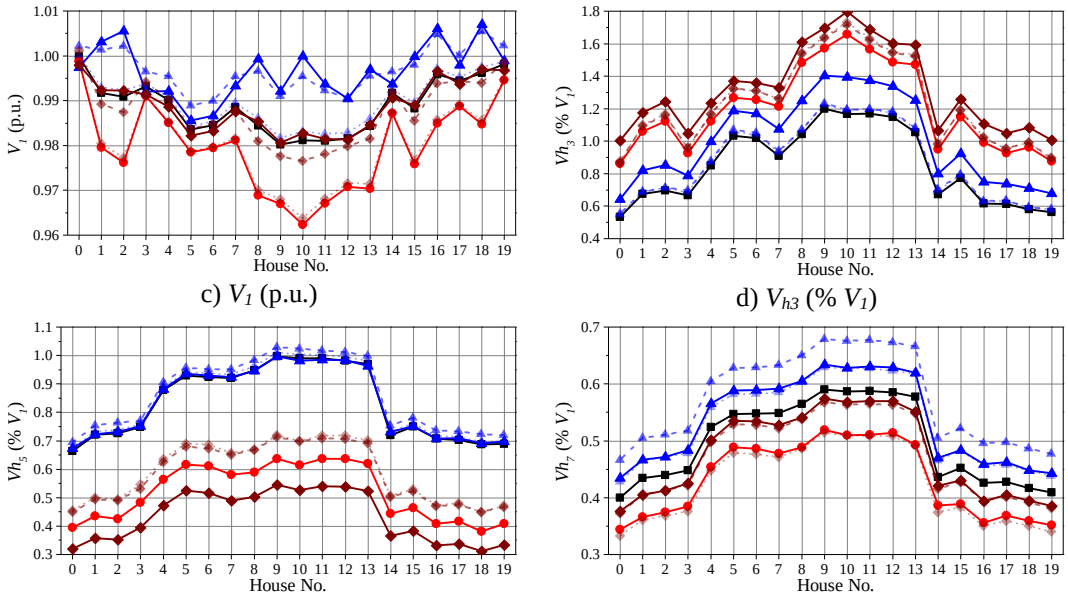
For the supply current distortion, it is noticed the connection of EVs only or the connection of PVs only (100% $P_{rated}$) tends to reduce the $THD_I$ (and hence the current waveform distortion) while the connection of PVs only (50% $P_{rated}$) or both EVs and PVs (100% $P_{rated}$) will increase the $THD_I$. This is because the connection of EVs only or PVs only (100% $P_{rated}$) apparently increases the fundamental current component and hence alleviate the current waveform distortion (compared with the reference case), as illustrated by the time-domain voltage and current waveforms in Figure 7.16(a) and 7.16(c). When only PVs (50% $P_{rated}$) are connected or both EVs and PVs (100% $P_{rated}$) are connected, the fundamental current component will be significantly reduced, resulting in the aggravation of supply current waveform distortion, as shown in Figure 7.16(b) and 7.16(c). In short, the apparent variation of fundamental current component plays a key role in supply current waveform distortion as opposed to the relatively small change of current harmonics.




a) $THD_V$



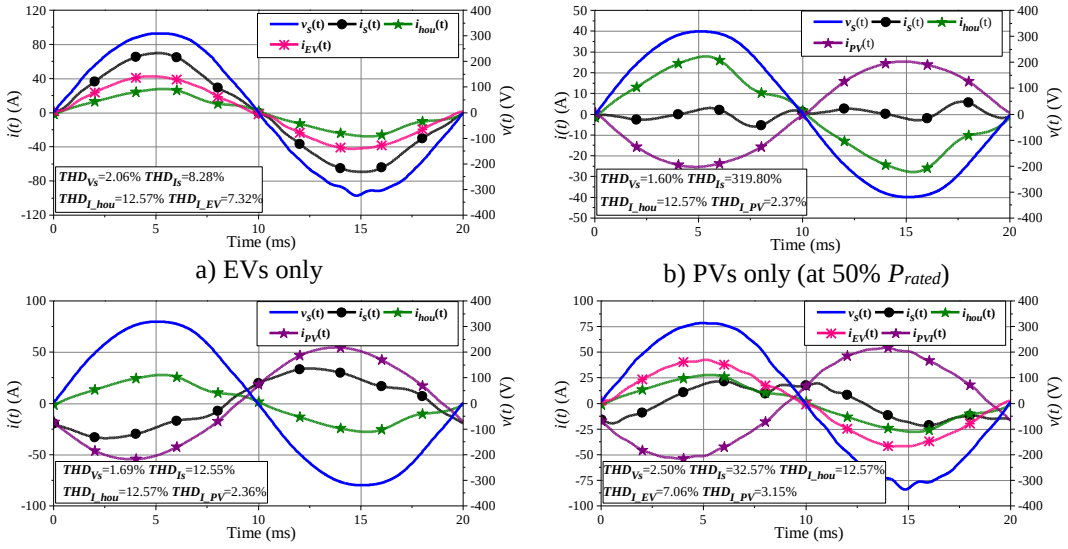

b) $THD_I$




c) $V_1$ (p.u.) d) $V_{h3}$ (% $V_1$)

e) $V_{h5}$ (% $V_1$) f) $V_{h7}$ (% $V_1$)

**Figure 7.15:** The $THD_V$, $THD_I$, $V_1$, $V_3$, $V_5$ and $V_7$ at different house clusters for Case D with different EV and/or PV connection scenarios.




a) EVs only b) PVs only (at 50% $P_{rated}$)

c) PVs only (at 100% $P_{rated}$) d) EVs & PVs (at 100% $P_{rated}$)

**Figure 7.16:** The simulated time-domain voltage and current waveforms at H8 for Case D with selected EV and/or PV connection scenarios.

**Impact of harmonics on the distribution transformer**

As distribution transformer is a key component of the LV network and its operation performance is closely related to the current harmonics circulating in its windings (as discussed in Chapter 2), the impact of EV and/or PV deployment for the four cases on the power losses, working temperature increase and the derating factor of the distribution transformer will be investigated. The basic information of the distribution transformer of the urban generic LV distribution network model are: 1) rated power is

500 kVA with delta-wye connection (oil-filled); 2) the nominal phase-to-phase voltage on the primary and secondary sides are 11 kV and 400 V respectively; 3) impedance lumped on the secondary side is (0.0102+0.0464j) p.u. (p.u. on transformer rating); 4) $P_{NL\text{-}R}$ and $P_{LL\text{-}R}$ are 680 W and 5100 W respectively; 5) $\theta_{TO\text{-}R}$, $\theta_{g\text{-}R}$ and $\theta_A$ are 65°C, 5°C and 35°C respectively. As the transformer is the same with the one discussed in Section 2.4 of Chapter 2 which provides the detailed calculation procedure of the main indices (including $F_{HL}$, $F_{HL\text{-}STR}$, $P_{LL}$, $P_{NL}$, $P_T$, $P_{DC}$, $P_{EC}$, $P_{OSL}$, $\theta_H$, $\theta_{TO}$, $\theta_g$, $I_{2\text{-}max}$, $F_{AA}$ and K-factor), the related indices calculation is not repeated here.

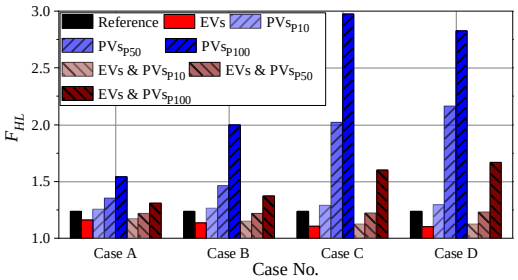
The calculated harmonic loss factor for winding eddy currents ($F_{HL}$), the harmonic loss factor for other stray loss ($F_{HL\text{-}STR}$), K-factor, the maximum permissible secondary-side current ($I_{2\text{-}max}$), the load losses ($P_{LL}$) and the hottest-spot temperature ($\theta_H$) for the four cases with different scenarios are illustrated in Figure 7.17. It is observed from Figure 7.17(a) and 7.17(b) that both $F_{HL}$ and $F_{HL\text{-}STR}$ are the highest when only PVs (with operating power at 50% or 100% $P_{rated}$) connected as opposed to the other scenarios for all the four cases, implying that their eddy current loss ($P_{EC}$) and the other stray loss ($P_{OSL}$) will be the highest as well. It is also noticed that $F_{HL}$ and $F_{HL\text{-}STR}$ gradually increase with the increasing operating power of PVs when only PVs connected, indicating that the waveform distortion of the transformer secondary-side current is aggravated (can be confirmed by the $THD_I$ values at H0 illustrated in Figure 7.15). For all the four cases, the connection of EVs or the connection of both EVs and PVs (at 10% $P_{rated}$) will slightly reduce $F_{HL}$ and $F_{HL\text{-}STR}$ as opposed to the reference case.

In terms of the $P_{LL}$ shown in Figure 7.17(c), the connection of only PVs (at 100% $P_{rated}$) achieves the highest $P_{LL}$ among the eight scenarios of Case B-D, with the connection of EVs only ranked the second. For the Case A, $P_{LL}$ value is between 0.62 and 0.65 for the eight scenarios. According to the definition of the maximum permissible secondary-side current, $I_{2\text{-}max}$, given in Chapter 2, $I_{2\text{-}max}$ is inversely related to $F_{HL}$ and $F_{HL\text{-}STR}$, and hence an opposite trend is observed for $I_{2\text{-}max}$ as opposed to $F_{HL}$ and $F_{HL\text{-}STR}$, with minimum $I_{2\text{-}max}$ obtained when only PVIs connected (at 100% $P_{rated}$) for each case. For $\theta_H$, it is positively related to $P_{LL}$, and therefore the same trend is observed between $\theta_H$ and $P_{LL}$. The increase of $\theta_H$ will accelerate the aging process of the transformer.

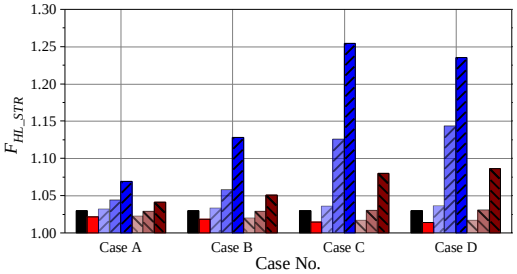
It turns out that $F_{HL}$, $F_{HL\text{-}STR}$, $P_{LL}$, $I_{2\text{-}max}$ and $\theta_H$ all indicate that the connection of PVs (at 100% $P_{rated}$) has the strongest harmonic impact on the transformer operation as opposed to the other scenarios. However, unlike the other indices, K-factor given in Figure 7.17(e) suggests that the connection of PVs only (at 100% $P_{rated}$) has the lowest harmonic impact on the transformer while the connection of EVs only has the highest impact. It is because K-factor represents the weighted current harmonics in terms of the rated secondary-side current instead of the actual one, as in (7.2). It can be predicted from (7.2) that when the current harmonics is much smaller than the fundamental component (i.e. the current waveform is not highly distorted), the fundamental component plays a key role of K-factor. As the connection of EVs only will apparently increase the current demand on the transformer secondary side while the connection of PVs only (at 100% $P_{rated}$) will do the opposite, K-factor for the former scenario will be obviously larger than the later one, as shown in Figure 7.17(e). Based on the above discussion, it can be concluded that K factor cannot accurately reflect the impact of current harmonics on the transformer when the transformer secondary-side current is quite different from its rated value. Instead of using K-factor, indices like $F_{HL}$, $F_{HL\text{-}STR}$, $P_{LL}$, $I_{2\text{-}max}$ and $\theta_H$ should be applied under that situation.

$$K-factor=\frac{1}{I_{2-R}^2}\sum_{h=1}^{h_{max}}(I_{2-h}^2\times h^2) \tag{7.2}$$

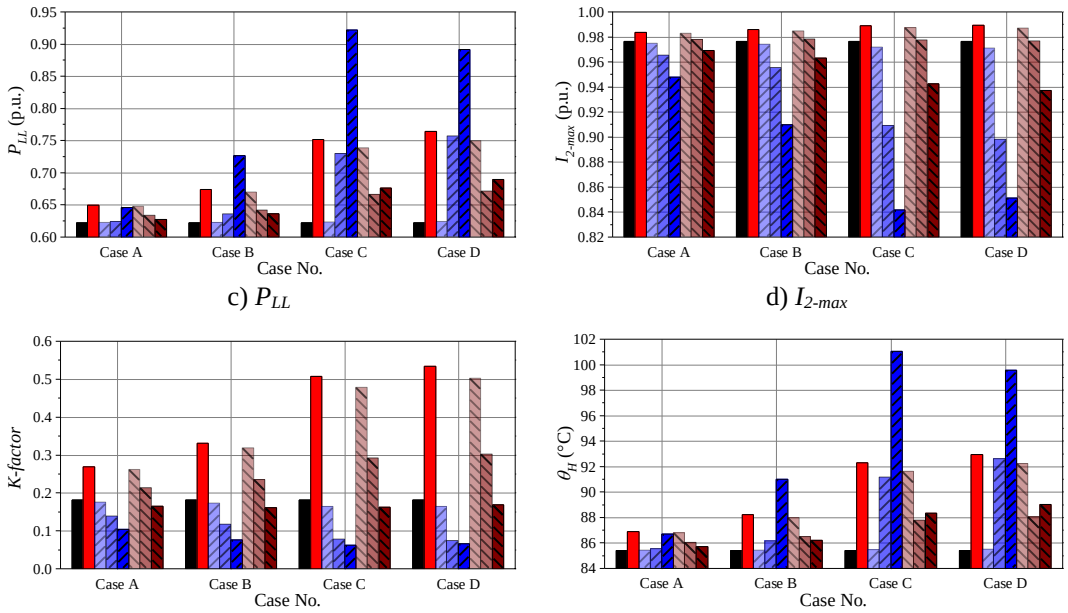
where: $I_{2\text{-}h}$ and $I_{2\text{-}R}$ are the $h$-order current harmonic and the rated current at the transformer secondary side respectively, with $h$ and $h_{max}$ representing the harmonic order and the maximum considered harmonic order respectively.




a) $F_{HL}$




b) $F_{HL\text{-}STR}$




c) $P_{LL}$ d) $I_{2\text{-}max}$

e) K-factor f) $\theta_H$

**Figure 7.17:** The considered performance indicators of the distribution transformer for different cases.

## 7.6 Chapter conclusions

As different models might be applied according to the information available of the modelled PE devices, hybrid modelling technique which allows different forms of harmonic models to be used under the same harmonic network modelling environment, is required. Accordingly, two hybrid harmonic modelling approaches are proposed and demonstrated on a simple network study with both CBMs for EVs and FDMs for CFLs connected. The results from the network case study suggest that the time domain simulations are preferred hybrid modelling approach if FDMs should be applied for the specific PE devices, for which CBMs are not available, or are too complex for the implementation. To further demonstrate the performance of the hybrid modelling approach on complex network, hybrid modelling approach using FDMs in a time-domain simulator is applied to investigate the harmonic interactions between various numbers of EVs and PVs, based on the urban generic distribution network. The network study results suggest that the connection of PVs (at 100% $P_{rated}$) has the strongest harmonic impact on the transformer operation as opposed to the other considered scenarios, with increased harmonic power losses, winding temperature and reduced lifetime. All those findings suggest that the grid-connection of EVs and PVs should take into account their potential harmonic impacts on the network operation, in

order to ensure a good supply voltage quality and the proper operation of grid-connected electrical equipment.

# Chapter 8

# Conclusions and further work

The final chapter reviews the main research work presented in the thesis and its contributions to harmonic modelling and analysis research area. Based on the discussion of the practical implications and limitations of presented work, further work and improvements to methodologies are also indicated.

## 8.1 Thesis summary

This thesis fills in the gap in harmonic modelling of modern PE devices in LV networks, which coverers four different categories of PE devices including LED lamps, SMPS' and PVIs. For each considered device category, comprehensive laboratory tests are first applied to selected test samples in order to investigate the electrical characteristics and performance of the device category, with special attention given to the sensitivity of their harmonic emission and other general power electric quantities to the varying supply conditions. It turns out that the ac current waveform distortion characteristics of considered modern PE devices in the thesis are affected by the varying supply conditions and the operating powers (for power-dependent devices) to different extents. In order to accurately represent the harmonic characteristics of modern PE devices under comprehensive grid conditions and operating powers/modes, the developed harmonic models have to fully take into account those external factors.

On the other hand, the sensitivity of the grid-side ac current waveform distortion to the external factors is mainly determined by the internal factors-circuit topologies and corresponding controls of PE devices, as they determine the current regulation strategy applied. For example, it is observed in Chapter 4 that the three main SMPS' types with different PFC types have distinctive input ac current waveform shapes which have different dependency on the supply conditions. Accordingly, the evaluation of the impact of circuit topologies and control algorithms on the harmonic characteristics of modelled devices is the prerequisite of developing accurate CBMs for PE devices, and is also provided in Chapter 3 to Chapter 6.

Based on the laboratory testing results and a careful review of the general circuit topologies of each device category, CBMs are developed for all the four considered device categories, with the model accuracy fully validated with measurements. In addition to CBMs, FDMs are also provided for the four devices categories. Unlike CBMs, FDMs treat the modelled device as a "black box" without knowing the actual physical circuits, and are built on the basis of laboratory tests focusing on investigating the sensitivity of fundamental and harmonic current components to the fundamental and harmonic voltage components, by applying the generalised modelling procedure introduced in Chapter 2.

To further investigate the differences between CBMs and FDMs, the comparison between CBMs and FDMs is demonstrated on the EVBC modelling, as given in Chapter 5. It turns out that the selection between CBMs and FDMs is mainly determined by the complexity and the available information of the PE devices. For PE devices having simple circuit topologies (e.g. CFLs, the capacitive dropper based LED lamps and SMPS' with no-PFC or with p-PFC), their circuit topologies and corresponding component parameter values can be easily obtained from their typical time-domain input current waveforms, as demonstrated in Chapter 2. Accordingly, component-based modelling approach is more suitable for them as opposed to the frequency-domain modelling approach which requires large numbers of individual voltage harmonic tests, especially when the considered harmonic orders are high.

However, for modern PE devices like EVBCs and PVIs, they are featured by switched-mode converter or inverter circuits with sophisticated control algorithms, and their typical ac current waveforms are close to sinusoidal, implying that it is complex to estimate their circuit topologies and corresponding control strategies based on the measured electrical characteristics of the device. Accordingly, when the information on the circuit topologies of modern PE devices is not available, the frequency-domain modelling approach provides a good solution. For the power-dependent PE devices, conventional FDM requires to be obtained at all considered powers, resulting in the increased number of tests and measurements. Accordingly, two HAM modification based frequency-domain modelling approaches are proposed in Chapter 7 and are demonstrated on the case of PVI modelling. It turns out that the HAM modification

based FDMs have competitive accuracy as opposed to the traditional measurement based FDMs, and are able to correctly represent the power-dependency of the harmonic characteristics of PVIs with significantly reduced number of required tests. As FDMs have generalised model forms, investigating the frequency-domain model aggregation naturally becomes the next step. By comparing the aggregate FDM derived from individual HFMs (i.e. direct summing-up of HAM elements) with aggregate FDM derived from the measurements of different parallel-connected PVI units, it turns out that the presented aggregation approach can well represent the harmonic interactions among different power-dependent PE devices.

From the above discussions, it can be expected that different model forms might be used under the same network simulation environment when investigating the harmonic interactions among PE devices of different categories. To achieve that objective, the hybrid harmonic modelling techniques are investigated through a case study on harmonic interactions between EVs and CFLs in Chapter 7. Based on the network study results, it turns out that the time domain simulations are preferred hybrid modelling approach if FDMs should be used for the specific PE devices, for which CBMs are not available, or are too complex for the implementation. To further assess the applicability of the hybrid modelling approach to a complex network, the harmonic impact of different deployment scales of EVs and/or PVs on the urban generic distribution network model is investigated, for which both EVs and PV are represented by their FDMs. It turns out that high penetration levels of EVs and/or PVs will have an impact on the voltage and current profiles of the network, which will further affect the normal operations of the PE connected devices and the lifetime of distribution transformer.

Furthermore, some of the tested power-dependent PE devices (referring to SMPS', EVBCs and PVIs in the thesis) may significantly increase their non-harmonic distortion contents when their operating power drops to certain levels. Therefore, new indices for the evaluation of current waveform distortions are proposed, allowing for a separate analysis of contributions of low and high frequency harmonics and interharmonics to the total waveform distortion of PE devices (demonstrated on EVBCs in Chapter 5). As all the three power-dependent device categories in the thesis

have their electrical characteristics affected by the varying operating powers, their electric power quantities at rated power cannot represent the overall performance of PE devices under specific operating cycle. Hence, an operating cycle based method for evaluating overall performance of PE devices across the entire range of operating powers is proposed and demonstrated on SMPS'.

## 8.2 Implications of the research

The main focus of the thesis is the harmonic modelling and characterisation of modern PE devices which are expected to keep increasing their penetration into LV networks in the next decades. The considered four device categories include LED lamps, SMPS', EVBCs and PVIs, for which the harmonic characteristics and other general electric power quantities are still not sufficiently studied in existing literatures. For example, the harmonic characteristics of the four device categories are normally investigated based on fixed supply condition and operating mode in related publications without fully taking into account the impact of varying supply conditions and operating powers. Considering the fact that LV networks are generally featured by supply voltage distortion and magnitude deviation, evaluating the sensitivity of the electrical characteristics of modern PE devices to the change of supply conditions and operating powers is one of the main contributions of the thesis, and is also the premise of developing appropriate harmonic models which are capable of accurately representing the PQ performance of modern PE devices working under practical grid conditions.

Regarding the harmonic modelling of considered modern PE devices, they are generally divided into two types which are component-based modelling and frequency-domain modelling. For the component-based modelling of modern PE devices, existing literatures mainly focus on proposing new circuit topologies with improved device performance, and the developed CBMs generally cannot represent the electrical characteristics of existing commercial PE devices. To solve that issue, the CBMs developed in the thesis can well represent the PQ performance of selected commercial PE devices operating under different supply conditions and powers. Accordingly, the provided CBMs can be directly or indirectly applied for different network analysis. In terms of the frequency-domain modelling of modern PE devices,

although a variety of publications discuss the development of FDMs for those devices with good accuracy achieved, the network implementation approaches of FDMs are rarely investigated. Therefore, this thesis not only provides accurate FDMs for considered PE devices, but also investigates the implementation approach of FDMs in both time-domain and frequency domain simulator, as given in Chapter 7. In addition, by observing the relationships among HAMs for PVIs operating at different powers, HAM modification based FDMs are also proposed, which contributes to a significantly reduced number of tests required. After that, the frequency-domain model aggregation is also investigated based on two different parallel-connected PVI units.

Although both CBMs and FDMs can be applied for network studies, their implantation approaches and purposes are different. Specifically, CBMs are a type of electromagnetic transient (EMT) simulation model and require time-domain simulation environment, suggesting that they cannot be directly applied to a conventional harmonic power flow solver. For applying CBMs in a frequency-domain network simulation environment, the hybrid harmonic modelling techniques can be used (as demonstrated in Chapter 7). However, the performance of the hybrid harmonic modelling approaches highly depends on the complexity of the network model. For example, the hybrid harmonic modelling approaches may fail (i.e. unconvergence) for a highly three-phase unbalanced network model. Although CBMs can also be directly applied in a time-domain network simulator, the connection of a large number of CBMs to the network model can significantly increase the computational burdens due to the intensive EMT simulation involved, making it not suitable for large-scale network modelling. Accordingly, CBMs are mainly applied for investigating the network dynamic response due to the connection/disconnection of electrical equipment of interest.

Unlike CBMs which inherently require EMT simulation, FDMs are based on root mean square (RMS) simulation and only take into harmonics of interest. Depending on the mathematical formulation of FDMs, FDMs can be directly or indirectly integrated with harmonic power flow solver, making it applicable for large-scale network model with much less computational burden as opposed to applying CBMs in a time-domain network simulation environment. Therefore, it is worthwhile to further

investigate the compatibility between the Newton-Raphson based conventional harmonic power flow solver and different forms of FDMs, which will facilitate the next step of evaluating the large-scale penetration of PE devices on complex network models.

At last, a methodology is proposed to evaluate the PQ performance of power dependent PE devices over their entire operating cycles, which is demonstrated on a desktop PC-SMPS with assumed operating cycles. The presented approach takes into account the power dependency of the electrical characteristics, which gives a correct performance assessment for the power-dependent PE devices and could be considered as a part of standard device assessment procedures.

## 8.3 Limitations of the research

**Component-based modelling for EVBCs and PVIs**

For the component-based modelling of EVBCs and PVIs, the CBMs developed based on their typical circuit topologies (due to lack of information on the actual circuits), which might not be exactly the same with actual physical circuits of the modelled devices. However, the developed CBMs indeed accurately represent the electrical characteristics of EVBCs and PVIs operating under varying supply conditions and operating powers.

**Validation of frequency-domain model aggregation approach**

The proposed frequency-domain model aggregation approach is only demonstrated on two different parallel-connected PVI units. To fully verify the correctness of the aggregation approach, it is necessary to take into account other combinations of modern PE devices.

**Network harmonic analysis**

As the main purpose of the network harmonic analysis in this thesis is to discuss the implementation approach of the proposed harmonic models and the hybrid harmonic modelling approaches on a network simulator, the applied network case studies are relatively simple and based on a variety of assumptions (e.g. three-phase balanced network and the constant harmonic current emission from the households). In addition, as the PQ performance of modern PE devices is closely related to their implemented

circuit topologies which are normally highly diversified among different manufacturers, the network harmonic analysis by using the harmonic models of selected PE devices may lead to conservative results.

## 8.4 Further work

**Investigating the causes of lost periodicity phenomenon for SMPS'**

During the laboratory tests of SMPS', it is observed that two of the tested SMPS' (with a-PFC) exhibit lost periodicity phenomenon when their operating powers drops below certain values, which does occur to SMPS' with no-PFC or with p-PFC. Although the impact of lost periodicity on the input ac side current harmonic emission and other electric power quantities are fully discussed in the thesis, the possible causes of lost periodicity are only briefly mentioned. To ensure the proper operation of a-PFC converter based PE devices over their entire power ranges, it is necessary to evaluate the causes of lost periodicity phenomenon from the circuit operation perspective.

**Application of frequency-domain aggregation to FDMs of different device categories**

In the thesis, the frequency-domain model aggregation approach is validated on the two parallel-connected PVIs only. It is necessary to further investigate the applicability of the aggregation approach for different types of PE devices, which will facilitate the further network harmonic analysis by using FDMs.

**Development of dedicated harmonic power flow simulator**

Although the hybrid modelling approaches proposed in Chapter 7 allows FDMs to be implemented on either time-domain or frequency-domain network simulator, they are generalised harmonic network analysis approaches and their performance (e.g. accuracy and convergence of simulation) is closely related to the complexity of modelled network and the model forms of connected FDMs. In addition, current commercial software for network harmonic analysis normally represent the harmonic emission of nonlinear devices by constant voltage or current harmonic sources without taking into account the supply voltage and power dependency of harmonics. Accordingly, a dedicated harmonic power flow simulator which is compatible with HAM based FDMs should be developed. By fully considering the supply voltage dependency of the current harmonic emissions of modern PE devices, the harmonic

power flow simulator will be able to well represent the harmonic interactions among modern PE devices of different categories, which is important for understanding the potential harmonic related PQ issues due to the proliferation of PE devices seen in LV networks.

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# Appendix A
# List of publications


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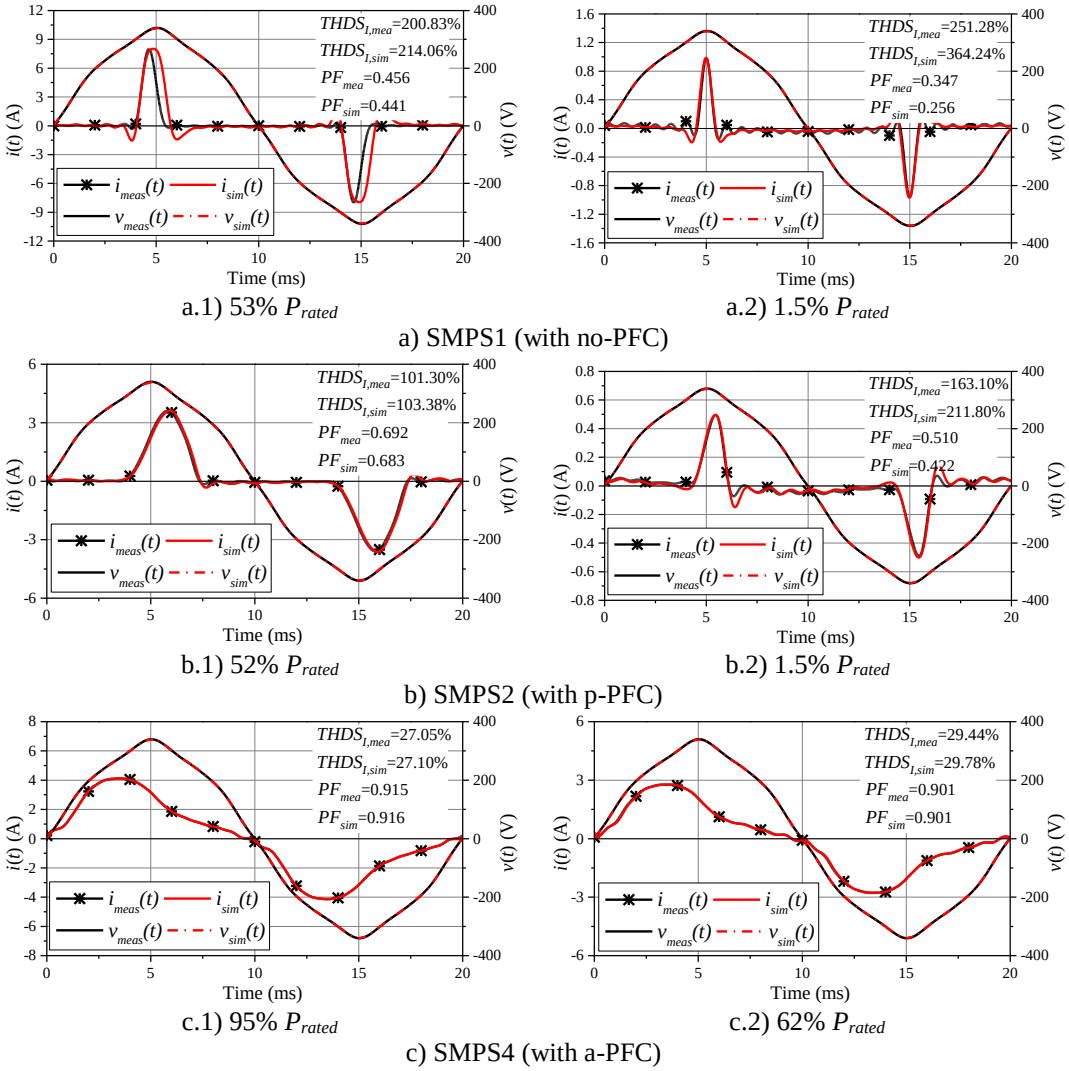
# Appendix B

# Validation of CHNMs for SMPS'




a.1) 53% $P_{rated}$ a.2) 1.5% $P_{rated}$

a) SMPS1 (with no-PFC)

b.1) 52% $P_{rated}$ b.2) 1.5% $P_{rated}$

b) SMPS2 (with p-PFC)

c.1) 95% $P_{rated}$ c.2) 62% $P_{rated}$

c) SMPS4 (with a-PFC)

**Figure B.1:** The comparison between measured and simulated (CHNMs) input ac current waveforms for tested SMPS' operating at different power levels with WF3 distorted supply voltage.

# Appendix C

# Distribution network data

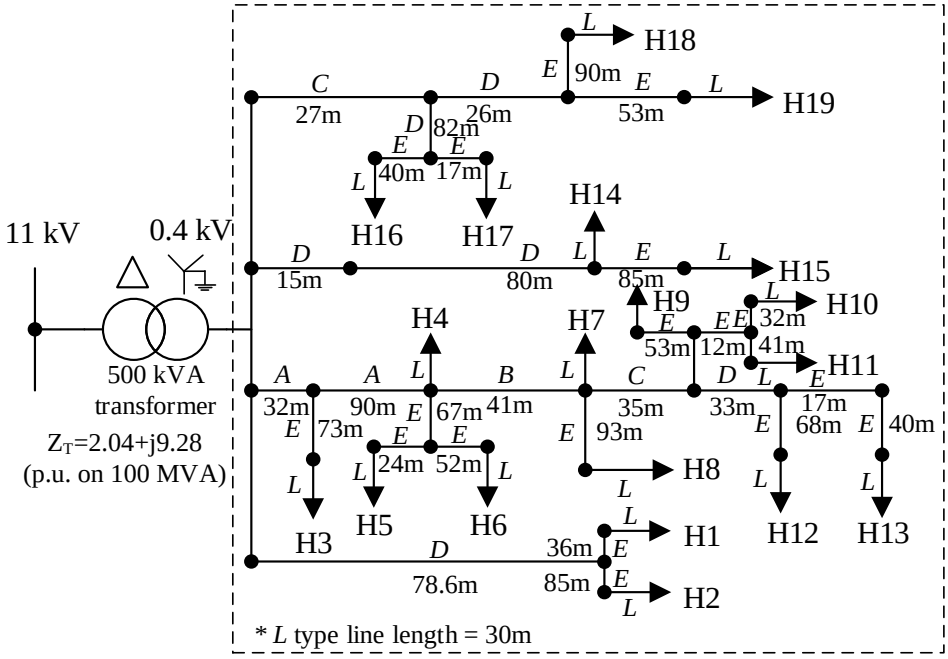



**Figure C.1:** Urban generic LV distribution network model with information on line lengths.

**Table C.1:** Generic UK urban MV/LV distribution network component values [2].

| Id. | Type | CSA ($mm^2$) | Impedance | | | | | $I_{max}$ (A) |
|---|---|---|---|---|---|---|---|---|
| | | | Positive seq. | | Neutral | Negqtive seq. | | |
| | | | R | X | R | R | X | |
| | | | Ω/km | | | | | |
| **LV lines** | | | | | | | | |
| A | UG | 300 | 0.100 | 0.073 | 0.1268 | 0.593 | 0.042 | 465 |
| B | UG | 185 | 0.163 | 0.074 | 0.168 | 0.656 | 0.050 | 355 |
| C | UG | 120 | 0.253 | 0.071 | 0.253 | 1.012 | 0.047 | 280 |
| D | UG | 95 | 0.320 | 0.0975 | 0.320 | 1.280 | 0.051 | 245 |
| E | UG | 70 | 0.443 | 0.076 | 0.443 | 1.772 | 0.052 | 205 |
| L | UG | 35 | 0.851 | 0.041 | 0.900 | 3.404 | 0.030 | 120 |
| **MV lines** | | | | | | | | |
| P | UG | 185 | 0.1227 | 0.0658 | - | 0.85896 | 0.23011 | 415 |
| Q | UG | 95 | 0.1440 | 0.0667 | - | 1.00824 | 0.23318 | 355 |
| where: UG - underground cable and CSA is the cross sectional area. | | | | | | | | |

**Table C.2:** The phase connection of the households.

| House cluster No. | Numbers of households | Numbers of households at each phase | | |
|---|---|---|---|---|
| | | Phase A | Phase B | Phase C |
| H1 | 15 | 5 | 5 | 5 |
| H2 | 12 | 4 | 4 | 4 |
| H3 | 12 | 4 | 4 | 4 |
| H4 | 12 | 4 | 4 | 4 |
| H5 | 14 | 5 | 5 | 4 |
| H6 | 9 | 3 | 3 | 3 |
| H7 | 6 | 2 | 2 | 2 |
| H8 | 12 | 4 | 4 | 4 |
| H9 | 9 | 3 | 3 | 3 |
| H10 | 6 | 2 | 2 | 2 |
| H11 | 6 | 2 | 2 | 2 |
| H12 | 12 | 4 | 4 | 4 |
| H13 | 9 | 3 | 3 | 3 |
| H14 | 15 | 5 | 5 | 5 |
| H15 | 15 | 5 | 5 | 5 |
| H16 | 8 | 2 | 3 | 3 |
| H17 | 8 | 3 | 2 | 3 |
| H18 | 6 | 2 | 2 | 2 |
| H19 | 4 | 1 | 2 | 1 |