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HW/SW Co-Simulation System for Enhancing Hardware in the Loop of Power Converter Digital Controllers

Aránzazu Fernandez-Alvarez, Marta Portela-García, Mario García-Valderas, Jaime López, Marina Sanz

***Abstract*—Digital controllers of power converters are more and more implemented in FPGAs due to the increasing complexity of current control algorithms, higher switching frequencies and concurrency requirements. System behavior depends not only on the control algorithm but also on implementation issues. Thus, closed-loop controller evaluation at early design stages is a main concern. In this work, a new Hardware-in-the-loop method is proposed. It profits from FPGAs and their design tools in order to validate the closed-loop power converter before prototyping the power stage. The proposed solution presents a general architecture that does not depend on specific vendors or CAD tools, but it uses those utilized for the final implementation of the controller. A case study is presented with a given implementation of the proposed solution. Comparisons with existing alternatives show the advantages of our approach.**

***Index Terms*— Hardware-in-the-loop, power converter digital controller, FPGA**

I. Introduction

DIGITAL control of power converters is more and more used in modern power electronic circuits and this trend will continue to grow with the increasing of power circuitry integration. Digital control provides flexibility, higher tolerance to noise and higher robustness against thermal and ageing effects [1][2]. However, the digital-based implementation of the power converter control involves new concerns with respect to analog implementations, mainly due to the time discretization and finite resolution features [3][4].

Digital control can be implemented by using a microprocessor, DSP or an FPGA-based platform [5]. Depending on the application requirements one or the other kind of implementation will be more convenient. On the one hand, microprocessor or DSP-based platforms are cheaper and easier to use. On the other hand, the FPGA-based implementation, requires a higher design effort, especially if arithmetic operations with real numbers are required; in general, they are more expensive but they provide higher performance since they support concurrency. Therefore, in case of applications with high performance requirements, FPGAs would be the most convenient solution for the control implementation [6][7][8].

This work is aimed at providing a solution to evaluate the behavior of the close-loop control of power converters, during the design stage, for applications with FPGA-based control implementations. Efficient validation mechanisms at early design stages allow the designer to reduce the design time and cost and the time to market. The presented approach is intended to detect any malfunction or deviation from the requirements of the closed-loop power converter due to digital implementation issues, before the prototyping phase of the power stage and speeding up the evaluation process with respect to simulation-based approaches.

The method is based on a new approach for FPGA-In-the-Loop (FIL) mechanism, which is faster than existing approaches and widely applicable. It should be applied without modifying the design flow, that is, by using the same description mechanisms for circuits than those used by designers.

This approach follows the existing trend in current digital design methodologies (independently on the application), where emulation is increasing its relevance against simulation-based debugging tasks. This is a fact in current microcontrollers, DSPs and FPGAs due to the provided performance and realistic results. In this work, an emulation step is included in the whole power converter design method in order to enhance the debugging tasks related with the control implementation.

The rest of the paper is organized as follows. Section II summarizes the related work available in the literature. Section III presents the proposed Hardware-in-the-loop (HIL) system, describing the required components and the system architecture. Section IV presents the features of a case study that will be used to obtain experimental results and to validate

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the proposed approach. Section V presents experimental results and section VI collects the main conclusions.

II. Related Works

The interest of using FPGAs to implement the controller of a power system is increasing due to the raising number of applications where concurrency is a requirement (for example, when multiple channels must be controlled) or where the control algorithm complexity is very high along with high speed requirements [6], for example, in the case of flexible AC transmission systems [7]. Other examples are illustrated in [8] and [9], where the authors proposed the use of FPGAs in order to increase the time resolution of digital pulse width modulators for applications with high switching frequencies.

During the design process of the closed-loop power converter, the validation of the complete system is a key step. This paper is focused on the digital control validation since the implementation issues are critical for the correct behavior of the application. In the literature, there are several proposals intended to evaluate the closed-loop digital controllers taking into account the specific effects due to the chosen digital implementation. Two main different approaches can be distinguished:

- Simulation-based by combining analog and digital simulators.
- Emulation by means of hardware in the loop (HIL) methods. A HIL method consists in replacing part of the system model by a hardware implementation. This way, the validation is sped-up and, in some cases, it can be used to assess implementation dependent effects [10].

Simulation-based validation is required in order to detect any possible error before the prototyping phase. In [11], a true co-simulation method is proposed by combining an electrical simulator (PSIM) with a digital one (ModelSim) in order to obtain realistic results.

HIL platforms can be categorized in two main types:

- Platforms that use a hardware implemented digital model of the system to control, the power stage. The controller can be either simulated in the computer or it can be also implemented in hardware. This approach is used to accelerate the simulation process.
- Only the digital controller is implemented in the HIL platform while the power stage is simulated in a host computer. This approach is used to validate the digital controller using a real implementation.

[12] presents a comparison between different HIL alternatives where the complete system is implemented in HW and co-simulation-based solutions for closed-loop evaluation of power converters. This work analyzes the advantages and disadvantages of each approach. Simulation is a very time-consuming method and it usually considers behavioral simulations. Thus, no synthesis related errors can be detected. Using digitals models for power stages in order to speed-up the closed loop power system evaluation is a current research topic. However, the development of the device models implies a very high design effort.

There are high end solutions to the mixed signal simulation problem, like real time simulators OPAL-RT [13] or RTDS [14]. They propose to implement hardware models of the power stage, involving FPGA or multi-processor simulation systems. These solutions are expensive and usually imply the cost of the emulation or simulation specific hardware and the associated software.

Regarding solutions where only the controller is in the HIL, the approaches presented in the literature are based on the use of some specific CAD. In [13], a HIL platform based on using DSP Builder from Intel® FPGAs (previously Altera) and Simulink connection is proposed. In [16], C. Paiz et al. present a method based on Simulink/Matlab and System Generator, from Xilinx, capabilities.

In [17], the authors present a HIL platform integrated in a Zynq device from Xilinx, a System on Chip device. This approach is tied to the proposed implementation and there are no comparisons with other existing approaches.

This paper proposes a new HIL platform based on Systems on Chip, where the power stage is simulated at electrical level by an embedded microprocessor while the digital control is emulated in programmable logic. A preliminary version of an embedded system aimed at evaluating mixed-signal circuits is described in [18]. That approach has been modified and enhanced and oriented to the power converters systems. In this work, we use the proposed HIL platform in the control design flow (see figure 1), where that platform presents a general architecture, non-dependent on vendors or specific CADs.

We propose to use FPGA emulation in the digital control design process for power converters, as a verification mechanism at the end of the design process (figure 1). FPGA emulation is used as a way to test the digital control implementation along with a simulation of the power stage. We propose to perform the analog simulation in a device close to the digital emulator, so that analog-digital communication time is minimized.

The approach we propose make use of commercial FPGA boards and use the standard tools provided by FPGA vendors. The methodology does not require any specific hardware, as long as the platform provides embedded processors and programmable logic.

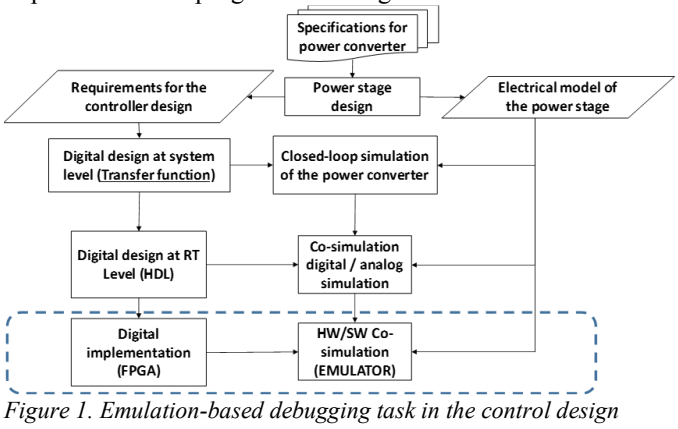

Figure 1. Emulation-based debugging task in the control design methodology

III. FPGA EMULATION IN THE CONTROL DESIGN FLOW

The proposed method consists in adding an emulation-based debugging step in the control design methodology by profiting from the fact that the FPGA is the platform used in field to implement the controller of the power converter. The proposed emulator is based on a hardware/software (HW/SW) embedded system intended to speed up the debugging task, since this is an iterative task within the design process. The proposed emulator consists in prototyping the digital part of the circuit in a programmable device, an FPGA, while the power stage is simulated at the required abstraction level in an embedded microprocessor, next to or inside the FPGA. Therefore, the accuracy of electrical level simulations required for the power stage can be exploited along with the speed of hardware executions for digital blocks.

This approach profits from the high performance and resource availability of modern FPGA devices. All the FPGA vendors provide the necessary tools to support the implementation of such a system.

If the final implementation of the digital controller is FPGA based, the proposed method provides two main advantages. The digital controller is simulated through FPGA emulation, so it is a verification step with a hardware very similar to the final implementation. FPGA emulation also provides a great simulation time improvement.

The emulator has a modular design in order to make its application easy for any digital design and power stage. Figure 2 shows the main components of the proposed emulator: the embedded microprocessor, the digital component, the communication interface (between the host and the emulator) and the analog/digital interconnection which is the most critical part of this proposal. Each component is explained in detail in the following subsections.

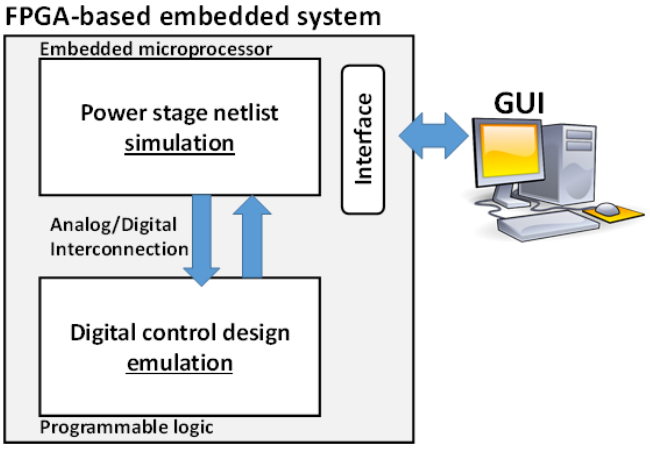

Figure 2. Emulator-based debugging tool block diagram

A. Embedded Microprocessor

This component is in charge of executing the simulation of the power stage at electrical level as well as managing the complete process by controlling the interconnection with the digital hardware component. The electrical simulation can be implemented by using two different approaches:

- Standalone based approach: numeric methods are used to solve the differential equations. In order to facilitate the usage of this approach a library with known topologies and electrical models of the power stage is provided, including parasitic effects.
- Operating System based (OS) approach: a SPICE-like simulator is running on an embedded OS. The electrical netlist generated as part of the design stage is directly used in this approach.

With respect to the managing tasks, user level software is responsible for initializing and configuring the hardware platform and handling synchronization between analog simulation and digital emulation.

Data exchange and synchronization mechanisms affect both simulation accuracy and speed. A memory sharing mechanism is required to support data exchange between the microprocessor and the custom hardware implemented in the programmable logic. Every time both components achieve a synchronization point, input and output states are read from or written to shared memory buffers, accessible from the microprocessor as well as from the programmable logic.

Regarding the simulation/emulation time step, there are two options depending on the chosen approximation for the software component:

- In case of the standalone approach, the integration step is fixed. Time step must be a multiple or a submultiple of the digital resolution, which is one digital clock cycle (Tclk). Synchronization points are established periodically, and the synchronization period is defined as the least common multiple of the analog step size and the digital resolution.
- In case of using the OS approach, due to the usage of a SPICE-like engine, the step size will be variable, although the digital resolution will always be one digital clock cycle (Tclk).

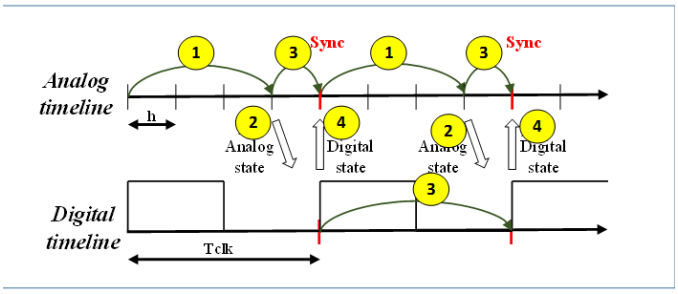

Figure 3. System synchronization. Example for h < Tclk

Figure 3 shows an example of synchronization between the power stage simulation and the digital emulation for the case of fixed analog simulation step (h). In this case, the clock period is greater than the simulation step (h < TClk). The necessary steps are the following:

1. Analog simulation advances up to the simulation step immediately before a synchronization point.
2. Analog output states are written to the shared memory region.

3. The processor starts the IP core. The last analog step and the next emulation cycle are executed concurrently.
4. Digital output states are read from the shared memory space when the processor and the IP block finish the execution.

B. Digital Component Implemented in Programmable Logic

The FPGA-based subsystem consists of a soft Intellectual Property core (IP) that emulates the digital controller of the power converter at the register transfer level. Figure 4 shows the diagram block of the implemented IP in the programmable logic. It includes the digital controller of the power converter as well as other components to manage the emulation and communication with the rest of the embedded system. All the modules but the digital controller can be reused in different designs.

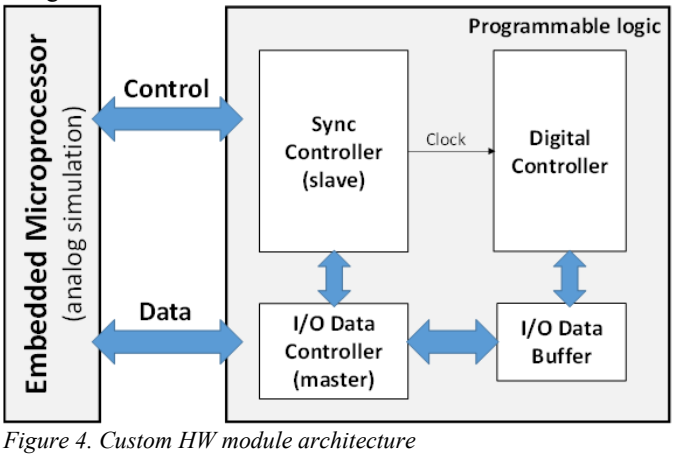

Figure 4. Custom HW module architecture

As explained in a previous subsection, the embedded microprocessor manages and synchronizes the whole system execution. For this purpose, the clock signal of the digital controller is enabled or disabled as needed. Clock gating is a common technique in low power architectures. Furthermore, current FPGA devices support these functions by means of using clock buffers with enable, which prevent the appearance of clock glitches. Therefore, this functionality can be implemented easily and in a reliable way.

Regarding the communication interfaces, the custom hardware includes a slave interface to receive commands from the embedded microprocessor and a master interface to launch the reading or writing process of data to exchange with the power stage.

The algorithm executed by the digital component is described with a flow chart in figure 5. The custom IP is waiting for a start signal from the embedded microprocessor. Then, shared memory is accessed in order to obtain the input data and the digital clock is enabled for a number of clock cycles fixed by the embedded microprocessor. After that, the results are written to the shared memory and an interrupt request is sent to the microprocessor to warn about a synchronization instant.

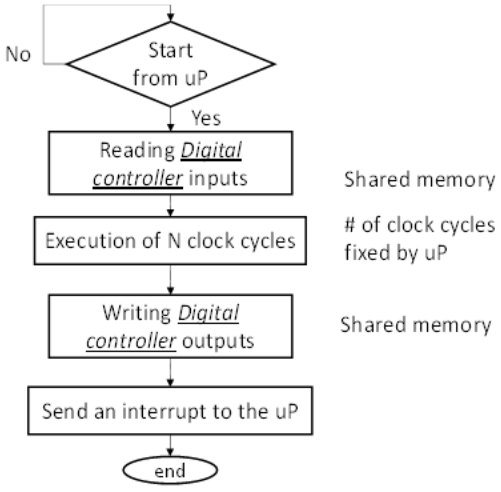

Figure 5. Flow chart of the algorithm executed by the digital component implemented in the programmable logic

C. Analog/Digital Interconnection

The interconnection between both subsystems is a critical block since it determines the data exchange speed and it could limit the required time for the co-simulation process.

In order to ensure the applicability and portability of the proposed approach, protocols of the ARM Advanced Microcontroller Bus Architecture (AMBA) open standard should be used. Most of current embedded microprocessors provided by FPGA vendors are compliant with this standard.

D. Integration

The proposed solution requires a connection to a host PC in order to configure the complete emulation system and to collect the outputs and signals to test. The communication interface should be fast enough so that it is not a bottleneck in the debugging process, but there are no restrictions related to usage requirements or imposed by the presented approach.

Figure 6 shows the user level process required to configure and launch a debugging process by using the proposed system. A graphical user interface and the developed modular design allow a highly automatic and user friendly configuration and implementation of the proposed solution.

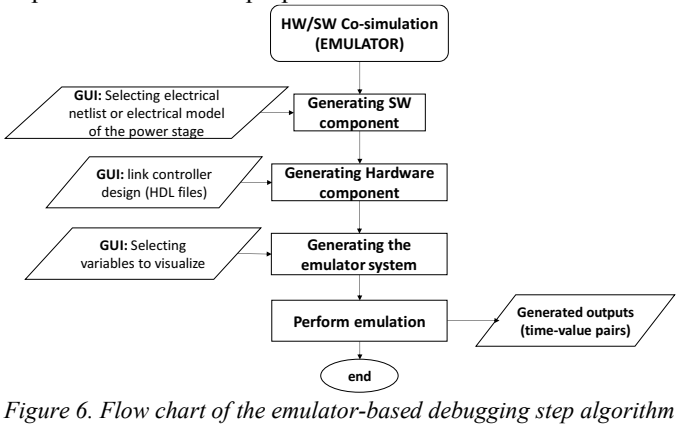

Figure 6. Flow chart of the emulator-based debugging step algorithm

IV. Case Study: Digital Control for DC-DC Power Converter

In order to prove the feasibility of the approach described in this work, several experiments have been developed for a synchronous buck converter. Figure 7 shows the general block diagram of the chosen case study.

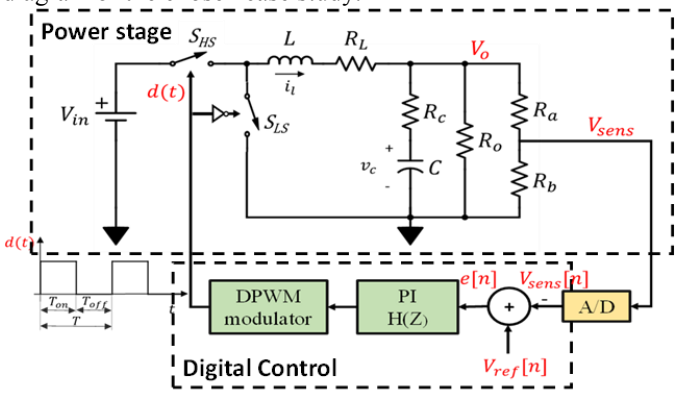

Figure 7. General block diagram of the digitally controlled buck converter

Two different experiments have been developed with two different power converters. Experiment 1 uses an electrical model of the power stage, while in experiment 2, tests with a real prototype of the power stage have also been performed. The buck converter selected to perform the experiment 2 is the PTD08A020W from Texas Instruments [19]. Table 1 presents the values of power stage parameters for each experiment.

TABLE 1. PARAMETERS OF THE BUCK CONVERTERS USED FOR DEVELOPING THE EXPERIMENTAL RESULTS

Parameter	Exp 1	Exp 2 (PTD08A020W)
Vin	11.0 V	6.1 V
Vref	2.0 V	1.65 V
R_{dsonHS}	-	5 mΩ
R_{dsonLS}	-	2.5 mΩ
L	38 µH	1 µH
R_L	1.0 nΩ	1.5 mΩ
C	200 µF	377 µF
Rc	1.0 mΩ	0.375 mΩ
Ro	5 Ω	0.4 Ω
Rsensor (Ra, Rb)	15 kΩ, 45 kΩ	100 kΩ, 100 kΩ
fsw	100 kHz	390.625 kHz

TABLE 2. PARAMETERS OF THE DIGITAL CONTROLLER USED FOR DEVELOPING THE EXPERIMENTAL RESULTS

Parameter	Exp 1	Exp 2
f_{clk}	100 MHz	50 MHz
#bits ADC	8 (LSB=12.9 mV, Vref+=3.3V)	
#bits DPWM	10 (1000 cycles, 11 mV)	9 (11.9 mV)
f_{DPWM}	100 MHz	200 MHz
Control Type	Proportional-integral	Integral

Regarding the digital control system, Table 2 shows the corresponding data. Both controllers implement a digital pulse-width modulator (DPWM) and a digital proportional-integral controller. As shown in table 2, the DPWM has a higher voltage resolution than the ADC to prevent limit cycles from appearing at the output.

Experiment 1 is aimed at comparing different simulation methods, by comparing computer simulation approach, the Matlab HIL approach and our proposed HIL approach, as it is shown in figure 8.

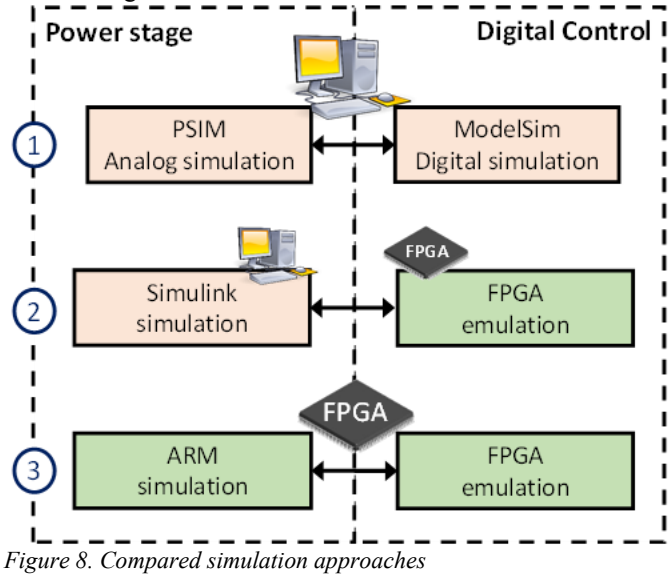

Figure 8. Compared simulation approaches

1. PSIM/ModelSim co-simulation: PSIM simulates the power stage (analog) and ModelSim simulates the digital control. Both simulations run in a single computer.
2. MATLAB FIL (FPGA in the Loop). The power stage is modelled with Matlab-Simulink, obtaining a discretized model of the analog circuit. The digital controller is implemented in a Virtex-6 FPGA (XC6VLX240T), using a ML605 development board from Xilinx. Analog simulation runs in a computer and digital emulation runs in the FPGA.
3. Proposed HIL method. A Xilinx Zynq device is used to implement the power stage simulation in the ARM embedded microprocessor and the digital control is emulated in the FPGA part of the device. Both analog and digital systems run in the FPGA

Experiment 2 has been used to compare the proposed approach with a real implementation of the power converter, using a commercial power stage and an FPGA.

V. Experimental Results

In experiment 1, the results provided by the proposed HIL method, for a given application, have been compared with results obtained by using the existing and widely accepted mechanisms.

Figure 9 shows the output voltage obtained by the three mechanism and Table 3 presents the data for execution time and output error, in terms of the root mean square deviation (RMSD) with respect to the PSIM/ModelSim co-simulation method. The three graphs have been represented separately instead of in a same figure, since the difference is so small that

it cannot be appreciated without applying a very high zoom-in. Indeed, in Table 3, the error metric (RMSD) illustrates this value is particularly small in case of the proposed approach and less than the error in case of MATLAB FIL.

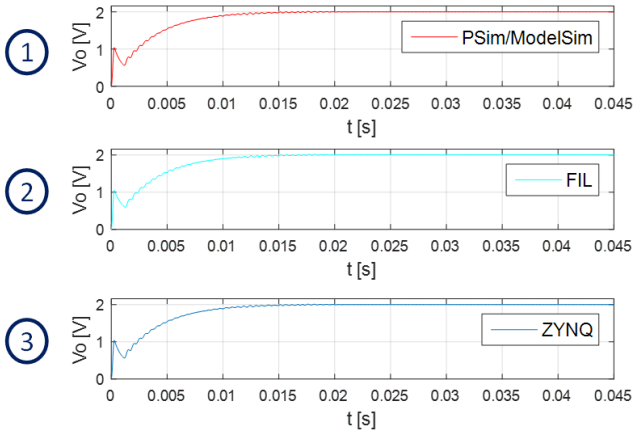

Figure 9. Output voltage generated by the closed-loop power converter by using three different co-simulation or HIL mechanisms: (1) PSIM/ModelSim, (2) MATLAB FIL and (3) proposed HIL.

Regarding execution time, the proposed approach speeds-up, the reference FIL method. Although this factor is low, it has to be taken into account that this goes with an improvement of two orders of magnitude in the result accuracy.

TABLE 3. RESULTS OF THE EVALUATION OF THE CLOSED-LOOP CONTROL IN TERMS OF EXECUTION TIME AND ROOT MEAN SQUARE DEVIATION OF THE OUTPUT WITH RESPECT TO THE PSIM/MODELSIM CO-SIMULATION

Co-simulation environment	Execution time	RMSD
PSIM/ModelSim	61 min	-
FIL ODE1 Euler (Rpl=0.5M)	6.10 min	$1.01 \cdot 10^{-2}$ V
Zynq. Runge Kutta 2nd order	5.78 min	$5.48 \cdot 10^{-4}$ V

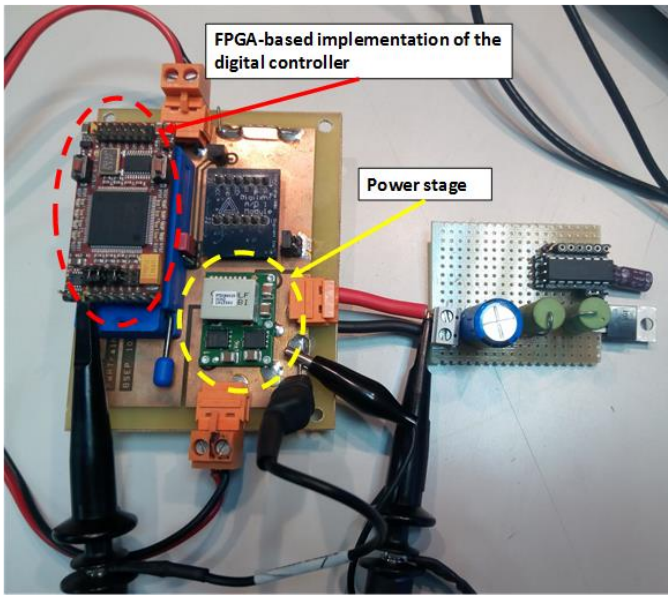

Figure 10. Experimental setup of the power converter

A test with a real power converter has also been performed (experiment 2). It consists in a step at the reference voltage that results in an output voltage (Vo) step, which is recorded by the oscilloscope (Tektronix MSO4104, 1GHz, 5Gs/s). It is compared with the step response obtained with the proposed HIL mechanism to validate results. The reference voltage step changes from 1.65 V to 1.86 V.

Figure 10 shows the experimental setup of the closed-loop system with the PTD08A020W power converter. The digital controller consists of a Xilinx XC3S200 FPGA and an AD7476A ADC.

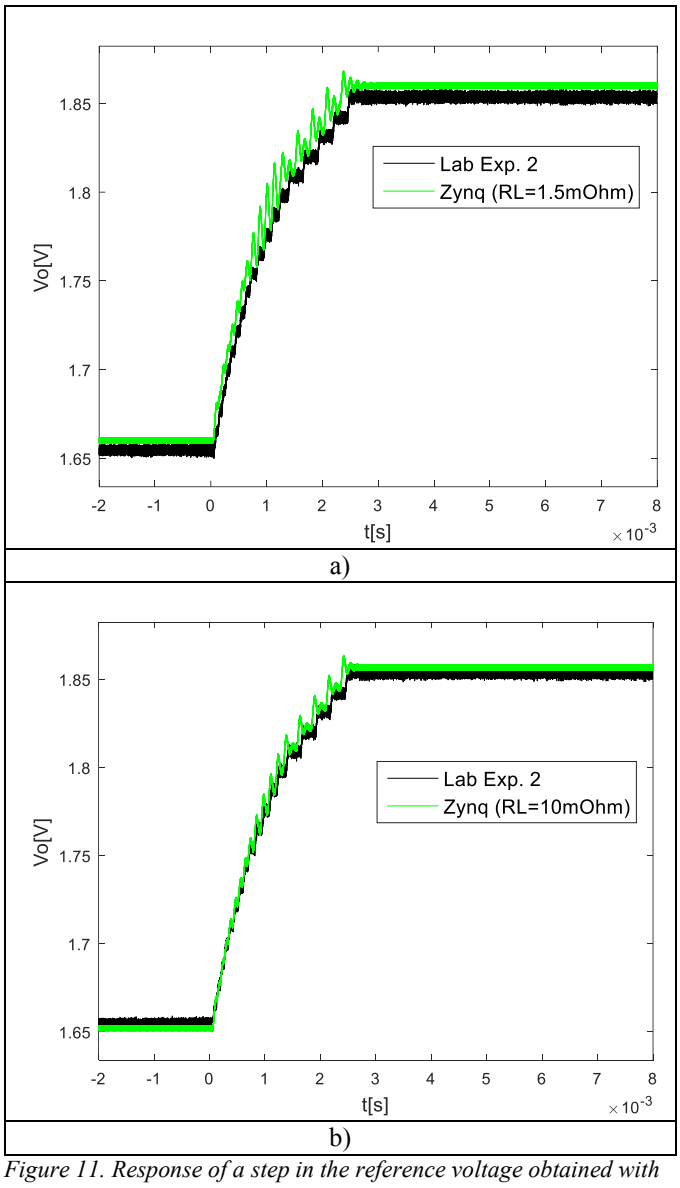

Figure 11. Response of a step in the reference voltage obtained with the real power converter (Lab, in black) and with the proposed HIL (Zynq in light green). a) Parasitic resistance in the inductor RL = 1.5mΩ, b) RL = 10 mΩ

In Figure 11, the response to the voltage reference step is shown. The response generated by the real power converter is shown in black. The response generated by the proposed HIL method is shown in green. In Figure 11.a) and Figure 11.b), results changing the value of the parasitic resistance in the

inductor illustrate how the plant simulation model affects the response. Therefore, the differences that appear in both responses (real and emulated) are due to the unknown values of the actual power stage components.

Table 4 shows a qualitative comparison based on this paper results and information available in literature. It shows some characteristics of the different methods available for power converter simulation. Simulation based methods (PSIM & ModelSim co-simulation) are accurate, but very slow. Matlab & emulation methods are reasonably fast and accurate. Their cost is also high because of Matlab cost. Real Time simulation systems are very powerful, in fact, they provide the best performance in terms of execution time. However, these solutions are very expensive, as they imply the use of proprietary hardware and software.

The solution we propose is a tradeoff. Speed and accuracy are good, while the cost is low. For the hardware, we require a commercial board with a modern FPGA. It can contain a hard core microprocessor, like Zynq (Xilinx) or Stratix (Intel/Altera) devices, or otherwise, a soft core microprocessor can be prototyped. Thus, even if the FPGA-based platform for in-field implementation does not include a microprocessor, the FPGA can be programmed with the necessary core (main vendors provide ARM cores for the current FPGA devices). For the software, we just require the use of FPGA vendor tools, which are not very expensive and even free for some devices. We are also platform independent, being able to use several available commercial boards.

In summary, the proposed solution is the method that provides a best tradeoff in terms of cost, speed, accuracy and applicability. The main limitation of single FPGA based methods, like Simulink FIL or our proposal, is the scalability: for very big circuits, the available resources in the FPGA can be insufficient.

TABLE 4. MIXED SIGNAL APPROACHES COMPARATIVE TABLE

System	Power stage	Digital control	SW requirements	HW requirements	Speed	Accuracy	Cost
PSIM & ModelSim	Simulation	Simulation	PSIM ModelSim	None	Slow	Very High	Medium
Simulink FIL	Simulation Discretized	FPGA emulation	Matlab Simulink	Commercial	High	High	High
Real Time Simulation System (RTDS, OPAL-RT)	Emulation	Emulation	Proprietary	Proprietary	Very high	Very High	Very high
Our HIL proposal	Simulation	FPGA Emulation	FPGA vendor	Commercial	High	Very High	Low

VI. CONCLUSION

This paper presents a new Hardware-in-the-loop FPGA based solution to accelerate analog-digital co-simulation for power converter design. The selected FPGA can be a platform intended to develop the debugging test or the device what will be used as the final implementation platform for the digital controller. The proposed approach consists of an embedded microprocessor to simulate an electrical model of the power stage and the programmable logic to emulate the digital controller. This method can be implemented just by using tools and devices provided by programmable logic vendors, since current devices support embedded systems with microprocessors and programmable logic.

Experiments have been performed for a case study and a particular implementation with a Zynq SoC. Obtained results are compared with a real hardware implementation and with other existing simulation mechanisms, like PSIM/ModelSim co-simulation and Matlab FIL mechanism. Results show that the proposed method provides high accuracy as well as it speeds up the debugging process. Furthermore, the method is applicable to different FPGA vendors and only requires the tools provided by them, making this approach very general and low cost with respect to state of the art tools.

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