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Low-Cost Soft Error Robust Hardened D-Latch for CMOS Technology Circuit

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Abstract: In this paper, a Soft Error Hardened D-latch with improved performance is proposed, also featuring Single Event Upset (SEU) and Single Event Transient (SET) immunity. This novel D-latch can tolerate particles as charge injection in different internal nodes, as well as the input and output nodes. The performance of the new circuit has been assessed through different key parameters, such as power consumption, delay, Power-Delay Product (PDP) at various frequencies, voltage, temperature, and process variations. A set of simulations has been set up to benchmark the new proposed D-latch in comparison to previous D-latches, such as the Static D-latch, TPDICE-based D-latch, LSEH-1 and DICE D-latches. A comparison between these simulations proves that the proposed D-latch not only has a better immunity, but also features lower power consumption, delay, PDP, and area footprint. Moreover, the impact of temperature and process variations, such as aspect ratio (W/L) and threshold voltage transistor variability, on the proposed D-latch with regard to previous D-latches is investigated. Specifically, the delay and PDP of the proposed D-latch improves by 60.3% and 3.67%, respectively, when compared to the reference Static D-latch. Furthermore, the standard deviation of the threshold voltage transistor variability impact on the delay improved by 3.2%, while its impact on the power consumption improves by 9.1%. Finally, it is shown that the standard deviation of the (W/L) transistor variability on the power consumption is improved by 56.2%.

Keywords: Hardened D-latch; Complementary Metal Oxide Semiconductor (CMOS) technology; Power-Delay Product (PDP); Soft Error (SE); SEU (Single Event Upset); High Impedance State (HIS); Single Event Transient (SET)

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1. Introduction

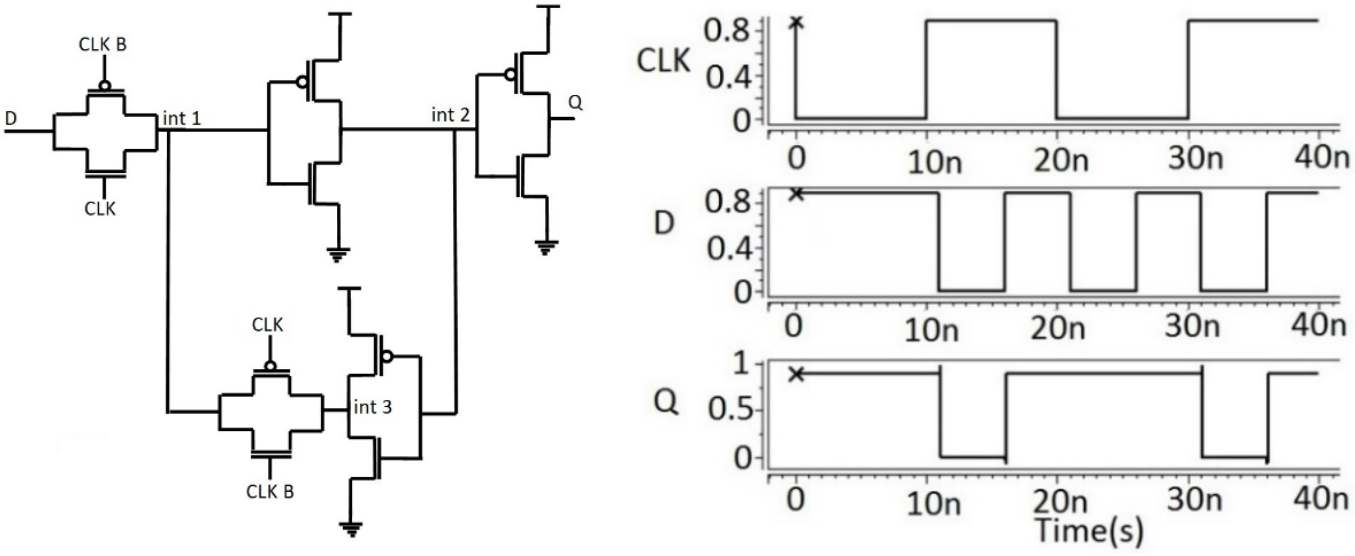
The advent of nano-scale transistors is a movement towards the reduction of the supply voltage of circuits, but this implies increases in delay and parasitic effects [1]. Thus, nano-scale CMOS circuits are more vulnerable to errors, such as the Soft Error (SE) caused by Single Event Upset (SEU) [1]. These errors have a huge negative impact on hardware security of integrated circuits, which is invested frequently [2,3], even for electronic applications [4–6]. In the particular case of SE, they have to be addressed as a hardware security or hardware reliability issue since they can be caused by and from the environment. Environmental radiation can be constituted by high energy particles (such as neutrons, protons, alpha particles, etc.), whose impact is similar to an injected charge or SEU to internal nodes. These charge injections can potentially change the value of stored data inside digital circuits. Another typical error is Single Event Transient (SET), which is the result of a combinational path connecting to the input of D-latch in digital circuits [7]. This undesirable pulse, as error, can change the output voltage level of a D-latch. Traditional D-latches and memory cells are very vulnerable against upsets; thus, many approaches have been proposed to solve this problem; among these are hardened circuit design [8], error correcting codes (ECC) [9] and temporal redundancy [10]. Many new D-latches have

also been proposed to increase immunity against SEU [11–17] and SET [7,13]. The design of these D-latches is based on filtering the SEU or/and SET. However, the highest immunity of D-latches against the SEU and SET is achieved by increasing the number of transistors, which yields several penalties such as higher power consumption, larger area, and delay. This work proposes a new D-latch considering this trade-off and aiming at achieving a better solution in terms of power consumption, delay, working condition (temperature), process variation, and filtering the possible length of SET pulses. Immunity against SEU for various nodes is also observed. These features have been paired with a low-cost and reliable design, having a power consumption and delay close to the Static D-latch, set as a reference D-latch.

The paper is structured as follows: Section 2 revisits previous works on the topic including a review of existing hardened latches. The new D-latch architecture is introduced in Section 3, where SEU and SET immunity of the proposed D-latch are also tested by an exponential current pulse model that is inserted in various internal nodes. In Section 4, the impact of technological variability and temperature on the proposed and previous D-latches is investigated. The main conclusions are drawn in Section 5.

2. Previous Work

Traditional D-latches are very vulnerable against upset, which reduces their reliability for storing data in environments affected by single ionizing particles striking sensitive nodes. One of the better known of these traditional D-latches is the so-called Static D-latch. Among the advantages of this latch are its low power consumption and simplicity. However, it is not immune to SEU and SET. The input and output signals of the Static D-latch and its schematic are shown in Figure 1.



(**a**) (**b**)

Figure 1. (**a**) Static D-latch schematic; (**b**) input and output signals of the Static D-latch.

As the reliability of data storage in the D-latch is of paramount importance, D-latches are typically classified in four types based on their immunity against SEU and SET:

(i). The first type of D-latch can tolerate SEU in some nodes, but they have some sensitive nodes against charge injection. The proposed D-latches in [13–15] are examples of this first type. It is important to mention that only some of this kind of D-latch can filter the SET by using a delay element, which is usually in the input lines [18–20].

(ii). The second type of D-latch is fully immune against the SEU, but they cannot filter input SET. In this family the output can also be in a high impedance state (HIS). An example of this type of D-latch is the Dual Interlocked storage CEll (DICE) latch [8].

(iii). The third type of D-latch can tolerate SEU in various nodes and avoids high impedance states, so high impedance at output cannot occur. However, they cannot filter the SET [21].

(iv). The fourth type of D-latch is not only fully immune against the SEU and SET, but also has a high impedance state at the output [22–24]. The high impedance state of the output can be solved by a keeper, which is a buffer that connects input and output nodes [22–24].

A summary of the different types of D-latch is shown in Table 1.

According to the four types of hardened D-latch, the so-called DICE belongs to the second type of hardened latch, being immune against SEU based on-cross the coupled inverter [8]. When SEU occurs in one node, the DICE structure can handle this SEU since it stores the input data in two different nodes. However, it cannot tolerate two simultaneous upsets to the two sensitive nodes and cannot filter SET pulses. Furthermore, the DICE presents high power consumption and delay in comparison to other hardened D-latches [25].

Table 1. Classification of different type of D-latch in regard to their soft-error immunity.

Type	Full Immune SEU	Filtering SET	HIS Insensitive	Examples
First	×	×	×	[14–16]
Second	✓	×	×	DICE [8], TMR [23]
Third	✓	✓	×	[21]
Fourth	✓	✓	✓	TPDICE-based [24], FERST [23], LSEH-1 [7]; LSEH-2 [1,7], This work

The Triple Modular Redundancy (TMR) latch presents a hardened design that makes it totally immune against upset, which fits the second type [23]. The TMR architecture can detect and correct SEU. However, it has a large number of transistors, which means that power consumption, area and delay penalty of this latch are far from ideal. In Ref. [23], a TMR D-latch including three Static D-latches with a voting circuit is discussed in regard to its performance and how it can be fully immune against upsets. In Ref. [23] a feedback redundant SEU/SET-tolerant latch (FERST) is also presented. FERST consists of two feedbacks and a delay element to avoid upset and there are two inverters as keepers to avoid a floating output node. Despite being fully immune against SEU, it consumes less power in comparison to TMR.

In Ref. [26], the authors proposed a latch design applying the hysteresis property of the Schmitt trigger inverter to increase immunity against SET; however, a Schmitt trigger based inverter with hysteresis property can reduce the speed of the D-latch. The feedback of this D-latch includes a C-element and two dynamic inverters. This feedback is active when CLK is "0" and holds the data in one node.

On the other hand, a Low-cost and Soft Error Hardened (LSEH) D-latch is proposed in [7], called LSEH-1, which has two separated paths to store the input data. These two paths have different delays to filter the SET of the input data. These two paths are connected to the C-element to trigger the output stage. LSEH-1 has three stages to store the input data at holding time. If the particle strikes in one stage, the two other stages can correct the output without any upsets. Furthermore, a so-called LSEH-2 is proposed in [7] having two latching stages in two different paths, which are connected to the C-element. Each input data, "0" and "1", passes through a different path to reach the output nodes, so SET pulses can be filtered in this D-latch. These LSEH-1 and LSEH-2 D-latches are benchmarked against the TMR in different parameters, such as delay, power consumption, temperature variation and process variation. This comparison shows better performance of these two LSEH-1 and LSEH-2 D-latches when compared to that of TMR [7].

In addition, full immunity against the SEU in any single node and filtering SET are the features of the D-latch proposed in [1]. This D-latch stores the data in two inverters with

positive feedbacks during holding time. Moreover, it can tolerate single event multiple upsets (SEMUS), along with other features, such as reliability and low-cost structure.

Finally, the Triple Path DICE (TPDICE)-based D-latch in [24] can tolerate SEU and filter SET. It can handle Single Event Double-Upset (SEDU), which means that this D-latch can tolerate different charge injections at multiple nodes. The structure of this D-latch consists of a TPDICE, a triple-input Muller C-element, a Schmitt trigger inverter, and a keeper in the output node. The TPDICE is triggered by the clock and the D-input. The inputs of the triple-input Muller C-element of this D-latch are provided by TPDICE. This structure of TPDICE with C-element can recover the data, with a single event upset in one node. Moreover, the TPDICE is applied in this D-latch to tolerate SEDU. The keeper is used in the output of TPDICE-based D-latch to avoid the high impedance state at the output. Besides, the embedded Schmitt trigger inverter on the propagation path can filter SET of the input.

It is worth mentioning that although this work focusses on SEU, hardened D-latches to tackle DNU (double node upset) [5,27], and TNU (triple node upset) [28] are also being investigated. However, those alternatives, out of the scope of this work, are also penalized by higher transistor count and power consumption.

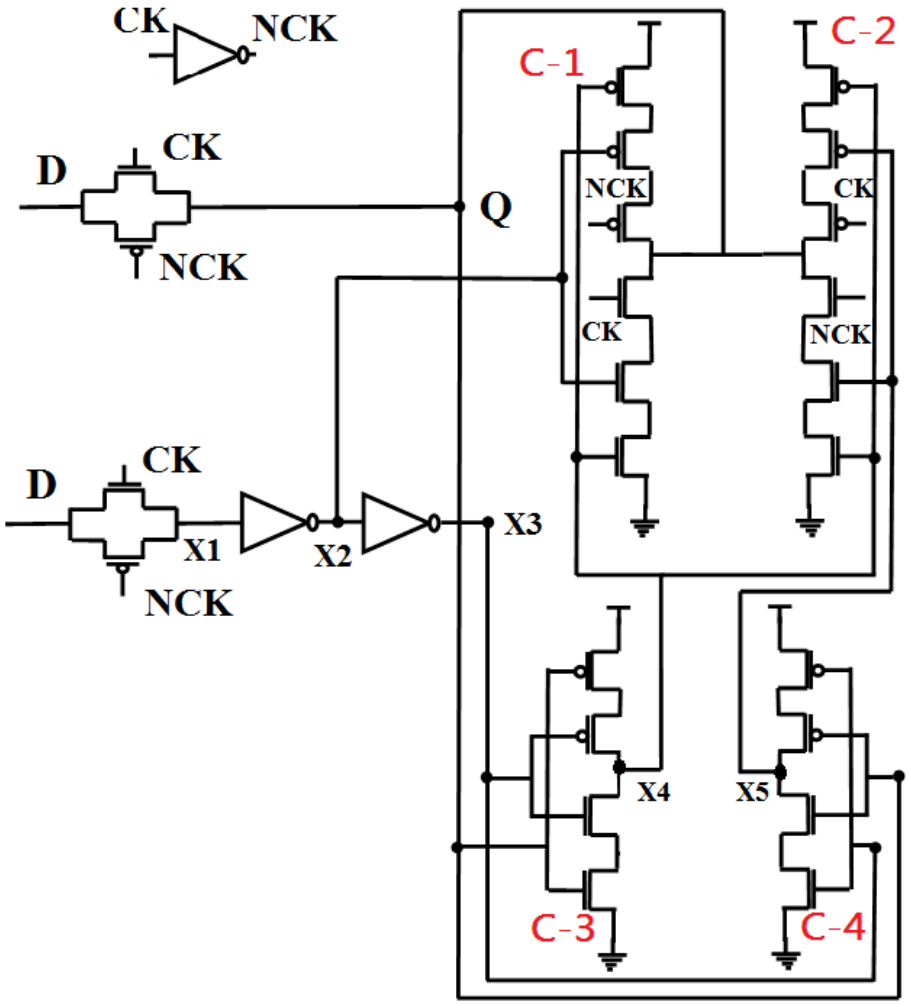
The proposed D-latch in this paper belongs to the fourth type and its immunity against SEU is better than that of the TPDICE-based D-latch [24], which is already considered fully immune, since the proposed design can tolerate a significant charge injection. The proposed D-latch also has lower transistor count and better performance in comparison to the TPDICE-based D-latch and other previous D-latches, regarding lower process variation, power consumption and delay. The next two sections are devoted to the presentation of the proposed D-latch and to analyzing these benefits in detail.

3. Proposed D-Latch

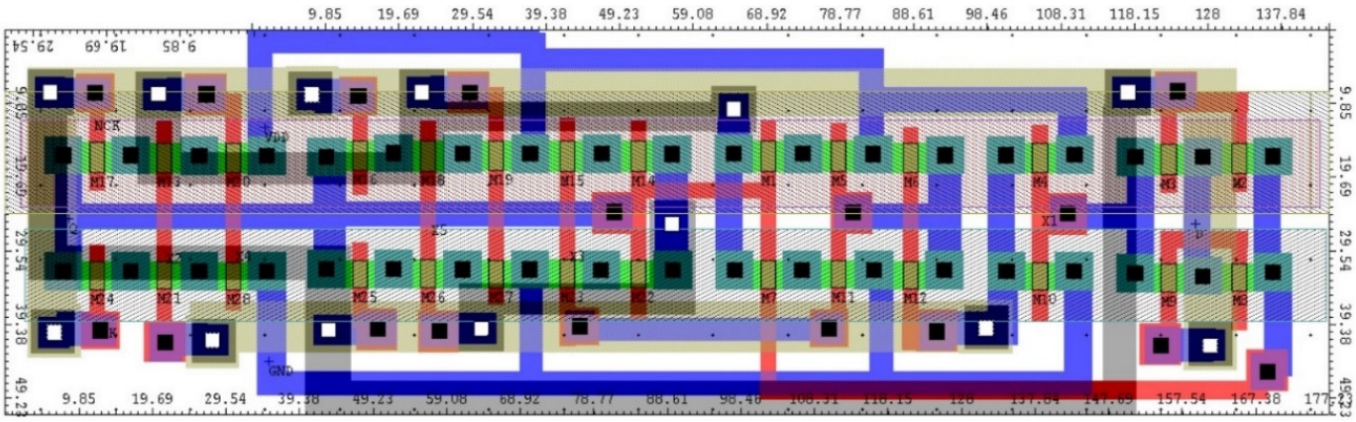
The schematic of the novel D-latch is shown in Figure 2a. The D-input passes through two paths; one path is integrated by one switch connecting the input to the output D-latch and the other path is formed by two inverters and one switch that is ON when CK = "1". The "X4" and "X2" nodes are connected to the first C-element to delete the SET of D data; this C-element increases the delay because it is ON when CK = "1". The third and fourth C-elements are used to store the output for the holding time. The second C-element of the feedback path is ON when CLK = "0" and provides the feedback in the hold mode. Storing the D-input in two different C-elements makes the structure reliable against SEU. The C-element with the same inputs works as an inverter; however, when the values of two or three inputs are not the same, the output of the C-element does not change. For example, when one SEU occurs in one of the two or three different paths, the output node does not change. The layout of the proposed D-latch is shown in Figure 2b. The equivalent schematics for each case (CK = "0" and CK = "1") are also shown in Figure 2c,d, respectively.

As mentioned above for the D-latch in [26], the feedback is applied to hold the data during the holding time. As the positive feedback of the D-latch increases the side effects of the process variations, the activation of the positive feedback only during holding time reduces power consumption and improves immunity against process variability in threshold voltage and W/L.

As can be seen, the proposed D-latch has extra circuitry for masking SET, which turns into area consumption and larger delay. However, when CK = "1", there are two paths to connect input to output: one path consists only of the transmission gate and the other comprises inverters and the C-1, and C-3 elements. Therefore, the second path introduces more delay and masks SET. However, in this design input and output are connected by the transmission gate, therefore the delay will be reduced and it is not directly affected by the inverters and the C-1, and C-3 elements. Similarly to other approaches of hardened D-latches [5,24], two sample paths of input are used for improved reliability. Furthermore, the proposed D-latch features two separated circuits in transmission mode and holding that, combined with clock-gating technique, lead to a very low power consumption.

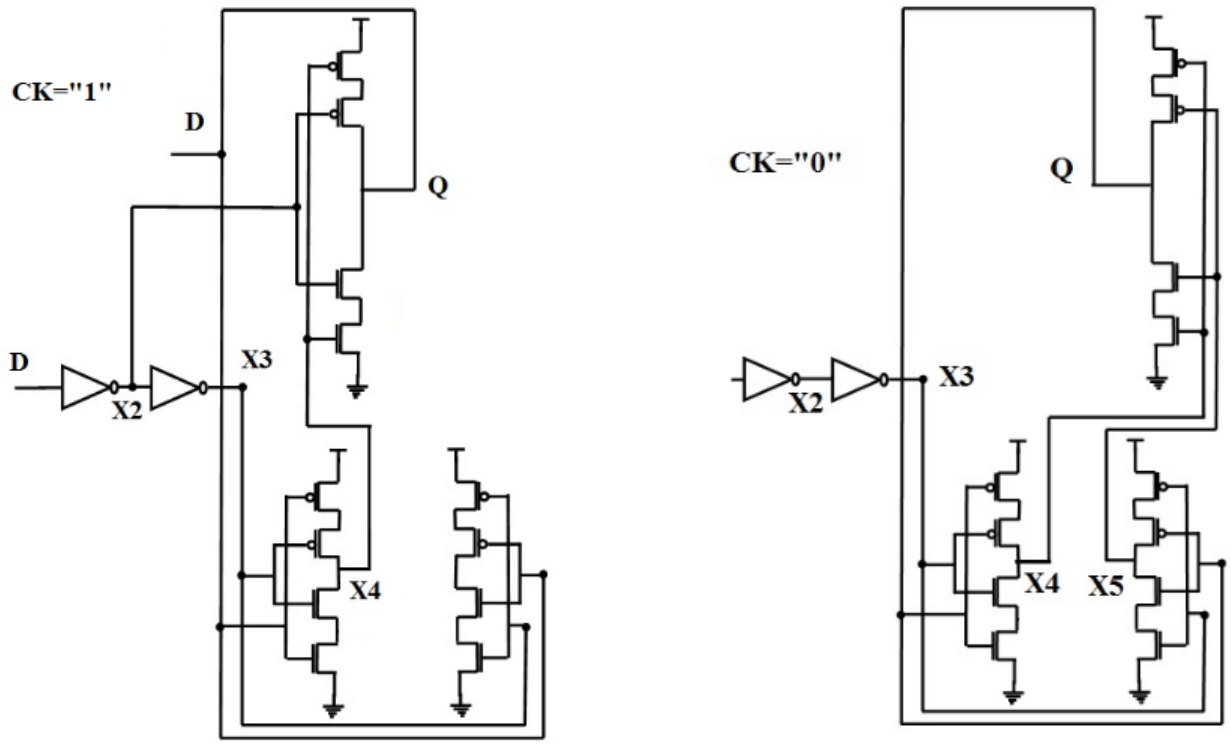


(**a**)



(**b**)

Figure 2. *Cont*.



(**c**) (**d**)

Figure 2. Proposed D-latch (**a**) schematic (**b**) layout (**c**) Equivalent schematic when CK = "1", (**d**) Equivalent schematic when CK = "0".

To investigate the SEU capability of the proposed D-latch, a number of SEUs are injected to various internal nodes. Then, the output signal is monitored to prove immunity against SEU at different nodes. The model of injected charge is based on an exponential current source [23]. The charge injection with different values is introduced during 0.3 ns and 0.9 V supply voltage at different internal nodes in reference CMOS technology at room temperature. Since different nodes can tolerate different values of charge injections, the maximum value of charge injection has been calculated for each specific node to produce voltage spikes slightly over the supply voltage and under zero volts [7,24], as shown in Figures 3–5 to test SEU immunity. The shape of the current source can be expressed mathematically [29]:

$$Q = \int_0^t \frac{Q_{total}}{\tau_f - \tau_r} \times \left(e^{-t/\tau_f} - e^{-t/\tau_r} \right) .dt \quad (1)$$

where Q_{total} is the total charge generated by the upset, τ_f is a constant coefficient of fall time and τ_r is a constant coefficient of rise time. Four different situations for each node are considered to test the proposed D-latch to observe the output. For example, the positive and negative charge injections are introduced to the "X1" node, when the output is "1" or "0" at the holding time. Thus, these four situations are tested for all internal nodes. Figure 3 shows the results of this test, when the output is "1" during the holding time with positive charge injections introduced in "X3" node and with negative charge injections introduced in "X2", "X4", and "X5" nodes. As can be observed, the output node "*Q*" is not affected by the SEU event in each one of these tests. For example, when the negative charge is injected in the "X5" node when "*Q*" is in the high logic value "1", the value after this charge injection maintains the valid value. In another test, the positive charge is injected to the "X3" node when the value of "*Q*" is "1" and, as can be seen, the value of "*Q*" does not change. This kind of test shows the immunity of the proposed D-latch against SEU. Moreover, for all of these tests (SEU immunity) for various nodes and for monitoring the

Q node, the high impedance state does not occur, which means this proposed D-latch is insensitive to high impedance.

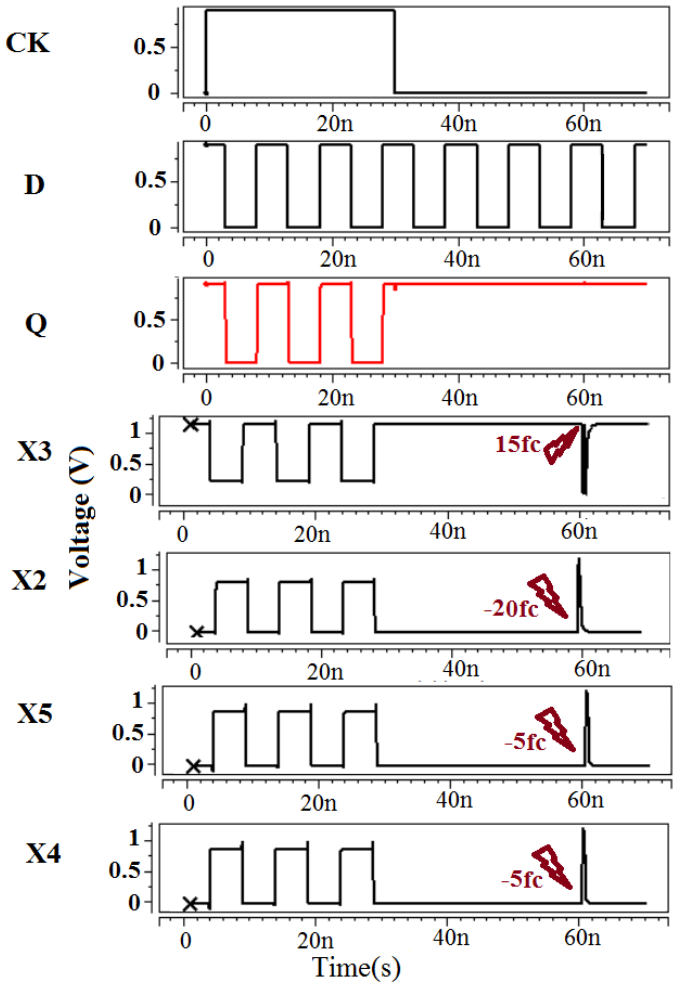


Figure 3. Test results for SEU injection to nodes when the output is "1" during the holding time; positive SEU injection to "X3" and negative SEU injection to "X2", "X4", and "X5" nodes.

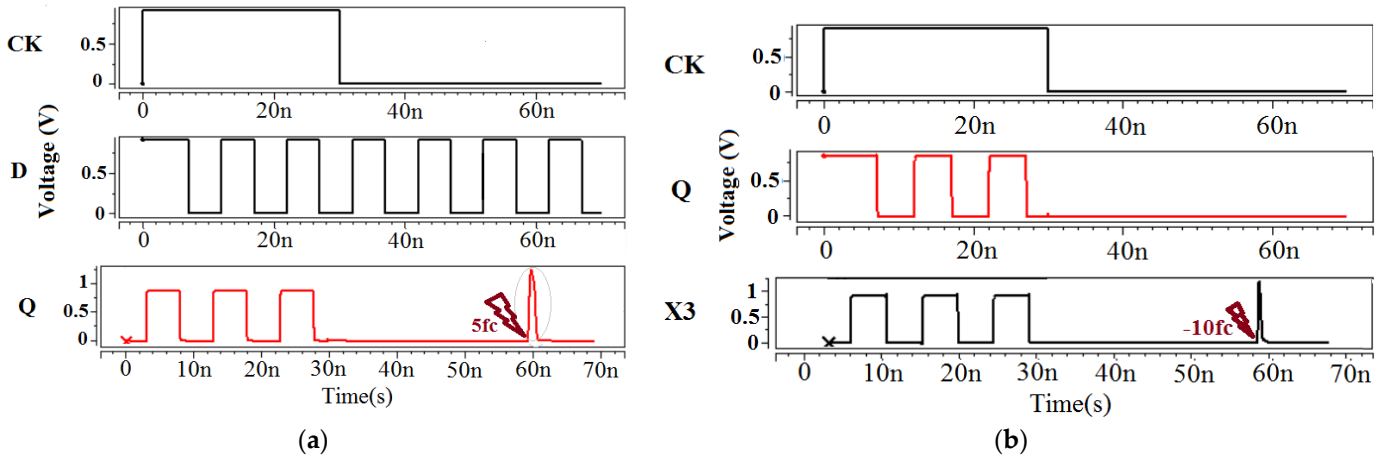


Figure 4. Test results for a positive and negative SEU injections to nodes when the output is "0" during the holding time: (**a**) to "*Q*" node; (**b**) to "X3" node.

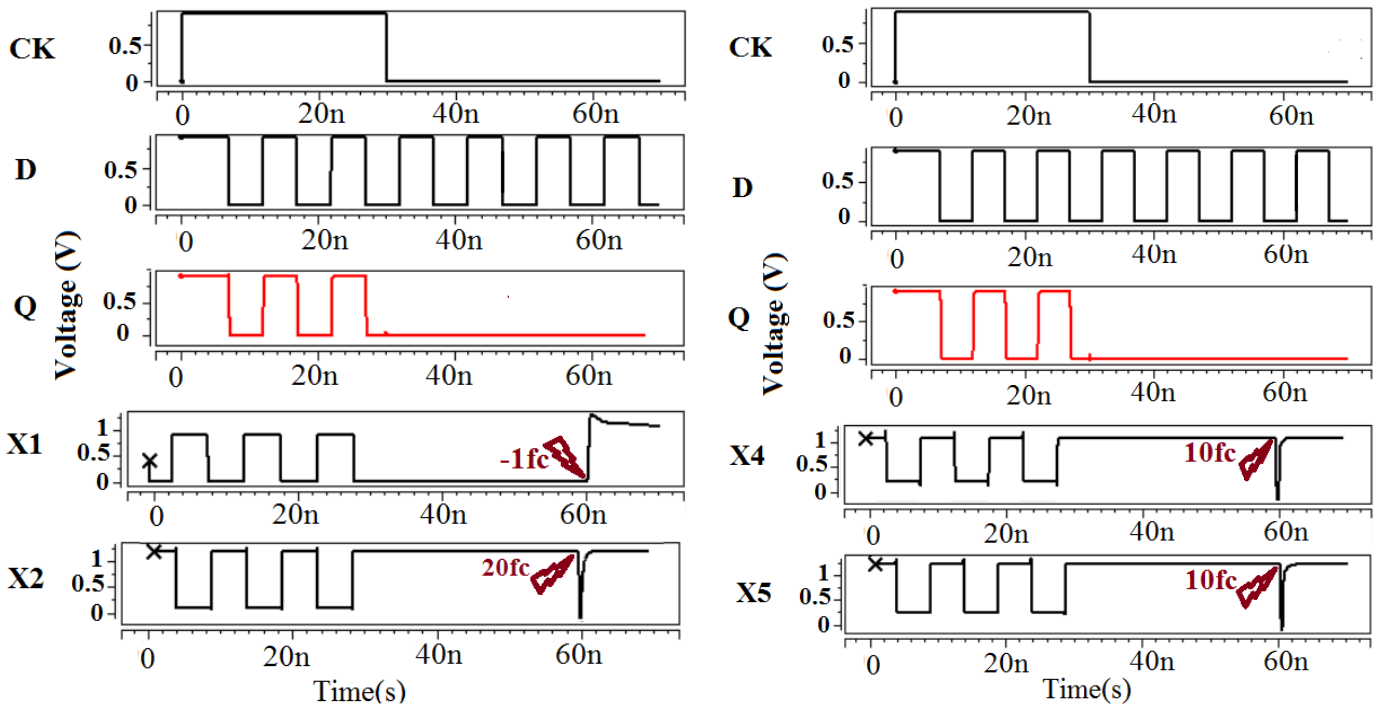


Figure 5. Test results when the output is "0" during the holding time: (**a**) negative and positive SEU injection to "X1" and "X2" nodes, respectively; (**b**) positive SEU injection to "X4" and "X5" nodes, respectively.

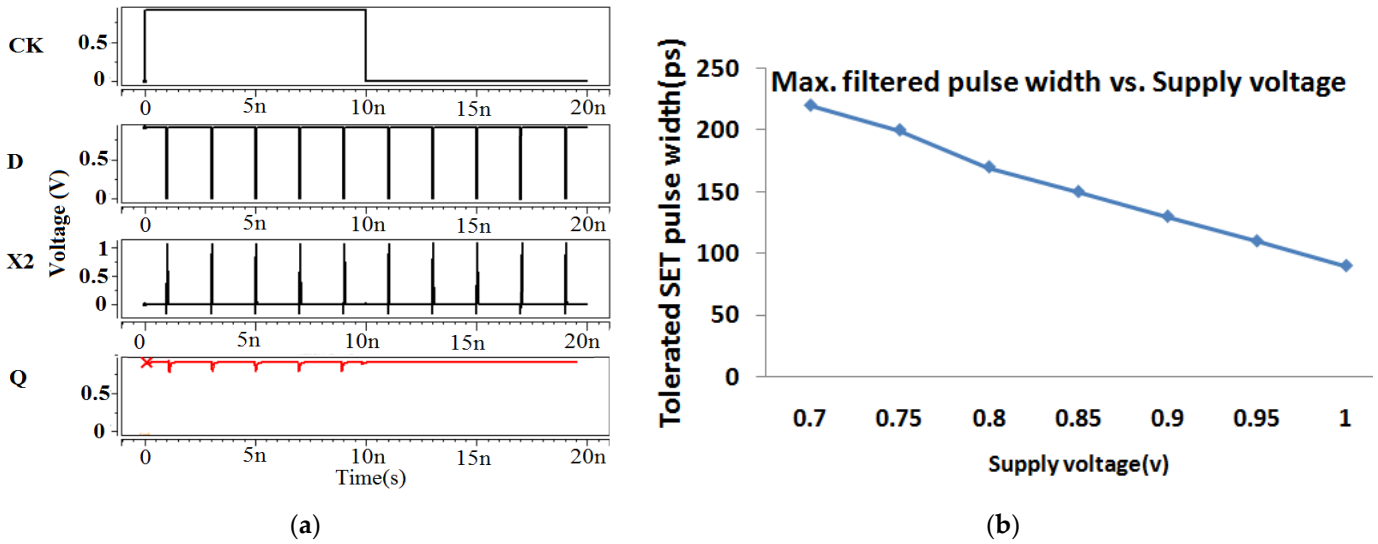
Figures 4 and 5 show test results of charge injection when the output is "0" during the holding time. In Figure 4, "*Q*" and "X3" nodes in the direct path are injected with charge. In Figure 4a, the positive charge injection is introduced to the "*Q*" node and, as shown, the proposed D-latch can tolerate this injection since the value of the output does not change after the upset. In Figure 4b, the test is performed for the "X3" node; in this case the output of the proposed D-latch does not change its value either.

Figure 5 shows results when the output is "0" and a negative injection is introduced in "X1" node and a positive injection is introduced in "X2", "X4", and "X5" nodes. As can be observed in this figure, in neither case would the output be affected.

The results of the study on critical charge injection in different nodes show that N1 can lose its data and valid logic state by small charge injections. N2 has more tolerance against charge injection. If more than 85 fC charge is injected to N2, it loses its value, but even this situation does not affect the Q value. The tolerance of N3, N4 is better, as they can tolerate up to 800 fC without disturbance in the data. Tolerance of N5 is lower since approximately 160 fC can be injected without losing the data. More importantly, for all these situations, the logic value of Q does not change. The previous figures for charge injections are very high, substantially over the usual value for testing SEU immunity, i.e., 20 fC [7].

A further test has been carried out to demonstrate the SET masking capability of the proposed D-latch. The result of this test is shown in Figure 6. The proposed design can mask undesirable pulses that are generated at the combinational digital circuits of previous D-latch stages. In the transparent mode, SET can be filtered by two simple inverters and the first and third C-elements comparing data of two paths, with differences in two inverters and two C-elements to produce delay. Those two inverters, and the first, and third C-elements in the direct path, increase the delay but provide the D-latch with one important feature: the filtering of the SET. SET has no impact on the output from the feedback path from "X4" and "X5" nodes, since the second C-element connecting these nodes is not ON at the transparent mode. In Figure 6a, the input signal is shown with a 100 ps SET pulse at 0.9 V supply voltage, illustrating how this SET pulse is filtered by the

proposed D-latch. It is worth mentioning that this masking depends on the supply voltage, the width of SET pulse, the delay and the temperature. The maximum width of SET pulses filtered by the proposed D-latch is shown as a function of supply voltages in Figure 6b. As can be seen, the maximum pulse width of SET decreases as the voltage supply increases (higher conductivity of the transistors) [7]. This dependency should be considered when it is necessary to suppress the SET pulse in sensitive applications [30–32].



(**a**) (**b**)

Figure 6. (**a**) SET pulse filtering capability of the proposed D-latch; (**b**) maximum pulse width of SET filtered by the proposed D-latch at various supply voltages.

It is worth mentioning that in [24], aiming at masking SET, a Schmitt Trigger Inverter is used in transparent mode; however, it has a large impact on delay because of the hysteresis property. LSEH-2 [7] also has two different paths for two different inputs, "0" and "1", which implies huge power consumption and area for filtering SET without double sampling, reducing reliability. These solutions are avoided in this work in order to achieve reasonable delay and accuracy. Thanks to the double sampling with different delays, SET is masked. The delay of the two paths (one transmission gate, and the inverters and C-elements) depends indirectly on the delay of inverters and C-1 and C-3 elements. The aspect ratio of PMOS and NMOS of the inverter and C-1 and C-3 element can also affect the delay. However, in our design they do not have a significant impact in comparison to the approach used for masking SET in other D-latches [7,23,24]; therefore, this effect has been neglected.

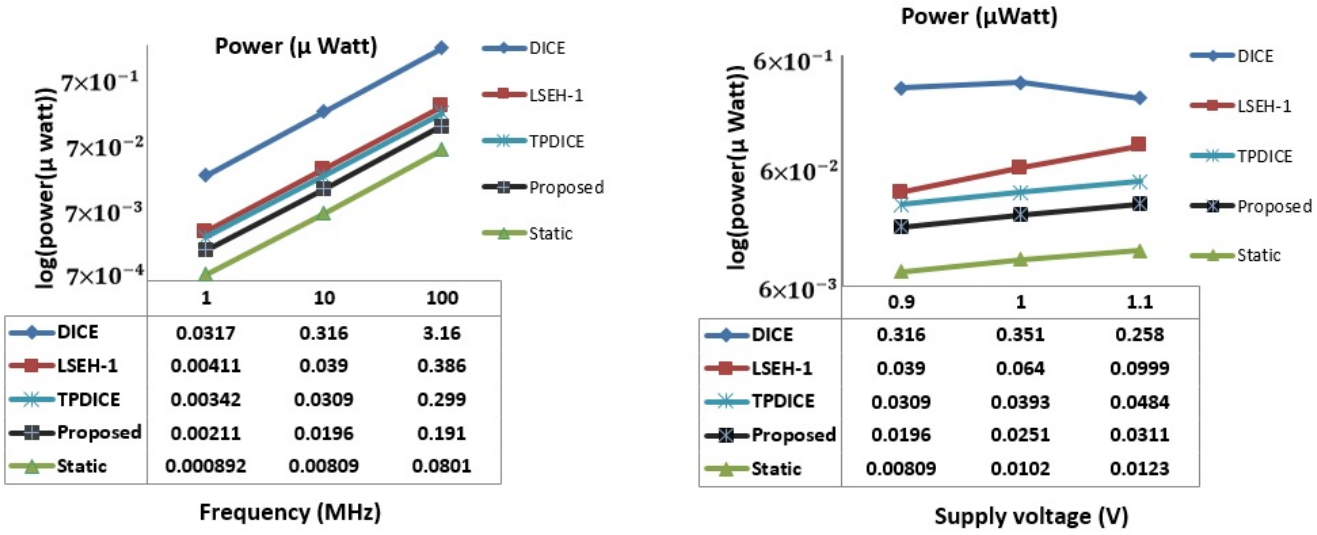
4. Latch Evaluation and Benchmarking

In this section the Static D-latch, DICE [8], TPDICE-based D-latch [24], LSEH-1 D-latch [7] and the proposed D-latch are simulated at three power supply voltages and three frequencies using HSPICE in the reference TSMC 65 nm CMOS technology. In these simulations, the aspect ratio of PMOS transistors is W/L = 130 nm/65 nm, while the aspect ratio of NMOS transistors is W/L = 120 nm/65 nm. Benchmarking of various important characteristics, such as power consumption, Power Delay Product (PDP), and (D-Q) delay is presented. All these D-latches are immune against SEU apart from the Static D-latch, which is chosen as a reference since it features less power consumption and propagation delay. Furthermore, the proposed D-latch, TPDICE-based D-latch, and LSEH-1 D-latches can filter SET pulses.

4.1. Power Consumption

As can be observed in Figure 7, the power consumption of the proposed D-latch is lower than those of all the other previous hardened D-latches (all of them designed to

achieve minimum footprint), DICE [8], TPDICE-based D-latch [24] and LSEH-1 latch [7]. They all have been simulated at different frequencies, from 1 MHz to 100 MHz. at 0.9 V power supply voltage (Figure 7a), and different supply voltages, ranging from 0.9 V to 1.1 V, at 10 MHz input frequency (Figure 7b). The power consumption of the proposed D-latch is higher than that of the Static D-latch, with an increment of 142%, but with the introduction of immunity against SEU and SET. The lower power consumption of the proposed D-latch in comparison to the other alternatives is attributed to the use of the clock-gating C-elements. There are two clock-gating C-elements in the proposed D-latch: the first one on the transparent path for filtering SET, which is ON whenever the CK = "1", and the second in the feedback path, which is ON whenever CK = "0". Moreover, the proposed D-latch has separate stages for transparent mode and holding time, which further reduces power consumption and delay. The delay decreases because in transparent mode the output can be set without passing from the saving nodes, which are used for holding time, while power consumption is reduced since, by separating two modes, it is possible to use clock gating-based C-elements.



	1	10	100
DICE	0.0317	0.316	3.16
LSEH-1	0.00411	0.039	0.386
TPDICE	0.00342	0.0309	0.299
Proposed	0.00211	0.0196	0.191
Static	0.000892	0.00809	0.0801

	0.9	1	1.1
DICE	0.316	0.351	0.258
LSEH-1	0.039	0.064	0.0999
TPDICE	0.0309	0.0393	0.0484
Proposed	0.0196	0.0251	0.0311
Static	0.00809	0.0102	0.0123

(**a**) (**b**)

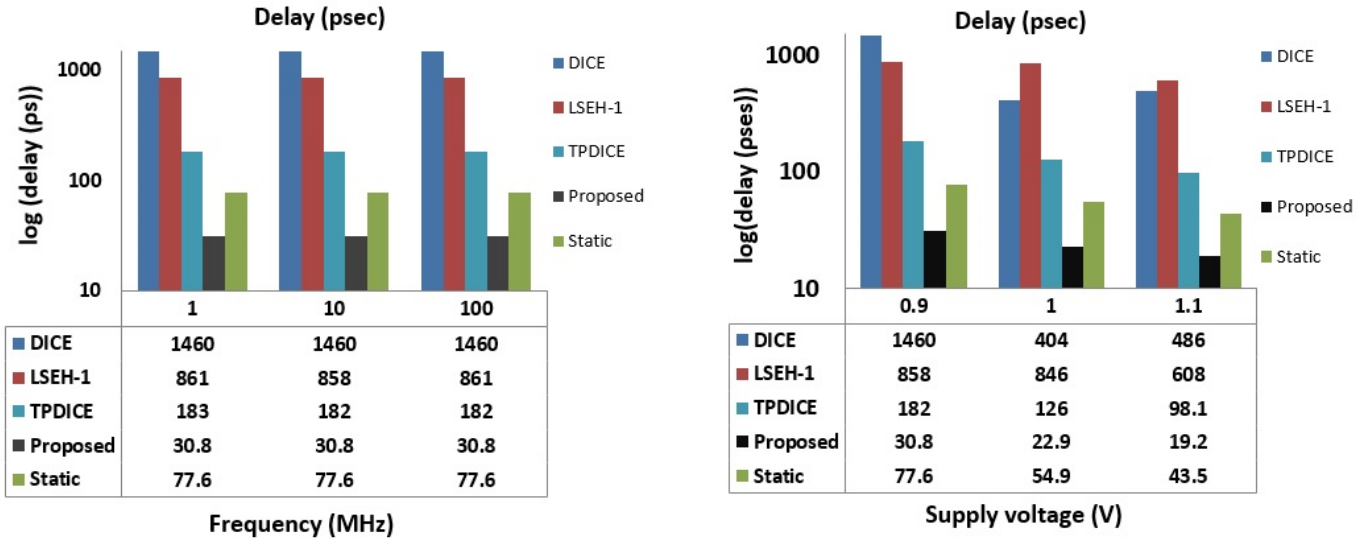
Figure 7. Power consumption of various D-latches: (**a**) at three frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (**b**) at three supply voltages and 10 MHz input frequency.

4.2. Delay

The delay is one of the most important parameters of D-latches. This decreases with increasing supply voltages due to the higher conductivity of the channel of the transistors, as shown in Figure 8. According to the results, the improvement of the proposed D-latch delay in comparison to the Static D-latch is up to 60%.

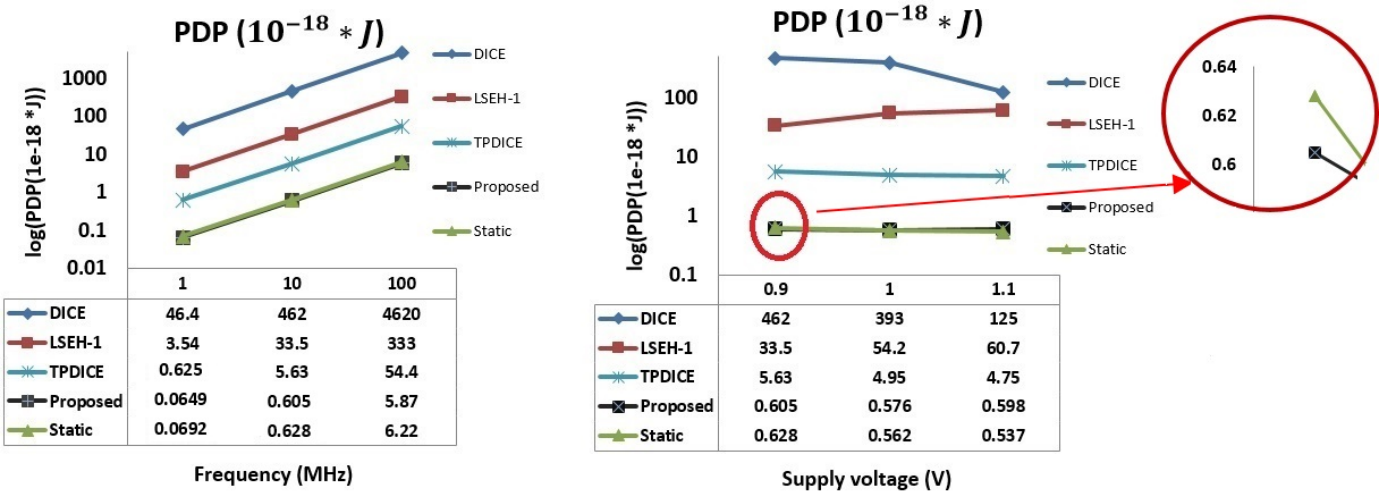
4.3. PDP

Furthermore, as PDP is a figure of merit showing the total performance of D-latches and, in particular, commonly used to evaluate hardened D-latches [7,30], a PDP comparison of the proposed and previous D-latches is shown in Figure 9. As can be seen, the PDP of the proposed D-latch is even slightly better than that of the Static D-latch, with a 3.67% improvement. This improvement is achieved by reducing delay, as PDP is power consumption multiplied by delay.



(**a**) (**b**)

Figure 8. Delay of various D-latches: (**a**) at various frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (**b**) at three supply voltages and 10 MHz input frequency.



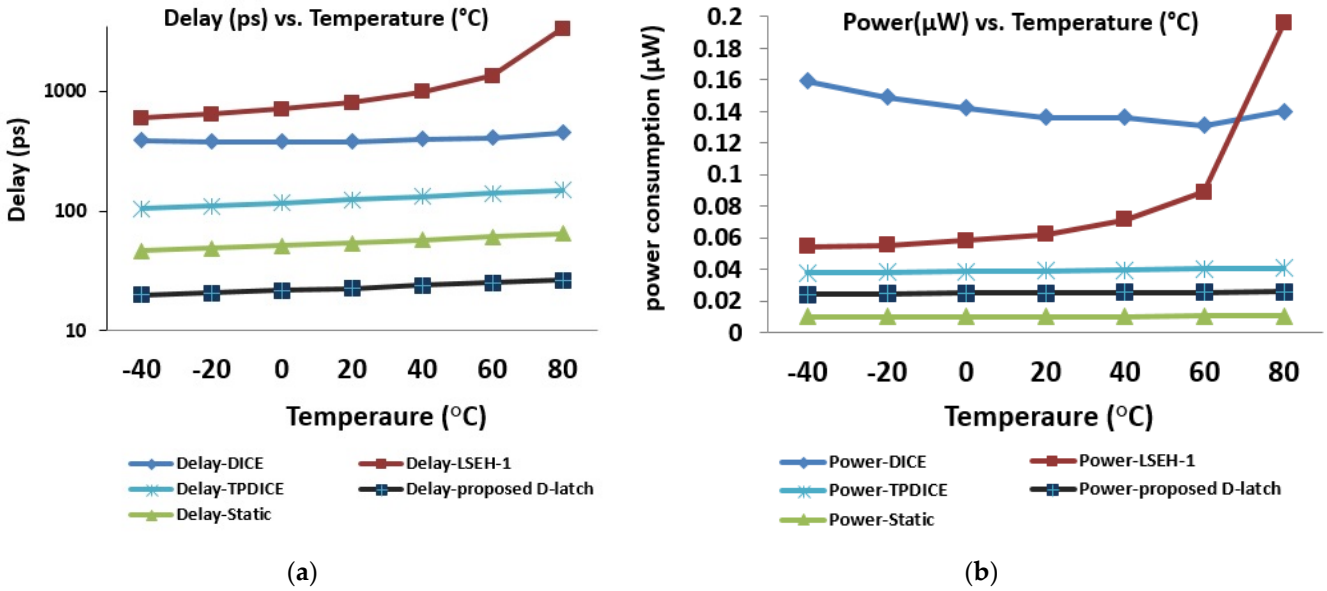
(**a**) (**b**)

Figure 9. PDP of various D-latches: (**a**) at various frequencies from 1 MHz to 100 MHz and 0.9 V power supply voltage; (**b**) at three supply voltages and 10 MHz input frequency.

4.4. Temperature Variation

One of the most important operational parameters considerably affecting the D-latch performance is temperature, which may change dramatically under different conditions. To show this impact, the DICE, TPDICE-based D-latch, Static, LSEH-1, and proposed D-latches are simulated at different temperatures ranging from −40 °C to 80 °C (industrial range) with 10 °C steps.

As expected, raising the temperature increases the delay (above 30 °C for DICE) due to the lower electrical conductivity (lower carrier's mobility) and increases the power consumption (above 60 °C for DICE), as high temperature increases current leakage [33]. However, the temperature effect on the proposed D-latch is lower than in other D-latches, such as LSEH-1, DICE, and TPDICE-based D-latches, as deduced from Figure 10 (a comparative study in terms of a temperature coefficient has been included in Appendix A).



(**a**) (**b**)

Figure 10. Temperature variation effect on: (**a**) delay vs. temperature; (**b**) power consumption vs. temperature.

4.5. Area Usage

Another important benchmarking parameter is area usage; this parameter can be evaluated from the device layout. Table 2 shows the area comparison between the proposed D-latch and previous D-latches designed with Tanner L-EDIT [34] (all designs targeting minimum area). As can be observed, the proposed D-latch footprint matches that of DICE with the advantage of presenting better immunity and power consumption parameters.

Table 2. Comparative area of D-latches.

D-Latch	Proposed D-Latch	Static	TPDICE [19]	DICE [8]	LSEH-1 [7]
Area $(\mu m)^2$	7.959	3.0816	18.04	7.944	12.21

4.6. Process Variations

Finally, process variability, such as variation of transistor aspect ratio (W/L) or threshold voltage are analyzed. Monte Carlo simulations constitute a helpful tool to assess how the delay and power consumption are affected by these variations. A Gaussian distribution has been considered to model (W/L) and threshold voltage variability. The maximum deviations from the original (W/L) values of transistors and threshold voltages are set from 2% to 16%, which is the probable range of change normally used for comparison in this kind of study [1,7,27]. For each maximum deviation, 20 simulations are carried out to study the effect of (W/L) and threshold voltage variability on the delay and power consumption. Figure 11 shows the delay as the result of (W/L) transistor variability. In Figure 11a, the delay changes of the proposed D-latch as a result of (W/L) transistor variations are shown. It can be seen that the results have approximately the same delay variation as that of the TPDICE-based D-latch (Figure 11c), and the Static D-latch (Figure 11b), while it is much better than that of DICE (Figure 11d) and LSEH-1 D-latches (Figure 11e). The results are normalized to the delay of the original D-latch without any process variation. This normalization helps better visualize the effect of (W/L) transistor variations on delay. Figure 11f clearly shows the minimum variations of delays for the proposed D-latch when compared to other D-latches in maximum deviation.

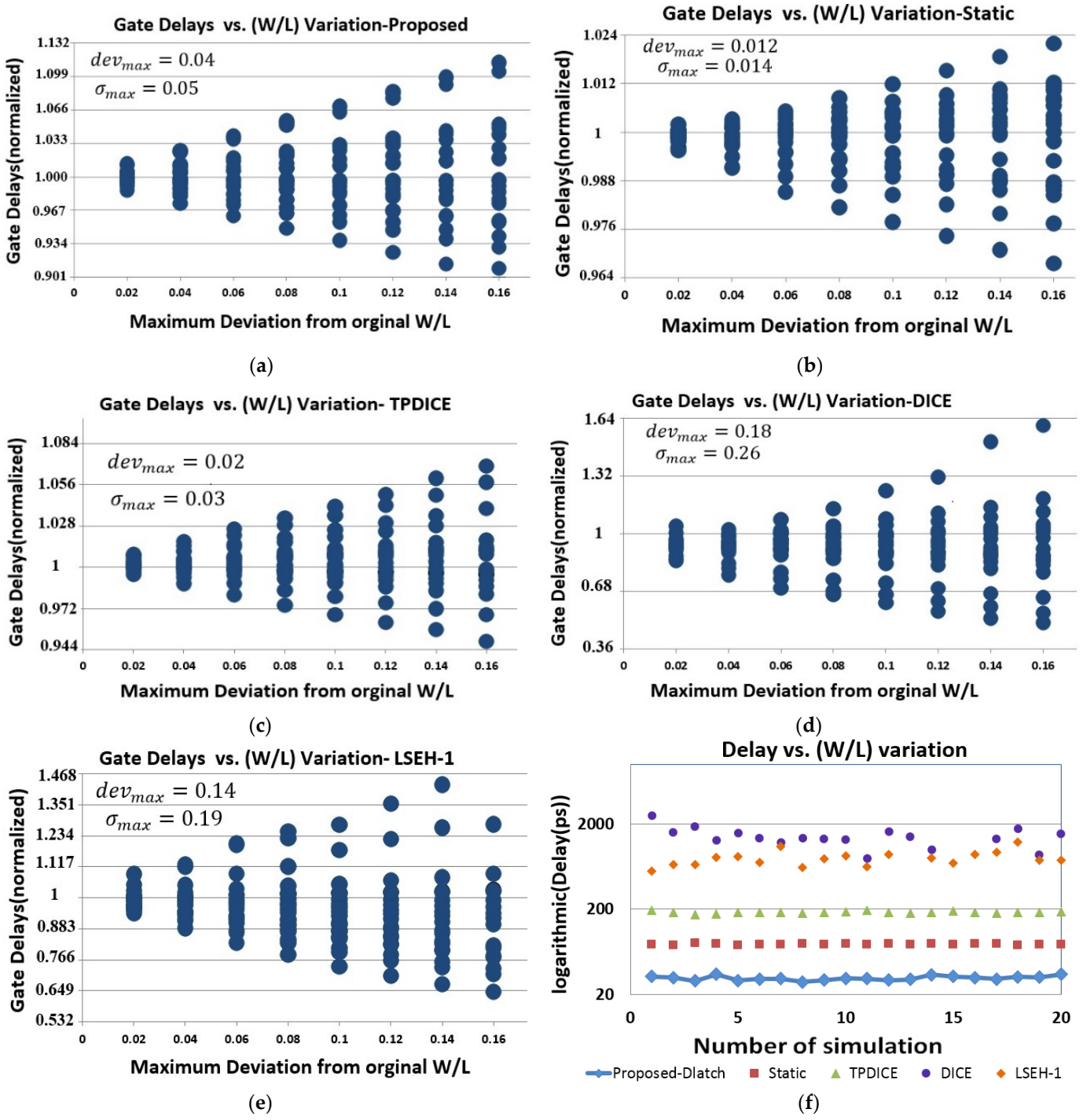


Figure 11. (W/L) variation effect on D-latch delay: (**a**) proposed D-latch; (**b**) Static D-latch (**c**) TPDICE-based D-latch (**d**) DICE (**e**) LSEH-1 latch (**f**) delay of D-latches with maximum deviation, 0.16, from original W/L.

In Figure 12, the effect of (W/L) variability on the power consumption is shown. As can be seen by varying (W/L) of the transistors by 2–16% deviations from the original value, the power consumption of the proposed D-latch is affected similarly to that of the TPDICE-based D-latch and it is much better than that of the Static-latch, DICE, and LSH-1 latches.

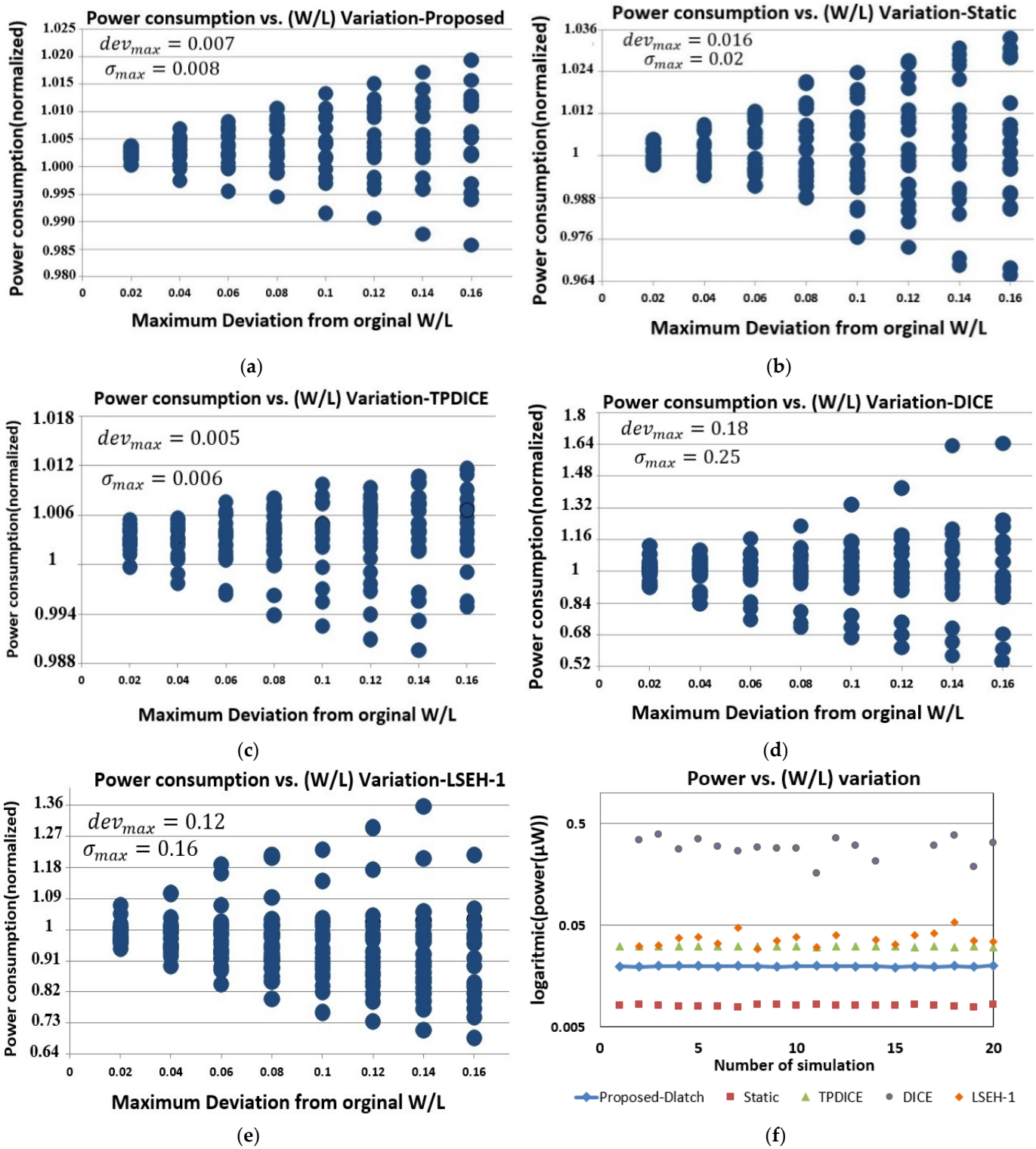


Figure 12. (W/L) variation effect on power consumption: (**a**) proposed D-latch (**b**) Static D-latch (**c**) TPDICE-based D-latch (**d**) DICE (**e**) LSEH-1 latch (**f**) power consumption of D-latches with maximum deviation, 0.16, from original W/L value.

The maximum variance (σ_{max}) and standard deviation (dev_{max}) are calculated for the delay and power consumption of the proposed, Static, and TPDICE-based D-latch, DICE, and LSEH-1 D-latches. These variance and standard deviation measurements are for the maximum deviation from the original (W/L) transistors, which is 16%. Maximum variance and deviation are shown in the insert of the plot for each D-latch in Figures 11–14. The impact of (W/L) variations on the power consumption of the proposed D-latch is low,

but the delay deviation of the proposed D-latch is more than that of the Static D-latch. The delay standard deviations of the proposed D-latch, Static, and TPDICE-based D-latch, DICE, and LSEH-1 are 0.04, 0.012, 0.02, 0.18 and 0.14, respectively. The maximum variance of the delay of the proposed D-latch, Static, TPDICE-based D-latch, DICE, and LSEH-1 are 0.05, 0.014, 0.03, 0.26, and 0.19, respectively. The standard deviation improvement of the (W/L) transistor variability on power consumption of the proposed D-latch, compared with the Static D-latch as reference, is 56.2%. In general, process variations have a negative effect on power consumption and delay.

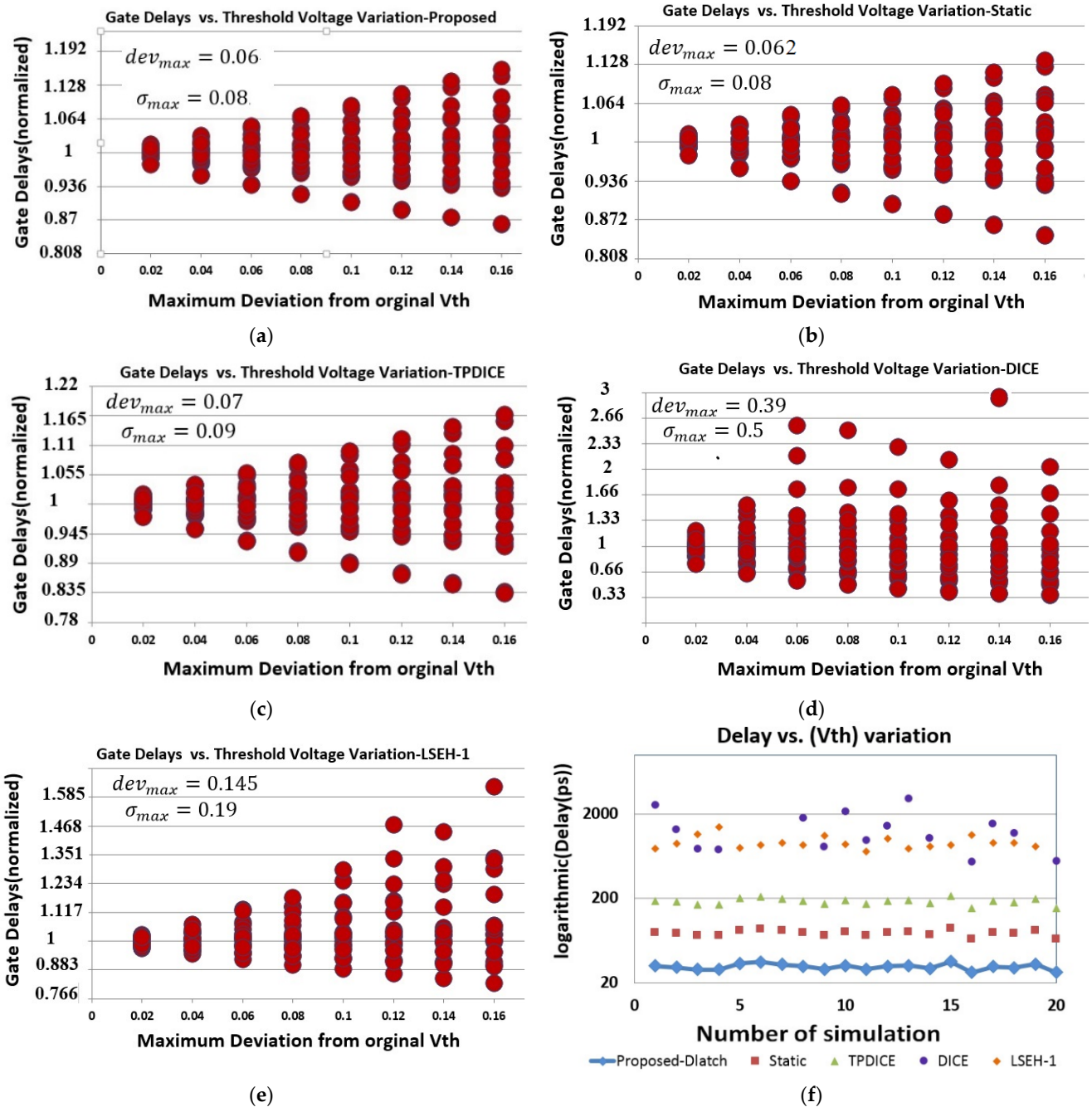


Figure 13. Threshold voltage variation effect on D-latch delay: (**a**) proposed D-latch (**b**) Static D-latch (**c**) TPDICE-based D-latch (**d**) DICE (**e**) LSEH-1 latch (**f**) delay of D-latches with maximum deviation, 0.16, from original threshold voltage.

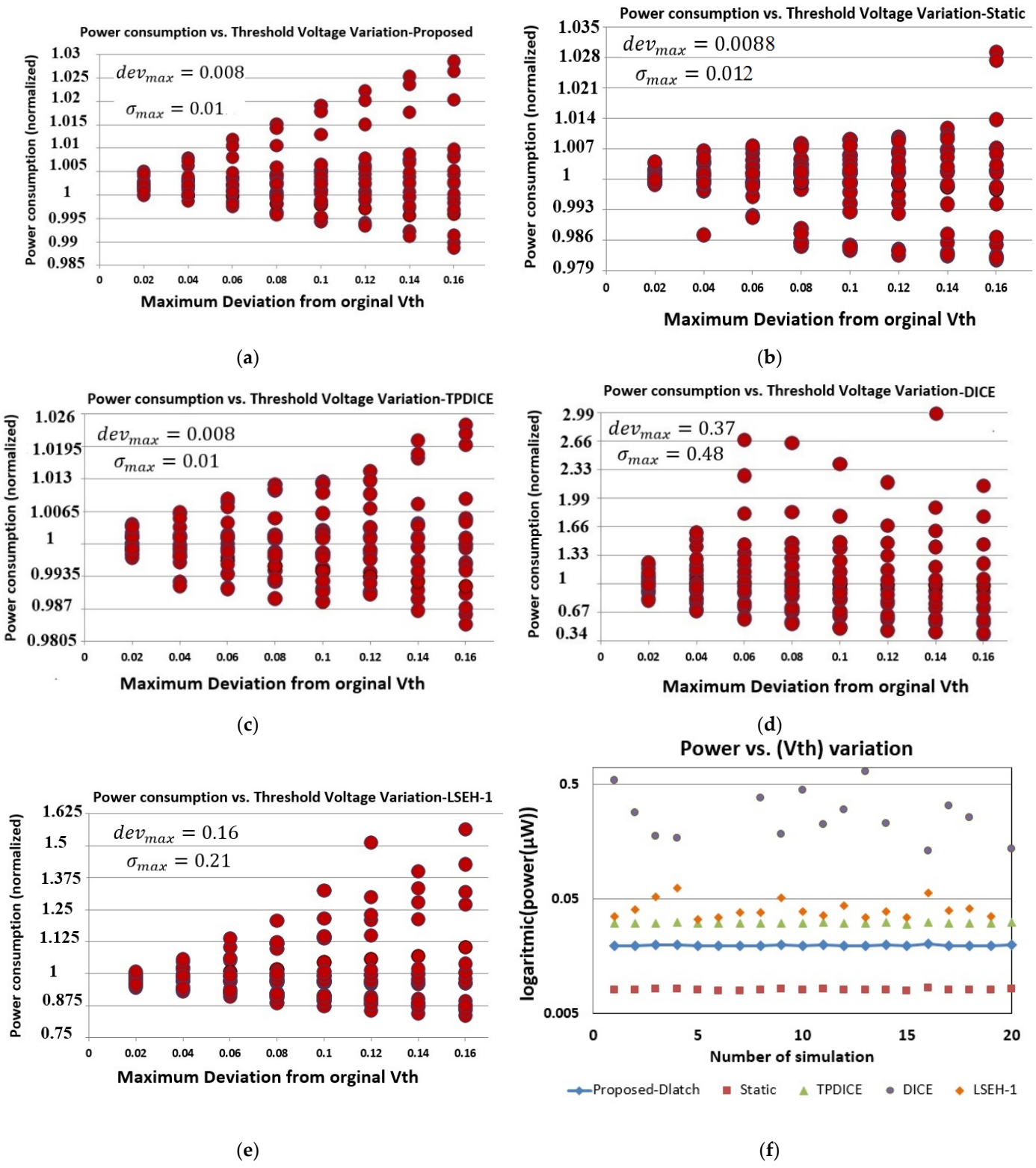


Figure 14. Threshold voltage variation effect on power consumption: (**a**) proposed D-latch (**b**) Static D-latch (**c**) TPDICE-based D-latch (**d**) DICE (**e**) LSEH-1 (**f**) power consumption of D-latches with maximum deviation, 0.16, from original threshold voltage.

The gate delay and power consumption variation versus threshold voltages are shown in Figures 13 and 14, respectively. The threshold voltages of the different transistors are changed by 2–16% of their original values. As can be seen in Figures 13 and 14, the delay (D-Q) and power consumption variations of the proposed D-latch are lower in comparison to those of Static, TPDICE-based D-latch, DICE, and LSEH-1 D-latches. This fact demonstrates a superior reliability of the proposed D-latch as compared to other alternatives. These lower variations of power consumption and delay for the proposed D-latch can be attributed to the lower effect of the positive feedback loop in this design (positive feedback yields huge process variation): in the proposed D-latch positive feedbacks are only activated during holding time and their paths are separated from the transparent path. These feedbacks enter a clock-gating C-element, which may reduce the effect of the positive feedback loop.

The impact of threshold voltage variations on the power consumption of the proposed D-latch is negligible. The delay standard deviations of the proposed D-latch, Static, and TPDICE-based D-latch, DICE, and LSEH-1 are 0.06, 0.062, 0.07, 0.39 and 0.145, respectively. The maximum threshold voltage variance of the delay of the proposed D-latch, Static, TPDICE-based D-latch, DICE, and LSEH-1 are 0.08, 0.08, 0.09, 0.5, and 0.19, respectively. The standard deviation improvement of threshold voltage transistors variability on the delay of the proposed D-latch, compared with that of a Static D-latch set as reference, is 3.2% and improvement for power consumption is 9.1%. In summary, threshold voltage variations have low effect on power consumption and delay on the proposed D-latch in comparison to the other hardened alternatives considered in this study.

5. Conclusions

In this contribution, a low-cost hardened D-latch is proposed with full immunity against SET and SEU. Additionally, it features a lower power consumption and delay in comparison to those of previous hardened D-latches alternatives, such as DICE, TPDICE-based D-latch, and LSEH-1. For benchmarking, the performance of the Static D-latch is set as reference, and the proposed D-latch provides the closest values in terms of delay and power consumption. The delay and PDP of the proposed D-latch improve 60.3% and 3.67%, respectively, in comparison to those of the reference latch at the expense of a power consumption increase (142%) with regards to the reference latch. A comparison between Static, DICE, TPDICE-based D-latch, LSEH-1, and the proposed D-latches reveals the superior performance of the proposed D-latch and a lesser impact from temperature and process variability in terms of transistor threshold voltage and aspect ratio. The standard deviation improvement of threshold voltage transistor variability impact on the delay is improved by 3.2%, whereas its impact on the power consumption is improved by 9.1%. Furthermore, it has been shown that the standard deviation improvement of (W/L) transistor variability on the power consumption is 56.2%. Finally, the additional benefits do not come at the expense of a significant increase in cost (PDP, power consumption, area, delay) in comparison to the other hardened alternatives.

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Appendix A

To show how the temperature effects on delay, the following coefficient can be defined.

$$\alpha = \frac{\left(delay - delay_{ref}\right)}{\left(T - T_{ref}\right)delay_{ref}} \quad \text{(A1)}$$

In Equation (A1), reference temperature is 20 °C and α is the delay coefficient by temperature, which is calculated for different D-latches and the proposed D-latch in Table A1. As can be seen, the delay coefficient of the proposed D-latch is lower than those of the other alternatives.

Table A1. Comparative delay coefficient by temperature of D-latches.

D-Latch	Proposed	Static	TPDICE	DICE	LSEH-1 [7]
Delay coefficient by temperature	0.0028	0.0032	0.0034	0.0031	0.053

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