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THE DEVELOPMENT OF NEW BACKSIDE DECAPSUALTION TECHNIQUE TO INVESTIGATE INTEGRATED CIRCUIT FAILURE IN THE AUTOMOTIVE APPLICATION ENVIRONMENT

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ABSTRACT

The semiconductor industry is the aggregate collection of companies engaged in the design and fabrication of semiconductor devices. To establish the good company of semiconductor, the development of failure analysis organization must be made. Failure analysis is the process of collecting and analyzing data to determine the cause of a failure. It is an important discipline in many branches of manufacturing industry, such as the electronics industry, where it is a vital tool used in the development of new products and for the improvement of existing products. The failure analysis process relies on collecting failed components for subsequent examination of the cause or causes of failure using a wide array of methods, especially microscopy and spectroscopy. This project will discuss about the failure analysis step and procedure. The aim of this project is to design a new backside decapsulation method in order to improve the failure analysis processing time and root cause finding. This project contains of several parts which are electrical analysis, IC decapsulation with chemical analysis and fault isolation step. Comparison between the old method and new method result has been made and the effectiveness of the sample has been measured by performing analysis on 20 samples. The simulation and measurement results show 85.5% of improvement in term of failure analysis processing time by comparing with old method. In term of root cause identification, the root cause has been successfully identify for all samples which were related to EOS, ESD and Wafer Fabrication related failure classified as Poly and GOX. Based on this result, the success rate for 20 samples by using new backside decapsulation technique is 100%.

ABSTRAK

Industri semikonduktor adalah koleksi agregat syarikat yang terlibat dalam reka bentuk dan pembuatan peranti semikonduktor. Untuk menubuhkan syarikat semikonduktor yang lengkap, pembangunan organisasi analisis kegagalan mesti dibuat. Analisis kegagalan adalah proses mengumpul dan menganalisis data bagi menentukan punca kegagalan. Ia adalah satu disiplin penting dalam pelbagai cabang industri pembuatan seperti industri elektronik, di mana ia adalah kaedah penting yang digunakan dalam pembangunan produk baru dan bagi penambahbaikan produk sedia ada. Proses analisis kegagalan bergantung kepada pengumpulan komponen untuk pemeriksaan seterusnya mencari punca atau sebab-sebab kegagalan menggunakan pelbagai kaedah, terutama mikroskop dan spektroskopi. Projek ini akan membincangkan mengenai langkah analisis kegagalan dan prosedur. Tujuan projek ini adalah untuk merekabentuk satu kaedah bahagian belakang pembukaan baru dalam usaha untuk meningkatkan masa pemprosesan analisis kegagalan dan punca kegagalan. Projek ini mengandungi beberapa bahagian iaitu analisis elektrik, pembukaan IC dengan analisis kimia dan langkah mencari punca kegagalab. Keputusan simulasi dan pengukuran menunjukkan peningkatan dalam tempoh masa analisis pemprosesan kegagalan. Perbandingan antara kaedah lama dan kaedah baru telah dibuat dan keberkesanan sampel telah diukur dengan melakukan analisis pada dua puluh sampel. Keputusan simulasi dan pengukuran menunjukkan 85.5 % daripada peningkatan dari segi kegagalan masa pemprosesan analisis dengan membandingkan dengan kaedah lama. Dari segi punca pengenalan, punca telah berjaya mengenal pasti untuk semua sampel yang berkaitan dengan EOS, ESD dan Wafer kegagalan berkaitan fabrikasi diklasifikasikan sebagai Poly dan GOX . Berdasarkan keputusan ini, kadar kejayaan untuk 20 sampel dengan menggunakan teknik bahagian belakang decapsulation adalah 100 %.

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LIST OF SYMBOL AND ABBREVIATIONS

-	Integrated Ciccuit
-	Scanning Acoustic Microscopy
-	Scanning Electron Microscopy
-	Nitric Acid
-	Sulfuric Acid
-	Emission Microscopy
-	Optical Beam Induced Resistance
	Change
-	Serial Peripheral Interface
-	Copper
	-

CHAPTER 1

INTRODUCTION

1.1 Background of Study

Semiconductors are the foundation of modern electronics. The modern understanding of the properties of a semiconductor relies on quantum physics to explain the movement of electrons and holes in a crystal lattice. The unique arrangement of the crystal lattice makes silicon and germanium the most commonly used elements in the preparation of semiconducting materials. An increased knowledge of semiconductor materials and fabrication processes has made possible continuing increases in the complexity and speed of microprocessors and memory devices. Semiconductor devices can display a range of useful properties such as passing current more easily in one direction than the other, showing variable resistance, and sensitivity to light or heat. Because the electrical properties of a semiconductor material can be modified by controlled addition of impurities or by the application of electrical fields or light, devices made from semiconductors can be used for amplification, switching, and energy conversion. Almost all of today's technology involves the use of semiconductors, with the most important aspect being the integrated circuit (IC). Some examples of devices that contain integrated circuits include laptops, scanners, cell-phones and many more. Generally, the ICs are produced from various semiconductor companies around the world such is Intel, AMD, STMicroelectronics, NXP Semiconductor and etc. The semiconductor company has produced a smart and intelligent integrated circuit to be used in motor control application, computing application, medical application, industrial application and automotive application.

The automotive application is a wide range of companies and organizations involved in the design development, manufacturing, marketing and selling of motor vehicles. It is one of the world's most important economic sectors by revenue. Nowaday, the invention of the automotive device is parallel with the expension of the IC. Most of the automotive device is controlled by the IC for every single application.

Automotive application environment is referring to the application inside the transportation system such as car's system. It is working for transmission, engine injection, battery stabilizer, window controller, Anti-lock Braking System (ABS), alarm system, brake system module, airbag, mobile system and etc. These are the new technology build inside the car for the purpose of facilitating and safety. The new technology invented has produced a smart car which provided comfortable and user friendly car. In term of safety, it plays a very important part because it is correlated to human life. Cars nowadays are equipped with various safety device such sensors, ABS, airbag and etc. The failure of the safety device application will turn to huge damage and fatality.

The failure on safety device application is a life matter. It is very important to avoid any single IC failure from being happened during car application. If it happened, failure analysis must be done on the specific IC to find the root cause of the failure to avoid the same tragedy happen. Failure analysis must be done the failing IC. Failure analysis is the process of collecting and analyzing data to determine the cause of a failure. It is an important discipline in many branches of manufacturing industry, such as the electronics and semiconductor industry, where it is a vital tool used in the development of new products and for the improvement of existing products. The failure analysis process relies on collecting failed components for subsequent examination of the cause or causes of failure using a wide array of methods. It is related to electric measurement, and by physical and chemical analysis techniques if necessary, to confirm the reported failure and clarify the failure mode or mechanism.

Generally for IC failure, there are three major defects the failure can be related to which are Electrical Over Stress (EOS) / Electrostatic Discharge (ESD), Wafer Fabrication failure and assembly related failure. For all failure cases, failure analysis must be performed correctly to assure the failure mechanism is preserved. Effective root cause analysis of part failures is required to assure proper corrective action can be implemented to prevent reoccurrence. Determination of root cause is also important for high reliability systems such as brake, engine and airbag system where failures are critical, as well as consumer products where the cost of a single failure mode can be replicated multiple times.

1.2 Problem Statement

The invention of automotive device integrated with smart IC has their advantages and disadvantages. The advantages are, it makes the driving moment enjoy full without giving distraction on driver's focus and it increase the comfort while driving. A part of that, it also provides the safety concern for car user. In term of disadvantages with the new technology, since they are invented with the advanced IC, therefore there are possibilities of the failure to be happened on IC itself which is a bit sensitive for any changes of voltage and current with dynamic atmosphere condition. The failure can be related the quality and reliability of the device, human handling mistake during the electrical connection and disconnection and also the uncertainty of the surrounding and atmosphere. Failure on IC will turns the car down and it is no more working for their specific functionality either for safety purpose or other facility.

In IC appllication, failure condition can be classified in to two types, the first one is failure happened at manufacturing line and the second failure is failure happened at customer's site or user's site. Manufacturing line is a work to produce the electrical board and testing the board with relevant device. The failure in manufacturing line is normal because there are a lot of trial and error and quality and reliability test has been done on electrical board to measure the board and microchip performance. A very good board will be produced to be mounted on car. Failure at customer's site is a tragedy. This is because, the IC failure could be happened during the operation of the car which mean during the driving moment. The functionality of the car system such as brake or engine would be functionless and caused an accident. Therefore, it is important to perform failure analysis on the failure IC to avoid the same error happen.

However, the technologies are not perfect. Even the failure analysis has been performed on failure IC, sometime the root couse is not clear. In failure analysis field, another aspect of failure analysis is associated with Physical Defect Not Found (PDNF) which is a term used in the field of failure analysis to describe a situation where an originally reported mode of failure can't be duplicated by the evaluating technician and therefore the potential defect can't be fixed.

PDNF can be attributed to oxidation, defective connections of electrical components, temporary shorts or opens in the circuits, software bugs, temporary environmental factors, but also to the operator error. Sometime, the PDNF case is related to procedure of failure analysis itself.

PDNF for the failure IC is a failure for Failure Analysis Enginner. PDNF returns can seriously erode profit margins for manufacturers and service providers. The time, materials, and shipping costs in exchanging hardware are massive in relation to the cost of the item being replaced. Further, PDNF returns can also indicate those failure occurances at manufacturing side and customers' problems have not been resolved, and thus imply reduced customer satisfaction and reduce brand value.



Figure 1.0 : Failure rate for specific root cause in year 2012.



Figure 1.1 : Failure rate for specific root cause in year 2013

Figure 1.0 and Figure 1.1 shows the distribution of failure in automotive environment captured on 2012 and 2013 respectively. The PDNF cases marked 22% for year 2013 and 28.4% for year 2014 which both can be considered as high percentage [1][2].

Based on data above, therefore this project will discuss about the new technique of IC decapsulation which is believed to be able to reduce the percentage of PDNF cases.

1.3 Objectives

- To investigate the root cause of the microchip failure in the correlation between Electrical Over Stress (EOS) / Electrostatic Discharge (ESD) or Wafer Fabrication failure.
- ii. To develop a new backside decapsulation method of failure analysis in order to reduce the processing time and also to reduce the PDNF percentage.
- iii. To investigate the performance of the new purposed failure analysis method by analyzing failing IC.

1.4 Scope

The main scope of this project consist several parts which are electrical analysis that will be performed by using curve tracer, IC decapsulation by using physical and chemical analysis and fault isolation step. The electrical analysis will be done to measure the failing behavior of electrical characteristic. In the IC decapsulation section, the feature about the new method of backside decapsulation will be detail explained with physical analysis, material used and also chemical reaction. For fault isolation step, Emission Microscopy (EMMI) will be used to point out the failing location of IC. The type of IC that will be discussed in this project is Automotive IC.

1.5 Thesis Arrangement

This thesis is starting with the introduction in Chapter 1 where it covers the overview of semiconductor industry and also the important of failure analysis. Also include in Chapter 1 are the problem statement, objectives and scope of the project. Detail of failure analysis step and procedure is described in Chapter 2. It is also consisted with the failure analysis flows that have been done in semiconductor industry and also the old method of backside decapsulation technique. Chapter 3 is related to methodology for this project. The new method of backside decapsulation is detail explained together with material used, chemical analysis and physical analysis. While in Chapter 4, the simulation, analysis and result for old method and new method of backside decapsulation is enlighted. The result comparison is shown in graph form. This thesis is ending with Chapter 5 which is conclusion of the result and recommendation for future project improvement.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

This chapter reviews some similar previous work, related journals and researches which include failure analysis on IC that can contribute ideas for completing this project. This chapter also will discuss about the various machine and device used in perfoming detail failure analysis in semiconductor industry. This chapter is essential to know about the step required to analyzing the failing IC from the beginning till the end of analysis.

2.2 Importance of Failure Analysis

Failure analysis is the process of investigating semiconductor devices after failure by electric measurement, and by physical and chemical analysis techniques if necessary, to confirm the reported failure and clarify the failure mode or mechanism.

Progress of semiconductor devices has rapidly accelerated toward high integration, high density and high functionality. In addition, use applications are widely penetrated into various civil and industrial fields.

The wafer fabrication and assembly process involves more than 100 steps using various types of materials. This, combined with the fact that devices are used in a variety of environments, requires a wide range of knowledge about the design and manufacturing processes.

Semiconductor industries try to consider high reliability through the design, development and manufacturing processes of semiconductor devices with the goal of "zero failures" and to provide those products to customers. However, it is impossible to eliminate all failures. Failure analysis engineer analyzes failures occurring during the manufacturing process, reliability test, mounting process at the customer's site and in the market field, investigates the failure mechanism and cause thoroughly, and feeds them back to each department in charge to prevent a failure from recurring.

2.3 **Procedures for Failure Analysis**

Failure analysis technology is not simply a means to investigate the failure causes and mechanisms of failed products. It is a vital and essential technology for quality and reliability improvement activities aimed at reducing failures in customer processes and the market to as close to zero as possible.

The failure analysis begins when a device under observation is determined to have lost its basic functions according to the failure criteria. Failures include complete loss of functions and various levels of degradation.

The most important factor in failure analysis is how far the failure location can be narrowed down while still maintaining the failure symptoms. The failure cause clarification rate varies widely according to whether the location can be narrowed down only to the function block level or whether the location of the trouble can be pinpointed.

Figure 2.0 and Table 2.0 respectively show the procedures for failure analysis and an example of devices to be used.



Figure 2.0 : Steps and procedures of Failure Analysis

Purpose	Equipments	
Observation	Stereoscopic microscope Metallographic microscope Infrared microscope Ultrasonic microscope X-ray fluoroscope Ultrasonic flaw detection equipment Liquid crystal analysis equipment Emission microscopic analysis equipment Photographic projection equipment Scanning electron microscope (SEM) Transmission electron microscope (TEM) OBIC/OBIRCH equipment	
Electrical characteristic measurement	Curve tracer Transistor tester/IC tester LSI tester/memory tester EB tester Oscilloscope Pulse oscillator Ammeter/voltmeter Noise meter Laser tester CV meter LCR meter Manipulator	
Elemental analysis	Electron probe micro analyzer (EPMA) X-ray fluorescence spectrometer Auger electron spectroscopy (AES) Ion micro analyzer (IMA) Electron beam diffraction analyzer X-ray diffraction analyzer Electron spectroscopy analyzer (ESCA) Infrared absorption spectrometer Emission spectrophotometer Atomic absorption spectrometer Ion chromatography equipment Gas chromatography equipment Mass spectrometer Cutting machine/Grinding	
Sample preparation	Cutting machine/Grinding equipment Sample packing device Package unsealing equipment Plasma etcher	

Table 2.0 : Example of main equipment used for Failure Analysis

	Deposition equipment Etching liquid Clean bench Ultrasonic disc cutter Laser cutter FIB
Thickness/shape	Ellipsometer
measurement	Tunneling microscope

2.4 Non-destructive Analysis

Non-destructive analysis is a type of analysis techniques used in semiconductor industry to evaluate the properties of a material, component or system without causing damage on the IC [7]. Non-destructive analysis does not permanently alter the sample being inspected, it is a highly valuable technique that can save both money and time in product evaluation, troubleshooting, and research. Common non-destructive analysis methods include External Visual Inspection (EVI), X-RAY and Scanning Acoustic Microscopy (SAM) analysis. Non- destructive analysis is a compulsory method to be done before performing further analysis.

2.4.1 External Visual Inspection (EVI)

Visually inspecting the external condition of the device often provides valuable information for subsequent analysis. First the device is inspected by eyes to check for any differences from good ones. Then microscopic inspections are carried out for detailed observation. A stereomicroscope with magnifying power 5X to 100X is used. Illumination from various angles is used to obtain the best view of the sample. A regular microscope with higher magnification power 50X to 2,000X is sometimes used to search for failure spots. Figure 2.1 below showes the example of stereomicroscope with multiple magnification lense.



Figure 2.1 : Stereomicroscope

If further observation is required to detect package cracks, surface wear, particles, whiskers, discoloration, or migration, a Scanning Electron Microscope (SEM) is used. SEM is a type of electron microscope that produces images of a sample by scanning it with a focused beam of high energy electrons to generate a variety of signals at the surface of solid specimens. Sample from 1 cm to 5 microns in width can be imaged in a scanning mode using conventional SEM techniques which has magnification ranging from 20X to approximately 30,000X, spatial resolution of 50 to 100 nm. Figure 2.2 below shows the SEM machine and its basic working principle.



Figure 2.2 : Scanning Electron Microsocopy

2.4.2 X-RAY

X-RAY is used to check the internal state of a device without opening or removing the package. X-ray examination uses the fact that X-ray penetration varies according to the type of material and thickness which the principle the smaller the atomic weight, the greater the penetration. Aluminum (Al), silicon (Si) and the like with light atomic weight have a high transmission rate and are difficult to identify, but gold (Au), cupper (Cu), iron (Fe), solder (Sn, Bi, Ag, Pd) and the like have a low transmission rate, so the state can be identified easily. The differences create an X-ray image. This method is effective for detecting particles, breakage or looping of bonding wires, and voids or peeling in mold resins or the die bonding section inside the plastic sealed IC package.

Figure 2.3 shows the example of X-RAY image on IC to check the wire bonding formation and frames condition.



Figure 2.3 : X-RAY image on IC

2.4.3 Scanning Acoustic Microscopy

Scanning acoustic microscopy (SAM) is a non-invasive, non-destructive technique that use ultrasound wave to image the internal features of an IC package. It is currently less used than X-ray due its less familiar underlying technology, and a more complex process requiring greater skill and training to operate and interpret. Nonetheless, SAM provides some advantages over other available inspection technologies which make it a superior tool for certain materials and processes. It is highly sensitive to the presence of delaminations, which are difficult to detect using X-ray radiography. Moreoever, SAM can detect delaminations at sub-micron thicknesses. It is one of the only techniques capable of efficiently evaluating popcorning in IC and able to evaluate low and high-density plastic materials. SAM is particularly useful for inspection of small, complex devices. It can detect sub-micron air gaps, as thin as 0.13µm and has a defect resolution of 5µm, allowing for inspection of material.



Figure 2.4 : Scanning Acoustic Microscopy Machine

Figure 2.4 shows the physical of SAM machine. The working principle of SAM is, it is working by using sound energy to image a sample through the use of transducers. Samples are submerged in a liquid medium such as distilled water or alcohol to ensure that the ultrasound waves are delivered to and from the samples. The ultrasonic transducers send pulses into the liquid and through the samples. The transducer also receives reflected pulses from discontinuities and disturbances from the sample. The transducer transforms the reflected sound pulses into electromagnetic pulses which are displayed as pixels with defined gray values thereby creating an image.

Figure 2.5 and Figure 2.6 below show the basic construction of SAM machine and its scanning result to for specific function of scanning method.



Figure 2.5 : Basic Construction of SAM



Figure 2.6 : SAM working principle

2.5 Destructive Analysis

Destructive analysis is a process of changing the physical of the IC package. Basically, the destructive analysis will be done after non-destructive analysis has been performed. It includes the decapsulation process and cross section process which can be done by mechanical machine or chemical solution.

2.5.1 Decapsulation

To reveal the silicon chip of the IC package, the resin or mold must be removed by decapsulation process. The purpose of decapsualtion is to expose the surface of the chip without damaging the surface of the silicon chip, the wire and the lead frame and to make the later observation and measurement, but it is unexpectedly difficult to decapsulate in a non-skilled method and firmly. During decapsualtion, it is important to select the method in view of the types and the materials of packages. In case of ceramic encapsulation devices, the cover is unsealed with a mechanical technique.

There are two types of decapsulation which are frontside decapsulation and backside decapsualtion.

2.5.1.1 Frontside Decapsulation

Frontside decapsulation is a process of removing resin from the top side of the IC package. Normal decapsulation method is using laser machine and chemical acid wet etching at the topside/frontside of the package. Laser machine is used to remove the resin from top of the package until it reaches certain level of package which is basically 100-200um of the resin remain.

Figure 2.7 and Figure 2.8 show the illustration of sample decapsulation by using laser machine to remove top resin.



Figure 2.7 : Before laser decapsulation

Figure 2.8: After laser decapsulation

After laser decapsulation done, sample will be proceeded with chemical wet etch by using Nitric Acid 100% fuming (HNO3) or Sulfuric Acid (H2SO4) on hot plate 70-100°C. Figure 2.9 shows the illustration of sample decapsulation by using Nitric Acid 100% fuming.



Figure 2.9 : Chemical wet etch on Hot Plate

This decapsulation process will expose the die and wire bonding connection. The process must be done very carefully without any mishandling on the sample during process decapsulation.

Table 2.1 illustrates the final result of front side decapsulation technique.



Table 2.1 : Frontside decapsulation process



There are several advantages and disadvantages of this process. The advantages of topside decapsulation process are listed below;

- 1- Easy and fast process
- 2- The ability to view the overall die surface for detail inspection
- 3- The ability to perform microprobing for advance electrical verification.

Meanwhile the disadvantages of topside decapsulation are the following;

- 1- The possibility of mishandling during decapsulation which will scratch the die.
- 2- The possibility of metal lift-off if over etch and over heat occurred.
- 3- The possibility of losing failure evidence if related to foreign material especially on adjacent pins connection.
- 4- The possibility of failure recover after decapsulation
- 5- EMMI and OBIRCH spots are not accurate if the failure is located under the thick Metal Layer especially on Power DMOS area.

2.5.1.2 Backside Decapsulation

The increasing number of metallization layers used in modern ICs, which physically block the view of microscopes from seeing faults and point defects, rendered front-side techniques inadequate for complete failure analysis. Therefore, backside decapsulation is needed for this case.

Backside decapsulation is a process of removing resin from the bottom of the IC package. It will directly expose the silicon die structure of active area instead of exposing metal connection on front side decapsulation [8]. Normal operation of backside decapsulation of automotive devices is basically taken four to five hours to be completed. Normally, the total hour to complete this standard backside decapsulation is around two to four hours. Sometime it is not so practical to perform backside decapsulation for automotive device due to long time duration of decapsulation process.



Figure 2.10 : Backside decapsulation overview

Figure 2.10 above illustrated the backside decapsulation technique. A standard technique for backside decapsualtion is using laser machine and backside grinding machine. The process need to be carefully performed by following its standard decapsulation recipe. The first step is removing resin by using laser machine and followed by frame removal. Proper grinding to remove frame must be properly done in order to avoid any stress on the glue and silicon. After completely removing frames, glue must be polished by specific chemical with the help of grinding machine.

2.5.2 Die Deprocessing/Delayering

Delayering is a commonly used process in failure analysis, debug, and general construction analysis in the production of ICs. In many cases it is necessary to remove layers from the integrated circuit for inspection, whether it be electrical testing, deposition uniformity, or device integrity investigation. The precise removal of these layers requires accuracy, knowledge of components and materials systems, and equipment capable of implementing precision polishing techniques.

Delayering is useful to remove specific device layers when evaluating the design of any device or for specific failure analysis techniques. Equipment used for this type of specimen preparation must be adaptable to many different materials such as Nitrides, Oxides, Aluminum, Copper and low dielectric constant materials. Planarity is critical in deprocessing applications where individual device layers are sub-0.5 um and below.

Table 2.2 illustrates the delayering result at Metal 3, Metal 2, Metal 1, Poly and Oxide layer for Bipolar CMOS DMOS (BCD) technology.

Delayering Result	Detail
	Metal 3 – Metal 3 is a metallization that is functioning to connect the component at active layer. Metal 3 is located at the top side of the silicon die.

Table 2.2 : Delayering result for BCD technology





2.6 Fault Isolation / Localization

Different companies have different failure analysis flows but all failure analysis steps will need to start with fault isolation. Fault isolation is the step to narrow down the focus area of a failing component or product to a manageable area that will allow us to improve success of finding the defect that is causing the failure and significant speed up turn-around time for analysis.

There are many different challenges to consider in localization techniques since there are multiples electrical with multiples failures mechanisms. Practically, depending on the location of the physical defect, the faults mechanism will vary and it is determining the effectiveness of the physical failure analysis by identifying and localising suspected failures.

In addition, localization techniques require interfacing with electrical test to stimulate the fault, selecting the appropriate detection techniques, ensuring correct interpretation of the result with Computer Aided System (CAD) software between physics and the electrical consequence of the fault.

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