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ESTIMATION OF COMMON MODE RADIATED EMISSIONS FROM CABLES ATTACHED TO HIGH SPEED PCB USING IMBALANCE DIFFERENCE MODEL

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ABSTRACT

The functional (Differential-Mode) signals on Printed Circuit Board (PCB)-traces are not possibly responsible for higher emissions. However, they can induce unwanted Common–Mode (CM) signals on the nearby metallic structures such as PCB-attached cables. Commonly, PCB-attached cables can act as unintentional antenna resulting in higher emissions that may make the PCB easily fail to meet the Electromagnetic Compatibility (EMC) regulatory compliance test. This process requires repeating all the product-building procedures to obtain the optimum design of the prototype, which increases the unit cost, as well as delay in the product marketing. Therefore, an early prediction of CM Radiated Emissions (RE) is helpful for circuit designers to avoid the RE issues before the first prototype is built. PCB- REs are estimated using 3D-full wave numerical solver. However, it is not practical option since it requires intensive computational time. It also does not provide insight into how the electric/magnetic coupling occurs. In this paper, the imbalance difference theory, which has shown successful demonstration in the low frequencies, is adopted for high frequencies. Based on this theory, a mathematical solution is developed for estimating CM-RE from cables attached to high speed PCB. For verification of the proposed model, an open-circuit PCB-configuration is used to validate the proposed mathematical model. Then, the results obtained from this model are compared with results obtained from 3D-HFSS full wave simulation and a good agreement is obtained between the two results.

Key words: Common-Mode radiation · Imbalance Difference Model · Printed Circuit Board · Voltage-driven ·

INTRODUCTION

The ever increasing of clock frequency on Printed Circuit Board (PCB) to several gigahertz has enhanced the PCB-attached cables to become efficient radiators of electromagnetic energy. Hence, properly designed PCBs can offer a cost-effective approach for achieving Electromagnetic Compatibility (EMC) compliance [1]. Hence, the consideration of EMC during the design phase is becoming critically important.

The most conventional method for quantifying the Radiated Emissions (RE) is to measure the first manufactured prototype in Semi Anechoic Chamber (SAC). However, this method is quite iterative and time-consuming. Alternatively, the RE can be predicted earlier in the design stage using many approaches such as a 3D-full wave modelling. Unluckily, this method is not preferable since the today's electronic devices are quite complex. Therefore, it is desired to provide efficient simplified equivalent models to predict the radiated emissions analytically instead of 3D full wave simulation for the entire PCB.

Generally, the total RE of PCBs is generated due to both Differential-Mode (DM) and Common-Mode (CM) currents. Although CM currents have significantly lower values compared to DM currents, its contribution to the total RE are much more than that due to DM currents [2], [3].

Practically, numerous CM-RE sources can be identified on the electronic product such as attached cables, heatsink and enclosure. Although many researchers have approved that these cables are significant sources of CM-RE, there is lack of fundamental mechanisms to explain how the DM signals are converted to CM signals in the high frequency range.

Hockanson et. al, have developed two equivalent models for explaining how the DM signals are converted to CM signals [4]. These models are commonly referred to as current-driven and voltage-driven mechanisms. The current-driven mechanism refers to CM currents induced by the DM signal currents returning in the "ground" structure causing voltage differences between objects referenced to different parts of the structure [5],[6]. The dominant coupling in this mechanism is magnetic field coupling wraps from trace to ground plane. The parasitic inductance on the ground plane enable the DM current to create fluctuated voltage on the ground plane resulting in potential CM voltage source on the ground plane such as short-circuit trace. On the other hand, the voltage-driven mechanism refers to electric field coupling from traces or heat sinks that are at one potential to cables or other external objects that are at a different potential [7]-[8] such as open-circuit trace.

H. Shim and T. Hubing in [7] have introduced an equivalent wire antenna model for estimating voltage-driven CM currents. The CM voltage source is placed at the connection point between the ground plane and the attached cable. The magnitude of the equivalent voltage source is given in terms of the ratio of the self and stray capacitances of the board and the trace.

However, these two mechanisms are applied when one coupling mechanism is dominant. In fact, the CM-RE is produced due to both mechanisms (electric and the magnetic field coupling). Therefore, it is necessary to estimate the CM-RE model without specifying a particular field coupling mechanism. Alternatively, imbalance

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difference has been approved as a successful model for estimation CM RE from PCB-attached cables. Commonly, the entire PCB is simulated including all the design details. Instead, simulation of the equivalent model would give the same results with less complexity.

The another methods for estimating RE from PCB-attached cables is to determine the CM currents on the PCB and cable that enable estimation of CM-RE. This method require current probe to measure CM current as in [9], [10]. However, this method is inconsistent due to the dependency of CM current on probe position and frequency.

To overcome these constraints, Su and Todd [11] had applied imbalance difference model for quantifying the CM currents on cables attached to a PCB. Various PCB structures are employed to verify that model and the results obtained are compared to those obtained with traditional voltage/current-driven models, as well as 3D-full-structure simulations [12]. However, the current distribution is assumed uniform along the trace where the trace is electrically short. For high speed (high operating frequency), the Transmission-Line (TL) theory is adopted. Hence, Su's model must be extended to cover the high frequency range.

In 2015, Zhang et. al, [13] has developed model for predicting CM-RE using imbalance difference model with aid of asymmetrical dipole concept. However, more analysis and investigation of the coupling mechanisms are required. The effect of DM current distributions along the TL and the cable position on RE can be studied in details to obtain complete model for predicting RE from PCB-attached cables. Generally, both the imbalance difference theory and the voltage/current driven model are valid as the cross section of the board-trace configuration small as relatively to a wavelength. In other words, the condition of quasi-Transverse ElectroMagnetic (quasi-TEM) must be fulfilled.

In this paper, a model based imbalance difference theory is presented for predicting the CM-RE from cables attached to high speed (high operating frequency) PCB with more attention is given to the coupling of electric field. Hence, open-circuit configuration is used in our analysis as illustrated in the next sections.

MODELING AND ANALYSIS

Introduction to Imbalance Difference Theory

Watanabe et. al, [14] have introduced a general theory for predicting the CM RE from circuits. They have approved the degree of change in the electrical imbalance is responsible about CM-RE. According to this theory, parasitic CM voltage is identified at the junction point between the PCB-attached-cable and the PCB-ground plane where the electrical imbalance changes. At that point, the CM voltage is evaluated based on the degree of change in the electrical imbalance and the corresponding DM voltage at that point.

Later, this theory has been adopted by many researchers as in [15]-[16] It has been verified as an efficient tool for modelling of PCB structures. In order to clarify how this theory can be applied to high-speed PCBs-attached cables, a simple structure shown in Figure1 is used for this study. It consists of a simple circuit board structure with one signal trace etched over a solid ground plane. The board has cables attached to both ends of the ground plane. The transmitted DM signal is injected at the near-end of the trace while the far-end of the trace is connected to the ground plane through circuit load. There is a dielectric material with thickness t is sandwiched between the ground plane and the signal trace. In Figure 2, the thickness t is exaggerated for better clarity of the PCB structure.

In contrast to the previous studies, the trace-board geometry is electrically long at high frequencies. Therefore, the DM-RE can be evaluated based on transmission line theory. In this case, the DM current is non-uniformly distributed along the PCB trace. The transmission line model is capable to predict DM currents only; this is because an infinite perfect return plane is assumed. Theoretically, the DM currents flow in two- parallel traces with same magnitude but opposite in direction, and thus the produced DM fields will tend to cancel each other. Practically, the PCB ground plane is finite and non-perfect thus, CM voltage sources can exist on the ground plane then the CM currents pass through on the attached cables which possibly be a significant source of RE. In this paper, the imbalance difference concept is applied for estimating the CM-RE from cables attached to high speed PCB with aid of transmission line theory as illustrated in the next sections.

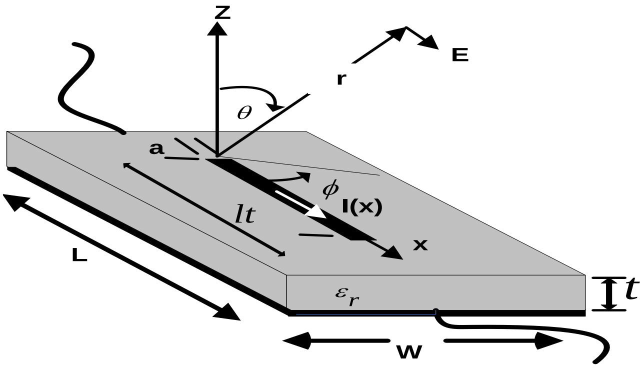
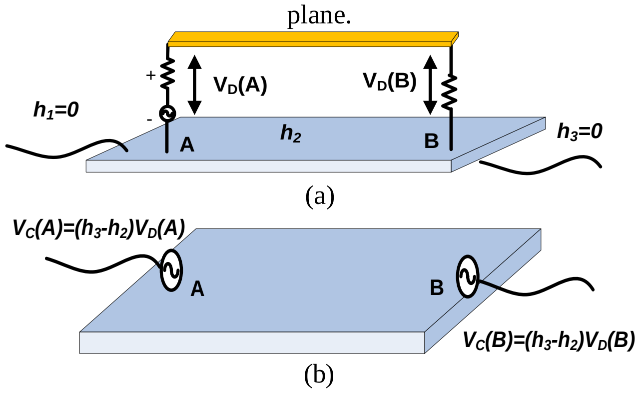


Figure 1: PCB structure with cables attached to the ground plane.



(a)

(b)

Figure 2: Application of Imbalance difference concept (a) exaggerated schematic of PCB under study (b) Equivalent model.

Trace-Current/Voltage distribution

In contrast to electrically short traces, the current distribution on electrically long PCB-traces is no longer uniform through the PCB-trace. It can be approximated by transmission line theory [17] or estimated by a numerical method, such as the method of moments [18]. In this paper, the transmission line theory is adopted for trace-current calculation because of its simplicity.

The DM current flows as depicted in Figure 3 from the signal source to the load through a transmission-line (trace) of length l.

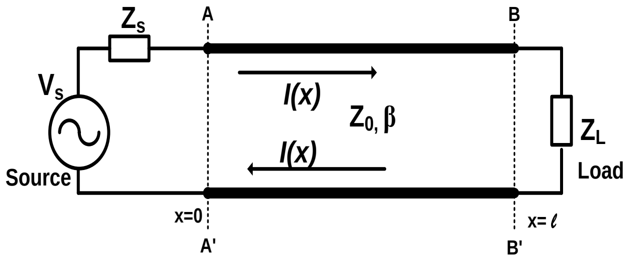


Figure 3**:** Equivalent transmission-line model of PCB

Simply, the signal source on the left is represented by open-circuit signal voltage V_S, and source output impedance Z_S. The receiver input impedance is represented by the load impedance Z_L while the PCB trace is modelled as a transmission line. In this situation, the assumption of quasi-TEM mode propagation through the microstrip PCB is adopted in the frequency range of the analysis, which means that the dielectric thickness and trace width must be electrically smaller than the signal wavelength. As a result the approximate frequency limit of the quasi-TEM operation can be given as [19]

$$f[GHz] \approx \frac{21.3}{(w[mm] + 2t[mm])\sqrt{\varepsilon_r} + 1} \tag{1}$$

where t is the dielectric thickness, ε_r is the relative dielectric permittivity and w is the trace width.

Commonly, the transmission-line is described by the characteristic impedance Z_0 and the phase constant β. The phase constant can be given in terms of the effective relative permittivity $\varepsilon_{r,eff}$ that is related to β through the phase velocity v_p on the line as [19]

$$\beta = \frac{\omega}{v_p} = k_0\sqrt{\varepsilon_{r,eff}} \tag{2}$$

where ω is the angular frequency, c_0 is the wave speed in the air, and k_0 is the free-space wavenumber which can be given as

$$k_0 = \omega / c_0 \tag{3}$$

The effective relative permittivity and the characteristic impedance can be calculated using various closed-form expressions available in [19]. However, the calculation of the DM current on the transmission line depends on the loading conditions across the terminals is taken from [1]. Assuming a lossless trace, the DM current at point x can be written as [1]

$$I(x) = \frac{V_S}{Z_S + Z_0}\frac{1}{1 - \rho_S\rho_L e^{-j\beta 2l}}\left(e^{-j\beta x} - \rho_L e^{-j\beta 2l} e^{j\beta x}\right) \tag{4}$$

while the source/load -reflection coefficients are given as

$$\rho_{S,L} = \frac{Z_{S,L} - Z_0}{Z_{S,L} + Z_0} \tag{5}$$

respectively.

The DM voltage also can be computed based on the theory of the transmission-line also as [1]

$$V(x) = \frac{V_S\, Z_0}{Z_S + Z_0} e^{-j\beta x}\frac{1 + \rho_L e^{-j\beta 2l} e^{j2\beta x}}{1 - \rho_S\rho_L e^{-j\beta 2l}} \tag{6}$$

while the input impedance $Z_{in}(x)$ at any point on the TL is given as

$$Z_{in}(x) = Z_0\frac{Z_L + jZ_0\tan(\beta x)}{Z_0 + jZ_L\tan(\beta x)} \tag{7}$$

Modelling Example

Commonly, any transmission-line geometry has imbalance value between 0 and 0.5. This number is known as imbalance parameter. An imbalance parameter of 0.5 denotes for perfect balanced structure (e.g., two symmetric conductors with identical cross sections) whereas the value 0 of imbalance parameter means perfectly unbalanced structures (e.g., a coaxial cable or a trace over an infinite ground plane).

In this paper, a microstrip PCB structure is employed as PCB test board. Consider Figure 2 as an example, there is a change in the imbalance parameter h at both ends of the PCB. At each end, the width of the trace varies from a finite value a to zero. Therefore, CM voltages are induced on the junction between the cable and the ground plane. The magnitudes of CM voltages are computed as the product of the DM voltage and the change in the imbalance parameter as [15]

$$V_{CM}(x) = \Delta h\, V_{DM}(x) \tag{8}$$

where $V_{DM}(x), V_{CM}(x)$ are the DM/CM voltage at the position x respectively and Δh denotes for the degree of change in the imbalance difference factor.

Based on equation (8), the induced CM voltage at the location A can be expressed as

$$V_{CM}(A) = (h_2 - h_1)\, V_{DM}(A) \tag{9}$$

while the induced CM voltage at the location B can be given as

$$V_{CM}(B) = (h_3 - h_2)\, V_{DM}(A) \tag{10}$$

In the literature, the CM-RE has been predicted according to voltage-driven (Electric field coupling) and current driven (magnetic fields coupling) mechanisms. The Electric field coupling is dominant in open circuit case whereas the magnetic coupling is dominant at short-circuit case. In this paper, we focused on the voltage driven mechnsims(Electric field coupling). Therfore, the imbalance difference factor, h for microstrip structure can be expressed as [11]

$$h = \frac{C_{trace}}{C_{trace} + C_{board}} \tag{11}$$

where C_{trace}, C_{gnd} are the stray capacitance of trace and ground plane respectively. It's known the imbalance parameter for the trace-board portion h_2 must always be between 0 and 0.5. Since h_1 and h_3 are zero, the common-mode voltages in equation (9) and (10) can be rewritten as follows:

$$V_{CM}(A) = h_2\, V_{DM}(A) \qquad (12)$$

Practically, the signal trace and the return plane are not perfect conductors resulting in an unwanted noise voltage source is induced as shown in Figure 4

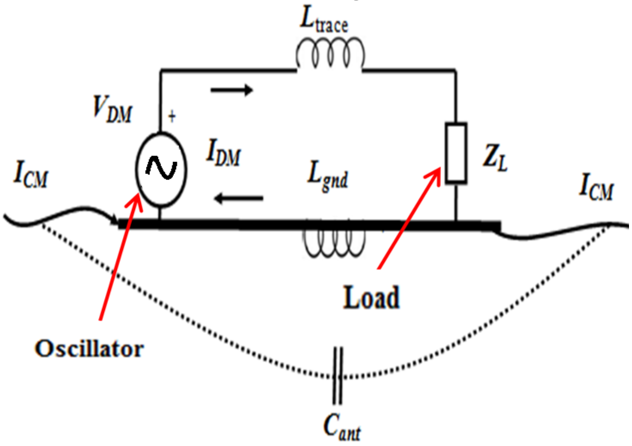


Figure 4: Equivalent model of PCB with attached cables

DESCRIPTION OF PCB TEST BOARD

In this paper, a simple PCB in open-circuit configuration with one attached cable connected to the PCB ground plane at the far-end of the trace as depicted in Figure 5. A virtual CM voltage exists at the junction between the cable and PCB according to the imbalance difference concept. Hence, the equivalent model for this configuration is developed using the equivalent CM voltage with cancellation for all DM sources as shown in Figure 5.

This CM voltage is evaluated using Matlab software then verified by comparing the result obtained in 3D-High Frequency Strucure Simulator (HFSS) full wave simulator using PCB with trace length l =10.16 cm and a width a = 0.51 mm, and is positioned on a finite-size board with ε_r= 4.6 and t= 0.775 mm. It is fed by a voltage source with constant amplitude V_S = 1 V and output impedance Z_S = 50Ω and is open circuited at the load terminal for open circuit configurations. The corresponding transmission-line parameters of this PCB were computed to $\varepsilon_{r,eff}$ = 3.2 and Z_0 = 84.

Based on the transmission-line theory, the open-circuit configuration is described with reflection coefficient $(\rho_L = 1)$. Thus, the CM voltage source is expressed based on (6) and (7) with substitution of open-circuit reflection coefficient. The voltage varies along the TL from source to load with different behaviour in open and short circuit load as shown in Figure 6. The results of CM RE using the analytical and HFSS 3D simulation solver are illustrated in Figure 7.

The analytical approach is adopted for computing the stray capacitances in all the calculation process using equations available in [11], [20], [21]. The proposed analytical solution consist of two stages; identifying and quantifying the CM voltage as shown in Figure 6 then estimating the CM RE as shown in Figure 7 which produced to this virtual CM voltage on the structure.

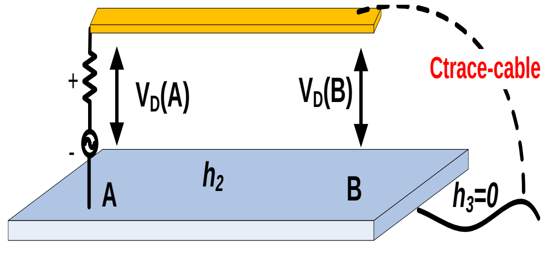
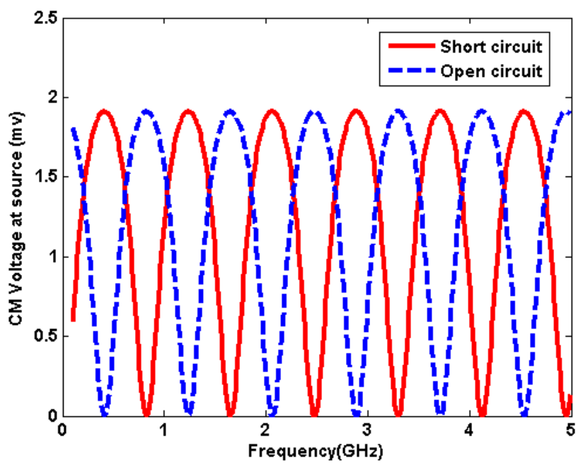


Figure-5. Application of Imbalance difference concept (a) exaggerated schematic of PCB under study (b) Equivalent model.

RESULTS AND DISCUSSIONS

The voltage/current distribution is no longer uniform along the PCB trace. It varies based on many parameters as illustrated in (4) and (6). Figure 6(a) shows the equivalent CM voltage at the input of the trace $(x = 0)$ for both short and open circuit. Both of configurations had same magnitude of voltage but out of phase. However, the magnitude, which is obtained by multiplying the imbalance difference factor by the DM voltage, at that point is 2 mv. On the other hand, the DM voltage at the load-end $(x = l)$ is zero for short-circuit. Therefore, the equivalent CM voltage is zero at load-end junction as shown in Figure 6b.. In contrast to this, the CM voltage at the far-end for open-circuit configuration is also 2 mv but with different phase as shown in Figure 6b. Therefore, only open circuit configuration is taken for verifying the proposed mathematical solution.



(a)

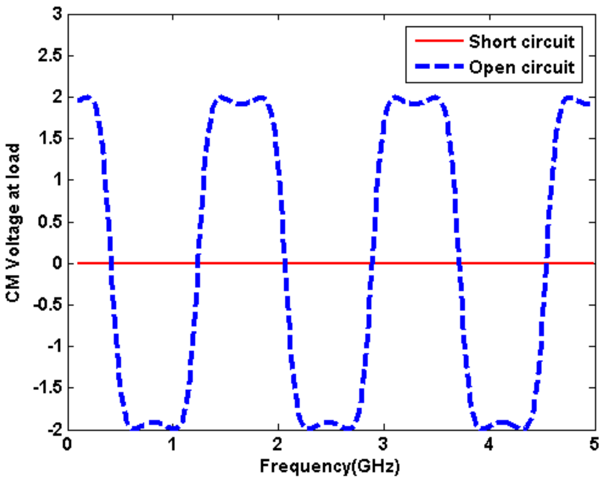


Figure 6: Estimated CM voltage at the (a) near-end to source (b) far-end near to load

The CM RE is predicted based on the estimated CM voltage with antenna theory. In this paper, the cable is modelled as monopole antenna and the board factor is taken into account [8], [22]. Figure 6 shows a comparison of the electric field at 3 meters obtained from 3D full wave HFSS simulation of the entire PCB structure and the equivalent analytical model considering imbalance difference concept. The analytical model is demonstrated in MATLAB consuming less time for execution comparing with full wave solvers. This analytical solution does not provide same accuracy as provided in HFSS simulation. However, it can be used to predict the CM RE with reasonable estimation to indicate the maximum possible CM RE.

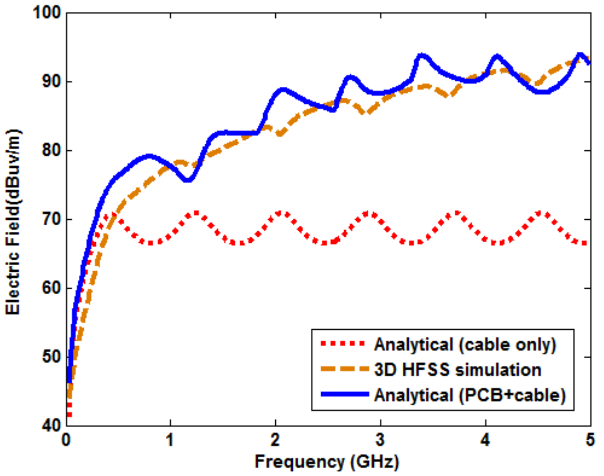


Figure 7: Estimated CM RE for PCB-cable structure using HFSS simulation and analytical solution

CONCLUSIONS

In this paper, the imbalance difference concept is utilized for developing an analytical solution for estimating the maximum CM-RE produced from cables attached to high speed PCB. In this case, the PCB-traces are electrically long. Hence, a transmission-line theory is applied for computing the voltage distribution along the PCB-trace. In this developed model, more focus is given to voltage-driven mechanism where the CM-voltage depends mainly on the DM voltage. Results obtained from both analytical and 3D simulation are in a good agreement. Therefore, this model can provide a reasonable estimation of CM RE from PCB attached-cables as long as the PCB operates in quasi-TEM range. In the future, this model will be extended to consider the case when the current-driven mechanism is dominant. Later, the general solutions would be introduced for developing an expert system that can characterize and identify the CM RE in the design stage.

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