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INVESTIGATION OF THRESHOLD VOLTAGE AND TRANSCONDUCTANCE VARIATIONS IN PMOS

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ABSTRACT
Scaling process of MOSFET has yielded great benefit in term of processor technology evolution. However, it is worth to note that the scaling process also affects the electrical parameters as well. It is expected that as MOSFET gradually scaled into the submicron regime, the variation of electrical parameters due to scaling becomes more apparent. The study is carried out through simulation work of 45 nm p-type MOSFET (PMOS) using a commercial device simulator. This tool is used as a medium to observe changes in threshold voltage (V_{TH}) and transconductance (g_m). Changes of both parameters are investigated against three factors; oxide thickness (t_{ox}), doping concentration of dopant in substrate and doping energy. Observation in simulation results suggest that increment in both t_{ox} and doping energy increases V_{TH} and reduces g_m. In contrast, increment in doping concentration of dopant improves g_m and trims V_{TH}. Analysis of results deduces that the variations of both V_{TH} and g_m against those three factors are related to number of free carriers during device operation.

Keywords: threshold voltage • transconductance • submicron PMOS •

INTRODUCTION

The scaling process has contributed to significant changes in device dimension of MOSFET. To date, the scaling process helps integrated circuit industry to sustain the Moore's Law. A compromise design is essential to accommodate both high performance and low power logic (Zeitzoff and Chung, 2005) as the transistor technology advances. High switching speed and low leakage current are required to achieve the compromised design. The scaling process also heavily dependent on velocity and mobility of carriers to ensure a proper operation (Khakifirooz and Antoniadis, 2008).

High leakage current and electron tunnelling mechanism have been identified as major issue when transistor is scaled (Zietzoff and Chung, 2002), (Ning, 2007). Parasitic resistance due to source or drain extension also another issue in transistor scaling (Plummer, 2000). Furthermore, variation in fabrication process also affects the performance of scaled transistor (Saha, 2014). High bias potential also leads to other shortcoming such as hot electrons and oxide reliability (Ning, 2007). A proper bias in accordance to scaled device dimension is important to preserve reliability (Bohr, 2007).

In spite of numerous challenge in MOSFET scaling, it is expected that the scaling process will continue. Innovations in channel material selection (Antoniadis et al., 2006), (Thompson et al., 2005) and device structure (Majumdar et al., 2014), (Xin et al., 2008) are among novel approaches that will extend the scaling process. Using metal as source.drain terminals is also being considered since it could reduce electron tunnelling and sheet resistance (Larson and Snyder, 2006), (Zietzoff and Chung, 2002). Another approach is to consider variants of MOSFET such as junction FET (Jackson et al., 2009) as a potential candidate of transistor in submicron regime.

The main objective of this work is to investigate the variations of V_{TH} and g_m of PMOS in the submicron scale. The investigation is made against three factors, which substrate and doping energy of dopant. The investigation is made through device simulation using Sentaurus TCAD.

DEVICE SIMULATION

Figure 1 exhibits the flow of device simulation carried out in this work. The work flow involves five components in Sentaurus TCAD which are Sentaurus Workbench (SWB), Ligament, Sentaurus Device (SDevice), Tecplot and Inspect.

Firstly, the device input parameter was set in the SWB such as the gate length. Each node of input parameters could be run independently to obtain specific output files. During simulation, each node status would be represented with a unique colour. For example, a blue node represents a running simulation and an amber node represents a completed simulation. In general, the SWB acts as a tool to give an overview of the whole process in Sentaurus TCAD. Nevertheless, the individual process must be defined before it appears on the SWB interface.

Next, the changes in oxide thickness were simulated in Ligament. This was done by specifying the length of oxidation process in Ligament. At the end of the process simulation, a series of oxidation thickness was obtained to be used in the next step of simulation. The variability of oxide thickness was then used to examine the change in the V_{TH}.

The following steps were to obtain the device doping profile in Tecplot. The doping profile was generated according to the doping concentration specified in SWB. The doping profile was obtained once the process simulation in Ligament has completed. It means that any changes in process simulation defined in Ligament will affect the doping profile. As shown in Figure 2, two input files were required in Tecplot which were *<filename>.cmd* and *<filename>.tdr*. Next, SDevice was used to extract output data of device operation such as current and voltage of interest. In addition, this tool also helped to determine the final solution of all structure variables. Finally, the electrical

The drain-to-source current (I_{DS}) was one of the main output parameter viewed in Inspect. Two input files were required in this simulation, namely *<filename>.cmd* and *<filename>.plt*. Figure 3 shows the pre-process in Inspect before the output parameters are extracted.

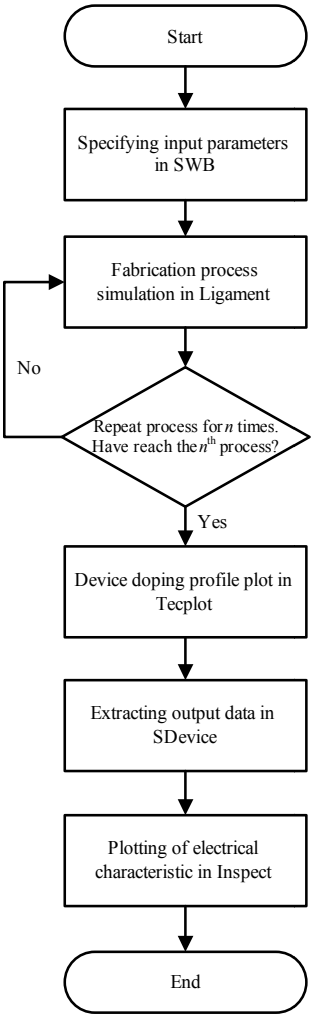

Figure 1: Work flow of device simulation

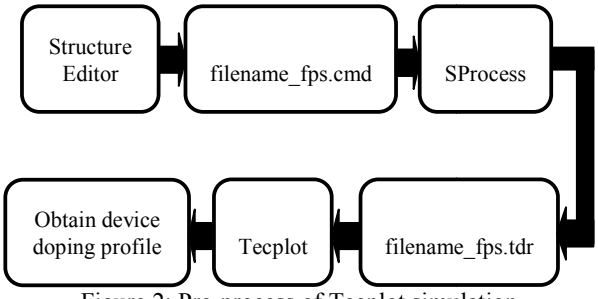

Figure 2: Pre-process of Tecplot simulation

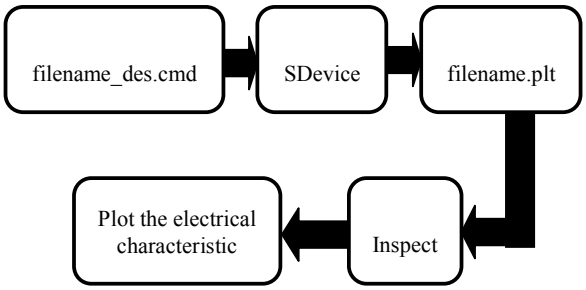

Figure 3: Pre-process of Inspect simulation

RESULTS AND DISCUSSION

A structure of 45 nm PMOS is obtained through fabrication process simulation in Ligament. Tecplot SV tool is used to display the device structure with the corresponding doping concentration as shown in Figure 4. The gate length is 44.47 nm as measured in the Tecplot SV.

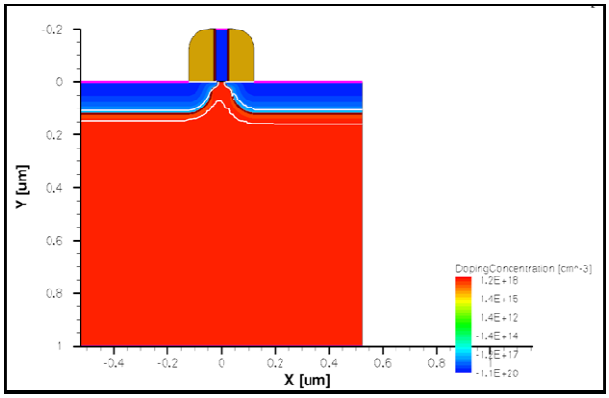

Figure 4: Device structure of 45nm PMOS

The oxide thickness shows linear relationship with both the V_{TH} and g_m. As shown in Figure 5, the V_{TH} increases with respect to increment of the oxide thickness. Negative values of voltage indicate the operation of PMOS, which requires negative gate voltage to turn on the device. An inversion layer will be created when V_G is applied. The inversion layer, in turn, will aid the creation of channel just beneath the oxide layer to allow current flow between source and drain terminals. Therefore, a thinner oxide layer will require less V_G to create channel and implies less V_{TH}. However, t_{ox} has opposite effect on g_m as shown in Figure 6. The changing trend implies that a larger V_G change is required to obtain the same amount of I_D. Increasing the t_{ox} will require a higher potential to be applied on gate terminal to allow current conduction in PMOS. This causes a higher change in V_G is needed to obtain the same I_D compared to lower t_{ox}. This explains the inverse proportionality between the t_{ox} and g_m.

The second factor being investigated is the effect of doping concentration of dopant in substrate towards V_{TH} and g_m. The doping concentration exhibits an inverse proportionality with V_{TH} as illustrated in Figure 7. In other words, as the doping concentration increases, the V_{TH} becomes smaller or less negative. This relationship is related to number of free carriers being created in the substrate. As the doping concentration is increased, so does the number of electrons. This will lead to creation a similar

number of holes just beneath the oxide layer when V_G is applied. A low V_G is enough to create channel under the oxide layer due to high number of holes available for conduction. Therefore, as the doping concentration is increased, a higher number of holes will be available and a lower potential threshold is imposed for conduction. In Figure 8, it is observed that the doping concentration of dopant in the substrate has an exponential relationship with g_m. This trend can be seen when the doping concentration is changed from 10^{10} cm^{-3} to 10^{11} cm^{-3}, there is a significant change in g_m. It implies that at high doping concentration of dopant, a small change in V_{DS} results in large change of I_D. This observation shares the same argument as in the case of V_{TH} variation. As the dopant in substrate increases, a higher number of holes are created. When there are huge number of free carriers flow between the electrodes, a high current is created. This explains a big change in current with a small variation in applied V_G as the doping concentration increases.

Finally, the variations of V_{TH} and g_m are being investigated against doping energy. As shown in Figure 9, V_{TH} increases as the doping energy is increased. In general, doping energy is related to the depth of implanted dopants in the substrate. It means a high doping energy created a deep dopant implantation. It also implies that any free carriers available are placed much further away from the oxide layer. When V_G is applied, these free carriers are also further away from channel that conducts I_D. Therefore, a higher threshold potential is being imposed to turn the device into conduction mode. This observation explains the reason V_{TH} is getting larger as the doping enegy increases. The same argument can also be used to explain the relationship between g_m and doping energy. As illustrated in Figure 10, as the doping energy is increased, g_m reduces that implies a lower ratio of I_D to V_{DS}. Higher doping energy means the dopant is implanted much further in the substrate. Therefore, lower number of free carriers present during conduction that leads to low current. Any change in current will require a larger change in V_{DS}, due to limited free carriers in the channel. In other words, g_m reduces as less free carriers are available.

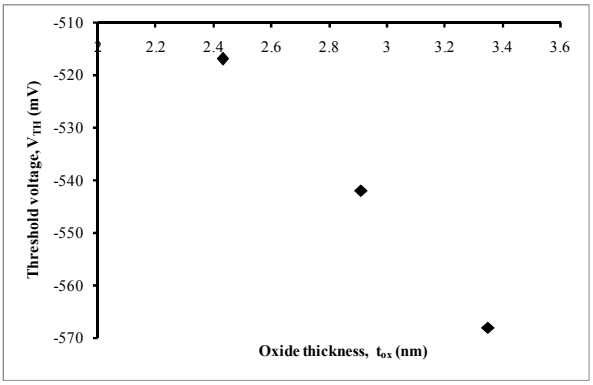

Figure 5: Change of V_{TH} with respect to oxide thickness

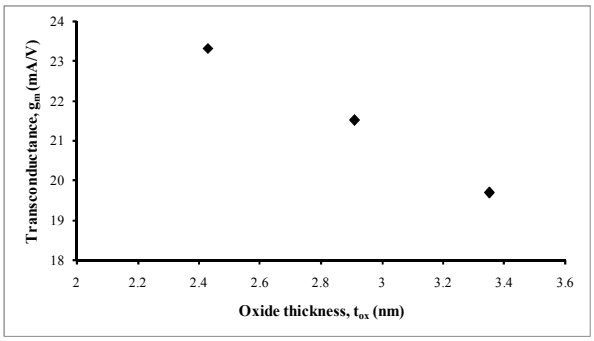

Figure 6: Change of g_m with respect to t_{ox}

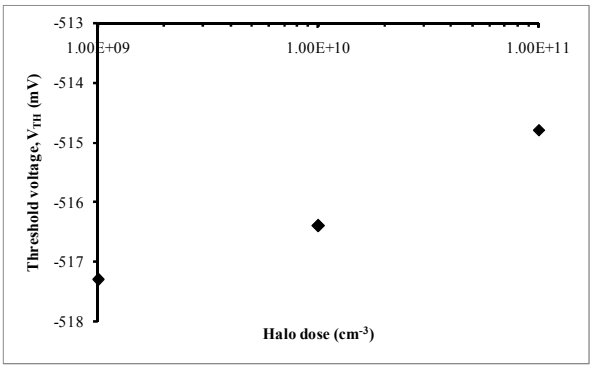

Figure 7: Change of V_{TH} with respect to impurity doping concentration in substrate

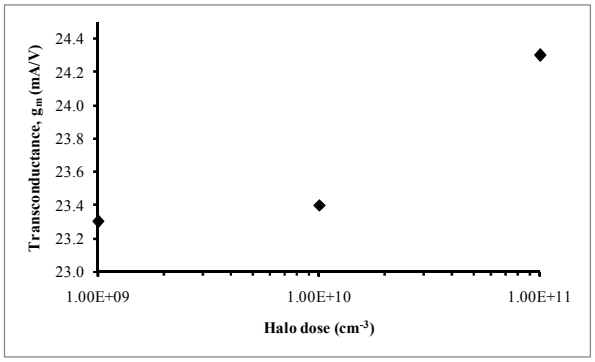

Figure 8: Change of g_m with respect to impurity doping concentration in substrate

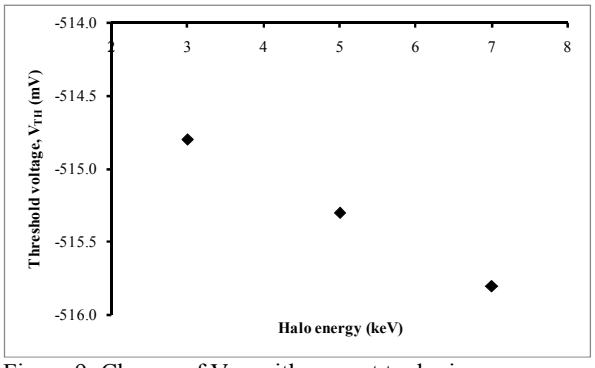

Figure 9: Change of V_{TH} with respect to doping energy

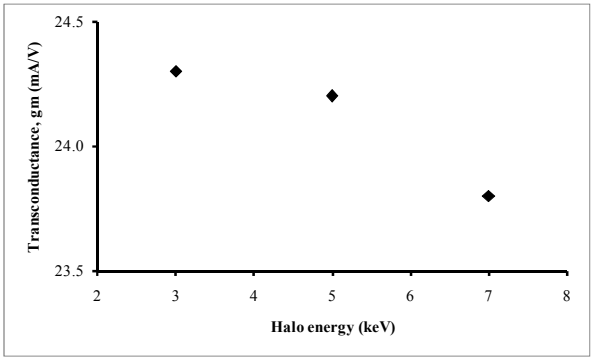

Figure 10: Change of g_m with respect to doping energy

CONCLUSION

The scaling process of MOSFET is no doubt has yielded a significant evolution in integrated circuit technology. The transistor size reduces in several order and thus higher transistor count present in the integrated circuit. The processor, in turn, could provide more functionality as desired in the mass market.

Nevertheless, there are other changes in the scaling process apart from the device dimension. The variation of electrical paramenters are also important as the MOSFET enters the submicron regime. Therefore, this study is carried out to investigate the effect of scaling process on PMOS of 45 nm technology. The investigation is narrowed down to two electrical parameters, which are V_{TH} and g_m.

There are three factors being investigated that may affect the values of V_{TH} and g_m; t_{ox}, doping concentration of dopant in substrate and doping energy of dopant. Simulation results show that both oxide thickness and doping energy has the same effect on V_{TH} and g_m. However, the doping concentration has opposite effect on V_{TH} and g_m compared to the other two factors.

The difference of effect among the three factors lies in the presence of free carriers in the channel. Increment in the doping concentration promotes higher number of free carriers, and thus improves the g_m and reduces V_{TH}. In contrast, increment in both oxide thickness and doping energy suppresses the number of free carriers. This leads to less available free carriers that flow in the channel, which increases V_{TH} and reduces g_m.

Analysis of observation in this work gives a perspective of V_{TH} and g_m variations in PMOS. The three factors investigated in this study could help in optimising those factors to obtain the best I_D. In addition, the analysis also emphasis the importance of the availability of free carriers in device operation.

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