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INVESTIGATION OF THRESHOLD VOLTAGE VARIATIONS IN NMOS

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ABSTRACT

As MOSFET is rigorously scaled down to meet the expected circuit evolution according to the Moore's Law, the issue of threshold voltage (V_{TH}) becoming more dominant in transistor operation. This parameters is worth to be investigated since it dictates the performance of the transistor operation. On top of that, channel length modulation, which related to transistor scaling, plays dominant role in affecting the V_{TH}. The investigation is performed primarily based on transistor modelling that relates the parameters of interest in device operation. It is carried out through simulation work of 45 nm n-type MOSFET (NMOS) in Sentaurus TCAD to see changes in transistor operation. Simulation results suggest that oxide thickness and dopant cocncentration in substrate have significant effect on the V_{TH}. The changes in both parameters are related to changes in oxide layer capacitance and number of minority carriers that essentially affect the V_{TH}.

Key words: threshold voltage • submicron MOSFET • oxide thickness •

INTRODUCTION

MOSFET has long been used as the basic building block in integrated circuits. It offers high switching speed that is very attractive in digital electronic applications. This key feature is attained due to its characteristic that could produce large output current through a small change in gate voltage. Besides, MOSFET is also known for low power consumption due to its characteristic of producing low leakage current. The main reason that made MOSFET relevant for decades is its adaptability through changes in its structure known as scaling process.

The scaling process refers to a process that reducing the gate length of MOSFET to improve the device performance. It also implies reduction of other structure parameters of MOSFET to maintain the device aspect ratio. By specifying a scaling constant, the gate length is reduced compared to the existing dimension. Since the other structure parameters will be reduced due to the same scaling constant, thus a smaller device size will be produced. In addition, the electrical parameters would also be scaled down to match the new gate length. This is done to ensure the device output characteristic is preserved.

The scaling process works very well in terms of miniaturising the device size. In addition, the scaling process also affects the electrical characteristic of MOSFET. The changes of electrical properties are due to changes of how the majority carriers behave when the device is in operation. As such, it is essential to evaluate the electrical properties as the device is undergoing the scaling process.

Threshold voltage, V_{TH}, defines the potential barrier that must be surpassed to allow the output current to flow. Since V_{TH} is related to minimum required gate voltage for MOSFET to conduct current, it is desirable to have the V_{TH} to be as low as possible. This work is carried out with specific goal to investigate the variations of V_{TH} in submicron scale of NMOS. Three device parameters are identified that may affect the variation of V_{TH}, namely oxide thickness, doping concentration of substrate and doping energy of source/drain terminals. Each of the identified factors is expected to have a significant effect on the V_{TH}.

RELATED WORK

The scaling process has regarded as the main factor that drives the evolution of transistor technology in integrated circuit. The scaling process is closely related to variation in fabrication process which can be categorised either as stochastic or systematic variation (Saha, 2014). The success of scaling process is due to its dependence on velocity and mobility of carriers (Khakifirooz and Antoniadis, 2008). A design strategy is needed to achieve a tradeoffs between high performance and low power logic (Zeitzoff and Chung, 2005). High switching speed is desired in the former whereas minimising leakage current is prioritised in the latter.

One of the main challenge in scaling includes high leakage current and electron tunnelling from gate terminal (Zietzoff and Chung, 2002). However, it is anticipated that the scaling eventually would have to cease as the transistor technology is bound to the atom size (Skotnicki et al., 2005). In addition, the scaling process is expected to reach its limit sooner as the tunnelling current and off current dominate in MOSFET (Ning, 2007). Parasitic resistance that caused by source/drain extension also becomes a challenge as the device is further scaled (Plummer, 2000).

Several alternatives have been explored to improve the performance of MOSFET such as metal source/drain terminals (Larson and Snyder, 2006). Metal source/drain terminals are expected to mitigate the electron tunnelling and also minimise the sheet resistance (Zietzoff and Chung, 2002). The future of MOSFET lies on new materials and innovation in device structure that could extend the scaling process (Thompson et al., 2005).

As the MOSFET is scaled into submicron regime, there are other effect on device performance such as non-squasi-static behaviour (Srinivasan and Bhat, 2003). This is critical in RF-based applications. The other significant factor is the reluctance of industries to scale supply voltage according to scaling constant (Ning, 2007). This trend led to problems in device operation such as hot electrons and

oxide reliability. Only when the power dissipation is no longer manageable, then the trend starts to lower power supply to 3.3 V and 2.5 V (Critchlow, 2007). The importance of power supply scaling also related to managing the existing power density, which determines the device reliability (Bohr, 2007).

DEVICE SIMULATION

In this work, simulation of NMOS operation was carried out using Sentaurus TCAD. V_{TH} had been set as the prime output parameter of investigation. Three input parameters had been identified as the factors of V_{TH} variation; oxide thickness, doping concentration of substrate and doping energy of source/drain terminals. Figure **1** exhibits the flow of device simulation carried out in this work. The work flow involved five components in Sentaurus which were Sentaurus Workbench (SWB), Ligament, Sentaurus Device (SDevice), Tecplot and Inspect.

Firstly, the device input parameters were set in the SWB such as the gate length. Each node of input parameters can be run independently to obtain specific output files. Figure **2** shows the snapshot of SWB interface during simulation. During simulation, each node status was represented with a unique colour. For example, a blue node represents a running simulation and an amber node represents a completed simulation. In general, the SWB acts as a tool to give an overview of the whole process in Sentaurus TCAD. Nevertheless, the individual process must be defined first before it appears on the SWB interface.

Next, the changes in oxide thickness were simulated in Ligament. This was done by specifying the oxidation process in Ligament as illustrated in Figure **3**. Ligament tool, in general, is used to simulate the fabrication process carried out in a cleanroom. Oxide thickness will be determined by the length of the oxidation process. At the end of the process simulation, a series of oxidation thickness was obtained to be used in the next step of simulation. The variability of oxide thickness was then used to examine the change in the V_{TH}.

The following step was to obtain the device doping profile in Tecplot. The doping profile was generated according to the doping concentration specified in SWB. The doping profile was only possible once the process simulation in Ligament had completed. It means that any changes in process simulation defined in Ligament affected the doping profile. As shown in Figure **4**, two input files were required in Tecplot which are *<filename>.cmd* and *<filename>.tdr*.

Next, SDevice was used to extract output data of device operation such as current and voltage of interest. In addition, this tool also helped to determine the final solution of all structure variables.

Finally, the electrical characteristic was extracted in visual mode using Inspect. The drain-to-source current (I_{DS}) was one of the main output parameter viewed in Inspect. Two input files were required in this simulation, namely *<filename>.cmd* and *<filename>.plt*. Figure **5** shows the pre-process in Inspect before the output parameters were extracted.

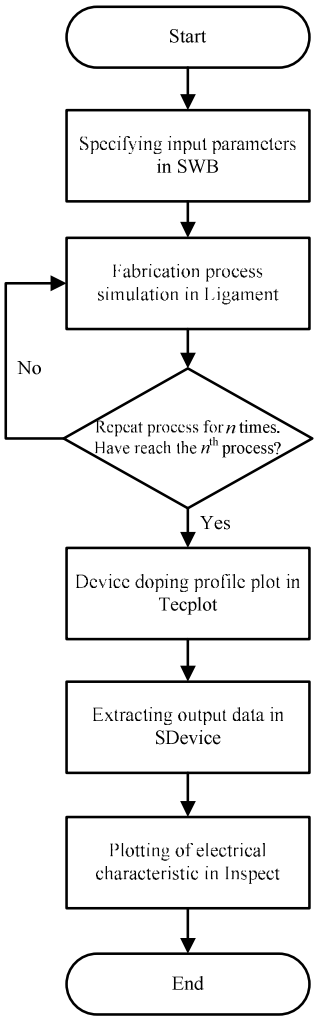

Figure 1: Work flow of device simulation

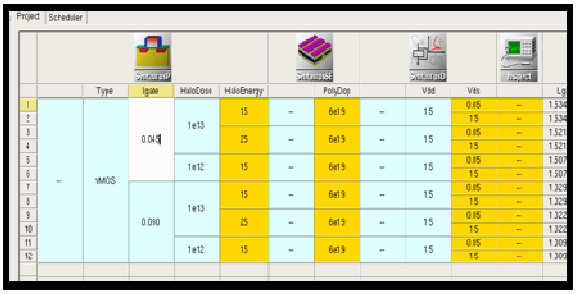

Figure 2: Snapshot of SWB interface

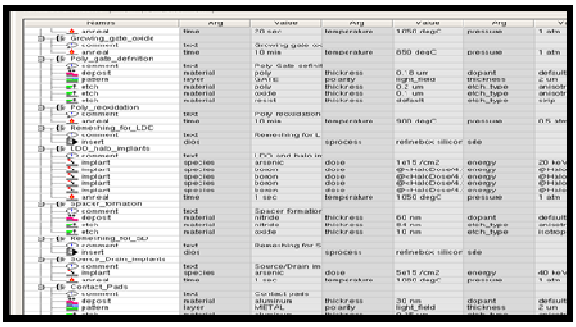

Figure 3: Snapshot of Ligament interface

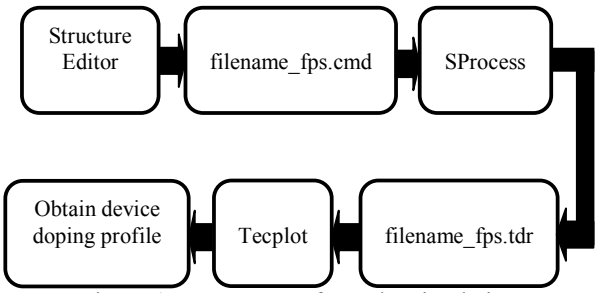

Figure 4: Pre-process of Tecplot simulation

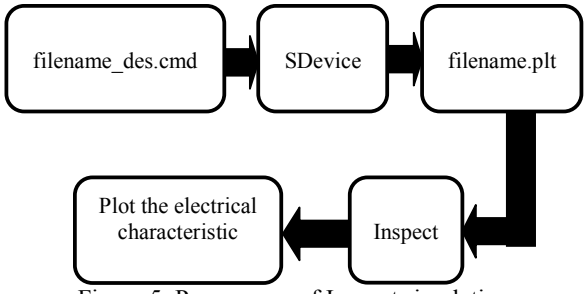

Figure 5: Pre-process of Inspect simulation

RESULTS AND DISCUSSION

Variations of the V_{TH} due to the three factors are presented herein. The three factors are the oxide thickness, dopant concentration in substrate and source-drain doping energy. The results presented are based on simulation of 45 nm NMOS using Sentaurus TCAD tools. The structure of 45 nm NMOS with the corresponding doping concentration is shown in Figure **6**.

The relationship between the oxide thickness and the V_{TH} are failry straightforward. As shown in Figure **7**, the V_{TH} changes in a direct proportion manner with respect to the oxide thickness. The oxide thickness in NMOS is reversely proportional to capacitance of the oxide layer. This is because the oxide thickness acts as the separation distance between two conducting plates of oxide layer capacitance. As the oxide thickness increases, the oxide capacitance will be reduced since the separation of capacitance plate is increased.

The increment in oxide capacitance brings a two-fold effect; reduction in leakage current and reduction in tunnelling current as well. This is true since reduction in oxide layer promotes tunnelling of electron moving from the gate terminal to the substrate. In other words, increasing the oxide layer will mitigate the tunnelling current towards gate terminal and thus increase the on-current between drain and source, I_{DS}. This, in turn, requires a higher potential to be applied on gate terminal to allow current conduction in NMOS. This explains the relationship of a direct proportionality between the oxide thickness and V_{TH}.

The second factor that affects the V_{TH} is the dopant concentration in the substrate. In this work, boron is chosen as the dopant for the substrate in NMOS. Figure **8** illustrates that the V_{TH} increasing linearly as the doping concentration of Boron increases. Assuming that the oxide thickness is kept constant, therefore the increment of doping concentration of Boron will promote higher number of minority carriers in the substrate along the transistor channel. Higher number of minority carriers will essentially produce larger I_{DS}. This is true since the flow of minority carriers is directly proportional to the strength of I_{DS}. However, as in the case of oxide capacitance, the increment of doping concentration of dopant in substrate requires a higher potential at the gate terminal. A higher potential is needed since a higher number of minority carriers need to be swept away from drain to source terminal. Therefore, as the doping concentration of Boron is increased, the V_{TH} of NMOS will increase as well.

The final factor that affect the V_{TH} variations in NMOS is the doping energy at the source and drain terminals. In general, a high doping energy at source/drain terminal is desired. The reason is that a low doping energy will result in a shallow channel which causes high resistivity and impurity absorbance. Therefore, to avoid the shallow channel effect, the doping energy on source and drain terminals is to be kept as high as possible. As shown in Figure **9**, the V_{TH} of NMOS is fairly stable as the doping energy at source and drain terminals increases. The only notable change in V_{TH} is when the doping energy changes from 30 KeV to 35 KeV. Therefore, this observation suggest that the doping energy has insignificant effect on the V_{TH} of NMOS.

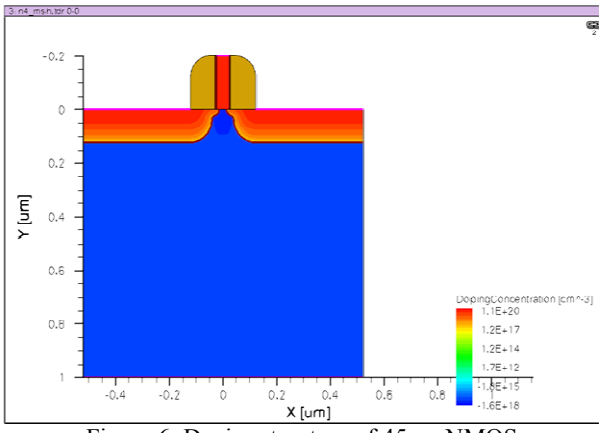

Figure 6: Device structure of 45nm NMOS

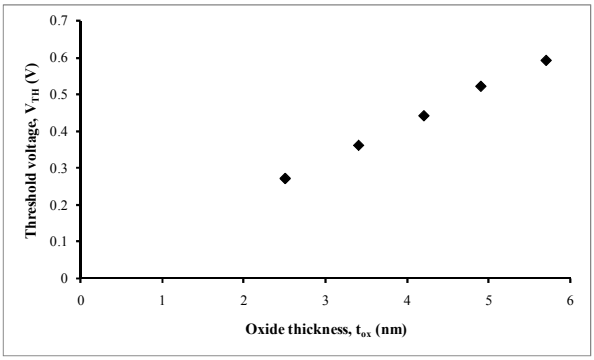

Figure 7: Change of V_{TH} with respect to oxide thickness

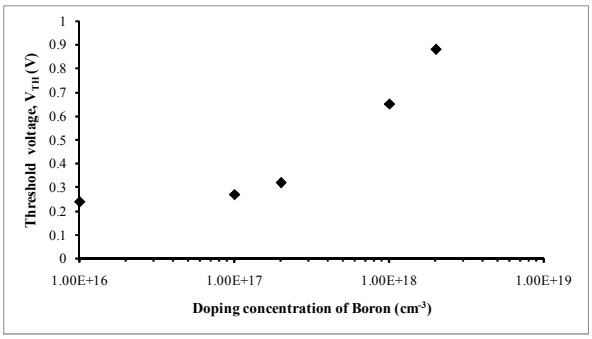

Figure 8: Change of V_{TH} with respect to doping concentration of Boron

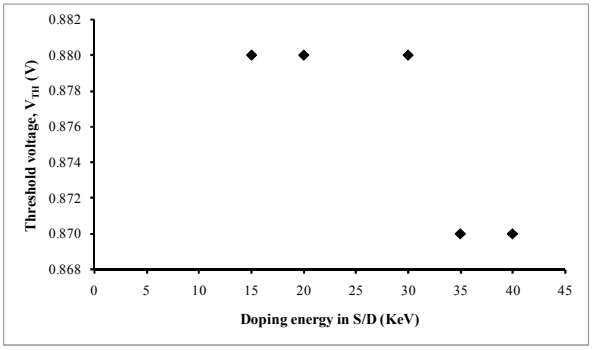

Figure 9: Change of V_{TH} with respect to doping energy in source/drain terminal

CONCLUSION

The scaling process of MOSFET is an essential innovation that supports a higher complexity in integrated circuit design. This is achieved by having smaller transistor size, and hence more transistors can be fit into the same chip area. However, as the transistor size is scaled down even further, it is expected that there are other electrical parameters being affected. This study is carried out to investigate the effect of scaling process on the V_{TH}.

There are three factors being investigated that may affect the value of V_{TH}, namely oxide thickness, doping concentration of dopant in substrate and doping energy at source and drain terminals. Simulation results show that the first two factors are directly proportional with the V_{TH} whereas the last factor has insignificant effect on the V_{TH}.

The change of the V_{TH} with respect to oxide thickness is due to the changes in oxide capcitance when the device is in operation. As the oxide thickness is reduced according to a scaling factor, the V_{TH} is also reduced. In the case of change in doping concentration of dopant in substrate, the V_{TH} changes exponentially as the dopant concentration in substrate is increased. This reflects the relation of the V_{TH} with the number of minority carriers along the transistor channel.

Finding of this study gives an insight of the V_{TH} changes as the channel length is reduced according to the scaling process. Reduction in oxide thickness and doping concentration of dopant in substrate is in favour of smaller V_{TH}. Therefore, a thin oxide layer and low dopant concentration in susbstrate are the key factors that help to lower the V_{TH}, which then improves the device performance.

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