2014 IEEE International Conference on Control System, Computing and Engineering, 28 - 30 November 2014, Penang, Malaysia

FPGA-in-the-Loop Co-simulation of Reentrant Arrhythmia Mechanism in One Dimensional (1D) Ring-Shaped based on FitzHugh-Nagumo Model

Nur Atiqah Adon^{1, 3}, Farhanahani Mahmud^{1, 4}, Mohamad Hairol Jabbar^{2, 5} and Norliza Othman^{1, 6}

¹Cardiology and Physiome Analysis Research Laboratory,

²Manycore System on Chip (MCSoC) Research Laboratory,

Microelectronics and Nanotechnology - Shamsudin Research Centre (MiNT-SRC),

Faculty of Electrical and Electronic Engineering,

Universiti Tun Hussein Onn Malaysia (UTHM),

Batu Pahat, Johor, Malaysia

{³ge130013, ⁶ge130062}@siswa.uthm.edu.my {⁴farhanah, ⁵hairol}@uthm.edu.my

Abstract— This paper presents the simulation of reentrant excitation-conduction of cardiac cells realized by coupling 80 active circuits in one dimensional (1D) ring-shaped based on FitzHugh-Nagumo (FHN) model. 1D ring-shaped cable model is designed using Simulink in order to simulate an action potential signal and its conduction for a hardware design by using HDL Coder to automate the model for Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) code generation. Then, the VHDL design is functionally verified on a Field Programmable Gate Array (FPGA) Xilinx Virtex-6 board using HDL Verifier proving the model through FPGA-in-the-Loop (FIL) co-simulation approach. It can then be downloaded into a target FPGA device for real-time simulations. This novel approach of prototyping cardiac reentrant excitation-conduction provides a fast and effective FPGA-based hardware implementation flow towards a stand-alone implementation to perform complex real-time simulations compared with manual HDL designs.

Index Terms— Reentrant, FitzHugh-Nagumo Model, HDL Coder, FPGA-in-the-Loop, real-time simulations.

I. INTRODUCTION

Cardiac action potential is responsible for conduction of excitation in cardiac tissues and allows the heart to contract rhythmically. Nevertheless, dysfunction of electrical excitation and their spatial propagation can induce abnormal contractions of the heart [1]. Such abnormalities are often called arrhythmia and the vast majority of that disease perpetuated by reentrant mechanism [2]. Reentrant cardiac arrhythmias occur when cardiac tissue is excited repeatedly by the action potential wave that keeps reentering the same anatomical region. Such reentry could lead to ventricular tachycardia that causes extremely rapid excitation of the heart [3]. This potentially causes a fatal risk of the heart's ability to efficiently pump blood throughout the body which could leads to a sudden death.

In order to understand dynamic mechanism of action potential generation and conduction, many mathematical models of cardiac action potential have been developed and analyzed. Mathematical modeling is useful techniques for a computer simulation of cardiac electrical behavior are not associated with such complications. Recent models of the cardiac cells starting from the electrical excitation model of the FitzHugh-Nagumo (FHN) [4, 5], Noble [6, 7], continued by Beeler and Reuter [8, 9], Luo-Rudy [10, 11] Faber-Rudy [12] and many others have been developed to represent different regions of the heart.

With the progress of time, the computational techniques become more advanced but complicated as parameters in the mathematical descriptions and size of the models increase which cause a drawback in the amount of computations for the dynamic simulations of the mechanism. Therefore, to overcome the computational challenge, hardware implementation appears as one of main choices recently that provides valuable tools for electrical excitation modeling [13]. A previous study have provided the analog-digital circuits of hardware-implemented cardiac excitation model designed by using analog circuits and a dsPIC30f4011 microcontroller [14] that could reproduce a real-time simulation of Luo-Rudy based cardiac action potential model. However, the models show some limitations due to its power consumption and physical size.

The aim of this paper is to demonstrate an FHN model based on cardiac excitation-conduction model in one dimensional (1D) ring-shaped cable through fast and effective FPGA implementation flow towards the development of realtime cardiac electrophysiological analysis tool. Simulating this complex model in real-time using software implementation does not produce acceptable computation speed motivating us to proceed with hardware implementation. It is known that the FPGA is suitable for solving higher ordinary differential equation (ODE) with multimillion gate counts and special lowpower packages [15]. At present, the Very High Speed Integration Circuit (VHSIC) Hardware Description Language (VHDL) code for the FPGA hardware implementation is produced by a rapid prototyping method introduced by MathWorks which are MATLAB Simulink and HDL Coder tools. The HDL Coder is used to automate the design process by converting Simulink blocks into VHDL code for FPGA

implementation. For verification of the model, HDL Verifier tool which is also from the MathWorks is then used to verify the designed through FPGA-in-the-Loop (FIL) approaches [16].

The rest of the paper is organized as follows. An overview of the methodology is given in Section 2. Section 3 exposes the results and discusses the resulting outcomes. Finally, concluding remarks and further potential ideas to be explored are given in Section 4.

II. FHN THEORY AND MODELING

Numerical models of cardiac cell are widely used in several studies related to the reentrant arrhythmia to investigate the underlying dynamics of reentrant wave [14]. Basically, these electrophysiology of isolated cardiac cell models are coupled together to perform simulations of action potential (AP) propagation in the cardiac tissue.

One of the models that have been used intensely in modeling the reentrant wave is FitzHugh-Nagumo (FHN) model. The FHN model is described by a set of nonlinear ordinary differential equations (ODEs) that includes two dynamic state variables for describing the excitation and the recovery states of a cardiac cell and the model is able to reproduce many characteristics of electrical excitation in cardiac tissues [17].

Initially, the modified FHN mathematical modeling has been built by blocks from HDL supported library in Simulink for developed design of software is made principally to solve a set of nonlinear ODEs as in Eq. (1) and Eq. (2) to generate action potential (AP) [18].

$$\frac{\partial V}{\partial t} = -V(V - 0.139)(V - 1) - W + I + D\frac{\partial^2 V}{\partial x^2}$$
(1)

$$\frac{\partial W}{\partial t} = 0.008 \left(V - 2.54W \right) \tag{2}$$

- *V* : membrane voltage
- *W* : refractory period
- *I* : diffusion coefficient
- *t* : time and space dependent injected current
- *x* : spatial in one dimension

A cardiac contraction is initiated by propagating electrical waves of excitation. The spread of excitation in the heart occurs associated with the excitability of individual cardiac cells and a close electrical coupling of cardiac cells via gap junctions, thereby allowing propagation of these electrical excitations from cell to cell in tissue [19]. The propagation of action potentials in an excitable tissue is often modeled by using significantly simplified quantitative method that can be represented by the one dimensional (1D) cable model. To describe wave propagation in cardiac tissue, it is necessary to specify the currents resulting from the intercellular coupling, which can usually be approximated by a differential in Eq. (3).

$$\frac{\partial V}{\partial t} = D\left(\nabla^2 V_m\right) - \frac{I_m}{C_m} \tag{3}$$

 V_m : cardiac cell membrane voltage

- D : conductivity tensor (10⁻³ cm²/ms)
- C_m : diffusion coefficient (1µF/cm²)
- I_m : transmembrane ionic current

According to Eq. (3), the cable model of the 1D ring consists of *N* cell models can be illustrated as shown in Figure 1, where R_d is a gap junction resistance and $R_d C_m = (\delta x)^2 / D$. In this study, the circumference of the 1D ring, *L* is assumed as $L=2\sqrt{5}$ cm with $\delta x = 0.005L$, therefore $R_d = 0.5$ k Ω cm². The applied value of R_d is considered in the relevant range that provides a moderate coupling and allows a propagation of the action potential (AP) [17].



Fig. 1. A ring-shaped cable model. The ring model consists of N cell models and gap junction resistance, R [20].

For the rapid design, the HDL coder in the Simulink supports HDL code generation automatically for the FPGA implementation. Moreover, through the FIL simulation from the HDL Verifier, it can increase confidence that the model will work in real world and to ensure it will behave as expected when implemented in the hardware. The HDL Coder automates the design process, from modeling to FPGA implementation, as depicted in Figure 2.



Fig. 2. FPGA rapid design with the HDL Coder and the FIL.

When using HDL Coder, the model needs to be modified into a discrete-time framework with the conversion of floatingpoint to fixed-point data type. The conversion from the floating-point to fixed-point code is subjected to two opposing constraints which are the word-length of fixed-point types must be optimized and the outputs of the fixed-point data types must be accurate. Fixed-point optimization is being done in order to improve performance of the designed model through MATLAB Fixed-point Designer tool as it can reduce implementation cost, provide better performance and reduce power consumption.

III. RESULTS AND DISCUSSION

A. An Implementation of Model-based Design

Figure 3 shows the comparison of the FHN cardiac excitation waveform between the floating point and fixed-point design of the model where panels (a), (b), and (c) indicate the floating points, the fixed-point, and the differences of the floating point and the fixed-point, respectively. Here, the optimal number of word-length and fraction-length for the fixed-point are set to 24 and 22 bits, respectively, which indicate the maximum values that are being used on the blocks systems. Based on the comparison result, the fixed-point data type design produced results that are comparable to the floating-point data type in continuous-time modeling with maximum difference of 0.244mV.



Fig. 3. Comparison of floating point and fixed-point of LR-I model. Panel (a) and (b) represent the floating-point data type and fixed-point data type, respectively. Panel (c) corresponding differences after compare the both of simulation.

Figure 4 shows the top level of the designed FHN 1D cable model using the MATLAB Simulink, where existing subsystems in the FHN model Subsystem block is in three layers within the model. Here, the input clock represents the timing of the stimulation and the output of the membrane voltage visualized by using the scope block.



Fig. 4. The top level of FHN 1D cable model using the Simulink.

The designed FHN model subsystem block is realized by coupling eighty membrane cells of the FHN model together with the diffusion coefficient of $D/\Delta x^2 = 2\text{ms}^{-1}$, where $\Delta x = 0.005L\text{cm}$ is the spatial discretization at position x [18].

B. FPGA-in-the-Loop Co-simulation

The FIL co-simulation is used to verify the model based design in real hardware for the generated VHDL code. Figure 5 demonstrates the model based designed in the Simulink connected with the FPGA Xilinx Virtex-6 board using the FIL simulation which is done through an HDL Workflow Advisor.



Fig. 5. FPGA-in-the-loop co-simulation. Panel (a) and (b) represent the top level of FHN and generated block FIL co-simulation, respectively.

The generated blocks through the FIL workflow corresponding to error analysis between the FIL and the Simulink simulations are shown in Figure 6.



Fig. 6. Generated block for comparison of FIL simulation on FPGA hardware implementation by HDL Coder and Simulink simulation.

Figure 7 (a) and (b) show the conduction of action potential wave produced by the FIL and Simulink simulation respectively, from the first cell to the eightieth cell and the action potential is initiated at the first cell by 250ms of periodical external current stimuli starting at t = 100ms. Both results are noted to be comparable to the waveform in FHN model [4, 18] as both waveforms showed the same result of action potential duration around 100ms which gave the result of no difference between them as shown in Figure 7 (c). Apparently the results in Figure 7 (a) and (b) also show a high speed of action potential conduction which largely influenced by the value of the diffusion coefficient applied.



Fig. 7. Simulated 80 cells conduction of FHN model waveforms. Panel (a) and (b) represent the cardiac excitation-conduction generated by the FIL simulation and Simulink simulation, respectively. Panel (c) shows zero error between FIL and Simulink simulation.

C. Initiation of Reentrant in the Ring-shaped Cable Models

In this project, a simulation of anatomical circus reentry around the closed ring cable consists of eighty cells of the FHN model has been performed. It is known that the reentry occurs because the present of unidirectional conduction block of conducting action potential and excitable gap. Unidirectional block occurs when an action potential wave-front fails to propagate in one particular direction, but can continue to propagate in other directions. Here, a unidirectional block was induced by using the so called S1-S2 protocol where single or several impulsive stimulations referred to as S1 were applied at a given location of the ring, and then another impulsive stimulation referred to as S2 was applied at a different location from the S1 site in a particular time.

As shown in Figure 8, two S1 stimulations were applied to the ring at the first cell at time t = 100ms and t = 250ms (red arrows marked the area and the time where the simulations were applied), pacing the excitation of the medium. Each stimulus evokes excitation at the stimulated site, generating two conducting action potential. The S2, corresponding to an ectopic focus excitation in the real heart, was then applied at a position slightly away from the S1 site at an appropriate time interval after the second application of S1. For the result, S2 was applied at the nineteenth cell at t = 460ms, where the time interval of S1 and S2 was 110ms after the S1 stimulation. This causes a generation of a single AP by the S2 from mechanisms of unidirectional block, initiating the circus movement reentrant wave.



Fig. 8. A space-time diagram showing membrane voltage as a function of time and position around the ring-shaped cable presented by FHN model using Simulink.

D. FPGA stand-alone implementation

Towards a stand-alone FPGA hardware implementation, the model will be developed by FPGA Virtex-6 XC6VLX240T ML605 development board which is suitable for solving higher order of ODEs and real-time applications with low power consumption as illustrates in Figure 9. The clock is the configuration clock bit and the configuration data is slide after all rising edge of this clock to start the simulation through a switch. Here, the FPGA offers a direct on-board interface which is FPGA Mezzanine Card (FMC) daughter card connector as well as many high level system capabilities, which is a dual channel 16 bits to convert digital-to-analog signal with maximum voltage of 2.5 V [21-23]. The action potential waveform in real-time data from the system will be acquired using a data logger and displayed on the LCD in which the data acquisition system must remain tethered to a computer to acquire data.



Fig. 9. Configuration image of the FPGA design.

IV. CONCLUSION

In conclusion, rapid FPGA-based hardware implementation flow of the FHN model of the anatomical circus movement reentry in 1D ring-shaped of cardiac excitation-conduction cable model has been successfully done using the MATLAB Simulink HDL Coder which has been verified using the FIL simulation on the XC6VLX240T FPGA Xilinx Virtex-6 board. Good agreement between simulation results from the MATLAB Simulink and the HDL Coder generated code reveals that the HDL Coder provides very efficient technique in rapidly prototyping the model on FPGA. This novel hardware prototyping flow for cardiac reentrant excitation-conduction model will be very useful for exploring hardware implementation trade-off of more complex models which is not practical when using manual HDL designs. Ongoing research is focusing on the stand-alone hardware implementation to perform real-time simulations of realizing large-scale implementations on the FPGA. Reentrant wave termination and phase resetting of the sustained reentry will be further explored to demonstrate the capability of the proposed simulation in biomedical application systems.

ACKNOWLEDGEMENT

The authors gratefully acknowledges the support by Fundamental Research Grant Scheme (FRGS) (vote no. 1053), under Ministry of Higher Education Malaysia.

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