Optimization in MATLAB for Cardiac Excitation Modeling Towards FPGA Standalone Simulation Tools

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Abstract. In past few decades, most of the modern electrophysiological concepts and methods were developed by the computational technique extensively to compute the cardiac action potential in nerve cells. Thus, tissue models consisting of a large number of single cell models cause a problem in the amount of computation required to obtain meaningful results from simulations. One of the solutions to this problem is by implementing the simulation through hardware modeling using a Field Programmable Gate Array (FPGA). Here, a research on developing a real-time simulation tool responsible for reentrant excitations in a ring of cardiac tissue based on the FitzHugh-Nagumo (FHN) model has been carried out by using a Xilinx Virtex-6 XC6VLX240T ML605 development board FPGA. In order to invest some of the time savings for creating the FPGA prototype, rapid prototyping method introduced by MathWorks which are MATLABSimulink and its HDL Coder toolbox have been used to automate the algorithm design process by converting Simulink blocks into Hardware Description Language (HDL) code for the FPGAusing afixed-point data type in discrete-time framework. In this paper, the method and the optimization of the HDL design through the MATLAB Simulink have been discussed and the model is successfully converted into an optimal fixed-point VHDL design and the operating frequency is increased from 26.29 MHz to 53.61 MHz by using HDL Coder.

Introduction

The mathematical modeling computation by using hardware is used to generate action potential generation and conduction in order to study the underlying mechanism of the human ventricular cells since it is not associated with experimental problems.Until now, many models of the cardiac cells have been developed to represent different regions of the heart [1, 2]. With the progress of time, the computational techniques become more advance but complicated as parameters in the mathematical descriptions and size of the models increase which cause a drawback in the amount of computations for the dynamic simulations of the mechanism. Therefore, to overcome the computational challenge, hardware implementation using a Field Programmable Gate Array (FPGA) appears as one of main choices recently which able to provide valuable tools for electrical excitation modeling [3].

Nowadays, model-based development is common practice with a wide range of specialized software tools for modeling and simulation such as MATLAB Simulink.Through HDL Coder toolbox, it gives opportunities for obtaining hardware descriptions without handwriting of Hardware Description Language (HDL) code and for rapid prototyping in order to design algorithms on FPGA whereas designingusing a manual coding technique is tedious, time consuming and error prone. On the other hand, automatic code generation lets researcher to make changes in the design level

model, and to produce an updated HDL implementation in minute by regenerating the HDL code. It saves a lot of time, while the generated code contains some optimizations to meet speed-area-power objectives for the FPGA [4].

The design of FPGA hardware implementation using MATLAB Simulink software is commonly done using floating-pointdata types in design-environments. In most hardware designs, a high-precision floating-point implementation is often too much of a luxuryand the hardware cost estimation block calculate FPGA hardware utilization in terms of slice registers, flip-flops and look-up tables (LUTs) [5]. Hardware requirements such as area, power consumption, and operating frequency all demand more economical representations of the signal. Therefore, it is necessary to convert the floating-point model into fixed-point for speed and efficiency reasonsespecially in embedded systems. The fixed-point implementation reduces implementationcost, provides better performance and reduces power consumption [6, 7].

The conversion from floating-point designs to fixed-point code is subjected to two opposing constraints which are the word-length of fixed-point types must be optimized and the outputs of the fixed-point data types must be accurate.However, fixed-point conversion is quite challenging and time consuming, typically demand 25 to 50 percent of the total design and implementation time [8].A fixed-point number consists of a sign mode bit either 0 if the data is unsigned or is 1 if the data is signed and a pair of integerswhich are called as word-length (WL) and fraction-length (FL) of the parameters. Larger values WL and FLwill give better performance and lower bit error but the design consumes larger resources in FPGA, optimum fixed-point design is required to meet the desired accuracy.

Through this project a *Fixed-Point Advisor*in HDL Coderis used as an interactive process which ableto accelerate the conversion process from floating-point to fixed-point algorithm. It also verifies the generated fixed-point code by comparing the floating and fixed-point result [9].Besides, manual conversion also can be done furthermore to get the optimum fixed-point design afterward. Because of these benefits of MATLAB Simulink for FPGA design, in this paper, fixed-point optimization through HDL Coder is presented in order to get the truly optimum performance of FPGA implementation for FHN cardiac modeling.The FHN model is described by a set of nonlinear ordinary differential equations (ODEs) that includes two dynamic state variables for describing the excitation and the recovery states of a cardiac cell and the model is able to reproduce many characteristics of electrical excitation in cardiac tissues.

Design Methodology

Model-based Design of Cardiac Excitation. Basically, the MATLAB Simulink HDL Coder from MathWorks has been applied for rapidly prototyping algorithms on FPGA through hardware description language (HDL) codes generation from the designed Simulink blocks of the FHN model [10].Initially, the modified FHN mathematical modeling [11] has been built by blocks from *hdlsupported* library in Simulink to solve a set of nonlinear ODEs as in Eq. 1 and Eq. 2in order to simulate an action potential generation and conduction of cardiac cells.

$$\frac{\partial V}{\partial t} = -V(V-0.139)(V-1)-W+I+D\frac{\partial^2 V}{\partial x^2} \quad (1)$$

$$\frac{\partial W}{\partial t} = 0.008(V-2.54W) \quad (2)$$

Here, *V*is a membrane voltage, *W* is a refractory period, *D* is a diffusion coefficient, *I*is a time and space dependent injected current. Generally, the designed and verified FHN model using the Simulink is initially represented by continuous time modeling in a floating-point data types.However, for the FPGA hardware implementation, conversion into a fixed-point data types in discrete-time framework is needed to be done during the process of designing the modeling

algorithm. Moreover, a WL and FL optimization of the fixed-point is one of challenging aspects of implementing an algorithm on a FPGA that needs to be considered here to enhance the performance in terms of power consumption and design area. The Simulink blocks of the HDL design model is as shown in Fig. 1 for single cell FHN model. As can be seen in Fig. 2,the simulation result of action potential generation and the recovery variablevarying against time by the FHNmodel based numerical cardiac excitation in single cellare as shown in Fig. 2(a)andFig. 2(b), respectively.
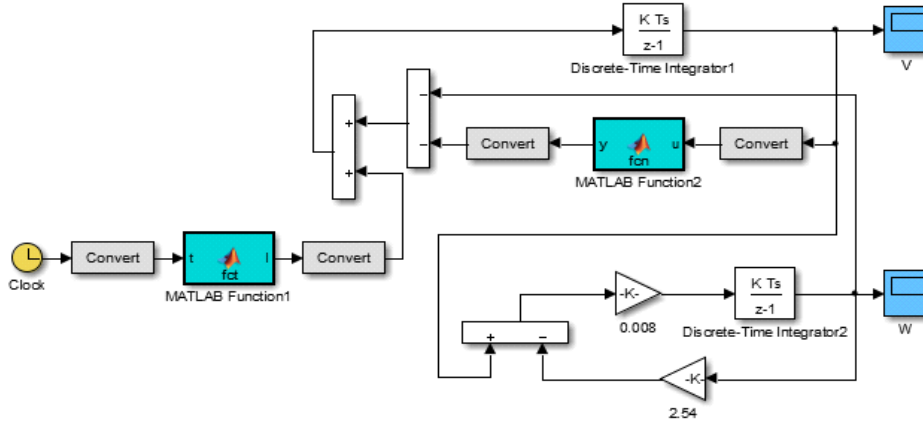

Fig. 1: The FitzHugh-Nagumo model of single cell by using Simulink

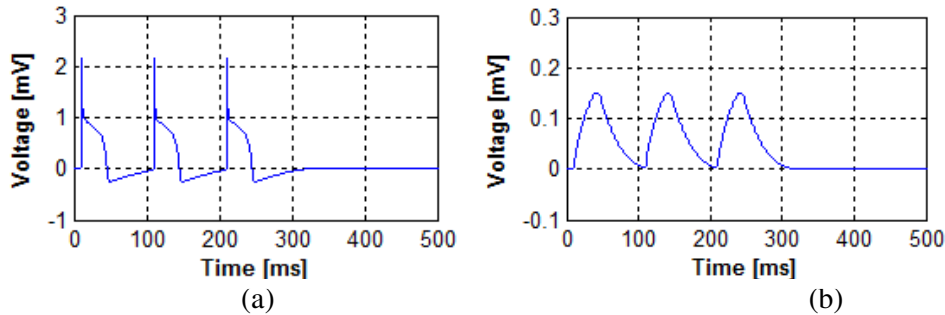|	
(a)	(b)

Fig. 2: The action potential and recovery state waveforms of single cell produced by the FHN model. (a) and (b) represent the time variance of membrane potential and the time variance of recovery variable, respectively.

Results

Fixed-point OptimizationUsing HDL Coder. According to fixed-point optimization process, appropriate WL and FL applicable to the design model have been proposed. In addition, the WL and FL values proposed by the *Fixed-Point Advisor* also have beenused as a reference to improve the optimization further by manually reduce the proposed WL and FL while the accuracy of the simulation results are maintained. As a result of the optimization, three optimum values of WL and FL are used for the optimization processes which are (24, 22), (48, 44) and (96, 88). These values indicate the maximum values that have been set in the block system designed.From these three optimum fixed-point values, the VHDL codes are generated through *HDL Workflow Advisor* in the HDL Coder and then, ISE Design Suite 14.6 is used to analyze the hardware utilizations in terms of slice registers and slice LUTs, operating frequency and power consumption of the HDL design model.

The overall system is implemented on a Xilinx Virtex-6 XC6VLX240T ML605 development board FPGA with 200MHz working frequency, which has 301440 of slices registers and 150720 of slice LUTs and Table 1 shows the FPGA implementation summaryof hardware performance for single cell of FHN model. In terms of area, fixed-point (24,22) data types requires less slice registers (0.02%) and slice LUTs (0.05%) with 37 mW power consumption at 53.61 MHz speed. In comparison with larger fixed-point (48, 44) and (96, 88), it can be clearly seen that the

minimumfixed-point (24,22) implementation requires less complicates mapping which is due to the complex algorithms and edge problem that occurs with maximize fixed-point data types. Moreover, the fixed-point data types which are (48, 44) and (96, 88) implementation consumes more resources, hence for fixed-point (48, 44), 0.02% and 0.13% of more area for slice registers and slice LUTs, respectively are required and 15mW of more power is obtained with 32.90 MHz clock frequency. Whilst, 0.06% and 0.69% of more area for slice registers and slice LUTs, respectively is needed to implement the fixed-point (96, 88) data types and 61 mW more power is obtained with 26.29 MHz maximumfrequency.From this analysis result of performance for the HDL design model, it can be described that the fixed-point optimization reduces the area in terms of slice registers and slice LUTs which leads to the low power consumption and maximum operating frequency.

Table 1: Hardware performance results of a single cell of the FHN model for the proposed fixed-point data types.

Parameters	Proposed fixed-point data types		
	Fixdt(1,24,22)	Fixdt(1,48,44)	Fixdt(1,96,88)
Number of slice registers	59 (0.02%)	121 (0.04%)	227 (0.08%)
Number of slice LUTs	81 (0.05%)	273 (0.18%)	1111 (0.74%)
Maximum frequency [MHz]	53.61	32.90	26.29
Power consumption [mw]	37	52	98

Cellular and Tissue Level. Basically, electrophysiology of isolated cardiac cell models are coupled together to perform simulations of an action potential propagation in the cardiac tissue and it is often modeled by using significantly simplified quantitative method that can be represented by the 1D cable model. Here, the optimal number of WL and FL are set to 24 and 22 bits, respectively for the conduction simulation by extending the number of the FHN cell model to twenty.The comparison ofhardware performance for a single cell and twenty membrane cells is as shown in Table 2. In summary, for the conduction simulation, the results indicate that the optimum fixed-point provides the area for slice registers by 0.38% and slice LUTs (1.54%) which show that the number of hardware utilization make greater when the number of cell is increased. In terms of maximum frequency, twenty cells yields to a slightly lower value of 49.83 MHz and consumes slightly more power by 367mWcompared to the single cell. It is important to note that these changes yet still under consideration for a reasonable performance.Moreover, according to the accurate result in Fig. 3, thevalue of the fixed-point for the single cell can be directly used to extend the number of cell for the action potential propagation in tissue level.

Table 2: Hardware performance results of a single cell and twenty cells of the FHN model.

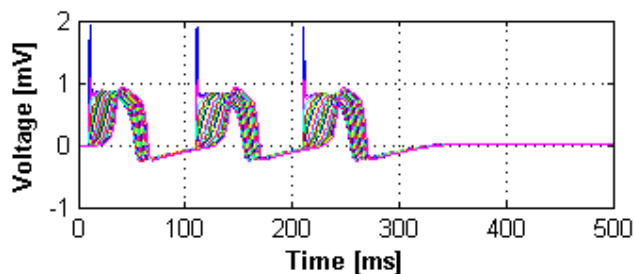| Parameters	Fixdt(1,24,22)	
	Single cell	Twenty cells
Number of slice registers	59 (0.02%)	1150 (0.38%)
Number of slice LUTs	81 (0.05%)	2315 (1.54%)
Maximum frequency [MHz]	53.61	49.83
Power consumption [mW]	37	367

Fig. 3: Simulated twenty cells conduction of FHN model waveforms.

Concluding Remarks

In conclusion, the system design of FHN model of cardiac excitation-conduction for the FPGA hardware implementationon the Xilinx Virtex-6 XC6VLX240T development board is successfully done using the Simulink HDL Coder.The HDL Coder in MATLAB provides very efficient in rapid design to generate the VHDL code automatically. Here, the fixed-point optimization of the HDL design model and its hardware performanceanalysis have been done in obtaining an optimum value of the WL and FL that will increase the operating frequency from 26.29 MHz to 53.61 MHz in order to produce reliable simulation results through the FPGA implementation. In agreement with the results from the comparison studies of the fixed-point optimization, it shows that there isa tradeoff between the maximum frequency and the power consumption in order to achieve a reasonable performance of the FPGA. For future work, a stand-alone FPGA hardware implementation of the optimized HDL design model will be conducted towards real-time simulations of cardiac excitation for analysis tools of electrophysiological mechanism.

Acknowledgement

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