Voltage Clamp Simulation of Cardiac Excitation: Field Programmable Gate Array (FPGA) Implementation

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Abstract. This paper presents the simulation study of voltage clamp technique that enables to analyze current-voltage (*I-V*) characteristics of ion currents based on Luo-Rudy Phase-I (LR-I) model by using a Field Programmable Gate Array (FPGA). Here, the *I-V* relationship presents the characterization of each ion channel by a relation between membrane voltage, V_m and resulting channel current. In addition, the voltage clamp technique also allows the detection of single channel currents in biological membranes and is known to be applicable in identifying variety of electrophysiological problems in the cellular level. As computational modeling needs a vast amount of simulation time, a real-time hardware implementation using FPGA could be the solution as it provides high configurability and performance, and able to executes in parallel mode operation for high-performance real-time systems. For rapid prototyping, MATLAB Simulink software that provides a link with the FPGA has been used to design the algorithm. Simulink HDL Coder capable to convert the designed MATLAB Simulink blocks into hardware description language (HDL). As a result, the MATLAB Simulink successfully simulates the voltage clamp of the LR-I excitation model and identifies the *I-V* characteristics of the ionic currents through Xilinx Virtex-6 XC6VLX240T development board. According to the results of *I-V* characteristics for six ionic currents in the LR-I model, a fast inward sodium current (I_{Na}), a slow inward current (I_{si}), a time-dependent potassium current (I_K), a time-independent potassium current (I_{K1}), a time-independent plateau potassium current (I_{Kp}) and a background current (I_b), there are two types of current; time-dependent and time-independent. The time-independent currents which are the I_{K1}, I_{Kp} and I_b have a steady-state *I-V* relationship and the time-dependent currents which are the I_{Na}, I_{si} and I_K often referred to as having a transient *I-V* relationship but is asymptotic to the steady-state *I-V* relationship.

Introduction

Voltage clamp technique allows the detection of single channel currents in biological membranes and is known to be applicable in identifying variety of electrophysiological problems in the cellular level. During the implementation of the voltage clamp to the cell, the membrane potential is kept at a controlled value which is typically at several constant levels with stepwise changes to record the transmembrane current [1]. This technique has contributed to the understanding of the electrical behavior of the current-voltage (*I-V*) characteristics of the ionic currents [2,3,4]. Here, the *I-V* relationship presents the characterization of each ion channel by a relation between membrane

voltage, V_m and resulting channel current. Due to a tedious and an expensive procedure of the voltage clamp experiment, a simulation approach of the voltage clamp is more preferred as it is easier and cost effective. However, simulating the dynamics of cellular models requires a significant amount of computational processing time which would increase a time required for computer simulation of the models [2]. In addition, the voltage clamp method needs to be developed by real-time system because it requires the real-time evaluation and injection of simulated membrane current. In order to solve the problems, the real-time hardware implementation is needed to model the *I-V* on ionic currents.

In [5,6,7] Real-time analog-digital hybrid model has been developed in order to perform *I-V* relationship of six ionic currents which are a fast inward sodium current (I_{Na}), a slow inward current (I_{si}), a time-dependent potassium current (I_K), a time-independent potassium current (I_{K1}), a time-independent plateau potassium current (I_{Kp}) and a background current (I_b) based on the Luo-Rudy Phase-I (LR-I) model [8] for hardware implementation. However, one of the ionic currents, which is a fast sodium inward current, I_{Na} was not quantitatively comparable because the I_{Na} produced by hybrid model relatively smaller than the LR-I model since it was developed by analog circuit. Therefore, digital implementation of Field Programmable Gate Array (FPGA) is one of the solutions needed to solve the analog problem because it is capable to run in real-time simulation, and it can be adapted to any changes in design by dynamic reconfiguration. FPGA could be the solution as it provides high configurability and performance and also executable in parallel mode operation [9,10]. Thus, a main objective of this paper is to design the quantitative description of the six ionic currents of the LR-I model of single biophysical cellular membrane for voltage clamp simulation by using the FPGA.

The structure of this paper is as follows. Discussion on the methodology with an overview of the proposed system applications is presents in next section. Research findings are presented on the next section. Finally, concluding remarks are given in the last section of this paper.

Design Methodology

In this research, voltage clamp simulation is developed based on the LR-I model [8]. The LR-I is developed to model the generation of cardiac excitation for mammalian ventricular cell. This model is chosen because it well described the six ionic currents that retain enough structure of basic currents involved in cardiac excitation to reproduce exact AP morphologies [11] and is flexible enough that the parameters can be fitted to replicate accurately the properties and dynamics of other complex ionic models as well as experimental data [12-13] such as action potential duration (APD), thresholds for excitation, upstroke velocities, minimum APD before reaching conduction block, and phase-locking response characteristics to current stimulations. Based on the previous work, the LR-I algorithm has been done for FPGA hardware implementation [14-15]. The work is designed by using the MATLAB Simulink that gives an opportunity for obtaining Hardware Description Language (HDL) code without handwriting of the HDL code and by using an automatic code generation process [10].

Here, for the voltage clamp simulation based on the LR-I, the MATLAB Simulink blocks are designed to represent the six ionic currents. According to the voltage clamp method, the changes of six ionic currents can be monitored based on the input of several values of membrane voltage to establish the *I-V* relationship of a certain ionic current. Fig. 1 shows the voltage clamp model for the ionic current I_{Na} designed using the MATLAB Simulink for FPGA rapid prototyping. Based on the Fig. 1, mathematical equations mainly consist of Ordinary Differential Equations (ODEs) in the LR-I are designed inside the subsystems.

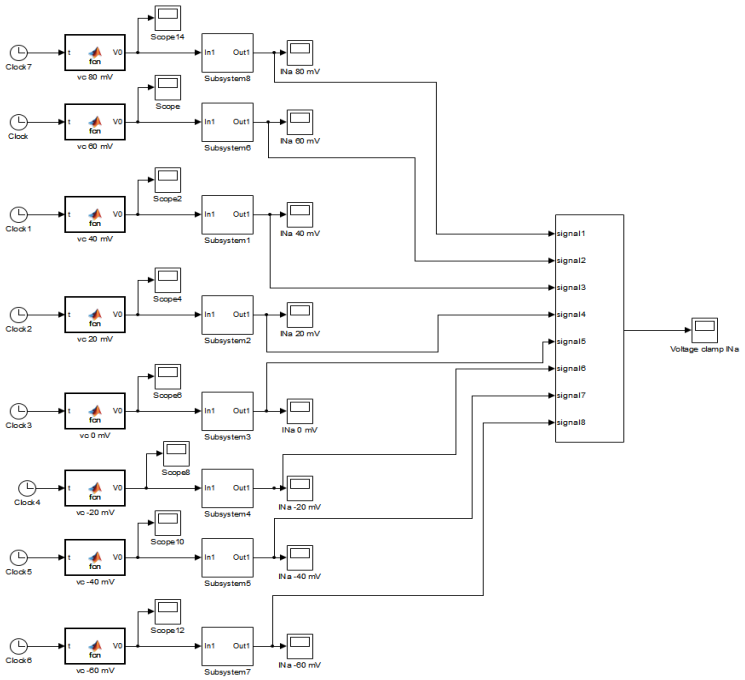
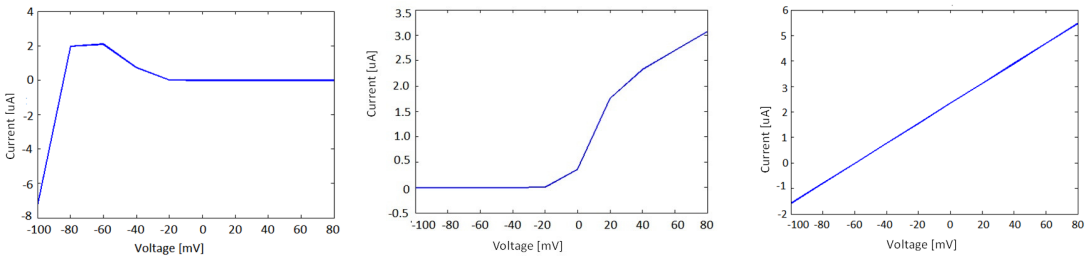


Fig. 1: The designed MATLAB Simulink blocks for the voltage clamp simulation of I_{Na}.

Results

According to the designed Simulink blocks for the voltage clamp of six ionic currents based on the LR-I, the simulation studies are done by applying the input clamped voltages of 80 mV, 60 mV, 40 mV, 20 mV, 0 mV, -20 mV, -40 mV and -60 mV to each of the six ionic channels, in order to produce the *I-V* characteristic of the ionic currents. From the *I-V* characteristics obtained, I_{K1}, I_{Kp} and I_b are classified as the time-independent currents, whereas, I_{Na}, I_K and I_{si} are classified as the time-dependent currents.

Time-independent ionic currents. Fig. 2(a) shows the result of the *I-V* relationship of I_{K1}. The LR-I time-independent potassium current, I_{K1} plays a role to maintain the resting potential as it flows at negative potential. The LR-I time-independent plateau potassium current I_{Kp} is activated during the plateau phase of the action potential along with the other potassium currents to restore the cell to its resting state. This current does not flow at low but at high membrane potential. A graph of the *I-V* relationship of I_{Kp} for the LR-I model designed by using the MATLAB Simulink is depicted in the Fig. 2(b). The background current, I_b in the LR-I, is a composite current representing the hodgepodge of other currents left in the cell. The *I-V* relationship of this current is a linear function of membrane potential. Plots of the *I-V* relationship of I_b is shown in Fig. 2(c). These *I-V* relationships of I_{K1}, I_{Kp} and I_b obtained from the MATLAB Simulink are generally comparable to the features of LR-I model [8].



(a) (b) (c)

Fig. 2: Simulated *I-V* characteristics waveform. Panels (a), (b) and (c) represents corresponding *I-V* of I_{K1}, I_{Kp} and I_b, respectively.

Time-dependent ionic currents. The fast inward sodium current I_{Na} in the LR-I causes the rapid upstroke of the action potential. A short time-constant behavior of I_{Na} is reproduced by using the MATLAB Simulink blocks as shown in Fig. 3(a). Dynamics of I_{Na} are analyzed by plotting the ion current over time in response to the voltage step inputs as refer to the voltage clamp experiment with various clamp voltage from -60 mV to 80 mV by voltage clamp step of 20 mV. The LR-I time-dependent potassium current I_K, is activated by the increase of the membrane potential and it is not activated until the cell returns to its resting state. A long time-constant behavior of I_K is reproduced by using the MATLAB Simulink. The dynamic response of the current to the voltage step shown in Fig. 3(b). The slow inward current I_{si} flows due to the entry of Na^+ during the plateau phase. I_{si} changes slowly over time. Fig. 3(c) illustrates the dynamics response of I_{si}. These *I-V* relationships of I_{Na}, I_K and I_{si} from the MATLAB Simulink are generally comparable to the features of LR-I model [8].

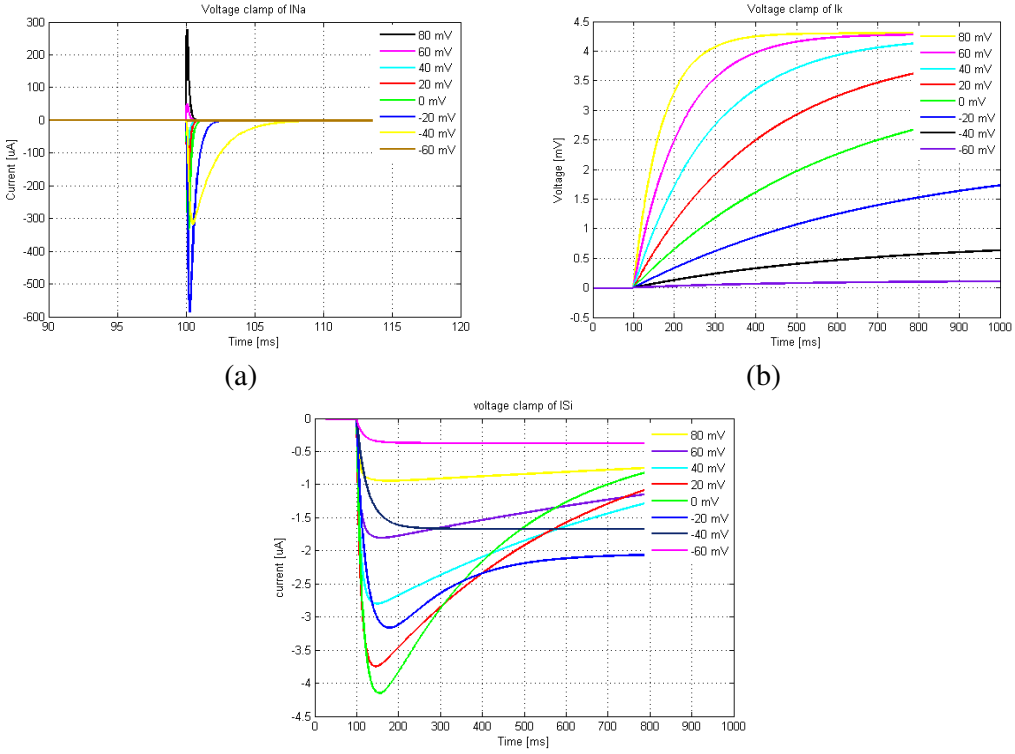


Fig.3: Luo-Rudy phase I model in response to various intensity of the voltage step (from -60 mV to 80 mV) for an initial holding voltage of -85 mV. Panels (a), (b) and (c) represents corresponding voltage clamp waveform of I_{Na}, I_K and I_{si}, respectively.

Concluding Remarks

In conclusion, the AP dynamics is successfully designed by using MATLAB Simulink that could generate the AP that is quantitatively comparable to the previous LR-I model [8]. This mathematical model is designed using MATLAB Simulink in order to implement it on the FPGA since this graphical user interfaces have significant link in order to auto-generated HDL code that will be used for FPGA board programming afterwards. In order to develop FPGA algorithm design by using MATLAB Simulink, several processes have been performed. These include the process of designing algorithm using a fixed-point data type in discrete-time system using the Simulink HDL supported libraries and applying optimization in setting the value of the fixed-point data type to enhance the performance of the designed system according to the speed, power consumption and hardware utilities. For future work, the designed model will be implemented on FPGA board for the stand-alone implementation of the system.

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