Characterizations of FPGA Chip Electromagnetic Emissions Based on GTEM Cell Measurements

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Abstract—**Miniaturized, dense integration and high operating frequencies of FPGAs are factors contributing to electromagnetic emissions. Consequently the radiation issue that used to be discussed at PCB level has shifted to component level. Thus it is of interest and challenging to investigate chip electromagnetic performance. GTEM cell is widely accepted to characterize chip emission and the common measurement practice is mounting the device under test at the GTEM cell body. This paper presents an alternative approach to measure electromagnetic emissions by locating the entire FPGA test board inside the GTEM cell instead of mounting it at the wall of the cell. Before measurements, the FPGA board is properly shielded with metallic enclosure to avoid unintentional contribution from supporting components on the board. During measurements, the shielded FPGA board is arranged in horizontal or vertical positions and for each position the FPGA chip is configured with two different logic circuits. The results have shown a significant impact of FPGA chip positions and IO pins on the electromagnetic emissions.**

I. Introduction

Today, sophisticated integrated circuits (ICs) with highly dense integration and clock speed sustain continuing growth in advance electronic systems. Endless demand to create even better electronic systems is a key factor for the development. Consequently the electromagnetic compatibility (EMC) problem that used to be discussed at the printed circuit board (PCB) level has shifted down to the component level. Many literature studies have reported the contribution of ICs as potential source of electromagnetic emissions (EMEs) in near future due to new process technology, increasing the number of chip IOs and operating frequency [1, 2].

Preceding works have established SAE J1752/3 [3] and the IEC 61967-2 [4] documentations as standard procedures for evaluating radiated emission from ICs in the frequency range 150 kHz to 1 GHz. As suggested, standard TEM cells and broad-band TEM or GTEM cells are accepted as the suitable test facilities to characterize EMEs of IC. Fig. 1 shows the measurement setup where the IC test board is mounted on the cell wall while the IC, which is device under test (DUT), is inside the cell. This setup ensures the radiation is merely contributed by IC under test, and the potential emission contributed by other noise sources can be eliminated. Unfortunately, the setup only allows horizontal positioning of the chip. The drawback is the possibility of neglecting current loop sources in other positions which might be significant sources of emission.

In this paper, we will report on preliminary results of an attempt to characterize radiated emission of a FPGA chip by placing the whole FPGA test board inside a GTEM cell. The EMEs of the FPGA chip are evaluated in horizontal and vertical positions in order to improve the limitation of standard measurement setup that tends to neglect horizontal radiating loop. The 3D finite element radiation simulation in [5] has shown evidence that chip feed-through between package leads and PCB is identified as a crucial EME problem. This finding will be experimentally proven in our work by manipulating a simple toggle flip flop (TFF) logic circuit via a tri-state buffer gate in managing the connection between virtual pins of the circuit to physical pins of a FPGA chip.

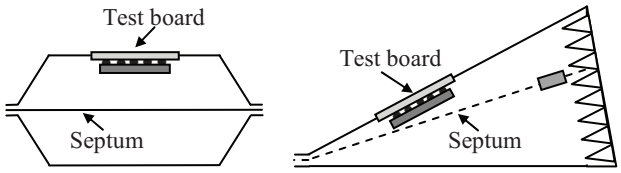

Fig. 1 Evaluation of EME of IC using (a) TEM cell and (b) GTEM cell

II. Field Coupling Mechanism of Current Loop

IC current loops are the primary radiation sources behaving as magnetic and electric dipoles to radiate undesired EMEs of IC [6]. The coupling mechanism of a current loop on the TEM cell septum is investigated in [7]. The IC pulsed currents are the consequence of transistor simultaneous switching activities of silicon die which driven by a clock signal. These currents are commonly drawn from source terminal and return via ground terminal of IC. Generally, the pulsed currents flowing along a path consists of package leads, wire bonding and interconnections on silicon die as shown in Fig. 2 (a). Fig. 2(b) illustrates decomposition of the current

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loop into two auxiliary components of vertical loop and horizontal loop.

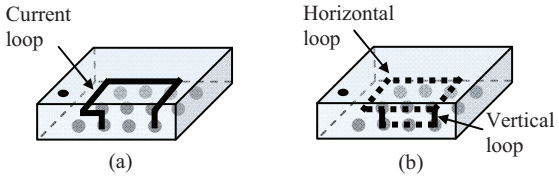


Fig. 2 IC current loops

The magnetic field in far field region due to a small current loop in Fig. 3 is given as [8],

$$\vec{H} = -\frac{\omega\mu_0 IA\beta_0}{4\pi\eta_0}\sin\theta\frac{e^{-j\beta_0 r}}{r}\hat{a}_\theta \quad (1)$$

where $\omega = 2\pi f$ is the angular frequency, μ_0 is the permeability of free space, I is the loop current source, $A = \pi b^2$ is the area enclosed by the loop, $\beta_0 = 2\pi/\lambda_0$ is the phase constant, η_0 is the intrinsic impedance of free space, θ is the angle between the observation point from the z axis, r is the radial distance from the midpoint of the loop to the observation point, and $\hat{a}_\theta$ is the unit vector of the field in spherical coordinate. The electric field is related to magnetic field as $\vec{E} = -\eta_0\hat{r}\times\vec{H}$ and given as

$$\vec{E} = \frac{\omega\mu_0 IA\beta_0}{4\pi}\sin\theta\frac{e^{-j\beta_0 r}}{r}\hat{a}_\phi \quad (2)$$

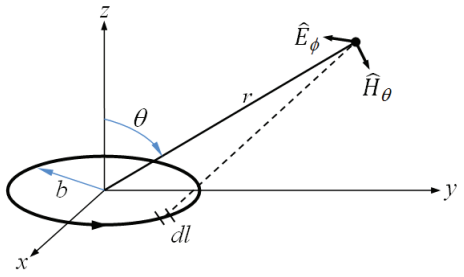


Fig. 3 A current loop

Equation (2) indicates that the strongest electric field is observed in the plane that contains the loop ($\theta = 90^0$) and least field at the right angle of the loop ($\theta = 0^0$ and $\theta = 180^0$). In short, a horizontal current loop emits a horizontally polarized electric field.

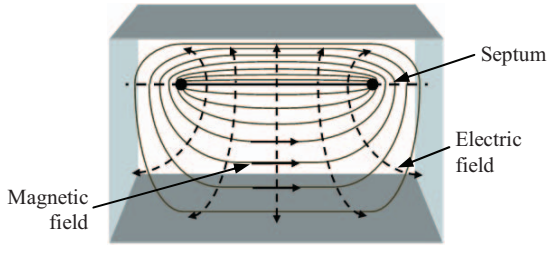


Fig. 4 Field distributions in a GTEM cell

An idealized electric and magnetic field distributions in a GTEM cell is illustrated in Fig. 4. It seems that the field coupling to the septum is efficient for vertical current loops as shown in Fig. 5. The emissions due to horizontal current loops are not easily coupled and hence errors in the total emission measurements of the IC.

In reality, modern ICs are likely to have thinner package indicating the possibility that the number of horizontal loops is greater than vertical loops. Loop area is a contributing factor affecting direct EMEs as indicated in equations (1) and (2). Unfortunately, the current EME measurement setup as described in Fig. 1 relies on contributions from vertical loops only. Hence, the measurement results cannot precisely signify total radiation from the ICs.

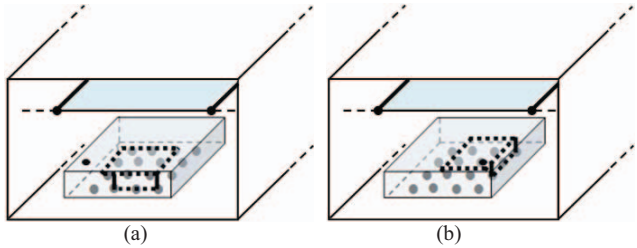


Fig. 5 TEM mode coupling with IC in (a) orientation 1 and (b) orientation 2

III. Effect of IC Packaging on Chip Level EME

IC packaging and interconnection techniques are key technologies for continuing growth of IC performance and lead density with the drop in IC feature sizes. Emerging of new packaging approaches for instance ball grid arrays (BGAs) technique for surface mount assembly (see Fig. 6(b)) and flip-chip technique at the chip level (see Fig. 6(c)) secure the demand for high-density I/O interconnections. At present, complex area array packages with higher number of I/Os and finer pitch as well as flip-chip packaging have turned into fashionable compared to the low count peripheral lead frame based packages as in Fig. 6(a).

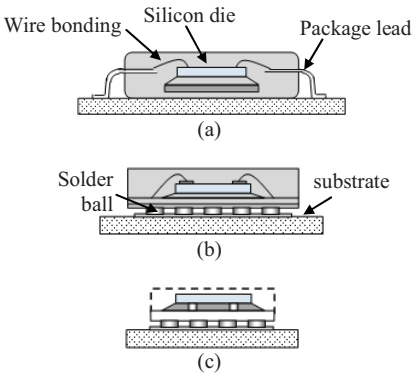


Fig. 6 The moved from (a) lead frame based package with I/Os on side, (b) area array package that distributes the connection on the substrate, and (c) flip-chip at silicon level

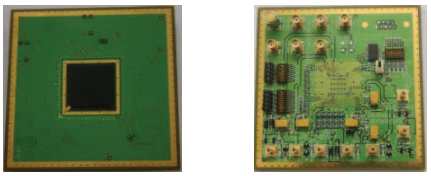
The revolution of the flip-chip technique and the complex area array packages are efficient to shorten the connection between the chip die and the PCB. As a result, the reduction on the connection length has significantly reduced the $L\,di/dt$ noise voltage because of the inductance on package bond wire and package leads.

In the study of the effectiveness of decoupling capacitors in reducing EM radiation from a PCB, it had been proven that lead inductance affects EM radiation and lower inductance would considerably decrease the EM radiation [9]. The study in [10] has confirmed that IC packaging types have significant effect on chip level emissions.

IV. Measurement Setup

A. Radiated Emission and Orientations

FPGA chip is ever increasing in popularity and highly sought for replacing custom application specific integrated circuit (ASIC) chip due to its flexibility and rapid prototyping. The reprogrammable feature available on the FPGA device offers an excellent platform to investigate EME performance on chip level. Hence the EME test can be done by configuring the FPGA device with various circuits without changing its package parameters. In this paper, a commercial Altera Cyclone III device has been selected as DUT for EME measurements using a GTEM cell. The FPGA device is mounted on a standardized 10cm x 10cm IC EMC PCB test board as shown in Fig. 7. The FPGA device has a BGA package with 780 pins.



(a) (b)

Fig. 7 IC EMC test board (a) front view, (b) rear view

There has been tremendous challenge to ensure the FPGA device as the only radiation source while performing EME evaluation by placing the entire FPGA test board inside the GTEM cell. Due to this reason, the entire board must properly be shielded to prevent interference from the test board. In this case, the whole board is shielded inside a metallic enclosure except the FPGA chip is exposed outside the enclosure throughout a window. Moreover, all edges of the enclosure are covered with copper tape in order to prevent leakage along the edges.

When the FPGA test board is housed inside the metallic enclosure, note that there is a small gap between the test board and the enclosure of the opening for the FPGA chip. Thus, there is a possibility for undesired signal propagating out of the enclosure by way of the gap. To enhance shielding effectiveness of the enclosure, metallic gasket is enclosed around the opening. In this case, the gasket can act as a barrier to isolate undesired signal to propagate in or out of the enclosure. Furthermore, the conductive characteristic of the gasket also provides ground contact between the enclosure and the test board. The photo of the shielded FPGA test board is shown in Fig. 8.

Since the FPGA chip consumes massive current during operation, the device must be regulated with external DC voltage supply instead of battery. Consequently, double shielded coaxial cable has been employed for voltage supply and clock signal connections. This can avoid the cables from being a potential transmitting antenna while carrying data from a point to another point. In addition, ferrite beads are added along the cables to suppress and attenuate high frequency noise from leaking into the cell via the cables.

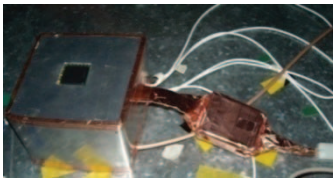


Fig. 8 Shielded FPGA test board

Fig. 9 illustrates the measurement setup of the shielded FPGA test board inside GTEM cell. The DUT is positioned on the cell holder in the middle of the free space as recommended in the manual. The FPGA chip is positioned in three orthogonal directions to get maximum coupling with the septum of the cell. The emission from the FPGA chip is examined in frequency domain with the aid of a spectrum analyzer attached to feeding point of the GTEM cell.

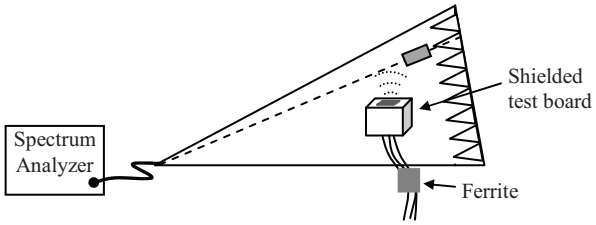
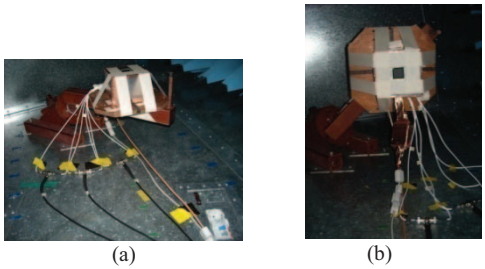


Fig. 9 Setup of enclosed FPGA test board inside GTEM cell

In previous sections, it has been pointed out that emissions due to horizontal current loops in IC of a DUT are somewhat neglected in standard IC EME measurement setup. This is due to the DUT rotation is restricted to horizontal positions since it is located on the wall of the cell. This limitation can be improved with both horizontally and vertically positioned DUT as shown in Fig. 10.



(a) (b)

Fig. 10 Actual shielded FPGA test board inside GTEM cell for (a) horizontal position, and (b) vertical position

Since the radiation pattern of the FPGA chip is unknown, the EME measurements were done by manipulating the chip into four different orientations (O1=0^o, O2=90^o, O3=180^o, O4=270^o) for both horizontal and vertical positions as indicated in Fig. 11. Hence the total emission of the measurement can be determined by vectorial summation of the respective components.

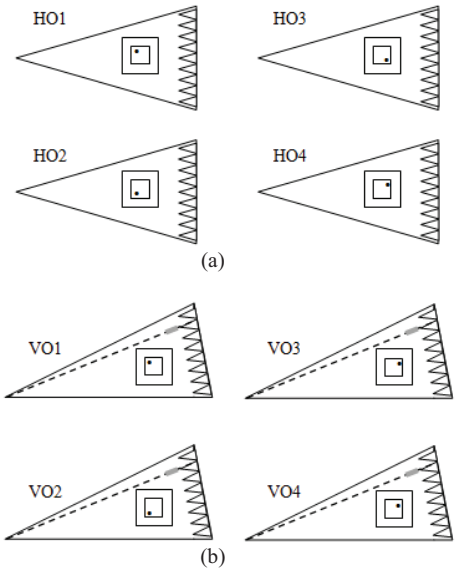


Fig. 11 Four FPGA orientations of (a) plan view for horizontal positions and (b) side view for vertical positions

B. *Output Buffer Control Circuit*

In the literature on chip level EMI/EMC management, chip I/O pins had been identified as the major source of radiation [5]. In this paper, a toggle flip-flop (TFF) logic circuit was developed to study the impact of I/O pins on chip EME. The TFF circuit has two I/O terminals, an input terminal for receiving external clock signal and an output terminal to deliver toggled signal. Fig. 12(a) shows the TFF circuit that was utilized to configure the FPGA chip.

The toggle terminal T of the TFF circuit is permanently tied to logical high for toggling the output signal while the TFF is clocked using an external clock signal. To differentiate the emission source either being contributed by the external clock or the output signal, a dc biased sinusoidal wave was employed as the external clock signal for exercising the TFF which results in a trapezoidal signal as the output.

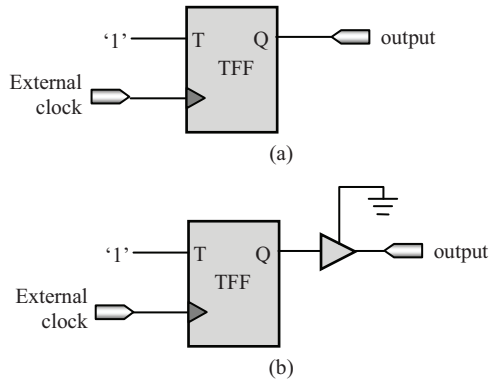


Fig. 12 TFF circuit for FPGA chip configuration. (a) With enabled tri-state buffer. (b) With disabled tri-state buffer.

A tri-state buffer gate is added in between the TFF output terminal and package pin as shown in Fig. 12(b). The purpose is to investigate the FPGA chip EME characteristics when the FPGA chip operates without dispatching signal to the output. In other words, the tri-state buffer symbolizes a logical switch that has been employed to manage connection between the TFF output terminal and the package lead. As the control terminal of the tri-state buffer is grounded, the connection to FPGA output pin is terminated, thus the TFF output will not be transmitted to external device although the TFF is excited by the external clock signal.

V. Results and Analysis

The FPGA chip was exercised with a 100MHz external clock signal. Fig. 13 shows the background noise spectrum for three different shielded FPGA test board configurations inside a GTEM cell: (i) inactive FPGA chip, (ii) active FPGA chip, and (iii) after configuring FPGA chip with TFF circuit. The quiet spectrum of the three conditions evidently implied no radiation from the shielded FPGA test board even though the FPGA chip is activated and loaded with TFF circuit.

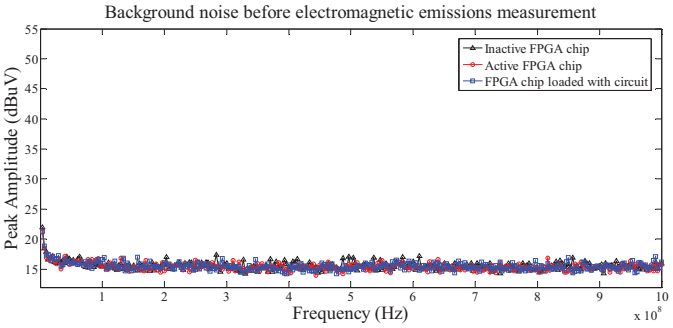
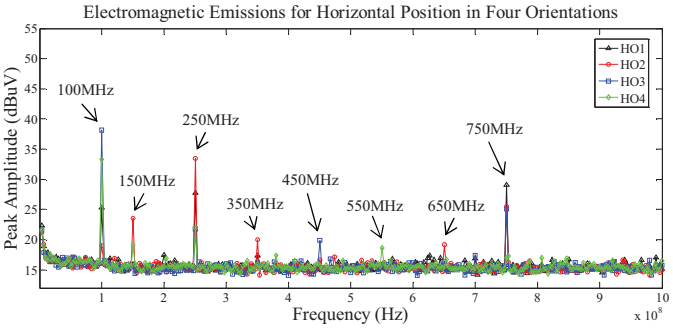
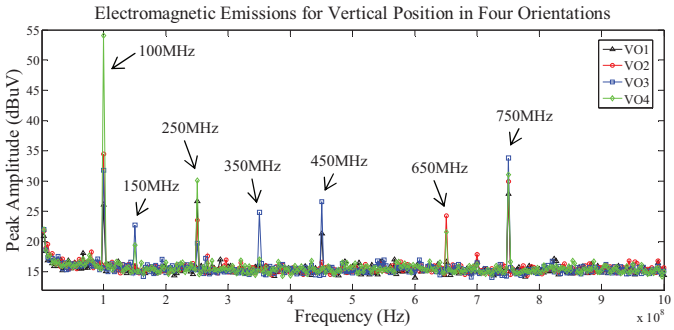


Fig. 13 Background noise for different FPGA chip configurations

Fig. 14 (a)-(b) show the EME results for horizontal and vertical orientations of the FPGA chip loaded with TFF circuit with enabled tri-state buffer as in Fig. 12 (a). Both figures show comparable EME for each vertical and horizontal position regardless of the orientations in that plane. This is to be expected due to the relatively small size of the FPGA chip compared to the working volume of the cell. It is interesting to discover that the EME of the FPGA chip is mainly contributed by the external clock and output signal. The highest peak at 100MHz is contributed by the pure sinusoidal clock signal and the other peaks are harmonics of the output signal. In Fig. 15, the average amplitude of the EME at vertical position of the IC is generally greater than horizontal position which reflects that the horizontal current loop plays a significant role in evaluating EME of the FPGA chip.



(a)



(b)

Fig. 14 EME of FPGA chip in (a) horizontal position and (b) vertical position

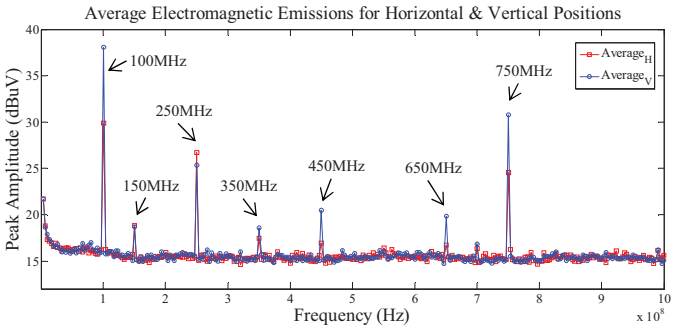


Fig. 15 Comparison of FPGA chip EMEs in horizontal and vertical position

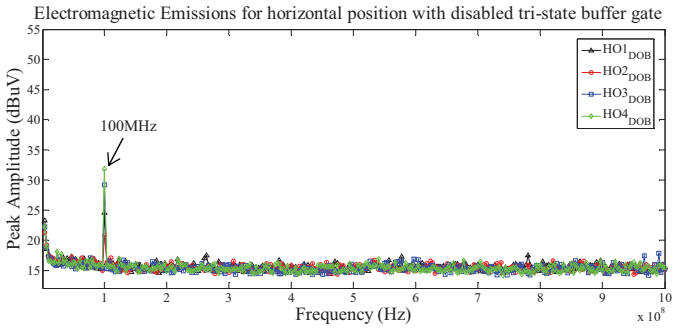


Fig. 16 FPGA chip EMEs in horizontal position after TFF was added with disabled tri-state buffer gate

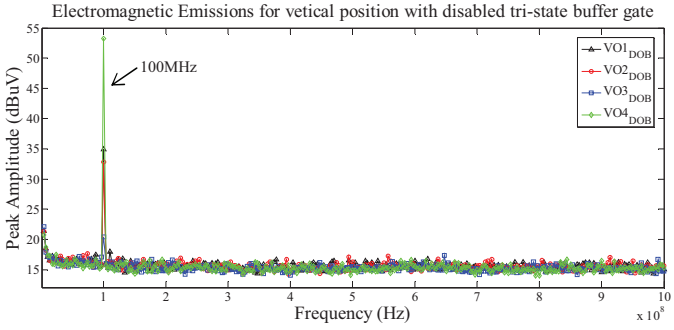


Fig. 17 FPGA chip EMEs in vertical position after TFF was added with disabled tri-state buffer gate

Fig. 16 and Fig. 17 show the EME measurement results when the FPGA chip was configured with the TFF circuit as in Fig. 12(b). The circuit has an additional tri-state buffer gate which is used for handling connection of TFF output terminal to FPGA package lead. The tri-state buffer was grounded while evaluating EME of the FPGA chip. As expected, the results detect no radiation from output terminal regardless of the chip orientations and positions. The emission is merely contributed by the external clock signal that has been employed for clocking the TFF circuit.

VI. Conclusions

This paper has addressed a possibility to perform EME measurement of FPGA by placing the entire test board inside a GTEM cell and regulated by an external voltage supply. A proper shielding of the FPGA test board and careful setup to avoid ambient interference are crucial to obtain the desired results.

The measurements proved that current IC emission measurement setup needs to be improved to allow both the contributions from vertical and horizontal current loops in the chip. We have experimentally shown the impact of IC I/O pins on EME.

Acknowledgment

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