IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received February 2, 2021, accepted February 22, 2021, date of publication March 8, 2021, date of current version March 18, 2021.

Digital Object Identifier 10.1109/ACCESS.2021.3064190

Characterization of Parasitic Impedance in PCB Using a Flexible Test Probe Based on a Curve-Fitting Method

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This work was supported in part by the Gobierno de Aragón-FSE 2014-20 under Grant IIU/2023/2017, and in part by the ECSEL Joint Undertaking (JU) under Grant 783158.

ABSTRACT Switching in power semiconductors with emerging materials such as silicon carbide (SiC) leads to undesired overvoltages and oscillations that limit switching frequency, largely due to impedance in the current commutation loop. Minimizing this parasitic impedance in printed circuit boards (PCB) requires precise characterization. To this end, this work presents a new measurement method based on obtaining S-parameters with a vector network analyzer (VNA) and on using a shielded flexible probe with mobile test terminals. The flexible probe uses a metal shielding plane perpendicular to the PCB to prevent the main measurement errors resulting from the variation in the magnetic flux responsible for loop inductance during the VNA frequency sweep. The proposed curve-fitting procedure consists of measuring the characteristic impedance and propagation time of the traces, considering they form ideal transmission lines. These values are used for a nonlinear least squares adjustment for the actual line (with losses). Finally, an experimental assembly with microstrip transmission lines was developed to validate the proposed method experimentally. The experimental results were compared with those obtained by using a rigid test fixture as a reference, those calculated analytically and those obtained from partial element equivalent circuit (PEEC) simulation. The curve-fitting method yields better results than the analytical and the simulation methods and they exhibit (up to 350 MHz) precisions of 1.37% in the characteristic impedance measurement and of 0.81% in the propagation time.

INDEX TERMS Curve-fitting procedure, flexible test probe, impedance measurement, parasitic impedance, printed circuit board (PCB), propagation time, silicon carbide (SiC), S-parameters, vector network analyzer (VNA).

I. INTRODUCTION

Emerging wide bandgap (WBG) semiconductor materials, such as silicon carbide (SiC), can switch higher frequencies than silicon (Si)-based semiconductors; therefore, they allow high power densities and efficiency in inverters. SiC-based semiconductors have higher thermal conductivity, higher critical electric field, less permittivity and higher saturation speed than Si-based semiconductors [1], [2]. Furthermore, devices such as SiC MOSFET have lower parasitic capacities between the connections of drain, source and gate regions than their Si-based counterparts [3], which enables shorter timeframes for voltage and current switching. However, this leads to very high voltage (dv/dt) and current (di/dt) variations [4]: dv/dt reaches 88 V/ns and di/dt 4.4 A/ns for SiC MOSFET [5]. Consequently, unwanted overvoltages and oscillations occur during the switching. The switching frequency of power inverters is limited by the amplitude and frequency of these oscillations, which depend on the impedance in the current commutation loop. Therefore, achieving an optimal design for SiC MOSFET-based inverters requires precise characterization to minimize parasitic impedance [6], [7]. In addition, high-frequency oscillations caused by parasitic impedance are the main electromagnetic interference (EMI) sources [8]–[11] in inverters.

Parasitic impedance can be characterized experimentally or by electromagnetic simulation using several numerical methods that consider PCB geometry and materials [12].

The associate editor coordinating the review of this manuscript and approving it for publication was Nagarajan Raghavan.

There are two methods for estimating parasitic impedance by simulation: partial element equivalent circuit (PEEC) method [13]–[15] and finite element analysis (FEA) method [16], [17]; both have been used to characterize parasitic impedance in power modules [14]–[16] and parasitic inductance in the direct-current bus in SiC-based laminated inverters [18] and in PCB-based busbars [19]. Numerical methods require exact knowledge of the geometry, the materials used and their properties to obtain precise results. They also involve a high computational cost in complex structures that require an analysis in the frequency domain.

Experimental techniques can be performed in the time domain or in the frequency domain, depending on the response analyzed by the measuring equipment. Time Domain Reflectometry (TDR) [20] consists of obtaining the step or impulse response of the circuit. The TDR measurement method can be complex, especially due to frequency errors [21] at each and every time instant, which requires a later processing of the data [22]. The second technique is the double-pulse test (DPT), used to study the switching transients response in a hard switching of power electronic devices [23] in a half-bridge branch. In this test, the switching analysis makes it possible to obtain losses, visualize overshoots and estimate the parasitic inductance of the commutation loop [24] in hard switching. This is an often-used method to check the result of parasite reduction by observing oscillation mitigation [19]–[25]. However, since inductance in the commutation loop is estimated with the frequency of voltage oscillations during switching and with the capacity of the power device connection, it is impossible to distinguish each parasitic impedance in the converter.

Impedance in the frequency domain can be measured using an impedance analyzer [26] or a vector network analyzer (VNA). The impedance analyzer was used to characterize the parasitic impedance of the commutation loop in three-phase two-level inverters up to 100 MHz [19] and in a T-Type inverter up to 10 MHz [27], both with a custom-designed test fixture. It was also used to characterize parasitic impedance in Si power semiconductor devices [28] and in SiC devices [29]. The VNA characterizes impedance in the range from hundreds of kHz to GHz using S-parameters. It was used to determine parasitic impedance in a small-sized PCB for a gallium nitride (GaN) low-power converter [30] with measurement connections integrated in the PCB, in other words, using rigid test fixtures. The VNA was also used to characterize parasitic impedance in discrete devices and power modules with one-port and two-port measurement techniques [31]. In contrast, commercial flexible test fixtures, such as the currently available Keysight 16089D and E, are limited in frequency up to 13 MHz [32].

Therefore, to the best of our knowledge, no method has been found in the literature for measuring impedance in PCB with measuring terminals spaced several centimeters apart, as those found in converters in the tens of kW range.

The aim of this paper is to present a method for frequency characterization up to 350 MHz of parasitic impedance in PCB with long traces, such as laminated busbars, based on a new test fixture (flexible test probe) with measuring terminals spaced up to 20 centimeters apart. The flexible test probe is formed by a shielded probe with one rigid connection and one flexible connection, as shown in Fig. 1. A microstrip transmission line was used for validation and the results are similar to those obtained with an identical microstrip based on a rigid test fixture designed to be used as a reference. These measures were also compared with those obtained by PEEC electromagnetic simulation and with calculations obtained analytically, and showed a clear improvement in precision.

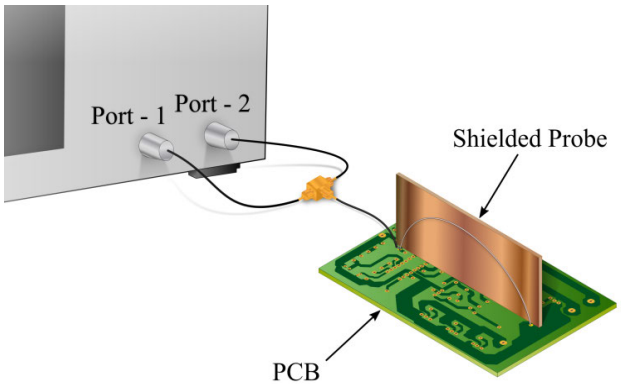

FIGURE 1. Experimental setup and the proposed shielded probe.

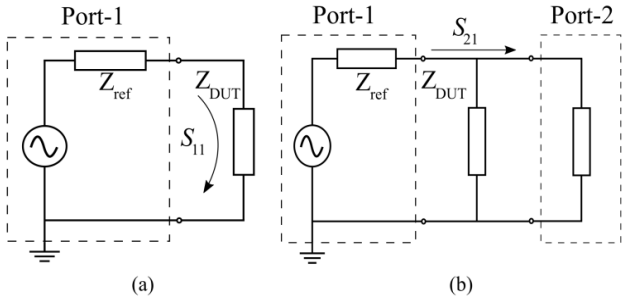

FIGURE 2. Impedance measurement methods in shunt connection with VNA: (a) 1-port reflection, (b) 2-port shunt-thru.

II. IMPEDANCE MEASUREMENT

A. IMPEDANCE MEASUREMENT WITH VNA

The VNA is used to measure the S-parameters of the connected DUT (device under test), the reflection coefficient (S_{11}) in one-port configuration (Fig. 2 (a)) and the transmission coefficient (S_{21}) in two-port configuration with the DUT connected in series or shunt (Fig. 2 (b)). Depending on these measurements and the reference measurement (Z_{ref}) used, the DUT impedance value in each of these methods is given by:

1-port reflection

$$Z_{DUT} = Z_{ref} \frac{1 + S_{11}}{1 - S_{11}} \tag{1}$$

2-port series-thru

$$Z_{DUT} = 2 \cdot Z_{ref} \left(\frac{1}{S_{21}} - 1 \right) \tag{2}$$

2-port shunt-thru

$$Z_{DUT} = \frac{Z_{ref}}{2}\left(\frac{S_{21}}{1-S_{21}}\right) \tag{3}$$

The precision of each of these methods depends on the range of impedance values to be measured [33]. The one-port reflection method is appropriate for the low-to-middle impedance range (0.5 Ω – 2 kΩ). In contrast, the series-thru connection in the two-port method allows the characterization of impedance from tens of Ω to tens of kΩ, while the shunt-thru connection is preferable for low impedance values (250 μΩ - 25 Ω), such as those in PCB traces with inductance values in the nH range. Therefore, given that the impedance value is low, the measurement method used for parasitic impedance in PCB traces is the two-port shunt-thru.

The VNA-DUT connection usually requires a specific test fixture. Commercial test fixtures can characterize the impedance of discrete electronic components in standard through-hole or surface-mount packages. However, when the DUT is not a standard discrete component or cannot be connected directly to the VNA with a coaxial, an interconnection PCB (test fixture) has to be designed between the VNA ports and the DUT terminals to precisely measure impedance based on the frequency. In all cases, as part of the measurement, the equipment has to be calibrated to eliminate the influence of the test fixture in the measurement.

B. FLEXIBLE TEST PROBE FOR PARASITIC IMPEDANCE MEASUREMENT

The purpose of the proposed probe is PCB characterization between spaced-apart points. As shown in Fig. 1, the probe connects with VNA PORT-1 and PORT-2 terminals by means of a coaxial T-connector with SMA terminals. It is formed (see Fig. 3) by a pigtail coaxial cable and a RG-316/U-type ground coaxial cable that allows the current to return to ground. The probe pigtail has an SMA connector at one end and is open at the other. To facilitate the connection with the measurement point in any plated hole of the PCB, the central pigtail conductor is connected to a test pin at the open end while the shield is connected to the ground coaxial. The central conductor and shield of the ground coaxial are short-circuited at both ends. The characteristic impedance of both cables is 50 Ω, like the impedance of the VNA ports. The pigtail cable is 100 mm long with an outside diameter of 1.37 mm, while the RG-316/U-type ground coaxial is 220 mm long.

The ground cable is a moving part of the probe that can be adapted to different connection points in the PCB, thus avoiding the need to develop a rigid test fixture for every measurement. However, the probe is on an isolated conductor plane perpendicular to the horizontal plane of the PCB where the measurements are taken. The purpose of this conductor plane is to shield the magnetic field, whose source is the current circulating during the frequency sweep with the VNA. The design criterion for the proposed flexible test probe is that

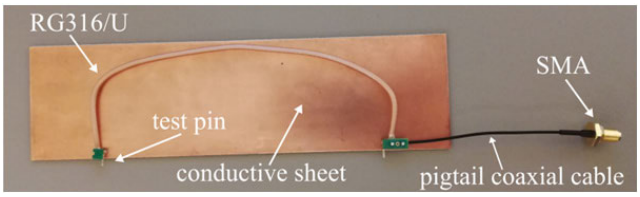

FIGURE 3. Flexible test probe for impedance measurement.

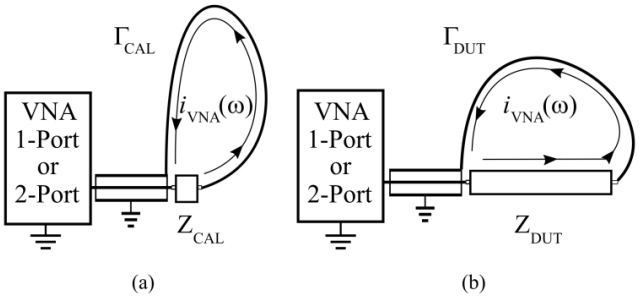

FIGURE 4. Variation in the current path: (a) path in calibration and (b) path in the DUT measurement.

the size of the conductive sheet is larger than the size of the loop. Therefore, the aspect ratio of the conductive sheet can be adapted according to the size of the trace to be measured.

To prevent unacceptable errors, both the VNA cables and the pigtail must remain in the same position during the calibration and measurement.

C. FLEXIBLE TEST PROBE PARASITES

When measuring low impedance with the flexible test probe, there are parasitic series impedances that cannot be fully compensated with calibration. This limits the probe frequency range.

Measurement errors are due to variations in the probe parasitic impedances between calibration and measurement. Firstly, this is due to variation in the probe spatial position (with respect to open-circuit calibration), which produces variations in parasitic capacities between the probe and the measurement environment. Secondly, the shape adopted by the flexible test probe varies, causing an inductance change in the probe with respect to the short-circuit calibration.

Therefore, the flexible test probe must be kept in the same position during calibration and measurement to prevent variations in parasitic impedance. However, as shown in Fig. 4, this is not possible with the ground coaxial cable, since the forced variation in the shape of the cable during calibration and measurement causes a variation in the loop inductance L_{loop} due to the current loop between the DUT and the probe. However, if the ground coaxial plane is kept perpendicular to the PCB in both measurements, the variations in parasitic capacities are negligible.

The inductance of loop L_{loop} depends on the current $i_{\text{VNA}}(\omega)$ and on the magnetic flux Ψ enclosed by the loop. Magnetic field $\mathbf{B}$ is related to magnetic vector potential $\mathbf{A}$ as

$$\mathbf{B} = \nabla \times \mathbf{A} \tag{4}$$

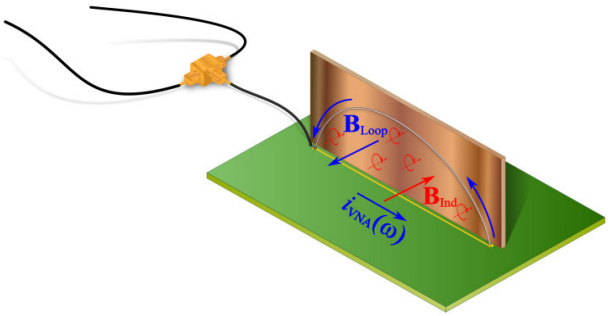

FIGURE 5. Probe with parasite mitigation techniques.

Using Stokes' theorem, magnetic flux Ψ through the surface enclosed by the loop Γ is equal to the integral of the magnetic vector potential $\mathbf{A}$ around the loop Γ, so that the loop inductance can be expressed as

$$L_{loop} = \frac{1}{i_{\mathrm{VNA}}} \cdot \oint_{\Gamma} \mathbf{A} \cdot d\mathbf{l} \tag{5}$$

This expression is valid as long as the current density is constant and there are no nonlinear magnetic materials in the surrounding medium. Therefore, L_{loop} is a function of the loop shape and its dimensions, as well as of the material properties of the surrounding medium. As shown in Fig. 4, the loop shape Γ_{CAL} during calibration is different to the loop shape in the DUT measurement Γ_{DUT} due to varying DUT lengths and the calibration load, so L_{loop} is different in both situations.

D. PARASITE MITIGATION TECHNIQUES

By calibrating with different loads, the probe parasitic impedances, the set of cables and the coaxial connectors plugged into the VNA ports are measured and compensated. The calibration standard used in the VNA is SOL, which consists of calibrating with three loads: a short-circuit (S), an open circuit (O) and a load of 50 Ω (L).

Parasitic impedance due to the position of the ground coaxial cannot be removed, but can be minimized. To that end, the ground cable is always perpendicular to the measurement plane, as shown in Fig. 5, where the ground cable has been attached to a supporting element made of non-magnetic material.

The loop inductance created by the ground cable can be prevented by cancelling the magnetic field $\mathbf{B}_{\mathrm{Loop}}(\omega)$, whose source is the measurement current $i_{\mathrm{VNA}}(\omega)$. A 35-μm-thick copper sheet is used as shielding for that purpose and the ground cable is attached to it. As can be seen in Fig. 5 eddy currents are induced with the same frequency as $i_{\mathrm{VNA}}(\omega)$ and they flow in closed loops within the copper shield. These eddy currents also produce a magnetic field $\mathbf{B}_{\mathrm{ind}}$ that opposes the field that generates them.

This manages to reduce the total magnetic flux responsible for loop inductance during the VNA frequency sweep. However, in the frequency range of interest, the use of the shielding board slightly changes the impedance of the PCB trace due to the proximity effect, which affects the attenuation factor α, as pointed out in Section V-C.

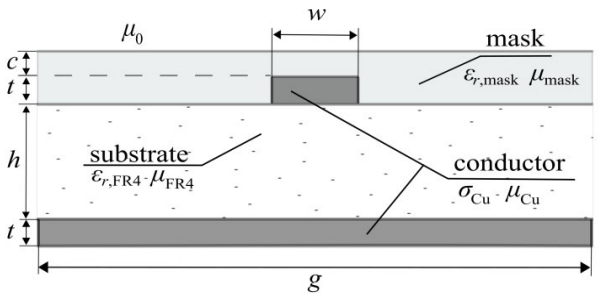

FIGURE 6. Structure of a microstrip.

TABLE 1. Design parameters of reference microstrip.

Symbol	Description	Value
w	Trace width	0.21 mm
t	Trace thickness	40 µm
g	Ground plane width	29.3 mm
l	Trace length	122 mm
h	Substrate height	1.6 mm
c	Mask height	25 µm
$\varepsilon_{r,\mathrm{FR4}}$	FR4 relative permittivity	4.6
$\varepsilon_{r,mask}$	Mask relative permittivity	3.5–4.2

III. EXPERIMENTAL SETUP

A. REFERENCE CIRCUIT

Microstrips are transmission lines that have been widely studied in the literature [34], [35], which is why they were chosen as the reference circuit. As shown in Fig. 6, a microstrip is formed by two copper conductors with conductivity σ_{Cu} printed on both external sides of the dielectric substrate with a thickness h and dielectric permittivity $\varepsilon_{r,\mathrm{FR4}}$.

The signal conductor with width w and thickness t is on the top side of the PCB (see Fig. 6). There is a conductor with width g and thickness t on the bottom side as a ground plane. The media forming the structure are not magnetic, their magnetic permeability is considered to be the same as in the vacuum μ_0 ($\mu_{mask} \approx \mu_{FR4} \approx \mu_{Cu} \approx \mu_0$). The PCB is covered by a protective isolating mask with relative permittivity $\varepsilon_{r,mask}$ similar to that of the substrate and permeability equal to that of the vacuum. The geometric parameters and physical properties used to manufacture the microstrip transmission line are shown in Table 1.

Although there are two means of propagation (substrate and mask), given that the geometric dimensions of the microstrip are far shorter than the length of wave λ, it can be considered that there are neither electric nor magnetic components in the direction of propagation, hence the field propagates as a transverse electromagnetic (TEM) wave. This type of propagation solves the fields as if they were quasi-static (DC). According to this approach, in the calculation of the characteristic impedance Z_0, the substrate-mask media are replaced by a homogenous medium with effective dielectric

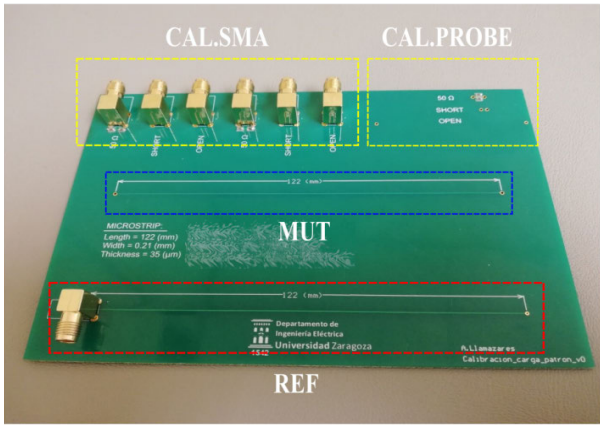

FIGURE 7. Experimental PCB developed for validation tests.

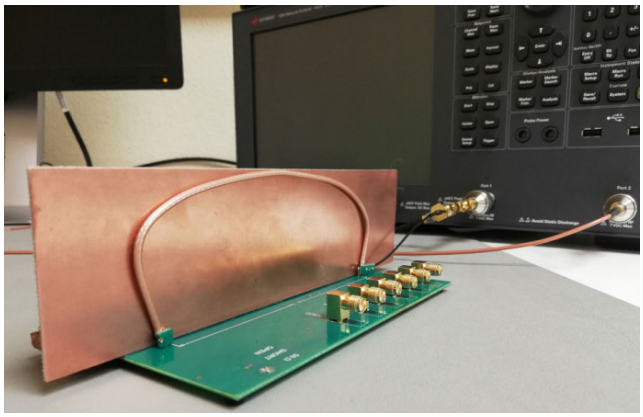

FIGURE 8. Measurement of the MUT line with the proposed probe.

constant $\varepsilon_{r,eff}$ [36], [37] that depends on the geometry and properties of the media. Therefore, Z_0 can be expressed as a function of $\varepsilon_{r,eff}$ and of capacity C_a ($\varepsilon_r = 1$) per unit of length of the same structure with air instead of a mask, according to [38]

$$Z_0 = \left(c \cdot C_a \cdot \sqrt{\varepsilon_{r,eff}}\right)^{-1} \tag{6}$$

and the phase constant β based on the angular frequency ω as

$$\beta = \omega \cdot \sqrt{\varepsilon_{r,eff}} \cdot c^{-1} \tag{7}$$

B. EXPERIMENTAL PCB AND VNA

An experimental PCB (Fig. 7) was developed to conduct the tests and to validate the proposed measurement procedure.

The substrate chosen for the PCB is FR4, the finish protecting the copper traces from corrosion is electroless nickel immersion gold (ENIG) and the mask thickness, although not specified by the manufacturer, is considered less than 25 μm, according to [39].

As shown in Fig 7, there are two identical microstrip transmission lines (MUT and REF) in the experimental PCB that are both 122 mm long; their parameters are as defined in Table 1. Both lines have a shorting via at one end (all the vias used are 0.762 mm in diameter). The reference transmission line (REF) has a coaxial SMA connector plugged into the VNA by coaxial cables. The other transmission line (MUT), for the measurement method with the flexible test probe, has two vias at both ends to connect the test pins of the developed probe.

Furthermore, as shown in the top part of Fig. 7, there are two load calibration kits: CAL.SMA, to be used with the REF line, and CAL.PROBE, for the MUT line. The CAL.SMA calibration kit uses the same connector type (SMA) as the REF line to compensate the error introduced in the measurement by the connector. The precision of the 50 Ω loads is 1% connected to traces as short and as wide as possible. In the CAL.PROBE kit, a 0603 package is used to minimize the parasitic impedance of the 50 Ω load. The same type of traces (short and wide) are used in the short-circuit load. Impedance was characterized using the Keysight VNA E5061B (Fig. 8), which calculates impedance from scattering parameters [33].

IV. PCB CHARACTERIZATION

A. DIRECT MEASUREMENT PROCEDURE

The behavior of the transmission line is characterized by its surge impedance Z_0 and by its propagation constant γ. As the measured frequency range is below 1 GHz, the conductance of the PCB substrate can be considered negligible compared with line capacity C, and, if the traces have a negligible resistance compared with inductance L, their behavior can be approximated by the behavior of a line with no losses whose characteristic impedance is

$$Z_0 = \sqrt{L/C} \tag{8}$$

and the propagation constant is a pure complex number equal to the phase constant β

$$\gamma = j\beta = j\omega \cdot \sqrt{L \cdot C} \tag{9}$$

The frequency characterization of a PCB trace can occur with the line ending in an open circuit or in a short-circuit. However, a line ending in a short-circuit was chosen to visualize the error introduced by the parasitic inductance due to the ground-return current, since the line is inductive until it attains the anti-resonance frequency.

In short-circuit conditions, the input impedance Z_i of a line without losses and with length l is a complex value given by [40]

$$Z_i = jZ_0 \cdot \tan(\beta \cdot l) \tag{10}$$

The product of phase constant β of the wave and length l of the line is known as the electric length θ and its relation to the length of wave λ is

$$\theta = 2 \cdot \pi \cdot l \cdot \lambda^{-1} (\beta \cdot l) \tag{11}$$

The wavelength is the quotient between the wave propagation speed in medium v_p and its frequency f; reordering the terms in (11) electric length θ can be expressed in terms of the wave angular frequency ω, thus obtaining

$$\theta = \omega \cdot l \cdot v_p^{-1} \tag{12}$$

this relationship can be expressed by the line delay time t_{pd} (time a wave takes to travel 1 m at propagation speed v_p) as

$$\theta = \omega \cdot l \cdot t_{pd} \tag{13}$$

According to (10) when $\theta = \pi/2$, the input impedance presents a maximum, which occurs for a wave length of $\lambda/4$ and at the anti-resonance frequency $f_{\lambda/4}$, as shown in Fig. 12. Therefore, $\omega_{\lambda/4}$ is obtained directly from the experimental measurement, which enables t_{pd} and v_p. to be calculated from the relationship

$$t_{pd} = \pi \cdot \left(2 \cdot \omega_{\lambda/4} \cdot l\right)^{-1} \tag{14}$$

The line characteristic impedance Z_0 is obtained from the measurement value at $f_{\lambda/8}$, since, according to (10), the measured impedance is directly Z_0 for a length $\lambda/8$ ($\theta = \pi/4$). This analysis is similar and equally valid for transmission lines ending in an open circuit. Using the same procedure, a transmission line ending in an open circuit can be characterized from the measurement of $f_{\lambda/4}$ and $f_{\lambda/8}$, due to the dependence of the input impedance on the cotangent of θ.

B. CURVE FITTING PROCEDURE

In an ideal short-circuited transmission line, impedance at the anti-resonance frequency tends to be infinite. However, the impedance measurement, obtained at $f_{\lambda/4}$, is always a finite value. Therefore, the transmission line behaves like a line with low losses whose attenuation constant α is other than zero. Considering a line model with losses involves introducing new unknowns: besides Z_0 and t_{pd}, the unknown α is introduced, which, in the case of low losses, can be approximated by [40]

$$\alpha \approx \frac{1}{2} \cdot \left(R \cdot Z_0^{-1} + G \cdot Z_0\right) \tag{15}$$

where R is the resistance per unit of length and G the conductance per unit of length. Disregarding resistance in DC, R is proportional to the root of the frequency due to the skin effect, and G depends directly on the frequency; therefore, α can be expressed in terms of the constants k_1 and k_2 as

$$\alpha \approx k_1 \cdot \sqrt{f} + k_2 \cdot f \tag{16}$$

Z_0 and t_{pd} are calculated by the direct measurement procedure and refined by using nonlinear least-squares minimization [41], which is also applied to find k_1 and k_2. Nonlinear least-squares solves the equation

$$\min\left(\sum_f \|Z_i - Z_{VNA}\|^2\right) \tag{17}$$

where Z_i is given by

$$Z_i = |Z_0 \cdot \tanh(\gamma \cdot l)| \tag{18}$$

and Z_{VNA} are the experimental values measured by the VNA.

The Z_0, t_{pd}, k_1 and k_2 values are iterated until a satisfactory result is reached with a coefficient R^2 above 0.95.

C. PEEC SIMULATION

The partial element equivalent circuit (PEEC) method allows the physical layout of a circuit to be turned into a lumped element circuit network. The PEEC method analyzes static and quasi-static problems and it is used to extract parasitic inductances and capacities in power module packages, busbars and electromagnetic compatibility (EMC) applications [14].

Based on the data in Table 1, the microstrip line was modeled in PEEC as two rectangular conductors. Two static conditions are simulated to obtain the microstrip characteristic impedance and delay time. Firstly, the conductors are considered surrounded by air, without a substrate or a mask. The equivalent capacity between both conductors forming the microstrip is obtained from the PEEC analysis and its value per unit of length with air substrate C_a is obtained by dividing by the transmission line length. Secondly, the FR4 substrate and the solder mask with relative permittivity $\varepsilon_{r,mask} = 4.2$ and a constant height of 25 μm are considered. The capacity obtained per unit of length in these conditions is C_{FR4}. The quotient between both is the so-called the effective dielectric constant ($\varepsilon_{r,eff}$)

$$\varepsilon_{r,eff} = C_{FR4}/C_a \tag{19}$$

The characteristic impedance Z_0 of the microstrip line is calculated through (6) with C_a and $\varepsilon_{r,eff}$, obtained in the PEEC analysis, while the propagation delay t_{pd} per unit of length in a transmission line without losses is obtained as

$$t_{pd} = \sqrt{\varepsilon_{r,eff}}/c \tag{20}$$

V. RESULTS

A. MAGNETIC SHIELD ANALYSIS

The probe is characterized with and without the magnetic shield to assess its effects on the proposed probe. The inductance measurements for both probes are compared in Fig. 9. The inductance value of the shielded probe includes the pigtail, the SMA connector and the ground cable. Consequently, for a frequency of 10 MHz, for example, the inductance measured in the unshielded probe is 184 nH; with shielding, the value the value drops to 77.54 nH.

As can be seen in Fig. 9, the unshielded probe behaves as an inductance up to the resonance frequency of 124 MHz; after that, the capacitive effect predominates. When the ground return loop is shielded, in other words, with the shielded probe, the resonance frequency rises up to 218 MHz due to the decrease in loop inductance. There is also attenuation in the impedance due to an increase in power dissipation (Fig. 10).

Shielding effectiveness (SE_{dB}) is defined by the attenuation of the magnetic field after passing through the shielding. In this case, shielding losses are due to absorption losses A_{dB} and reflection losses R_{dB} [42]. Due to the Joule effect, absorption losses appear inside the metal shielding when eddy currents circulate. These absorption losses depend on the penetration depth of the skin effect and the shielding

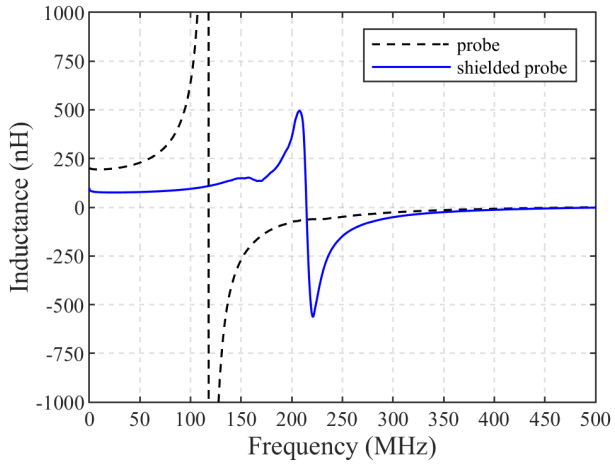

FIGURE 9. Inductance measured with the probe with and without shielding during the short-circuit calibration from 100 kHz to 500 MHz.

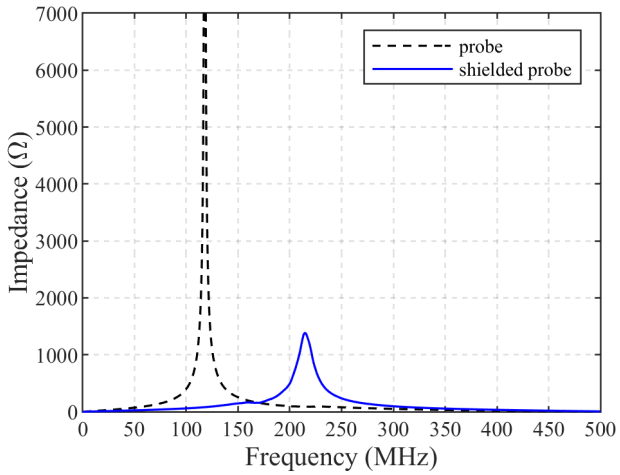

FIGURE 10. Impedance measured in the probe with and without shielding during the short-circuit calibration from 100 kHz to 500 MHz.

thickness; the thinner the shielding, the less absorption losses. Reflection losses appear as a result of the difference between the characteristic impedances between the medium where the incident wave is propagated (air) and the shield copper.

Fig. 11 shows the SE_{dB} for a 35-μm copper sheet, considering a distance of 1.5 mm between the central conductor of the ground cable and the shielding plane. These calculations were made using the approximate expressions for near-field magnetic shielding effectiveness developed for the copper in [42]

$$A_{dB} = 8.686 \cdot (s/\delta) \tag{21}$$

$$R_{dB} = 14.57 + 10 \cdot \log(f \cdot r^2) \tag{22}$$

$$SE_{dB} = A_{dB} + R_{dB} + MR_{dB} \tag{23}$$

where s is the thickness of the copper shielding, δ is the penetration depth due to the skin effect in the copper, f is the frequency and r is the shielding distance. The term MR corresponds to losses due to multiple reflections appearing in the shielding copper.

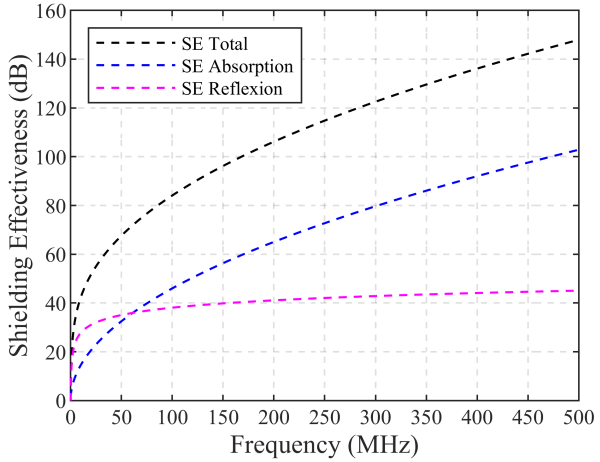

FIGURE 11. Shielding effectiveness of the magnetic shield.

Therefore, the calculated attenuation is 19 dB at 1 MHz, and it increases with the frequency. However, for frequencies below 1 MHz, the shielding was observed to be less effective, 4.7 dB at 200 kHz. Consequently, the option chosen was a shield with a second copper plane with the same characteristics and 1.6 mm apart from the other plane to strengthen attenuation in the magnetic field for frequencies below 1 MHz. A two-sided, 35-μm-thick copper PCB was used to construct the double shielding.

B. DIRECT MEASUREMENT PROCEDURE

This section presents the characterization results of the REF and MUT microstrips applying the direct measurement procedure, which was previously described in SECTION IV-A. The REF microstrip is measured using a rigid SMA connection and the MUT line with the proposed flexible test probe.

Fig. 12 and Fig. 13 show the impedance and phase of the REF and MUT lines measured based on frequency up to 500 MHz. The measured anti-resonance frequency, corresponding to a wave length of $\lambda/4$, is 324.41 MHz in the REF line and 327.22 MHz in the MUT. Fig. 12 shows that impedance changes from inductive to capacitive at the anti-resonance peak, which is larger in the REF line than in the MUT line. This is because skin effect losses in the shielding have not been fully compensated by the probe change in geometry in the MUT line. In an ideal transmission line, impedance at anti-resonance is infinite and its value drops as the resistive component increases. The same can be concluded from Fig. 13, which shows a smaller gradient (in the phase change) in the MUT line than in the REF line. This figure also reveals how the phase exceeds $-90°$ from 380 MHz, probably due to an equivalent parasitic capacity that has not been compensated during calibration. This capacity limits the probe frequency scope.

C. CURVE-FITTING PROCEDURE

As described in SECTION IV-B, the behavior of the microstrip line is similar to the behavior of a line with

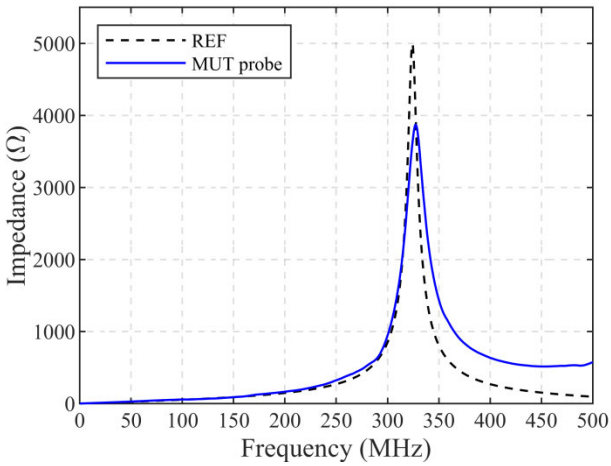

FIGURE 12. Impedance measured in the REF and MUT lines from 100 kHz to 500 MHz.

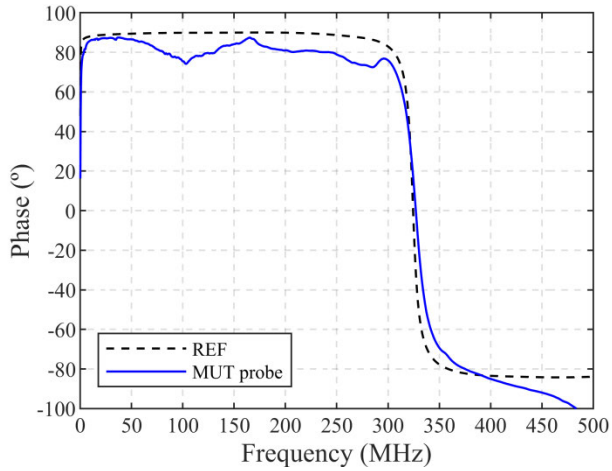

FIGURE 13. Impedance phase measured in the REF and MUT lines from 100 kHz to 500 MHz.

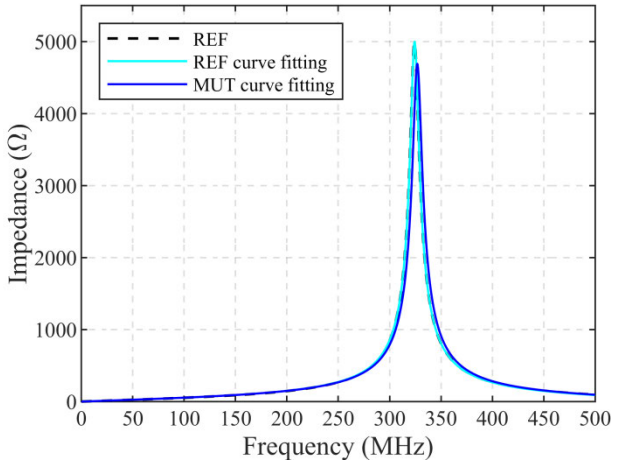

FIGURE 14. Impedance of the REF and MUT lines adjusted by the curve-fitting procedure.

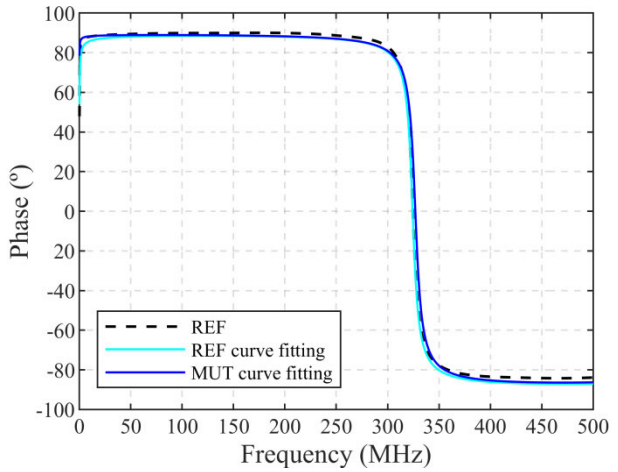

FIGURE 15. Phase of the REF and MUT lines adjusted by the curve-fitting procedure.

losses using an iterative method (curve-fitting procedure) to measure impedance. This method was applied to the REF and MUT lines, which were measured with rigid SMA connectors and a flexible test probe, respectively. The maximum adjustment frequency considered in the procedure was 350 MHz.

Fig. 14 and Fig. 15 show the impedance and the phase of the REF and MUT lines based on frequency. The anti-resonance frequency obtained is now 324.34 MHz in the REF line (almost the same result as before) and 326.92 MHz in the MUT; in other words, the error with the flexible test probe can be reduced to 0.8%.

When the curve-fitting procedure is applied, the measurement with SMA terminal in the REF line gives a value for α of 0.21 Np/m at 500 MHz. This value contrasts with the one obtained with the flexible test probe for the MUT line, 0.24 Np/m. This is an error of 14.3% due to attenuation or losses in the flexible test probe that have not been considered in the adjustment model, and they exist, and are included, in the attenuation of the propagation constant.

D. COMPARATIVE RESULTS

Table 2 compares the results of the surge impedance Z_0 and the propagation delay t_{pd} obtained experimentally by direct measurement and curve-fitting procedures with the results of the PEEC simulation and those obtained analytically using the closed-form formula [43] applying the microstrip parameters given in Table 1. The PEEC simulation results were obtained using expressions (19) and (20) by calculating the capacity of the microstrip surrounded by air and without a substrate C_a, and the capacity of the microstrip considering the FR4 substrate and a mask with relative permittivity $\varepsilon_{r,mask} = 4.2$.

The results (Table 2) are compared using the result obtained in the curve-fitting procedure on the microstrip REF line as a reference. Consequently, the propagation time has an error under 1% in all cases. However, the errors are greater

TABLE 2. Impedance and propagation delay estimation.

	Z_0 (Ω)	t_{pd} (ns/m)	ε_{rror} Z_0 (%)	ε_{rror} t_{pd} (%)
REF direct measurement	100.54	6.316	-1.91	-0.03
REF curve fitting	102.50	6.318	-	-
MUT direct measurement	104.51	6.262	1.96	0.89
MUT curve fitting	103.9	6.267	1.37	0.81
Closed-form formula [43]	112.25	6.377	9.51	0.93
PEEC	115.56	6.258	12.74	0.95

in the case of characteristic impedance, attaining values of up to 12.7% in the PEEC simulation, probably because it is impossible to model actual conductor traces as they have tolerances, rough surfaces and, generally, a trapezoidal shape. The error (9.51%) in the characteristic impedance obtained analytically with the closed-form formula [43] is probably caused by the precision of the expressions based on the microstrip geometry and by considering the mask as uniform and having a constant height over the top conductor.

The direct measurement procedure applied to the MUT line gives an error of 1.96% in impedance and 0.89% in propagation time. These errors are mainly caused by impedance variation due to changes in the probe shape between calibration and measurement. Although considering the line without any losses simplifies the calculation procedure, it also introduces a certain error.

The curve-fitting procedure applied to the MUT line with the proposed probe has errors of 1.37% in impedance and 0.81% in propagation time. This technique offers very precise values and has the advantage of determining the impedance of a long trace in a PCB (with a separation of several centimeters between the connection points) to avoid conducting a fixed fixture test for every trace.

The phase constant β can be directly obtained from t_{pd} by applying (11) and (13). The ABCD matrix, together with Zo, α and l, is obtained as follows

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\alpha + j\beta) \cdot l & Z_0 \cdot \sinh(\alpha + j\beta) \cdot l \\ \frac{1}{Z_0} \cdot \sinh(\alpha + j\beta) \cdot l & \cosh(\alpha + j\beta) \cdot l \end{bmatrix} \quad (24)$$

and the T-equivalent circuit for the two-port network is easily calculated from the ABCD parameters [40].

VI. CONCLUSION

This article presents a characterization procedure for PCB traces with ends (connection points for the measurement) that can be spaced several tens of centimeters apart. Impedance measurement is based on the S-parameter measurement through a VNA using the two-port shunt-thru method. To that end, this work proposes the use of a flexible probe (Fig. 3) formed by a pigtail coaxial cable and a ground coaxial placed on a copper plate perpendicular to the measurement plane. This manages to minimize the main measuring errors, which are due to the magnetic flux responsible for loop inductance during the VNA frequency sweep.

If the line is considered ideal, the propagation time t_{pd} is obtained directly from measuring impedance at anti-resonance frequency $f_{\lambda/4}$, while the measurement obtained at length λ/8 is directly the characteristic impedance Z_0. However, as observed experimentally, the line behaves like a line with low losses. This involves introducing a new unknown, which is the attenuation constant α; consequently, the curve-fitting procedure was developed to determine the parameters of this model with losses. In the proposed method, the starting point is the initial measurement of t_{pd} and Z_0 obtained using the direct method, and a nonlinear least-squares method is applied to obtain the values of α, Z_0 and t_{pd}, which minimize the objective function defined by (18). Two identical microstrip lines were used to validate the method described with the shielded flexible probe: one with a rigid test fixture serving as a reference and another for measuring with the proposed procedure. The values were compared with each other, with the values calculated using an analytical approximation and with those obtained from the PEEC simulation. The results (Table 2) show that the curve-fitting procedure is extremely precise compared with the reference measurement obtained with the rigid test fixture, and they are an improvement over those of the direct measurement method, of the analytical results and of the results calculated by the PEEC simulation.

Lastly, as the probe is flexible, there is no need to design a specific test fixture for the measurement of the traces in a PCB. The flexible probe procedure can also be applied to characterize laminated busbars in PCBs. Likewise, the flexible test probe can be used not only for impedance measurement, as in the microstrip, but also for the measurement of parasitic inductances in PCB traces of power semiconductor devices (for example, in a half-bridge).

ACKNOWLEDGMENT

The JU receives support from the European Union's Horizon 2020 research and innovation programme and Italy, Germany, Belgium, Sweden, Austria, Romania, Slovakia, France, Poland, Spain, Ireland, Switzerland, and Israel.

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