

Automatic Analog Circuit Synthesis by BF methods

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Abstract—As we wrote in our earlier article [10] the automatic synthesis of digital circuit is mostly solved, at a well defined boundary conditions. Algorithm of a digital topology generating can be performed. From traditional discrete electronic parts an analog circuit implementation is almost impossible, because analog integrated circuits configurable through a digital interface already exist.

Automatic synthesis of analog circuits can be important, because are through a digital interface configurable analog integrated circuits.

All these, and increasing processing performance of computers are new approaches to be made, even the brutal force (BF) methods [23] [25].

Such synthesis may be important not only in the synthesis of discrete components, but circuit modules can be used, whether the case of configurable analog circuitry system synthesis.

In engineering practice the commonly used brute force method is very resource-intensive process.

The present article shows an optimization method by which the purely theoretical possibilities are considerably reduced thereby it increases the rate of synthesis.

In the current article, partly as a result, finished a computer program that can automatically generate circuit topologies. We will now deal with some aspects of this.

I. INTRODUCTION

An analog electronic circuit function (Γ_c) and behavior (f) is determined by the parameters of the used components ($\bar{\mathbf{P}}$) and the connect topology (n), according to (1);

$$\Gamma_c = f(n, \bar{\mathbf{P}}). \quad (1)$$

The circuit function is of course not an exact definition, but it can mean for example from input to output time domain determined amplitude function, frequency-domain amplitude behavior...etc. The used circuit description depends on the suspected, or the realized function of circuit [24] [26] [28].

Parameter (n) describes the network of the discrete component, in there pins are well determined connected to each other.

In equation (1) the $\bar{\mathbf{P}}$ parameter is a scalar vector, that contains the relevant parameters of used electronic parts in formal (2);

$$\bar{\mathbf{P}} \in p_0, p_1, p_2 \dots p_n; \quad (2)$$

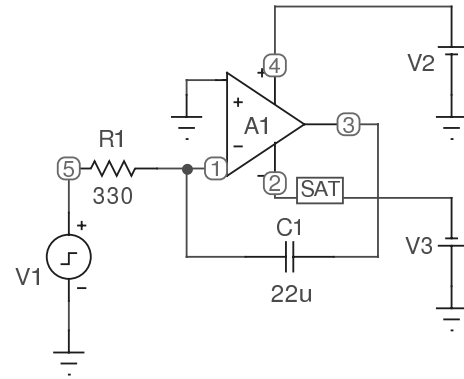


Fig. 1. Integrator circuit.

where p_n the significant parameter of electronic part, for example resistance of a resistor, capacitance of the a capacitor, h_{21} of a bipolar tranzistor... etc. [6] [22].

On Fig. 1 is seen, as above example an integrator circuit. This circuit contains an operational amplifier (A_1), a square wave input generator; (V_1) $U_{pp} = 2V$, $U_{offset} = -1V$, two power source; (V_2 , V_3) with $\pm 15V$, a feedback capacitor (C_1) its value is $22\mu F$, and a resistor (R_1) and value of last one is 330Ω . These parts lists and entering a value defining of the $\bar{\mathbf{P}}$ vector [2] [3] [9].

Fig. 2 shows a connection network in short form "netlist" about of circuit of Fig. 1. This netlist describes the nods of circuits ($N\$1$, $N\$3$, $N\$5$). The nods $N\$3$ connect 2 number pads of capacitor (C_1), output of amplifier (A_1) with 4 pads of integrated circuit, and output of circuit to X_2 connector [5] [7].

Nowadays the development of such a circuit heuristic means. We know the circuit operation, the availability of parts and components to form a network with the appropriate values [16] [1]. To draw the circuit CAD tools are used, as well as circuit simulation. Network of Fig. 2 is generated from wiring diagrams[8] [4] [27] [29].

Computing environment is possible to check by circuit simulation software the operation of the realized circuit. Fig. 3 shows in time domain the circuit operation from input to output [13] [14] [15].

Net	Part	Pad	Pin
GND	IC1	1	+IN
	X1	1	S
	X2	2	S
N\$1	C1	1	1
	IC1	3	-IN
	R1	2	2
N\$5	R1	1	1
	X1	2	S
N\$3	C1	2	2
	IC1	4	OUT
	X2	1	S
VCC-	IC1	2	V-
VCC+	IC1	5	V+

Fig. 2. A integrator circuit's connection network.

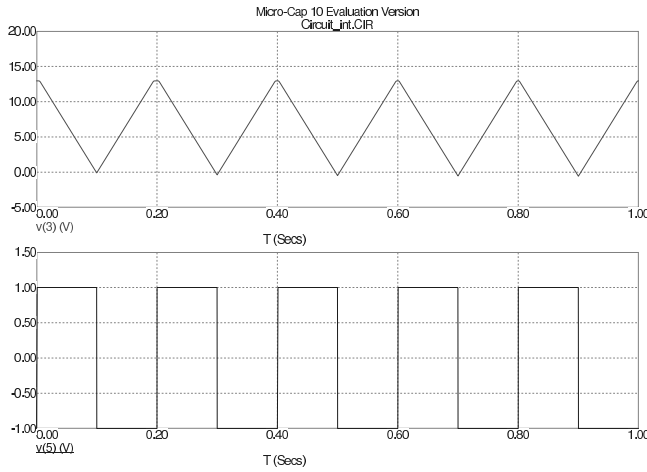


Fig. 3. Time domain simulation of integrator circuit. Bottom input signal, above the output.

II. ANALOG CIRCUIT REALIZATION BY A SWITCHING MATRIX

Theoretically, if we have n numerous electronic components each of them has got ϕ_i pins which are necessary to properly connect with a wished analog circuit. If every possible way we want to create a circuit network, we need a matrix that consists of o number of columns according the (3);

$$o = \sum_{i=0}^{n-1} \sum_{j=0}^{\phi_i-1} c_{ij}, \quad (3)$$

where for $A_{m,(i,j)}$ is true (4);

$$A_{m,(i,j)} \in [0, 1]. \quad (4)$$

On Fig. 4 theoretical arrangement of a switching matrix is shown. This matrix consists of electronic parts's dev_0-dev_n leg wires as columns $c_{00}-c_{n(\phi-1)}$, and row wires for possible interconnections r_0-r_{m-1} . In (4) 0 means no connection between column and row wires, and 1 case is have got, this is

actually a switch function, which is described of turned ON and OFF state. On Fig. 4 we signed this function by a switch k_g [20] [19].

It can be seen that the pins of electronic components and the interconnection wires formed from a matrix of $m \times n$ type, where $m=n$, so there is square matrix, which contains all the possible options of connections, according in equation (5):

This square matrix from equation (3) contains numerous cross points according to (6) is;

$$C_p = o^2. \quad (6)$$

Thus, the number of theoretically possible different topology (T_n) from equations (5) and (6) is;

$$T_n = 2^{C_p}. \quad (7)$$

Fig. 4 layout and description of equations (5) and (6) are so perfectionist that includes abilities of all the parts legs wires the possibility of connecting a node, as well as the possibility of all parts foot stand-alone, a unique node [18] [17].

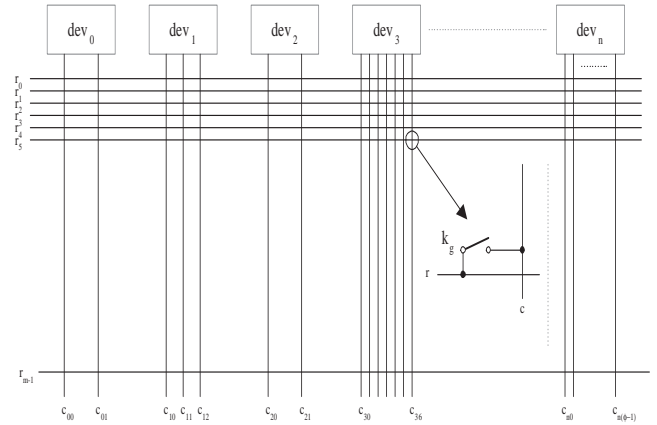


Fig. 4. Theoretical arrangement of a switching matrix for the evolving every abilities connections.

III. OPTIMIZATION OF A SWITCHING MATRIX

In the previous paragraph the possibility formation of the theoretical switch matrix is shown. According to the described solution we generate from the circuit of Fig. 1 or net list of Fig. 2 in matrix's in Fig. 5.

On Fig. 5 it can followed that every nodes of netlist means a row of matrix; $r_0 = GND$, $r_1 = N\$1$, $r_2 = N\$2$, $r_3 = N\$3$, $r_4 = N\$4$, $r_5 = N\$5$. You can see that the rest of any unused nodes abilities from r_6-r_{16} .

The electrotechnical or physical reason of the not used abilities is understandable, because it is meaningless to connect, for example, two power supplies (N_2, N_4), or output of operational amplifier (N_3) with input signal source (N_5). Of course one can find too much refusal of this kind.

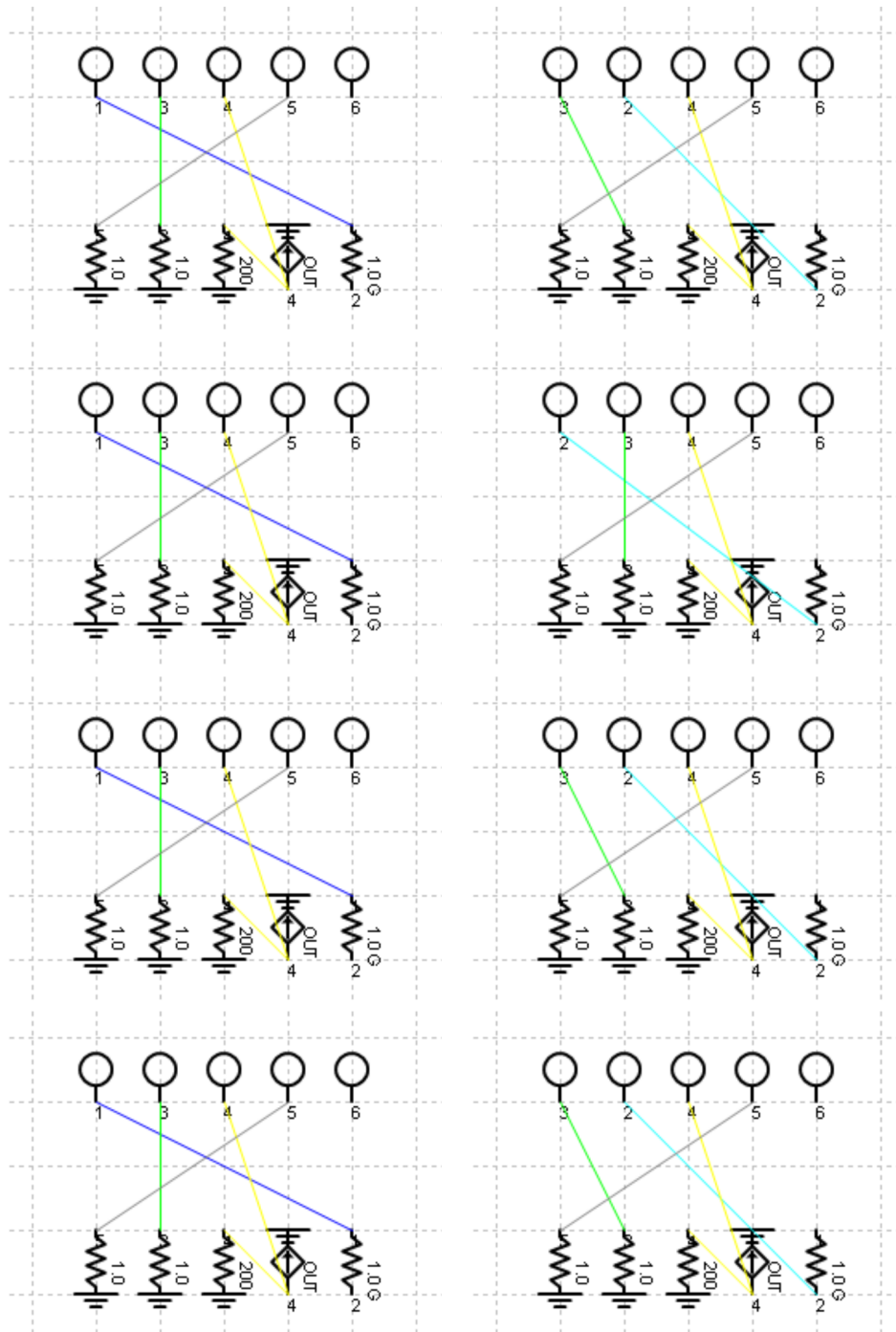


Fig. 10. Any automatically generated "integrator" circuits on a Netlist-viewer program's screen. On upper side of figures there are from 1-6 poles of ability nodes of integrator of Fig. 1.

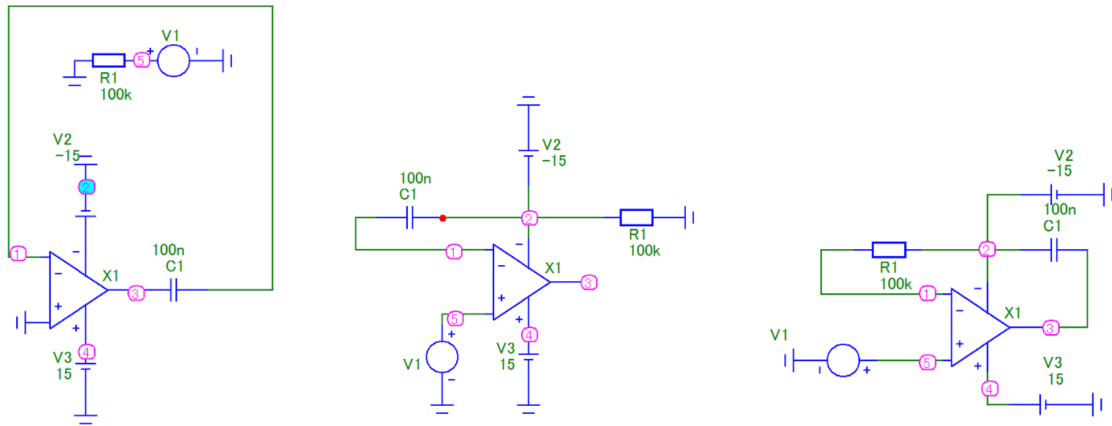


Fig. 11. Three wrong "integrator" circuit in Micro-Cap simulation environment.

displayed in the traditional circuit diagrams, some examples of which are shown in Fig 11.

V. CONCLUSIONS

The previously proposed structured switch-matrix we can generate a combinatorial topology with an appropriate computer program. Later we can analyze with a circuit simulation method the function of generated circuit, and the appropriate parametric fine settings carried out. This article provides a solution the applicability of high performance computers and

advanced cross-bar switch circuits appearance. The proposed methods are extendable for the system generated from functional blocks, and subsystems too.

Further work is needed to search for efficient algorithms, and exclusion of generating the self understood wrong circuits.

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U3 4 0 DC 15
U2 2 0 DC -15
C1 0 3 100N
R1 0 5 100K
U1 5 0 DC 0 PULSE 0 1 0.05 0.032001 1 29.918 32
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RSUPPLUS 5 0 1
RSUPMIN 3 0 1
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GOUT 0 4 1 2 1000
RIN 1 2 1G
.ENDS LM741
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.END
; $SpiceType=SPICE2G

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Fig. 9. A standard file format (CKT) for Spice-like circuit simulations program.

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