Reliable aluminum contact formation by electrostatic bonding

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Abstract

The paper presents a detailed study of a reliable method developed for aluminum fusion wafer bonding assisted by the electrostatic force evolving during the anodic bonding process. The IC-compatible procedure described allows the parallel formation of electrical and mechanical contacts, facilitating a reliable packaging of electromechanical systems with backside electrical contacts. This fusion bonding method supports the fabrication of complex microelectromechanical systems (MEMS) and micro-opto-electromechanical systems (MOEMS) structures with enhanced temperature stability, which is crucial in mechanical sensor applications such as pressure or force sensors. Due to the applied electrical potential of $-1000\,\mathrm{V}$ the Al metal layers are compressed by electrostatic force, and at the bonding temperature of $450\,^{\circ}\mathrm{C}$ intermetallic diffusion causes aluminum ions to migrate between metal layers.

Keywords: metal fusion bonding, anodic bonding, hybrid bonding, electrostatic force, MEMS

(Some figures may appear in colour only in the online journal)

1. Introduction

Reliable readout and control of complex microelectromechanical systems (MEMS) devices, sensors and actuators requires, in addition, the development of innovative packaging technologies. Packaging has to simultaneously guarantee the long-term stability of electrical connections and the mechanical support of functional subsystems [1]. In several sensor applications the temperature-dependent mechanical stability of the structure is crucial. Due to the differences between thermal expansion coefficients of the MEMS structural materials and the package a significant offset or sensitivity shift can be experienced. The application of a reliably bonded supporting back substrate can improve the temperature sensitivity of the output signals of these critical systems [2]. Accordingly, selection and development of appropriate, economic wafer-bonding processes for the packaging technologies is critical to ensure proper mechanical and electrical integration of MEMS devices.

A variety of bonding processes is needed for the different sensor applications to fulfill specific functional requirements of the given structures. Anodic bonding is a conventional solution used in capacitive mechanical sensors, based a on movable electrode of silicon membrane and static-patterned metal counterelectrodeon a glass substrate [3, 4]. Several applications (including absolute pressure or vacuum gage sensors) require hermetic sealing or vacuum encapsulation of the MEMS structures [5, 6]. As a drawback of this case, however, the metallization runs in etched grooves making the hermetic sealing difficult.

Glass frit bonding can also provide proper sealing between wafers; however, the required geometry control is rather difficult [7–9].

Other structured adhesives (such as benzocyclobutene—BCB, polyimide, nafion, SU-8) are also viable alternatives for gluing or wafer bonding at relatively low temperature (\sim 400 °C) considering the limitation of precise and homogeneous intermediate gap formation [10–12].

Excellent vacuum sealing can be achieved by using specific intermediate layers (e.g. sputtered amorphous silicon) in glass-to-glass electrostatic wafer bonding, as required for field wmission displays (FEDs) and plasma display panels (PDPa) [13].

Phosphorus-doped polycrystalline silicon or aluminum and gold films are also used between silicon and glass wafers to

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Table 1. Typical process parameters applicable for metal diffusion bonding of gold, copper and, aluminum layers.

| Parameter | Au–Au | Cu–Cu | Al–Al |
|--|--|--|--|
| Resistivity ($\mu\Omega$ cm) | 2.20 | 1.69 | 2.67 |
| Melting point (°C) | 1064.4 | 1083 | 660.4 |
| CTE $(\times 10^{-6} \mathrm{K}^{-1})$ | 14.1 | 17.0 | 23.5 |
| Thermal conductivity (W mK ⁻¹) | 318 | 401 | 237 |
| Temperature range (°C) | 300-450 | 380-450 | 400-550 |
| Applied force range (kN) ^a | min. 40 | min. 30 | min. 18 |
| Process time (min) | 20–45 | 20–60 | 20-60 |
| Atmosphere | vacuum or H ₂ /N ₂ | vacuum or H ₂ /N ₂ | vacuum or H ₂ /N ₂ |
| $Cost (US\$lb^{-1})$ | 25 881.44 | 4.4198 | 1.1798 |

^a Applied force depends on wafer diameter and pattern density.

form localized fusion or metal eutectic bonding at relatively low temperature. In this case the surfaces are fused by an intermetallic phase formation at lower temperature than the melting point of the specific intermediate layer. Au eutectic bonding was presented in [14] using a 360 °C bonding temperature. In the case of localized heating the required temperature is mainly affected by the glass softening temperature (e.g. 820 °C for Pyrex glass) [15, 16].

Metal intermediate-layer bonding is also applied for low-temperature encapsulation and packaging of MEMS structures by utilizing intermetallic phase formation just above the eutectic point [17]. This solid–liquid interdiffusion (SLID) or transient liquid phase (TLP) bonding technique utilizes low-melting-point metal alloys to obtain high-melting-point bonds. First Au/In, Ag/In, and Cu/In metal systems were applied [18]; however, the most common alloys in the semi-conductor industry nowadays are Au/Sn, Ag/Sn, Cu/Sn, and Ni/Sn. The use of specific intermediate alloys as In/Sn or Ga/Sn facilitates additional temperature reduction (160 °C) as reported in [19, 20].

The thermal issues in these packaging techniques are rather critical from the point of view of the induced residual stresses; therefore, reduced-temperature or restricted, localized high-temperature treatment is preferred in several cases [21, 22].

The wafer scale packaging techniques described are focusing on mechanical bonding and sealing only, but not on a simultaneous electrical contact formation. The conventional method for backside contact formation is the flip-chip (or ball) bonding technique. For integration and packaging CMOS circuits or less complex MEMS structures solder bonding techniques are applied at chip scale with limited mechanical stability [23]. As a cheap alternative to the flip-chip bonding, anisotropic conductive film (ACF) can be applied as adhesive to form electrical and moderated mechanical backside contacts between the chips and the substrate [24].

To achieve adequate wafer-level electrical and mechanical packaging of the MEMS structures, complex vertical or lateral feed-through technology must be applied in combination with hermetic bonding processes (like anodic bonding) [25]. Using a suitable combination of bonding parameters during packaging the direct hybrid bonding is also applicable to form mechanical and electrical contacts between the functional parts of MEMS structures. The deposition of intermediate sticking layers (e.g. BCB) and formation of through silicon

via (TSV) structures, however, complicate the fabrication process [26].

To develop adequate packaging technology simultaneously providing high mechanical stability and excellent electrical contacts in the proposed MEMS applications is a real challenge. In view of possible industrialization the applied technology has to be implemented at wafer scale. Our aim is to offer a possible solution for cheap, quick, and reproducible bonding processes meeting the above criteria.

Metal thermocompression bonding combining the bonding of structural materials and the metallization of the surfaces to be fused is a conventional procedure in microtechnology for structural and electrical integration, hermetic sealing, and packaging of 3D MEMS systems. The method is generally applied in the case of packaging mechanical sensors to simultaneously ensure adequate backside electrical connections and mechanical stability in a wide temperature range [6].

The low-temperature metal thermocompression bonding utilizes the fusion of the touching metal surfaces by simultaneous application of force and heat. Both diffusion bonding and eutectic bonding are based on atomic migration across both metal surfaces in contact assisted by elevated temperature. Due to possible spontaneous surface oxidation of the metal layers, either extremely large force or relatively high temperature is normally required to break the contiguous oxide layer covering the contacting surfaces. In terms of achieving high bonding quality, the limitation of the thermal budget of MEMS and packaging technology is, however, absolutely desirable. The metal diffusion bonding is referred to as thermocompression or solid-state welding, indicating material transport at elevated temperature and pressure. Typical processing parameters for the metal diffusion bonding of gold, copper, and aluminum layers are summarized in table 1 [27-31].

Although the most common metallization layer in conventional CMOS and MEMS technology is aluminum, to achieve high-quality Al–Al bonding is a considerable challenge considering the force required, especially at wafer scale. The application of Au or Cu metallization is able to decrease the bonding temperature. The increased complexity and cost of MEMS processing as well as material compatibility issues must be, however, taken into account. From the technological and economical point of view the Al–Al diffusion bonding could be an optimal choice, considering the simplicity and

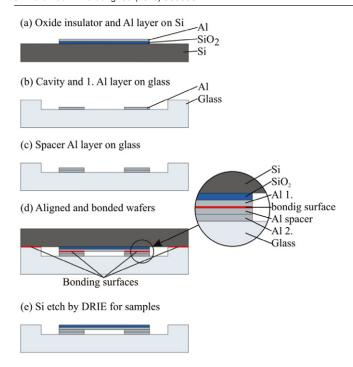


Figure 1. The process flow: (a) insulator and Al layer deposition on Si; (b)–(c) wet chemical etching and Al layer evaporation on glass; (d) wafer alignment and bonding; (e) sample preparation.

Table 2. Material composition of the applied Schott Borofloat[®]33 glass [34].

| B_2O_3 | Na ₂ O/K ₂ O | Al ₂ O ₃ | SiO ₂ |
|----------|------------------------------------|--------------------------------|------------------|
| 13% | 4% | 2% | 81% |

moderate cost of the technology sequence. However, homogenous, wafer-size bonding could be obtained, with adequate and reliable mechanical and electrical contacts, by applying appropriate force loading at low temperature. We used the extreme electrostatic force evolving between the silicon and glass substrates during anodic bonding to compress the metallic surfaces and simultaneously achieve wafer and metal diffusion bonding as shown in figure 1.

The anodic bonding occurs between silicon and special borosilicate glass wafer (specifications of Borofloat®33 glass are presented in table 2). The applied glass substrate contains mobile positive alkali ions, e.g. K⁺ and Na⁺, able at elevated temperature to migrate to the negatively charged cathode in the presence of a suitable electric field. Due to the shifting of these positively charged ions toward the cathode, a negatively charged region (mainly by fixed oxygen ions) is built up in the glass, which induces positive mirror-charges in the silicon wafer by depletion of mobile carriers in the vicinity of the contacting surfaces. Between the contacted surfaces extremely high electrostatic force can be generated by the space charges in this narrow region, which presses them together and promotes the formation of strong bonding by Si-O-Si atomic bonds. Figure 2 is the schematic representation of the bonding process. The parameters typically applied are also indicated; temperature: 200-450°C, electric potential: 200-2000V [32, 33].

Although the press-on metal contact formation during silicon-glass anodic bonding was presented earlier for different

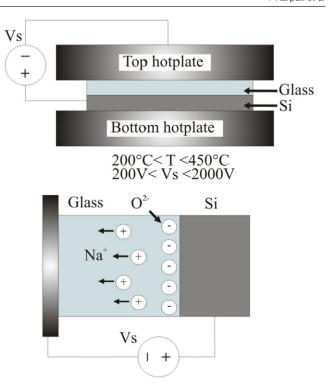


Figure 2. The scheme of anodic bonding.

micromechanical structures in [35, 36], the Al–Al metal diffusion bonding was not yet investigated in detail. In this work we confirm that the evolving electrostatic force assists the simultaneous metal bonding, thereby facilitating an electrical and mechanical packaging of the MEMS structure. Moreover, the nanoscale material structure of the metal contact formed was also analyzed to explain the electrical properties of the formed metal contacts.

The force range obtained for Al–Al metal fusion bonding by electrostatic compression is quite high (> $36 \, \text{kN}$ at $450 \,^{\circ}\text{C}$) [31]. The evolving electrostatic force between the surfaces to be bonded can be deduced from the Poisson equation (1):

$$\nabla^2 V = -\frac{\rho}{\epsilon},\tag{1}$$

where V is the applied electric potential and ρ and ε denote the charge density and the dielectric coefficient of the material, respectively. Applying a 1D model, while assuming that anions are immobile during the bonding process and wafer edge effects are neglected, equation (1) can be simplified:

$$\frac{\mathrm{d}^2 V}{\mathrm{d}x^2} = -\frac{\mathrm{d}E}{\mathrm{d}x} = -\frac{\rho_g}{\varepsilon_g},\tag{2}$$

where E is the evolving electric field and ρ_g and ε_g denote charge density and dielectric coefficient of the borosilicate glass. The electric potential distribution can be expressed as

$$V(x) = \frac{\rho_{\rm g}}{\varepsilon_{\rm g}} \left(xd - \frac{x^2}{2} \right) \tag{3}$$

where d is the thickness of the depletion layer. The electric field between the silicon and glass wafers to be bonded (E_b)

can be estimated as the function of the space charge built up on the glass surface, as indicated in figure 2:

$$E_{\rm b} = \frac{\rho_{\rm g} d}{\varepsilon_{\rm g}},\tag{4}$$

In equilibrium conditions during bonding the electric potential and the compressing force between the surfaces in contact can be estimated as follows:

$$V = \frac{\rho_{\rm g}}{\varepsilon_{\rm g}} \frac{d^2}{2}$$

$$F = \frac{\varepsilon_0 E_{\rm b}^2}{2} = \frac{\varepsilon_0 (\rho_{\rm g} d)^2}{2\varepsilon_{\rm g}^2}.$$

$$F = \frac{\varepsilon_0 \rho_{\rm g}}{\varepsilon_{\rm g}} V$$
(5)

The maximum value of this force could amount to 10^6 N as reported in [37]; however, it is mainly affected by the evolving space charge in the applied glass wafer. The charge distribution in the glass is determined by the process parameter-dependent ion mobility (e.g. as a function of temperature) [38], so for optimal bonding quality a critical parameter range can be defined [39]. Due to the thickness of the applied metalization in the range of $1-3\mu$ m, which is approximately 10-30 times thicker than the depletion layer, we can estimate a 30-100 kN pressing force between the surfaces of the contacting Al layers.

2. Experimental

The nanoscale formation of the metal contacts during the above-described electrostatic force-assisted metal diffusion bonding was studied for the reliable electrical and mechanical packaging of MEMS devices. Since the offset of the output signal and the sensitivity of mechanical sensor systems (e.g. pressure or force sensors) are extremely dependent on thermal loading, stability of electrical and mechanical bonding is crucial for the functionality. Special test structures were designed and fabricated to characterize the electrical contacts and the atomic scale material structure of the fused metal surfaces.

2.1. Design of the test structure

A special test structure was designed to ensure precise electrical characterization of the bonded metal surfaces by four-terminal resistance measurements. Aluminum test pads $(3400 \times 200 \,\mu\text{m})$ were formed on the SiO₂ insulator covered single-crystalline Si chip. Al wiring and bonding pads were delineated on the carrier Borofloat33® substrate as shown in figure 3. The process flow can be followed in figure 1.

A 500 nm-thick SiO₂ layer was deposited by atmospheric-pressure CVD (APCVD; ASM SOX 10–2) on silicon substrate as insulator between the metal wiring and the bulk Si. 500 nm-thick Al metallization was formed subsequently by electron-beam vacuum evaporation (Varian 3120H) and patterned by photolithography (SÜSS MicroTech MA6 mask

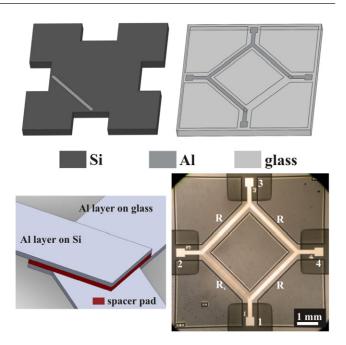


Figure 3. Schematic structures on the Si (left) and glass (right) substrates designed for bonding tests. The fabricated test structure is shown in the bottom right image.

aligner) (figure 1(a)). The Si chip was processed by deep reactive-ion etching (DRIE; Oxford Plasmalab System100) to form rectangular windows through the wafer facilitating a convenient wire bonding to the contact pads on the glass substrate.

On the glass carrier wafer an indentured pattern was defined by adequate photolithography and formed by wet chemical etching using buffered oxide-etch solution for $3\mu m$ depth (figure 1(b)). Two patterned Al layers were subsequently deposited into the recessed cavity by separate evaporation steps, having 1.5 and $0.5 \mu m$ thicknesses, respectively (figures 1(b) and (c)). The upper metal layer acts as a spacer between the main Al wires formed on the Si and the glass carrier substrates. The top surfaces of these Al spacer pads serve as contact surface during metal diffusion bonding. Moreover, the secondary Al layer allows additional thickness correction before the bonding step to ensure precise adjustment of the metallic contact between the two wafers. The thickness tolerance of the bonding process is estimated to be 100-150 nm; therefore, the Al layer thicknesses must be accurately controlled to achieve a reliable electrical contact. This requirement must be fulfilled in order to avoid the need for any additional polishing process (e.g. chemical-mechanical polishing—CMP). The frame size of the test chip is 7×7 mm with a thickness of 1 mm.

2.2. Wafer alignment and bonding process

SÜSS MicroTech MA6/BA6 Mask and Bond Aligner equipment was used for wafer alignment before anodic bonding. The wafers were fixed by clamps and transferred into the SÜSS MicroTech SB6L wafer bonder. The applied bonding parameters are summarized in table 3.

Table 3. Process parameters for metal diffusion bonding used for aluminum fusion.

| Voltage | - 1000V |
|-----------------------|-------------------------|
| Temperature | 450°C |
| Temperature ramp rate | 10 °C min ⁻¹ |
| Chamber pressure | $10^{-3}\mathrm{mbar}$ |
| Tool force | 8.8 kN |
| Electrode type | plate |
| Process time | 90 min |
| Atmosphere | $<10^{-3}{\rm mbar}$ |
| | |

2.3. Cyclic thermal shock test for studying mechanical and electrical stability of the contacts

For characterization of the mechanical and electrical stability of the Al–Al bonding, cyclic thermal shock tests were performed to reveal any possible degradation of the fusion between the Al surfaces. The test arrangement shown in figure 3 was heated at $100\,^{\circ}$ C for 1 min and cooled down to $-20\,^{\circ}$ C for 1 min. The resistance of the test structures consisting of two Al–Al contact pads, a reference Al line (between points 1 and 2 in figure 3), and a reference Al line (between points 3 and 4 in figure 3) were measured following every 20 thermal cycles. Their values were taken at room temperature.

2.4. Sample preparation for structural characterization

In order to provide easier sample preparation for atomic scale cross-sectional transmission electron microscopy (XTEM) analysis the Si was etched away from the test chip by DRIE (see figure 1(e)). The XTEM cross section of the bonded metal layer structure was revealed by using a focused ion beam milling process (JEOL LEO 1540XB) as shown in figure 4. The obtained thickness of the sample was estimated at ~40 nm, i.e. adequate for XTEM analysis.

3. Experimental results

In order to characterize the mechanical stability and electrical parameters of the bonded interconnections, tensile strength, resistance measurements, and atomic scale structural analysis were performed.

Results of the bonding strength and electrical characterization were published elsewhere [40] previously. The *I–V* characteristics proved perfect Ohmic resistance of the interconnections. *The total resistance value obtained across the two contacting and the spacer Al layers was 0.2*. The total bonded area in a test chip was estimated as 34.18 mm² and the measured bonding strength was approximately ~22 MPa. In order to compare the electrostatically assisted and the thermocompression Al–Al bonding [31] typical parameters of the fused structures are summarized in table 4.

For verifying the mechanical and electrical stability of the bonded Al–Al surfaces, cyclic thermal shock tests were performed. The contact resistance was measured after every 20 cycles. In figure 5 the resistance of the measurement setup (consisting of two contact pads and a reference Al line) and

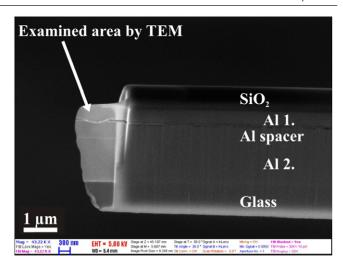


Figure 4. SEM image of the bonded metal layer structure cross section obtained by FIB milling for XTEM analysis.

the resistance of the contact pad is presented. The resistance change obtained following cyclic heating and cooling is less than 10%. Note that after 60 cycles the decreased resistance was measured following relaxation for a night. We established that the resistances of the Al–Al contacts were not degraded significantly as a consequence of cyclic thermal shock. Therefore, we can conclude that the applied bonding process is able to produce reliable and stable metal contacts for backside packaging.

The cross section of the metal layer structure was studied by high-resolution transmission electron microscopy (JEOL JEM-3010). The nanoscale structure of the contact surface between the Al layers is shown in figure 6. The XTEM image clearly reflects the native Al₂O₃ layer between the metal surfaces broken-up during the bonding process and reveals the conducting metal channels between the oxide grains.

Atomic resolution XTEM image was recorded to characterize the nanoscale structure of the fused metallic channels. The metal lattice of the Al is revealed in figure 7 showing ~ 2.34 and $2.025 \,\text{Å}$ atomic distance periods corresponding to Al <111> and Al <200> planes, respectively.

The presence of the multicrystalline metal grain structure is also verified by electron diffraction in figure 8. As confirmed by the diffraction map the <111> is the dominant grain orientation in the fused interface. This observation clearly coincides with the results presented in [41] and can be explained by the bonding mechanism. The grains in the fused interfaces could be reoriented during the bonding process to ensure the atomic planes to be parallel with the bonded interface and to achieve the most compact atomic area packing.

4. Conclusions

In this work the metal contact between Al wiring placed on separate Si and glass wafers fused by a low thermal budget anodic bonding was analyzed. In systemin-package (SiP) solutions the developed electrostatic force-assisted

Table 4. Typical parameters of the electrostatically assisted and the thermocompression Al-Al bonded structures.

| Bonding type | Electrostatic-assisted | Thermocompression |
|-----------------------|---|--------------------------------|
| Voltage | -1000 V | |
| Temperature | 450°C | 450°C |
| Tool force | $8.8\mathrm{kN}$ | 36kN |
| Process time | 90 min | 60 min |
| Dicing yield | almost 100% | almost 100% |
| Strength | ~22 MPa (square; $4 \times 200 \times 200 \mu m$) | 30–50 MPa (geometry-dependent) |
| Electrical resistance | 0.2Ω (contact area: $200 \times 200 \mu m$) | _ |

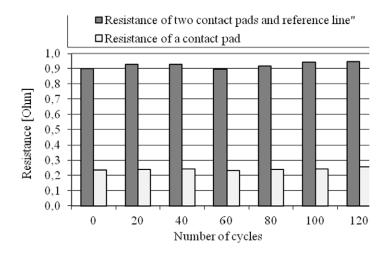


Figure 5. Resistance change of measured Al-Al contacts with and without connected Al reference line.

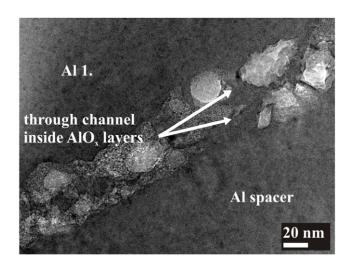


Figure 6. Cross section XTEM image of the bonded Al interfaces. The arrows indicate the fusion of the Al layers across the AlO_x layers.

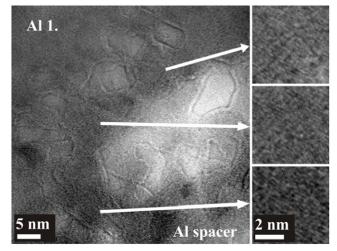


Figure 7. Atomic structure of Al metal grains forming conducting channels between the diffusion bonded metal layers.

Al fusion bonding offers potential CMOS compatibility for bonded MEMS.

Besides reliable silicon–glass bonding, Al–Al bonding was also achieved in conventional anodic bonding equipment, at the moderate temperature, voltage, and pressure conditions offered by the tool. Mechanically and electrically stable Ohmic contacts were formed between the Al layers as proven by the established bond-strength and *I–V* measurements. The reliability of the Al–Al bond was verified by cyclic thermal

shock tests. The resistance values of the stressed electrical contacts proved to change by less than 10%. The Al fusion between the surfaces in contact was analyzed on the nanoscale by XTEM microscopy. Between the individual Al_2O_3 grains conducting metal channels were formed in the multicrystal-line matrix. The electrically conductive and mechanically strong bonds between the silicon sensor chips and the metalized glass carrier substrate are formed in a single step by the proposed method. The simultaneously obtained features

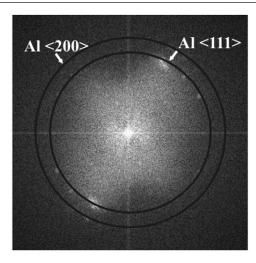


Figure 8. Electron diffraction map of the multicrystalline Al metal structure in the conducting channel.

facilitate a reliable mechanical support and backside electrical contacts [40]. Thereby the wafer-level solution presented is an alternative to the cumbersome TSV-based packaging technology. Care has to be taken with proper selection of the applied materials and complexity of the processes. Due to the backside glass carrier support a slight increase in the die size has to be taken into account.

AQ3 Acknowledgments

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