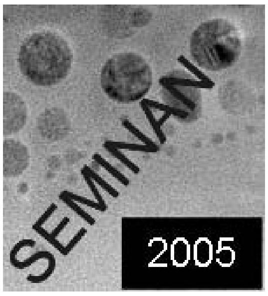
SEMICONDUCTOR NANOCRYSTALS
Volume 2

Proceedings of the First International Workshop on Semiconductor Nanocrystals, SEMINANO2005

September 10-12, 2005
Budapest, Hungary



Editors:
B. Pődör, Zs. J. Horváth, P. Basa

Felelős kiadó: Magyar Tudományos Akadémia
Műszaki Fizikai és Anyagtudományi Kutató Intézet, Budapest
Készült a Budapesti Műszaki Főiskola Nyomdájában
Munkaszám: 144/2005
ISBN 963 7371 20 6, ISBN 963 7371 18 4
Műszaki vezető: Bélteky István

First International Workshop on Semiconductor Nanocrystals,
SEMINANO2005, September 10-12, 2005, Budapest, Hungary

Si nanocrystals in sandwiched SiN_X structures

Zs. J. Horváth, P. Basa, P. Petrik, Cs. Dücső, T. Jászi,
L. Dobos, L. Tóth, T. Lohner, B. Pécz, and M. Fried

Hungarian Academy of Sciences
Research Institute for Technical Physics and Materials Scienc
Budapest 114, P.O.Box 49, H-1525 Hungary
E-mail: horvzsj@mfa.kfki.hu, ducso@mfa.kfki.hu, basa@mfa.kfki.hu

The structure and composition of multilayered SiN_x structures prepared by low pressure chemical vapour deposition were studied by cross-sectional transmission electron microscopy and spectroscopic ellipsometry. Using appropriate deposition parameters and post deposition annealing, well separated Si nanocrystals were obtained with avarage grain size of 8-10 nm.

1. Introduction

Dielectric layers with embedded semiconductor nanocrystals have been widely studied recently, in order to overcome difficulties of non-volatile memory devices connected with technology scale-down, and to develop Si-based light emitting diodes (LED's). One of the methods used for creating Si nanocrystals in SiO_x, is the high temperature annealing of these films containing excess Si. It has been reported recently that this method is suitable for Si-rich SiN_x layers prepared by plasma-enhanced chemical vapour deposition (PECVD) as well [1]. However, in our recent experiment with annealed single Si-rich SiN_x layers with 7-10% excess Si grown by low pressure chemical vapour deposition (LPCVD), no nanocrystals were obtained after annealing in forming gas in the temperature range of 900-1100 °C [2,3]. On the other hand, Si nanocrystal formation was obtained recently even in as-grown PECVD Si-rich SiN_x layers without post deposition annealing [4,5]. In this work we report a third method for Si nanocrystal formation in SiN_x layers using a thin nanoscrystalline Si layer sandwiched between two Si-rich SiN_x layers.

2. Experimental

Two different multilayered structures were studied. The layers were deposited on monocrystalline Si substrates by LPCVD at 830 °C and 30 mPa using SiH_2Cl_2 and NH_3 in three steps. The first bottom layer was deposited with flow rates of SiH_2Cl_2 and NH_3 of 100 and 25 sccm, respectively. The flow rates for the middle layers different in the two structures, were 100 and 0 sccm (Wafer SZ1) or 150 and 10 sccm (Wafer SZ3), respectively. The third top layer was grown with the same parameters as the bottom layer. The deposition time was 5 min for each layer. So, a sandwiched structure was expected with a thin middle fine-grained polycrystalline Si layer, embedded between Si-rich SiN_x layers. After the deposition, the wafers were cut to pieces of about 1 cm^2. A few of them were annealed in forming gas (95% N_2 and 5% H_2) at 1000 °C for 1 hour.

The structures were studied by cross-sectional transmission electron microscopy (XTEM) and spectroscopic ellipsometry.

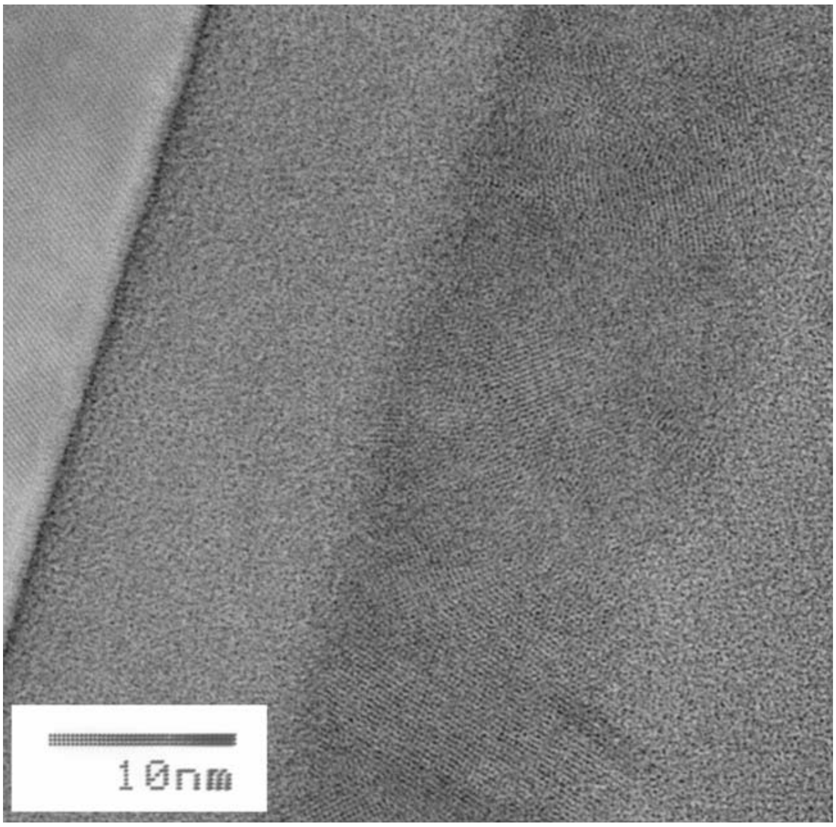


Fig. 1. Cross sectional transmission electron microscope image of Wafer SZ1 with nanocrystalline Si layer sandwiched between two amorphous SiN_x layers

3. Results and discussion

XTEM pictures showed a nanocrystalline Si middle layer in Wafer SZ1 with grain sizes of a few nm, as presented in Fig. 1. After annealing the grains became larger and well separated with amorphous phase. The avarage size of nanocrystals was about 8-10 nm.

However, no crystallites were found in the middle layer of Wafer SZ3, even after annealing. The change of the SiH_2Cl_2 flow rate from 100 sccm to 150 sccm yielded such a significant difference. The exact mechanism of this effect isn't understood yet.

The results of spectroscopic ellipsometry presented in Table 1 for Wafer SZ1 [6], are in good agreement with the XTEM results. In the evaluation of the obtained spectra, the non-stoichiometric top and bottom SiN_x layers were modelled by a mixture of Si_3N_4 and amorphous Si. For the middle layers, crystalline Si, nanocrystalline Si and amorphous Si components were used. However, it was obtained that a good fit of theoretical spectra to the experimental ones required an additional SiO_2 layer at the top of the structure [6], as presented in Table 1.

The thickness of the as-grown layers is about 18 nm in good agreement with the XTEM results. It yields a growth rate of 3.6 nm/min for the SiH_2Cl_2 flow rate of 100 sccm. Due to these results, the middle layer consists of 86% nanocrystalline Si, 4% amorphous Si and 10 % crystalline Si with larger grain sizes. The bottom layer contains about 17% excess Si in Si_3N_4 layer. However, the top layer deposited at the same conditions, contains about

6.5% excess Si only. This indicates a diffusion of Si from the top layer into the middle layer during the deposition of the top layer.

After annealing the Si content of the top layer decreased further to 4.5%. This confirms the diffusion of Si atoms from the top to the middle layer. However, the thickness of the top SiN_x layer also decreased with 4 nm, while the thickness of the top SiO_2 layer increased with 6 nm. This indicates the oxidation of a part of the top SiN_x layer. During annealing a part of excess Si might also oxidize. But, this oxidation isn't clear either, since forming gas is a reducing atmosphere.

There was also a significant change in the composition of the middle layer after annealing. The decreeased nanocrystalline Si to crystalline Si ratio means that the amount of the crystalline phase increased, which is consistent with an increase of the long-range order and an increase of the grain size [6], in agreement with XTEM results.

Table 1. The thickness and composition of layers on Wafer SZ1 obtained by spectroscopic ellipsometry

	Wafer SZ1	
	as-deposited	annealed
Top SiO_2 layer thickness (nm)	1.015±0.14	7.29±0.14
Top SiN_x layer thickness (nm)	18.2±0.08	13.94±0.09
Top SiN_x layer composition (a-Si %)	6.48±0.15	4.54±0.20
Middle nc-Si layer thickness (nm)	17.2±0.19	17.62±0.14
Middle nc-Si layer composition (nc-Si + a-Si %)	85.99±2.06 + 4.09±0.52	77.74±1.56 + 2.22±0.4
Bottom SiN_x layer thickness (nm)	18.6±0.41	18.84±0.31
Bottom SiN_x layer composition (a-Si %)	17.28±3.11	16.96±2.35

4. Conclusions

The structure and composition of multilayered SiN_x structures prepared by low pressure chemical deposition from SiH_2Cl_2 and NH_3, were studied by cross-sectional transmission electron microscopy and spectroscopic ellipsometry. Nanocrystalline Si layer with a thickness of 18 nm embedded between two Si-rich SiN_x layers was obtained by appropriate deposition parameters. After annealing performed in forming gas at 1000 ^oC for 1 hour, the grains became larger and well separated with an avarage size of 8-10 nm. The annealing affected the composition and thickness of the top SiN_x layer as well.

Acknowledgement

This work has been supported by the (Hungarian) National Scientific Research Fund under Grant No. T048696 and by the European Comission in the frame of FP6 project SEMINANO No. 505285.

References

[1] Z. Pei, H. L. Hwang, Appl. Surf. Sci., **212-213**, 760, 2003.
[2] P. Szöllősi, P. Basa, Cs. Dücső, B. Máté, M. Ádám, T. Lohner, P. Petrik, B. Pécz, L. Tóth, L. Dobos, L. Dózsa, Zs. J. Horváth, Current Appl. Phys., in press.
[3] Zs. J. Horváth, Cs. Dücső, P. Basa, P. Szöllősi, T. Lohner, P. Petrik, L. Dobos, B. Pécz, L. Tóth, M. Fried, Proc. 1st Int. Workshop on Semiconductor Nanocrystals, SEMINANO2005, Sept. 10-12, 2005, Budapest, Hungary, p. 201.
[4] T.-Y. Kim, N.-M. Park, K.-H. Kim, G. Y. Sung, Y.-W. Ok, T.-Y. Seong, C.-J. Choi, Appl. Phys. Lett., **85**, 5355, 2004.
[5] K. S. Cho, N.-M. Park, T.-Y. Kim, K.-H. Kim, G. Y. Sung, J. H. Shin Appl. Phys. Lett., **86**, 071909, 2005.
[6] P. Basa, P. Petrik, Proc. Int. Semicond. Conf. CAS2005, Oct. 3-5, 2005, Sinaia, Romania, in press.