AN EXPLORATORY STUDY OF PULSE WIDTH AND

DELTA SIGMA MODULATORS

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Logan Penrod

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COMMITTEE MEMBERSHIP

TITLE: An Exploratory Study of Pulse Width and
Delta Sigma Modulators

AUTHOR: Logan Penrod

DATE SUBMITTED: December 2020

COMMITTEE CHAIR: Vladimir Prodanov, Ph.D.
Professor of Electrical Engineering

COMMITTEE MEMBER: Tina Smilkstein, Ph.D.
Associate Professor of Electrical Engineering

COMMITTEE MEMBER: Wayne Pilkington, Ph.D.
Associate Professor of Electrical Engineering

ABSTRACT

An Exploratory Study of Pulse Width and
Delta Sigma Modulators

Logan Penrod

This paper explores the noise shaping and noise producing qualities of Delta-Sigma Modulators (DSM) and Pulse-Width Modulators (PWM). DSM has long been dominant in the Delta Sigma Analog-to-Digital Converter (DSADC) as a noise-shaped quantizer and time discretizer, while PWM, with a similar self oscillating structure, has seen use in Class D Power Amplifiers, performing a similar function. It has been shown that the PWM in Class D Amplifiers outperforms the DSM [1], but could this advantage be used in DSADC use-cases? LTSpice simulation and printed circuit board implementation and test are used to present data on four variations of these modulators: The DSM, PWM, the out-of-loop discretized PWM (OOLDP), and the cascaded modulator. A generic form of an Nth order loop filter is presented, where three orders of this generic topology are analyzed in simulation for each modulator, and two orders are used in physical testing.

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BACKGROUND

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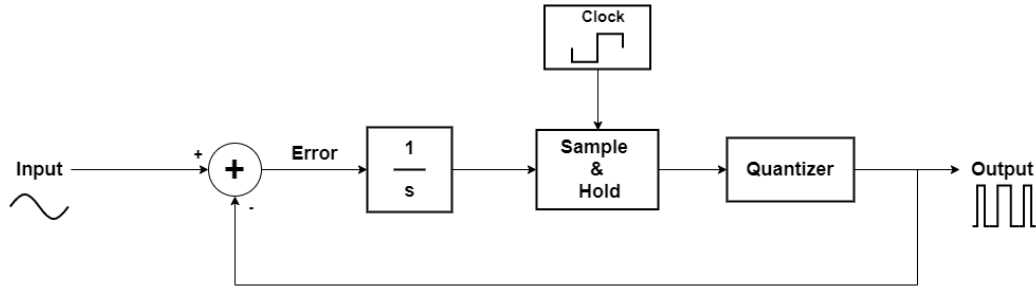
Figure 1.1: Delta Sigma Modulator Block Diagram

Figure 1.1 above shows a simple first-order one-bit delta-sigma modulator block diagram. The modulator encodes the value of the continuous-valued input in a series of pulses with discretized magnitude and time duration [2]. Given that the output of the integrator is bounded, that is Equation 1.1 is satisfied, then the average value of the output and input must be identical. Any long period discrepancies between the input and output averages would result in continual drifting of the continuous-time integrator, thus producing an unbounded result, negating Equation 1.1. Therefore, the average value of the input is encoded in the output as a series of binary-valued discrete time pulses.

$$\int (Vin - Vout)dt \leq Bound \tag{1.1}$$

An example delta-sigma modulator input and output are shown below in Figure 1.2. The Figure shows the modulator output given DC values from Negative Full-Scale

(NFS) to Positive Full Scale (PFS). The output pulse width and density changes with the input value, much like a Pulse Width Modulator or Pulse Density Modulator.
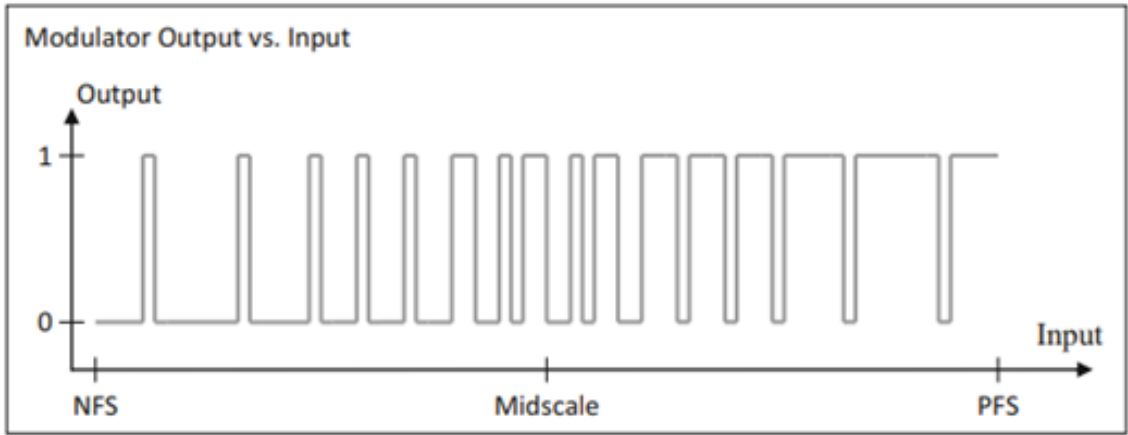
Figure 1.2: Delta Sigma Modulator Input and Output [2]

1.2 Quantization

When the magnitude of a continuous-valued signal is discretized, information about that signal is lost. The difference between the continuous and discrete valued signal is known as quantization error [3], this is graphically represented in Figure 1.3.
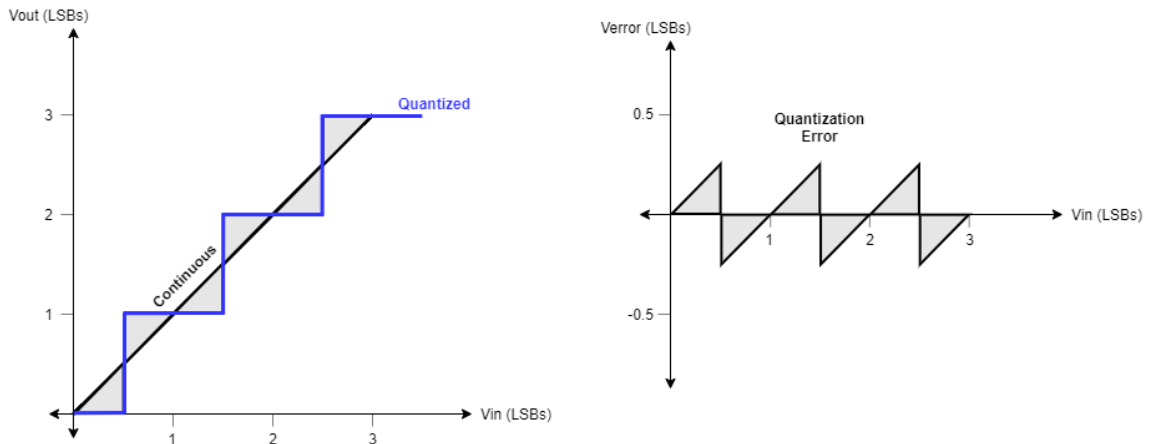
Figure 1.3: A Graph of Quantization Error

Figure 1.3 shows the input-output relation of a 4-level quantizer. The continuous input signal is given in black and the resulting 4-level output is given in blue. The shaded region between the continuous input and quantized output is highlighted gray in the left side of 1.3 and plotted on the right side. Though the error in this figure is shown for a full-scale ramp function, the error is fundamental to all forms of quantization and exists for any varying signal in every case. For the purposes of this paper, and as has been done in numerous others [2], the quantization error given a full-scale ramp input will be used for analysis. Though the quantization error correlates to the input signal and the resolution of the quantizer, the error can be thought of as an additive band-limited noise for signals that traverse between multiple bins per period [2]. The RMS-square values of the quantization noise and the signal-to-noise ratio of an ideal quantizer for a full-scale sinusoidal input are given in Equations 1.2, 1.3, and 1.4 [4].

$$N_{Quant}(V_{RMS}^2) = \frac{1}{V_{LSB}} \int_{-0.5V_{LSB}}^{+0.5V_{LSB}} Error^2 dV_{in} = \frac{V_{LSB}^2}{12} \tag{1.2}$$

$$Signal(V_{RMS}^2) = (\frac{FS}{2\sqrt{2}})^2 = \frac{FS^2}{8} = 2^{2n-3} \cdot V_{LSB}^2 \tag{1.3}$$

$$SNR(dB) = 10\log_{10} \frac{Signal}{N_{Quant}} = 6.02n + 1.76 \tag{1.4}$$

Therefore, quantization noise can be reduced by increasing the resolution of the quantizer. Intuitively, a more precise, or higher resolution, quantizer will more accurately capture the input signal and the difference between the discrete and continuous-valued representations will be diminished. By the Nyquist sampling theorem, the bandwidth of any sampled signal is half of the sampling rate. Therefore, in what other ways,

though, can the quantization noise be reduced? This will be discussed more in further sections.

1.3 Sampling Error

Sampling errors generally arise from clipping, aliasing, and clock jitter [5][6]. Though these errors may seem to only appear in the discrete time modulators, they can occur due to comparator hysteresis in the continuous time case as well.

First, op amp clipping introduces nonlinear effects in the circuit, and can result in poor noise shaping or outright errors in the output. Clipping normally occurs when comparator hysteresis is too wide or sample period is too long. Under most normal operating conditions of the delta sigma modulator, clipping is little to no issue.

Aliasing can occur both from the input to the modulated output of the loop, as well as in the sampling of the integrated error signal. Aliasing occurs when the sampled signal contains high frequency components that spectrally bleed in-band causing unwanted distortion. While the integrator is low-pass in nature, and the op amp bandwidth generally omits high frequency components, aliasing can still occur in a delta sigma modulator.

Clock jitter arises from differences in timing from clock edge to clock edge. This results in a smearing of the frequency content of the clock, and can assist in op amp clipping and result in mistiming of the output signal and feedback as well as unexpected spectral responses of the loop. In some cases, significant increases in quantization noise, and reduction in noise shaping can result from clock jitter[7].

1.4 Delta Sigma Modulator Noise Shaping

The delta-sigma modulator (DSM) can be analyzed in the time or frequency domain. In previous sections, the basic working principles have been explained mostly in the

time domain, but to fully understand the control loop, frequency domain analysis is required. Under the tacit assumption of uncorrelated signal and quantization noise, quantization noise within the modulator's quantizer can be modeled additively with a band-limited noise source in the quantizer itself. Figure 1.4 shows the additive nature of the quantization noise, allowing for analysis of the quantization noise within the loop. Additionally, sampling errors are introduced in the Sample-and-Hold of the loop.
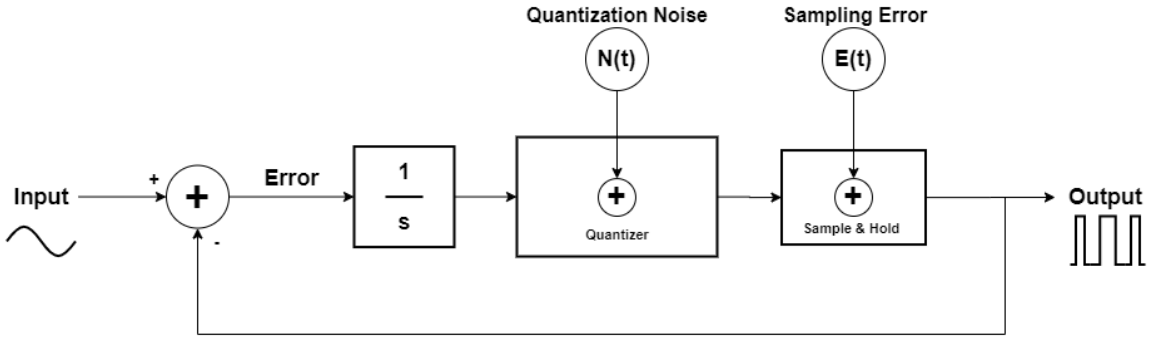
Figure 1.4: Delta Sigma Modulator with the Addition of Noise Sources

Following Figure 1.4 above, one can approximate the output signal as a linear addition of the input signal and noise sources, as shown in equations 1.5, 1.6, and 1.7 below. Additionally, it should be noted that the Sample-and-Hold and Quantizer are commutative, and both the quantization and sampling noise sources will see the same noise shaping regardless of circuit order.

$$V_{int} = -\frac{V_{in} - V_{out}}{s} \tag{1.5}$$

$$V_{out} = -\frac{V_{in} - V_{out}}{s} + N(s) + E(s) \tag{1.6}$$

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$$V_{out} = V_{in} \cdot \frac{1}{1+s} + (N(s) + E(s)) \cdot \frac{s}{1+s} \qquad (1.7)$$

The output can be interpreted as an addition of the input signal and noise sources, with a separate signal and noise transfer function as in Equation 1.8. The signal transfer function shows low-pass filtering while the noise transfer function shows high-pass filtering. For a first-order integrator loop filter, both transfer functions are of first-order. It can be shown, however, that as the order of the loop filter integrator increases, the order of the high-pass noise transfer function increases too. If the signal of interest lies in the reject band of the high-pass noise transfer function and in the pass-band of low-pass signal transfer function, the output can be low-pass filtered to produce a higher signal to quantization noise ratio than an open loop quantizer of the same resolution would. Additionally, higher order integrator loop filters can increase the noise transfer function roll-off and produce even higher signal to quantization noise ratios.

$$V_{out} = V_{in} \cdot STF + (N(s) + E(s)) \cdot NTF \qquad (1.8)$$

In this example, a simple first-order integrator was used to accumulate error over time. Higher order integrators, or loop filters with transfer function H(s) can be used as error accumulators, resulting in a more general equation for the STF and NTF given in Equations 1.9 and 1.10 below [8]. This establishes that for higher order loop filters, higher order noise shaping can be achieved.

$$STF = \frac{H(s)}{1 + H(s)} \qquad (1.9)$$

6

$$NTF = \frac{1}{1 + H(s)} \tag{1.10}$$

1.5 Pulse-Width Modulator

As with a delta-sigma modulator, the average value of the output of a Pulse-Width Modulator matches the average value of the input signal. For a discrete-time delta-sigma modulator, the output can only change value on a clock edge and sampling errors are introduced, as in Figure 1.4. With a continuous-time Pulse-Width Modulator, however, because no sampling occurs, these errors are not present in the same way. The rate at which the pulse width modulator operates is not dependent on a clock, but instead on the time constant of the integrator, the hysteretic window of the comparator, and the value of the input signal [1].
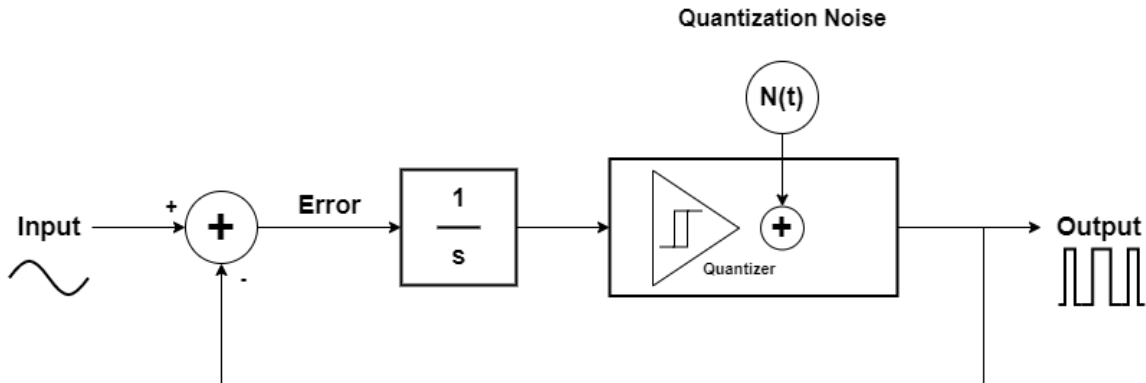
Figure 1.5: Pulse-Width Modulator

In this case, the output exhibits a higher SNR than the delta-sigma modulator due to asynchronous quantizer updates. However, this modulator is not practical in a delta-sigma analog to digital converter, as the output of the modulator must be synchronous to the digital low-pass filter to avoid aliasing and other forms of distortion [9], [1]. In class D Amplifiers, however, PWM is often preferred to DSM due to favorable noise shaping, and the need for high oversampling in DSM for audio [1]. While

the frequency of the loop is set by parameters listed previously, it will not be a stationary frequency as the input signal changes value over time and the loop requires discretization through either a simple Sample-and-Hold circuit, or through cascading with a delta-sigma modulator. Given the advantageous nature of PWM in Class D Amplifiers, perhaps some time discretization technique could bring that advantage to the PWM as a Delta Sigma Modulator used in Analog to Digital Conversion.

1.5.1   Time Discretization of a Continuous Time Loop

Lam et al. [5] have shown that a PWM followed by a DSM can yield improved power supply rejection and harmonic distortion, but can it yield improved noise shaping over a simple discrete time case? In this section, two methods for discretization of the continuous time PWM will be analyzed. First, a flip-flop could discretize the signal. This is a simple, but poor solution. First, the flip-flop could simply be introduced in the forward path of the modulator, thus allowing the loop to settle with discrete time, rather than potentially missing a change from discretizing out of the loop. Therefore, a discrete time delta-sigma modulator would be preferable in most cost cases. Nevertheless, the loop, which we will call the out-of-loop discretized PWM in this paper, is considered for the benefits of low complexity and the possibility to integrate the flip-flop in the low-pass filter stage of the delta-sigma ADC, or in use in a continuous time DSP stage [9]. The advantages and disadvantages of this topology are shown in Table 1.1. Figure 1.6 shows the flip-flop as a Sample-and-Hold device, where the output values are only able to change on a clock edge. Sampling errors such as aperture error, aliasing, and jitter would be added outside of the control loop and would see no noise shaping.

Table 1.1: Cost/Benefit Analysis of Out-of-Loop Discrete Time PWM as a DSM

Benefits	Costs
Low Complexity	No Sample Noise Shaping
Could be integrated into DSP Stage	Few advantages over DSM
CT Output Possible	Requires Clock Signal
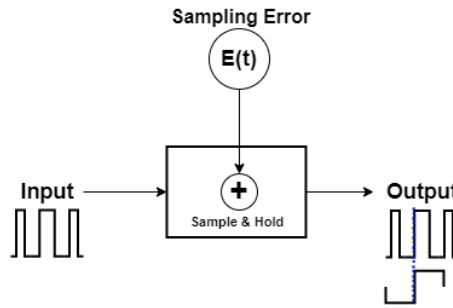
Figure 1.6: Sample-and-Hold as a Time Discretizer

An alternative approach is to introduce the discrete time DSM, as shown in Figure 1.7 below. This would offload sampling error shaping and correction from the first stage, that is the continuous time PWM, to the output stage where discretization alone is at hand in the error correcting loop. As discussed previously, Lam et. al [5] used this method in their audio amplifier and showed improved performance over conventional methods.
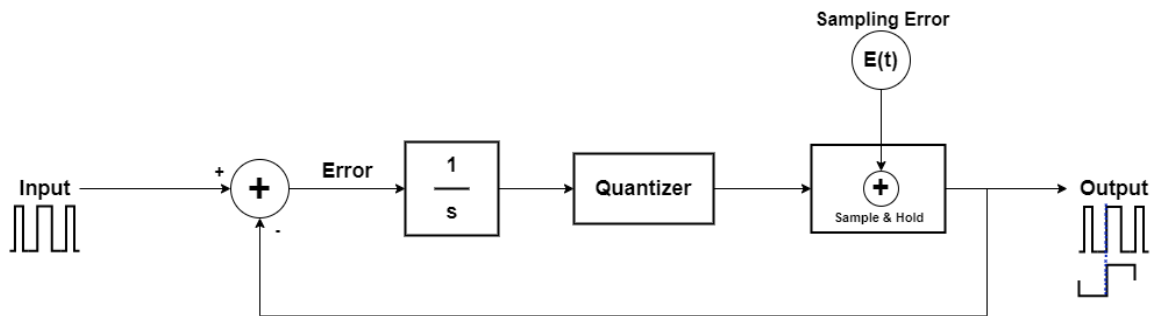
Figure 1.7: DSM as a Time Discretizer

The cascade of a PWM and DSM could allow for better performance in total harmonic distortion, and quantization and sampling noise in-band. This cascade is shown in Figure 1.8.
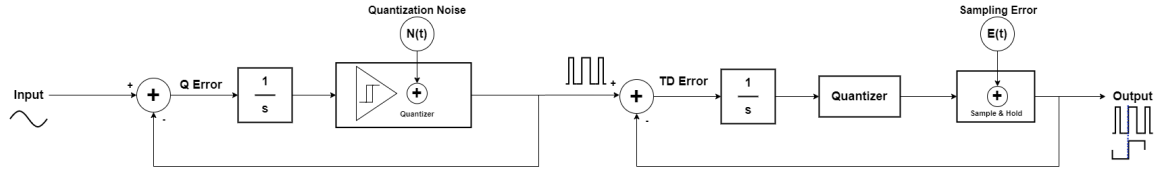
Figure 1.8: Cascaded PWM and DSM

The costs and benefits of using this design are outlined in Table 1.2.

Table 1.2: Cost/Benefit Analysis of the Cascaded DS Modulator

Benefits	Costs
Sampling Error Shaping	Adds Design Complexity
Provides a CT and DT Output	More Intrinsic Noise Added
Increases PSRR and Lowers THD [5]	Requires Clock Signal

Chapter 2

SIMULATION

2.1 Modulator Components

2.1.1 Loop Filter

Classically, a first or second order integrator is used as a loop filter in DSM and PWM [5, 10, 11]. Higher order filters have been used, but are often rejected due to conditional stability and the need for low component mismatch [12]. Nevertheless, N order noise shaping can be achieved with a single loop filter by expanding on the ideas in [10, 11], and as expected from Equation 1.10. By stacking series capacitors with shunt resistors in the feedback network of the loop filter, therefore implementing an additional integrator pole and left-half plane (LHP) zero for each RC added in the network, an N order can be achieved following the schematic in Figure 2.1. The LHP zero is crucial in keeping BIBO stability of the loop where multiple integrator poles could otherwise cause phase issues with the feedback signal. Note capacitor values scaling linearly with order and resistor values scaling linearly with one less than the order. By keeping with these passive component values, the signal transfer function and loop bandwidth will be retained, while adding additional integrator poles and LHP zeros. For higher values of N, component mismatch becomes progressively more obtrusive to zero placement, thus this circuit is not advised for physical implementation of high order filters due to potential BIBO stability violations.
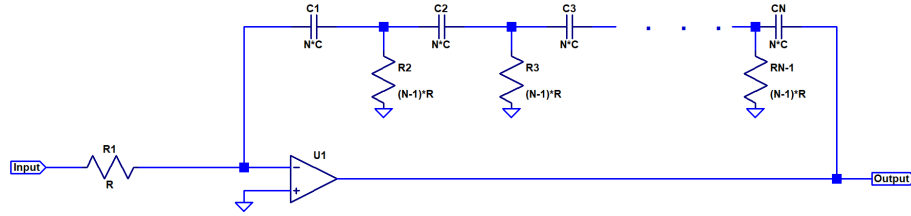
Figure 2.1: N Order Integrator General Schematic

N = 1, 2, and 3 of 2.1 will be utilized separately as the loop filters in simulation. These integrator LTSpice schematics are given in Figures 2.2, 2.3, and 2.4 below, with transfer functions in Equations 2.1, 2.2, and 2.3. Note the transfer functions implementing N integrator poles and N-1 LHP zeros.
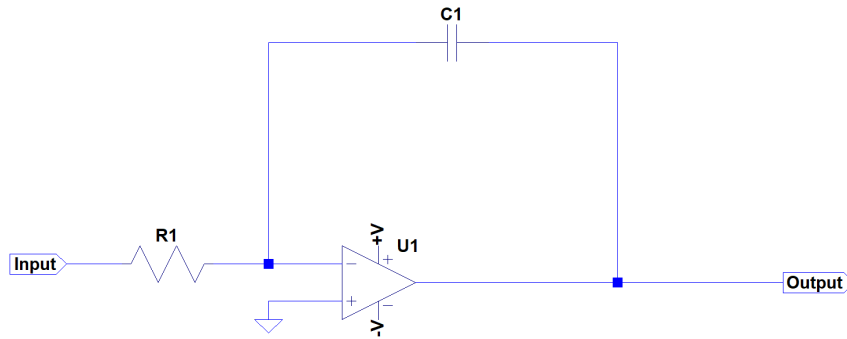
Figure 2.2: First Order Integrator Schematic

$$H(s) = -\frac{1}{(C1R1)s} \tag{2.1}$$
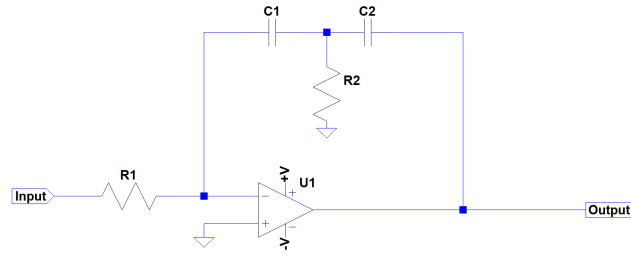
Figure 2.3: Second Order Integrator Schematic (2 Poles at Origin)

$$H(s) = -\frac{(C1R2 + C2R2)s + 1}{(C1C2R1R2)s^2} \qquad (2.2)$$
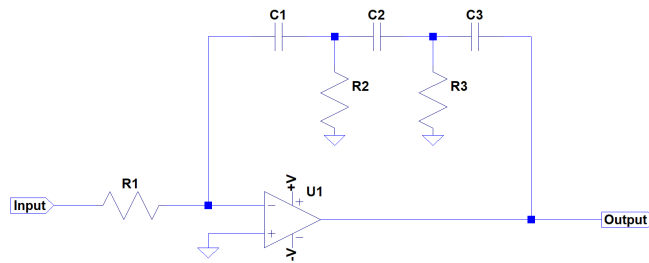
Figure 2.4: Third Order Integrator Schematic

$$H(s) = -\frac{(C1C2R2R3 + C1C3R2R3 + C2C3R2R3)s^2 + (C1R2 + C2R3 + C2R2 + C3R3)s + 1}{(C1C2C3R1R2R3)s^3} \qquad (2.3)$$

For the entirety of Chapter 2, Loop Filter Values in Table 2.1 are used, following Figure 2.1.

Table 2.1: Loop Filter Values

Order	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C1 (nF)	C2 (nF)	C3(nF)
1	10	-	-	1	-	-
2	10	10	-	2	2	-
3	10	20	20	3	3	3
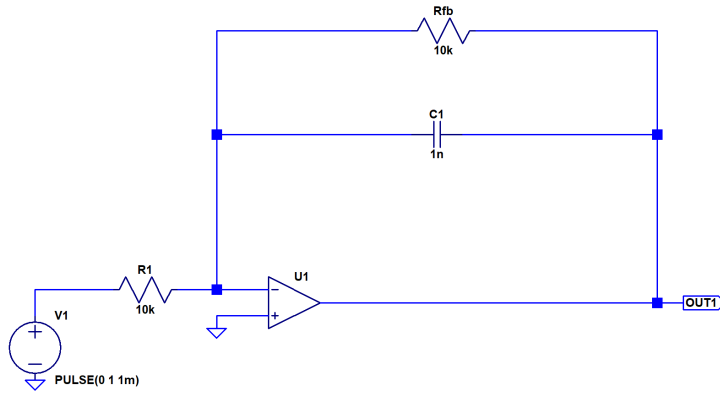
Figure 2.5: 1st Order Loop Filter Step Response LTSpice Schematic
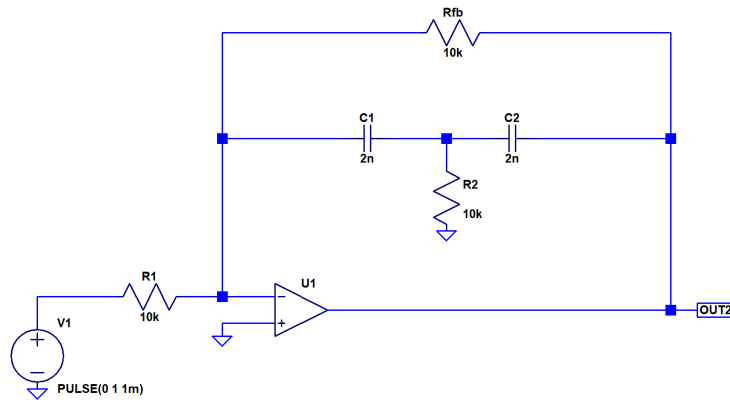
Figure 2.6: 2nd Order Loop Filter Step Response LTSpice Schematic
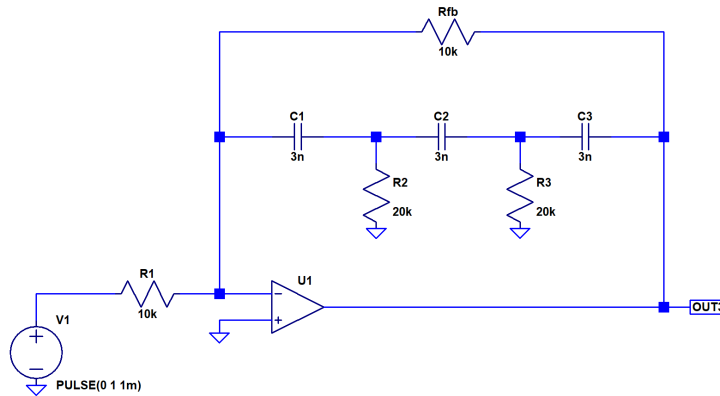
Figure 2.7: 3rd Order Loop Filter Step Response LTSpice Schematic

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Figures 2.5, 2.6, and 2.7 show the LTSpice schematics for testing the signal transfer function of the 1st, 2nd, and 3rd order integrator loop filters from Figures 2.2, 2.3, and 2.4. Figure 2.8 shows the result of the simulation. The input (n002) is shown in teal, while the output of each filter is given in black, blue, and red for 1st, 2nd, and 3rd order respectively. The same schematic was used to test the signal transfer function, but the step generator was replaced with an AC source and AC analysis was done instead of transient.
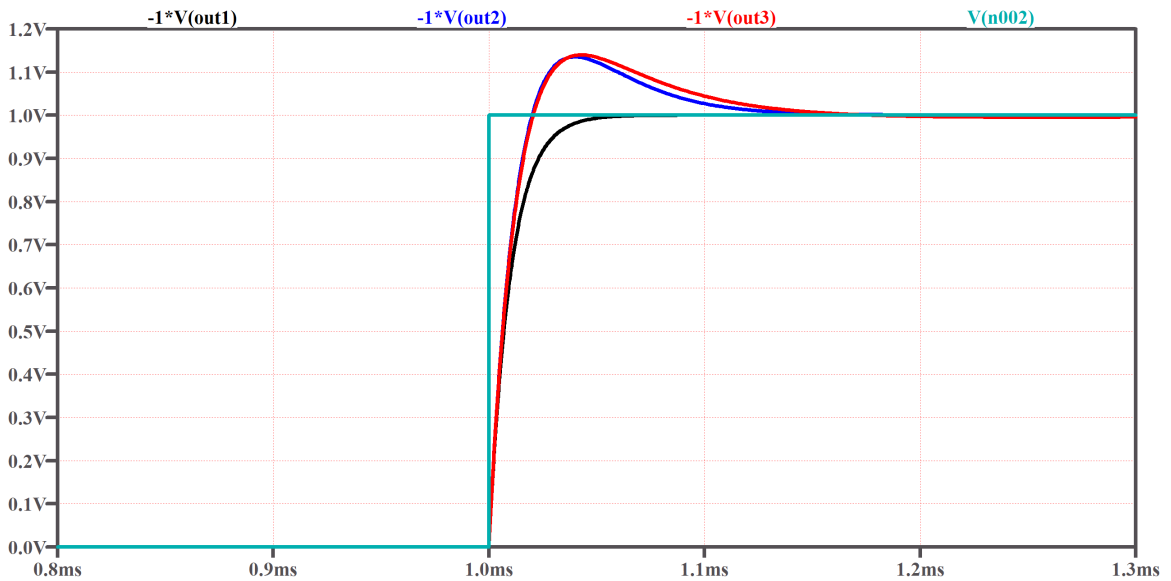
Figure 2.8: 1st, 2nd and 3rd Order Loop Filter Step Responses, in Black, Blue, and Red Respectively

For each loop filter order, the step response shows similar 10-90% rise times, given in Table 2.2. This rise time is inversely related to the bandwidth of each loop. Because each loop's bandwidth is similar, changing filter order does not substantially alter the behavior of the modulator. Therefore, fair comparison between different circuits and of varying order can be made.

Table 2.2: Loop Filter Step Response 10 - 90% Rise Times

Order	Rise Time (μs)
1	22
2	16
3	16

The results of the signal transfer function simulation are given in Figure 2.9. As predicted from the step response rise times, each loop order has a similar bandwidth, of about 16 kHz. Again, this allows each loop order to only affect noise shaping, and not the integrity of the loop allowing for comparison in different loop topologies between different orders.
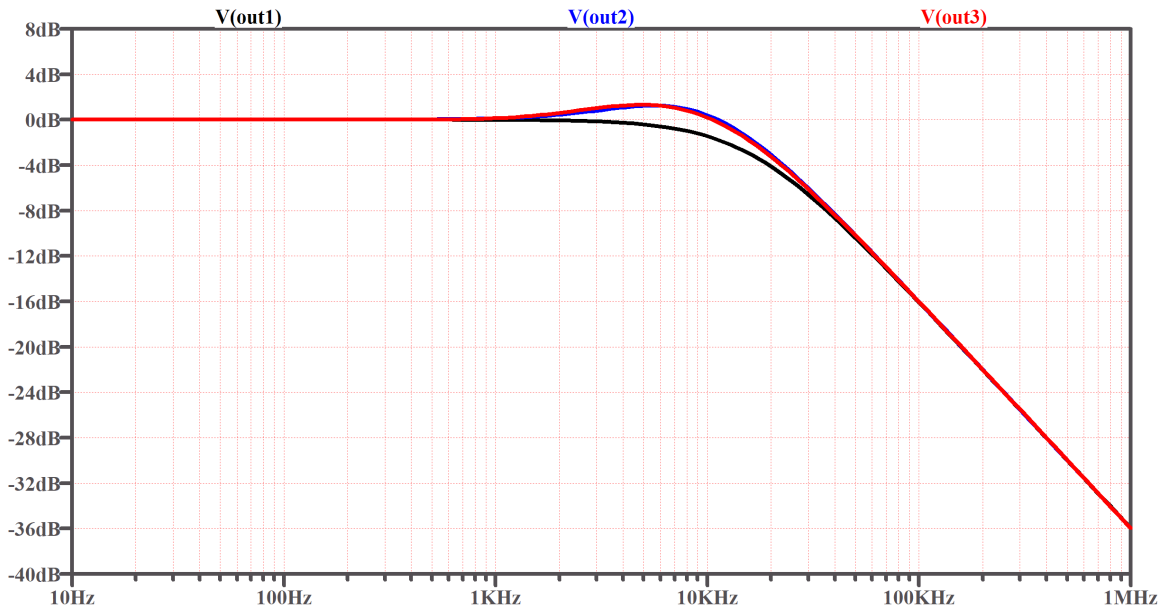
Figure 2.9: 1st, 2nd, and 3rd Order Loop Filter Signal Transfer Function, in Black, Blue, and Red Respectively

The noise shaping characteristics of each circuit in Figure 2.2, 2.3, and 2.4 can be analyzed using a closed feedback loop, with an addition of an AC source, modelling the addition of noise from Figure 1.4. Analyzing the transfer function from the AC source to the feedback path will determine how noise is shaped by the filter.
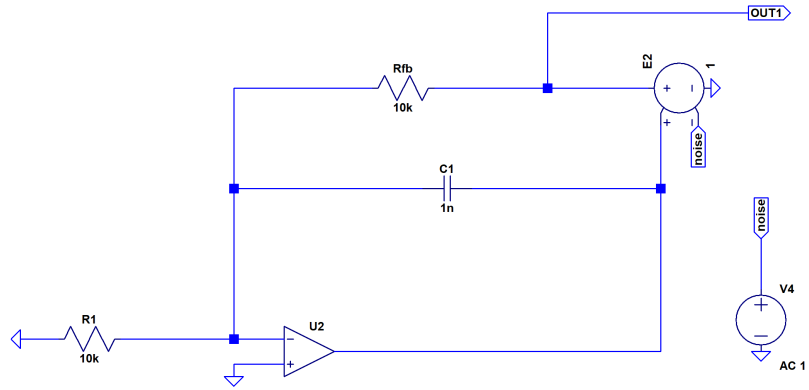
Figure 2.10: 1st Order Noise Shaping LTSpice Schematic
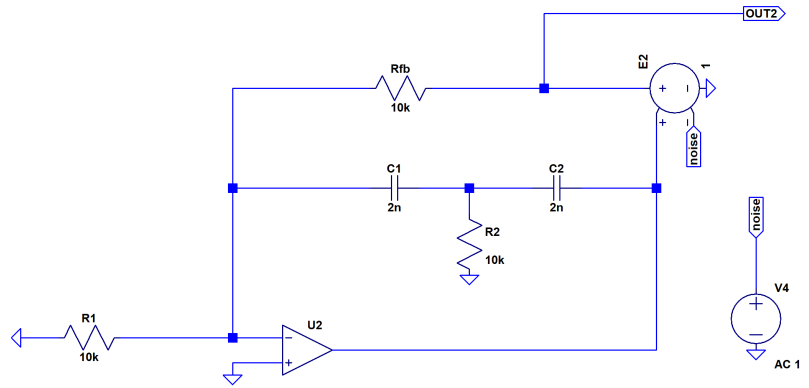
Figure 2.11: 2nd Order Noise Shaping LTSpice Schematic
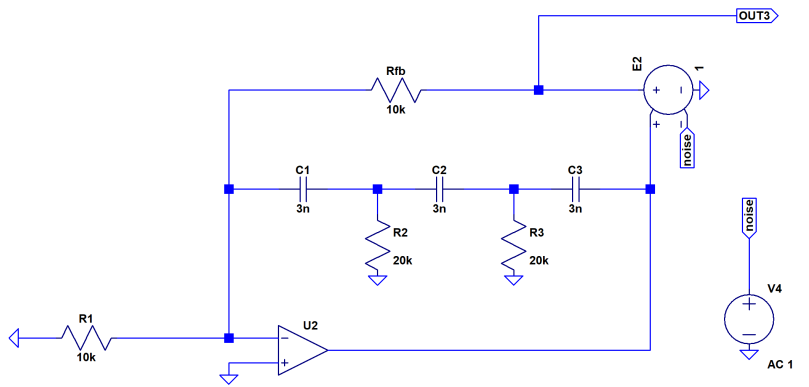
Figure 2.12: 3rd Order Noise Shaping LTSpice Schematic

The results of this simulation for the schematics in Figures 2.10, 2.11, and 2.12 are given in Figure 2.13 and Table 2.3. As expected, increasing the loop filter order in-

creases the high-pass filtering of the noise signal. Note, the op amp in each schematic was modelled with near-infinite gain-bandwidth and slew rate, allowing only the filter network and feedback to affect the noise transfer function. In reality, the gain-bandwidth product of the op-amp would restrict the high-pass roll-off and result in a raised noise floor altering the results in Figure 2.13.
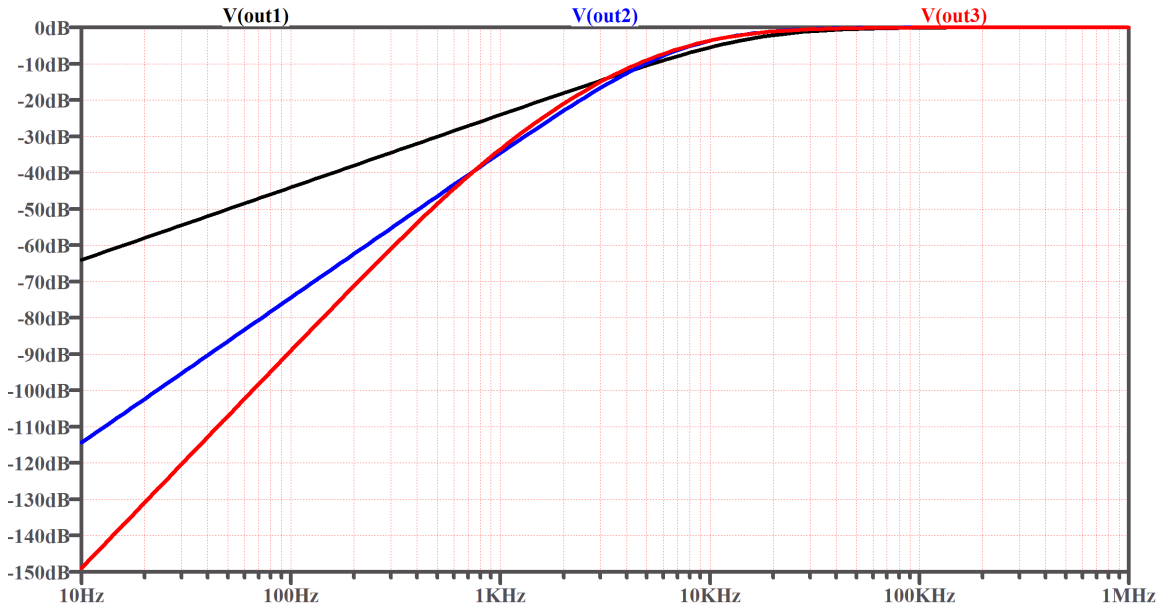
Figure 2.13: 1st, 2nd, and 3rd Order Noise Transfer Function, in Black, Blue, and Red Respectively

Table 2.3: LTSpice Noise Transfer Function Results

Order	-3 dB Bandwidth (kHz)	Roll Off (dB/decade)
1	15.85	20.09
2	11.22	39.83
3	11.22	55.49

2.1.2 Sample-and-Hold and Quantizer

In order to study the introductions of distortion and error due to time discretization and magnitude quantization, the sign function implemented with a dependent behavioral or "b" LTSpice voltage source will be used to quantize the signal's value,

while an ideal sample and hold circuit will be used to discretize the signal's time as shown in Figure 2.14. The output of the sample-and-hold is input in the LTSpice sign function with the behavioral voltage source, to return a quantized value of +/- 1V.
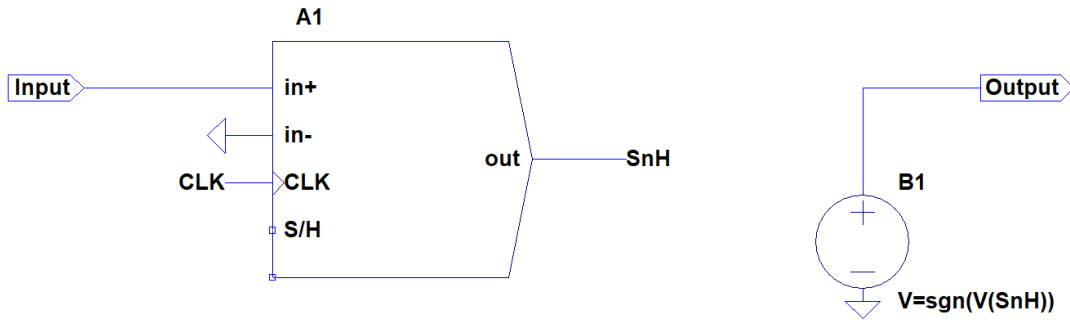
Figure 2.14: Ideal Quantization Circuit Schematic

2.2 Spectral Domain Simulation Methods

To best understand the characteristics of each modulator discussed in this section, LTSpice simulation is used to analyze the modulator outputs in the frequency domain. For these data, an input signal as described in Table 2.4 will be used.

Table 2.4: LTSpice Signal Parameters

Signal	Wave Shape	Amplitude (Vp)	Frequency (kHz)
Two-Tone Input	Sinusoidal	0.4 and 0.4	1.017 and 0.983
Clock	Square	1	300

The Schematics in Sections 2.3 and 2.4 were simulated for 60 ms with a maximum timestep of 0.01 μs and the LTSpice fft used a Blackman-Harris windowing function with 7-point binomial smoothing and a 1 million sample window. Voltage rails were +/- 1V with GND used as reference for the op-amp, which was modeled with infinite Gain-Bandwidth and Slew Rate. The input signal was a two-tone sinusoid as per Table 2.4, selected to reduce harmonic responses that could arise from a single tone,

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and the oversampling ratio of the loop was 150. This oversampling ratio was selected to provide multiple decades of quantization noise for ease of analysis. The frequency of the input signal was selected to fall in the pass-band of the low-pass signal response of the filters from Figure 2.9 and in the reject band of the noise transfer function from Figure 2.13.

2.3   Delta-Sigma and Pulse-Width Modulator Simulation

Two Modulator topologies are simulated and discussed in this section: the discrete time Delta Sigma Modulator (DSM) and the continuous time Pulse-Width Modulator (PWM). For each topology, separate simulations will be done for a first, second, and third order loop filter from Figures 2.2, 2.3, and 2.4.

2.3.1   Delta Sigma Modulator

The Delta Sigma Modulator (DSM) is of the most discussed and implemented modulator topologies in research and production [13]. It quantizes magnitude and discretizes time in a single loop to provide a usable output for a digital filter to accept in Delta Sigma Analog-to-Digital Converters. The LTSpice implementation of this modulator is given in Figures 2.15, 2.16, and 2.17. Each modulator order utilizes an integrator as a loop filter from either Figure 2.2, 2.3, or 2.4 depending on the order of the loop.
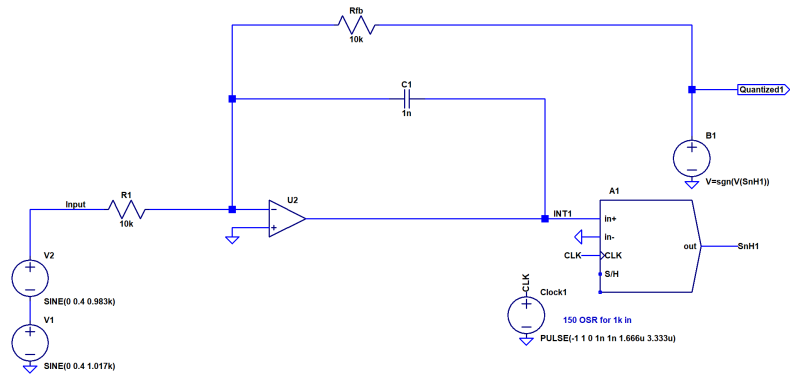
Figure 2.15: 1st Order Delta Sigma Modulator LTSpice Schematic
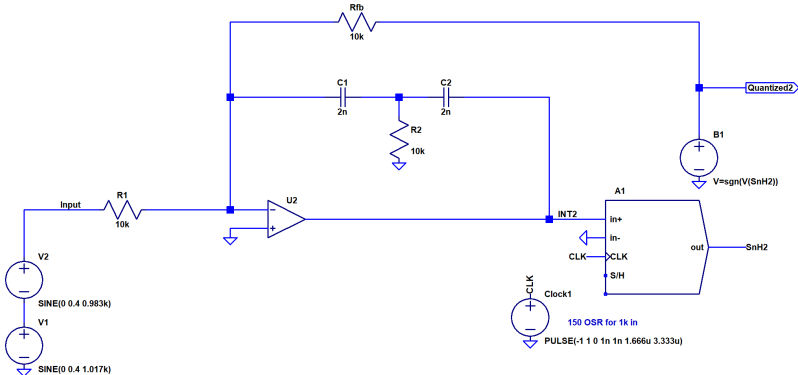
Figure 2.16: 2nd Order Delta Sigma Modulator LTSpice Schematic
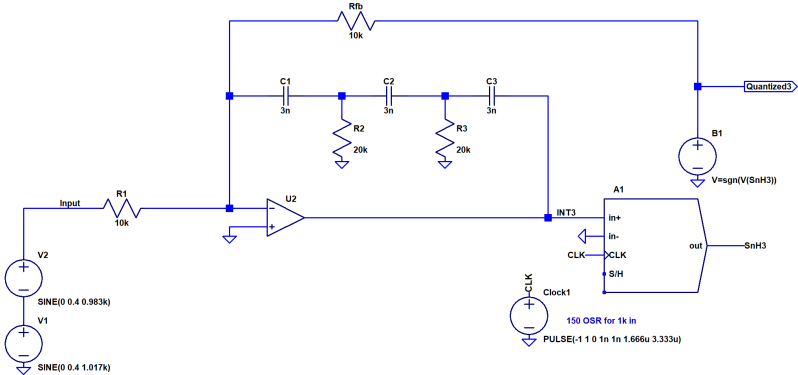
Figure 2.17: 3rd Order Delta Sigma Modulator LTSpice Schematic

The results of the simulation are shown in Figure 2.18. The noise shaping is similar for each order, but the 2nd and 3rd order loops have about 5 dB greater SNR in-

band. In all cases, the input signal is clearly observed at 1kHz and quantization noise is shaped out of band, as expected.
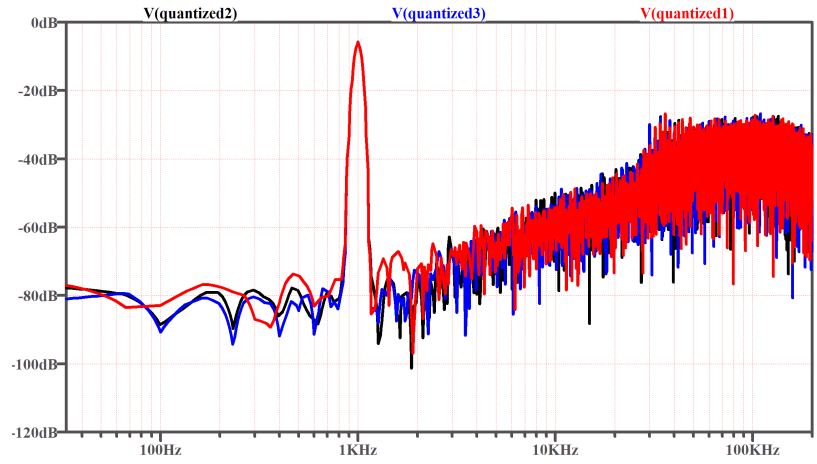
Figure 2.18: Delta Sigma Modulator LTSpice Schematic for 1st, 2nd, and 3rd Order Loop Filter in Red, Black, and Blue Respectively

2.3.2 Pulse-Width Modulator

The Pulse-Width Modulator operates without discretizing the output signal in time. This enables the loop to operate without the requirement of a clock edge. While this doesn't necessarily affect noise shaping, it may lower the overall noise present in the bandwidth of the modulator, as Figures 1.5 and 1.4 would suggest. The LTSpice implementation of this modulator is given in Figures 2.19, 2.20, and 2.21. Note that Rhys1 and Rhys2 with B3 implement a hysteretic comparator.
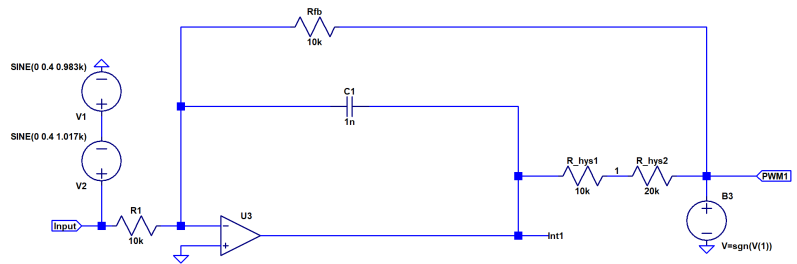
Figure 2.19: 1st Order Pulse Width Modulator LTSpice Schematic

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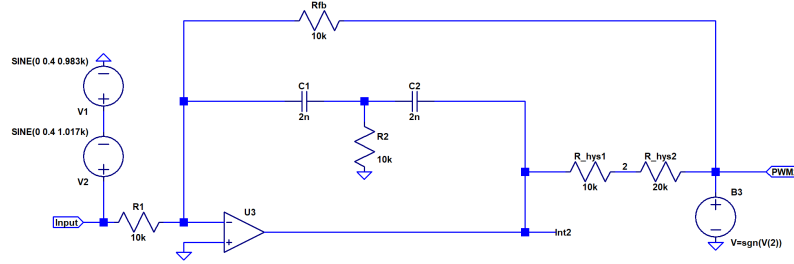
Figure 2.20: 2nd Order Pulse Width Modulator LTSpice Schematic
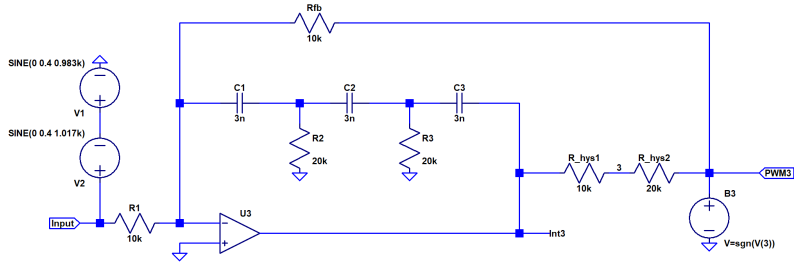
Figure 2.21: 3rd Order Pulse Width Modulator LTSpice Schematic

2.3.2.1 DC Testing

For changing DC input voltages, the circuit encodes the value in a series of binary valued pulses. The frequency of the output for various DC input signals is given in Figure 2.22 and the duty cycle is given in Figure 2.23. The duty cycle should map directly and linearly to the input value, such that the average value of the output matches the average value of the input, as discussed in Section 1.1. This is reflected in the DC results. Additionally, the duty cycle has an inverse relationship with the value of the input signal, reflective of the inverting nature of the loop filters. The frequency of the input also varies with the input signal, as the integrator output depends on both the value of the modulator output as well as the value of the modulator input. DC results agree with this expectation, with modulator frequency ranging from 200kHz to 500kHz from -0.75V to 0.75V input, where the maximum frequency occurs at 0V and minimum frequency at the end points, Lam et al determined the closed form

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expression for the frequency of a modulator of this type in [5]. This response was measured for a first-order loop filter.

$y = -496.54x^2 - 1.1493x + 498.88$
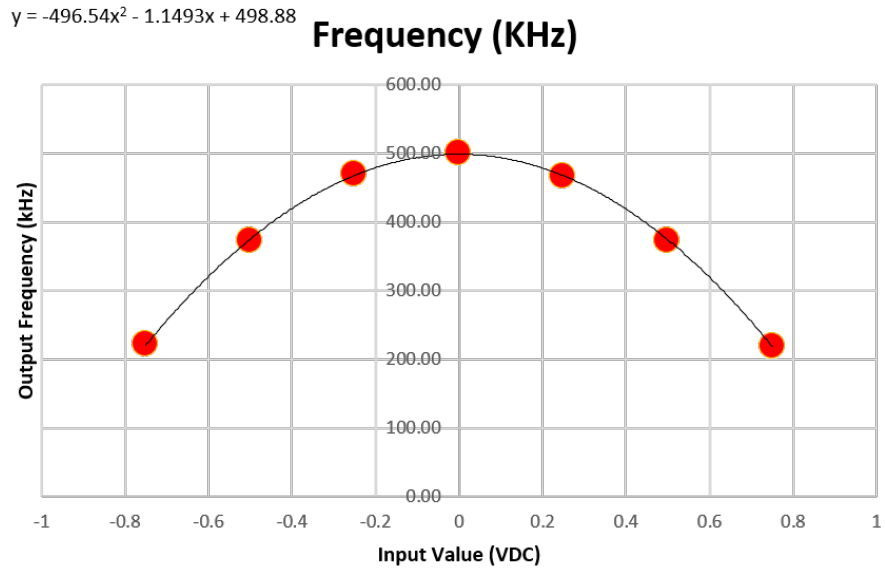
Frequency (KHz)

Figure 2.22: Pulse Width Modulator Output Frequency

$y = -50.2x + 50.006$
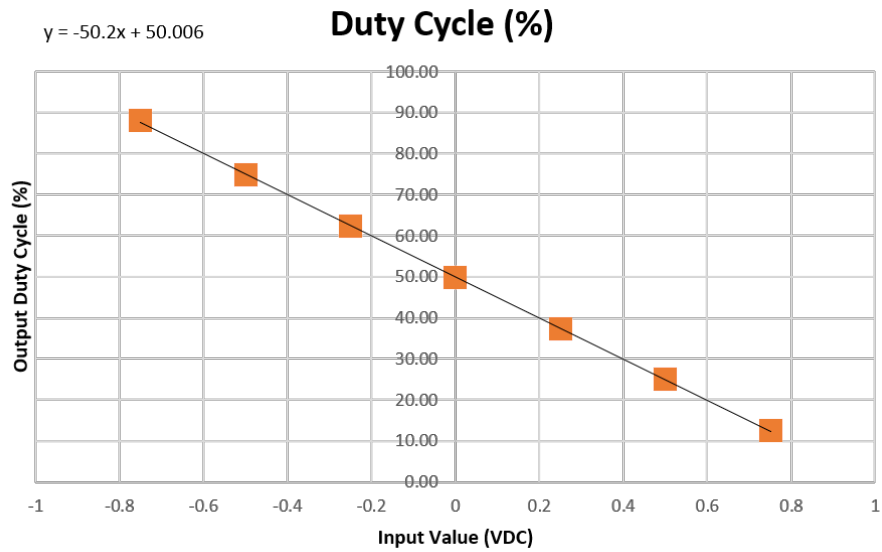
Duty Cycle (%)

Figure 2.23: Pulse Width Modulator Output Duty Cycle

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2.3.2.2   PWM FFT Simulation Results

The FFT results of the LTSpice Schematics in Figures 2.19, 2.20, and 2.21 are given in Figure 2.24. Notice the noise floor of -85 dB and the sharp increase in spectral components above 10kHz, the corner of the noise and signal transfer functions. Each of the three orders shows roughly the same noise shaping and noise floor.
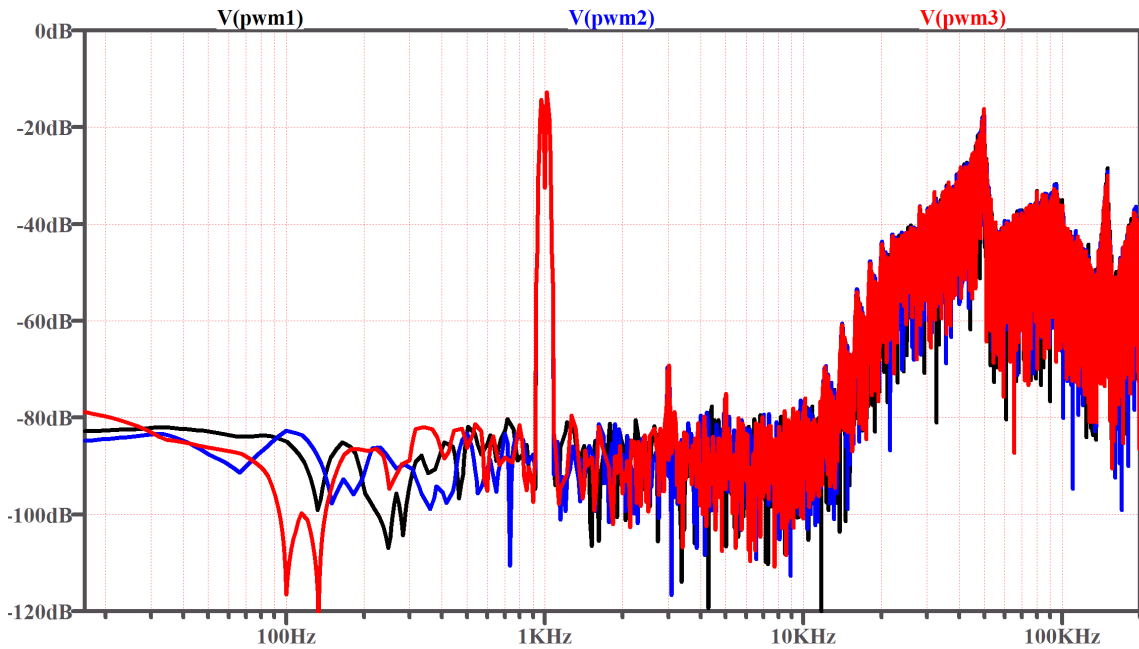
Figure 2.24: Pulse Width Modulator LTSpice Schematic for 1st, 2nd, and 3rd Order Loop Filter in Red, Black, and Blue Respectively

2.3.3   DSM and PWM Simulation Results Comparison

The DSM and PWM output FFT are given in Figure 2.25. The PWM, in red for first-order and teal for second-order, shows favorable quantization noise over the DSM, in blue for first-order and black for second-order. The PWM shows a significantly lower noise floor than the DSM from 1kHz to 15kHz. This decrease in the noise floor is due to the 500 kHz frequency peak from Figure 2.22, resulting in a higher oversampling ratio in the PWM than the discretized DSM.
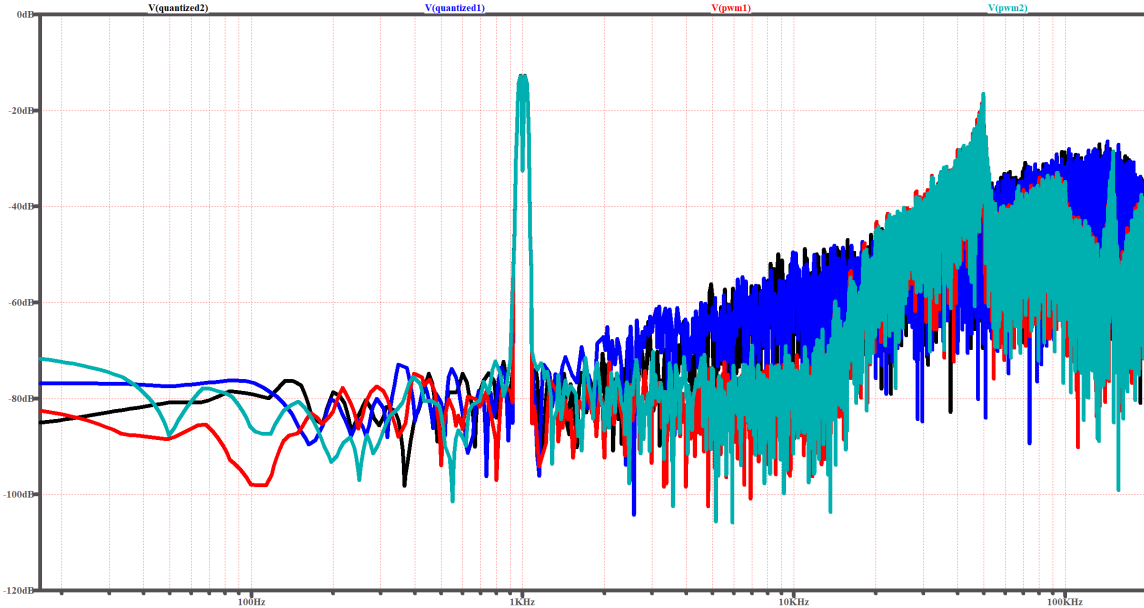
Figure 2.25: PWM and DSM Output FFT Comparison, in Red and Teal, and Blue and Black Respectively

2.4   Out of Loop Discretized Modulator LTSpice Simulation

2.4.1   Out Of Loop Discretized PWM

The Out Of Loop Discretized PWM (OOLDP) aims to preserve the low quantization noise floor of the PWM, while time discretizing the output, as shown in Figure 2.26. The loop filter is adapted between different orders as in Figures 2.19, 2.20, and 2.21 and in each case the output is time discretized with a sample-and-hold with a 300 kHz clock. This clock rate was selected to match with the DSM clock rate, and it fits nicely in the 200 to 500 kHz range that the PWM oscillates in, although some under-sampling and aliasing can occur in this case.
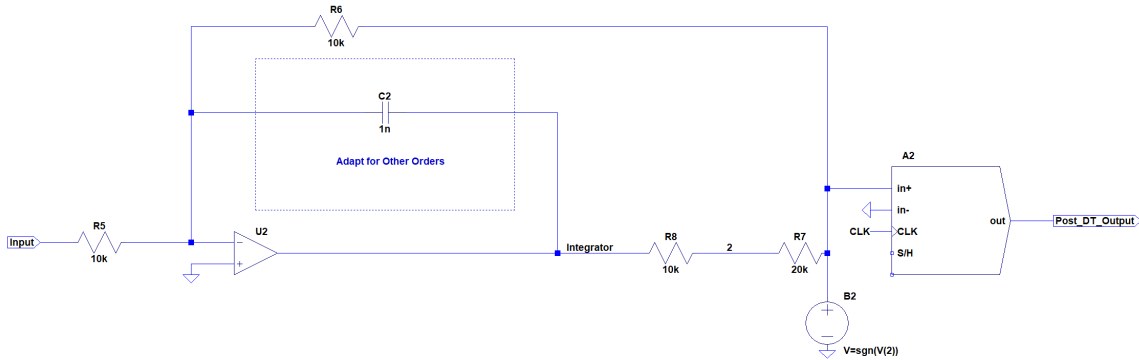
Figure 2.26: OOLDP LTSpice Schematic

2.4.2 Cascaded Delta Sigma Modulator

As in the OOLDP, the cascaded modulator aims to keep the advantageous low quantization noise of the PWM, while time discretizing the output. Unlike the OOLDP, the Cascaded DSM noise shapes the added sampling noise in a separate loop. The First stage of the cascade is the PWM from Figures 2.19, 2.20, and 2.21. The second loop is the DSM from Figures 2.15, 2.16, and 2.17 used as a noise shaping time discretizer. The output of the PWM is a bilevel signal with transitions occur at any time. The DSM forces the edge to align with the clock and noise shapes any errors that result from the alignment. Lam et al. showed a similar cascade in their IEEE paper on a Class D Audio Amplifier [5]. In their application, the added loop decreased the inter-modulation distortion of the output, and increased the power supply rejection ratio. Perhaps the loop could be utilized in other applications, such as in Delta Sigma Analog-to-Digital Converters, and outperform an OOLDP in in-band quantization noise. Lam's implementation involved a cascade of first and second-order loops, nearly identical to a PWM to DSM cascade. The LTSpice implementation of this circuit is given in Figure 2.27.

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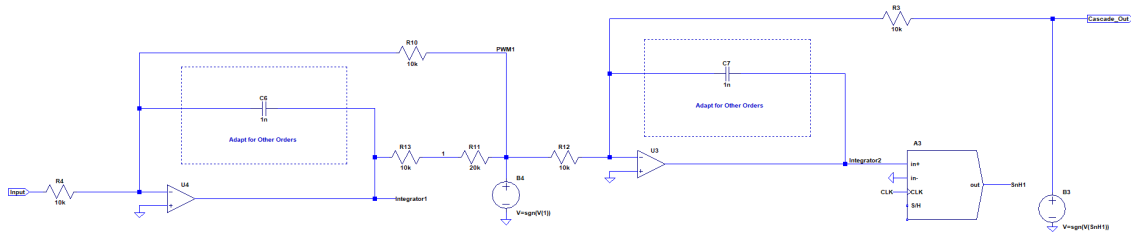
Figure 2.27: Cascaded Time Delta Sigma Modulator LTSpice Schematic

2.4.2.1 Cascaded DSM Simulation Results and Comparison

The cascaded DSM and OOLDP output FFTs are shown in Figure 2.28. The cascaded DSM output, in black and red for first and second-order respectively, show a sloped, but 20-30dB lower noise floor compared to the OOLDP output, in blue and teal for first and second-order respectively. The lowered noise floor of the cascaded DSM point to its advantageous noise shaping over the OOLDP.
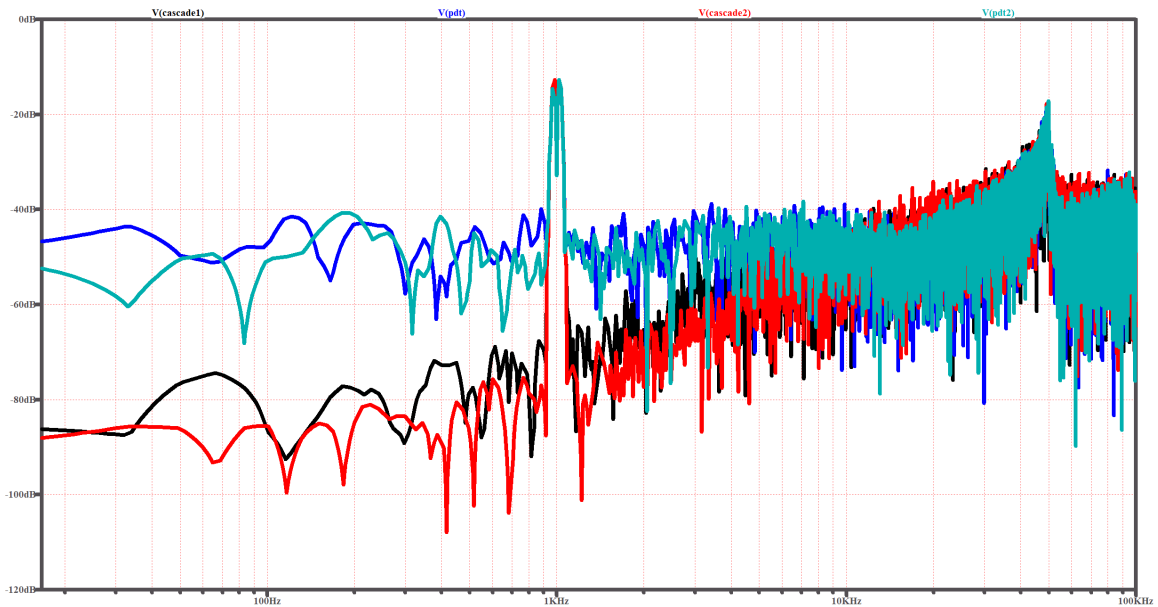
Figure 2.28: Cascaded and OOLDP Output FFT Comparison, in Black and Red, and Blue and Teal Respectively

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2.4.3 Spectral Domain Results Summary

Overall, for a two-tone 80% of full scale sinusoid with an oversampling ratio of 150, the PWM, cascaded DSM, and DSM show similar results as the best for lowering quantization noise with around -85 dBV and a noise shaping slope of 20 dB/decade in most cases, whereas the OOLDP shows the highest noise floor of about -50 dBV.

2.5 DC Input Transient Simulations

By Equation 1.1, the average value of the input and output of each modulator should approach equality for long enough averaging windows. To verify the functionality of the modulators in simulation, the output is averaged over a 0.92 ms window for a DC input voltage and a 300 kHz clock using the .meas op command in LTSpice. Values from -1 to +1 V were used for inputs with increments of 0.1 V. The transient simulation is performed for 1ms in every case, where data is captured after the first 0.08 ms. The results of these simulations is shown in Figures 2.29, 2.30, 2.31, 2.32. In every case except OOLDP, the maximum deviation from linearity is less than 15 mV for the entire input range. In the OOLDP however, the maximum deviation is 40 mV, over twice the deviation of all other modulator topologies. These results align with those earlier in this chapter, where the noise shaping and producing qualities of the OOLDP prove to be outperformed by the cascaded circuit.

Figure 2.29: Input DC Value and Output Average Value for 1st, 2nd, and 3rd Order DSM with Blue, Orange, and Red Markers Respectively
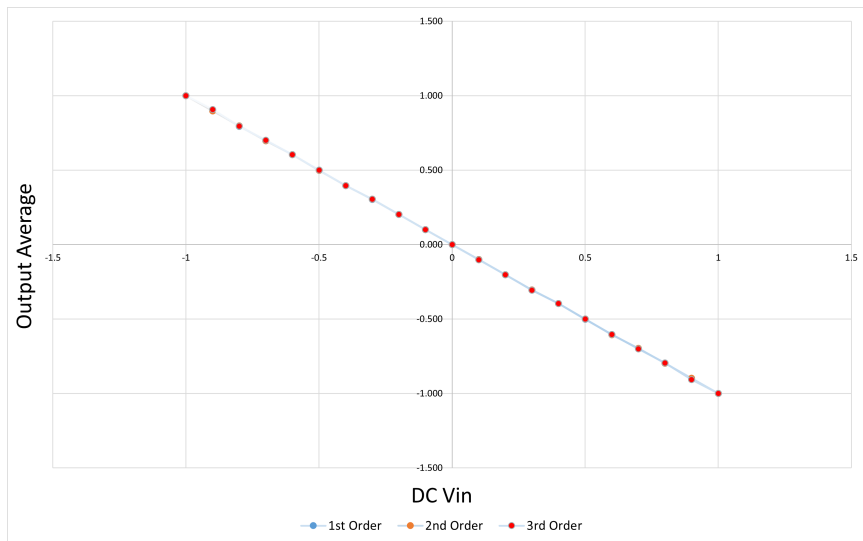
Figure 2.30: Input DC Value and Output Average Value for 1st, 2nd, and 3rd Order PWM with Blue, Orange, and Red Markers Respectively
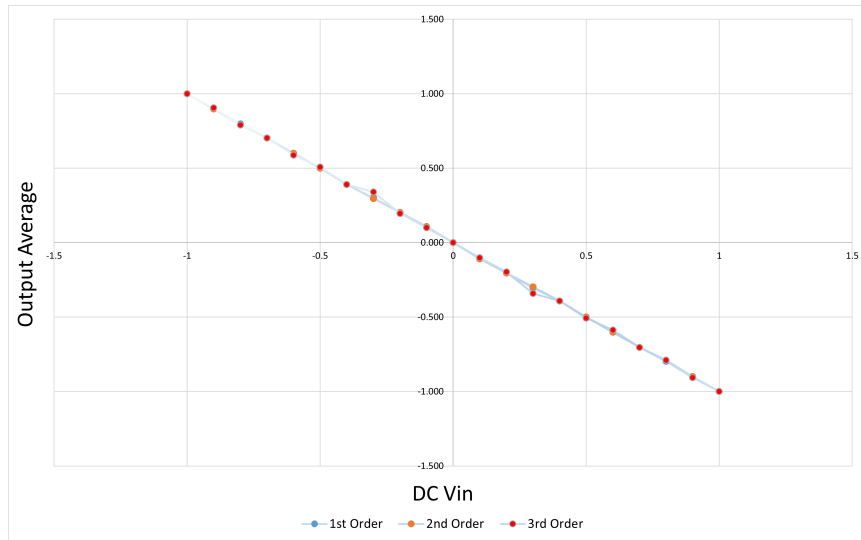
Figure 2.31: Input DC Value and Output Average Value for 1st, 2nd, and 3rd Order OOLDP with Blue, Orange, and Red Markers Respectively

In the average value linearity plot in Figure 2.32, the input and output values are positively correlated. This is expected due to the inverting nature of each of the two modulators in the cascade.
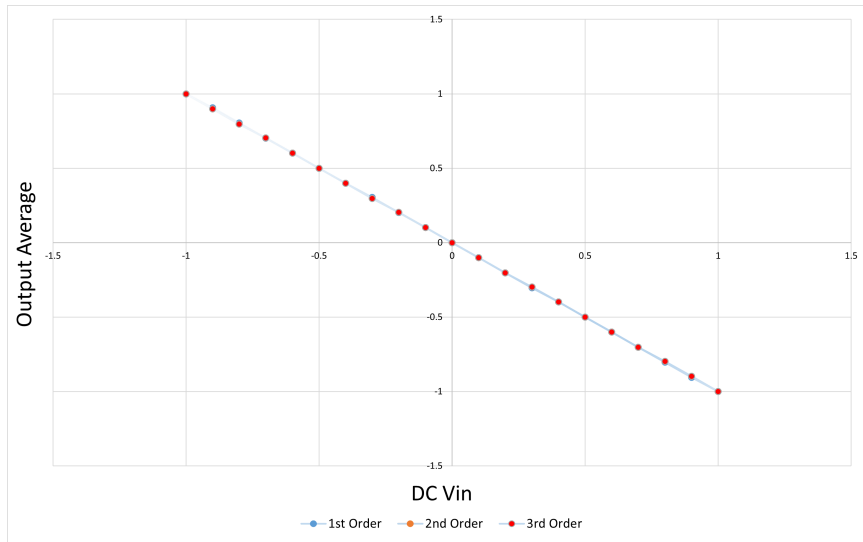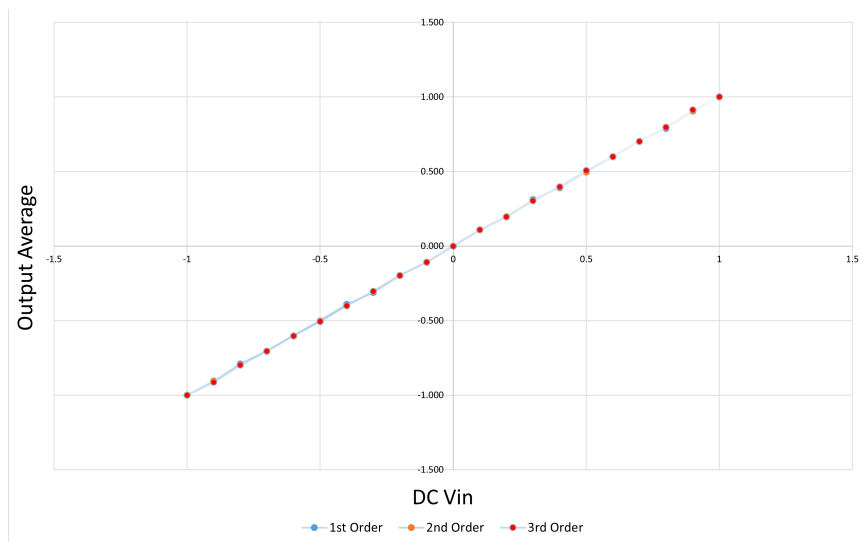

Figure 2.32: Input DC Value and Output Average Value for 1st, 2nd, and 3rd Order Cascade with Blue, Orange, and Red Markers Respectively

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Chapter 3

PHYSICAL IMPLEMENTATION

Altium Designer was used to design the Modulators discussed in this paper. Printed Circuit Board development was decided due to favorable low parasitics compared to breadboard and protoboard options. This is especially important in a mixed-signal board such as this, where a 300kHz clock is used.

3.1 Component Selection

The active components of the design were selected for their power capability, bandwidth, and delay.

3.1.1 Operational Amplifier

For each modulator, a single op-amp from the OPA4820ID IC is used. The parameters of the circuit are summarized in Table 3.1. The Gain-Bandwidth product and Slew Rate were tested in LTSpice and proved to not restrict the results of the loop. The voltage capability is well within the target of +/- 2.5V, making this device suitable for use on the Modulator PCB.

Table 3.1: OPA4820ID op-amp Parameters

Parameter	Value
Max Voltage	+/- 6.3 V
GBW	250 MHz
Slew Rate	240 V/μs

3.1.2 D Flip-Flop

The time discretizer of both the DSM and OOLDP is the SN74LVC2G74DCUR D Flip-Flop. The parameters of the Flip Flop are summarized in Table 3.2. The voltage rating of this device doesn't quote dual supply values, but for a single supply differential of 5.5V, a +/- 2.5V supply is within the IC's capabilities. The max clock frequency and propagation delay are insignificant when operating on a 300 kHz clock, and the output current capability is more than enough to drive the feedback of the loop.

Table 3.2: SN74LVC2G74 Parameters

Parameter	Value
Max Voltage	5.5 V
Max Clock Frequency	200 MHz
Propagation Delay	4.4 ns
Output Current	32 mA

3.1.3 Comparator

The comparator of both the DSM and OOLDP circuits is the LT1711. The parameters of the LT1711 are given in Table 3.3. The voltage capability is within specification at +/- 6V, the device has high gain, and the propagation delay is in the single digit nanosecond scale. The device follows all requirements of the Modulator PCB.

Table 3.3: LT1711 Parameters

Parameter	Value
Max Voltage	+/-6 V
Small Signal Gain	15 V/mV
Max Propagation Delay	8.5 ns

3.2   Schematic

The Altium schematic was adapted from LTSpice simulation schematics in 2.3. The printed circuit board contains two major loops, as seen in Appendix A. One loop follows the OOLDP structure as in Figure 2.26, where the output of a PWM is time discretized by a Flip Flop. The other loop on the printed circuit board is a DSM as in Figures 2.15, 2.16, and 2.17. With these two loops, and access to intermediate nodes within the loops, a DSM, PWM, OOLDP, and Cascaded Delta-Sigma Modulator can be tested. Additionally, the loop filter in each loop contains a jumpered capacitive feedback section. Jumpers 1-12 in Appendix A can be adapted for 1st, 2nd, or 3rd order filtering.

3.3   Layout

Layout was performed using Altium Designer and board milling was done with the help of Simon Schoennauer and Scientific Drilling. The final layout of the board is shown in Appendix B. Figure 3.4 is a picture of the populated board.
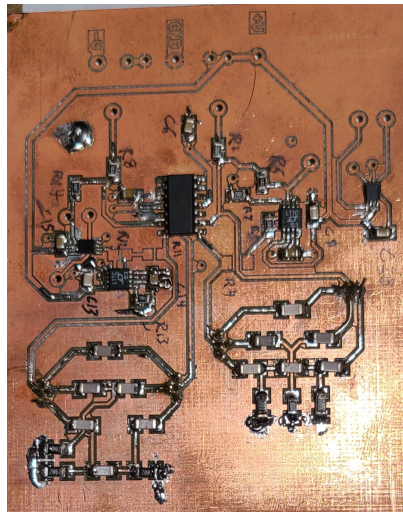
Figure 3.1: Populated Modulator Printed Circuit Board

3.4 Testing

An Agilent E3631A Dual Power Supply, a Tektronix AFG3022B Function Generator, and a Rigol DS1054 Oscilloscope were used to test the DS Mod Board. The parameters of each input device are given in Table 3.4.

Table 3.4: Test Equipment Settings

Device	Channel	Signal Type	Voltage	Frequency (kHz)
Function Generator	C1	Square Wave	5 Vpp	300
	C2	Sine Wave	3.5 Vpp	1
Power Supply	V+	DC	2.5	-
	V-	DC	-2.5	-

To test the DSM, OOLDP, and PWM Modulators, each loop could be run independently, but share a clock and input signal. This configuration is shown in Figure 3.2.
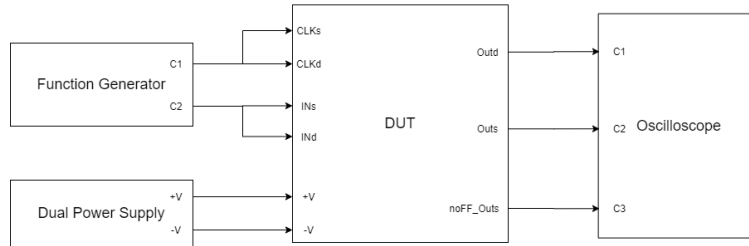
Figure 3.2: Testing Configuration for Non-Cascaded Modulators

To test the Cascaded Delta Sigma Modulator, the output of the PWM is routed to the input of the DSM, as shown in Figure 3.3.
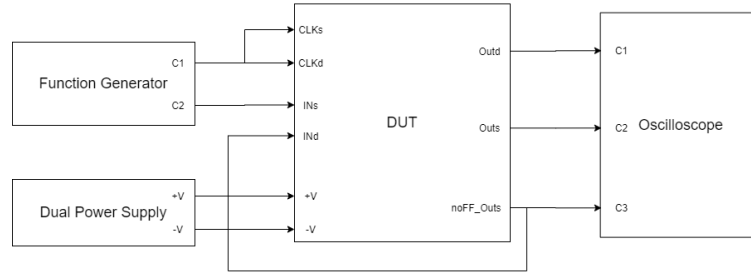
Figure 3.3: Testing Configuration for Cascaded Modulator
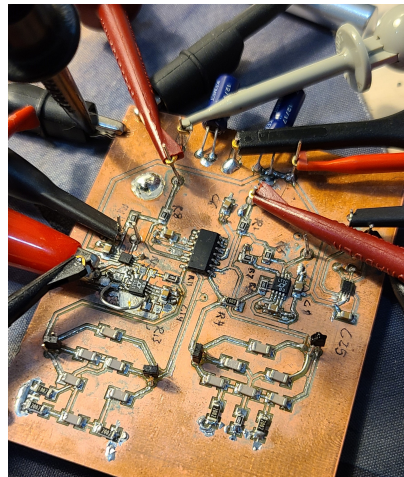
Figure 3.4: Modulator PCB During Testing

For all tests an oversampling ratio of 150 and an input signal of 70% of full scale sine wave was used.

For all Time Domain Measurements in Section 3.5, the Digilent Analog Discovery 2 module was used to measure values and generate input DC values, with a Rigol DP832 Power Supply to provide power rails.

3.5   Time Domain Measurements

Two primary measurements were made in the time domain: the DC input modulator frequencies and the input and output average linearity, as discussed in Section 2.5.

Additionally, to show the behavior of the DSM and PWM, time domain plots from the Analog Discovery 2 are shown.

Figure 3.11 below shows the output waveform for a 0 VDC input to the PWM circuit. The output waveform shows a duty cycle of 50.16%, in line with what is expected from Figure 2.23. The frequency of the waveform, however, is lower than expected, peaking at about 49 kHz. The discrepancy between simulation and measured frequency is one order of magnitude, and is likely attributed to an error in capacitor values used in the implementation.
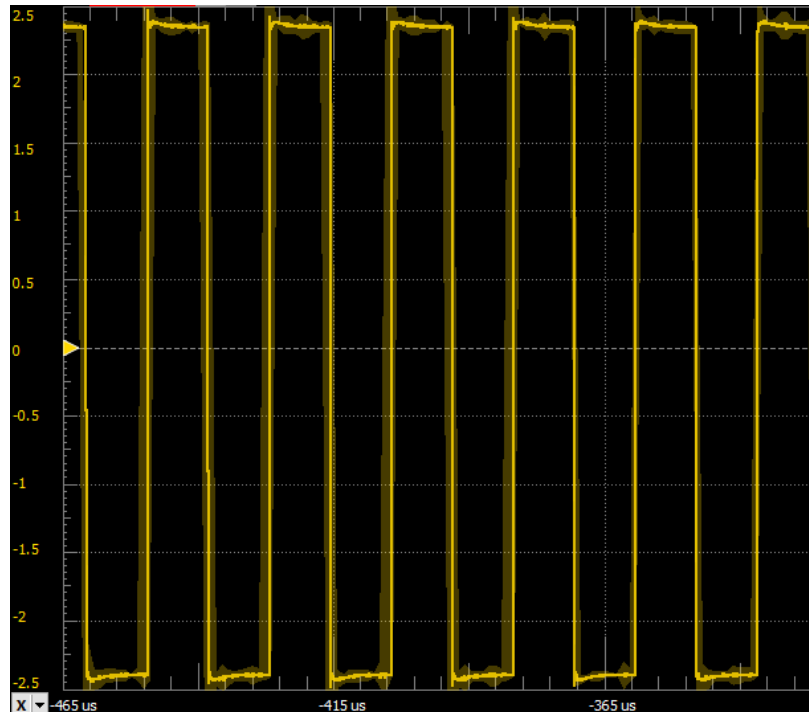
Figure 3.5: PWM Output for 0 VDC Input

For a -1.4 VDC input, the waveform in Figure 3.6 is measured. Note how the output remains high longer than it is low. This is expected as the loop maintains the equal average value of input and output. The same concept, but inverse is true given a +1.4 VDC input in Figure 3.7.
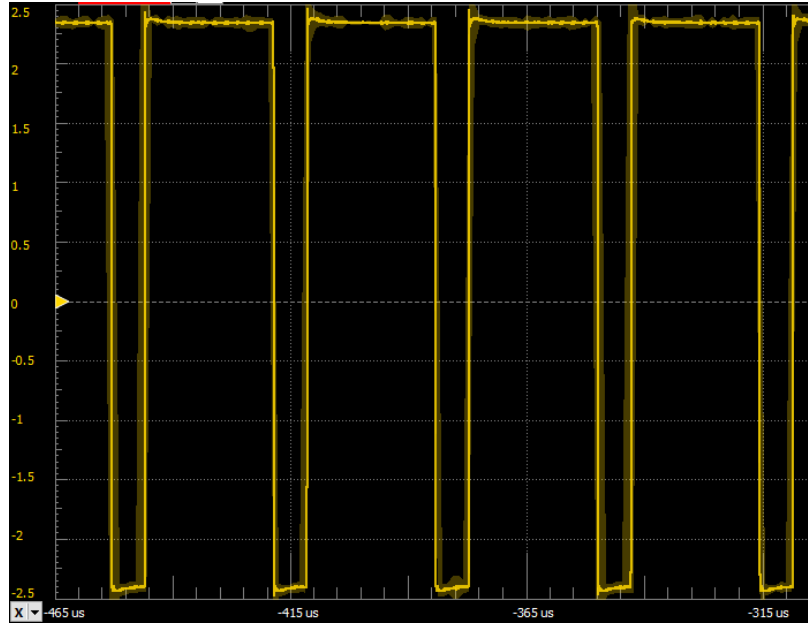
Figure 3.6: PWM Output for -1.4 VDC Input
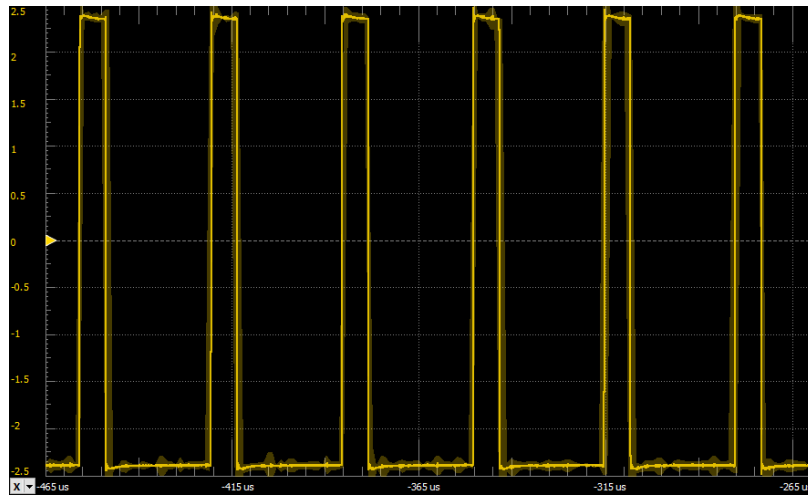
Figure 3.7: PWM Output for 1.4 VDC Input

For the DSM, unfortunately an IO offset of about 0.38 V was measured for each IO average pair. This is evident in Figures 3.8 and 3.9, where the output duty cycle is observably incorrect for the given input DC values of -0.4 and 1.2 VDC respectively. However, the offset error is not significant enough to disqualify any other results, such

as in the cascaded modulator, where only rail to rail inputs will be provided to the DSM, effectively drowning the offset error.
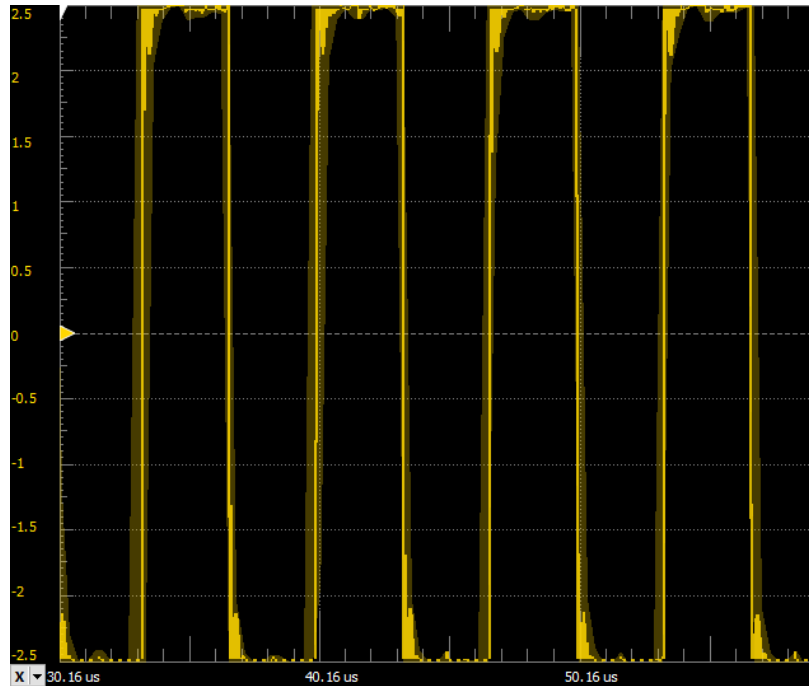
Figure 3.8: DSM Output for -0.4 VDC Input
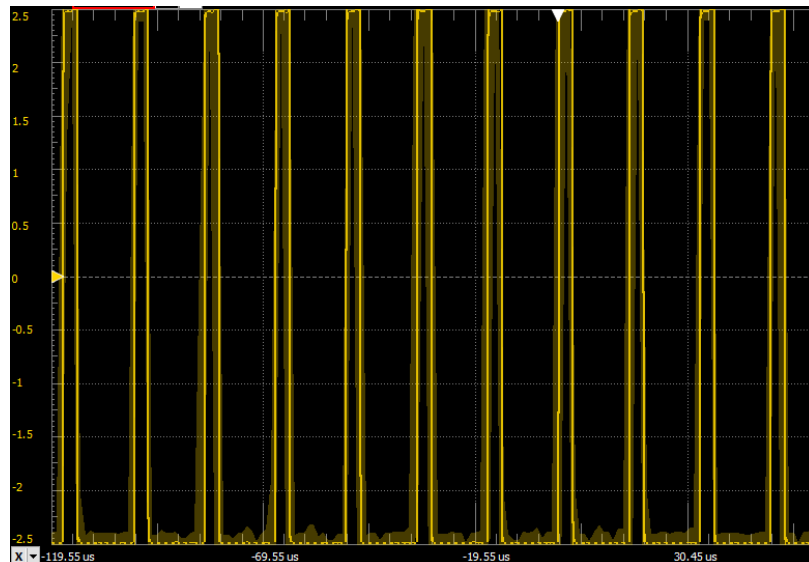
Figure 3.9: DSM Output for 1.2 VDC Input

3.5.1 DC Input PWM and DSM Frequencies

The frequency of the PWM and DSM arise from different circuit parameters.

For a DSM, in the case of a loop quantizer with no hysteresis, the loop frequency is set by the loop filter bandwidth and the time discretizer clock frequency. For the implementation of this thesis, the DSM frequencies were measured for DC input voltages from -2.2 to 1.8 V in increments of 0.5 V and a clock frequency of 300 kHz. The results of this simulation are given in Figure 3.10. As expected from Figures 3.8 and 3.9, we see the offset error in this graph as well, where the peak frequency occurs at about -0.6 VDC. One unexpected result of these measurements is the linearity of the graph, forming a less quadratic response compared to the PWM. The reasoning for this could be researched further in future experimentation.
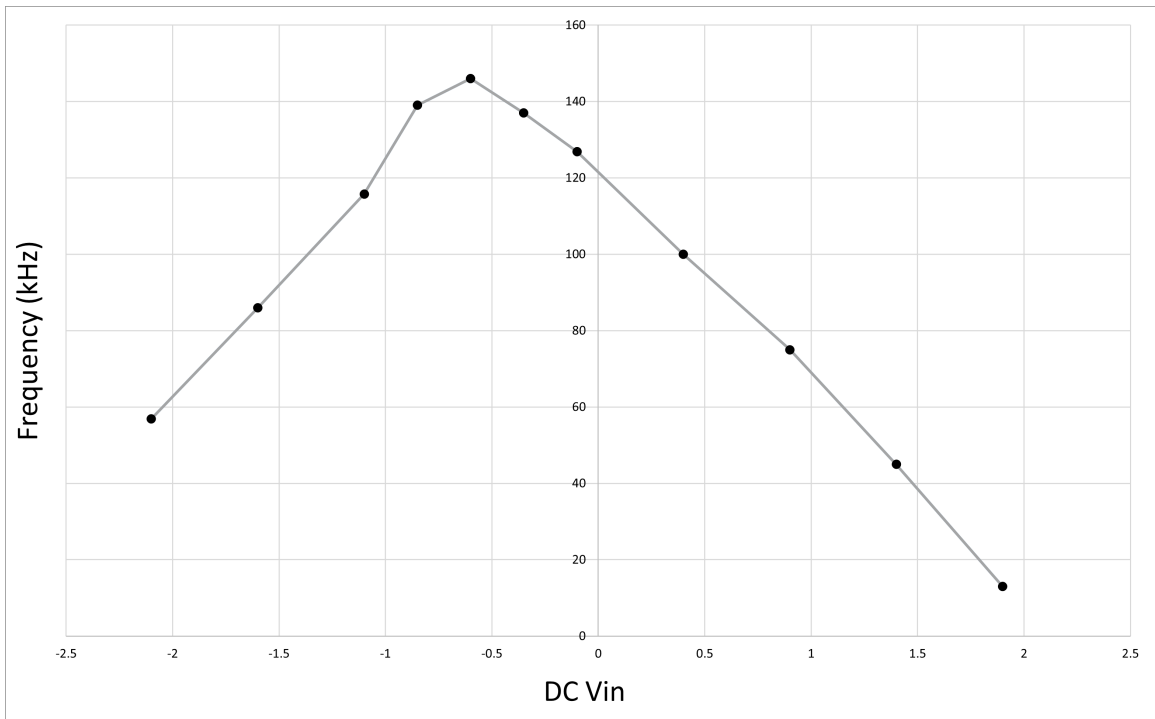
Figure 3.10: DSM Approximate Loop Frequency for A Range of DC Inputs

For a PWM, the output frequency is set by loop parameters, and the input signal value. Figure 3.11 gives the loop filter error accumulation signal over time for a second-order loop filter. The hysteresis window, set by the feedback and input resistor of the comparator, is set to $+/-$ half supply, as expected. We see a more gradual rising slope and a more significant falling slope, in line with the 1.4 VDC input signal, consistently flowing current onto the loop filter capacitors.
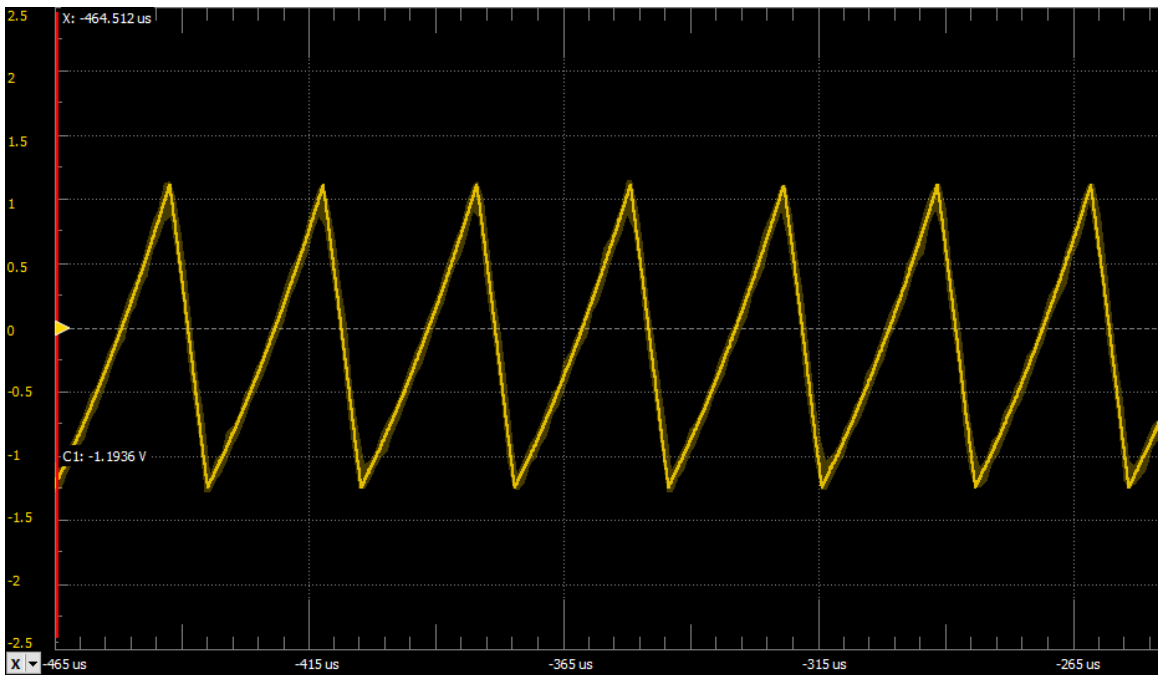
Figure 3.11: PWM Loop Filter Output for 1.4 VDC Input

Figure 3.12 gives the loop frequency of the PWM for input VDC values from -2.5 to $+2.5$ in increments of 0.5. While the peak value is not what was expected, due to variations in loop filter bandwidth, and active component behaviors, the quadratic shape of the graph matches that in Figure 2.22. The charge-discharge cycle of the loop filter sets a quadratic response as discussed in [5].
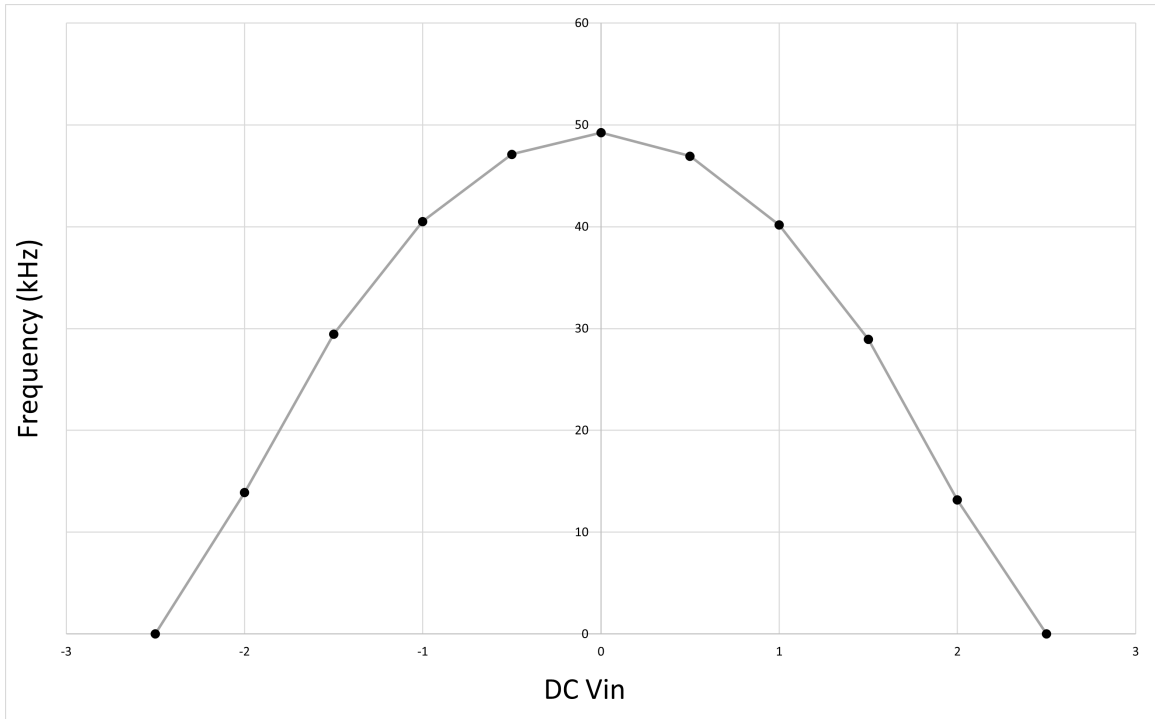
Figure 3.12: PWM Approximate Loop Frequency for A Range of DC Inputs

Figure 3.12 frequencies are an order of magnitude lower than those in Figure 2.22 due to an implementation error where capacitor values used were an order of magnitude greater than those used in simulation.

3.5.2 Input and Output Average Linearity

As in Section 2.5, the output and input averages should be equal for long enough averaging windows. To verify the functionality and noise shaping qualities of the modulators on the printed circuit board, measurements similar to those done in Section 2.5 are performed.

In Figure 3.13, the DSM from the printed circuit board implementation is tested with DC inputs from -2.4 to +2.4 VDC in 0.2 V increments. The first-order loop filter is

given in blue and the second-order in orange. The ideal linearity is shown in black. As expected from Figures 3.8, 3.9, and 3.10, the input and output are offset by about 0.38 Volts in the second-order case and 0.5 Volts in the first-order case. If adjusted for these offsets, the maximum linear deviation from -1.8 to 1.8 Volts is 0.15 Volts. Operating in this range, the output average will have a consistent offset from the input, and operating in this region should result in predictable noise shaping and output characteristics.

Figure 3.13: DSM Input and Output Average Linearity of 1st Order, 2nd Order, and Ideal Case in Blue, Orange, and Black Respectively

Figure 3.14 shows input and output average linearity of the PWM on the printed circuit board, tested for DC inputs from -2.4 to +2.4 VDC in 0.2 volt increments. The first-order loop filter is given in blue and the second-order in orange. The ideal linearity is shown in black. No offset error is graphically observed in this case, and the maximum deviation from the ideal case is 66 mV in the first-order case at 0.8

VDC in for the first-order loop filter in the range of -1.8 to +1.8 VDC input. This shows good performance of the PWM circuit on the printed circuit board.

Figure 3.14: PWM Input and Output Average Linearity of 1st Order, 2nd Order, and Ideal Case in Blue, Orange, and Black Respectively

Figure 3.15 gives the input and output linearity of the OOLDP on the printed circuit board. As in previous figures, the DC input is tested from -2.4 to +2.4 VDC in 0.2 volt increments. The first-order loop filter is given in blue and the second-order in orange. The ideal linearity is shown in black. While no offset error is observable, there is a gain issue in that the output average leans higher for negative inputs and lower for positive inputs. Nevertheless, in the range of -1.8 to +1.8 VDC input, the maximum deviation from ideal is 0.16 volts at an input of +1.6 VDC. The OOLDP shows expected input average tracking and should produce expected noise shaping.
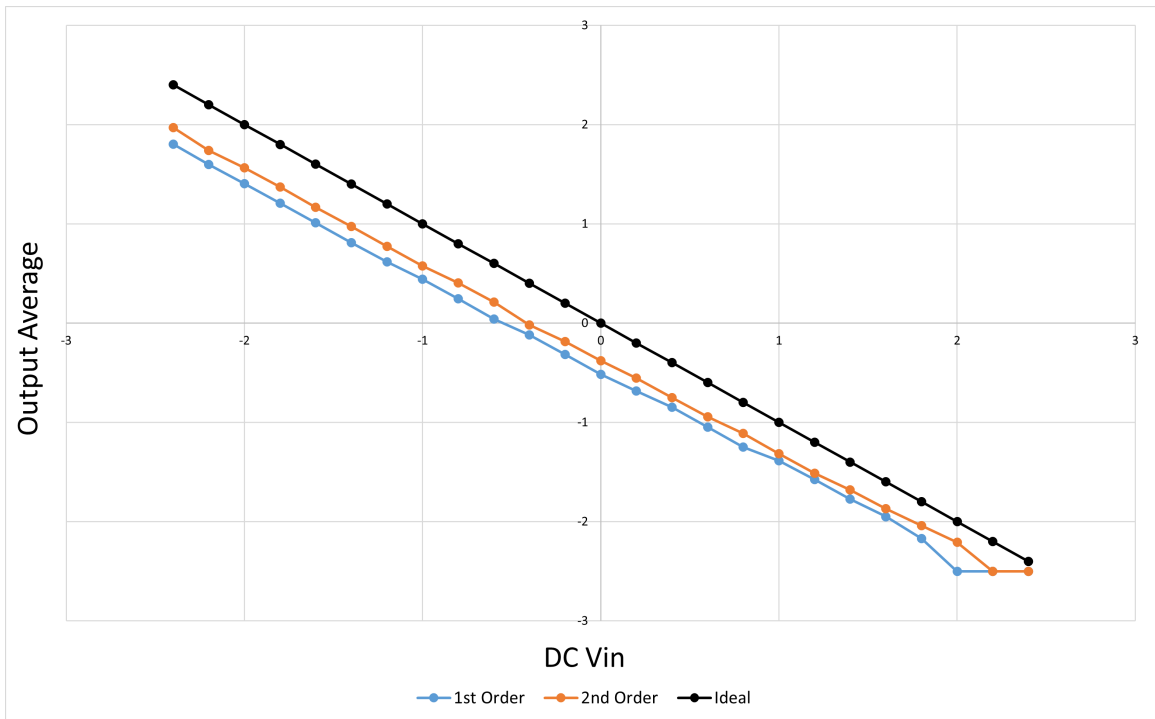
Figure 3.15: OOLDP Input and Output Average Linearity of 1st Order, 2nd Order, and Ideal Case in Blue, Orange, and Black Respectively

For the cascaded modulator, the output and input are positively correlated, as expected from Figure 2.32 due to two inverting stages in series. Figure 3.16 shows the input and output average linearity for input VDC values from -2.4 to +2.4 in increments of 0.2 volts. As expected, some offset error is evident in the second-order case, but surprisingly a gain error exists for both the first and second order cases. This likely arises from time discretization, as shown in the OOLDP in Figure 3.15. Given this error, the maximum deviation in the input range of -1.8 to +1.8 VDC is 0.502 volts, occuring at -1.6 volts in the first-order case. While this error is significant, it shouldn't obstruct the operating behavior or noise shaping qualities of the cascaded modulator, as long as the input voltage remains in the specified -1.8 to +1.8 VDC range.
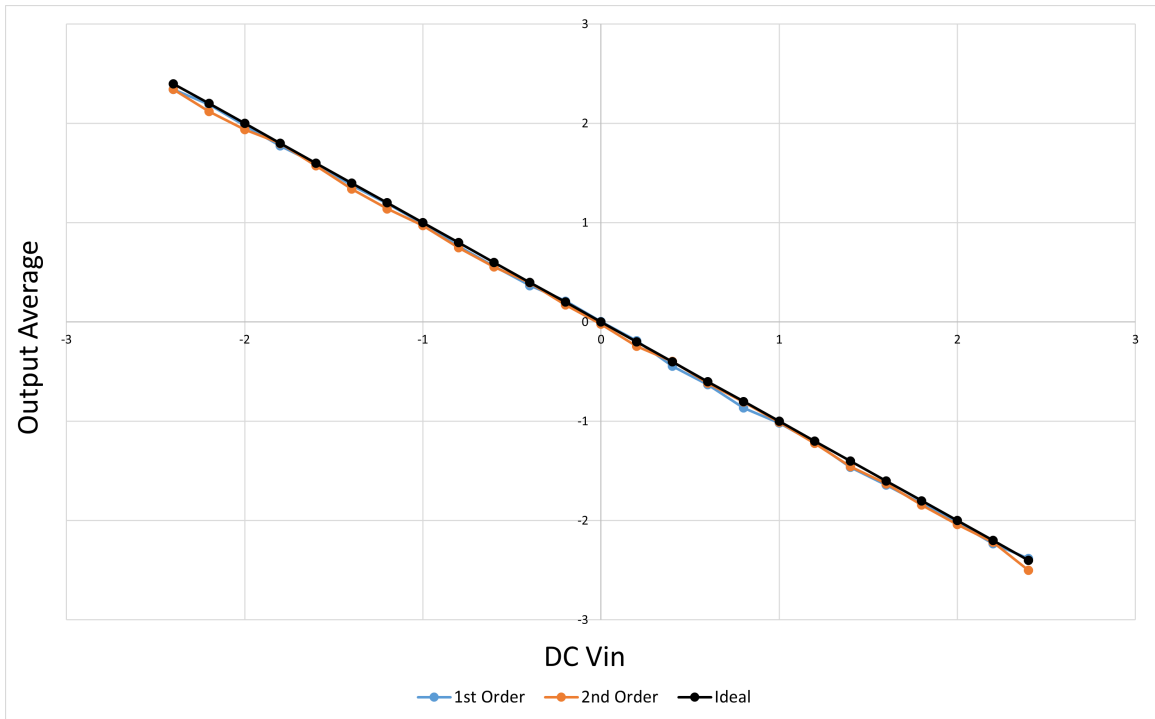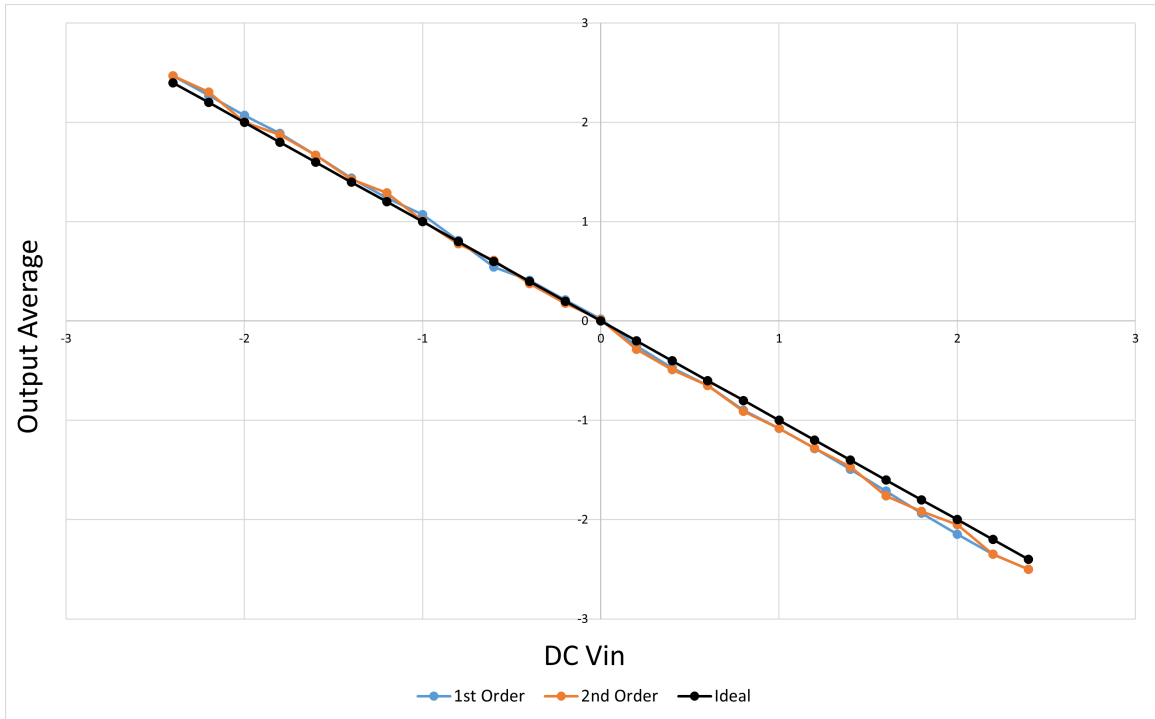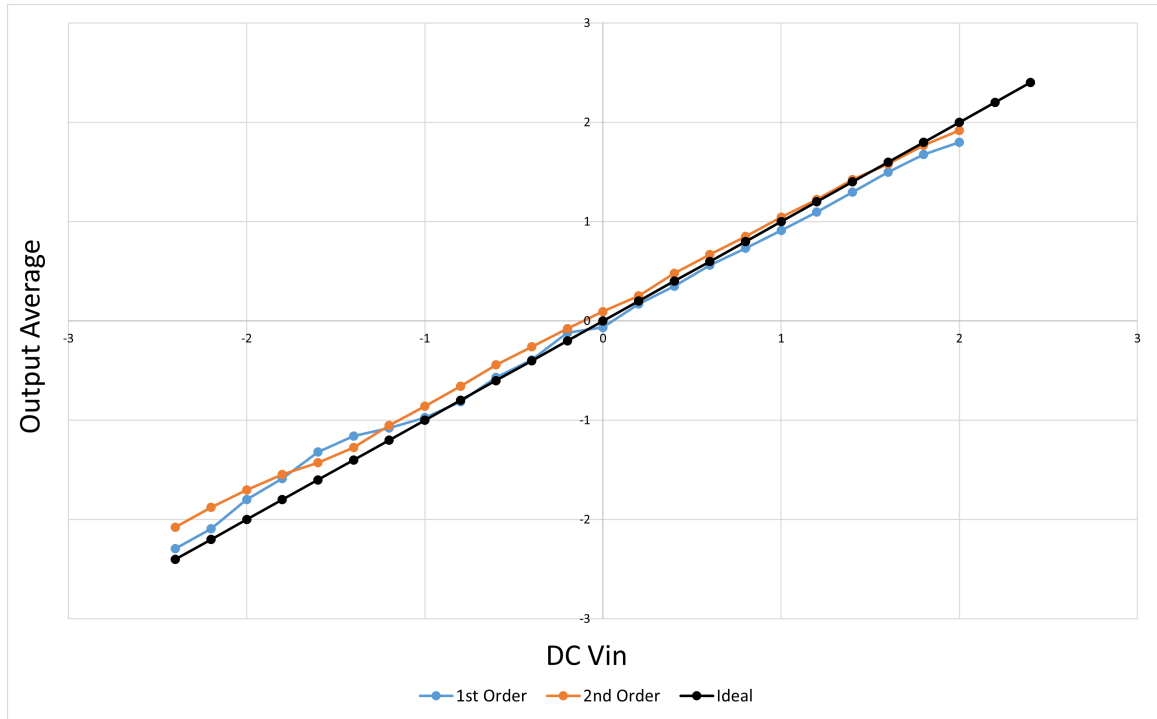
Figure 3.16: Cascade Input and Output Average Linearity of 1st Order, 2nd Order, and Ideal Case in Blue, Orange, and Black Respectively

3.6 Spectral Domain

Due to the limited memory of the Rigol Oscilloscope, only 1200 points per channel were able to be captured simultaneously. In order to preserve the quality of the data captured, all outputs for a given loop filter order were to be captured at the same time, so resulting data was only able to span about 6 ms corresponding to 6 input sinusoidal cycles. Capturing any more data resulted in aliasing and a loss of information. The input value used was a 1 kHz 3.5Vpp sinusoid, ensuring the -1.8 to +1.8 V input restriction set through DC measurements.

To determine which modulator provides the best performance on a printed circuit board, oscilloscope data was analyzed in Matlab to produce a frequency domain representation of the output for each modulator. The results for 1st and 2nd order loop filters are given in Figures 3.17 and 3.18 respectively.

In both the first and second order cases, FFT data was processed with a 12 point moving average filter to better understand the spectral qualities of each signal. The moving average was omitted around the frequency of the input (1kHz) to show its value. The third order case was measured, but neglected due to substandard results in the time domain.

For the first-order case, the DSM and OOLDP outputs best preserved the input signal, with the PWM and cascaded outputs having 1 to 2 more dB of attenuation in comparison. When looking near-band, the OOLDP output clearly had the worst spectral qualities, with about 2 dB greater noise for a decade around the input signal. Surprisingly, the PWM output showed the second worst output characteristics. This could be due to the lower oversampling ratio of the circuit, as shown in Figures 3.10 and 3.12. But these results were not expected from simulation, so some other causes may be the culprit. The cascaded and DSM outputs showed similar near-band noise, but the DSM wins overall as it also best preserves the input signal and produces the lowest quantization noise floor.

This implies that a delta-sigma modulator (DSM) both best preserves the input signal and best diminishes noise and distortion compared to other topologies studied in this thesis.
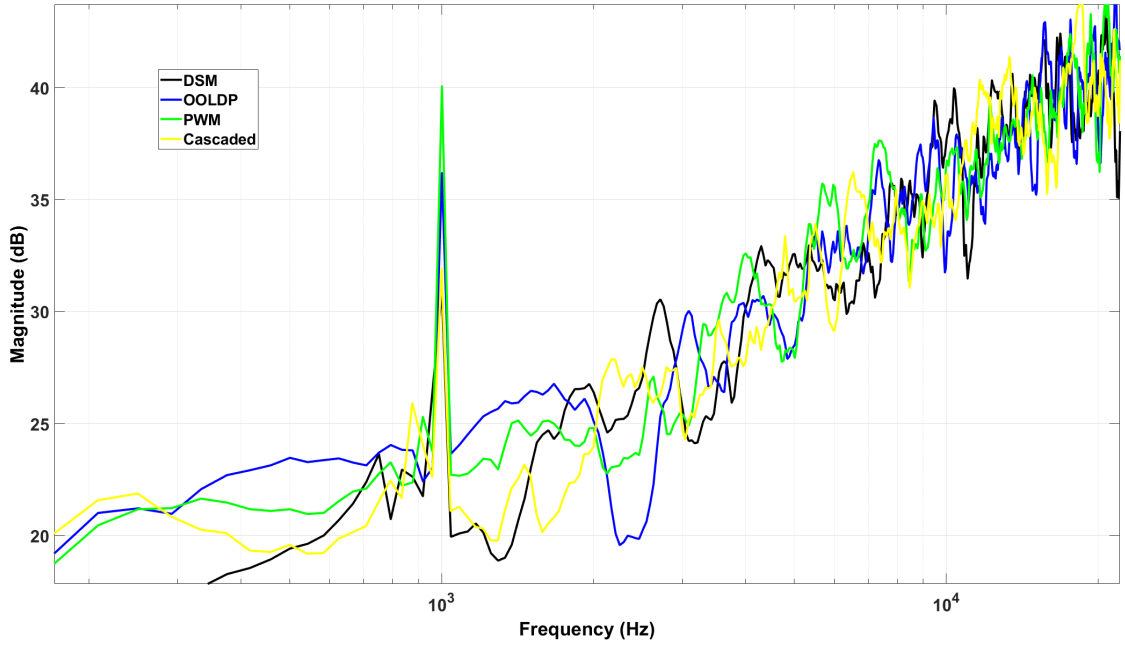
Figure 3.17: 1st Order Loop Filter Modulator Outputs

For a second-order loop filter, results were similar but not as explicit. The OOLDP output best preserves the input signal, but clearly has the worst in-band noise and distortion. The PWM and cascaded outputs showed very similar qualities in both input preservation and SINAD, with better qualities than OOLDP and worse qualities than the DSM. The DSM output showed the lowest magnitude at almost all frequencies, therefore having the least in-band noise and distortion, but additionally having the lowest input signal preservation.
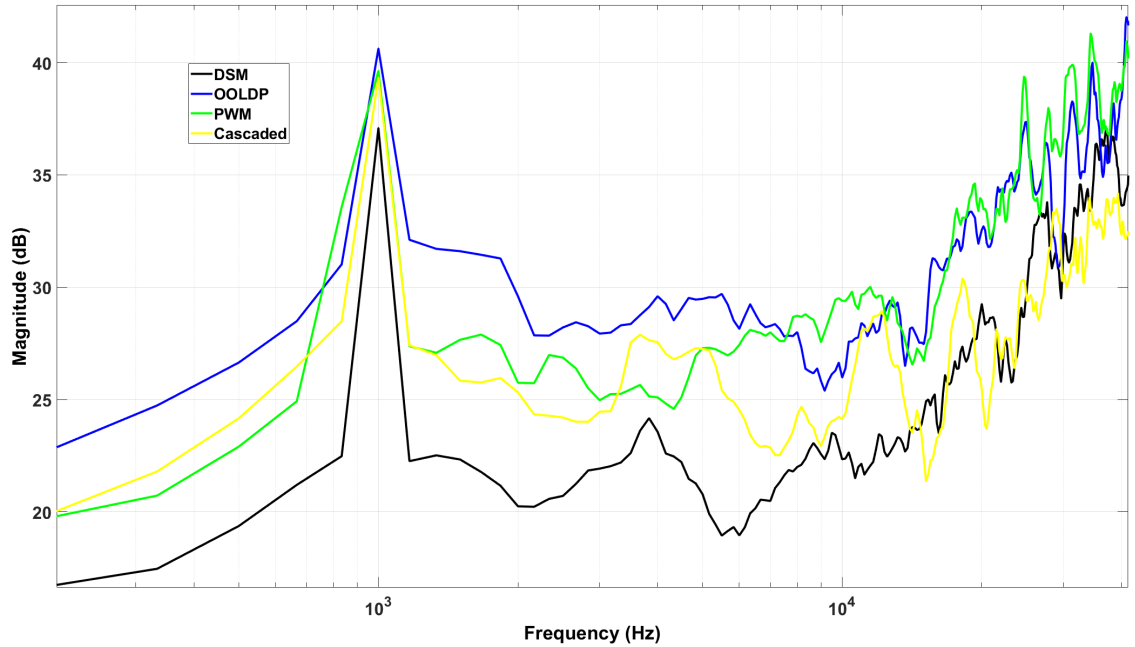
Figure 3.18: 2nd Order Loop Filter Modulator Outputs

These results point to the classic DSM as outperforming other alternatives, although this goes against other papers' findings [14] and results from simulation. There is some merit in using a cascaded modulator in that more output options are available and perhaps other advantages could arise from different oversampling ratios and loop filters. Overall, though, the discrete time modulator shows the most predictable results with a simple and versatile design.

Chapter 4

CONCLUSION

4.1 Summary

In an effort to maintain the advantageous noise floor of the PWM over the DSM, the OOLDP and Cascaded Modulator were presented as time-discretized PWMs. Ultimately, for an oversampling ratio of 150 the DSM showed favorable noise floor properties in printed circuit board implementation compared to all other modulators but weaker input to output average linearity, due to an offset issue in this implementation. The Cascaded and OOLDP results show that the DSM has merit as a noise-shaped time-discretization circuit, where a quantized magnitude, but continuous time signal is input. Overall, the DSM ostensibly retains its dominance in DSADC applications, where its simplicity and performance seem to outclass PWM alternatives presented in this paper, although further research needs to be done.

4.2 Future Work

The scope of this thesis originally involved pulse-width modulation of the input signal to provide a noise-shaped clock signal for the time discretization circuit in a DSM. Unfortunately, the supporting evidence was not strong enough to discern exactly what factors were at play in the circuit, so the idea was pivoted to what is in this paper. More research should be done on clock modulation, and other forms of noise shaping through clocking could be analyzed, such as alternate over sampling ratios for DSM, OOLDP, and Cascade DSMs. Other hysteretic windows could also be tested with the PWM to analyze the effect on quantization noise and noise shaping. Additionally,

the underlying cause of the frequency response of the DSM for varying DC inputs could be expanded upon.

4.3   Impacts of the Coronavirus Pandemic

Given the 2020 Coronavirus Pandemic, campus resources are limited and the design, build, and testing of the printed circuit board presented in this paper was made measurably more difficult. Resources from colleagues, my thesis committee, and the Cal Poly EE Department were pivotal in making any practical experimentation possible.
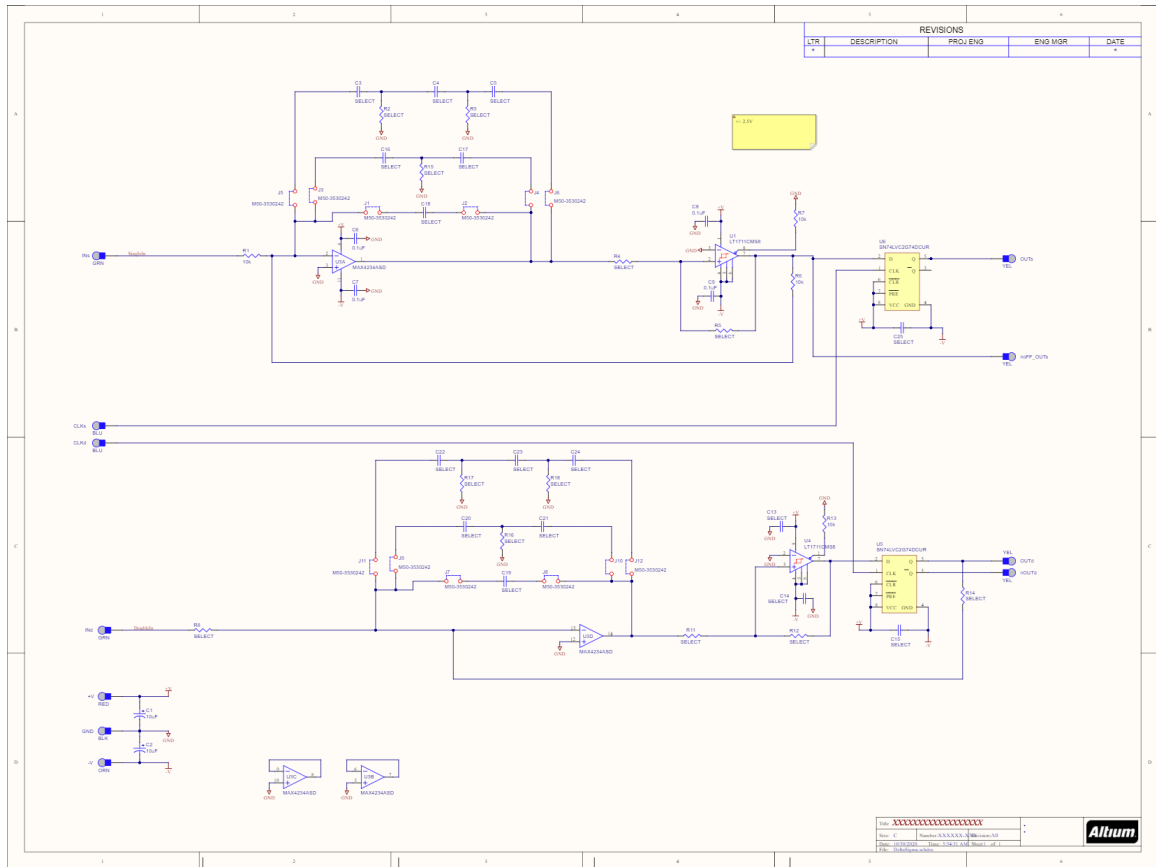
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APPENDICES

Appendix A

ALTIUM SCHEMATIC

Appendix B

ALTIUM LAYOUT