Joint Equalization and Synchronization for Carrierless Amplitude and Phase Modulation in Visible Light Communication

Kabiru O. Akande*, Paul Anthony Haigh† and Wasiu O. Popoola*

*Institute for Digital Communications, School of Engineering, The University of Edinburgh, Edinburgh

{K.Akande,W.Popoola}@ed.ac.uk

† Communications and Information Systems Group, University College London, London, WC1E 6BT, United Kingdom

{paul.anthony.haigh}@ucl.ac.uk

Abstract—In this paper, a linear adaptive least mean square (LMS) fractionally spaced equalizer (FSE) is proposed to jointly mitigate the severe inter-symbol interference (ISI) and timing jitter encountered by carrierless amplitude and phase modulation (CAP) in visible light communication (VLC) systems. The performance of FSE is compared to that of its counterpart, the symbol spaced equalizer (SSE), at the forward error control (FEC) bit error rate (BER) limit. It is shown that at a signal-to-noise ratio (SNR) of 20 dB and FEC BER limit of 3×10^{-3}, FSE is able to achieve a bit rate of 95 Mb/s (spectral efficiency η of 14.6 bits/s/Hz) while only 30 Mb/s (η of 4.6 bits/s/Hz) is possible with SSE using CAP-64. It is observed that the FSE performance is insensitive to timing jitter while SSE performance suffers severe degradation. The results therefore indicate that FSE is better suited for CAP-based VLC systems than the widely used SSE.

Index Terms—Carrierless amplitude and phase modulation (CAP), visible light communication (VLC), fractionally spaced equalization (FSE), timing jitter, optical communication.

I. INTRODUCTION

Visible light communication (VLC) is a promising technology that is attracting growing research interests due to its ability to achieve both lighting and data communication using light emitting diodes (LEDs) [1]. It is proposed as a low-cost complementary technology to radio frequency communication [1]. The main factor at the core of VLC is the use of LEDs and their unique fast switching speeds which are not found in other non-solid state lighting devices. LEDs are very efficient lighting devices that offer benefits such as low power consumption, long life expectancy, high tolerance to humidity, minimal heat generation lighting and higher luminous efficacy in comparison to the traditional incandescent and fluorescent lighting devices [2]. In addition to these benefits, the fast switching speeds of LEDs enable the possibility of data modulation on its radiated intensity without degrading the quality of the emitted light [3]. This property has led to the emergence of many interesting applications of VLC in indoor wireless communication [2]. The phosphorous-converted white LED (PC-LED), mainly employed for dual lighting and data communication, is generated by coating blue LED with a yellow-ish phosphorous. However, this phosphorous coating severely limits the

modulation bandwidth of the PC-LED to just a few megaHz [4]. Hence, a major challenge in the deployment of VLC for applications requiring high data rate transmission is the limited available bandwidth. The bandwidth-limiting effect of phosphorus coating can be reduced by employing a range of techniques including the use of blue filter, spectrally efficient modulation techniques, pre-equalization at the transmitter, post-equalization at the receiver and any combination of these techniques [5]–[10].

Orthogonal frequency division multiplexing (OFDM) is a complex modulation technique with great potential for improving the transmission speed of VLC links. However, its implementation complexity which arises from the use of an inverse fast Fourier transform (IFFT), in addition to a high peak-to-average power ratio (PAPR), serves as the motivation for considering alternative modulation schemes [11]. Carrierless amplitude and phase modulation (CAP) is a spectrally efficient modulation scheme currently being studied as an alternative to OFDM due to its many attractive features. The use of finite impulse response (FIR) filter for pulse shaping in CAP is the main advantage as it eliminates the need for carrier recovery and IFFT/FFT implementation as required in QAM and OFDM, respectively [4], [11]. CAP has also been demonstrated to achieve a better performance than OFDM in VLC system with a data rate of 3.22 Gb/s as against 2.93 Gb/s for OFDM [11]. Therefore, the combination of high spectral efficiency together with simplified transceiver makes CAP a competitive alternative candidate to OFDM in high speed VLC systems. To overcome the frequency selectivity and ISI that result from the non-flat frequency response and the limited bandwidth of the PC-LED, various equalization techniques have been proposed for CAP-based VLC systems. With a weighted pre-equalization and a modified constant multi-modulus algorithm (CMMA) based post-equalization, 1.35 Gb/s has been achieved in a multi-band CAP system [12]. A cascaded Volterra series-based non-linear equalizer was implemented for CAP in [13] to achieve an aggregate data rate of 4.5 Gb/s at a BER of less than 3.8×10^{-3}. Similarly, a hybrid post equalization involving both linear and non-linear equalizers was employed to achieve a high data
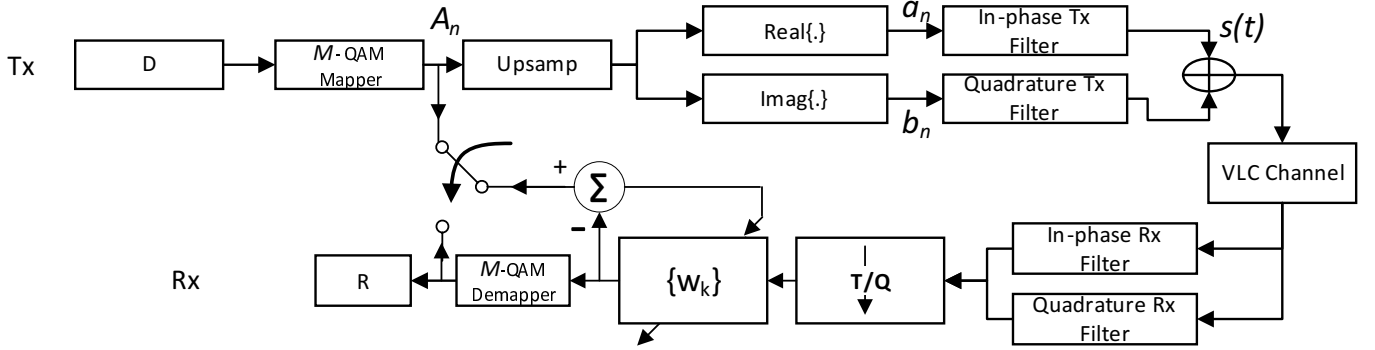
Fig. 1. Schematic block diagram of CAP modulation system with the equalizer component.

rate of 8 Gb/s using high order CAP modulation scheme in a VLC system [14]. Furthermore in [15], a decision feedback equalizer (DFE) has also been employed to mitigate severe ISI in a highly band-limited VLC system employing multi-band CAP (m-CAP). A comprehensive survey of the literature shows that the existing equalizers for CAP in VLC systems have been implemented mainly by setting the tap-spacing of the equalizer weights at the symbol duration which results in symbol-spaced equalizer (SSE). This is despite the reported advantage of non-adaptive fractionally spaced equalizer (FSE) over SSE [8], [10]. CAP has also been shown to be highly sensitive to timing jitter due to its simplified transceiver [16]. We therefore present in this paper, for the first time, the performance evaluation of adaptive FSE for CAP-based VLC systems. The FSE is proposed to mitigate both ISI and timing jitter using an experimental VLC channel.

The main difference between FSE and SSE is that the input sampling rate of SSE is the symbol rate while that of FSE is at least the Nyquist rate. This results in the summation of aliased components in SSE which could potentially lead to occurrence of null in the frequency spectrum of the SSE inputs when there is cancellation of aliased components with similar phase delay. Consequently, SSE will need to synthesize a high gain to compensate for this null which could result in noise enhancement and subsequent degradation in performance [17]. However, FSE avoids this potential pitfall by using no less than the Nyquist sampling frequency to avoid aliasing [18]. Thus, FSE is able to compensate directly for channel distortion before aliasing and mitigate the effect of any phase error in the equalizer input. As such, it is well suited to address the severe ISI and timing jitter sensitivity of the CAP modulation technique in VLC systems.

The rest of the paper is organized as follows: The CAP system and its jitter sensitivity are described in section II, section III discusses the proposed FSE architecture while the simulation results and discussions are presented in section IV. Finally, section V states the conclusion and future works.

II. CAP Modulation Scheme and Its Sensitivity to Timing Jitter

CAP is a multi-level, high order and spectrally efficient modulation technique with ease of implementation. It is essentially a variant of quadrature amplitude and phase modulation (QAM) with its quadrature carriers implemented as part of pulse shaping FIR filter to avoid the need for carrier modulation and carrier recovery at the transmitter and receiver, respectively. This approach leads to the realization of a low complexity transceiver which is the main advantage of CAP modulation. The block diagram of the CAP modulation scheme is shown in Fig. 1. The digital bits from the source, D, are mapped into multi-level symbols A_n by the M-QAM mapper. The resulting symbols are up-sampled by sufficient zero-padding in order to match the system sampling rate, f_s. The up-sampled signal is split into both real (a_n) and imaginary (b_n) components before being respectively passed through the transmit in-phase (I) and quadrature (Q) filters for pulse shaping. The impulse responses of the I and Q filters are generated as the multiplication of a root raised cosine filter (RRC) with cosine and sine waveforms, respectively. The output of the transmit filters are then added together with a DC bias (not shown in the block diagram) to ensure that a unipolar signal is sent over the VLC channel. The transmitted CAP signal, $s(t)$, is formulated as:

$$s(t) = \sum_{n=-\infty}^{\infty} [a_n p(t - nT) - b_n \tilde{p}(t - nT)] \qquad (1)$$

where T is the symbol period and n is the symbol index. The orthogonal filters, $p(t)$ and $\tilde{p}(t)$ are given as

$$p(t) = g(t)\cos(2\pi f_c t) \text{ and } \tilde{p}(t) = g(t)\sin(2\pi f_c t) \qquad (2)$$

where $g(t)$ is the RRC and f_c is the sinusoid frequency which must satisfy the following condition [16]:

$$f_c \geq \frac{(1 + \alpha)}{2T} \qquad (3)$$

where α is the roll-off factor which determines the extra bandwidth occupied by the transmitted symbols. At the receiver, the received signal is fed into the receive in-phase

and quadrature filters for matched filtering. The matched filter output is down-sampled at T/Q rate where Q determines how many samples are taken in each symbol duration. For SSE, $T/Q = T$ while $T/Q < T$ for FSE. The down-sampled signal is used as the equalizer input while the equalizer output is sampled at the symbol rate and converted to bits by the M-QAM demapper.

CAP Sensitivity to Timing Jitter

CAP is highly sensitive to timing jitter in comparison to its QAM counterpart [16]. The use of an f_c which is of the same order of magnitude as the symbol rate ensures a feasible filter realization but leads to reduced tolerance to timing jitter in CAP receiver architecture [19]. The CAP sensitivity to timing jitter was studied in [20] by examining the received eye diagram. A modified receiver was then proposed to reduce the timing jitter sensitivity but this solution increases the complexity of the receiver thereby nullifying the low complexity advantage of the CAP transceiver. The impact of timing jitter sensitivity on CAP performance has also been studied in [16]. The paper shows that with CAP-4 and a timing jitter of $0.2T$, the error rate is 0.5 indicating a total failure of the communication link. The proposed FSE can address any timing jitter error in the received CAP symbols, thereby eliminating the need for additional complexity in the receiver architecture.

III. FRACTIONALLY SPACED EQUALIZER

An optimum receiver for a signal corrupted by additive white Gaussian noise (AWGN) is a filter matched to that signal and whose output are sampled periodically at the symbol rate. If the channel introduces ISI then an equalizer is required to remove the ISI effect from the samples of the matched filter output. An SSE is designed by taking the samples of the matched filter output at the symbol rate. However, this results in spectrum aliasing as the symbol rate sampling is not sufficient to satisfy the Nyquist rate [18]. The presence of spectrum aliasing could result in the occurrence of nulls in the aliased spectrum when there is timing jitter, and hence this will potentially degrade the SSE performance as it will have to compensate for the nulls with large gains resulting in noise enhancement [17]. FSE, on the other hand, avoids spectrum aliasing by sampling its inputs faster than the symbol rate. The usual choice in the literature is twice the sampling rate resulting in $T/2$-spaced equalizer taps. The equalizer's output is then taken at the symbol rate which makes the FSE a decimating filter [18], [21].

The frequency response of an SSE equalizer can be expressed as [18]:

$$W_T(f) = \sum_{k=0}^{L-1} w_k e^{-j2\pi fkT} \tag{4}$$

where $\{w_k\}$ are the weights of the equalizer and L is the number of equalizer taps. The equalized spectrum can then be expressed as [18]:

$$H_T(f) = W_T(f) \sum_n X\left(f - \frac{n}{T}\right) e^{j2\pi(f-n/T)\tau} \tag{5}$$

where $X(f)$ is the spectrum of the received corrupted signal and τ is a timing delay. The transmitter and receiver clock frequencies should be perfectly synchronized ideally but there is usually some offset τ in practice due to mismatch in the transceiver clock rate. It can be observed that the summation term in (5) is a folded spectrum consisting of the sum of the aliased components and that the presence of a phase factor can result in potential noise enhancement due to spectral nulls.

However, FSE circumvents this potential noise enhancement in SSE by sampling its input at a higher rate of $T' = T/Q$. Hence, (4) and (5) can be expressed for FSE as:

$$W_{T'}(f) = \sum_{k=0}^{L-1} w_k e^{-j2\pi fkT'} \tag{6}$$

and

$$H_{T'} = W_{T'}(f) \sum_n X\left(f - \frac{n}{T'}\right) e^{j2\pi(f-n/T')\tau} \tag{7}$$

respectively. If Q is chosen appropriately to prevent aliasing in the folded spectrum, then (7) becomes [17]:

$$H_{T'}(f) = W_{T'}(f)X(f)e^{j2\pi(f)\tau}, \quad |f| \leq \frac{1}{2T'} \tag{8}$$

and the spectrum of FSE output can be expressed as:

$$H_{T'}(f) = \sum_n W_{T'}\left(f - \frac{n}{T}\right) X\left(f - \frac{n}{T}\right) e^{j2\pi(f-n/T)\tau} \tag{9}$$

since the output is sampled at the symbol rate (because the decisions on the received data are made at T-interval) and $\{w_k\}$ are adjusted only once for every Q inputs (Q/T rate adjustment does not result in faster convergence [18]). The main difference in the performance of SSE and FSE can be seen by comparing their outputs given by (5) and (9), respectively. It is seen that while (5) is the equalization of sum of aliased components, (9) is the aliased sum of equalized components. Therefore, the FSE is able to compensate directly for the received signal spectrum and any resulting timing jitter before aliasing due to symbol rate sampling at the equalizer output. This characteristic enables the FSE to avoid potential noise enhancement due to occurrence of null in the received spectrum and thus the possibility of performance degradation resulting from timing jitter error. Another intuitive explanation is that since the SSE takes one sample for every symbol, the sampling requirement is very strict such that the sampling clock needs to be adjusted to ensure the samples are taken at the peak, the "top dead center" [21], of the received pulses. FSE relaxes this strict sampling requirement by taken at least two samples for each received symbol. Hence, the FSE is more suitable to mitigate the timing jitter sensitivity of CAP and the severe ISI introduced by the bandlimited VLC system.
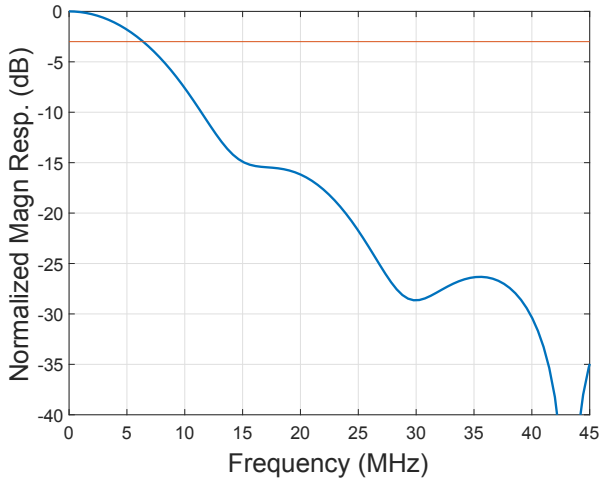
Fig. 2. The normalized frequency response of the overall measured VLC channel with a line through the -3 dB point.

Fig. 3. Sensitivity of the BER performance of the two equalizers to different step sizes (μ) and varying number of equalizer taps using CAP-4, SNR =15 dB and $R_b = 30$ Mb/s.

The two equalizers under test have been implemented as an adaptive FIR filter using least mean square (LMS) algorithm for training and adaptation of the equalizer taps. Equalizers generally require a training phase during which the equalizer tap coefficients are adaptively computed to mimic the channel through which the corrupted signal has traversed. In this paper, the LMS algorithm is used due to its simplicity of implementation and lower computational complexity [7], [17]. During the training phase, known transmitted symbols are compared to the equalizer outputs to generate an error signal which is used to adaptively update the equalizer weights.

The error signal at the ith iteration is given as [7]:

$$e_i = d_i - W_i^T X_i \tag{10}$$

where d is the desired symbol, X is a vector that represents the input samples to the equalizer and W^T is the transpose of the equalizer weight vector given as [7]:

$$W_{i+1} = W_i + \mu e_i X_i \tag{11}$$

The training phase lasts until the weights converge and the equalizer settles into steady state. The optimum weights, obtained after the equalizer convergence, are then used to equalize the received symbols in a decision-directed mode. In this mode, the decisions made on the equalizer outputs are used to guide the weights update as opposed to the known pattern that was used during the training phase.

Both FSE and SSE have been implemented in this paper using the same number of taps. This means that FSE incurs the same computational cost as SSE. Nevertheless, the FSE still demonstrates superior performance over SSE in mitigating ISI and correcting for timing jitter as depicted in the results of Section IV.

IV. SIMULATION RESULTS AND DISCUSSIONS

The performance of both FSE and SSE for CAP modulation in VLC system is investigated through extensive simulations.
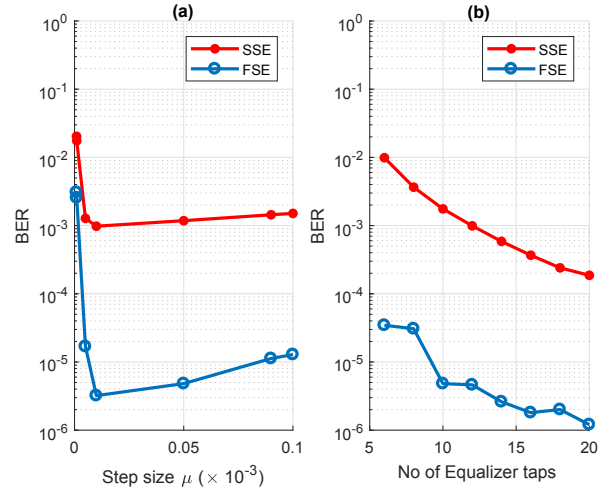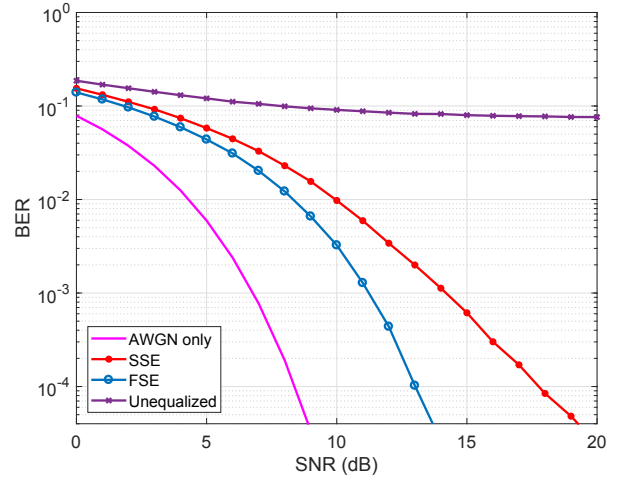

Fig. 4. BER performance of FSE and SSE for CAP-4 in bandlimited VLC channel, $R_b = 30$ Mb/s.

An experimental VLC channel with a non-flat frequency response whose -3 dB frequency cut-off is approximately 6.5 MHz as shown in Fig. 2 is used for the simulations. The two equalizer types are evaluated with regards to their performance for different data rate, SNR and varying constellation sizes. The sampling rate of the system is fixed as $f_s = 2$ GHz. This way, both the transmitted and the VLC channel samples have the same temporal and frequency resolution. The tap-spacing for FSE is set to $T/2$ to conform with the literature [18]. In all cases, the received electrical SNR is used in the simulations.

The sensitivity of the BER performance of the two equalizers to different step sizes (μ) and varying number of equalizer taps are presented in Fig. 3 (a) and 3 (b), respectively. The selection of the optimum value of μ is very critical to
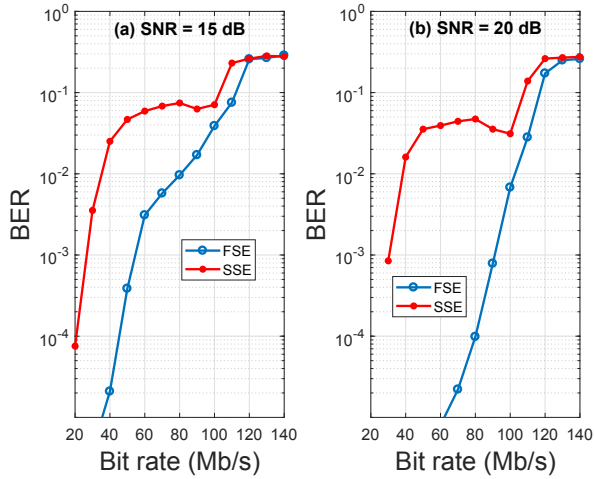
Fig. 5. BER performance of FSE and SSE for CAP-16 in bandlimited VLC channel for different data rate at SNR of (a) 15 dB and (b) 20 dB.

Fig. 7. Mitigation of timing jitter sensitivity of CAP-16 by FSE and SSE at $R_b = 10$ Mb/s and SNR=10 dB.
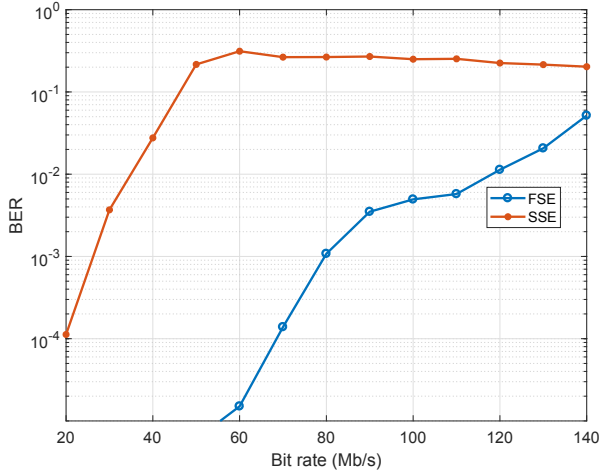

Fig. 6. BER performance of FSE and SSE for CAP-64 in bandlimited VLC channel for different data rate at SNR of 20 dB.

the performance of the equalizers as small step size leads to slow convergence rate while a large step size results in instability in the algorithms. An illustration of the process of choosing μ is shown Fig. 3 (a) with an optimum step-size of $\mu = 1 \times 10^{-5}$ occurring at the "elbow" of the curve. Based on Fig. 3 (b), the number of equalizer taps is chosen as 12 to achieve a compromise between performance and complexity. This is because the performance of an equalizer generally improve with increasing number of taps but results in higher computational complexity.

The comparison of the BER performance of both the FSE and SSE for CAP-4 transmission over a VLC channel with 6.5 MHz bandwidth is depicted in Fig. 4 at $R_b = 30$ Mb/s. The figure also shows the unequalized and theoretical (AWGN only) performance. The theoretical performance in AWGN only is the benchmark for measuring the severity of the ISI and
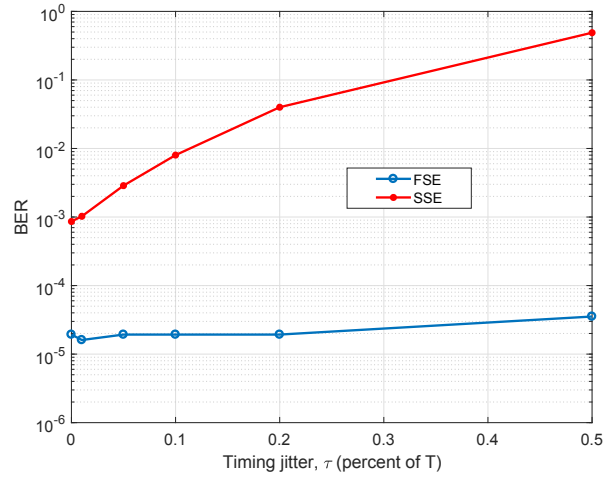
the subsequent performance of the equalizers in mitigating the ISI. The severity of VLC ISI is shown in this figure, as the system is unable to achieve a reliable transmission without equalization judging from the BER of 10^{-1} attained by the unequalized performance. Furthermore, for any given SNR, the BER performance of FSE is lower than that of SSE and the difference in performance between FSE and SSE becomes more pronounced as the SNR increases. For example, the SNR required for FSE to achieve a BER of 10^{-4} is 13 dB while SSE requires 18 dB resulting in a substantial SNR gain of 5 dB for FSE. Further simulations are carried out at different data rates and constellation sizes to highlight the performance gain of FSE over SSE in mitigating ISI for a CAP-based VLC system.

The BER performance of FSE and SSE for CAP-16 at different transmission speeds are presented in Figs. 5 (a) and 5 (b) corresponding to SNR of 15 dB and 20 dB, respectively. The FSE has a lower BER than SSE in all the transmission speeds and SNR considered. The performance gain increases with increasing SNR. At an SNR of 15 dB and the FEC BER limit of 3×10^{-3}, SSE is only able to achieve 30 Mb/s ($\eta = 4.6$ bits/s/Hz), while FSE achieves 65 Mb/s ($\eta = 10$ bits/s/Hz). This translates to a 5.4 bits/s/Hz increase in η as shown in Fig. 5 (a). Also, the performance improvement in η increases with increasing SNR. It is shown in Fig. 5 (b) that at the same FEC BER limit and SNR of 20 dB, a bit rate of 95 Mb/s ($\eta = 14.6$ bits/s/Hz) is attainable using FSE as against only 35 Mb/s ($\eta = 5.4$ bits/s/Hz) for SSE. This means an increase of 9.2 bits/s/Hz for a 5 dB increase in SNR.

For CAP-64, FSE results in a bit rate of 95 Mb/s ($\eta = 14.6$ bits/s/Hz) while only 30 Mb/s ($\eta = 4.6$ bits/s/Hz) is achievable with SSE as shown in Fig. 6. Therefore, it can be concluded that FSE performs better than SSE and the performance improvement increases with increase in SNR and constellation size. Although not presented here, the FSE requires shorter training sequence as it converges faster to

a steady state and to a lower mean square error (MSE) in comparison to the SSE.

Finally, Fig. 7 depicts the performance of the two equalizers over a range of timing jitter using CAP-16. It is shown that as timing jitter increases, FSE is able to correct for the timing jitter effects as its performance remains constant while SSE performance suffers severe degradation making reliable communication impossible. Therefore, a separate synchronization circuit is not required to correct for the extreme sensitivity of CAP to timing jitter when using FSE. This leads to reduction in the overall system cost and the low complexity pedigree of CAP is thus preserved.

V. CONCLUSION

Carrierless amplitude and phase modulation encounters severe ISI in bandlimited VLC systems and its high sensitivity to timing jitter results in further performance degradation. FSE has been proposed for the joint equalization and synchronization of CAP, for the first time, in VLC systems. It is shown that at the FEC BER limit and an SNR of 15 dB, for a 6.5 MHz bandwidth CAP-based VLC system, the attainable data rate (and the spectral efficiency) increases from 30 Mb/s ($\eta = 4.6$ bits/s/Hz) for SSE to 65 Mb/s ($\eta = 10$ bits/s/Hz) for the FSE using CAP-16. The FSE improvement over SSE is more pronounced when the SNR and the constellation size are increased. At an SNR of 20 dB using CAP-64, the gain in data rate and η increases to 65 Mb/s and 10 bits/s/Hz, respectively for FSE over SSE. Therefore, FSE achieves a higher data rate and spectral efficiency than the usually employed SSE and the improvement increases with increasing SNR and constellation size. Finally, FSE is able to mitigate the high timing jitter sensitivity of CAP in VLC systems as its BER performance remains constant with increasing timing jitter while SSE performance degrades.

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