FIELD PROGRAMMABLE GATE ARRAY ARCHITECTURE OF PROPORTIONAL-INTEGRAL-DERIVATIVE CONTROLLER

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requirements for the award of the degree of
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"in The Name of Allah The Most Gracious The Most Merciful

seeking forgiveness from Rabb All-Hearer All-Sufficient"

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ABSTRACT

Proportional-integral-derivative (PID) control is widely used in control and automation. PID implementation in software especially using microcontroller requires a lot of CPU execution time. The performance of PID controller can be improved by accelerating control function in hardware. Thus, the performance and throughput can be further improved when incorporated in FPGA architecture system. This project focuses on exploration of hardware architecture of PID controller and targeted for implementation on FPGA system. The architecture exploration include concurrent, serial and pipeline designs, functionality correctness and non-functional verification. These architectures was designed to support modularity and can be use for other control applications. Serial design architecture of PID is able to reduce ~ 60% of datapath unit resources compared to concurrent design but it required five cycles to produce the output. High throughput can be achieve using pipeline design and required 7 more registers compared to concurrent design with pipeline speed up about 1.5 and five times compared to serial design architecture.

ABSTRAK

Kawalan berkadar terus-berkamiran-pembeza (PID) digunakan secara meluas dalam sistem automasi. Perlaksanaan sistem kawalan berkadar terus-berkamiran-pembeza dalam bentuk perisian terutama pegawal terbenam memerlukan masa yang panjang memproses arahan. Prestasi kawalan berkadar terus-berkamiran-pembeza dapat ditingkatkan dengan menjana fungsi kawalan ke dalam perkakasan. Oleh itu, prestasi dan hasil keluaran dapat ditingkatkan dengan lebih tinggi melalui penggabungan sistem seni bina FPGA. Projek ni memberi tumpuan kepada penerokaan seni bina perkakasan kawalan berkadar terus-berkamiran-pembeza yang boleh dilaksanakan melalui sistem FPGA. Penerokaan meliputi reka bentuk serentak, sesiri dan saluran paip, menguji ketepatan fungsinya dan aspek yang lain. Reka bentuk seni bina yang dibangunkan direka untuk menyokong kesesuaian modul dan boleh diguna pakai untuk kegunaan kawalan yang lain. Seni bina pengawal dengan reka bentuk sesiri dapat mengurangkan sumber pembinaan laluan data sebanyak 60 peratus berbanding rekabentuk serentak tetapi memerlukan masa lima kali ganda untuk mengeluarkan hasil keluaran. Pemprosessan tinggi boleh dihasilkan dengan menggunakan reka bentuk saluran paip dan ia memerlukan lebih tujuh penyimpan memori berbanding rekabentuk serentak dengan kelebihan 1.5 kali ganda hasil keluaran and lima kali ganda dibandingkan dengan reka bentuk sesiri.