Title: A closed loop control based power manager for WiNoC architectures

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Abstract: In modern CMOS technologies, the integration density continues to increase while limitations due to the wires interconnect become a bottleneck especially in multi-hop intra-chip communications. Emerging architectures, such as Wireless Networks-on-Chip (Wi- NoC), represent the candidate solutions to deal with communication latency issues which affect the many-core architectures. In WiNoC, metallic wires are replaced with long-range radio interconnections. Unfortunately, the energy consumed by the RF transceiver (i.e., the main building block of aWiNoC), and in particular by its transmitter, accounts for a significant fraction of the overall communication energy. Current WiNoC proposals use the same transmitting power for each transmitter regardless the physical location of the receiver antenna. This paper proposes a closed loop control mechanism that, based on the bit error rate observed by the receivers, selectively reconfigures the transmitters by calibrating their transmitting power. Preliminary results show the effectiveness of the proposed technique which allows to save up to 40% of energy with less than 2% of performance degradation.