CNTFET-BASED TERNARY LOGIC DESIGN AND ARITHMETIC CIRCUIT SIMULATION USING HSPICE

EE POEY GUAN

UNIVERSITI TEKNOLOGI MALAYSIA

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EE POEY GUAN

A project report submitted in partial fulfilment of the
requirements for the award of the degree of
Master of Engineering (Electrical - Computer and Microelectronic System)

Faculty of Electrical Engineering
Universiti Teknologi Malaysia

JANUARY 2015

Specially dedicated to my beloved family, lecturers and friends
For the guidance, encouragement and inspiration
Throughout my journey of education

ACKNOWLEDGEMENT

First, I would like to take this opportunity to express my deepest gratitude to my project supervisor Ir. Dr. Michael Tan Loong Peng, for his supports and supervision. He has been very helpful with the installation of circuit simulator, and has been guiding me to the right path ever since. I sincerely thank him for his supports.

In addition, I wish to thank my postgraduate course-mates for their cooperation and information sharing in completing this project. Yet, not to forget my fellow friends for their care and moral support when it was most required.

Furthermore, I would like to thank my friends for their encouragement and supports. They had gave me useful opinion and assistance. Last but not the least, I am very thankful for my family members for their spiritual and financial supports.

ABSTRACT

This project report focuses on the multiple-value logic (MVL) or commonly known as ternary logic gates by using carbon nanotube (CNT) FETs devices (CNTFETs). It is shown ternary logic has promising future in CNTFETs when compare to conventional binary logic design, due to its simplicity and energy efficiency in digital design reduced circuit overhead such as chip area and interconnection. In this research, existing CNTFET-based binary inverter and standard ternary inverter with resistive-load (STI-R) for comparison with the other three types of inverter are proposed - Complementary Standard Ternary Inverter (CSTI); Standard Ternary Inverter with 1 resistor and 3 NCNTFET (NSTI-R); Standard Ternary Inverter with 1 resistor and 3 PCNTFET (PSTI-R) to analysis the performance, structure design and application. In addition, the research covers all the basic logic Ternary NAND gate and Ternary NOR gate for further benchmarking. All simulation results using SPICE are obtained and analyzed in the Direct Current (DC) setting and verifed using half adder. Further study behavior of ternary logic includes the implementation of partial binary design into the ternary design and performance benchmarking. The result shows the CSTI have advantage on low power design with low leakage while NSTI-R has advantage on high-speed design inverter. In addition, partial binary design in the arithmetic circuit ternary design with CSTI shows added advantage in a low power design.

ABSTRAK

Projek ini berfokus multi nilai logik atau dikenal pasti sebagai gate logik pertigaan dengan menggunakan "tiub nano karbon peranti kesan sirip transistor (CNTFETs)" logik pertigaan telah menunjukkan masa depan yang cerah dan menyakinkan dari segi permudahan and penjimatan tenaga dari kajian apabila dibandingkan dengan logik binari dari segi penggunaan jumlah kawasan chip dan hubungan antara transistor. Pada kajian ini, CNTFET-based binari penyongsang dan ternari penyongsang jenis beban resistor akan dibanding dengan tiga jenis invertor yang dicadangkan - Pelengkap Standard pertigaan Penyongsang (CSTI); Standard pertigaan penyongsang dengan 1 perintang dan tiga NCNTFET (NSTI-R); Standard pertigaan penyongsang dengan 1 perintang dan tiga PCNTFET (PSTI-R) untuk mengkaji prestasi, stuktur bina dan penggunaan. Semua keputusan simulasi dikaji dengan menggunakan SPICE untuk menentu prestasi arus terus dengan pengesahan penggunaan litar aritmatik panambah separuh untuk mengenalpasti prestasi logik pertigaan. Kajian mengenalkan sebahagian reka binari digunakan ke atas rekaan logik pertigaan dengan memerhatikan prestasiny. Keseluruhanya, CSTI menunjukkan kelebihan dalam litar kuasa rendah dengan kebocoran tenaga rendah dan NSTI-R menunjukan pantasannya pada litar laju. Manakala, pengenalan reka binary ke dalam litar aritmetik ternari dengan menggunakan CSTI lagi menunjukkan kelebiahan pada litar kuasa rendah.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	DECLARATION	ii
	DEDICATION	iii
	ACKNOWLEDGEMENT	iiv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	ix
	LIST OF FIGURES	x
	LIST OF ABBREVIATIONS	xiii
	LIST OF APPENDICES	xv
1	**INTRODUCTION**	1
	1.1 History of Transistor	1
	1.2 Problem Statements	5
	1.3 Objectives	5
	1.4 Scope of Work	6
	1.4 Signigicance of Study	6
2	**LITERATURE REVIEW**	7
	2.1 Review of Ternary Logic.	7
	2.2 Carbon Nanotube (CNT)	10
	2.3 Carbon Nano Tube FET	12
	2.4 CNTFET-Based Ternary Inverter design	14
	2.5 Ternary Arithmetric	18

3	**RESEARCH METHODOLOGY**	19
	3.1 Introduction	19
	3.2 Stanford University CNFET Model	20
	3.3 HSPICE	21
	3.4 CosmosScope	21
	3.5 Gantt Chart	22
	3.6 CNTFET Schematic	23
	3.7 Ternary K-Map and Arithmetic Design	24
	3.8 Ideal & Non-Ideal input for Ternary Design	25
4	**RESULTS AND DISCUSSION**	26
	4.1 Inverter	26
	4.1.1 Proposed 2 new type of STI for the circuit	26
	4.1.2 Ternary Resistive Load	28
	4.1.3 Ternary CSTI	30
	4.1.4 PSTI-R and NSTI-R Simulation result	32
	4.1.4 Inverter result	32
	4.2 T-NAND Gate and T-NOR Gate	37
	4.3 Tenary Half Adder (T-HA)	40
5	**CONCLUSION AND FUTURE WORK**	46
	5.1 Conclusion	46
	5.2 Future Work	48
REFERENCES		49
Appendices A – E		52

LIST OF TABLES

TABLE NO.	TITLE	PAGE
1.1	Technology node versus gate length	3
1.2	Samsung Unveil SSD using its new 3-bit V-NAND Storage Technology	4
2.1	Ternary inverter logic	8
2.2	Truth Table of STI, PTI and NTI.	9
2.3	Truth Table of T-NAND gate and T-NOR gate.	9
2.4	Ternary addition rules	18
3.1	Gantt chart for first semester	22
3.2	Gantt chart for second semester	22
4.1	Summation K-Map from HA	40
4.2	Carry K-Map from HA	40

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	Moore's Law	1
2.1	Single-wall carbon nanotubes (SWCNT)	10
2.2	Multi-wall carbon nanotubes (MWCNT) with three shells	10
2.3	Number of articles which contain the phrase 'CNT'	11
2.4	Number of issues and applications that contain the phrase 'CNT'	11
2.5	Cross sectional view Schematic diagram of a CNT transistor	12
2.6	Top view of Schematic diagram of a CNT transistor	13
2.7	Threshold voltage of CNTFETs versus n (for m = 0)	14
2.8	Schematic diagram of resistive load CNTFET-based STI proposed in.	15
2.9	Proposed CNTFET-based STI design complementary style (CSTI)	26
2.10	Schematic diagram of (a) NTI and (b) PTI	17
2.11	Symbols of (a) STI, (b) NTI, and (c) PTI	17
3.1	Research methodology flowchart	20
3.2	Proposed new way of sketching the CNT in diagram	23

3.3	2 variable K-Map	24
4.1	N-type ternary with only one resistor (NSTI-R)	27
4.2	P-type ternary with only one resistor (PSTI-R)	28
4.3	STI-R Simulation on R1 versus R2	29
4.4	Delay of the STI-R	29
4.5	CSTI VTC curve	30
4.6	CSTI transient response	30
4.7	CSTI with different configuration tube	31
4.8	PSTI-R VTC curve	32
4.9	PSTI-R transient response	32
4.10	NSTI-R VTC curve	33
4.11	NSTI-R transient response	33
4.12	Transient response on all TIs and binary inverter	34
4.13	PDP for TI and Binary CNTFET inverter	35
4.14	EDP for CSTI and Binary CNTFET inverter	35
4.15	EDP for PSTI-R, NSTI-R & STI-R	36
4.16	Output result for T-NAND	37
4.17	Transient response for T-NAND	37
4.18	Output result for T-NOR	38
4.19	Transient response for T-NOR	38

4.20	PDP for T-NAND & T-NOR	39
4.21	EDP for T-NAND & T-NOR	39
4.22	RT buffer	41
4.23	Unary decoder	41
4.24	Output Unary decoder	42
4.25	Ternary Half adder circuit	42
4.26	Ternary HA result with ideal input	43
4.27	Ternary Half adder circuit with Binary Logic mixture	43
4.28	Transient response of different HA	44
4.29	PDP of different HA	44
4.30	EDP of different HA	45
5.1	Binary versus ternary data handling in bits	47
5.2	Proposed ternary ALU	48

LIST OF ABBREVIATIONS

CMOS	-	Complementary Metal–Oxide–Semiconductor
MOSFET	-	Metal–Oxide–Semiconductor Field-Effect Transistor
R	-	Resistor
L	-	Inductor
C	-	Capacitor
W	-	Width
L	-	Length
NMOS	-	N-channel Metal-Oxide-Semiconductor
PMOS	-	P-channel Metal-Oxide-Semiconductor
FET	-	Field Effect Transistor
CNTFET	-	Carbon Nano Tube Field Effect Transistor
NCNTFET	-	N-type Carbon Nano Tube Field Effect Transistor
PCNTFET	-	N-type Carbon Nano Tube Field Effect Transistor
V_{th}	-	Threshold Voltage
STI	-	Standard Ternary Inverter
PTI	-	Positive Ternary Inverter
NTI	-	Negative Ternary Inverter
STI-R	-	Standard Ternary Inverter With resistor load
NSTI-R	-	Standard Ternary Inverter with 1 resistor and 3 NCNTFET
PSTI-R	-	Standard Ternary Inverter with 1 resistor and 3 PCNTFET
CSTI	-	Complimentary Standard Ternary Inverter
TI	-	Ternary Inverter
T-NAND	-	Ternary NAND Gate Logic
T-NOR	-	Ternary NOR Gate Logic
CT-NAND	-	Complimentary Ternary NAND Gate Logic
NT-NAND-R	-	Ternary NAND Gate Logic with NSTI-R inserted
T-HA	-	Ternary Half Adder
SOC	-	System on Chip

SSD	-	Solid State Devices
SWNT	-	Single Wall Nano Tube
MWNT	-	Multi Wall Nano Tube
VLSI	-	Very Large Scale Integration
VTC	-	Voltage Transfer Curve
DC	-	Direct Current
SPICE	-	Simulation Program with Integrated Circuit Emphasis
PDP	-	Power Delay Product
EDP	-	Energy Delay Product

LIST OF APPENDICES

APPENDIX	TITLE	PAGE
A	CNTFET HSPICE Netlist Model	52
B	Binary CNTFET HSPICE Netlist	53
C	Ternary CNTFET HSPICE Netlist	54
D	Ternary CNTFET Arithmetic Circuit HSPICE Netlist	56
E	Binary CNTFET Results	58

CHAPTER 1

INTRODUCTION

1.1 History of Transistor

According to the popular Moore's Law, the number of transistors that can be placed on a single die doubled every two years [1]. Based on this assumption, it is predicted that in 2018, the end of complementary metal-oxide semiconductor (CMOS) era is immiment. Thus, new material and technique of fabrication or design system have been proposed and tested in many of the semiconductors manufacturing industries.

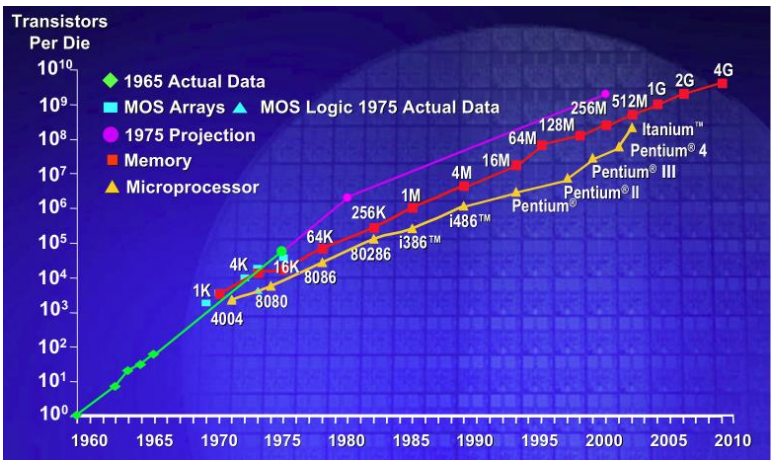

Figure 1.1 Moore's Law [2]

This is very promising when the number of transistors is increasing that allow more features in a system-on-chip (SOC) and more transistor in the same die size. Technology node and their respective physical gate length from 2007 to 2014 is tabulated in Table 1.1

Table 1.1 : Technology node versus gate length [3]

Year	Technology node (nm)	Physical gate length (nm)
2007	45	32/29
2009	32	27/24
2011-2012	22	22/20
2013-2014	16	18/16

When downscaling is done to increase the gate count and high switching rate, it introduces a high leakage current ratio due to the limitation of conventional CMOS. Thus, new materials such as carbon nanotube, silicon nanowire and graphene are introduced to overcome this problem. In this research, carbon nanotube FET (CNTFET) in digital circuit simulation is explored. In other words, this project is focused on the simulation of Carbon Nanotube Field-Effect Transistors (CNTFET) with the ternary design and benchmark with binary design. Ternary logic design later to be verified the performance and correctness using arithmetic circuit.

Since digital logic is introduced, digital computation is only performed on two-valued logic (0 or 1, TRUE or FALSE) in the Boolean space. Multiple-valued logic (MVL) replaces the classical Boolean characterization of variables with either finitely or infinitely many values such as ternary logic [4] or fuzzy logic [5]. Ternary logic (or three-valued logic) has attracted considerable interests due to its potential advantages over binary logic for designing digital systems. For example, it is possible for ternary logic to achieve simplicity and energy efficiency in digital design since the logic reduces the complexity of interconnects and chip area. Furthermore, serial and serial-parallel arithmetic operations can be faster if the ternary logic is employed. Besides

resistive load design, ternary logic using CMOS can be found in the technical literature [6-7]. Chip area and power dissipation is reduced by more than 50 percent using an efficient MVL implementation for a signed 32-bits multiplier compared to its fastest binary counterpart [8]. MVL modules have been inserted into binary logic ICs to enhance the performance of CMOS technologies [9].

There are two kinds of MVL circuits based on MOS technology, namely the current-mode MVL circuits and the voltage mode MVL circuits. Voltage-mode MVL circuits have been achieved in multithreshold CMOS design [10]. The carbon nanotube (CNT) FET (CNTFET) is a promising alternative to the bulk silicon transistor for low-power and high-performance design due to its ballistic transport and low OFF-current properties [11-15]. A multithreshold CMOS design relies on body effects using different bias voltages to the base or the bulk terminal of the transistors. In a CNTFET, the threshold voltage of the transistor is determined by the diameter of the CNT. Therefore, a multithreshold design can be accomplished by employing CNTs with different diameters (and, therefore, chirality) in the CNTFETs. A resistive-load CNTFET-based ternary logic design has been proposed in Ref. [8]. However, in this configuration, large OFF-chip resistors (of at least 100MΩ values) are needed due to the current requirement of the CNTFETs. The design technique proposed in this paper base on Ref. [16] to eliminate the large resistors by employing active load with p-type CNTFETs in the ternary logic gates. In this paper, the multivalued logic design based on multithreshold CNTFETs is assessed and compared with existing multivalued logic designs based on CNTFETs.

In this research, designs of basic ternary gates/operators inverter is described in details namely ternary inverters (TI), ternary NAND (T-NAND), and ternary NOR (T-NOR). Beside resistive load inverter, another three type of inverter is used to benchmark performance. Ternary half adder (T-HA) is used for the reference to verify and analysis are presented as examples of the application of these ternary gates design technique.

For the arithmetic circuit design, a modified ternary logic circuit design technique is used to speed up and reduce power consumption of the circuits. The modified ternary logic design uses both ternary logic gates and binary logic gates based on the previous ternary logic design structures to take advantage of the two logic design styles' merits. The ternary logic gates are a good candidate for decoding block since it requires less number of gates while binary logic gates are a good candidate for fast computation. In this report, the modified ternary logic design method is proposed to achieve gate count reduction. Figure 1.2 is another solid proof that at CMOS design, Samsung already produce Solid State Device using 3-Bit V-NAND Technology and it proof the ternary can be very useful to handle the massive data. System on Chip (SOC) become main stream design, data handling become more heavy and most probably ternary design can be the replace binary design in some application .

Figure 1.2 Samsung unveil SSD using its new 3-bit V-NAND storage technology [17]

1.2 Problem Statements

Silicon (Si) MOSFET has reached its limits as the technology is scaling down. Unlike Si MOSFET, CNTFET is favorable [8] due to its ballistic transport and low OFF current properties. This research addressed the following issues: How many type of Ternary inverter can be proposed for CNTFET-based design? What type of application can be applied on these few type of ternary inverter? What is the performance of ternary logic in CNTFET versus Binary logic in CNTFET? What is the maximum number of CNT can be placed in the channel to obtain the optimum performance of the device? How to model the 3 bits input for the ternary design using HSPICE?

1.3 Objectives

Since the Silicon based MOSFET is reaching the end of roadmap, this project is based on SPICE circuit-simulation of a type of multi-level logic gate design using Carbon Nanotube Field Effect Transistor (CNTFET). The objectives are:

1. To compare CNTFET-based binary inverter and standard ternary inverter with resistive-load (STI-R) with other three type of inverter is proposed - Complementary Standard Ternary Inverter (CSTI); Standard Ternary Inverter with 1 resistor and 3 NCNTFET (NSTI-R); Standard Ternary Inverter with 1 resistor and 3 PCNTFET (PSTI-R) to analysis the performance
2. To extend the ternary logic design to arithmetic ternary design and analyze the performance.
3. To study the combination of ternary design and binary design hence benchmark it performance.

1.4 Scope of Work

The main scope of this project is to study and simulate four types of inverter ternary design using CNTFET where the SPICE model is obtained from Stanford University. Four types ternary Inverter design is further analysis and benchmarks with Binary design to evaluate the performance. Arithmetic circuit used to verify the correctness from the ternary design. In addition, combination of ternary design and binary design in the ternary arithmetic is studied and simulated to improve the performance. HSPICE is used alongside Cosmoscope to perform digital circuit simulation. 3 bits input from the HSPICE model is introduced for ternary design and used for all ternary design simulation. Arithmetic circuit is used to simulate and study the energy efficiency and benchmarked with binary logic CNTFET design.

1.5 Significance of Study

This project has several important outcomes, which are

1. A new design of inverter is propose into the ternary design and identify the performance in several application.
2. Ternary design shown is state of art at the future to handle massive data processing and storage.
3. Tolerance of ternary input is identify with imperfect three levels (logic 0, 1 and 2) of square wave.

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