

HARDWARE AND SOFTWARE CO-SIMULATION PLATFORM FOR
CONVOLUTION OR CORRELATION BASED IMAGE PROCESSING
ALGORITHMS

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My genuine dedications to,
My beloved wife, father and mother;
My enduring and experienced supervisor;
Who are always there for me,
Every step of the way,
Thanks!

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ABSTRACT

Software implementation of image processing algorithms in which convolution or correlation is applied is too slow to be real-time. As long as the system design gets larger, it should be partitioned into two parts: software and hardware. In order to achieve real time performance, it is essential to map the fast convolution or correlation module, which is the heaviest computation intensive part, in hardware instead of software. Our test case is “generic image pre-processing algorithm” which includes resizing, noise filtering and normalization. In noise filtering part of the preprocessing algorithm in which convolution is used should be implemented in hardware while the rest of the preprocessing algorithm stays in software. Next, to verify our hardware/design software we can deploy it on FPGA board, but it is very time consuming and involves a lot of technical complexities. In that case, this design used hardware/software co-simulation and direct programming interface (DPI-C) whereas it allows System Verilog calls C functions and vice versa. The proposed work has overcome the problems faced when running a co-simulation based on Modelsim simulated using direct programming interface (DPI) technique.

ABSTRAK

Pelaksanaan perisian algoritma pemprosesan imej di mana kekusutan atau korelasi digunakan adalah terlalu lambat untuk dilaksanakan dalam masa nyata. Apabila reka bentuk sistem bertambah besar, proses berkenaan harus dibahagikan kepada dua bahagian: perisian dan perkakasan. Untuk mencapai prestasi masa nyata, ia adalah penting untuk memetakan modul kekusutan atau modul korelasi, yang merupakan bahagian pengiraan yang intensif, dalam perkakasan dan bukannya perisian. Kes ujian kami adalah algoritma pra-pemprosesan imej yang generik termasuk penyelerasan saiz, penapisan hingar dan normalisasi. Bahagian kekusutan dalam modul penapisan hingar telah direkakan sebagai perkakasan manakala modul-modul lain dalam algoritma pra-pemprosesan imej kekal sebagai perisian. Seterusnya, untuk mengesahkan rekabentuk perkakasan / perisian berkenaan, papan *Field-Programmable Gate Arrays* boleh digunakan tetapi proses tersebut mengambil masa yang panjang dan melibatkan banyak kerumitan teknikal. Dalam kes itu, reka bentuk ini menggunakan simulasi perkakasan / perisian dengan teknik antara muka pengaturcaraan langsung (DPI-C) yang membolehkan panggilan fungsi C dari Sistem Verilog dan sebaliknya. Kerja yang dicadangkan telah mengatasi masalah yang dihadapi apabila melaksanakan simulasi bersama berdasarkan simulator Modelsim yang menggunakan antara muka pengaturcaraan langsung teknik (DPI).