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Hybrid DDS-PLL based reconfigurable oscillators with high spectral purity for cognitive radio

Mazumdar, Dipayan

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By
Dipayan(Tim) Mazumdar

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A thesis submitted in partial fulfilment of the University's requirements for the Degree of Doctor of Philosophy

Research carried out at
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CERTIFICATE

*This is to certify that the Doctoral Dissertation titled "**Hybrid DDS-PLL Based Reconfigurable Oscillators With High Spectral Purity for Cognitive Radio"** is a bonafide record of the work carried out by **Mr. Dipayan Mazumdar** in partial fulfilment of requirements for the award of Doctor of Philosophy Degree of Coventry University*

Dec- 2016

Dr. Govind R. Kadambi
Director of Studies
M. S. Ramaiah School of Advanced Studies, Bangalore

Dr. Yuri A. Vershinin
Supervisor
Coventry University, U.K.

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Abstract

Analytical, design and simulation studies on the performance optimization of reconfigurable architecture of a Hybrid DDS – PLL are presented in this thesis. The original contributions of this thesis are aimed towards the DDS, the dithering (spur suppression) scheme and the PLL. A new design of Taylor series-based DDS that reduces the dynamic power and number of multipliers is a significant contribution of this thesis. This thesis compares dynamic power and SFDR achieved in the design of varieties of DDS such as Quartic, Cubic, Linear and LHSC.

This thesis proposes two novel schemes namely “Hartley Image Suppression” and “Adaptive Sinusoidal Interference Cancellation” overcoming the low noise floor of traditional dithering schemes. The simulation studies on a Taylor series-based DDS reveal an improvement in SFDR from 74 dB to 114 dB by using Least Mean Squares -Sinusoidal Interference Canceller (LM-SIC) with the noise floor maintained at -200 dB.

Analytical formulations have been developed for a second order PLL to relate the phase noise to settling time and Phase Margin (PM) as well as to relate jitter variance and PM. New expressions relating phase noise to PM and lock time to PM are derived. This thesis derives the analytical relationship between the roots of the characteristic equation of a third order PLL and its performance metrics like PM, Gardner’s stability factor, jitter variance, spur gain and ratio of noise power to carrier power. This thesis presents an analysis to relate spur gain and capacitance ratio of a third order PLL. This thesis presents an analytical relationship between the lock time and the roots of its characteristic equation of a third order PLL. Through Vieta’s circle and Vieta’s angle, the performance metrics of a third order PLL are related to the real roots of its characteristic equation.

List of Publications Associated with the Thesis

1. Dipayan Mazumdar and Govind R. Kadambi, “Method and Apparatus for Direct Digital Synthesis of Signals Using Taylor Series Expansion”, **U.S. Patent #9100044** B2, Aug. 04,2015
2. Dipayan Mazumdar and Govind R. Kadambi, “Method and Apparatus for Direct Digital Synthesis of Signals Using Taylor Series Expansion”, **U.S. Patent #8570203** B2, Oct. 29,2013
3. Dipayan Mazumdar, Govind R. Kadambi, Yuri A. Vershinin and Imran Rashid, “On the Usage of Hartley Image Rejection Receivers and Adaptive Sinusoidal Interference Cancellation in Automotive Wireless Links”, IEEE Conference on Intelligent Transportation Systems (ITSC), Qingdao, page(s):508-513, October 2014
4. Dipayan Mazumdar, Govind R. Kadambi and Yuri A. Vershinin, “Closed form Expression for Phase Noise, Lock time of a 2^{nd} order PLL and its Optimization”

CONTENTS

Nomenclature

$\phi(t)$ - Instantaneous value of phase perturbation of the frequency source

$S_\phi(f)$ - Power spectral density in dBc/Hz

$S_\phi(\Delta f)$ - Double sided PSD at an offset of Δf

$L_\phi(f)$ - Single sided PSD

s_e - Number of segments per quadrant of DDS

b_n - Fourier coefficient corresponding to the n^{th} -harmonic of DDS

K_V - VCO sensitivity of a PLL

K_ϕ - PFD sensitivity of a PLL

K_{G2} - Gardner sensitivity constant for second-order PLL

K_{G3} - Gardner sensitivity constant for third-order PLL

T_m - Multiplier delay for Taylor Series DDS or Cubic DDS

T_a - Adder delay for Taylor Series DDS or Cubic DDS

k_1 - First order coefficient for Taylor series DDS

k_2 - Second order coefficient for Taylor series DDS

y_k, m_k, p_k, q_k, v_k - Coefficients of Quartic DDS

T_q - Matrix to compute coefficients for Quartic DDS

b_q - Vector to compute coefficients for Quartic DDS (4x1)

z_j - Phase argument to DDS range j is the sample number

$\varepsilon(n)$ - Quantization noise

Δ_P - Phase Quantizer step size originally defined by

$p(n)$ - scaled distance

FZ_SPSR- SPSR computed originally by Flanagan

Mo_SPSR- Modified SPSR expression proposed in this thesis

ω_{LO} - Output frequency of the quadrature oscillator in Hartley suppressor

ω_f - Fundamental frequency of the DDS and input to Hartley suppressor

ω_h - Image frequency of the DDS output, input to Hartley Suppressor

b_I - Amplitude of the sinusoidal interference to LMS-SIC

e_{LMS} - Error in LMS algorithm

$w_{LMS}(n)$- n^{th} iteration of the weight vector in LMS algorithm

$k_{RLS}(n)$- Kalman gain for RLS algorithm

$e_{RLS}(n)$- Error in n^{th} iteration of RLS algorithm

$w_{RLS}(n)$- n^{th} iteration of the weight vector in RLS algorithm

s - Laplace variable for complex frequency

τ - Time Constant of loop filter of second order PLL

ω_n - Natural Frequency of second order PLL

ζ - Damping Coefficient of second order PLL

N - Divide ratio of second order PLL

K_V - Sensitivity of the VCO(Hz/volt)

K_ϕ - Gain of Phase Frequency Detector (PFD)

ϕ - Phase Margin of second-order PLL

$tan\phi$ - Tangent of the Phase Margin of second-order PLL

T_s - Settling Time of second – order PLL

T_d - Sampling Interval of DAC

$k_{i,j}$ - Coefficient of Phase noise for i refers to the power of f^{-1} and j refers to noise source

T_{lock} - Lock Time of second-order PLL

j_n - Period Jitter, difference of the actual period in n^{th} sample with the nominal period

$\sigma_J^2(kT)$- Variance of Period Jitter

k_B - Boltzmann's constant (same symbol used in chapters 4 and 5)

Θ - Angle between two complex poles of second order PLL

c_{WN} - Jitter coefficient for white noise (unit seconds)

c_{FN} - Jitter coefficient for flicker noise (dimensionless)

κ - Figure of Merit of VCO in Mansuri's Model

ΔT - Time Interval in Mansuri's model

T_d - Sampling interval of the ZOH or FOHI DAC

ϕ_{ZOH} - Phase shift due to Zero-order hold DAC

ϕ_{FOHI} - Phase shift due to First-order hold interpolation DAC

θ	-	Phase shift correction (advancement) of analog phase shifters
α	-	Parameters for analog phase shifters
τ_{AP}	-	Time constant of analog phase compensation network
$\angle\phi_{CUMU}$	-	Cumulative for the combination of FOHI DAC, compensator and PLL
$\angle\phi_{FOHI}$	-	Phase shift due to FOHI DAC
$\angle\phi_{COMP}$	-	Phase shift due to analog compensator
$\angle\phi_{PLL}$	-	Phase shift due to second order PLL
s_e	-	Number of segments of DDS
$R2$	-	Series resistance of loop filter
$C2$	-	Series capacitance of loop filter
$C3$	-	Parallel capacitance of loop filter
N	-	Divide ratio of third order PLL
$A0$	-	Sum of capacitances of third order PLL
x_N	-	One of Nickall's parameters for third-order PLL
δ	-	Nickalls parameter for third-order PLL also Half-radius for Vieta's circle
y_N	-	Nickalls parameter for third order PLL
h	-	Nickalls parameter for third order PLL
3θ	-	Vieta's angle – another Nickalls parameter for third order PLL
Δ	-	Discriminant of a third order PLL
G , H	-	Parameters of Cardano for third order PLL
α, β and γ	-	Real poles of a third order PLL
θ	-	Vieta's angle for real poles of a third order PLL
m	-	Parameter of PLL related to Sensitivity of the VCO, PFD sensitivity, Divide ratio (N) and sum of capacitances(A0)
b_c	-	Capacitance ratio of third order PLL, equal to the ratio of time constants
ω_c	-	Loop BW of third order PLL
ω_z	-	Zero of third order PLL
ω_{p2}	-	Higher pole of third order PLL
$tan\phi$	-	Tangent of the PM of a third order PLL
G_{Spur}	-	Open loop gain of third order PLL at comparison frequency
$\frac{P_n}{P_c}$	-	Noise power to Carrier power ratio (dB)

k_B - Boltzmann's constant ($1.38064852 \times 10^{-23}$ m^2 kg s^{-2} K^{-1})

T - Absolute temperature in Kelvin

$\Delta\omega$ - Frequency offset from center frequency

List of Abbreviations

ADC - Analog to Digital converter
BER - Bit Error Rate
CE - Characteristic Equation
CP - Cyclic Prefix
CPE - Common Phase Error
CR - Cognitive radio
CSU - Coefficient Selection Unit
DAC - Digital to Analog converter
DDS - Direct Digital Synthesizer
DSBPN- Double Side Band Phase Noise
EVM - Error Vector Magnitude
FCW - Frequency Control Word
FFT - Fast Fourier Transform
FIR - Finite Impulse Response
FOHI - First-Order Hold Integral
GCD - Greatest Common Divisor
ICI - Inter Carrier Interference
IFFT - Inverse Fast Fourier Transform
IIR - Impulse Response
IMD - Inter Modulation Distortion
IRR - Image Rejection Ratio
ISE - Integral of Square Error
ISI - Inter Symbol Interference
ITAE - Integral of Time multiplied by Absolute Error
LHSC - Linear High Segment Count
LMS - Least Mean Square
LMS-SIC Least Mean Squares- Sinusoidal Interference Canceller
LNA - Low noise amplifier
LO - Local Oscillator

MAE - Maximum Absolute Error

MSE - Mean Square Error

NCO - Numerically Controlled Oscillator

NF - Noise Figure

NTF - Noise Transfer Function

OFDM - Orthogonal Frequency Division Multiplexing

PA - Power Amplifier

PAC - Phase to Amplitude Converter

PACC - Phase ACCumulator

PCB - Polynomial Computation Block

PCU - Polynomial computation unit

PDF - Probability Density Function

PFD - Phase Frequency Detector

PID - Proportional Integral Derivative

PLL - Phase Locked Loop

PM - Phase Margin

PSD - Power Spectral Density

RLS - Recursive Lest Squares

RLS-SIC - Recursive Least Squares – Sinusoidal Interference Canceller

RMS - Root Mean Squared

RSRP - Reference Signal Received Power

RSSI - Received Signal Strength Indicator

SCMF - Sine-Cosine Mapping Function

SDR - Software Defined Radio

SFDR - Spurious Free Dynamic Range

SNR - Signal to Noise Ratio

SpSR - Spurious to Signal Power Ratio

SSBPN - Single Side Band Phase Noise

VCO - Voltage Controlled Oscillator

ZOH - Zero Order Hold

CHAPTER 1 Introduction

The special significance attributed to the introductory chapter stems from its emphasis on the relevance of the thesis. To be more precise, it discusses the preamble, the background, the relevance of the thesis's topic in the contemporary status of research, the motivation for the research of the thesis, and the research questions to be addressed. Those questions lead to the understanding of the thesis's objectives and its organization.

Over the past three decades, despite all the technological advancements in multiple disciplines of wireless communication, bandwidth remains a factor that still determines both the efficiency of system performance and operational effectiveness of service providers. The term *bandwidth*, when referred to wireless communication must be viewed both from the perspectives of allocation and utilization of spectrum. Allocation of spectrum for commercial communication system applications is the prerogative of the both the national and international regulatory bodies. In addition to allocation of frequency spectrum, equally important aspect in wireless communication is utilization or full utilization of an allocated spectrum. A prominent research domain which addresses the theme of spectrum utilization is Software Defined Radio (SDR) or Cognitive Radio (CR). This thesis addresses the significant issues pertaining to Direct Digital Synthesis (DDS) and Phase Lock Loop (PLL), which constitute two important subsystems of CR.

1.1 Introduction to SDR and CR

This section is an introductory discussion on SDR and CR highlighting their relevance in meeting the ever-increasing demand for bandwidth of modern wireless communication systems.

SDR is a term coined by [Mitola, 1999]. It refers to a radio transmitter and receiver whose modulation technique, gain, noise level, center frequency and number of carriers are all controlled by software. A simple block diagram of an SDR radio is illustrated in Figure 1.1.

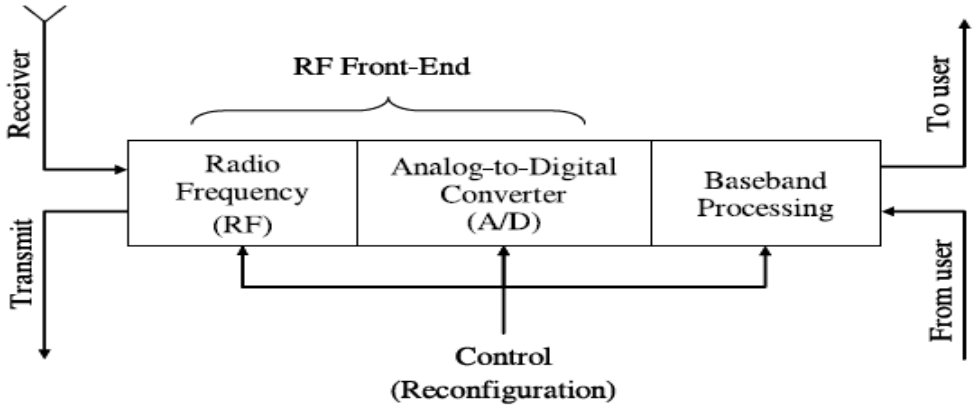


Figure 1.1 Simple Block diagram of SDR

The simple block diagram in Figure 1.1 illustrates three main blocks of a SDR radio. The SDR radio is connected to transmit and receive antennas that can be a common antenna. It comprises a RF portion which performs power amplification for transmission, frequency translation for transmission, frequency translation for reception and power amplification for reception of RF signals. In a typical receiver, the RF portion comprises of software controlled analog circuits. The RF portion is connected to a digital baseband processing block through an Analog-to-Digital Conversion (ADC) block. The ADC block converts analog data from the RF block into digital sampled data for further processing by the baseband section (reception side). The SDR radio also includes a Digital to Analog Converter (DAC). The DAC converts the digital based band signal into an analog format for further processing by the RF portion (transmission side). The baseband processing block is under software control. This block performs demodulation, carrier tracking, symbol tracking, error detection and correction as well as framing and de-framing.

CR technology is an approach to achieve improved efficiency of bandwidth usage in a crowded radio spectrum. CR utilizes a baseline software created for SDR. Radios design based on CR technology senses un-utilized slots (holes) in the spectrum and effectively frequency hop to the unutilized slots. A frequency synthesizer based on DDS will allow a CR receiver to rapidly switch operating frequency band. Current DDS oscillators have limitations on their maximum operational frequency range and spectral purity.

1.2 Spectrum Sensing Receivers and DDS-PLL

CR has been defined by its inventor [Mitola, 2000] as a radio unit that can adapt to frequencies of operation by sensing the unutilized licensed spectrum (termed as spectrum holes), as well as the modulation techniques in real time. There are four major features previously identified by the inventor of CR in order to determine a device that can be referred to as a CR. These features are:

1. The ability to achieve frequency agile operation utilizing spectrum usage information to locate gaps or 'holes' in the spectrum usage in a specific location
2. Dynamic Frequency Selection (DFS) – CRs have software and hardware support to search for holes in the frequency spectrum
3. Incorporate Adaptive Modulation (AM) circuits – the Modulation techniques utilized by CR transmitters must feature flexible modulation methods, the specific chosen method being dependent on a preset Bit Error Rate (BER) for a channel and considering dynamic time varying channel models. The modulation technique used is a function of energy per bit to noise ratio ($\frac{Eb}{N0}$) where Eb is the signal magnitude and $N0$ is the noise level
4. Dynamic Transmit Power Control is aimed at controlling the BER, transmit power, channel characteristics, which are dependent on the carrier frequency and modulation technique. The CR transmitters utilize dynamic power control to achieve a prior set minimum ($\frac{Eb}{N0}$) to meet specified BER requirements for a channel

The CR device switches its operational carrier frequency, channel bandwidth and modulation methods as per available spectrum. It continually senses Reference Signal Received Power (RSRP) and Received Signal Strength Indicator (RRSI). This ensures that a properly designed CR operates in frequency bands where no other transmitter is operating. Once a CR transmitter or receiver is powered or turned on, its modulation technique can be dynamically altered depending on channel conditions. In addition to utilizing a baseline software created for SDR, CR also adds additional features for smart sensing of spectrum, BER and power levels. The noise floor (N_{floor}) of radio receiver is defined as the minimum level of received signal below which transmitted signals cannot be detected irrespective of the method of tuning the receiver. The same unit can be operated with a high noise floor or a low noise floor merely by re-programming the unit. The software in a CR

radio defines the parameters of operation as and when the user moves from place to place. Different locations produce wide variations in amplitude of received signal and the CR unit can alter its own RF system parameters to account for wide variations in channel conditions. In the US the development, CR was led by the Federal Communication Commission (FCC), which has addressed the research on the commercial applications of CR technology. Defense Advanced Research Projects Agency (DARPA) has also carried out research on the military applications of CR.

A CR or SDR requires a frequency source to down-convert or up-convert signals. Down conversion occurs when an incoming RF signal is combined with the output of local frequency producing source (usually termed as Local Oscillator (LO)) to produce sum or difference signal using a non-linear device called an RF mixer. The RF mixer must be excited at least in one port by source for the generation of a local frequency. In frequency domain, the random fluctuations or variations of phase of a signal are known as phase noise. The time domain equivalent of phase noise is known as jitter [Rubiola, 2007].

The primary focus and emphasis of the research proposed in this thesis are on the design and architecture of the source for generation of local frequency in a RF mixer. DDS-PLL is a type of frequency synthesizer that has many of the characteristic features required from a source for generation of local frequency or LO in CR. These features include:

1. Ability to alter the frequency very fast – within 100 µs and even below 10µs
2. Low frequency step size, which is especially useful in systems such as GSM as small as 200 kHz
3. Suppression of DDS generated spurs (spurious frequencies) and PLL generated spurs. Practically all communication standards benefit by operation with no spurs

A frequency source for a SDR or CR must have the following characteristics listed in Table 1.1 [Aktas and Ismail, 2004]. Table 1.1 illustrates the frequency bands and phase noise requirements for several standards. Standards such as Wi-Fi and UMTS specify the maximum allowable phase noise at a given frequency offset. Only Mobile Wi-Max standard provides the time domain specification of jitter variance. The two standards in frequency domain or time domain are interchangeable through the usage of the Fourier integral taken over the BW of receiver channel. They are also compared with respect to settling time which provides a strict upper bound for the

oscillator to switch frequencies. The channel width would impose a limitation on the 3 dB points of an oscillator.

Table 1.1 Oscillator requirements for some wireless communication systems

Standard	Frequency B and (MHz)	Phase Noise (dBc/Hz)	Settling time for channel switching (μs)	Channel width (MHz)
GSM	880-960 1710-1880	-122@600KHz -132@1.6MHz -139 @3 MHz	577 (GSM) 150 (GPRS)	0.2/0.2
UMTS (FDD/TDD)	1920-2170 1900-2025	-132@3 MHz -132@10 MHz -144 @15 MHz	200	5/0.2
Bluetooth	2402-2480	-84@1 MHz -114@2 MHz -129 @3 MHz	150	1/1
Mobile WiMAX 802.16e	2300-2400 2305-2320 2469-2690 3300-3400 3400-3800	Phase Jitter < 1 degree rms	<100(HFDD)	3.5-10/0.25
Wi-Fi IEEE 802.11a	5150-5350 5470-5825	-102@1 MHz -125 @ 25 MHz	500	20/20
Wi-Fi IEEE 802.11b	2412-2472		225	20/5
Wi-Fi IEEE 802.11g	2412-2472		225	20/5

Table 1.1 requires frequency step sizes of an oscillator to be 10^{-4} or better. For future requirements a step size of 10^{-6} or better is desirable. DDS based oscillators have the promise of very small step size that is even below 10^{-6}. This is accomplished by having a wider phase word size of phase accumulator in DDS.

1.3 Role of Frequency Sources in RF receivers

A combination of LO and RF mixer is used to enable radio receivers to down convert carrier frequency information into base band for further processing. On the transmitter side, up conversion converts baseband information into carrier frequencies. The frequency down or up conversion is performed by a non-linear three port device called a mixer which generates sum or difference of the two input frequencies. The down conversion mixer has two input ports; one connected to the antenna and the other energized by LO. The mixer has a single output port which provides the sum or difference of the two frequencies. The topic of this research is the frequency source which energizes the LO port of RF up-conversion or down-conversion mixer. Every frequency source has some level of random fluctuations in its amplitude and phase. The random phase fluctuations have been known to affect operation of receivers. Random phase fluctuations affect the operation of devices such as radio receivers, radio telescopes, spectrometers and laser power detectors.
The mixer is a device used to perform frequency translation in a radio receiver. At the transmitter side, incoming signal from a DAC and power amplifier is up converted to a higher frequency. The corresponding device is called an up-conversion mixer. At the receiver side, a Low Noise Amplifier (LNA) amplifies the incoming signal from the antenna. In turn, a down-conversion mixer down-converts this signal to a lower frequency.

1.4 Motivation for Research

Spectral purity of DDS and PLL is very significant for operational efficiency and Quality of Service (QoS) of CR. In DDS and PLL, the spectral purity is addressed through a term called Spurious Free Dynamic Range (SFDR). SFDR is defined as the logarithm of ratio of amplitudes

of the signal at the fundamental and the maximum of all subsequent harmonics. Apart from the SFDR, phase noise, lock time and frequency step size, another factor that is important is Phase Margin (PM). PM is defined as the excess phase of the system when the forward gain is unity.

For the analysis of SFDR performance of DDS, the DDS is treated as a polynomial with fixed coefficients and a quadrant of a sine wave output is divided into several segments. The analysis of DDS reveals that DDS architectures that utilize higher order polynomial interpolation exhibit significantly better SFDR that those that utilize lower order polynomial interpolation. Also, for the same order of polynomial of a DDS it has been postulated that greater the number of segments per quadrant of sine wave better(higher) the SFDR. The conventional architecture of DDS does not permit the change of segments in the design at will and therefore the number of segments must be fixed at the time of finalizing the architecture. The commonly referred nomenclature of DDS architecture are quadratic (Taylor Series), cubic polynomial based (third order) and quartic (fourth order). A significant contribution in the analysis of DDS is reported by (De Caro and Strollo, 2005). However, their approach was valid only for cubic polynomial based DDS. It cannot be applied to quartic DDS (fourth-order). For a given architecture of DDS, an avenue to improve its SFDR is to invoke dithering or spur suppression schemes. However, with the conventional dithering schemes, the improvement in SFDR is associated with a raise in noise floor of the signal spectrum.

Similarly, PLL can be analyzed as a system of defined order like 2^{nd} order or 3^{rd} order. Majority of the analysis of PLL is through its transfer function. It would involve parameters of PLL such as the sensitivities of Voltage Control Oscillator (VCO) and PFD, time constant of loop filter and capacitance ratio. However, the analysis of PLL through solution of Characteristic Equation (CE) derived through the order of PLL can lead to relationship between performance metrics of PLL and the location of poles of PLL.

The design of PLL to make it achieve to very small frequency step is also one of the important requirements for its utility in CR. The concept of Diophantine Frequency Synthesis (DFS), which involves multiple PLLs can result in an impressively small frequency step. However, the presence of multiple PLLs in DFS has deleterious effect of a higher level of phase noise. Reduction of phase noise of DFS must be addressed through schemes to reduce the phase noise of the VCO or the pre-dividers.

From the discussions presented thus far, the following key points emerge as consequential and significant for further research.

1. CR is an emerging and evolving technology. It has a great potential to address the prevalent constraint on limited bandwidth by utilizing the instantaneous unutilized spectrum in a given location almost in a real time;
2. The utility and operational efficiency of CR depend upon the rapidity with which the CR radio can adapt to the unutilized licensed spectrum;
3. The bandwidth efficiency of CR also can be improved by the minimum step size of the frequency of operation to use the unutilized spectrum so that many CR users can have access to the same unutilized spectrum of the same frequency band;
4. Phase noise, spur levels and locking time are important attributes for satisfactory operation of CR;
5. DDS, DAC and PLL form critical subsystems of CR;
6. Satisfactory performance of DDS and PLL from phase noise perspective will ensure spectral purity at the output of PLL for CR;
7. Individual lock time of DDS, DAC and PLL determines the effective lock time of CR;
8. CR comprises a cascade of DDS, DAC and PLL implying the degradation in spectral purity of the preceding block affects the spectral purity of next block. Frequency spurs generated by the DDS should not get amplified by the PLL;
9. Spectral purity of DDS can only be a necessary condition;
10. Spectral purity of DDS as well as PLL is a sufficient condition;

1.5 An Overview of Succinct Research in DDS-PLL

An overview of some of the key research publications that serve as a basis on based on which the aim and objectives of the proposed thesis have been formulated is presented in this sub section. [Vankka, 2000] had designed Taylor series DDS but the limitation of his DDS design is that its throughput was limited due to a pipeline requiring two adders and one multiplier. The limited throughput and increased power dissipation are due to the presence of a multiplier. Vankka has not focused on the computation of SFDR for a Taylor series DDS or any other polynomial based

DDS. He also does not provide the results for the Maximum Absolute Error (MAE) of Taylor series DDS.

[Ashrafi, 2000] has not provided any reasoning or basis for the realized SFDR of 117 dB for the DDS design. His design features a critical path length of 2 multiplier delays combined with 3 adder delays. He has not attempted to reduce the critical path length substantially.

[Fanucci, 2000] has proposed a Quadratic DDS. But his paper does not address the schemes either to reduce the dynamic power or to optimize the quadratic DDS for maximal SFDR.

[De Caro and Strollo, 2005] proposed a theory of cubic polynomial based DDS. They have provided an approach for deriving the coefficients of a DDS with a bounded number of segments. Their results have not been extended to Taylor series-based DDS. Their results do not cover Quartic DDS as well. They have not performed a comparison of MAE for various types of DDS such as cubic polynomial based DDS, Taylor Series DDS, Quartic DDS and Linear High Segment Count (LHSC) DDS.

[Storiadis, 2003] has provided a design to perform Diophantine Frequency Synthesis (DFS). DFS provides very small frequency step size of 1 in 10^5, which conventional fractional N PLLs cannot achieve. However, his proposed DFS arrangement will invariably lead to high levels of phase noise due to two pre-dividers and two VCOs. He has not provided a means to reduce the phase noise of the VCO or the pre-dividers.

[Banerjee, 2006] has provided expression for the magnitude of spurs in PLL generated by leakage current as well as for spurs generated by mismatches. The limitation is that it has not related the spur magnitudes with poles of a 3rd order PLL. He has provided expressions for PM of a third order PLL but has not related the PM to values of the poles of a third-order PLL.

[Mansuri, 2002] has provided expressions for Jitter variance of a second- and third-order PLLs. He has not related the PLL parameter to the poles of a third-order PLL.

[Lam and Razavi, 2000] provided an expression to compute the ratio of the noise power to carrier power of a 3rd order PLL. They have not related it to the loop bandwidth or the poles of the 3rd order PLL.

[Dorf, 2005] has provided the 'Integral of Time multiplied by Absolute Error' (ITAE) criterion for optimal error of a third-order system. But he has not illustrated its application of this generic concept to a third-order PLL. He has also not addressed the calculation of PM of such a PLL.

[Gray and Stockham, 1993] have provided two important theorems on dither addition to a quantizer. They have provided conditions of the Characteristic Function (CF) of added dither. However, there is no discussion on application of their theorems for the improvement of the SFDR of a DDS with added amplitude dither. They have also provided relationships between the quantization error and input signal. But their theorems cannot be applied easily to an amplitude dithered DDS.

[Flanagan and Zimmerman, 1995] presented a scheme to compute the Spurious to Signal power Ratio (SpSR) for a DDS to which a random phase dither signal has been added. Their results for SpSR include only the first and second order moments of quantization error. Their paper does not consider higher order moments such as third order of the quantization error. The paper does not provide a scheme to improve the SFDR of a DDS without adversely raising the noise floor.

1.6 Research Questions

Based on the discussions presented in the previous sections, the following questions have emerged when viewed with a perspective of seeking solutions or answering the important and relevant questions/issues pertaining to the broad domain of DDS- PLL combination.

- What modifications in the architecture of conventional Taylor series-based DDS are needed for the reduction of the critical path without the degradation of its SFDR?
- Is it possible to extend or modify the analytical formulation by (De Caro and Strollo, 2005) for the computation of SFDR of cubic DDS to Taylor series-based DDS and quartic DDS?
- Is it feasible to arrive at a switchable DDS configuration to facilitate realization of a range of pre-selected SFDR from a single DDS architecture with a feature of higher efficiency of dynamic power?
- Is it feasible to formulate a scheme for design of DDS combined with a PLL which features low frequency step size and low phase noise?
- Are there low power alternatives to the conventional dithering scheme for the suppression of spurs of DDS without significant degradation of noise floor?
- For a second-order PLL is it possible to relate phase noise, lock time and phase margin in a single analytical expression? In the same way is it possible to relate a phase noise or jitter to stability of the PLL?

- For third-order PLLs with real roots or complex roots is there a geometric way that the PLL can be represented and what is the relationship between the phase margin and the root locations?
- Is it possible to relate performance of PLL such as Jitter and spur gain to the roots of its Characteristic Equation (CE)?
- Is it possible to apply some classical control system criterion to design an ideal third-order PLLs?

1.7 Objectives of Research

This thesis proposes to explore solutions or answers to the aforementioned research questions with a perspective to facilitate original contributions to the domains of DDS, as well as Spur suppressions schemes applicable to DDS and PLL. The aim of this research is to design and demonstrate hybrid Direct Digital Synthesis-Phase Locked Loop (DDS-PLL) based reconfigurable oscillators featured with high spectral purity for CR. The specific objectives of this thesis are:

1. To develop re-configurable Direct Digital Synthesis (DDS) oscillators with greater ROM compression, lower power and enhanced spectral purity;
2. To develop re-configurable dithering schemes that enhance spectral purity of the waveform at the input to the Digital to Analog Converter (DAC) of DDS oscillators;
3. To design architectures for hybrid DDS-PLL based re-configurable oscillator featured with minimum latency, step size, maximal bandwidth and high spectral purity for cognitive radio;
4. To develop the designed hybrid DDS-PLL based re-configurable oscillator and demonstrate their performance over the GSM to WLAN range using FPGA.

The research attempts to provide theoretical relationships that are useful for the DDS-PLL designer an allow trade-off of lock time versus phase noise. The outcome of these expected results is new types of PLLs where the phase noise is tightly bounded for a given Lock time. Therefore, the proposed research title Hybrid DDS-PLL Based Reconfigurable Oscillators with High Spectral Purity for Cognitive Radio is justified**.**

1.8 Original Contributions

Following is list of significant original contributions emerging out of the research studies presented in this thesis.

- Two US patents have been granted for the architecture of the Taylor Series DDS. US patent numbers U.S. Patent #9100044 B2, Aug. 04,2015 U.S. Patent #8570203 B2, Oct. 29,2013
- A Hartley spur suppressor has been proposed to improve the SFDR of a DDS with a poor SFDR. The resultant SFDR is improved from 74 dB to about 120 dB by using a Hartley spur suppressor. An adaptive notch filter based on LMS or RLS has been proposed in the Hartley spur suppressor. The additional power required is only 100 mW.
- A more accurate expression for the signal to total interference ratio SPSR of a phase noise dithered DDS has been derived for the first time. It is a correction to the expression originally proposed by [Flanagan and Zimmerman, 1995] which considers higher order moments;
- A new analytical expression for phase noise of a second-order PLL in terms of its PM has been derived for the first time;
- A new analytical expression has been derived for the derivative of lock time with respect to the damping coefficient. The expression explores the dependence of lock time variance on the PM of a second-order PLL;
- A differential expression is derived linking the lock time and PM of second-order PLL;
- Phase noise of a second-order PLL has been related for the first time to its lock time and PM in Chapter 4. This is an important new expression derived in chapter 4;
- New analytical expression has been derived to relate the Jitter variance of a second-order Type II PLL and PM. This allows the trade-off of Jitter variance with PM of the second-order PLL. It is an important contribution of chapter 4
- A new analytical relationship between the Jitter variance and PM of a second-order PLL has been derived;
- Analytical relationship between the angle between the two complex poles and the PM of a second-order PLL has been derived for the first time;
- New methods of correcting the phase shift due to DAC and due to PLL using a digital phase shift correction filter have been proposed in this thesis;

- For the case of three real poles of a third order PLL, a new equation which relates between the PM and Vieta's angle has been derived for the first time;
- A new expression for the noise power to the carrier power ratio in terms of poles and another one in terms of the loop BW has been derived for the first time in chapter 5;
- A new expression for the lock time of a third-order PLL has been derived for the first time in this thesis using Vieta's circle half radius and Vieta's angle. It relates roots of CE of PLL to the lock time.

1.9 List of Publications

1. Dipayan Mazumdar and Govind R. Kadambi, "Method and Apparatus for Direct Digital Synthesis of Signals Using Taylor Series Expansion", U.S. Patent #9100044 B2, Aug. 04, 2015.
2. Dipayan Mazumdar and Govind R. Kadambi, "Method and Apparatus for Direct Digital Synthesis of Signals Using Taylor Series Expansion", U.S. Patent #8570203 B2, Oct. 29, 2013.
3. Dipayan Mazumdar, Govind R. Kadambi, Yuri A. Vershinin and Imran Rashid, "On the Usage of Hartley Image Rejection Receivers and Adaptive Sinusoidal Interference Cancellation in Automotive Wireless Links", IEEE Conference on Intelligent Transportation Systems (ITSC), Qingdao, page(s):508-513, October 2014.

1.10 Organization and Outline of the Thesis

The thesis is organized into seven chapters and a brief description of the individual chapters is as follows.

Chapter 2: This chapter introduces the architecture of the DDS-PLL. A discussion on basic parameters of DDS and PLL as well as the succinct review of relevant research publications on DDS and PLL are presented in this chapter.

Chapter 3: This chapter discusses the improvements to a Taylor series-based DDS for reduced dynamic power and multifold increase in throughput. These improvements provided the basis for the two granted US patents. The chapter analyzes new and alternate spur suppression schemes based on Hartley image reject architecture and LMS-based sinusoidal interference suppression schemes. This chapter describes the computation of the SFDR of a Taylor series DDS and LHSC DDS using the framework provided by [De Caro and Strollo, 2005]. This chapter also compares the MAE of four different DDS designs having the same number of segments per quadrant. A new expression for Signal to Spurious Ratio (SpSR) has been derived by considering the higher order moments.

Chapter 4: This chapter explores analytical relationships of a second order PLL. It includes numerous new analytical formulations which have not been addressed in prior literature. It presents a formulation of the relationship between settling time of a second order PLL and its VCO sensitivity for a fixed PM. A new analytical expression for the cumulative phase noise at the output of the second-order PLL in terms of PLL parameters is derived. A closed form expression for the variance of lock time with respect to damping coefficient is derived as a function of loop BW and damping coefficient. A closed form expression for the variance of lock time with PM is derived for the first time. One of the important contributions of this thesis is a relationship between the phase noise and the PM of a second-order PLL presented in this chapter. Analytical relationships between jitter variance and PM are derived in this chapter for Type I and Type II second order PLLs. A relationship between the PM and the angle between two complex poles is derived in this chapter.

Chapter 5: This chapter presents analytical results on the location of three real poles of a third order PLL and its relationship with PLL parameters such as VCO sensitivity, capacitance ratio, capacitance of loop filter and divide ratio. This chapter also discusses new analytical relationship between the PM and the capacitance ratio of a third-order PLL with real roots. The time domain response of a third-order PLL with three real and equal roots is discussed in this chapter. It includes a discussion on the characterization of the jitter variance with the overshoot of a third-order PLL. A new expression is derived to relate the ratio of the noise power and the carrier power of a third-order PLL to VCO sensitivity, capacitance ratio and the algebraic sum of the three poles. An equation relating the ratio of the noise power and the carrier power to the real roots and loop BW

of a third-order PLL is presented in this chapter. This chapter also contributes a closed form expression for a relationship between the poles of a third-order PLL and its lock time.

Chapter 6: This chapter presents implementation of various design configurations of DDS proposed earlier in chapter 3 using Xilinx Virtex6 FPGA. This chapter compares the dynamic power and SFDR of various design configurations of DDS. FPGA implementation as well as comparison of dynamic power of Hartley spur suppressor and the spur suppressor using LMS based adaptive notch filter are also covered in this chapter.

Chapter 7: This chapter highlights the summary of the research presented in this thesis based on the arrived conclusions, as well as the inferences derived through a combination involving analytical formulation and simulation results. This chapter also proposes suggestions for future research work to further the envisaged orientation or scope of the research presented in this thesis.

Chapter 2: A REVIEW OF THE PRINCIPLES OF DDS-PLL MODULES AND ITS COMPONENTS

This chapter deals with the background theory necessary to appreciate the functional principles and theoretical concepts of DDS and PLL which constitute the research topics of this thesis. A brief discussion on the functional block diagram of Software Defined Radio (SDR), phase noise and significance of quadrant symmetry in DDS is presented in this chapter. Besides, this chapter also covers a preliminary discussion on the performance metrics of DDS such as SFDR, MAE and SpSR. This chapter also highlights the functional principles and the key components of PLL through functional block diagram. Requisite technical details on the role of PFD, VCO, Loop filter and divider in PLL are described in this chapter. The definition and significance of spurs, overshoot and stability criterion of PLL are also presented in Chapter 2. Chapter 2 also includes a succinct review of relevant and significant prior research studies on second and third-order PLLs, DDS and notch filters from the perspective of the research proposed in this thesis. The organization of this chapter is as follows:

Section 2.1 illustrates the position and connectivity of the DDS block within the broad architecture of SDR. It also discusses the sub-components of DDS and PLL combined architecture, such as PACC, Phase to Amplitude conversion and DAC. Section 2.2 discusses the concept of phase noise and the rationale for its reduction in the design of DDS. Section 2.3 presents the details on quadrant symmetry and segmentation in the design of DDS.

Sections 2.4 and 2.5 explain the SFDR and MAE as performance parameters of DDS. In turn, Section 2.6 describes another important performance parameter of DDS - namely SpSR. Section 2.7 discusses the concept of PLL and the stability criteria associated with PLL. Section 2.8 presents a discussion on spurs in PLL. Section 2.9 deals with overshoot in PLL. Section 2.10 presents a succinct review of prior research pertaining to various orders of PLL and DDS. Finally, a summary of chapter 2 is presented in Section 2.11.

Chapter 2 discusses key theoretical concepts like SFDR, MAE, phase noise, cubic and quartic DDS and provides some insight into the prior literature and patents.

2.1 System level block diagram for SDR

This section presents the generic functional block diagram of a SDR, as well as the associated digital as well as analogue functions, to be performed in a SDR It also presents the role and significance of DDS and PLL in a broad architecture of SDR.

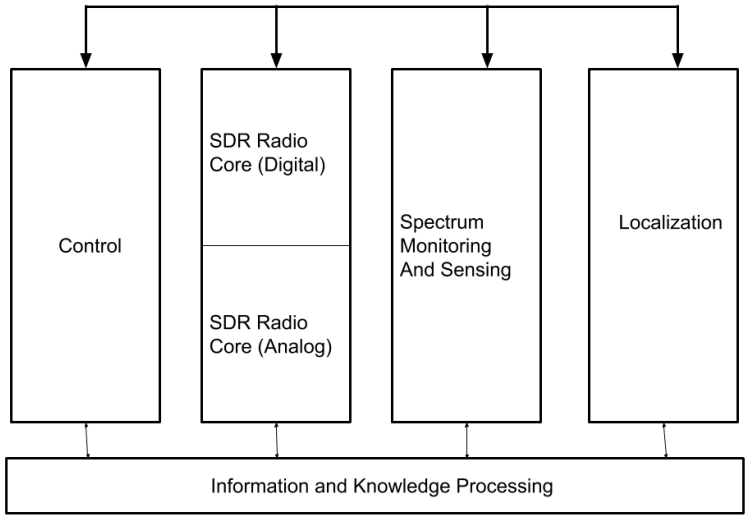


Figure 2.1 Generic block diagram of SDR.

Figure 2.1 is a block diagram for a complete SDR system which performs a complex list of digital and analog functions. The digital functions, such as spectrum monitoring, energy sensing, localization, demodulation and decoding, are not relevant to this thesis. The top-level Cognitive Radio block diagram is following [Jondral, 2015]. For this thesis the only relevant sub-block in the block diagram of Figure 2.1 is the SDR radio core-Analog. Within the SDR radio core, are the transmit and receive chains. The receive chain is further detailed in Figure 2.2, following [Abidi, 2007], it comprises a receive antenna which receives Radio Frequency (RF) energy. The RF signal is amplified by the Low-Noise Amplifier (LNA) block. The output of the LNA block is passed to the mixer or down-conversion mixer. The down-conversion mixer is a three-port device – it has an RF port, a Local oscillator port and an output port - Intermediate Frequency (IF) port. The RF port receives the amplified RF output of the LNA. In turn, its local oscillator port receives the output of a stable local frequency source called the Generic Local Oscillator. The mixer output is

further amplified by an IF amplifier (identified in Figure 2.1). The IF amplifier output forms the input to the Analogue to Digital Converter (ADC). The ADC output is further processed by a Baseband processor. This thesis is concerned only with the block entitled Generic Local Oscillator. The block in Figure 2.2 titled Generic Local Oscillator (GLO) is further expanded in Figure 2.3 where it shows the DDS part and PLL part clearly separated.

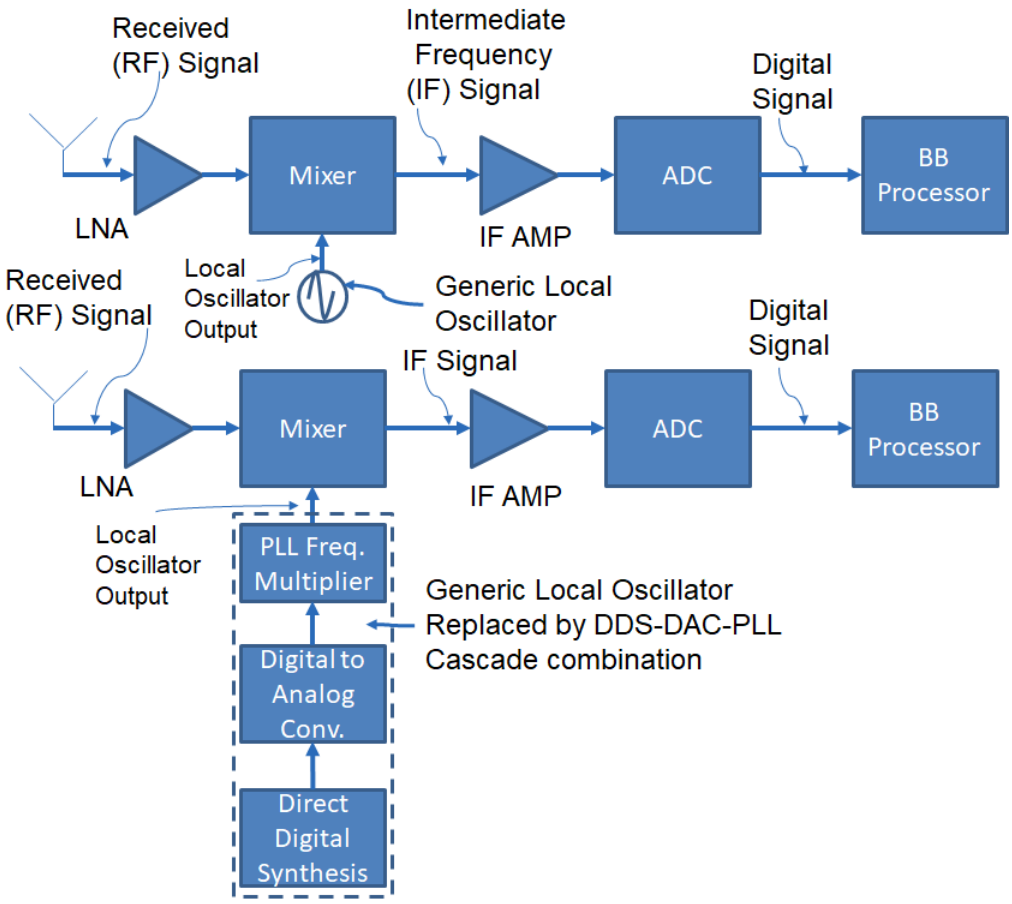


Figure 2.2: The Generic Local Oscillator is replaced by short form of the DDS-PLL block.

In Figure 2.2 the GLO is illustrated further and subdivided into three sub-blocks. The first block is the DDS block, which produces an ideal sinusoid of pre-determined frequency and phase. Its output is fed to the Digital to Analogue Converter (DAC). The DAC converts the digital sinusoid into and analog signal. The output of the DAC is frequency multiplied by the block named “PLL Frequency Multiplier”. Figure 2.3 provides further details of the DDS-DAC-PLL block.

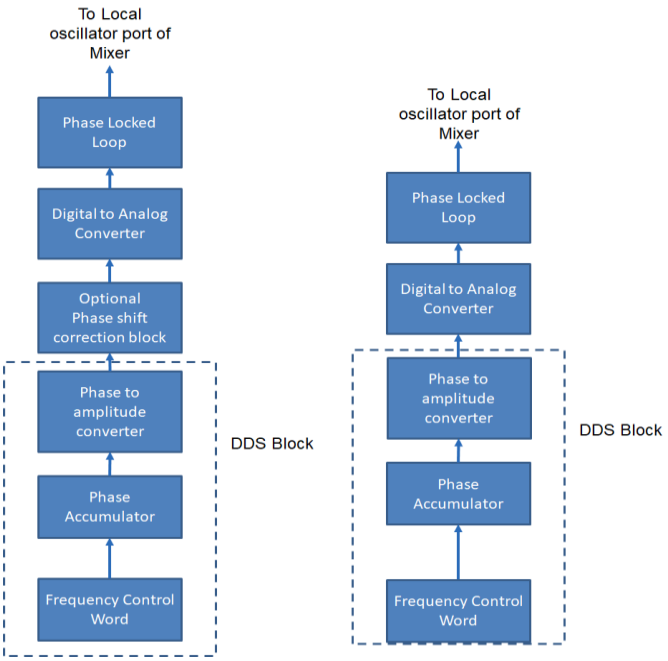


Figure 2.3 a **Figure 2.3b**

Figure 2.3 Comparative DDS-PLL blocks

Figure 2.3a illustrates that the DDS block is further decomposed into three sub-blocks. The Frequency control word block is used to produce a frequency word which is the minimum frequency step. The output of the Frequency control block is fed to the Phase Accumulator (PACC) block. The phase accumulator uses the frequency step information and produces of digital phase word representing a phase angle between 0 and 2π. The output of the PACC block feeds the Phase to Amplitude Conversion (PAC) block, which converts a digital phase word of fixed width into the amplitude of a sinusoid.

The output of the DDS block is the amplitude of a sinusoid. The phase shift of sinusoid is phase corrected (a programmed positive phase shift is added to the DDS output) by the "Optional phase shift correction block". The phase shift corrected output is fed to a DAC of sufficiently high sampling rate. Figure 2.3b does not have the optional Phase shift correction block. The phase shift correction block will not be found in previous references as its inclusion is an idea that emerged out of this thesis. Previous authors on DDS-PLL such as [Gentile,2006] and [Vankka,2002] do not include the phase shift correction block. The inclusion of phase shift block is an idea that has emerged out of this thesis. It was done totally as an independent idea.

The analog output of the DAC is fed to the input of a PLL. The PLL frequency multiplies the DAC output. The PLL output is a frequency multiplied version of the waveform at the DAC output and fed to LO port of the Mixer (Figure2.2). The same mechanism is followed whether the PLL output is fed to a down conversion mixer or a up conversion mixer. In this thesis the terms DDS-PLL and DDS-DAC-PLL are used interchangeably.

2.2 Phase Noise and its Spectra

Phase noise of an oscillator can be considered as a distribution of energy around its center frequency. A greater level of phase noise is said to exist when there is more energy in the spectral bands closest to the center frequency. If the level of phase noise at the output of the DAC-PLL is too high, the noise distribution can mask the presence of a desired received signal. Therefore, lowering the level of phase noise is a goal in design of DDS-PLL.

The voltage of an oscillator in the presence of both random variations in amplitude and phase can be represented as

$$V(t) = (A + v(t))cos(2\pi f_0 t + \phi(t)) \tag{2.1}$$

In Equation (2.1), A is the Unperturbed amplitude of the original frequency synthesizer source. Random variable $v(t)$ is the Random amplitude variation of the frequency synthesizer source. Frequency $f_0$is the Design frequency (Fixed) of the synthesizer source. $\phi(t)$ is the instantaneous value of phase perturbation of the frequency synthesizer. Phase noise arises because of the randomness of $\phi(t)$.

The energy due to the phase perturbation term can be written as a square of the magnitude of Fourier Transform of the auto-correlation function of the phase variation. The spectral density of any signal is written as

$$S_\phi(f) = |F(\phi(t)|^2 \tag{2.2}$$

In Equation (2.2) F is the Fourier Transform operator. The variable $\phi(t)$ is a time-domain random variable representing phase noise. $S_\phi(f)$ is Power Spectral Density (PSD) of phase noise units dBc/Hz.

Phase noise is only expressed in terms of the PSD. PSD can be defined as the amount of energy dissipated in a 1-ohm resistor using filter with a Band Width (BW) of 1Hz. Variation in PSD with change in frequency is not uniform. PSD of phase noise is used to compute the sensitivity of radio receiver. Typically, PSD for a commercial oscillator is maximum around the center frequency and drops off at frequencies of a higher offset. A PSD spectrum for a commercial source can be divided into regions. Each region has a different dominant mechanism for the generation of phase noise and its level of PSD. An alternative way to express the PSD of phase noise is in terms of a wide array of band pass filters each having BW of 1 Hz. If an infinite array of band-pass filters each with a BW of 1Hz is attached at the output of a frequency source and then the output of each filter is measured for power level, the resulting array would provide a complete PSD of phase noise for a source.

Single Sided PSD of phase noise has been defined formally by [He, 2007]. The single sided PSD ($L_\phi(f)$) is expressed a s a ratio of the noise power contained in a BW of 1 Hz to carrier power as

$$L_\phi(f) = \frac{10\log_{10}\left(P_{noise}(f0+\Delta f, 1Hz)\right)}{10\log_{10}(P_{carrier})} = 10\log_{10}\left(\frac{\left(S_\phi(\Delta f)\right)}{2}\right)\text{dBc/Hz} \quad (2.3)$$

In Equation (2.3), $S_\phi(\Delta f)$ is the double-sided PSD. The Single Side Band (SSD). PSD is indicated by the symbol $L_\phi(f)$. Single Side Band (SSB) phase noise is a measure of the level of phase noise of a frequency source. For the best frequency sources, $L_\phi(f)$ should be below140dBc/Hz.

Phase noise in frequency domain corresponds to Jitter in time domain. The two are related through a Fourier integral relationship, as expressed in Equation (2.4). Jitter is a definite integral of phase noise, which is usually expressed as a variance of a time domain quantity.

$$var(J(t)) = \int_{-B_{sw}/2}^{B_{sw}/2} S_\varphi(f)df \quad (2.4)$$

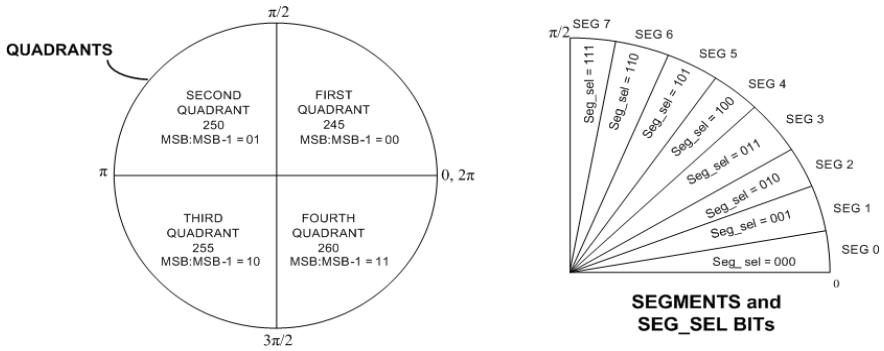
In Equation (2.4) B_{sw} is the Band-width of phase noise under consideration. In turn, $var(J(t))$ is the variance of jitter (time-domain). The integration is performed with frequency offset (f) as a

variable. $S_{\varphi}(f)$ is the power spectral density of phase noise. In practice the variance of jitter can be measured by either one sided or two-sided integration of the area under the phase noise curve ([Rubiola, 2005], [Mansuri, 2002]). The unit of variance is rad^2.

2.3 Quadrant Symmetry and Segmentation in DDS

Quadrant symmetry technique for DDS is well described in the literature [Goldberg, 1999] and implemented in DDS chips. Its advantage is to reduce the silicon die area (due to a 75% drop in memory size for ROM-based DDS), dynamic power and leakage power [Reed, 2000]. For ROM-less DDS, there is elimination of additional HW elements and dynamic power reduction. In a sinusoidal waveform, it is possible to generate the values for all the four quadrants based on the waveform values of a single quadrant [Vankka, 2000]. This is known as quadrant symmetry. A DDS (ROM-based or ROM-less) featuring Quadrant symmetry decomposes the sinusoidal cycle into four quadrants, the waveform is stored or computed for a single quadrant. At appropriate points within the entire range of 2π, the phase and amplitude are inverted in a logical way to ensure all four quadrants can be generated. Quadrant Symmetry minimizes dynamic power, leakage power and die area dues to reduced memory for a ROM-based DDS and reduced HW for a ROM-less DDS.

Segmentation is the process of sub-dividing a quadrant of DDS operation into segments, which is typically a power of two say 32 or 64. The sinusoid is approximated by a cubic or quadratic Polynomial on a per segment basis. Hence, coefficients are calculated for each segment separately to achieve the best approximation.



(a) Quadrant Symmetry **(b) Segment Numbering**

Figure 2.4 Cubic Polynomial DDS

Figure 2.4a depicts the four quadrants used to generate a sinusoidal waveform and the bits used to select each quadrant of a cubic DDS. The Most Significant Bit (MSB) and the second Most Significant Bit (MSB-1) are used to select the quadrant. In Figure 2.4b, each quadrant is shown to be further subdivided into 8 segments. The segments are numbered from 000 to 111. Figure 2.4b illustrates that the "**SEG_SEL**" (SEGment_SELection) bits used to select specific segment of a quadrant. These "**SEG_SEL**" bits are typically a string of upper bits produced by the PACC. Each segment number corresponds to a 3-bit decoder value. The bits that determine the segment number are collectively referred to as the "**SEG_SEL**" bits throughout this chapter.

For a cubic, quartic polynomial based DDS, a quadrant is further sub-divided into segments warranting a distinct polynomial used to compute an ideal sinusoid for each segment. The block diagram of a Cubic polynomial DDS is described in Figure 2.5.

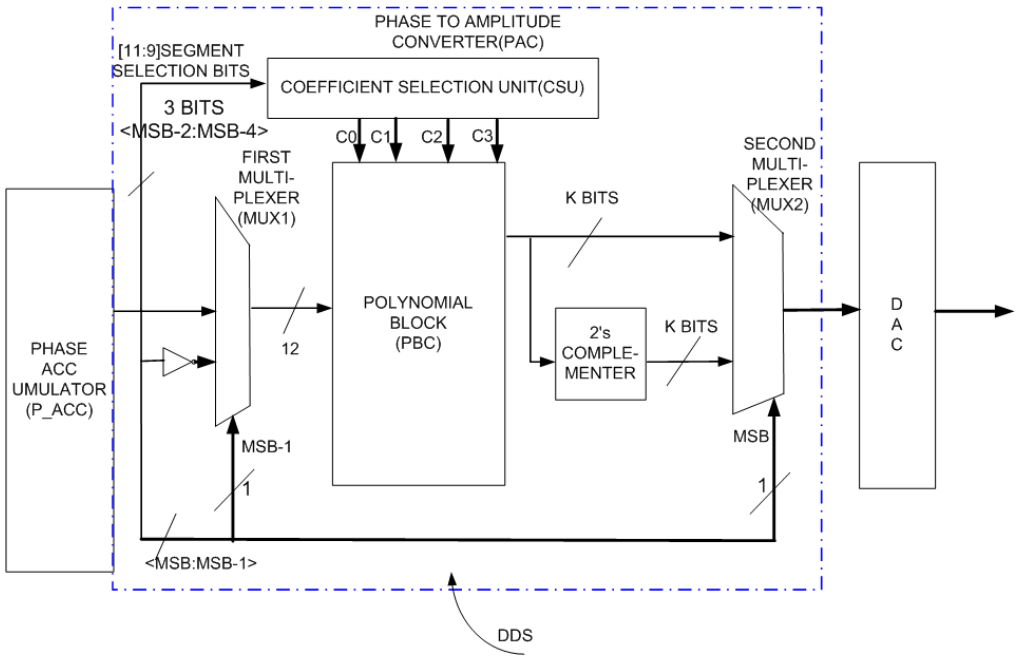


Figure 2.5 Block diagram of Cubic DDS

Figure 2.5 includes the main element of a Cubic DDS including PACC (Phase Accumulator), Coefficient Selection Unit, Polynomial Block and DAC.

In Figure 2.5 the first block of the proposed DDS is the P_ACC or PACC whose function is to generate a 14-bit wide phase word which represents the argument to the sine function, an angle between 0 and 2π. Of the 14-bit output of the PACC, the uppermost bits (bits <13:12>)) are used as control bits of the two multiplexers MUX1 and MUX2. Multiplexers MUX1 and MUX2 enable the cubic DDS to reduce complexity by enabling quadrant symmetry. The next most significant bits, that is the bits 11 through 9 of the PACC are used as Segment Selection (SS) bits by the Coefficient Selection Unit (CSU). The lowest 12 bits of output of PACC and their complements form an input to the first multiplexer (MUX1). The output of MUX1 is fed to the Polynomial Block (PBC)- which performs polynomial computation. The coefficients required by the PBC are fed by CSU. The output of the PBC is fed to a 2's complementer and simultaneously to a second multiplexer (MUX2). The output of the multiplexer MUX2 is fed to the Digital-to-Analog Converter (DAC) block.

Polynomial Block (PBC): To compute each sample of the output of a cubic DDS, three multiplications and a total of four additions must be performed. The PBC (Figure 2.6) uses a three-

stage pipeline to ensure the actual multiplications and additions with the appropriate coefficients in every clock cycle. The interconnections of the PBC comprises three multipliers, three adders and three registers structured in a three-stage pipeline, as shown in Figure 2.6. Including the phase accumulator and the final register at the DDS output the total number of stages of a cubic DDS is five.

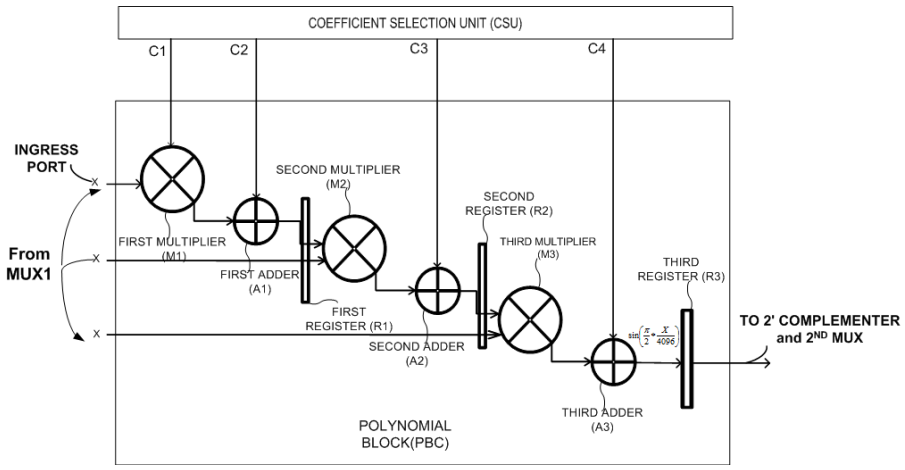


Figure 2.6 Block diagram of Polynomial Block (PBC)

The common reference clock (REFCLK) is also used to clock the PBC in Figure 2.6.

The **Coefficient Selection Unit (CSU)** block that supplies the required coefficients to the PBC for the cubic polynomial computation is illustrated in Figure 2.7.

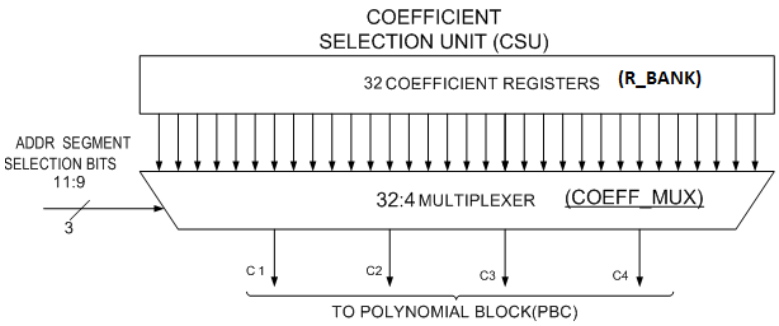


Figure 2.7 CSU with 32 coefficient registers and <32:4> Multiplexer

The CSU in turn comprises a register bank (R_BANK) and <32:4> multiplexer (COEFF_MUX). In turn, the 32:4 multiplexer is implemented by using four <8:1> multiplexer elements. The R_BANK comprises 32 storage registers divided into eight register banks. Each register bank comprising four registers. Each one of the eight register banks provide the coefficients required for a specific segment of the waveform (one register bank dedicated per segment in a quadrant-Figure 2.4b). Bits 11 through to 9 (**SEG_SEL**) form a control word to select the appropriate coefficients from the register bank.

2.4 SFDR of DDS as a quality measure for a frequency source

Spurious Free Dynamic Range (SFDR) is defined as the logarithm of ratio of amplitudes of the signal at the fundamental and the maximum of all subsequent harmonics. (SFDR) is the key measure of performance for any DDS and can be used for comparison of various DDS designs. It is the ratio of the fundamental to the maximum spur when considered in the frequency domain. [De Caro and Strollo, 2005] have derived a procedure which allows the computation of the SFDR of a cubic polynomial-based DDS through a closed form expression. In the derivations of [De Caro and Strollo, 2005] the SFDR measures the ratio of the fundamental to the $(4s_e + 1)^{\text{th}}$ harmonic on a logarithmic scale. The procedure derived by [De Caro and Strollo, 2005] is based on Fourier expansion and the analytical prediction of the levels of the generated harmonics. Their analysis and optimization procedure yield an idealized SFDR as a function of the number of segments (s_e) used by the DDS. The formulation by [De Caro and Strollo, 2005] for computation of SFDR is a very significant research contribution in the DDS theory.

In [De Caro and Strollo, 2005], the equation of the cubic polynomial used to compute DDS output is represented as,

$$V_k(x) = y_k + m_k(x - x_k) + p_k(x - x_k)^2 + q_k(x - x_k)^3 \tag{2.5}$$

In Equation (2.5) $k = 1,2, \dots, s$. Integer s_e is the number of segments within a quadrant of the generated output sinusoid of DDS. Coefficients $y_k, m_k, p_k \; and \; q_k$ are coefficients for the k^{th} segment of the polynomial function V_k. V_k represents the output waveform of k^{th} segment of DDS. x_k is the lowest argument value of the k$^{\text{th}}$ segment. Equation (2.6) provides an upper limit to the

achievable SFDR for a given number of segments. Thus, computation of SFDR provides a benchmark to assess the efficacy of a new DDS design.

The SFDR is defined as,

$$SFDR = 20\log_{10}\left(\frac{b_1}{\max(b_{n)}}\right) n = 2,3, \ldots. \quad (2.6)$$

In Equation (2.6), b_1 is the Fourier coefficient of the fundamental. In Equation (2.6) $\max(b_n)$ is the highest Fourier coefficient of any of the higher harmonics, where b_n is the nth order Fourier coefficient.

If an optimized cubic DDS for maximal SFDR, the SFDR [De Caro and Strollo, 2005] as a function of the number of segments (s_e)as

$$SFDR = 20\log_{10}\left(\frac{5 + 768s_e^2 + 5120s_e^4}{3}\right) = 20log_{10}\left(\frac{b_1}{\max(b_n)}\right) \quad (2.7)$$

In Equation (2.7) b_1 is the Fourier coefficient corresponding to the fundamental. In Equation (2.7) b_n is the Fourier coefficient corresponding to the nth -harmonic. s_e is the number of segments per quadrant. The maximum indicated in the denominator of Equation (2.7) is the maximum of the Fourier coefficients for all harmonics except the fundamental or $n = 1$. Equation (2.7) provides an upper limit to the achievable SFDR for a given number of segments. Thus, computation of SFDR provides a benchmark to assess the efficacy of a new DDS design.

Index n is the order of the Fourier coefficient, with $n = 1$ corresponding to the fundamental. For $n = 3,5,7, \ldots\ s - 1,$ the values of coefficients $g(n), h(n), l(n)\ and\ m(n)$ are optimized to zero in the method by [De Caro and Strollo, 2005]. All even harmonics $\{b(2n)\}$ vanish because of quadrant symmetry [De Caro and Strollo, 2005]. Details of how $g(n), h(n), l(n)\ and\ m(n)$ are computed is provided in De Caro and Strollo's paper.

For the optimized cubic DDS (with a given number of segments $'s_e'$), the closed form expressions for $g(1), h(1)\ l(1)\ and\ m(1)$ have been given by [De Caro and Strollo, 2005] as

$$g(1) = -B\frac{\pi^2(1 + 40\ s_e^2)}{8s_e^2(5 + 768\ s_e^2 + 5120\ s_e^4)} \quad (2.8)$$

$$h(1) = -B\frac{\pi^2(11 + 240s_e^2 - 2176s_e^4)}{64\ s_e^2(5 + 768s_e^2 + 5120s_e^4)} \quad (2.9)$$

$$l(1) = -B\frac{\pi^3(-5 + 80s_e^2 + 4224\, s_e^4)}{128s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{2.10}$$

$$m(1) = -B\frac{\pi^4(3 - 200s_e^2 - 128s_e^4 + 40960\, s_e^6)}{1536s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{2.11}$$

In Equations (2.8 to 2.11), the value B corresponds to the magnitude of the output waveform, while s_e corresponds to the number of segments in the DDS. The significance of Equations (2.8 through 2.11) is that they relate the number of segments for an optimal cubic DDS to the coefficients $g(1), h(1), l(1)\ and\ m(1)$ and through these coefficients, to the Fourier coefficient of the output waveform. Thus, in a design of a cubic DDS optimized for maximal SFDR for a given number of segments, Equations (2.8 to 2.11) together with Equation (2.7) provides the mathematical connectivity from maximal achievable SFDR to the values to $g(1), h(1)l(1), m(1)$

2.5 Maximum Absolute Error (MAE) of DDS

MAE of a DDS is defined as the absolute difference of DDS output versus an ideal sinusoid for the same phase input value. It is one of the performance parameters of a DDS. For any type of DDS, the MAE can be expressed as

$$MAE = Max(abs(\text{DDS output for a given phase input} - \text{ideal sinusoid for the same phase input})) \tag{2.12}$$

Equation (2.12) provides a definition for MAE. The MAE is a difference between two values – one for the ideal sinusoid and one for the actual sinusoid at the output of DDS. The abs operator in Equation (2.12) refers to the absolute difference between two quantities. The absolute difference is measured over all the samples which constitute a quadrant. For a cubic polynomial DDS, the above description is written as

$$MAE = Max(abs\left(DDS\_out(z_j) - Ideal((z_j)\right)) \tag{2.13}$$

In Equation (2.13) the *DDS_out* is estimated by a cubic polynomial using the polynomial expression which can be written as

$$DDS\_out(z_j) = C_{4,k} + C_{3,k}z_j + C_{2,k}z_j^2 + C_{1,k}z_j^3 \quad (2.14)$$

DDS_out is the DDS output for a cubic DDS with the phase argument z_j. The index j denotes the sample number. Coefficient $C_{1,k}$ are the third-order coefficient of the kth segment. Coefficient $C_{2,k}$ are the second-order coefficient of the k^{th} segment. Coefficient $C_{3,k}$ are the first-order coefficient of the k^{th} segment. Coefficient $C_{4,k}$ are the zeroth-order coefficient of the k^{th} segment. The ideal sinusoid with the same phase argument z_j is represented by

$$Ideal((z_j) = \sin(z_j) \quad (2.15)$$

The range of input phase arguments for application of Equation (2.15) is $0 \leq z_j \leq \pi/2$

All the points within a segment and at the boundaries of a segment must be considered while computing the MAE of a DDS. The absolute error of any of the DDS proposed in Equation (2.13) depends on the segment under consideration and the specific part of the segment. This is because coefficients are always computed for a given DDS on a per segment basis. Therefore, the value of the DDS output and its accuracy (MAE) depends on how accurately the coefficients are computed. Comparative MAE curves which are a contribution of this thesis have been included in Chapter 3.

2.6 SpSR of DDS designs

Defined as Spurious power divided by Signal power. SpSR measure the ratio of powers – that is the cumulative power in spurious tones divided by the power delivered at the fundamental frequency. Unlike SFDR which focusses on the largest maximum unwanted spur, SpSR focusses on the squares of amplitude or power.

2.7 PLL components and Stability criteria for PLLs

The Phase locked loop concept has been well described by [Banerjee, 2005]. Here only a brief mention is made about the components of a PLL and their functions. This section aims at a succinct review of the components of a PLL and their functions. A functional block diagram of a PLL with its important components is shown in Figure 2.8.

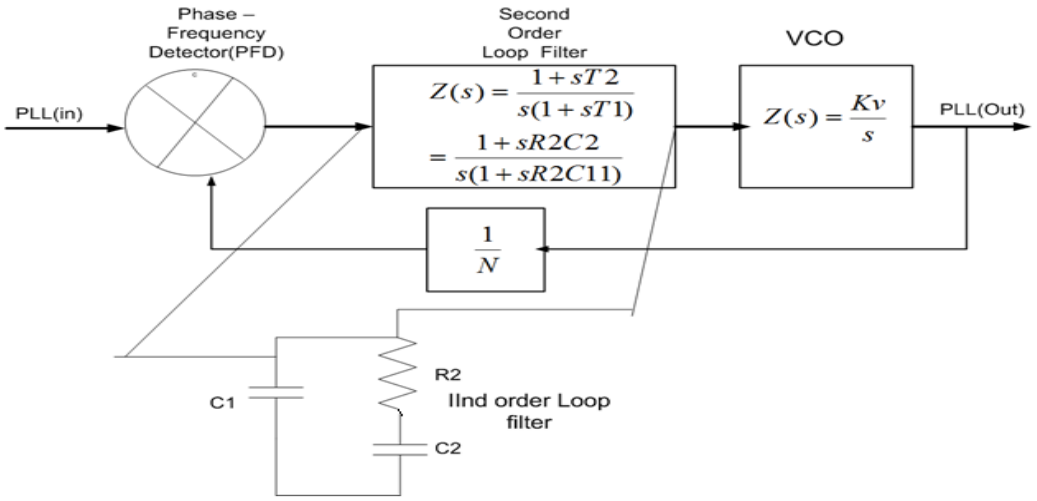


Figure 2.8 Block diagram of PLL showing PFD, VCO and Loop filter and divider

A PLL has at its input either a crystal oscillator source – whose output frequency has been divided by a suitable divider. The PLL is a device with a forward path and a feedback path. In the forward path, the first device (PLL sub-block) is the Phase-Frequency Detector (PFD). The PFD is a device that operates at a frequency known as the comparison frequency and produces an output current proportional to the phase difference between two signals. The first input signal to the PFD being the PLL primary input and the second input signal to the PFD being a divided version of the PLL primary output. The PFD is usually comprised of two current sources one to source current and the other to sink current (sometimes referred to as charge pumps). When the PLL primary input is advanced in phase compared to a divided version of the output, the PFD sources current. If on the other hand, the PLL input is behind in phase compared to a divided version of the output, the PFD sinks current. The PFD has a constant sensitivity in the regular operating region of the PLL it is denoted by $K_\phi/2\pi$. The constant K_ϕ is called the PFD sensitivity. This value of PFD sensitivity affects the transfer function, phase noise and lock time of the PLL.

The output of the PFD is filtered by an active or passive filter. The simplest passive filter is a single RC filter. Such a filter gives rise to a second-order PLL transfer function. The next level of complexity comprises of a RC filtered combined with a second parallel capacitor. This type of configuration gives rise to a cubic transfer function for a PLL, and in this thesis, this type of PLL is considered for development of analytical formulation.

The filtered output of the PFD is fed to a Voltage – Controlled Oscillator (VCO). The VCO is an active electronic circuit that converts a control voltage input into a known frequency output. In a PLL design, the VCO is operated in a region where there is a linear relationship between the control voltage at VCO input at the frequency at the VCO output. The VCO device has a control port where a filtered control voltage input is applied. The output of the VCO is the final PLL output. The VCO sensitivity controls PLL stability, lock time and phase noise. The VCO sensitivity is denoted by the symbol K_v. The VCO transfer function is indicated as K_v/s. K_v (VCO sensitivity) has the units of Hz/volt. The other fundamental parameter is the Phase-Frequency Detector (PFD) sensitivity K_ϕ which is a ratio of the current generated by the PFD divided by a phase shift. The phase shift is the difference in phase between the primary input to the PLL and a divided version of the PLL output.

The VCO output is connected to the PLL output. The VCO output is also fed back to the PFD through a frequency divider (block marked 1/N in Figure 2.8). The divider can be an integer or a fractional. Fractional dividers are composed of sigma-delta converters.

The Characteristic Equation (CE) of a third-order PLL is written as,

$$as^3 + bs^2 + cs + d = 0 \tag{2.16}$$

In Equation (2.16) a, b, c and d are coefficients; s is a Laplace variable

The Routh-Hurwitz stability criterion for a third-order transfer function corresponding to a third-order PLL can be written as

$$ad - bc \ < 0 \ and \ \{a, b, c, d\} > 0 \tag{2.17}$$

To account for the charge pump behavior, multiple other stability criteria have been suggested. The oldest one being that due to [Gardner, 1980] and newer ones, to [Van Paemel, 1994] and [Daniels, 2006]. Equation (2.18) applies to a second-order PLL,

$$K_{G2} = \frac{1}{\frac{\pi}{\omega_R \tau_2}(1 + \frac{\pi}{\omega_R \tau_2})} \tag{2.18}$$

In Equation (2.18) the variable τ_2 is the time constant of the loop filter (RC) of a second-order PLL. The constant ω_R is the comparison frequency of the second-order PLL.

[Gardner, 1980] proposed for third order PLLs the stability criterion can be written as

$$K_{G3} < \frac{4(1+a)}{\frac{2\pi(b_c-1)}{\omega_R\tau_2}\left(\frac{2\pi(a+1)}{\omega_R\tau_2}+\frac{2(1-a)(b_c-1)}{b_c}\right)} \tag{2.19}$$

In Equation (2.19), $a = e^{-\frac{2\pi(b_c)}{\omega_R\tau_2}}$ is an exponential constant defined by Gardner. Constant $b_c = \frac{C2+C3}{C3}$ is the capacitance ratio of the third-order PLL. τ_2 is the series time constant of the third-order PLL. The stability criteria due to [Van Paemel,1994] and [Daniels, 2006] are not used for further development in this thesis. Hence, it is not required to go deeper into them.

2.8 PLL spurs

PLL Spurs – Every PLL produces internally generated Spurs (Spurious Frequencies). Even if a pure sinewave is injected at the PLL input, the output of the PLL will still exhibit spurs. Spurs generated by PLL itself arise because of mismatches in the charge pump. Those spurs have been termed as "Mismatch spurs". The second source of source of spurs in a PLL is determined by leakage current in the phase detector. Such spurs are termed as "leakage spurs".

Leakage spurs are the result of leakage currents that flow in the VCO, loop filter and charge pump even when the PLL is locked. The charge pump is in a high impedance state when PLL is locked. Even within the high impedance state, alternating pulses of current flow through the charge pump. These pulses of leakage current alter the input to the VCO control input. Hence, the VCO control input value is no longer fixed. The alternation of the VCO control input generates spurs at the output of VCO and, therefore, at output of the PLL. There are no realistic analytical models possible for the magnitude of the leakage spur.

The spur magnitudes are usually computed by using a three-term empirical formula. The spur magnitude formula is provided by [Banerjee, 2005] as

$$\begin{aligned} &Leakage\ spur\ amplitude \\ &= Base\ Leakage\ spur + 20\log\left(\frac{Leakage\ current}{Phase\ detector\ sensitivity}\right) \\ &+ Spur\ Gain \end{aligned} \tag{2.20}$$

Equation (2.20) is an empirical equation. The *Base Leakage Spur* is empirically determined to be 16dB. The Leakage current is dependent on the Phase detector. The *Spur Gain* is the closed loop

gain of the PLL at a fixed comparison frequency. Modern PLLs have little charge pump leakage of the order of pico-amperes, so the amplitude of Leakage spurs keeps getting reduced with the advancement of process technology.

Mismatch spurs are produced in PLLs due to transistor level mismatches. Mismatches can arise due to transistor switching time mismatches in the charge pump transistors. Mismatch spurs can arise due to mismatch of charge pump current between the source side (usually PMOS) and the sink side (usually NMOS). It can arise due to unequal turn-on times between the source side and sink side, although designers try to match both turn–on times as closely as possible. They can rise due to a third cause, which is the inclusion of dead zone elimination circuits in the PLL. These circuits are designed to switch on the charge pump when the phase detector is sitting in the dead zone. The dead zone is a very small range of phase shift (around zero phase shift) for which there is no phase detector output.

The empirical equation for mismatch spurs has also been provided for the first time by [Banerjee,2006].

$$PulseSpur = Base\ Pulse\ Spur + Spur\ Gain + 40log_{10}\left(\frac{F_{spur}}{1Hz}\right) \quad (2.21)$$

In Equation (2.21), the *Base Pulse Spur* is an empirical constant whose magnitude is around -300dBc. The *Spur Gain* is the closed loop gain of the PLL at the PLL comparison frequency. The F_{spur} is the spur frequency under consideration.

2.9 Overshoot and phase margin of a PLL

Any underdamped system exhibits oscillatory behavior when a step input is applied. It can be a voltage step, a current step, a frequency step, or a phase step for electronic systems. In mechanical systems, it is a force step. Overshoot is a numerical measure of the maximum instantaneous amplitude of the output which is much higher than the steady-state output. Overshoot is expressed as a percentage of the absolute difference between the steady state output and the peak output divided by the steady-state output.

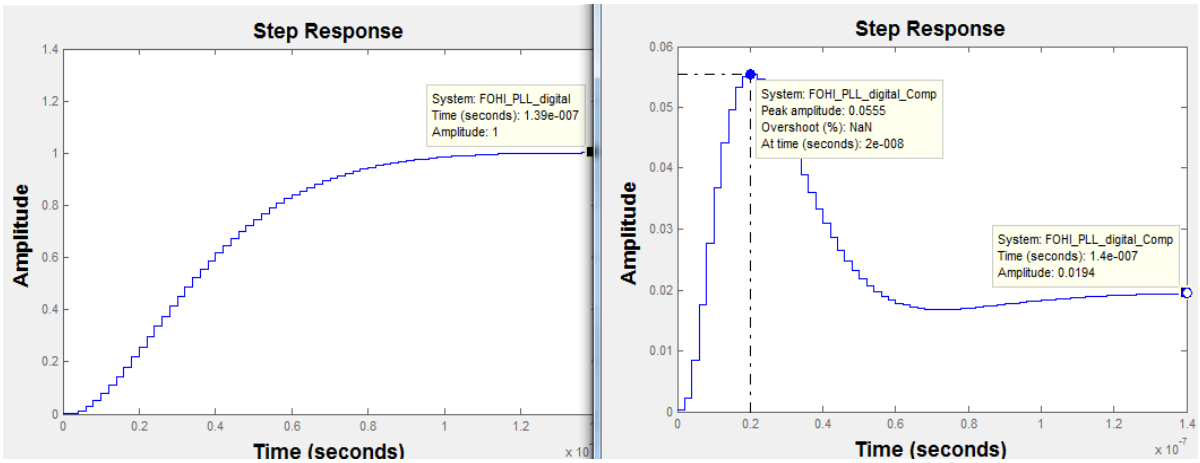


Figure 2.9 Example of overshoot of a PLL versus a steady state rise in output.

Phase Margin (PM): PM is defined as the excess phase of the PLL when the forward gain is unity. Its connected with the concept of Loop gain of a PLL. The loop gain is a product of the forward gain (G) and the feedback path gain (H). If the Loop gain (GH) of a PLL exceeds unity, then the phase margin must be positive. Otherwise, the PLL will be unstable.

2.10 Literature Review

2.10.1 Review of Research Studies on second-order PLL

[Banerjee,2005] has provided expressions for lock time, spur gain and methods to compute loop filter parameters. His models for leakage spurs and mismatch spurs have been directly used in chapter 5 of this thesis. Banerjee has provided models for phase noise and jitter as well.

[Drucker, 2000] has discussed models of multiple noise sources. He has also provided methodology to compute the noise transfer function for various sources. Drucker has not provided a methodology to compute a composite Power Spectral Density (PSD) of Phase Noise at the output of PLL in closed form.

[Amornthippart, 2008] describes the additive model for phase noise, thereby leading to cumulative phase noise of PLL. His analysis of phase noise does not cover analytical treatment of Noise Transfer Function (NTF) of various sources of noise and the analysis did not attempt to link the relationship of the phase noise with other performance metrics of DAC- PLL.

[He, 2007] has provided an analysis of PM of second-, third- and fourth-order PLL and the variance of "normalized" lock time with PM. [He, 2007] has provided the conditions for maximization of PM of a third-order PLL and the generalized transfer function of a third-order PLL both of these results are utilized in this thesis. [He, 2007] does not include the relationship between PM, rise time, damping coefficient and Phase noise.

[Daniels, 2008] discusses stability issues of higher order PLLs and introduces charge approximation methodologies. Based on charge approximation methodologies, Daniels avoids a lot of mathematical limitations of earlier research. Daniels's research supersedes earlier work due to Van Paemel on third-order charge pump PLLs. However, the relationship between phase noise and the referred performance metrics of PLL have not been explored in [Daniels, 2008].

[Lee, 2002] has provided an additive model for the jitter of a second-order Type II PLL. Further work has been done in chapter 4 by using Lee's model and relating jitter and PLL parameters such as phase margin.

[Mansuri, 2002] has provided jitter variance expressions for second-order PLLs. The derivations dues to Mansuri have been used to derive multiple new expressions for PLL parameters and jitter in Chapters 3 and 4.

2.10.2 Review of prior Research on Papers relating to third and high order PLLs

[Van Paemel, 1994] has proposed a behavioral model for the design and analysis of charge pump PLLs. The CP-PFD (Charge Pump-Phase Frequency detector) is a device that undergoes state transitions when the output state of the CP-PFD changes. This state machine behavior means it has three states – and UP state in which it supplies current, a DOWN state in which it sinks current and a "NULL" state where the current sourcing and sinking functions are off. When the Charge Pump-Phase Locked Loop (CP-PLL) is stable in one of these states without state transitions, the PLL acts like a linear system. Hence, it can be described by state equations. In [Van Paemel, 1994], paper there are two state variables – the pulse width of the phase detector and the loop filter capacitor voltage. His model attempts to compute the next phase detector pulse width as a function of the capacitor voltage picking one of four scenarios. The next value of capacitor voltage is estimated using the pulse width value. The disadvantages of his model are the stability limits

computed by Van Paemel's model, which means that it fails to capture the effect of non-linearity of the CP-PFD. It also suffers from the limitation of using a fixed time step.

[Hedayat, 1999] extended Van Paemel's method to a variable time step. The non-uniform time step is certainly an advance over Van Paemel's model. Hedayat's model requires 6 internal states His model cannot be extended beyond fourth-order however his results on stability margins are more accurate than those of Van Paemel.

[Herzel, 2010] has derived the NTFs for a fractional-N PLL with the sigma-delta modulator in the feedback path. A PLL without a sigma-delta modulator in the feedback path is the model under consideration of this thesis and PLL model of [Drucker, 2000] has been adopted for the analysis. The second clear distinction is with respect to the placement of the noise source of divider. In [Herzel,2010], divider noise source is placed before the feedback path of PLL.

The ITAE criterion is a control system criterion that provides a square of error multiplied by time passed in an integral form as a measure of performance for a control system. For a second-order system, [Dorf, 2005] plotted the ITAE performance criterion as a function of the damping coefficient. In this thesis, the ITAE performance criterion has been explored for a third-order PLL. The research in this thesis utilizes the theory of equations as applied to a third order PLL. The solution of a generalized cubic equation was studied by Giacomo Cardano (anglicized to Cardan) [Bernard and Child, 2011], and the classical solution of a cubic is known as Cardan's solution since the 1550s.

[Nickalls, 1993] makes a fundamental contribution to applied mathematics by introducing a new set of parameters different from the G and H parameters defined by Cardan's. Nickalls's solution of a cubic equation results in three categories of nature of roots: all three roots are real and unequal; all three roots are real and equal; of the three roots one root is real and the other two are complex conjugate roots.

Cardan's original solution technique for third-order equations is explained in [Bernard and Child, 2011]. In this thesis a variant of the classical technique is used to analyze third-order PLLs originally due to [Nickalls, 1993]. A definition of the discriminant of a third-order nonlinear equation is desirable, as its properties can be used to define the stability and the nature of the PLL. Such a definition is provided in chapter 5.

[Abramowitz, 2002] has written an important paper on application of Lyapunov's stability and Sylvester's theorem to third order PLLs. The stability measures addressed in this chapter are

related to linear models. [Abramowitz, 2002] applies non-linear (Lyapunov) system theory to the third order PLLs.

[D'Amato et. al., 2017] propose a polar transmitter architecture for beam steering that utilizes a DDS-PLL which phase shifting. This work has been published after this thesis was presented in 2016 and much after the original phase shifter work was done in 2011 (by this author). Their application is a circuit that performs 16-PSK modulation.

[Tonelli et. al. 2014] describes a X- band frequency oscillator comprising of a DDS, DAC and low phase noise and low lock time PLL. They claim a 30dB improvement in phase noise and a lock time of below 10us. They also claim fine frequency resolution.

[Vishnu and Anulal, 2015] propose an algorithm to detect whether a spur generated by a DDS lies within the loop BW of the PLL to which the DDS output is connected. If such a spur is detected their algorithm reconfigures the system to filter out the spur. The algorithm alters the DDS frequency such that the incoming spurs are filtered by the PLL.

2.10.3 Review of Research Studies on DDS

[De Caro, Napoli and Strollo, 2002] compares second order polynomial-based DDS versus CORDIC based DDS. This paper describes a featuring an SFDR of 80dBc using third-order polynomials and a second DDS (with an SFDR of 60dBc) using second-order polynomials and compares them with a CORDIC-based DDS.

[De Caro and Strollo, 2005] provides a theoretical framework to compute the SFDR of a cubic polynomial DDS. Their approach allows a DDS to be designed with integer number of segments per quadrant. The theory described in this paper is applicable to cubic DDS, quadratic DDS, LHSC DDS and Taylor series-based DDS. The theory explains how to achieve a SFDR of 180dB for a cubic DDS using $s_e = 32$. Its basic theory has been utilized to compute SFDR in chapter 3. It has also been extended to a quartic DDS in chapter 3.

[De Caro, Petra and Strollo, 2011] describes a DDS design which uses segments of unequal length with piecewise linear approximation in each segment. A conventional polynomial DDS utilizes fixed number of samples per segment. The authors propose a DDS deign with unequal segment where the segment length is adjusted to maximize SFDR. They demonstrate how to obtain the segment lengths for maximal SFDR. The number of segments is computed as a solution to a mixed integer and linear programming problem.

[Vankka, Waltari, Kosunen and Halonen, 1997] have described a DDS design incorporating an on-chip DAC. The overall SFDR is 60dBc and with a small step size of .0349 Hz. The frequency step size is 140ns. The device described in this paper incorporates a 10-bit DAC. It has an overall power dissipation of 0.6W.

[Vankka, Lindeberg and Halonen, 2004] have proposed error feedback techniques to suppress phase and amplitude spurs in DDS designs. The error feedback technique proposed by [Vankka, Lindeberg and Halonen, 2004] extracts error signals from the DDS. The output of the phase accumulator is truncated. The truncated signal is fed back after a second order FIR filtering to the phase accumulator. A similar feedback structure is placed after the phase to amplitude converter, after truncation of the phase to amplitude signal one part of the amplitude output is fed back to an adder after being filtered by a second-order FIR filter. Hence, both phase signal from PACC and amplitude signal produced by the Phase to amplitude converter are subjected to error feedback with two tunable coefficients. [Vankka, Lindeberg and Halonen, 2004] estimated that this improves SFDR by around 20dB.

2.10.4 Review of Research Studies (2014-2017) on high-order PLLs

[Golestan, Freijedo and Guerrero, 2015] present higher-order PLL design for power system applications. A systematic method for the design of higher-order PLLs is described. It does not discuss theoretical issues with the roots of a third-order PLL.

[Golestan et. al., 2017] discusses three-phase Frequency Locked Loops [FLLs] and provides models and stability analysis of three-phase second-order FLLs. Three-phase frequency locked loops are common in power systems. This is because when power systems are imbalanced, the instantaneous frequencies of each phase can be slightly different. A second-order FLL is one which

tracks both frequency and the derivative of frequency. This work is a bit different from the third -order PLL design issues addressed in this thesis.

[Genovese and Napoli, 2013] follows up on the earlier work due to De Caro and Napoli to implement multiple DDS designs on FPGA.

[Zhang et. al., 2017] have implemented a Taylor series DDS on an FPGA. They claim a SFDR of 114dBc. Besides, they stated that their approach which uses a Taylor series calculation and a new way of using look-up tables, reduced HW complexity and improved SFDR.

2.10.5 Important papers about adaptive notch filters

[Martens et al., 2006] addressed the issue of variable amplitude and random phase power line interference (50-60 Hz) in ECG signals. [Martens et al., 2006] tracks the amplitude and frequency and phase of all interference components in an ECG signal in real time. The proposed architecture uses a PLL type structure to correct for harmonics with varying amplitude and phase. Hence, the weight vector is split into two parts corresponding to amplitude and phase observations. This paper proposes combining error signals corresponding to each harmonic in the ECG as a composite signal. The proposed approach is to make the convergence rate independent of the magnitude of the interference signal. This is important when the interference signal magnitude can vary from cycle to cycle. [Martens et.al. 2006] uses an LMS algorithm with a matrix type structure. This approach completely suppresses spurs at 150 Hz.

2.11 Summary

This chapter aimed to present an overview of functional principles and analytical basics of DDS and PLL to facilitate the better appreciation of the rationale for proposed research and its findings. As a preamble, this chapter is focussed on establishing the functional and performance connectivity of DDS and PLL in a broad architecture of SDR/CR. Chapter 2 has also dealt with requisite details on the performance metrics of both DDS and PLL.

Phase noise, SFDR, MAE, SpSR and PM are among the significant parameters most commonly used in the evaluation of efficacy of the DDS design. Therefore, this chapter has

covered the basics of these performance metrics of DDS. The concept of stability criteria, spur and overshoot in PLL have also been addressed.

Chapter 2 has facilitated succinct review of prior research related to DDS and PLL with the perspective of the research proposed in this thesis. The presented succinct review has highlighted the scope, novelties and limitations of the prior research. In addition, this chapter has aimed at the discussion on the basis, relevance and significance of some of the referred research studies to the research topic of the proposed thesis.

The concise review of various principles and techniques, analysis and description of various sub systems as well as pertinent prior research presented in this chapter is intended to facilitate better appreciation of the analysis and simulation of DDS, PLL and DDS-PLL discussed in later chapters of this thesis.

Chapter 3 DDS for Enhanced Spectral Purity

Introduction

This chapter focuses on dither theory, application of dither and three other spur suppression techniques to DDS. Dithered schemes alter the SFDR and noise floor of DDS systems. The objective of this chapter is to analyze new and alternate schemes to improve the DDS. Section 3.1 pertains to a new architecture for the Taylor series DDS. This architecture reduces power while improving throughput. Section 3.2 is on literature review of Dither. In Section 3.2, a comprehensive literature review of papers pertaining to dither theory and quantization theory is presented. The literature review includes research publications on Hartley image reject architectures and on LMS based sinusoidal interference suppression schemes. Section 3.3 describes the computation of the SFDR of a Taylor series DDS. Section 3.4 describe computation of SFDR of LHSC DDS using the framework provided by [De Caro and Strollo, 2005]. The specific derivations are original contributions. Section 3.5 compares the MAE of four different types of DDS designs having the same number of segments per quadrant. Section 3.6 is dedicated to the classification of dither. All the equations in 3.6 are original contributions described the first time in this thesis. Section 3.7 contains a review of prior research in dithered DDS. A new expression for SpSR of phase dithered DDS has been derived by considering the higher-order moments in Section 3.8. Section 3.9 discusses Hartley image suppression for DDS. This section includes underlying theory and the addition of Hartley image suppression for Taylor series DDS and LHSC-DDS. Section 3.10 discusses Adaptive sinusoidal interference cancellation techniques for DDS including theory, implementation and illustrations of SFDR improvement before and after application of the adaptive harmonic canceller. Section 3.11 is the chapter's conclusion.

3.1 A new architecture for the Taylor Series DDS

This subsection proposes a low-power and high throughput DDS design using Taylor series expansion to generate sinusoidal waveforms.

Let the argument of sine function be $\left(\frac{\pi}{2}P\right)$where P is real and P varies between 0 and 4. This ensures so that sine function argument covers all the four quadrants.

The argument of sine function can be split into a sum of angles u and $(P-u)$

$$sin\left(\frac{\pi}{2}P\right) = sin\left(\frac{\pi}{2}(u+P-u\right) \tag{3.1}$$

In Equation (3.1) (u) is the value of the post significant bits of the argument. $(P-u)$ is the value of the least significant bits of the argument.

Using the Taylor Series expansion, the expression $sin\left(\frac{\pi}{2}(u+P-u\right)$ can be written as

$$sin\left(\frac{\pi}{2}P\right) = sin\left(\frac{\pi}{2}(u)\right)\left(1-\frac{\left(\frac{\pi}{2}(P-u)\right)^2}{2}\right) + cos\left(\frac{\pi}{2}(u)\right)\left\{\frac{\pi}{2}(P-u) - \frac{\left(\frac{\pi}{2}(P-u)\right)^3}{6}\right\} \tag{3.2}$$

Considering only first- and second-order term of $(P-u)$, one can represent the Taylor series expansion of the function $sin\left(\frac{\pi P}{2}\right)$ as

$$sin\left(\frac{\pi P}{2}\right) = sin\left(\frac{\pi u}{2}\right) + k_1(P-u)cos\left(\frac{\pi u}{2}\right) \quad -\frac{1}{2}k_2\{(P-u)\}^2 sin\left(\frac{\pi}{2}u\right) \tag{3.3}$$

In Equation (3.3) $k_1 = \frac{\pi}{2}$ and $k_2 = \left(\frac{\pi}{2}\right)^2$ are constants estimated by interpolation. Constants $k_1\ and\ k_2$ are required to convert radian angle arguments into normalized values so that the multiplication is possible. Taylor Series DDS has been designed earlier [Vankka, 2000] and [Goldberg, 1999].

Figure 3.1 Taylor Series DDS of [Vankka,2000]

The Taylor series DDS in Figure 3.1 comprises of a Phase ACCumulator (PACC), three ROMs, one multiplier and two adders. The Taylor Series DDS shown in Figure 3.1 was proposed by [Vankka, 2000].

The PACC produces a 12-bit wide address, which is further split into (u) the most significant bits and $(P-u)$ the least significant bits. The final output of Vankka's DDS which is a function of the outputs of ROMs M1, M2, M3 in Figure 3.1 can be written as

$$sin\left(\frac{\pi P}{2}\right) = sin\left(\frac{\pi u}{2}\right) + k_1(P-u)cos\left(\frac{\pi u}{2}\right) \; - \frac{1}{2}k_2\{(P-u)\}^2 sin\left(\frac{\pi}{2}u\right) \tag{3.4}$$

The limitation of Vankka's architecture is that the longest path (critical path) includes 1 multiplier(M1) and 2 adders (A1 and A2) in a cascade, thereby limiting the maximum throughput. The critical path of the Taylor series DDS is $T_m + 2T_a$(where T_m= multiplier delay and T_a = adder delay) which limits the possible upper range of operating frequency.

$$f_{out\_max} = \frac{1}{T_m + 2T_a} \tag{3.5}$$

In Equation (3.5) variable f_{out_max} is the maximum operating frequency or maximum throughput of the DDS.

The Taylor Series DDS of [Vankka, 2000] requires a multiplier and two adders with three ROMS dissipating much higher dynamic power. To implement a better DDS that overcomes both above limitations one must first consider the equation implemented in a Taylor series DDS. The second

term $k_1(P-u)cos\left(\frac{\pi u}{2}\right)$in RHS of Equation (3.4) can be replaced by the addition of two terms;

$\frac{1}{4}k_1\left\{(P-u)+cos\left(\frac{\pi}{2}u\right)\right\}^2$ and $-\frac{1}{4}k_1\left\{(P-u)-cos\left(\frac{\pi}{2}u\right)\right\}^2$

Thus, Equation (3.5) can be rewritten as a summation of four independent terms as

$$sin\left(\frac{\pi P}{2}\right)=sin\left(\frac{\pi u}{2}\right)+\frac{1}{4}k_1\left\{(P-u)+cos\left(\frac{\pi}{2}u\right)\right\}^2-\frac{1}{4}k_1\left\{(P-u)-cos\left(\frac{\pi}{2}u\right)\right\}^2 -\frac{1}{2}k_2\{(P-u)\}^2sin\left(\frac{\pi}{2}u\right) \tag{3.6}$$

The transformation of Equation (3.4) to Equation (3.6) signifies, that multiplication for a real function can be replaced by a subtraction of two different functions if the input functions are both real. This transformation allowed a new type of multiplier-less architecture for Taylor series DDS. The arguments of sine and cosine functions described above translate to the ROM address of DDS. The bit string represented by u is the most significant bits of the ROM address and the bit string represented by $(P-u)$ is least significant bits of the ROM address. In the implementation of Taylor Series in DDS, four ROMs (indexed as A through D) are mandatory since they are corresponding to the four terms on the RHS of Equation (3.6). The four ROMs belonging to the series (A through D) may include values, according to the Equations (3.7-3.10) so that one of the four ROMs includes values for each term of Equation (3.6).

The first ROM (ROM_A) stores the first term in Equation (3.6) and stores the output value O_A given by

$$O_A=sin\left(\frac{\pi}{2}u\right) \tag{3.7}$$

The second ROM (ROM_B) stores the output O_B, given by

$$O_B=-\frac{1}{4}k_1\left\{(P-u)+cos\left(\frac{\pi}{2}u\right)\right\}^2 \tag{3.8}$$

The third ROM (ROM_C) stores the output O_C and is given by

$$O_C=-\frac{1}{4}k_1\left\{(P-u)-cos\left(\frac{\pi}{2}u\right)\right\}^2 \tag{3.9}$$

The stored output of fourth ROM (ROM_D) has the output (O_D) defined by

$$O_D=-\frac{1}{2}k_2\{P-u\}^2sin\left(\frac{\pi}{2}u\right) \tag{3.10}$$

The proposed Taylor series DDS shown in Figure 3.2. The new proposed DDS requires 4 ROMs which store values $O_A, O_{B,} O_C, O_D$ and their outputs must be added for every sample using a four-input adder. The four-input adder performs single cycle addition of four operands (one from each ROM) from a set of four ROMs. The speed of the adder, which is the time required to propagate through the carry chain of the adder must be lower than the access time of the slowest of the four ROMs.

The proposed Taylor's series DDS [Mazumdar and Kadambi, 2013; Mazumdar and Kadambi, 2015] comprises six major logical blocks organized in a single six-stage data-path with four parallel data-path segments – each segment being possessed by a different ROM (Figure 3.2).

Figure 3.2 Block Diagram of Proposed Taylor Series Based DDS [Mazumdar and Kadambi, 2013]

Figure 3.2 is the composite datapath of the new type of Taylor series DDS invented by the author. It comprises of six separate blocks. The first block of the new DDS described is the PACC which

receives a reference clock input (frequency f_{clk}) and generates a digital phase word, thus forming address to the ROMs. The output of Phase Accumulator Register (PACR) output u is a digital word of width greater than 16 bits representing a phase angle between 0 and 2π. The PACC is not part of the invention, and hence its details are excluded [Vankka, 2000].

The second stage of the six-stage pipeline comprises four ROM blocks whose address lines are driven by the PACC. The ROM blocks (A, B, C and D) generate terms in accordance with Equation (3.6). The output bit-width of all the 4 ROMs is the same. The address size for all the 4 ROMs is the same as the output bit width of the PACC. The ROM A is programmed with the first term of Equation (3.6). Likewise, ROM B, ROM C and ROM D are programmed with the second term, the third term and fourth term of Equation (3.6) respectively. The ROM depth for all the ROMs A through D is given by 2^N where N is the output bit-width of PACC. For proper operation of the DDS, all the memories in Figure 3.2 must operate by utilizing a common reference clock (f_{clk}). ROM A, ROM B, ROM C and ROM D store values given by Equations (3.7, 3.8, 3.9 and 3.10) respectively. The final output of the DDS is the summation of the outputs of the four ROMs using the four-input adder in Figure 3.2.

$$sin\left(\frac{\pi P}{2}\right) = sin\left(\frac{\pi u}{2}\right) + \frac{1}{4}k_1\left\{(P-u) + cos\left(\frac{\pi}{2}u\right)\right\}^2 - \frac{1}{4}k_1\left\{(P-u) - cos\left(\frac{\pi}{2}u\right)\right\}^2 - \frac{1}{2}k_2\{(P-u)\}^2 sin\left(\frac{\pi}{2}u\right) \quad (3.11)$$

The net effect of adding the second term (in Equation 3.11) from ROM B and third term (in Equation 3.11) from ROM C is that the second multiplicative term in Equation (3.4) can be generated without having to perform an actual multiplication. The eliminates the need for an additional multiplier. The third stage of the proposed six-stage data path (in Taylor Series DDS) comprises 4 registers RxA, RxB, RxC and RxD which receive the outputs from ROM A, ROM B, ROM C and ROM D respectively. The register widths of registers RxA, RxB, RxC and RxD must be equal to the bit-widths of ROM output. The operating clocks of registers are the same as the operating clock of ROMs to ensure proper operation of the synchronous data path. There are two possible connective paths between the output of the register and the input of the following computational stage (four input adder) –one being a serial path and the other being a parallel path [Mazumdar and Kadambi, 2013].

The fourth stage of the six-stage data path (in Figure 3.2) in the Taylor Series DDS is a four-input adder used to summation of outputs of the four registers in the third stage namely RxA, RxB, RxC and RxD. The fifth stage is the register located at the output of the four-input adder (fourth stage). The fifth stage register is connected to the input of the sixth and final stage, which is the DAC block. The DAC block synthesizes a continuous time waveform from the discrete time signal present at the output of the fifth stage register. The architecture of Taylor series DDS shown in Figure 3.2 constitutes an original contribution of this thesis.

3.2 Quartic DDS theory and block diagram and a new integral

The cubic polynomial DDS with $s_e = 32$ segments can achieve an SFDR of 185dB. This paves the way for one to look for an alternative DDS which can achieve a higher SFDR for the same number of segments, say for $s_e = 8$ where the cubic polynomial DDS achieves an SFDR of 136 dB. In the process, one attempts to achieve a slightly better MAE. The quartic DDS shown in Figure 3.1 appears to have not been attempted earlier. It requires an additional coefficient for each segment within a quadrant and an additional stage in the pipeline. The quartic DDS requires a more complex Coefficient Selection Unit (CSU) and a more complex data path as compared to the cubic polynomial DDS in Figure 3.11. The CSU of the quartic DDS outputs five coefficients per cycle (Fig 3.3), as compared to four coefficients per cycle in the cubic DDS (Figure 2.5 in Chapter 2 of this thesis).

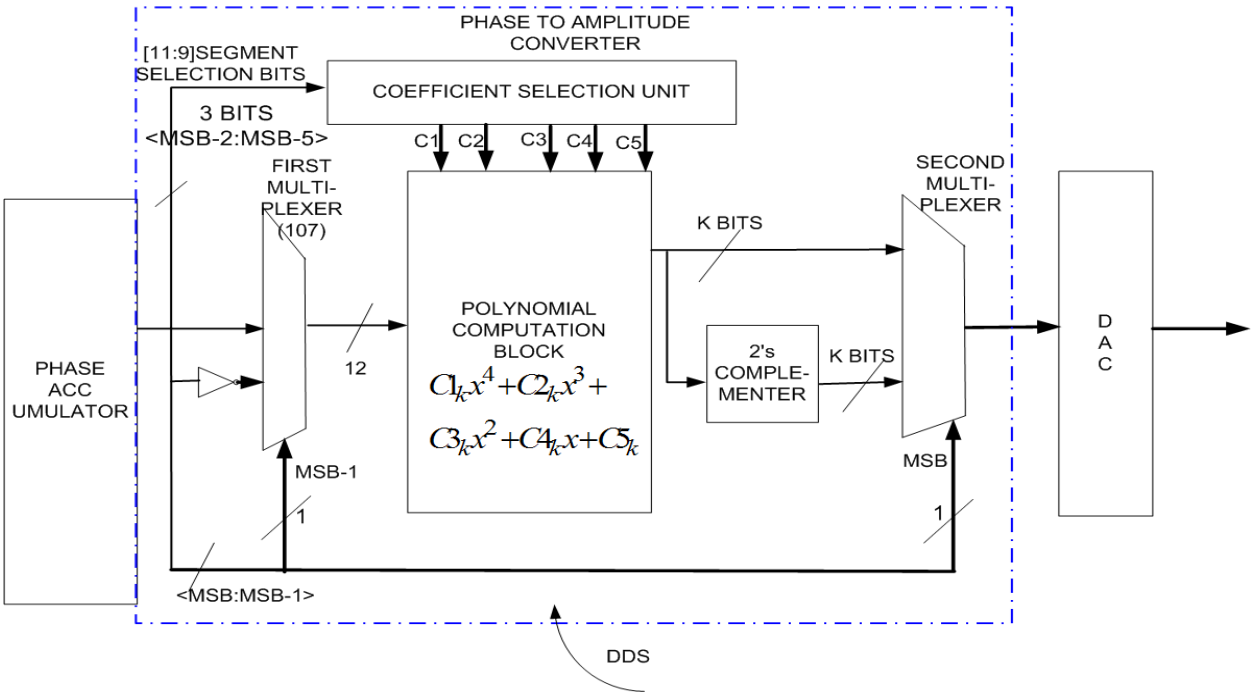


Figure 3.3 Quartic DDS block diagram

Figure 3.3 illustrates a structure similar to the cubic polynomial DDS. Figure 3.3 is a modified version of the cubic polynomial DDS described in Figure 2.5. One difference between Figure 3.4 and Figure 2.5 is that the CSU is more complex and requires an additional multiplexer because it must generate five coefficients for every segment versus four coefficients per segment for the cubic DDS. The CSU for the quartic DDS (Figure 3.3) requires more storage than the CSU for the cubic polynomial DDS (Figure 2.7). Specifically, it requires that additional s_e registers (where s_e is the number of segments) are necessary to store the additional coefficients required for quartic DDS. Figure 3.4 illustrates the additional pipeline stage that must be used for the quartic DDS.

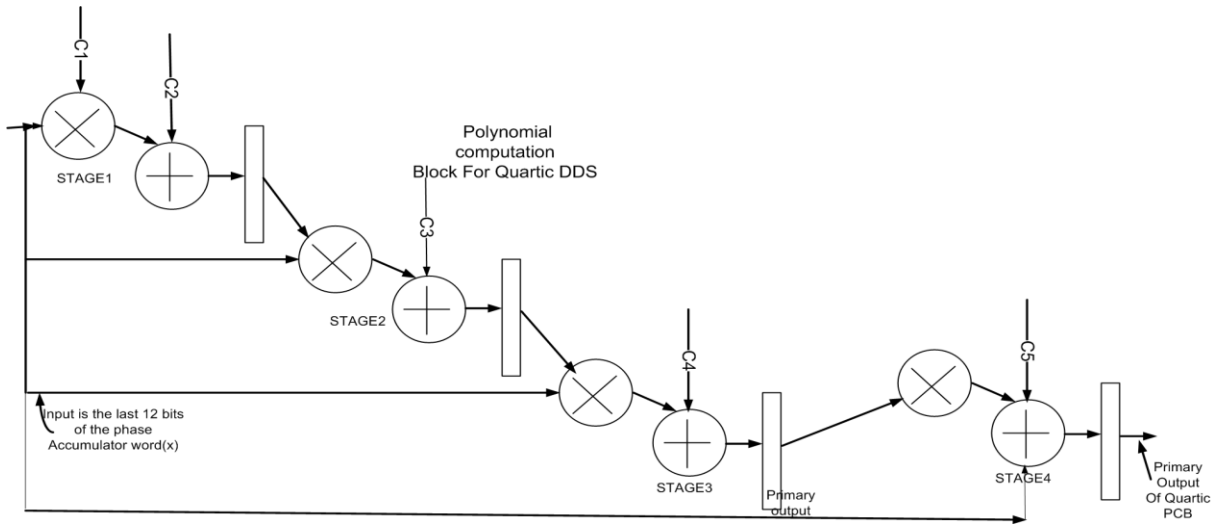


Figure 3.4 Polynomial Computation Block (PCB) for quartic DDS

Figure 3.4 illustrates the Polynomial Computation Block (PCB) or the polynomial computation pipeline for the quartic DDS. For the quartic DDS, a model by [De Caro and Strollo, 2005] can be extended with the following expression:

$$V_k(x) = v_k(x - x_k)^4 + q_k(x - x_k)^3 + p_k(x - x_k)^2 + m_k(x - x_k) + y_k \text{ for } k = 1,2, \dots s_e \quad (3.12)$$

In Equation (3.12), the symbols y_k, m_k, p_k, q_k, v_k are coefficients and each can be considered as a row vector s_e wide where s_e is the number of segments per quadrant. The additional quartic term has a coefficient vector v_k. The coefficient v_k is the coefficient for the fourth power of the difference (the fourth order term).

v_k is the quartic coefficient for $k = 1,2, \dots s_e$. The constant $x_k$is the lower limit of the k^{th} segment. The variable x is an independent phase angle argument varying between 0 and 1($0 \leq x \leq 1$).

The coefficient computation follows the least squares approach like the one that was performed for the cubic polynomial interpolation.

$$Z = C_1 z^4 + C_2 z^3 + C_3 z^2 + C_4 z + C_5 \quad (3.13)$$

The independent phase variable z in Equation (3.13) varies between 0 and $\frac{\pi}{2}$. The cubic DDS output is the variable Z.

Equation (3.12) utilizes a difference form whereas Equation (3.13) utilizes a simple polynomial approach. Since both must produce the same result, the values of the coefficients in Equation (3.12) and (3.13) can be related.

To compute the coefficients v_k, y_k, m_k, p_k, q_k , one must first introduce the variable $c = \frac{\pi}{2}$ which is used to convert the range of the variable z into the range of the variable x.

To convert from the least squares form (Equation 3.13) to [DeCaro and Strollo, 2005] form as in Equation 3.12, one must perform the substitution $z = cx$ in (3.13), so that the RHS of both Equation (3.12) and Equation (3.13) are in powers of x. In the next step the coefficients of the powers of x are equated and this leads to 5 conversion formulae.

Thus, by equalizing powers of x in Equation (3.12) and a converted form of Equation (3.13), the coefficient computed by least squares formulation can be readily converted to the form of [DeCaro and Strollo, 2005]. The conversion formulae can be expressed as

$$v_k = C_{1,k} c^4 \; where \; c = \frac{\pi}{2} \tag{3.14}$$

$C_{1,k}$ is the quartic coefficient for segment k as computed by using least squares approach.

The cubic polynomial coefficient can be computed by the following equation,

$$q_k = C_{2,k} c^3 + 4 v_k \; for \; k = 1,2, \dots, s \tag{3.15}$$

The quadratic polynomial coefficient can be computed by the following equation:

$$p_k = C_{3,k} c^2 + 3 q_k x_k - 6 v_k x_k^2 \tag{3.16}$$

The linear polynomial coefficient in [De Caro and Strollo, 2005] form can be computed using the following expression:

$$m_k = C_{4,k} c + 2 p_k x_k - 3 q_k x_k^2 + 4 v_k x_k^3 \tag{3.17}$$

The constant polynomial coefficient can be computed by using the following expression:

$$y_k = C_{5,k} + m_k x_k - p_k x_k^2 + q_k x_k^3 - \; v_k x_k^4 \tag{3.18}$$

The least squares equation to estimate the polynomial coefficients for a range of 0 to $\pi/2$ can be written as in Equation (3.3). It is noted that, compared to the 4x4 matrix computation for the cubic DDS, the solution of the coefficients of the quartic DDS requires solution of a 5x5 matrix equation. The equation or matrix size is the order of the polynomial approximation incremented by one.

One must express the least squares coefficient computation in a matrix form (for the k^{th} segment) as in Equation (3.19). One must solve $C_{1,k}, C_{2,k}, C_{3,k}, C_{4,k}$ and $C_{5,k}$ for the k^{th} segment

$$\begin{bmatrix} \sum_i z_i^8 & \sum_i z_i^7 & \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 \\ \sum_i z_i^7 & \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 \\ \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 & \sum_i z_i^2 \\ \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 & \sum_i z_i^2 & \sum_i z_i \\ \sum_i z_i^4 & \sum_i z & \sum_i z_i^2 & \sum_i z_i & N \end{bmatrix} \begin{bmatrix} C_{1,k} \\ C_{2,k} \\ C_{3,k} \\ C_{4,k} \\ C_{5,k} \end{bmatrix} = \begin{bmatrix} \sum_i y_i z_i^4 \\ \sum_i y_i z_i^3 \\ \sum_i y_i z_i^2 \\ \sum_i y_i z_i \\ \sum_i y_i \end{bmatrix} \tag{3.19}$$

In Equation (3.19), z_i is Input phase angle arguments for i^{th} sample within the k^{th} segment. The variables y_i are the output value for i^{th} sample within the k^{th} segment. The vector $[C1_k, C2_k, C3_k, C4_k, C5_k]$ is the vector of coefficient values for the k^{th} segment. The 4X4 matrix in Equation (3.19) is referred to in this chapter as Matrix T_q where q refers to quartic.

The values z_i and y_i are known and from Equation (3.19), only the Coefficient values must be computed. The coefficient vector from Equation (3.19) can simply be solved by matrix inversion of the matrix T,

$$T_q = \begin{bmatrix} \sum_i z_i^8 & \sum_i z_i^7 & \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 \\ \sum_i z_i^7 & \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 \\ \sum_i z_i^6 & \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 & \sum_i z_i^2 \\ \sum_i z_i^5 & \sum_i z_i^4 & \sum_i z_i^3 & \sum_i z_i^2 & \sum_i z_i \\ \sum_i z_i^4 & \sum_i z & \sum_i z_i^2 & \sum_i z_i & N \end{bmatrix} \tag{3.20}$$

Using the classical least squares solution applied to Equation (3.19),

$$\begin{bmatrix} C_{1,k} & C_{2,k} & C_{3,k} & C_{4,k} & C_{5,k} \end{bmatrix}^T = \left(T_q{}' T_q\right)^{-1} (T_q{}' b_q) \tag{3.21}$$

In Equation (3.21), $T_q{}'$ is the Matrix transpose of the matrix T_q. Vector b_q is the RHS column vector in Equation (3.19). Next, the computed coefficients are converted to the form, which is like the expressions used by [De Caro and Strollo, 2005].

$$Z = y_k + m_k(x - x_k) + p_k(x - x_k)^2 + q_k(x - x_k)^3 + v_k(x - x_k)^4 \quad (3.22)$$

Expanding the power of x in Equation (3.22) one obtains:

$$Z = (y_k - m_k x_k + p_k x_k^2 + q_k x_k^3 + v_k x_k^4 + (3q_k x_k - 4v_k x_k^2 - 2p_k x_k + m_k)x + (-3q_k x_k + 6v_k x_k^2 + p_k)x^2 + (q_k - 4v_k)x^3 + v_k x^4 \quad (3.23)$$

Equating the fourth power coefficients (x^4, x^3, x^2, x) between Equations (3.22 and 3.23**)** one obtains four equations. Constant $C_{1,k}, C_{2,k}, C_{3,k}, C_{4,k}$ and $C_{5,k}$ is evaluated as

$$C_{1,k}c^4 = v_k \quad (3.24)$$

Constant $C_{2,k}$ is evaluated as

$$C_{2,k}c^3 = q_k - 4v_k \Rightarrow q_k = C_{2,k}C2_k c^3 + 4v_k \quad (3.25)$$

Constant $C_{3,k}$ is evaluated as

$$C_{3,k}c^2 = -3q_k x_k + 6v_k x_k^2 + p_k \Rightarrow p_k = C_{3,k}c^2 + 3q_k x_k - 6v_k x_k^2 \quad (3.26)$$

Constant $C_{4,k}$ is evaluated as

$$m_k = C_{4,k}c - 3q_k x_k^2 + 4v_k x_k^3 + 2p_k x_k \quad (3.27)$$

Equating the constant term between Equations (3.22 and 3.23) one obtains an expression for y_k as

$$y_k = C_{5,k} + m_k x_k - p_k x_k^2 + q_k x_k^3 - v_k x_k^4 \quad (3.28)$$

This Equation (3.24) through Equation (3.28) must be solved for all the intervals to compute the corresponding coefficients $(y_k, m_k, p_k. q_k, v_k)$. Of these five coefficients, only v_k is new and has been added in this chapter.

Since the coefficients and their equivalents in terms of coefficients defined by [De Caro and Strollo, 2005] are easily computable, the SFDR of such a quartic DDS can be derived as the ratio of the maximum to the third harmonic as explained in Equation (3.29 and (3.30).

The Fourier coefficients of the fundamental and third harmonic are computed as

$$b_1 = 0.99999999971;\ b_3 = 0.00000001 \quad (3.29)$$

Hence the SFDR is computed as the ratio of the fundamental and the third harmonic,

$$SFDR = 10 * log10\left(\frac{b_1}{b_3}\right) = 185\ dB \quad (3.30)$$

One validation of this is that the computed Fourier coefficient is almost close to 1. If it is not the computed coefficients will be incorrect. This observation is same as in Cubic DDS.

3.2.1 Integrals and results on Quartic DDS

This section illustrates the computation of a closed form integral required for the final computation of analytical SFDR of a quartic DDS. Only the integral computation and not the SFDR computation is claimed as an original computation.

The Fourier coefficients for any order of interpolation have been provided by [De Caro and Strollo, 2005] as

$$b_n = 2\int_0^1 f(x)\sin(\frac{n\pi x}{2})dx \tag{3.31}$$

For the quartic DDS, the output function $f(x)$ is written as

$$f(x) = y_k + m_k(x - x_k) + p_k(x - x_k)^2 + q_k(x - x_k)^3 + v_k(x - x_k)^4 \tag{3.32}$$

In Equation (3.32), x is the phase argument with $x_k \leq x \leq x_{k+1}$ for the k^{th} segment, where x_k is the starting value of x for the k^{th} segment. The range of the phase argument x is limited between $x_1 = 0\ and\ x_{s+1} = 1$. This is for alignment with the range proposed by [De Caro and Strollo, 2005].

The closed form single integral (Equation 3.31) is split into a sum of five integrals for each segment, and the five integrals summed over s segments. The five integrals for a Quartic DDS are derived like what was derived by [De Caro and Strollo, 2005]. The generic form of a Fourier coefficient is a sum of s_e terms, each term comprising a definite integral. Four of these terms are common with the derivation of [DeCaro and Strollo, 2005]. It is the fifth term that is of interest in this chapter and the new expressions are simplified forms of the fifth term. These five integrals are required to derive a closed form expression for the b_n Fourier coefficients for a Quartic DDS, The relationship between the b_n and the integrals $(I'_{k,n}, I''_{k,n}, I'''_{k,n}, I''''_{k,n}, I'''''_{k,n})$ are listed as

$$b_n = \sum_{k=1}^{s}\left(I'_{k,n} + I''_{k,n} + I'''_{k,n} + I''''_{k,n} + I'''''_{k,n}\right) \tag{3.33}$$

In Equation (3.33), b_n is the n^{th} Fourier coefficient of the quartic DDS.

The four definite integrals on the right-hand side of Equation (3.33) are expressed in closed form as function of the quartic polynomial coefficients as

$$I'_{k,n} = \int_{x_k}^{x_{k+1}} 2y_k sin\left(\frac{n\pi x}{2}\right) dx \tag{3.34}$$

$$I''_{k,n} = \int_{x_k}^{x_{k+1}} 2m_k(x - m_k) sin\left(\frac{n\pi x}{2}\right) dx \tag{3.35}$$

$$I'''_{k,n} = \int_{x_k}^{x_{k+1}} 2p_k(x - x_k)^2 sin\left(\frac{n\pi x}{2}\right) dx \tag{3.36}$$

$$I''''_{k,n} = \int_{x_k}^{x_{k+1}} 2q_k(x - x_k)^3 sin\left(\frac{n\pi x}{2}\right) dx \tag{3.37}$$

Finally, the fifth integral only for a quartic DDS is written as

$$I'''''_{k,n} = \int_{x_k}^{x_{k+1}} 2v_k(x - x_k)^4 sin\left(\frac{n\pi x}{2}\right) dx \tag{3.38}$$

The five integrals must now be evaluated and each of the limits are substituted. The closed form expression for the first four integrals have been expressed in [De Caro and Strollo, 2005]. The lower limits of the integrals are written as

$$x_k = \frac{(k-1)}{s_e} \tag{3.39}$$

The upper limits of the integrals are written as

$$x_{k+1} = \frac{(k)}{s_e} \tag{3.40}$$

The four integrals, $I'_{k,n}, I''_{k,n}, I'''_{k,n}, I''''_{k,n}$ have been computed in [De Caro and Strollo, 2005] paper. It is the fifth integral ($I'''''_{k,n}$)that is unique to the quartic DDS and is not part of [De Caro and Strollo, 2005]. A closed form expression for ($I'''''_{k,n}$)has been derived in this chapter.

Incorporating the expansion of $(x - x_k)^4$, the fifth integral (Equation 3.38) is written as

$$\begin{aligned} 2v_k \int (x - x_k)^4 sin\left(\frac{n\pi x}{2}\right) dx = \; & 2v_k \int (x^4 - 4x^3 x_k + 6x^2 x_k^2 - 4x x_k^3 \\ & + x_k^4) sin\left(\frac{n\pi x}{2}\right) dx \end{aligned} \tag{3.41}$$

The indefinite integral for the quartic term is written as

$$\int (x^4 - 4x^3 x_k + 6x^2 x_k^2 - 4x x_k^3 + x_k^4) sin\left(\frac{n\pi x}{2}\right) dx \tag{3.42}$$

The corresponding definite integral can be written as

$$I''''_{k,n} = \int_{\frac{(k-1)}{s}}^{\frac{(k)}{s}} (x^4 - 4x^3x_k + 6x^2x_k^2 - 4xx_k^3 + x_k^4) sin\left(\frac{n\pi x}{2}\right) dx \tag{3.43}$$

With $x_k = \frac{(k-1)}{s_e}$ and the integral being taken between the limits $x = \frac{(k-1)}{s_e}$ to $x = \frac{(k)}{s_e}$, the resultant integral (without the final summation from $k = 1\ to\ k = s_e$) is written as

$$I''''_{k,n} = \frac{768cos\left(\frac{\pi n - \pi kn}{2s_e}\right) - 768cos\left(\frac{\pi kn}{2s_e}\right)}{\pi^5 n^5} - \frac{2\pi^4 n^4 cos\left(\frac{\pi kn}{2s_e}\right) - 16\pi^3 n^3 s_e\left(sin\left(\frac{\pi kn}{2s_e}\right)\right) - 96\pi^2 n^2 s^2 cos\left(\frac{\pi kn}{2s_e}\right) + 384\pi n s^3\left(sin\left(\frac{\pi kn}{2s_e}\right)\right)}{\pi^5 n^5 s^4} \tag{3.44}$$

In Equation (3.44), considering the sum of such terms from $k = 1\ to\ k = s_e$ one can write,

The first sum $S1$ is written as

$$S1 = \sum_{k=1}^{s} v_k \frac{(384\pi n s^3 - 16\pi^3 n^3 s)\left(sin\left(\frac{\pi kn}{2s}\right)\right)}{\pi^5 n^5 s^4} = \frac{(384\pi n s^3 - 16\pi^3 n^3 s)}{\pi^5 n^5 s^4} \sum_{k=1}^{s} v_k \left(sin\left(\frac{\pi kn}{2s}\right)\right) \tag{3.45}$$

The second sum $S2$ is written as

$$S2 = \sum_{k=1}^{s} v_k \frac{(-2\pi^4 n^4 - 96\pi^2 n^2 s^2 - 768s^4)\left(cos\left(\frac{\pi kn}{2s}\right)\right)}{\pi^5 n^5 s^4} = \frac{(-2\pi^4 n^4 - 96\pi^2 n^2 s^2 - 768s^4)}{\pi^5 n^5 s^4} \sum_{k=1}^{s} v_k \left(cos\left(\frac{\pi kn}{2s}\right)\right) \tag{3.46}$$

The third term $S3$ is written as

$$S3 = \sum_{k=1}^{s} v_k \frac{768\left(cos\left(\frac{\pi(k-1)n}{2s}\right)\right)}{\pi^5 n^5 s^4} = \frac{(768)}{\pi^5 n^5 s^4} \sum_{k=1}^{s} v_k \left(cos\left(\frac{\pi(k-1)n}{2s}\right)\right) \tag{3.47}$$

The summation of such integrals$(S1, S2, S3)$ provides the final closed form expression for fourth power part of b_n

$$\sum_{k=1}^{s}\left(I_{k,n}^{'''''}\right) = \frac{(768)}{\pi^5 n^5 s^4}\sum_{k=1}^{s} v_k\left(cos\left(\frac{\pi(k-1)n}{2s}\right)\right) + \frac{(-2\pi^4 n^4 - 96\pi^2 n^2 s^2 - 768s^4)}{\pi^5 n^5 s^4}\sum_{k=1}^{s} v_k\left(cos\left(\frac{\pi kn}{2s}\right)\right) + \frac{(384\pi n s^3 - 16\pi^3 n^3 s)}{\pi^5 n^5 s^4}\sum_{k=1}^{s} v_k\left(sin\left(\frac{\pi kn}{2s}\right)\right) \quad (3.48)$$

The expression of the integral $I_{k,n}^{'''''}$ as a summation of the definite integrals with the limits $k = 1\ to\ k = s_e$ is a major theoretical contribution of this section. Such an expression has not been discussed in the open literature. Equation (3.48) is a new contribution, not found in the open literature.

Equations (3.49-3.52) summarize the exact contributions made by [De Caro and Strollo, 2005] and the specific additional terms (only Equation 3.53) which are derived in this chapter.

The integral $I_{k,n}^{'}$ is written in closed form as

$$I_{k,n}^{'} = \frac{4y_k}{n\pi}\left[cos\left(\frac{(k-1)n\pi}{2s}\right) - cos\left(\frac{(k)n\pi}{2s}\right)\right] \quad (3.49)$$

The integral $I_{k,n}^{''}$ is written in closed form as

$$I_{k,n}^{''} = -\frac{4m_k}{n^2\pi^2 s}\left[2s\left(sin\left(\frac{(k-1)n\pi}{2s}\right) - sin\left(\frac{(k)n\pi}{2s}\right)\right) + n\pi cos\left(\frac{(k)n\pi}{2s}\right)\right] \quad (3.50)$$

The integral $I_{k,n}^{'''}$ is written in closed form as

$$I_{k,n}^{'''} = -\frac{4p_k}{n^3\pi^3 s^2}\left[8s^2 cos\left(\frac{(k-1)n\pi}{2s}\right) + (n^2\pi^2 - 8s^2)cos\left(\frac{(k)n\pi}{2s}\right) - 4n\pi sin\left(\frac{(k)n\pi}{2s}\right)\right] \quad (3.51)$$

The integral $I_{k,n}^{''''}$ is written in closed form as

$$I_{k,n}^{''''} = -\frac{4q_k}{n^4\pi^4 s^3}\left[+n\pi(n^2\pi^2 - 24s^2)cos\left(\frac{kn\pi}{2s}\right) + 6s((8s^2 - n^2\pi^2)sin\left(\frac{kn\pi}{2s}\right) - 8s^2 sin\left(\frac{(k-1)n\pi}{2s}\right))\right] \quad (3.52)$$

Only the 5th Integral in this list (Equation 3.51) is a contribution of this chapter. The other four integrals (Equation (3.48) – (3.52) have been derived by [De Caro and Strollo, 2005].
Only the closed firm of

$$I''''''_{k,n} = \int_{x_k}^{x_{k+1}} 2v_k(x - x_k)^4 sin\left(\frac{n\pi x}{2}\right) dx \tag{3.53}$$

Such a closed form integral result for a quartic DDS has not been described in open literature. The integral $I''''_{k,n}$ has not been derived by [De Caro and Strollo, 2005] and in any of their subsequent papers.

3.3 Analytical model to compute SFDR for Taylor series DDS

SFDR is the most common performance parameter of a DDS used to measure the efficacy of a DDS design. The other measures covered in this chapter are SNR and MAE. The SFDR of a DDS is a function of the ratio of the magnitude of the fundamental divided by the magnitude of the highest spur. The computed ratio is first computed as a logarithm to the base 10 and then multiplied by 10. In this section, an analytical formulation is provided for computation of SFDR for Taylor's series DDS with a fixed number of segments. The objective of performing this exercise is to derive the SFDR for a Taylor's series DDS when the number of segments is known. Such a formulation for a Taylor's series DDS appears not to have been discussed in the open literature.
The analytical expression for the output waveform of Taylor's series DDS considering up to quadratic terms can be written as

$$O_{DDS} = sin\left(\frac{\pi}{2}P\right) = sin\left(\frac{\pi}{2}(u)\right) - sin\left(\frac{\pi}{2}(u)\right)\frac{\left(\frac{\pi}{2}(P-u)\right)^2}{2} + cos\left(\frac{\pi}{2}(u)\right)\left[\frac{\pi}{2}(P-u)\right] \tag{3.54}$$

Equation (3.55) is obtained by substituting $z = \frac{\pi}{2}(P-u)$ in Equation (3.54).

$$O_{DDS} = sin\left(\frac{\pi}{2}(u)\right) - sin\left(\frac{\pi}{2}(u)\right)\frac{(z)^2}{2} + cos\left(\frac{\pi}{2}(u)\right)[z] \tag{3.55}$$

Let the lower limit of the argument in each of k segments be written as u_k , where $0 \leq u_k \leq 1$.
The output of DDS, using [De Caro and Strollo, 2005] model, can be written as

$$O_{DDS} = y_k + m_k(u - u_k) + p_k(u - u_k)^2 + q_k(u - u_k)^3 \tag{3.56}$$

Comparing powers between the RHS of Equations (3.56) and (3.55), one obtains the following polynomial coefficients corresponding to [De Caro and Strollo, 2005] model.

$$y_k = sin\left(\frac{\pi}{2}(u_k)\right); m_k = \frac{\pi}{2}cos\left(\frac{\pi}{2}(u_k)\right); q_k = 0; p_k = -\frac{1}{2}sin\left(\frac{\pi}{2}(u_k)\right)\left(\frac{\pi}{2}\right)^2 \quad (3.57)$$

Assuming, that the quadrant is split into 8 equal intervals, the values u_k can be written as

$$u = \begin{bmatrix} 0 & \frac{1}{8} & \cdots & \frac{7}{8} \end{bmatrix} \quad (3.58)$$

Argument $(P - u)$ in Equation (3.54) will vary between 0 and $1/8$.

Using the values of y_k, m_k, p_k and q_k , one must compute $\alpha_k, \beta_k, \gamma_k, \delta_k$ in accordance with the Equations in [De Caro and Strollo, 2005]. These expressions for $\alpha_k, \beta_k, \gamma_k, \delta_k$ are stated in Appendix A.

SFDR is defined as logarithm of the ratio of the fundamental over the largest spur (in this case the 3rd harmonic). After performing the rest of operations detailed in Appendix A, Equations (A.24 to A.39) the coefficient b_1 and b_3 are computed. The SFDR for Taylor series-based DDS is computed the ratio of the Fourier coefficient fundamental(b_1) to the highest harmonic (b_3).

$$SFDR = 20log_{10}\left(\frac{b_1}{b_3}\right) = 74dB \quad (3.59)$$

Hence, for a Taylor Series DDS with 8 segments the computed SFDR=74dB.

The computed SFDR for Taylor series DDS is a function of the number of segments under consideration. It will increase as the number of segments is increased from $s_e = 8$ onwards. The next sub-section describes a new kind of DDS which is inherently non-sinusoidal- called LHSC.

3.4 LHSC DDS and its SFDR

The equations due to [DeCaro and Strollo, 2005] are used to compute the SFDR of LHSC DDS. The need for a DDS with non-sinusoidal output is to reduce the latency and dynamic power without sacrificing SFDR as compared to cubic polynomial based DDS. A non-sinusoidal DDS does not attempt to create a perfect sinusoidal output. It attempts to generate a periodic wave with minimum dynamic power and minimum latency while controlling the magnitude of the harmonics. Linear

High Segment Count (LHSC) DDS is an attempt to create a minimum power waveform synthesizer with an increased number of segments to achieve an improved SFDR. A type of non-sinusoidal DDS has been considered in this section. In this approach, a high segment count is used. A LHSC DDS divides a quadrant into a minimum of 32 smaller segments or intervals. For each such interval, one must compute a suitable line segment (with appropriate coefficients), to approximate the sinusoid. This is performed by a least squares approach.

This approach has been attempted for $s_e = 32$ and $s_e = 64$. One advantage is that due to the linear approximation the only a three-stage pipeline is required as compared to a five-stage pipeline required for the cubic polynomial DDS (Figure 2.13). Lower depth of pipeline reduces dynamic power (Equation 3.58) and generates lower latency (number of clock cycles required to produce the first output sample). Dynamic power is defined as

$$P = kCV^2f \tag{3.60}$$

In Equation (3.60), C is the overall capacitance of a network, V is the supply voltage, and f is the operating frequency of a circuit. Equation (3.58) is generic and does not pertain to a specific type of circuit. A representation using a line fit within ~~a~~ the k^{th} segment of output waveform of DDS can be written as

$$y_k = C_{3,k}z + C_{4,k} \tag{3.61}$$

In Equation (3.61) $C_{3,k}$ and $C_{4,k}$ are coefficients for the k^{th} segment, argument z is the input argument (phase angle), and y_k is the computed output. For the k^{th} segment the coefficients $C_{3,k}$ and $C_{4,k}$ must be estimated first.

Let the segments (corresponding to a given quadrant) be numbered from 1 to 32($s = 32$). The Equation (2.99b) summarizes the computational procedure to compute coefficients for the k^{th} segment.

That is for each segment $k = 1,2, \ldots 32$, one must compute the coefficients corresponding to that segment. Using the basic principles of Least Squares and Linear interpolation, the matrix form equation to compute the coefficients of the k^{th} segment is written as

$$\begin{bmatrix} \sum_i z_i^2 & \sum_i z_i \\ \sum_i z_i & N \end{bmatrix} \begin{bmatrix} C_{3,k} \\ C_{4,k} \end{bmatrix} = \begin{bmatrix} \sum_i z_i y_i \\ \sum_i y_i \end{bmatrix} \tag{3.62}$$

In Equation (3.62),z_i is the i^{th} instantaneous input phase varying between $\frac{k-1}{s} * (\pi/2)$ and $k/s * (\pi/2)$; where k is the segment number; where y_i is the i^{th} instantaneous output sample of DDS within the k^{th} segment; Where i is the i^{th} sample within a given segment; where N is the number of output samples per segment N; where $C3_k$ and $C4_k$ are the Coefficients for the k^{th} segment (computed)

Once the coefficients for the k^{th} segment are computed by using Equation (3.60), they must be converted into the cubic coefficients form as suggested by [De Caro and Strollo, 2005]. This is to facilitate computation of Fourier coefficients and thereby SFDR. This is performed by expanding powers and comparing coefficients.

$$y_{j,k}(z_{j,k}) = C_{4,k} + C_{3,k}z_{j,k} + C_{2,k}z_{j,k}^2 + C_{1,k}z_{j,k}^3 \tag{3.63}$$

In Equation (3.63) k is the segment number, the index j refers to the sample number within the k^{th} segment.

The Equation (3.63) represents the general way a cubic DDS computation can be performed with

$$z_{j,k} = \frac{(k-1)}{s_e}\frac{\pi}{2} + (j-1)\Delta z_k \text{ where, } \Delta z_k = \frac{\frac{(k)}{s_e}\frac{\pi}{2} - \frac{(k-1)}{s_e}\frac{\pi}{2}}{N/s_e} \tag{3.64}$$

To compute the SFDR, it is necessary to convert coefficients from the form in Equation (3.63) into the form in Equation (3.65).

The expression for DDS output in k^{th} interval using the expression given by [De Caro and Strollo, 2005]

$$y_k(x) = q_k x^3 + (p_k - 3q_k x_k)x^2 + (m_k - 2p_k x_k + 3q_k x_k^2)x + (y_k - m_k x_k + p_k x_k^2 - q_k x_k^3) \tag{3.65}$$

The variable $z_{j,k}$ must be scaled to the variable x which ranges between 0 and 1. This is accomplished by the substitution described in Equation (3.64):

$$x = {}^{z_{j,k}}\Big/_{\frac{\pi}{2}} = z_{j,k}/1.57 = z_{j,k}/c \tag{3.66}$$

The factor $c = 1.57$ is a constant of conversion. Constant c is a scaling factor that maps the range of $z_{j,k}$ into the range of x.

Equating coefficients of power of $z_{j,k}$ between Equations (3.63) and (3.65), one obtains the following connective relations for the coefficients.

$$C_{1,k} = \frac{q_k}{c^3} \implies q_k = c^3 C_{1,k} \tag{3.67}$$

The coefficient is computed as

$$C_{2,k} = \frac{p_k - 3x_k q_k}{c^2} \implies p_k = C_{2,k} c^2 + 3x_k q_k = C_{2,k}\, c^2 + 3x_k c^3 C_{1,k} \tag{3.68}$$

The coefficient $C_{3,k}$ is computed as

$$C_{3,k} = \frac{m_k - 3x_k p_k + 3q_k x_k^2}{c} \tag{3.69}$$

The coefficient $C_{4,k}$ is computed as

$$C_{4,k} = (y_k - m_k x_k + p_k x_k^2 - q_k x_k^3) \tag{3.70}$$

The cubic equation that has been utilized to approximate the DDS output values in a given segment in terms of the variable $z_{j,k}$ can be written as

$$y_{j,k}(z_{j,k}) = C_{4,k} + C_{3,k} z_{j,k} + C_{2,k} z_{j,k}^2 + C_{1,k} z_{j,k}^3 \tag{3.71}$$

In LHSC, the higher power coefficients corresponding to second and third powers of $z_{j,k}$ are 0. That is $(C_{1,k} = 0; C_{2,k} = 0)$ because of the approximation is linear.

Comparing Equation (3.68) with the corresponding DDS output equation given by [DeCaro and Strollo, 2005],

$$\begin{aligned} y_{j,k}(z_{j,k}) = {} & q_k x^3 + (p_k - 3q_k x_k)x^2 + (m_k - 2p_k x_k + 3q_k x_k^2)x \\ & + (y_k - m_k x_k + p_k x_k^2 - q_k x_k^3) \end{aligned} \tag{3.72}$$

Equating coefficients of powers of x in Equations (3.71) and (3.72), the coefficients for LHSC approximation can be written as

$$q_k = c^3 C_{1,k} \; if \; C_{1,k} = 0 \; ; \; q_k = 0 \; for \; all \; k \tag{3.73}$$

$$\Rightarrow p_k = c^2 C_{2,k} + 3xc^3 C_{1,k} \; \; if \; C_{1,k}, C_{2,k} = 0 \; ; \; q_k = 0 \; for \; all \; k \tag{3.74}$$

$$m_k = C_{3,k} c + 2p_k x_k - 3q_k x_k^2 = C_{3,k} c + 2\left(c^2 C_{2,k} + 3x_k c C_{1,k}\right)x_k + 3(c^3 C_{1,k})x_k^2 \tag{3.75}$$

$$m_k = C_{3,k} c \tag{3.76}$$

Similarly, one can write the equations for the coefficient y_k as

$$y_k = C_{4,k} + m_k x_k - p_k x_k^2 + q_k x_k^3 = C_{4,k} + C_{3,k} c x_k \tag{3.77}$$

Through the derivation in Equations (3.73- 3.77), one computes the values of coefficients m_k and y_k.

In this case $p_k = 0$ and $q_k = 0$ for all k (quadratic and cubic terms do not exist since it's a linear approximation).

From the coefficients y_k, m_k, p_k, q_k, the coefficients $\alpha_k, \beta_k, \gamma_k, \delta_k$ must be computed using the in-Appendix A (Equations (A.24-A.31)).

The computed SFDR is the ratio of the first and third harmonic as in this case the other harmonics keep reducing. The computed values of b_1 (the first or fundamental Fourier coefficient) and b_3 (the Fourier coefficient for the third harmonic) for LHSC-64 are written as

$$b_1 = 0.999999991943803;\ b_3 = .000000000032$$

The SFDR is computed by taking the logarithm of the ratio of fundamental and third-order Fourier coefficient as

$$\text{SFDR} = 20\log\left(\frac{b_1}{b_3}\right) = 210\text{dB} \tag{3.78}$$

3.5 A comparison of MAE of Quartic, Cubic, LHSC and Taylor Series DDS

MAE stands for Maximum Absolute Error. The Maximum Absolute Error (MAE) of a DDS is defined as the absolute difference of DDS output versus an ideal sinusoid for the same phase input value. It is one of the performance parameters of a DDS. For any type of DDS, the MAE can be expressed as

$$MAE = Max(abs(\text{DDS output for a given phase input} - \text{ideal sinusoid for the same phase input})) \tag{3.79}$$

For a cubic polynomial DDS Equation (3.79) can be written as

$$MAE = Max(abs\left(DDS\_out(z_j) - Ideal((z_j)\right)) \tag{3.80}$$

In Equation (3.80),

$$DDS\_out(z_j) = C_{4,k} + C_{3,k} z_j + C_{2,k} z_j^2 + C_{1,k} z_j^3 \tag{3.81}$$

$DDS\_out(z_j)$ is the DDS output for a cubic DDS with the phase argument z_j

$$Ideal((z_j) = \sin(z_j) \tag{3.82}$$

$Ideal((z_j)$ is the ideal sinusoidal output for the same phase argument z_j

The range of input phase arguments for application of Equation (3.80) and (3.82) is $0 \leq z_j \leq \pi/2$

For the DDS designs, the points selected to compute the MAE include all the points within a segment and at the boundaries of a segment. The absolute error of any of the DDS proposed in this section depends on the segment under consideration and the specific part of the segment. This is because coefficients are always computed for a given DDS on a per segment basis. Therefore, MAE of a DDS design depends on the accuracy of the coefficients. To capture the MAE over an entire quadrant and to observe the variation of MAE, all the points for the DDS, 16384 points for a DDS with $s_e = 32$ and 512 samples per segment must be included in the MAE analysis.

Figure 3.5 is a comparative MAE curve including the cubic DDS with $s_e = 32$, Quartic DDS ($s_e = 32$), LHSC DDS ($s_e = 32$) and Taylor series-based DDS ($s_e = 32$). The importance of Figure 3.5 is that it illustrates the variation of the MAE as the number of segments is varied across 4 different types of DDS.

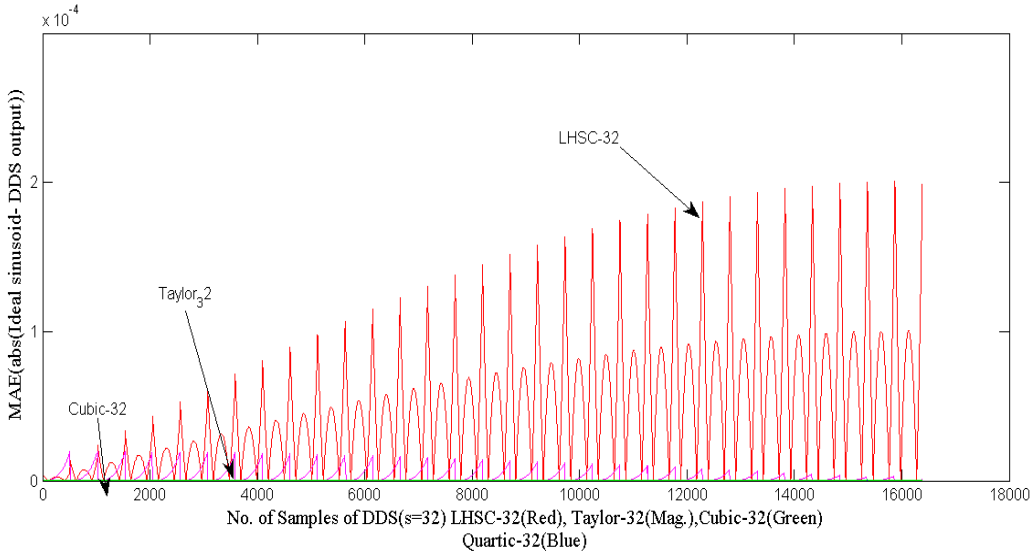


Figure 3.5 Comparative MAE for LHSC-32 DDS, Taylor Series DDS ($s_e = 32$), cubic DDS (s_e=32) and Quartic DDS ($s_e = 32$) with 16384 samples/segment

A comparative MAE of the 4 different types of DDS (Figure 3.5) is not to be found in the open literature, and this plot is an original contribution.

3.6 Definition and Classification of Dither

This section deals with fundamental definitions and a broad classification of dither signal. Dithering is a requirement in DDS to suppress unwanted frequencies at the output of the DDS. Dither can be defined as a random signal with a specified Probability Density Function (PDF) and Characteristic Function (CF) which can be added to a deterministic signal. The variation of a dither signal is not defined with respect to time, and this distinguishes it from a general periodic or aperiodic signal.

Dither is a type of signal which is defined exclusively by its probability density and amplitude, it has no defined frequency. The CF of a random variable completely characterizes the probability distribution and the moments of the random variable. The CF is the Fourier transform of probability density function. The deterministic signal can be an input to a quantizer, ADC, DAC or DDS output. A quantizer is a device that performs quantization. It maps a single sample of an analog input signal into one of many equally spaced digital signal levels. A quantizer is a device converts an incoming analog signal into one of multiple levels. The process performed by a quantizer which maps a given analog signal into one of many levels, is known as quantization. Quantization error is the difference between the quantizer output and quantizer input. The quantization error is not uniform over a quantizer interval.

Random variable $X(\mu)$ is a single-valued real function that assigns a real number called the value of $X(\boldsymbol{\mu})$ to each sample point μ of S where S is the sample space of an experiment. Random signal is the value of a random variable varying over time. The probability mass function of a random variable is formally defined as

$$F_X(x) = P(X \leq x) \tag{3.83}$$

In Equation (3.83), X is the Random variable and x is one value of the random variable. Operator P in Equation (3.79) the probability that the value of x is greater or equal to X.

The Probability Density Function (PDF) of a random variable is the derivative of its Probability Mass Function or PMF [Hsu, 2005]. The integral of the PDF of a continuous random variable over its entire range equals unity.

The Characteristic Function (CF) of a random variable is the Fourier transform of its PDF, the Fourier integral being computed over the entire range of the random variable. In case of rectangular (uniform) dither, the CF is expressed using the Fourier integral in Equation (3.80),

$$M_W(ju) = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} \frac{e^{jux}dx}{\Delta} = \frac{1}{\frac{\Delta}{2}j2u}\left\{e^{ju\frac{\Delta}{2}} - e^{-ju\frac{\Delta}{2}}\right\} = sinc\left(\frac{u\Delta}{2}\right) \tag{3.84}$$

In Equation (3.84), the range $\left(\pm {}^{\Delta}/_{2}\right)$ is the range of dither. Variable u is the argument of the Characteristic Function (CF), where variable W is the uniformly distributed random variable; the variable $M_W(ju)$ is the CF of the function W with an argument(u),

The other related definition is a m^{th} order moment of a random variable, which is defined as

$$\mathrm{E}(x^m) = \int_{-x1}^{x1} f(x)\, x^m dx \tag{3.85}$$

In Equation (3.85), $\mathrm{E}(x^m)$is the m^{th} moment of the random variable x. To convert CF of a random variable to the moments of the random variable ($\mathrm{E}(x^m)$), one must compute the appropriate order of derivative of the CF at an argument value ($u = 0$).

This is because of the fundamental expression given by [Papoulis, 2005 and Hsu, 2013]:

$$\mathrm{E}(x^m) = \frac{d^m}{du^m}\left(M_X(ju)\right)\Big|_{u=0} \tag{3.86}$$

Equation (3.86) states that the m^{th} moment of a random variable is the m^{th} derivative of its characteristic function with the CF argument being set to zero. The constant $j = \sqrt{-1}$ and variable u is the argument of CF.

3.6.1 Rectangular and Triangular Dither

This classification is based on the probability density of dither. Rectangular dither is uniformly distributed that is the probability density of the dither signal is uniform over a quantization interval. A representative illustration of a Rectangular dither is shown in Figure 3.6. The CF of rectangular dither is a $sinc$ function.

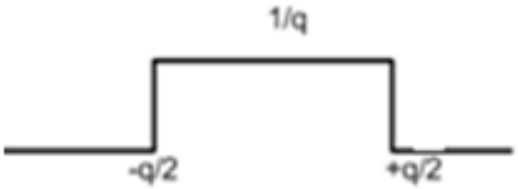


Figure 3.6 PDF of Rectangular Dither

Following [Kollar, 2005] the CF of rectangular dither can be written as

$$CF_{RECT}(q,u,L) = \frac{sin\frac{qu}{2}}{2^{L}\sin(2^{-L}\frac{qu}{2})} \tag{3.87}$$

In Equation (3.87), L is the bit length of the dither generation function, Pseudo Random Binary Sequence (PRBS). L is really the number of bits used to represent a dither signal whose amplitude varies between $-q/2\ and\ q/2$. $L = \log_2\left(\frac{q}{q_d}\right).q_d$ is defined as dither least significant bit (LSB)[Kollar,2005]. Equation (3.83) is originally defined by Kollar.

A triangular dither implies the dither signal is distributed with the highest value of probability density at the center of the interval and drops off linearly towards the edge of the quantization interval (Figure 3.7), and the CF of triangular dither is a $sinc^2$ function.

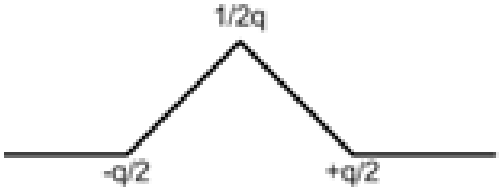


Figure 3.7 PDF of Triangular Dither

The quantization interval is the range of input in a mid-tread quantizer. A mid-tread quantizer is a device in which if and only if the magnitude of the input value equals or exceeds $[q/2]$, its output changes from zero to a $q/2$ value. Its output is equal to $q/2$ if and only if the input to the quantizer

exceeds $q/2$. The value q is known as the quantization interval. The value $q/2$ can be directly related to the number of output bits of the quantizer, which corresponds to one output value.
CFs are important tools in the analysis of dithered systems as illustrated in [Wanamaker ,1990], [Gray ,1993] and [Gray ,1990]. The next subsection illustrates the difference between additive and subtractive dither.

3.6.2 Additive and subtractive dither

One classification of dither is based on the nature of combining operation performed on the original dither signal. Additive dither (also referred to be as non-subtractive) refers to a system or procedure where the dither is added to a signal and never removed subsequently. [Wanamaker, 2003] and [Gray, 1993] refer to additive dither as non-subtractive dither. Figure3.8 is the block diagram of and ADC with an additive analog dither.

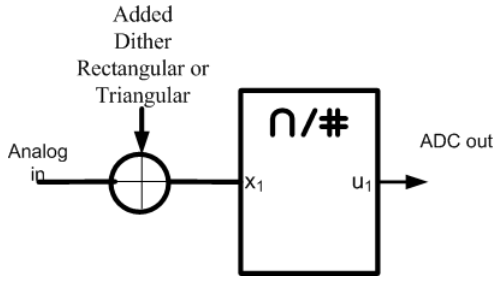


Figure 3.8 Block diagram of ADC with additive analog dither

Subtractive dither refers to a system where the dither signal is added at one stage and subtracted at a subsequent stage of processing, typically before and after quantization. This model of dither injection is known as the subtractive dither model. The subtractive dither requires perfect synchronization of the operations of addition and subtraction.

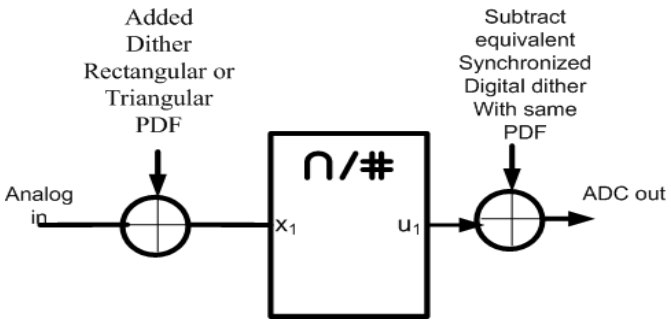


Figure 3.9 Block diagram of ADC with subtractive dither

In Figure 3.9, an analog dither signal is added before the ADC (quantizer) and the same signal in digital form is subtracted after the ADC (quantizer). To make a subtractive dither work, the dither signals (before and after quantization) must be synchronized and be of the same dynamic range. Besides, they must possess the same CF. Subtractive dither has positive stochastic properties [Gray, 1993] only in case the addition and subtraction are synchronized. The added dither at the input of ADC is a continuous time signal but the signal subtracted at the output of the ADC is a discrete time signal but with same CF and dynamic range. The contributions in this chapter in Section 3.7 utilize additive dither.

3.6.3 Phase, Amplitude and Phase + Amplitude dither

Phase dithering refers to the addition of a dither signal before the conversion from Phase angle to magnitude in a DDS. Amplitude dithering refers to the addition of a dither signal after the conversion from Phase angle to magnitude in a DDS.

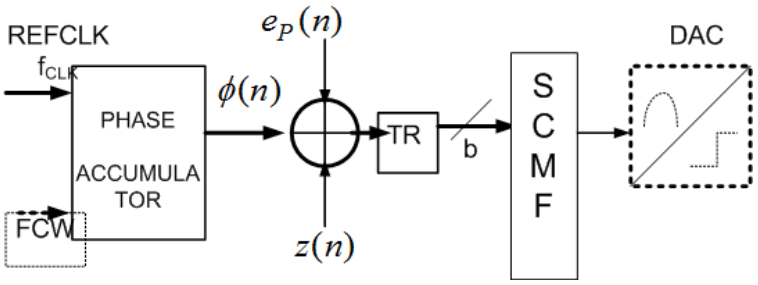


Figure 3.10 Phase dither before phase to amplitude conversion in DDS

Phase dithering scheme shown in Figure 3.10 comprises a Phase Accumulator (PACC), an addition block where both the phase dither $z(n)$ and the phase quantization error $e_P(n)$ are added, A Sine-Cosine Mapping Function (SCMF) which converts the dithered phase word into a time varying amplitude, and finally a DAC. The phase dither signal $z(n)$ can have a rectangular PDF or a triangular PDF. DDS designs can have both phase and amplitude dither added as illustrated in Figure 3.11.

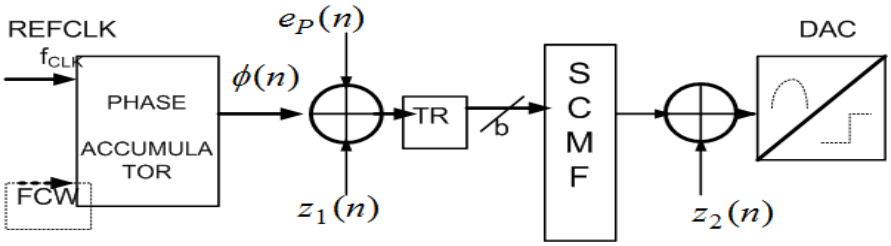


Figure 3.11 DDS with both amplitude and Phase dither addition

Figure 3.11 illustrates a DDS where dither addition is performed both before the phase to amplitude conversion and after the phase to amplitude conversion. The structure illustrated in Figure 3.11 shows a Phase Accumulator (PACC) which generates a phase word $\phi(n)$. Phase dither $z_1(n)$ is added to the phase word. The phase quantization error $e_P(n)$ is shown to be added at the output of the PACC.

The phase word undergoes phase truncation (where the lowest bits are truncated or ignored) in the TR block. The output of the phase truncation step is passed as an input to the SCMF (Sine-Cosine Mapping Function) block which converts the phase information into amplitude of a sinusoid amplitude. Amplitude dither signal $z_2(n)$ is added at the output of the SCMF block. The amplitude with added dither forms the input to a DAC. The dither signal $z_1(n)$ is the added phase dither and the signal $z_2(n)$ is the added amplitude dither. The added phase and amplitude dither can be uniformly distributed (rectangular) or triangular. The next section summarizes prior papers on dither.

3.7 A review of prior research on Dither

This section summarizes prior research studies on dither. [Schuchman, 1964] was one of the earliest contributors to Dither. He established that in a dithered quantizer, the CF of dither will attain value of zero at integer multiplies of quantization interval in order that the quantization noise can be statistically independent of the signal. This is known as *Schuchman's condition,* and subsequent authors have used this condition. DDS generates many different types of Spurs (Spurious Frequencies). One of the types of Spurs is the Phase Truncation Spurs [Olsen, 1985] and [Mehrgardt, 1990]. [Olsen, 1985] and [Mehrgardt, 1990] have computed the location and magnitudes of phase truncation spurs in DDS. These are some spurs one wants to mitigate using dithering techniques.

[Reinhart, 1995] has illustrated the addition of a random word to the *Phase accumulator output*. This is referred to as phase dither. Reinhart has discussed *Randomized DAC dither,* which is termed amplitude dither – where a random word is added at the output of a ROM based DDS before the result is truncated.

The following references in this section pertain to Hartley Image suppressor and Adaptive filtering for Spur suppression.

[Chen and Huang, 2001] have described and image-reject Hartley architecture which incorporates a multistage Hartley image rejection receiver, which is cascaded and provides two outputs. The first output enhances the desired signal and the second output enhances the image signal. Multiple image rejection receivers are cascaded, and the final output of the cascade is driven into a final block, which performs digital signal rejection. Their architecture can be built using hybrid analog and digital components and achieves an image rejection > 60dB.

[Kim and Shin, 2002] have proposed a composite image rejection and spurious rejection architecture, which achieves an Image Rejection Ratio (IRR) > 70dB. Image rejection ratio is defined as the ratio of a desired signal to the image signal.

[Iqbal, 2004] has improved the basic Hartley based image rejection circuitry by the addition of an analog self-calibration scheme. His proposed scheme improves the image rejection by 59 dB.

[Chang and Bibyk, 2005] have modified the traditional Hartley image reject architecture to add two sigma-delta ADCs and convert the filter outputs to digital bit streams. These digital bit streams

enable the usage of a digital phase shifter in the Hartley receiver which is less susceptible to process and temperature variations.

[Widrow et. al., 1975] were one of the earliest to address the problem of removing unwanted power signals (60Hz) from ECG signals. The authors explain the theory of the adaptive notch filter and provides the simplified expressions for the transfer function of an adaptive notch filter.

[Martens et al., 2006] address the issue of variable amplitude and random phase power line interference (50-60 Hz) in ECG signals. The architecture proposed by the authors tracks amplitude and frequency and phase of all interference components in an ECG signal by using a PLL type structure to correct for harmonics with varying amplitude and phase. The weight vector is split into two parts corresponding to amplitude and phase observations. This approach completely suppresses spurs at 150 Hz. The next section details the extension the theory of phase-dithered DDS.

3.8 A new derivation of the SpSR of a phase-dithered DDS

In this section an extension to the theory of phase-dithered DDS in [Flanagan and Zimmerman, 1995] has been discussed. This section uses SpSR as a performance parameter of DDS. SpSR is defined as total energy dues to spurs divided by the energy in the fundamental expressed in dB as suggested by [Flanagan and Zimmerman, 1995].

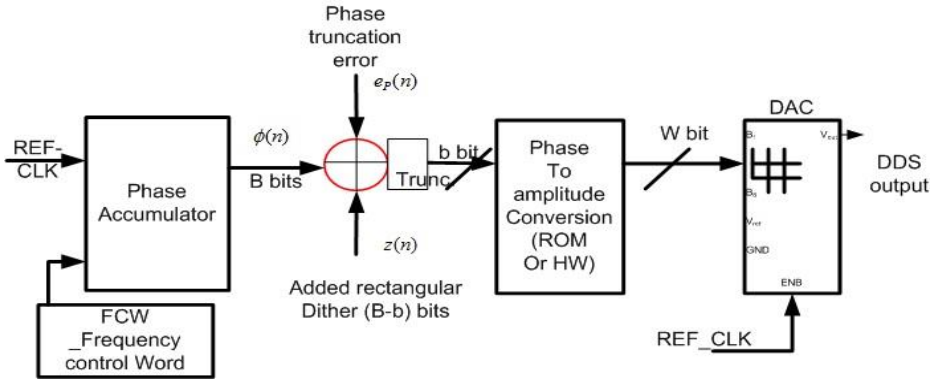


Figure 3.12 DDS design with phase dither addition and truncation of phase word

The DDS described by [Flanagan and Zimmerman, 1995] comprises four major blocks as shown in Figure 3.12. The first block is a phase accumulator which has a frequency control word as an input. The output of the phase accumulator is synchronized with a high-frequency reference clock

and is fed to a dither addition block. The phase accumulator output is a phase word representing and angle between 0 and 2π. The output of the dither addition block is truncated from B to b bits and is an input to the Phase to Amplitude Conversion (PAC) block, usually a ROM. The output of the PAC block forms an input to a DAC. [Flanagan and Zimmerman, 1995] proposed an additive model of the phase error, as a summation of dither $z(n)$ and phase error $e(n)$ was proposed. Rectangular phase dither is added to the DDS. Phase quantization occurs in DDS due to the finite word-length of the phase word. The phase quantization noise refers to additional noise at the output of the phase accumulator block before and after dither addition. The phase truncation noise is also referred to as phase quantization noise. The phase truncation noise is reflected in the output spectrum of the DDS as spurs. The first contribution of [Flanagan and Zimmerman, 1995]is the generation of uniformly distributed dither (without regard to word-length) using a PN sequence generator. The second contribution of Flanagan was the replacement of the original infinite resolution white dither with uniformly distributed periodic dither.

[Flanagan and Zimmerman, 1995] computes the auto-correlation of added dither $z(n)$, which is a finite series of weighted exponentials and simplifies the autocorrelation expression of $z(n)$ to an infinite series based on expression of [Schuchman,1965] for CFs. The first assumption of [Flanagan and Zimmerman, 1995] is that the first moment of the total quantization noise is zero which is captured in Equation (3.88).

$$E\big(\varepsilon(n)\big) = 0 \tag{3.88}$$

The second assumption of [Flanagan and Zimmerman, 1995] is that the total quantization noise is spectrally white. This will hold when added dither values $z(n)$ are independent of the lag m**.** The lag m is the shift in terms of samples considered for the autocorrelation:

$$E\big(\varepsilon(n)\varepsilon(n+m)\big) = \delta(m) \tag{3.89}$$

Equation (3.89) shows the autocorrelation of quantization noise ($\varepsilon(n)$) for a sample shift of m. The right-hand side is the delta function, $\delta(m) = 1$ if $m = 0$ and $\delta(m) = 0$, otherwise. The quantity $p(n)$ is a scaled distance that determines the second order moment of the quantization noise

$$E\big(\varepsilon^2(n)\big) = \Delta_P^2\big(p(n) - p^2(n)\big)\ \ \Delta_P = {}^{1}\!/_{2^b} \tag{3.90}$$

In Equation (3.90), $\Delta_P = {}^{1}\!/_{2^b}$ where b is the truncated bit-width of the phase accumulator (Δ_P=Phase Quantizer step size)

The variable $p(n)$ is the difference of unquantized phase value to nearest quantized phase value scaled by the quantization step size. The expression for SpSR derived in [Flanagan and Zimmerman ,1995] is represented as

$$SpSR_{Flanagan}(b) = \left(\frac{\pi^2 \Delta_P^2}{4}\right)^2 \tag{3.91}$$

While deriving the Equation (3.91), only second moment of $\varepsilon(n)$ was considered. In this section, modifications to Equation (3.91) considering higher order moments of $\varepsilon(n)$ are also considered to obtain an alternative expression for signal expectation and SpSR. The output waveform expression given by [Flanagan and Zimmerman, 1995] is written as

$$x(n) = \cos(2\pi f n + \Phi + \varepsilon(n)) \tag{3.92}$$

In Equation (3.92), $x(n)$= n^{th}output sample, Φ is the Initial phase angle of DDS, and $\varepsilon(n)$ is the n^{th}sample of the total quantization noise. By applying expectation operator to Equation (3.92), one can obtain expression for the moments. [Flanagan and Zimmerman,1995] substitutes the Taylor expansions of the total quantization noise, and the same approach is followed in this chapter. Considering Taylor's expansion for the cosine of the total quantization noise and retaining only the first two terms are shown in the equation:

$$E(\cos(2\pi\varepsilon(n)) = 1 - 2\pi^2\{E(\varepsilon(n))\}^2 + \cdots. \tag{3.93}$$

The Taylor expansion for the sine function of quantization noise can be simplified by considering only the first two terms as

$$E(\sin(2\pi\varepsilon(n)) = E(2\pi\varepsilon(n)) - E\left(\frac{(2\pi\varepsilon(n))^3}{3!}\right) + \ higher\ terms \tag{3.94}$$

Since the quantization error is a zero-mean process,$E(\varepsilon(n)) = 0$, the RHS of Equation (3.94) is simplified as

$$E(\sin(2\pi\varepsilon(n)))) = E(2\pi\varepsilon(n)) - \frac{1}{3!}E((2\pi\varepsilon(n))^3) = -\frac{8\pi^3}{6}E((\varepsilon(n))^3) \tag{3.95}$$

Substituting for the expected values for the sine and cosine functions of the quantization error into the RHS of Equation (3.92), the expression for the expectation of the output signal of DDS is further expanded as

$$E(x[n]) = cos(2\pi f n + \Phi)\, E(cos(2\pi\varepsilon(n)) - \ sin(2\pi f n + \Phi)E(sin(2\pi\varepsilon(n)) \tag{3.96}$$

Substituting the values of $\cos(2\pi\varepsilon(n))$ and $\sin(2\pi\varepsilon(n))$, Equation (3.92) is rewritten as

$$E(x[n]) = cos(2\pi fn + \Phi)\left\{1 - 2\pi^2\left\{E\left(\varepsilon(n)\right)\right\}^2\right\} - sin(2\pi fn + \Phi)\left\{-\frac{8\pi^3}{6}E\left(\left(\varepsilon(n)\right)^3\right)\right\} \quad (3.97)$$

with the first-order moment of total quantization noise written as

$$E\left(2\pi\varepsilon(n)\right) = 0 \quad (3.98)$$

The second-order moment of quantization error is written as

$$E(\varepsilon^2(\mathrm{n})) = \frac{(\Delta_\mathrm{P})^2}{8} \quad (3.99)$$

The third-order moment of quantization error is written as

$$E(\varepsilon^3(\mathrm{n})) = [p(n)\Delta_\mathrm{P}]^3\left(1 - p(n)\right) + [(1 - p(n))\Delta_\mathrm{P}]^3\left(p(n)\right) \quad (3.100)$$

One can obtain an estimate of the worst-case amplitude of quantization noise by maximizing the third-order moment of $\varepsilon(n)$. The condition for the maxima is given in Figure 3.13 which is a plot of the third-order moment versus the range of p.

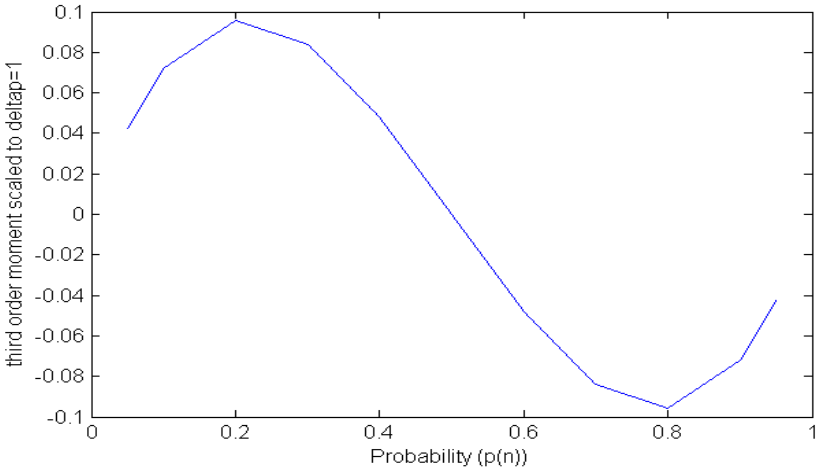


Figure 3.13 Scaled value of Third-order moment of quantization error, $E(\varepsilon^3)$ scaled by versus probability, $p\,(n)$

The X- axis of Figure 3.13 is the parameter $p(n)$, and the Y-axis is the scaled value of the third-order moment of quantization error ($E(\varepsilon^3(n))$). The maximal value of the third-order moment of quantization noise occurs at $p(n) = 0.17$.

The maximal value of the third-order moment can be derived by setting the derivative of the third order moment to zero:

$$\frac{\partial E(\varepsilon^3(\mathrm{n}))}{\partial p(n)} = 0 \tag{3.101}$$

This implies upon taking derivative of Equation (3.101):

$$\frac{\partial}{\partial p(n)}\left\{p(n)^3 - p(n)^4 + \left(1 - p(n)\right)^3 p(n)\right\} = 0 \tag{3.102}$$

Simplifying the condition expressed in Equation (3.102) with $p(n) = 0.17$, the derivation for the maximal condition of the third-order moment is expressed as

$$E(\varepsilon^3(\mathrm{n})) = [\Delta_\mathrm{P}]^3\big(1 - p(n)\big)p(n) + p(n)(1 - p(n\,))[\Delta_\mathrm{P}]^3 = 0.1[\Delta_\mathrm{P}]^3 \tag{3.103}$$

Substituting the second-order and third-order moments from Equations (3.98) and Equation (3.99) into Equation (3.97), the RHS of Equation (3.97) is simplified further as

$$E(x) = \cos(2\pi fn + \Phi)\{1 - 2\pi^2 E(\varepsilon^2)\} - \sin(2\pi fn + \Phi)\left\{-{}^{8}\!/_{6}\,\pi^3 E(\varepsilon^3)\right\} \tag{3.104}$$

Substituting the second and third moments of $\varepsilon(n)$, the expression for the expectation of the output signal of DDS is written as

$$E(x) = \cos(2\pi fn + \Phi)\left\{1 - 2\pi^2\,{}^{\Delta_\mathrm{P}^2}\!/_{8}\right\} + \sin(2\pi fn + \Phi)\left\{{}^{8}\!/_{6}\,\pi^3 0.1\Delta_\mathrm{P}^3\right\} \tag{3.105}$$

Where $\Delta_P = {}^{1}\!/_{2^b}$ where b is the truncated bit-width. From the Equation (3.105), a new expression for SpSR, the ratio of spurious power to signal power at DDS output can be derived as

$$SPSR\ \text{Modified} = \frac{Spurious\ Power}{Signal\ Power} = \frac{\left\{\left(\frac{\pi^2\Delta_\mathrm{P}^2}{4}\right)^2 + \left(\frac{8\pi}{6}\pi^3 0.1\Delta_\mathrm{P}^3\right)^2\right\}}{1} \tag{3.106}$$

Taking logarithms of both sides of Equation (3.106), one can write:

$$Mo\_SPSR = 10log_{10}(SPSR\ \text{Modified}) \tag{3.107}$$

The additional term in the numerator of Equation (3.106) is because the third-order moment has been considered. The expression for SpSR as derived by [Flanagan and Zimmerman, 1995] is written as

$$SpSR_{Flanagan}(b) = \left(\frac{\pi^2\Delta_\mathrm{P}^2}{4}\right)^2 \tag{3.108}$$

The RHS of Equation (3.108) is a function of the truncated bit-width 'b' as $\Delta_P = {}^{1}\!/_{2^b}$

The RHS of Equation (3.108) is the SpSR computed in accordance with [Flanagan and Zimmerman, 1995]. SpSR must be expressed in dBc. Upon taking logarithms of both sides of Equations (3.106) and (3.108) and multiplying by 10, the relationship between the SpSR computation performed in this chapter and that performed by [Flanagan and Zimmerman, 1995] is obtained. *Modified_SpSR* is used to denote the SpSR as computed in this chapter. *FZ_SpSR* which is the same as $SpSR_{Flanagan}(b)$ in Equation (3.104) is used to denote the SpSR as computed by [Flanagan and Zimmerman ,1995].

Equation (3.108) can be further simplified by taking logarithms and substituting $\Delta_P = 1/2^{-b}$. After simplification, the right-hand side of Equation (3.108) can be written as

$$10log_{10}(FZ\_SpSR) = 7.845 - 12b \tag{3.109}$$

The relationship between the SpSR as derived by [Flanagan and Zimmerman, 1995] and the *Modified_SpSR*(which is the result of Equation 3.107) derived in this chapter can be written as a single expression:

$$10log_{10}(Mo\_SPSR) = 10log_{10}(FZ\_SPSR) + 10log_{10}\left(1 + 16 * 0.133 * \pi\left(\frac{1}{2^b}\right)^2\right) \tag{3.110}$$

Figure 3.14 illustrates the variation of SpSR computed using the Equation (3.109) (*SpSR_FZ*) and Equation (3.110) (Mo_SPSR). The observable differences between the $SpSR\_FZ$, computed using the Equation (3.109) and Mo_SPSR, computed using Equation (3.110) are at lower range of bit width between 2 and 6.

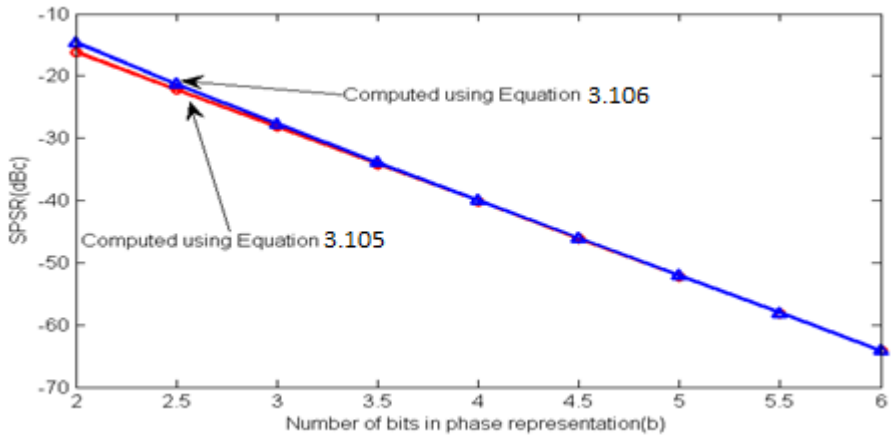


Figure 3.14 Plot of SpSR vs. bit width(b) illustrating where the SPSR really differs

A comparison of the modified SpSR and SpSR derived through [Flanagan and Zimmerman's, 1995] expression is illustrated in Figure 3.14. The blue track is calculated by using the Equation (3.110) and the Figure 3.14 are original contributions of this thesis. The red track is computed using Equation (3.109).

3.9 SFDR improvement and Spur filtering using Hartley image suppressor

This section presents a review of a Hartley image reject receiver (also known as a Hartley suppressor or Hartley image suppressor) and its application for the reduction of the presence of unwanted spurs at the output of a DDS. Hartley image reject receiver is widely used in receiving chain of RF receivers. A block diagram of Hartley image reject receiver is shown in Figure 3.15. Hartley image suppressors are used in RF frequencies using analog phase shifter. In a digital version, the analog phase shifter must be replaced by a Hilbert Transformer. A digital version of the Hartley suppressor can suppress the dominant spur of DDS occurring at a specified spur frequency. The spur frequency of DDS is analogous to image frequency in a conventional RF receiver. The adaptation of Hartley Image suppression technique to improve the SFDR of DDS is a contribution of this chapter and such a recourse appears to have not been addressed in open literature.

Figure 3.15 Block diagram of the Hartley suppressor [Razavi, 2005]

A Hartley image rejection receiver (Figure 3.15) has two branches driven by a common input (DDS output in Figure 3.15), each comprising a multiplier(mixer) and a Low Pass Filter (LPF). The multipliers (mixer) in both branches are fed by a Quadrature Local Oscillator (LO) whose

output frequency is midway between the first and third harmonic (the third harmonic acts as the image frequency of signal and the third harmonic must be suppressed). The preferred LO frequency is selected to lie midway between the fundamental and the image frequency. At node A of LPF1 (Figure 3.15), the output waveform can be written as

$$\nu = \frac{A_f}{2}\sin\left(\omega_{LO} - \omega_f\right)t + \frac{A_h}{2}\sin(\omega_{LO} - \omega_h) \tag{3.111}$$

In Equation (3.111), ω_{LO} is the output frequency of the quadrature oscillator, ω_f is the fundamental frequency of the DDS output (input to Hartley Image suppressor), $\omega_h$is the Image frequency of the DDS output (input to Hartley Suppressor) , A_f is the Signal amplitude at the fundamental frequency, and A_h is the Signal amplitude at the image frequency

At node B of LPF2 (Figure 3.15), the output waveform can be written as

$$\eta = \frac{A_f}{2}\cos\left(\omega_{LO} - \omega_f\right)t + \frac{A_h}{2}\cos(\omega_{LO} - \omega_h)\,t \tag{3.112}$$

The signal ν (Equation 3.111) is phase shifted by 90^o (digitally) through a Hilbert Transformer. The phase shifted output at node C (Figure 3.15) can be written as

$$K_C = \frac{A_f}{2}\cos\left(\omega_f - \omega_{LO}\right)t - \frac{A_h}{2}\cos(\omega_{LO} - \omega_h) \tag{3.113}$$

The output Y of the Hartley image suppressor, which is the phasor summation of ν and K_C comprises only the fundamental component after the cancellation of the image frequency component ($A_h/2$).

A DDS system must suppress spurs at the output of DDS before the spur reaches the DAC. In a digital Hartley suppressor, the two LPFs in Figure 3.15 are implemented as digital LPFs with narrow transition band and high stop-band attenuation. The 90^o phase shift must be accomplished through a digital Hilbert Transformer, which is a high order Finite Impulse Response (FIR) filter. In practice, the Hilbert Transformer's function is accomplished by a 64th order FIR filter in Sysgen™ (Figure 3.16). It was established through simulations that is not possible to achieve exact 90^o phase shift by using a lower order FIR filter. To achieve any image cancellation, an exact 90^o phase shift is necessary, and the Hilbert transformer needs to facilitate it. FDAtool™ from Matlab® was used to design the Hilbert Transformer.

In Figure 3.15 and subsequently in this section, the term *spur* refers to the image frequency. The term spur suppression wherever it is used is the same as an image suppression.

Following [Younous, 2004] and [Joo, 2004], the Hartley image suppressor for a DDS (Figure 3.16) comprises a local quadrature oscillator. Notably, the quadrature oscillator must have a frequency twice as high as the DDS output frequency. Besides, the Hartley image suppressor features two LPFs, a phase shifter to provide 90^{o} phase shift on one branch and a signal combiner(adder). The DDS output (which consists of fundamental and one or more spurs after conversion into analog) is fed directly to the input of the Hartley Image suppressor. The output is obtained at node Y (Figure 3.15) through the summation of the outputs of two branches. The quadrature oscillator is a Numerically Controlled Oscillator (NCO) whose FCW is shared with the original DDS and is always double the value being used by the original DDS. A change in the FCW of the original DDS immediately alters the FCW of the quadrature oscillator in the Hartley image suppressor**.** The Taylor series DDS generates the fundamental and the third harmonic, and the frequency of the LO can be centered exactly to lie between the first and third harmonics which is a feature of Hartley suppressor. Positioning the frequency of the quadrature oscillator frequency exactly between the first and third harmonic leads to better spur suppression of DDS. Digital elliptic filters are exactly replicated for both branches, and this ensures that mismatched LPFs do not cause phase and amplitude mismatches. Figure 3.16 shows the Hartley Spur suppressor implemented in Simulink™ in terms of discrete blocks.

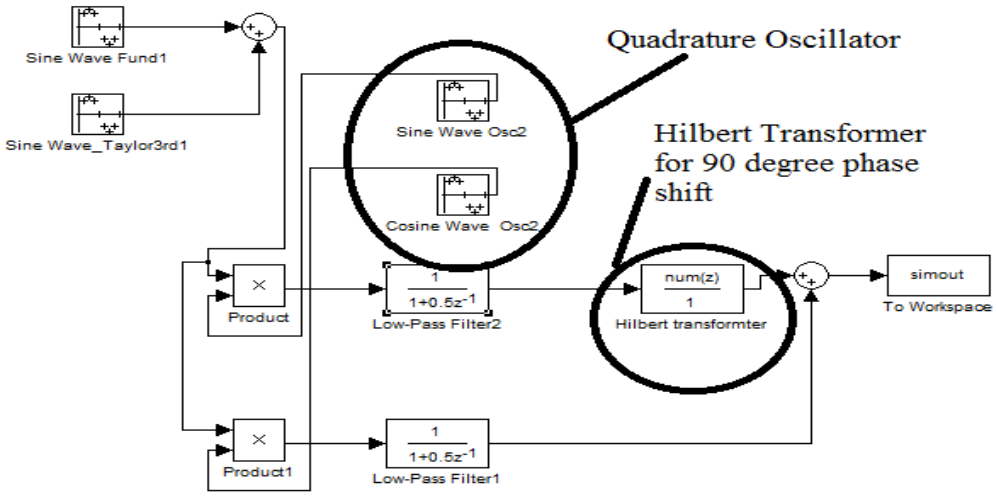


Figure 3.16 Block diagram of Hartley Spur suppression circuit with digital low pass filters and Digital Hilbert Transformer

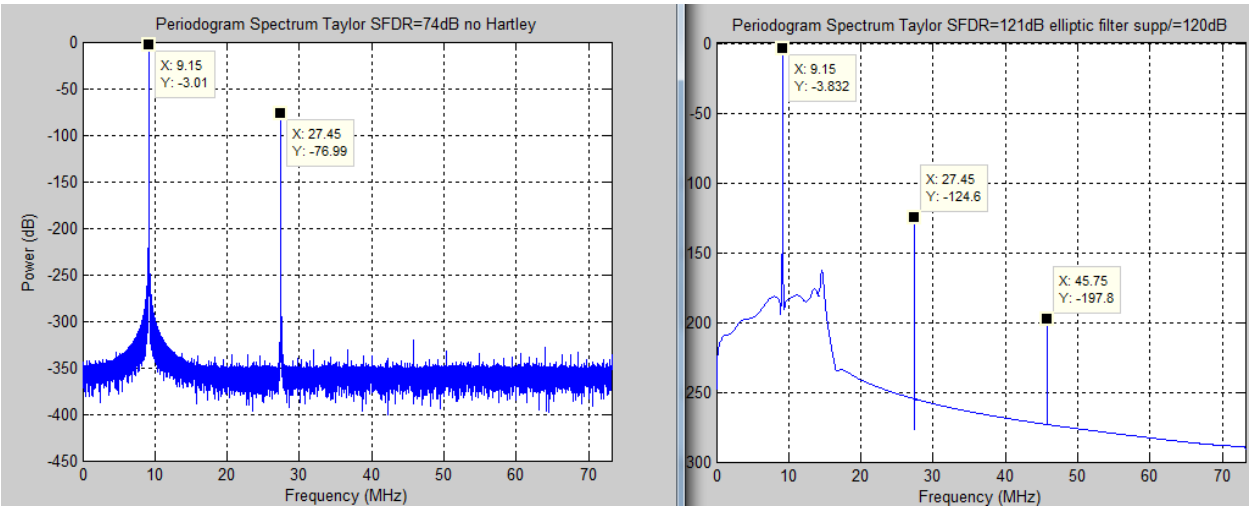
Figure 3.16 performs a Hartley spur suppression using all discrete time filters, discrete time input sources, digital local oscillator and a digital Hilbert Transformer. A discrete time FIR filter performs the task of generating a 90-degree phase shift called a digital Hilbert Transformer [Lyon, 2003]. The DDS output into the Hartley block is on the far left side which as a fundamental plus a third harmonic. These two blocks are marked in Figure 3.16 as DDS output w/ 3rd harmonic. The local oscillator (marked Quadrature Oscillator) produces sine and cosine version at the same input frequency, and the DDS output is multiplied and 'mixed' in two different multipliers. The outputs of both the multipliers are low-pass filtered and the one low pass filtered signal is phase shifted by 90 degrees using a Hilbert Transformer. The final output of block Figure 3.16 is a single signal with the third harmonic suppressed.

Table 3.1 illustrates that the LPFs must feature high stop-band suppression to achieve high SFDR. The usage of low-order IIR filters to implement LPF can achieve high SFDR improvement at a fraction of the power. A Hartley image suppressor has been implemented in a Xilinx Virtex6™ FPGA using LPFs with FIR (Implementation is described in chapter 6).

Table 3.1 SFDR of DDS with and without Hartley image suppressor

Type of DDS	**Original SFDR without Hartley (dB)**	**Final SFDR with Hartley (dB)**	**Stop Band Attenuation of LPF (dB)**
Taylor series DDS	74dB	79dB	80dB
Taylor series DDS	74dB	120dB	120dB

Table 3.1 leads to the conclusion that significant improvement in SFDR is possible for Taylor series DDS. When IIR filters are used with 120dB stop band attenuation, the maximum possible improvement in SFDR is 46 dB (74 dB to 120 dB). Figures 3.17a and 3.17b illustrate the PSD at the output of digital Taylor series-based DDS with and without Hartley Image suppressor (f_0=9.15 MHz).



(a) SFDR=74dB without Hartley Suppressor **(b)SFDR=120 dB with Hartley**

Figure 3.17 Comparison of SFDR of Taylor Series DDS with and without Hartley Image Suppressor (Stop Band Attenuation of Filter=120 dB)

The cutoff frequency for the elliptic IIR filter to generate the results of Figure 3.17 is set to 27.5MHz. An FPGA implementation model of the Hartley supressor is provided in chapter 6. Table 3.2 illustrates the different components of power dissipation of a Hartley suppressor.

Table 3.2 Power Dissipation of the Hartley Image suppressor with FIR filters (30th order)

Clocks (mW)	Logic (mW)	Signals (mW)	DSP (mW)	Dynamic Power(mW)	Leakage Power(mW)	Total Power-Leakage+ Dynamic (mW)
51	58	81	225	445	335	821

In Table 3.2, it is observed that the dynamic power dissipation can be quite high because of the DSP blocks (which are signal processing elements in the FPGA) as high order (orders greater than 30) FIR filters are used. Dynamic power is computed as the summation of power dissipation in clocks, logic, signals and DSP blocks. FIR filters are readily available as FPGA blocks. One approach to reduce the power dissipation is the usage of IIR filters. Lower order IIR filters produce shorter transition bands and greater stop band suppression than FIR filters of comparable order do. IIR filters (of much lower orders) use fewer multipliers and adders than FIR filters do for a

comparable transition bandwidth and stop band attenuation. The 80 dB stop band attenuation can be achieved by an IIR filter of 8^{th} order. In Figure 3.16, the two low-pass FIR filters are replaced with lower-order IIR filters with similar stopband attenuation of 120dB. The Hilbert Transformer is still implemented as a FIR filter as it requires linear phase. The IIR implementation of the Hartley suppressor was necessitated because of the higher power dissipation in FIR-based Hartley receivers.

In Table 3.3, power dissipation due to FIR implementation of a Hartley image suppressor and IIR implementation of a Hartley image suppressor is compared. For a given stop band attenuation (120 dB) of filter, the order of an IIR filter(8^{th}) is far lower than the corresponding FIR filter (30^{th}). The first design of the Hartley image suppressor used two 40^{th} order FIR filters while the final design used two 8^{th} order IIR filters. An 8^{th} order IIR filter with a transition band of $0.1\omega s$ can provide the necessary transition band stop-band attenuation of 120dB.

Table 3.3 Power dissipation for Hartley suppressor (Virtex6 FPGA)

Design (Type of Filter)	Clocks (mW)	Logic (mW)	Signals (mW)	DSP (mW)	Total (Dynamic) (mw)	Leakage (mW)	Total (mW)
FIR (30^{th} order)	51	58	81	225	445	335	821
IIR (8^{th} order)	23	10	9	13	55	335	380

Table 3.3 illustrates the advantages of implementing a Hartley image suppressor using IIR filters. Two different designs are compared one which has a Hartley compensator using FIR filters of 30^{th} order and the other utilizing IIR filters of 8^{th} order. The results of Figure 3.3 show that The Hartley suppressor featuring an 85% reduction in dynamic power due to usage of IIR filters instead of FIR filters. The results of Table 3.4 reveal that the combination of the Taylor-series DDS (with poor SFDR) and the Hartley image suppressor can achieve improved SFDR comparable to that of a cubic polynomial DDS. The combined power dissipation of a Hartley suppressor and a Taylor series DDS is comparable to a baseline cubic polynomial DDS with 8 segments and 16k

samples/cycle. A comparison of power budget of 8 segment Cubic polynomial DDS and Taylor series DDS combined with Hartley suppressor is summarized in Table 3.4.

Table 3.4 Comparison of SFDR and Power dissipation of Cubic DDS & Taylor DDS + Hartley Spur suppressor

	Cubic polynomial DDS ($s = 8$)	Taylor DDS + Hartley Spur Suppressor
SFDR	136dB	120dB
Dynamic power	114mW	97mW total (Taylor DDS (42mW), Hartley suppressor(55mW)

A simulation is performed to compare power dissipation of Taylor DDS combined with Hartley suppressor and compare its power dissipation with a cubic DDS with $S = 8$. The achieved SFDR values of a Cubic polynomial DDS and that of a combination of Taylor series DDS and Hartley image suppressor are comparable. But the combination of Taylor series DDS and Hartley image suppressor consumes lesser dynamic power. The next section describes the usage of Adaptive notch filters for spur suppression.

3.10 Adaptive Notch Filtering for Spur Suppression in DDS

Adaptive notch filtering in DDS involves filtering unwanted spurs that are generated by sinusoidal external disturbances. An adaptive filter which can not only locate the spur but quickly adjusts its own parameters as the spur location changes is ideal for applications such as CR, where the output of DDS can change rather swiftly. This section proposes an adaptive sinusoidal interference canceller (Figure 3.18) as a suitable mechanism to suppress a single dominant spur as in case of the Taylor series DDS. The proposed name for a system as in Figure (3.18) is Least Mean Squares-Sinusoidal Interference Canceller (LMS-SIC).

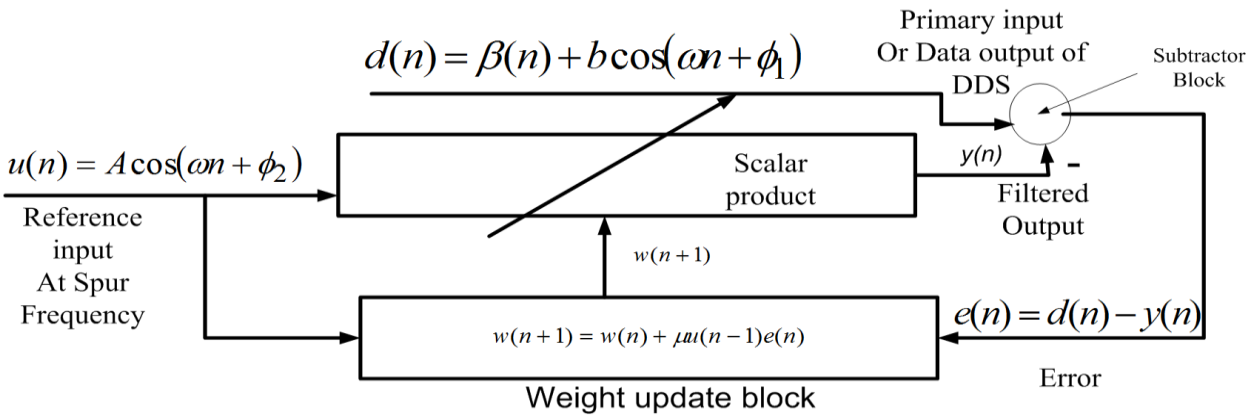


Figure 3.18 Block diagram of Adaptive Sinusoidal Interference Canceller (LMS-SIC)

Figure 3.18 illustrates an adaptive notch filtering scheme which comprises 2 major blocks – the weight update block and the output computation block (block marked scalar product block in Figure 3.18). The two inputs to the canceller are an M element vector of reference input of DDS, which is nothing but the previous M input samples of u and the input samples of $d(n)$ which is the reference signal plus spur. The amplitude of input sample $u(n)$ is A. An error signal $e(n)$is generated which is the difference between the desired output signal $d(n)$and the output $y(n)$of the filter. The weight update block updates its weight vector values $w(n)$ based on the error $(e(n))$and the previous value of the input vector $u(n)$. The output computation block computes $(w^T u)$, the scalar product of weight vector and input vector. The rate of convergence of the LMS algorithm (implemented in block diagram of Figure 3.18) is controlled by the factor μ ,a step-size control parameter. If the step size control parameter μ is too high, the results will be divergent. If μ is too small, the convergence will require greater number of iterations. For the block diagram of Figure 3.18, the explanation for various symbols is provided below.

$u(n)$ is the difference between the Reference input and magnitude of the spur. A is the amplitude of the reference input, $d(n)$ is the DDS output comprising of fundamental $\beta(n)$ + added spur($bcos(\omega n + \phi 1)$, $\beta(n)$ is the Information bearing signal same as the DDS output – fundamental without harmonics. b_I is the Amplitude of the sinusoidal interference (spur)and it need not be known a-priori. Angular frequency ω is the normalized angular frequency of the sinusoidal interference (known), ϕ_1 is the Phase of the sinusoidal interference (unknown). Finally, ϕ_2 is the Phase of the reference input (known).

The adaptive interference canceller is named as Least Mean Squares –Sinusoidal Interference Canceller (LMS-SIC). It uses the LMS algorithm of [Widrow, 1977] to perform cancellation of sinusoidal interference. Equation (3.110) presents the formulation of the primary input to the LMS-SIC.

$$d(n) = \beta(n) + b_I cos(\omega n + \phi_1) \tag{3.114}$$

In Equation (3.114), $\beta(n)$ is the information bearing signal. It is the DDS output – fundamental without harmonic spurs. The constant b_I is the amplitude of the sinusoidal interference (spur). In turn, ω is the normalized angular frequency of the sinusoidal interference (known); where ϕ_1 is the phase of the sinusoidal interference (unknown).

The working principle of the LMS-SIC is summarized as follows:

- Signal $d(n)$(Figure 3.18) is the primary filter input combining the fundamental output of DDS (first part in Equation 3.114) plus the sinusoidal interference tone (second part in Equation 3.114).
- The second part of the primary input in Equation (3.114) must be removed from the DDS output.

The reference input to the LMS-SIC comprises only of the sinusoidal interference given by Equation (3.115).

$$u(n) = Acos(\omega n + \phi_2) \tag{3.115}$$

In Equation (3.115), A is the amplitude of the sinusoid, ϕ_2 is the initial phase of the sinusoid, and ω is the angular frequency of the sinusoid. Output of the filter *y(n)* can be written as

$$y(n) = \sum_{i=0}^{M-1} w^T(i)u(n-i) \tag{3.116}$$

In Equation (3.116) $y(n)$ is a result of the convolution of the weight vector ($w(i)$) and the input vector($u(i)$). The error signal $e_{LMS}(n)$ (Equation 3.117) is defined as a difference of the reference input $d(n)$ and the filter output $y(n)$.

$$e_{LMS}(n) = d(n) - y(n) \tag{3.117}$$

In Equation (3.118), the weight update vector (in weight update block of Figure 3.35) is computed (in each step) as

$$w_{LMS}(n+1) = w_{LMS}(n) + \mu u(n-1)e_{LMS}(n)\ for\ n = 0,1,..N_{LMS} - 1 \tag{3.118}$$

In Equation (3.118), n is the Iteration number, N_{LMS} is the Maximum number of iterations, $w_{LMS}(n)$ is the weight vector at the n^{th} iteration, $u(n-1)$ is the input vector at the $(n-1)^{th}$ iteration, and μ is the convergence control factor of the weight update. Figure 3.19 explores the rapidity of convergence of (LMS-SIC).

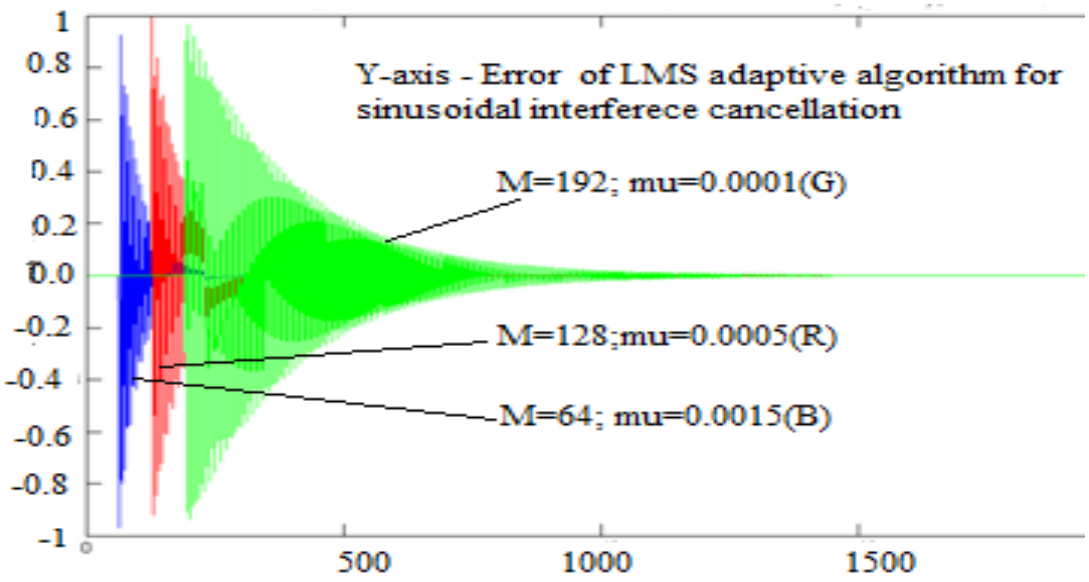


Figure 3.19 LMS error versus number of LMS iterations for LMS-SIC (the value mu refers to the constant μ in the LMS algorithm)

Figure 3.19 compares the LMS error of three filter orders in LMS algorithm $M = 64$(the 64th order), $M = 128$(the 128th order) and $M = 192$ (the 192th order). Figure 3.19 depicts the influence of number of iterations on the convergence of LMS. Figure 3.19 illustrates that the highest order adaptive filter ($M = 192$) which has the lowest value of μ, takes the largest number of iterations to converge (color green in Figure 3.19). The fastest convergence of LMS-SIC is observed when the value of μ is high (0.0015). The red track corresponds to $M = 128$ and μ=0.0005, blue track corresponds to $M = 64$ and μ=0.0015. Table 3.5 illustrates how an LMS algorithm based sinusoidal interference canceller could converge faster with greater μ and greater filter order (M).

Table 3.5 Number of iterations required to converge to less than 0.1% of final error for various order of LMS-SIC

Value of μ and filter size	Number of iterations	Value of μ and filter size (M=64)	Number of iterations
μ =0.0001; M=64	900	μ =0.0005;	322
μ=0.0015; M=64	447	μ =0.0010;	400
μ=0.0005; M=128	500	μ = 0.0015;	800

It can be concluded from Table 3.5 that increasing μ by a factor of 3 reduces the number of iterations by 40%. Too high a value of μ can also lead to instability of the LMS-SIC.

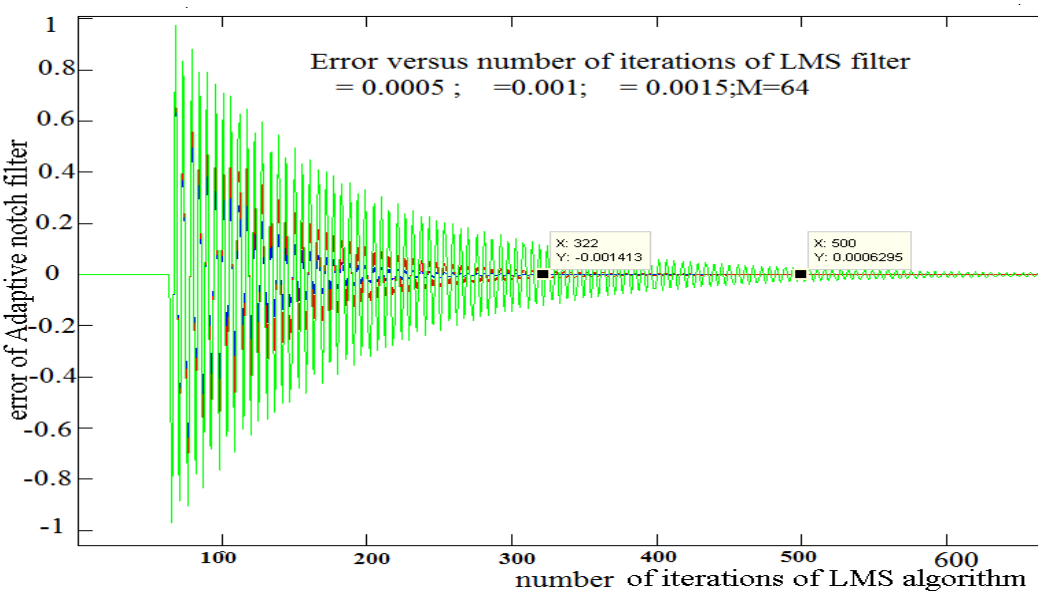
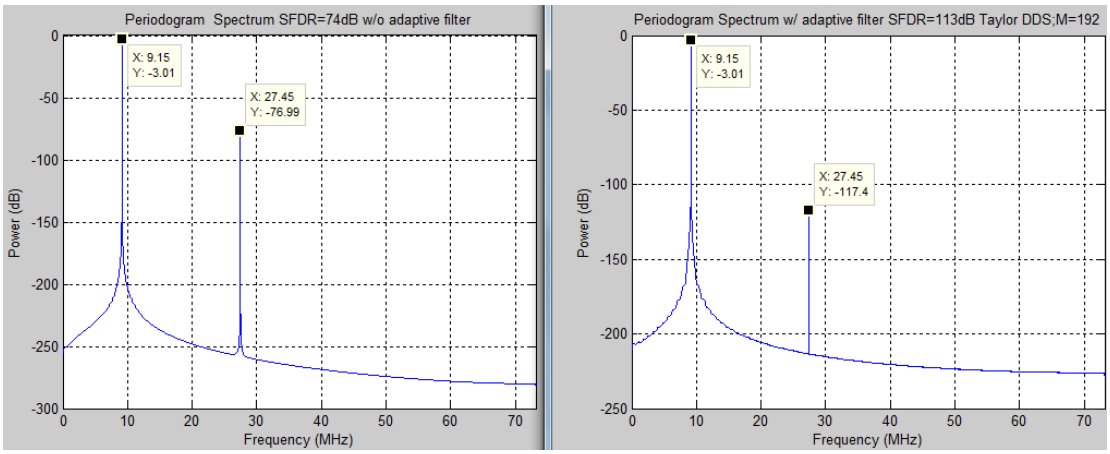


Figure 3.20 Error in adaptive filtering versus Number of iterations for $M = 64$; $\mu = 0.0005/0.001/0.0015$

Figure 3.20 illustrates that as μ(convergence control factor of LMS algorithm) is increased from 0.0005 to 0.0015, the number of iterations required to converge drops from 800 to around 320. The convergence of the LMS-SIC depends on the statistical characteristics of the added noise. It is independent of the output frequency of the DDS. The original SFDR of the Taylor Series DDS is 74dB (Figure 3.21a).



(a) Without Suppressor (b) With Suppressor

Figure 3.21 SFDR of Taylor Series DDS with and without Adaptive Spur Suppression($M = 192$; $\mu = 0.0005$)

Figure 3.21b SFDR of a Taylor's series DDS can be improved to up to 114 dB by using 192th order FIR filter (Figure 3.21b). The curves in Figure 3.21 illustrate an SFDR of 74 dB for the Taylor's series DDS alone and 114dB using a cascade of the Taylor series DDS and an LMS-SIC filter of 192th order. The structure of LMS-SIC can be analyzed in the frequency domain. The adaptive notch filter behaves as a second-order IIR filter with the transfer function given by [Widrow, 1975; Glover, 1977]. The transfer function is written as

$$H(z) = \frac{z^2 - 2zcos\omega_0 + 1}{z^2 - 2\left(1 - \frac{\mu M A^2}{2}\right)(zcos\omega_0) + \left(1 - \frac{\mu M A^2}{2}\right)} \tag{3.119}$$

In Equation (3.119) z is the z-domain variable, μ is the convergence factor, and A is the amplitude of input. In turn, ω_0 is the center frequency of the notch filter. M is the order of the LMS-SIC filter.

Figure 3.22 illustrates the difference in the attenuation of filter realized with two different order of filters with , $\mu = 0.2, A = 1$, M=32, and M=64 when both the notch filters are tuned to 27.45MHz, which is the third harmonic corresponding to a f_0=9.15MHz (where, f_0 is Output frequency of DDS).

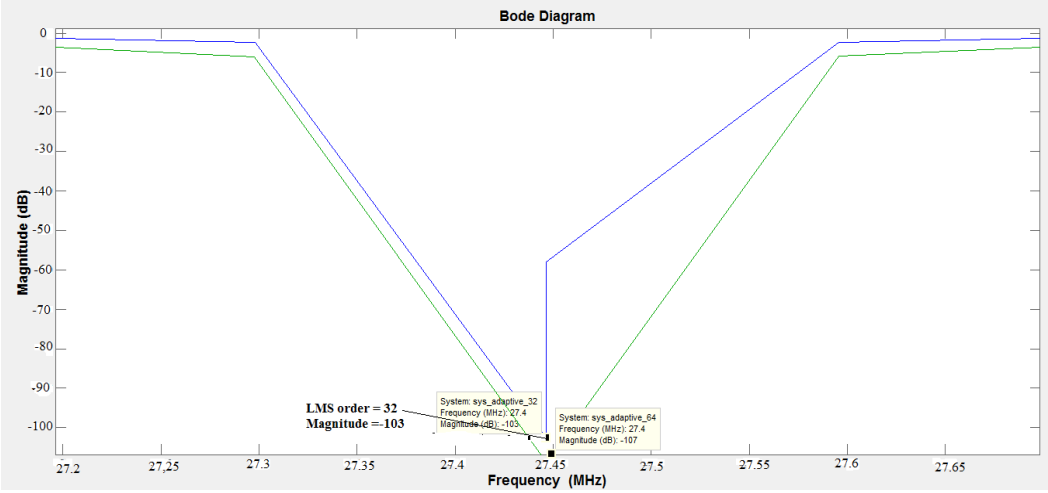


Figure 3.22Notch dilter transfer function($H(z)$) with 32 order($M = 32$) and 64th order(($M = 64$) filter maximum attenuation=-107dB)

In Figure 3.22, it is observed that an additional spur suppression of 4dB (-107dB vs -103dB) is achieved by using a 64th-order filter(green track) instead of a 32nd-order filter(blue track). Table 3.6 compares the efficacy of dither, Hartley and adaptive notch filtering techniques of spur suppression.

Table 3.6 Comparison of performance of dither, Hartley and adaptive notch filter

Suppression scheme	SFDR (dB)	Number of additional base-band waveform generators	HW resources	Dynamic Power (mW)	Noise Floor below fundamental
Dither addition		up to 2 dither sources (for triangular)	Dither generators	< 10mW	-120dB is not achievable

Hartley suppressor	120 (120dB elliptic)/ 80 (80dB elliptic)	One quadrature Source sinusoidal source (centered to $2f_0$)	2 IIR filters + one 64th order Hilbert Transformer + 2 multipliers + 1 adder	55mW Power on account of RF source = 45mW	200dB is achievable easily Figure 3.17
Adaptive Notch filter	93dB (M= 128); 97dB (M=192)	1 sinusoidal source of fixed amplitude (centered to $3f_0$)	Single 64th order FIR filter	20mW(filters) 45mW – NCO waveform generator	180dB achievable Figure 3.21 and Figure 3.23

Table 3.7 compares the performance and hardware resources for both the approaches of spur suppression after their mapping on a Xilinx Virtex-6 FPGA, and the dynamic power is compared. Leakage power of individual circuits cannot be estimated since the DDS circuit is a small component of the whole FPGA.

Table 3.7 SFDR and HW complexity comparison of Hartley suppressor and LMS-SIC

Suppression scheme	SFDR (dB)	Number of additional waveform sources	HW resources
Hartley suppression scheme	120dB/78dB (filter stopband 120dB/80dB)	One quadrature NCO ($2f_0$)	Two 8th order IIR filters+ one 64th order (FIR)+ 2 multipliers+ 1 adder
LMS-SIC	113db(M=192)	1 NCO ($3f_0$)	One FIR filter and one multiplier

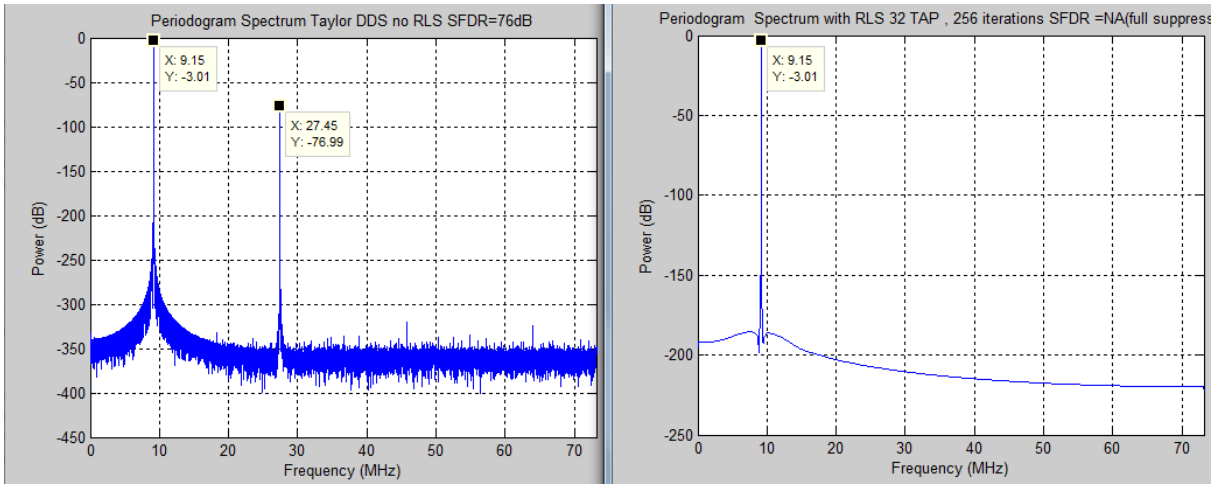
Table 3.8 compares the achieved noise floor and dynamic power (with the input clock frequency at 100 MHz and input voltage set to 2.5V).

Table 3.8 Dynamic Power and Noise Floor Comparison of Hartley Image Suppressor and LMS-SIC Using Virtex-6 FPGA

Suppression scheme	Dynamic Power (mW)	Noise Floor below Fundamental
Hartley suppressor	100mW	180dB (Figure 3.17)
Adaptive Notch filter	65mW	180dB (Figure 3.21)

In Table 3.8, it is observed that the LMS adaptive notch filter consumes 35mW less power than the Hartley suppressor for the same level of noise floor. The LMS-SIC and the Hartley type suppressor require an external Numerically Controlled Oscillator (NCO) source (quadrature for Hartley and non-quadrature for Adaptive) which consumes 45mW at a clock frequency of 100 MHz frequency. The proposed LMS-SIC requires a single higher-order filter in contrast to the three different filters and two additional multipliers required for Hartley Image suppressor.

An attempt was made to design an adaptive sinusoidal interference canceller which uses a different algorithm to achieve faster convergence. The algorithm chosen is the Recursive Least Squares (RLS) algorithm. An adaptive notch filter based on the RLS is referred to as the Recursive Least Squares – Sinusoidal Interference Canceller (RLS-SIC) algorithm. The RLS algorithm has been discussed by [Haykin, 2005]. The convergence of the RLS algorithm is faster than LMS in applications like Adaptive Line Enhancement (ALE). The speed of convergence depends on the ratio of the maximum and minimum eigenvalues of the input covariance matrix. RLS performs suppression of the third-harmonic spur.



(a) **(b)**

Figure 3.23 SFDR of Taylor series DDS without RLS-SIC (a) and with RLS-SIC(b)

SFDR = 74dB (without RLS) full suppression SFDR 190dB

Figures 3.23 (a) and 3.23(b) were generated by the RLS algorithm [Haykin, 2005], which was executed with the following initialization parameters.

Initial weight vector = Initialized to all zeros, weight vector($w(0)$) is initialized to all 0s

Weight vector length = 32 (a 32 TAP FIR filter).

It is observed that RLS completely suppresses the spur at the third harmonic that is at 27.45 MHz frequency. The RLS equations can be written in a summary as

$$\Phi_{yy}(n) = \delta I \tag{3.120}$$

In Equation (3.120), $\Phi_{yy}(n)$ is the Initial value of inverse covariance matrix, the constant δ is the Regularization parameter (set to 0.0004), λ is the Memory factor(constant) usually set to 1. Matrix I is the NxN unit matrix, and $W(0)$=zeros (N). N dimensional weight vector initialized to all 0s. For each iteration of the RLS algorithm, the following computation is performed. For each iteration, one must first calculate the intermediate vector as

$$\pi(n) = P(n-1)y(n) \tag{3.121}$$

In Equation (3.121), $P(n-1)$ is the Cross-covariance vector and $y(n)$ is the input vector.

In the second step, the Kalman gain (k_{RLS}) is computed as

$$k_{RLS}(n) = \frac{\pi(n)}{\lambda + y^T(n)\pi(n)} \tag{3.122}$$

In the third step, the step error is computed as

$$e_{RLS}(n) = d(n) - w^h(n-1)y(n) \tag{3.123}$$

In Equation (3.123) the Hermitian ($h\ superscript$) reduces to the transpose for real weight vector, as in this case. The weight update is a function of the error ($e_{RLS}(n)$) at each step, the original weight vector ($w_{RLS}(n-1)$), and the Kalman gain ($k(n)$), the weight update step can be written as

$$w_{RLS}(n) = w_{RLS}(n-1) + k(n)e(n) \tag{3.124}$$

In Equation (3.124), $w(n-1)$ is the weight vector in $(n-1)^{\text{th}}$ step and $w(n)$ is updated weight vector in n^{th} step. The inverse covariance matrix ($\Phi_{\text{yy}}(n-1)$)can be updated as

$$\Phi_{\text{yy}}(n) = \lambda^{-1}\Phi_{\text{yy}}(n-1) + \lambda^{-1}k_{RLS}(n)y^T(n)\Phi_{\text{yy}}(n-1) \tag{3.125}$$

The explanation for Equation (3.125) is that updated inverse covariance matrix must be computed at each step. The values of δ and λ are chosen which are typical of the RLS algorithm following [Haykin, 2005]. Table 3.9 compares the performance of RLS and LMS in terms of SFDR.

Table 3.9 Comparison of performance of LMS and RLS

Algorithm	Number of iterations and parameters	SFDR (dB)
LMS	$442(\mu = 0.0015; M = 64)$	100
RLS	$256(\lambda = 1; \delta = 0.0004)$	200

3.11 Conclusion

The initial approach was to achieve significant spur suppression by the addition of amplitude and phase dither to DDS. The initial approach in this chapter did not yield the expected results of spur suppression without compromising the noise floor. It was concluded that to achieve the required results suitable for cognitive radio, one must create alternate spur suppression techniques, which did not result in a poor SFDR. The three techniques–namely Hartley, an adaptive sinusoidal interference cancellation using LMS algorithm, and a sinusoidal interference cancellation using RLS algorithm - have been analyzed to assess the spur suppression feature without significantly raising the noise floor. The proposed technique involved addition of a Hartley noise suppressor after the DDS. It resulted in a SFDR improvement of 45dB (maximum). The second technique

utilized an LMS filter to improve the SFDR, and SFDR improvement of 30dB has been realized using a 128-tap LMS filter. With a 192-tap LMS filter, the improvement in SFDR has been of the order of 39 dB. The third technique utilized an RLS filter to improve the SFDR and achieved an SFDR improvement of 100 dB using a 32-tap RLS filter. All the three techniques have been proved to ensure a final SFDR above 100 dB even with a choice of initial DDS configuration with a low SFDR (74dB). One can use a Taylor series DDS with 74 dB with Hartley image suppressor to still realize SFDR of 120dB at the DAC input. The power budget of DDS + LMS filter (65 mW) is considerably less than a cubic polynomial DDS (136mW) while achieving a good SFDR of around 113dB. Hence, using an LMS filter to improve SFDR is a real alternative to using dither, and it does not raise the noise floor. If the power budget is not very critical and the additional silicon area is acceptable, the Hartley image suppressor is the best solution which can achieve an SFDR of 120 dB. If the power budget is more critical and about 10-12 cycles of delay are acceptable to achieve the SFDR, then the LMS-SIC and RLS-SIC are better solutions. The RLS –SIC requires 32 tap filters as opposed to 128 tap filters for LMS-SIC. However, the computation per sample of output is more for RLS. The 100mW power budget for a Hartley suppressor (in addition to the quadrature oscillator) can be reduced to 20mW using an RLS type suppressor. The RLS-SIC requires an additional 6 cycles of sinusoidal output to minimize the spur as compared to the Hartley suppressor.

An analysis has been performed with an additional term for phase dithered DDS with rectangular phase dither. Additional correction terms for the second- and third-order moments of error yield a different expression for SpSR. It has been illustrated that these corrections can be significant if the ROM bit-width is small – below 5 bits.

Chapter 4

Optimal Analytical Model of DAC &Second-Order PLL for Phase Noise, Lock time

A PLL is a closed-loop system having the ability to track the phase and frequency of an input waveform if the frequency of that input waveform is within a bounded range termed as a lock range. A PLL can multiply the frequency of input waveform by an integer or fractional multiple. Cascade of Digital to Analog converter- PLL (DAC- PLL) is an important subsystem in DDS-DAC-PLL that, in turn, is a critical sub set of Cognitive Radio. The performance metrics of DAC-PLL are phase margin, settling time, phase noise, damping coefficient, time constant of loop filter as well as sensitivities of Voltage Controlled Oscillator (VCO) and Phase detector.

4.1 Introduction

This chapter describes the relationships amongst the performance metrics of DAC-PLL. The definitions of the parameters of DAC-PLL along with their implications are discussed in the appropriate sections of this chapter. Multiple analytical relationships pertaining to DAC- PLL parameters are derived in this chapter. These relationships appear to have not been reported in the open literature. A closed-form expression relating the damping coefficient and the phase margin of a second-order PLL is derived. This chapter also analyses the utility of an analytical expression to relate the settling time of DAC- PLL to the time constant of the loop filter. An explicit expression relating the Phase Margin of PLL to its settling time has also been derived in this chapter. The derived closed-form expression forms the basis for the subsequent results required for phase noise performance of a second order PLL. An expression for the computation of the natural frequency of a DAC-PLL with its settling time and Phase Margin has also been derived to facilitate time response of DAC-PLL. The cumulative phase noise of DAC- PLL, which is expressed as a product of transfer function of reference noise sources and the summation of Noise Power Spectral Density for a plurality of noise sources of PLL, has also been analyzed.

This chapter comprises multiple sections. Thus, section 4.1 provides a description of the chapter objectives. Besides, a listing of the various sections of the chapter is also introduced. Section 4.2 introduces the functional block diagram and key sub-blocks of DAC-PLL. Section 4.3 presents

formulation and analysis of composite transfer function of the DAC-PLL. An analytical relationship between the phase margin and the damping coefficient of a second-order PLL is explored in section 4.4. Section 4.5 discusses an expression for the settling time of a DAC-PLL. Section 4.6 provides the analytical relationship between the settling time and Phase Margin of a DAC-PLL. Section 4.7 presents an introduction to phase noise and discusses the various noise sources in a PLL. Analytical expressions for the Noise Transfer Functions (NTFs) for noise sources inside a DAC-PLL are derived in Section 4.8. Section 4.9 relates lock time and Phase margin for a second-order PLL. Section 4.10 explores the linkage between the lock time and the phase noise of a second-order PLL. Section 4.11 explores the relationship between jitter and phase margin of a second order PLL. Section 4.12 derives a new expression for the angle between the two complex poles as a closed-form expression of the PLL phase margin. Section 4.13 presents an introduction to the phase shift due to the DAC. Section 4.13 includes analog approach to compensate the phase shift introduced by the DAC and PLL. Section 4.13 also presents a digital phase shift correction scheme and plots results of how it compensates for the phase shift introduced. Section 4.13 looks at the effect of the digital phase shift compensation in SFDR and Overshoot. Section 4.14 is the conclusion section.

4.2 Cascade of DAC-PLL

A functional block diagram of DDS-PLL with a second-order PLL is illustrated in Figure 4.1. The functional block comprises a cascade arrangement of a DDS, a Zero-Order Hold (ZOH) DAC, and a second-order PLL. The PLL segment of the functional block diagram is comprised of a first-order low-pass loop filter, a linear phase detector, a linear VCO, and a feedback loop frequency divider (divide by N). The focus of the chapter is on the sub-systems comprising of only the DAC and the PLL.

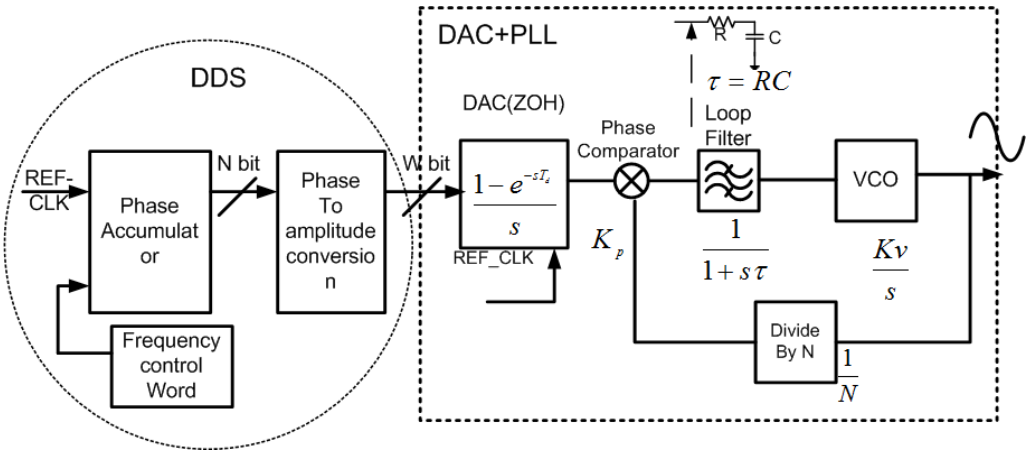


Figure 4.1 Block diagram of DDS-PLL showing DAC and a second-order PLL

The DDS portion (which is on the left-hand side circled section of Figure 4.1) further comprises a Phase accumulator block and a Phase-to-Amplitude Conversion (PAC) block, and its output (discrete sinusoid) is fed to the input of the Zero- Order Hold (ZOH) DAC. The dotted portion on the right-hand side of Figure 4.1 comprises only the DAC and the second-order PLL. The ZOH DAC converts the discrete time samples of the DAC input into continuous time signal at the output of the DAC. The PLL tracks the output of DAC and multiplies the frequency of the output of DAC by N, which is the divider ratio (N) in the PLL feedback path.

4.3 Transfer function of the DAC-PLL cascade

The cascaded DAC and PLL blocks (Figure 4.1) are characterized by their s-domain transfer functions. The cumulative transfer function is a product of the transfer functions of DAC and PLL. The transfer function of a ZOH DAC is given by [Dorf, 2008] and [Cleveland,1976] and is represented as

$$H_{ZOH} = \left(\frac{1 - e^{-sT}}{Ts}\right) \tag{4.1}$$

In Equation (4.1), H_{ZOH} is the transfer function of the DAC. The subscript ZOH denotes Zero-Order Hold. The variable s is the Laplace variable ($s = \sigma + j\omega$) and T is the sampling interval of the ZOH DAC. The loop filter in the forward path the PLL has a time constant τ given by RC,

as shown in Figure 4.1. The transfer function of the second-order PLL that has a first-order loop filter is given by

$$H_{PLL}(s) = \frac{G(s)}{1 + G(s)H(s)} = \frac{N}{s^2 \frac{\tau N}{K} + s\frac{N}{K} + 1} \tag{4.2}$$

In Equation (4.2), $G(s)$ is the transfer function of the forward path, $H_{PLL}(s)$ is the transfer function of the PLL, and $H(s)$ is the transfer function of the feedback path. Variable ($K = K_V K_\phi$) is the product of the VCO sensitivity and the Phase-Frequency Detector (PFD) sensitivity. Variable ($\tau = RC$) is the time constant of the loop filter and N is the feedback divide ratio. Variable K_V is the VCO sensitivity, in turn $K_\phi$is the PFD sensitivity. Converting Equation (4.2) to the standard format of transfer function for general second-order system, one obtains the transfer function of a second order Type I PLL in terms of its the natural frequency and damping coefficient as

$$H_{PLL}(s) = \frac{N\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.3}$$

In Equation (4.3), s is the Laplace variable, ω_n is the Natural Frequency of second-order PLL and ζ is the Damping Coefficient. In Equations (4.2 and 4.3), the denominator polynomial is of the second-order. The Equation (4.3) describes only the PLL as a generic second-order system. Together, Equations (4.2 and 4.3) allow the extraction of the natural frequency (ω_n)and damping coefficient (ζ) in terms of the time constant (τ) of loop filter and the product of sensitivities of VCO and PFD, *K*. The damping coefficient (ζ) and natural frequency (ω_n) are unambiguously defined for second-order systems [Dorf, 2008]. Henceforth, this cascaded block comprising of a DAC and PLL is referred to as DAC-PLL. The combined transfer function of the DAC-PLL systems is the product of the DAC transfer function and the PLL transfer function and it can be expressed as

$$H_{DACPLL}(s) = H_{ZOH}H_{PLL}(s) = \left(\frac{1 - e^{-sT}}{Ts}\right)\frac{N}{\left(s^2 \frac{\tau N}{K} + s\frac{N}{K} + 1\right)} \tag{4.4}$$

In Equation (4.4), $H_{DACPLL}(s)$ is the composite transfer function of the system comprised of the ZOH DAC and the second-order PLL.

4.4 Phase Margin and Damping Coefficient of second-order DAC-PLL

The section deals with the relationship between Phase Margin (PM), damping coefficient and PLL parameters. The PM is an important performance criterion for all systems. It is a measure of relative stability of a second-order system. PM is defined as the excess phase of the system when the forward gain is unity. In a second-order system, such as the PLL of the DAC- PLL with a feedback loop, the PM is the value of the phase shift for which the amplitude of the Bode plot shows a gain of 0 dB or unity gain. In a PLL, phase margin of a second order system can be controlled by controlling the damping coefficient, ζ [Dorf, 2008]. The damping coefficient determines how fast a second-order PLL can settle down after a unit step function has been applied at the input of the PLL. Underdamped systems $(\zeta < 1)$ have much faster rise times for step input, are oscillatory, exhibit lower PM. Overdamped systems $(\zeta > 1)$ have longer rise time to step input, are non-oscillatory featuring a higher PM compared to underdamped systems. Second-order PLLs have a damping coefficient which is sufficiently low to guarantee smaller rise time for step input as well as smaller lock times.

A derivation for PM as a function of ζ is presented in this section. The PM of a second-order system is a function of the damping coefficient for a second order system. The expression relating these two parameters (PM and Damping coefficient) originally given by [Dorf, 2008] is written as

$$PM = tan^{-1}\left(\frac{2\zeta}{\sqrt{\sqrt{4\zeta^4 + 1} - 2\zeta^2}}\right) \tag{4.5}$$

Equation (4.5) is a closed-form expression for the PM of the PLL in a DAC-PLL. Commercial PLLs are designed with PM of 45^o or greater [Curtin, 1999].

The natural frequency of a second-order system is expressed in terms of VCO sensitivity, PFD sensitivity and time constant:

$$\omega_n = \sqrt{\frac{K_V K_\phi}{\tau}} = \sqrt{\frac{K}{\tau}} \tag{4.6}$$

In Equation (4.6), ω_n is the natural frequency of the PLL. In Equation (4.6) K_V is the Sensitivity of the VCO, $K_\phi$is the Gain of Phase Frequency detector, and τ is the loop filter time constant. The damping coefficient of the PLL is written as

$$\zeta = \frac{\omega_n}{2K} = \frac{1}{2\sqrt{K\tau}} = \frac{1}{2\sqrt{K_V K_\phi \tau}} \tag{4.7}$$

In Equation (4.7), K_V is the Sensitivity of the VCO, and K_ϕ is the Gain of the PFD. $K = K_V K_\phi$ is the product of the sensitivity of the VCO and the sensitivity of the PFD. Figure 4.2 illustrates the variation of the time constant of loop filter with a change in sensitivity of the VCO for a range of damping coefficients (0.42 to 0.65). The results of Figure 4.2 allow the determination of a maximum time constant of loop filter for a given K.

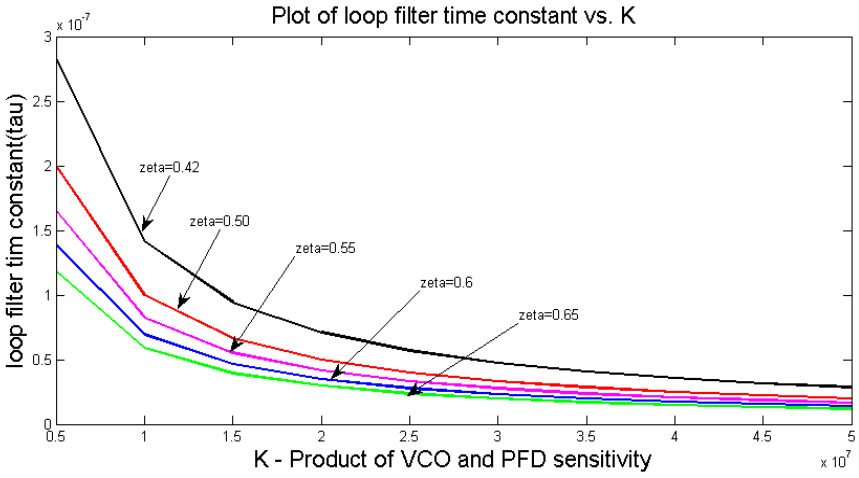


Figure 4.2 Time constant of Loop filter vs. sensitivity of VCO for a given ζ

From the results of Figure 4.2, it is seen that with a given (ζ), for a range of K from 0.5x10^7 to 5x10^7, the value of time-constant (τ) reduces to a low value. A smaller time constant might not be achievable as it requires too small a value of capacitance in an integrated circuit. In practice, the sensitivity of VCO (K_V) combined with the sensitivity (K_ϕ) of Phase Frequency Detector determines the value of K. In an implementation of DAC-PLL where the sensitivity of VCO (K_V) is low, results of Figure 4.2 requires a greater value of the capacitance (C) of loop filter, which might not be realizable in an integrated circuit which limits loop filter capacitance to few nFs.

In Equations (4.8 and 4.9) a new relationship between the damping coefficient and the phase margin is derived. A contribution of this section is an explicit expression to compute the damping coefficient as a function of the PM. Taking tangent of the PM (ϕ) in Equation (4.5), one can write an expression for PM as

$$\tan(\phi) = \left(\frac{2\zeta}{\sqrt{\sqrt{4\zeta^4 + 1} - 2\zeta^2}} \right) \tag{4.8}$$

After inverting and squaring both sides of Equation (4.8) and rearranging the terms a new expression for the damping coefficient in terms of PM, is obtained as

$$\zeta^4 = \frac{1}{\left(16\left(cot^2\phi + \frac{1}{2} \right)^2 - 4 \right)} \tag{4.9}$$

Equation (4.9) is not represented in open literature. The damping coefficient (ζ) is positive, so there is no ambiguity whether positive or negative root should be chosen. The slope of damping coefficient with respect to PM for a second-order system is written as

$$4\zeta^3 \frac{d\zeta}{d\phi} = \frac{d}{d\phi}\left\{ \frac{1}{\left(16\left(cot^2\phi + \frac{1}{2} \right)^2 - 4 \right)} \right\} = \frac{64cot\phi\left(cot^2\phi + \frac{1}{2} \right) cosec^2\phi}{\left(16\left(cot^2\phi + \frac{1}{2} \right)^2 - 4 \right)^2} \tag{4.10}$$

Equation (4.10) provides a closed-form expression for the derivative of the damping coefficient with respect to the phase margin. It is useful for designers who can use it in optimization procedures. The slope is written as

$$\frac{d\zeta}{d\phi} = \frac{1}{4\zeta^3} * \frac{64cot\phi\left(cot^2\phi + \frac{1}{2} \right) cosec^2\phi}{\left(16\left(cot^2\phi + \frac{1}{2} \right)^2 - 4 \right)^2} \tag{4.11}$$

Equation (4.11) can be used to optimize damping coefficient. Equation (4.11) provides the derivative of the damping coefficient with respect to the PM of a second-order PLL. Equation (4.11) is not found in the open literature.

4.5 Settling Time of a DAC-PLL

The settling time is the time taken by the composite DAC-PLL to settle to 5% of the final value of phase response with unit step input to the DAC [Dorf, 2008]. The faster the settling time is, the more rapid the response of the DAC-PLL is when it comes to settling down after the application of a phase step. A lower settling time for a PLL is desirable if stability is not compromised (low). In this section, it is assumed that the settling time of a cascade of DAC PLL is a sum of the delay of the DAC and the settling time of the PLL. By following [Dorf, 2008], the settling time of a cascade of DAC-PLL is written as a summation of the setting time of the PLL and the sampling interval of DAC:

$$T_{sDACPLL} = T_s + T_d \tag{4.12}$$

In Equation (4.12), $T_{sDACPLL}$is the settling time of DAC-PLL, T_s is the Settling Time of PLL with respect to a unit step input, and T_d is the sampling interval of the DAC. An expression for the settling time (T_s) for a second-order PLL derived by [Dorf, 2008] is represented as

$$T_s = \frac{4}{\zeta \omega_n} \tag{4.13}$$

Substituting the values of damping coefficient(ζ) and natural frequency (ω_n) and simplifying, them, one can write the settling time of the DAC+PLL cascade in the following way:

$$T_{sDACPLL} = 8\tau + T_d \tag{4.14}$$

In Equation (4.14), τ is a time constant of loop filter of PLL. Equation (4.14) is a new expression not found in the open literature. In case of a high sampling rate DAC, $T_d \ll \tau$, and, therefore, Equation (4.14) can be approximated as

$$T_{sDACPLL} \approx 8\tau = 8RC \tag{4.15}$$

4.6 Relationship between Settling time and Phase Margin

This section deals with a formulation to relate the setting time and the PM. From Equation (4.13), after substituting the time constant of loop filter as a function of settling time, the relationship between the damping coefficient and settling time can be rewritten after squaring:

$$\zeta^4 = \frac{4}{K^2 T_s^2} \tag{4.16}$$

Substituting the Equations (4.16) and (4.13) in Equation (4.8), one obtains a relationship between setting time and PM as

$$\tan(\phi) = \frac{2\zeta}{\sqrt{\sqrt{4\zeta^4 + 1} - 2\zeta^2}} = 2\left(\frac{2}{\sqrt{2KT_s}}\right)\left(\frac{1}{\sqrt{\sqrt{4\left(\frac{4}{K^2 T_s^2}\right) + 1} - \frac{4}{KTs}}}\right) \tag{4.17}$$

Equation (4.17) directly relates the PM with the settling time (T_s), sensitivity of VCO, K_V, and sensitivity of the phase detector, K_ϕ. Figure 4.3 illustrates the variation of the settling time versus K_V for various fixed values of the PM. The relationship between the PM and the settling time for a DAC PLL is not expressed in the open literature.

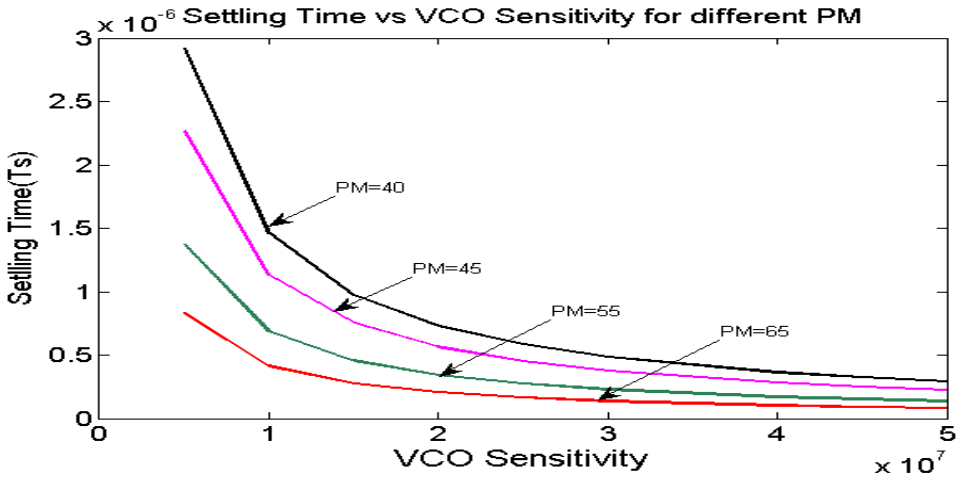


Figure 4.3 Settling Time vs. VCO Sensitivity for a range of Phase margins

For a given PM(ϕ), one can determine the settling time with K being a variable parameter. Figure 4.3 illustrates variation of T_s with K_V for a range of PM. In a practical PLL, there will be a variation in the fabricated capacitance. This leads to a secondary analysis of the effect of a variation of capacitance on the PM, ϕ of any designed and fabricated PLL. In practical analog CMOS processes [Chiu, 2014] at least a 10% variation will occur in the value of the loop filter capacitance.

In accordance with Equation (4.15), this leads to a variation of around 10% in the settling time ($\Delta Ts \approx 8R\Delta C$). This is because if RC is the filter time constant the capacitance is slightly perturbed, the perturbation of the time constant can be expressed as, $\Delta\tau = 8R\Delta C$.

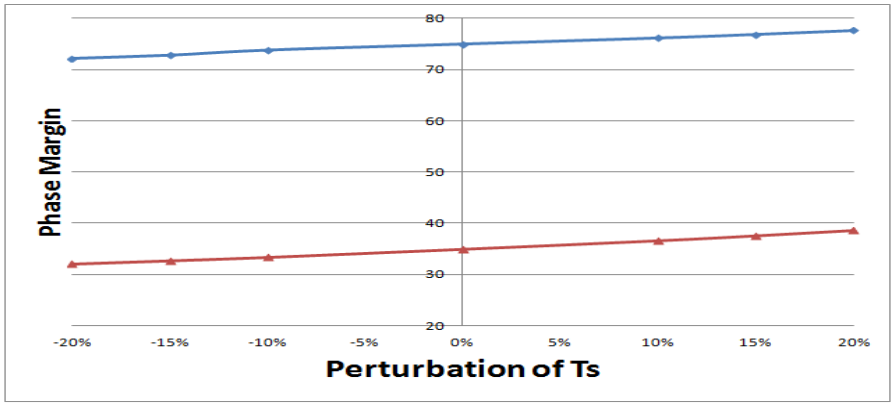


Figure 4.4 Variation of the PM with perturbation of Settling Time

Figure 4.4 shows the effect of perturbations of settling time on the PM of a DAC-PLL. A range of perturbations in settling time (from -20% to +20% in steps of 5%) is applied to the PLL. It is noticed that a 20% perturbation in the settling time (correspondingly capacitance of loop filter) leads to a 6.5^o variation in PM when PM=35^o. At a PM of 75^0, a 20% perturbation in settling time results 5.47^o variation in PM. This leads to the conclusion that the relative stability of DAC- PLL is most vulnerable to variations in settling time when the PLL is operating at a lower PM.

4.7 Phase Noise of the DAC-PLL

The two important reasons for the imposition of limits of phase noise on oscillators used in communication are due to its influence on BER performance and adjacent channel interference. Higher levels of phase noise degrade the BER performance of a digital communication system. It is observed that doubling of phase noise can degrade BER from $0.5x10^{-7}$ to 10^{-5} for BPSK modulated communication systems at SNR of 13dB [Tomba, 2008]. [He, 2007] has discussed the effect of phase noise on adjacent channels. Low phase noise oscillators (PLL or DDS) avoid the long tail from adjacent channels from very closely spaced channels by avoiding reciprocal mixing. Reciprocal mixing is defined as a condition under which the desired signal cannot be recovered

due to an interferer located close to a desired RF signal (in frequency domain). This is due to the mixing of the sideband of a PLL oscillator with the interferer. Reciprocal mixing poses a challenge when the adjacent channels in a communication system are closely space. Low phase noise PLLs can minimize reciprocal mixing. For low noise oscillators the frequency spectrum of output exhibits a very sharp drop-off from the center frequency.

The principal objective of this section is to improve the mathematical model for the phase noise of DAC-PLL considering multiple noise sources such as reference Noise, VCO noise, Loop Filter noise as well as Divider noise. Analytical derivations of the transfer functions of the noise sources and pertinent details of computation of Power Spectral Density (PSD) of various sources of noise have been covered by [Drucker, 2000] and [Amornthipparat, 2008]. [Drucker, 2000] has discussed models of multiple noise sources without providing a methodology to compute a composite PSD (Phase Noise) at the output of a PLL. Since [Drucker, 2000] addresses the analysis of the noise sources at secondary input points of the PLL and since the secondary input points of each of the noise sources vary, an expression for composite phase noise of PLL was not feasible. Consequently, all its expressions of phase noise of individual sources cannot be aggregated to arrive at a composite phase noise of the PLL. Further [Drucker, 2000] and [He,2007] did not relate the influence of performance metrics of DAC-PLL such as PM, settling time and damping coefficient, with the phase noise of the DAC- PLL.

[He, 2007] has provided an analysis of PM of third- and fourth-order PLL and the variance of lock time with the PM. [Savic, 2007] considers the variation of PM with bandwidth of loop filter in a third-order PLL but analytical expressions for NTFs of noise sources are not derived. [Daniels, 2008] deals with stability issues of higher order PLLs but the relationship between phase noise and the referred performance metrics of PLL are not explored. An analysis to derive an expression for cumulative phase noise of DAC-PLL has been considered in this thesis. In addition, several new variants of the relation between the phase noise and the referred performance metrics have been derived to compute the individual phase noise of the sources of noise and the cumulative phase noise of DAC- PLL as well. Such explicit relational expressions of DAC- PLL appear to have not been addressed in the open literature. As discussed in chapter 2, higher levels of phase noise at DAC-PLL output makes it difficult to detect desired signals of low amplitude. Therefore, lowering the level of phase noise is a goal in DDS-PLL design. There are, in general, two types of phase noise models – single-side band Noise or $\mathcal{L}(f_m)$and double side band noise of $S(f_m)$. Of these the

two noise models, this chapter adopts the double side band noise model of [Drucker, 2000]. [Drucker, 2000] subdivides the phase noise spectrum into regions with dominant physics (Figure B.1 in Appendix B of this thesis). The DAC-PLL designer is more interested in the regions of offset frequencies, which are influenced by flicker FM, white FM and flicker phase, as the frequency offset is more comparable to channel spacing in RF communication. Phase noise is treated as a distribution function, and hence, is more amenable to be expressed via PSD (dBc/Hz) of noise sources.

Modeling and Analysis of the various noise sources in a PLL

The representation of phase noise of a PLL has taken two known approaches in the existing literature. For the sake of clarity and unambiguity of the discussions to follow on phase noise, it is preferable to identify these two approaches and distinguish between the two different phase noise representations in terms of their dimensional properties and units. Table 4.1 depicts a comparison of the two approaches- Single Side Band Phase Noise **(**SSBPN) and Double Side Band Phase Noise **(**DSBPN) to measure level of phase noise in an oscillator.

Table 4.1 Single Side Band Phase Noise (SSBPN)/Double Side band Phase Noise (DSBPN)

SSBPN/DSBPN	**Expression**	**Explanation of Noise expression**
Single Side Band Phase Noise (SSBPN) (unit dBc/Hz.)	$\mathcal{L}(f_m) = \frac{P(f_c+f_{cm},1Hz)}{P_{carrier}}$ (4.18)	It is a ratio of the power contained within a BW of 1 Hz at an offset of f_{cm} ($P(f_c + f_{cm}, 1Hz)$ divided by the carrier power ($P_{carrier}$) at the center frequency[Cerda, 2006]
Double Side Band Phase Noise (DSBPN) (unit rad^2/Hz)	$S_\phi(f_m) = 2\mathcal{L}(f_m)$ (4.19)	Demodulation of the output waveform of a noise source using an ideal demodulator and filter is performed. Demodulator output is in baseband with a filter which has a resolution 1 Hz [Drucker, 2000].

The SSBPN approach uses an ideal spectrum analyzer with a 1 Hz resolution- the bandwidth to measure the normalized noise power within a 1 Hz BW at an offset frequency of f_m. The definition of SSBPN can be written as follows [Cerda, 2006] (Equation 4.18). In Equation (4.18), f_m is the offset frequency from the center frequency of the PLL. The variable f_c is the Centre frequency of the PLL. $P(f_c + f_m, 1Hz)$ is the Power in a 1Hz bandwidth at a frequency of $f_c + f_{cm}$ and $P_{carrier}$ is the level of Carrier Power. The unit of Phase Noise $\mathcal{L}(f_m)$is dBc/Hz (the symbol is referred to a $\mathcal{L}$ (script L)).

The second (Double-Side Band Phase Noise (DSBPN)) representation of the phase noise involves the demodulation of the output waveform of a noise source using an ideal demodulator and filter. Its output is now in the baseband with a filter, which has a 1 Hz resolution [Drucker 2000]. The DSBPN representation is followed in the analysis to follow.

There are multiple sources of noise within the PLL, namely the VCO, the low-pass filter, the PFD, and the feedback divider. The additive noise model for the PSD of a noise source is given in terms of the offset frequency (or its inverse) and a set of coefficients. The additive phase noise model followed by [Drucker, 2000] is empirical. The coefficients $k_{i,j}$ in the model (Equations 4.18-4.21) are based on the measurements performed by the PLL manufacturer. Typical values of these coefficients have been given by [Drucker, 2000]. Table 4.2 depicts the representation of the four sources of noise considered for the analysis with f being the offset frequency.

Table 4.2 Noise models of various sources in PLL

Source of Noise	Expression for Power Spectral Density (rad^2/Hz)
VCO	$S_{VCO}(f) = (k_{0,V} + \frac{k_{2,V}}{f^2} + \frac{k_{3,V}}{f^3})$ (4.20)
Reference	$S_{REF}(f) = (k_{0,REF} + \frac{k_{1,REF}}{f} + \frac{k_{2,REF}}{f^2} + \frac{k_{3,REF}}{f^3})$ (4.21)
Divider	$S_{DIVIDER}(f) = \left(k_{0,MD} + \frac{k_{1,MD}}{f}\right)$ (4.22)
Filter	$S_{FILT}(f) = (k_{0,FILT} + \frac{k_{1,FILT}}{f})$ (4.23)

In Table 4.2, the symbols $S_{VCO}(f), S_{DIVIDER}(f), S_{REF}(f), S_{FILT}(f)$ are the sources of phase noise generated by the VCO, divider, reference, and filter, respectively. For the notation of $k_{i,j}$ parameters, the first index (i) denotes the inverse power of the offset frequency (f) and the second index(j)

refers to the type of noise source. The coefficients $k_{i,j}$ are curve-fitted coefficients and S is the PSD of a noise source. Table 4.3 shows typical values of the $k_{i,j}$ parameters corresponding to the phase noise models in Table 4.2 for a PLL described by [Drucker, 2000].

Table 4.3 Values of the $k_{i,j}$ coefficients for the four noise sources in DAC-PLL

Noise source	K parameters
VCO	$k_{0,VCO}$ =$10^{-15.5}$; $k_{2,VCO}$ =10^{-3}; $k_{3,VCO}$ =$10^{0.7}$
Reference	$k_{0,ref}$ =$10^{-15.8}$; $k_{1,ref}$ = $10^{-12.7}$; $k_{2,ref}$ =$10^{-9.86}$; $k_{3,ref}$ =$10^{-7.82}$
Divider	$k_{0,divider}$ = $10^{-15.5}$; $k_{1,divider}$ = $10^{-12.5}$
Filter	$k_{0,filter}$ = $10^{-15.38}$; $k_{1,filter}$ = $10^{-16.02}$;

The Equations (4.18 to 4.21) along with the pertinent $k_{i,j}$ parameters of Table 4.3 are used to generate the results pertaining to the variation of the phase noise or PSD as a function of the offset frequency. Figure 4.6 illustrate the variation of PSD of various sources of noise in a PLL following [Drucker, 2000].

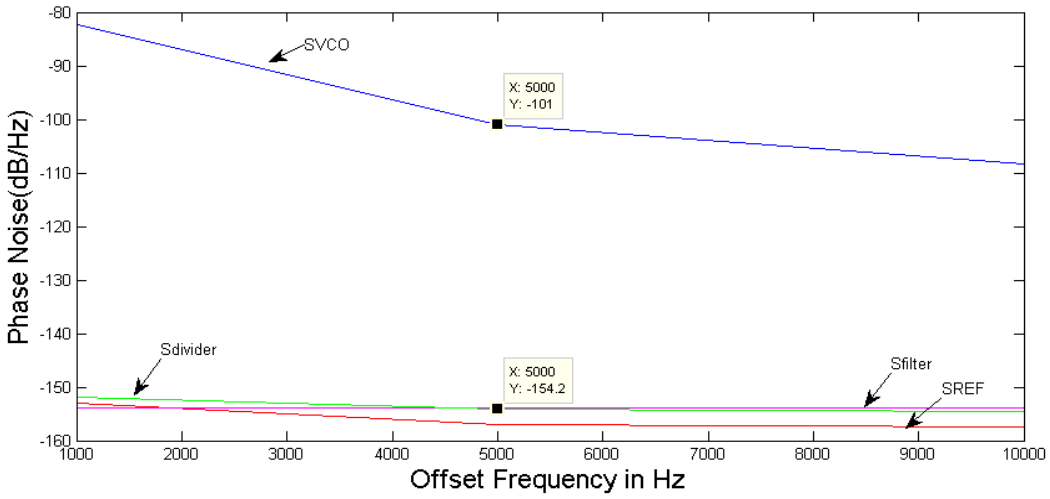


Figure 4.5 Phase Noise of noise sources in PLL versus frequency offset

The X axis in Figure 4.5 is the offset frequency from the center frequency and the Y axis is the phase noise computed with the coefficient values from Table 4.3. The phase noise of the VCO is

much higher (-101dB/Hz) than the phase noise of both the reference and the divider (-154dB/Hz) at an offset frequency of 5 kHz. Figure 4.5 reflects the phase noise at the output of the PLL for all four sources of noise when considered separately. NTF relates the PSD of a specific noise source to the noise observed at the output of the PLL. If a source has low phase noise, its phase noise contribution will be significant at an output of the PLL if the absolute magnitude of its NTF is high. Expressions for NTF are derived in Section 4.8.

4.8 Transfer Functions of the Noise Sources of DAC- PLL

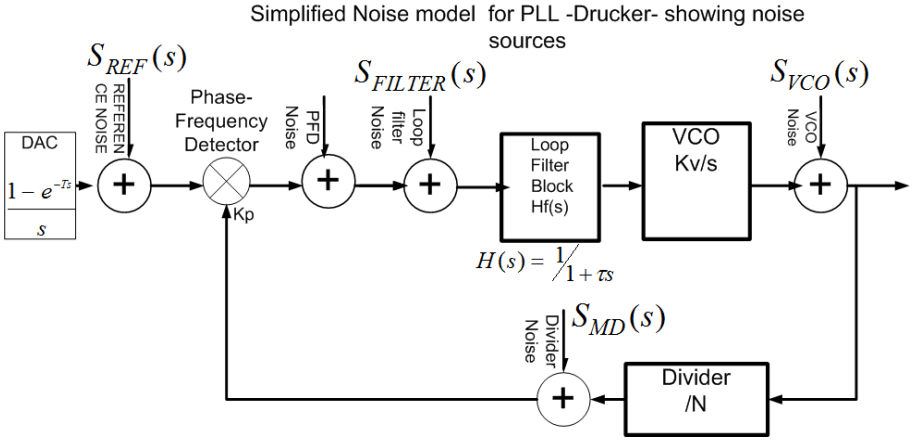


Figure 4.6 Phase noise model with Phase Noise Sources within the DAC-PLL

Figure 4.6 illustrates the multiple noise sources inside a PLL as captured in a frequency domain noise model. A simple phase noise model comprising of several noise sources is appropriate for second- and higher- order PLLs as in [Drucker 2000] with the additional DAC. Each noise source is modeled using an additive model with multiple terms, each term having a fixed coefficient multiplied by an inverse power of the frequency offset from a central frequency. The additive noise model of [Drucker, 2000] and [Amornthippart, 2008] captures the cumulative PSD (phase noise) at the output of the PLL as a summation of the contributions of individual noise sources weighted with quadratic weights. Each weight being the magnitude of the respective transfer function from a specific noise source to the output of the PLL. None of the above cited research has dealt the explicit expression for NTF of various sources of noise in DAC- PLL. [Herzel, 2010] has analyzed

and derived the Equations for NTFs of VCO, reference source, Loop filter and divider. [Herzel, 2010] places the divider noise source between the VCO output and the divider block.

The phase noise model in Figure 4.6 incorporates five noise sources. VCO noise source is placed after the VCO in the PLL model. Divider noise source is placed after the divider. A reference noise source representing the noise contribution of the reference source driving the PLL. The reference noise source can also account for the DAC noise. Two additional noise sources are incorporated - one for the PFD and one for the loop filter.

4.8.1 NTF of a Noise Source (Oscillator)

A schematic for the computation of NTF of noise source in a DAC- PLL is depicted in Figure 4.7. $\boldsymbol{S_{REF}(s)}$ in Figure 4.7 represents the PSD or phase noise of the reference source (a source outside the PLL itself) with $\boldsymbol{s}$ denoting the Laplacian variable.

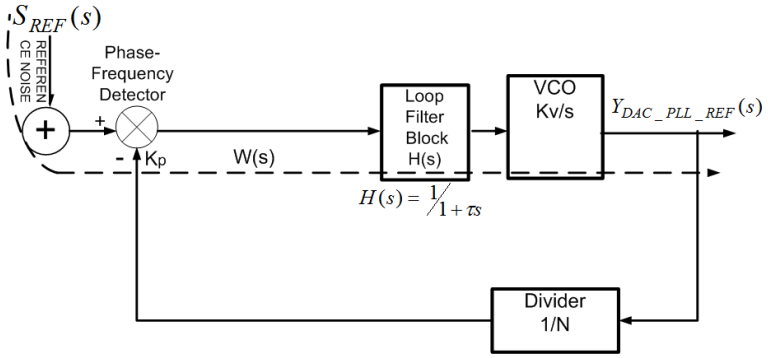


Figure 4.7 Model for calculating NTF of Reference Source in DAC- PLL

The NTF of reference source is the same as the standard closed-loop transfer function of the PLL. Substituting the transfer functions of forward and feedback paths one obtains the NTF of the reference source , $W(s)$ and it is written as

$$W(s) = \frac{G(s)}{1 + G(s)H(s)} = \frac{K_\phi \frac{K_v}{s} \frac{1}{(1+\tau s)}}{1 + K_\phi \frac{K_v}{Ns} \frac{1}{(1+\tau s)}} = \frac{K}{\tau(s^2 + 2\zeta\omega_n s + \omega_n^2)} \quad (4.24)$$

Equation (4.24) represents the NTF of the reference source which is the same as the transfer function of the PLL. In Equation (4.24), ω_n is the natural frequency (defined in Equation 4.6) and

ζ is the damping coefficient (defined in Equation 4.7).

4.8.2 NTF of VCO

A model for the determination of NTF of VCO in DAC-PLL is illustrated in Figure 4.8.

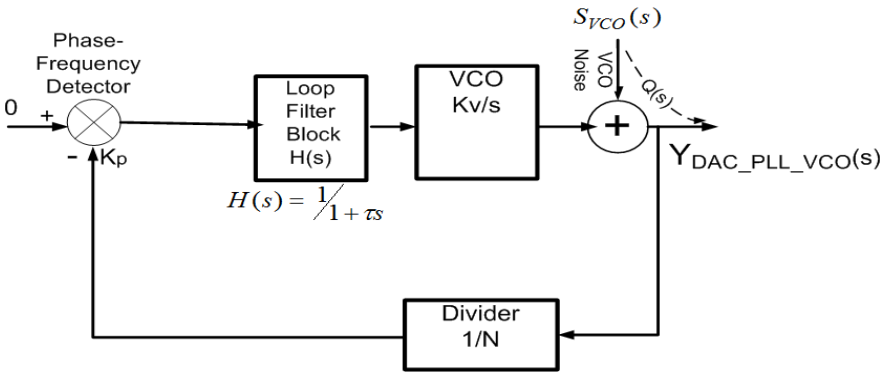


Figure 4.8 Noise Model for the computation of NTF of VCO in DAC-PLL

The PSD of VCO is denoted by $S_{VCO}(s)$ in Figure 4.8. One assumes this PSD, ($S_{VCO}(s)$) as an input to the system and computes the response at the DAC-PLL output ($Y_{DAC\_PLL\_VCO}(s)$). A closed-form expression for the NTF of VCO noise source is obtained as

$$Q(s) = \frac{Y_{DAC_{PLL_{VCO}}}(s)}{S_{VCO}(s)} = \frac{s(1+s\tau)}{\tau(s^2 + s\frac{1}{\tau} + \frac{K}{N\tau})} = \frac{W(s)s(1+\tau s)}{K} \quad (4.25)$$

Equation (4.25) relates the NTF ($Q(s)$) of VCO with NTF ($W(s)$) of the reference source.

4.8.3 NTF of Loop Filter

An analytical model for NTF of Loop Filter in DAC-PLL is shown in Figure 4.9. Figure 4.9 represents the PLL with only the Loop filter noise source present with the primary input grounded. It can be used to compute the NTF of loop filter noise source in DAC- PLL.

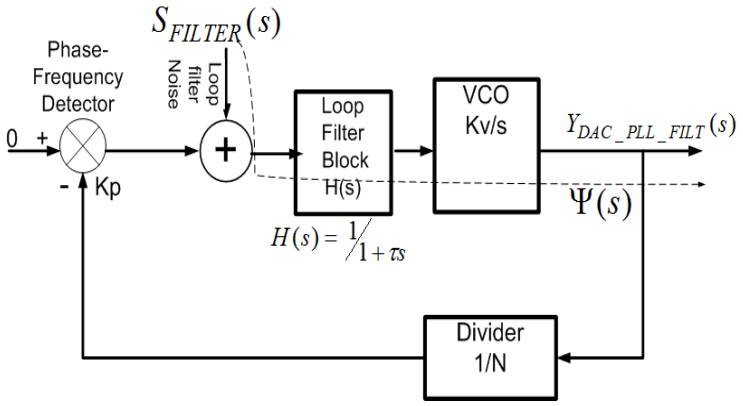


Figure 4.9 Model for NTF of Loop Filter in DAC-PLL

In Figure 4.9, the assumed PSD of Loop Filter is marked as $S_{FILTER}(s)$. One assumes this as the primary input phase noise to the system and computes the response at the output of the DAC-PLL ($Y_{DAC\_PLL\_FILT}(s)$). The NTF of Loop Filter ($\Psi(s)$), is derived as

$$\Psi(s) = \frac{Y_{DAC\_PLL\_FILT}(s)}{S_{FILTER}(s)} = \frac{K}{K_\phi \tau} \frac{1}{(s^2 + \frac{1}{\tau}s + \frac{K}{n\tau})} = \frac{W(s)}{K_\phi} \tag{4.26}$$

Equation (4.26) expresses the NTF of the Loop filter in terms of the NTF of the reference source. The detailed derivation is in Appendix B.

4.8.4 NTF of the Divider

The NTF of noise source of the divider in a DAC-PLL can be determined through the model illustrated in Figure 4.10. In Figure 4.10, the PLL is represented with only the divider noise source present and the primary input grounded.

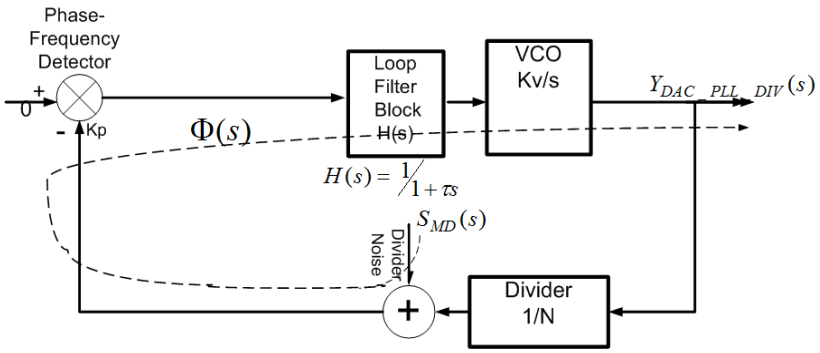


Figure 4.10 Model for NTF due to Divider Noise Source in DAC- PLL

In the noise source of the divider (Figure 4.10), the assumed PSD is marked as $S_{MD}(s)$. One assumes this to be the primary input to the system and computes the response at the DAC-PLL output ($Y_{DAC\_PLL\_DIV}(s)$). By further simplification, the NTF for the noise source of divider, ($\Phi(s)$) can be written as

$$\Phi(s) = \frac{Y_{DAC\_PLL\_DIV}(s)}{S_{MD}(s)} = -\frac{K}{\tau}\frac{1}{\left(s^2 + \frac{1}{\tau}s + \frac{K}{n\tau}\right)} = -W(s) \tag{4.27}$$

The square of the magnitude of NTF of the divider ($\Phi^2(s)$)is the same as that of an NTF of the reference source ($W^2(s)$). Equation (4.27) allows the simplification of the cumulative PSD at the DAC-PLL output in Equation (4.41). The detailed derivation is in Appendix B.

4.8.5 The Weiner-Khintchine Theorem

The Weiner-Khintchine theorem [Herzel and Piz, 2005] determines the PSD at the output in terms of the PSD at the input of a given system as defined in Equation (4.28).

$$S_{zz}(j\omega) = |\Gamma(j\omega|^2 S_{xx}(j\omega) \tag{4.28}$$

In Equation (4.28), the multiplier $|\Gamma(j\omega|^2$ is the square of the magnitude of the transfer function of a noise source. $S_{xx}(j\omega)$ is the PSD of Phase noise at system input and $S_{zz}(j\omega)$ is the PSD of phase noise at system output. The multiplier can be written as

$$\Gamma(j\omega) = \frac{G(j\omega)}{1 + G(j\omega)H(j\omega)} \tag{4.29}$$

In Equation (4.29), $\Gamma(j\omega)$ is the Noise transfer function. $G(j\omega)$ is the transfer function of the forward path. $H(j\omega)$ is the transfer Function of the feedback path. The Weiner-Khintchine theorem is relevant for the DAC- PLL since it provides the relationship between the PSD at the output of DAC- PLL and the PSD of a given noise source assumed as the input.

In the subsections 4.8.1 to 4.8.4, the NTFs of the four types of noise sources of a DAC- PLL have been discussed. The NTF of reference source, $W(s)$ is expressed through Equation (4.24). Equation (4.25) determines the $Q(s)$, the NTF of VCO. $\Psi(s)$, the NTF of Loop filter is derived in Equation (4.26). The NTF of the divider, $\Phi(s)$ is expressed by Equation (4.27).

In accordance with Wiener-Khintchine theorem (Equation 4.28), the composite PSD of the DAC-PLL is given by the sum of the PSDs of individual noise sources. While deriving the PSD of an individual noise source, rest of all other noise sources must be set to zero. This is in accordance with the application of the principle of superposition.

The combined phase noise is the sum of the contributions from all four sources is written as

$$S_{CUMU}^{OUT}(s) = S_{REF}(s)|W(s)|^2 + S_{VCO}(s)|Q(s)|^2 + S_{FILTER}(s)|\Psi(s)|^2 + S_{MD}(s)|\Phi(s)|^2 \qquad (4.30)$$

In Equation (4.30), S_{OUT}^{CMU} is the cumulative PSD at DAC-PLL output, $S_{REF}^{OUT}(s)$ is the PSD at output of PLL due to the reference source alone. Transfer function *W(s)* is the NTF of the reference noise source, $S_{MD}^{OUT}(s)$ is the PSD at PLL output due to the divider alone, $\Phi(s)$ is the NTF of the Divider noise source, $S_{VCO}^{OUT}(s)$is the PSD at PLL output due to the VCO alone, *Q(s)*is the NTF of the VCO, $S_{FILTER}^{OUT}(s)$is the PSD at PLL output due to the loop filter alone, and $\Psi(s)$ is the NTF of the loop filter.

In a phase noise analysis of DAC-PLL, it must be assumed that the noise sources are uncorrelated to derive Equation (4.30). The RHS in Equation (4.30) is the summation of the output PSDs from Equations (4.24 to 4.27). The units of both sides of Equations (4.30) are rad^2/Hz or $dBrad^2/Hz$. PSD of each noise source is weighted by the square of the respective NTF for that specific noise source. Substituting the value of NTF of each noise source in terms of NTF $W(s)$ of reference source, the expression for composite PSD in Equation (4.30) gets further simplified. This step paves the way for subsequent application of optimization schemes for phase noise. The composite phase noise expression in Equation (4.30) can be written with the NTFs being expressed in terms of the $W(s)$, which is the NTF for the reference source as well as the transfer function of PLL.

The values of NTFs $Q(s)$,*Ψ(s), Φ(s)* are substituted in Equation (4.30) utilizing Equations (4.26-4.27) to yield Equation (4.31) in terms of $W(s)$ as

$$S_{CUMU}^{OUT}(s) = W^2(s)(S_{REF} + S_{MD} + S_{FILTER}\left(\frac{1}{Kp}\right)^2 + S_{VCO}\left(\frac{s(1+\tau s)}{K}\right)^2) \quad (4.31)$$

Equation (4.31) allows further simplification by substitution of the values of K_ϕ and K these simplifications can be performed to optimize phase noise. The zero in the numerator of the fourth term of Equation (4.31) occurs at tens of GHz which is far greater than the frequency of interest. The factor K in the denominator of VCO noise term (Equation 4.31) has significant impact on phase noise as it reduces the $Q(s)$ (magnitude of Transfer function of VCO) significantly. Commercial PLLs have typical K_V values ranging between 10 MHz/volt to 200 MHz/volt, [Banerjee, 2006]. The expression for phase noise (in Equation 4.31) contains the factor of $1/K_\phi^2$ for the term corresponding to the loop filter and hence the contribution of the loop filter to the phase noise at the output of PLL can be mitigated by using a higher sensitivity of PFD. Equation (4.31) predicts that the phase noise of VCO propagated to the output of PLL can be regulated by the control of K. Different versions of Equation (4.31) must be developed for the design of various classes of PLL. Equation (4.31) is useful for problems addressing optimization of phase noise.

4.8.6 Comparison of Derived NTF with the NTF expression of [Herzel, 2010]

The NTFs of VCO, reference, Loop filter and divider have been analyzed in [Herzel, 2010]. The analysis and derivation of NTFs of various noise sources in a DAC- PLL were carried out with a defined goal of conforming the expressions of NTF to be amenable for optimization of phase noise. Further, from analysis perspective to gain additional insight into the overall noise performance of a DAC- PLL, it is preferable and desirable to have these expressions in a form that may involve normalization. An attempt has been made and it has been proved to be successful in normalizing the NTFs of the sources of noise considered in this section with respect to the NTF of reference noise source. In the sections to follow, the NTF expressions derived in normalized form are utilized which leads to a compact closed-form expression for phase noise. An exercise of expressing the NTFs of noise sources of a DAC- PLL normalized with respect to NTF of any of the noise sources appears to have not been attempted earlier. [Herzel, 2010] has also derived the NTFs for a

fractional N PLL. [Herzel,2010] places the divider noise source after the feedback element leading to different NTFs in contrast in this chapter the divider noise source is placed before the feedback element.

4.8.7 Relationship between Phase Noise, Phase Margin & Damping Coefficient

In this section the relationship between PM, settling time and phase noise using a two-part procedure. In the first part K_ϕ, the sensitivity of phase detector is substituted in the cumulative phase noise as a function of the following independent variables - divider ratio (N), damping coefficient ζ, time constant (τ) of the loop filter, and the sensitivity (K_V) of the VCO. For this one must start with the definition of the damping coefficient including the additional factor of divider ratio (N). The damping coefficient is defined in terms of$K$, time constant (τ) of loop filter and divide ratio (N) as in Equation (4.32). Taking fourth powers of Equation (4.16), one obtains:

$$\frac{1}{K^2} = \frac{4\zeta^4\tau^2}{N^2} \tag{4.32}$$

Substituting the values of K and K_ϕ into the expression of NTF (Equation 4.31), one obtains an expression for the total phase noise as

$$T1 + T2 = S_{CUMU}^{OUT}(s) = W^2(s)(S_{REF} + S_{MD}) + W^2(s)(S_{FILTER}\left(\frac{1}{K_\emptyset}\right)^2 + S_{VCO}\left(\frac{s(1+\tau s)}{K}\right)^2) \tag{4.33}$$

In Equation (4.33), $T1$ is the Phase noise of Reference noise source and divider noise source and $T2$ is the Phase noise of VCO noise source and loop filter noise source in Figure 4.6. $T1$ is the sum of the PSDs of the reference source and divider times the square of the magnitude of TF $W(s)$ at a specific offset frequency. Simplification is possible for the term $T2$ of Equation (4.34), which involves the sources of noise in VCO and loop filter.

$$T2 = (W(s))^2\left\{S_{VCO}\frac{4\zeta^4\tau^2}{N^2}\left(s(1+\tau s)\right)^2 + S_{FILTER}\left(\frac{4\zeta^4\tau^2K_v^2}{N^2}\right)\right\} \tag{4.34}$$

Since the PSD of VCO is most predominant, the optimization approach must address the phase noise contribution at the output due to the VCO and loop filter (term $T2$). The expression for $T2$ in Equation (4.34) is further simplified by the substitution of value of the time constant (τ) of loop filter and the damping coefficient ζ in terms of phase margin. The final expression for phase noise including the effects of the noise sources of VCO and loop filter.

$$T2 = (W(s))^2 \left(\frac{4\zeta^4\tau^2}{N^2}\right)\{S_{VCO}(s(1+\tau s))^2 + S_{FILTER}(K_V^2)\} \quad (4.35)$$

Substituting the value of time constant (τ) of loop filter in terms of PLL settling time T_s

$$T2 = (W(s))^2 \left(\frac{\zeta^4 Ts^2}{16N^2}\right)\{S_{VCO}(s(1+\tau s))^2 + S_{FILTER}(K_V^2)\} \quad (4.36)$$

Substituting the value of damping coefficient in terms of PM,

$$T2 = (W(s))^2 \left(\frac{Ts^2}{16N^2}\right)\left(\frac{1}{\left(16\left(cot\phi + \frac{1}{2}\right)^2 - 4\right)}\right)\{S_{VCO}(s(1+\tau s))^2 + S_{FILTER}(K_V^2)\} \quad (4.37)$$

Equations (4.33-4.37) are part of new derivations and have not been discussed in open literature. For design and optimization of design of DAC- PLL, it is always desirable to have a set of closed-form expression which allow usage of variational methods to optimize.

4.9 Differential analysis of Lock time versus PM for second-order PLLs

Lock time of a PLL is defined as the time required in achieving an output frequency, which is within a small but specified range of a desired output frequency when a frequency step of a bounded size is applied to the PLL. A small lock time is necessary for communication systems such as UMTS (less than 200usec) to less than 100usec for WIMAX 802.16e. Lock time is an inverse function of loop bandwidth for PLL of any order. Lower lock times can lead to additional phase noise and jitter variance at the output of PLL.

A closed-form expression relating lock time and damping coefficient of a second-order Type II PLLs has been derived. Locking is achieved in a PLL, when the output frequency of PLL approaches a desired and specified frequency after the application of a frequency step. During

locking an absolute frequency difference between the frequency of output of the PLL and the target frequency must be specified.

The frequency step applied to the PLL must be within the lock range of the PLL. The lock range is defined as the maximum frequency range within which the PLL can track its input frequency. Lock time has been defined by [Banerjee, 2006] as

$$T_{lock} = \frac{-ln\left(\frac{tol}{(f2-f1)}\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)}{\zeta\omega_n} \tag{4.38}$$

In Equation (4.38), T_{lock} is lock time of a second-order Type I PLL, time (in seconds) required for PLL to reach an output value which differs from the final target frequency by a deviation (specified in Equation (4.38) by the variable tol) or less. In Equation (4.38), variable ζ is the damping coefficient of the second-order PLL, ω_n is the natural frequency of the second-order PLL in radians /second, $(f2-f1)$ is the size of frequency input step to the PLL (Hz), and tol is the final tolerance of frequency (Hz). The final tolerance is defined as the deviation of the PLL frequency to the final target frequency. $R2C2$ is the time constant of the loop filter (in seconds).

If the time constant of the loop filter is small $T2 = R2C2 \ll 1$(an approximation that is reasonable in practical PLLs), the expression for lock time can be further simplified as,

$$T_{lock} = \frac{-ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right)}{\zeta\omega_n} \tag{4.39}$$

Equation (4.39) is valid only if $T2 = R2C2$ is very small, that is for low time constants. An expression for the derivative of lock time with respect to the damping coefficient can be obtained by taking derivatives of both sides of Equation (4.39).

$$\frac{\partial T_{lock}}{\eth\zeta} = ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right)\left(\frac{1}{\zeta^2\omega_n}\right) - \frac{1}{\zeta\omega_n}\left(\frac{1}{\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}}\right)\frac{tol}{(f2-f1)}\frac{\partial}{\eth\zeta}\left(\sqrt{1-\zeta^2}\right) \tag{4.40}$$

Simplifying Equation (4.40), one obtains a further simplified expression for lock time gradient That is the derivative of lock time with respect to the damping coefficient as

$$\frac{\partial T_{lock}}{\eth \zeta} = ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right)\left(\frac{1}{\zeta^2\omega_n}\right) - \left(\frac{1}{(1-\zeta^2)\omega_n}\right) \tag{4.41}$$

The Equation (4.41) depicts the variation of the lock time with damping coefficient and comprises of two terms. The differential relationship of Equation (4.41) allows the computation of a locally optimized value of damping coefficient within a certain range to achieve a narrower range of the lock time. Equations (4.40) and (4.41) are not discussed in the open literature. When ζ is small and for a large ω_n, the variation in lock time is an inverse function of the frequency step size ($f2-f1$). Since the lock time is inversely proportional to ω_n, higher the natural frequency, lower is the lock time. In the hybrid DDS -PLL, the lock time is determined by the highest possible ω_n and an optimal value of ζ , which reduce lock time without compromising the lock range. A closed-form expression for the relationship between the derivative of the lock time and the loop Band Width (BW) has been obtained. Upon the substitution of the relation between natural frequency ω_n and loop BW, Equation (4.41) can be written as

$$\frac{\partial T_{lock}}{\partial \zeta} = \frac{1}{\omega_n}\left\{\frac{1}{\zeta^2} ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right) + \frac{1}{(1-\zeta^2)}\right\} \tag{4.42}$$

Substituting the natural frequency in terms of loop BW, the final expression is obtained in terms of loop bandwidth (ω_c) and ζ as

$$\frac{\partial T_{lock}}{\partial \zeta} = \frac{2\zeta}{\omega_c}\left\{\frac{1}{\zeta^2} ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right) + \frac{1}{(1-\zeta^2)}\right\} \tag{4.43}$$

The difference between the Equations (4.42 and 4.43) is that a substitution has been made to express the loop BW in terms of natural frequency using the equation proposed by [Banerjee,2006] is written as

$$\omega_c = 2\zeta\omega_n \tag{4.44}$$

Equation (4.43), demonstrates that the sensitivity of the lock time to the damping coefficient is inversely proportional to the loop BW (ω_c). Such an expression in a differential form relating the gradient of the lock time with ζ of second-order PLL and its loop BW has not been discussed in open literature.

Figure 4.11 illustrates the variation of the lock time of a second order PLL with the change in PM for various values of natural frequency. Figure 4.11 reveals that the lock time of a second-order PLL drops rapidly, as the PM or ζ, is increased. The second observation is that lock time is inversely proportional to the natural frequency (ω_n) of PLL.

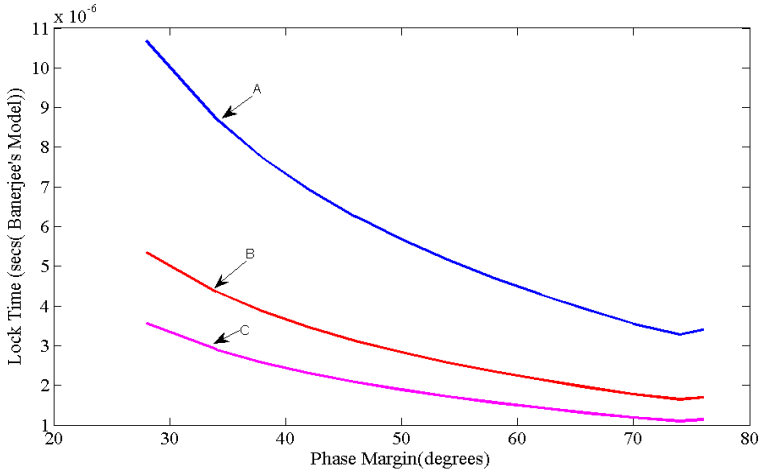


Figure 4.11 Lock Time versus PM for Type I second-**order PLL (A: 2.6MHz; B: 5.2MHz; C: 7.8MHz)**

The result of Figure 4.11 tracks generated for a frequency step size of 1 MHz ($f2 - f1$) and a frequency tolerance (tol) of 1 kHz. Equation (16.39) of (Banerjee, 2005) provides the relationship between PM with the damping coefficient can be written as

$$(sec\phi - tan\phi) = \frac{1}{4\zeta^2} \tag{4.45}$$

In Equation (4.45), ϕ is the phase margin and ζ is the damping coefficient.

Taking derivative of both sides of Equation (4.45) with respect to the damping coefficient (ζ),

$$(sec\phi tan\phi - sec^2\phi) = \frac{1}{8\zeta^3}\frac{d\zeta}{d\phi} \tag{4.46}$$

By using the result of Equation (4.46) and substituting in Equation (4.43), an expression relating the derivative of the lock time to the PM can be derived as

$$\frac{dT_{lock}}{d\phi} = \left(\frac{2\zeta}{\omega_c}\left\{\frac{1}{\zeta^2} ln\left(\frac{tol}{(f2-f1)}\sqrt{1-\zeta^2}\right) + \frac{1}{(1-\zeta^2)}\right\}\right)\left((sec\phi tan\phi - sec^2\phi)8\zeta^3\right) \tag{4.47}$$

A closed-form expression (Equation 4.47) for the derivative of lock time with respect to PM has not been derived in open literature. Its effectiveness is that it expresses perturbation of speed of response with respect to PM. A perturbation of either K_V (VCO sensitivity) or capacitance of loop filter (C) leads to a perturbation of a PM of PLL (Equation 4.32). The perturbation of the lock time for a nominal PM value is illustrated in Figure 4.12.

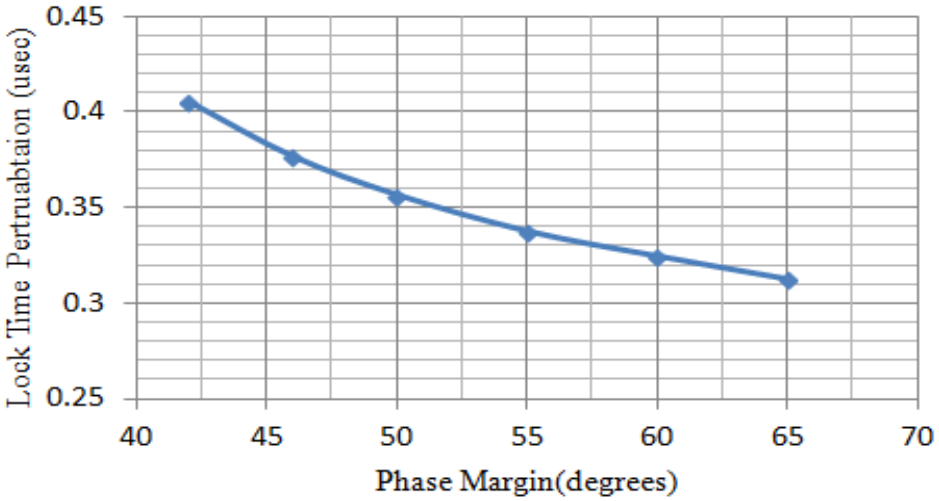


Figure 4.12 Perturbation of Lock Time with nominal Phase Margin(degrees)

The lock time perturbation versus phase margin (Figure 4.12) was generated for an input frequency step size of 1 MHz and a tolerance of 1 kHz. The X –axis of Figure 4.12 is the PM before perturbation and the Y axis in Figure 4.12 is the perturbation of the lock time in microseconds. With the above specified parameters, the lock time is the time required to settle within 1 kHz of the final frequency. The natural frequency of the PLL is as low as 10 MHz frequency. At higher levels of PM (55^o and above), the variation in lock time is lower for a given PM. A unique compact equation in the form of Equation (4.48) which relates the lock time directly to tangent of the phase margin, has been derived for the first time (detailed derivation is presented in Appendix B).

$$T_{lock} = \frac{1}{\frac{\omega_n}{2}\sqrt{\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{\left(1-tan\left(\frac{\phi}{2}\right)\right)}}}\left(\ln\left(1-\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{4\left(1-tan\left(\frac{\phi}{2}\right)\right)}\right)-2\ln\left(\frac{tol}{(f2-f1)}\right)\right) \quad (4.48)$$

A third form of expression relates the T_{lock} to the loop filter time constant (τ). This has not been discussed in open literature and relates lock time to PM:

$$T_{lock} = 2\tau\left(-ln\Gamma_{tol} - \frac{1}{2}ln\left(1 - \frac{\left(1 + tan\left(\frac{\phi}{2}\right)\right)}{4\left(1 - tan\left(\frac{\phi}{2}\right)\right)}\right)\right) \tag{4.49}$$

In Equation (4.49) $\Gamma_{tol} = \left(\frac{tol}{(f2-f1)}\right)$

Equation (4.48) relates the PLL lock time to its filter time constant and half of its phase margin. It is a key contribution of this chapter. The derivation of Equation (4.49) is provided in the last part of Appendix B (Equation B.20). Equation (4.49) relates the loop filter time constant with the lock time of the PLL - a result that has not been discussed in open literature.

4.10 Link between the lock time and phase noise for second-order PLL

In this section, a formulation that links the lock time to the phase noise of second-order PLL is presented. Equation (4.34) for phase noise is repeated here to describe an extension,

$$T2 = (W(s))^2\left(\frac{4\zeta^4\tau^2}{N^2}\right)\{S_{VCO}(s(1+\tau s))^2 + S_{FILTER}(K_v^2)\} \tag{4.50}$$

Now, by observing the variables $\frac{1}{K^2} = \frac{4\zeta^4\tau^2}{N^2}$ and relating the time constant 'τ' to the lock time 'T_{lock}' (using Equation (4.49)) one obtains:

$$4\tau^2 = \frac{(T_{lock})^2}{\left(-ln\delta - \frac{1}{2}ln\left(1 - \frac{\left(1 + tan\left(\frac{\phi}{2}\right)\right)}{4\left(1 - tan\left(\frac{\phi}{2}\right)\right)}\right)\right)^2} \tag{4.51}$$

The derivation for lock time (T_{lock}) is explained in Appendix B. The final expression for $T2$ can be derived as

$$T2$$

$$= (W(s))^2 \left(\frac{1}{N^2} \left\{ \frac{\left(1 + tan\left(\frac{\phi}{2}\right)\right)}{4\left(1 - tan\left(\frac{\phi}{2}\right)\right)} \right\}^2 \left\{ \frac{(T_{lock})^2}{\left(-ln\delta - \frac{1}{2} ln\left(1 - \frac{\left(1 + tan\left(\frac{\phi}{2}\right)\right)}{4\left(1 - tan\left(\frac{\phi}{2}\right)\right)} \right) \right)^2} \right\} \right) \{S_{VCO}(s(1 \quad (4.52)$$

$$+ \tau s))^2 + S_{FILTER}(K_V^2)\}$$

This expression relates lock time, phase margin and phase noise. Equation (4.51) is unique and has never been derived in open literature. It is a key contribution of this chapter.

4.11 Relationship between jitter and phase margin – extension to [Lee, 2002] and [Mansuri, 2002]

This section describes the relationship between jitter and PM for a Type I and Type II second-order PLL. Some of the derivations in this section originate with the work of [Lee, 2002] & [Mansuri,2002]. Type I PLL has been discussed in the previous sections. A brief discussion on Type II PLL in terms of its transfer function is also presented. The Type II PLL of second-order has an additional zero as compared to a Type I PLL of second-order.

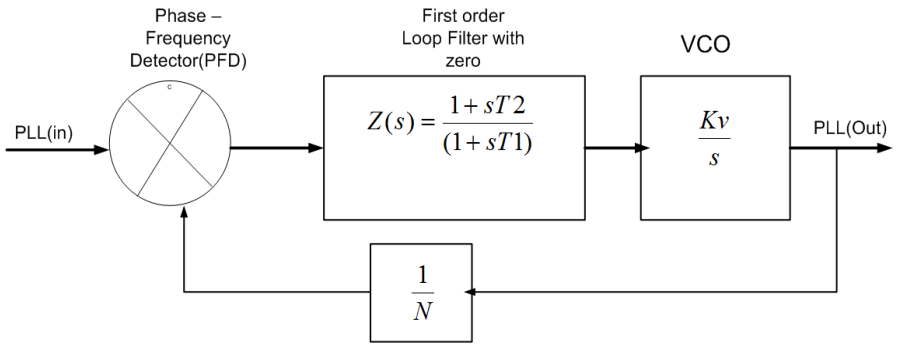


Figure 4.13 Type II PLL illustrating loop filter with one pole and one zero

The block diagram of Figure 4.13 illustrates the loop filter, VCO, divider, and PFD of a second-order Type II PLL. The transfer function, the natural frequency and damping coefficient of a Type II PLL are derived for logical continuity. The transfer function of a Type II PLL can be written as

$$G(s) = \frac{\frac{(1+s\tau_2)}{(1+s\tau_1)}\frac{K}{s}}{1+\frac{(1+s\tau_2)}{N(1+s\tau_1)}\frac{K}{s}} = \frac{N(1+s\tau_2)K}{Ns + Ks\tau_2 + N\tau_1 s^2 + K} \tag{4.53}$$

Dividing numerator and denominator of Equation (4.53) by $N\tau_1$, the transfer function of a Type II PLL can be written in a classical form as

$$G(s) = \frac{NK(1+s\tau_2)}{N\tau_1 s^2 + s(N+K\tau_2) + K} = \frac{\omega_n^2 + (\frac{K\tau_2}{\tau_1})s}{s^2 + s2\zeta\omega_n + \omega_n^2} \tag{4.54}$$

For a Type II PLL the natural frequency is defined as

$$\omega_n = \sqrt{\frac{K}{N\tau_1}} \tag{4.55}$$

The damping coefficient for a Type II PLL can be written as

$$\zeta = \frac{1}{2\omega_n}(N + K\tau_2) \tag{4.56}$$

This section discusses the relationship between jitter and phase margin of a Type I and Type II second-order PLL. Type I and Type II PLLs differ in the fact that Type II PLLs have a zero in their transfer function which is not the case in a Type I PLL. This results in different transfer functions for Type I and Type II PLLs as illustrated in Figure 4.14.

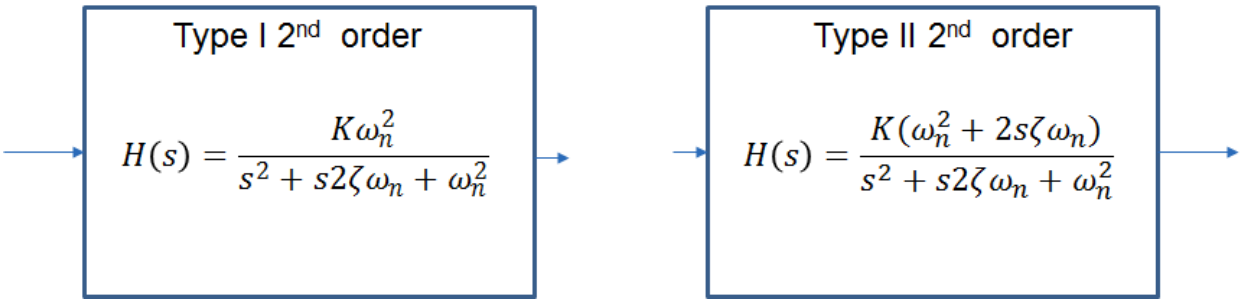


Figure 4.14 Difference in TFs of Type I and Type II PLL

Jitter is defined as the variation of period of a sinusoidal output of a DDS-PLL[Cordesses,2003]. This section analyses Jitter in the time domain mainly through the computation of Jitter variance. Absolute jitter is a time varying quantity best described as the difference between successive zero crossing times of a waveform [Lee, 2002] which is expressed as

$$\{j_{a,n} = t_n - nT\} \tag{4.57}$$

In Equation (4.57), t_n is the time of Zero crossing at the end of nth cycle, nT is the cycle number multiplied by the nominal period of a waveform. The discrete sequence $j_{a,n}$ is the absolute jitter in the nth cycle. T is nominal period of a waveform.

The absolute jitter in Equation (4.57) is a sequence of values (hence it is expressed within curly brackets). The absolute jitter can be expressed in radians as([Lee,2002],

$$\{\theta_{a,n} = 2\pi f_0(t_n - nT)\} \tag{4.58}$$

In Equation (4.58), f_0 is the nominal frequency of an oscillator, t_n is the zero crossing at n^{th} cycle end, T is the nominal period of the waveform, and $\theta_{a,n}$ is the phase in radians.

If the nominal period for a time domain waveform is known and the zero crossing points of the said time domain waveform are accurately known, then the period jitter can be defined in a way as proposed by ([Lee,2002]).

$$\{j_n = t_{n+1} - t_n - T\} \tag{4.59}$$

In Equation (4.59), T is the nominal period of a waveform, t_n is the zero crossing at n^{th} cycle end, t_{n+1} is the zero crossing at $(n+1)^{th}$ cycle end, and j_n is the period jitter of n^{th} cycle. In Equation (4.59) period jitter is a sequence of time values. Sequence j_n captures the variation of the period from the nominal period in a PLL.

The period jitter variance is related to the phase noise generated by various sources of noise within the PLL using the following Fourier integral([Mansuri,2002]), is written as

$$\sigma_j^2(kT) = \frac{1}{(\pi f_0)^2}\int_{-f_0/2}^{f_0/2} \sin^2(\pi f k_B T) S_\theta(f) df \tag{4.60}$$

In Equation (4.60), $S_\theta(f)$ is the phase noise of a frequency source, f_0 is frequency BW under consideration, $\sigma_j^2(kT)$ is the variance of period Jitter, k_B is the Boltzmann's constant, and T is the

absolute temperature. If the phase noise of the signal is known, Equation (4.60) facilitates the computation of jitter variance of the same signal either through numerical integration or analytically, using a definite Fourier integral. Considering only the noise source of VCO, a relationship between Root–Mean Square (RMS) Jitter variance, damping coefficient and natural frequency have been given by [Lee, 2002] for a second-order Type II PLL.

$$\sigma_A^2 = \frac{c_{WN}}{4\zeta\omega_n} + \frac{c_{FN}}{\omega_n^2} f(\zeta) \tag{4.61}$$

In Equation (4.61), σ_A^2 is the variance of absolute jitter at PLL output (sec^2), c_{WN} is the jitter coefficient for white noise (unit seconds), c_{FN} is the jitter coefficient for flicker noise (dimensionless), ω_n is the natural frequency of Type II second-order PLL, and ζ is the damping coefficient of Type II second order PLL. Function $f(\zeta)$ is the non-linear function relating the damping coefficient to the flicker noise.

The relationship in Equation (4.61) comprises two terms – the first term is the contribution of the white noise and the second term is the contribution of the flicker noise. The flicker noise coefficient is a function of the damping coefficient and the PM of the PLL. For an underdamped PLL, the flicker noise coefficient has been described by [Lee, 2002] as

$$f(\zeta) = \frac{\frac{\pi}{2} - tan^{-1}\left(\frac{\zeta}{\sqrt{1-\zeta^2}}\right)}{\zeta\sqrt{1-\zeta^2}} \quad for\ \zeta < 1 \tag{4.62}$$

The corresponding expression in [Lee, 2002] for the flicker noise coefficient of an over-damped PLL is written as

$$f(\zeta) = \frac{Re(tanh^{-1}\left(\frac{\zeta}{\sqrt{\zeta^2-1}}\right))}{\zeta\sqrt{\zeta^2-1}} \quad for\ \zeta > 1 \tag{4.63}$$

The operator Re in Equation (4.63) implies only the real part of the hyperbolic inverse is considered.

The first contribution of this thesis to the theory advanced by [Lee, 2002] is an analytical one. It relates the PM to the closed-form jitter variance for a Type II PLL. The first step is to compute a simpler form of the flicker noise coefficient. By rearranging the terms in Equation (4.61), one obtains:

$$f(\zeta)\zeta\sqrt{1-\zeta^2} = \frac{\pi}{2} - \tan^{-1}\left(\frac{\zeta}{\sqrt{1-\zeta^2}}\right) \tag{4.64}$$

Using basic trigonometry, one simplifies the RHS of Equation (4.64) as

$$f(\zeta)\zeta\sqrt{1-\zeta^2} = \frac{\pi}{2} - \sin^{-1}(\zeta) \tag{4.65}$$

The damping coefficient $'\zeta'$ and PM 'ϕ' are related through Equation (4.9) which is repeated here for continuity:

$$\zeta^4 = \frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)} \tag{4.66}$$

By taking the fourth root of both sides of Equation (4.66), one obtains an expression for the damping coefficient in terms of PM:

$$\zeta = \sqrt[4]{\frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)}} \tag{4.67}$$

By substituting the value of ζ from Equation (4.67), the flicker noise function can be written as

$$f(\zeta) = \frac{\frac{\pi}{2} - \sin^{-1}\left(\sqrt[4]{\frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)}}\right)}{\sqrt[4]{\frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)}}\sqrt{1 - \sqrt{\frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)}}}} \tag{4.68}$$

Equation (4.68) relates the flick noise function $f(\zeta)$ in terms of PM 'ϕ'. Substituting Equation (4.68) into the expression for jitter in [Lee, 2000], (Equation (4.60)) one obtains an expression for the jitter variance.

$$\sigma_A^2 = \frac{c_{WN}}{4\zeta\omega_n} + \frac{c_{FN}}{\omega_n^2} f(\zeta) \tag{4.69}$$

After substituting the values of the damping coefficient in terms of PM one obtains a single expression for the jitter variance which is written as

$$\sigma_A^2 = \frac{c_{WN}}{4\sqrt[4]{\frac{1}{\left(16\left(cot^2\phi+\frac{1}{2}\right)^2-4\right)}}\,\omega_n} + \frac{c_{FN}}{\omega_n^2}\left\{\frac{\frac{\pi}{2}-sin^{-1}\left(\sqrt[4]{\frac{1}{\left(16\left(cot^2\phi+\frac{1}{2}\right)^2-4\right)}}\right)}{\left(\sqrt[4]{\frac{1}{\left(16\left(cot^2\phi+\frac{1}{2}\right)^2-4\right)}}\right)\left(\sqrt{1-\sqrt{\frac{1}{\left(16\left(cot^2\phi+\frac{1}{2}\right)^2-4\right)}}}\right)}\right\} \quad (4.70)$$

The direct relationship as expressed in Equation (4.70), for an underdamped Type II PLL between the PM and jitter variance has not been reported in open literature. Equation (4.70) allows computation for the variance of absolute jitter, if the PM (ϕ) is known.

Alternative Relationship Between PM and Absolute Jitter for Type II PLL

The relation between PM and absolute jitter for type II PLL can be analytically derived using another procedure. The loop bandwidth (ω_c) of a PLL can be expressed as a function of its natural frequency (ω_n) [Banerjee,2005] as

$$\omega_c = (2\zeta)\omega_n \quad (4.71)$$

The damping coefficient (ζ) can be expressed in terms of PM as

$$\zeta = \frac{\omega_c}{2\omega_n} \quad (4.72)$$

From the Equation provided by [Banerjee, 2005], one obtains:

$$sec\phi - tan\phi = \frac{1}{4\zeta^2} \quad (4.73)$$

Modifying Equation (4.71) by substituting the values of $sec\phi$ and $tan\phi$ one obtains:

$$\zeta = \frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}} \tag{4.74}$$

The expression for the variance of absolute jitter (σ_A^2) can be written as

$$\sigma_A^2 = \frac{c_{WN}}{4\zeta\omega_n} + \frac{c_{FN}}{\omega_n^2}\frac{\frac{\pi}{2} - sin^{-1}(\zeta)}{\zeta\sqrt{1-\zeta^2}} \tag{4.75}$$

Substituting $\zeta = \frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}$ and $\zeta^2 = \frac{cos\phi}{4(1-sin\phi)}$into Equation (4.75), one obtains the expression connecting the PM(ϕ) with the variance of absolute jitter(σ_A^2)

$$\sigma_A^2 = \frac{c_{WN}}{4\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\omega_n} + \frac{c_{FN}}{\omega_n^2}\frac{\frac{\pi}{2} - sin^{-1}\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)}{\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}} \tag{4.76}$$

Equation (4.76) facilitates the determination of the absolute jitter for the under-damped Type II second-order PLL in terms of PM. Such an expression is not expressed in open literature. It is an original contribution of this chapter.

For the over-damped Type II second-order PLL, the numerator of the jitter variance expression (Equation 4.62) is a hyperbolic function. In this case the variance of absolute jitter can be simplified by substituting the damping coefficient in terms of the PM of the PLL and it can be written as

$$\sigma_A^2 = \frac{c_{WN}}{4\zeta\omega_n} + \frac{c_{FN}}{\omega_n^2}\frac{Re(tanh^{-1}\left(\frac{\zeta}{\sqrt{\zeta^2-1}}\right))}{\zeta\sqrt{\zeta^2-1}} \tag{4.77}$$

Substituting $\zeta = \frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}$ in Equation (4.77), one obtains

$$\sigma_A^2 = \frac{c_{WN}}{4\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\omega_n} + \frac{c_{FN}}{\omega_n^2}\frac{Re(tanh^{-1}\left(\frac{\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}}{\sqrt{\frac{cos\phi}{4(1-sin\phi)}-1}}\right))}{\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\sqrt{\frac{cos\phi}{4(1-sin\phi)}-1}} \tag{4.78}$$

Equation (4.78) relates the absolute jitter for over-damped Type II second-order PLL with its PM. An expression such as Equation (4.78) is new and has is not been expressed in open literature. Figure 4.15 depicts jitter variance versus PM for various values of ω_n.

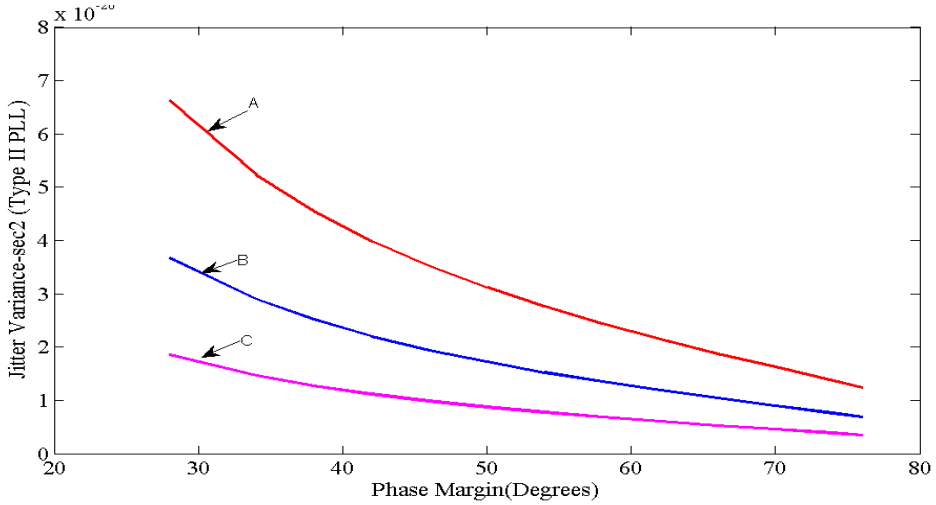


Figure 4.15 Jitter Variance versus Phase Margin for Type II PLL (A: ω_n =3.46x 10^4 rad/sec**;** B: ω_n =4.9x10^4 rad/sec; C: ω_n =6.9x10^4 rad/sec)

Figure 4.15 illustrates that greater the PM is, lower is the jitter variance for Type II PLL is. Figure 4.15 is computed for the values of $c = 1.67x10^{-17}sec;\ c_{FN} = 1.6x - 10^{-11}$. For the same level of the phase margin (for example 50°), the jitter variance is significantly reduced, as ω_n is increased. The greater the natural frequency is the lower is the jitter variance.

[Mansuri, 2002] has derived closed-form jitter variance models for type I PLL of second-order. Mansuri defines a noise figure κ for the VCO noise source. The noise figure of a noise source of VCO which is defined as $'\kappa'$ can be written as

$$\kappa = \sqrt{\frac{4\pi^2 N_{VCO}}{\omega_0^2}} \tag{4.79}$$

In Equation (4.79), ω_0 is the center frequency of VCO and N_{VCO} is the phase noise of VCO, dBc/Hz. In Equation (4.79), the units of κ are $1/\sqrt{Hz}$ or $\sqrt{sec}$. The VCO noise term N_{VCO} is a product of two terms, $K^2 e_n^2 = Hz^2/V^2 * V^2/Hz$. The unit of the constant K^2(gain of the clock source oscillator) is Hz/V and the unit of the white noise voltage e_n is volts /$\sqrt{Hz}$. Equation (4.79)

assumes that the VCO is a white noise source. Figure 4.18 illustrates the change in jitter variance with the change in PM for an under damped PLL. Jitter variance for Type I second-order under-damped PLL([Mansuri,2002]) can be shown as

$$\sigma_{\Delta T}^2 = \left(\frac{4\pi^2 N_{VCO}}{\omega_0^2}\right)\left\{\left(\frac{1}{2\zeta\omega_n}\right) + \left\{\frac{e^{-\Delta T\zeta\omega_n}}{2(1-\zeta^2)}\left(\frac{sin(\omega_d\Delta T+\theta)}{\omega_n} - \frac{cos(\omega_d\Delta T)}{\zeta\omega_n}\right)\right\}\right\} \quad (4.80)$$

In the Equation (4.80) the damped frequency (ω_d) is defined as

$$\omega_d = \omega_n\sqrt{1-\zeta^2} \quad (4.81)$$

And an additional phase shift which is written as

$$\theta = cos^{-1}\sqrt{1-\zeta^2} \quad (4.82)$$

Figure 4.16 illustrates the change in jitter variance with the change in PM for an under damped PLL.

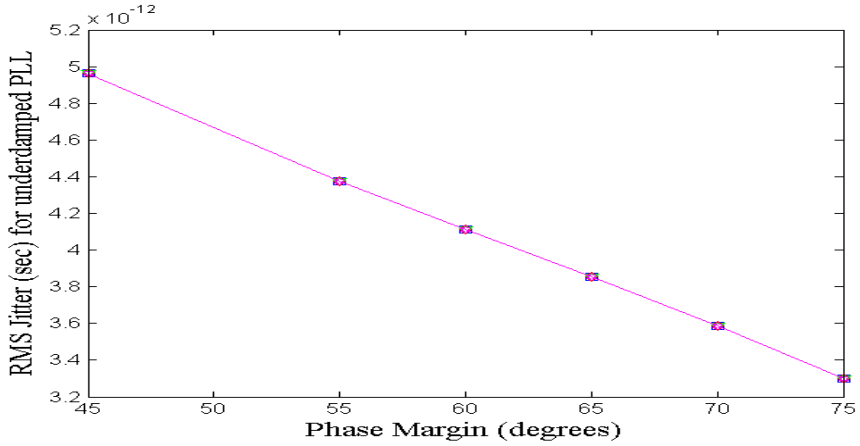


Figure 4.16 RMS jitter predicted by [Mansuri's 2002] model for under-damped second-order PLL (VCO noise)

The results of Figure 4.16, the damping coefficient ζ ranges from 0.42 to 0.9 with the figure of merit (κ) being a fixed value of $\kappa = 5.4x10^{-8}\sqrt{sec}$.

To compute the results of Figure 4.16 one must take into consideration each value of PM that corresponds to a unique value of ζ. This computed value of ζ is plugged into the time-invariant (not a function of part of ΔT in Equation (4.78) to compute the jitter variance. The exponential

term in Equation (4.78) can be safely neglected as it goes to zero when the interval ΔT goes to infinity. Figure 4.16 illustrates that the RMS jitter value is reduced by 36% (from $5x10^{-12}$ sec^2 to $3.2x10^{-12}$ sec^2) as the PM increases from 45° to 75°.To simplify the analysis one must first consider the function without the brackets in the RHS of Equation (4.78). This function represents the multiplicative part of jitter variance, which is independent the figure of merit parameter in Equation (4.78).

$$\Psi(\zeta, \omega_n, \Delta T) = \left\{ \frac{e^{-\Delta T \zeta \omega_n}}{2(1-\zeta^2)} \left(\frac{sin(\omega_d \Delta T + \theta)}{\omega_n} - \frac{cos(\omega_d \Delta T)}{\zeta \omega_n} \right) \right\} \tag{4.83}$$

In Equation (4.83), ΔT is the time interval under consideration for jitter measurement. ω_d is defined in Equation (4.81) and angle θin Equation (4.82).

$\Psi(\zeta, \omega_n, \Delta T)$ is defined as the "Mansuri's jitter variance function". It is the part of jitter variance that depends on the time interval ΔT . The jitter variance function is the part which is dependent only on $\Delta T, \zeta \; and \; \omega_n$. It is the only part that can be designed in a PLL with a given noise level of VCO which controls $\left(\kappa^2 = \frac{4\pi^2 N_{VCO}}{\omega_0^2}\right)$. The parameter '$\kappa^2$' cannot be altered by the PLL designer without using a different VCO. A trade off can be made between the jitter variance function and PLL performance parameters such as PM and settling time, $T_{sPLL} = \frac{4}{\zeta \omega_n}$.

Figure 4.17 shows the variation of jitter variance with ΔT, the time interval for jitter variance estimation for various values of the PM. The Y axis of Figure 4.17 is the jitter variance divided by $\kappa^2 = \frac{4\pi^2 N_{VCO}}{\omega_0^2}$. κ^2 is term as the figure of merit of the VCO. After an initial transient, only the steady state part contained in the first term of Equation (4.78) dominates, this is when ΔT is larger.

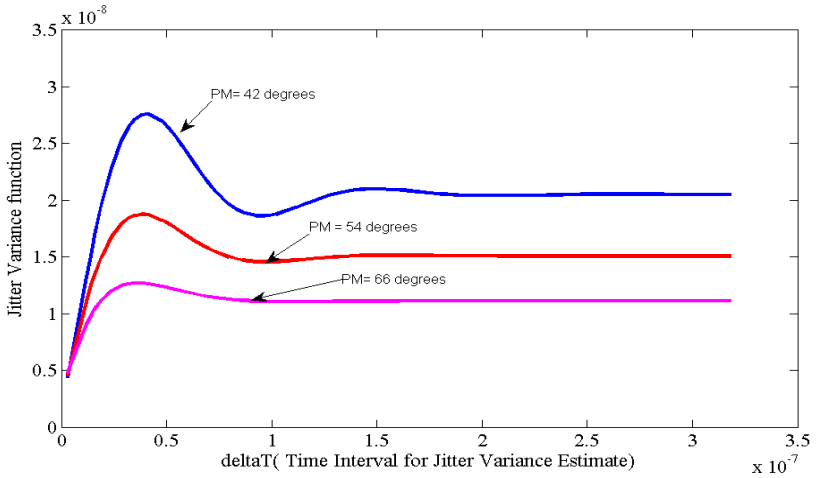


Figure 4.17 Jitter Variance function versus ΔT for 3 values of PM (for 3 values of damping coefficient) for second-order under-damped PLL

Figure 4.17 illustrates that the component, which is a function of time interval (ΔT), ω_n and (ζ), damping coefficient exhibits oscillatory behavior and settles down to a final value within $\Delta T = 2 \times 10^{-7}$. The higher the phase margin (damping coefficient, ζ) the lower is the final value of jitter variance and lower is the initial high part of the jitter variance. Figure 4.17 is illustrated for 3 values of PM (for an under damped PLL). Between a PM of 42° and that of 66°, the initial peak reduces by 50% (from 26×10^{-8} to 1.2×10^{-8}). Figure 4.18 illustrates the jitter variance function in [Mansuri, 2002] versus the PM for a fixed value of ΔT.

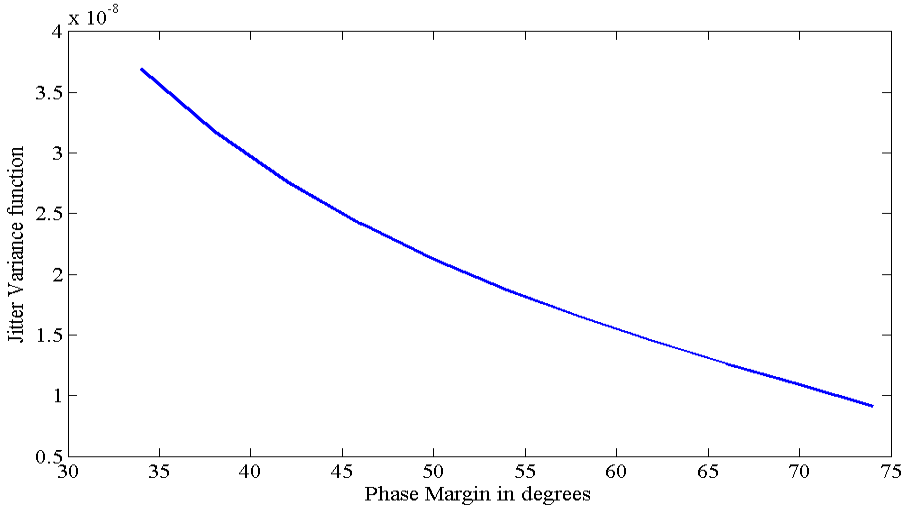


Figure 4.18 Jitter Variance function for fixed ΔT close to its peak

Figure 4.18 illustrates the relationship between PM and the jitter variance of a second-order Type I PLL. It is observed that the jitter variance $\sigma_{\Delta T}^2$ for the type I PLL is reduced as the PM is increased. Figure 4.19 illustrates the variation of the jitter variance function with settling time of a second-order PLL.

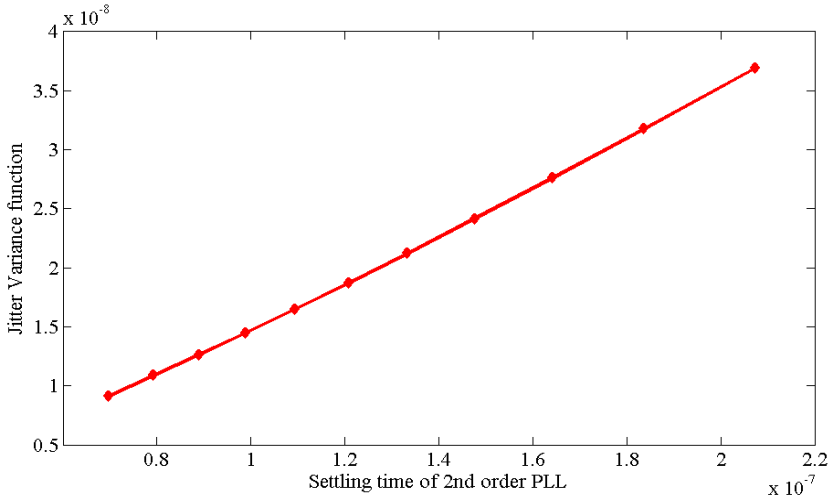


Figure 4.19 Jitter Variance function ($\Psi(\zeta, \omega_n, \Delta T)$) versus settling time of a second-order Type I PLL

Figure 4.19 illustrates that the jitter variance function increases with an increased settling time (a lower damping coefficient) and therefore, a faster settling PLL is better from a jitter standpoint. Lower settling times imply a larger damping coefficient and larger phase margin. From the results of Figure 4.19, it is observed that for under damped PLLs, higher PM results in lower settling time and lower jitter variance. If the settling times are high (Figure 4.19), the damping coefficients are lower. Hence, jitter variance is higher. Therefore, the PM is lower, and this is associated with higher jitter variance. The jitter variance versus the PM for the over-damped PLL is illustrated in Figure 4.20.

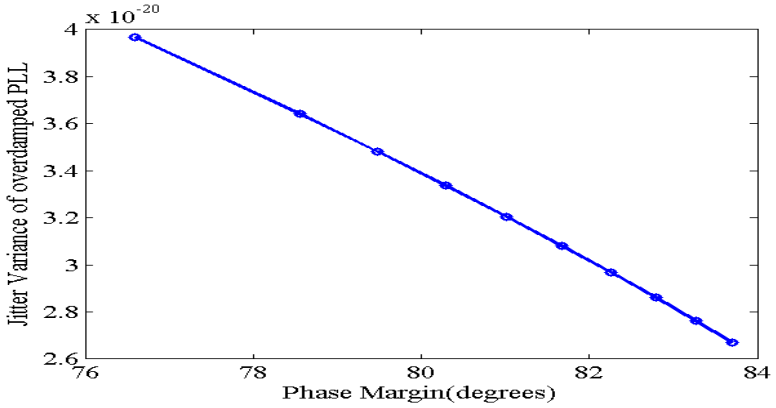


Figure 4.20 Variation of Jitter variance versus phase margin of a second-order PLL

The results of Figure 4.20 illustrate that a higher value of PM is necessary to reduce the value of Jitter variance of a second-order PLL. Increase of PM reduces the Jitter variance from $4x10^{-20}$ to $2.6x10^{-20}$ as the PM increases from 76º to 84º. It can be concluded from Figure 4.20 that the Jitter variance falls almost linearly as the PM is increased for over damped PLLs. Finally, an analytical contribution in the form of an extension to Mansuri's models has been presented in this section. An analytical relationship between the PM(ϕ)and the periodic jitter of PLL is given in Equation (4.76).

Substituting $\zeta = \frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}$ in the jitter variance expression of [Mansuri, 2002] for underdamped PLLs in Equation (4.78),

$$\sigma_{\Delta T}^2 = \kappa^2\{\left(\frac{1}{2\zeta\omega_n}\right) + \left\{\frac{e^{-\Delta T\zeta\omega_n}}{2(1-\zeta^2)}\left(\frac{sin(\omega_d\Delta T+\theta)}{\omega_n} - \frac{cos(\omega_d\Delta T)}{\zeta\omega_n}\right)\right\}\} \tag{4.84}$$

In Equation (4.84) the constant κ^2 is defined in Equation (4.79).

$$\sigma_{\Delta T}^2 = \kappa^2\{\left(\frac{1}{2\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n}\right) + \left\{\frac{e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n}}{2\left(1-\frac{cos\phi}{4(1-sin\phi)}\right)}\left(\frac{sin(\omega_d\Delta T+\theta)}{\omega_n} - \frac{cos(\omega_d\Delta T)}{\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\omega_n}\right)\right\}\} \tag{4.85}$$

The damped frequency (ω_d) is defined in terms of natural frequency (ω_n) and PM as

$$\omega_d = \omega_n \sqrt{1 - \frac{cos\phi}{4(1 - sin\phi)}} \tag{4.86}$$

In Equation (4.86), ϕ is the PM of the PLL. The expression relating jitter to PM jitter in the form in Equation (4.85) is new and has not been discussed by [Mansuri, 2002]. A closed-form expression for the derivative of jitter variance with respect to the PM of a second-order PLL.

The first term is the derivative of the first additive term of the RHS of Equation (4.85),

$$\frac{\partial}{\partial\phi}\left\{\kappa^2 \frac{1}{2\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1 - sin\phi)}}\right)\omega_n}\right\} = \kappa^2 \left\{\frac{1}{2\omega_n} * \frac{sin\phi - 1}{(\sqrt{(1 - sin\phi)})cos^{3/2}\phi}\right\} = T_C \tag{4.87}$$

The second term is the derivative of the exponential term of the second additive term in Equation (4.83),

$$\frac{\partial}{\partial\phi}\left\{\kappa^2 \frac{e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n}}{2\left(1 - \frac{cos\phi}{4(1 - sin\phi)}\right)}\right\} =$$

Equals

$$\kappa^2 \left\{\frac{\sqrt{1 - sin\phi}\; e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n}(4(\Delta T\omega_n)(sin\phi - 1) + (\Delta T\omega)cos\phi + 4\sqrt{1 - sin\phi}\;\sqrt{cos\phi}}{2\sqrt{cos\phi}\;(4sin\phi + cos\phi - 4)^2}\right\} = T_D \tag{4.88}$$

The third term is the derivative of the sinusoidal term of the second additive term in Equation (4.83). Substituting $\omega_d = \omega_n\sqrt{1 - \zeta^2}$ and the additional phase shift angle, $\theta = cos^{-1}\sqrt{1 - \zeta^2}$. The final substitution is $\zeta^2 = \frac{cos\phi}{4(1-sin\phi)}$

$$T_E = \frac{\partial}{\partial\phi}\left\{\left(\frac{sin(\omega_d\Delta T + \theta)}{\omega_n}\right)\right\} =$$

equals

$$(cos\left(\omega_n\sqrt{1-\zeta^2}\Delta T+cos^{-1}\left(\sqrt{1-\zeta^2}\right)\right)\Delta T)\frac{1}{\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}}$$
$$*\left(\frac{sin\phi}{4\sqrt{cos\phi}\sqrt{1-sin\phi}}\frac{\sqrt{cos\phi}}{2\sqrt{1-sin\phi}}-\frac{\sqrt{cos\phi}}{2\sqrt{1-sin\phi}}\frac{cos^{\frac{3}{2}}\phi}{4(1-sin\phi)^{\frac{3}{2}}}\right) \quad (4.89)$$

$\frac{\partial}{\partial\phi}\left\{\left(\frac{sin(\omega_d\Delta T+\theta)}{\omega_n}\right)\right\}=$

$(cos\left(\omega_n\sqrt{1-\zeta^2}\Delta T+cos^{-1}\left(\sqrt{1-\zeta^2}\right)\right)\Delta T)\frac{1}{\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}}*\left(\frac{sin\phi}{4\sqrt{cos\phi}\sqrt{1-sin\phi}}\frac{\sqrt{cos\phi}}{2\sqrt{1-sin\phi}}-\right.$

$\left.\frac{\sqrt{cos\phi}}{2\sqrt{1-sin\phi}}\frac{cos^{\frac{3}{2}}\phi}{4(1-sin\phi)^{\frac{3}{2}}}\right)=T_E$

(4.87)

The fourth term, is the derivative of $\frac{cos(\omega_d\Delta T)}{\zeta\omega_n}$ with respect to PM ϕ

$$T_F=\frac{\partial}{\partial\phi}\left\{\left(\frac{cos\left(\omega_n\Delta T\sqrt{1-\zeta^2}\right)}{\zeta\omega_n}\right)\right\}=$$

The derivative above equals

$$\left\{\frac{1}{\omega_n}\left(\frac{\omega_n\Delta T\,sin(\omega_n\Delta T\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}}{\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}}-\frac{cos\left(\omega_n\Delta T\sqrt{1-\frac{cos\phi}{4(1-sin\phi)}}\right)}{\frac{cos\phi}{4(1-sin\phi)}}\right)\right\}*$$

Multiplied by a second term

$$\left(\frac{cos^{\frac{3}{2}}\phi}{4(1-sin\phi)^{\frac{3}{2}}}-\frac{sin\phi}{4\sqrt{cos\phi}\sqrt{1-sin\phi}}\right) \quad (4.90)$$

The composite expression for the derivative of Jitter variance with respect to phase margin is,

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$$\frac{\partial \sigma_{\Delta T}^2}{\partial \phi} = T_C + \qquad ()$$

The second term is written as,

$$\left(\frac{\sqrt{1-sin\phi}\; e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n} (4(\Delta T\omega_n)(sin\phi-1) + (\Delta T\omega_n)cos\phi + 4\sqrt{1-sin\phi}\;\sqrt{cos\phi}}{2\sqrt{cos\phi}\;(4sin\phi + cos\phi - 4)^2} \right) \qquad ()$$

$$\frac{\partial \sigma_{\Delta T}^2}{\partial \phi} = T_C +$$

$$\left(\frac{\sqrt{1-sin\phi}\; e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega_n} (4(\Delta T\omega_n)(sin\phi-1)+(\Delta T\omega_n)cos\phi+4\sqrt{1-sin\phi}\;\sqrt{cos\phi}}{2\sqrt{cos\phi}\;(4sin\phi+cos\phi-4)^2} \right) \left\{ \frac{sin(\omega_d \Delta T+\theta)}{\omega_n} - \right.$$

$$\left. \frac{cos(\omega_d \Delta T)}{\zeta \omega_n} \right\} + \frac{e^{-\Delta T\left(\frac{\sqrt{cos\phi}}{2\sqrt{(1-sin\phi)}}\right)\omega}}{2\left(1-\frac{cos\phi}{4(1-sin\phi)}\right)} (T_E + T_F)$$

(4.89)

Equation (4.89) is an original contribution of this chapter. A derivative of the jitter variance with respect to PM is unreported in prior literature and its usefulness is towards optimization techniques such as Lagrange multipliers applied to a PLL.

4.12 The relationship between PM and the angle between two complex poles of a second-order PLL

This section presents an analysis to formulate the relationship between the PM and the two complex poles of a second order PLL. For a second-order PLL, there is a relationship between the PM of the PLL and its pole locations. For an underdamped or overdamped second-order PLL, the relationship between the PM (ϕ) and the damping coefficient (ζ) is expressed as in Equation (4.90). ζ can be expressed directly in terms of ϕ as

$$\zeta^4 = \frac{1}{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)} \tag{4.93}$$

The transfer function for the second-order PLL can be written as

$$TF(s) = \frac{N\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.94}$$

In Equation (4.94), ω_n is the natural frequency of the second-order PLL, ζ is the damping coefficient, and N is the PLL divide ratio. For the existence of two complex poles, the discriminant of the quadratic equation can be written as

$$4\zeta^2\omega_n^2 - 4\omega_n^2 < 0 \tag{4.95}$$

This implies $|\zeta| < 1$, and ζ is positive. For the underdamped PLL ($\zeta < 1$), the two complex conjugate poles $(z1, z2)$ can be written as

$$z1, z2 = \frac{-2\zeta\omega_n \pm j2\omega_n\sqrt{1-\zeta^2}}{2} = -\zeta\omega_n \pm j\omega_n\sqrt{1-\zeta^2} \tag{4.96}$$

From Equation (4.96), the angle Θ between the two complex poles $z1, z2$ is written as

$$\Theta = 2tan^{-1}\left(\frac{\sqrt{1-\zeta^2}}{\zeta}\right) \tag{4.97}$$

Substituting the value of the ζ in terms of the PM (from Equation 4.93), the angle Θ between the two poles of a second-order PLL is expressed in terms of ϕ as after simplification.

$$\Theta = 2tan^{-1}\left\{\sqrt{\left(16\left(cot^2\phi + \frac{1}{2}\right)^2 - 4\right)^{1/2} - 1}\right\} \tag{4.98}$$

The expression relating the angle $'\Theta'$ between the two complex conjugate poles and the PM $'\phi'$ for a second-order PLL has not been explored in open literature. Figure 4.21 depicts the variation of Θ as a function of PM.

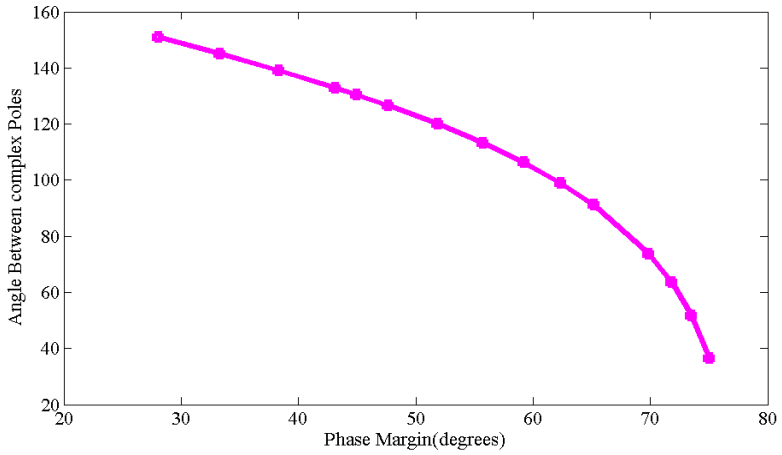


Figure 4.21 Variation of Θ versus ϕ for a second-order PLL

As the PM is increased, the angle between the complex roots becomes smaller, implying their closer angular proximity.

4.13 Phase shift correction in DDS PLL combination

This section discusses phase shifts induced in DDS by DAC and proposes scheme for compensation of phase shift. A cubic polynomial DDS with First-Order Hold Interpolation (FOHI) DAC is considered for further analysis to overcome the effect of resulting static phase which can be attributed to the FOHI DAC. This section proposes and analyzes a phase compensating scheme introduced at the output of the FOHI DAC.

4.13.1 Phase shifts of ZOH and FOHI DAC

The magnitude and phase of the (Zero-Order Hold) ZOH-DAC transfer function [Cleveland, 1976] can be written as

$$A = \frac{2}{\omega T_d} sin\left(\frac{\omega T_d}{2}\right) \tag{4.99}$$

The phase shift due to a ZOH-DAC is written as

$$\phi_{ZOH} = -\frac{\omega T_d}{2} \tag{4.100}$$

In Equation (4.99), T_d is the sampling interval of the ZOH DAC, where ω is the angular frequency of sinusoidal input to the ZOH DAC. In turn, A is the magnitude part of the transfer function for ZOH DAC. ϕ is the phase part of transfer function for ZOH-DAC.

The magnitude(A) and phase(ϕ_{FOHI}) of the (First-Order Hold Integral) FOHI- DAC transfer function [Cleveland, 1976] can be represented as

$$A = \frac{4}{\omega^2 {T_d}^2} sin^2\left(\frac{\omega T_d}{2}\right) \tag{4.101}$$

The phase shift due to a FOHI DAC is written as

$$\phi_{FOHI} = -\omega T_d \tag{4.102}$$

A comparative illustration of variation of the phase of transfer functions of the ZOH and the FOHI-DACs with change in ωT_d is depicted in Figures 4.22.The change in the phase shift and not the magnitude change, is the focus of this chapter and its range is only 6% for a range of (ωT_d) from 0.1 to 0.99.

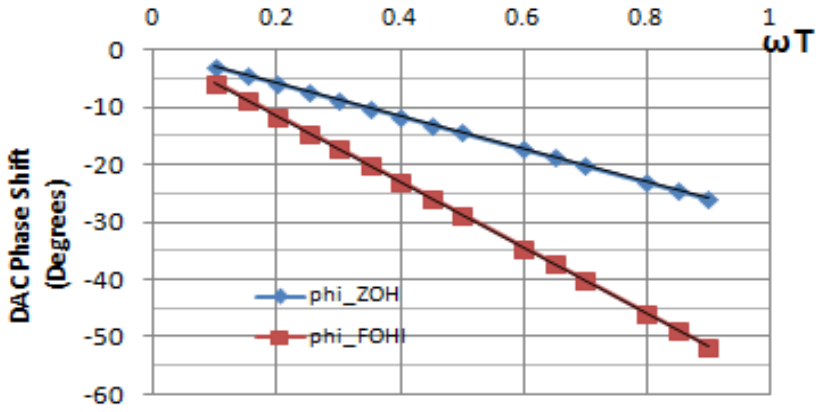


Figure 4.22 Phase of Transfer Function vs ωTplot for ZOH and FOHI DACs

The results of Figure 4.22 indicate of relative sharp roll-off of the phase of FOHI DAC. Let ϕ and θ be the phase of the transfer function of DAC and the initial phase of the input waveform respectively. The transfer function of the FOHI DAC in polar form can be expressed as

$$H(s) = |H(s)|\angle\phi = Ae^{j\phi_{FOHI}} \tag{4.103}$$

In Equation (4.103), the terms A and ϕ_{FOHI} are defined in Equations (4.101) and (4.102) respectively. With the amplitude M of the input waveform, output the the FOHI DAC can be written as

$$V(\omega, t, \theta) = MAe^{j(\omega t+\theta_s+\phi)} \tag{4.104}$$

The additional phase shift (ϕ) is determined by the sampling interval of DAC (Equation (4.102) and cannot be ignored for systems where a phase shift of the generated waveform is important. A phase compensation circuitry designed to offset the phase shift ϕ through the DAC is covered in the following sub section. Angle θ_s in Equation (4.104) is the original phase of the input (input is assumed to be of the form $Ae^{j(\omega t+\theta_s)}$.

4.13.2 Analog Phase Compensation for phase shift of DAC

A schematic representation of the phase compensating network to offset the phase shift (ϕ introduced by FOHI DAC is depicted in Figure 4.23. In this section the angle θ is used to denote the phase shift due to the phase compensator and the angle ϕ is used to denote the phase shift due to the DAC alone.

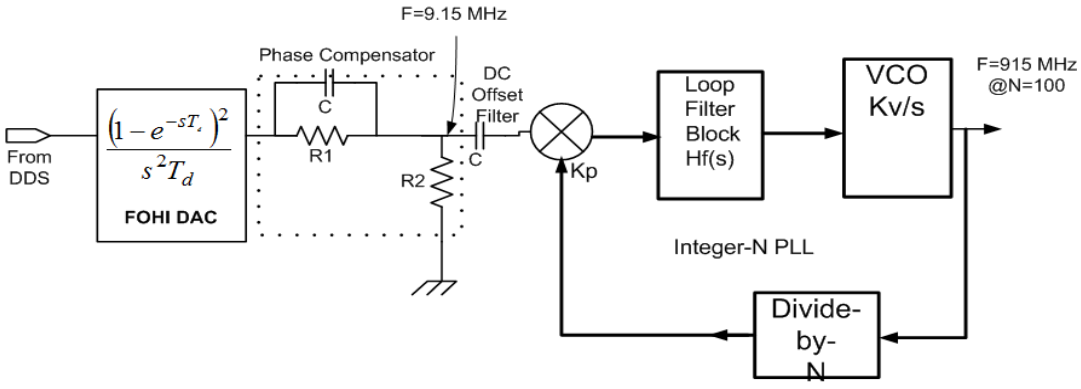


Figure 4.23 DDS+ FOHI DAC with analog Phase Compensator and PLL

The phase compensator is analog and placed after the DAC. Following [Dorf, 2005], its transfer function can be written in the form following [Dorf, 2005],

$$G(s) = \frac{(1 + \alpha\tau_{AP}s)}{(\alpha + \alpha\tau_{AP}s)} \tag{4.105}$$

In Equation (4.105), time constant (τ_{AP}) and the phase shift constant (α) of the compensating network of Figure 4.23 can be related to circuit parameters. The relationship between phase shift generated by the compensator θ and α [Dorf, 2005] is expressed as

$$sin\theta = \frac{\alpha - 1}{\alpha + 1} \tag{4.106}$$

By relating the exact phase shift generated by the FOHI DAC (from Equation (4.102)), the following relationship can be written as

$$\alpha = \frac{1 + sin\omega T_d}{1 - sin\omega T_d} \tag{4.107}$$

Equations (4.107) facilitates to compute the phase shift parameter (α) that is necessary when only the sampling time (T_d) of the FOHI DAC and the input frequency ω are known. The second parameter of the phase compensation network is its time constant τ. The formula for the time constant τ_{AP} [Dorf, 2005] is

$$\tau_{AP} = \frac{1}{\omega_m\sqrt{\alpha}} \tag{4.108}$$

In Equation (4.108) ω_m is the center frequency of DDS output. In turn, τ_{AP} is the time constant of the analog phase shifter. The maximum phase shift $\phi = \omega T_d$ to be compensated must be specified first. The phase shift generated by the FOHI DAC is written as ϕ, lagging the phase shift induced by the compensator is written as θ. Equations (4.107) and (4.108) will suffice to compute parameters of the compensating network (α and τ). the transfer function of the FOHI DAC can be written as

$$G(s) = \frac{(1 - e^{-sT_d})^2}{s^2 T_d} \tag{4.109}$$

By substituting the value of (τ) from Equation (4.108), the transfer function of phase compensation network can be expressed in terms of α and ω_m as

$$G(s) = \frac{(1 + \frac{\sqrt{\alpha}}{\omega_m} s)}{\left(\alpha + \frac{\sqrt{\alpha}}{\omega_m} s\right)} \tag{4.110}$$

The Equation (4.110) allows the computation of the transfer function ($G(s)$) in terms of parameter (α) and the center frequency ω_m. The transfer function of phase compensator (Equation (4.107)) and the transfer function of FOHI DAC (Equations (4.109) and (4.110)) are used to simulate the response of the cascade of DAC and analog compensator of Figure 4.24.

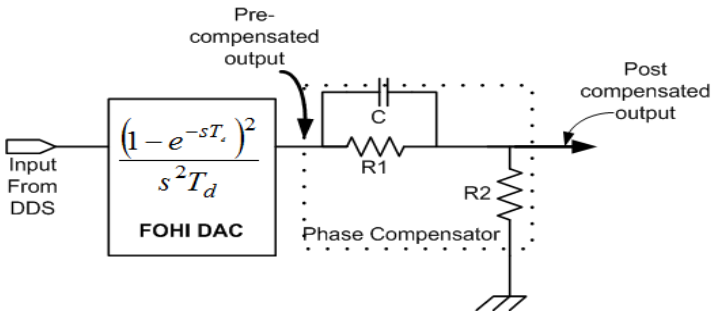


Figure 4.24 Block diagram of Cascade of DAC and Phase Compensator

The intended objective of the compensating network is demonstrated by generating two Bode phase plots, one for the FOHI DAC alone and the other for the cascade of the DAC and the compensator. The phase shift frequency response of a FOHI DAC is shown Figure 4.25. The Bode plot of the FOHI DAC with $\phi_{FOHI} = 28.7^o$ and T_d= 8.697ns is shown in Figure 4.25. The chosen value of phase shift corresponds to a phase shift of 0.5 radian when the sampling frequency is 8.697ns and input is at 9.15MHz. This is a significantly large phase shift to compensate.

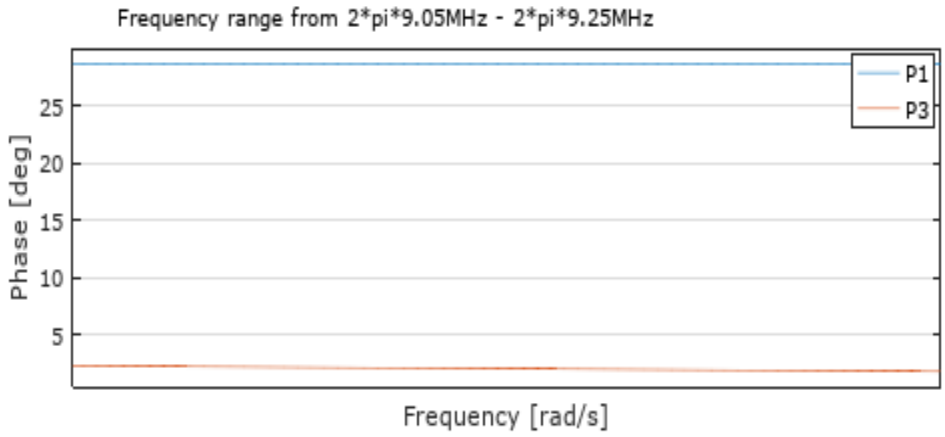


Figure 4.25 Bode plot (Phase) for the cascade of FOHI DAC and compensator ($f = 9.15$ MHz)

Figure 4.25 illustrates that the phase shift for a FOHI DAC can be as high as 28^o at a center frequency of DDS (9.15 MHz) (P1). The phase shift frequency response of the cascade of a FOHI DAC and the phase compensator is shown Figure 3.26(P3). Figure 4.25 illustrates the performance effectiveness of the phase compensator to offset the phase shift introduced by FOHI DAC alone. The blue track in Figure 4.25 is the uncompensated phase shift and the red track is Figure 4.25 is the phase shift after compensation. Figure 4.25 illustrates that the phase shift due to the FOHI-DAC has been effectively compensated from an original -28.7^o to a final 0.58^o. The designed phase compensator virtually completely offsets the phase shift induced by FOHI-DAC. The very small residual phase shift after the phase compensation (Figure 4.25) illustrates the efficacy of the discussed phase compensating network. Figure B.1 illustrates that the phase compensating network designed for 9.15 MHz is used over a frequency range of 8.5 to 10.5 MHz, the residual error after compensation shows a variation from 2^o to 3^o. The pre and post compensated phase responses of block diagram of Figure 4.24 are depicted in Table 4.4.

Table 4.4 Comparison of pre and post compensated phase shift of FOHI DAC (Input Frequency = 9.15 MHz)

Phase shift due to DAC alone (Degrees)	Compensator α	Phase shift due to DAC + compensator (Degrees)	τ of compensator(ns)
-20.00	2.0396	+0.60^o	12.18
-25.00	2.4639	+0.40^o	11.08
-28.38	2.8360	+0.50^o	10.33
-30.00	3.0000	+0.45^o	10.04
-35.00	3.6900	+0.52^o	09.05

Table 4.4 illustrates that a wide range of phase angles are readily compensated. The response of the cascade of FOHI DAC- Phase Compensator – PLL is also of interest to analyze the effect of phase shift introduced by the DAC on the performance of the PLL. The transfer function of the second-order Type I PLL used for simulation is written as

$$W(s) = \frac{N\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4.111}$$

In Equation (4.111), ζ or damping coefficient =0.22, natural frequency $\omega_n = 14x10^7$ rad/sec, and (N =100) is the divider ratio

$$W(s) = \frac{1.9x10^{18}}{s^2 + 6.16\,x10^7 s + 1.96x10^{16}} \tag{4.112}$$

The cumulative phase shift $\angle\phi_{CUMU}$ for the cascade of combination of FOHI, $(\angle\phi_{FOHI})$,Compensator $(\angle\phi_{COMP})$ and PLL $(\angle\phi_{PLL})$ in Figure 4.24 is additive and thus it can be written as

$$\angle\phi_{CUMU} = -\omega T + \left(tan^{-1}(\alpha\tau\omega) - tan^{-1}(\tau\omega)\right) + tan^{-1}\left(\frac{2\zeta\omega\omega_n}{-\omega^2 + \omega_n^2}\right) \tag{4.113}$$

The parameters α and τ are defined in Equation (4.107) and Equation (4.108) respectively. In Equation (4.113), the first term corresponds to the phase shift introduced by the FOHI DAC, the

second term represents the phase shift introduced by the compensator, and the third term (in Equation 4.113) represents the phase shift due to the second-order PLL. The corresponding cumulative magnitude (M_{CUMU}) for the cascade combination (of the DAC, the compensator, and the second-order PLL) in Figure 4.24 is written as

$$M_{CUMU} = \frac{4}{\omega^2 T_d^2} sin\left(\frac{\omega T_d}{2}\right)^2 \left\{\frac{\sqrt{1+(\alpha\tau\omega)^2}}{\sqrt{(\alpha)^2+(\alpha\tau\omega)^2}}\right\}\left\{\frac{N\omega_n^2}{\sqrt{(\omega_n^2-\omega^2)^2+4\zeta^2\omega_n^2\omega^2}}\right\} \quad (4.114)$$

Equation (4.113) and (4.114) are new contributions and have not been described in open literature. Over a range of 200 kHz in the DAC input frequency, the cumulative phase shift of FOHI DAC and PLL varies between 40^0 to 42^0. Over the same range, the phase shift induced by PLL alone is 12.3^0. If the compensator is included (Figure 4.26), the resultant phase shift is much lower than without the compensator. In Figure 4.26 the phase shift correction is around 28^o.

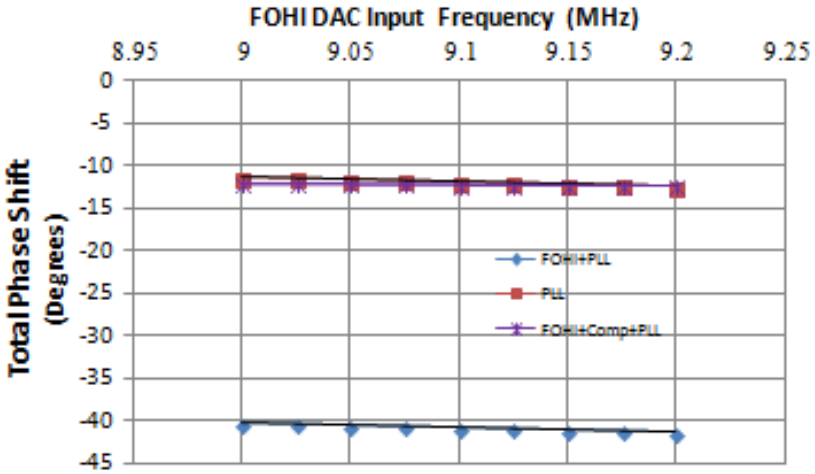


Figure 4.26 Compensation of phase shift; PLL alone, FOHI-DAC+PLL, FOHI-DAC+ Analog Phase Compensator +PLL

Figure 4.26 illustrates that phase compensation occurs over the frequency range of 9.00 MHz to 9.20 MHz. The analog compensator succeeding the FOHI DAC) almost completely offsets the phase shift introduced by FOHI resulting in an ideal input to the PLL. It must be considered whether the compensator for FOHI degrades the temporal performance of the FOHI -PLL combination. Table 4.5 illustrates the overshoot and settling time of the proposed phase compensator over a range of phase corrections. In Table 4.5, T_d is the DAC sampling time. In

Table 4.5 overshoot is defined as the percentage over the final value that the output reaches when a unit step input is applied at the input to the DAC.

Table 4.5 Performance Comparison of Partial and Full Digital Compensation in FOHI DAC and Second order PLL

T_d (μs)	Phase Shift due to DAC	Phase shift Due to DAC+PLL	Overshoot (Fully Compensated) (%)	Settling Time (Fully Compensated)
2.00	-6.588^o	-18.850	110.9	187.5
2.50	-8.230^o	-20.498	119.0	189.0
2.80	-9.223^o	-21.485	122.5	189.5
3.00	-9.882 ^{o}	-22.144	124.2	189.8
3.60	-11.86 ^{o}	-24.120	132.8	191.5
4.20	-13.83 ^{o}	-26.097	139.9	192.5
4.40	-14.49 ^{o}	-26.756	143.4	193.0
4.80	-15.80 ^{o}	-28.073	143.6	194.0

Full compensation refers to the case where the phase compensator corrects the phase shift due to both DAC and PLL. It is observed in Table 4.5 firstly that the settling time, which is a measure of how fast the DDS can switch (phase) increases by only 3.4% across the range of T_d. Secondly, the overshoot percentage rapidly increases by 35% across the range of T_d. The introduction of the phase-shift compensator to offset the phaseshift induced by the FOHI DAC and PLL results in the degradation of overshoot, as well as settling time characteristics of the cascade of the FOHI-DAC, phase compensator and PLL.The variation of overshoot of the cascade of the FOHI-DAC, compensator, and PLL with increase in the phase shift to be compensated is shown in Figure 4.27.

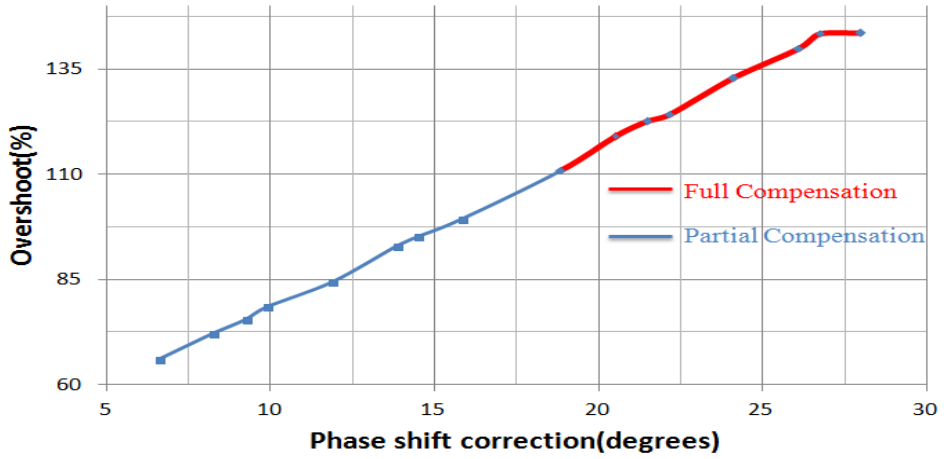


Figure 4.27 Percentage Overshoot (unit step) versus Compensator Phase Shift (in degrees)

Figure 4.27 highlights that the overshoot rises rapidly with an increasing phase shift introduced by the FOHI-DAC and the PLL. In Figure 4.27, full compensation include offsetting the phaseshifts introduced by both FOHI DAC and PLL.The term partial compensation in Figure 4.27 implies that only the phase shift introduced by FOHI-DAC alone is corrected(considered). For this simulation, the frequency of interest is the center frequency of DDS (9.15 MHz). The degradation in the settling time of the cascade of the FOHI-DAC, compensator and, PLL in lieu of the compensator is illustrated in Figure 4.28.

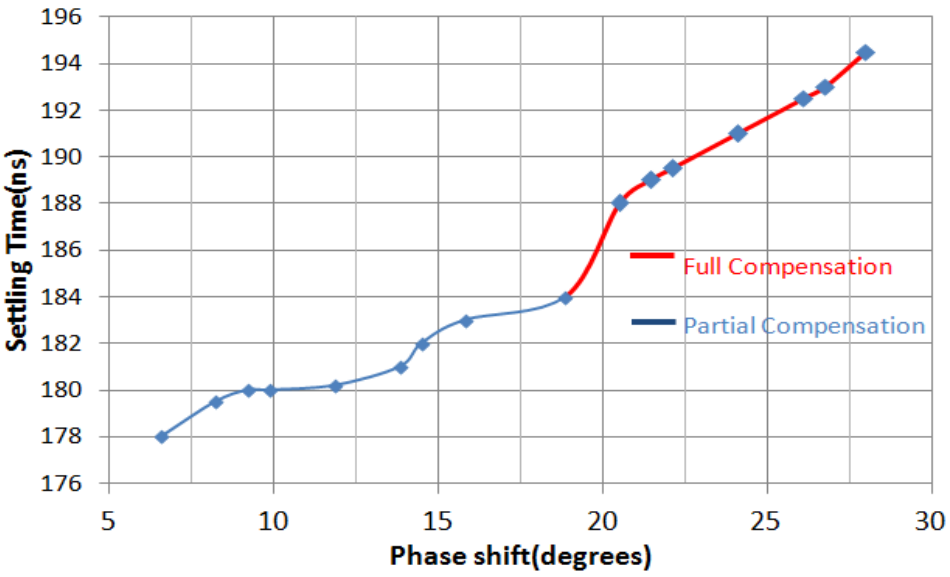


Figure 4.28 Settling Time (unit step) versus Compensator phase shift

Figure 4.28 makes it possible to conclude that the settling time is marginally impacted (from 180ns to 194ns) when the value of phase shift is increased from 10^o to 30^o. Within the range of the phase shifts considered, the settling time increases slightly faster when the phase angle to be compensated exceeds 20^o.

A relationship between the PLL phase margin and the overall phase shift ($\angle\phi_{CUMU}$) through the PLL, the FOHI-DAC, and the compensator is useful, as it allows the system designers to account for the effect of the phase margin. Such a relationship between PM and the overall phase shift expressed through Equation (4.115) appears to have not been attempted in literature.

$$\angle\phi_{CUMU} = -\omega T + \left(tan^{-1}(\alpha\tau\omega) - tan^{-1}(\tau_{AP}\omega)\right) + tan^{-1}\left(\frac{2\sqrt{\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{4\left(1-tan\left(\frac{\phi}{2}\right)\right)}}\omega\omega_n}{-\omega^2+\omega_n^2}\right) \quad (4.115)$$

4.13.3 Digital phase shift compensator added before the DAC

An alternative approach to achieve phase compensation is to add a digital phase compensator before the DAC (Figure 4.29) rather than to add an analog phase compensator after the DAC (Figure 4.23). Figure 4.29 shows a ZOH-DAC. The approach is equally applicable to FOHI-DACs.

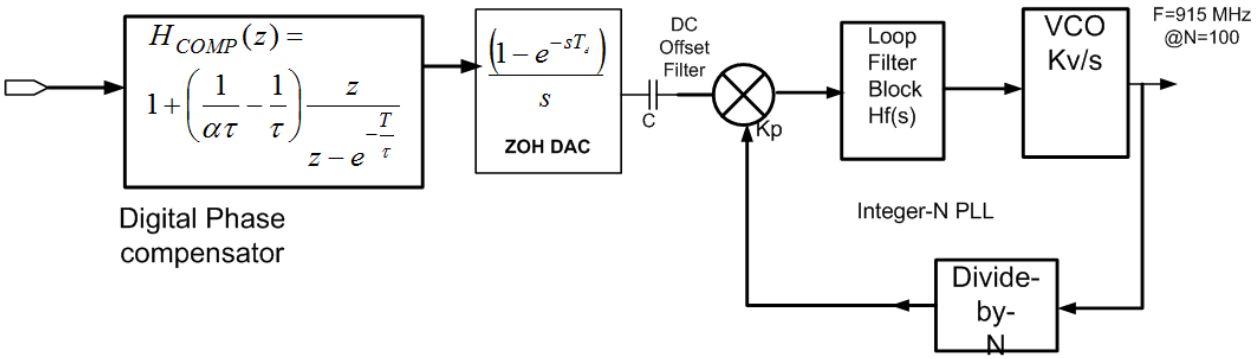


Figure 4.29 Block diagram with Digital compensator, ZOH DAC and PLL

A digital compensator has significant advantages over an analog compensator. Firstly, a digital compensator is easier to integrate on an FPGA or an integrated circuit with predominantly digital component libraries. Secondly, the parasitic capacitance of the analog compensator might make it difficult to implement at frequencies above 500 MHz, however, parasitic capacitances have no effect on the digital phase compensator. Thirdly, the phase shift parameter (α) and the phase compensation angle (φ) are susceptible to the tolerances of resistor and capacitor tolerances in an analog comparator, but not in a digital compensator. A digital phase compensator has no resistors or capacitors and therefore it is not susceptible to component tolerances. Lastly, the digital compensator can compensate over a wider range of phase shifts by just reprogramming filter coefficients.

In Figure 4.30 the red track illustrates the phase shift due to a FOHI DAC. The uncompensated phase shift at the output of the PLL with digital phase compensator ranges from -2.5^o to 2.5^o over a frequency range of 8- 10 MHz. In Figure 4.30, the blue track illustrates the phase shift with an added digital compensator followed by a FOHI-DAC. The phase shift generated by a FOHI-DAC alone is compared with the phase shift produced by a digital compensator followed by a FOHI DAC. The digital compensator imparts a phase shift which is equal and opposite to the phase shift imparted by the FOHI-DAC. The residual phase shift of -0.202^o (at 9.15 MHz input frequency) is the uncompensated phase.

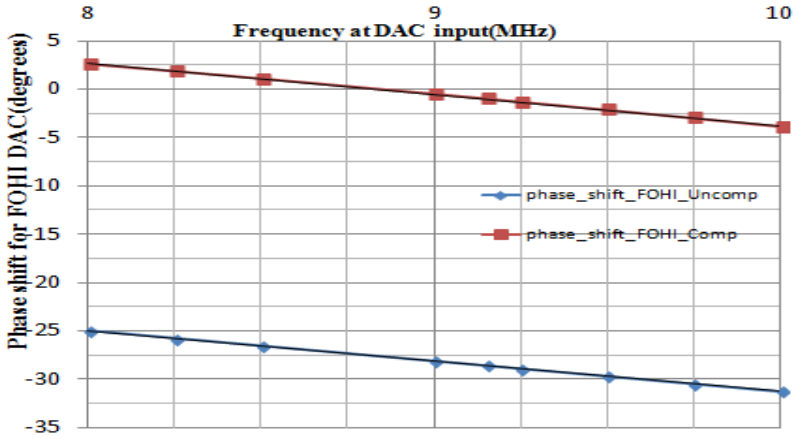
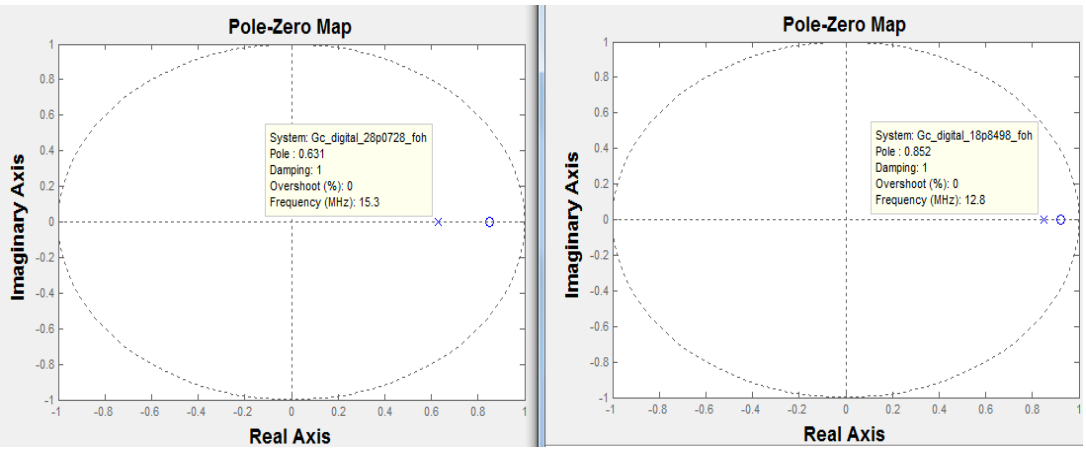


Figure 4.30 Phase shift of Digital Compensator cascaded with FOHI DAC

The digital compensator is an Infinite Impulse Response (IIR) filter with a sampling period of 8.6831ns (corresponding to a DAC phase shift of 0.5 radian) with its transfer function written as

$$G_{COMP}(z) = \frac{0.902 - 0.6033z^{-1}}{1 - 0.5054z^{-1}} \tag{4.116}$$

In Equation (4.116), z is the general complex number of the form $z = Ae^{j\phi}$. It is used in generating a z-transform. The pole-zero plots of Figure 4.31 show that the compensator is inherently stable with its pole being inside the unit circle. A comparison of Figure 4.31(a) for phase shift of 28^o and Figure 4.31(b) for phase shift of 18^o reveals that pole shifts towards the edge of the unit circle as the required phase compensation angle is lowered. As the phase compensation angle is lowered from 28^o to 18^o, the pole location for the compensator has shifted from 0.631 to 0.852.



(a) **Phase Compensation Angle=28º** **(b) Phase Compensation Angle=18º**

Figure 4.31 Pole- Zero diagram of integrated digital phase compensator

To highlight the effect of adding a digital compensator before the ZOH-DAC, Table 4.6 depicts the resulting temporal effects – the overshoot, effect on settling time, and maximum throughput. The maximum throughput is the inverse of the settling time. The digital compensator structure can be derived from the corresponding analog compensator by making use of analog to digital conversion methods in DSP albeit with a specified sampling time of 2000 ps and a FOHI DAC. In Table 4.6 MSPS refers to Mega-Samples Per Second. Settling time refers to the settling time of PLL + DAC + Compensator in nanoseconds.

Table 4.6 Effect of addition of digital compensator before FOHI DAC

Phase Shift of Compensator (degrees)	Compensator phase shift constant(α)	% Overshoot	Settling Time (ns)	Maximum Throughput(1/Ts) In MSPS
10	1.42	64.8	262	3.8
12	1.52	66	285	3.5
14.3	1.656	74.8	290	3.4
16	1.761	78.5	293	3.4
18	1.8944	79	300	3.33

From the tabulated results of Table 4.6, it is observed that the overshoot increases significantly (from 64.8 % to 79 %), and the settling time increases slightly with an increase in the required

phase compensation angle. Similar effects have been noticed for the analog compensators also. Since the minimum time required to perform a phase increment at the input of the compensator (DDS output) is determined by the settling time of the combination, it is better to have to have a compensator for smaller phase shifts than larger phase shifts.

An additional simulation has been performed to demonstrate the utility of a multi-stage digital compensator that can be used for phase compensation over a much wider phase shift (even greater than 90 degrees). For this purpose, a PLL is chosen, which introduces a phase shift of around -72^0. The multi-stage compensator structure is a cascade of three compensators, as per the general IIR model of Equation (4.18).

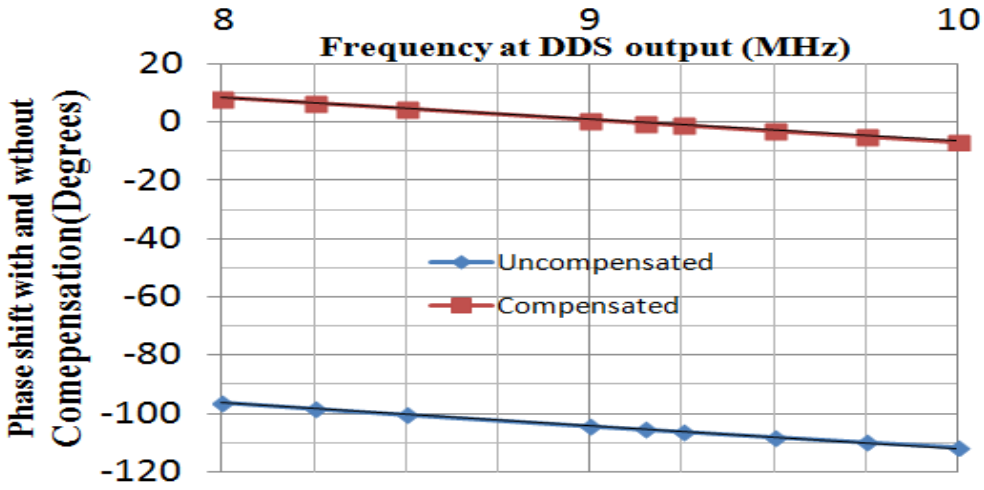


Figure 4.32 Phase Compensation with Multi Stage Compensators

The frequency response performance of the three-stage phase compensator is shown in Figure 4.32. The three-stage phase compensator has been designed for the center frequency of 9.15 MHz for a combined phase shift of -105^o through the PLL and FOHI-DAC. Even with high phase shift correction requirements, the residual phase shift of below 0.25^o is achievable. The time-domain performance parameters of the three-stage phase compensator are shown in Table 4.7. In Table 4.7 a total phase shift of 105 degrees is compensated by three-stage fully digital IIR phase compensator.

Table 4.7 Overshoot, settling time, SFDR at compensation angle of 105 degrees using three-stage cascade compensation ($s_e = 32$)

Uncompensated phase shift of PLL+FOHI	105.4°
Overshoot (%) (with full compensation)	186%
Settling time (with full compensation)	142 ns
Overshoot (%) (without compensation)	0% (due to high ζ of PLL)
Settling time (without compensation)	140 ns
SFDR ($s_e = 8$) (DDS output) (dB)	92
SFDR($s_e = 8$)(uncompensated PLL output) (dB)	19
SFDR (s_e=8) (PLL output with full compensation) (dB)	19

The conclusions drawn from the results of Table 4.7 are presented in this paragraph. Firstly, there is a small difference in the settling time with and without compensator (142 ns versus 140 ns). There is a significant difference in overshoot with and without a phase compensator (overshoot of 186% versus 0 %).

4.13.4 Simulation of Composite configuration of DDS, Phase Compensator, DAC and PLL

The analytical formulations and simulations on DDS have been performed keeping in view of the wider context of the output of the DDS that drives the PLL. This section presents the simulation results derived through the configuration, which is an aggregation of DDS, FOHI DAC, phase compensator and PLL. It is pertinent to emphasize that the PLL model is represented through a second-order transfer function.

Figure 4.33 depicts the functional block diagram of the composite assembly of DDS, FOHI DAC, phase compensator and PLL. The cubic polynomial-based DDS is implemented through Sysgen™ and forms the first block. The output of this DDS forms the input to the digital phase compensator.

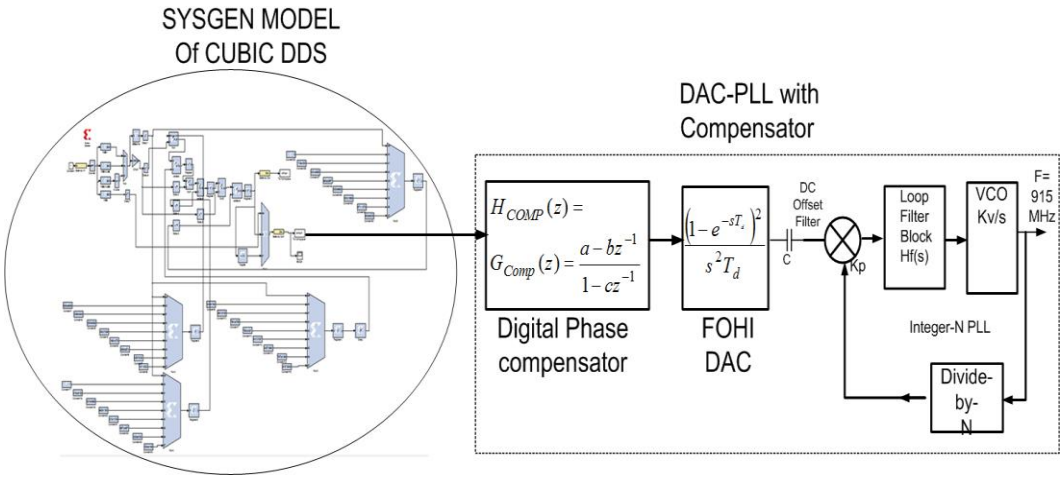


Figure 4.33 Block diagram of the Cubic Polynomial DDS, Digital Compensator, FOHI DAC and second-order PLL

The mathematical model of phase compensator-DAC-PLL was derived by cascading the z- domain transfer functions of each of the constituents. The Sysgen™ models of DDS discussed in (chapter 6) are used to generate the output of the cubic-polynomial DDS for $s_e = 8, 16$ and 32, respectively. Figure 4.34 illustrates the effects of phase compensation for an uncompensated phase shift between 12° and 22°.

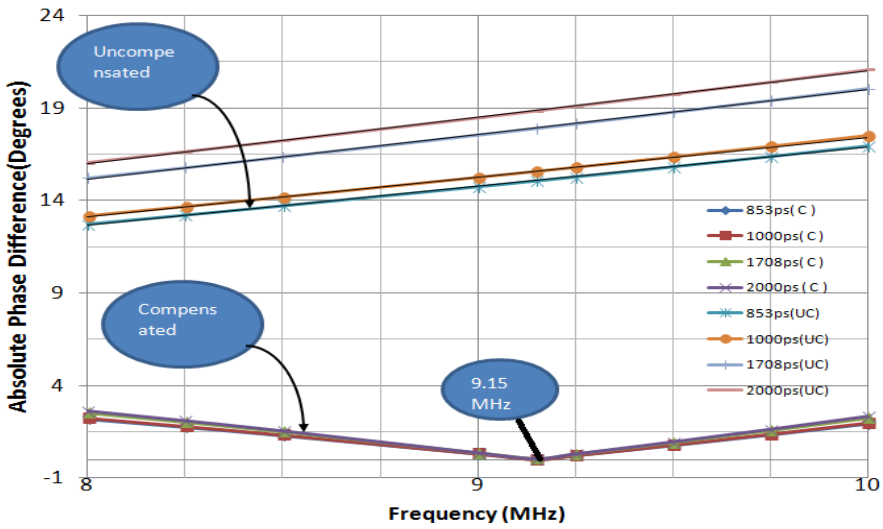


Figure 4.34 The phase difference between DDS output and PLL output with and without compensation

Figure 4.34 shows the absolute difference between phase at the outputs of cubic-polynomial DDS and the PLL with and without the phase compensator. In Figure 4.34, a total of 8 tracks are illustrated: 4 tracks with compensation (titled C Tracks) and 4 tracks without compensation (titled UC Tracks). The compensator is designed to correct the phase shift introduced by both the DAC and the PLL at 9.15 MHz. The phase shift induced by the FOHI-DAC must be corrected in addition to the phase shift due to the PLL of 12.36^{o}. The phase shift introduced by the FOHI-DAC is a linear function of its sampling frequency, the efficacy of the compensation is traced over the range of sampling rates of FOHI-DAC (from 853 ps to 2000 ps). It is observed with the phase compensator that the residual phase shift after the compensation is only 0.3^{o} over a frequency range spanning from 8MHz to 10MHz. The phase shift reduces for lower sampling times (higher sampling rates) with compensator. The term *uncompensated* in Figure 4.34 refers to the phase shift of the cascade of DDS-FOHIDAC-PLL. The term *compensated* in Figure 4.34 refers to the phase shift of the cascade of DDS-COMPENSATOR-FOHIDAC-PLL, and this refers to the case of phase shift compensated.

4.13.5 Influence of the phase compensator on SFDR -Compensator-DAC-PLL

The study on variations in the output parameters of DDS, such as SFDR caused by the addition of the compensator to the cascade of FOHI DAC and the PLL is of interest. [De Caro and Strollo, 2005] has shown that the number of segments of the DDS determines the achievable SFDR of the DDS. It will be of importance to analyze whether the number of segments of the DDS has any effect on the achievable SFDR for a cascade of the DDS-PLL with and without phase compensator. To assess the effect of the compensator on the SFDR when the compensator-DAC-PLL cascade combination is driven by an optimal cubic polynomial-based DDS, the coefficients of the optimal DDS are generated in accordance with the mathematical models of [De Caro and Strollo, 2005]. The SFDR at the output of the PLL is computed when the number of segments of the DDS is varied. The greater the number of segments, the better the SFDR is in accordance with [DeCaro and Strollo, 2005]. The reason to consider the harmonics $(4s_e + 1)$ and $(4s_e - 1)$ (where s_e is the number of segments) is that by a suitable choice of coefficients, other lower odd harmonics have

been eliminated[De Caro and Strollo, 2005] through optimization. Even harmonic components are not present since the output of cubic DDS is an odd function.

One approach to analyze the effects of the compensator on DAC and PLL is to excite the cascade using optimal Fourier coefficients, which are generated through the [DeCaro and Strollo, 2005] model. Such an analysis through simulation seems to have not been discussed in the open literature. Such an analysis is based on the research reported in [De Caro and Strollo, 2005] to determine analytical expressions for the Fourier coefficients when the harmonics from 3rd order to $(4s_e - 3)^{th}$ order are forced to zero, and the SFDR at the output of DDS is maximized. According to [De Caro and Strollo, 2005], the expression for the fundamental component of the DDS output in terms of the number of segments for the cubic polynomial interpolation can be written as

$$b_1 = \frac{4g(1)}{\pi} - \frac{8h(1)}{\pi^2} - \frac{32l(1)}{\pi^3} + \frac{192m(1)}{\pi^4} \tag{4.117}$$

b_1 is a Fundamental Fourier component and function of s_e(number of segments)

The coefficients of RHS of Equation (4.117) are as follows:

$$g(1) = -B\frac{\pi^2(1 + 40\, s_e^2)}{8s_e^2(5 + 768\, s_e^2 + 5120\, s_e^4)} \tag{4.118}$$

$$h(1) = -B\frac{\pi^2(11 + 240s_e^2 - 2176s_e^4)}{64\, s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{4.119}$$

$$l(1) = -B\frac{\pi^3(-5 + 80s_e^2 + 4224\, s_e^4)}{128s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{4.120}$$

$$m(1) = -B\frac{\pi^4(3 - 200s_e^2 - 128s_e^4 + 40960\, s_e^6)}{1536s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{4.121}$$

In Equations (4.118) to (4.121), B is the Amplitude of the resultant output sinusoid, s_e is the number of segments in cubic polynomial DDS. The magnitudes of the next higher harmonics $(4s_e + 1, 4s_e - 1)$ that are present at the output of the DDS can be easily determined using the expressions originally derived by [De-Caro and Strollo, 2005]. When the coefficients $g(1), h(1), m(1)\ and\ m(1)$ are determined for the fundamental, they can also be used to compute the magnitude of the Fourier coefficients for the $(4s_e + 1)^{th}$ and $(4s_e - 1)^{th}$ harmonic.

The Fourier coefficient for the $(4s_e + 1)th$ harmonic is expressed as

$$b_{4s_e+1} = \frac{4}{(4s_e + 1)}g(1) - \frac{8}{(4s_e + 1)^2}h(1) - \frac{32}{(4s_e + 1)^3}l(1) + \frac{192}{(4s_e + 1)^4}m(1) \tag{4.122}$$

The Fourier coefficient for the $(4s_e - 1)th$ harmonic is expressed as

$$b_{4s_e-1} = \frac{4}{(4s_e-1)}g(1) + \frac{8}{(4s_e-1)^2}h(1) - \frac{32}{(4s_e-1)^3}l(1) - \frac{192}{(4s_e-1)^4}m(1) \quad (4.123)$$

In Equation (4.123), $b_{4s_e+1}$is the Fourier coefficient for the $(4s_e + 1)^{th}$ harmonic, and b_{4s_e-1} is the Fourier coefficient for the $(4s_e - 1)^{th}$ harmonic.

Combining the 3 harmonics in Equations (4.117), (4.122) and (4.123), the final output for the optimal cubic polynomial based DDS is written in terms of its harmonic components as

$$OUT_{DDS} = b_1 sin\left(\frac{n\pi}{2}x\right) + b_{4s+1}sin\left(\frac{(4s+1)\pi}{2}x\right) + b_{4s-1}sin\left(\frac{(4s-1)\pi}{2}x\right) \quad (4.124)$$

In Equation (4.124), OUT_{DDS} is the output of the DDS; x is the phase argument to the DDS.

Once the output of the cascade combination is determined for the harmonic excitation, the SFDR can be computed in accordance with

$$SFDR = -10log_{10}\left(\frac{\max(b_{4s_e+1}, b_{4s_e-1}}{b_1}\right) \quad (4.125)$$

In Equation (4.125), b_1 is the amplitude of the fundamental component at the output of the DDS, b_{4s_e+1} is the amplitude of the $(4s_e + 1)^{th}$ harmonic, and b_{4s_e-1} is the amplitude of the $(4s_e - 1)^{th}$ harmonic. The SFDR at the output of the DDS is a logarithmic measure of the ratio of the magnitudes of the fundamental and the maximum harmonic of interest. The SFDR is measured both at the input to the compensator (output of the DDS) as well as at the output of the PLL. Table 4.8 depicts the effects of propagation of harmonics through the cascade of the combination comprising the compensator, DAC and PLL.

Table 4.8 Variation of harmonic coefficients of DDS, PLL and Cascade with s_e

S	b1			Abs(b($4s_e$+1)) x 10^{-10}			Abs(b($4s_e$-1)) x10^{-10}		
	DDS	PLL without Compensator	PLL with Compensator	DDS	PLL without Compensator	PLL with Compensator	DDS	PLL without Compensator	PLL with Compensator
8	1	0.387	0.505	6.16460	4.89000	0.3240	5.5000	2.130000	0.304000
16	1	0.387	0.505	0.36735	0.20900	0.2090	0.3310	0.065500	0.067400
32	1	0.387	0.505	0.02400	0.00278	0.0028	0.0212	0.000795	0.000793

The variation of SFDR is illustrated in Table 4.9.

Table 4.9 Variation of SFDR at the outputs of DDS and PLL with S

s_e	SFDR (dB)		
	DDS	PLL without Compensator	PLL with Compensator
8	92.00	88.00	101.00
16	104.34	102.92	103.79
32	116.50	121.43	122.50

In Table 4.9, the SFDR is computed using the formulation of [De Caro and Strollo, 2005]. It is noted from the results of Table 4.9 that the compensator also affects the SFDR at the output. The $b(4s_e + 1)^{\text{th}}$ and $b(4s_e - 1)^{\text{th}}$ coefficients are reduced in the presence of the compensator.

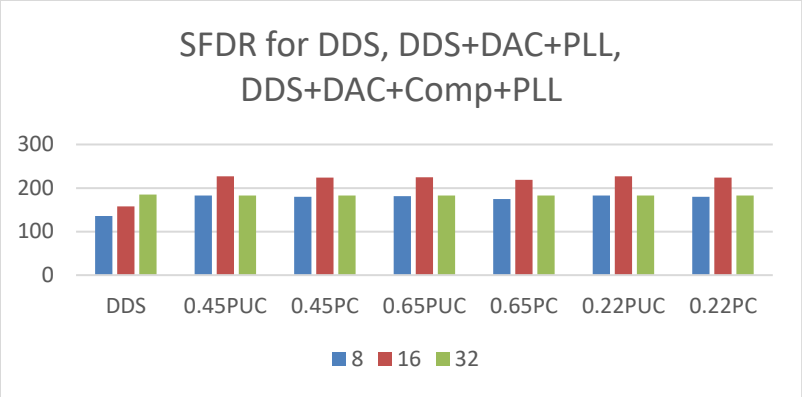


Figure 4.35 SFDR for DDS, DDS-PLL with and without compensation

The simulation results shown in Figures 4.35 on the model of integrating a cubic polynomial DDS($s_e = 8$) with the coefficients of [De-Caro and Strollo, 2005] , a digital phase compensator, a FOHI-DAC and a second-order PLL are not available in open literature. Appendix B provides two additional SFDR plots at different levels of damping coefficient. Figure 4.37 illustrates that in order to improve SFDR(at DDS-PLL output), a higher number of DDS segments must be used and the DDS output must be optimised so that the PLL filters the unwanted harmonics further. Consequently, less harmonics are present at the PLL output when compared to the DDS output. The uncompensated SFDR_UC is the SFDR at the output of PLL when the compensator is absent. It is included as a reference. At higher numbers of segments($s_e = 16,32$), the SFDR at the PLL output for the uncompensated system approaches the SFDR for the corresponding compensated system. A decision to have a phase compensator or not is influenced by the SFDR requirement. A new analytical expression relating the transfer function of the digital compensator with the PLL parameters has been derived in Appendix B. Such an expression is not derived in the open literature and is useful for future designers.

$$H(z) = \frac{z^{-1}\left(\omega_m - 2f_s\sqrt{\alpha}\right) + \left(\omega_m + 2f_s\sqrt{\alpha}\right)}{z^{-1}\left(\alpha\omega_m - 2f_s\sqrt{\alpha}\right) + \left(\alpha\omega_m + 2f_s\sqrt{\alpha}\right)} \tag{4.126}$$

In Equation(4.126), f_s is the the sampling frequency. Constants α, ω_m are defined in Equation (4.107) and (4.108) respectively. In turn, z is the Z-transform variable.

4.14 Conclusion

This chapter explores the PLL stability of a second-order PLL, the speed of response (lock time), the phase noise at PLL output, the phase jitter as a function of PLL parameters, such as the damping coefficient and the phase margin. This chapter has presented an analysis of phase noise due to various noise sources of a second-order PLL. A relationship between the lock time and the phase margin has also been arrived at. An additional perturbation analysis has been performed for the phase margin as the settling time is varied. A significant contribution of this chapter is the closed-form analytical relationship between phase noise and K_V, N, and settling time of a second-order Type I PLL. A significant contribution is the equation relating the phase noise to the lock time of a second-order PLL. The cumulative phase noise of DAC- PLL which is expressed as a product of transfer functions of reference noise sources and the summation of noise PSD for a plurality of noise sources of PLL has also been analyzed.

This chapter has also placed emphasis on the lock time, its relationship with the phase margin and the damping coefficient as well as the relationship between the jitter variance and other PLL parameters such as the phase margin and the damping coefficient. The relationship between the lock time and the damping coefficient has been explored in closed-form as a new expression derived for the derivative of the lock time with respect to the damping coefficient. Lock time is characterized for a range of phase margins for different values of natural frequencies. It is concluded that, for lower lock time higher natural frequency, higher VCO sensitivity and higher phase margin values are necessary. A significant contribution is the equation relating the lock time to the loop filter time constant of a second-order PLL, which has been derived for the first time.

This chapter provides a new relationship between the jitter variance and the phase margin of a second order type II PLL. The analytical form for jitter variance proposed by [Lee,2002] has been extended substantially as the relationship between jitter and PM has been analytically expressed and plotted. Jitter variance has been plotted for a range of natural frequencies (therefore loop BW) of a second-order PLL. It provides a closed-form expression, which relates the angle between the complex poles of a of second-order PLL to its phase margin.

Finally, two approaches for phase shift correction – one analog and the other digital have been explored in detail. Multiple simulations are performed to demonstrate the efficacy of the proposed phase shift compensation scheme. The effect of phase compensators on the overall overshoot and the settling time of PLL are analyzed. This chapter has also presented the simulation results on the SFDR and the overshoot of cubic DDS with and without phase shift compensation.

Chapter 5: The roots of a third-order PLL and their relationship to PLL parameters

This chapter is aimed to present analytical results, design procedures and simulations for third order PLLs. In many perspectives, the Chapter 5 is a continuation of Chapter 4. The focus in Chapter 4 is on second-order PLLs – both Type I and Type II. The performance criteria considered in Chapter 4 are phase margin (relative stability), jitter (in the time domain), phase noise (in the frequency domain). A second-order PLL has only two poles and the pole locations affect phase noise, phase margin and jitter. A third-order PLL has a characteristic equation of the third order. The CE of a third-order PLL will have three roots which correspond to three poles. Depending on the locations of these three poles, the third-order PLL will produce different levels of phase margin, phase noise and jitter. The third-order PLL has a more complex relationship between pole locations and performance parameters than a second-order PLL. The additional degree of freedom implies greater possibilities of instability and greater opportunities to minimize jitter and improve phase margin. Third-order PLLs are the mainstay in main cognitive radio applications. They have been analyzed by ([He, 2007], [Daniels, 2008]) because of their practical significance. This chapter presents analytical formulations to get additional insights into the relationship of location of poles to phase margin, stability criterion and jitter.

Section 5.1 introduces the block diagram of a third-order PLL and identifies its subblocks. It includes a Table of terms and symbols used ion this chapter. Section 5.2 reviews some important papers on third-order polynomial equations. Section 5.3 provides literature provides a review of stability, jitter and phase noise of a third order PLL. Section 5.4 derives a transfer function of a third-order PLL and introduces its CE. Section 5.5 describes the parameters of a third-order PLL. Section 5.6 applies a geometric technique called Vieta's Circle for the location of the three real roots of a third-order PLL. Section 5.7 derives a closed form equation relating the phase margin of a third-order PLL and Vieta's angle for the case where the third-order PLL 3 real and unequal poles. Section 5.8 analyzes the case of a third-order PLL with three real and unequal roots. Section 5.9 derives a new expression for the Spur gain of a third-order PLL with three real and unequal

poles. Section 5.10 analyzes the case of the third-order PLL with one real and two complex poles. Section 5.11 derives new expression for the ratio of noise power to carrier power of a third-order PLL. Section 5.12 derives new results and applies a criterion called ITAE to a third-order PLL. A new expression for the phase margin of a third-order PLL is derived in Section 5.12. Section 5.13 is the conclusion section.

5.1 Block diagram and Parameters of a Third-order PLL

The main blocks of a third order PLL are Phase-Frequency Detector (PFD), second order loop filter, a Voltage Controlled Oscillator (VCO) and a feedback frequency divider. Figure 5.1 illustrates the block diagram for a third-order PLL. The PFD senses the difference between two phases at its input and produces an output signal which is function of the phase difference. The output of the PFD is the primary inputs to the loop filter. The output of the loop filter constitutes an input to the VCO. The VCO generates a specific output frequency which is dependent on the control voltage at the VCO.

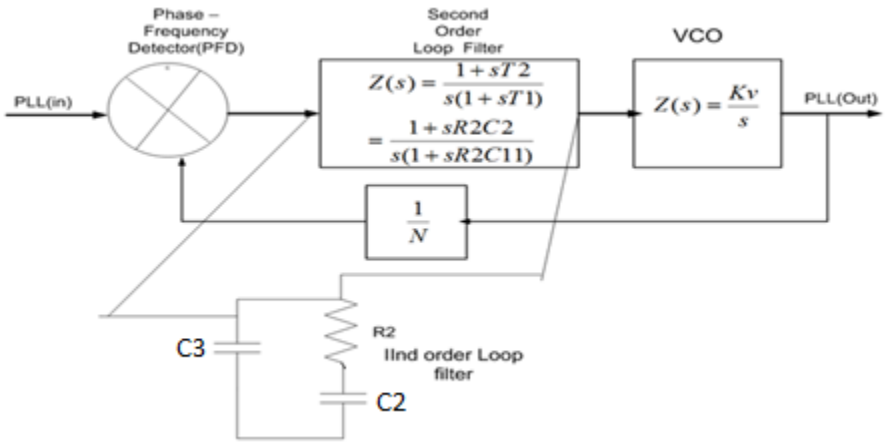


Figure 5.1 Block Diagram of Third –Order PLL with second order passive loop filter

The feedback frequency counter can be either an integer divider such as $\boldsymbol{N}$(**an integer**) or a fractional divider (to divide the output frequency of the PLL with fractional form such as $\boldsymbol{N\frac{x}{y}}$, where $\boldsymbol{N, x, y}$ are integers). The output frequency of VCO is divided by either an integer plus a

fractional number and fed back to the PFD. The loop filter of the third-order PLL comprises a series RC circuit in parallel in a second capacitor. This configuration smoothens the control voltage applied to the VCO as compared to a second-order PLL. The shape of the control voltage applied to the VCO is ramp rather than a step. In practice PLLs of third-order can be built with charge pumps in the PFD [He, 2007] or analog multiplier-based PFDs [Gray, 2002]. A charge pump comprises two current sources arranged in an UP-DOWN configuration, only one of which drives current at a time. A second important concept is that of the charge-pump PFD. It is a device comprising of a three-state phase detector, an 'UP' state, a 'DOWN' state and a neutral state – neither 'UP' or 'DOWN', two switches, and two current sources. There is a first current source termed as the 'UP' source and a first switch. In the 'UP' state a first switch is turned on, the second switch is off and the 'UP' current source drives current into the loop filter. In the 'DOWN state, a second switch is turned on, the first switch is turned off and a DOWN current source allows current to be driven from the input port of a loop filter to ground. Since the loop filter contains a minimum of one or two capacitors (one capacitor for second order PLL and two capacitors for third order PLL), the charge pumps control the input voltage to the loop filter. The loop filter is thus driven in one direction in the 'UP' state of the PFD and in a different direction when driven by the DOWN state of the PFD. A PLL with a charge pump type phase detector is known as a charge pump PLL (CP-PLL). A CP-PLL can be of any order depending on the transfer function of the loop filter. Table 5.1 describes all the terms and abbreviations used in this chapter including the associated symbols and units. Parameters $K_V, K_\phi, N, \zeta,\ \omega_n$ are already defined in Chapter 4 for a second-order PLL. They apply also to a third-order PLL.

Table 5.1 List of Symbols for Analysis of PLL

Parameter	Name and short definition	Unit and symbol
Loop gain	$K = \frac{K_v K_\phi}{N}$ a parameter used to simplify many PLL performance criterion such as spur gain	MHz/v-mA
Spur gain	Open loop transfer function of a PLL at its comparison frequency – which is the frequency at the output of the feedback divider and controls the level of leakage spurs	$Gspur$, dB
Absolute Jitter	A sequence of time intervals which measures the actual zeros crossings from the ideal zero crossing for any oscillator multiplied by the nominal oscillator frequency	σ_{A}^2, Radians
Period Jitter	A sequence of time intervals which measures the deviation of periods from the nominal period. It is a first order difference of absolute jitter	$\sigma_{\Delta \mathrm{T}}$, sec^2
Jitter variance	Variance of jitter at a time interval of ΔT, its and integral of the product of power spectral density with sinc squared function	$\sigma_{\Delta \mathrm{T}}^2$, sec^2
ω_c	Loop Band-width (Loop BW) is the frequency where the gain of loop filter drops to 0 dB	ω_c, radians/second
Normalized Lock time	Lock time divided by standard lock time. A function of damping coefficient and loop bandwidth	Dimensionless quantity
CE	Characteristic Equation (CE), The equation formed by equating the denominator of a transfer function to zero.	CE
Polynomial roots	Roots of a cubic polynomial equation	NA

5.2 A review of the existing literature for Cubic equation solutions

A cubic equation is generally of the form

$$as^3 + bs^2 + cs + d = 0 \tag{5.1}$$

In Equation (5.1), the coefficients $a, b, c\ and\ d$ are termed as the coefficients of the cubic equation or polynomial. The Characteristic Equation (CE) of the denominator of the transfer function of a third-order PLL is a cubic equation. Solution of this CE determines the poles of the PLL. The roots of the characteristic equation determine whether the given third-order PLL is over-damped or under-damped, whether it is stable or not- either through Routh's stability criterion or Nyquist [Dorf, 2005]. The roots of the CE also determine performance parameters of a third-order PLL such as its settling time, Noise Transfer Function (NTF), phase noise or jitter variance.

The solution of a generalized cubic equation was studied by Cardan, [Bernard and Child, 2011]. [Nickalls, 1993] makes a fundamental contribution to applied mathematics by introducing a new set of parameters different from the G and H parameters defined by Cardan's. The solution proposed by Nickalls for a cubic equation broadly results in three categories of nature of roots; all three roots are real and unequal; all three roots are real and equal; of the three roots one root is real and the other two are complex conjugate roots. [Nickalls, 1993] relates the discriminant of Cardan with the new parameters (y_N, δ, h and a) for a generalized cubic equation.

5.3 Review of Literature on Stability, Jitter and Phase noise of Third-Order PLL

This section presents a succinct review of literature related to stability, jitter and phase noise of a PLL. [Gardner,1980] provided the two stability formulae for third-order PLLs. Gardner's stability criterion can be used to check whether a PLL will be stable for a given combination or R1, C1 and C2 in Figure 5.1.

[De-Smedt and Geilen, 1998] have proposed a simulation approach to evaluate the phase noise spectrum of a PLL based on a behavioral model of the VCO. Their approach has been compared to actual SPICE models of the PLL and the claim of the accuracy is up to 0.25dBc/Hz.

[Hedayat, 1999] proposed one of the early event driven models of third-order charge pump PLL with a non-uniform sample time. [Lam and Razavi, 2000] have proposed a formula for the ratio of noise power to carrier power for a linear third-order PLL. Their formula utilizes the capacitance values of the loop filter, sensitivity of VCO, offset frequency in radians, resistance and - kT(Boltzmann's constant (k) times absolute temperature (T).

[Mansuri and Yang, 2002] have derived a closed-from expression for jitter at the output of a third-order PLL based on buffer noise and VCO noise sources. Their expression for the output jitter variance is used in this chapter. They define a "figure of merit" which is related to the center frequency of the VCO and its Single Side Band Phase Noise (SSBPN).

[Abramowitz, 2002] has addressed an application of Lyapunov's stability and Sylvester's theorem to third-order PLLs. The stability measures addressed in this chapter are related to linear models. Abramowitz proves that the form of the Lyapunov function is amenable for obtaining stability conditions. His results provide stability conditions for a PLL with a sinusoidal non-linearity.

[Musa, 2002] and [Rategh, 2000] have provided a closed-form expression for ratio of the phase noise power to carrier power an extension of this has been addressed in this chapter.

[Carlosena, 2003] proposes the introduction of a low-pass filter in a PLL termed as a Przedpelski filter and he proposes the inclusions of an additional frequency feedback loop for accelerated locking. His paper also proposes a novel type of chirp tracking PLL featured with three feedback paths which can be used to track an input signal of linearly varying frequency.

[Herzel and Piz, 2003] have defined a system level simulation model for a third-order PLL using the phase noise of VCO as an Ornstein-Uhlenbeck type of process. [Herzel, 2003] proposes a novel and unique simulation model for the jitter at the output of a second-order Type II PLL. His model considers white Gaussian model for the reference oscillator and white Gaussian noise for the VCO.

[Heydari, 2004] provides a detailed analysis of PLL jitter due to power ground and substrate noise. He proposes a stochastic model for the substrate noise.

[He, 2007] provides a linear model for a third-order PLL. Her thesis describes the detailed design of VCO and loop filter of a third-order PLL. [He, 2007] has provided several new theoretical and practical contributions to the theory of third-order PLLs. The normalized lock time versus phase margin characterization provided *in* the thesis exhibits a feature of minima of normalized lock time for certain phase margin values. The relative frequency error is defined as the ratio of the frequency deviation (difference between actual PLL output frequency and ideal frequency as commanded by input) from a final PLL frequency divided by the final frequency (the frequency that will be finally attained after an input frequency step has been applied to the PLL).

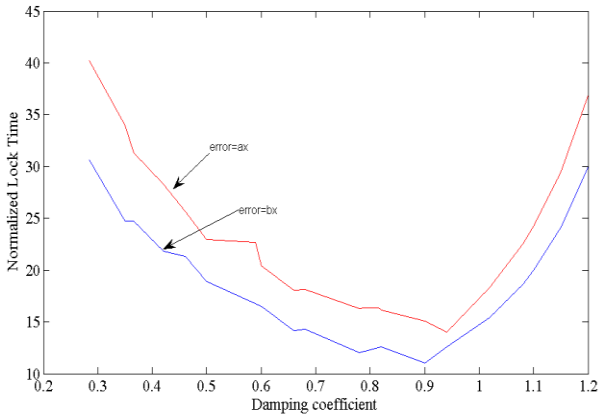


Figure 5.2 Lock Time versus Damping coefficient for a relative frequency Error (ax = 10^{-5}) and relative frequency Error (bx= 10^{-4}) following [He, 2005]

Figure 5.2 is generated for a relative frequency error of 10 $^{-4}$ and 10^{-5}. The normalized lock time drops to a minimum as demonstrated in Figure 5.2 and in [He,2007].

[Thacker et. al., 2009] describe multiple state feedback mechanisms in PLLs used in synchronization of inverter in power systems. Their schemes incorporate feedback of cosine of phase error times the sine of the phase error to a modified phase frequency detector.

[Abdelfattah-et al., 2013] have performed studies of loop filter design and selection in PLL. Their approach leads to loop filter design of various orders for phase noise and stability of PLL. The proposed approach by the above authors yields filter designs for better stability for different orders of PLL.

[Hangmann, 2013] describes a third-order event driven model for a digital PLL. His model expresses extended event driven behavioral model for higher order PLLs which have comparable accuracy to a SPICE simulation. The advantage of this model is the faster time of simulations without loss of accuracy as compared to a SPICE model.

[Abidi, 2003] is a classic paper on phase noise and jitter in ring oscillators. His paper establishes the relationship between period jitter and phase noise in a ring oscillator, through the integral relationship which relates the PSD of the phase noise to the variance of period jitter.

5.4 Transfer function of a third-order PLL in terms of PLL parameters

Analyzing external parameters of a third-order PLL through poles relates the geometry of the pole locations to the parameters such as PM and jitter to the pole values. This provides great insight into the third-order system.

The following analysis explores the nature of the Characteristic Equation (CE) of a third-order PLL. The roots of a third-order PLL, can be real or complex conjugate and three conditions can occur. Each condition refers to the coefficients of the CE of a third-order PLL. The first condition yields three real and equal roots. The second condition yields three real and unequal roots. The third condition yields a pair of complex roots and one real root. The specific condition that emerges can be identified without computing the values of the roots by checking the value of the discriminant which is a function of the coefficients of the CE. The CE is formed by considering the denominator of the transfer function of the PLL. The transfer function of a linear third-order PLL of Type I is derived from its model shown in Figure 5.1.

A PLL with a charge pump type phase detector is known as a Charge Pump PLL (CP-PLL). A CP-PLL can incorporate a loop filter of any order. The order of the loop filter only affects the transfer function of loop filter. In this chapter a linear model of the charge pump is used to facilitate simpler derivation. The nonlinear effects of a CP-PLL are not considered in this chapter.

The two distinct time constants for the third-order PLL (Figure 5.1) and the sum of the capacitances can be written in the form of the equations as explained in this section. The series(first) time constant of series RC is written as

$$\tau_1 = R2C2 \tag{5.1}$$

The parallel(second) time constant of parallel RC filter is written as

$$\tau_2 = R2(C2 \parallel C3) \tag{5.2}$$

Since usually the series capacitance of the loop filter exceeds the shunt capacitance or $C2 >> C3$

$\tau_2 \approx R2C3$. In the general case one can write

$$\tau_2 = R2\frac{C2C3}{(C2 + C3)} \tag{5.3}$$

The sum of the series and capacitances occurs frequently in transfer functions. It is written as

$$A0 = C2 + C3 \tag{5.4}$$

The notation $A0$ was first expressed by [Banerjee, 2006]. $A0$ is the sum of the series and parallel capacitances in the loop-filter. The transfer functions and feedback path follow the convention

followed by [Banerjee, 2006] and [He, 2007]. The transfer function ($G(s)$) of the forward path for the third-order PLL (Figure 5.1) can be written as

$$G(s) = \frac{K_V K_\emptyset}{s} \frac{(1 + sR2C2)}{s\big((C2 + C3) + C2C3R2s\big)} = \frac{K_V K_\emptyset}{s} \frac{(1 + s\tau_1)}{s\big((A0) + A1s\big)} \tag{5.5}$$

In Equation (5.5) parameters $K_V, K_\emptyset$ have been defined in chapter 4. Constant $A1 = C2C3R2$ in Equation (5.5). The transfer function $H(s)$ of the feedback path can be written as

$$H(s) = \frac{1}{N} \tag{5.6}$$

The transfer function of the third-order PLL can be written as

$$TF(s) = \frac{G(s)}{1 + G(s)H(s)} \tag{5.7}$$

Upon substituting the values of $G(s)$ and $H(s)$ from Equations (5.5) and (5.6) in Equation (5.7), the transfer function of a third-order PLL is written as

$$TF(s) = \frac{\left(\frac{K}{N}\right)N(1+s\tau_1)}{(s^3A1+s^2A0+s\frac{K}{N}\tau_1+\frac{K}{N})} = \frac{\left(\frac{K}{N}\right)N(1+s\tau_1)}{A1(s^3+s^2\frac{A0}{A1}+s\frac{K}{NA1}\tau_1+\frac{K}{NA1})} = \frac{\left(\frac{K}{A1}\right)(1+s\tau_1)}{(s^3+s^2\frac{1}{\tau_2}+sm\frac{1}{\tau_2}\tau_1+m\frac{1}{\tau_2})} \tag{5.8}$$

After simplification, the transfer function ($TF(s)$) of the third-order PLL can be written as

$$TF(s) = \frac{\left(\frac{K}{A1}\right)(1 + s\tau_1)}{(s^3 + s^2\frac{1}{\tau_2} + sm\frac{1}{\tau_2}\tau_1 + m\frac{1}{\tau_2})} \tag{5.9}$$

The CE of the third-order PLL or the denominator of $TF(s)$ can be written as

$$(s^3 + s^2\frac{1}{\tau_2} + sm\frac{1}{\tau_2}\tau_1 + m\frac{1}{\tau_2}) = 0 \tag{5.10}$$

The new constant m is written as

$$m = \left(\frac{K}{NA0}\right) \tag{5.11}$$

In Equation (5.11) $m = \left(\frac{K}{NA0}\right)$ is a gain factor$\left(\frac{K}{N}\right)$ divided by sum of capacitances ($A0 = C2 + C3$). The constant m has been used throughout this chapter. Equation (5.9) states that m, τ_1, τ_2 control the poles of a third-order PLL. The pole values in turn control the unit step response, lock time, and other performance parameters of a third-order PLL.

This expression for the CE of a third-order PLL-can be compared with the canonical CE for a third-order system as

$$as^3 + bs^2 + cs + d = (s^3 + \frac{1}{\tau_2}s^2 + m\frac{\tau_1}{\tau_2}s + m\frac{1}{\tau_2}) = 0 \quad (5.12)$$

Equating the coefficients of the powers of s in Equation (5.12), one obtains:

$$a = 1 \quad (5.13)$$

$$b = \frac{1}{\tau_2} \quad (5.14)$$

$$c = m\frac{\tau_1}{\tau_2} \quad (5.15)$$

$$d = \frac{m}{\tau_2} \quad (5.16)$$

Equation (5.13-5.16) relates to the canonical coefficients of the characteristic equation of third-order system to the PLL parameters thereby allowing stability criteria such as Routh stability to be applied to the PLL. This approach of equating coefficients has been used multiple times in this chapter. All other control theoretical techniques such as Routh and Nyquist can be applied to the PLL. From Routh stability standpoint two equations which determine stability of a third-order PLL can be added following [Dorf, 2005]. The inequalities for the coefficients following Routh-Hurwitz criteria are written as

$$ad - bc > 0 \; and \; a, b, c, d > 0 \quad (5.17)$$

Using the PLL parameters by substituting Equations (5.13) to (5.16) Equation (5.17) can be written as

$$\frac{m}{\tau_2} - \left(m\frac{\tau_1}{\tau_2}\right)\frac{1}{\tau_2} > 0 \quad (5.18)$$

5.5 Nickalls's Parameters for all roots

To relate the roots of CE to the PLL parameters, this section makes use of Nickalls's method [Nickalls, 1993] to solve for roots of CE of a third order PLL in terms of its parameters. This section also provides performance criteria of PLL from the roots of its CE. To solve for the roots the CE, the parameters in Equations (5.12-5.15) must be related to certain intermediate parameters. Then these intermediate parameters can be used to develop expressions for the roots.

The subsection attempts to highlight the parameters that one needs to compute the roots of a cubic PLL. These parameters are used and are related to the PLL performance parameters such as phase

margin and jitter. This section establishes the viability of Nickalls's approach for solution of cubic equation. Parameters a, b, c, d have been explained in Equation (5.12) to (5.15).

First parameter as defined by [Nickalls, 1993] (x_N), in terms of PLL parameters is expressed as

$$x_N = -\frac{b}{3a} = -\frac{1}{3\tau_2} \tag{5.19}$$

Second parameter as defined by [Nickalls, 1993], in terms of PLL parameters is written as

$$\delta^2 = \frac{b^2 - 3c}{9} = \frac{1}{(3\tau_2)^2} - \frac{m\tau_1}{3\tau_2} \tag{5.20}$$

Third parameter as defined by [Nickalls, 1993], in terms of PLL parameters is written as

$$y_N = \frac{2b^3}{27} - \frac{bc}{3} + d = \frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right) \tag{5.21}$$

Fourth parameter as defined by [Nickalls, 1993], in terms of PLL parameters after squaring can be expressed as

$$h^2 = 4\delta^6 \tag{5.22}$$

Substituting the value of δ^2, the parameter h is expressed in terms of coefficients b and c as

$$h^2 = 4\left(\frac{b^2 - 3c}{9}\right)^3 = 4\left(\frac{\left(\frac{1}{\tau_2}\right)^2 - 3\frac{m\tau_1}{\tau_2}}{9}\right)^3 \tag{5.23}$$

Fifth parameter defined by [Nickalls, 1993] in terms of PLL parameter is written as

$$\cos 3\theta = \frac{-y_N}{h} = -\left\{\frac{\frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right)}{2\left(\frac{\left(\frac{1}{\tau_2}\right)^2 - 3\frac{m\tau_1}{\tau_2}}{9}\right)^{3/2}}\right\} \tag{5.24}$$

The discriminant (Δ) of a third-order PLL (with CE) can be written following [Barnard and Child,2011] as

$$\Delta = 18bcd - 4b^3d + b^2c^2 - 4c^3 - 27d^2 \tag{5.25}$$

The parameters required for computation of the Nickalls's parameters x_N, δ^2 *and* y_N [Nickalls, 1993] are independent of whether the third-order PLL has two complex conjugate roots or all real roots.

Table 5.2 Discriminants and Cardano's parameter for a PLL

Parameter	Expression
Discriminant	$\Delta = 18\left(\frac{1}{\tau_1}\right)\left(m\frac{\tau_2}{\tau_1}\right)\left(\frac{m}{\tau_1}\right) - 4\left(\frac{1}{\tau_1}\right)^3\left(\frac{m}{\tau_1}\right) + \left(\frac{1}{\tau_1}\right)^2\left(m\frac{\tau_2}{\tau_1}\right)^2 - 4\left(m\frac{\tau_2}{\tau_1}\right)^3 - 27\left(\frac{m}{\tau_1}\right)^2$ (5.26) Setting $\Delta = 0$ in Equation (5.24) allows the terms with positive and negative signs to be separated $18\frac{m^2\tau_2}{\tau_1^3} + \frac{m^2\tau_2^2}{\tau_1^4} = 4\left(\frac{1}{\tau_1}\right)^4(m) + 4\left(\frac{m\tau_2}{\tau_1}\right)^3 + 27\left(\frac{m}{\tau_1}\right)^2$ (5.27) Canceling the common factor of m/τ_1^2 on both sides of Equation (5.26) and rearranging the terms, $\Delta_{\text{LHS}} = 18\frac{\text{m}\tau_2}{\tau_1} + \frac{\text{m}\tau_2^2}{\tau_1^2}$ (5.28) $\Delta_{\text{RHS}} = \frac{4}{\tau_1^2} + 4\frac{\text{m}^2\tau_2^3}{\tau_1} + 27\text{m}$ (5.29) The inequalities for the three cases have been duly described in [Barnard and Child,2011] If $\Delta < 0$ or equivalently $\Delta_{\text{LHS}} - \Delta_{\text{RHS}}$ <0, the PLL has complex roots If $\Delta > 0$ or equivalently $\Delta_{\text{LHS}} - \Delta_{\text{RHS}}$ >0, the PLL has real roots If $\Delta = 0$ or equivalently $\Delta_{\text{LHS}} = \Delta_{\text{RHS}}$, the PLL has real and equal roots The signs of discriminant are different from the conditions described by Nickalls's Equations.
Parameter G of Cardan	Characteristic Equation $= s^3 + s^2\left(\frac{1}{\tau_1}\right) + s\left(\frac{m}{\tau_1}\right)\tau_2 + \left(\frac{m}{\tau_1}\right)$ (5.30) To derive G and H parameters of Cardan [Barnard and Child, 2011], a cubic CE of the form must be written, $s^3 + 3b_1s^2 + 3c_1s + \left(\frac{m}{\tau_1}\right) = 0$ (5.31)

	This is a slightly different form of the CE (different from Equation (5.9)) which is written to maintain conformity with the original derivations of [Barnard and Child, 2011]. Equating the powers of the coefficients of Equation (5.9) with the corresponding canonical form of CE of cubic equation $b_1 = \left(\frac{1}{3\tau_1}\right)$ (5.32) $c_1 = \left(\frac{m\tau_2}{3\tau_1}\right)$ (5.33) $d = \left(\frac{m}{\tau_1}\right)$ (5.34) The parameter G of Cardan, [Barnard and Child, 2011] can be written in terms of PLL parameters as, $G = d - 3b_1c_1 + 2(b_1)^3$ (5.35) Substituting $a1, b1, c1, d1$ in Equation (5.34), parameter G is written as, $G = \left(\frac{m}{\tau_1}\right) - 3\left(\frac{1}{3\tau_1}\right)\left(\frac{m\tau_2}{3\tau_1}\right) + 2\left(\frac{1}{3\tau_1}\right)^3$ (5.36)
Parameter H of Cardan	$H = ac_1 - {b_1}^2$ (5.37) Substituting for b_1 and c_1 in Equation (5.36), the parameter H of Cardan is written as $H = \left(\frac{m\tau_2}{\tau_1}\right) - \left(\frac{1}{3\tau_1}\right)^2$ (5.38)
Relationship of G and H To the discriminant	As provided in [Bernard and Child, 2011], the discriminant for any cubic system has been historically described in terms of G and H Parameters of Cardano. $\Delta = \mathrm{G}^2 + 4\mathrm{H}^3$ for a = 1 (5.39) It determines the whether the roots are real or complex

The description of the discriminant (Equation (5.26)), Cardano's G (Equation (5.35)) and H (Equation (5.37)) in term of PLL parameters has been done in this thesis for the first time.

5.6 Application of the Vieta's Circle for the location of the three real roots of a third-order PLL

This section presents a complete geometrical interpretation of a PLL with three real and distinct roots, that is the primary equation (5.11) has three real and unequal roots. The construction of the Vieta's circle is presented with greater detail than was presented in [Nickalls, 1993]. Next the locations of poles are related to the three Nickalls's parameters δ , θ and x_N . Finally, the parameters of PLL are expressed in terms of the geometry of the Vieta's circle. In Figure 5.3, the perpendiculars, the location of the center $(x_N, 0)$ or $\left(-\frac{1}{3\tau_2}, 0\right)$ and the values of the three roots are illustrated.

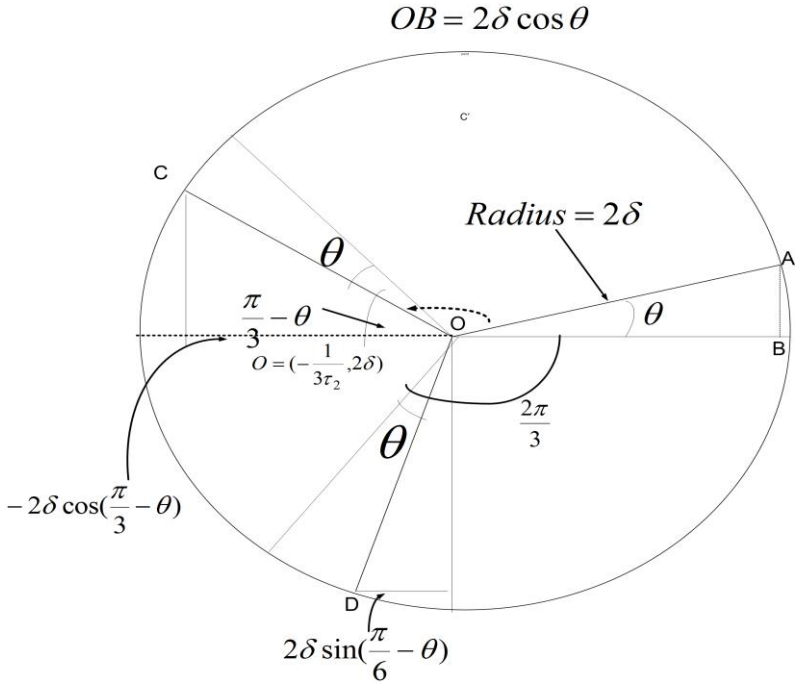


Figure 5.3: Construction of the Vieta's circle with center at $\left(-\frac{1}{3\tau_2}, 0\right)$ and radius 2δ

The original construction of the Vieta's circle in [Nickalls, 1993] lacked a detailed description and it has been now added to this chapter. Smaller the time constant of the LPF (τ_2) **,** the further away the center of the Vieta's circle is from the origin.

In Figure 5.3, the center of the circle $(x_N, 0)$ is located following [Nickalls, 1993]. x_N-is the x coordinate of the center of Vieta's circle and y co-ordinate of the center of circle is $0;2\delta$ is the

radius of Vieta's circle and θ is the rotation angle in Vieta's circle. Since the poles α, β and γ, the associated equations for the poles are written as

$$\alpha = x_N + 2\delta cos\theta \tag{5.40}$$

$$\beta = x_N + 2\delta \cos\left(\theta + \frac{2\pi}{3}\right) \tag{5.41}$$

$$\gamma = x_N + 2\delta \cos\left(\theta + \frac{4\pi}{3}\right) \tag{5.42}$$

It is necessary to describe the construction of the Vieta's circle and the subsequent location of the 3 poles. The first root can be located by considering the second term of Equation (5.40). To locate point B, one must first consider line OB along the X axis of with its length equal to the radius. Then the radius (OB) is rotated through an angle θ anti-clockwise to form line OA (same length as OB). Then line AB which is perpendicular to the X axis is dropped from point A to the X axis. From the triangle OAB, the location of the first root is written as

$$\alpha = Location\ of\ centre\ (O) + \ OAcos\theta \tag{5.43}$$

To locate the second root, one must first examine the second term on the RHS of Equation (5.41). One must rotate the phasor OA by multiplying it with $e^{j2\pi/3}$(this constitutes a120^o anticlockwise rotation). One must drop a second perpendicular from the point C down to the X axis. Thus, geometrically the location of the second real pole can be written as

$$\beta = x_N + 2\delta \cos\left(\theta + \frac{2\pi}{3}\right) = x_N - 2\delta \cos\left(\frac{\pi}{3} - \theta)\right) \tag{5.44}$$

Finally, to compute the location of third root, one must apply the following transformation, considering it is in the third quadrant between π and $\frac{3\pi}{2}$,one must rotate the phasor OA by multiplying it with $e^{j4\pi/3}$, (240^0 anticlockwise). This implies that phasor OD is obtained by multiplying the phasor OA with $e^{j4\pi/3}$. The location of third pole (Equation 5.42) is written as

$$\gamma = x_N + 2\delta \cos\left(\theta + \frac{4\pi}{3}\right) = x_N - 2\delta \sin\left(\frac{\pi}{6} - \theta\right) \tag{5.45}$$

The next step is the establishment of the analytical connection between the real poles of a third-order PLL and the Nickalls's parameters δ, θ and x_N. In a matrix form, the Equations (5.40, 5.41 and 5.42) can be written as

$$\begin{bmatrix}\alpha\\ \beta\\ \gamma\end{bmatrix} = \begin{bmatrix}1 & 1 & 0\\ 1 & cos\frac{2\pi}{3} & -sin\frac{2\pi}{3}\\ 1 & cos\frac{4\pi}{3} & -sin\frac{4\pi}{3}\end{bmatrix}\begin{bmatrix}x_N\\ 2\delta cos\theta\\ 2\delta sin\theta\end{bmatrix} \tag{5.46}$$

One can compute of the radius of the Vieta's circle if the roots of the third-order PLL are already known. If the roots(α, β, γ) are known, the parameters $x_N, 2\delta cos\theta,$ and $2\delta sin\theta$ must be computed by inverting the 3x3 matrix in Equation (5.46). The closed-form expressions for $x_N, 2\delta cos\theta, 2\delta sin\theta$ can be written as

$$\begin{bmatrix} x_N \\ 2\delta cos\theta \\ 2\delta sin\theta \end{bmatrix} = \begin{bmatrix} 1 & 1 & 0 \\ 1 & cos\frac{2\pi}{3} & -sin\frac{2\pi}{3} \\ 1 & cos\frac{4\pi}{3} & -sin\frac{4\pi}{3} \end{bmatrix}^{-1} \begin{bmatrix} \alpha \\ \beta \\ \gamma \end{bmatrix} \tag{5.47}$$

Carrying out the 3x3 matrix inversion analytically of Equation (5.44), one obtains the closed-form expressions for the parameters of the Vieta's circle in terms of the three roots.

The combined three equations can be written as

$$x_N = \frac{1}{3}(\alpha + \beta + \gamma) \tag{5.48}$$

$$2\delta cos\theta = \left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right) \tag{5.49}$$

$$2\delta sin\theta = (-0.5774\beta + 0.5774\gamma) \tag{5.50}$$

Equations (5.48) to (5.50) connect the roots of the third-order charge pump PLL to the parameters of the Vieta's circle which are real linear combinations of the roots. Once $x_N, 2\delta cos\theta \; and \; 2\delta sin\theta$ are computed, they are required to compute the radius (2δ) of the Vieta's circle and the Vieta's angle (θ) as a function of the roots. This establishes the relationship between the parameters of the Vieta's circle and the roots of a third-order PLL.

From the Equations (5.49) and (5.50), the expression for Vieta's angle θ can be written as

$$tan\theta = \frac{(-0.5774\beta + 0.5774\gamma)}{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)} \tag{5.51}$$

Equation (5.51) relates Vieta's angle (θ) of [Nickalls, 1993] to the values of the three real roots and it has not been discussed in open literature. Squaring both sides of Equations (5.49) and (5.50) and simplifying leads to a new expression for the square of the radius of Vieta's circle,

$$\delta^2 = \frac{1}{4}\{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)^2 + (-0.5774\beta + 0.5774\gamma)^2\} \tag{5.52}$$

Equation (5.52) is a relationship between the roots of the CE of Third order PLL and the half-radius of the Vieta's Circle (δ). This relationship between the half-radius of Vieta's circle and the three real roots of third-order PLL constitutes a new contribution and has not been discussed in the open literature. Equations (5.49 and 5.50) relate the three real roots of third-order PLL to the two parameters $\delta$and θ which were originally described by [Nickalls,1993]. These expressions are not found in the open literature for a third-order PLL.

Finally, an analytical derivation is performed to compute the product of the sensitivities of VCO and PFD when the real poles are known. This derivation relates the real poles of a third order PLL to the capacitance ratio. The next phase relates the coefficients of the CE to sums and products of its roots. The denominator of closed loop transfer function of third order PLL is written as

$$(s^3 + \frac{1}{\tau_2}s^2 + m\frac{\tau_1}{\tau_2}s + m\frac{1}{\tau_2}) \tag{5.53}$$

Following [Nickalls, 1993, Dickson, 1922] the product of the roots is equal to the coefficient of the 0^{th} power of s in Equation (5.53)

$$\alpha\beta\gamma = -\frac{m}{\tau_2} \tag{5.54}$$

The negative sign on the right side of Equation (5.54) is explained by ([Barnard and Child, 2017, Nickalls, 1993]). Now the sum of the three roots is equal to the coefficient of the second power of s^2 (in Equation (5.53).

$$(\alpha + \beta + \gamma) = -\frac{1}{\tau_2} \tag{5.55}$$

Substituting Equation (5.55) in Equation (5.54) and simplifying, one obtains

$$m = \frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)} \tag{5.56}$$

The parameter m is directly related to the sensitivity of VCO, the sensitivity of PFD, the divide ratio and the time constant τ_1,where $\tau_1$is the time constant of the series path, $\tau_1 = R2C2$. For a stable PLL with 3 real poles or 2 complex and 1 real pole both the numerator and the denominator of Equation (5.56) are negative.

The divider ratio (N) of feedback path is estimated as a division of the output and input frequencies of the PLL.

$$N = (f_{out}/f_{in}) \tag{5.57}$$

The ratio N will be an integer for integer PLLs and a fractional number for fractional-N PLLs. The divider ratio is related to a fixed input frequency (f_{in}) and a fixed output frequency (f_{out}) of the PLL. For real roots and an over-damped PLL, the approach to estimate K_V, K_ϕ and N from the roots of CE of PLL is rather straight forward.

From Equation (5.56), the parameter 'm' of a third-order PLL is determined through the expression $m = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)}$, we also know $m = \frac{K_V\, K_\phi}{NA0}$ from [He,2007] and Equation (5.11)

From the expression for the PLL parameter m , (Equation 5.56) the quantities N the VCO sensitivity K_V, the PFD detector sensitivity K_ϕ can be related to the roots as

$$m = \frac{K_V\, K_\phi}{NA0} = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)} \tag{5.58}$$

In Equation (5.58), N is the divider ratio of the PLL and the variable($A0$=$C2 + C3$) is the sum of the loop filter capacitances. Equation (5.58) connects the product of sensitivities of the VCO and the PFD to the three poles of a third-order PLL. The function $\frac{K_V\, K_\phi}{NA0}$ has been termed to as a "loop gain" by [He, 2007].

The final parameter of the PLL that should be computable from the roots of the CE is the capacitance ratio b_c which is expressed as

$$b_c = \frac{\tau_1}{\tau_2} = \frac{C2}{C2||C3} \tag{5.59}$$

From Equation (5.20) the value of δ^2 is written as

$$\delta^2 = \frac{1}{(3\tau_2)^2} - \frac{m\tau_1}{3\tau_2} \tag{5.60}$$

Rearranging the terms in Equation (5.60), one obtains:

$$\frac{m\tau_1}{3\tau_2} = \frac{1}{(3\tau_2)^2} - \delta^2 \tag{5.61}$$

Substituting the value of m from Equation (5.56) the capacitance ratio (b_c) can be expressed as

$$b_c = \frac{3}{m}\left\{\frac{1}{(3\tau_2)^2} - \delta^2\right\} = \frac{3}{\frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)}}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \delta^2\right\} \tag{5.62}$$

By substituting the value of δ^2 from Equation (5.52) into Equation (5.62), one obtains:

$$b_c = \frac{3(\alpha+\beta+\gamma)}{\alpha\beta\gamma}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \left(\frac{1}{4}\{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)^2 + (-0.5774\beta + 0.5774\gamma)^2\}\right)\right\} \quad (5.63)$$

Equation (5.63) establishes the relationship between the three real roots (α, β, γ) and the capacitance ratio (b_c). This new relationship has not been reported in open literature. From b_c it is possible to estimate the second time constant (τ_1)

$$\tau_1 = b_c\tau_2 \quad (5.64)$$

The complete expression for the time constant (τ_1)can be written in terms of the poles as

$$\tau_1 = \frac{3(\alpha+\beta+\gamma)}{\alpha\beta\gamma}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \left(\frac{1}{4}\{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)^2 + (-0.5774\beta + 0.5774\gamma)^2\}\right)\right\}\left\{-\frac{1}{(\alpha+\beta+\gamma)}\right\} \quad (5.65)$$

Once the capacitance ratio (b_c) and sum of capacitances $(A0 = C2 + C3)$ are calculated, it is possible to calculate a known parameter such as Phase Margin (PM). One can calculate the PM of

$$PM = \left(tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right)\right) \quad (5.66)$$

A derivation allows the connectivity to be established between the roots of the CE and the phase margin. Comparing the denominators of the closed-loop transfer functions. The first denominator (first form of the CE) expression is written as

$$(s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2}) = 0 \quad (5.67)$$

The second denominator expression (second form of the CE) is written as

$$\{s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c\} = 0 \quad (5.68)$$

The second denominator expression has been given by [He,2007]. Next, the parameters of the first denominator$((s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2})$ are expressed in terms of those of the second denominator$\{s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c\}$. This is accomplished by taking ratios of coefficients in the first and second denominator expressions.

Firstly, taking the ratio of the coefficients for s^0 and s^2 in the first denominator expression and the second denominator expressions

$$\frac{\frac{m}{\tau_2}}{\frac{1}{\tau_2}} = \frac{\omega_z\omega_{p2}\omega_c}{\omega_{p2}} = \omega_z\omega_c \quad (5.69)$$

By cancelling the constant terms in Equation (5.69) one can write the PLL constant m in terms of its loop BW and zero as

$$m = \omega_z \omega_c \tag{5.70}$$

By taking the ratio of the coefficients for s^0 an s^1 in the first denominator expression and the second denominator expressions

$$\frac{\frac{m}{\tau_2}}{\frac{m\tau_1}{\tau_2}} = \frac{\omega_z \omega_{p2} \omega_c}{\omega_{p2} \omega_c} = \omega_z \tag{5.71}$$

Lastly taking the ratio of the coefficients for s^1 and s^2 in the first and second denominator

$$\frac{\frac{m\tau_1}{\tau_2}}{\frac{1}{\tau_2}} = \frac{\omega_{p2} \omega_c}{\omega_{p2}} = \omega_c \; Implies \; m\tau_1 = \omega_c \tag{5.72}$$

From Equation (5.67) can expression can be written for the Loop Bandwidth (ω_c) in terms of roots, the numerator expression in (5.72) equals the sum of the roots taken two at a time. The denominator is Equation (5.72) equals the sum of the roots with a negative sign. This follows [Nickalls, 1993 and Barnard and Child, 2011].

$$\omega_c = \frac{\frac{m\tau_1}{\tau_2}}{\frac{1}{\tau_2}} = \frac{(\alpha\beta + \beta\gamma + \gamma\alpha)}{-(\alpha + \beta + \gamma)} \tag{5.73}$$

Considering the sum of the roots of the CE and equating it to the coefficient of s^0 one can write

$$\frac{1}{\tau_2} = \omega_{p2} = -(\alpha + \beta + \gamma) \tag{5.74}$$

One additional derived expression will help to close this by using Equations (5.69) and (5.65) and substituting the value of b_c from Equation (5.61),

$$\frac{\omega_{p2}}{\omega_z} = \frac{\frac{1}{\tau_2}}{\frac{1}{\tau_1}} = b_c \tag{5.75}$$

The ratios in Equations (5.68-69) should be used to compute a new expression for Phase Margin. The original equation for phase margin is given by [He, 2007]. Taking the tangent of both sides of Equation (5.63) one obtains a new equation

$$tan\phi = \frac{\frac{\omega_c b_c}{\omega_{p2}} - \frac{\omega_c}{\omega_{p2}}}{1 + \left(\frac{\omega_c}{\omega_z}\right)\left(\frac{\omega_c}{b_c \omega_z}\right)} \tag{5.76}$$

Now applying the substitutions derived in Equations (5.68) and (5.69) one obtains an expression for the tangent of the PM in terms of the roots. Secondly, the ratio $\frac{\omega_c}{\omega_z}$ is expressed in term of the ratio $\frac{\omega_c}{\omega_{p2}}$ using Equation (5.70). Finally, the following substitutions are made $\omega_c = -\frac{(\alpha\beta+\beta\gamma+\gamma\alpha)}{(\alpha+\beta+\gamma)}$ using Equation (5.73) and $\omega_{p2} = -(\alpha + \beta + \gamma)$ using Equation (5.74), the expression for PM is written as

$$tan\phi = \frac{\left(\frac{\omega_c}{\omega_z}\right) - \left(\frac{\omega_c}{\omega_{p2}}\right)}{1 + \left(\frac{\omega_c}{\omega_z}\right)\left(\frac{\omega_c}{\omega_{p2}}\right)} = \frac{\left(\frac{\omega_c}{\omega_{p2}}\right) b_c - \left(\frac{\omega_c}{\omega_{p2}}\right)}{1 + \left(\frac{\omega_c}{\omega_{p2}}\right) b_c \left(\frac{\omega_c}{\omega_{p2}}\right)} \tag{5.77}$$

Substituting the values in Equation (5.77) one obtains

$$tan\phi = \frac{\frac{\omega_c}{\omega_{p2}}(b_c - 1)}{1 + \frac{\omega_c^2 b_c}{\omega_{p2}^2}} = \frac{\frac{(\alpha\beta + \beta\gamma + \gamma\alpha)}{(\alpha + \beta + \gamma)^2}(b_c - 1)}{1 + \frac{(\alpha\beta + \beta\gamma + \gamma\alpha)}{(\alpha + \beta + \gamma)^2} b_c \frac{(\alpha\beta + \beta\gamma + \gamma\alpha)}{(\alpha + \beta + \gamma)^2}} \tag{5.78}$$

Equation (5.78) relates the tangent of the PM with the root values and the capacitance ratio. Equation (5.78) is an original contribution of this chapter and not found in the open literature.

5.7 Relationship between Phase margin and Vieta's angle for all 3 real poles

The first equation (related to expression for δ^2 in [Nickalls, 1993]) relates the capacitance ratio with the Vieta's circle center (x_N) and its half radius (δ). The parameters b and c are replaced by PLL parameters following Equations (5.14) and (5.15),

$$\delta^2 = \frac{b^2 - 3c}{9} = \frac{1}{(3\tau_2)^2} - \frac{m\tau_1}{3\tau_2} = \frac{1}{(3\tau_2)^2} - \frac{mb_c}{3} \tag{5.79}$$

In Equation (5.79) b_c is the capacitance ratio. By multiplying both sides of Equation (5.79) by the constant 3 one can write a new equation as

$$3\,\delta^2 = \frac{1}{3(\tau_2)^2} - mb_c \tag{5.80}$$

Substituting the value of m from Equation (5.56) one obtains:

$$3\,\delta^2 = \frac{1}{3(\tau_2)^2} - \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)}b_c = \frac{1}{3(\tau_2)^2} - \frac{\alpha\beta\gamma}{3x_N}b_c \tag{5.81}$$

Substituting the expressions for the three roots from Equations (5.46) - (5.48) in terms of x_N and 2δ, one the following expression for the product of the roots:

$$\alpha\beta\gamma = (x_N + 2\delta cos\theta)\left(x_N + 2\delta\cos\left(\theta + \frac{2\pi}{3}\right)\right)(x_N + 2\delta\cos\left(\theta + \frac{2\pi}{3}\right)) \tag{5.82}$$

Simplifying Equation (5.82) one obtains:

$$\alpha\beta\gamma = x_N^3 - \frac{3}{4}x_N(2\delta)^2 + \frac{1}{4}(2\delta)^3\left(\cos^3(\theta) - 3cos\theta + 3\cos^3(\theta)\right) \tag{5.83}$$

Further simplifying Equation (5.83) one obtains:

$$\alpha\beta\gamma = x_N^3 - \frac{3}{4}x_N(2\delta)^2 + \frac{1}{4}(2\delta)^3 cos(3\theta) = N_\theta \tag{5.84}$$

The new intermediate variable N_θ is used to simplify Equation (5.84). Substituting the new intermediate variable N_θ back into Equation (5.81)

$$3\delta^2 = \frac{1}{3(\tau_2)^2} - N_\theta b_c \tag{5.85}$$

By substitution of the value of $\tau_2 = \frac{1}{(\alpha+\beta+\gamma)} = \frac{1}{3x_N}$ into Equation (5.85) one obtains:

$$(N_\theta)b_c = \frac{1}{3(\tau_2)^2} - 3\delta^2 = \frac{9x_N^2}{3} - 3\delta^2 = 3x_N^2 - 3\delta^2 \tag{5.86}$$

Dividing both sides of Equation (5.86) by N_θ $b_c = \frac{3x_N^2 - 3\delta^2}{\left(x_N^3 - \frac{3}{4}x_N(2\delta)^2 - \frac{1}{4}(2\delta)^3(cos3\theta)\right)}$

$$b_c = \frac{3x_N^2 - 3\delta^2}{x_N^3 - \frac{3}{4}x_N(2\delta)^2 - \frac{1}{4}(2\delta)^3(cos3\theta)} = \frac{M_\theta}{N_\theta} \tag{5.87}$$

Equation (5.87) is written in a compact form as the numerator expression $3x_N^2 - 3\delta^2$ is equated to a new intermediate variable M_θ

$$M_\theta = 3x_N^2 - 3\delta^2 \tag{5.88}$$

The second expression relates the PLL loop BW (ω_c) and phase margin with the capacitance ratio (b_c). This expression can be traced back to [He,2007] and modified with the substation $\frac{\omega_c}{\omega_{p2}} = \omega_c\tau_2$ following Equation (5.71), the tangent of the PM of a third order PLL is written as

$$tan\phi = \frac{(\omega_c\tau_2) - \left(\frac{\omega_c\tau_2}{(b_c)}\right)}{1 + (\omega_c\tau_2)\left(\frac{\omega_c\tau_2}{(b_c)}\right)} \tag{5.89}$$

Now let us substitute the intermediate variable

$$\gamma_c = \omega_c\tau_2 \tag{5.90}$$

From the Equation (5.89) a new expression for the capacitance ratio b_c is written as

$$b_c = \left(\frac{({\gamma_c}^2 tan\phi + \gamma_c)}{\gamma_c - tan\phi}\right) \tag{5.91}$$

the expressions for b_c in Equation (5.87) and (5.91) are equivalent. This allows us to derive a new relationship between Vieta's angle and phase margin is written as

$$\left(\frac{({\gamma_c}^2 tan\phi + \gamma_c)}{\gamma_c - tan\phi}\right) = \frac{M_\theta}{N_\theta} \tag{5.92}$$

By cross multiplying both sides of (5.92) and simplifying for $tan\phi$

$$N_\theta {\gamma_c}^2 tan\phi + M_\theta tan\phi = M_\theta\gamma_c - N_\theta\gamma_c \tag{5.93}$$

From Equation (5.93) one can derive the final expression relating Vieta's angle and the PM of a third-order PLL with all real roots. One must substitute the values of M_θ, N_θ from Equations (5.88) and (5.84) respectively to obtain to the final form of Equation (5.94),

$$tan\phi = \frac{M_\theta\gamma_c - N_\theta}{N_\theta{\gamma_c}^2 + M_\theta} = \frac{(3x_N^2 - 3\delta^2)\gamma_c - \left(x_N^3 - \frac{3}{4}x_N(2\delta)^2 - \frac{1}{4}(2\delta)^3(cos3\theta)\right)}{\left({\gamma_c}^2\left(x_N^3 - \frac{3}{4}x_N(2\delta)^2 - \frac{1}{4}(2\delta)^3(cos3\theta)\right) + (3x_N^2 - 3\delta^2)\right)} \tag{5.94}$$

Equation (5.94) directly relates three times the Vieta's angle (3θ) with the PM of a third-order PLL. A relationship between the Figure 5.3 which illustrates the geometry of the roots with the PLL phase margin has been derived for the first time. It is significant and makes a connection between control system stability with the geometry of Vieta's circle none of which have been proposed by previous authors.

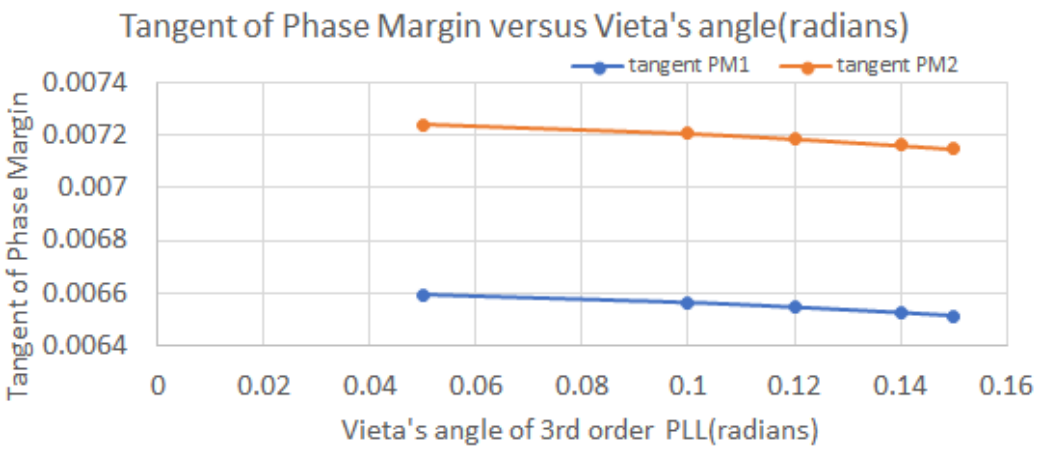


Figure 5.4 Tangent of phase margin versus Vieta's angle

A second expression can be derived which provides for the sensitivity of the phase margin with the variation of Vieta's angle by taking derivatives of both sides in Equation 5.58. the red track and blue track are plotted for two different values of $\frac{x_N}{2\delta} = 3,4$.

5.8 Analysis of third-order PLL with three equal and real roots

[Nickalls, 1993] describes the case when all three roots of a cubic equation are both equal and real. As well as the case when two roots of a cubic equation are equal and real. Both these cases are considered for the third-order PLL. The difference is the in the two equal real roots case, the radius of Vieta's circle is non-zero. In the case of three equal real roots, the radius of Vieta's circle is zero. In accordance with [Nickalls, 1993], the conditions for two equal roots are written as

$$\delta = \sqrt[3]{\frac{y_N}{2a}} \tag{5.95}$$

In Equation (5.95) the parameter y_N has been defined in Equation (5.21). Equation (5.95) has been described in Section 2.3 of [Nickalls, 1993]). In turn, parameter a is the first coefficient of the Cubic $(a = 1)$ for a third-order PLL. By substituting the numerator y_N (from Equation 5.20) in Equation (5.95) one obtains:

$$\delta = \sqrt[3]{\frac{\frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right)}{2}} \tag{5.96}$$

In Equation (5.96) δ is the half-radius of Vieta's circle as in Figure 5.3. The case of two equal roots has been defined by [Nickalls, 1993] with the roots being, $\{x_N + \delta, x_N + \delta, x_N - 2\delta\}$ as defined in section 2.2 of [Nickalls, 1993]. Substituting a =1, the roots of the third-order PLL (when two roots are real and equal) can be written in the form a column vector as

$$Z2 = \begin{bmatrix} x_N + \delta \\ x_N + \delta \\ x_N - 2\delta \end{bmatrix} \tag{5.97}$$

In Equation (5.97), the vector $Z2$ is the vector of roots of the third-order PLL written in a column format.

Substituting the values of $a = 1$ and $x_N = -\frac{1}{3\tau_2}$ and the value of δ in Equation (5.97), the three real roots of a third-order PLL can be written as

$$Z2 = \begin{bmatrix} \alpha \\ \beta \\ \gamma \end{bmatrix} = \begin{bmatrix} -\frac{1}{3\tau_2} + \sqrt[3]{\frac{\frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right)}{2}} \\ -\frac{1}{3\tau_2} + \sqrt[3]{\frac{\frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right)}{2}} \\ -\frac{1}{3\tau_2} - 2\left(\sqrt[3]{\frac{\frac{2}{27}\left(\frac{1}{\tau_2}\right)^3 - \frac{1}{3}\left(\frac{1}{\tau_2}\right)\left(\frac{m\tau_1}{\tau_2}\right) + \left(\frac{m}{\tau_2}\right)}{2}}\right) \end{bmatrix} \tag{5.98}$$

An expression of the form of Equation (5.98) appears to have not been derived for a third- order PLL in open literature. Equation (5.98) establishes the analytical connectivity between the PLL parameters m, τ_1, τ_2 and the three real roots of the CE of PLL in the case where two of the three roots are real and equal. In this section case of all the three real and equal roots case-of a third-order PLL has also been considered. The condition for this as explained in Section 2.2 of [Nickalls, 1993] as

$$y_N^2 = h^2 \tag{5.99}$$

Variable y_N is defined in Equation (5.21). Variable h is defined in Equation (5.19). This corresponds to the discriminant ($\Delta = 0$ being equal to 0. The discriminant Δ has been defined in Equation (5.25). The three equal roots case has been defined by [Nickalls, 1993] as

$$y_N^2 = 0 \tag{5.100}$$

The parameter δ is expressed as

$$\delta^2 = 0 \tag{5.101}$$

In this case the Vieta's circle (Figure 5.3) reduces to a point and computing either the diameter of Vieta's circle or $cos3\theta$ may not be meaningful. It must be remarked the three equal roots are at $s = x_N = \frac{1}{3\tau_2}$[Nickalls, 1993].

The time domain response of a third-order PLL when the three roots are equal is studied through its transfer function. The transfer function with generic poles for a third-order PLL multiplied by Laplace transform of a unit step is written as

$$G(s) = \frac{1}{s}\frac{\left(\frac{K}{A1}\right)(1 + s\tau_1)}{(s^3 + s^2\frac{1}{\tau_2} + sm\frac{1}{\tau_2}\tau_1 + m\frac{1}{\tau_2})} = \left(\frac{K}{A1}\right)\frac{(1 + s\tau_1)}{s(s+\alpha)(s+\beta)(s+\gamma)} \tag{5.102}$$

For the equal real poles case, the poles α, β, γ are equal. To relate a time constant (τ_2)related to a single pole (α) an expression can be written as

$$\alpha = x_N = \frac{1}{3\tau_2} \tag{5.103}$$

The transfer function of a PLL with 3 real and equal roots can be considered. The step response in time domain for a third-order PLL with 3 equal roots is written as

$$W(t) = L^{-1}\left(\left(\frac{K}{A1}\right)\frac{(1 + s\tau_1)}{s\left(s + \frac{1}{\tau_a}\right)\left(s + \frac{1}{\tau_a}\right)\left(s + \frac{1}{\tau_a}\right)}\right) \tag{5.104}$$

In Equation (5.104), $\frac{1}{\tau_a} = \frac{1}{3\tau_2}$ is the real and repeated pole, and the operator L^{-1} denotes the inverse Laplace transform. After performing the inverse Laplace transform the time domain response of the PLL with all three real and equal roots is written as

$$W(t) = \left(\frac{K}{A1}\right)\left\{\tau_a^3 - \tau_a^3 e^{-\frac{t}{\tau_a}} - t\tau_a^2 e^{-\frac{t}{\tau_a}} + \frac{t^2(\tau_2\tau_a^3 - \tau_a^4)}{2\tau_a^3} e^{-\frac{t}{\tau_a}}\right\} \tag{5.105}$$

The time domain step response $W(t)$of a third-order PLL with equal poles has not been discussed in the open literature. The next step is to derive an expression for m, τ_1, τ_2 in terms of the time constants and the capacitance ratio b_c . The idea is to derive a closed-form expression for the PM of a third-order PLL is terms of its single zero and its three equal poles. Such an expression has not been provided in open literature. For a generic third-order PLL, from Equation (5.56), when all the roots are equal ($\alpha = \beta = \gamma$)

$$m = \frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)} = \frac{\alpha^2}{3} \tag{5.106}$$

For the consistent root values the ratios of the coefficients of the first of the characteristic equation ($(s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2}) = 0$ will be the same as the second form of the characteristic equation. $\{s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c = 0\}$. This term by term comparison allows new relationships to be established between the ratios involving m, τ_1, τ_2 and those involving $\omega_{z,}\omega_{p2}, \omega_c$ to be related in Equations (5.92) and (5.93).

Substituting, $\alpha = \frac{1}{3\tau_1}$, one can relate the parameter m to the time constant τ_1 for the 3 equal poles.

By comparing the coefficient of s^0 between $(s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2}) = 0$ and $s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c = 0$ one obtains

$$\frac{\frac{m}{\tau_2}}{\frac{m\tau_1}{\tau_2}} = \frac{\omega_z\omega_{p2}\omega_c}{\omega_{p2}\omega_c} = \omega_z \tag{5.107}$$

By further simplifying Equation (5.107) one obtains:

$$\omega_z = \frac{1}{\tau_1} \tag{5.108}$$

By comparing the coefficient of s^1 between $(s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2}) = 0$ and $s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c = 0$ one obtains:

$$\frac{\frac{m\tau_1}{\tau_2}}{\frac{1}{\tau_2}} = \frac{\omega_{p2}\omega_c}{\omega_{p2}} = \omega_c \tag{5.109}$$

Simplifying Equation (5.109) one obtains:

$$\frac{\frac{m\tau_1}{\tau_2}}{\frac{1}{\tau_2}} = \frac{\omega_{p2}\omega_c}{\omega_{p2}} = \omega_c \tag{5.110}$$

In Equation (5.110) after cancelling common terms, an expression can be written as

$$m\tau_1 = \omega_c \Rightarrow m = \omega_c/\tau_1 = \omega_c\omega_z \tag{5.111}$$

Finally by comparing the coefficients of s^2 between $(s^3 + s^2\frac{1}{\tau_2} + s\frac{m\tau_1}{\tau_2} + \frac{m}{\tau_2}) = 0$ and $s^3 + s^2\omega_{p2} + s\omega_{p2}\omega_c + \omega_z\omega_{p2}\omega_c = 0$, one can write a relationship between the higher pole and the time constant as

$$\frac{1}{\tau_2} = \omega_{p2} \tag{5.112}$$

Now by considering only the sum of roots (coefficient of s^2) for three real and equal roots α one can write an expression for the higher pole as

$$\omega_{p2} = -3\alpha = \frac{1}{\tau_2} \tag{5.113}$$

Equation (5.113) implies by using the fact $\omega_{p2} = b_c\omega_z$ a new equation can be written

$$\omega_z = \frac{3\alpha}{-b_c} \tag{5.114}$$

Now by using the capacitance ratio and substituting the value of τ_2 from Equation (5.103)

$$\tau_1 = b_c\tau_2 = -b_c\left(\frac{1}{3\alpha}\right) \tag{5.115}$$

Next one needs to express the loop-bandwidth in terms of the real root. The first step to do this is to use the Equation (5.111) and write:

$$m = \omega_z\omega_c \tag{5.116}$$

Hence from Equation (5.116) one can write:

$$\omega_c = \frac{m}{\omega_z} \tag{5.117}$$

The second step is to use Equation (5.108) and write and expression for the zero (ω_z) as

$$\omega_z = \frac{1}{\tau_1} \tag{5.118}$$

Substituting (5.118) into Equation (5.117) one obtains for the three equal roots case

$$\omega_c = m\tau_1 = \left(\frac{\alpha^2}{3}\right) - b_c\left(\frac{1}{3\alpha}\right) = \frac{-b_c\alpha}{9} \tag{5.119}$$

Substituting the value of ω_z(equal roots case) from Equation (5.114) and ω_c from Equation (5.119) one obtains:

$$\frac{\omega_c}{\omega_z} = \frac{\frac{-b_c\alpha}{9}}{\frac{3\alpha}{-b_c}} = \frac{(b_c)^2}{27} \tag{5.120}$$

Substituting Equation (5.120) into the expression for the tangent of the Phase Margin in [He, 2007]

$$tan\,\phi = \frac{\left(\frac{\omega_c}{\omega_z}\right) - \left(\frac{\omega_c}{\omega_{p2}}\right)}{1 + \left(\frac{\omega_c}{\omega_z}\right)\left(\frac{\omega_c}{\omega_{p2}}\right)} = \frac{\left(\frac{\omega_c}{\omega_z}\right)(1 - \frac{1}{b_c})}{1 + \left(\frac{\omega_c}{\omega_z}\right)^2 \frac{1}{b_c}} = \frac{\left(\frac{(b_c)^2}{27}\right)(1 - \frac{1}{b_c})}{1 + \left(\frac{b_c^2}{27}\right)^2 \frac{1}{b_c}} \tag{5.121}$$

Equation (5.121) directly relates phase margin to poles for the equal roots case of a third-order PLL. Such an expression relating the phase margin to the single equal root and capacitance ratio (b_c) has not been discussed in open literature. It is significant that in this case the phase margin is only a function of b_c. Since for a stable pole the roots are on the left half of complex plane, $\alpha < 0$, for stable third-order PLLs and the argument of the inverse tangent function is always positive. For all equal roots, the phase margin is low. Table 5.10 describes the variation in phase margin with change in capacitance ratio. Equations (5.105) and (5.121) are the two final contributions for this section.

Table 5.3 Phase margin for various values of capacitance ratio for the equal roots case

At $\boldsymbol{\omega = \omega_c}$

Capacitance Ratio (b_c)	2	4	6	8	10	12	14	16
Phase Margin (degrees)	4.19	22.22	40.60	50.62	54.56	55.41	54.74	53.32

5.9 Relationship between PM and Spur Gain for a third-order PLL

This section aims to present to formulation to establish the relationship between the PM and the spur gain of a third order PLL. The term *Spur* stands for spurious frequencies. **Spurs stands for spurious frequencies.** The spectrum at the output of a DDS-PLL will contain spurs generated by the DDS which get propagated by the PLL. The final spectrum of a DDS-PLL combination will contain spurs generated by the DDS and additional Spurs which are generated by the PLL. Spurs produced by the DDS-PLL can readily propagate to a RF down conversion mixer and undermine the detection of an incoming RF signal by creating multiple spurious down-converted signals. In this section an alternative expression for Spur Gain (SG) of a third-order PLL is derived. SG can be defined as the closed-loop gain of a third-order PLL at the comparison frequency of a PLL. There is significance of the SG if the computed SG is considered for a given band and its adjacent bands. A high spur gain can cause a spur generated by a PLL to propagate to an adjacent band around the output frequency affecting other transmitters and receivers. It is important to identify the underlying causes of spur gains and optimize the PLL to control them.

Spurs arise in a PLL due to leakage currents and charge pump mismatches. [Banerjee, 2006] explains how spurs arise within the PLL. He also addresses the causes that largely determine the amplitude of spur. Spurs generated by the PLL make it difficult to detect a received signal due to their nearness to the received signal.

Banerjee's spur model is an empirical model arrived at after measuring and analyzing spur levels for a very large number of PLLs [Banerjee, 2006]. A type of spur is called a reference spur in [Banerjee, 2006]. Reference spurs (Spurious frequencies) are a consequence of the un-symmetric nature of the PLL charge pump which is part of the PFD (Figure 5.1). Reference spurs arise in the output spectrum of a PLL in adjacent bands and their levels can be high enough to affect the output of down conversion mixer in RF receivers. GSM application has a channel BW of 5 MHz and requires that the reference spurs are below -65dB in the adjacent bands [Shu and Sanchez-Sinencio, 2005].

Spurs can be classified based on their origin. Their origins are due to leakage currents or dues to the un-symmetric nature of PLL charge pump which leads to current mismatch. Leakage originated spurs are described in [Banerjee, 2006] and [He, 2007]. Leakage spurs originate due to leakage currents in charge pump, VCO and loop filter capacitors. On the other hand, mismatch spurs arise due to mismatches in the transistors of the charge pump. Spur gain is the amplitude of the closed-loop transfer function which controls the level of output spur. Spur gain is the same as the close

loop gain of the PLL if the frequency band under consideration is within the loop BW of the PLL. It is expressed as the logarithm of square of the amplitude of the closed-loop gain if the input frequency is below the loop BW times 10. Outside the loop BW, Spur gain is defined as the open loop gain in [Banerjee, 2006].

The Banerjee spur model is a function of comparison frequency, sensitivity of VCO, leakage current, and impedance of loop filter. The closed-form expression for SG was first given by [Banerjee, 2006]. [Banerjee, 2006] has provided an empirical expression for leakage spur model which determines the level of the leakage spur and is written as

$$S_{leakage} = L_{Base} + 20log\left(\left|\frac{I_{cpn}}{K_{\phi}}\right|\right) + Spur\ Gain \tag{5.122}$$

In Equation (5.122), $S_{leakage}$ is the amplitude of leakage spur. L_{base} is an empirical constant determined by measurement to be 16dB. [Banerjee, 2006], I_{cpn} is the charge pump leakage current (usually in nA), K_{ϕ} is the sensitivity of PFD, and $Spur\ Gain$ is the spur gain (dB). Equation (5.122) is an empirical model applicable only to leakage spurs.

Figure 5.4 illustrates the variation of spur gain as a function of leakage current. The spur gain is also affected by the K_V and sensitivity of PFD ($K_{\phi} = I_{cp}/2\pi$). For a given maximum level of leakage spur, as the leakage current in the phase detector increases the spur gain (third term in Equation (5.109).

Figure 5.4-Spur gain versus leakage current ([Banerjee, 2006] leakage model)

Figure 5.4 plots the leakage Spur gain as a function of the leakage current for thre different values of PFD sensitivity.

The spur gain is defined as the closed-loop gain at the comparison frequency or f_c. [Banerjee, 2006] refers to this as. If the loop BW is large enough, VCO sensitivity (K_v) is high and the RHS of Equation (5.109) is quite high. The resultant increased spur gain will allow propagation of spurs from the charge pump mixed with spurs in the output of DAC to propagate to the output of DDS-PLL which affects the operation of adjacent close-spaced channels.

Mismatch spurs arise due to mismatches in transistor speed, turn on and turn off times of transistors in the charge pump being. [Banerjee, 2006] has provided a second empirical model applicable to mismatch spurs model, which can be written as

$$PulseSpur(dB) = Base\ Pulse\ Spur\ + Spur\ Gain\ + 40log\left(\frac{F_{spur}}{1Hz}\right) \tag{5.123}$$

In Equation (5.123), the Spur Gain (dB) is computed at the given comparison frequency of the PFD. The first empirical constant in Equation (5.123) is $Base\ Pulse\ Spur\ = -300dB$ (defined first by ([Banerjee, 2006]). F_{spur} is the input frequency under consideration, usually integer multiples of comparison frequency. In simple terms it is the input frequency to third-order PLL (at PFD) $PulseSpur(dB)$ is the mismatch spur magnitude in dB. Equation (5.123) is an empirical equation and it is unknown whether it holds for smaller process nodes especially below 40nm. Banerjee provides an approximate analytical expression for spur gain as

$$G_{spur} = 20\log(\frac{K_v K_\phi}{4\pi^2 C2 f_c^2}) \tag{5.124}$$

The closed-loop gain in Equation (5.124) is measured at an input frequency of f_c. Equation (5.124) follows equation (11.13) in [Banerjee,2006].

$G_{Spur}$is the open loop gain at $(f = f_c)$. An expression for G_{Spur} Following [He, 2007] can be written as

$$G_{Spur} = \frac{1}{N}\frac{K}{A0}\frac{(1+s\tau_1)}{s^2(1+s\tau_2)} = m\frac{(1+s\tau_1)}{s^2(1+s\tau_2)} \tag{5.125}$$

The magnitude of spur gain can be expressed in terms of the roots of a third-order PLL as the constant term can be derived from m and m is related to the roots by an established closed-form expression (Equation (5.56)).

A procedure to compute the spur gain given the pole values or roots of CE of third-order PLL is as follows. First the parameter m is related to the three poles of the third-order PLL.

$$m = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)} \tag{5.126}$$

The time constant (τ_2) for the third-order PLL is written in terms of the PLL roots as

$$\tau_2 = -\frac{1}{(\alpha+\beta+\gamma)} \tag{5.127}$$

The expression for the capacitance ratio b_c , substituting the value of τ_2 from Equation (5.127) and the value of m from Equation (5.126) can be expressed as

$$b_c = \frac{3}{m}\left\{\frac{1}{(3\tau_2)^2} - \delta^2\right\} = \frac{3}{\frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)}}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \delta^2\right\} \tag{5.128}$$

Substituting the value of δ one obtains a new expression for the capacitance ratio(b_c)

$$b_c = \frac{3(\alpha+\beta+\gamma)}{\alpha\beta\gamma}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \left(\frac{1}{4}\left\{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)^2 + (-0.5774\beta + 0.5774\gamma)^2\right\}\right)\right\} \tag{5.129}$$

In the case of 3 real poles, the spur gain Equation (5.74) can be written in terms of the PLL parameters $m, \tau_2, and\ b_c$ as

$$G_{Spur} = m\frac{(1+s\tau_2 b_c)}{s^2(1+s\tau_2)} \tag{5.130}$$

Substituting Equation (5.76) for τ_2 in Equation (5.130), the G_{Spur} can be simplified as

$$G_{Spur} = m\frac{\left(1 - s\frac{b_c}{(\alpha+\beta+\gamma)}\right)}{s^2\left(1 - s\frac{1}{(\alpha+\beta+\gamma)}\right)} \tag{5.131}$$

Substituting Equation (5.126) for m and Equation (5.129) for the capacitance ratio b_c, in Equation (5.131), spur gain (G_{Spur}) in closed-form is written as

$$G_{Spur} = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)} * \frac{\left(1 - s\frac{\frac{3(\alpha+\beta+\gamma)}{\alpha\beta\gamma}\left\{\frac{(\alpha+\beta+\gamma)^2}{9} - \frac{1}{4}\{\left(\frac{2}{3}\alpha - \frac{\beta}{3} - \frac{\gamma}{3}\right)^2 + (-0.5774\beta + 0.5774\gamma)^2\}\right\}}{(\alpha+\beta+\gamma)}\right)}{s^2\left(1 - s\frac{1}{(\alpha+\beta+\gamma)}\right)} \quad (5.132)$$

In Equation (5.132) G_{Spur} is the Spur gain expressed as a non-linear function of the three roots. The actual spur gain is computed by taking using the following equation due to [Banerjee, 2005].

$$Spur\ Gain = 20log_{10}(G_{Spur}) \quad (5.133)$$

The closed-form expression relating spur gain to the poles as in Equation (5.118) is an original contribution. Table 5.4 illustrates the close correlation of the results on Spur gain obtained through the approach of roots of CE of third-order PLL (Equation (5.118) and that through the parameters of PLL (Equation (5.112). and a close agreement is evident between the results of two approaches.

Table 5.4 Spur gain computed from roots versus from PLL parameters

Frequency shift(kHz)	4	5.99	7.99	10	11.98	13.98
Spur Gain (Computed through Equation 5.112) (dB)	-20.62	-24.148	-26.647	-28.58	-30.169	-31.5
Spur Gain (Computed through Equation 5.123) (dB)	-20.73	-24.221	-26.64	-28.64	-30.0182	-31.53

The results of Table 5.4 illustrate that Spur gain is altered as the frequency shift is changed.-For the simulation of results of Table 5.4, m=1.34x10^{15}; τ_1 = 4.4x10^{-9}; ω_c = 5.9x10^6. The poles are, α = -32x10^6 rad/sec; β=-96x10^6 rad/sec; γ=-99.2x10^6 rad/sec.

5.10 Case of two complex roots and one real root of CE of a third-order PLL

In the previous sections, the case of a third-order PLL with all real poles or all real and equal poles has been analyzed with details and discussions. As an extension of that case, it is necessary to analyze the third order PLL with two complex poles and one real pole. The three roots are written following [Nickalls, 1993] but the root expressions are connected to PLL parameters.

The expression for the real root of a third-order PLL is written as (following, [Nickalls, 1993])

$$\alpha = x_N + \sqrt[3]{\frac{1}{2a}\left(-y_N + \sqrt{y_N^2 - h^2}\right)} + \sqrt[3]{\frac{1}{2a}\left(-y_N - \sqrt{y_N^2 - h^2}\right)} \tag{5.134}$$

The hyperbolic form for the real root of a cubic equation was first given by [Holmes, 2002]. The expression can be written as

$$\alpha = x_N - 2\delta\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right) \tag{5.135}$$

The advantage of the Equation (5.135) is that its more compact than the complex cubic form in Equation (5.134). Corresponding to the real root (α), the corresponding complex conjugate roots of the CE are written as functions of α, δ. Equation (5.136) is derived in [Nickalls, 1993] paper (section 2.2) as

$$\beta, \gamma = -\frac{\alpha}{2} \pm j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2} \tag{5.136}$$

The hyperbolic formulation for the real root is written as in terms of parameter that have been defined earlier x_N(defined in Equation (5.19)), δ – defined in Equation (5.20), y_N- defined in Equation (5.21) and h – defined in Equation (5.21). The hyperbolic form expression for the real root is written as

$$\alpha = x_N - 2\delta\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right) \tag{5.137}$$

The first contribution is the relationship between the angle between the root versus PLL parameters $m, \tau_1 \; and \; \tau_2$. The amplitude of the complex roots($\beta \; and \; \gamma$) is computed by taking the expressions for the real part($-\frac{\alpha}{2}$) and imaginary part($\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}$) from Equation (5.136) then

computing the squares of the real part and imaginary part, summing the squares and generating square root of the sum. The amplitude of the complex root is written as

$$|\beta| = \sqrt{\left(\frac{\alpha}{2}\right)^2 + \left(\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right)^2} \tag{5.138}$$

Simplifying the above and substituting the value of δ^2 from Equation (5.19) one can write the final expression as

$$|\beta| = \sqrt{\alpha^2 - \left(\frac{\frac{1}{\tau_2^2} - \frac{3m\tau_1}{\tau_2}}{3}\right)} \tag{5.139}$$

The closed-form expression of Equation (5.139) provides a means of connecting the magnitude of the complex roots to the real root $|\beta|$ and PLL parameters m, τ_1 and τ_2

The second closed-form expression of Equation (5.140) relates the phase angle between the two complex roots ($\angle\beta$) with the real root and PLL parameters m, τ_1 and τ_2. It is written as

$$\angle\beta = tan^{-1}\left\{\sqrt{3}\sqrt{1 - \frac{\frac{4}{9}\left(\frac{1}{\tau_2^2} - \frac{3m\tau_1}{\tau_2}\right)}{\alpha^2}}\right\} \tag{5.140}$$

If the third-order PLL has distinct maxima and minima ([Nickalls, 1993]), the real root can be written in a hyperbolic form following [Holmes, 2002]

$$\alpha = x_N - 2\delta\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right) \tag{5.141}$$

The complex conjugate roots can be expressed in terms of [Nickalls, 1993] parameters

$$\beta, \gamma = \frac{1}{2}\left(x_N - 2\delta\left(\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right) \pm j\sqrt{3}\sinh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right)\right)\right)\right) \tag{5.142}$$

From Equation (5.126) the value of m can be expressed as

$$m = \frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)} = \frac{\alpha\beta\gamma}{3x_N} \tag{5.143}$$

The denominator of (5.143) can be simplified as because the imaginary parts of $(\alpha + \beta + \gamma)$ cancel out. The numerator term $\alpha\beta\gamma$ of Equation (5.143) must be simplified further in terms of the Nickalls's parameter. Substituting the values of β, γ from Equation (5.136) into the numerator term of Equation (5.143) one obtains:

$$\alpha\beta\gamma = (\alpha)(\beta\gamma)$$

$$= \left(x_N - 2\delta\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right)\right)\left(-\frac{\alpha}{2} + j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right)\left(-\frac{\alpha}{2}\right.$$

$$\left. - j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right)$$

$$= \left(x_N - 2\delta\cosh\left(\frac{1}{3}\operatorname{arccosh}\left(\frac{y_N}{h}\right)\right)\right)\left(\left(\frac{\alpha}{2}\right)^2 + \frac{3}{4}\left(\alpha^2 - 4\delta^2\right)\right) \quad (5.144)$$

Simplification of Equation (5.144) allows the product of three roots to be expressed as

$$\alpha\beta\gamma = \left(x_N - 2\delta\cosh\left(\tfrac{1}{3}\operatorname{arccosh}\left(\tfrac{y_N}{h}\right)\right)\right)\left(\tfrac{3}{4}\alpha^2 + \tfrac{1}{4}\alpha^2 - 3\delta^2\right) = \left(x_N - 2\delta\cosh\left(\tfrac{1}{3}\operatorname{arccosh}\left(\tfrac{y_N}{h}\right)\right)\right)(\alpha^2 - 3\delta^2) \quad (5.145)$$

To compute the capacitance ratio (b_c) one must consider the sum of roots of a third-order PLL taken two at a time, this is because of the expression. One must form a simplified expression for the sum of roots taken two at a time is written as

$$mb_c = \alpha\beta + \beta\gamma + \alpha\gamma \quad (5.146)$$

Simplifying the sum of roots two at a time is written as

$$\alpha\beta + \beta\gamma + \alpha\gamma = \alpha(\beta + \gamma) + \beta\gamma = \alpha\beta + \beta\gamma + \alpha\gamma = \alpha\left(2 * \left(-\frac{\alpha}{2}\right)\right) + \beta\gamma$$

$$= -\alpha^2 + (\beta\gamma) \quad (5.147)$$

Substituting values of the two complex conjugate roots β, γ one obtains:

$$\alpha\beta + \beta\gamma + \alpha\gamma = -\alpha^2 + \left(-\frac{\alpha}{2} + j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right)\left(-\frac{\alpha}{2} - j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right) \quad (5.148)$$

Further simplifying Equation (5.148) an expression for the sum of the roots taken two at a time can be written as

$$\alpha\beta + \beta\gamma + \alpha\gamma = -\alpha^2 + \left(\alpha^2 - 3\delta^2\right) = -3\delta^2 \quad (5.149)$$

From [Nickalls, 1993] as well as Equation (5.46) the sum of three roots can be written as

$$(\alpha + \beta + \gamma) = 3x_N \quad (5.150)$$

Hence the ratio from Equations (5.131 and 5.134) can be expressed in simpler format. To shorten the composite expressions let us define $\varphi = \frac{1}{3}\text{arccosh}\left(\frac{y_N}{h}\right)$. After this substitution the variable m can be expressed as

$$m = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)} = \frac{\left(x_N - 2\delta\cosh\left(\frac{1}{3}\text{arccosh}\left(\frac{y_N}{h}\right)\right)\right)(\alpha^2 - 3\delta^2)}{3x_N} = \frac{(x_N - 2\delta\cosh\varphi)(\alpha^2 - 3\delta^2)}{3x_N} \tag{5.151}$$

The expression for m in terms of hyperbolic terms is unique has never been derived by any other authors. It is an original contribution of this chapter. A final additional derivation relates the capacitance ratio b_c to the terms $x_N, \delta \; and \; \varphi$. Equation (5.146) can be rewritten as

$$b_c = \frac{m}{(\alpha\beta+\beta\gamma+\alpha\gamma)} = \frac{(x_N - 2\delta\cosh(\varphi))\left(\alpha^2 - 3\delta^2\right)}{3x_N} \cdot \frac{1}{(\alpha(\beta+\gamma)+\beta\gamma)} \tag{5.152}$$

Substituting the values of roots β, γ in Equation (5.152)

$$b_c = \frac{(x_N - 2\delta\cosh(\varphi))\left(\alpha^2 - 3\delta^2\right)}{3x_N} \cdot \frac{1}{\left(\alpha\left(-2*\frac{\alpha}{2}\right)+\beta\gamma\right)}$$

$$b_c = \frac{(x_N - 2\delta\cosh(\varphi))\left(\alpha^2 - 3\delta^2\right)}{3x_N} \cdot \frac{1}{\left(\alpha\left(-2*\frac{\alpha}{2}\right)+\beta\gamma\right)}$$

$$= \frac{(x_N - 2\delta\cosh(\varphi))(\alpha^2 - 3\delta^2)}{3x_N} \cdot \frac{1}{(-\alpha^2+\beta\gamma)} \tag{5.153}$$

The sum of roots taken two at a time is expressed as

$$(\alpha(\beta+\gamma)+\beta\gamma) = -\alpha^2 + \beta\gamma$$

$$= -\alpha^2 + \left(-\frac{\alpha}{2} + j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right)\left(-\frac{\alpha}{2} - j\frac{\sqrt{3}}{2}\sqrt{\alpha^2 - 4\delta^2}\right) \tag{5.154}$$

Hence, substituting the value of m from Equation (5.135) and value of the $(\alpha\beta+\beta\gamma+\alpha\gamma)$ from Equation (5.137) one can write the expression for the capacitance ratio in a simplified form:

$$b_c = \frac{m}{(\alpha\beta + \beta\gamma + \alpha\gamma)} = \frac{(x_N - 2\delta\cosh(\varphi))\left(\alpha^2 - 3\delta^2\right)}{3x_N}\frac{1}{(\alpha(\beta+\gamma)+\beta\gamma)} = \frac{(x_N - 2\delta\cosh(\varphi))\left(\alpha^2 - 3\delta^2\right)}{3x_N}.\frac{1}{3\delta^2} \quad (5.155)$$

The time constant (τ_2) can be computed as

$$\tau_2 = -\frac{1}{(\alpha+\beta+\gamma)} = -\frac{1}{\left(\alpha + 2Re(\beta)\right)} = -\frac{1}{3x_N} \quad (5.156)$$

In Equation (5.156) $Re(\beta)$ refers to the real part of the two complex roots of a third-order PLL. The Equation (5.155) relates the capacitance ratio $b_c$with the three parameters defined originally in [Nickalls, 1993]. Such an expression has not been described earlier in open literature. The Equations (5.155) and (5.156) are significant contributions of this chapter. The hyperbolic form makes it easier than the original form proposed in [Nickalls, 1993].

5.11 New expressions for the ratio of Noise power to Carrier power

The phase noise and various sources of noise have been addressed in a detailed manner in chapter 4. The phase noise to carrier power ratio has been established by [Rategh, 2000], [Savic, 2002] and [Musa, 2002]. The phase noise must be measured and analyzed at a given offset frequency. If the Phase noise to carrier power ratio is too high, alternate values of sensitivity of VCO (K_V) and capacitance ratio (b_c) must be chosen to reduce the level of phase noise. That is one might need to use a VCO with a lower level of sensitivity to achieve a target ratio of noise power to carrier power. The ratio of noise power to carrier power based on [Lam and Razavi, 2000] can be written as

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{C2}{C2+C3}\right)^2\left(\frac{K_V}{2\Delta\omega}\right)^2\left(\frac{2k_BTR2}{1+(R2\frac{C3C2}{C2+C3}\Delta\omega)^2}\right)\right\} \quad (5.157)$$

In Equation (5.157) $\left(\frac{P_n}{P_c}\right)$ is the noise power to carrier power ratio (dB), K_V is the VCO sensitivity, k_B is the Boltzmann's constant($1.38064852 \times 10^{-23}$ m^2 kg s^{-2} K^{-1}), T is the absolute temperature in Kelvin, $R2$ is the series resistance of loop filter, $C2$ is the series capacitance of loop filter, $C3$ is the parallel capacitance of loop filter, and $\Delta\omega$ is the frequency offset from the carrier frequency.

Replacing the capacitance ratio $b_c = \frac{C2}{\frac{C2C3}{(C2+C3)}}$ and the time constant, $\tau_2 = R2\frac{C2C3}{(C2+C3)}$. Equation (5.157) can be rewritten as

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{b_c - 1}{b_c}\right)^2 (\frac{K_V}{2\Delta\omega})^2 \left(\frac{2k_BTR2}{1 + (\tau_2\Delta\omega)^2}\right)\right\} \quad (5.158)$$

In Equation (5.158) τ_2 is the time constant of value $R2 * (\frac{C2C3}{(C2+C3)})$. Equation (5.158) is in a form that facilitates the identification of the operative factors which can reduce noise. The first operative factor is(b_c), a capacitance ratio will very marginally reduce the noise power to carrier power ratio only if the capacitance ratio is low. The second operative factor is the loop BW contained in the last term (in Equation 5.158). The third operative factor is the resistance of loop filter. $\frac{P_n}{P_c}$ is reduced as the resistance of loop filter $(R2)$ is reduced. The noise level rises as loop BW is increased. Lower value of VCO sensitivity (K_V) (and hence longer lock time) will reduce $\frac{P_n}{P_c}$. The $\left(\frac{P_n}{P_c}\right)$ ratio drops rapidly as the offset frequency $(\Delta\omega)$ rises. Figures 5.5 depict the variation of the $(\frac{P_n}{P_c})$ ratio with change in offset frequency for fixed K_V and(b_c).

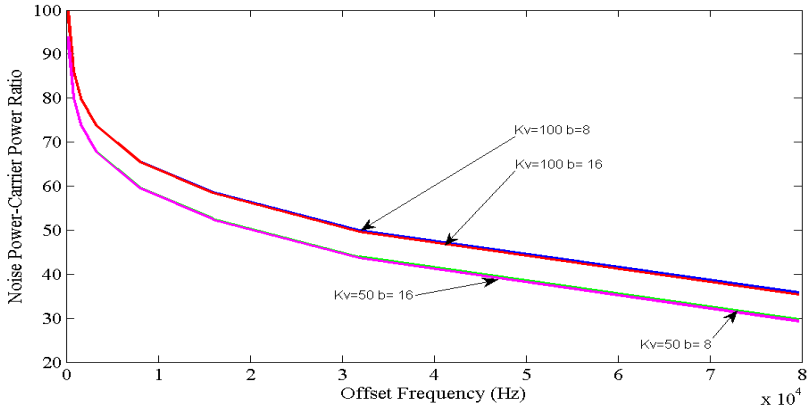


Figure 5.5 Noise power/Carrier power $(\frac{P_n}{P_c})$versus offset frequency for range of capacitance ratios and VCO sensitivity (Wider range of Offset frequencies)

Figure 5.5 is generated for a range of offset frequencies, from DC to 80kHz. It is generated for a VCO sensitivity of 100Hz/volt and 50 Hz/Volt. It is observed from Figure 5.5 that for a given

offset frequency, lower values of (K_V), leads to lower $\left(\frac{P_n}{P_c}\right)$. For a given offset frequency, greater the capacitance ratio($b_c = \frac{C2}{C3} + 1$), slightly lower will be the ratio $\left(\frac{P_n}{P_c}\right)$. Hence even though the response of the PLL will be slower to step change in frequency and phase step, to achieve lower noise level one needs to use a lower value of K_V. Additional detailed observations on the results of Figures 5.5 include that the ratio (Pn/Pc) is reduced by around 2dB as the capacitance ratio b_c is doubled (from 8 to 16). For a given value of b_c, (Pn/Pc) is raised by less than 6 dB as (K_V) is increased from 50MHz/V to 100 MHz/V.

Three conclusions can be drawn through the results of Figure 5.5. Firstly, as the VCO sensitivity is reduced the ratio Pn/Pc can be reduced for a given value of b_c. Secondly, for a given offset frequency and b_c the ratio Pn/Pc decreases rapidly as the offset frequency is altered. Analytical formulation to derive the relationship between the real poles and (Pn/Pc) and a simple characterization will be the focus of the discussion to follow.

A new derivation to link directly the loop BW of the PLL to $\left(\frac{P_n}{P_c}\right)$ is presented in this section in

The problem of estimating the Pn/Pc value when the roots are known by expressing τ_2 in terms of roots, α, β, γ is addressed. Since the time constant τ_2 can be written in terms of the roots as(following Equation (5.114),

$$\tau_2 = R2\frac{C3C2}{C2+C3} = -\frac{1}{(\alpha+\beta+\gamma)} \tag{5.159}$$

Hence Equation (5.158) can be written as

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{b_c-1}{b_c}\right)^2\left(\frac{K_V}{2\Delta\omega}\right)^2\left(\frac{2k_BTR2}{1+\left(-\frac{1}{(\alpha+\beta+\gamma)}\Delta\omega\right)^2}\right)\right\} \tag{5.160}$$

Equation (5.160) relates the sum of the 3 real roots (α, β, γ) or complex roots to $(\frac{P_n}{P_c})$. The form of the expression in Equation (5.160) as not been discussed in open literature. It is worth exploring if the VCO sensitivity (K_V) can be replaced with a closed-form expression involving only the roots of the CE. The middle term in Equation (5.160) is a direct function of m and the VCO sensitivity is related to m (following Equation (5.10) through the equation:

$$m = \frac{K_V K_\phi}{N(C2 + C3)} \tag{5.161}$$

Simplifying the expression for K_V one obtains, and replacing the value of m as a function of only the roots (following Equation 5.54),

$$m = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)} \tag{5.162}$$

It has been shown earlier in this chapter $\tau_2 = -\frac{1}{(\alpha+\beta+\gamma)}$ and $m\frac{\tau_1}{\tau_2} = (\alpha\beta + \beta\gamma + \alpha\gamma)$, this implies one can write an expression for the time constant as

$$\tau_1 = (\alpha\beta + \beta\gamma + \alpha\gamma)\frac{\tau_2}{m} \tag{5.163}$$

Substituting, the product of the three roots and the constant term $\frac{m}{\tau_2} = -(\alpha\beta\gamma)$, one obtains:

$$\tau_1 = -(\alpha\beta + \beta\gamma + \alpha\gamma)\frac{1}{\alpha\beta\gamma} \tag{5.164}$$

Now $b_c = \frac{C2}{\frac{C2C3}{(C2+C3)}}$ is the capacitance ratio of the PLL loop filter. The VCO sensitivity (K_V) can be derived from the value of m using Equation (5.10),

$$K_V = \frac{mN(C2 + C3)}{K_\phi} = \frac{mNR2(C2 + C3)}{K_\phi R2} = \frac{mNR2C2\left(1 + \frac{C3}{C2}\right)}{K_\phi R2} \tag{5.165}$$

Substituting $m = \frac{\alpha\beta\gamma}{(\alpha+\beta+\gamma)}$ in Equation (5.165) a new expression for K_V is written as

$$K_V = \frac{mN\tau_1}{K_\phi R2} = \frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)}\frac{N\tau_1}{K_\phi R2} \tag{5.166}$$

By substituting b_c , K_V and m one has a way to express (Pn/Pc) ratio in terms of all roots as

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{b_c - 1}{b_c}\right)^2\left(\frac{\frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)}\frac{N\tau_1}{K_\phi R2}}{2\Delta\omega}\right)^2 \frac{1}{(\alpha + \beta + \gamma)^2}\left(\frac{b_c}{b_{c-1}}\right)^2\left(\frac{2k_B TR2}{1 + \left(-\frac{1}{(\alpha + \beta + \gamma)}\Delta\omega\right)^2}\right)\right\} \tag{5.167}$$

Cancelling common terms in Equation (5.167) one obtains:

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{\frac{\alpha\beta\gamma}{(\alpha + \beta + \gamma)}\frac{N\tau_1}{K_\phi R2}}{2\Delta\omega}\right)^2 \frac{1}{(\alpha + \beta + \gamma)^2}\left(\frac{2k_B TR2}{1 + \left(-\frac{1}{(\alpha + \beta + \gamma)}\Delta\omega\right)^2}\right)\right\} \tag{5.168}$$

Equation (5.168) is obtained after cancelling $\left(\frac{b_c-1}{b_c}\right)$ terms one obtains the final form for $\frac{P_n}{P_c}$.

In Equation (5.168) the roots of the CE have been related to Pn/Pc. The ratio (Pn/Pc) has been computed by two approaches. The first approach uses the roots of CE of PLL only. The second

approach uses the circuit parameters of PLL. A noise power to carrier power relationship with real roots is not available in open literature. Its uniqueness lies in the logical connectivity between the among the three roots of CE of PLL and the Pn/Pc ratio. Figures 5.5 depicts the correlation of the results of noise power to carrier power ratio based on the approaches using parameters of PLL and the roots of CE of third-order PLL.

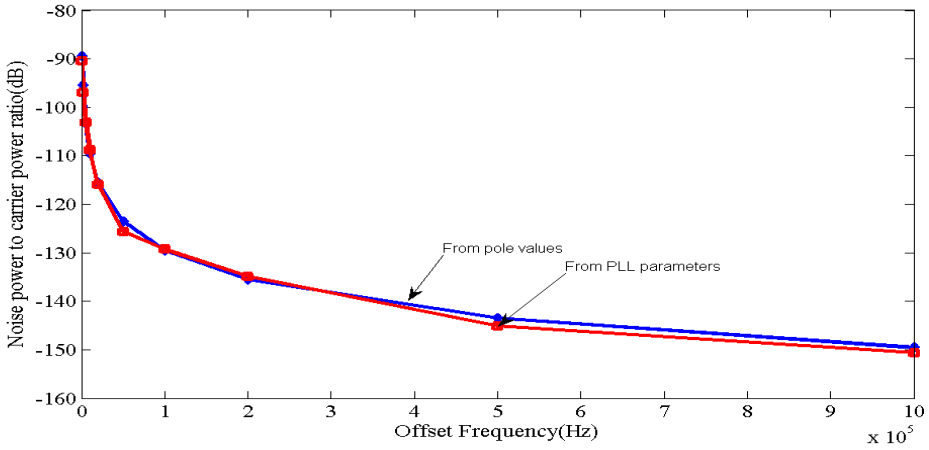


Figure 5.5 Correlation of Ratio of Noise power to Carrier power using roots of CE and parameters of PLL

There is a satisfactory agreement between the results based on conventional PLL parameters (Equation 5.157)) and the roots of CE of third-order PLL substantiating the validity of Equation (5.168). The second equation that must be considered the- relationship between the loop BW, time constant and the capacitance ratio. Equation (5.169) was first provided by [He,2007] (Equation (3.16))

$$\omega_c = \frac{\sqrt{b_c}}{\tau_2} \tag{5.169}$$

In Equation (5.169) ω_c is the loop band-width substituting value of the time constant in terms of loop BW, τ_2 is the time constant of the third-order PLL$(R2C2)$ and b_c is the capacitance ratio of third-order PLL from Equation (5.169) an expression is written as

$$b_c = (\omega_c \tau_2)^2 = \left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2 \tag{5.170}$$

In addition, the capacitance ratio can be expressed as

$$b_c = \frac{m}{(\alpha\beta + \beta\gamma + \alpha\gamma)} = \left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2 \tag{5.171}$$

This implies the PLL parameter m can be expressed in terms of poles as

$$m = \left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2 (\alpha\beta + \beta\gamma + \alpha\gamma) \tag{5.172}$$

The original equation (5.157) is written again as

$$\frac{P_n}{P_c} = 10log_{10}\left\{\left(\frac{b_c - 1}{b_c}\right)^2 \left(\frac{K_v}{2\Delta\omega}\right)^2 \left(\frac{2k_B TR2}{1 + \left(\frac{1}{(\alpha + \beta + \gamma)}\Delta\omega\right)^2}\right)\right\} \tag{5.173}$$

Substituting the values of b_c in terms of loop BW into Equation (5.173), the alternative expression is written as,

$$\frac{P_n}{P_c}$$

$$= 10log10\left\{\left(\frac{\left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2 - 1}{\left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2}\right)^2 \left(\frac{\left(\omega_c \frac{1}{(\alpha + \beta + \gamma)}\right)^2 (\alpha\beta + \beta\gamma + \alpha\gamma)N}{\frac{K_\phi R2}{2\Delta\omega}}\right)^2 \left(\frac{2k_B TR2}{1 + \left(\frac{1}{(\alpha + \beta + \gamma)}\Delta\omega\right)^2}\right)\right\} \tag{5.174}$$

An expression such as Equation (5.174) relating the noise power to carrier power ratio to the roots and the loop band-width (ω_c) , and roots has not been expressed in open literature. The loop BW (ω_c) is related to the time constant of the series path ($\tau_1 = R2C2$) and capacitance ratio (b_c)[Lam and Razavi, 2002].

5.12 Application of the ITAE criterion for third-order PLLs

The term 'Integral of Time multiplied by Absolute Error' (ITAE) is a performance measure for a control system of any order and has been proposed by [Dorf, 2005]. who provided the analytical definition for the ITAE criterion for third-order systems (Chapter 5 of [Dorf,2005]). This section is an attempt to analyze the potentially optimal third-order PLL based on control theoretic criteria. The ITAE is expressed in the form of an integral as

$$ITAE = \int_0^T t|e(t)|dt \tag{5.175}$$

In Equation (5.175), t is the time variable ranging from 0 to T and T is the finite integration interval. The term $|e(t)|$ is the absolute value of error at input to PLL (error being the difference of the primary input to the PLL and the feedback path signal). For a second-order system the ITAE performance criterion has been plotted versus ζ by [Dorf, 2005]. For a second-order system the minimum ITAE occurs at ζ=0.6. [Dorf, 2005] has provided optimum coefficients for (minimum ITAE) the CE of a third-order system (Chapter 5, Table 5.6, pp. 259). Since the coefficients b, c, d of Third order PLL are known, it is worthwhile to explore how the third-order PLL meets the ITAE criterion. The CE for third-order PLL is written as

$$s^3 + \frac{1}{\tau_2}s^2 + \frac{m\tau_1}{\tau_2}s + \frac{m}{\tau_2} = 0 \tag{5.176}$$

The canonical expression for the CE of a third order system is written as

$$as^3 + bs^2 + cs + d = 0 \tag{5.177}$$

In Equation (5.177) a is the third-order coefficient, constant b is the second-order coefficient, constant c is the first-order coefficient, and constant d is the zeroth-order coefficient.

The optimal third-order $T(s)$ (Denominator of Transfer Function) suggested by [Dorf, 2005] follows Equation (5.178). This means if a third-order system has a denominator of the form in Equation (5.178) the value of the integral in Equation (5.175) will be minimal. In this case optimal refers to the fact that ITAE is locally minimal for the suggested set of coefficients of the third-order system. The denominator of the Transfer Function of the third-order PLL is written as $(as^3 + bs^2 + cs + d)$ with $a = 1$. The expression $T(s)$ is the left-hand side of the CE. Equation (5.178) is written for optimal ITAE in a third-order system $T(s)$ is the denominator of the transfer function of the third-order PLL.

$$T(s) = s^3 + 1.75\omega_n s^2 + 2.15\omega_n^2 s + \omega_n^3 \tag{5.178}$$

Equation (5.178) is given in [Dorf, 2005], it expresses the CE of a third order system which is optimal in ITAE. By Equating the coefficients of Equations (5.176 and 5.178) and relating b, c, d to m, τ_2one can write the final expression relating the natural frequency and loop BW as

$$\omega_n = \omega_c \tag{5.179}$$

The smaller time constant (τ_2) is written as

$$\tau_2 = \frac{1}{1.75\omega_n} \tag{5.180}$$

The variable m is written in terms of the natural frequency (ω_n) as

$$m = \omega_n^3 \tau_2 = \frac{\omega_n^2}{1.75} \tag{5.181}$$

The larger time constant (τ_1) is written as

$$\tau_1 = \frac{2.15}{\omega_n} \tag{5.182}$$

Next, we attempt to derive a value or an expression for the PM of a third-order PLL. From [He, 2007], the expression for PM is written as

$$PM = \left(\frac{180}{\pi}\right) * \{\tan^{-1}(\omega_c T2) - \tan^{-1}(\omega_c T1)\} \tag{5.183}$$

To proceed further one must consider the transfer function of a third-order PLL, $H(s)$. If a form of the transfer function of a third-order PLL according to [He, 2007],

$$H(s) = N\frac{(1 + s/\omega_z)}{(1 + s/\omega_z + s^2/(\omega_z\omega_c) + s^3/(\omega_z\omega_c\omega_{p2}))} \tag{5.184}$$

In Equation (5.184) $\omega_z$is the zero of third-order PLL, ω_c is the loop BW of third-order PLL, and ω_{p2} is the higher order pole of third-order PLL. Equation (5.184) is first stated by [He,2007] (as Equation (3.19) in He's thesis). From Equation (5.178), the denominator of the transfer function of optimal third-order PLL is

$$s^3 + 1.75\omega_n s^2 + 2.15\omega_n^2 s + \omega_n^3 \tag{5.185}$$

The corresponding denominator of a third order PLL as expressed by [He, 2007] is written as

$$(s^3 + \omega_{p2}s^2 + \omega_{p2}\omega_c s + \omega_{p2}\omega_c\omega_z) \tag{5.186}$$

Phase margin can be calculated using the Equation (5.166) which is from [He,2007] thesis.

$$\text{PM} = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \tag{5.187}$$

The second pole is expressed as

$$\omega_{p2} = 1.75\omega_n \tag{5.188}$$

The loop BW is expressed in terms of natural frequency as

$$\omega_c = \frac{2.15\omega_n}{1.75} = 1.228\omega_n \tag{5.189}$$

The zero (ω_z) is expressed in terms of natural frequency (ω_n) as

$$\omega_z = \frac{\omega_n}{2.15} = 0.4\omega_n \tag{5.190}$$

Simplifying and substituting the values of $\omega_{p2}, \omega_c, \omega_z$ the into equation (5.187) the PM (radians) is written as

$$\text{PM} = \tan^{-1}\left(\frac{(2.15/1.75)\omega_n}{\frac{\omega_n}{2.15}}\right) - \tan^{-1}\left(\frac{(2.15/1.75)\omega_n}{1.75\omega_n}\right) = 0.5968\ radians \tag{5.191}$$

Equation (5.191) computes the PM as 0.5968 radians. Converting the PM value into degrees,

$$\text{PM} = \left(\frac{180}{\pi}\right) * \{\tan^{-1}\left(\frac{(2.15/1.75)\omega_n}{\frac{\omega_n}{2.15}}\right) - \tan^{-1}\left(\frac{(2.15/1.75)\omega_n}{1.75\omega_n}\right)\} = 34^o \tag{5.192}$$

Hence, PM $= 34^o$ for a third-order PLL which is optimal according to ITAE. The other conclusions is that for a third-order PLL. The first conclusion is that the third pole is as 1.75 times the natural frequency (Equation 5.188). The second conclusion is that the loop BW (ω_c) is 1.228 times the natural frequency (Equation 5.189). The third conclusion is the value of the frequency of the zero (ω_z) is 0.4 times the natural frequency (Equation 5.190). These three conclusions or the PM value for optimal ITAE have not been discussed in open literature. Equation (5.191) reveals that for ITAE optimal third-order PLL, the phase margin is independent of the loop bandwidth. This observation is a contribution of this section not covered either in [Dorf, 2005] or other previous authors.

5.13 Conclusion

This chapter has a list of significant original analytical contributions. The start of the chapter lists the application of [Nickalls, 1993] method to the three roots of the third-order PLL.

The third-order PLL is considered under three scenarios – all three real poles, all three real and equal poles and two complex conjugate poles and a single real pole.

One major original contribution for the three real roots case is the relationship between the Vieta's angle and the phase margin of the PLL which has been derived here for the first time in a closed-form.

This chapter also discussed the new analytical solutions that relate the phase margin as well as the capacitance ratio of a third-order PLL to the locations of the three real poles of the PLL. Other derived expressions proposed in this chapter relate the time constant of the loop filter to the geometrical positions of the poles. The above cited closed-form analytical solutions appear to have been addressed only by this thesis.

For the case of a third-order PLL with three real and equal poles, an expression has been derived for the step response. A new expression to capture the unit step response of a third-order PLL with three real and equal poles has been derived. It is illustrated that the parameter τ_a controls the nature of the response. The phase margin of the PLL under three real and equal poles case also been derived and it is illustrated that the PM is only a function of the capacitance ratio (b_c).

The quality of the output waveform of DDS- PLL combination is determined by both the spurs generated by the PLL as well as the phase noise or jitter. The spur gain is approximately the magnitude of open loop transfer function of the PLL if its divide ratio is high. This chapter has discussed a detailed procedure for the derivation of closed-form expression for the spur gain in terms of the three poles of a third-order PLL. Such a derivation appears to have not been attempted earlier in open literature.

This chapter compares the transfer function of a third-order PLL to an ideal third-order system whose response is optimal according to the ITAE criterion. An expression and a final value for the phase margin for a third-order PLL which meets the ITAE criterion has been derived for the first time.

This chapter has presented considerable analysis pertaining to ratio of noise power to carrier power in a PLL. This chapter has derived equation that relates the noise power to carrier power ratio to the three roots and the loop band-width (ω_c) of third order PLL. A new derivation to link directly the loop BW of the PLL to $\left(\frac{P_n}{P_c}\right)$ is also presented in this chapter.

Chapter 6 FPGA implementation of DDS and Hartley

Chapter 6 describes the FPGA implementation of the Cubic DDS, Quartic DDS, LHSC DDS and Taylor-series DDS. It compares power dissipation and FPGA resource requirements for these DDS designs. To create a proper benchmark all designs described in this chapter are implemented using the same 1.0 V core power supply, common IO voltage (2.5V), common auxiliary voltage (2.5V) and the common clock frequency of 100 MHz. All the designs are implemented on a common FPGA platform **Virtex-6™ xc6Vlx110t™** by means of the common base-board from Xilinx. The specific type of FPGA is characteristic for all designs. This ensures that for a given DDS design the common FPGA libraries are used with the similar supply voltages and frequencies. This chapter is focused on dynamic power dissipation of DDS designs and their usage of FPGA HW resources.

The relevant dynamic power is the summation of the clock power, signal power, logic power and DSP related power which is an example of a power dissipation. Dynamic power is a function of the primary clock frequency and supply voltage and the gate and wiring capacitances driven in a DDS design. Dynamic power is the power consumed by the internal circuity of a design. IO power is the power dissipated in the IO pads (Input-Output Pads) when the designed circuit is performing a DDS waveform generation at normal IO voltage. IO voltage is different and greater than core voltage and frequency. The IO power is also enhanced owing to the much larger capacitance in IO pads compared to the core circuitry. Including the IO power value in the dynamic power would be inappropriate as IO power dissipation would not have occurred if the DDS output fed a radio circuit which was also implemented on the same FPGA. The IO power dissipation is exhibited due the fact that the DDS design drives the external IO instead of driving internal circuitry in the FPGA. The IO power is a function of the output sample rate and IO load capacitance. It is not included in the Dynamic power curves. The FPGA resources are generated in Xilinx ISE (Version13.1) only after complete placement and routing has been performed.

This chapter incorporates six sections. Section 6.1 presents a design of architecture of a cubic polynomial featured with a previously specified number of switchable segments. The analysis of SFDR and dynamic power of LHSC DDS is covered in section 6.2. The implementation of the quartic DDS in FPGA is covered in section 6.3. The comparison of dynamic power and SFDR for cubic, LHSC and Taylor Series DDS is presented in section 6.4. The FPGA implementation for

the Hartley Image suppressor is discussed in section 6.5. Section 6.6 summarizes the key points highlighted in the chapter.

6.1 Cubic DDS with segment switching

This section presents an architecture for cubic DDS featured with variable number of segments. Figure 6.1 is the block diagram of a cubic polynomial DDS with the ability to switch to varying number of segments, thereby producing variable SFDR.

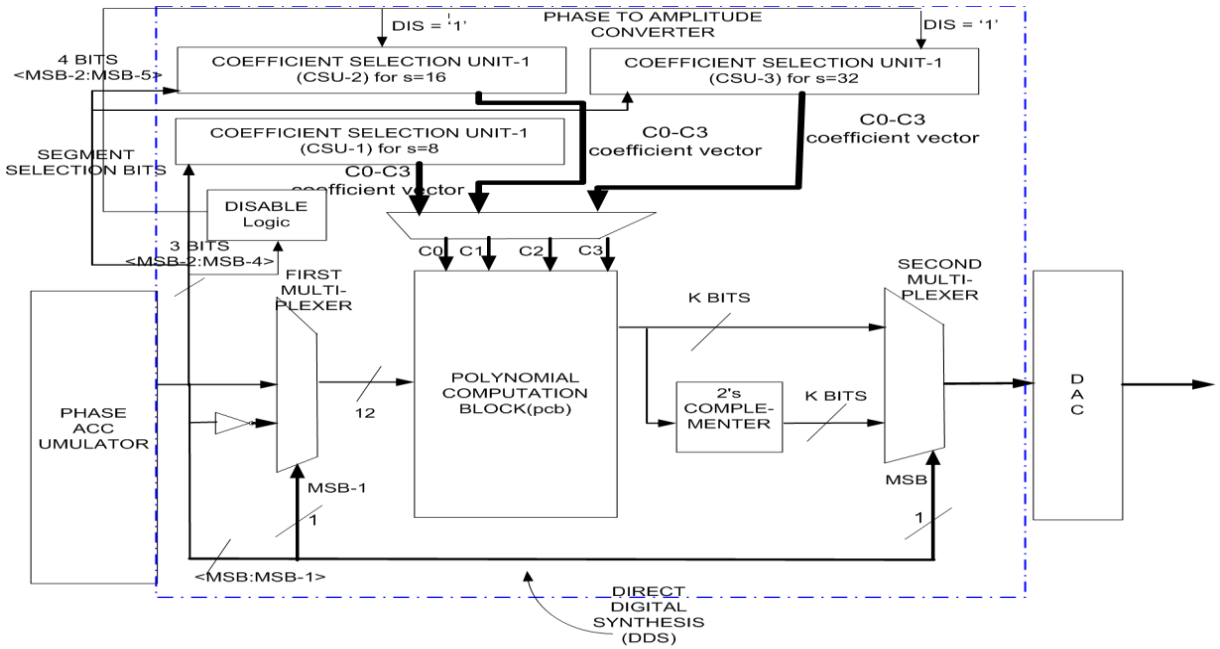


Figure 6.1 Block Diagram of cubic Polynomial DDS with a provision to select the number of segments

Figure 6.1 illustrates a modified form of the cubic DDS described in Chapter 2 (in Figure 2.5). Original blocks of Cubic DDS are included. Besides, it includes two additional CSUs each corresponding to a different number of segments instead of a single CSU, a single CSU design would be applicable if the number of segements is fixed. The selection circuitry allows the design to be operated with a variable number of segments ($s = 8 / 16 / 32$). The switchable DDS design of Figure 6.1 achieves an SFDR of 136dB for $s = 8$, and SFDR of 160dB for s=16, and the highest

SFDR of 180dB for $s = 32$. . The segment selector switch which sets the allowable various pre-designed segment numbers and the associated different CSU blocks earmarked for a chosen number of segments is shown in Figure 6.1. The phase accumulator in Figure 6.1 is split into three parts. The overall PACC word width is 14 bits. The top two bits (MSB, MSB-1) of the phase accumulator output select the quadrant. Only two bits of Phase accumulator output will suffice, as the selection is made for one of the four quadrants. The bit-width dedicated for segment selection (3 bits for $s = 8$, 4 bits for $s = 16$ and 5 bits for $s = 32$) is dedicated to the selection of the number of segments. Since the overall bit width its fixed, having greater number of bits for segment selection will reduce the number of available bits for a sample selection. The least significant bits, namely 9 bits for $s = 8$, 8 bits for $s = 16$ and 7 bits for $s = 32$, are dedicated for generation of a sample within a given segment. The coefficients are calculated in accordance with the technique discussed in [DeCaro and Strollo, 2005]. The design has three separate CSU units, which supply coefficients to the computational block called the Polynomial Computation Block(PCB). The disabling logic included in Figure 6.1 turns off the clocks of CSU-2 and CSU-3 if only CSU-1 is used($s = 8$). This ensures that unnecessary logic circuits are not kept active when they not required. If $s = 16$, the disabling logic turns off the clocks to CSU-1 and CSU-3. On the other hand, for $s = 32$, the disabling logic turns off the clocks to CSU-1 and CSU-2. The selection circuitry and disabling logic for a FPGA implemented Cubic polynomial DDS have been implemented for the first time to the best of the authors knowledge.

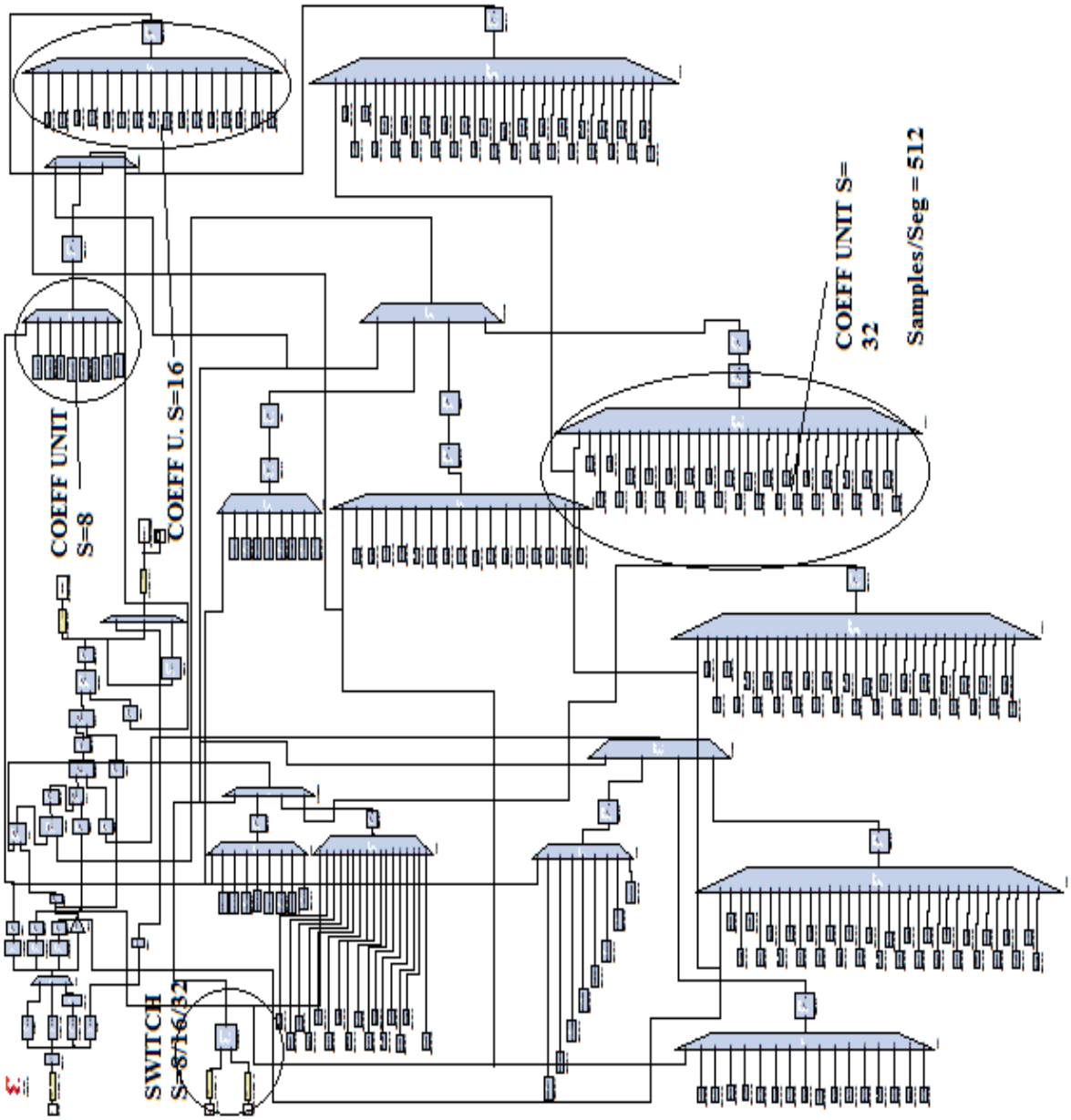


Figure 6.2 Sysgen Implementation of Cubic DDS with s=8/16/32 showing switching logic

The Sysgen™ model of a cubic polynomial based DDS with a segment selector switch allowing to select one of three possible number of segments ($s = 8, 16, 32$) with $N = 512$ is illustrated in Figure 6.2. In Figure 6.2, the Sysgen implementation includes a multipliexer with 8, 16 and 32 inputs. The different coefficient units (CSUs), as implemented on the FPGA are highlighted.The switching unit, which allows the combined DDS to operate with three different number of

segements, is highlghted as $s_e = 8/16/32$. The difference between the current research and results on hardware reported by [DeCaro and Strollo, 2005] is that neither dynamic power nor FPGA resources were mentioned in DeCaro and Strollo's paper. Besides, their paper also never made a comparison between LHSC, Taylor, quartic and cubic DDS.

6.2 LHSC DDS and its verification

Linear High Segment Count (LHSC) DDS generates sinusoids using large number of segments using a linear approximation function (the coefficient computation uses large number of points. within the segment) and a highly accurate approximation. Figure 6.3 illustrates the FPGA implementation of the LHSC DDS.

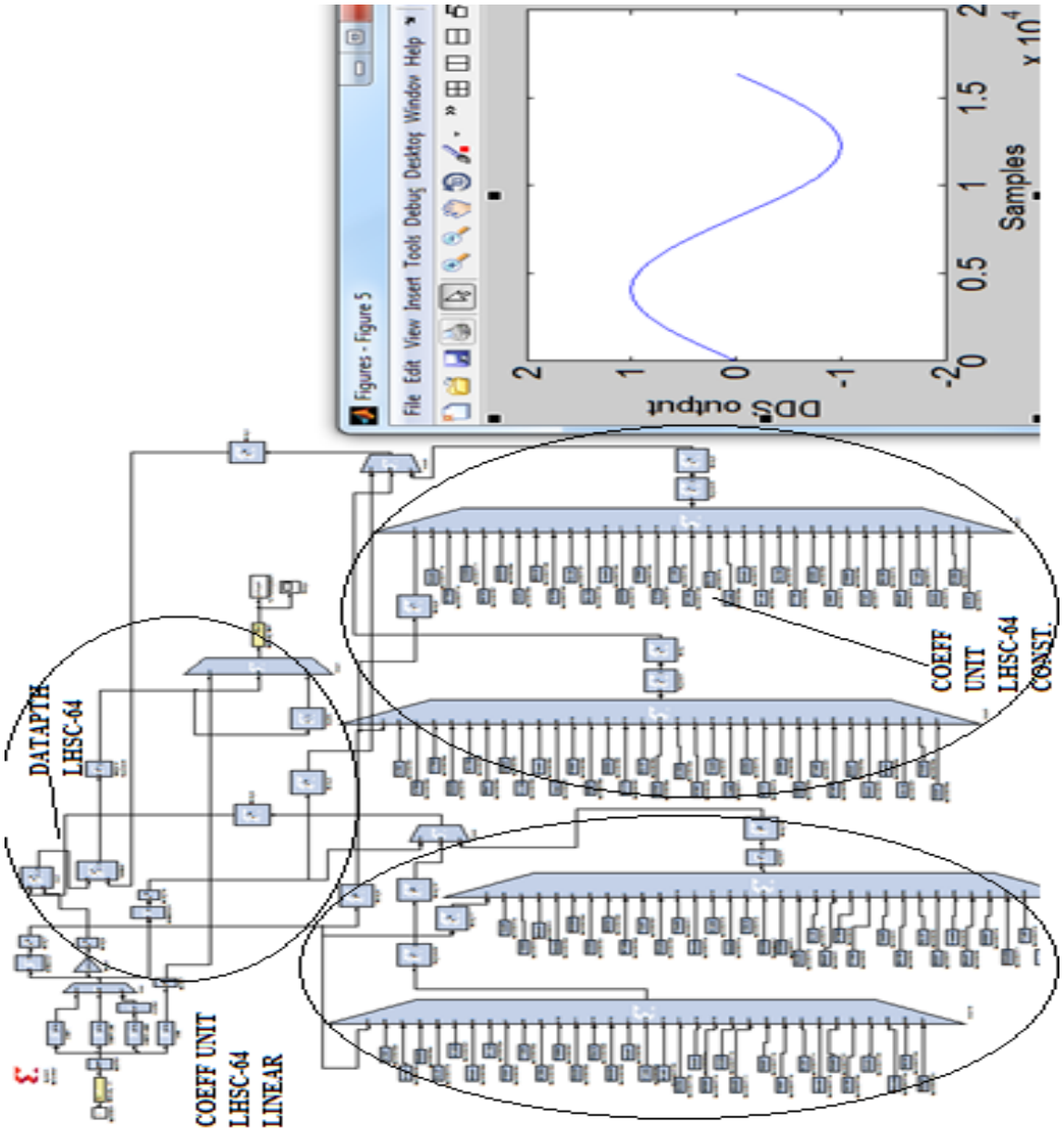


Figure 6.3 LHSC DDS with s=64 and N=512

The LHSC DDS design uses a two-stage pipeline, which is illustrated in Figure 6.3 with N=512 (512 samples per segment) and 64 segments per quadrant. The LHSC DDS uses a three-stage pipeline instead of a five-stage pipeline used in the Cubic DDS. The LHSC DDS block diagram would be same as that in Figure 6.1, except the CSU produces 2 coefficients per segment instead of 4 coefficients per segment. Two LHSC DDS designs with s=32 and 64 segments per quadrant have been implemented on Virtex™ FPGA with the same number of samples per segment. Figure

6.3 illustrates the Sysgen™ model of LHSC DDS with $s = 64$ and $N = 512$ samples/segment. The dynamic power is reduced from 122mW for cubic DDS ($s = 32$) to 23mW for LHSC DDS ($s = 32$). The LHSC DDS design has been implemented with a three-stage pipeline on a Xilinx Virtex-6 FPGA at a clock frequency of 100MHz.The LHSC-64($s = 64$) design utilizes 64 input multiplexers. Comparing the Figures 6.2 (Cubic polynomial DDS), in Figure 6.3 (LHSC DDS with $s = 64$), one can see that the data path for LHSC DDS only two stages deep as compared to five-stages deep for Cubic DDS. This difference in the number of stages is because of LHSC requires only one multiply-accumulate per sample versus three multiply-accumulates per sample for Cubic DDS. The dynamic power for the LHSC DDS design with $s = 64$ is 22% higher than the corresponding LHSC DDS with $s = 32$. Figure 6.3 illustrates the difference in dynamic power consumption between the Cubic polynomial DDS with $s = 32$ and the LHSC DDS with $s = 32$ and $s = 64$.

The SFDR of the cubic polynomial DDS($s = 32$) is 185 dB while that of LHSC DDS with $s = 32$ is 201 dB. The LHSC DDS with $s = 64$ exhibits a SFDR of 210 dB- Figure 6.4.The LHSC DDS features only one multiplier and one adder. The cubic polynomial DDS includes 3 multipliers and 3 adders. This difference means LHSC DDS has 25% of the power dissipation of a cubic polynomial DDS. The additional power dissipation of the cubic DDS is due to the additional two multipliers and two adders. It is sufficient to offset the power dissipation due to the larger muxes in LHSC DDS designs with $s = 32$ and $s = 64$**.** The LHSC DDS design with $s = 64$ has been programmed onto Virtex-6™ FPGA. A comparison of the dynamic power and resource utilization has been presented in Figure 6.5 and Figure 6.8.

6.3 Implementation of quartic DDS in FPGA

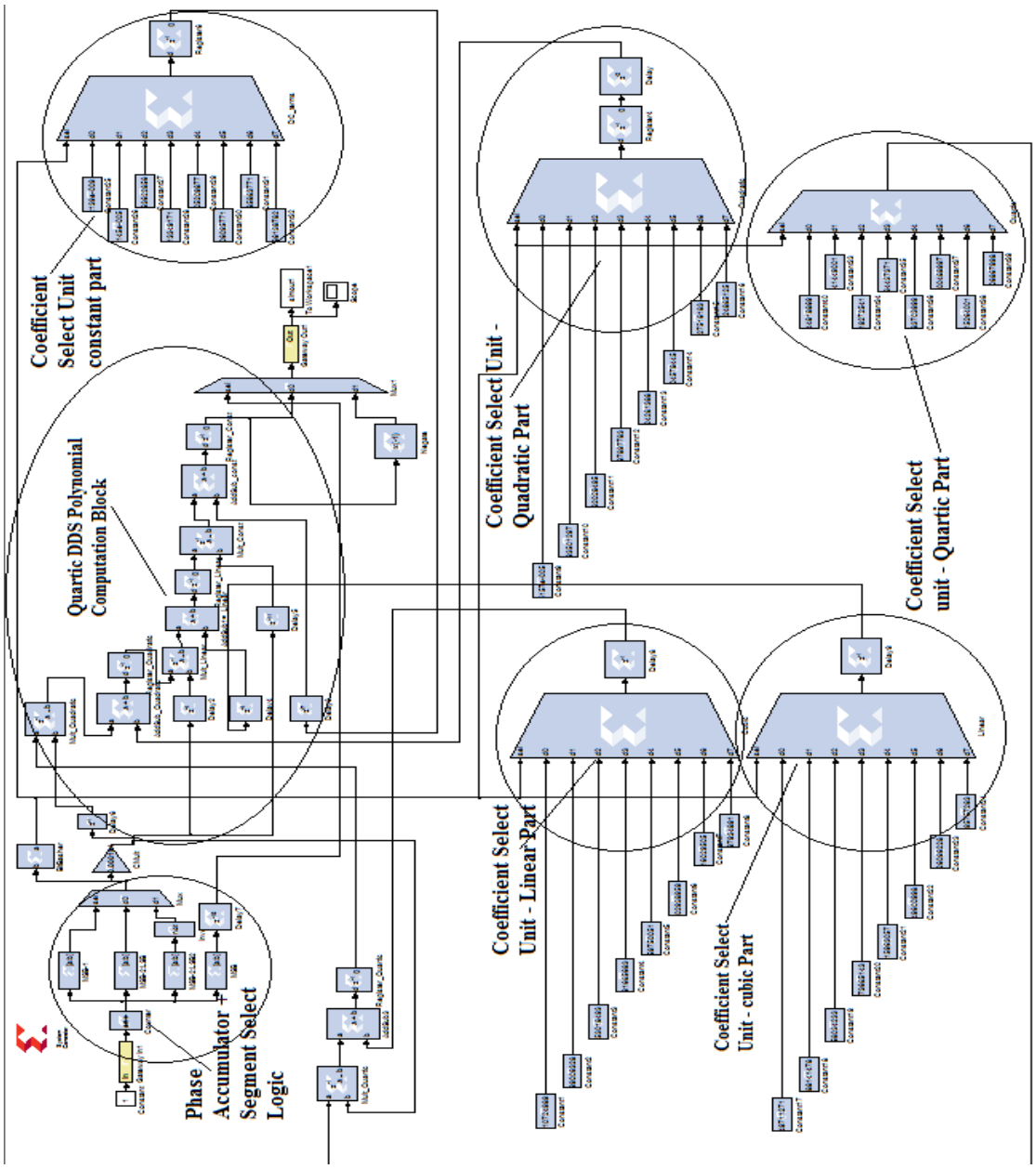


Figure 6.4 Sysgen™ model for quartic DDS with $s = 8$ and $N = 1024$ samples/segment

A Sysgen™ model of a quartic DDS (Figure 3.3/Chapter 3) with $s = 8$ and $N = 512$ samples/quadrant is illustrated in Figure 6.4. The Sysgen™ model depicted in Figure 6.4 illustrates both the datapath and the multiplexer selection (CSU) for quartic DDS. The datapath of quartic DDS requires an additional multiplier and adder, as compared to the cubic polynomial DDS single a quartic DDS requires four multiply-accumulates per output sample as opposed to three multiply-accumulates for a cubic DDS. It requires five multiplexers for coefficients vis-a-vis four

multiplexers in cubic polynomial DDS (Figure 6.4 versus Figure 6.2). The quartic DDS has a six-stage pipeline, as opposed to the three-stage pipeline for a LHSC DDS or the five-stage pipeline for the Cubic DDS. Figure 6.5 is a summary of the HW resources such as look -up tables, DSP resources, flip -flops used by different DDS designs.

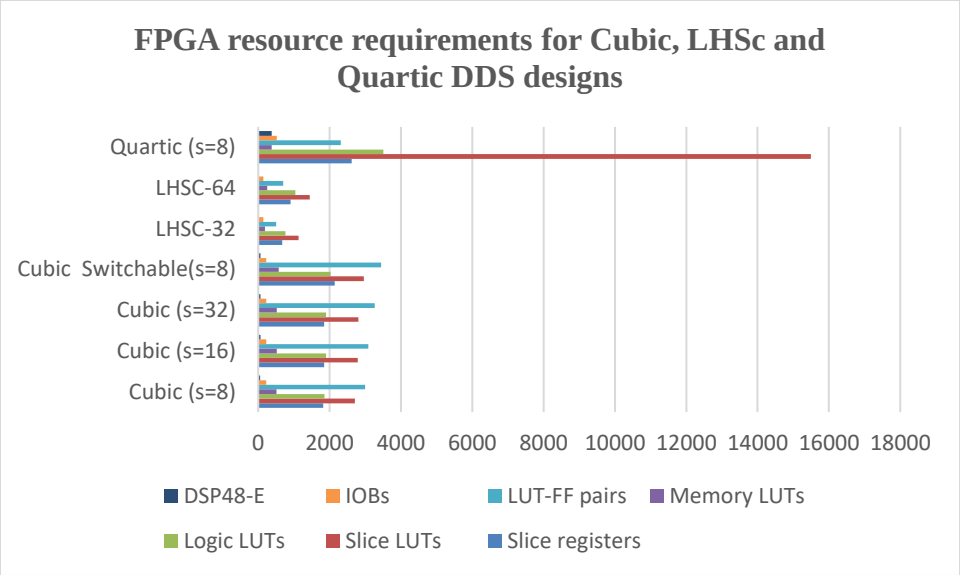


Figure 6.5 FPGA resources for different Cubic Quartic and LHSC DDS designs

In Figure 6.5 number of slice registers, number of slice-LUTs (Look-Up Tables), number of LUTs used for Logic; number of LUTs used for memory, number of LUT-Flip -flop pairs used, number of IO buffers used, and number of DSP-48E elements used for multipliers and adders.

The FPGA resource requirements for a Quartic DDS are shown in Figure 6.5, the dynamic power is shown in Figure 6.6. Comparing the power curves in Figure 6.6, it is observed that the dynamic power dissipation is increased by 150 % from 114mW (for cubic polynomial DDS, $\boldsymbol{s_e} = 8$) to 285mW (for Quartic DDS for $\boldsymbol{s_e} = 8$). For $\boldsymbol{s_e} = 8$, the additional 40 dB increase (from 136 dB to 176 dB) in SFDR of a quartic DDS over a cubic-polynomial DDS must be weighed against the higher power dissipation. Comparing the power requirements depicted in Tables 3.1a and 3.5a, it is observed that power requirement of quartic design increases by 100% because of the additional usage of the DSP48-E elements (which includes an additional multiplier and adder as compared to the cubic DDS). For quartic DDS ($\boldsymbol{s_e} = 8$), there is a six-fold increase in the number of DSP48E elements required (from 58 to 378) compared to a Cubic DDS ($\boldsymbol{s_e} = 8$), thereby contributing to

the additional power dissipation. Each column header is the power dissipated. The power values in the rows are in watts. The Xilinx compilation report automatically generates the raw information required to compile Table 6.1. The power is split up into six categories- clock, logic signals, DSP-48E (a multiplier-accumulator macro) and IO (input-output buffers). The leakage power is due to the whole FPGA not just the DDS design implemented in the FPGA hence it's a lot higher. The total Dynamic power in Table 6.1 is the sum of the power due to clocks, logic signals and DSP-48E.

Table 6.1 comparison of Dynamic power of Quartic DDS and Cubic DDS with $s_e = 8$

	Clocks	Logic	Signals	DSP-48E	IO (Input/output buffers)	Leakage	Total Dynamic Power(W)
Cubic DDS (s=8)	.024	.021	.032	.037	.400	4.3	.112
Quartic DDS (s=8)	.042	.064	.114	.065	.74	4.3	.285

In Table 6.1 both designs were implemented on the same base FPGA at common voltage and master clock frequency. The difference between the 285mW power dissipation(quartic) and the 112mW dissipation in cubic is because of an additional multiplier-accumulator and more multiplexers for a more complex CSU.

Three different Taylor series DDS designs were implemented using Virtex™ FPGA. The simulations were run at a frequency of 100MHz and supply voltage of 1.0V. All Taylor DDS designs had 32 segments per quadrant. However, the number of samples per cycle had to be reduced, as FPGAs could not accommodate very large memories. Simulations were performed for three different number of samples/cycle (N=1024 samples/cycle; N= 2048 samples/cycle and N= 4096 samples/cycle). One cannot have the huge number of samples per cycle for a Taylor series

DDS as compared to cubic DDS, owing to a lack of RAM in the FPGA. The FPGA resources for these three designs as compared to a cubic DDS with $s_e = 32$ are illustrated in Figure 6.6.

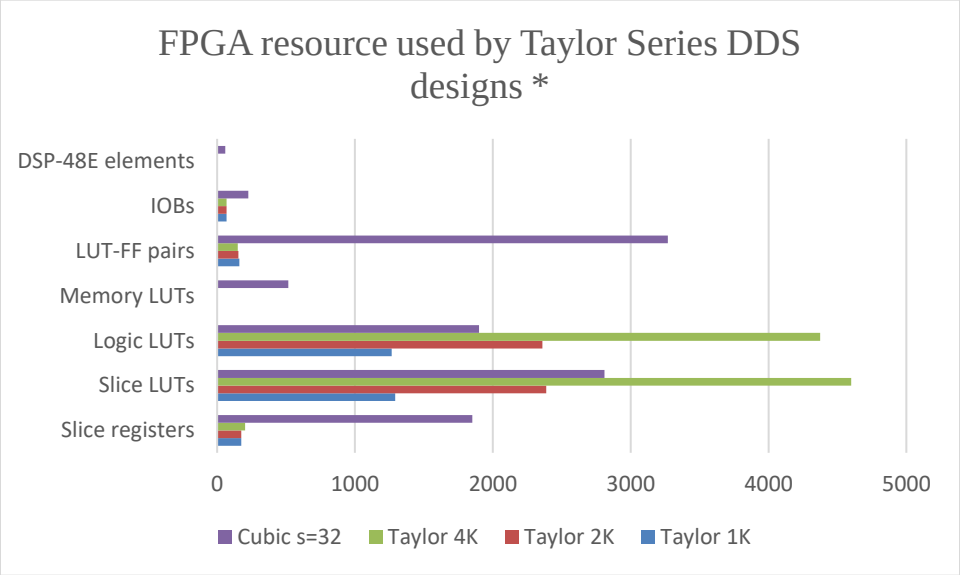


Figure 6.6 FPGA resources consumed by Taylor series DDS (N=1024/2048/4096 and s_e=32)

6.4 Dynamic power comparison for Cubic, LHSC, Taylor Series DDS

A comprehensive summary of power dissipation of various DDS designs discussed so far in this chapter is presented in Figure 6.7.

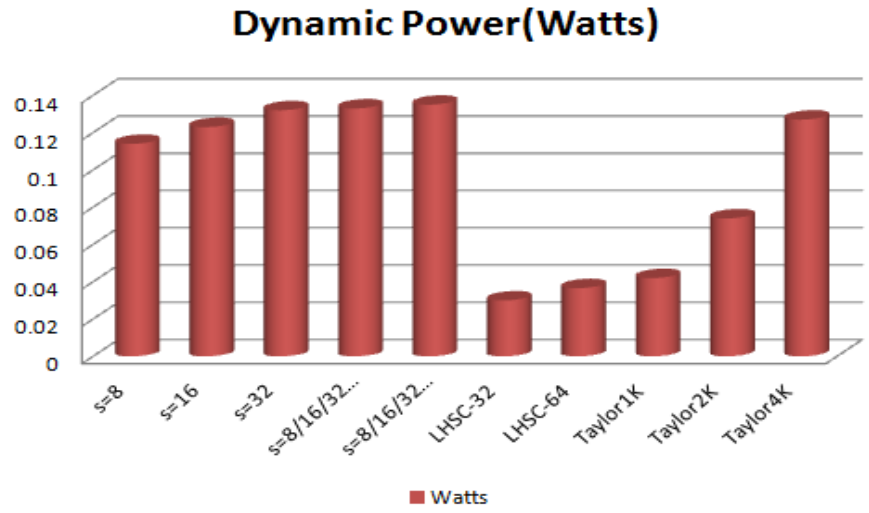


Figure 6.7 Comparison of Dynamic Power Dissipation of various DDS designs

Likewise, SFDR performance of various DDS designs is presented in Figure 6.8.

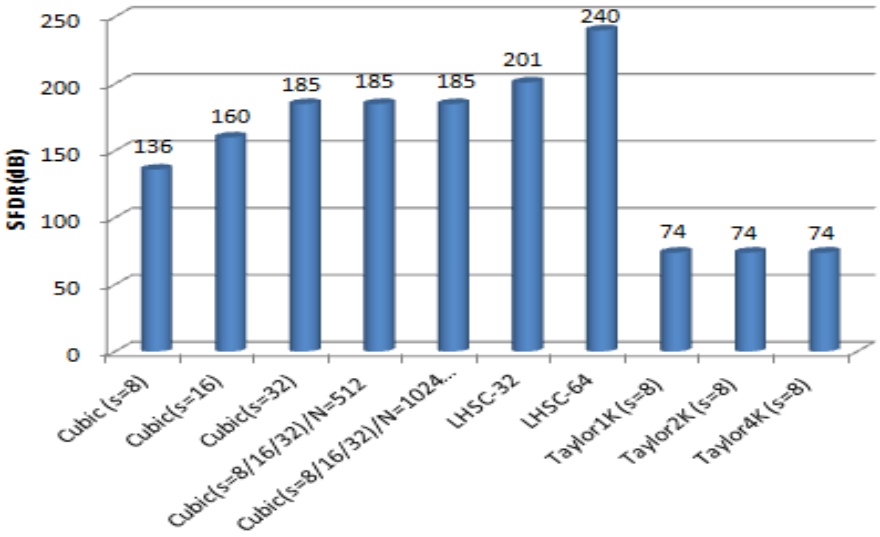


Figure 6.8 Comparison of SFDR of various DDS designs

From the results of Figures 6.7 and 6.8, it can be concluded that the LHSC DDS design with $s = 64$ offers the highest achievable SFDR (240dB) with a power budget that is about 25% that of cubic polynomial based DDS with $s = 32$. An additional observation is that the switchable cubic polynomial based DDS with $N = 512$ samples/segment offers the additional flexibility to achieve a variable SFDR without having to have three separate DDS designs- one for each value of SFDR and an additional power budget. Taylor Series DDS has a low SFDR of 74dB.

6.5 FPGA implementation for the Hartley suppressor

The Sysgen™ model of the Hartley image suppressor (using Virtex-6 FPGA) using only FIR filters for LPF portion is shown in Figure 6.9. In Figure 6.9 the 90-degree phase shifter has been implemented using a FIR compiler block, which is available from the Sysgen™ toolset. Figure 6.9 includes Sysgen™ model of the Hilbert phase shifter, which has been implemented both using eighth-order IIR filters and thirtieth-order FIR filters. But, the IIR filter implementation tends to consume much less power for comparable SFDR. The difference in power dissipation has been

explained in Chapter 3. The usage of IIR filters reduces the power dissipation from 445mW to 55mW due to reduction in order from 30th order FIR to 8th order IIR for the low-pass filters.

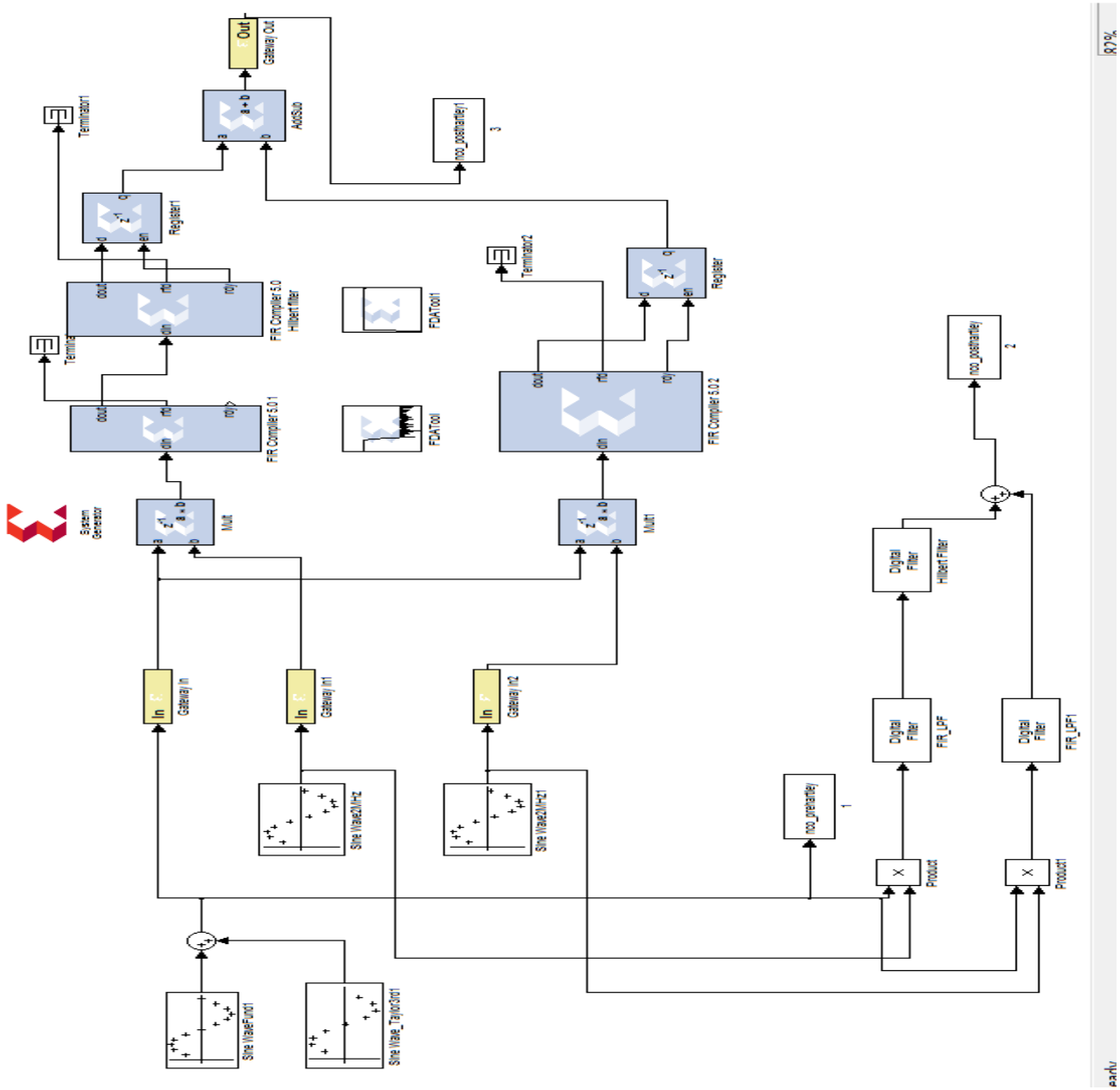


Figure 6.9 FPGA implementation of a Hartley suppressor using only FIR filters

This concludes the FPGA implementation section. The comparative power between a FIR and IIR implementation has already been presented in Table 3.3 of Chapter 3.

6.6 Summary of Chapter

This chapter has presented the FPGA implementation of the cubic DDS, quartic DDS, LHSC DDS and Taylor-series DDS. The dynamic power and FPGA resource requirements for various DDS designs have been discussed as well. The switchable cubic DDS design exhibits a SFDR of 136 dB for 8 segments. When the number of segments 's_e' is increased to 16, SFDR of the the cubic DDS is 160 dB. The cubic DDS design features a SFDR of 160 dB for $\boldsymbol{s_e}$=16 and it shows the highest SFDR of 180 dB for $\boldsymbol{s_e} = 32$.

The LHSC DDS design proposed in this thesis uses a three-stage pipeline instead of a five-stage pipeline used in cubic DDS. For LHSC DDS with $\boldsymbol{s_e} = 32$ with 512 samples/segment, the dynamic power is reduced from 122 mW for the cubic DDS to 23mW for the LHSC DDS. SFDR of cubic polynomial DDS ($\boldsymbol{s_e} = 32$) is 185 dB while that of LHSC DDS with ($\boldsymbol{s_e} = 32$) is 201 dB. The LHSC DDS with $\boldsymbol{s_e} = 64$ exhibits a SFDR of 210 dB. The dynamic power for LHSC DDS design with $\boldsymbol{s_e} = 64$ is 22% higher than the corresponding LHSC DDS with $\boldsymbol{s_e} = 32$. It is observed that the dynamic power dissipation is increased by 150 % from 114 mW (for cubic polynomial DDS with $\boldsymbol{s_e} = 8$) to 287 mW (for Quartic DDS with $\boldsymbol{s_e} = 8$). The additional observation is that the switchable cubic polynomial based DDS with $N = 512$ samples/segment offers the additional flexibility to achieve variable SFDR without having to have three separate DDS designs one for each value of SFDR and additional power budget. For $\boldsymbol{s_e} = 8$, the additional 40 dB increase in SFDR (from 136 dB to 176 dB) of a quartic DDS over a cubic polynomial DDS must be weighed against the higher power dissipation. An additional observation is that the switchable cubic polynomial based DDS with $N = 512$ samples/segment offers an additional flexibility to achieve a variable SFDR without having to create three separate DDS designs for each value of SFDR and an additional power budget. The Taylor Series DDS with $\boldsymbol{s_e}$ =8 has a low SFDR of 74 dB.

Chapter 7: Conclusions and Suggestions for Future Research

This chapter aims at a summary of the research presented in this thesis, the arrived conclusions, and the inferences derived through a combination involving an analytical formulation and simulation results. This chapter also proposes suggestions for future research work to further the envisaged orientation or scope of the research presented in this thesis.

7.1 Conclusions

A detailed explanation on the inferences and conclusions derived through the analytical studies and the results of simulation pertaining to DDS, dithering and PLL are presented in this section.

7.1.1 Direct Digital Synthesis

This thesis introduces the basic block structure of the DDS and introduces the concepts behind Taylor series-based DDS, cubic polynomial based DDS, LHSC DDS and quartic DDS. It also defines the common performance specifications for a DDS such as MAE, SFDR, SNR, latency and throughput. In addition, a discussion on the existing and proposed DDS structures is also presented in the thesis.

A new configuration of Taylor series-based DDS has been proposed in this thesis and patented. The new configuration replaces three ROMs, as well as a multiplier and adder with four ROMs and one four-input adder. The proposed architecture improves the throughput and reduces the dynamic power by eliminating multipliers through the usage of additional stages to a pipeline.

A DDS design called LHSC DDS has been proposed with either 32 or 64 segments per quadrant. LHSC DDS computes the sinusoid value using a linear interpolation. The key advantage of LHSC DDS over a cubic polynomial DDS is that it requires a single multiplier instead of three multipliers (less than 1/3 the power) and a pipeline depth of three stages instead of a five-stage deep pipeline for a cubic polynomial DDS. It produces comparable SFDR for a fraction of power and it features lower latency than the cubic DDS. The simulations confirm that the LHSC DDS with 32 segments produces a SFDR of 185 dB with a relative reduction of 80% of the dynamic power as compared to a traditional cubic polynomial based DDS with 32 segments, which has a maximum SFDR of 185 dB.

The quartic DDS proposed in this thesis has an additional stage to generate a six-stage pipeline, which is one stage more than the cubic polynomial based DDS has, and it has a low MAE of 9×10^{-6}. An analytical formulation to derive closed form expressions for these integrals, which are used to compute the SFDR of quartic DDS, has been presented in this thesis, and such a closed-form representation appears to have not been reported in the literature.

Two schemes for phase shift compensation in a DDS-DAC-PLL have been explored to compensate this phase shift. The first scheme is an analog RC filter phase compensator placed immediately next to the output of the DAC block. The second scheme features a digital phase compensator. which receives a discrete input from the DDS, compensates the phase shift both due to the DAC and the PLL.

With the analog phase compensator, a phase compensation of up to 28^{o} has been demonstrated. The proposed analog compensator produces an overshoot of 143% in response to a unit step input. A three-stage digital phase compensator, which comprises three cascaded IIR filters (placed before the DAC), has been proposed. This can compensate the phase shift introduced by both the DAC and second order PLL. Phase shift up to -105^{o} and a settling time of 142 ns have been considered. For a three-stage compensator, it is observed that a step input produces a large overshoot of 186%.

7.1.2 Hartley Spur Suppressor and Dithering Scheme

Conventional dithering schemes facilitate the realization of spur suppression (improvement in SFDR) at the undesirable feature of rise in noise floor of the dithered output. The focus of this thesis is on approaches, which would improve SFDR without raising the noise floor around the

fundamental or center frequency of operation of the DDS. An alternative spur suppression scheme using a Hartley suppressor has been explored.

A Hartley spur suppressor has been proposed for the DDS to improve SFDR without degrading the noise floor. The SFDR of Taylor Series based DDS is improved by 45 dB with Hartley spur suppression scheme characterized by a power dissipation of 55 mW.

A spur suppressor scheme using LMS filters (LMS-SIC) has also proposed in this thesis. The LMS-SIC improves SFDR from 74dB to 120 dB. The RLS based spur suppression (RLS-SIC) has been proposed as an improvement over the LMS-SIC. The RLS based compensator featuring a weight vector of length 32 improves the SFDR of a Taylor Series DDS from 74 dB to almost 190 dB.

7.1.3 Phase Lock Loop

This thesis has adequately addressed the design, analysis and simulation of PLL. The primary focus of the thesis is on the DDS-PLL combination. The DDS - PLL combination has a DDS cascaded with a DAC and a PLL, which can be of any order. This thesis has presented the analytical formulations and simulation results on second-order PLL, leading to multiple new results. The stability of PLL as measured by its phase margin is addressed in this thesis. The speed of response as measured by lock time is another measure of performance addressed in this thesis. Phase noise at the output of PLL is due to a combination of four noise sources is yet another measure of PLL performance. A lower phase noise is a critical requirement for a DDS-PLL system as explained in chapters 1 and 2.

Based on the numerous analytical formulations presented in the thesis, it is concluded that to achieve a lower lock time, there is a need for higher natural frequency, higher sensitivity of VCO and greater PM. A closed form expression has been derived for the derivative of the lock time with respect to the damping coefficient.

New analytical expressions relating the jitter variance in term of PM for a second-order PLL have been derived. This thesis presents simulation results on jitter variance versus PM for a range of natural frequencies (therefore loop BW) of a second order PLL.

A new closed from expression relating the angle between the two complex poles to its PM of a second-order PLL has been derived. It is observed that the angle between the two complex poles reduces rapidly as the PM is increased beyond 60^{o}.

This thesis presents an analysis on the characteristic properties of the roots of a third order PLL featuring a charge pump. In a combined system featuring both DDS and PLL, the PLL is usually designed to multiply the frequency of the DDS. It is desirable that the combined DDS-PLL combination exhibits the features of low power, a small frequency step size and a high spectral purity in the waveform at the output of the PLL.

Expressions have been derived to relate the three real poles of a third order PLL to the half radius and center of Vieta's circle. These expressions relate the geometry of circle to the PLL parameters. Such expressions have not been reported in the open literature.

This thesis presents analytical formulations that relate the PM of a third order PLL with the values of the three real poles of the PLL. The derived formulation expresses the capacitance ratio as a function of the poles. Other formulation presented in the thesis relate the time constant of the loop filter to the location of the poles. Such expressions are not available in the open literature.

An analysis of third order PLL with two real poles or three real poles have been dealt with an analytical formulation linking its performance to the location of the poles. For a case where a third order PLL has three real and equal poles, a new expression has been derived for the step response. Such an expression has not been described in open literature.

There are two requirements to have a better waveform generated by a DDS-PLL combination. The first requirement is the spurs generated by the PLL itself must be of very low magnitude. If the spurs are very small in magnitude a high SFDR is achieved at the PLL output. The second requirement being a lower phase noise or equivalently low Jitter variance at the output of PLL. A higher spur gain must be avoided for the two common types of spur, namely leakage spur and mismatch spur in a PLL. An analytical formulation has been presented in the thesis to relate the spur gain to the locations of the three poles of a third-order PLL.

This thesis presents the derivation of new expressions to relate the jitter variance at the output of a third-order PLL with the three roots of its CE. Such expressions appear to have not been previously addressed in the open literature.

This thesis also presents an analysis for the derivation of closed form expressions to relate the one real and two complex poles of a third-order PLL to the parameters of PLL, such as capacitance

ratio and the time constant (τ_1) of the loop filter. These expressions, which appear not to have been addressed in open literature, can be utilized in future work to derive closed form expressions for parameters of PLL, such as lock time and phase noise in term of the poles.

This thesis presents new expressions for the (P_n/P_c) (the ratio of the noise power (P_n) to the carrier power(P_c)) in terms of the loop bandwidth of the third-order PLL, loop bandwidth (ω_c), time constant τ_2 of the loop filter, the capacitance ratio of the loop filter (b_c) and the VCO sensitivity VCO (K_v). Through these four parameters the ratio (P_n/P_c) has been related to the three roots of a third-order PLL.

It has been proven in the thesis that for an ITAE optimal third-order PLL, the loop bandwidth has been related to the natural frequency of the PLL. The resultant PM for a third-order PLL which meets the ITAE optimal criteria, has been derived for the first time.

7.2 Original Contributions of the Thesis

The original contributions of the proposed thesis, which emphasized the research on DDS, Spur suppression schemes and PLL for CR applications are listed in this section.

- A characterization of the variation of PM with the perturbation of settling time of a second-order PLL has been performed for the first time. An important new derivation relates the output phase noise of a second-order PLL with its settling time and the cotangent of its phase margin.
- A new expression for the derivative of the lock time of a second-order PLL with respect to its damping coefficient as a function of its natural frequency or loop bandwidth is derived. A closed form expression is formulated relating the derivative of the lock Time of a second-order PLL with respect to its PM has been presented.
- An equation relating the lock time of a second-order PLL with respect to its loop filter time constant and the PM has been derived for the first time.
- An expression and a curve relating the jitter variance and PM of a Type II second-order PLL has been presented for the first time
- Another expression for the variation of Jitter variance with respect to the PM of a second-order Type I PLL is derived. This expression is accompanied with a second expression that

establishes the relationship for the first time between a derivative of the Jitter variance with respect to PM of a second order PLL

- A derivation for the Nickalls's parameters in terms of the three real poles of a third-order PLL has been derived for the first time. A derivation of the relationship between Vieta's angle and the PM of the third-order PLL has been derived for the first time in a closed-form. This is valid for a third-order PLL with three real roots
- A closed form expression for Spur Gain in terms of three real roots has been derived for the first time. An entirely new expression for the capacitance ratio of a third-order PLL has been derived in terms of Vieta's parameters. An entirely new derivation is formulated to characterize Jitter variance versus overshoot of a third order PLL
- New analytical solutions that relate the PM and the capacitance ratio of a third-order PLL to the locations of the three real poles of the PLL are proposed in this thesis. Derivation of a value for the PM of a third-order PLL, which meets the ITAE criterion, has been derived for the first time
- The ratio of noise power to carrier power of a third-order PLL has been related to the roots of CE of the PLL. Furthermore, the ratio of noise power to carrier power is related to the three real roots and the loop BW. A new expression has been derived for the lock time of third-order PLL in terms of the three real poles.

7.3 Suggestions for Future Research

Based on the research presented in the earlier chapters of the thesis, this section presents a potential scope for further additional research on DDS and PLL.

7.3.1 Direct Digital Synthesis

The analysis of chapter 3 of this thesis can be extended for quartic DDS so that a closed form expression can be derived for the SFDR of a quartic DDS in terms of the number of segments. The results on quartic DDS which have been derived in Chapter 3, can be further extended to a quantic DDS (fifth-order polynomial DDS).

One important direction for future work would be to explore a HW implementation of a 32-segment cubic or quartic polynomial DDS cascaded with an IIR filter-based phase shift compensator. The IIR phase compensator will be able to compensate the phase shift due to the DAC and the PLL.

Another aspect of future research potential would be to combine error feedback of DDS [Vankka, 2000] with a phase shift correction circuit after the DDS. An adaptive phase compensation scheme would be worthy of exploration.

7.3.2 Dithering Scheme and Hartley Spur Suppressor

The Hartley spur suppression circuit described in Chapter 4 of the thesis improves SFDR of Taylor series-based DDS by suppressing a single spur without degrading the noise floor. An avenue for future research can be a provision for extensions of Hartley spur suppression, which suppress more than one significant spur without increasing dynamic power or latency.

An extension of the conventional Hartley spur suppressor can be formulated combining the error feedback of DDS proposed in [Vankka, 2000] with a Hartley spur suppressor.

7.3.3 Phase Lock Loop

From the research perspective, it will be worthwhile to explore the extension of the analysis presented in Chapter 5 of the thesis to derive a closed form expression for the SFDR of a cubic polynomial DDS driving a ZOH DAC followed by a second order PLL. When spurs are generated within the second order PLL, one must have a means of trading of spur levels with PM of PLL. PLLs have been proposed to filter the spurs of DDS.

An expression for spur values has been provided by [He, 2007]. One can possibly consider it a worthwhile research exercise to extend the analysis presented in this thesis to directly relate the theoretical spur magnitude as derived by [He, 2007] to the locations of one real and 2 complex poles of a third-order PLL.

Jitter variance of a third-order PLL in terms of VCO parameters has been expressed by [Mansuri, 2 002]. It would be a good research contribution to analytically arrive at the expression of the Jitter

variance and facilitate their computation in terms of the parameters of Vieta's circle for real poles. It would be highly useful to relate the hyperbolic expressions for m , b_c and τ_2 derived in chapter 5 to the practical parameters such as jitter variance, lock time and spur gain, as derived in [Banerjee, 2006] or alternatively in [He, 2007]. The practical significance of this suggestion would facilitate the designers' efforts to relate the small perturbations in the values of a real and complex poles to actual changes of PLL parameters such a spur gain, lock time and step response.

Further analytical work can be attempted to extend the formulations of this thesis to derive expressions for SFDR and SNR of the output waveform of a third-order PLL in terms of locations of three real poles.

A study on phase noise optimized VCO design combined with optimized pole placement of PLL will be of great utility so that the resulting PLL has the desirable features of low lock time combined with low phase noise of VCO.

Appendix A

Appendix A is divided into two parts. Part A.1 illustrates the steps necessary to compute the polynomial coefficients of any DDS (using the model dues to [De Caro and Strollo, 2005]) when the SFDR is known and the maximal SFDR is achieved. The first part comprises equation (A.1) to (A.23) where given a value of SFDR the corresponding coefficients of an optimal Cubic DDS are computed.

The second part (A.2) (comprising of Equations (A.24) to (A.39)) illustrates the reverse computation the Fourier coefficients ($b(n)$) and ($b(1)$) are computed when the set of coefficients $y()$ ... are known.

There are two classes of problems where one can use the analysis proposed by [De Caro and Strollo, 2005]. The first class of problems (described in part A.1) deals with the computation of the coefficients of polynomial to meet a specified SFDR. The second class of problem is for the computation of SFDR from the given coefficients of an interpolating polynomial (described in part A.2). In either case the intermediate coefficients $\alpha_k, \beta_k, \gamma_k, \delta_k$ must be computed. Also, the values $g(n), h(n), l(n)\ and\ m(n)$ must be computed.

A.1 Computation of the coefficients when the SFDR is known

SFDR can be written in terms of the number of segments as

$$SFDR = 20\log_{10}\left(\frac{5 + 768{s_e}^2 + 5120{s_e}^4}{3}\right) = 20log_{10}\left(\frac{b_1}{\max(b_n)}\right) \quad \text{(A.1)}$$

In Equation (A.1) b_1 is the fundamental Fourier coefficient $\max(b_n)$ is the maximum of all harmonic produced by the DDS. s_e is the number of segments per quadrant. Equation A.1 computes the ratio of the fundamental to the highest harmonic when the number of segments per quadrant (s_e) is known.

$$g(1) = -B\frac{\pi^2(1 + 40\ s_e^2)}{8s_e^2(5 + 768\ s_e^2 + 5120\ s_e^4)} \quad \text{(A.2)}$$

$$h(1) = -B\frac{\pi^2(11 + 240s_e^2 - 2176s_e^4)}{64\ s_e^2(5 + 768s_e^2 + 5120s_e^4)} \quad \text{(A.3)}$$

$$l(1) = -B\frac{\pi^3(-5 + 80s_e^2 + 4224\, s_e^4)}{128s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{A.4}$$

$$m(1) = -B\frac{\pi^4(3 - 200s_e^2 - 128s_e^4 + 40960\, s_e^6)}{1536s_e^2(5 + 768s_e^2 + 5120s_e^4)} \tag{A.5}$$

In Equations (A.2 to A.5), the value B corresponds to the magnitude of the output waveform of the DDS. The periodicity of the coefficients has been covered in [De Caro and Strollo, 2005], the periodicity is expressed in Equations (A.6) to (A.9)

$$g(1) = g(4s_e - 1) \tag{A.6}$$

$$h(1) = -h(4s_e - 1) \tag{A.7}$$

$$l(1) = l(4s_e - 1) \tag{A.8}$$

$$m(1) = -m(4s_e - 1) \tag{A.9}$$

Let us define two square matrices T_1 and T_2 are of size s_eXs_e [De Caro and Strollo, 2005]. One matrix (T_1) is constructed using cosine functions and the other matrix (T_2) is constructed using sine functions. Matrix T_1 is used to compute the coefficients α and γ and matrix T_2 is used to compute the coefficients β and δ. Matrix T_1 is expressed in Equation (A.10) as

$$[T_1] = \begin{bmatrix} cos\left(\frac{0\pi}{2s_e}\right) & cos\left(\frac{\pi}{2s_e}\right) & \cdots & cos\left(\frac{(s_e-1)\pi}{2s_e}\right) \\ cos\left(\frac{0}{2s_e}\right) & cos\left(\frac{3\pi}{2s_e}\right) & \cdots & cos\left(\frac{3(s_e-1)\pi}{2s_e}\right) \\ \vdots & \vdots & \vdots & \vdots \\ cos\left(\frac{0}{2s_e}\right) & cos\left(\frac{(2s_e-1)\pi}{2s_e}\right) & \cdots & cos\left(\frac{(s_e-1)(2s_e-1)\pi}{2s_e}\right) \end{bmatrix} \tag{A.10}$$

Matrix T_2 is expressed in Equation (A.11) as

$$[T_2] = \begin{bmatrix} sin\left(\frac{\pi}{2s_e}\right) & sin\left(\frac{2\pi}{2s_e}\right) & \cdots & sin\left(\frac{s_e\pi}{2s_e}\right) \\ sin\left(\frac{3\pi}{2s_e}\right) & sin\left(\frac{6\pi}{2s_e}\right) & \cdots & sin\left(\frac{3s_e\pi}{2s_e}\right) \\ \vdots & \vdots & \vdots & \vdots \\ sin\left(\frac{(2s_e-1)\pi}{2s_e}\right) & sin\left(\frac{2(2s_e-1)\pi}{2s_e}\right) & \cdots & sin\left(\frac{s_e(2s_e-1)\pi}{2s_e}\right) \end{bmatrix} \quad \text{(A.11)}$$

Since the coefficients $g(n), h(n), l(n)\ and\ m(n)$ vanish for n greater than 1 up to $n = 2s_e - 1$[De Caro and Strollo, 2005], it is easy to form a vector for $g(), h(), l()\ and\ m()$ by only substituting the value of the first element of the respective vector and leaving the rest as 0.

Since the coefficients $g(1), h(1), l(1)$ and $m(1)$ are directly connected to the SFDR through the Equations (A.2 and A.5). The Equations (A.12 to A.17) complete the second part of the computations and allow the computation of the intermediate coefficient vectors $\alpha()$, $\beta(), \gamma()$ and $\delta()$ to the SFDR.

Once the coefficients $g(1), h(1), l(1)$ and $m(1)$ are known one can construct a corresponding vector of length s_e which has the coefficient(one of $g(1), h(1), l(1)$ and $m(1)$) as the first element and the rest of the rows are zero. Once the coefficients vectors $g(.), h(.), l(.)\ and\ m(.)$ are computed the intermediate vectors $\alpha()$ can be expressed [De Caro and Strollo, 2005] in the form of a matrix inversion as

$$\begin{bmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \vdots \\ \alpha_{s_e} \end{bmatrix} = [T_1]^{-1} \begin{bmatrix} g(1) \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \text{(A.12)}$$

The β coefficients are computed in a vector form by the following equation,

$$\begin{bmatrix} \beta_1 \\ \beta_2 \\ \beta_3 \\ \vdots \\ \beta_{s_e} \end{bmatrix} = [T_2]^{-1} \begin{bmatrix} h(1) \\ 0 \\ 0 \\ \vdots \\ 0 \end{bmatrix} \quad \text{(A.13)}$$

Now the intermediate vector γ can be computed as

$$\begin{bmatrix}\gamma_1\\ \gamma_2\\ \gamma_3\\ \vdots\\ \gamma_{s_e}\end{bmatrix}=[T_1]^{-1}\begin{bmatrix}l(1)\\ 0\\ 0\\ \vdots\\ 0\end{bmatrix} \quad \text{(A.14)}$$

The intermediate vectors δ are computed by the following operation

$$\begin{bmatrix}\delta_1\\ \delta_2\\ \delta_3\\ \vdots\\ \delta_{s_e}\end{bmatrix}=[T_2]^{-1}\begin{bmatrix}m(1)\\ 0\\ 0\\ \vdots\\ 0\end{bmatrix} \quad \text{(A.15)}$$

Equations (A.12, A.13, A.14 and A.15) form a group of four equations which constitute the second step of the derivations by [De Caro and Strollo, 2005] which relate the optimal values of $g(1), h(1), l(1)$ and $m(1)$ to the intermediate vectors $\alpha(),\ \beta(), \gamma()$ and $\delta()$ through the two matrices T_1 and T_2.

In the third and final step one must utilize the coefficients $\alpha_k, \beta_k, \gamma_k \ and \ \delta_k$ to compute the coefficients of the cubic polynomial $y_k, m_k, p_k \ and \ q_k$. These coeffcients are part of the polynomial function $V_k(x)$ defined through Equation (A.1). The coefficients $y_k, m_k, p_k \ and \ q_k$ are determined as described in Equations (A.16) and (A.23). The coefficients are computed in a sequential manner.

The first step the coefficients that must be computed are q_k,

$$q_s = \gamma_k \ for \ k = s_e \quad \text{(A.16)}$$

$$q_k = -\gamma_k + \ q_{k+1} \ for \ \ k = s_e - 1, s_e - 2, \dots, 1 \quad \text{(A.17)}$$

In the second step the quadratic coefficient p_k must be computed

$$p_1 = \gamma_k \ \ for \ k = 0 \quad \text{(A.18)}$$

$$p_{k+1} = \gamma_k + \ p_k + \frac{3q_k}{s_e} for \ k = 1,2, \dots, s_e - 1 \quad \text{(A.19)}$$

In the third step the linear coefficients of the power of x m_k must be computed.

$$m_s = \beta_s + \frac{p_k}{s_e} + \frac{w_k}{s_e^2} \ for \ k = s_e \quad \text{(A.20)}$$

$$m_{k+1} = \beta_k \quad + \ m_k + \frac{2p_k}{s_e} + \frac{3q_k}{s_e^2} \ for \ k = 1,2, \dots, s_e - 1 \quad \text{(A.21)}$$

Finally, in the fourth step the constant coefficients y_k must be computed.

$$y_1 = \alpha_k \qquad for \ k = 0 \quad \text{(A.22)}$$

$$y_{k+1} = \alpha_k \quad + y_k + \frac{m_k}{s_e} + \frac{p_k}{s_e^2} + \frac{q_k}{s_e^3} \; s_e^2 \, s_e^3 for \; k = 1,2, \dots, s_e - 1 \qquad \text{(A.23)}$$

The significance of the procedure outlined from Equations (A.1 to A.23) must be highlighted. Given a specified SFDR value, using (A.2 to A.5) the corresponding polynomial coefficients $(g(n), h(n), l(n) \; and \; m(n))$ are calculated. Equations (A.12 to A.15) form the second link in the chain to compute intermediate vectors $\alpha()$, $\beta(), \gamma()$ and $\delta()$. Equations (A.16 to A.23) are significant as they complete the third link in the chain connecting the intermediate coefficient vectors $\alpha()$, $\beta(), \gamma()$ and $\delta()$ which are function of the targeted SFDR and the number of segments to actual polynomial coefficients which are computed per segment. The first, second and third links allow the computation of the polynomial coefficients for a maximal SFDR DDS with a given specified SFDR value. That serves the necessity of describing the complete [De Caro and Strollo, 2005] procedure in this section.

A.2 Computation of the Fourier coefficients when the polynomial coefficients are known

This is the second flow of computations in this thesis. In this flow the SFDR is not it must be calculated when the polynomial coefficients are known. Its subdivided into three parts -Parts I through III.

A2.1 Producing the coefficients y_k, m_k, p_k, q_k

In the first step the coefficients y_k, m_k, p_k, q_k are input. They form the input to the rest of the computation. For a Taylor Series DDS, the coefficients are computed in Equation (3. 55) and (3.56). For a LHSC DDS the coefficients are computed using Equations (3.72) through (3.74). For LHSC DDS only the coefficients y_k, m_k are nonzero so the computation is simplified.

y_k= constant coefficient for segment k (power of $z_{j,k}^0$)

m_k= Linear coefficient for segment k (power of $z_{j,k}^1$)

p_k= Quadratic coefficient for segment k (power of $z_{j,k}^2$)

q_k= cubic coefficient for segment k (power of $z_{j,k}^3$)

A2.2 Computation of intermediate coefficients $\alpha_k, \beta_k, \gamma_k, \delta_k$

Now since the coefficients of the DDS polynomial have been calculated one must compute. The intermediate coefficients $\alpha_k, \beta_k, \gamma_k, \delta_k$ are computed using Equations (2.77a and 2.77b)(A.24 to A.31) to Equations (2.80a to 2.80b)(A.xx to A.yy)

$$\gamma_k = p_{k+1} - p_k - \frac{3q}{s_e} \qquad k = 1,2,\dots,s_e - 1 \tag{A.24}$$

$$\gamma_k = p_1 \qquad k = 0 \tag{A.25}$$

$$\delta_k = q_{k+1} - q_k \; k = 1,2,\dots,s_e - 1 \tag{A.26}$$

$$\delta_k = -q_{s_e} \; k = s_e \tag{A.27}$$

The next two coefficients can be written as,

$$\alpha_k = y_{k+1} - y_k - \frac{m_k}{s_e} - \frac{p_k}{s_e^2} - \frac{q_k}{s_e^3} \;\; k = 1,2,,\dots,s_e - 1 \tag{A.28}$$

$$\alpha_0 = y_1 \quad k = 0 \tag{A.29}$$

$$\beta_k = m_{k+1} - m_k - \frac{2p_k}{s_e} - \frac{q_k}{s_e^2} \quad k = 1,2,,\dots,s_e - 1 \tag{A.30}$$

$$\beta_s = -m_{s_e} - \frac{2p_{s_e}}{s_e} - \frac{q_{s_e}}{{s_e}^2} \;\; k = s_e \tag{A.31}$$

Equations (A.24 to A.31) are used to compute the intermediate coefficients $\alpha(.), \beta(.), \gamma(.), \delta(.)$. In the final part (A2.3), the coefficients *g(n)*, *h(n)*, *l(n)* and *m(n)* are computed by matrix-vector multiplications.

A2.3 Computation of Intermediate coefficients $\boldsymbol{h(n), g(n), l(n)}$ and $\boldsymbol{m(n)}$

In the third part the coefficients computed in Part I are used to form four vectors $\hat{\alpha}, \hat{\beta}, \hat{\gamma}, \hat{\delta}$ using a matrix multiplication as expressed in Equations (A.32) to (A.35).

$$M_1[\sin(k, s_e)]\hat{\beta} = h(n) \tag{A.32}$$

$$M_2[\cos(k, s_e)]\hat{\alpha} = g(n) \tag{A.33}$$

$$M_2[\cos(k, s_e)]\hat{\gamma} = l(n) \tag{A.34}$$

$$M_1[\sin(k, s_e)]\hat{\delta} = m(n) \tag{A.35}$$

The matrix $M[\cos(k, s_e)]$ can be expressed as

$$M_2[\cos(k, s_e)] = \begin{bmatrix} cos\left(\frac{(0)1\pi}{2s_e}\right) & cos\left(\frac{(1)1\pi}{2s_e}\right) & \cdots & cos\left(\frac{(s_e-1)1\pi}{2s_e}\right) \\ cos\left(\frac{(0)2\pi}{2s_e}\right) & cos\left(\frac{(1)2\pi}{2s_e}\right) & \cdots & cos\left(\frac{(s_e-1)2\pi}{2s_e}\right) \\ \vdots & \vdots & & \vdots \\ cos\left(\frac{(0)2\pi}{2s_e}\right) & cos\left(\frac{(1)s\pi}{2s_e}\right) & \cdots & cos\left(\frac{(s_e-1)(s_e)2\pi}{2s_e}\right) \end{bmatrix} \quad \text{(A.36)}$$

Similarly, the matrix $M_1[sin(k, s_e)]$ can be expressed as

$$M_1[\sin(k, s_e)] = \begin{bmatrix} sin\left(\frac{(1)1\pi}{2s_e}\right) & sin\left(\frac{(2)1\pi}{2s_e}\right) & \cdots & sin\left(\frac{(s_e)1\pi}{2s_e}\right) \\ sin\left(\frac{(1)2\pi}{2s_e}\right) & sin\left(\frac{(2)2\pi}{2s_e}\right) & \cdots & sin\left(\frac{(s_e)2\pi}{2s_e}\right) \\ \vdots & \vdots & & \vdots \\ sin\left(\frac{(1)2\pi}{2s_e}\right) & sin\left(\frac{(2)s_e\pi}{2s_e}\right) & \cdots & sin\left(\frac{(s_e)(s_e)2\pi}{2s_e}\right) \end{bmatrix} \quad \text{(A.37)}$$

In the first step all the coefficients are computed. In the second step the corresponding $g(n), h(n), l(n)\ and\ m(n)$ are computed for $n = 1$ and $n = 4s_e + 1$.

A2.4 Computation of SFDR from $h(n), g(n), l(n)$and $m(n)$

The SFDR (in dB) is computed as a ratio of the Fourier coefficients for $n = 1$ (fundamental) and $n = 4s_e + 1$ (highest harmonic). The Fourier coefficients for $n = 1$ and $n = 4s_e + 1$ are computed through Equation (A.38).

The Fourier coefficients for the cubic DDS with ($s = 8$), $b(n)$ are related to the intermediate coefficients $g(n), h(n), l(n)\ and\ m(n)$ (computed by A.32 through A.35) by the following equation.

$$b(n) = \frac{4g(n)}{n\pi} - \frac{8h(n)}{n^2\pi^2} - \frac{32l(n)}{n^3\pi^3} + \frac{192m(n)}{n^4\pi^4} \quad \text{(A.38)}$$

In Equation (A.38) n is the order of the Fourier coefficient, with $n = 1$ being the fundamental. The unwanted spur with highest magnitude is obtained for $n = 4s_e + 1$. The fundamental b_1 is

computed by substituting $n = 1$ in Equation A.38, the highest spur (b_{4s_e+1}) is computed by substituting $n = 4s_e + 1$

$$SFDR = 20log_{10}\left(\frac{b_1}{b_{4s_e+1}}\right) \tag{A.39}$$

APPENDIX B

Figure B.1 Regions of Phase Noise following [Drucker, 2000]

Figure B.1 illustrates the different regions of an oscillator in [Drucker, 2000] model. The plot is the PSD of phase noise with respect to the logarithm of the offset frequency. In each region, a different physics of phase noise becomes dominant. Since phase noise models are created with (1/offset frequency model) the figure illustrates what the specific region is named such as random walk, flicker FM, white FM… The power of 1/f shows the dominant behavior of phase noise PSD in a specific region.

B.1 Noise Transfer Function (NTF) of noise source of Reference

One must use the Figure 4.7 in Chapter 4 for reference. The NTF of reference source is the same as the standard closed loop transfer function of the PLL. The forward path transfer function of PLL ($G(s)$) is the product of the transfer functions of PFD, VCO and loop filter and can be written as,

$$G(s) = K_\phi \frac{K_v}{s} \frac{1}{(1+\tau s)} \tag{B.1}$$

The function $G(s)$is the cascaded Transfer function of the VCO ($\frac{K_v}{s}$), PFD (K_ϕ) and Loop filter ($\frac{1}{(1+\tau s)}$).

The feedback path transfer function can be written as

$$H = \frac{1}{N} \tag{B.2}$$

In Equation (B.2) N is the PLL divider ratio in Figure 4.7.

Substituting the transfer functions of forward and feedback paths from Equations (5.22 and 5.23), one obtains the NTF of the reference source , $W(s)$ and is written as

$$W(s) = \frac{G(s)}{1 + G(s)H(s)} = \frac{K}{\tau(s^2 + 2\zeta\omega_n s + \omega_n^2)} \tag{B.3}$$

In Equation (B.3), the natural frequency $\omega_n$and damping coefficient ζ have the same meanings as in Equation (5.3). Equation (B.3) represents the NTF corresponding to the reference source. It is the same as the transfer function of the PLL. From Equation (B.3), the natural frequency $\omega_n$and damping coefficient ζ are written in terms of the time constant (τ) of the LPF, the divider ratio N and K, the product of sensitivities of VCO and phase detector.

The natural frequency of the PLL can be written as

$$\omega_n = \sqrt{\frac{K}{\tau N}} \tag{B.4}$$

The damping coefficient can be written in terms of K, time constant and divide ratio as

$$\zeta = \frac{\sqrt{N}}{2\sqrt{K\tau}} \tag{B.5}$$

Equation (B.4) expresses the relationship between the natural frequency (ω_n), sensitivity (K) of forward path and the feedback path divider N. The relationship between the damping coefficient, the sensitivity (K) of forward path, time constant (τ) of the loop filter and the feedback path divider N is expressed equation (B.5).

B.2 Noise Transfer Function (NTF) of the noise source of VCO

One must use Figure 4.8 as a reference to compute the NTF. ($S_{VCO}(s)$) is the noise PSD of the noise source of the VCO acts as an input to the system (Figure (4.8)). The response at the DAC-PLL output ($Y_{DAC\_PLL\_VCO}(s)$) is written in terms of the input as

$$\frac{Y_{DAC\_PLL\_VCO}(s)}{S_{VCO}(s)} = \frac{G(s)}{1 + G(s)H(s)} \tag{B.6}$$

In Equation (B.6), $G(s) = 1$ is the transfer function of forward path

$$H(s) = \frac{K}{sN(1 + \tau s)} \tag{B.7}$$

$H(s)$ is the Transfer Function of the Feedback path. $Q(s)$ = NTF of noise source of VCO (illustrated with the small dotted arrow in Figure 4.8). Substituting the values of $G(s)$ and $H(s)$ in Equation (B.6), a closed form expression for NTF is obtained as

$$Q(s) = \frac{s(1 + s\tau)}{\tau(s^2 + s\frac{1}{\tau} + \frac{K}{N\tau})} \tag{B.8}$$

Substituting the PLL transfer function ($W(s)$) the NTF of the noise source in the VCO can be written in compact form as

$$Q(s) = \frac{W(s)s(1 + \tau s)}{K} \tag{B.9}$$

B.3 Noise Transfer Function (NTF) of noise source of the Loop filter

One must use Figure 4.9 as a reference to compute the NTF. In Figure 4.9, the assumed PSD of Loop Filter is marked as $S_{FILTER}(s)$. One assumes this as the primary input to the system and computes the response at the output of DAC-PLL ($Y_{DAC\_PLL\_FILT}(s)$). The output can be written in terms of the input as

$$Y_{DAC\_PLL\_FILT}(s) = \frac{K_v}{s}H(s)E(s) + \frac{K_v}{s}H(s)S_{FILTER}(s) \tag{B.10}$$

In Equation (B.10) $E(s)$ is the error signal in the PLL (at the output of Phase detector)
After further substitution of $H(s)$ in Equation (B.9) and further simplification, the NTF of Loop Filter, ($\Psi(s)$) is defined as

$$\Psi(s) = \frac{Y_{DAC\_PLL\_FILT}(s)}{S_{FILTER}(s)} = \frac{K}{K_\phi \tau} \frac{1}{(s^2 + \frac{1}{\tau}s + \frac{K}{n\tau})} \tag{B.11}$$

Substituting the transfer function $(W(s))$, the NTF of the VCO noise source can be written in compact form as

$$\Psi(s) = \frac{Y_{DAC\_PLL\_FILT}(s)}{S_{FILTER}(s)} = \frac{W(s)}{K_\phi} \tag{B.12}$$

B.4 Noise Transfer Function (NTF) of source of Divider noise

One must use Figure 4.10 as a reference to compute the NTF. In the noise source of the divider (Figure 4.10), the assumed PSD is marked as $S_{MD}(s)$. One assumes this to be the primary input to the system and computes the response at the DAC-PLL output ($Y_{DAC\_PLL\_DIV}(s)$). The output of the PLL can be written in terms of the input as

$$Y_{DAC\_PLL\_DIV}(s) = -\left(S_{MD}(f) + \frac{Y_{DAC\_PLL\_DIV}(s)}{N}\right)\left(K_p \frac{K_v}{s} H(s)\right) \tag{B.13}$$

In Equation (B.13) $H(s)$ is the Loop filter Transfer Function. $S_{MD}(f)$ is the power spectral density of the source of the divider noise. By further simplification, the NTF for the divider, ($\Phi(s)$) can be written as

$$\Phi(s) = \frac{Y_{DAC\_PLL\_DIV}(s)}{S_{FILTER}(s)} = -\frac{K}{\tau} \frac{1}{(s^2 + \frac{1}{\tau}s + \frac{K}{n\tau})} \tag{B.14}$$

Inserting the expression with the PLL transfer function in Equation (B.3) into Equation (B.14) one can write an expression for the NTF of the source of the Divider noise as

$$\Phi(s) = \frac{Y_{DAC\_PLL\_DIV}(s)}{S_{FILTER}(s)} = -W(s) \tag{B.15}$$

B.5 Lock time directly to tangent of the Phase margin (page 24)

Starting with the Equation for Lock Time the equation B.16 can be derived.

$$T_{lock} = \frac{-ln\left(\frac{tol}{(f2-f1)}\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)}{\zeta\omega_n} \tag{B.16}$$

The numerator in Equation (B.16) can be split into two separate logarithmic terms as

$$T_{lock} = \frac{1}{\zeta\omega_n}\left(-ln\left(\frac{tol}{(f2-f1)}\right) - \ln(\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)})\right) \tag{B.17}$$

By using Equation (4.45) the damping coefficient ζ is expressed in terms of the PM (ϕ) as

$$(sec\phi - tan\phi) = \frac{1}{4\zeta^2} \tag{B.18}$$

In Equation (B.18) the terms $sec\phi, tan\phi$ are replaced by equivalent expressions using $tan\frac{\phi}{2}$. By further simplifying one obtains an expression for ζ in terms of half the PM,

$$\frac{1}{4\zeta^2} = \frac{1-sin\phi}{cos\phi} = \frac{1-\frac{2\,tan\frac{\phi}{2}}{1+\,tan^2\frac{\phi}{2}}}{\frac{1-\,tan^2\frac{\phi}{2}}{1+\,tan^2\frac{\phi}{2}}} = \frac{(1-tan\frac{\phi}{2})^2}{\left(1-\,tan^2\frac{\phi}{2}\right)} = \frac{\left(1-tan\frac{\phi}{2}\right)}{\left(1+tan\frac{\phi}{2}\right)} \tag{B.19}$$

Hence the damping coefficient can be written as

$$4\zeta^2 = \frac{\left(1+tan\frac{\phi}{2}\right)}{\left(1-tan\frac{\phi}{2}\right)} \tag{B.17}$$

Taking square root of Equation (B.17) and retaining only the positive root one obtains

$$\zeta = \frac{1}{2}\sqrt{\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{\left(1-tan\left(\frac{\phi}{2}\right)\right)}} \tag{B.18}$$

Substituting the damping coefficient in Equation (B.17) into Equation (B.15) one obtains

$$T_{lock} = \frac{1}{\frac{\omega_n}{2}\sqrt{\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{\left(1-tan\left(\frac{\phi}{2}\right)\right)}}}\left(\ln\left(1-\frac{\left(1+tan\left(\frac{\phi}{2}\right)\right)}{4\left(1-tan\left(\frac{\phi}{2}\right)\right)}\right)-2\ln\left(\frac{tol}{(f2-f1)}\right)\right) \quad \text{(B.19)}$$

Finally, the expression $\frac{1}{\zeta\omega_n}$ can be easily expressed in terms of the time constant of a second order PLL by substituting the Equations (4.6) and (4.7) respectively. From Equation (4.6)

$$\omega_n = \sqrt{\frac{K_V K_\phi}{\tau}} = \sqrt{\frac{K}{\tau}} = \sqrt{\frac{K}{\tau N}} \quad \text{(B20)}$$

From Equation (4.7) the damping coefficient is written as

$$\zeta = \frac{\sqrt{N}}{2\sqrt{K\tau}} \quad \text{(B.21)}$$

Substituting the results for ζ, ω_n in Equation (B.16) the lock time is written as

$$T_{lock} = \frac{1}{\zeta\omega_n}\left(-ln\left(\frac{tol}{(f2-f1)}\right)-\ln\left(\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)\right)$$

$$T_{lock} = \frac{1}{\frac{\sqrt{N}}{2\sqrt{K\tau}}\sqrt{\frac{K}{\tau N}}}\left(-ln\left(\frac{tol}{(f2-f1)}\right)-\ln\left(\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)\right)$$

$$= 2\tau\left(-ln\left(\frac{tol}{(f2-f1)}\right)-\ln\left(\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)\right) \quad \text{(B.20)}$$

$$= 2\tau\left(-ln(\Gamma)-\ln\left(\frac{\sqrt{1-\zeta^2}}{(1-2R2C2\zeta\omega_n+(R2C2\omega)^2)}\right)\right) \quad \text{(B.21)}$$

B.6 Two additional SFDR plots at different levels of damping coefficient – page 55 of chapter 4

Figure B.2 compares the SFDR at three places firstly at the output the DDS, secondly at the output of the PLL with the Phase Compensator and thirdly at te output of the PLL without and without the Phase compensator.

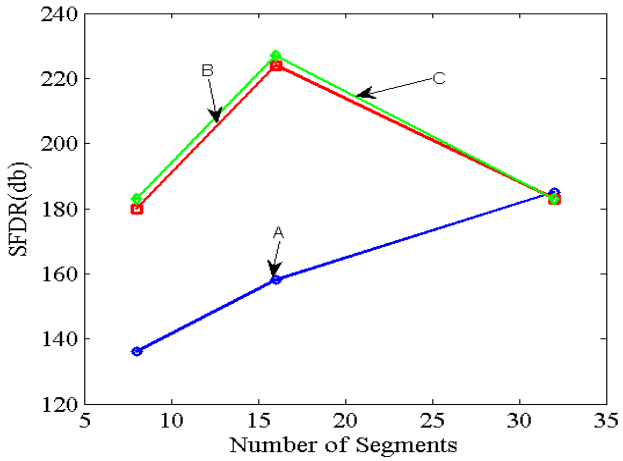


Figure B.2 Variation in SFDR with change in Damping coefficient of PLL ζ =0.22(A = DDS; B = DDS-DAC-PLL_compensated ; C = DDS-DAC-PLL_Uncompensated

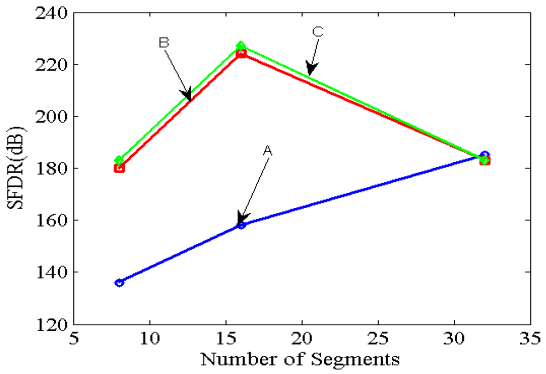


Figure B.3 Variation in SFDR with change in Damping coefficient of PLL ζ =0.45(A = DDS; B = DDS-DAC-PLL_compensated ; C = DDS-DAC-PLL_Uncompensated

Figure B.2 illustrates the variation of SFDR for a low value of damping coefficient. Figure B.3 illustrates the variation of SFDR for a medium level of damping coefficient. It illustrates that the inclusion of PLL improves the SFDR of a DDS-PLL system at low number of segments s=8,16. At higher numbers of segments the SFDR does not change much.

B.7 Derivation of new equation for phase shifter – page 56 of chapter 4

Writing out the analog transfer function of the phase shift compensator in terms of its two parameters(α) and (ω_m) following Equation (4.xx)

$$G(s) = \frac{(1 + \frac{\sqrt{\alpha}}{\omega_m} s)}{\left(\alpha + \frac{\sqrt{\alpha}}{\omega_m} s\right)} \tag{B.21}$$

The relationship between sampling time (Ts) and sampling frequency (f_s) is written as

$$Ts = 1/f_s \tag{B.22}$$

Substituting the Bi-linear transform to convert from s domain to z domain one obtains

$$s = \frac{2}{Ts}\frac{(1 - z^{-1})}{(1 + z^{-1})} = 2fs\frac{(1 - z^{-1})}{(1 + z^{-1})} \tag{B.23}$$

The final transfer function is written as

$$G(s) = \frac{\left(1 + \frac{\sqrt{\alpha}}{\omega_m} s\right)}{\left(\alpha + \frac{\sqrt{\alpha}}{\omega_m} s\right)} = \frac{\left(1 + \frac{\sqrt{\alpha}}{\omega_m} 2fs\frac{(1 - z^{-1})}{(1 + z^{-1})}\right)}{\left(\alpha + \frac{\sqrt{\alpha}}{\omega_m} 2fs\frac{(1 - z^{-1})}{(1 + z^{-1})}\right)} = \frac{\omega_m(1 + z^{-1}) + 2\sqrt{\alpha}\, fs(1 - z^{-1})}{\alpha\omega_m(1 + z^{-1}) + 2\sqrt{\alpha} fs(1 - z^{-1})} \tag{B.24}$$

Collecting the z^{-1} terms and z^0terms from Equation (B.24). The corresponding equivalent transfer function in discrete domain is written as

$$H(z) = \frac{z^{-1}\left(\omega_m - 2f_s\sqrt{\alpha}\right) + \left(\omega_m + 2f_s\sqrt{\alpha}\right)}{z^{-1}\left(\alpha\omega_m - 2f_s\sqrt{\alpha}\right) + \left(\alpha\omega_m + 2f_s\sqrt{\alpha}\right)} \tag{B.25}$$

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