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A Polynomial Analog Baseband Predistorter for Compensation of Wireless Amplifier's Distortion

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Abstract—**This paper presents a new analog polynomial pre-distortion circuit using 350nm CMOS technology to reduce the distortion of power amplifier in wireless communication systems. The proposed pre-distortion circuit uses the polynomial approach. The coefficients of the polynomial are controlled by multiplying them with sufficient digit defined through indirect learning process to provide best practice linearization. Circuit level simulation of the proposed circuit is using Cadence DFW II is used as proof of concept. The simulation set-up comprises a power amplifier, excited with a four carrier GSM signal, pre-distorted by the proposed circuit. Simulation results show that using the pre-distortion circuit the inter-modulation distortion is reduced on average by 16 dB.**

Fig. 1. Combination of predistorter and power amplifier (a): Predistorter (PD) and power amplifier (PA) block diagram. (b): AM-AM characterisitc of the predistorter, power amplifier, and linearized AM-AM power amplifier. The AM/AM response implies the nonlinear relationship between the output and input power or amplitude.

Keywords— Analog pre-distortion, power amplifier, polynomial model, linearization.

I. INTRODUCTION

In the last decades, the number of wireless users has significantly, increased. The needs of having high data rate and large capacity in dense networks requires highly efficient systems. In addition, the modern wireless communication uses advance modulation schemes in the wide band system. These features apply strict linearity requirement to the power amplifiers (PA). PA performance plays a crucial role in wireless communication quality and its efficiency determines the overall communication link performance. However, the PAs have unavoidable static and dynamic distortion that requires sophisticated linearization process to establish a high-performance wireless communication link. Amplifier linearization is a very concerning and challenging issue, especially for base-station (BS) transmitters (Txs) [1]. In order to compensate the exhibited distortion, one common approach relies on pre-distorting the input signal by mimicking the inverse nonlinear behavior of PAs, called pre-distortion (PD). A number of different linearization methods including the feed-forward [3], [4], feedback [5], digital PD [6] and analog PD [7], [8] have been widely employed to improve the linear characteristic of the PA. As for implementation, the digital PD will no longer be the optim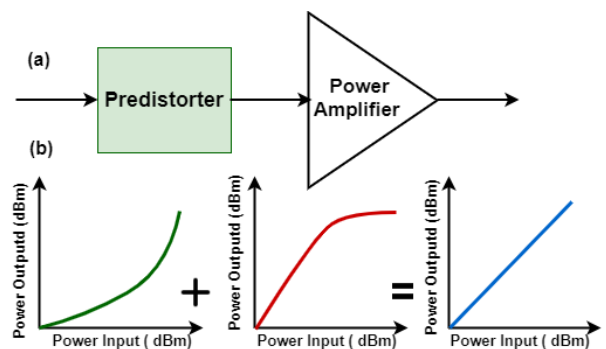um candidates. This is because of their bandwidth limitations and the need for high power supply [1], [2]. The challenge in analog PD methods is in designing a circuit that will accurately produce an inverse characteristic of the original PA's distortion [9], see Fig. 1. The objective of this work is to implement distortion compensation using recurring analog integrated circuit design (ICs). Analog pre-distortion circuit can be relaxed with respect to the limiting bandwidth. Moreover, analog pre-distortion circuits offer low power consumption compared to the digital-based PDs [18]. In this paper, we present an adaptive CMOS analog polynomial PD to improve the wireless communications link quality and performance. The proposed circuit is based current mode design approach. Current mode offers several advantages over conventional voltage mode design, namely: i) low voltage capability, as it explores the voltage compression characteristics of MOSFET transistors; ii) adequate for mathematical function synthesis, especially, addition, multiplication, squaring and power functions; and iii) reduced power consumption. The proposed pre-distortion circuit is able to support, fixed order polynomial function synthesizer with accurate coefficient programming. The proposed circuit is validated through simulation with Spectre, under the Cadence DFW II design environment. For that matter, the circuit is used to linearize a real class-AB PA. The polynomial coefficients are computed in Matlab based on the PA model.
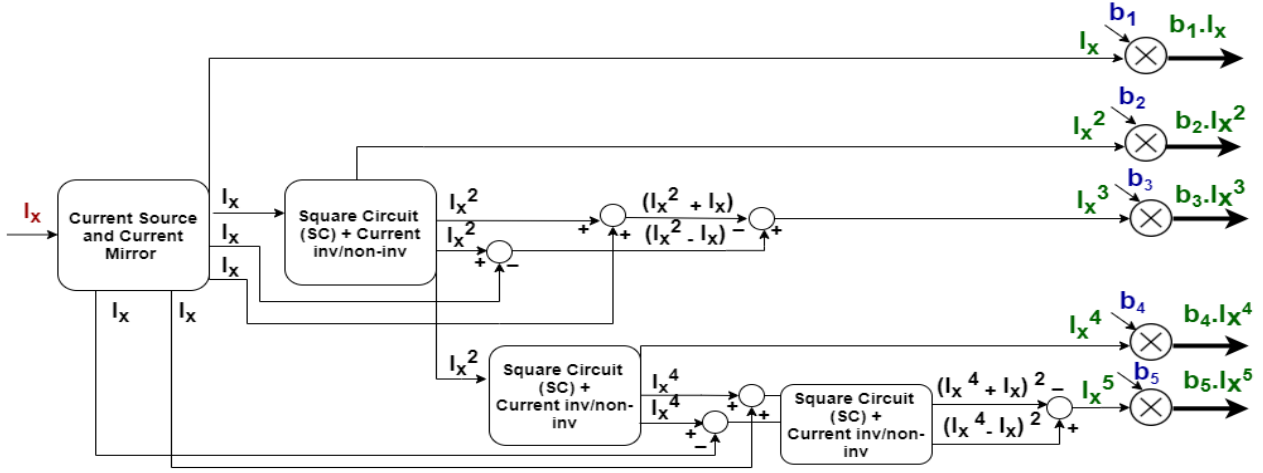
Fig. 3   Proposed 5th order polynomial block diagram. This polynomial is built by combination of squarer cell and current inverting non-inveting modules. The coefficients of polynomial adjusts through current multiplier with sufficient digit extracted from indirect learning.

The rest of the paper is organized as follows; section II describes the polynomial PD concept. Section III presents the proposed circuit, and in Section IV presents and discusses the simulation results. Sections V and VI draw the conclusions and outlook.

II.   POLYNOMIAL PREDISTORTER CONCEPT

PAs exhibit static and dynamic distortions. Static distortion indicates a memoryless nonlinearity and dynamic distortion refer to memory effects [17]. Distortion compensation circuits can be classified according to the type of nonlinearity they can compensate. The present work focus only on static distortion compensation. Figs. 1. (a) and (b) illustrates the gain profiles of the desired PD, PA and cascaded PD (PD-PA). The cascaded PD-PA attempts to combine two nonlinear systems into a single linear system, thus allowing the PA to operate closer to the saturation region (i.e., being more efficient in terms of the energy usage). The proposed PD is compensating the magnitude and phase nonlinearity of the signal, therefore as it shown in Fig. 2. we have used the following equations to represent the PA induced distortions:

$$I + jQ = R_n \cos(\theta_n) + jR_n \sin(\theta_n) \qquad (1)$$

$$R_n = \sqrt{I_n^2 + Q_n^2} \text{ and } \theta_n = -\arctan(Q_n/I_n) \qquad (2)$$

I and Q are input signal, thusR_n is the amplitude and θ_n is the phase of the input signal. The input of PA without PD is:

$$I_{in\_PA} = R_n \cos(\omega t + \theta_n) \qquad (3)$$

The output of PA, which contains both the amplitude

(AM/AM) $R_n'$and phase (AM/PM) θ'_n distortions, is given by:

$$I_{Out\_PA} = A_n(R_n') \cos\left(\omega t + \theta'_n + \emptyset_n(R_n')\right) \qquad (4)$$

Where A is the gain of PA and $\emptyset_n(R_n')$ is additive phase distortion. In complex format. The output of PA is given as:

$$I_n' = A_n(R_n') \cos\left(\theta'_n + \emptyset_n(R_n')\right)$$
$$Q_n' = A_n(R_n') \sin\left(\theta'_n + \emptyset_n(R_n')\right) \qquad (5)$$

It is important to note that, the amplitude and phase distortions only depend on the amplitude and independent of the phase distortion [19]. Therefore, we can first compensate for the amplitude distortion followed by the phase correction. In order to that I_n' and Q_n' are equal to I_n and Q_n, respectively we have:

$$A_n\left(R_n'\right) = R_n \qquad (6)$$

$$\theta'_n + \emptyset_n R_n' = \theta_n \qquad (7)$$

In [13], [20] and [21], polynomial functions were used to represent the nonlinear models. One options was to use the inverse of PA transfer function as means to compensate for the non-linearity using polynomial functions [13]. Polynomial PDs are used to cancel out the static nonlinearities of PAs by minimizing the out-of-band even order intermodulation distortion (IMD). The output of PD is given by equation (8). Where I_x is the input signal and b_1, ..., b_5 are the PD coefficients for the amplitude and phase correction, respectively, which are configurable .

In the following section, we propose a new method to implement an adaptive fifth order polynomial PD, see Fig. 3.÷

$$I_{o\_PD\_mag} = b_{5_{mag}}(I_x^5) + b_{4_{mag}}(I_x^4) + b_{3_{mag}}(I_x^3) + b_{2_{mag}}(I_x^2) + b_{1_{mag}}(I_x^1)$$

$$I_{o_{PD_{Phas}}} = b_{5_{Phas}}(I_x^5) + b_{4_{Phas}}(I_x^4) + b_{3_{Phas}}(I_x^3) + b_{2_{Phas}}(I_x^2)$$
$$+ b_{1_{Phas}}(I_x^1) \qquad (8)$$
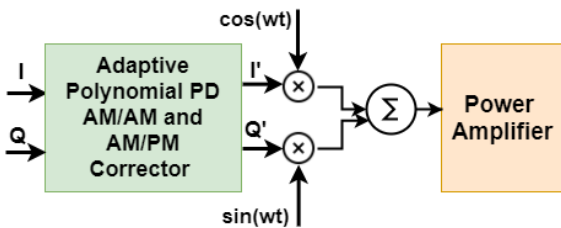
Fig. 2   The block diagram of PD signal generation
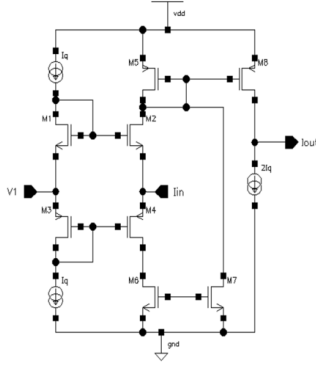
Fig. 4   Squarer Circuit [14].

Fig. 6 Four quadrant current multiplier [4].

III.   PROPOSED POLYNOMIAL CIRCUIT

Fig. 3 demonstrates the proposed polynomial system level circuit. The overall polynomial function includes sub-circuits using well-established current-mode (CM) techniques. The need for the CM building blocks, instead of the voltage mode, is because of the overall dynamic range. Commonly, the nodes within CM circuits are low impedance nodes, presenting small voltage swings, and low impedance leads to low time constant circuits, thus a good possibility of achieving a high bandwidth. Moreover, CM circuits have simple architectures and operate with a significant level of independence from the supply voltages [15]. Another advantage of using the CM approach for all sub-circuits is that, the operation of addition/subtraction is simply achieved through a connection node, following Kirchhoff current law, which is far much simpler and have wider bandwidth, than the addition/subtraction of voltages.

In the proposed circuit of Fig. 3, the input current I_x is replicated through a multiple-output current mirror. These replicated currents are then processed by the squarer circuits and adder/subtraction blocks, which isolate the basic terms of the polynomial, i.e., the monomials. In the final stage, current multipliers set the values of the monomial coefficients by multiplying the result monomial signals by the reference currents, which are set for this purpose. In the following, the sub-circuits used to implement the blocks of the polynomial architecture of Fig.3 are described in detail.
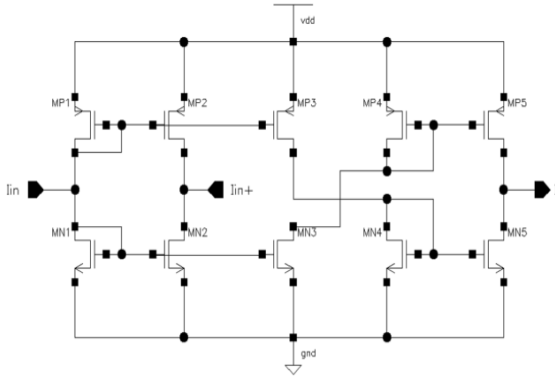

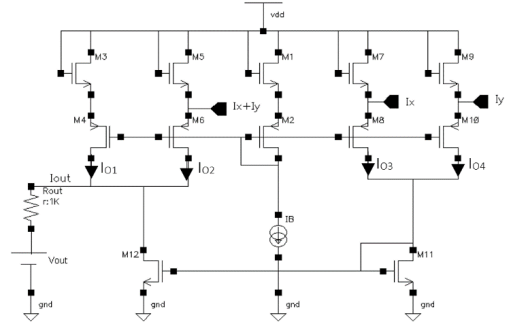Fig.5   Inverting-non inverting circuit. [13]

A.   Squarer Circuit

The squarer circuit follows the work presented in [14], which is derived from a class-AB current mirror, see Fig. 4 I_{in} is the input current signal, I_q is the bias current and I_{out} is the output current. Transistors M$_1$ to M$_4$ constitute a trans-linear loop, with all transistors operating in the saturation region. Adopting the proposed design in [14], the following relations are reached based on trans-linear principle:

$$V_{gs2} + V_{gs4} = V_{gs1} + V_{gs3} \tag{9}$$

$$\sqrt{I_{D2}} + \sqrt{I_{D4}} = \sqrt{I_{D1}} + \sqrt{I_{D3}} \tag{10}$$

$$2\sqrt{I_q} = \sqrt{I_{D2}} + \sqrt{I_{D3}} \tag{11}$$

$$I_{D4} = I_{D2} + I_{in} \tag{12}$$

Where V_{gs1} to V_{gs4} are the gate-source voltage of M$_1$ to M$_4$, respectively. Moreover, I_{D1} to I_{D4} are the drain current of M$_1$ to M$_4$, respectively, which are given by [14]:

$$\frac{I_{D2}}{I_q} = 1 - \frac{1}{2}\frac{I_{in}}{I_q} + (\frac{I_{in}}{4I_q})^2 \tag{13}$$

$$\frac{I_{D4}}{I_q} = 1 - \frac{1}{2}\frac{I_{in}}{I_q} + (\frac{I_{in}}{4I_q})^2 \tag{14}$$

The output current is given [14]:

$$\frac{I_{out}}{I_q} = \frac{1}{8}(\frac{I_{in}}{I_q})^2 \tag{15}$$

B.   Inverting-Non Inverting Circuit

This is based on the current mirrors, which provide a replica of the input current in two of its output terminals - one in the same direction of the input current and the other in the reverse direction. Fig. 5 illustrates the inverting noninverting circuit, where I_{in} is the input current, and I_{in+} and I_{in-} are the direct and reverse direction output currents, respectively. All transistors are operating in the saturation region [13]. Currents generated by this circuit can be replicated and applied to the distinct sections of the circuit, see Fig. 5, through the use of additional current mirrors with a sufficient current ratio.

C.   Current Multiplier

The nonlinear characteristics of the PD needs to be adjusted such that it is opposite to the PA, which is changing with the temperature and component aging. Therefore, the circuit allow controlling the polynomial
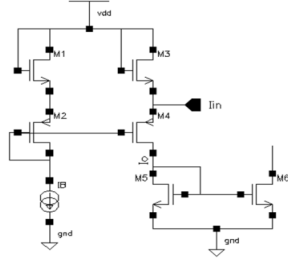
Fig. 7. Translinear loop circuit of multiplier [4].

Fig. 9. Illustrative set of 5th order polynomial input-output characteristics obtained through randomizing (within the admissible region) the currents that control the polynomail coefficients.

coefficients through current multiplier sub-circuits at each of the respective output currents of each polynomial order. In this approach, each coefficient terms of the polynomial, will multiply the current produced by the sub-circuits of each polynomial order by the constant coefficients of $b1$ to $b5$. Fig. 6 shows the circuit of the current multiplier, which is based on the four-quadrant analog multiplier structure using three trans-linear loops. The operation steps of this current multiplier can be described with reference to Fig. 7. Note, considering M1-M4 form a trans-linear loop, assuming equal threshold voltage for all (in absolute value), which leads to [16]:

$$\sqrt{I_{D1}} + \sqrt{I_{D2}} = \sqrt{I_{D3}} + \sqrt{I_{D4}} \qquad (16)$$

From Fig. 7, we have:

$$I_{D1} = I_{D2} = I_B, \ I_{D3} = I_{Do} - I_{in}, \ I_{D4} = I_{Do} \qquad (17)$$

Thus, substituting (9) in (8) yields to:

$$2\sqrt{I_B} = \sqrt{I_o - I_{in}} + \sqrt{I_o} \qquad (18)$$

The output current is extracted by double squaring equation (19) as [16], which leads to have I_o based on input current and bias current:

$$I_o = \frac{I_{in}^2}{16 I_B} + I_B + \frac{I_{in}}{2} \qquad (19)$$

Extending this result to the circuit shown in Fig. 6, which is composed of basic block of the form of that in Fig. 7, we have:
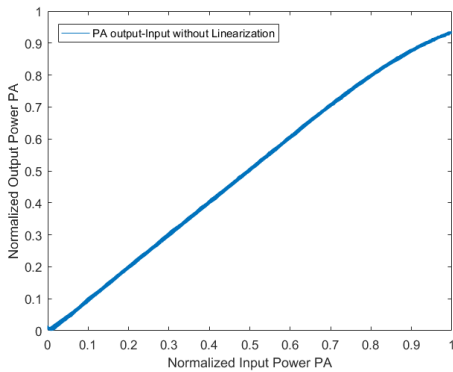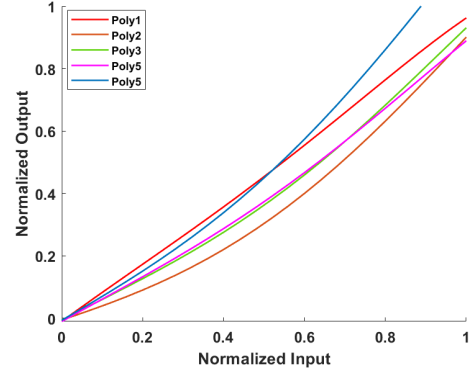
$$I_{out} = I_{o1} + I_{o2} - (I_{o3} + I_{o4}) = \frac{I_x I_y}{8 I_R} \qquad (20)$$

By applying a constant current to I_x and the current produced by a monomial sub-circuit to I_Y, the polynomial coefficients can be configured properly. The coefficients are digits number, which are normalized to proper current value in the range of CMOS transistors. Thus, using the presented sub-circuits to implement each of the blocks of the architecture of Fig. 3, and considering a four quadrant current multiplier applied to each of the currents generated by each monomial term, the following 5th order polynomial function can be implemented using the proposed analog PD circuit. In table (1) the simplified ratio of designed parameters for weight and length of transistor in each blocks are shown.

IV. VALIDATION OF PROPOSED MODEL

To test the polynomial performance, a four-carrier GSM baseband signal is used and pre-distorted. This signal has complex-valued, and therefore the following procedure is considered. Knowing that PAs react mostly to the amplitude of the input signal, the dominant behavior can be characterized by its gain and phase characteristics. The non-linear behavior of our PA model is shown in Fig. 8. Therefore, instead of receiving the in-phase and quadrature components of input signal, the analog PD will deal with the baseband amplitude signal. In order to compensate both the
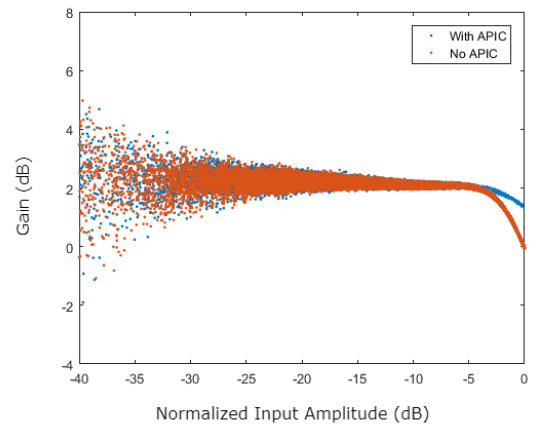

Fig. 8. Nonlinear behaviour of PA

Fig. 10 . AM/AM charectristic by implementing PD

amplitude and phase characteristics of the PA two replicas of the polynomial circuit are implemented operating in parallel and processing the same input signal, i.e., a current that is proportional to the amplitude of input signal and another PD is in charge of phase correction. Next, the coefficients of the two 5th order polynomial circuits are varied, i.e., by modifying the constant current inputs of the four quadrant current multipliers. Then the real and imaginary part of distorted amplitude and gain are extracted

Fig. 9 shows the normalized output of polynomial vs. the input for a range of coefficients as given in Table (2). This figure illustrates the ability of the proposed 5th order polynomial circuit in adapting to the behavior of distinct PAs by simply configuring the currents ($b1$ to $b5$), which controls the polynomial coefficients.

To validate the performance of the proposed polynomial circuit, we have tuned its current controlled coefficients so that it will pre-distort the nonlinear behavior of the PA model, which was retrieved from laboratory measurements of a real PA circuit (i.e., a class AB-based GaN transistor). With the analog PD running in a circuit simulator, we used the PA model to perform this validation test. For this purpose, the input signal is applied to the PA model and its output is retrieved. Then, the coefficients of the two static 5th order polynomials are tuned in MATLAB and using the iterative indirect learning method using the input and output signals of the PA under test [18]. Next, the two circuits implemented in Cadence Spectre are tuned to fit the coefficient. This is performed by varying the values of the current sources, which controls $b1$ to $b5$ coefficients of each analog polynomial. The baseband amplitude and phase of input signal is separated and normalized to the accepted
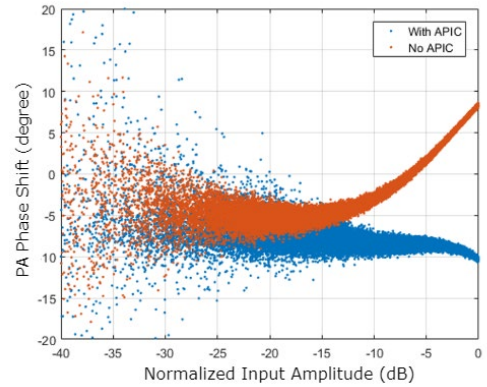

Fig.11. AM/PM charecteristic of power amplifier with and without PD. (AM/PM: amplitude to phasedistortion).

level of input current and processed. The resulting output currents are converted back (by scaling only) to the pre-distorted baseband input signal, which is then applied (in MATLAB) to the referred PA model, and the improvement on output distortion is assessed. Fig. 10 presents the gain characteristic of the PA with and without PD, which demonstrate successful compensation.

Fig. 11 presents the phase characteristics of the PA without and with PD. It demonstrates that, the proposed scheme clearly reduces the PA's phase shift deviation at higher input amplitudes. In Fig. 12, the spectrum of the PA output signal with and without APIC is depicted. As shown, the analog PD is able to reduce the dominant inter-modulation distortion by about 12 and 16 dB on the left and right regions of the spectrum, respectively. Moreover, the PA

Table1: Ratio of weigth and length (W/L) transistor dimension of sub circuits.

Square Cell	Dimension		
Transistors	W/L	Transistors	W/L
M1	10/1	M5	26/1
M2	10/1	M6	5.6/1
M3	65/1	M7	5.6/1
M4	65/1	M8	26/1
Current Inverting-Noninverting	Dimension		
MN1	4/1	MP1	13/1
MN2	4/1	MP2	13/1
MN3	4/1	MP3	13/1
MN4	4/1	MP4	13/1
Current Multiplier	Dimension		
M1	14/1	M2	25/1
M3	14/1	M4	25/1
M5	14/1	M6	25/1
M7	14/1	M8	25/1
M9	14/1	M10	25/1

Table 2. Set of current to generated poly1, ..poly 5, which each of the polys are 5th order polynomial for magnitude correction.

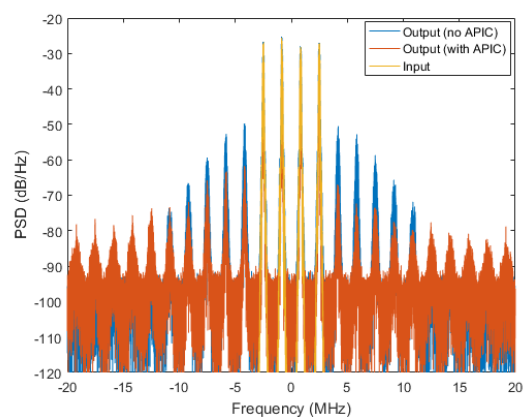| Output Polynomial	Current coefficient				
	$b_{5_{mag}}$	$b_{4_{mag}}$	$b_{3_{mag}}$	$b_{2_{mag}}$	$b_{1_{mag}}$
Poly1	5uA	7ua	13uA	27uA	29uA
Poly2	25uA	20uA	15uA	10uA	5uA
Poly3	20uA	15uA	20ua	5ua	10uA
Poly4	7uA	4uA	7uA	20uA	20uA
Poly5	7uA	7uA	7uA	4uA	4uA

Fig.12 Power spectral density before and after implementing PD

model was initially set in a highly compressed operation, by presenting a high distortion level - with an intermodulation ratio of about 25 dB (see Fig. 12).

V. CONCLUSION

In this paper a new analog polynomial PD circuit was presented for use in wireless communication. The polynomial PD circuit was proposed to meet the linearity requirement for advanced wireless system by using the current-mode sub-circuits to allow a wide dynamic range with configuration of the transfer function based on the characteristics of PAs. The proposed circuit was successfully validated through a mixture of circuit-level simulations (i.e., using Cadence) and system-level simulation using MATLAB to mimic the PA input-output behavior. The IMD level was reduced by 16dB using the proposed analog PD.

VI. OUTLOOK

The presented analog circuit can be used to make predistortion linearizing effect for other type of wireless communication link such as optical communication. One of the limiting factors in optical communications is nonlinear behavior in the transmitter and receiver due to nonlinear behavior of amplifier and driver of LED and photodiode. This claim will be validated only by placing the proposed PD before the nonlinear part of communication link and configured it. In addition, RF-based wireless communications is being combined with visible light communication in certain applications in order to improve the link's availability, increase transmission capacity and improve the performance. Therefore, the proposed linearization scheme can also be adopted.

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