Fabrication and modelling of MInM diodes with low turn-on voltage

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Multi-stack metal-insulator-metal (MIM) diodes of ultra-thin Ta_2O_5/Al_2O_3 dielectrics are investigated by experiment and modelling. Tunnelling transport is modelled using transfer matrix (TMM) and Wentzel-Kramers-Brillouin (WKB) methods. Rectification for a triple dielectric layer device is shown to occur at a turn-on voltage (V_{ON}) as low as 170 mV with a non-linearity of 3 and an asymmetry increasing from 2.2 at the V_{ON} to over two orders of magnitude at 1 V.

1. Introduction

Ultra-high speed rectification is needed for the development of rectennas used for scavenging thermal infrared radiation, imaging by detection of hot object emissions, recycling residual heat,[1] solar energy harvesting,[2,3] and wireless satellite communication. They could also be used in detectors for THz imaging in biomedical applications,[4] skin cancer detection,[5] and even passive imaging.[6] Metal-insulator-metal (MIM) tunnelling diodes have the potential for THz rectification,[7-9] and double dielectric structures allow greater flexibility in design.[10] Rectification is controlled by femtosecond-speed tunnelling[11] and requires sufficiently low turn-on voltage, ideally towards zero bias,[12] for efficient operation in low-power applications such as rectenna arrays.[13] The latest studies point to MIIM configurations based on Co/Co_3O_4-TiO_2/Ti[14] and Ti/TiO_2-ZnO/Al[15] with reported zero bias responsivity of 1.2 and 1.9 A/W respectively.

We previously reported tunnelling mechanisms in thickness-stepped MIIM structures.[16] We investigate in this work the influence of band gap engineering of the structures on the rectifying performance and focus on experiment-to-model matching, reporting well-defined rectification at low turn-on voltage.

2. Fabrication

Five 100^2 µm^2 MInM devices of n insulators were fabricated on cleaned Corning glass (CG) and Si substrates (*Table 1*). The thicknesses of the dielectric layers were verified by variable angle spectroscopic ellipsometry (VASE). Metal films of high purity were thermally evaporated, and patterned by lift-off photolithography using 1.2 µm thick *Shipley S1813* positive photoresist. Al_2O_3 and Ta_2O_5 were sputtered at room temperature for samples S1 and S2, and atomic layer deposited (ALD) at 200 ºC for sample S3. The current voltage (IV) measurements were done in the dark in a temperature-controlled heating stage or in a cryostat. Voltage was swept with 10 mV step size from 0 V to negative or positive bias.

Table 1: Device structures and layer thicknesses.

	nm	M_1	I_{NO1}	dep.	nm	I_1	nm	I_2	I_{NO2}	nm	M_2
S1	Si	80 Au	–	Sp.	4	Ta_2O_5	1	Al_2O_3	AlO_x	80	Al
S2	Si	80 Au	–	Sp.	0.5	Al_2O_3	4	Ta_2O_5	AlO_x	80	Al
S3	CG	80 Au	–	ALD	4	Ta_2O_5	1	Al_2O_3	AlO_x	80	Al
S4	Si	80 Au	–	Sp.	6	Ta_2O_5	–		–	20/60	Cr/Au
S5	Si	120 Al	AlO_x	Sp.	1	Al_2O_3	4	Ta_2O_5	AlO_x	120	Al

M_1/M_2: bottom/top metal, dep.: deposition technique for I_1/I_2, Sp.: sputtered, I_{NO1}/I_{NO2}: native oxides for M_1/M_2

The S5 layer structure was imaged using high resolution transmission electron microscopy (HR-TEM). FIG. 1(b) shows 3 nm thick AlO_x layers grown at the interfaces with Al metal electrodes. However, the actual thickness is expected to be less due to possible further oxidation by the coating used for HR-TEM sample preparation.[17]
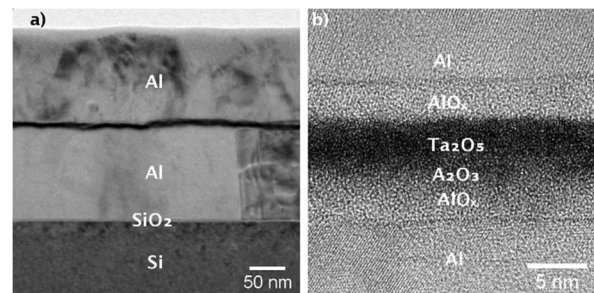

FIG. 1. HR-TEM images of S5: a) the layer structure and b) 24×24nm^2 of the active area showing AlO_x layer below the top Al and on top of the bottom Al in addition to the sputtered Al_2O_3/Ta_2O_5 oxide stack.

3. Tunnelling model

Modelling is based on the Tsu-Esaki method[6] where the tunnelling current density is calculated at each applied voltage as the charge transport flowing from M_1 to M_2 electrode minus that of opposite flow:

$$J \approx \int_{E_{min}}^{E_{max}} T(E_x) dE_x \int_0^\infty [f_1(E) - f_2(E)] \, dE_\rho \quad (1)$$

$T(E_x)$ is the transmission probability calculated using TMM and WKB approaches.[7] $f_1(E)$ and $f_2(E)$ are the energy distribution functions representing the probability of occupation of states near the dielectric interfaces with M_1 and M_2 respectively. E_{min} and E_{max} define the minimum and highest conduction band values of $E_C(x)$; dE_x is the energy segment taken by specifying the certain number of states included between the lower and upper limits.

Each barrier is divided into N slices, where the wave function and its derivative are assumed to be continuous at each boundary. The transmission coefficient is the ratio of the current reaching the second electrode to that at the first electrode:

$$T(E_x) = \frac{J_N}{J_1} = \frac{k_N m_N}{k_1 m_1} \frac{|A_N|^2}{|A_1|^2} \quad (2)$$

A_1 and A_N are the wave amplitudes at the dielectric interfaces with M_1 and M_2 respectively.

At each value of voltage bias, the position of the conduction band $E_{C,j}(x)$ is calculated taking into consideration the image force effect which lowers the barrier defined by the work function.[18] The energy, E_x is discretized, and the probability $T(E_x)$ for each is found using:

$$k_j = \sqrt{2m_j[E_x - E_{C,j}(x)]}/\hbar \quad (3)$$

and the TMM approach, considering a piecewise constant potential.[19]

For faster computation of $T(E_x)$, the Wentzel-Kramers-Brillouin (WKB) approximation is adopted, substituting the wave function in the time-independent Schrödinger equation[20] using the following approximation:

$$T_{WKB}(E_x) = \exp\left(-\frac{2}{\hbar} \int_0^{x_1} \sqrt{2m_{ox}(E_C - E_x)} \, dx\right) \quad (4)$$

4. Diode design

We focus on realising (a) larger asymmetry, defined as the ratio of the current at positive bias to that at negative bias at certain voltage: $f_{asym} = J_+/J_-$ (b) lower dynamic resistance, defined as: $R_d = dV/dI$, and (c) larger non-linearity, defined as the ratio of the static to dynamic resistance: $f_{NL} = (V/J)/(dV/dJ)$. A turn-on voltage (V_{ON}) is defined as the point at which the current becomes large enough at one polarity to create $f_{asym} = 3$. The aim is for rectification at the lowest possible V_{ON}.

At each applied voltage, a major factor for increasing the tunnelling probability is described by altering the shape of $E_C(x)$ to minimize the effective tunnelling distance (FIG. 2). To create an asymmetry, the structure is engineered for the effective tunnelling distance, energy band bending and barrier heights, to be larger at one polarity, e.g. larger at −1.5/−0.5 V as compared to +1.5/+0.5 V for S1 and S2. While this can only be obtained by increasing the work function dissimilarity of the electrodes in MIM structures, much larger asymmetry can be achieved in multi-stack dielectric structures by tuning the individual thickness of the dielectric layers. The use of 2 or more barriers serves to limit the dominance of thermal emission and could bring further enhancement in f_{NL} with step tunnelling (ST) and resonant tunnelling (RT), which is desirable. Fowler-Nordheim tunnelling (FNT) could dominate where band bending shortens the effective distance for electrons to tunnel, and ST is reached when the band bending is steep enough, as shown for S1 at +1.5 V.[21] RT arises from charge transport via intermediate bound states in the quantum well as the electron energy is matched with one of them (S2 at −1.5 and +1.5 V).[22]
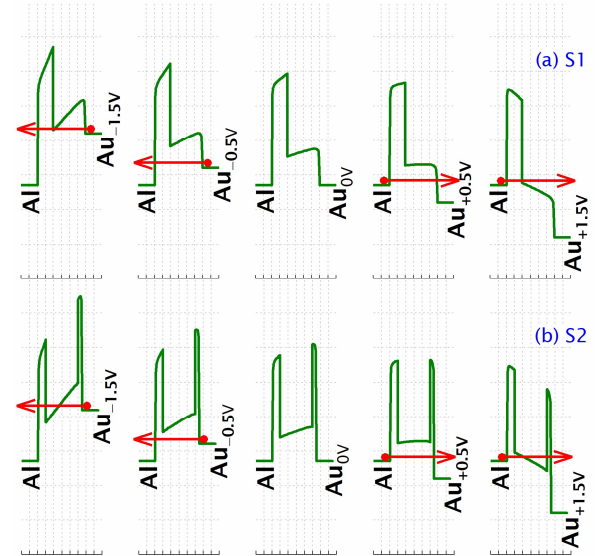

FIG. 2. (Color online) Conduction band diagrams of S1 (a) and S2 (b) structures at −1.5, −0.5, 0, +0.5, and +1.5 V where Al left electrode is grounded. Electron injection is indicated by the red arrow. Each x-axis tick corresponds to 1 nm. All axes set to the same scale.

5. Results and discussion
5.1 Experimental

FIG. 3 shows that sample S4 has the lowest R_d, but shows poor rectifying performance at low bias with f_{NL} of 3 obtained at V_{ON} of 0.84 V and low f_{asym} not exceeding 4.2 Despite having a similar structure, ALD-S3 achieves sufficient rectification at an order of magnitude larger R_d and at almost double V_{ON} of sputtered-S1, which makes the latter superior. Due to its lower R_d and slightly larger f_{asym} at its lower V_{ON}, S2 shows better low voltage rectifying performance than S1. Its close-to-zero V_{ON} value (0.17 V) associated with well-defined rectification (f_{NL} of 3 increasing towards 8.8 at 0.69 V and f_{asym} of 2.2 increasing towards 133 at 1.14 V) is distinguished as compared to other state-of-the-art tunnelling rectifiers.[23, 24]
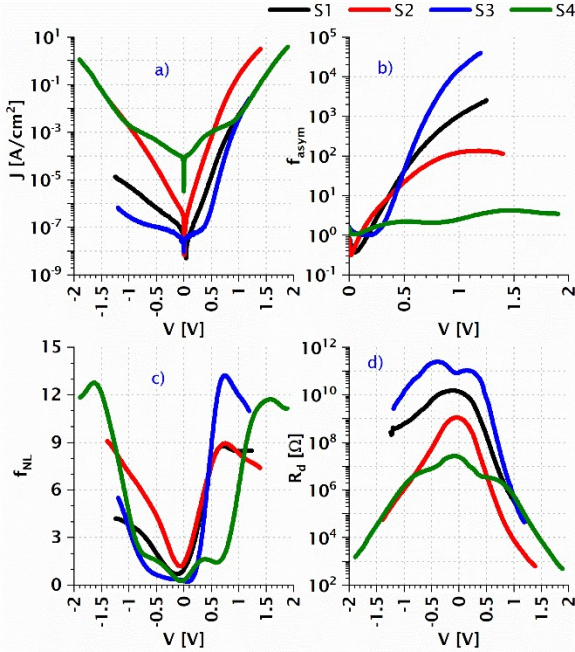

FIG. 3. (Color online) Rectifying characteristics of the devices at 300 K: (a) JV curves, (b) f_{asym}, (c) f_{NL}, and R_d.

5.2 Modelling of results

Best experimental-to-model fittings have been made considering an additional 1 nm layer of Al$_2$O$_3$ below the top Al layer (FIG. 1). For S1 and S2, WKB and TMM current calculations are nicely matched over the applied voltage range [FIG. 4(a,b)]. This is because RT and ST mechanisms of large energy barrier variation leading to inaccuracy in WKB, are unlikely to occur within the voltage range. Major negative peaks before negative differential resistance (NDR) are accounted for in calculating the tunnelling transmission probability $T(E_x)$ using TMM but not in the WKB method [FIG. 4 (c,d)]. The TMM model predicts the

currents have the first resonance peaks before NDR at −3.6 V for S1 and at −1.9/+1.6 V for S2 [FIG. 4(c,d)]. TMM also predicts smaller NDR peaks for step tunnelling for S1, starting at +1.5 V. The current rise is noticeably steep in positive bias for S1 and S2 [FIG. 4(a,b)]. This is explained for S1 by the lower conduction band, which bends steeply shortening the effective tunnel distance for electrons to reach step tunnelling at +1.5 V [FIG. 2(a)]. For S2, the potential well becomes wide and deep enough for resonant tunnelling to occur at +1.6 V for S2 [FIG. 2(b)]. The steeper current rise at negative bias for S2 as compared to S1 is explained by the shorter effective tunnel distance in the former (FIG. 2), where the conduction band is lower. Moreover, as the negative bias is increased, the conduction band of S2 as compared to S1 bends steeper towards wider and deeper resonance potential well [FIG. 2] for earlier occurrence of RT at −1.9 V for S2 as compared to − 3.6 V for S1 [FIG. 4(c,d)]. It should be noted that the voltage regime of the J-V measurements could not be exceeded due to the onset of breakdown, which is a common obstacle to achieving RT.
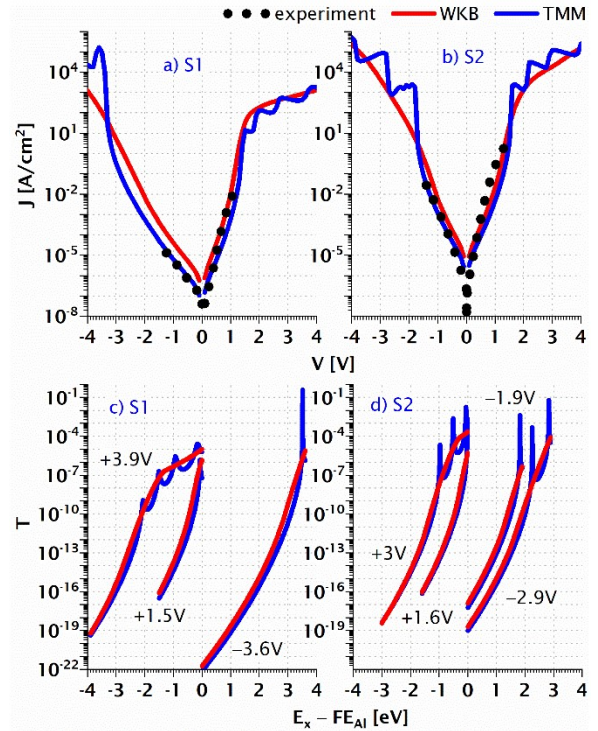

FIG. 4. (Color online) Experimental versus WKB/TMM modelled JV curves of S1 (a) and S2 (b) at 300 K and their corresponding $T(E_x - FE_{Al})$ at voltages of selected peaks (c,d).

The tunnelling model is closely matched to the experimental results confirming the dominance of tunnelling which is furthermore supported by the minor temperature sensitivity and by the current upsurge occurring for sample S3 at 77 K (FIG. 5), low enough

for thermal emission to become effectively frozen out. Besides, for S3, the existence of a larger number of defects in the ALD-deposited Ta_2O_5 bulk is indicated by the steady JV temperature sensitivity along the applied range [FIG. 5(c)], the larger offset in its V_{ON}, and its much larger hysteresis around 0 V as compared to the sputtered devices. For the 6 nm-Ta_2O_5 MIM S4, Schottky emission (SE) and PFE dominate over |0.2-1| V and |1-1.9| V ranges at both polarities respectively with dynamic relative permittivity ε_r of 5.2 eV and trap depth φ_T of 1.2 eV, extracted using the JV data at 300 K.
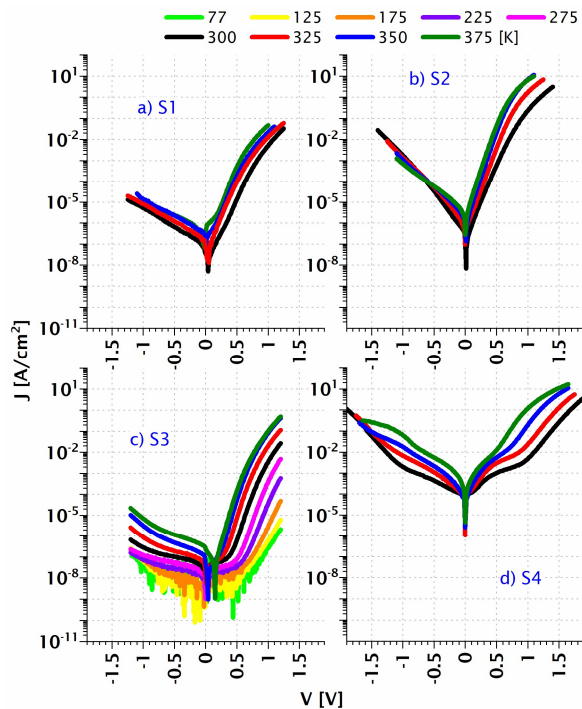

FIG. 5. (Color online) Temperature dependent JV curves of the devices (same axes scale for all) measured using heating stage at 300-to-375 K (a,b,d) or using the cryostat at 77-to-375 K (c).

6. Conclusion

The consistency of the experimental characteristics with the tunnelling transmission probability has been demonstrated for MI_nM diodes using Tsu-Esaki model calculations adapted with TMM and WKB. The MI_3M device (S2) with sputtered oxides, was seen to show the closest-to-zero rectifying performance at $V_{ON} = 0.17$ V, essential for passive ultra high-speed rectification.

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