

**BI-DIRECTIONAL CURRENT-FED MEDIUM FREQUENCY
TRANSFORMER ISOLATED AC-DC CONVERTER**

A Thesis

by

SOMASUNDARAM ESSAKIAPPAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2010

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee, Prasad Enjeti

Committee Members, Aniruddha Datta

Won-jong Kim

Chanan Singh

Head of Department, Costas Georghiades

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ABSTRACT

Bi-directional Current-fed Medium Frequency Transformer Isolated AC-DC Converter.

(May 2010)

Somasundaram Essakiappan, B.E., College of Engineering, Guindy, Anna University

Chair of Advisory Committee: Dr. Prasad Enjeti

The use of high power converters has increased tremendously. Increased demand for transportation, housing and industrial needs means that more number of power converters interact with the utility power grid. These converters are non-linear and they draw harmonic currents, significantly affecting power quality. To reduce harmonics, filters, power factor correction circuits and capacitor banks are required. And the development of hybrid technologies and renewable energy power stations trigger a demand for power converters with bi-directional capabilities. The objective of this thesis is to develop a high power quality, bi-directional AC-DC power converter that is a solution to the aforementioned problems.

This thesis studies an existing topology for a high power AC-DC power conversion with transformer isolation. The topology consists of an uncontrolled rectifier followed by a DC-DC converter to produce a set voltage output. A design example of the topology is simulated using the PSIM software package (version 6). Critical performance characteristics such as power factor and total harmonic distortion are analyzed.

Following that study a new topology is proposed, which is an improvement over the older design, with reduced power conversion stages. The new topology has a fully controlled current source Pulse Width Modulation (PWM) rectifier at the front end to replace the uncontrolled rectifier and DC-DC combination. This topology has multi-quadrant operational capabilities and the controller employs Selective Harmonic Elimination techniques to produce the programmed PWM switching functions for the rectifier. A design example of the converter and the digital controller are simulated in PSIM environment. The converter input current THD (Total Harmonic Distortion) and input power factor are within IEEE 519 and DoE standards. The converter is simulated in both first and fourth quadrant operations.

A side-by-side comparison of the two topologies is done with respect to design and performance features such as power factor, THD, filter size, etc. The new topology converter provides performance superior to that of the older topology. Finally the thesis explores possible applications for the converter in power supplies, renewable energy and hybrid technologies.

ACKNOWLEDGEMENTS

I would like to thank the chair of my advisory committee, Dr. Enjeti, for the support and guidance throughout the course of my work on this thesis. I would also like to thank my committee members, Dr. Datta, Dr. Kim and Dr. Singh for their support. I should thank all the professors whose expertise, through in-class and one-on-one discussions, helped me in my research. I would like to thank all the students, current and former, at the department of Electrical Engineering who helped me learn a lot from all the lively discussions and debates. I must thank the staff at the department for keeping the machine running smoothly so we could work on our research.

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CHAPTER I

INTRODUCTION

Power converters are ubiquitous. They condition the available power to be usable to any load. And with increasing consumption of electrical energy, high quality power converters are more important than ever.

1.1 Definition of power quality

Quality power in a very broad sense can be defined as electrical power supplied to a load as required by it – which could be a specified DC voltage or current, AC voltage or current at a particular frequency, a mix of both – within acceptable tolerances. Power quality measures quantify the deviation of supplied power from the ideal requirement. Some examples of power quality measures are power factor, total harmonic distortion, voltage sag, voltage flicker, voltage imbalance and frequency deviation. The definitions of these measures shall be discussed later.

1.2 Need for high power quality, multi-quadrant converters

The increasing use of high power converters, development of new kinds of applications and their interaction with the power utility grid pose design and operational challenges. These challenges need to be given a closer look to set design goals.

This thesis follows the style and format of *IEEE Transactions on Industry Applications*.

1.3 Problems arising from poor power quality

The performance of electrical and electronic applications can be very sensitive to power quality measures. The applications themselves play a very important role in power quality issues. Poorly designed systems as well as non-linear devices starting from simple diodes introduce harmonics into the supply. Harmonics are sinusoidal currents or voltages at frequencies that are integral multiples of the design frequency of the system.^[1] They affect the system in a number of ways including the following.^[2]

- Harmonics affect other sensitive loads connected to the point of common coupling, viz., the same voltage or current source
- They may excite series or parallel resonances leading to high voltages or high currents
- They overload the circuitry thereby reducing efficiency and life time
- They reduce actual available power by two-thirds and also increase losses in switches
- High neutral-earth voltages affect digital equipment and Local Area Networks

The presence of harmonics decreases the power factor of the system. Low power factor reduces the real power available to the load and customers who draw power at power factor lower than 0.95 lagging stand to pay hefty penalties to the regulatory authority.^[3]

These factors make high power quality a necessity. These converters should draw power at high power factors, introduce minimum amount of harmonics into the supply, provide minimum distortion power to the load and are better in efficiency.

1.4 Growth of renewable energy sources

In addition to conventional energy sources like fossil fuels and nuclear power, renewable sources like wind and solar power plants feed into the utility grid. The renewable energy sector has been consistently clocking double-digit growth. ^[4]

Wind turbines and photovoltaic cells provide power at very little operational costs. Figure 1 discusses the different ways in which these renewable energy sources can be integrated with the electrical utility grid. The wind turbines are either connected to the generator through a gearbox, or it is directly connected to the generator and the AC output is processed by power conditioning converter circuits to produce useable power. Photovoltaic arrays on the other hand, produce a DC current which is processed by an inverter to produce AC voltage to synchronize with the utility grid.

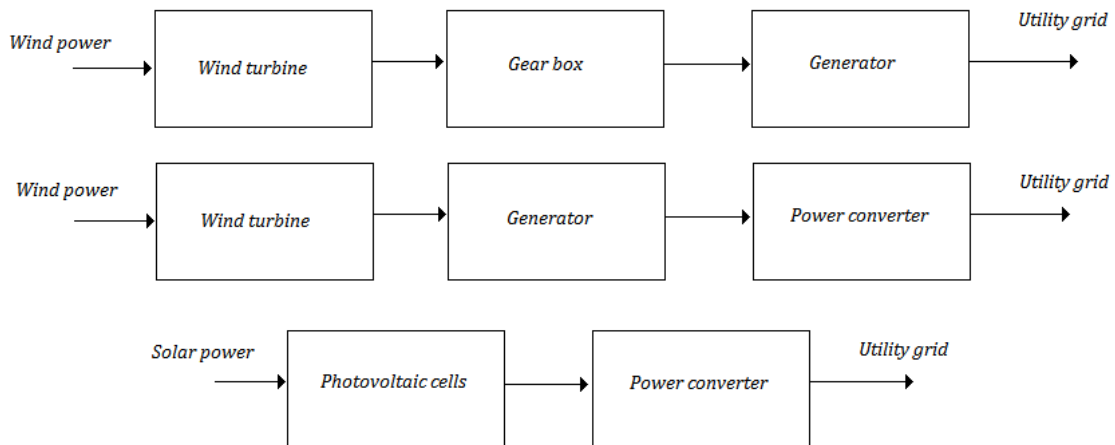


Figure 1: Power flow paths in wind and solar power generation

With increasing solar and wind energy input to the grid, even small percentages of harmonics could start making significant contributions to poor system performance. The solution to the integration problem of these sources to the grid is getting more complex because of the intermittent nature of their availability, geographic remoteness and the development of new grid systems like HVDC transmission lines.

The new solution proposed needs to incorporate methods for the renewable sources to receive power for monitoring and control, during periods of zero production. This calls for a power converter with bi-directional capabilities.

1.5 Dynamic loads and other special applications

Electric hybrid vehicles have achieved tremendous technological development and immense popularity in recent years. These vehicles operate with dual power houses, an Internal Combustion Engine (ICE) and an electric motor with a battery for voltage input.

During acceleration and normal cruising, the powers from the battery powered electric motor and the ICE are used to drive the vehicle. During deceleration, the braking power is regenerated and the energy is transferred to the battery. The power converter supplying power to the motor should be highly efficient and should have bi-directional capabilities for this to be possible. Besides hybrid electric vehicles, other applications like flywheel energy storage and regenerative braking systems employ similar techniques for power transfer in both directions.

Certain other applications are being developed which directly transfer power in both directions between an electric vehicle and the utility grid itself. Such vehicles are called Vehicle-to-Grid (V2G) cars, developed by the University of Delaware. ^[5] These are electric or plug-in electric hybrid cars but they are different in that they can also transfer power from the batteries in the car to the utility during times of peak power demand, as discussed in Figure 2.

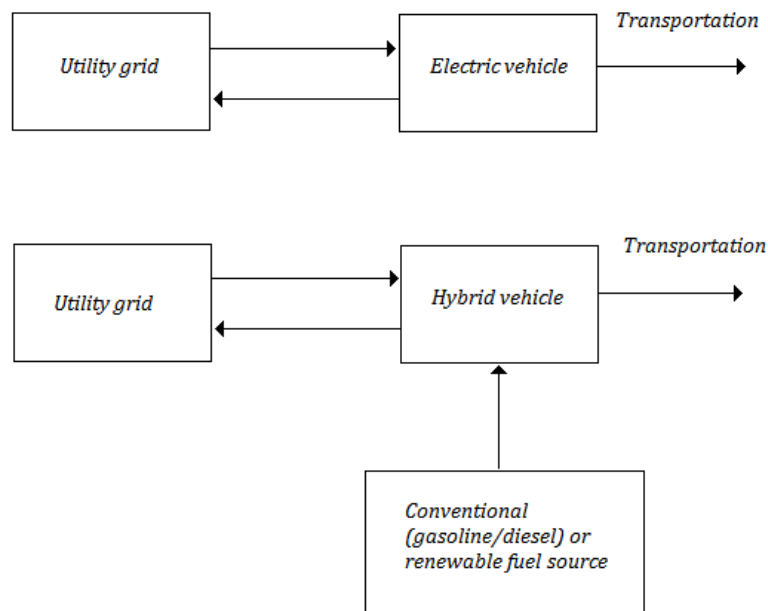


Figure 2: Flow of power in Vehicle-to-Grid cars

These cars thus help to fill the power demand - supply gap in power and average out the daily demand curve. This means the converters on-board have to produce high quality AC power which can be synchronized to the grid.

1.6 Objective of the thesis

The objective of this thesis is to propose a new topology and control methodology for high power AC-DC conversion. The thesis will first study existing topologies for AC-DC power conversion and weigh the pros and cons of those circuits. A design example of one of the topologies will be simulated and the performance measures will be analyzed.

The new topology proposed will provide a high power quality design under a range of operating conditions. It will also have bi-directional capabilities enabling the flow of power from the load side of the design to the source side. The proposed control methodology will eliminate significant amount of harmonics in the AC input current to the converter. The design will have multiple control variables for flexible control. The converter topology and the controller will be simulated for a design example and the performance measures will be compared with those of the previously existing topology. Potential applications for the new topology will also be explored.

1.7 Literature survey

The application notes from Magna-Power Electronics provide a description of the design and operation of a high power AC-DC converter. ^[6] Ned Mohan, Tore M. Undeland and William P. Robbins ^[2] study the different kinds of AC-DC conversion designs available, and also the IEEE standards for power quality measures like Total Harmonic Distortion (THD). Selective Harmonic Elimination (SHE) techniques to attenuate significant

harmonics are evaluated by Enjeti et al. ^[7] The design of input filters for PWM rectifiers is discussed by Zargari et al. ^[8]

1.8 Thesis outline

Chapter I introduces the importance of power quality and the impact of modern applications on the power supply grid. It also speaks about the need for high power quality bi-directional converters for modern applications and the advantages those converters bring with them.

Chapter II deals with a study of existing topologies for high power AC-DC conversion. It also discusses the regenerating capabilities and multi-quadrant operational capabilities of those designs.

In Chapter III, an existing topology for high power DC power supplies with transformer isolation is analyzed, simulated and its performance is studied, specifically with respect to measures such as THD and power factor.

In Chapter IV, the new topology for the power converter is described; its operation in both first and fourth quadrants is studied. This chapter also introduces the control techniques and switching algorithms used in the converter.

Chapter V deals with a design example and simulation results for the first and fourth quadrant operations, along with a comparison with the older topology.

Chapter VI concludes the thesis with a summary and also by discussing potential applications for this topology.

CHAPTER II

HIGH POWER AC-DC CONVERSION TOPOLOGIES

Since alternating current is the form in which electrical power is universally supplied, a rectifier also is a universally used power converter circuit.

2.1 Rectifiers introduction

Rectification converts AC power, usually supplied at 50/60 Hz, into a DC voltage specified by the load, as represented in Figure 3.

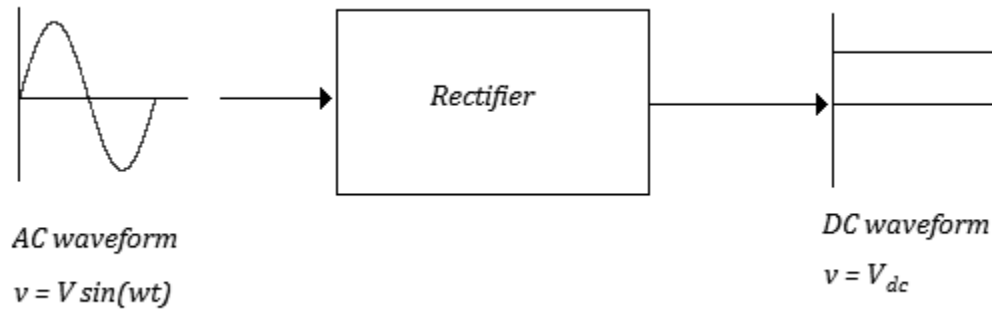


Figure 3: Rectifier function

The ideal rectifier produces a totally ripple free DC output and introduces no harmonics into the AC supply system. The practical systems accomplish these functionalities – within tolerances – by using various control techniques, input and output filters.

2.2 Multi-quadrant operation

The objective of this thesis is to develop a rectifier with bi-directional capabilities. It means that the converter should be able to operate in more than one quadrant in the V-I plot. In this thesis, the quadrants are named as in Figure 4.

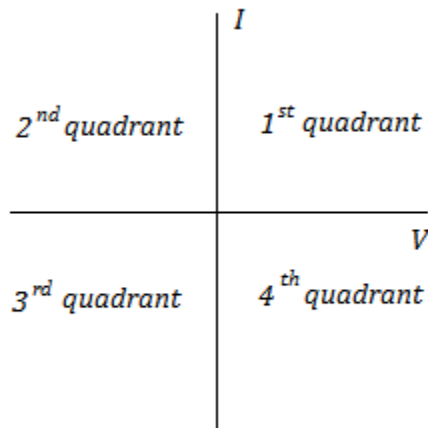


Figure 4: Four quadrants of operation in the V-I domain

There are three main types of rectifiers to provide a controlled DC voltage from an AC voltage source, based on the devices and control techniques used. They are

- Line frequency uncontrolled rectifier, followed by a DC-DC converter
- Line frequency phase controlled rectifier
- PWM rectifier

These rectifier types are to be studied with respect to power quality, hardware requirements (switches, output filters and EMI filters) and multi-quadrant capabilities.

2.3 Line frequency uncontrolled rectifier

Line frequency uncontrolled rectifiers are inexpensive diode rectifiers which convert the input AC into DC in an uncontrolled way. The properties of the p-n junction diode are the only elements dictating the operation of the uncontrolled rectifier. There are two different types of uncontrolled rectifiers. They are

- Half-bridge diode rectifier
- Full-bridge diode rectifier

A half-bridge diode rectifier, shown in Figure 5, uses just one diode for each phase of operation.

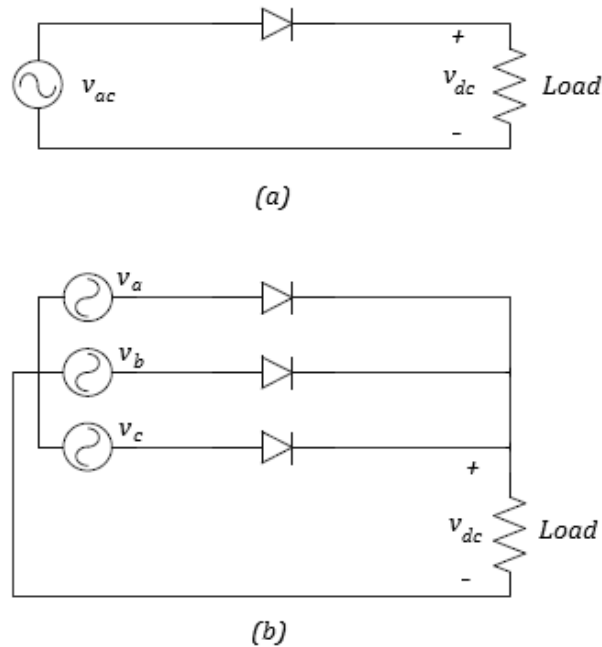


Figure 5: Single-phase (a) and three-phase (b) half-bridge rectifiers

In the single-phase rectifier, only one half of the AC wave is rectified and the three-phase rectifier output has a considerable ripple as shown in Figure 6.

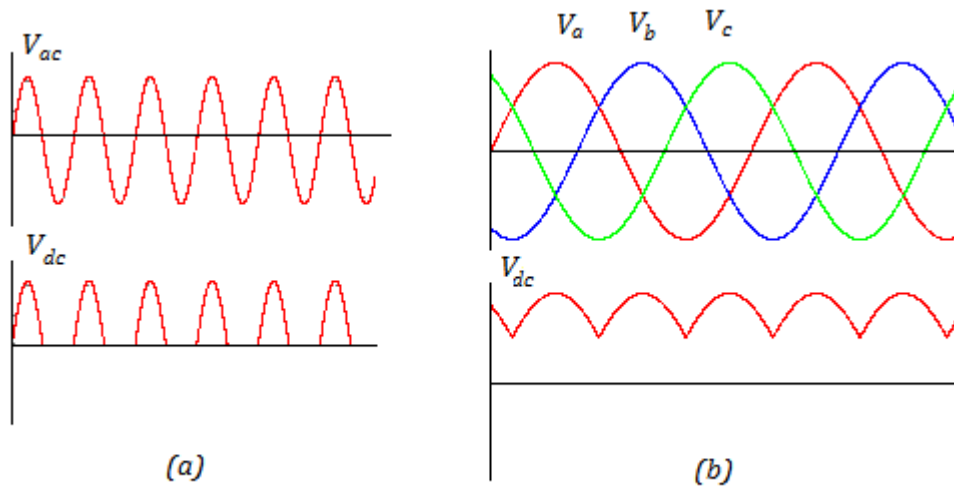


Figure 6: Input AC and output DC waveforms of a single-phase (a) half-bridge rectifier and a three-phase (b) half-bridge rectifier

The biggest problem with half-bridge rectification is that it draws an average DC current from the AC supply voltage. This would drive any input transformer into saturation. This, combined with underutilization (only one half rectified) makes half-bridge rectifiers unsuitable for high quality power conversion.

A full-bridge diode rectifier, however, rectifies both half cycles of the AC wave, providing a DC voltage that has a higher average value and lower ripple than the half-

bridge configuration. The construction of single-phase and three-phase full-bridge rectifiers are given in Figure 7.

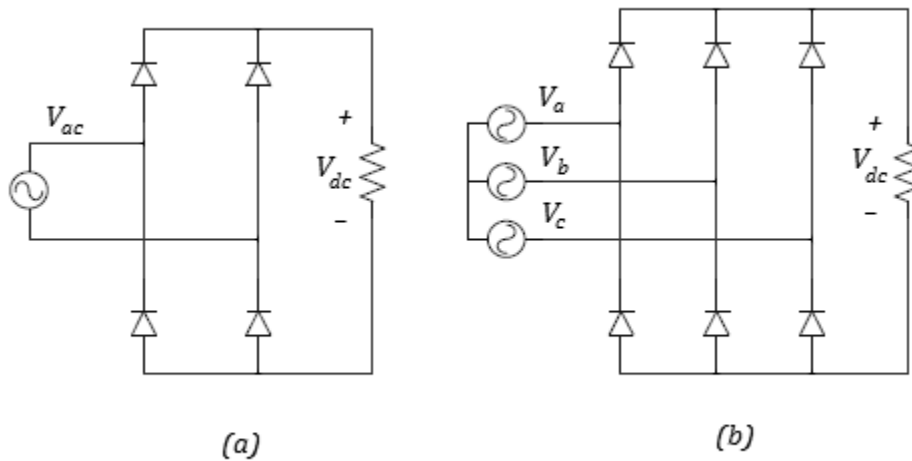


Figure 7: Single-phase (a) and three-phase (b) full-bridge rectifiers

The full-bridge converters do not suffer from the problem of drawing a DC average current. Nevertheless, they still have poor input current harmonics. This means they require heavy filters or special harmonic mitigation circuits^[9] to reduce harmonic levels. Harmonics may also be reduced if diode rectifiers are used in special configurations like 12 pulse and 18 pulse rectifiers.^[10]

Diode rectifiers are not capable of multi-quadrant operation. They cannot reverse the direction of flow of current or the polarity of voltage and so they only operate in the first quadrant.

2.4 Line frequency phase controlled rectifier

Line frequency phase controlled rectifiers employ thyristors for switches, as shown in Figure 8. Thyristors are line commutated devices which start conducting when a positive voltage is applied across it and an impulse is applied to the gate. They stop conducting current when the voltage across them becomes negative. They cannot be force commutated, which means they cannot be turned on and off at will.

Phase controlled rectifiers control the output DC voltage by changing the phase angle at which impulses are applied to the gates of the thyristors. With increasing phase angle values, the DC voltage decreases. The DC voltage follows the relation

$$V_{dc} = 1.35 V_{LL} \cos \alpha$$

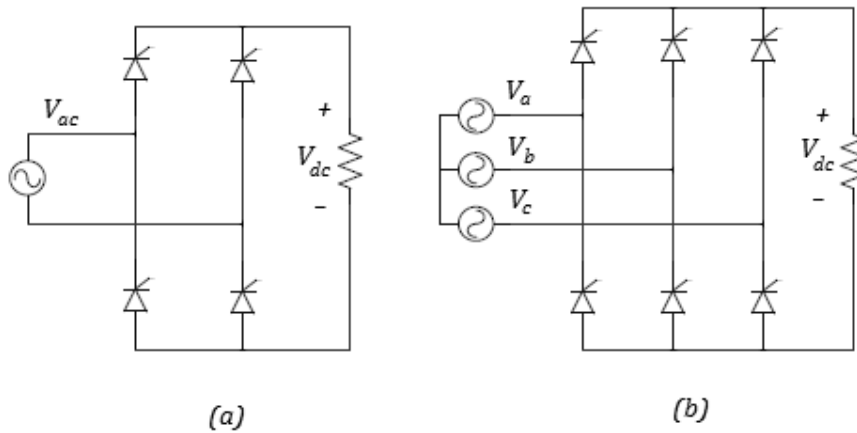


Figure 8: Single-phase (a) and three-phase (b) line frequency phase controlled rectifiers

When the phase angle α increases beyond 90° the converter moves from rectifier to inverter mode with the output voltage reversing its polarity. But reversal of current is not possible because thyristors do not allow reverse flow of current. Thus the converter can operate in the first and the second quadrants.

The displacement power factor of the converter is dependent on the phase angle. With increasing α , the symmetry of the input current waveform gets poorer and so does the power factor. Thyristor based rectifiers also suffer from commutation failure problems.

2.5 PWM rectifiers

PWM rectifiers are constructed using fully controllable switches that are gated using PWM signals. The PWM switching accomplishes mitigation of significant lower order harmonics. There are two types of PWM rectifiers

- Voltage source PWM rectifier
- Current source PWM rectifier

A voltage source PWM rectifier, illustrated in Figure 9, offers resistor emulation^[11] by controlling the switches and producing a converter input current has a near sinusoidal pulse-by-pulse average. The output of this converter is greater than the peak value of the input line voltage. The output voltage cannot be less than $\sqrt{2}$ times the input peak value. For this reason, this converter is also called a PWM boost rectifier.

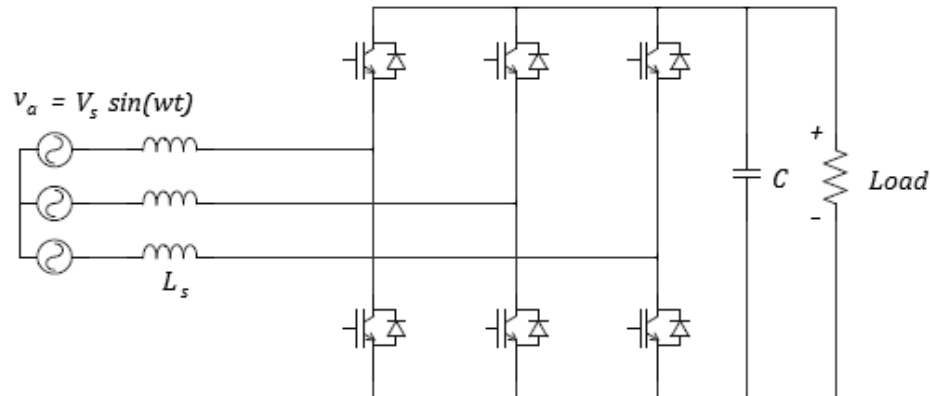


Figure 9: Voltage source PWM rectifier

In a current source PWM rectifier, shown in Figure 10, since IGBT's do not have reverse blocking capabilities the diodes are used to block the reverse voltage that appears at the output of the rectifier. The PWM signals applied maintain a constant current at the output, making the converter input current, pulses of a constant magnitude. Since the input current is a PWM signal, the lower order input current harmonics are eliminated. In this converter the output voltage is less than the input peak voltage so it is also called a PWM buck rectifier.

Since these converters mitigate lower order harmonics, they require smaller filters and have better input power factor than uncontrolled rectifiers and phase controlled rectifiers.

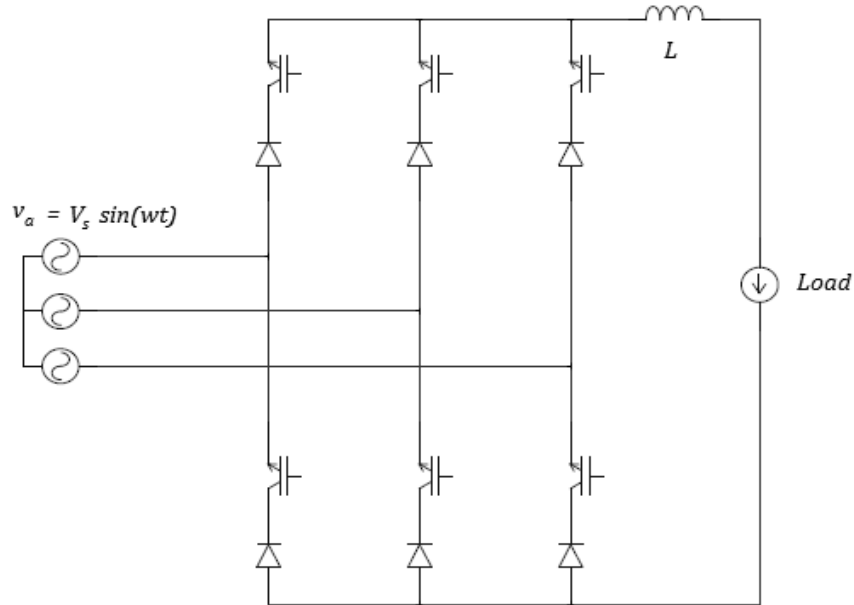


Figure 10: Current source PWM rectifier

PWM rectifiers can be made to operate as PWM inverters as well. They can be made to operate in all four quadrants by suitably adding reverse blocking switches.

2.6 Chapter conclusion

After the study of the different types of rectifiers, their performance characteristics, particularly the controllability of output voltage, distortion factor, displacement power factor and multi-quadrant capabilities are compared in Table 1.

Table 1: Comparison of different types of rectifiers

	Line frequency uncontrolled	Line frequency phase controlled	PWM rectifier
Output voltage	Uncontrollable	Controllable	Controllable
Distortion factor	High	High	Low
Displacement power factor	Low	Dependent on α	Low
Multi-quadrant operation	No	Yes, 1 st and 2 nd quadrants	Yes, 1 st , 2 nd , 3 rd and 4 th quadrants

The PWM rectifier offers great flexibility and most degrees of freedom. The filtering requirements for the PWM rectifier are the least and they are capable of multi-quadrant operation. This makes the PWM rectifier a suitable candidate for the new topology being proposed.

CHAPTER III

STUDY OF AN EXISTING TOPOLOGY FOR AC-DC POWER CONVERSION

As discussed in the previous chapter, one of the converter types used for AC-DC power conversion is a line frequency uncontrolled rectifier. The system taken up for study is based on a line frequency uncontrolled rectifier. The circuit constitutes a diode rectifier followed by a DC-DC converter which creates a current source and a full-bridge converter to produce the voltage level demanded by the load, as illustrated in Figure 11.

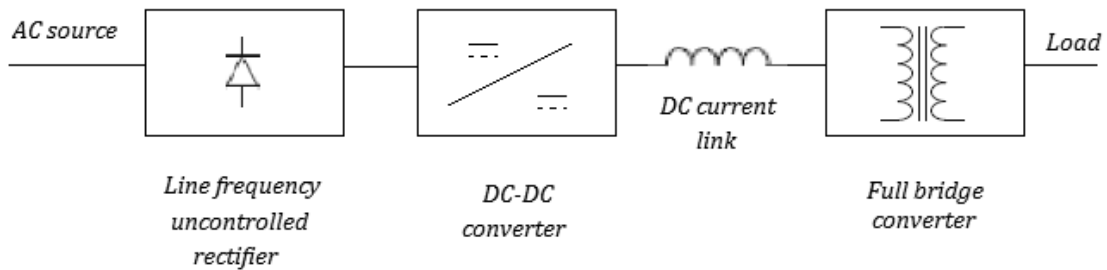


Figure 11: Block representation of an existing topology for AC-DC power conversion

The full-bridge transformer isolation converter used is a current-fed converter. The advantages to using transformer isolation and current source are to be discussed.

3.1 Transformer isolation in converters

The introduction of transformers into DC-DC converters is helpful in the following ways: ^[12]

- Transformers can serve as stages of voltage step-up / step-down, where very high ratios of stepping are needed. High ratios cannot be efficiently obtained only by duty ratio control
- Transformers are a handy solution when complete electrical isolation between input and output is needed. Instead of using a bulky 60 Hz / 50 Hz transformer at the AC side, smaller high frequency transformers can be used in the converter stage
- Multiple winding transformers are used in multi-output DC-DC converters

Whenever power transformers are employed, the average of the voltage across the transformer must be zero. If there is a non-zero DC component in the voltage, the unidirectional magnetic field will saturate the transformer core, which will ultimately result in short-circuiting the source. The solution to this problem is current-fed converters. Transformers in current-fed converters are driven by ampere-turns rather than volt-seconds. This makes saturation of the transformer core, a distant possibility. ^[6]

3.2 Current-fed full-bridge converters

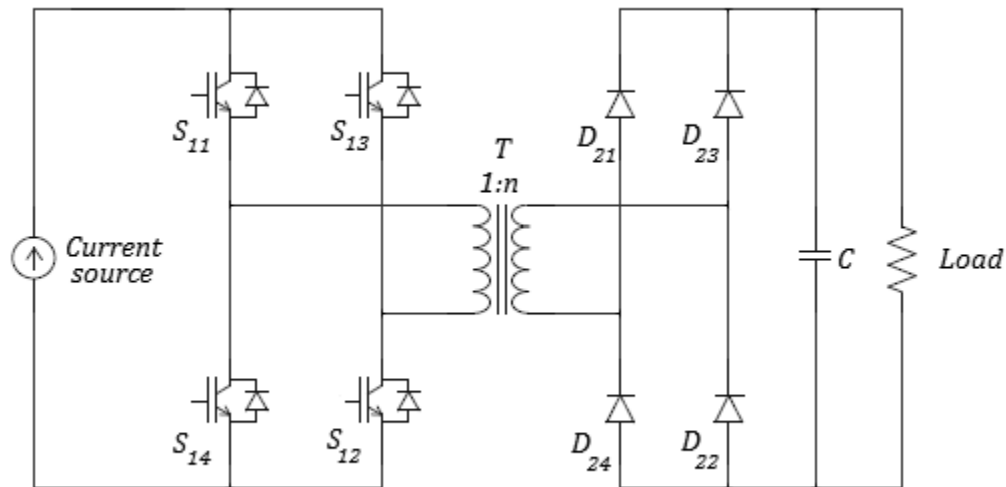


Figure 12: A current-fed full-bridge DC-DC converter

The full-bridge DC-DC converter shown in Figure 12 has a current source for the input and the transformer has a voltage ratio of $1:n$. The secondary side of the transformer has a diode H-bridge and the load side has an output capacitor. The output of the converter shown above is controlled by changing the ON time of the switches S_{11} through S_{14} . The resulting current pulses are stepped up or down in magnitude, depending on the ratio n . The pulses are rectified by the diode bridge and averaged to produce an output current, as demanded by the load. It must be made sure that S_{11} & S_{13} or S_{12} & S_{14} are not open simultaneously since it will result in the current source getting open circuited. The preferred dead time of a current-fed converter is short circuit. Dead

time, if needed, is provided by shorting either one or both of the arms of the primary side bridge.

3.3 Existing topology for current-fed transformer isolated AC-DC conversion

The current source in the current-fed converter has to be created from a voltage source, since current sources are not commonly available. This can be done by employing choppers or buck converters. The overall system consists of three components, as illustrated in Figure 13:

- A three-phase diode rectifier
- A poly-phase chopper to produce the current source
- A current source full-bridge DC-DC converter

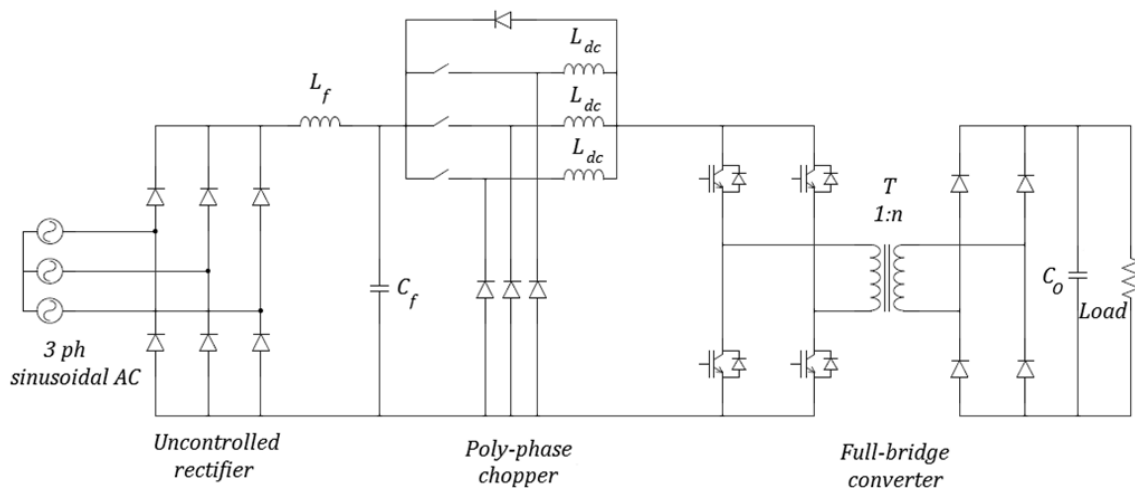


Figure 13: Current-fed full-bridge AC-DC converter with three-phase AC supply

The poly-phase (three-phase in this example) chopper produces a constant current from the constant voltage output of the uncontrolled rectifier, the maximum value of current being limited by the transformer and switch ratings. Using an m -section poly-phase chopper reduces the actual switching frequency m -fold from the required switching frequency. The switching pulses of the switches are displaced by $\frac{360}{m}$ degrees. This also reduces the input filter requirements of the chopper.

PWM gating pulses are applied to the switches S_{11} through S_{14} to produce current pulses, the average value of which is dictated by the output voltage demanded by the load. The inverter frequency is transparent to the output terminals. The control emphasis of the converter can be placed both on the DC-DC converter and the PWM control of the full-bridge.

For purposes of analysis, the full-bridge converter can be imagined to be a simple buck converter, as given below in Figure 14.

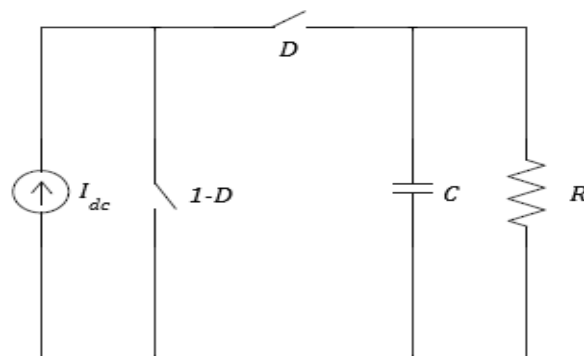


Figure 14: Full-bridge converter modeled as a buck converter for analysis purposes

For the buck converter modeled above, duty cycle is defined as the on time ratio of the switch D .

Output voltage of the converter when the duty cycle is 1 $= I_{dc} R$

Output voltage of the converter when the duty cycle is $D = I_{dc} D R$

If the duty cycle is expressed in terms of the phase angle φ , for which duration the switch is on during a positive or negative half cycle,

$$D = \frac{\varphi}{\pi}$$

$$V_{out} = \frac{\varphi}{\pi} I_{dc} R$$

The gating pulses for the switches S_{11} through S_{14} are as given below in Figure 15. The example shown is for a duty cycle of 33%. For one-third of the switching cycle, the switches are operated to supply the input current to the transformer. For the remaining two-thirds, the first arm of the H-bridge containing the switches S_{11} and S_{13} is short circuited and the current flow is uninterrupted. In other words, this period is called dead-time, the duration of which is dependent on the output voltage as demanded by the load.

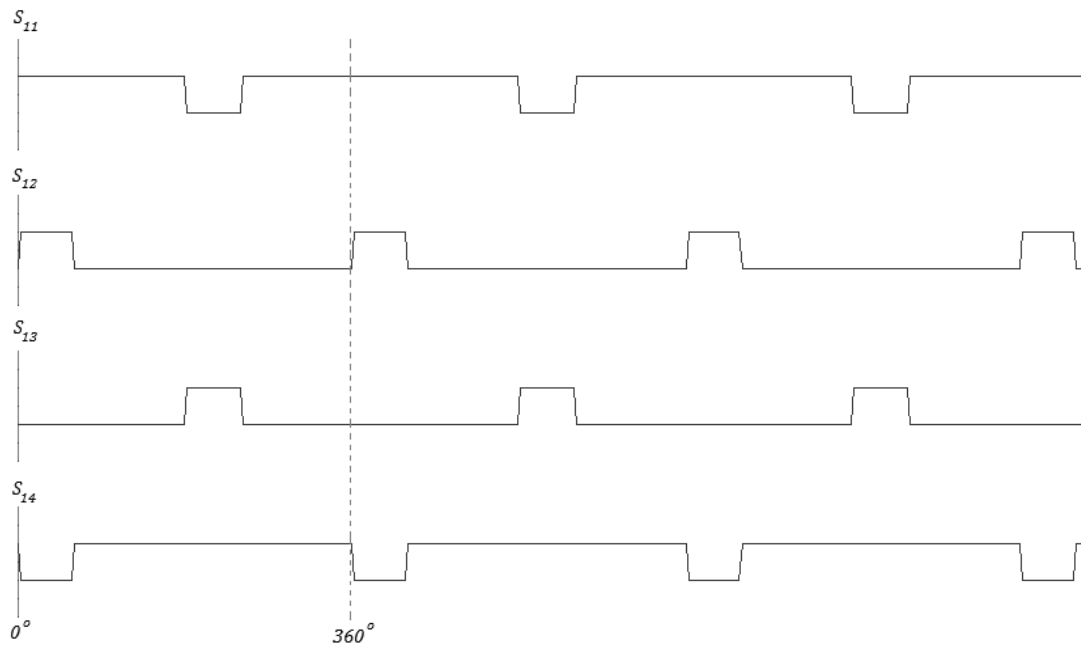


Figure 15: Gating pulses of full-bridge inverter switches

3.4 Design example

A design example for the topology will be discussed with the following specifications.

$$V_{\text{input}} = 1400 \text{ V, line-line rms, three-phase, 60 Hz}$$

$$\text{Output power} = 900 \text{ kW max.}$$

$$\text{Output voltage} = 5 \text{ kV max.}$$

$$\text{Inverter switching frequency} = 800 \text{ Hz}$$

$$\text{Number of phases in multiphase chopper} = m = 3$$

$$\text{Thus, in the per unit system, } P_{\text{base}} = 900 \text{ kW; } V_{\text{base}} = 1400/\sqrt{3}; Z_{\text{base}} = 2.18\Omega; f_{\text{base}} = 60 \text{ Hz}$$

The DC link current ripple is set at 3 A at full load and DC output voltage ripple, at 3%.

The chopper frequency is set at 2400 Hz, three times the inverter frequency. This means each of the three-phase chopper switches has to operate at 800 Hz. The minimum duty cycle of inverter switches is set at 33% to reduce the size of the DC link inductor.

To design the output filter components for the uncontrolled rectifier, the minimum value of inductor required to maintain continuous conduction and the capacitor required to filter out the 360 Hz component of the DC output are to be calculated.

$$L_{min} = \frac{0.0129 V_{LL}}{\omega I_{d,av}}$$

$$C = \frac{I_{d,6}}{6\omega V_d \cdot RF}$$

The DC output voltage from an uncontrolled rectifier is given by the expression

$$\begin{aligned} V_d &= 1.35 V_{LL} \\ &= 1890 \text{ V} \end{aligned}$$

Assuming 60 A to be the lower limit of DC link current, the duty cycle of the chopper turns out to be 0.776. From these values, the inductance and capacitance are calculated to be

$$L_{min} = 1028.9 \mu\text{H} = 0.1779 \text{ p.u.}$$

$$C = 701.75 \mu\text{F} = 1.73 \text{ p.u.}$$

The DC link inductor is designed to give a ripple current of 3 A, when the duty cycle of the inverter is 33%.

$$L_{dc} \frac{di}{dt} = V_d = 1890$$

That gives an L_{dc} value of 262.5 mH.

$$L_{dc} = 0.2625 \text{ H}$$

$$\begin{aligned} L_{chopper} &= L_{dc} \frac{1}{m} \\ &= 87.5 \text{ mH} = 15.13 \text{ p.u.} \end{aligned}$$

The output capacitor is designed to provide a voltage ripple of 3%.

$$\text{Load voltage} = 5 \text{ kV}$$

$$\begin{aligned} \text{Load current at full load} &= 900 \text{ k} / 4690.98 \\ &= 180 \text{ A} \end{aligned}$$

$$\text{Voltage ripple} = 3\% \text{ of } 5 \text{ kV}$$

$$C \frac{dv}{dt} = i$$

$$C = 500 \text{ } \mu\text{F} = 2.434 \text{ p.u}$$

The input current to the converter has harmonics starting from the 5th harmonic (300Hz).

So the input low pass LC filter and the RC damper are made to resonate at 150 Hz.

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}}$$

$$f_d = \frac{1}{2\pi R_d C_d}$$

$$L_f = 3.25 \text{ mH} = 0.56 \text{ p.u.}$$

$$C_f = 346.4 \text{ } \mu\text{F} = 3.51 \text{ p.u.}$$

$$C_d = 173.2 \mu F = 7.02 p.u.$$

$$R_d = 6.13 \Omega = 2.81 p.u$$

3.5 Simulation and results

The designed converter is constructed in PSIM and the circuit is digitally simulated with a step-size of $10 \mu s$. Besides the converter's performance in delivering the specified output voltage, the input current harmonic profile and the input power factor are also studied.

The simulated waveforms for the DC link current and the DC output voltage at the full load conditions are given in Figure 16.

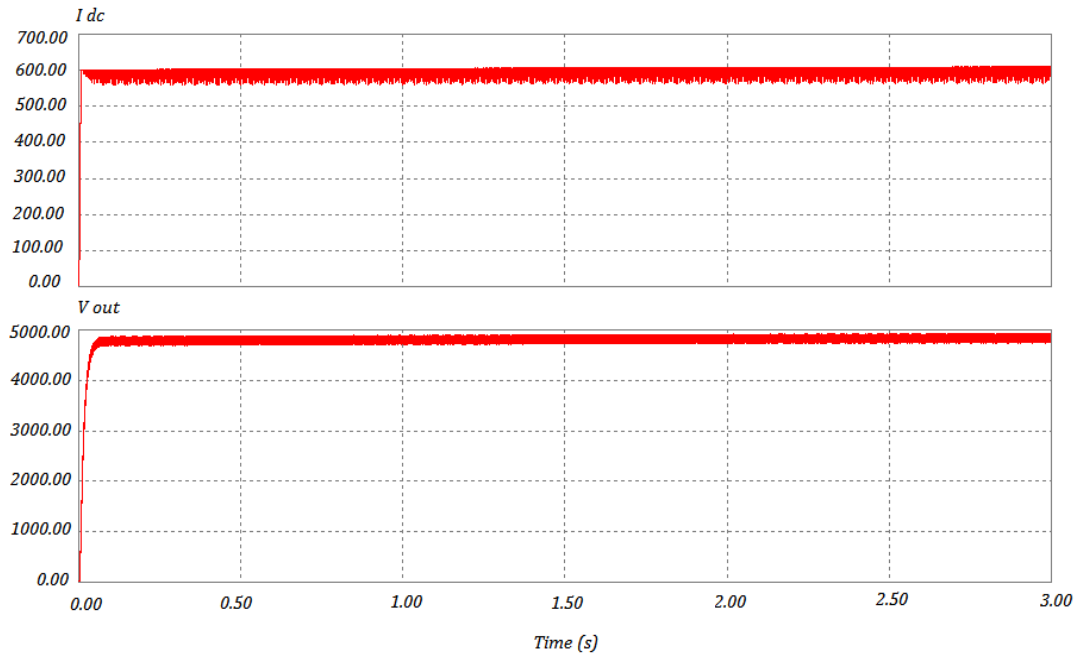


Figure 16: DC link current and converter DC output voltage with 3% ripple, at full load

The input current to the converter is analyzed in the frequency domain in Figure 17. The Total Harmonic Distortion (%THD) is calculated to be 73.5% for the unfiltered input current.

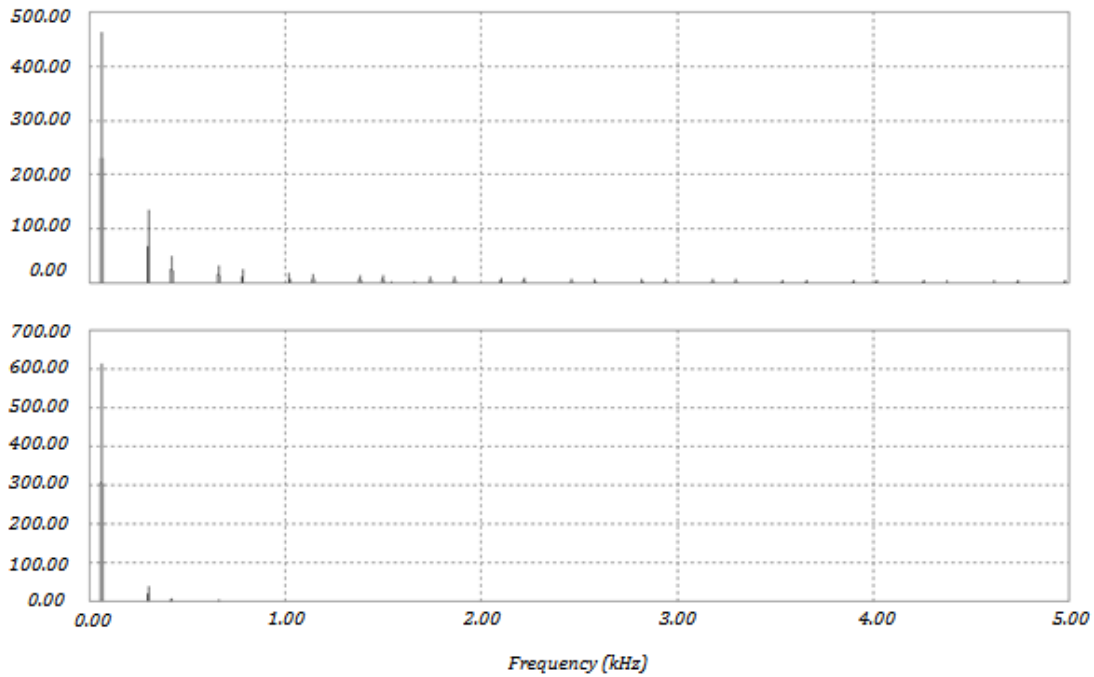


Figure 17: Converter AC input current in the frequency domain, filtered and unfiltered currents

To perform a Fourier analysis, the line current drawn from the mains can be expressed as

$$i_s = \sqrt{2} I_{sf} \sin(\omega_f t - \varphi_f) + \sum_{h \neq 1} \sqrt{2} I_{sh} \sin(\omega_h t - \varphi_h)$$

where I_{sf} is the rms of the fundamental component of the current and I_{sh} is the rms of the h-harmonic component.

Harmonic distortion current (rms) is given by the expression

$$I_{dis} = \sqrt{\sum_{h \neq 1} I_{sh}^2}$$

The percentage total harmonic distortion of current can be expressed as

$$\% \text{ THD} = \frac{I_{dis}}{I_{sf}} * 100 \%$$

The power factor is then calculated as

$$pf = \frac{1}{\sqrt{(1+THD^2)}} \cos \varphi$$

where $\cos \varphi$ is the displacement power factor of the input line current.

Table 2 in the following page, gives the significant harmonic components of the converter input current normalized with respect to the fundamental component, for different load levels. The total harmonic distortion of the input current of the converter and hence the power factor are also calculated. The lowest order harmonic is the 5th harmonic and the triplen harmonics are absent.

Table 2: Table of converter input current harmonics, normalized with respect to the fundamental component

DC link current	Converter input AC current harmonics, normalized to the fundamental									
Load level (p.u)	Fundamental (60)	5th (300)	7th (420)	11th (660)	13th (780)	17th (1020)	19th (1140)	23rd (1380)	25th (1500)	29th (1740)
1	1	0.30	0.41	0.43	0.29	0.02	0.08	0.05	0.04	0.000
0.73	0.850	0.29	0.37	0.46	0.31	0.03	0.08	0.04	0.02	0.000
0.51	0.588	0.30	0.34	0.34	0.22	0.07	0.08	0.03	0.02	0.011
0.375	0.433	0.32	0.32	0.26	0.17	0.09	0.07	0.02	0.01	0.012
0.28	0.331	0.30	0.28	0.20	0.16	0.09	0.06	0.02	0.01	0.015
0.225	0.263	0.24	0.22	0.16	0.13	0.08	0.05	0.02	0.01	0.012
0.18	0.210	0.20	0.18	0.13	0.11	0.06	0.04	0.02	0.01	0.009
0.17	0.199	0.18	0.17	0.13	0.11	0.06	0.04	0.02	0.01	0.010
0.14	0.162	0.15	0.14	0.11	0.09	0.05	0.04	0.01	0.01	0.007
0.125	0.139	0.13	0.12	0.09	0.08	0.05	0.03	0.01	0.01	0.006

Figure 18 gives the THD of the unfiltered converter input current and the distortion factor, for different load levels. The displacement power factor for an uncontrolled rectifier is high, above 0.99 for all ranges of load. So the distortion factor reflects the overall power factor also, since power factor is only the product of distortion factor and displacement power factor. From the figure, we observe that the minimum THD achieved is 73.5% and the power factor is 0.806 at full load.

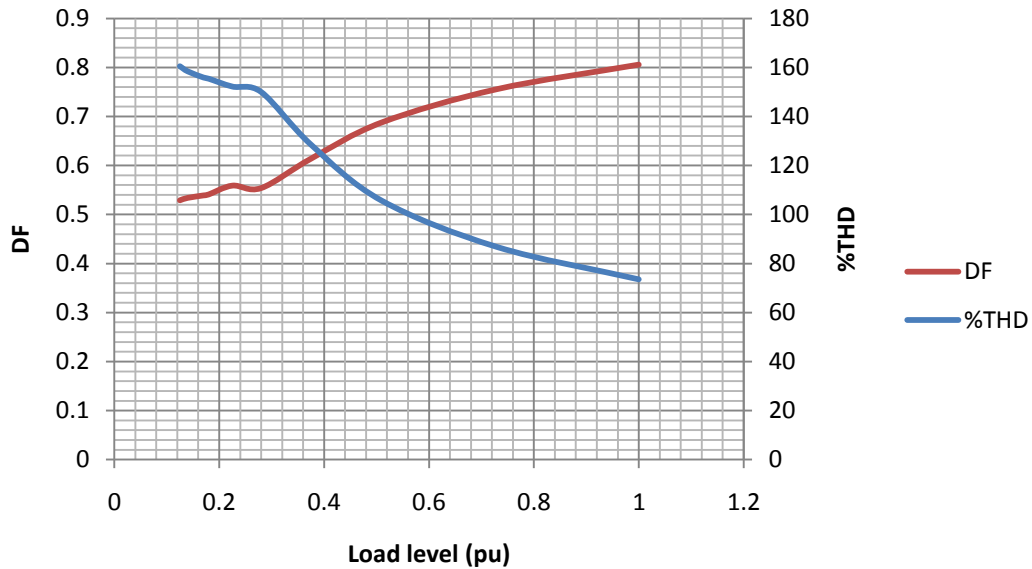


Figure 18: THD and distortion factor of the unfiltered converter input current for existing topology

3.6 Chapter conclusion

The topology studied in this chapter is a line frequency uncontrolled rectifier followed by a current-fed full-bridge DC-DC converter. The design example is simulated using PSIM and the performance characteristics such as input power factor and total harmonic distortion are observed. The converter draws a high amount of lower order harmonics and as a result the input power factor is low. Power factor correction could require heavy filters or additional power factor correction circuits. Any alternative topology proposed should include solutions to these problems.

CHAPTER IV

PROPOSED TOPOLOGY FOR HIGH POWER AC-DC CONVERSION

The line frequency, uncontrolled rectifier discussed in the previous chapter was proven to be of low power quality, as a result poor efficiency and as being overloading the circuitry. To address these problems and also to make the topology operational in all the four quadrants of the V-I plane, the following improvements are proposed.

1. The line frequency uncontrolled rectifier has three power conversion stages. The new topology will have a reduced number of power conversion stages by combining the front end uncontrolled rectifier and the DC-DC converter forming a controlled rectifier thereby improving efficiency
2. The controlled rectifier is to be switched at a high frequency, leading to mitigation of lower order harmonics. This calls for a PWM rectifier with IGBT's
3. The IGBT switches are to be accompanied by reverse blocking switches enabling the reversal of voltage and current thereby making four quadrant operation possible

The proposed converter will feature an AC input LC filter to attenuate the higher order harmonics stemming from the switching of PWM rectifier.

4.1 Description of proposed topology

The proposed topology, shown in Figure 19, consists of an IGBT based fully controlled rectifier forming a DC link which supplies a medium frequency transformer isolation full-bridge DC-DC converter.

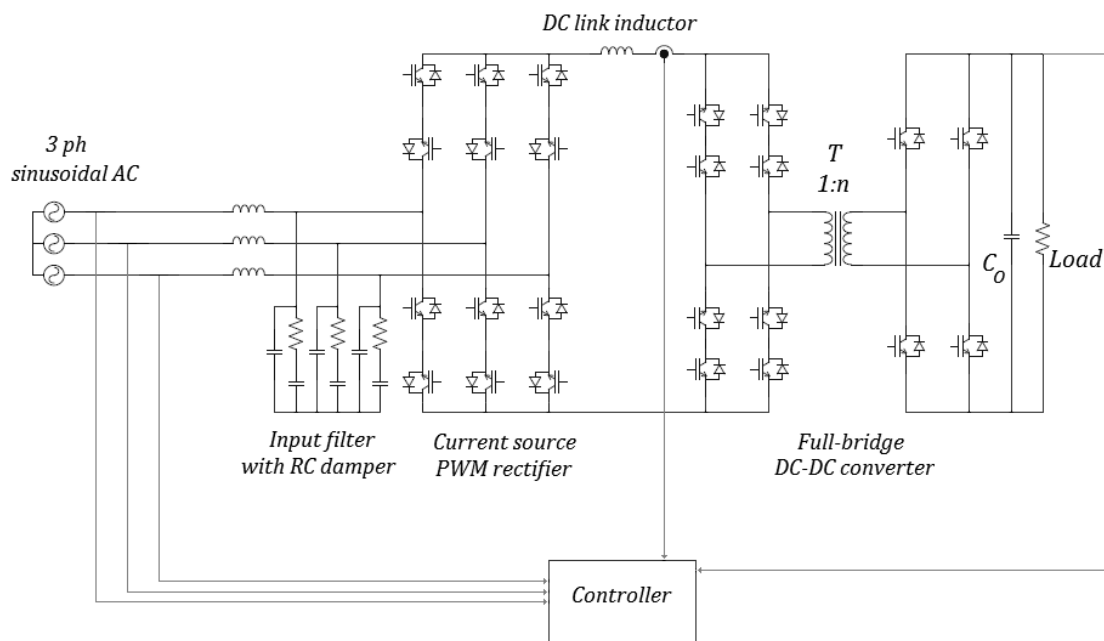


Figure 19: Proposed topology for multi-quadrant high power AC-DC converter

The switches in the fully controlled rectifier are operated to produce a constant DC current in the DC link inductor. This generates the current source needed to feed the current-fed full-bridge converter, which in turn produces the DC output voltage at the

output capacitor. The rectifier has a front end LC filter with an RC damper to attenuate the harmonics.

4.2 Multi-quadrant capabilities

The circuit is fully capable of operating in all four quadrants of the V-I plane. During forward operation, the fully controlled rectifier is supplied with PWM gating signals by the controller to produce a constant DC link current. This current is fed to the transformer through the full-bridge, whose switches are controlled to provide a constant DC voltage at the load. The switches connected in opposite fashion only serve to block the reverse voltage during forward operation and they are either switched on or switched off continuously depending on their orientation.

During regenerative operation, the oppositely connected switches are controlled. The full-bridge converter operates the same way in the reverse direction, controlling the DC link current. The fully controlled rectifier produces PWM voltages which when passed through the filter, produce sinusoidal voltages.

4.3 Control algorithm: Selective Harmonic Elimination and programmed PWM

In calculating the switching angles for the PWM rectifier/inverter, two methods may be used. They are (a) Carrier modulated sine wave PWM and (b) Programmed PWM. Of these, the programmed PWM method employs Selective Harmonic Elimination (SHE) to

selectively eliminate lower order harmonics to zero. The programmed PWM method has the following advantages over carrier modulated sine wave PWM.^[7]

- Reduction in switching frequency for the same performance, thereby reducing switching losses
- High voltage gain through overmodulation
- Precalculation of switching angles gives a lookup table, eliminating the need for online computations. This also eliminates the need for high speed microprocessors.

In the programmed PWM technique, the harmonic elements in the Fourier series are mathematically eliminated to derive solutions for switching functions. Among the many programmed PWM techniques, the TLL technique aims to optimize line-line waveforms whereas the TLN techniques optimize line-neutral waveforms. There are two TLN techniques: TLN1 has switching angles spread over 90° and TLN2, over 60° . TLN2 technique is used because, with folding symmetry, the switching angles are spread over 120° , the duration for which each switch conducts in a three-phase rectifier or inverter. The TLN2 technique also has a high voltage gain among all the techniques available.

The TLN2 technique used in the proposed converter has a PWM switching function with 20 switching angles. The switching function is illustrated in Figure 20. The leading edge of the first PWM pulse coincides with 30° of the phase voltage and the trailing edge of the twentieth pulse coincides with 150° of the phase voltage.

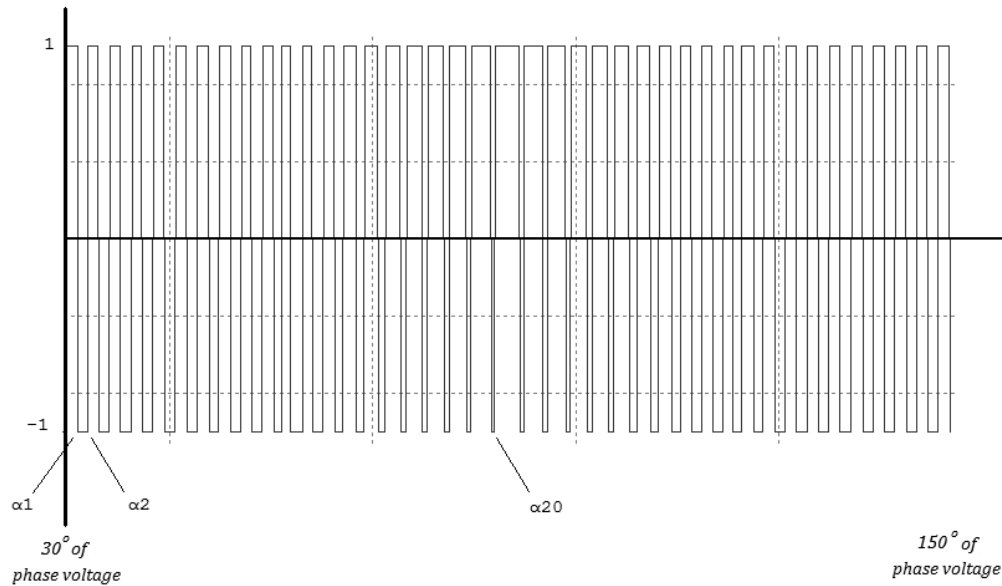


Figure 20: Programmed PWM switching function with $N = 20$

The Fourier coefficients of the TLN2 switching pattern are given by

$$a_n = \frac{4}{n\pi} \left[1 + 2 \sum_{k=1}^N (-1)^k \cos(n \alpha_k) \right]$$

$$b_n = 0$$

The switching angles α_1 through α_{20} are found out after equating all $a_n = 0$, thereby equating all harmonic elements to zero.

$$\begin{bmatrix} -2 \cos \alpha_1 & \cdots & 2(-1)^N \cos \alpha_N \\ \vdots & \ddots & \vdots \\ -2 \cos(x_2)\alpha_1 & \cdots & -2(-1)^N \cos(x_2)\alpha_N \end{bmatrix} = \begin{bmatrix} \frac{\pi a_1}{4} + 1 \\ \cdots \\ -1 \end{bmatrix}$$

$$N = 20; x_2 = 3N - 1 = 59$$

Solving these non linear equations ^{[13],[14]} for all values of a_1 between 0 and 1, sets of switching angles can be derived for each a_1 . The switching angles α_1 through α_{20} are nonlinear functions of a_1 , let it be called the variable v .

$$\alpha_1 = f_1(v)$$

...

...

$$\alpha_{20} = f_{20}(v)$$

The solution trajectories for switching angles α_1 through α_{20} for varying v are given in Figure 21. The nonlinearities appear towards the very end, near $v = 1$. Neglecting the nonlinearities, a lookup table for each switching angle α_1 through α_{20} can be generated for each value of v .

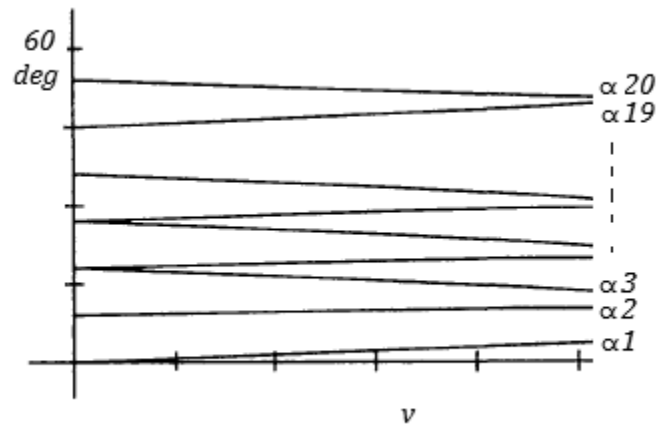


Figure 21: Switching angles as functions of variable 'v'

The switching angles α_1 through α_{20} are mirrored on 90° of the phase voltage to produce the angles α_{21} through α_{40} .

The switching frequency of this technique is given by

$$f_s = (2N + 1)f$$

where $N = 20$, $f = 60$ Hz; giving a switching frequency of 2460 Hz.

4.4 First quadrant operation

In the first quadrant of the V-I plane, the converter transfers power from the source port to the load port. The front end fully controlled converter acts as a rectifier providing a DC link current. In this mode, there are two control variables and emphasis can be placed on either or both variables:

- The variable ' v ' as discussed before, determines the PWM switching function for the rectifier
- The duty cycle of the full-bridge DC-DC converter

Figure 22 describes the controller of the converter in the first quadrant operation. The switching angles for each switch are individually generated after calculating the 60 ms block average (per AC cycle) of the DC link current. The switching angles are converted into switching time instances. The controller then keeps track of time and it turns on or off the switch at these switching time instances.

4.5 First quadrant controller

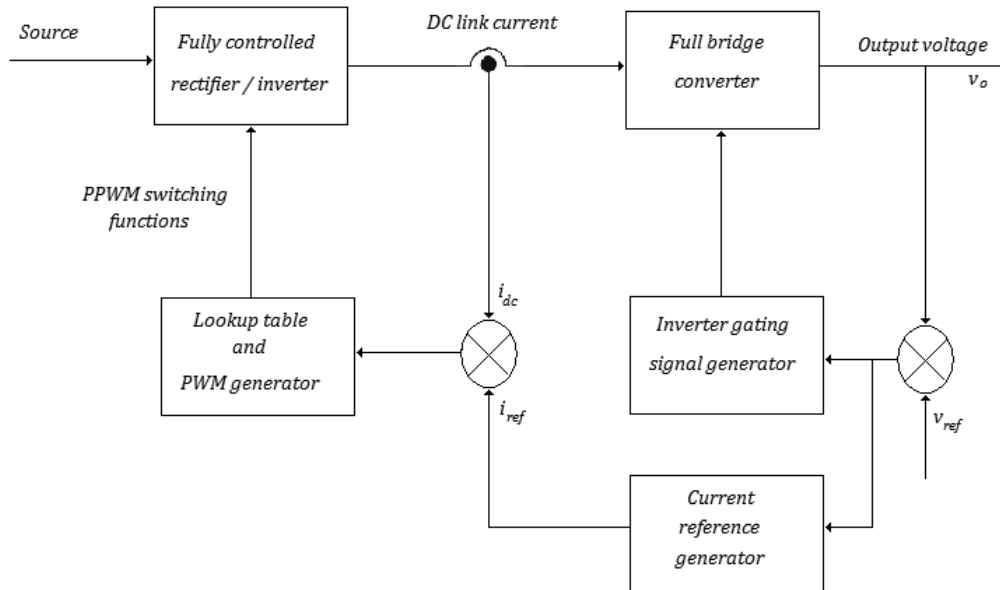


Figure 22: Block diagram of controller for first quadrant operation of converter

The proposed converter has two loops, a voltage loop and a current loop. The voltage loop compares the output voltage of the converter with the reference voltage and based on the error, generates the current reference. The duty cycle of the full-bridge converter is also determined by this loop. The voltage loop uses a simple proportional feedback system. This is also the faster of the two loops, enabling quicker settling times.

The inner current loop generates the switching functions for the rectifier switches to track the current reference, as generated by the voltage loop. The current loop uses a variable step-size control to incrementally change the variable ‘ v ’ depending on the DC link current. The algorithm is described in Figure 23 in the following page.

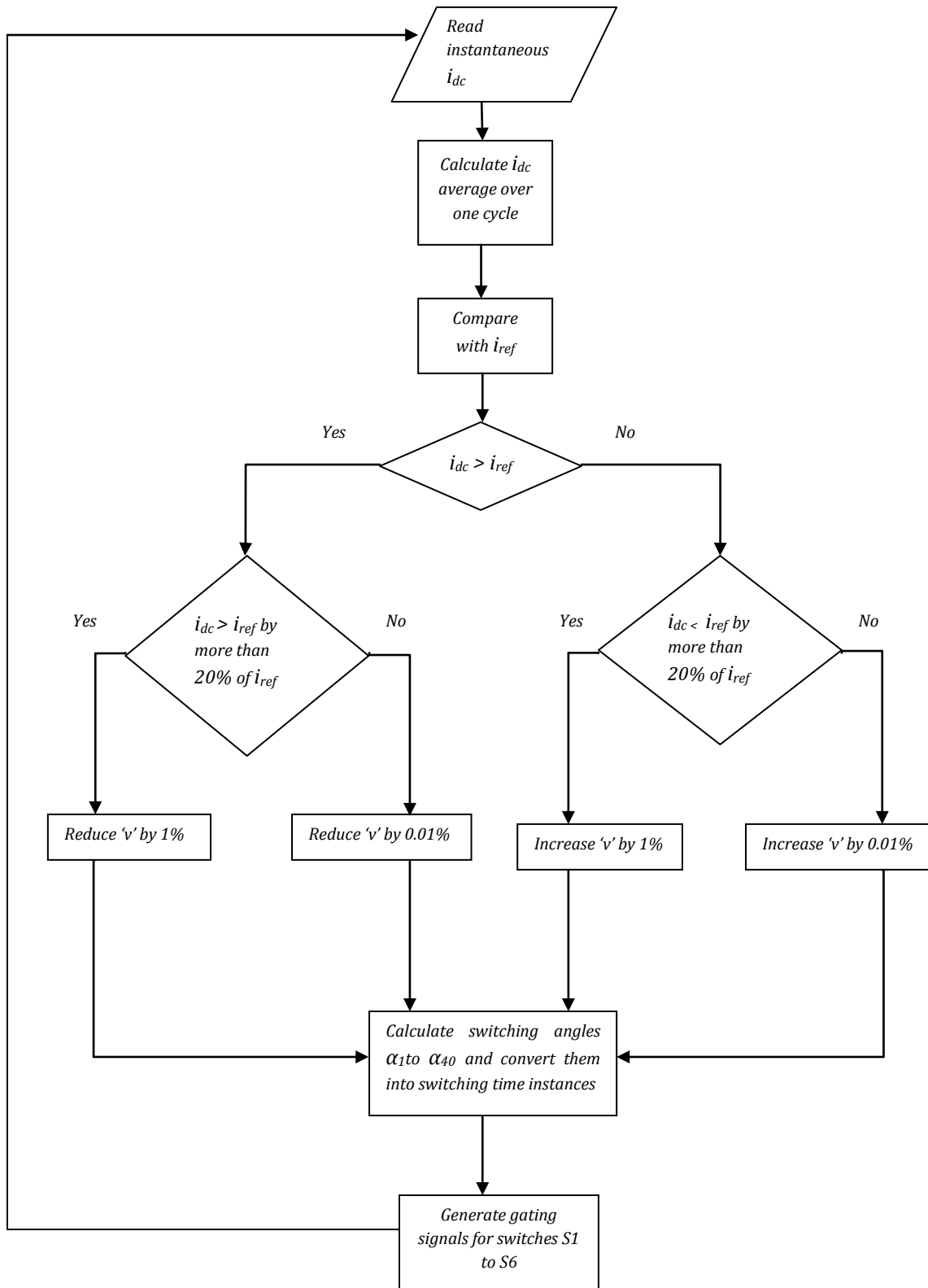


Figure 23: Algorithm to generate PWM switching functions for rectifier

When the PWM switching functions are generated and the gating signals are applied to the switches, there are instances when all the switching functions have zero value. These states are called zero states. But we have a DC link inductor acting as a current source which cannot be open circuited. To prevent that, we turn on one leg of the fully controlled rectifier which provides a freewheeling path for the inductor current. A particular leg is turned on only when the phase connected to that leg is not one of the two phases carrying the line current. The freewheeling paths are chosen in the following fashion, depicted in Figures 24, 25 and 26. The switching instances for this additional switching are generated by digital logic circuits.

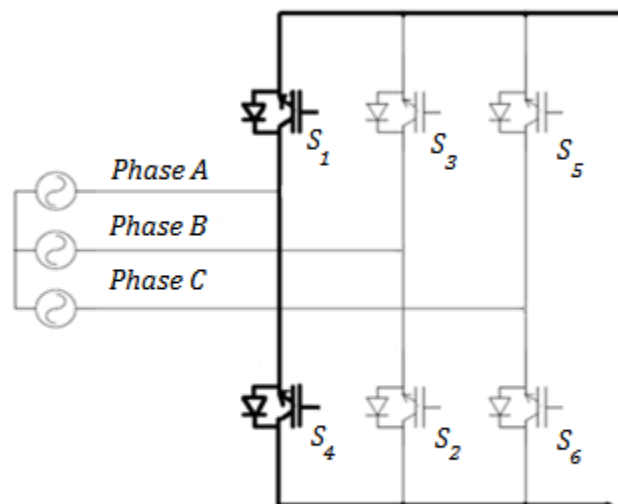


Figure 24: Choice of freewheeling path, angles with respect to phase 'a': 0° to 30° ,
 150° to 210° , 330° to 360°

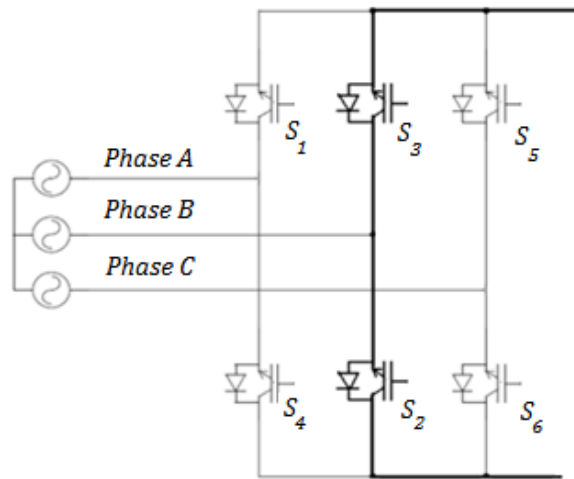


Figure 25: Choice of freewheeling path, angles with respect to phase 'a': 90° to 150° ,
 270° to 330°

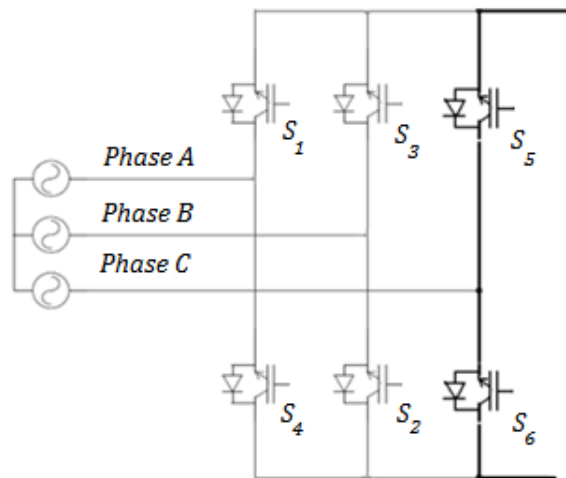


Figure 26: Choice of freewheeling path, angles with respect to phase 'a': 30° to 90° ,
 210° to 270°

4.6 Boosting action in full-bridge converter in the first quadrant

As discussed before, the switches in the primary side of the full-bridge converter are controlled (duty cycle = D) to produce a constant DC voltage. The dead states in the inverter are provided by shorting one of the legs of the bridge since it is a current-fed inverter as against opening all switches in the case of a voltage fed inverter. The inverter circuit can be redrawn as below in Figure 27 for purposes of analysis.

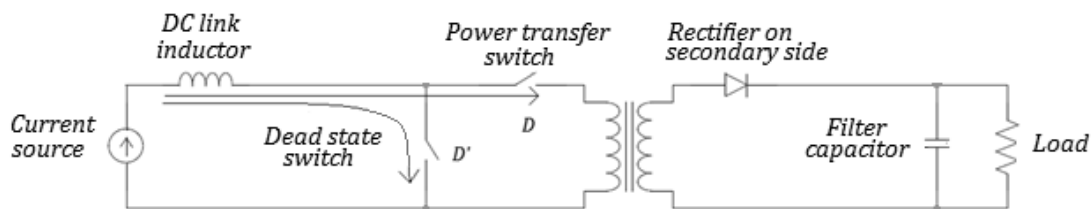


Figure 27: Full-bridge converter drawn as a boost converter

From the circuit it can be seen that the inductor and capacitor, in combination with the primary side switches and secondary side diodes, form a boost converter. The inductor charges during the dead states (D') and discharges during the power transfer state (D). This boosts the output voltage by a factor of $\frac{1}{1-D}$. Alternatively, the DC link current is boosted since the energy transfer to the inductor happens for a duration D' .

$$V_o I_o = V_{in} I_{in}$$

$$V_o = \frac{V_{in}}{1 - D'}$$

$$I_o = \frac{V_{in}}{(1 - D')R}$$

$$\Rightarrow I_{in} = \frac{V_{in}}{(1 - D')^2 R}$$

The DC link current varies non-linearly against duty cycle D , for a constant v .

4.7 DC link inductor modes of operation

The switches in the rectifier and inverter operate independently to produce constant DC link current and DC output voltages. This gives rise to four modes of operation of the inductor, as illustrated in Figure 28.

When both the source and the load are connected to the DC link inductor as in Figure 28(a) it is the “Direct power transfer mode” wherein power from the source is directly transferred to the load.

When the source is connected to the inductor and the load side is shorted as in Figure 28(b) the inductor current rises, increasing the energy in the inductor. This is the “Inductor charging mode”.

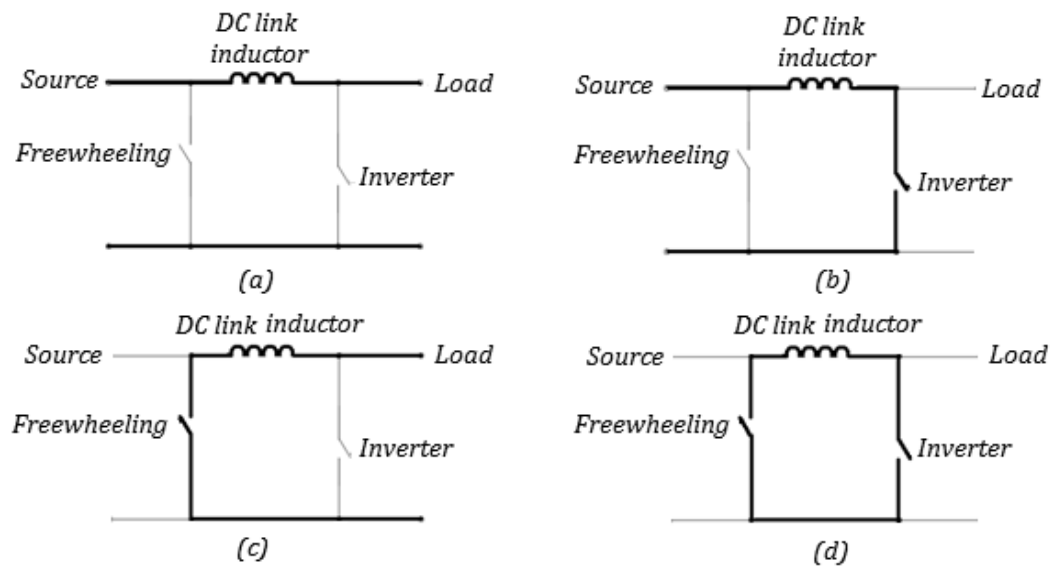


Figure 28: DC link inductor modes of operation

When the source is disconnected from the inductor and the load is supplied by the inductor as in Figure 28(c) it is called “Inductor discharging mode”.

When both the source and the load are disconnected from the inductor as shown in Figure 28(d), the inductor current freewheels through the rectifier and inverter switches. This is called the “Inductor freewheeling mode”.

4.8 Fourth quadrant operation

To operate in the fourth quadrant of the V-I plane, the converter reverses the direction of current but the direction of voltage remains the same as the first quadrant. In place of the

load, there is a DC voltage source in the form of a battery, a dynamic load or a renewable energy source such as fuel cell.

The switches in operation are the same as in the first quadrant, in the full-bridge rectifier. The IGBTs on the secondary side of the full-bridge converter are switched to produce a constant DC link current. The IGBTs on the primary side are not gate grounded and their body diodes rectify the square wave form at the primary side of the transformer.

The top switches in the front end fully controlled rectifier, shown before in Figure 19, which served the purpose of reverse blocking in the first quadrant operation, are now supplied with the programmed PWM switching function.

The duty cycle of the full-bridge converter is the only available control variable in fourth quadrant operation and the front end programmed PWM inverter is operated supply the maximum average voltage at the AC side, meaning that the variable v is always set at 1. The AC side filter eliminates the higher order harmonics to provide a cleaner fundamental frequency wave.

In case of synchronization applications with the utility grid, the converter starts transferring power as soon as the instantaneous phase voltage at the AC side of the converter exceeds the instantaneous phase voltage of the three-phase supply. The AC filter now operates with the source impedance of the utility grid as the load.

4.9 Fourth quadrant controller

The controller block diagram of the converter for fourth quadrant operation is given below in Figure 29.

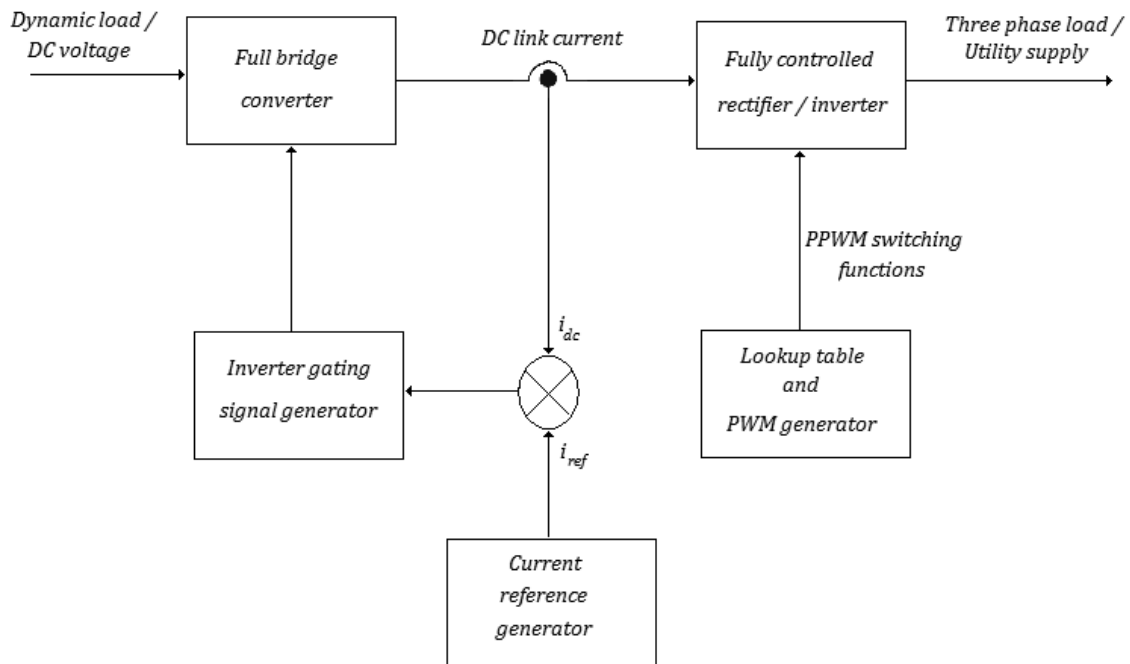


Figure 29: Controller block diagram for fourth quadrant operation

The controller has only one feedback loop, the current loop. The current reference generator calculates the DC link current with is then fed to the inverter gating signal generator which compares it with the feedback DC link current and the error is used to calculate the duty cycle of the full-bridge converter. The programmed PWM generator produces PWM switching functions to maximize the AC voltage at the output.

The switches in the front end fully controlled inverter that are directed to drive current from the DC link current to the AC side are operated by the programmed PWM switching functions generated by the controller. The TLN2 programmed PWM waveform with 20 pulses per cycle is given again in Figure 30 below for reference.

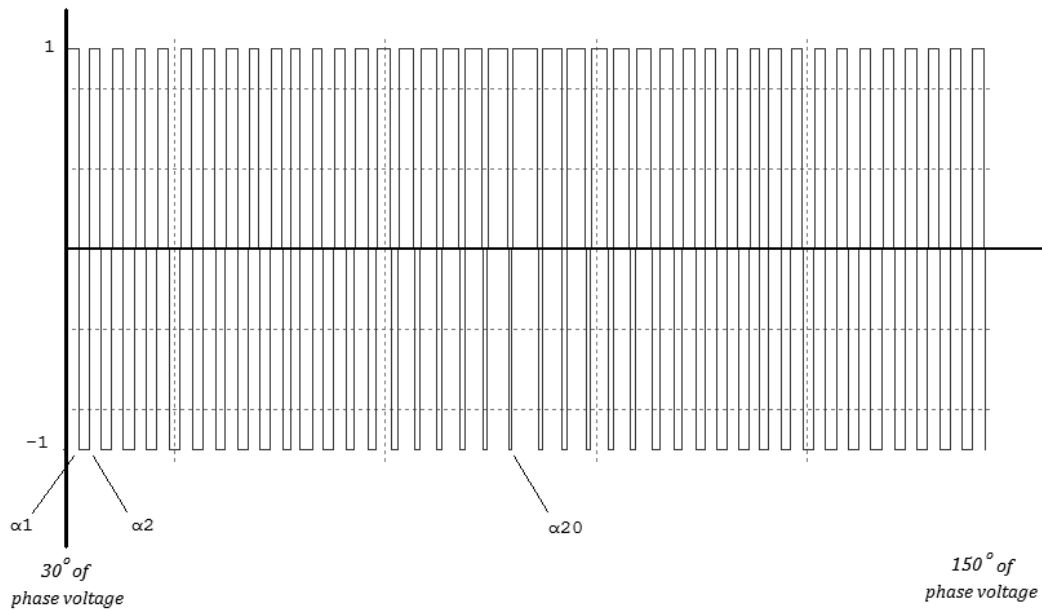


Figure 30: Programmed PWM switching function, reproduced

When the programmed PWM switching function for one of the phases is in the +1 (high) state, the top switch of the corresponding bridge is turned on. When the gating signal is in the -1 (low) state, the bottom switch is turned on. The description of switches selected is given in Figure 31 in the following page.

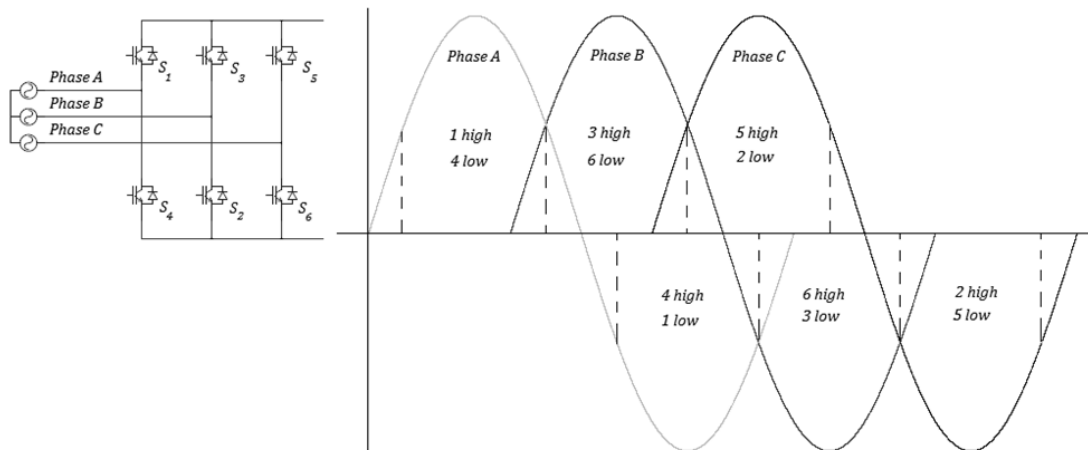


Figure 31: Programmed PWM switching functions in the inverter switches, fourth quadrant operation

As in the first quadrant operation, the switches in the front end converter are also used in freewheeling mode to allow the DC link current to flow continuously during dead states. The switches are chosen based on the phase A reference angle. During any instance, the one bridge which does not carry the line current is chosen as the freewheeling path.

4.10 Full-bridge converter operation in fourth quadrant

As discussed before, the gates of the switches on the full-bridge primary side S_{11} through S_{14} are grounded and the body diodes produce the DC link current I , shown in Figure 32.

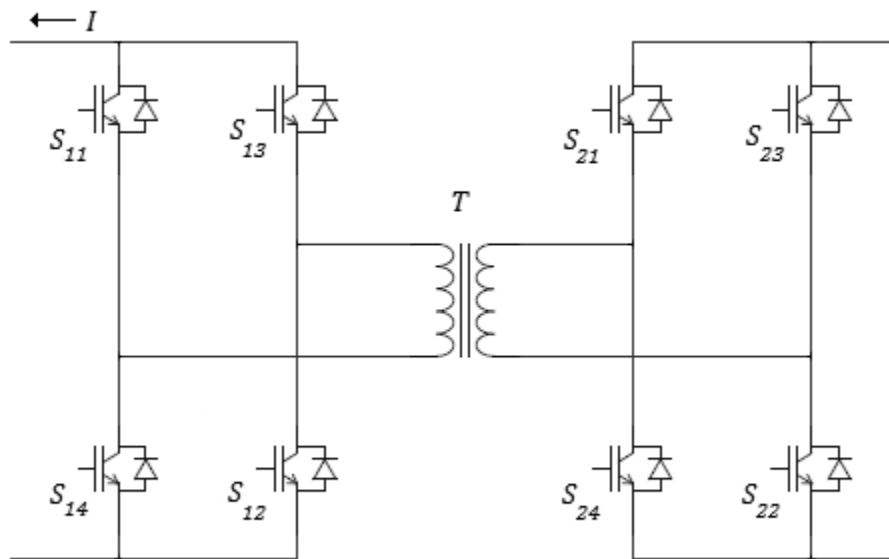


Figure 32: Full-bridge converter with direction of current I in the fourth quadrant

The duty cycle of switches S_{21} through S_{24} is calculated by the controller to produce a constant DC link current. The algorithm used to calculate the duty cycle of the switches is given in Figure 33, in the following page.

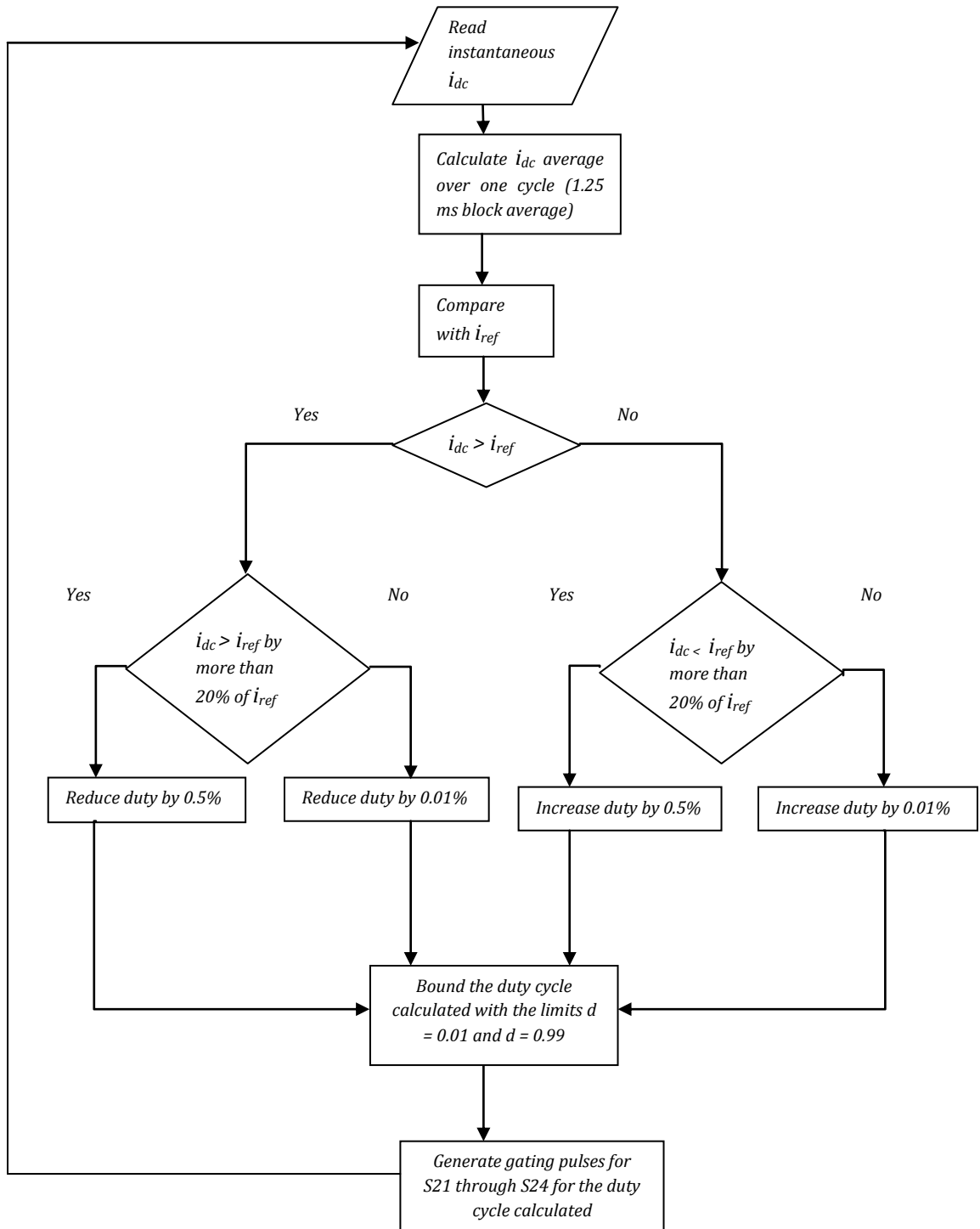


Figure 33: Algorithm to generate gating pulses for the full-bridge converter in fourth quadrant operation

But the switches S_{21} through S_{24} also require additional switching in order to keep the DC link inductor current freewheel through the body diodes of S_{11} through S_{14} without interruption, during the dead states. This is accomplished by grounding the two bottom switches, S_{22} and S_{24} . The logic circuit used is a NOR circuit, which produces a “TRUE” state when both the positive half cycle switches and the negative half cycle switches tend to be off. The logic circuit is given in Figure 34.

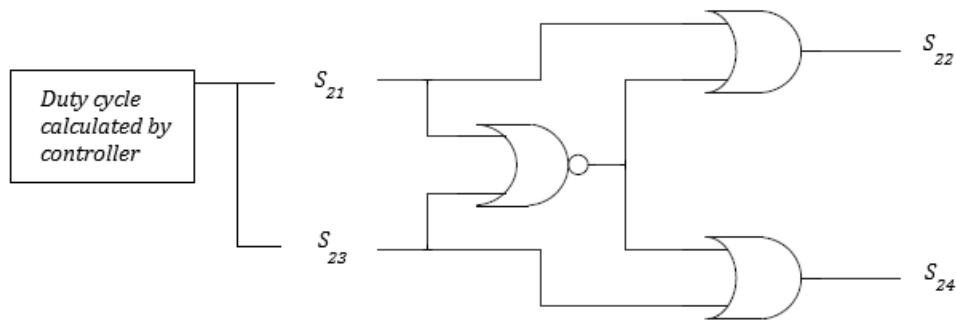


Figure 34: Logic circuit for full-bridge converter gating signals

4.11 Chapter conclusion

The construction, operation and control of the multi-quadrant high power quality AC-DC converter were discussed in this chapter. The algorithms used to generate the switching signals were also explained. In the following chapter, a design problem is discussed, simulated and the results will be examined.

CHAPTER V

DESIGN EXAMPLE AND SIMULATION RESULTS

In this chapter the design of the multi-quadrant high power quality AC-DC converter and the controller discussed previously are tested using a design example.

5.1 Design example

The following specifications are selected as the design parameters.

Three-phase supply $V_{\text{input}} = 1400$ V, line-line rms at 60 Hz

Output power = 900 kW

Output voltage = 4.5 kV

Inverter switching frequency = 800 Hz

Minimum duty cycle of current-fed converter = 33%

In the per unit system, $P_{\text{base}} = 900$ kW; $V_{\text{base}} = 1400/\sqrt{3}$; $Z_{\text{base}} = 2.18\Omega$; $f_{\text{base}} = 60$ Hz

Performance specifications at full load:

- DC link current ripple = 3 A
- DC output voltage ripple = 3%
- Total Harmonic Distortion < 5% (IEEE 519 standards)
- Input power factor > 0.95 lagging (DoE standards)

The DC link inductor, DC output capacitor and the AC side low pass filter are the components to be designed and the converter is to be simulated in both the first and the fourth quadrants.

5.2 DC link inductor design

From the Fourier analysis of the programmed PWM switching function applied to the fully controlled rectifier, the rectified output voltage has a DC component and higher order harmonics with the first significant component being the 61st harmonic. At the other side of the inductor, the inverter switches operate at 800 Hz square wave, reflecting on the inductor as 1600 Hz. To calculate the average voltage across the inductor as applied from the source, the average of the uncontrolled rectified wave is impressed against the programmed PWM function as illustrated in Figure 35.

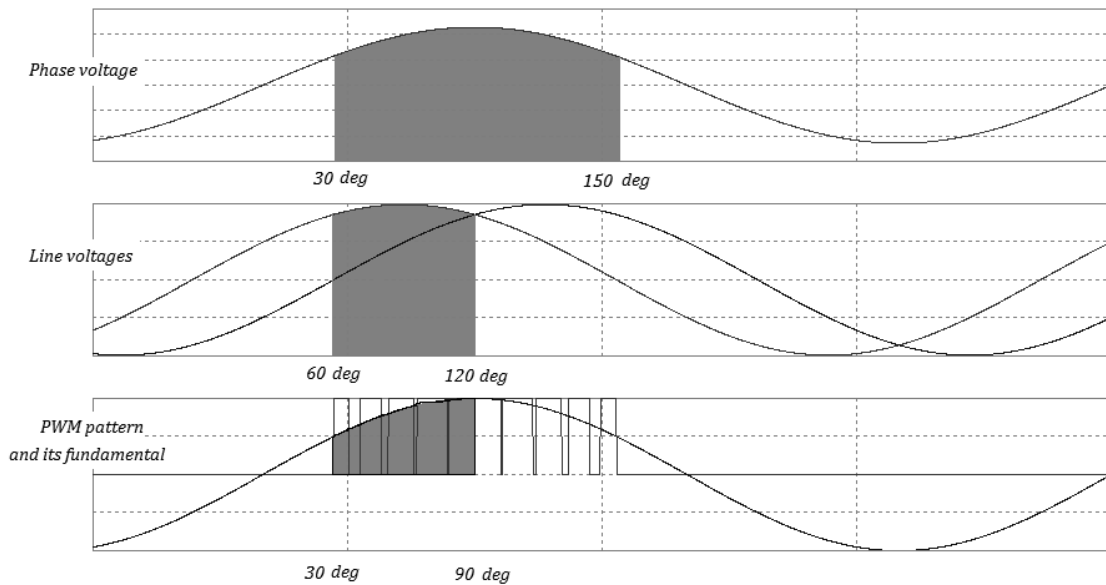


Figure 35: Calculation of average voltage across DC link inductor

From the diagram, the average voltage is calculated to be

$$\begin{aligned}
 V_{ave} &= \frac{3}{\pi} \int_{\frac{\pi}{6}}^{\frac{\pi}{2}} \sin(\omega t) d(\omega t) \cdot \frac{2}{(\pi/3)} \int_{\frac{\pi}{3}}^{\frac{2\pi}{3}} \sqrt{2} \cdot (1400) \sin(\omega t) d(\omega t) \\
 &= \frac{3\sqrt{3}}{2\pi} \cdot \frac{3}{\pi} \cdot \sqrt{2} \cdot (1400) \\
 V_{ave} &= 1563.65 \text{ V}
 \end{aligned}$$

When the full-bridge converter switches are shorted to provide dead states in the current-fed converter, the inductor current increases because of energy transfer from the rectified DC output. The minimum duty cycle of the full-bridge converter is set at 33% as before. So the inductor is applied to the load for a minimum of 33% duty cycle of 1600 Hz. This means the inductor gets charged for a maximum of 66% duty cycle of 1600 Hz.

$$L \frac{di}{dt} = V_{ave}$$

$$L = 1563.65 \frac{2}{3} \cdot \frac{1}{1600} \cdot \frac{1}{3}$$

$$L = 217.2 \text{ mH} = 37.56 \text{ p.u.}$$

5.3 Output capacitor design

The full-bridge converter also acts to boost the DC voltage providing a maximum boost ratio of 3. This results in a theoretical maximum DC output voltage of $3 \cdot 1563.65$, i.e. 4690.98 V.

$$\text{Load voltage} = 4690.98 \text{ V}$$

$$\text{Full load} = 900 \text{ kW}$$

$$\text{Load current at full load} = 900 \text{ k} / 4690.98$$

$$= 191.86 \text{ A}$$

$$\text{Voltage ripple} = 3\% \text{ of } 4690.98 \text{ V}$$

$$C \frac{dv}{dt} = i$$

$$C = 191.86 \frac{2}{3} \cdot \frac{1}{1600} \cdot \frac{1}{0.03 * 4690.98}$$

$$C = 568.2 \mu\text{F} = 2.14 \text{ p.u.}$$

5.4 AC side filter design

The AC side low pass filtering is accomplished by an LC filter with an RC damper to attenuate resonance oscillations. Since the first significant harmonic at the AC side, according to the Fourier analysis, is the 61st (3660 Hz) the input LC filter is made to resonate at 1800 Hz, the 30th harmonic. The RC damper parallel to the filter capacitor also resonates at 1800 Hz. The designed components are listed in the following page.

$$f_r = \frac{1}{2\pi\sqrt{L_f C_f}}$$

$$f_d = \frac{1}{2\pi R_d C_d}$$

$$L_f = 0.65 \text{ mH} = 0.112 \text{ p.u.}$$

$$C_f = 12.4 \text{ } \mu\text{F} = 98.13 \text{ p.u.}$$

$$C_d = 124 \text{ } \mu\text{F} = 9.813 \text{ p.u.}$$

$$R_d = 0.725 \text{ } \Omega = 0.333 \text{ p.u.}$$

5.5 Simulation tools and digital implementation

The design example would be simulated digitally on a PSIM 6.0 platform integrated with a C++ compiler. The designed components and other circuits would be constructed in PSIM and the controller would be digitally coded in the C++ compiler. The compiler generates a DLL file which handshakes with the PSIM to simulate the circuit at the specified time step size, as illustrated in Figure 36.

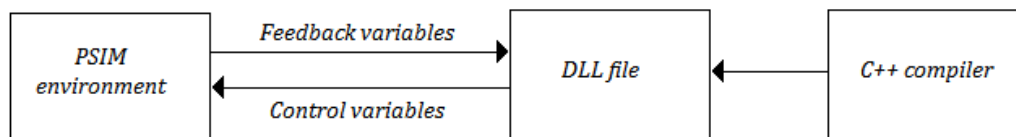


Figure 36: Simulation environment and elements

5.6 Simulation results for first quadrant operation

The converter is simulated in the first quadrant for different load conditions. In addition to testing the operation of the converter for various reference voltages and current, the profiles of various input current harmonics and input power factor are also studied. The time waveforms of currents and voltages at full load condition are produced here.

Figure 37 gives the DC link current at full load condition. This happens when the duty cycle of the full-bridge converter is set at the minimum value of 33%.

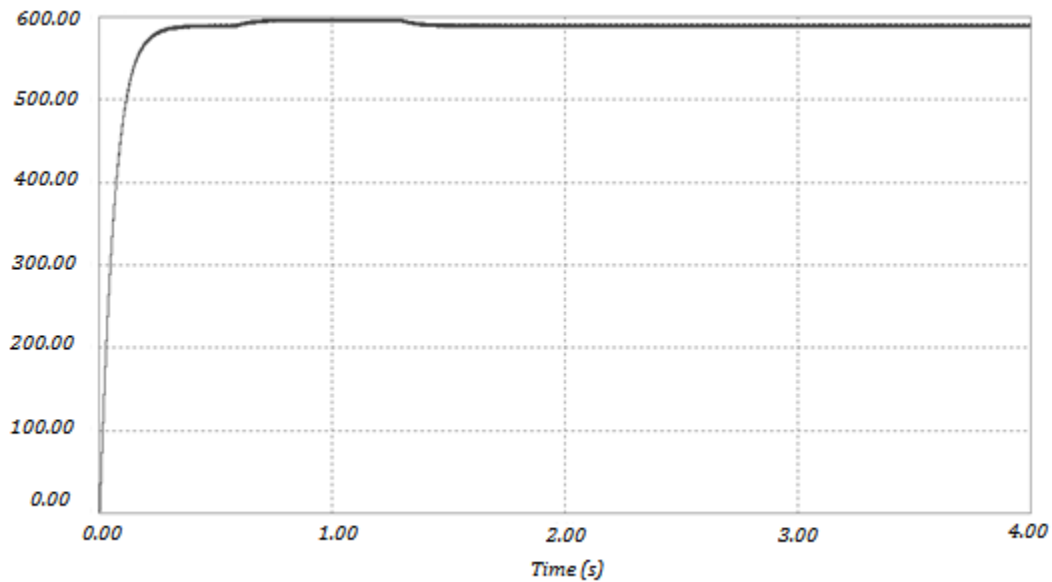


Figure 37: Full load DC link current when inverter duty cycle = 33%

Figure 38 shows the DC link current profile much closer; describing the DC current ripple performance which satisfies the design condition of 3 A. Figure 39 verifies the DC output voltage at the output capacitor to be having a voltage ripple of 3%.

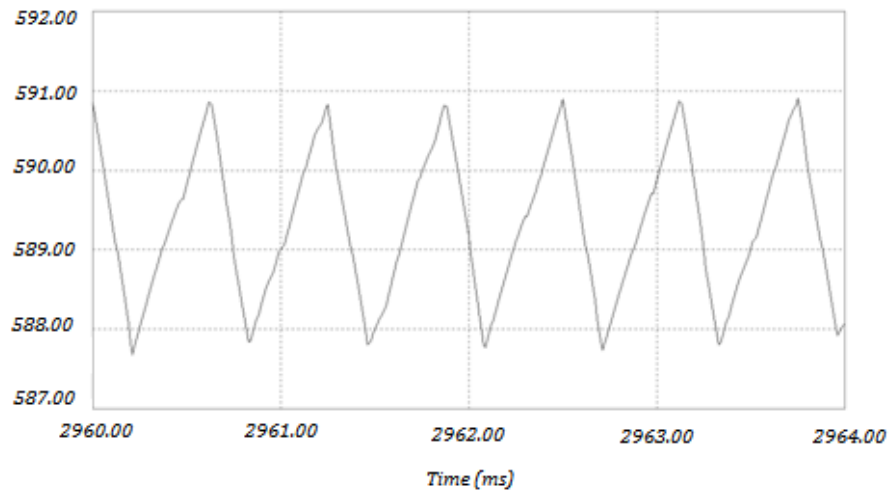


Figure 38: DC link inductor current ripple = 3 A at full load

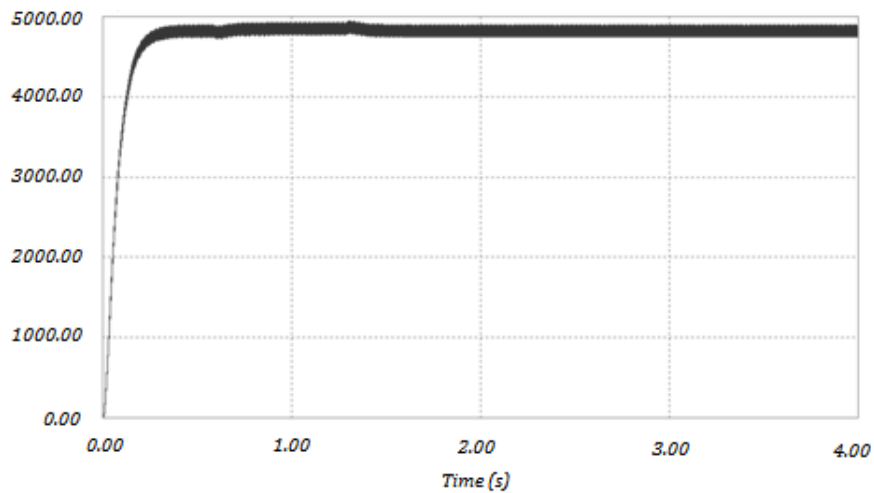


Figure 39: DC output voltage with voltage ripple = 3%

The variation of the DC link current is found to be linearly varying with respect to v for different duty cycles of the full-bridge converter and the different operating points of the converter lie within the two lines in Figure 40. The current ripple performances across the board for different v are also analyzed in Figure 41 below.

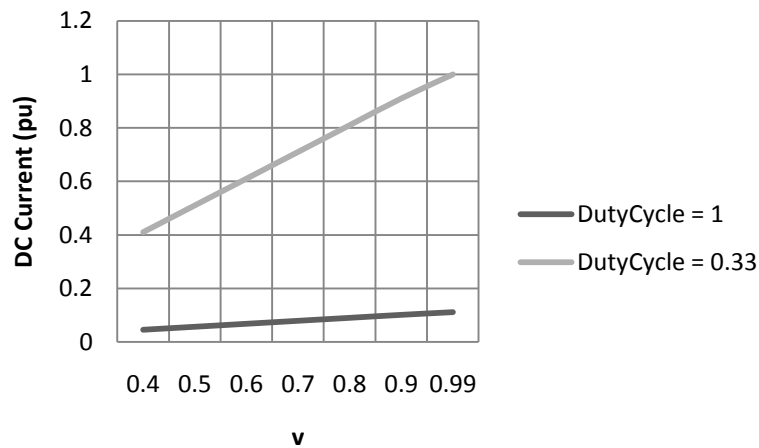


Figure 40: DC link current with respect to v

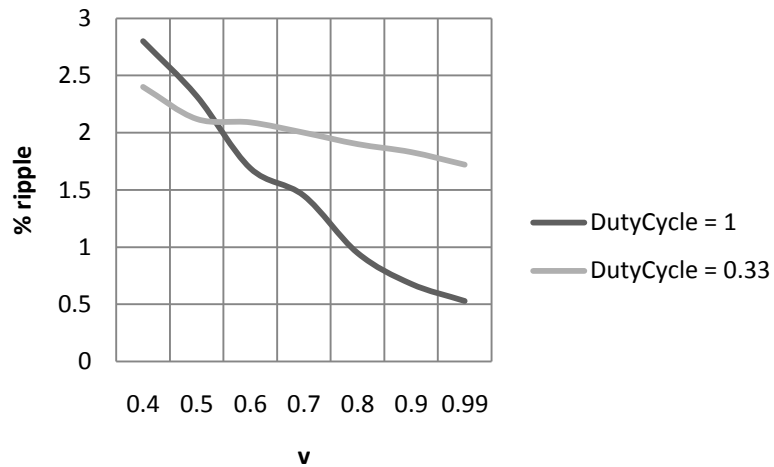


Figure 41: Current ripple with respect to v

The purpose of this converter is to deliver high power quality. The controller generates the switching functions as given in Figure 42 and the input phase current is illustrated. The AC side input current both unfiltered and filtered are given in Figure 43. The unfiltered programmed PWM current pulses have a THD of 60.7% and the filtered AC current has a THD of 2.0%.

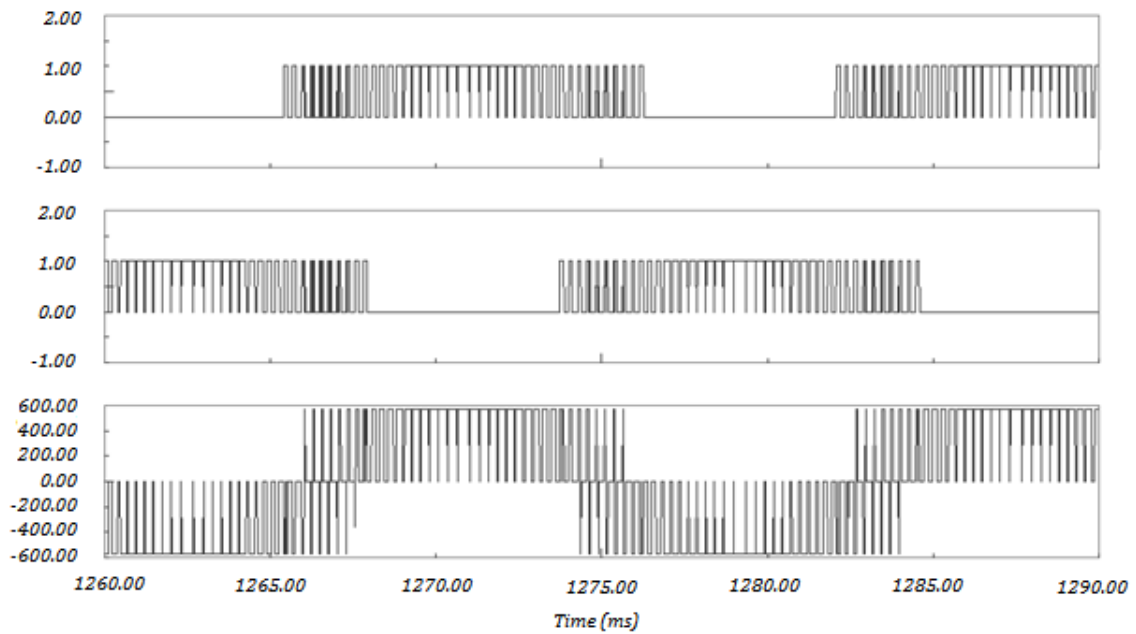


Figure 42: Switch S₁ gating function, switch S₄ gating function and input phase A current

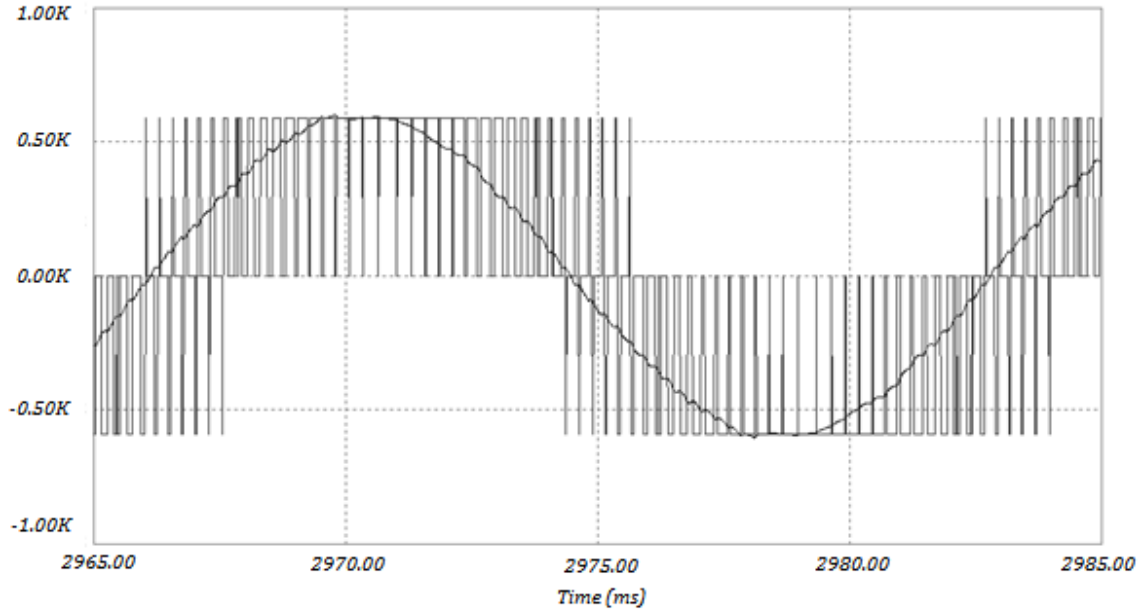
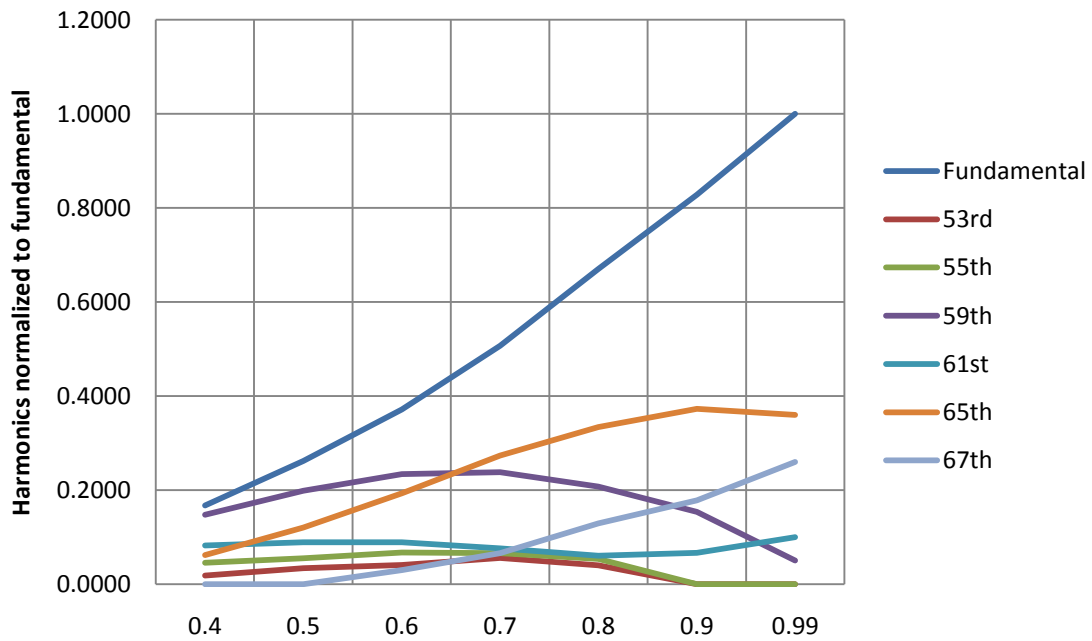


Figure 43: AC input current filtered (THD = 2.0%) imposed against programmed PWM current pulses (THD = 60.7%) at full load with $v = 1$

The values of the first few significant harmonics starting with the 53rd are given in Table 3. The 61st is the first significant harmonic at full load and lower orders get more prominent at lower loads. The profiles of the harmonics with respect to v are also given below in Figure 44. The harmonics are expressed as a percentage of the fundamental component.

Table 3: AC input current harmonics for different ν

ν	Fundamental	53 rd	55 th	59 th	61 st	65 th	67 th	%THD (unfiltered)	%THD (filtered)
0.99	1	0	0	0.05	0.1	0.36	0.26	60.7	2.0
0.9	0.83	0	0	0.15	0.07	0.37	0.18	73.7	4.0
0.8	0.67	0.04	0.05	0.21	0.06	0.33	0.13	85.8	5.8
0.7	0.51	0.06	0.07	0.24	0.08	0.27	0.07	99.5	7.9
0.6	0.37	0.04	0.07	0.23	0.09	0.19	0.03	114.4	8.4
0.5	0.26	0.03	0.05	0.20	0.09	0.12	0	134.0	11.4
0.4	0.17	0.02	0.05	0.15	0.08	0.06	0	156.1	11.0

Figure 44: Profile of significant harmonics against ν

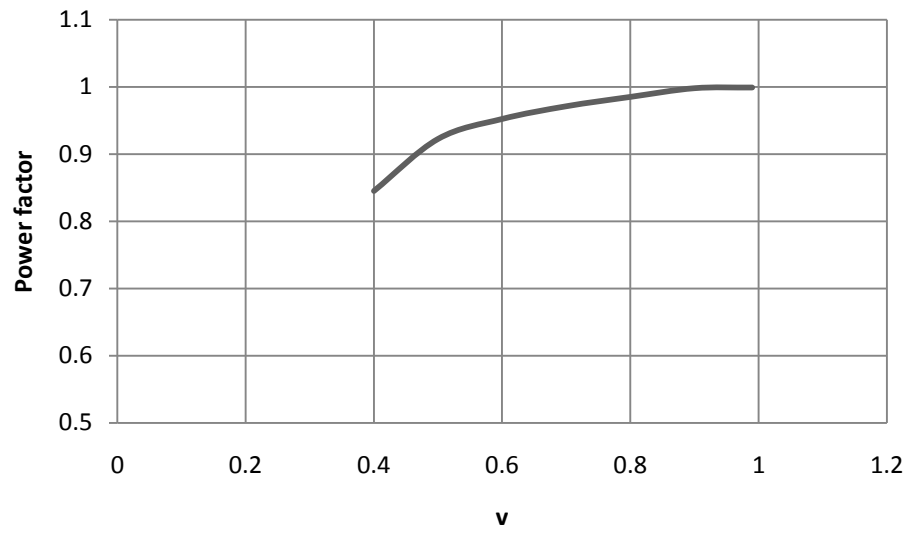


Figure 45: Input power factor of the converter for different v

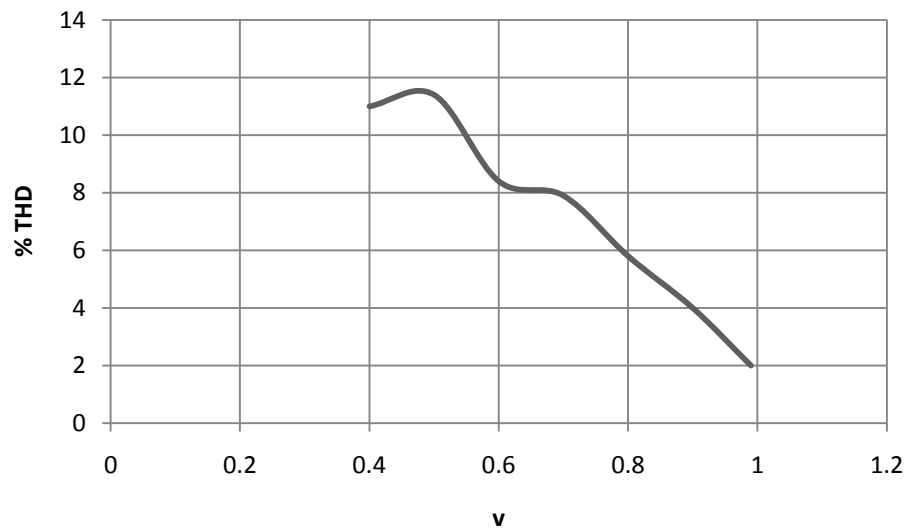


Figure 46: % THD of the input filtered current to the converter

As evident from Figure 45 giving the input power factor and Figure 46 giving the %THD of input current, the most favorable input power factor values occur above $v = 0.6$ and the most favorable %THD values occur at $v = 0.8$ and above.

5.7 Simulation results for fourth quadrant operation

The converter is operated in the fourth quadrant using the respective control algorithm. The converter feeds AC current into the utility grid by means of programmed PWM currents filtered by the AC side filter. The source impedance of the utility grid is included into the simulation. The load is replaced by a constant full load DC voltage.

The AC side phase current waveform at the converter end in the unfiltered form is produced in Figure 47. The unfiltered current has a THD of 136.4%. The fundamental component of the waveform is superimposed on the programmed PWM waveform.

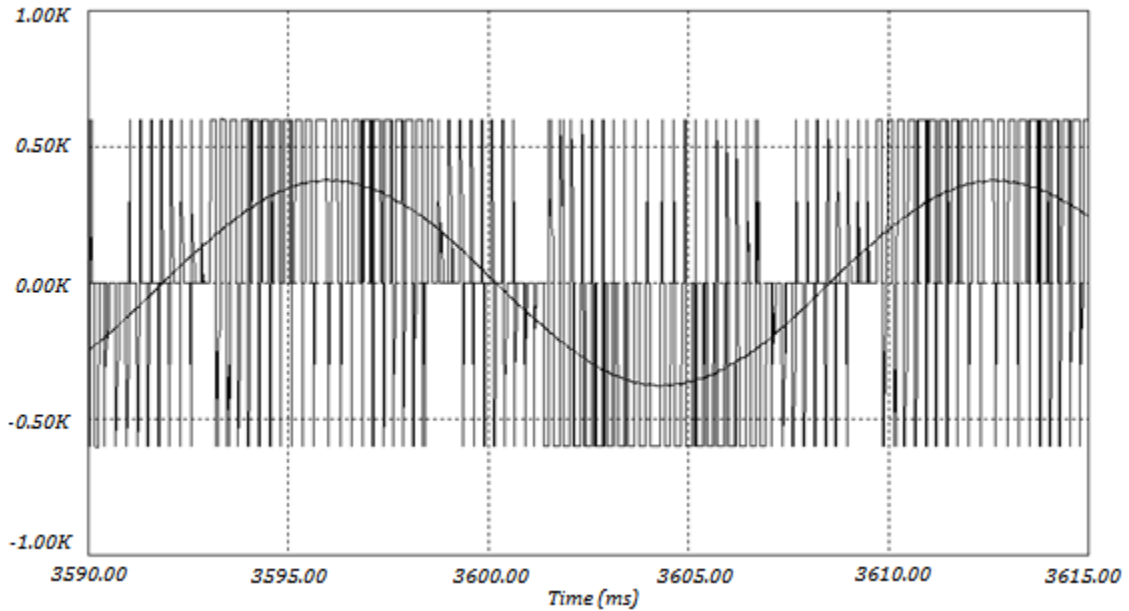


Figure 47: Unfiltered AC phase current in fourth quadrant operation, fundamental superimposed

The filtered phase current waveform is given in Figure 48. The current has a THD value of 11%. The frequency spectra of the unfiltered and filtered waveforms are given in Figure 49. While the programmed PWM controller selectively eliminates the lower order harmonics, the AC side input filter attenuates the higher order harmonics.

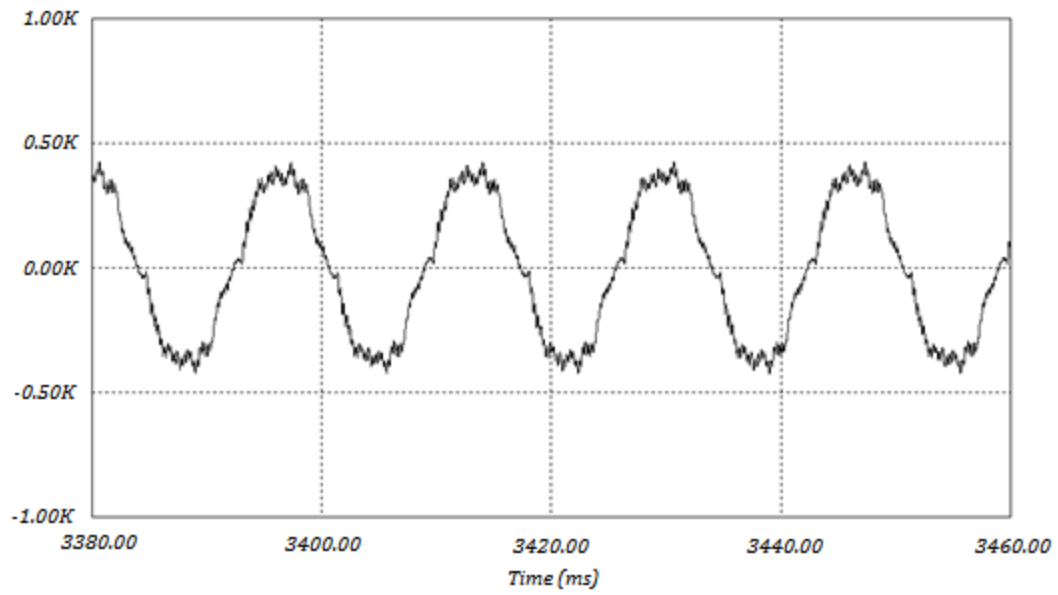


Figure 48: Filtered AC side phase current

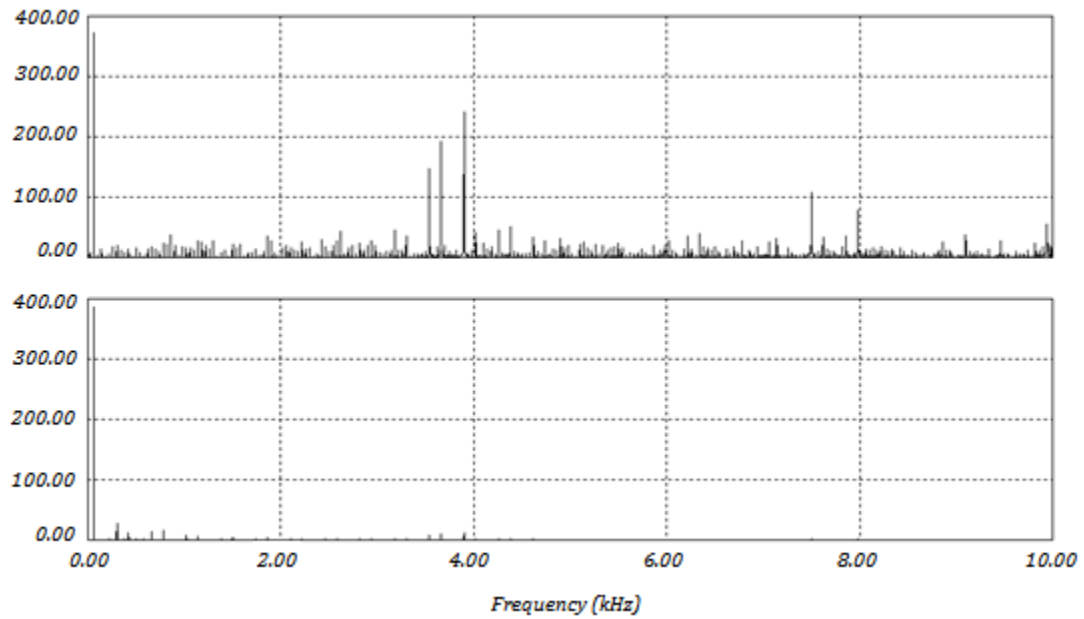


Figure 49: Frequency spectra of unfiltered and filtered AC side currents

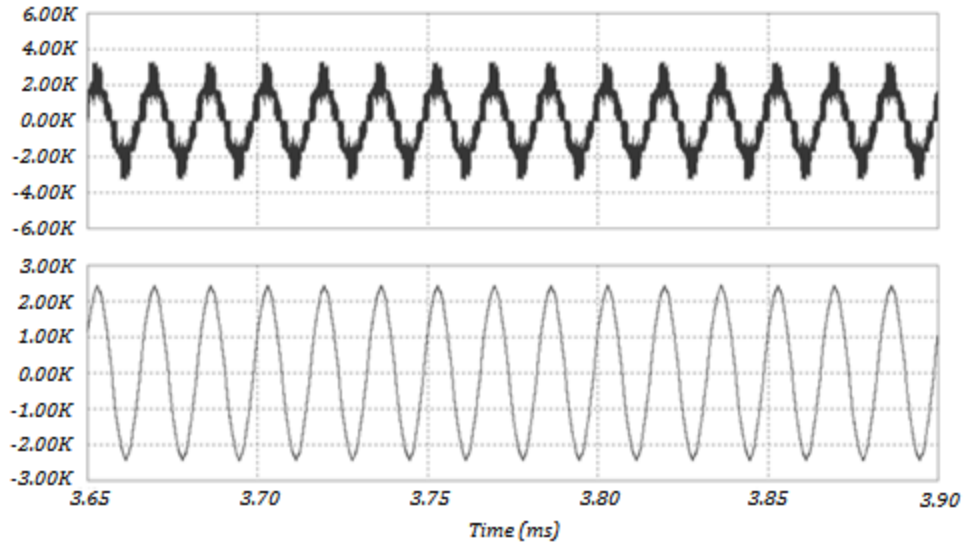


Figure 50: Line voltage at source end - unfiltered (THD = 28.9%) and filtered (THD = 1.9%)

Figure 50 gives the converter side line voltage and also the filtered line voltage. The input current THD values and input power factor for different values of DC link current are given in Table 4.

Table 4: % THD and power factor of the converter in fourth quadrant operation

DC link inductor current (p.u)	Filtered current %THD	Displacement factor	Distortion factor	Power factor
1	11.00	0.9762	0.994	0.9703
0.92	10.18	0.9754	0.9949	0.9704
0.83	9.35	0.9728	0.9957	0.9686
0.75	9.46	0.9701	0.9956	0.9658
0.67	9.89	0.9673	0.9951	0.9626
0.58	11.18	0.9603	0.9938	0.9543

5.8 Comparisons between existing and proposed topologies

After studying the design and performance of the existing topology and the proposed topology for high power AC-DC conversion, the proposed topology is determined to have better performance features than the existing one as described in Table 5:

Table 5: Comparisons between existing topology and proposed topology

Characteristic	Existing topology	Proposed topology
Number of power conversion stages	3	2
Number of active switches in front end	12	12
Multi-quadrant?	No	Yes
Converter input current THD at full load	73.5%	60.7%
First significant harmonic	5 th	61 st
Input filter size	Larger	Smaller than the existing topology by 10 times
Unity power factor	No	Yes

5.9 Chapter conclusion

The proposed topology was simulated using a design example and it was determined to have performance superior to that of the existing topology. The improvements were done without increasing the number of active switches thereby improving efficiency. The input current THD values are only around 15% better but since the lower order harmonics are selectively eliminated, low pass filter requirements are an order of magnitude lesser.

CHAPTER VI

CONCLUSION

The converter topology proposed has the capabilities to provide high power quality and to operate in all four quadrants. These properties make it suitable for a variety of applications.

6.1 Applications profile of the proposed converter

- The converter operating in the first quadrant is a suitable candidate DC power supplies with isolation requirements
- The converter may also be employed in high power DC motor drives, electrolysis applications, battery chargers, UPS and solar array simulators
- The ability of the converter to transient into a different quadrant in the V-I plane quickly could be applied to technologies such as regenerative braking
- The converter in fourth quadrant operates as an inverter with transformer isolation
- The converter operating in the fourth quadrant is a suitable candidate for solar power grid integration
- The front end fully controlled rectifier could be mirrored on the other side of the DC link inductor to form a matrix converter, making it suitable for AC motor drives and transformer emulation topologies. ^[15]

6.2 Summary of the thesis

The emphasis on high power quality has gone up, alongside the ever increasing demand for high power converters. The development of renewable energy sources and hybrid technologies meant that converters should be bi-directional. These requirements were outlined in this thesis in chapter I. Chapter II focused on the available topologies for high power AC-DC conversion. Operation and performance characteristics of uncontrolled rectifiers, line frequency controlled rectifiers and PWM rectifiers were discussed. In chapter III an existing topology for high power AC-DC conversion is examined. The converter is simulated in PSIM and the performance characteristics like input power factor and THD are studied. An improved topology with less number of power conversion stages is proposed in chapter IV. The operation of the controller in the first quadrant and the fourth quadrant is studied. In chapter V, a 900 kW rated system is designed and simulated using PSIM. The input power factor and THD performance of the proposed converter was found to match the regulatory requirements, with a full load THD of 2.0%.

Finally it was concluded that the proposed topology has better performance characteristics than the existing topology in all criteria studied.

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APPENDIX A

DIGITAL CONTROLLER PROGRAM FOR FIRST QUADRANT

OPERATION

```

#include <math.h>
#include <stdio.h>
#include <conio.h>

__declspec(dllexport) void one (t, delt, in, out)

double t, delt;
double *in, *out;

{
double vdc, idc, sp1, sp2, sp3, delv, vref;
static double vl1 = 0.5, vl2 = 0.5, vl3 = 0.5;
static double psp1 = -1, psp2 = 0, psp3 = 0;
static double sw1, sw2, sw3, sw4, sw5, sw6;
static double time1, time2, time3, time4, time5, time6;
double oal1, oal2, oal3, oal4, oal5, oal6, oal7, oal8, oal9, oal10, oal11,
oal12, oal13, oal14, oal15, oal16, oal17, oal18, oal19, oal20, oal21, oal22,
oal23, oal24, oal25, oal26, oal27, oal28, oal29, oal30, oal31, oal32, oal33,
oal34, oal35, oal36, oal37, oal38, oal39, oal40, twal1, twal2, twal3, twal4,
twal5, twal6, twal7, twal8, twal9, twal10, twal11, twal12, twal13, twal14,
twal15, twal16, twal17, twal18, twal19, twal20, twal21, twal22, twal23, twal24,
twal25, twal26, twal27, twal28, twal29, twal30, twal31, twal32, twal33, twal34,
twal35, twal36, twal37, twal38, twal39, twal40;
double thal1, thal2, thal3, thal4, thal5, thal6, thal7, thal8, thal9, thal10,
thal11, thal12, thal13, thal14, thal15, thal16, thal17, thal18, thal19, thal20,
thal21, thal22, thal23, thal24, thal25, thal26, thal27, thal28, thal29, thal30,
thal31, thal32, thal33, thal34, thal35, thal36, thal37, thal38, thal39, thal40;
static double o0 = 1, o1 = 1, o2 = 1, o3 = 1, o4 = 1, o5 = 1;
static double iref = 0, idcc1 = 0, idcc2 = 0, idcc3 = 0, idcav1 = 0, idcav2 =
0, idcav3 = 0, vdcc = 0, vdcav = 0, avetime = 0;
vref = in[0];
idc = in[1];
sp1 = in[2];
sp2 = in[3];
sp3 = in[4];
vdc = in[5];
avetime = avetime + 1;
vdcc = vdcc + vdc;

if (avetime == 100.0)
{
vdcav = vdcc/100.0;
vdcc = 0;
avetime = 0;
iref = iref + 0.005*iref*((vref-vdcav)/vref);
}

if (iref >= 600)

```



```

    {iref = 600;
    }

else if (iref <= 20)
    {iref = 20;
    }

idcc1 = idcc1 + idc;
idcc2 = idcc2 + idc;
idcc3 = idcc3 + idc;

if (psp1 == -1 && sp1 == 1)
    {
    idcav1 = idcc1*60.0*delt;
    idcc1 = 0;
    if(idcav1 > iref && idcav1-iref > 0.2*iref)
        {
        v11 = v11 - 0.01;
        }
    if(idcav1 > iref && idcav1-iref <= 0.2*iref)
        {
        v11 = v11 - 0.0001;
        }
    if(idcav1 < iref && iref-idcav1 > 0.2*iref)
        {
        v11 = v11 + 0.01;
        }
    if(idcav1 < iref && iref-idcav1 < 0.2*iref)
        {
        v11 = v11 + 0.0001;
        }
    }

if (v11 >= 0.99)
    {v11 = 0.99;
    }

else if (v11 <= 0.05)
    {v11 = 0.05;
    }

if (psp2 == -1 && sp2 == 1)
    {
    idcav2 = idcc2*60.0*delt;
    idcc2 = 0;
    if(idcav2 > iref && idcav2-iref > 0.2*iref)
        {
        v12 = v12 - 0.01;
        }
    if(idcav2 > iref && idcav2-iref <= 0.2*iref)
        {
        v12 = v12 - 0.0001;
        }
    if(idcav2 < iref && iref-idcav2 > 0.2*iref)
        {
        v12 = v12 + 0.01;
        }
    if(idcav2 < iref && iref-idcav2 < 0.2*iref)
        {

```

```

        v12 = v12 + 0.0001;
    }
}

if (v12 >= 0.99)
{v12 = 0.99;
}

else if (v12 <= 0.05)
{v12 = 0.05;
}

if (psp3 == -1 && sp3 == 1)
{
    idcav3 = idcc3*60.0*delt;
    idcc3 = 0;
    if(idcav3 > iref && idcav3-iref > 0.2*iref)
    {
        v13 = v13 - 0.01;
    }
    if(idcav3 > iref && idcav3-iref <= 0.2*iref)
    {
        v13 = v13 - 0.0001;
    }
    if(idcav3 < iref && iref-idcav3 > 0.2*iref)
    {
        v13 = v13 + 0.01;
    }
    if(idcav3 < iref && iref-idcav3 < 0.2*iref)
    {
        v13 = v13 + 0.0001;
    }
}

if (v13 >= 0.99)
{v13 = 0.99;
}

else if (v13 <= 0.05)
{v13 = 0.05;
}

oal1 = 2.859*v11;
oal2 = -0.699*v11+6;
oal3 = 2.618*v11+6;
oal4 = -1.355*v11+12;
oal5 = 2.393*v11+12;
oal6 = -1.969*v11+18;
oal7 = 2.179*v11+18;
oal8 = -2.541*v11+24;
oal9 = 1.974*v11+24;
oal10 = -3.067*v11+30;
oal11 = 1.779*v11+30;
oal12 = -3.541*v11+36;
oal13 = 1.603*v11+36;
oal14 = -3.951*v11+42;
oal15 = 1.469*v11+42;
oal16 = -4.272*v11+48;
oal17 = 1.455*v11+48;
oal18 = -4.42*v11+54;

```

```
oal19 = 1.956*v11+54;  
oal20 = -3.996*v11+60;  
oal21 = 120.0-oal20;  
oal22 = 120.0-oal19;  
oal23 = 120.0-oal18;  
oal24 = 120.0-oal17;  
oal25 = 120.0-oal16;  
oal26 = 120.0-oal15;  
oal27 = 120.0-oal14;  
oal28 = 120.0-oal13;  
oal29 = 120.0-oal12;  
oal30 = 120.0-oal11;  
oal31 = 120.0-oal10;  
oal32 = 120.0-oal9;  
oal33 = 120.0-oal8;  
oal34 = 120.0-oal7;  
oal35 = 120.0-oal6;  
oal36 = 120.0-oal5;  
oal37 = 120.0-oal4;  
oal38 = 120.0-oal3;  
oal39 = 120.0-oal2;  
oal40 = 120.0-oal1;
```

```
oal1 = oal1/21600.0;  
oal2 = oal2/21600.0;  
oal3 = oal3/21600.0;  
oal4 = oal4/21600.0;  
oal5 = oal5/21600.0;  
oal6 = oal6/21600.0;  
oal7 = oal7/21600.0;  
oal8 = oal8/21600.0;  
oal9 = oal9/21600.0;  
oal10 = oal10/21600.0;  
oal11 = oal11/21600.0;  
oal12 = oal12/21600.0;  
oal13 = oal13/21600.0;  
oal14 = oal14/21600.0;  
oal15 = oal15/21600.0;  
oal16 = oal16/21600.0;  
oal17 = oal17/21600.0;  
oal18 = oal18/21600.0;  
oal19 = oal19/21600.0;  
oal20 = oal20/21600.0;  
oal21 = oal21/21600.0;  
oal22 = oal22/21600.0;  
oal23 = oal23/21600.0;  
oal24 = oal24/21600.0;  
oal25 = oal25/21600.0;  
oal26 = oal26/21600.0;  
oal27 = oal27/21600.0;  
oal28 = oal28/21600.0;  
oal29 = oal29/21600.0;  
oal30 = oal30/21600.0;  
oal31 = oal31/21600.0;  
oal32 = oal32/21600.0;  
oal33 = oal33/21600.0;  
oal34 = oal34/21600.0;  
oal35 = oal35/21600.0;  
oal36 = oal36/21600.0;
```

```
oal37 = oal37/21600.0;
oal38 = oal38/21600.0;
oal39 = oal39/21600.0;
oal40 = oal40/21600.0;

twal1 = 2.859*v12;
twal2 = -0.699*v12+6;
twal3 = 2.618*v12+6;
twal4 = -1.355*v12+12;
twal5 = 2.393*v12+12;
twal6 = -1.969*v12+18;
twal7 = 2.179*v12+18;
twal8 = -2.541*v12+24;
twal9 = 1.974*v12+24;
twal10 = -3.067*v12+30;
twal11 = 1.779*v12+30;
twal12 = -3.541*v12+36;
twal13 = 1.603*v12+36;
twal14 = -3.951*v12+42;
twal15 = 1.469*v12+42;
twal16 = -4.272*v12+48;
twal17 = 1.455*v12+48;
twal18 = -4.42*v12+54;
twal19 = 1.956*v12+54;
twal20 = -3.996*v12+60;
twal21 = 120.0-tw120;
twal22 = 120.0-tw119;
twal23 = 120.0-tw118;
twal24 = 120.0-tw117;
twal25 = 120.0-tw116;
twal26 = 120.0-tw115;
twal27 = 120.0-tw114;
twal28 = 120.0-tw113;
twal29 = 120.0-tw112;
twal30 = 120.0-tw111;
twal31 = 120.0-tw110;
twal32 = 120.0-tw19;
twal33 = 120.0-tw18;
twal34 = 120.0-tw17;
twal35 = 120.0-tw16;
twal36 = 120.0-tw15;
twal37 = 120.0-tw14;
twal38 = 120.0-tw13;
twal39 = 120.0-tw12;
twal40 = 120.0-tw11;

twal1 = twal1/21600.0;
twal2 = twal2/21600.0;
twal3 = twal3/21600.0;
twal4 = twal4/21600.0;
twal5 = twal5/21600.0;
twal6 = twal6/21600.0;
twal7 = twal7/21600.0;
twal8 = twal8/21600.0;
twal9 = twal9/21600.0;
twal10 = twal10/21600.0;
twal11 = twal11/21600.0;
twal12 = twal12/21600.0;
twal13 = twal13/21600.0;
```

```
twal14 = twal14/21600.0;
twal15 = twal15/21600.0;
twal16 = twal16/21600.0;
twal17 = twal17/21600.0;
twal18 = twal18/21600.0;
twal19 = twal19/21600.0;
twal20 = twal20/21600.0;
twal21 = twal21/21600.0;
twal22 = twal22/21600.0;
twal23 = twal23/21600.0;
twal24 = twal24/21600.0;
twal25 = twal25/21600.0;
twal26 = twal26/21600.0;
twal27 = twal27/21600.0;
twal28 = twal28/21600.0;
twal29 = twal29/21600.0;
twal30 = twal30/21600.0;
twal31 = twal31/21600.0;
twal32 = twal32/21600.0;
twal33 = twal33/21600.0;
twal34 = twal34/21600.0;
twal35 = twal35/21600.0;
twal36 = twal36/21600.0;
twal37 = twal37/21600.0;
twal38 = twal38/21600.0;
twal39 = twal39/21600.0;
twal40 = twal40/21600.0;
```

```
thal1 = 2.859*v13;
thal2 = -0.699*v13+6;
thal3 = 2.618*v13+6;
thal4 = -1.355*v13+12;
thal5 = 2.393*v13+12;
thal6 = -1.969*v13+18;
thal7 = 2.179*v13+18;
thal8 = -2.541*v13+24;
thal9 = 1.974*v13+24;
thal10 = -3.067*v13+30;
thal11 = 1.779*v13+30;
thal12 = -3.541*v13+36;
thal13 = 1.603*v13+36;
thal14 = -3.951*v13+42;
thal15 = 1.469*v13+42;
thal16 = -4.272*v13+48;
thal17 = 1.455*v13+48;
thal18 = -4.42*v13+54;
thal19 = 1.956*v13+54;
thal20 = -3.996*v13+60;
thal21 = 120.0-thal20;
thal22 = 120.0-thal19;
thal23 = 120.0-thal18;
thal24 = 120.0-thal17;
thal25 = 120.0-thal16;
thal26 = 120.0-thal15;
thal27 = 120.0-thal14;
thal28 = 120.0-thal13;
thal29 = 120.0-thal12;
thal30 = 120.0-thal11;
thal31 = 120.0-thal10;
thal32 = 120.0-thal9;
```

```
thal33 = 120.0-thal8;  
thal34 = 120.0-thal7;  
thal35 = 120.0-thal6;  
thal36 = 120.0-thal5;  
thal37 = 120.0-thal4;  
thal38 = 120.0-thal3;  
thal39 = 120.0-thal2;  
thal40 = 120.0-thal1;
```

```
thal1 = thal1/21600.0;  
thal2 = thal2/21600.0;  
thal3 = thal3/21600.0;  
thal4 = thal4/21600.0;  
thal5 = thal5/21600.0;  
thal6 = thal6/21600.0;  
thal7 = thal7/21600.0;  
thal8 = thal8/21600.0;  
thal9 = thal9/21600.0;  
thal10 = thal10/21600.0;  
thal11 = thal11/21600.0;  
thal12 = thal12/21600.0;  
thal13 = thal13/21600.0;  
thal14 = thal14/21600.0;  
thal15 = thal15/21600.0;  
thal16 = thal16/21600.0;  
thal17 = thal17/21600.0;  
thal18 = thal18/21600.0;  
thal19 = thal19/21600.0;  
thal20 = thal20/21600.0;  
thal21 = thal21/21600.0;  
thal22 = thal22/21600.0;  
thal23 = thal23/21600.0;  
thal24 = thal24/21600.0;  
thal25 = thal25/21600.0;  
thal26 = thal26/21600.0;  
thal27 = thal27/21600.0;  
thal28 = thal28/21600.0;  
thal29 = thal29/21600.0;  
thal30 = thal30/21600.0;  
thal31 = thal31/21600.0;  
thal32 = thal32/21600.0;  
thal33 = thal33/21600.0;  
thal34 = thal34/21600.0;  
thal35 = thal35/21600.0;  
thal36 = thal36/21600.0;  
thal37 = thal37/21600.0;  
thal38 = thal38/21600.0;  
thal39 = thal39/21600.0;  
thal40 = thal40/21600.0;
```

```
if (psp1 == -1 && sp1 == 1)  
{  
    sw1 = 1;  
    sw4 = 0;  
    time1 = t;  
}
```

```
if (psp2 == -1 && sp2 == 1)  
{
```

```

    sw3 = 1;
    sw6 = 0;
    time3 = t;
}

if (psp3 == -1 && sp3 == 1)
{
    sw5 = 1;
    sw2 = 0;
    time5 = t;
}

if (psp1 == 1 && sp1 == -1)
{
    sw4 = 1;
    sw1 = 0;
    time4 = t;
}

if (psp2 == 1 && sp2 == -1)
{
    sw6 = 1;
    sw3 = 0;
    time6 = t;
}

if (psp3 == 1 && sp3 == -1)
{
    sw2 = 1;
    sw5 = 0;
    time2 = t;
}

if (sw1 == 1)
{
    if ((t >= time1+30.0/21600.0-delt && t <= time1+30.0/21600.0) || (t >=
time1+oal1+30.0/21600.0-delt && t <= time1+oal1+30.0/21600.0) || (t >=
time1+oal2+30.0/21600.0-delt && t <= time1+oal2+30.0/21600.0) || (t >=
time1+oal3+30.0/21600.0-delt && t <= time1+oal3+30.0/21600.0) || (t >=
time1+oal4+30.0/21600.0-delt && t <= time1+oal4+30.0/21600.0) || (t >=
time1+oal5+30.0/21600.0-delt && t <= time1+oal5+30.0/21600.0) || (t >=
time1+oal6+30.0/21600.0-delt && t <= time1+oal6+30.0/21600.0) || (t >=
time1+oal7+30.0/21600.0-delt && t <= time1+oal7+30.0/21600.0) || (t >=
time1+oal8+30.0/21600.0-delt && t <= time1+oal8+30.0/21600.0) || (t >=
time1+oal9+30.0/21600.0-delt && t <= time1+oal9+30.0/21600.0) || (t >=
time1+oal10+30.0/21600.0-delt && t <= time1+oal10+30.0/21600.0) || (t >=
time1+oal11+30.0/21600.0-delt && t <= time1+oal11+30.0/21600.0) || (t >=
time1+oal12+30.0/21600.0-delt && t <= time1+oal12+30.0/21600.0) || (t >=
time1+oal13+30.0/21600.0-delt && t <= time1+oal13+30.0/21600.0) || (t >=
time1+oal14+30.0/21600.0-delt && t <= time1+oal14+30.0/21600.0) || (t >=
time1+oal15+30.0/21600.0-delt && t <= time1+oal15+30.0/21600.0) || (t >=
time1+oal16+30.0/21600.0-delt && t <= time1+oal16+30.0/21600.0) || (t >=
time1+oal17+30.0/21600.0-delt && t <= time1+oal17+30.0/21600.0) || (t >=
time1+oal18+30.0/21600.0-delt && t <= time1+oal18+30.0/21600.0) || (t >=
time1+oal19+30.0/21600.0-delt && t <= time1+oal19+30.0/21600.0) || (t >=
time1+oal20+30.0/21600.0-delt && t <= time1+oal20+30.0/21600.0) || (t >=
time1+oal21+30.0/21600.0-delt && t <= time1+oal21+30.0/21600.0) || (t >=
time1+oal22+30.0/21600.0-delt && t <= time1+oal22+30.0/21600.0) || (t >=
time1+oal23+30.0/21600.0-delt && t <= time1+oal23+30.0/21600.0) || (t >=

```



```
time6+twal39+30.0/21600.0-delt && t <= time6+twal39+30.0/21600.0) || (t >=
time6+twal40+30.0/21600.0-delt && t <= time6+twal40+30.0/21600.0))
    {
        if (o5 == 0)
            { out[5] = 1;
              }
        else if (o5 == 1)
            { out[5] = 0;
              }
    }
else if (t >= time6+150.0/21600.0-delt && t <= time6+150.0/21600.0)
    {
        out[5] = 0;
    }
}

psp1 = sp1;
psp2 = sp2;
psp3 = sp3;
o0 = out[0];
o1 = out[1];
o2 = out[2];
o3 = out[3];
o4 = out[4];
o5 = out[5];

}
```

APPENDIX B

DIGITAL CONTROLLER PROGRAM FOR FOURTH QUADRANT

OPERATION

```

#include <math.h>
#include <stdio.h>
#include <conio.h>

__declspec(dllexport) void one (t, delt, in, out)

double t, delt;
double *in, *out;

{
double iref, idc, sp1, sp2, sp3, vl1, vl2, vl3;
static double psp1 = -1, psp2 = 0, psp3 = 0;
static double sw1, sw2, sw3, sw4, sw5, sw6;
static double time1, time2, time3, time4, time5, time6;
double oal1, oal2, oal3, oal4, oal5, oal6, oal7, oal8, oal9, oal10, oal11,
oal12, oal13, oal14, oal15, oal16, oal17, oal18, oal19, oal20, oal21, oal22,
oal23, oal24, oal25, oal26, oal27, oal28, oal29, oal30, oal31, oal32, oal33,
oal34, oal35, oal36, oal37, oal38, oal39, oal40, twal1, twal2, twal3, twal4,
twal5, twal6, twal7, twal8, twal9, twal10, twal11, twal12, twal13, twal14,
twal15, twal16, twal17, twal18, twal19, twal20, twal21, twal22, twal23, twal24,
twal25, twal26, twal27, twal28, twal29, twal30, twal31, twal32, twal33, twal34,
twal35, twal36, twal37, twal38, twal39, twal40;
double thal1, thal2, thal3, thal4, thal5, thal6, thal7, thal8, thal9, thal10,
thal11, thal12, thal13, thal14, thal15, thal16, thal17, thal18, thal19, thal20,
thal21, thal22, thal23, thal24, thal25, thal26, thal27, thal28, thal29, thal30,
thal31, thal32, thal33, thal34, thal35, thal36, thal37, thal38, thal39, thal40;
static double o0 = 1, o1 = 1, o2 = 1, o3 = 1, o4 = 1, o5 = 1, o6 = 1, o7 = 0;
static double idcc = 0, idcav = 0, tstart = 0, duty = 0;
iref = in[0];
idc = in[1];
sp1 = in[2];
sp2 = in[3];
sp3 = in[4];

idcc = idcc + idc;
if (tstart > 1/800.0 && tstart <= (1/800.0)+delt)
{
tstart = 0;
}
if (tstart == 0)
{
o6 = 1;
o7 = 0;
idcav = idcc * 800.0 * delt;
idcc = 0;
if(idcav > iref && idcav-iref > 0.2*iref)
{
duty = duty - 0.005;
}
}
}

```

```

    }
    else if(idcav > iref && idcav-iref <= 0.2*iref)
    {
        duty = duty - 0.0001;
    }
    else if(idcav < iref && iref-idcav > 0.2*iref)
    {
        duty = duty + 0.005;
    }
    else if(idcav < iref && iref-idcav <= 0.2*iref)
    {
        duty = duty + 0.0001;
    }
}

if (duty > 0.99)
{
    duty = 0.99;
}
else if (duty < 0.01)
{
    duty = 0.01;
}

if (tstart > duty/1600.0 && tstart <= (duty/1600.0)+delt)
{
    o6 = 0;
}
if (tstart >= 1/1600.0 && tstart < (1/1600.0)+delt)
{
    o7 = 1;
}
if (tstart > (1+duty)/1600.0 && tstart <= ((1+duty)/1600.0)+delt)
{
    o7 = 0;
}
tstart = tstart + delt;

v11 = 0.99;
v12 = v11;
v13 = v11;

oal1 = 2.859*v11;
oal2 = -0.699*v11+6;
oal3 = 2.618*v11+6;
oal4 = -1.355*v11+12;
oal5 = 2.393*v11+12;
oal6 = -1.969*v11+18;
oal7 = 2.179*v11+18;
oal8 = -2.541*v11+24;
oal9 = 1.974*v11+24;
oal10 = -3.067*v11+30;
oal11 = 1.779*v11+30;
oal12 = -3.541*v11+36;
oal13 = 1.603*v11+36;
oal14 = -3.951*v11+42;
oal15 = 1.469*v11+42;
oal16 = -4.272*v11+48;
oal17 = 1.455*v11+48;
oal18 = -4.42*v11+54;

```

```
oal19 = 1.956*v11+54;  
oal20 = -3.996*v11+60;  
oal21 = 120.0-oal20;  
oal22 = 120.0-oal19;  
oal23 = 120.0-oal18;  
oal24 = 120.0-oal17;  
oal25 = 120.0-oal16;  
oal26 = 120.0-oal15;  
oal27 = 120.0-oal14;  
oal28 = 120.0-oal13;  
oal29 = 120.0-oal12;  
oal30 = 120.0-oal11;  
oal31 = 120.0-oal10;  
oal32 = 120.0-oal9;  
oal33 = 120.0-oal8;  
oal34 = 120.0-oal7;  
oal35 = 120.0-oal6;  
oal36 = 120.0-oal5;  
oal37 = 120.0-oal4;  
oal38 = 120.0-oal3;  
oal39 = 120.0-oal2;  
oal40 = 120.0-oal1;
```

```
oal1 = oal1/21600.0;  
oal2 = oal2/21600.0;  
oal3 = oal3/21600.0;  
oal4 = oal4/21600.0;  
oal5 = oal5/21600.0;  
oal6 = oal6/21600.0;  
oal7 = oal7/21600.0;  
oal8 = oal8/21600.0;  
oal9 = oal9/21600.0;  
oal10 = oal10/21600.0;  
oal11 = oal11/21600.0;  
oal12 = oal12/21600.0;  
oal13 = oal13/21600.0;  
oal14 = oal14/21600.0;  
oal15 = oal15/21600.0;  
oal16 = oal16/21600.0;  
oal17 = oal17/21600.0;  
oal18 = oal18/21600.0;  
oal19 = oal19/21600.0;  
oal20 = oal20/21600.0;  
oal21 = oal21/21600.0;  
oal22 = oal22/21600.0;  
oal23 = oal23/21600.0;  
oal24 = oal24/21600.0;  
oal25 = oal25/21600.0;  
oal26 = oal26/21600.0;  
oal27 = oal27/21600.0;  
oal28 = oal28/21600.0;  
oal29 = oal29/21600.0;  
oal30 = oal30/21600.0;  
oal31 = oal31/21600.0;  
oal32 = oal32/21600.0;  
oal33 = oal33/21600.0;  
oal34 = oal34/21600.0;  
oal35 = oal35/21600.0;  
oal36 = oal36/21600.0;
```



```
oal37 = oal37/21600.0;
oal38 = oal38/21600.0;
oal39 = oal39/21600.0;
oal40 = oal40/21600.0;

twal1 = 2.859*v12;
twal2 = -0.699*v12+6;
twal3 = 2.618*v12+6;
twal4 = -1.355*v12+12;
twal5 = 2.393*v12+12;
twal6 = -1.969*v12+18;
twal7 = 2.179*v12+18;
twal8 = -2.541*v12+24;
twal9 = 1.974*v12+24;
twal10 = -3.067*v12+30;
twal11 = 1.779*v12+30;
twal12 = -3.541*v12+36;
twal13 = 1.603*v12+36;
twal14 = -3.951*v12+42;
twal15 = 1.469*v12+42;
twal16 = -4.272*v12+48;
twal17 = 1.455*v12+48;
twal18 = -4.42*v12+54;
twal19 = 1.956*v12+54;
twal20 = -3.996*v12+60;
twal21 = 120.0-tw120;
twal22 = 120.0-tw119;
twal23 = 120.0-tw118;
twal24 = 120.0-tw117;
twal25 = 120.0-tw116;
twal26 = 120.0-tw115;
twal27 = 120.0-tw114;
twal28 = 120.0-tw113;
twal29 = 120.0-tw112;
twal30 = 120.0-tw111;
twal31 = 120.0-tw110;
twal32 = 120.0-tw19;
twal33 = 120.0-tw18;
twal34 = 120.0-tw17;
twal35 = 120.0-tw16;
twal36 = 120.0-tw15;
twal37 = 120.0-tw14;
twal38 = 120.0-tw13;
twal39 = 120.0-tw12;
twal40 = 120.0-tw11;

twal1 = twal1/21600.0;
twal2 = twal2/21600.0;
twal3 = twal3/21600.0;
twal4 = twal4/21600.0;
twal5 = twal5/21600.0;
twal6 = twal6/21600.0;
twal7 = twal7/21600.0;
twal8 = twal8/21600.0;
twal9 = twal9/21600.0;
twal10 = twal10/21600.0;
twal11 = twal11/21600.0;
twal12 = twal12/21600.0;
twal13 = twal13/21600.0;
```

```
twal14 = twal14/21600.0;
twal15 = twal15/21600.0;
twal16 = twal16/21600.0;
twal17 = twal17/21600.0;
twal18 = twal18/21600.0;
twal19 = twal19/21600.0;
twal20 = twal20/21600.0;
twal21 = twal21/21600.0;
twal22 = twal22/21600.0;
twal23 = twal23/21600.0;
twal24 = twal24/21600.0;
twal25 = twal25/21600.0;
twal26 = twal26/21600.0;
twal27 = twal27/21600.0;
twal28 = twal28/21600.0;
twal29 = twal29/21600.0;
twal30 = twal30/21600.0;
twal31 = twal31/21600.0;
twal32 = twal32/21600.0;
twal33 = twal33/21600.0;
twal34 = twal34/21600.0;
twal35 = twal35/21600.0;
twal36 = twal36/21600.0;
twal37 = twal37/21600.0;
twal38 = twal38/21600.0;
twal39 = twal39/21600.0;
twal40 = twal40/21600.0;
```

```
thal1 = 2.859*v13;
thal2 = -0.699*v13+6;
thal3 = 2.618*v13+6;
thal4 = -1.355*v13+12;
thal5 = 2.393*v13+12;
thal6 = -1.969*v13+18;
thal7 = 2.179*v13+18;
thal8 = -2.541*v13+24;
thal9 = 1.974*v13+24;
thal10 = -3.067*v13+30;
thal11 = 1.779*v13+30;
thal12 = -3.541*v13+36;
thal13 = 1.603*v13+36;
thal14 = -3.951*v13+42;
thal15 = 1.469*v13+42;
thal16 = -4.272*v13+48;
thal17 = 1.455*v13+48;
thal18 = -4.42*v13+54;
thal19 = 1.956*v13+54;
thal20 = -3.996*v13+60;
thal21 = 120.0-thal20;
thal22 = 120.0-thal19;
thal23 = 120.0-thal18;
thal24 = 120.0-thal17;
thal25 = 120.0-thal16;
thal26 = 120.0-thal15;
thal27 = 120.0-thal14;
thal28 = 120.0-thal13;
thal29 = 120.0-thal12;
thal30 = 120.0-thal11;
thal31 = 120.0-thal10;
thal32 = 120.0-thal9;
```

```
thal33 = 120.0-thal8;  
thal34 = 120.0-thal7;  
thal35 = 120.0-thal6;  
thal36 = 120.0-thal5;  
thal37 = 120.0-thal4;  
thal38 = 120.0-thal3;  
thal39 = 120.0-thal2;  
thal40 = 120.0-thal1;
```

```
thal1 = thal1/21600.0;  
thal2 = thal2/21600.0;  
thal3 = thal3/21600.0;  
thal4 = thal4/21600.0;  
thal5 = thal5/21600.0;  
thal6 = thal6/21600.0;  
thal7 = thal7/21600.0;  
thal8 = thal8/21600.0;  
thal9 = thal9/21600.0;  
thal10 = thal10/21600.0;  
thal11 = thal11/21600.0;  
thal12 = thal12/21600.0;  
thal13 = thal13/21600.0;  
thal14 = thal14/21600.0;  
thal15 = thal15/21600.0;  
thal16 = thal16/21600.0;  
thal17 = thal17/21600.0;  
thal18 = thal18/21600.0;  
thal19 = thal19/21600.0;  
thal20 = thal20/21600.0;  
thal21 = thal21/21600.0;  
thal22 = thal22/21600.0;  
thal23 = thal23/21600.0;  
thal24 = thal24/21600.0;  
thal25 = thal25/21600.0;  
thal26 = thal26/21600.0;  
thal27 = thal27/21600.0;  
thal28 = thal28/21600.0;  
thal29 = thal29/21600.0;  
thal30 = thal30/21600.0;  
thal31 = thal31/21600.0;  
thal32 = thal32/21600.0;  
thal33 = thal33/21600.0;  
thal34 = thal34/21600.0;  
thal35 = thal35/21600.0;  
thal36 = thal36/21600.0;  
thal37 = thal37/21600.0;  
thal38 = thal38/21600.0;  
thal39 = thal39/21600.0;  
thal40 = thal40/21600.0;
```

```
if (psp1 == -1 && sp1 == 1)  
{  
    sw1 = 1;  
    sw4 = 0;  
    time1 = t;  
}
```

```
if (psp2 == -1 && sp2 == 1)  
{
```

```

    sw3 = 1;
    sw6 = 0;
    time3 = t;
}

if (psp3 == -1 && sp3 == 1)
{
    sw5 = 1;
    sw2 = 0;
    time5 = t;
}

if (psp1 == 1 && sp1 == -1)
{
    sw4 = 1;
    sw1 = 0;
    time4 = t;
}

if (psp2 == 1 && sp2 == -1)
{
    sw6 = 1;
    sw3 = 0;
    time6 = t;
}

if (psp3 == 1 && sp3 == -1)
{
    sw2 = 1;
    sw5 = 0;
    time2 = t;
}

if (sw1 == 1)
{
    if (t >= time1+30.0/21600.0-delt && t < time1+30.0/21600.0)
    {
        out[0] = 1;
        out[3] = 0;
    }
    else if ((t >= time1+oal1+30.0/21600.0-delt && t <
time1+oal1+30.0/21600.0) || (t >= time1+oal2+30.0/21600.0-delt && t <
time1+oal2+30.0/21600.0) || (t >= time1+oal3+30.0/21600.0-delt && t <
time1+oal3+30.0/21600.0) || (t >= time1+oal4+30.0/21600.0-delt && t <
time1+oal4+30.0/21600.0) || (t >= time1+oal5+30.0/21600.0-delt && t <
time1+oal5+30.0/21600.0) || (t >= time1+oal6+30.0/21600.0-delt && t <
time1+oal6+30.0/21600.0) || (t >= time1+oal7+30.0/21600.0-delt && t <
time1+oal7+30.0/21600.0) || (t >= time1+oal8+30.0/21600.0-delt && t <
time1+oal8+30.0/21600.0) || (t >= time1+oal9+30.0/21600.0-delt && t <
time1+oal9+30.0/21600.0) || (t >= time1+oal10+30.0/21600.0-delt && t <
time1+oal10+30.0/21600.0) || (t >= time1+oal11+30.0/21600.0-delt && t <
time1+oal11+30.0/21600.0) || (t >= time1+oal12+30.0/21600.0-delt && t <
time1+oal12+30.0/21600.0) || (t >= time1+oal13+30.0/21600.0-delt && t <
time1+oal13+30.0/21600.0) || (t >= time1+oal14+30.0/21600.0-delt && t <
time1+oal14+30.0/21600.0) || (t >= time1+oal15+30.0/21600.0-delt && t <
time1+oal15+30.0/21600.0) || (t >= time1+oal16+30.0/21600.0-delt && t <
time1+oal16+30.0/21600.0) || (t >= time1+oal17+30.0/21600.0-delt && t <
time1+oal17+30.0/21600.0) || (t >= time1+oal18+30.0/21600.0-delt && t <
time1+oal18+30.0/21600.0) || (t >= time1+oal19+30.0/21600.0-delt && t <
time1+oal19+30.0/21600.0) || (t >= time1+oal20+30.0/21600.0-delt && t <

```

```

time1+oal20+30.0/21600.0) || (t >= time1+oal21+30.0/21600.0-delt && t <
time1+oal21+30.0/21600.0) || (t >= time1+oal22+30.0/21600.0-delt && t <
time1+oal22+30.0/21600.0) || (t >= time1+oal23+30.0/21600.0-delt && t <
time1+oal23+30.0/21600.0) || (t >= time1+oal24+30.0/21600.0-delt && t <
time1+oal24+30.0/21600.0) || (t >= time1+oal25+30.0/21600.0-delt && t <
time1+oal25+30.0/21600.0) || (t >= time1+oal26+30.0/21600.0-delt && t <
time1+oal26+30.0/21600.0) || (t >= time1+oal27+30.0/21600.0-delt && t <
time1+oal27+30.0/21600.0) || (t >= time1+oal28+30.0/21600.0-delt && t <
time1+oal28+30.0/21600.0) || (t >= time1+oal29+30.0/21600.0-delt && t <
time1+oal29+30.0/21600.0) || (t >= time1+oal30+30.0/21600.0-delt && t <
time1+oal30+30.0/21600.0) || (t >= time1+oal31+30.0/21600.0-delt && t <
time1+oal31+30.0/21600.0) || (t >= time1+oal32+30.0/21600.0-delt && t <
time1+oal32+30.0/21600.0) || (t >= time1+oal33+30.0/21600.0-delt && t <
time1+oal33+30.0/21600.0) || (t >= time1+oal34+30.0/21600.0-delt && t <
time1+oal34+30.0/21600.0) || (t >= time1+oal35+30.0/21600.0-delt && t <
time1+oal35+30.0/21600.0) || (t >= time1+oal36+30.0/21600.0-delt && t <
time1+oal36+30.0/21600.0) || (t >= time1+oal37+30.0/21600.0-delt && t <
time1+oal37+30.0/21600.0) || (t >= time1+oal38+30.0/21600.0-delt && t <
time1+oal38+30.0/21600.0) || (t >= time1+oal39+30.0/21600.0-delt && t <
time1+oal39+30.0/21600.0) || (t >= time1+oal40+30.0/21600.0-delt && t <
time1+oal40+30.0/21600.0))
    {
        if (o0 == 0)
            { out[0] = 1;
            }
        else if (o0 == 1)
            { out[0] = 0;
            }
        if (o3 == 0)
            { out[3] = 1;
            }
        else if (o3 == 1)
            { out[3] = 0;
            }
    }
else if (t >= time1+150.0/21600.0-delt && t < time1+150.0/21600.0)
    {
        out[0] = 0;
        out[3] = 0;
    }
}

if (sw2 == 1)
    {
        if (t >= time2+30.0/21600.0-delt && t < time2+30.0/21600.0)
            {
                out[1] = 1;
                out[4] = 0;
            }
        else if ((t >= time2+thal1+30.0/21600.0-delt && t <
time2+thal1+30.0/21600.0) || (t >= time2+thal2+30.0/21600.0-delt && t <
time2+thal2+30.0/21600.0) || (t >= time2+thal3+30.0/21600.0-delt && t <
time2+thal3+30.0/21600.0) || (t >= time2+thal4+30.0/21600.0-delt && t <
time2+thal4+30.0/21600.0) || (t >= time2+thal5+30.0/21600.0-delt && t <
time2+thal5+30.0/21600.0) || (t >= time2+thal6+30.0/21600.0-delt && t <
time2+thal6+30.0/21600.0) || (t >= time2+thal7+30.0/21600.0-delt && t <
time2+thal7+30.0/21600.0) || (t >= time2+thal8+30.0/21600.0-delt && t <
time2+thal8+30.0/21600.0) || (t >= time2+thal9+30.0/21600.0-delt && t <
time2+thal9+30.0/21600.0) || (t >= time2+thal10+30.0/21600.0-delt && t <
time2+thal10+30.0/21600.0) || (t >= time2+thal11+30.0/21600.0-delt && t <
time2+thal11+30.0/21600.0) || (t >= time2+thal12+30.0/21600.0-delt && t <

```

```

time2+thal12+30.0/21600.0) || (t >= time2+thal13+30.0/21600.0-delt && t <
time2+thal13+30.0/21600.0) || (t >= time2+thal14+30.0/21600.0-delt && t <
time2+thal14+30.0/21600.0) || (t >= time2+thal15+30.0/21600.0-delt && t <
time2+thal15+30.0/21600.0) || (t >= time2+thal16+30.0/21600.0-delt && t <
time2+thal16+30.0/21600.0) || (t >= time2+thal17+30.0/21600.0-delt && t <
time2+thal17+30.0/21600.0) || (t >= time2+thal18+30.0/21600.0-delt && t <
time2+thal18+30.0/21600.0) || (t >= time2+thal19+30.0/21600.0-delt && t <
time2+thal19+30.0/21600.0) || (t >= time2+thal20+30.0/21600.0-delt && t <
time2+thal20+30.0/21600.0) || (t >= time2+thal21+30.0/21600.0-delt && t <
time2+thal21+30.0/21600.0) || (t >= time2+thal22+30.0/21600.0-delt && t <
time2+thal22+30.0/21600.0) || (t >= time2+thal23+30.0/21600.0-delt && t <
time2+thal23+30.0/21600.0) || (t >= time2+thal24+30.0/21600.0-delt && t <
time2+thal24+30.0/21600.0) || (t >= time2+thal25+30.0/21600.0-delt && t <
time2+thal25+30.0/21600.0) || (t >= time2+thal26+30.0/21600.0-delt && t <
time2+thal26+30.0/21600.0) || (t >= time2+thal27+30.0/21600.0-delt && t <
time2+thal27+30.0/21600.0) || (t >= time2+thal28+30.0/21600.0-delt && t <
time2+thal28+30.0/21600.0) || (t >= time2+thal29+30.0/21600.0-delt && t <
time2+thal29+30.0/21600.0) || (t >= time2+thal30+30.0/21600.0-delt && t <
time2+thal30+30.0/21600.0) || (t >= time2+thal31+30.0/21600.0-delt && t <
time2+thal31+30.0/21600.0) || (t >= time2+thal32+30.0/21600.0-delt && t <
time2+thal32+30.0/21600.0) || (t >= time2+thal33+30.0/21600.0-delt && t <
time2+thal33+30.0/21600.0) || (t >= time2+thal34+30.0/21600.0-delt && t <
time2+thal34+30.0/21600.0) || (t >= time2+thal35+30.0/21600.0-delt && t <
time2+thal35+30.0/21600.0) || (t >= time2+thal36+30.0/21600.0-delt && t <
time2+thal36+30.0/21600.0) || (t >= time2+thal37+30.0/21600.0-delt && t <
time2+thal37+30.0/21600.0) || (t >= time2+thal38+30.0/21600.0-delt && t <
time2+thal38+30.0/21600.0) || (t >= time2+thal39+30.0/21600.0-delt && t <
time2+thal39+30.0/21600.0) || (t >= time2+thal40+30.0/21600.0-delt && t <
time2+thal40+30.0/21600.0))
    {
        if (o1 == 0)
            { out[1] = 1;
            }
        else if (o1 == 1)
            { out[1] = 0;
            }
        if (o4 == 0)
            { out[4] = 1;
            }
        else if (o4 == 1)
            { out[4] = 0;
            }
    }
else if (t >= time2+150.0/21600.0-delt && t < time2+150.0/21600.0)
    {
        out[1] = 0;
        out[4] = 0;
    }
}

if (sw3 == 1)
    {
        if (t >= time3+30.0/21600.0-delt && t < time3+30.0/21600.0)
            {
                out[2] = 1;
                out[5] = 0;
            }
        else if ((t >= time3+twal1+30.0/21600.0-delt && t <
time3+twal1+30.0/21600.0) || (t >= time3+twal2+30.0/21600.0-delt && t <
time3+twal2+30.0/21600.0) || (t >= time3+twal3+30.0/21600.0-delt && t <

```



```

time6+twal36+30.0/21600.0) || (t >= time6+twal37+30.0/21600.0-delt && t <
time6+twal37+30.0/21600.0) || (t >= time6+twal38+30.0/21600.0-delt && t <
time6+twal38+30.0/21600.0) || (t >= time6+twal39+30.0/21600.0-delt && t <
time6+twal39+30.0/21600.0) || (t >= time6+twal40+30.0/21600.0-delt && t <
time6+twal40+30.0/21600.0))
    {
        if (o5 == 0)
            { out[5] = 1;
              }
        else if (o5 == 1)
            { out[5] = 0;
              }
        if (o2 == 0)
            { out[2] = 1;
              }
        else if (o2 == 1)
            { out[2] = 0;
              }
    }
else if (t >= time6+150.0/21600.0-delt && t < time6+150.0/21600.0)
    {
        out[5] = 0;
        out[2] = 0;
    }
}

```

```

psp1 = sp1;
psp2 = sp2;
psp3 = sp3;
o0 = out[0];
o1 = out[1];
o2 = out[2];
o3 = out[3];
o4 = out[4];
o5 = out[5];
}

```

VITA

Somasundaram Essakiappan graduated with a Bachelor of Engineering degree in Electrical Engineering from the College of Engineering, Guindy, Anna University, India in 2007. He joined the graduate program in Electrical Engineering at Texas A&M University in Fall 2007 and received his Master of Science degree in May 2010.

His research interests include power converters, power quality issues and renewable energy sources.

He can be reached at somasundaram_anm@tamu.edu or through the Department of Electrical Engineering at 3128 TAMU, Mailbox # 300, College Station, Texas 77843-3128