A PARTITIONING APPROACH FOR PARALLEL SIMULATION OF AC-RADIAL SHIPBOARD POWER SYSTEMS

A Dissertation

by

FABIAN MARCEL URIARTE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2010

Major Subject: Electrical Engineering

A PARTITIONING APPROACH FOR PARALLEL SIMULATION OF AC-RADIAL SHIPBOARD POWER SYSTEMS

A Dissertation

by

FABIAN MARCEL URIARTE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Approved by:

Chair of Committee,	K.L. Butler-Purry
Committee Members,	S.P. Khatri
	C.O. Malave
	C. Singh
Head of Department,	C.N. Georghiades

May 2010

Major Subject: Electrical Engineering

ABSTRACT

A Partitioning Approach for Parallel Simulation of AC-Radial Shipboard Power Systems. (May 2010)

Fabian Marcel Uriarte, B. S. Virginia Tech;
M.S., Virginia Tech
Chair of Advisory Committee: Dr. Karen L. Butler-Purry

An approach to parallelize the simulation of AC-Radial Shipboard Power Systems (SPSs) using multicore computers is presented. Time domain simulations of SPSs are notoriously slow, due principally to the number of components, and the time-variance of the component models. A common approach to reduce the simulation run-time of power systems is to formulate the electrical network equations using modified nodal analysis, use Bergeron's travelling-wave transmission line model to create subsystems, and to parallelize the simulation using a distributed computer. In this work, an SPS was formulated using loop analysis, defining the subsystems using a diakoptics-based approach, and the simulation parallelized using a multicore computer.

A program was developed in C# to conduct multithreaded parallel-sequential simulations of an SPS. The program first represents an SPS as a graph, and then partitions the graph. Each graph partition represents a SPS subsystem and is computationally balanced using iterative refinement heuristics. Once balanced subsystems are obtained, each SPS subsystem's electrical network equations are formulated using loop analysis. Each SPS subsystem is solved using a unique thread, and each thread is manually assigned to a core of a multicore computer.

To validate the partitioning approach, performance metrics were created to assess the speed gain and accuracy of the partitioned SPS simulations. The simulation parameters swept for the performance metrics were the number of partitions, the number of cores used, and the time step increment. The results of the performance metrics showed adequate speed gains with negligible error.

An increasing simulation speed gain was observed when the number of partitions and cores were augmented, obtaining maximum speed gains of <30x when using a quad-core computer. Results show that the speed gain is more sensitive to the number partitions than is to the number of cores. While multicore computers are suitable for parallel-sequential SPS simulations, increasing the number of cores does not contribute to the gain in speed as much as does partitioning.

The simulation error increased with the simulation time step but did not influence the partitioned simulation results. The number of operations caused by protective devices was used to determine whether the simulation error introduced by partitioning SPS simulations produced a inconsistent system behavior. It is shown, for the time step sizes uses, that protective devices did not operate inadvertently, which indicates that the errors did not alter RMS measurement and, hence, were non-influential.

DEDICATION

To my nuclear family. I thank them all for their immense patience,

which was the only necessary and sufficient condition to complete this work.

ACKNOWLEDGEMENTS

First and foremost I would like to acknowledge the effort, support, and trust bestowed upon me by my advisor Dr. K. L. Butler-Purry. I thank her for encouraging me through difficult times and believing in me. Without her guidance, far-sighted experience, and faith in the investigation this work could not have been completed.

The works of the following authors in the areas of modeling and simulation implementation was considered inspirational during the development of this dissertation: H. W. Dommel and J. R. Marti (University of British Columbia), K. Strunz (University of Washington), N. Watson (University of Canterbury), and T. Noda (Doshisha University). I would like to thank the aforementioned authors for the level of detail presented in their writings, which motivated the beginnings of this work.

I would thank Dr. A. Abur for teaching the course of Power System Electromagnetic Transient Analysis during his association with Texas A&M University in 2004. I would like to thank Dr. Khatri for his guidance in the area of computer engineering during the final stages of this dissertation. Additionally, I would like to thank Dr. P. Li, also from the department of Computer Engineering, for providing recommendations on this work. I would like to thank Dr. C. Malave for his friendship and, most importantly, for encouraging me to “stay put” in the doctoral degree program at Texas A&M.

TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

Page

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 INTRODUCTION

Time domain computer simulations of Shipboard Power Systems (SPSs) are required to assess electric-service continuity under hostile conditions in advance of deployment [1]. Said simulations, however, are notoriously slow, limit the number of case studies that can be conducted in a day, and consume many machine hours. Time domain simulations are slow principally due to: the order of full-order SPS models, the quantity and time-varying nature of the component models, and the single-matrix approach taken by simulation programs to perform the simulations.

The purpose of this research is to reduce the run-time of AC-Radial SPS time domain simulation. Time domain simulation is a comprehensive simulation scheme that can be used for the following types of studies: steady-state analysis, short-circuit analysis, power flow analysis, protective device coordination studies, preventive and predictive topology reconfiguration studies, among others. To address the problem of slow SPS time domain simulations, the solution methodology presented in this work parallelizes the simulation of SPSs using multicore computers.

This dissertation follows the style of the IEEE *Transactions on Power Systems*.

Multicore computers are commercially available desktop computers containing a single processor with embedded (and independent) processing units called cores. The advent of multicore computers has reduced parallel computing costs to an all-time low and has become an attractive low-cost parallel computing option.

Presently, SPS simulation is conducted using either general purpose commercial power system simulation software or real-time simulators. Commercial software simulators are typically used to simulate reduced order SPSs in favor of timely results. The simulation of reduced order SPSs returns fast simulation results at the expense of not knowing the entire system's behavior. Real-time simulators [2-4] are an integrated hardware-software solution used to interface power apparatus and simulations in real-time, are extremely efficient, and are faster than commercial power system simulators. However, real-time simulators are also limited to power systems of small order.

The present-day inability to obtain timely simulation results of full-order SPS simulations has motivated to reducing the run-time of SPS simulation using multicore computers. The approach to parallelize the simulation of SPSs in this work is presented in three stages: discretization and formulation, partitioning, and simulation. A brief description of each stage ensues.

Discretization is the process of mathematically representing a system described in the time domain as a system modeled at discrete intervals of time. To discretize the SPS model used in this work, each SPS component model was discretized by replacing the inductors and capacitors with equivalent discretized branches. After each component model was discretized, the SPS was formulated in loop current as variables by interconnecting all of the discretized component models together. The resulting formulation is a system of equations solved at discrete intervals of time.

The partitioning stage consists of tearing a SPS into subsystems to parallelize time domain simulations. To determine where to tear the SPS, a weighted graph representative of an SPS was created. Each graph vertex represents a discretized SPS component model and each graph edge represents an electrical junction where two or more component models interconnect. The weight of each vertex is based on the estimated computational effort of solving the equations of the model a vertex represents. This stage begins by partitioning the representative graph using the mincut algorithm [1-2],[3] to produce an initial segregation. To balance the weighted graph partitions, balancing heuristics are used to move vertices across partitions. The edge-cut resulting from the balancing heuristics corresponds to the points of disconnection on the SPS where tearing occurs.

When the points of disconnection of the SPS have been determined, a partitioning approach motivated by diakoptics [4] is used to tear the SPS into subsystems. The partitioning approach presented in this work uses capacitor loops as the points of disconnection. By shorting two (out of three) capacitors on three-phase cables, a large portion of the network matrix's off-diagonal region is depleted producing subsystem decoupling. This rapid off-diagonal depletion is a direct result of the formulation approach taken, which concentrates loop currents at bus node capacitors where most of disconnection points are.

Finally, the simulation stage consists of using threads to simulate the SPS subsystems, and manually assigning the threads to the cores of a multicore computer. A multithreaded program was developed in C# to solve SPS subsystems using the electromagnetic transients program (EMTP) solution approach [5], where each subsystem's electrical network is solved before its control network. After finding the loop currents in each subsystem, the branch currents and node voltages for all components are found. Select instantaneous voltages and currents from the electrical network are passed to the control network as inputs to solve controller equations, determine diode commutation times, calculate the root-mean-squared (RMS) voltages and currents, and determine if protective devices should operate.

To assess the performance and validity of the partitioning approach, the speed, accuracies, and time step variations are used as performance metrics. Speed is assessed by taking the ratio between unpartitioned and partitioned simulation run-times. Accuracy is determined by comparing the unpartitioned and partitioned simulation results at each time step of the simulation. The time step was varied to determine how the simulation error (if any) varies when using different time step sizes.

The contributions of this work are in four areas. The first lies in the formulation approach, where the loop currents are concentrated at bus node capacitor loops. This formulation approach is advantageous because tearing only a few capacitors depletes the off-diagonal structure of the network matrix and permits block-diagonalizing the network matrix. The second is related to the first in that after partitioning the representative graph using the mincut algorithm, the SPS subsystems are balanced with a minimal (if any) edge-cut increase. The edge-cut does not increase when vertices at bus nodes are moved to another partition adjacent at the same bus node. The third resides in the tearing of only two out of three capacitors in a loop. By tearing only two capacitors at each boundary, the number of constraint equations is two for each disconnection point regardless of how many graph edges are torn from the same boundary; having only a few constraint equations keeps the computation of the boundary condition low. And the fourth consists in the empirical determination that sequential-parallel SPS simulations (i.e., many threads per core and even with load imbalance) on multicore computers are computationally more efficient than purely parallel simulations. To note, the most important final result is that AC-Radial SPS simulation run-time is significantly reduced at bare cost since multicore computers are already (*virtually*) on every desktop if not all.

1.2 ORGANIZATION

This dissertation is organized into five chapters. The second chapter introduces the difficulty of large-scale SPS simulation, justifies the work discussing recent efforts in computational burden reduction, and presents a differential-algebraic (DAE) formulation of a notional AC-Radial SPS. The third chapter describes the solution methodology in three stages: discretization, partitioning, and simulation. The fourth chapter assesses the solution methodology's performance by evaluating three performance metrics. The fifth chapter concludes and examines future work.

CHAPTER II

LITERATURE REVIEW AND PROBLEM FORMULATION

2.1 INTRODUCTION

This chapter reviews common commercial power system simulators, introduces AC-Radial SPSs, common solutions to partitioning power systems, and presents the differential-algebraic equation (DAE) formulation of a notional SPS. Power system simulators are also introduced to discuss current simulation tools and simulation approaches. Time domain simulations are introduced to explain how computer resources can be rapidly depleted. A general description of AC-Radial SPSs is presented to introduce the topology and saliencies found on SPSs as the system that will be studied in this work. Since the approaches to parallelize power system simulation is fairly commonplace and well documented elsewhere, only those approaches that frequently appear in the literature are reviewed. The DAE formulation at the end of this chapter is used to assess the complexity of SPS time domain simulations and to estimate the order of a notional SPS.

2.2 MOTIVATION OF THE WORK

Power system simulators rely on analytical methods programmed into desktop computers (e.g., PCs) to simulate behavior of electrical power systems. The drawback of simulators is the lengthy run-time in simulating large-scale electrical networks. The simulation of large-scale electrical networks imposes considerable computational burdens and can rapidly deplete available processing power and memory storage.

The result of simulations depleting computing resources is a limitation in the system order that can be simulated in a reasonable amount of time. The depletion of processing power and memory is especially true of time domain simulations, where the computational burden is pronounced and millions of data points are saved. Simulation of full order SPSs can take valuable hours, days, or even weeks to complete depending on the case study, order, and simulation end time $\left(t_{end}\right)$. Such time dedication of computational resources may be detrimental to research budgets and has motivated the reduction of run-time by parallelizing SPS simulations. The considerations that motivated this work are summarized in Fig. 2.2.1, where the current problem is depicted on the left side and the aspects desired from a solution are shown on the right.

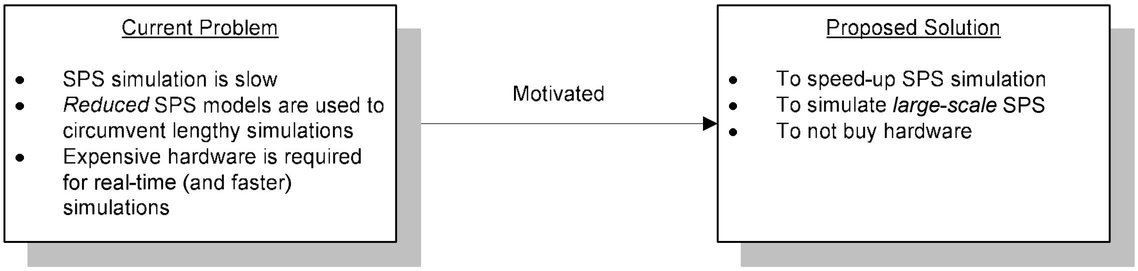

Current Problem
• SPS simulation is slow
• *Reduced* SPS models are used to circumvent lengthy simulations
• Expensive hardware is required for real-time (and faster) simulations
Motivated
Proposed Solution
• To speed-up SPS simulation
• To simulate *large-scale* SPS
• To not buy hardware

Fig. 2.2.1. Motives and desired aspects of a solution

In what follows of this chapter, the system order, complexity, and common characteristics found on SPSs are presented. The following subsection introduces AC-

Radial SPSs followed by a formulation that gives an ideal of the system order in the form of DAEs.

2.2.1 AC-Radial Shipboard Power Systems

This section presents a brief overview of AC-Radial SPSs. More details on AC-Radial SPSs are documented in [6-10]. The SPS examined here shares some characteristics of the U.S. CG 61 surface combatant [11].

Generally, a combatant type ship consists of a three-generator system in a ring configuration; in typical operation, two generators are used, while the third serves as an emergency supply. Three-phase power is generated and distributed in an ungrounded delta fashion to ensure continued electrical supply despite single-phase to hull faults [9]. An illustration of a notional AC-Radial SPS is given in Fig. 2.2.2.

The voltage is generated at 450V at 60Hz and distributed to the system via switchboards. Generator switchboards are composed of one of more switchgear units and are located close to their associated generators. The switchboards, among themselves, are connected in ring topology so that loads can be fed from any generator. Bus tie circuits interconnect the generator switchboards, which allow for the transfer of power from one switchboard to another.

From each switchboard emanate radial paths to supply loads directly or from load centers. Load centers are distribution centers below the switchboard level and are used to supply power to load concentrations in various areas of the ship. There are two types of loads, non-vital and vital. The non-vital loads have only one supply path to a switchboard and are connected from the load centers. Vital loads have two supply paths (normal and alternate) and are connected to switchboards or load centers via automatic- or manual bus transfers (ABTs and MBTs, or XBTs to refer to either).

The major types of protective devices utilized in the U.S. Navy ship electrical power systems are fuses, circuit breakers, and relays [10]. The purpose of protective devices is to mitigate damage to electrical equipment during abnormal conditions. The fundamental characteristics of protective devices are to monitor system voltage and current levels, detect the presence of abnormalities, and to intelligently reconfigure the routing of power to maintain power continuity at loads vital to crew survival.

The vessel's load to generation ratio is high (i.e., stiffly-connected system); thus, there is not much of a reserve margin in case of severe faults or catastrophic conditions. The generation system is a finite inertia one, where, as opposed to terrestrial systems, generation has a limited capacity. A consequence of finite-inertia systems is that during disturbances the system is prone to pronounced under-frequencies, under-voltages, and inter-rotor oscillations.

A general description of AC-Radial systems was given in this subsection to highlight saliencies that distinguish SPSs from terrestrial power systems. The next section introduces commercial power system simulators.

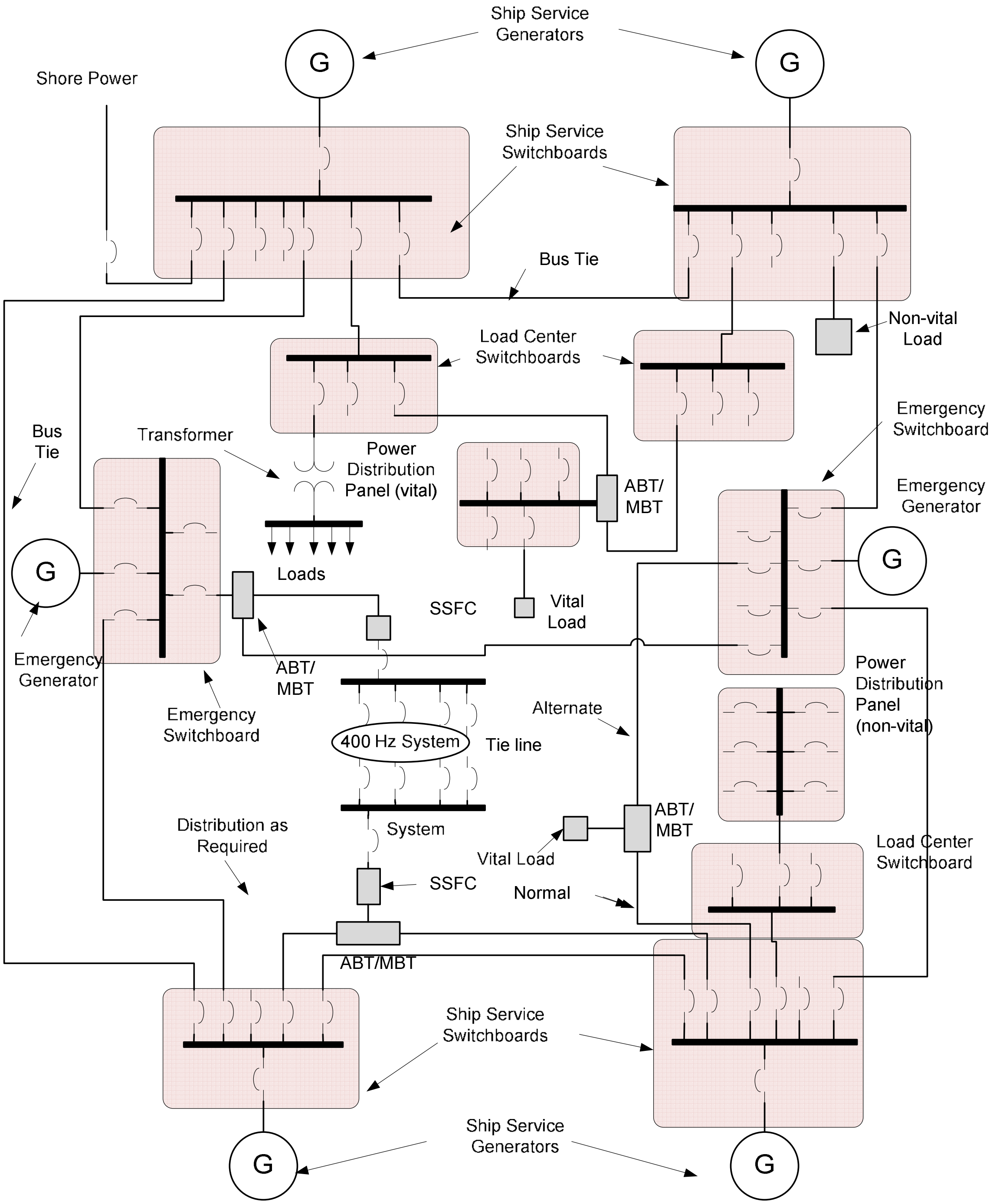


Fig. 2.2.2. General electrical layout of AC-Radial Shipboard Power Systems [12]

2.2.2 Power System Transient Simulators

Available power systems simulators range from commercial ones to free ones [13]. Some well-known commercial simulators are EMTDC/PSCAD [14], ETAP [15], EMTP-RV [16], PLECS [17], SimPowerSystems [18], PowerFactory [19], and PowerWorld [20]. Some of free simulators include ATP [21], InterPSS [22], and VTB [23].

Most simulators solve power systems by implementing the electromagnetic transients program (EMTP) solution approach [5],[24]. The EMTP approach discretizes power system branches (i.e., inductors and capacitors) and forms a large nodal conductance matrix, which corresponds to writing Kirchhoff's current law (KCL) equations at each node. The set of nodal equations have the form $\mathbf{A}\cdot\mathbf{x}=\mathbf{b}$, where **A** represents the nodal conductance matrix, **x** represents the vector of node voltages, and **b** represents the vector current injection at each node. The solution of the node voltages takes place in incremental time steps (i.e., at $k = 0, k = 1, k = 2, \ldots$) and rapidly becomes burdensome as the order of the system increases. The aforementioned simulators all experience the problem of burdensome time domain simulations and depletion of computational resources which lead to the problems listed in Fig. 2.2.1.

Albeit multicore technology in desktop computers, commercial power system simulators do not fully exploit their potential for parallelism. For example, PSCAD/EMTDC uses two cores: one core for PSCAD [25] to render the graphical interface and run-time meters, and the other for the solver (EMTDC [26]). Since the solution produced by EMTDC is executed by only one core, the simulation is not a parallel one.

Other simulators such as EMTP-RV [16] have not yet implemented any parallel strategies. At InterPSS [22], a distributed power system simulation approach has been developed. Such approach uses grid-computing, where transient stability case studies for large-scale power systems can be ran simultaneously on different computers. The solution of *each* case study, however, is not divided. Each case study runs concurrently on a different machine. A limitation of distributed grid-computing is the linear speed gain limit, where if *M* computers are used, the maximum speed gain would be *M*.

Real-time simulators, such as RTDS® and Opal-RT®, can partition power systems only if Bergeron's traveling-wave line model can be used. That is, a transmission line of sufficient physical length must exist in order to partition power systems. If said line does not exist in the power system being modeled, short-lines (stublines [27]) with one time step delay can be used instead. The effects of inserting one time step delay stublines where none exist may introduce phase drifts and run longtime simulations unstable [28]. As of this writing, the largest system that can be simulated in real-time is by company Opal-RT®, which currently can solve 330 buses in real-time [29] using a cluster of quad-core computers ; however, hardware cost is significant and stublines would be required to partition the short cables on SPSs. A summary of partitioning capabilities (if any) of today's commercial power system simulators is reported in Table II.1.

TABLE II.1. SUMMARY OF COMMERCIAL POWER SYSTEM SIMULATOR PARTITIONING ABILITIES

Program	Partitioning Ability
ATP	Does not partition
EMTP-RV	Does not partition
ETAP	Does not partition
InterPSS	Transient stability case studies possible on a distributed computer
PowerFactory	Does not partition
PSCAD/EMTDC	One thread renders graphics (PSCAD); one thread solves power system (EMTDC)
RSCAD	Real-time simulation software power systems using Bergeron's travelling-wave model
RTLAB	Real-time simulation software power systems using Bergeron's and/or stublines
SimPowerSystems	Uses MATLAB's engine which is multicore capable; power systems are not partitioned
Virtual Test Bed	Does not partition

*Information based on in-person conversations and emails with technical support

The concepts of time domain simulation and how computing resources are depleted are presented next. After focusing on background information in time domain simulation, relevant solutions to ameliorate time domain simulations are described.

2.2.2.1 Time Domain Simulation

Time domain simulations are computer-based simulations of physical systems for an intended continuum of time (e.g., from $t_{start} = 0\text{s}$ to $t_{end} = 20\text{s}$). Since computers actuate on clock pulses, computer simulations are inherently a discrete-time processes. To simulate physical systems for an intended continuum of time, said systems are discretized and solved at discrete instances with a time step increments of Δt seconds.

A time line illustrating the concept of time domain simulation is depicted in Fig. 2.2.3. The first time step (step, hereinafter) solved is $k = 0$, which represents $t = 0\text{s}$. After the system is solved at $k = 0$, the step advances to $k = 1$ and the system is solved again using part of the previous solution from $k = 0$. The integer increments of k are continued throughout the intended simulation time. As illustrated by Fig. 2.2.3, if

$\Delta t = 50\mu\text{s}$, a simulation of $t_{end} = 20\text{s}$ would require $k_{end} = \frac{t_{end}}{\Delta t} = \frac{20}{50\mu\text{s}} = 400{,}000$ solutions of $\mathbf{A} \cdot \mathbf{x} = \mathbf{b}$, which can take hours, days, or even weeks depending on how long the solution at each k takes.

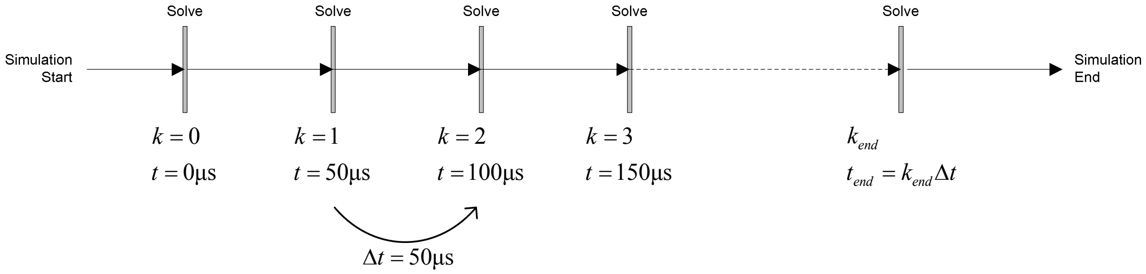


Fig. 2.2.3. Illustation of fixed time step time domain simulation

2.2.2.2 Computational Burden

Simulation run-time is directly related to the solution time at each k as illustrated in Fig. 2.2.3. If the solution at step k takes 0.216s to complete, solving 400,000 steps would take $0.216 \times 400{,}000 / 3{,}600 = 24$ hours. Spending 24 hours on a single case-study is impractical in terms of the number of cases studies that can be ran in one day; hence, a motivation to reduce the computational burden exists.

A close-up of the solution process at each k in Fig. 2.2.3 is given in Fig. 2.2.4. In Fig. 2.2.4, a few sub-processes occur at each k (details can be found in Fig. 12.23 in [30]). The solution to $\mathbf{A} \cdot \mathbf{x} = \mathbf{b}$ at each k constitutes ~90% percent of the solution time, particularly when the order of the system is $O\left(10^3\right)$.

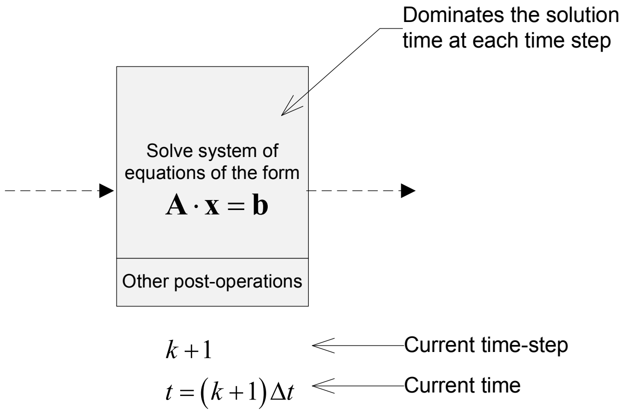

Dominates the solution time at each time step
Solve system of equations of the form
$\mathbf{A}\cdot\mathbf{x}=\mathbf{b}$
Other post-operations
$k+1$
Current time-step
$t=(k+1)\Delta t$
Current time

Fig. 2.2.4 The simulation process at each time step (fixed Δt assumed)

Lengthy run-time often leads researchers into buying costly equipment to speed-up simulation, or modeling reduced equivalent power systems at the expense of not being able to observe system-wide dynamics. An important argument may be made at this point: the main reason time domain simulation is slow is due to the solution of a large system of equations in the form $\mathbf{A}\cdot\mathbf{x}=\mathbf{b}$ at every time step. If the solution to $\mathbf{A}\cdot\mathbf{x}=\mathbf{b}$ can be sped up, run-time will be reduced dramatically.

2.2.2.3 Memory Depletion

Time domain simulations of power systems aim to capture node voltages and branch current in as many places as possible (i.e., preferably at every relay). To save system-wide voltage and current information, 12 quantities may have to be saved: 3 instantaneous voltages, 3 instantaneous currents, 3 RMS voltages, and 3 RMS currents. To store each of these 12 quantities in memory at each k, computer numbers of type *double* are typically used.

Each double requires 8KB (64 bits) of memory (RAM) on desktop computers. To illustrate how a computer's memory can be depleted, consider saving 12 values per relay and at each k. Supposing there are 100 relays in a system, and $t_{end} = 20\text{s}$, the total memory that must be allocated is computed in (2.1), which is a considerable amount considering that desktop computers (as of this writing) typically sell with 4GB of RAM (expansion capability to 8-16GB is typical).

$$\begin{array}{c}\text{Memory}\\ \text{Storage}\end{array} \rightarrow \underbrace{100}_{\text{relays}} \times \underbrace{12}_{\text{quantities}} \times \underbrace{400,000}_{\text{no. steps}} \times \underbrace{8}_{\text{bytes}} = 3.84 \times 10^{9} \approx 3.8\text{GB} \qquad (2.1)$$

If more than 12 quantities were saved at each k, 4GB could be exceeded. Simulations requiring 4GB of memory are impractical and slow down user-interface response times.

To avoid depleting computer memory, it may be possible to i) save numeric data using a different number type (e.g., *floats* instead of *doubles*), ii) save less data per relay (e.g., only instantaneous quantities), iii) reduce the number of relays, iv) simulated for less time, or v) move the data from memory to files on the hard-drive. The former may result in loss of accuracy. Reasons ii)-iv) hinder the ability to observe system-wide dynamic phenomena. The latter solution increases simulation timeas writing data to the file system introduces a new bottleneck.

This section presented the concept of time domain simulation and the main reasons they are slow. The next section reviews common partitioning approaches to reduce simulation run-time.

2.3 EXISTING SOLUTIONS TO REDUCE SIMULATION RUN-TIME

The tendency to reduce power system simulation run-time has been, and is, to parallelize power system simulations [31]. However, it is only recently that multicore computers have made this objective a closer and a low-cost possibility. To parallelize power system simulations, the power system models must be partitioned first. A review of power system partitioning methods is reported in this section, where a classification of said methods is shown in Fig. 2.3.1.

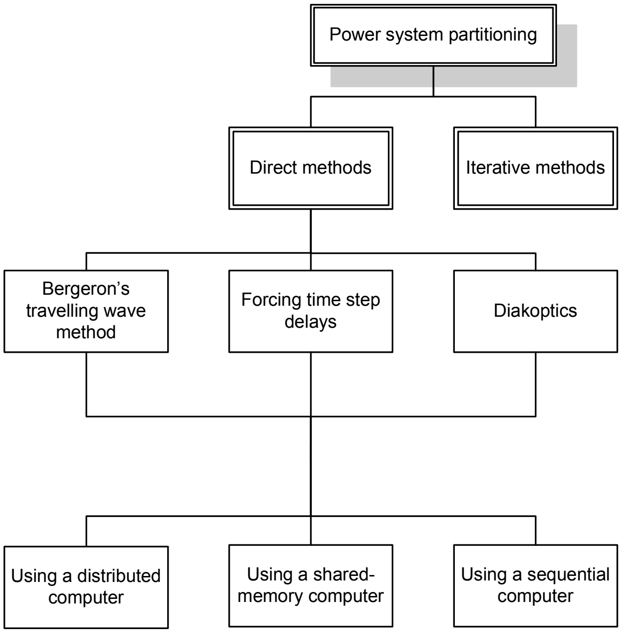

Power system partitioning
Direct methods
Iterative methods
Bergeron's travelling wave method
Forcing time step delays
Diakoptics
Using a distributed computer
Using a shared-memory computer
Using a sequential computer

Fig. 2.3.1. Classification of power system partitioning methods

Direct methods divide power systems into subsystems, and solve each subsystem using factorization. After the solution of each subsystem takes place, there is an exchange of boundary variables to accountfor the influence of neighbor subsystems.

Iterative [32-33] methods solve the subsystems by guessing their solution and then exchanging boundary information several times during the same time step until converge is reached. The present work uses a direct partitioning approach; hence, iterative methods are not considered here. The implementation of a partitioning method to parallelize a power system's simulation can be on a combination of a distributed computer, shared-memory computer, or a sequential computer.

A distributed computer is a group of computers networked together working towards a common goal [34]. Each computer in a distributed computer network is referred to as a computational node, which is a stand-alone computer having independent memory and processor. The communication among computational nodes requires a physical communication network where messages among computational nodes are synchronized by the master computer. The computational nodes may or may not be in physical proximity. The main disadvantage of distributed computers is the communication network's latency, and constitutes a bottleneck in parallel simulations when too many computers are used.

A shared-memory computer is a computer having multiple processing units sharing on-board memory [35]. The processing units communicate by writing/reading to/from on-board shared-memory, which is fast and does not require an external communication network for the processing units to exchange data. A modern day example of shared-memory computers are multicore computers, which have one processor with various internal independent processing units (cores) that can work concurrently. The main drawback of shared-memory computers is that the number of cores is fixed, and cannot be changed unless the computer is replaced.

An alternative form of shared-memory computer is the graphical processing unit (GPU). GPUs are graphical cards embedded in PCs (can be added after purchase) containing cores that also communicate with via shared-memory. GPUs are designed to be extremely fast at processing large graphics data. However, GPU use for non-graphic operations such as scientific computation has drawn much attention in recent years [36]. The main reasons to use GPUs are the performance/$ or benefit-cost ratio, increasing performance growth (i.e., at a faster rate than PCs), faster on-board memory bandwidth, and outstanding performance: GPUs can outperform PCs in floating-point arithmetic . In this work, GPUs are not considered, because of the need for a user to own specialized hardware, low on-board memory [37], and the initial hardware investment requirement. Multicore computers remain an attractive option due to their larger on-board memory, ubiquity, and positioned market (in-place) infrastructure, which implies a zero-cost investment.

A sequential computer is a computer with one processing unit. Work carried out with single-processor computers is purely sequential and processing cannot be parallelized. Sequential computers are no longer commonplace desktop computers as the advent, low-price, and performance of multicore computers outweigh sequential computers.

The work in this dissertation falls under the category of direct methods using a shared-memory (multicore) computer. The next subsection reviews direct partitioning methods relevant to this work.

2.3.1 Bergeron's Travelling-Wave Model

Long transmission lines naturally decouple power system areas due to wave propagation delays on transmission lines. This natural decoupling has motivated simulating each power system area on a different processor. The parallel simulation approach that exploits wave propagation delays is known as Bergeron's model [38].

Consider the one-line diagram of a transmission-line shown in Fig. 2.3.2. Due to the line length, an event occurring in area k (sending-end) will not be perceived by area m (receiving-end) until τ seconds later. In this regard, Bergeron's equations suggest the equivalent circuit in Fig. 2.3.3.

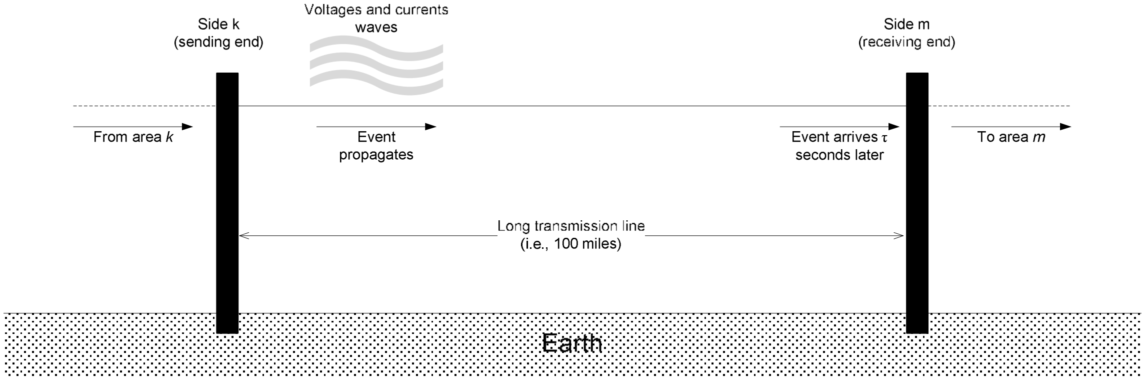


Fig. 2.3.2 . A long transmission-line representation

In Fig. 2.3.3, the current sources are delayed by τ seconds and inject current for events that occurred in the neighbor area τ seconds ago (noted as $t-\tau$). The equations describing Bergeron's model are given in (2.2). In (2.2), Z_C is the characteristic impedance of the line, d is the line length, υ is the propagation speed, and $\{L',C'\}$ are the line's per-unit length inductance and capacitance.

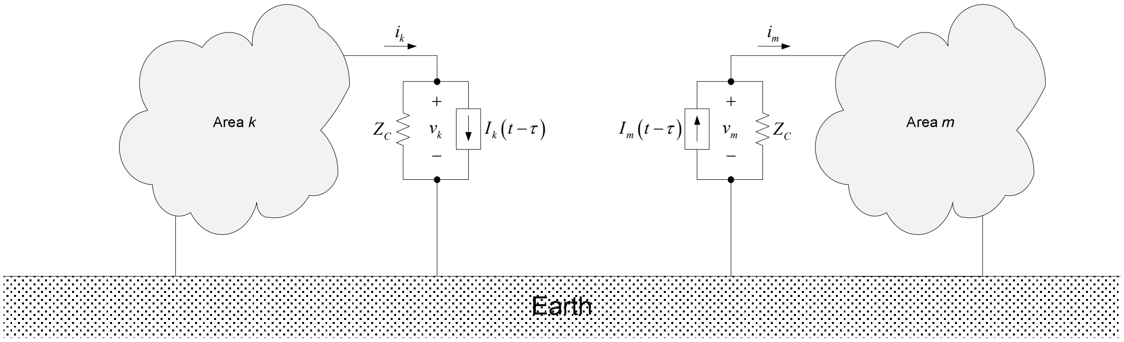


Fig. 2.3.3. Bergeron’s equivalent circuit model for a long (lossless) transmission line

$$
\begin{aligned}
I_k &= i_m\left(t-\tau\right)+\frac{1}{Z_c}v_m\left(t-\tau\right)\\
I_m &= i_k\left(t-\tau\right)+\frac{1}{Z_c}v_k\left(t-\tau\right)\\
\tau &= \frac{d}{\upsilon} \quad \upsilon=\frac{1}{\sqrt{L'C'}}\; Z_C=\sqrt{\frac{L'}{C'}}
\end{aligned}
\tag{2.2}
$$

The advantage of Bergeron’s model is that power systems can be formulated in block-diagonal form [39] and simulations easily parallelized. Bergeron’s method appears frequently in power system partitioning literature and is introduced first.

J. A. Hollman and J. R. Marti [40] used a real-time PC-cluster to simulate terrestrial transmission systems. The inter-PC decoupling was based on Bergeron’s model, where each power subsystem was solved on a different computational node. When using two PCs, speed gains of 32.89% and 37.05% were reported [41]. Four years later, the same authors published a paper [40] showing results from a five-computer PC-cluster as well as the expected results from a 19-computer cluster. The gains achieved with five computers neared 4, while the gains expected with 19 computers neared 19, which are close to linear speed-ups. It was shown that Bergeron's model was suitable for PC-cluster implementations which resulted in higher speed gains than when simulating subsystems on a single computer.

D. M. Falcao *et al*. [39] implemented Bergeron's method on a Inmos Transputer T800 connected in a hypercube topology. A speed gain of 4.92 was observed for a power system consisting of 1,026 nodes, 2,457 branches, and 146 lines, partitioned into 77 subsystems.

J. R. Marti and L. R. Linares [42] implemented Bergeron's traveling wave model to simulate small power systems in real-time using an IBM RISC System/6000 Model 560, also on a hypercube architecture. When using two processors, a 45% improvement of speed (gain of 2.22) was reported; 66% (gain 4.93) on four-processors, and gains of ≤ 1 beyond four processors. The loss of gain is attributed to the increasingly communication overhead from adding more processors (or when creating more subsystems).

Bergeron's model allows formulating power systems in block-diagonal form and is highly desirable in parallel simulations. However, there is a fundamental limitation intrinsic to Bergeron's model: the time step Δt must be an integer fraction N of the travel-time delay (i.e., must be smaller) τ [43] as given by (2.3).

$$\Delta t = \frac{1}{N}\tau = \frac{1}{N}\frac{d}{\upsilon} \tag{2.3}$$

For example, for a line of d=10km, the maximum time step (N=1) is restricted to Δt=50μs [40] (assuming a phase velocity of $\upsilon = 200 \times 10^6$ m/s). Application of

Bergeron's model in SPSs would result in even a smaller time steps because the transmission lines on SPSs are cables of very short physical length. For example, in a SPS cable of $d = 100\text{m}$ (assuming $\upsilon = 200 \times 10^6$ m/s), the time step would be restricted to $\Delta t \le 50\text{ns}$ and would counter-act any speed gains obtained from parallelizing SPS simulations.

2.3.2 The Use of Time Step Delays

Discretization of differential equations results in difference equations with both present and previous time step terms. One approach to parallelize simulations is via explicit integration algorithms (e.g., inductors become historical current sourcesand capacitors become historical voltages sources). Discretization of (2.4) using the trapezoidal rule of integration yields (2.5), where appearance of $v(t)$ on the LHS makes the integration implicit (i.e., the state-variable $i(t)$ and input $v(t)$ are solved simultaneously).

$$v(t) = L\frac{d}{dt}i(t) \tag{2.4}$$

$$\frac{v(t) + v(t-\Delta t)}{2} = \frac{L}{\Delta t}\big(i(t) - i(t-\Delta t)\big) \qquad \text{(implicit)} \tag{2.5}$$

T. Noda and S. Sasaki [44] simulated a power distribution network on a PC-cluster by partitioning the network using explicit integration to create decoupling. The explicit integration presented in [44] is a modified version of the trapezoidal rule, which is given in (2.6). The advantage of explicit integration is that state-variables can be expressed as functions of previous time step (i.e., known) values. For example, in (2.6) if $i_L(t)$ represents an inductor's current, an inductor branch can be modeled as a historical current source instead of in resistive-companion form [45].

Explicit integration permits partitioning inductors by current source transportation [46], and shunt capacitances by voltage splitting. In [44] the simulation speed gain resulting from explicit integration to partition distribution lines was the use of Δt=85μs at a real-time simulation speeds.

$$\frac{3}{2}v(t-\Delta t)-\frac{1}{2}v(t-2\Delta t)=\frac{L}{\Delta t}\big(i(t)-i(t-\Delta t)\big) \qquad (\text{explicit}) \qquad (2.6)$$

Another method to parallelize simulations based on time step delays is the latency insertion method (LIM) [47-48]. The LIM algorithm takes advantage of the inherent latency in inductors and capacitors to generate a leapfrog algorithm, which first solves for an electrical network's branch currents and then for the node voltages. In the LIM, if branches do not contain inductors, or if nodes do not contain capacitors, inductors and capacitors are artificially added to force the latency exploited by the leapfrog algorithm. When using the LIM, all branches and nodes are treated as shown in Fig. 2.3.4. The independent sources are non-zero only if they are physical present.

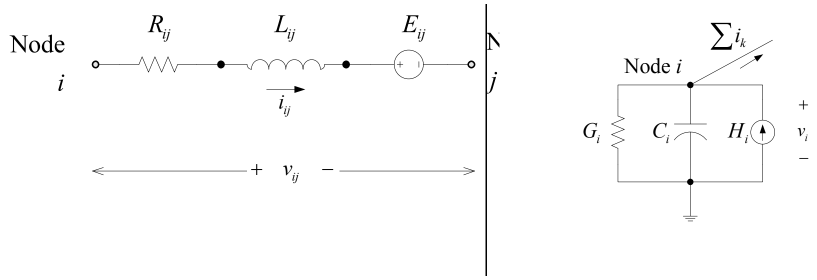


Fig. 2.3.4. Branch (left) and node (right) as modeled by the latency insertion method

In the LIM, which uses the backward Euler discretization, the branch currents and node voltages in Fig. 2.3.4 are discretized and solved as (2.7) and (2.8), respectively.

$$i_{ij}^{k+1} = i_{ij}^{k} + \tfrac{\Delta t}{L_{ij}}\left(v_{ij}^{k+\frac{1}{2}} - R_{ij} i_{ij}^{k} + E_{ij}^{k+\frac{1}{2}}\right) \tag{2.7}$$

$$v_i^{k+\frac{1}{2}} = \frac{\frac{C_i v_i^{k-\frac{1}{2}}}{\Delta t} + H_i^k - \sum i_k}{\frac{C_i}{\Delta t} + G_i} \tag{2.8}$$

At time step $k+1$, the leapfrog algorithm first solves for all branch currents using (2.7). Once all branch currents are known, and before advancing the time step to $k+2$, all node voltages are solved using (2.8). The notation $k+\frac{1}{2}$ in (2.8) indicates that the node voltages are found from a post-computation following the branch current solution at $k+1$. Once the time step is advanced to $k+2$, the voltages found at $k+\frac{1}{2}$ are used to compute the branch currents at $k+2$ by using (2.7) again. The pattern of latency exploitation is clear as branch currents and node voltages are solved separately leaping back-and-forth between their solutions.

Watanabe *et al*. [49] used the LIM leapfrog method to parallelize the simulation of a power distribution network on a PC-cluster. The speed gains reported were between 20-100 times with an efficiency of 94% when using five computational nodes. The approach used to parallelize the simulations was to divide a large power distribution network into subsystems, where each subsystem was assigned to a different computational node.

At the subsystem boundaries there are a deliberate number of repeated (interface) branches and nodes considered the subsystem overlap. The subsystem overlap simultaneously exists on all subsystems created from the same boundary. At each time step of the simulation, each subsystem solves for its branch currents and node voltages using (2.7) and (2.8), respectively. Before advancing the time step, the subsystems exchange their branch current by sending them across the communication network. After receiving the currents from the adjacency subsystems, the boundary node voltages are updated by injecting the received current.

There are limitations in the LIM that prevent its application to SPSs. The first limitation is that datum nodes in SPS do not exist because when SPSs are modeled as purely ungrounded. Thus, the node model on the right of Fig. 2.3.4 cannot be formed. If said node model does not exist, the leapfrog algorithm cannot be used. Another limitation is the time step size requirement. In the case a fictitious (virtual) datum node were created for SPSs, shunt capacitors would have to be added to every node. Further, all branches containing capacitors would require inductors to be added to the same branches. Adding inductors to all branches containing capacitors, and adding capacitors to all nodes not containing capacitors, implies adding parasitic inductances and capacitances to the system. Parasitic reactance introduces fast transients that may not be physically presented and require a very small Δt to observe.

Moreover, to maintain numerical stability after introducing parasite reactance, it is recommended that the $\Delta t \leq \sqrt{LC}$, where L represents a branch inductance and C represents a node's shunt capacitance. In [49] time steps were in the order of $O\left(10^{-12}\right)$, which does not make $\Delta t \leq \sqrt{LC}$ a significant restriction. However, in power system simulation the typical time step is $\Delta t = 50\mu\text{s}$. Unless the time step is decreased, unstable simulations are possible. If the time step is reduced to $O\left(10^{-9}\right)$, run-time is significantly affected. If instead of using parasitic values for inductors and capacitors, larger values are were used instead, the physical significant of the results change. Other uncertainties regarding the application of LIM to SPSs are the suitability to time-varying and ungrounded networks, which have not been reported.

At Florida State University, a 9-rack RTDS® simulator [50] implements time step latency in two ways. The first is to create SPS subsystems by using transmission lines with travel-times of Δt [50-51]. It is noted that this line is not physically present on a SPS model; the line is intentionally placed in the SPS model to form subsystems from time step delays. The idea of placing (where physically not present) a Δt travel-time transmission line is to mimic Bergeron's travelling-wave model explained earlier.

The second method is to use a cross-rack transformer model to insert a latency and partition DC links. When partitioning DC links, the latency comes about inserting an inductor of specified value such that simulation stability is warranted. Since partitioning by insertion of latencies is artificial, its impact on simulation results should be carefully studied [52] and, hence, is not considered in this work.

2.3.3 Diakoptics-based Partitioning Approaches

Diakoptics (from Greek *kopto* meaning *to tear*, and English *dia* interpreted as *systems*) is a term associated with the work developed by G. Kron on tensorial analysis [53], which gave rise to a piecewise solution of large networks [4]. Between June 7, 1957 and February 22, 1959, G. Kron published a serial called "*Diakoptics*-The Piecewise Solution of Large-Scale Systems" in the *Electrical Journal*, London (formerly the *Electrician*), which later became available under one cover [4]. Kron's motivation was to obtain inter-area power flows knowing only intra-area power flows [54].

G. Kron's new partitioning theory was unique as it could solve large network problems using only the solutions of its component parts. Diakoptics was introduced before the digital computer, and did not receive attention until only after the sparse matrix ordering techniques suggested by Tinney [55], the discretization for computer simulation proposed by Dommel [5], and the modified nodal analysis formulation proposed by Ho [56], which became dominant and efficient digital computer methods. The introduction of Modified Nodal Analysis (MNA) by Ho and the reduction of computer size and cost led to believe that one computer alone was sufficient to solve power systems of moderate sizes during the 1970s.

Diakoptics is not taught in academia and is rarely found in electrical engineering textbooks. Other approaches, asides from diakoptics, have become main stream in the recent decades and most of the literature on partitioning does not address diakoptics as a viable option; perhaps, for the same reason that it disappeared during its beginnings. Diakoptics lost popularity before it was well established, but those who used it did see and learnt from its efficient advantages [54],[57-59].

G. Kron showed that an electrical network represented as (2.9) and solution (2.10), where $\mathbf{A}_{orig}$ is the original network (coefficient) matrix, $\mathbf{x}$ the vector of unknown variables, and $\mathbf{b}$ is the input vector, could be torn in p subsystems and reformulated as (2.11). Equation (2.11) leads to the parallelizable form in (2.12).

$$\mathbf{A}_{orig}\mathbf{x} = \mathbf{b} \tag{2.9}$$

$$\mathbf{x} = \mathbf{A}_{orig}^{-1}\mathbf{b} \tag{2.10}$$

$$\left[\begin{array}{c|c} \mathbf{A}_{block} & \mathbf{D} \\ \hline \mathbf{D}^{\mathrm{T}} & -\mathbf{S}^{-1} \end{array}\right]\left[\begin{array}{c} \mathbf{x} \\ \hline \mathbf{u} \end{array}\right] = \left[\begin{array}{c} \mathbf{b} \\ \hline \mathbf{0} \end{array}\right] \tag{2.11}$$

$$\mathbf{A}_{block} = \begin{bmatrix} \mathbf{A}_1 & & & \\ & \mathbf{A}_2 & & \\ & & \ddots & \\ & & & \mathbf{A}_p \end{bmatrix}; \qquad \mathbf{x} = \begin{bmatrix} \mathbf{x}_1 \\ \mathbf{x}_2 \\ \vdots \\ \mathbf{x}_p \end{bmatrix}_{n\times 1}; \quad \mathbf{b} = \begin{bmatrix} \mathbf{b}_1 \\ \mathbf{b}_2 \\ \vdots \\ \mathbf{b}_p \end{bmatrix}; \quad \mathbf{u} = \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_r \end{bmatrix};$$

$$\mathbf{D} = \begin{bmatrix} \mathbf{D}_1 \\ \mathbf{D}_2 \\ \vdots \\ \mathbf{D}_p \end{bmatrix}; \qquad \mathbf{S} = \begin{bmatrix} S_1 & & & \\ & S_2 & & \\ & & \ddots & \\ & & & S_r \end{bmatrix};$$

$$\mathbf{D}(i,j) \rightarrow \begin{cases} = 1, & \text{if } x_i \text{ is positively coupled to } \mathrm{u}_j \\ = -1, & \text{if } x_i \text{ is negatively coupled to } \mathrm{u}_j \\ = 0, & \text{if } x_i \text{ is not coupled to } \mathrm{u}_j \end{cases}$$

where $\mathbf{b}_i$ = excitation vector of subsystem i

$\mathbf{x}_i$ = unknown variable vector of subsystem i

$\mathbf{A}_i$ = network matrix of subsystem i

$\mathbf{A}_{block}$ = block-diagonal matrix of all subsystems' $\mathbf{A}_i$

$\mathbf{D}_i$ = tensor relating network and boundary variables

$\mathbf{S}$ = diagonal matrix of torn branch immitances

$\mathbf{u}$ = vector of torn branch boundary variables

$\cdot$ = zero matrix

p = number of network partitions.

$$\mathbf{x} = \mathbf{A}_{block}^{-1}\mathbf{b} - \mathbf{A}_{block}^{-1}\mathbf{D}\left(\mathbf{S}^{-1} + \mathbf{D}^{\mathrm{T}}\mathbf{A}_{block}^{-1}\mathbf{D}\right)^{-1}\left(\mathbf{D}^{\mathrm{T}}\mathbf{A}_{block}^{-1}\mathbf{b}\right). \tag{2.12}$$

The power systems research group at the University of British Columbia (UBC) has a PC-based real-time simulator (OVNI [28],[60]) that uses a two-level partitioning approach. The first level of partitioning uses Bergeron's traveling wave model to form subsystems that can be solved on different PC-cluster computers. The second level of partitioning is to use a diakoptics-based formulation (called MATE [61]), which tears resistive lines (inter-area links) to create subdivisions from the first-level subsystems.

In [28],[60] J. R. Marti and L. R. Linares used diakoptics to tear the resistance of lumped lines as illustrated by Fig. 2.3.5-Fig. 2.3.6. In Fig. 2.3.5 the areas joined by the line resistance were decoupled by replacing the line resistance by current sources of unknown value. After replacing the resistance with current sources, from the principle of current source transportation [46], the current sources were torn as current sinks (left) and current sources (right) as shown in Fig. 2.3.6.

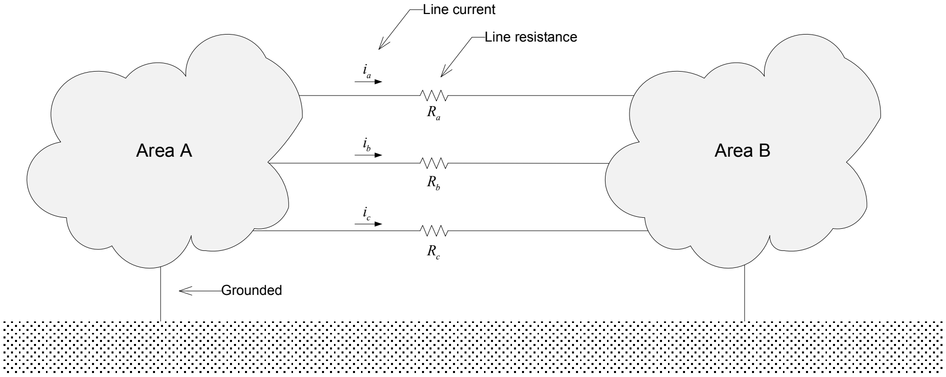


Fig. 2.3.5. Two areas joined by an inter-area link (lumped resistances)

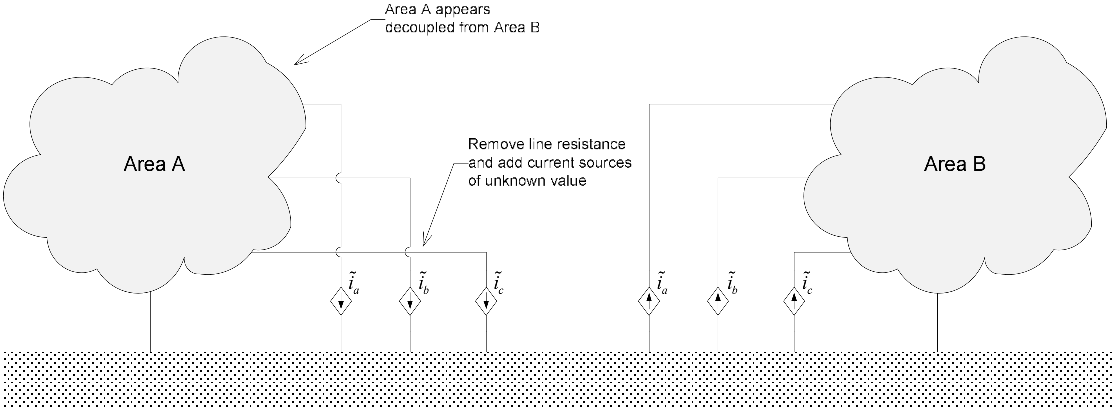


Fig. 2.3.6. Two areas decoupled by current source transportation [46]

To solve the partitioned system shown in Fig. 2.3.6, the current source constraint equations are included in the system formulation (MATE). The network matrix for the system in Fig. 2.3.6 is given in (2.13), where $\mathbf{G}_{nodalA}$ is the nodal conductance matrix of Area A, $\mathbf{0}$ is a zero matrix, and $\mathbf{i}_{nodalA}$ is the current injection vector for Area A. The unknown current source values are included in the lower part of node voltage vector and are part of the system's solution (i.e., solved simultaneously with the node voltages). Equation (2.13) has the form of (2.11), which is a diakoptical formulation.

$$
\begin{array}{r|ccc|ccc|ccc|c|c|c|}
\text{row } a_1 & & & & & & & 1 & & & v_{a1} & & \\
\text{row } b_1 & & \mathbf{G}_{nodalA} & & & \mathbf{0} & & & 1 & & v_{b1} & & \mathbf{i}_{nodalA} \\
\text{row } c_1 & & & & & & & & & 1 & v_{c1} & & \\
\hline
\text{row } a_2 & & & & & & & -1 & & & v_{a2} & = & \\
\text{row } b_2 & & \mathbf{0} & & & \mathbf{G}_{nodalA} & & & -1 & & v_{b2} & & \mathbf{i}_{nodalB} \\
\text{row } c_2 & & & & & & & & & -1 & v_{c2} & & \\
\hline
 & 1 & & & -1 & & & -R_a & & & \tilde{i}_a & & \\
 & & 1 & & & -1 & & & -R_b & & \tilde{i}_b & & \\
 & & & 1 & & & -1 & & & -R_c & \tilde{i}_c & & \\
\hline
 & \text{col. } a_1 & \text{col. } b_1 & \text{col. } c_1 & \text{col. } a_2 & \text{col. } b_2 & \text{col. } c_2 & & & & & &
\end{array}
\tag{2.13}
$$

K. W. Chan *et al.* [62] implemented a PC-based real-time simulator connected in a 4D-hypercube using diakoptics as the inter-processor partitioning scheme. The solution for an 811-busbar power system was measured in terms of speed gain and efficiency. The speed gain is the ratio between unpartitioned and partitioned simulation times. The efficiency is the ratio between speed gain and the number of processors used. When using two processors, the speed gain and efficiency were 1.76 and 88.2%, respectively. When using 16 processors, the speed gain and efficiency were 4.77 and 29.79%. The speed gains reported are sub-linear and show that inter-processor communication severely influences the overall performance of the parallel simulations. Another influential aspect is the computational imbalance among subsystems. The computation imbalance manifests itself as efficiency and is dominated by the processor finishing last at each time step (i.e., ideally, all processors finish their solutions at the same time). The major bottleneck of diakoptics is the communication overhead in unifying the subsystem solutions to obtain the overall solution.

S. Jiwu *et al*. [63] implemented an eight-computer cluster using diakoptics as the inter-processor partitioning scheme for transient stability simulations. The authors improved the coarse-grained algorithm used by K. W. Chan in [62] by proposing a multilevel partitioning scheme and a hierarchical form of the bordered-block diagonal form power network algorithm. Cluster optimizations are also used to reduce the bottleneck of the partitioning scheme. The three case studies presented by the authors reported sub-linear and super-linear speed gains for transient stability studies. Speed-gains of near ten were attained for eight processors, and efficiencies of 180% were attained for four processors, which improved the results in [62]. The work in [63] addresses transient stability simulations, which is not the main endeavor of this work. However, it should be noticed that super-linear gains and good efficiencies are possible using diakoptics.

A. Kalantari [64] and S. Esmaeili [65] used a diakoptical formulation for inter-area steady-state fault studies. Ideal circuit breakers at the onset of subsystems were used to create boundaries of disconnection as shown in Fig. 2.3.7; if circuit breakers did not exist at the desired locations, they were inserted in place. The inter-area constraint equations include the circuit breakers' status (F=0 when open, and F=1 when closed). The diakoptical formulation used by A. Kalantari *et al.* is given in (2.14).

$$\left[\begin{array}{cccc|c} \mathbf{Y}_1 & \cdot & \cdot & \cdot & \mathbf{C}_1 \\ \cdot & \mathbf{Y}_2 & \cdot & \cdot & \mathbf{C}_2 \\ \cdot & \cdot & \ddots & \cdot & \vdots \\ \cdot & \cdot & \cdot & \mathbf{Y}_s & \mathbf{C}_s \\ \hline F\mathbf{C}_1^{\mathrm{T}} & F\mathbf{C}_2^{\mathrm{T}} & \cdots & F\mathbf{C}_p^{\mathrm{T}} & (F-1)\mathbf{I} \end{array}\right] \left[\begin{array}{c} \mathbf{V}_1 \\ \mathbf{V}_2 \\ \vdots \\ \mathbf{V}_p \\ \hline \mathbf{I}_{ex} \end{array}\right] = \left[\begin{array}{c} \mathbf{I}_1 \\ \mathbf{I}_2 \\ \vdots \\ \mathbf{I}_s \\ \hline \mathbf{0} \end{array}\right] \tag{2.14}$$

where:

$\mathbf{I}_i$ = current injection vector of subsystem i

$\mathbf{V}_i$ = vector of unknown voltages of subsystem i

$\mathbf{Y}_i$ = admittance matrix of subsystem i

$\mathbf{C}_i$ = connection matrix relating subsystem i's internal node currents to its boundary currents

$\mathbf{I}_{ex}$ = boundary current injections

F = variable parameter that determines that status of boundary circuit breakers

s = number of network partitions.

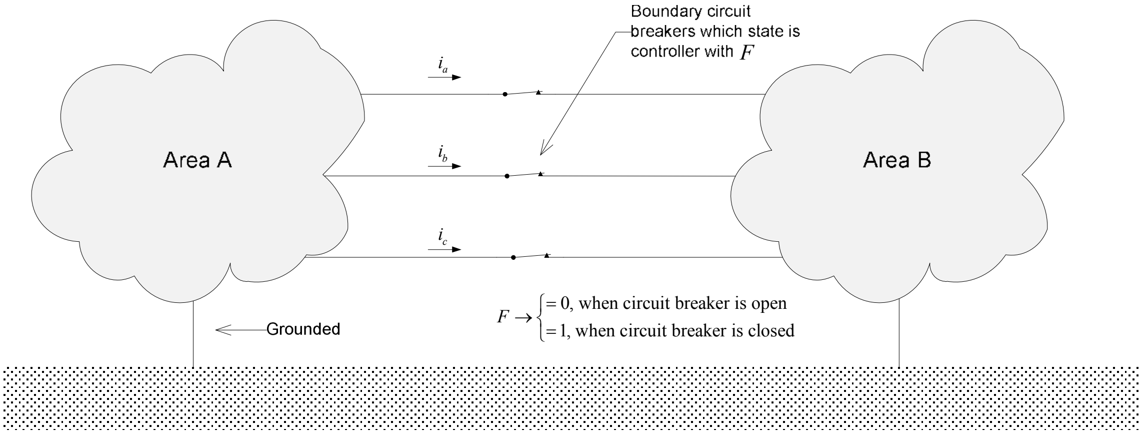

Boundary circuit breakers which state is controller with F
i_a
i_b
i_c
Area A
Area B
Grounded
$F \rightarrow \begin{cases} = 0, \text{ when circuit breaker is open} \\ = 1, \text{ when circuit breaker is closed} \end{cases}$

Fig. 2.3.7. Two areas joined by ideal circuit breakers

The network equations in [64] were parallelized by first solving the network with the circuit breakers open, and then with the breakers closed. The fault study solution approach in [64] is computationally efficient because obtaining the new fault pre-voltages does not require re-factoring the entire network matrix, only portions of each subsystem's bus impedance matrices (also called the Woodbury's method of inverting modified matrices [66-68]). The work in [64] was presented for steady-state results; the work in [65] for transient stability studies, grounded networks, use nodal analysis, and their breaker models did not exhibit arcing characteristics.

The main disadvantages of diakoptics are that branches must exist at the boundaries of disconnection for constraint equations to be written and that the computation of the patch term becomes computationally expensive as the number of partitions increases; more so in distributed computers having physical communication network delays. The former disadvantage poses a limitation on the number of places where a network can be torn, and limits the maximum number of partitions possible.

The latter disadvantage is due to the sequential work required to compute the boundary conditions at each disconnection point. The larger the number of partitions, the larger the sequential work involved in said boundary condition computation. While the boundary conditions are computed, the solution to the subsystems is halted until the boundary conditions are known.

2.4 DIFFERENTIAL-ALGEBRAIC FORMULATION OF A NOTIONAL SHIPBOARD POWER SYSTEM

To assess the complexity and order of AC-Radial SPS time domain simulations, a notional SPS was formulated mathematically using differential-algebraic equations (DAEs). The differential equation set contains the differential equations of all power apparatus and controllers. The algebraic equation set contains the voltage and current constraints at the junctions (e.g., single-phase and three-phase nodes) where two or more power apparatus interconnect. The list of the power apparatus used for the notional AC-Radial SPS formulation is presented after introducing the component models in Table II.4. The three-letter acronyms will be used frequently throughout this manuscript.

To formulate the DAEs, a multi-terminal component (MTC) theory [69] approach was adopted. In the following subsection MTC theory is introduced before presenting the DAE equation formulation.

2.4.1 Multi-Terminal Component Theory

Multi-terminal component theory is an abstraction that treats power apparatus as being enclosed by black-boxes called MTCs. By creating MTCs, each power apparatus can be mathematically described as a stand-alone component. Each MTC is mathematically described using differential and/or algebraic equations to describe the internal behavior of the MTC. After mathematically describing all MTCs, the MTCs are interconnected by writing voltage and current algebraic equations at all MTC terminals. After all MTCs are described and interconnected, a DAE formulation is obtained.

An illustration of an arbitrary MTC is shown in Fig. 2.4.1. The MTC in Fig. 2.4.1 has three-phase terminals on its input and output sides. Some MTCs may have only an input side (e.g., a motor), or may have mixed single-phase and three-phase terminals (e.g., a transformer).

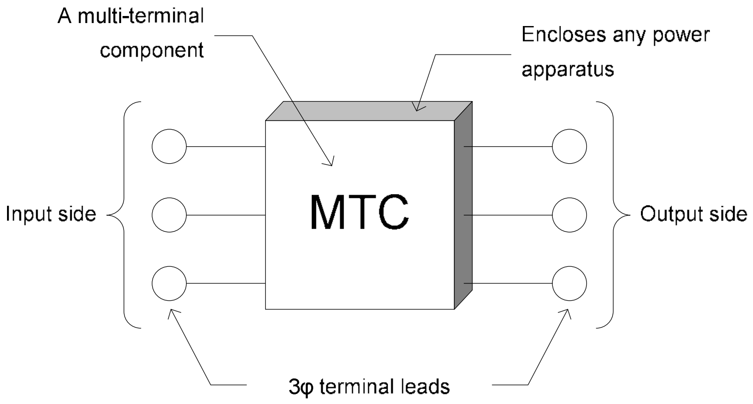


Fig. 2.4.1. A power apparatus enclosed inside a multi-terminal component (MTC)

An illustration showing four MTCs is given in Fig. 2.4.2. In Fig. 2.4.2, a synchronous generator (GEN1) is connected to an over-current relay monitoring a circuit breaker (BRK1) at three-phase node 1. The circuit breaker is connected to two cables (CBL1 and CBL2) at three-phase node 2. All MTCs were interconnected by writing voltage and current equations as described in Fig. 2.4.2, which rendered the entire notional SPS DAE formulation. An example of a bus connection is given at the end of section 2.4.3.

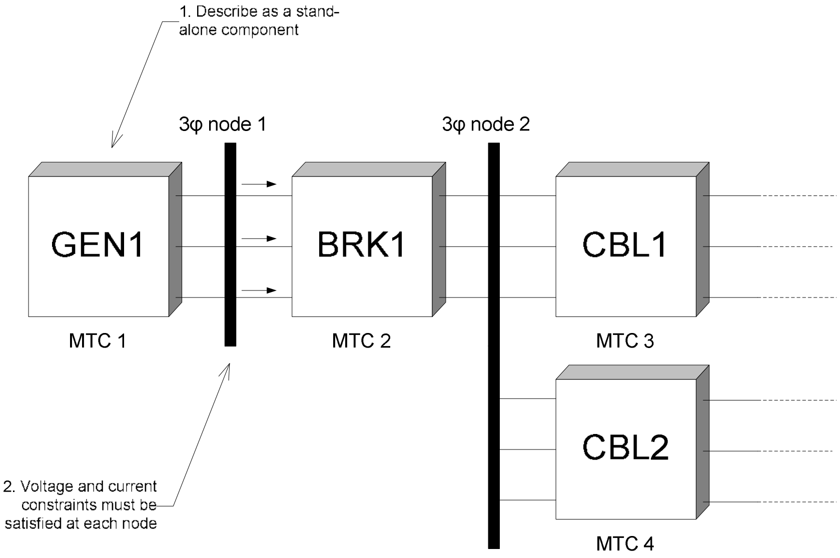

1. Describe as a stand-alone component
3φ node 1
3φ node 2
GEN1
BRK1
CBL1
CBL2
MTC 1
MTC 2
MTC 3
MTC 4
2. Voltage and current constraints must be satisfied at each node

Fig. 2.4.2. Radial connection of four MTCs

2.4.2 Component Models

The power apparatus models of the notional SPS are presented in more detail in this section. Each power apparatus is described using differential equations, and with differential-algebraic equations if they enclose subcomponents (e.g., generators and induction motors enclose subcomponents). None of the components presented next have a ground connection because SPSs are modeled as purely ungrounded in this work.

2.4.2.1 Synchronous Generator

Three synchronous generators are modeled in the notional SPS used in this work. The generators have delta-connected stator windings, are rated at 450V, 2.5MW, 3.125kVA, 900RPM (60Hz), 8-pole machine, and use the parameters presented in [70].

Each generator comprises four subcomponents: a rotor shaft (ROT), a prime-mover and governor (PMG), a voltage regulator and exciter (VRE), and six windings (WND). The generator's rotor dynamics are based on the swing equation (eq. 7.82 in [71]). The PMG model is based on the model presented in [70] and the VRE model based on the IEEE Type II excitation system [72-73]. The stator windings are modeled as three delta-connected windings and the rotor windings as a field, d-axis damper, and q-axis damper windings; the stator and rotor windings are magnetically coupled with time-varying inductances.

A representation of the generator model and its subcomponents is shown in Fig. 2.4.3. The generator subcomponents are ROT, PMG, VRE, and WND. To interconnect the generator's subcomponents, the state-variable relationships (indicated with arrows) in Fig. 2.4.3 are used. Each of the generator's subcomponent equations are introduced next.

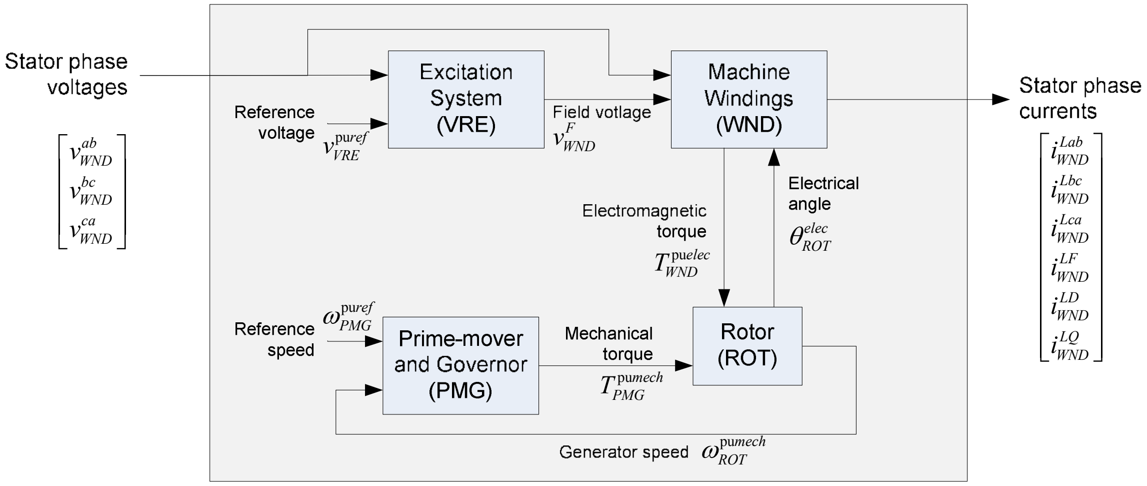

Stator phase voltages
$\begin{bmatrix} v_{WND}^{ab} \\ v_{WND}^{bc} \\ v_{WND}^{ca} \end{bmatrix}$
Excitation System (VRE)
Reference voltage v_{VRE}^{puref}
Field votlage v_{WND}^{F}
Machine Windings (WND)
Stator phase currents
$\begin{bmatrix} i_{WND}^{Lab} \\ i_{WND}^{Lbc} \\ i_{WND}^{Lca} \\ i_{WND}^{LF} \\ i_{WND}^{LD} \\ i_{WND}^{LQ} \end{bmatrix}$
Electromagnetic torque $T_{WND}^{\text{pu}elec}$
Electrical angle θ_{ROT}^{elec}
Reference speed $\omega_{PMG}^{\text{puref}}$
Prime-mover and Governor (PMG)
Mechanical torque $T_{PMG}^{\text{pu}mech}$
Rotor (ROT)
Generator speed $\omega_{ROT}^{\text{pu}mech}$

Fig. 2.4.3. Electrical and mechanical subcomponents of a synchronous generator

2.4.2.1.1 Machine Windings

The equations of the six generator winding are given in (2.15), where the state-variables are the winding currents and the inputs are the winding voltages. Derivation of (2.15) is based on the synchronous generator modeling presented in [74-76]. In (2.15), $\boldsymbol{\lambda}_{WND}$ is the vector of winding flux-linkages, $\mathbf{L}_{WND}$ is a coefficient matrix with time-varying self- and mutual-inductances, $\mathbf{R}_{WND}$ is a diagonal matrix with the winding resistances, θ_{GEN}^{elec} is the rotor's electrical angle in radians with respect to phase ab 's stationary magnetic axis, $\mathbf{x}_{WND}$ is the state-variable vector of winding currents, and $\mathbf{u}_{WND}$ is the input vector of impressed voltages on each winding.

$$\dot{\boldsymbol{\lambda}}_{WND} = -\mathbf{R}_{WND}\mathbf{x}_{WND} - \mathbf{u}_{WND} \tag{2.15}$$

$$\mathbf{L}_{WND} = \left[\begin{array}{ccc|ccc} L_{WND}^{aa} & L_{WND}^{ab} & L_{WND}^{ac} & L_{WND}^{abF} & L_{WND}^{abD} & L_{WND}^{abQ} \\ L_{WND}^{ab} & L_{WND}^{bb} & L_{WND}^{bc} & L_{WND}^{bcF} & L_{WND}^{bcD} & L_{WND}^{bcQ} \\ L_{WND}^{ac} & L_{WND}^{bc} & L_{WND}^{cc} & L_{WND}^{caF} & L_{WND}^{caD} & L_{WND}^{caQ} \\ \hline L_{WND}^{abF} & L_{WND}^{bcF} & L_{WND}^{caF} & L_{WND}^{F} & M_{WND}^{R} & \cdot \\ L_{WND}^{abD} & L_{WND}^{bcD} & L_{WND}^{caD} & M_{WND}^{R} & L_{WND}^{D} & \cdot \\ L_{WND}^{abQ} & L_{WND}^{bcQ} & L_{WND}^{caQ} & \cdot & \cdot & L_{WND}^{Q} \end{array}\right]_{6\times 6} \quad \mathbf{x}_{WND} = \left[\begin{array}{c} i_{WND}^{Lab} \\ i_{WND}^{Lbc} \\ i_{WND}^{Lca} \\ \hline i_{WND}^{LF} \\ i_{WND}^{LD} \\ i_{WND}^{LQ} \end{array}\right]_{6\times 1} \quad \mathbf{u}_{WND} = \left[\begin{array}{c} v_{WND}^{ab} \\ v_{WND}^{bc} \\ v_{WND}^{ca} \\ \hline v_{WND}^{F} \\ v_{WND}^{D} \\ v_{WND}^{Q} \end{array}\right]_{6\times 1}$$

$$\mathbf{R}_{WND} = \operatorname{diag}\left(R_{WND}^{s}, R_{WND}^{s}, R_{WND}^{s}, R_{WND}^{F}, R_{WND}^{D}, R_{WND}^{Q}\right)_{6\times 6} \qquad \boldsymbol{\lambda}_{WND} = \mathbf{L}_{WND}\mathbf{x}_{WND}$$

Stator
Self Inductances

$$\rightarrow \begin{bmatrix} L_{GEN}^{aa} \\ L_{GEN}^{bb} \\ L_{GEN}^{cc} \end{bmatrix} = \begin{bmatrix} L_{GEN}^{s} + L_{GEN}^{m}\cos\left(2\theta_{ROT}^{elec}\right) \\ L_{GEN}^{s} + L_{GEN}^{m}\cos\left(2\left(\theta_{ROT}^{elec} - \dfrac{2\pi}{3}\right)\right) \\ L_{GEN}^{s} + L_{GEN}^{m}\cos\left(2\left(\theta_{ROT}^{elec} + \dfrac{2\pi}{3}\right)\right) \end{bmatrix}$$

Stator-Stator
Mutual Inductances

$$\rightarrow \begin{bmatrix} L_{GEN}^{ab} \\ L_{GEN}^{bc} \\ L_{GEN}^{ca} \end{bmatrix} = \begin{bmatrix} -M_{GEN}^{s} - L_{GEN}^{m}\cos\left(2\left(\theta_{ROT}^{elec} + \dfrac{\pi}{6}\right)\right) \\ -M_{GEN}^{s} - L_{GEN}^{m}\cos\left(2\left(\theta_{ROT}^{elec} - \dfrac{\pi}{2}\right)\right) \\ -M_{GEN}^{s} - L_{GEN}^{m}\cos\left(2\left(\theta_{ROT}^{elec} + \dfrac{5\pi}{6}\right)\right) \end{bmatrix}$$

Stator-to-Field
Mutual Inductances

$$\rightarrow \begin{bmatrix} L_{GEN}^{abF} \\ L_{GEN}^{abD} \\ L_{GEN}^{abQ} \end{bmatrix} = \begin{bmatrix} M_{GEN}^{F}\cos\left(\theta_{ROT}^{elec}\right) \\ M_{GEN}^{D}\cos\left(\theta_{ROT}^{elec} - \dfrac{2\pi}{3}\right) \\ M_{GEN}^{Q}\cos\left(\theta_{ROT}^{elec} + \dfrac{2\pi}{3}\right) \end{bmatrix}$$

$$\text{Stator-to-D-damper winding Mutual inductances} \rightarrow \begin{bmatrix} L_{GEN}^{abD} \\ L_{GEN}^{bcD} \\ L_{GEN}^{caD} \end{bmatrix} = \begin{bmatrix} M_{GEN}^{D}\cos\left(\theta_{ROT}^{elec}\right) \\ M_{GEN}^{D}\cos\left(\theta_{ROT}^{elec}-\frac{2\pi}{3}\right) \\ M_{GEN}^{D}\cos\left(\theta_{ROT}^{elec}+\frac{2\pi}{3}\right) \end{bmatrix}$$

$$\text{Stator-to-Q-damper winding Mutual inductances} \rightarrow \begin{bmatrix} L_{GEN}^{abQ} \\ L_{GEN}^{bcQ} \\ L_{GEN}^{caQ} \end{bmatrix} = \begin{bmatrix} M_{GEN}^{Q}\sin\left(\theta_{ROT}^{elec}\right) \\ M_{GEN}^{Q}\sin\left(\theta_{ROT}^{elec}-\frac{2\pi}{3}\right) \\ M_{GEN}^{Q}\sin\left(\theta_{ROT}^{elec}+\frac{2\pi}{3}\right) \end{bmatrix}$$

The relationship between the rotor's mechanical angle and the stator windings' electrical angle (i.e., the stator frequency is different than the rotor frequency) is given in (2.16), where θ_{ROT}^{mech} is the rotor's mechanical angle with respect to the machine's top-dead center, and $p_{GEN} = 8$ is the total number of magnetic poles on the rotor.

$$\theta_{ROT}^{elec} = \frac{p_{GEN}}{2}\theta_{ROT}^{mech} \tag{2.16}$$

2.4.2.1.2 Prime-mover and Governor

The state-variable equations for the PMG are given in (2.17) and are based on [70], where T_{FT} and T_{FV} are prime-mover time constants, W_{F10s} and C_{2GT} are exogenous inputs, T_C and K_C are the governor's time constant and gain, respectively; $\omega_{PMG}^{\text{pu}ref}$ is the prime-mover's reference speed in per-unit, $\omega_{ROT}^{\text{pu}mech}$ is the rotor's instantaneous mechanical speed in per-unit. The aforementioned variables are labeled in Fig. 2.4.3.

$$\begin{bmatrix} \overset{\bullet}{x}^{1}_{PMG} \\ \overset{\bullet}{x}^{2}_{PMG} \\ \overset{\bullet}{x}^{3}_{PMG} \end{bmatrix} = \begin{bmatrix} \frac{-1}{T_{FT}} & \cdot & \frac{-1}{T_{FT}} \\ \cdot & \cdot & \cdot \\ \cdot & \frac{-1}{T_{FV}} & \frac{-1}{T_{FV}} \end{bmatrix} \begin{bmatrix} x^{1}_{PMG} \\ x^{2}_{PMG} \\ x^{3}_{PMG} \end{bmatrix} + \begin{bmatrix} \cdot & \cdot & \cdot & \cdot \\ \frac{K_C}{T_C} & \left(\frac{-K_C}{T_C} - K_C \frac{d}{dt} \omega^{\text{pu}mech}_{ROT} \right) & \cdot & \cdot \\ \cdot & \cdot & \frac{-1}{T_{FV}} & \cdot \end{bmatrix} \begin{bmatrix} \omega^{\text{pu}ref}_{PMG} \\ \omega^{\text{pu}mech}_{ROT} \\ W_{F10s} \\ C_{2GT} \end{bmatrix}$$

(2.17)

2.4.2.1.3 Rotor

The rotor's swing equations is given in (2.18), where J_{ROT} is the rotor's moment of inertia in kg-m^{2,}, $\omega^{\text{base}mech}_{GEN} = 900 \times \frac{2\pi}{60}\,\text{rad/s}$ is the generator's base mechanical speed, $T^{\text{base}mech}_{GEN}$ is the generator's base torque in N-m, $\omega^{\text{pu}mech}_{ROT}$ is the rotor's instantaneous mechanical speed in per-unit, $T^{\text{pu}mech}_{PMG}$ is the PMG's applied mechanical torque in per-unit, and $T^{\text{pu}elec}_{WND}$ is the windings' electromagnetic counter-torque in per-unit.

$$\begin{bmatrix} \overset{\bullet}{\theta}^{mech}_{ROT} \\ \overset{\bullet}{\omega}^{\text{pu}mech}_{ROT} \end{bmatrix} = \begin{bmatrix} \cdot & \cdot \\ \cdot & \frac{-D_{ROT}}{-J_{ROT}} \end{bmatrix} \begin{bmatrix} \theta^{mech}_{ROT} \\ \omega^{\text{pu}mech}_{ROT} \end{bmatrix} + \begin{bmatrix} \cdot \\ \frac{1}{J_{ROT}} \end{bmatrix} \left(T^{\text{pu}mech}_{PMG} - T^{\text{pu}elec}_{WND} \right) \qquad (2.18)$$

2.4.2.1.4 Voltage Regulator and Exciter

The VRE's state-variable equations are given in (2.19) and the non-linear relations in (2.20), where E^{FD}_{VRE} is the exciter's throughput voltage, $\left\{V^{1}_{VRE}, V^{2}_{VRE}, V^{3}_{VRE}\right\}$ are the regulator state- variables, $v^{\text{pu}ref}_{VRE}$ is the reference voltage in per unit, and $v^{\text{pu}term}_{VRE}$ is the stator's terminal voltage in per-unit. The VRE's non-linearity is modeled by $f_4(t)$, which models the regulator's limiter function, and $f_1(t)$, which models the exciter's saturation function. The parameters $\left\{K_E, K_A, K_F\right\}$ and $\left\{T_{F1}, T_{F2}, T_A, T_E\right\}$ are VRE gains and time constants, respectively.

$$\begin{bmatrix} \dot{E}_{VRE}^{FD} \\ \dot{V}_{VRE}^{1} \\ \dot{V}_{VRE}^{2} \\ \dot{V}_{VRE}^{3} \end{bmatrix} = \begin{bmatrix} -\dfrac{K_E}{T_E} & \cdot & \cdot & \cdot \\ \cdot & -\dfrac{1}{T_{F1}} & \dfrac{1}{T_{F1}} & \cdot \\ \cdot & \cdot & -\dfrac{1}{T_{F2}} & \cdot \\ \cdot & -\dfrac{K_A}{T_A} & \cdot & -\dfrac{1}{T_A} \end{bmatrix} \begin{bmatrix} E_{VRE}^{FD} \\ V_{VRE}^{1} \\ V_{VRE}^{2} \\ V_{VRE}^{3} \end{bmatrix} + \begin{bmatrix} \dfrac{1}{T_E}\left(f_4 - f_1\right) \\ \cdot \\ \dfrac{K_F}{T_{F2}}\dfrac{d}{dt}f_4 \\ \cdot \end{bmatrix} + \begin{bmatrix} \cdot & \cdot \\ \cdot & \cdot \\ \cdot & \cdot \\ \dfrac{K_A}{T_A} & \dfrac{-K_A}{T_A} \end{bmatrix} \begin{bmatrix} v_{VRE}^{\mathrm{pu}ref} \\ v_{VRE}^{\mathrm{pu}term} \end{bmatrix} \tag{2.19}$$

$$\text{Non-linearities} \rightarrow \begin{cases} f_4 = \dfrac{18}{\pi}\arctan\left(V_{VRE}^{3}\right) \\ f_1 = A \cdot e^{B \cdot E_{VRE}^{FD}} \end{cases} \tag{2.20}$$

2.4.2.2 Induction Motor

The motor loads on the notional AC-Radial SPS are modeled as induction motors including the motor drives. The motor ratings and parameters are listed in Table II.2 and Table II.3, respectively. As seen from Table II.2, the induction motors are loaded with a constant mechanical load torque and operated below their rated values. Similar to GENs, MOTs are comprised of several subcomponents. The MOT's subcomponents are an uncontrolled three-phase rectifier with DC-link bus capacitor, a sinusoidal pulse-width modulated voltage-source inverter [77], the motor windings, and the rotor shaft.

TABLE II.2. INDUCTION MOTOR TYPES, RATINGS, AND OPERATING POINTS

		Rated Values						Operating Values			
Type of Induction Motor	Number of	Rated Horsepower (HP)	Rated Power Factor	Rated Power (W)	Rated Torque (N-m)	Slip at Rated Torque	Rated Speed (RPM)	Loaded Power (W)	Loaded Torque (N-m)	Slip when Loaded	Loaded Speed (RPM)
AC Compressor	1	258.2	0.90	192,617	2099.3	51.6%	3,600	156,872	437.1	4.8%	3,427
Anchor Windlass	4	53.22	0.87	39,702	535.4	62.2%	3,600	18,856	51.6	3.0%	3,492
Fire Pump	6	154.5	0.83	115,257	1357.3	29.0%	3,600	96,171	262.5	2.8%	3,499
HP Compressor	2	5.63	0.82	4,200	52.3	40.8%	3,600	3,504	9.6	3.3%	3,481
Steering Gear	4	105.2	0.86	78,479	550.1	31.2%	3,600	38,333	104.8	3.0%	3,492
Water Pump	2	63.81	0.86	47,602	897.4	27.1%	3,600	71,900	196.6	3.0%	3,492
Total no. motors	19										

TABLE II.3. INDUCTION MOTOR PARAMETERS

	Electrical Parameters						Mechanical Parameters		
Type of Induction Motor	Number of Poles (total)	Stator Resistance (Ω)	Stator Leakage Inductance (H)	Magnetizing Inductance (H)	Rotor Resistance (Ω)	Rotor Leakage Inductance (H)	Rotor Damping Coefficient (N-m-s)	Rotor Moment of Inertia (kg-m^2)	Rotor Time Constant (secs)
AC Compressor	2	53.9E-3	431.7E-6	20.6E-3	170.3E-3	431.7E-6	111.3E-3	521.2E-6	4.7E-3
Anchor Windlass	2	300.0E-9	2.0E-3	92.4E-3	935.4E-3	2.0E-3	28.4E-3	143.5E-6	5.1E-3
Fire Pump	2	7.3E-3	777.6E-6	23.1E-3	169.9E-3	777.6E-6	72.0E-3	385.9E-6	5.4E-3
HP Compressor	2	2.3E+0	17.1E-3	526.6E-3	5.3E+0	17.1E-3	2.8E-3	14.9E-6	5.4E-3
Steering Gear	2	300.0E-9	1.9E-3	70.1E-3	456.9E-3	1.9E-3	29.2E-3	149.2E-6	5.1E-3
Water Pump	2	300.0E-9	1.2E-3	42.5E-3	242.9E-3	1.2E-3	47.6E-3	648.7E-6	13.6E-3

An illustration of the MOT model including subcomponents is shown in Fig. 2.4.4. The rectifier is modeled as a six-pulse line-commutated uncontrolled rectifier. The inverter is modeled as a six-pulse pulse-width modulated voltage-source inverter, where the speed controller is modeled as a lag compensator. The mechanical load is modeled as a constant mechanical torque. The rotor dynamics are modeled with the swing equation. Details of the MOT's subcomponent are presented next.

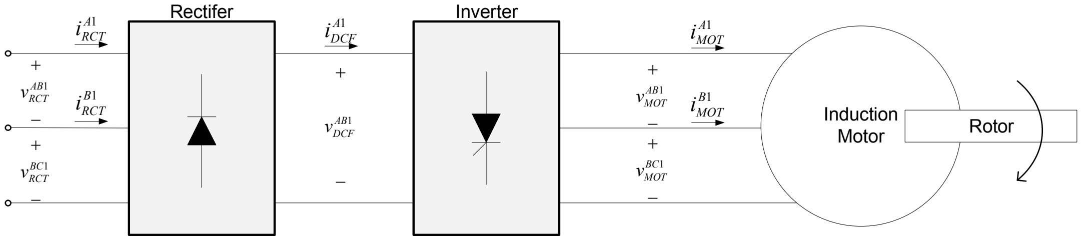


Fig. 2.4.4. Induction motor and drive

2.4.2.2.1 Rectifier

The rectifier and DC-link bus equations are given in (2.21). The rectifier equations are updated every time a diode commutates according to:

$$\begin{array}{c}\text{Diode}\\ \text{commutation}\end{array} \rightarrow \begin{cases} v_D > 1\text{V, diode turns on;} & R_D = 1\text{m}\Omega \\ v_D < 1\text{V, diode turns off;} & R_D = 1\text{M}\Omega \\ v_D = 1\text{V, no action; } R_D \text{ does not change} & \end{cases}$$

The three-phase rectifier model is shown in Fig. 2.4.5.

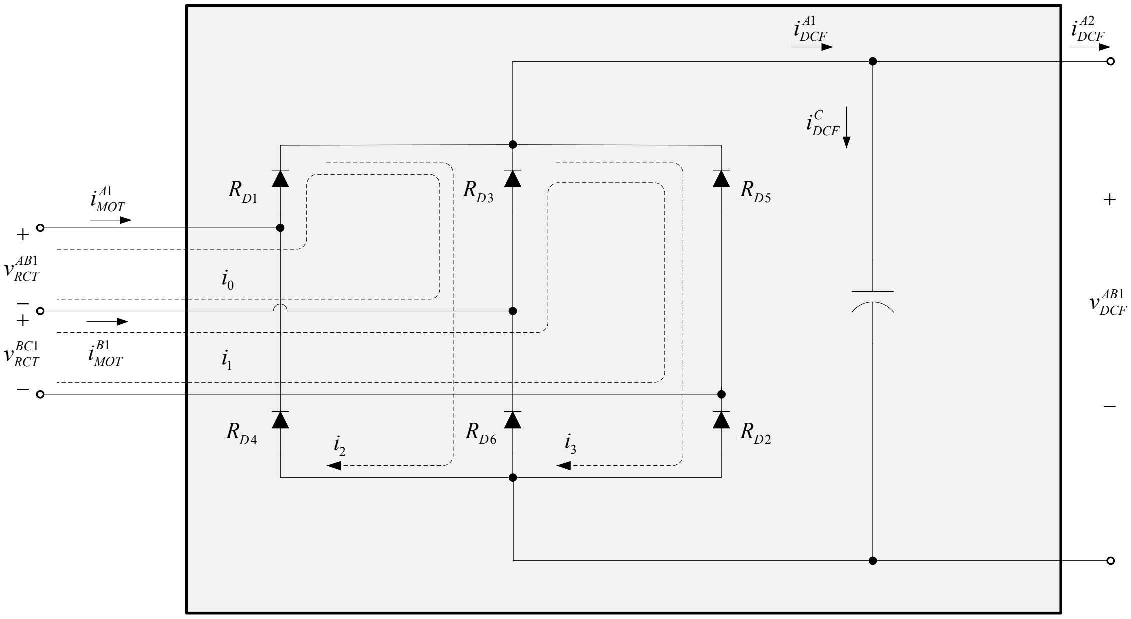


Fig. 2.4.5. Motor drive's line-commutated rectifier

$$\left\{\begin{array}{l}
C_{DCF}\dfrac{d}{dt}v_{DCF}^{C}=i_{DCF}^{C}\qquad i_{DCF}^{A1}=i_{D1}+i_{D2}+i_{D3}\\[2em]
\begin{bmatrix}
R_{D1}+R_{D3} & -R_{D3} & R_{D1}+R_{D3} & -R_{D3} & \cdot\\
-R_{D3} & R_{D3}+R_{D5} & -R_{D3} & R_{D3}+R_{D5} & -R_{D5}\\
R_{D1}+R_{D3} & -R_{D3} & \begin{pmatrix}R_{D1}+R_{D3}^{k+1}\\+R_4+R_6\end{pmatrix} & -R_{D3}-R_{D6} & \cdot\\
-R_{D3} & R_{D3}+R_{D5} & -R_{D3}-R_{D6} & \begin{pmatrix}R_{D2}+R_{D3}\\+R_{D5}+R_{D6}\end{pmatrix} & -R_{D2}-R_{D5}\\
\cdot & -R_{D5} & \cdot & -R_{D2}-R_{D5} & R_{D2}+R_{D5}
\end{bmatrix}
\begin{bmatrix}i_0\\i_1\\i_2\\\underline{i_3}\\i_4\end{bmatrix}=\begin{bmatrix}\cdot\\\cdot\\\cdot\\\cdot\\-\\\cdot\end{bmatrix}
\end{array}\right.$$

(2.21)

2.4.2.2.2 Inverter

The pulse-width modulated (PWM) voltage-source inverter is shown in Fig. 2.4.6, where the transistors are modeled as ideal switches ($1\text{m}\Omega$ when closed, and $1\text{M}\Omega$ when open). The algebraic (mesh) equations of the inverter and given in (2.22) , and are time-varying according to:

$$R_{Qi} \rightarrow \begin{cases} = 1\text{m}\Omega, \text{ when the } i^{\text{th}} \text{ transistor conducts} \\ = 1\text{M}\Omega, \text{ when the } i^{\text{th}} \text{ transistor blocks} \end{cases}$$

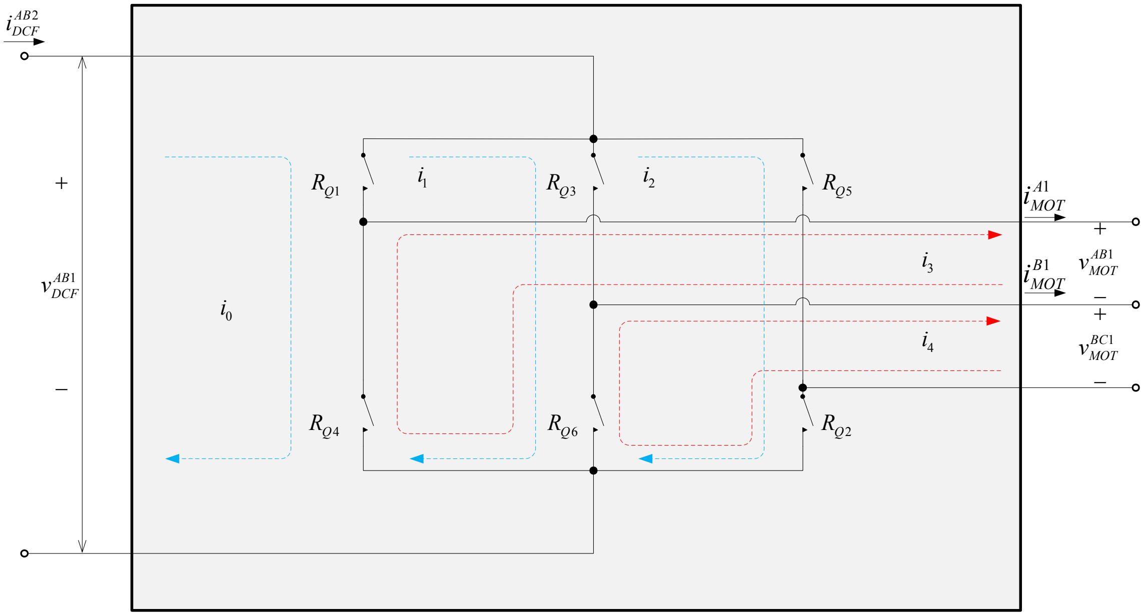


Fig. 2.4.6. Motor drive’s voltage-source inverter

$$\left[\begin{array}{ccc|cc} R_{Q1}+R_{Q4} & -R_{Q1}-R_{Q4} & \cdot & -R_{Q4} & \cdot \\ -R_{Q1}-R_{Q4} & \begin{pmatrix} R_{Q1}+R_{Q3} \\ +R_{Q4}+R_{Q6} \end{pmatrix} & -R_{Q3}-R_{Q6} & R_{Q4}+R_{Q6} & -R_{Q6} \\ \cdot & -R_{Q3}-R_{Q6} & \begin{pmatrix} R_{Q2}+R_{Q3} \\ +R_{Q5}+R_{Q6} \end{pmatrix} & -R_{Q6} & R_{Q2}+R_{Q6} \\ \hline -R_{Q4} & R_{Q4}+R_{Q6} & -R_{Q6} & R_{Q4}+R_{Q6} & -R_{Q6} \\ \cdot & -R_{Q6} & R_{Q2}+R_{Q6} & -R_{Q6} & R_{Q2}+R_{Q6} \end{array}\right] \begin{bmatrix} i_0 \\ i_1 \\ i_2 \\ \hline i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \end{bmatrix}$$

(2.22).

The inverter's firing signals were generated by comparing three reference signals (one for each phase *ab*, *bc*, and *ca*) against a common carrier signal. The signal-generating functions for the reference and carrier signals are based [77] on and are given in (2.23), where f_{refa} is the reference signal for phase *ab*, $f_r = 60\text{Hz}$ is the reference signals' frequency, and $f_c = 2000\text{Hz}$ is the carrier signal's frequency.

$$\begin{array}{ll} \begin{array}{c}\text{Reference signals}\\ \left(\text{sinusoidal}\right)\end{array} & \rightarrow \begin{cases} f_{refa}\left(t\right) = 1.1\sin\left(2\pi f_r t\right) \\ f_{refb}\left(t\right) = 1.1\sin\left(2\pi f_r t - 120°\right) \\ f_{refc}\left(t\right) = 1.1\sin\left(2\pi \cdot f_r t + 120°\right) \end{cases} \\ \begin{array}{c}\text{Carrier signal}\\ \left(\text{sawtooth}\right)\end{array} & \rightarrow \begin{cases} f_{carr}\left(t\right) = 0.9\dfrac{2}{\pi}\arcsin\left(2\pi f_c t + 90°\right) \end{cases} \end{array} \tag{2.23}$$

The following comparisons are made to determine whether R_{Qi} is in conducting or blocking mode.

$$\begin{array}{c}\text{Transistor}\\ \text{firing signals}\end{array} \begin{cases} \text{if}\left(f_{refa}\left(t\right) > f_{carr}\left(t\right)\right) & R_{Q1} = R_{on} \text{ and } R_{Q4} = R_{off} \\ \text{if}\left(f_{refb}\left(t\right) > f_{carr}\left(t\right)\right) & R_{Q3} = R_{on} \text{ and } R_{Q6} = R_{off} \\ \text{if}\left(f_{refc}\left(t\right) > f_{carr}\left(t\right)\right) & R_{Q5} = R_{on} \text{ and } R_{Q2} = R_{off} \end{cases}$$

2.4.2.2.3 Motor Windings

The induction motor windings are modeled using delta-connected approximate per-phase equivalent circuits [78-80] as shown in Fig. 2.4.7. In Fig. 2.4.7, L_{Mab} is the magnetizing inductance of phase *ab*, R_{srab} is the sum of phase *ab*'s stator and rotor winding resistances, and L_{srab} is the sum of phase *ab*'s stator and rotor leakage inductances. The resistance $R_{rab}\left(1-s\right)/s$ is a time-varying resistance that models the power transferred to the rotor by phase *ab*. The slip *s* is computed with (2.24), where $\omega_{elec} = 120\pi$ is the stator's electrical frequency in rad/s, ω_{MOT}^{mech} is the rotor's mechanical speed in rad/s, and p_{mot} is the total number of magnetic poles.

$$s = \frac{\omega_{elec} - \frac{p_{mot}}{2}\omega_{MOT}^{mech}}{\omega_{elec}} \tag{2.24}$$

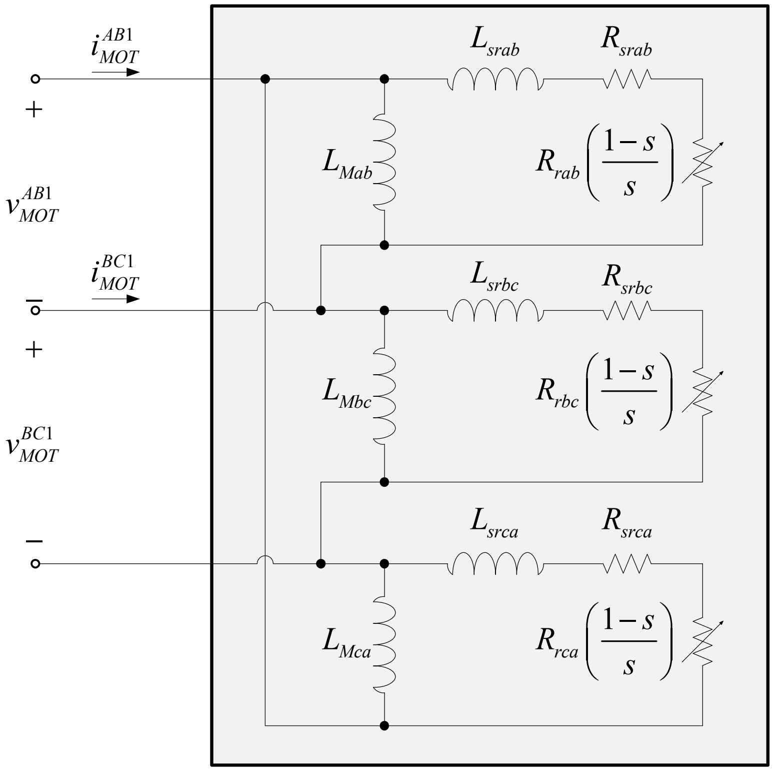


Fig. 2.4.7. Induction motor stator and rotor windings

2.4.2.2.4 Rotor

The induction motor's rotor dynamics are modeled with Newton's law of rotational motion, given in state-variable form in (2.25), where T_{MOT}^{elec} is the three-phase electromagnetic torque (in N-m) applied to the rotor, T_{MOT}^{mech} is the mechanical (constant) load torque in N-m, J_{MOT} is the rotor's moment of inertia in kg-m^2, ω_{MOT}^{mech} is the rotor's mechanical speed in rad/s, and D_{MOT} is the damping coefficient in N-m-s.

$$\begin{bmatrix} \overset{\bullet}{\theta}_{MOT}^{mech} \\ \overset{\bullet}{\omega}_{MOT}^{mech} \end{bmatrix} = \begin{bmatrix} \cdot & 1 \\ \cdot & \dfrac{-D_{MOT}}{-J_{MOT}} \end{bmatrix} \begin{bmatrix} \theta_{MOT}^{mech} \\ \omega_{MOT}^{mech} \end{bmatrix} + \begin{bmatrix} \cdot \\ \dfrac{1}{J_{MOT}} \end{bmatrix} \left(T_{MOT}^{elec} - T_{MOT}^{mech} \right) \tag{2.25}$$

The electromagnetic torque developed in each phase is found from (2.26), where R_{sr} is the sum of any phase's stator and rotor resistance in Ohms (e.g., $R_{srab} = R_{stator} + R_{rotor} / s$), L_{sr}^2 is the sum of any phase's stator and rotor leakage inductances in Henries, and R_{rotor} / s is the representative rotor resistance. Adding the torques developed by each phase results in T_{MOT}^{elec}, which is used to the compute the rotor speed ω_{MOT}^{mech} from (2.25). Once ω_{MOT}^{mech} and s are known, the windings' resistance term R_{rotor} / s are updated.

$$T_{phase}^{elec} = \frac{R_{rotor} V_s^2}{s \cdot \omega_{elec} \left(R_{sr}^2 + \omega_{elec}^2 L_{sr}^2 \right)} \tag{2.26}$$

2.4.2.2.5 Speed Controller

The speed controller regulates the reference signals' frequency f_r in (2.23) for each phase. The rotor's mechanical speed is compared to a reference speed and the difference passed to the speed controller block shown in Fig. 2.4.8, where T_{IM} is the controller's time constant in seconds.

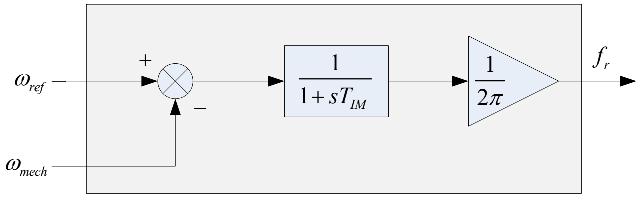


Fig. 2.4.8. Speed controller for induction motor

2.4.2.3 Single-Phase Cable

Single-phase cables distribute power to the single-phase side (120V) of the SPS. All single-phase cables are connected between transformer secondary sides and single-phase loads. The single-phase cable model is based on a nominal-pi line-segment as shown in Fig. 2.4.9, where the parallel conductors represent any two phases. The single-phase cable's differential equations are given in (2.27).

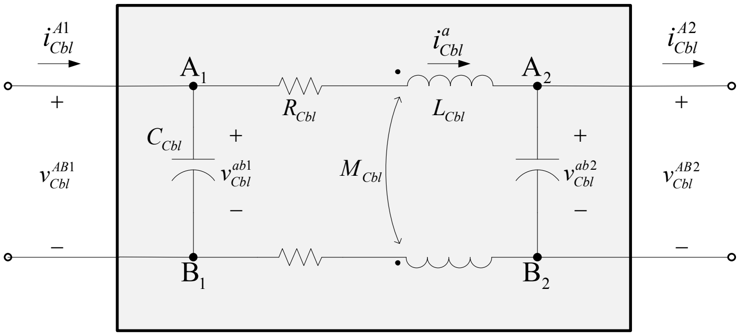


Fig. 2.4.9. Single-phase cable model (current-in, voltage-out)

$$\begin{bmatrix} C_{Cbl} & \cdot & \cdot \\ \cdot & C_{Cbl} & \cdot \\ \cdot & \cdot & L_{Cbl} \end{bmatrix} \begin{bmatrix} \overset{\bullet}{v}_{Cbl}^{ab1} \\ \overset{\bullet}{v}_{Cbl}^{ab2} \\ \overset{\bullet}{i}_{Cbl}^{a} \end{bmatrix} = \begin{bmatrix} \cdot & \cdot & -1 \\ \cdot & \cdot & 1 \\ \frac{4L_{Cbl}R_{Cbl}}{2L_{Cbl}-2M_{Cbl}} & \frac{-4L_{Cbl}R_{Cbl}}{2L_{Cbl}-2M_{Cbl}} & \frac{-4L_{Cbl}R_{Cbl}}{2L_{Cbl}-2M_{Cbl}} \end{bmatrix} \begin{bmatrix} v_{Cbl}^{ab1} \\ v_{Cbl}^{ab2} \\ i_{Cbl}^{a} \end{bmatrix} + \begin{bmatrix} 1 & \cdot \\ \cdot & -1 \\ \cdot & \cdot \end{bmatrix} \begin{bmatrix} i_{Cbl}^{A1} \\ i_{Cbl}^{A2} \end{bmatrix}$$

(2.27)

2.4.2.4 Three-Phase Cable

Three-phase cables distribute power to the three-phase side (450V) of the SPS and are used to interconnect all three-phase components together. The three-phase cable model is based on a nominal-pi line-segment and shown in Fig. 2.4.10, where the three parallel conductors represent phases *a*, *b*, and *c*, respectively. The three-phase cable's differential equations are given in (2.28).

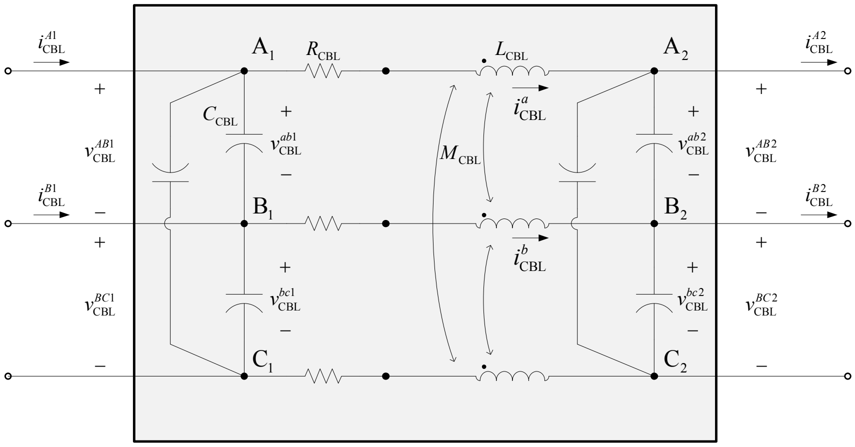


Fig. 2.4.10. Three-phase model (current-in, voltage-out)

$$\begin{bmatrix} 2C_{CBL} & C_{CBL} & \cdot & \cdot & \cdot & \cdot \\ C_{CBL} & -C_{CBL} & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & 2C_{CBL} & C_{CBL} & \cdot & \cdot \\ \cdot & \cdot & C_{CBL} & -C_{CBL} & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & L_{CBL}-M_{CBL} & -\left(L_{CBL}-M_{CBL}\right) \\ \cdot & \cdot & \cdot & \cdot & L_{CBL}-M_{CBL} & 2\left(L_{CBL}-M_{CBL}\right) \end{bmatrix} \begin{bmatrix} \overset{\bullet}{v}{}_{CBL}^{ab1} \\ \overset{\bullet}{v}{}_{CBL}^{bc1} \\ \overset{\bullet}{v}{}_{CBL}^{ab2} \\ \overset{\bullet}{v}{}_{CBL}^{bc2} \\ \overset{\bullet}{i}{}_{CBL}^{a} \\ \overset{\bullet}{i}{}_{CBL}^{b} \end{bmatrix} =$$

$$\begin{bmatrix} \cdot & \cdot & \cdot & \cdot & -1 & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & 1 \\ \cdot & \cdot & \cdot & \cdot & 1 & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & -1 \\ 1 & \cdot & -1 & \cdot & -R_{CBL} & R_{CBL} \\ \cdot & 1 & \cdot & -1 & -R_{CBL} & -2R_{CBL} \end{bmatrix} \begin{bmatrix} v_{CBL}^{ab1} \\ v_{CBL}^{bc1} \\ v_{CBL}^{ab2} \\ v_{CBL}^{bc2} \\ i_{CBL}^{a} \\ i_{CBL}^{b} \end{bmatrix} + \begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & -1 & \cdot & \cdot \\ \cdot & \cdot & -1 & \cdot \\ \cdot & \cdot & \cdot & 1 \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \end{bmatrix} \begin{bmatrix} i_{CBL}^{A1} \\ i_{CBL}^{B1} \\ i_{CBL}^{A2} \\ i_{CBL}^{B2} \end{bmatrix}$$

(2.28)

2.4.2.5 Single-Phase Static Load

The single-phase loads on the SPS are rated at 120V and modeled as static (constant impedance) loads. The single-phase loads are connected to the transformers via single-phase cables. The single-phase load model is shown in Fig. 2.4.11 and described with the differential equation in (2.29).

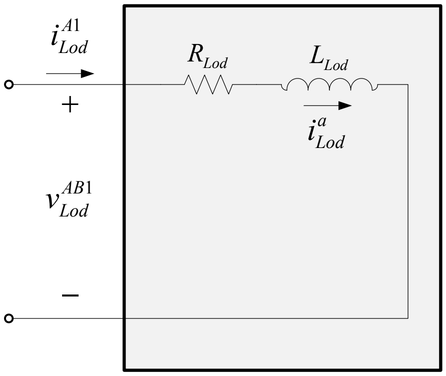


Fig. 2.4.11. Single-phase load model (voltage-in, current-out)

$$L_{Lod}\frac{d}{dt}i_{Lod}^{a} = -R_{Lod} + v_{Lod}^{AB1} \tag{2.29}$$

2.4.2.6 Three-Phase Static Load

The three-phase loads are rated at 450V and are modeled as delta-connected static loads. The three-phase load model is shown in Fig. 2.4.12, where the respective differential equations are given in (2.30).

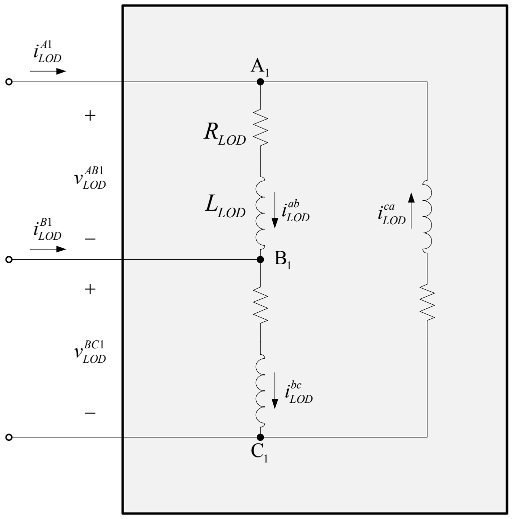


Fig. 2.4.12. Three-phase load model (voltage-in, current-out)

$$\begin{bmatrix} L_{LOD} & \cdot & \cdot \\ \cdot & L_{LOD} & \cdot \\ \cdot & \cdot & L_{LOD} \end{bmatrix} \begin{bmatrix} \dot{i}_{LOD}^{ab} \\ \dot{i}_{LOD}^{bc} \\ \dot{i}_{LOD}^{ca} \end{bmatrix} = -\begin{bmatrix} R_{LOD} & \cdot & \cdot \\ \cdot & R_{LOD} & \cdot \\ \cdot & \cdot & R_{LOD} \end{bmatrix} \begin{bmatrix} i_{LOD}^{ab} \\ i_{LOD}^{bc} \\ i_{LOD}^{ca} \end{bmatrix} + \begin{bmatrix} 1 & \cdot \\ \cdot & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} v_{LOD}^{AB1} \\ v_{LOD}^{BC1} \end{bmatrix}$$

(2.30)

2.4.2.7 Three-Phase Transformer

The transformers on the SPS are delta-delta 450:120V step-down transformers, and supply power to the single-phase loads [81]. The primary sides of the transformers are connected to the three-phase side (450V) of the SPS and the secondary to the single-phase side (120V). The transformers are modeled as three T-model banks connected in delta on both the primary and secondary sides as shown in Fig. 2.4.13.

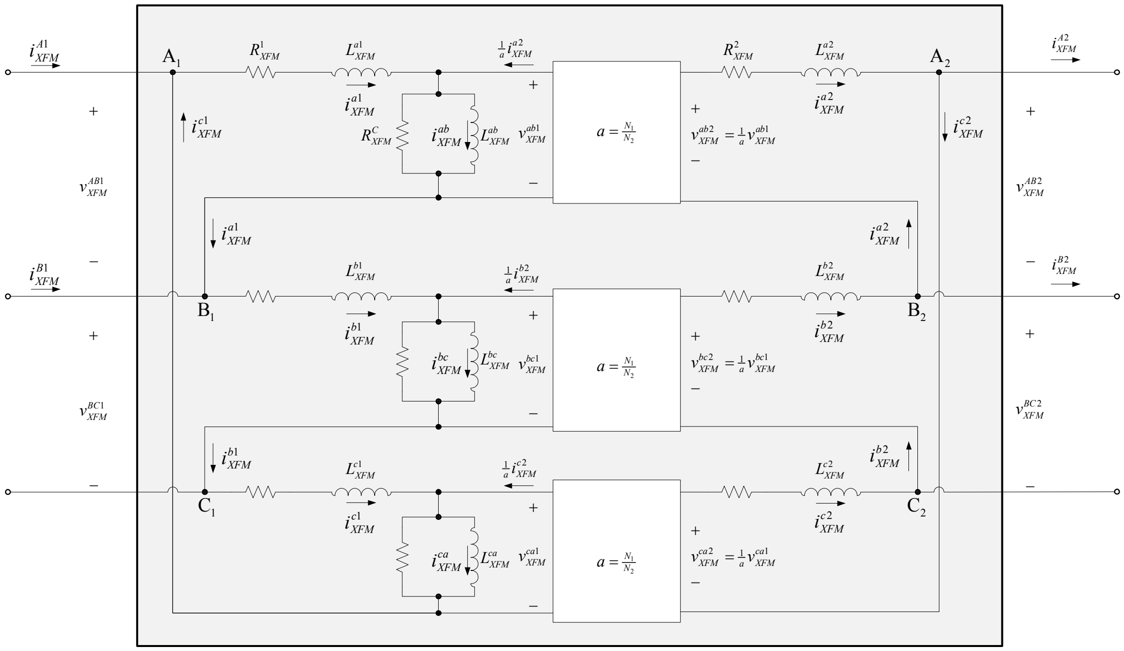


Fig. 2.4.13. Three-phase transformer model (450/120V step-down)

The differential equations for the transformer are given in (2.32).

$$\mathbf{i}_{XFM}=\begin{bmatrix} i_{XFM}^{La1} & i_{XFM}^{Lab1} & i_{XFM}^{La2} & i_{XFM}^{Lb1} & i_{XFM}^{Lbc1} & i_{XFM}^{Lb2} & i_{XFM}^{Lc1} & i_{XFM}^{Lca1} & i_{XFM}^{Lc2} \end{bmatrix} \quad (2.31)$$

$$\mathbf{L}_{XFM}\,\overset{\bullet}{\mathbf{i}}_{XFM}=\mathbf{R}_{XFM}\,\mathbf{i}_{XFM}+\begin{bmatrix} 1 & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & -1 & \cdot \\ \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & -1 \\ -1 & -1 & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & 1 & 1 \end{bmatrix}\begin{bmatrix} v_{XFM}^{AB1} \\ v_{XFM}^{BC1} \\ v_{XFM}^{AB2} \\ v_{XFM}^{BC2} \end{bmatrix} \quad (2.32)$$

$$\mathbf{L}_{XFM}=\mathrm{diag}\left(L_{XFM}^{a1},L_{XFM}^{ab1},L_{XFM}^{a2},L_{XFM}^{b1},L_{XFM}^{bc1},L_{XFM}^{b2},L_{XFM}^{c1},L_{XFM}^{ca1},L_{XFM}^{c2}\right)$$

$$\mathbf{R}_{XFM} = \operatorname{diag}\left(\mathbf{R}_{XFM}^{ab}, \mathbf{R}_{XFM}^{bc}, \mathbf{R}_{XFM}^{ca}\right)_{9\times 9}$$

$$\mathbf{R}_{XFM}^{ab} = \begin{bmatrix} -\left(R_{XFM}^{a1} + R_{XFM}^{Cab1}\right) & R_{XFM}^{Cab1} & \frac{-R_{XFM}^{Cab1}}{a} \\ R_{XFM}^{Cab1} & -R_{XFM}^{Cab1} & \frac{R_{XFM}^{Cab1}}{a} \\ \frac{-R_{XFM}^{Cab1}}{a} & \frac{R_{XFM}^{Cab1}}{a} & -\left(R_{XFM}^{a1} + \frac{R_{XFM}^{Cab1}}{a^2}\right) \end{bmatrix}_{3\times 3}$$

2.4.2.8 Protective Devices

The protective devices modeled in this work are over-current relays, low-voltage relays (LVP), low-voltage relays with automatic re-closers (LVR), automatic bus transfers (ABTs), and manual bus transfers (MBTs). The RMS voltages and currents of any phase and for any protective devices are computed using (2.33).

$$X_{RMS}^{y}\left(t\right) = \sqrt{\frac{1}{T_0}\int_{T_0}\left(x_y\left(t\right)\right)^2 dt} \qquad (2.33)$$

where:

T_0 = fundamental period in seconds

$x_y\left(t\right)$ = instantaneous measurement (voltage or current) of phase y

$X_{RMS}^{y}\left(t\right)$ = RMS value of $x_y\left(t\right)$

2.4.2.8.1 Over-current and Low-voltage Relays

Over-current and low-voltage relays are modeled as three-phase switches that change positions when their protective logic dictates to do so. The logic for over-current relays is based on instantaneous over-current and a fixed opening delay. The relay logic for under-voltage relays is based on a comparing whether the line-to-line voltage has reduced to <405V. If the under-voltage is controlling an LVP, human intervention is required to reclose the switching. If the under-voltage relay is controlling and LVR, the switches reclose automatically when the voltage is restored.

The over-current relay logic is depicted with Fig. 2.4.14, where when any of the line currents $\left\{I_{RMS}^{a}, I_{RMS}^{b}, I_{RMS}^{c}\right\}$ (in RMS Amps) exceeds I_{RMS}^{pickup} a timer is initiated. When the relay timer elapses, the relay issues a signal to the circuit breaker to open the contacts. The logic equations corresponding to Fig. 2.4.14 are given in (2.34), where t_{now} represents the present simulation time in seconds, t_{fault} represents the time in seconds when fault was detected, and t_{delay} is the delay in seconds that the relay waits before opening the circuit breaker contacts.

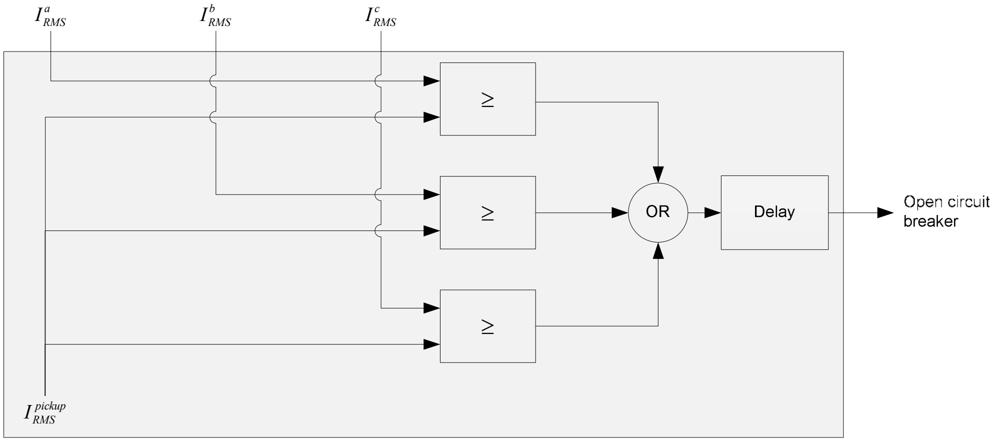


Fig. 2.4.14. Over-current relay logic

$$\begin{array}{l}\text{Over-current}\\\text{relay logic}\end{array}\left\{\begin{array}{l}\text{if}\left(\left(I_{RMS}^{a}>I_{RMS}^{pickup}\right)\text{ or }\left(I_{RMS}^{b}>I_{RMS}^{pickup}\right)\text{ or}\left(I_{RMS}^{c}>I_{RMS}^{pickup}\right)\right)\\\qquad\text{if }\left(t_{now}-t_{fault}\right)>t_{delay}\\\qquad\qquad\text{open conacts;}\\\qquad\text{end}\\\text{else}\\\qquad t_{fault}=t_{now};\qquad\left(\text{clear fault time flag}\right)\\\text{end}\end{array}\right. \tag{2.34}$$

The under-voltage relay logic for LVPs and LVRs is depicted in Fig. 2.4.15. The line-to-line voltages (RMS) as used as inputs to determine whether to isolate a load. If any of the line-to-line voltages of a load falls below 90% of the system's nominal voltage, the relay issues a command to open the LVP or LVR's contacts. In the case of LVRs when the voltage level is restored, the LVR contacts re-close automatically. The logic equations corresponding to Fig. 2.4.15 are given in (2.35).

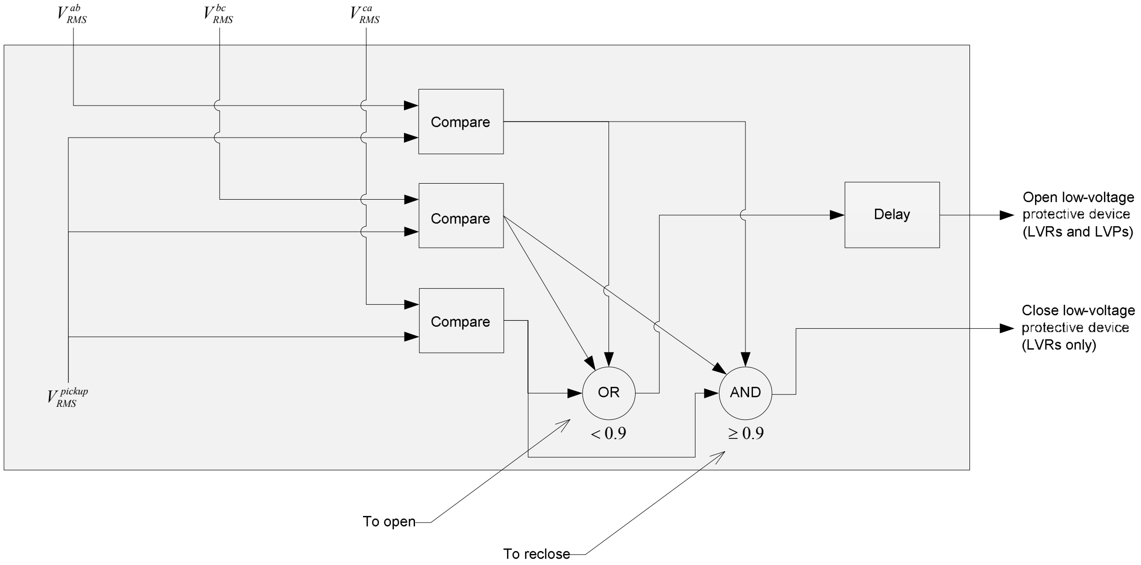


Fig. 2.4.15. Under-voltage relay logic for low voltage protective devices (LVXs)

$$\text{Under-voltage relay logic}\begin{cases} \text{if}\left(\left(V_{RMS}^{ab}<0.9*450\right)\text{ or }\left(V_{RMS}^{bc}<0.9*450\right)\text{ or}\left(V_{RMS}^{ca}<0.9*450\right)\right) \\ \quad\text{if }\left(t_{now}-t_{fault}\right)>t_{delay} \\ \quad\quad\text{open conacts;} \\ \quad\text{end} \\ \text{else} \\ \quad\text{if }\left(\text{LVR}\right) \\ \quad\quad\text{if }\left(\text{voltage is restored}\right) \\ \quad\quad\quad\text{close conacts;} \\ \quad\text{else} \\ \quad\quad t_{fault}=t_{now}; \qquad \left(\text{clear fault time flag}\right) \\ \text{end} \end{cases} \tag{2.35}$$

The electrical network model used for over-current and low-voltage relays is shown in Fig. 2.4.16. The in-line voltage sources $\left\{u_{BRK}^{a}, u_{BRK}^{b}, u_{BRK}^{c}\right\}$ are included to model arcing behavior when the contacts part according to Cassie's model [82]. The equations for electrical network shown in Fig. 2.4.16 are given in (2.36).

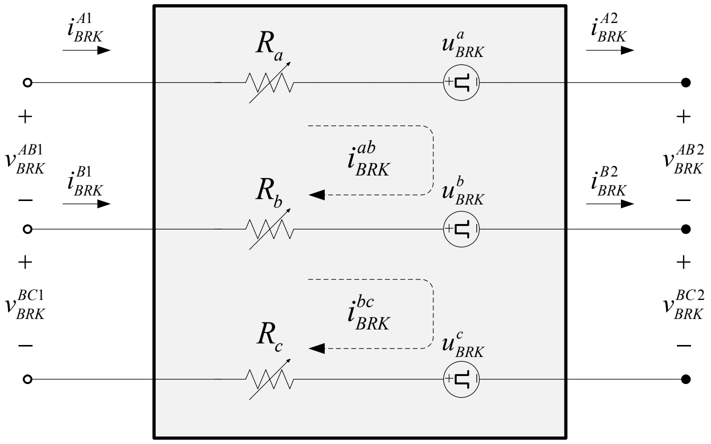


Fig. 2.4.16. Over-current relay and low-voltage protective device model

$$\begin{bmatrix} R_a + R_b & -R_b \\ -R_b & R_b + R_c \end{bmatrix} \begin{bmatrix} i_{BRK}^{ab} \\ i_{BRK}^{bc} \end{bmatrix} = \begin{bmatrix} v_{BRK}^{AB1} - u_{BRK}^{a} - v_{BRK}^{AB2} + u_{BRK}^{b} \\ v_{BRK}^{BC1} - u_{BRK}^{b} - v_{BRK}^{BC2} + u_{BRK}^{c} \end{bmatrix} \tag{2.36}$$

The over-current relay states shown in Fig. 2.4.17 illustrate the transition stages from the closed to open positions. If the protective device is an LVR, the contacts are re-closed when the voltage is restored; if the protective device is an over-current or low-voltage relay, the contacts remain open.

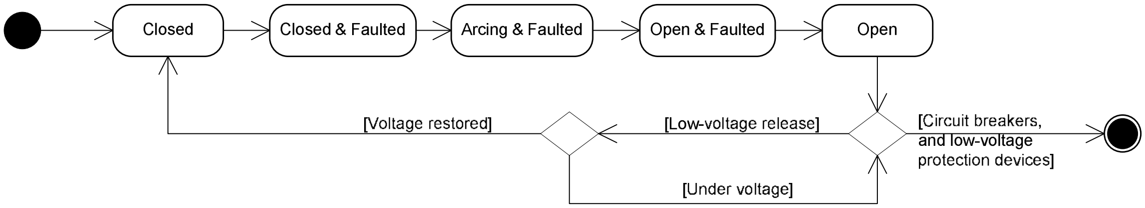


Fig. 2.4.17. Over-current relay and low-voltage protection device states

The arcing sources activate during the arcing stage and are modeled as square-waves with amplitude V_{arc} as given by (2.38), where $\{i_a, i_b, i_c\}$ are the branch currents through phases *a*, *b*, and *c*, respectively.

$$R_{BRK} = \begin{cases} 1\text{m}\Omega\text{, when closed} \\ 0\Omega\text{, when arcing} \\ 1\text{M}\Omega\text{, when open} \end{cases} \tag{2.37}$$

$$\begin{aligned} u_{BRK}^{a} &= \begin{cases} 0\text{V, when closed and open} \\ V_{arc}\,\text{sgn}\left(i_a\right) \end{cases} \\ u_{BRK}^{b} &= \begin{cases} 0\text{V, when closed and open} \\ V_{arc}\,\text{sgn}\left(i_b\right) \end{cases} \\ u_{BRK}^{c} &= \begin{cases} 0\text{V, when closed and open} \\ V_{arc}\,\text{sgn}\left(i_c\right) \end{cases} \end{aligned} \tag{2.38}$$

2.4.2.8.2 Bus Transfer Devices

Bus transfer devices serve loads from either of two paths: a normal path, or an alternate path. All bus transfers all closed on their normal path by default. There are two kinds of bus transfer devices (XBTs): automatic bus transfers (ABTs) and manual bus transfers (MBTs). During low-voltage conditions, ABTs switch from the normal path to the alternate path. When the voltage is restored on the normal path, ABTs automatically switch back to the normal path. Manual bus transfers behave like ABTs except that human intervention is required to switch the MBT to normal path.

An illustration of the XBT model is shown in Fig. 2.4.18. Side 1 is the normal path, side 2 is where the load connects from, and side 3 is the alternate path and only used when the normal path's voltage drops below 405V. The inline voltage sources model the arcing behavior during the switching operation and follow the form of (2.38). The resistance values model the switch positions for sides 1, 2, and 3 and follow (2.37). The algebraic equations for XBTs are given in (2.39).

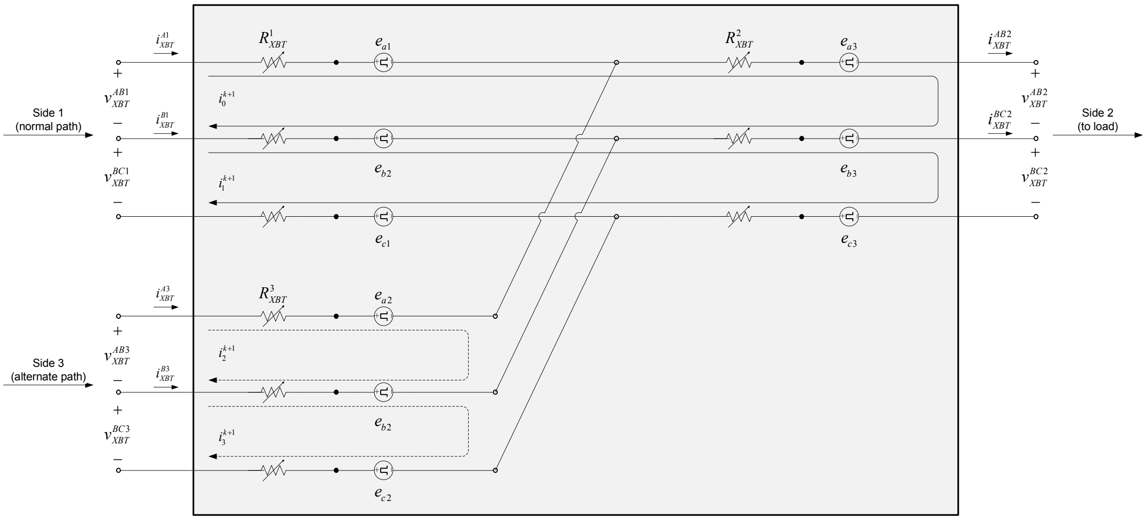


Fig. 2.4.18. Bus transfer model

$$\begin{bmatrix} 2\left(R_{XBT}^{1}+R_{XBT}^{3}\right) & -R_{XBT}^{1}-R_{XBT}^{3} & 2R_{XBT}^{3} & -R_{XBT}^{3} \\ -R_{XBT}^{1}-R_{XBT}^{3} & 2\left(R_{XBT}^{1}+R_{XBT}^{3}\right) & -R_{XBT}^{3} & 2R_{XBT}^{3} \\ 2R_{XBT}^{3} & -R_{XBT}^{3} & 2\left(R_{XBT}^{2}+R_{XBT}^{3}\right) & -R_{XBT}^{2}-R_{XBT}^{3} \\ -R_{XBT}^{3} & 2R_{XBT}^{3} & -R_{XBT}^{2}-R_{XBT}^{3} & 2\left(R_{XBT}^{2}+R_{XBT}^{3}\right) \end{bmatrix} \begin{bmatrix} i_{XBT}^{ab1} \\ i_{XBT}^{bc1} \\ i_{XBT}^{ab2} \\ i_{XBT}^{bc2} \end{bmatrix} = \begin{bmatrix} v_{XBT}^{AB1}-v_{XBT}^{a}-v_{XBT}^{AB3}+v_{XBT}^{b} \\ v_{XBT}^{BC1}-v_{XBT}^{b}-v_{XBT}^{BC3}+v_{XBT}^{c} \\ v_{XBT}^{AB2}-v_{XBT}^{a}-v_{XBT}^{AB3}+v_{XBT}^{b} \\ v_{XBT}^{BC2}-v_{XBT}^{b}-v_{XBT}^{BC3}+v_{XBT}^{c} \end{bmatrix} \tag{2.39}$$

When switching from side 1 to side 2, the inline voltage sources at side 1 arc before side 2 is closed. The transition states when switching from side 1 to side 2 are shown in Fig. 2.4.19.

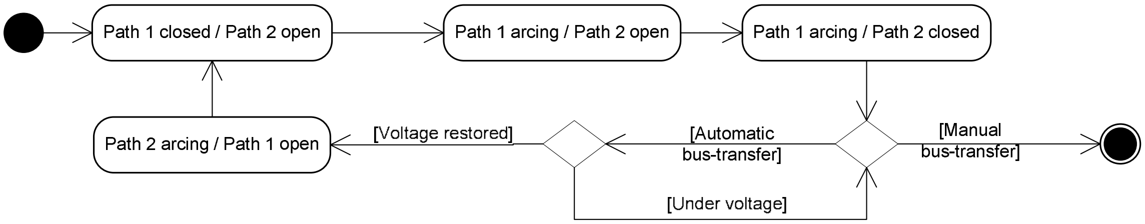

Path 1 closed / Path 2 open
Path 1 arcing / Path 2 open
Path 1 arcing / Path 2 closed
Path 2 arcing / Path 1 open
[Voltage restored]
[Automatic bus-transfer]
[Manual bus-transfer]
[Under voltage]

Fig. 2.4.19. Bus-transfer device states

The relay logic for XBTs is similar to the relay logic for LVXs as shown in Fig. 2.4.20. When any of the three line-to-voltages on side 1 falls below 90%, the contacts move from side 1 to side 2 following the transition states in Fig. 2.4.19. If the XBT is an ABT, the contacts will reposition themselves on side 1 when side 1's voltage is restored (i.e., $\geq 90\%$). Similar to LVXs, the XBT's under-voltage relay logic is given in (2.40).

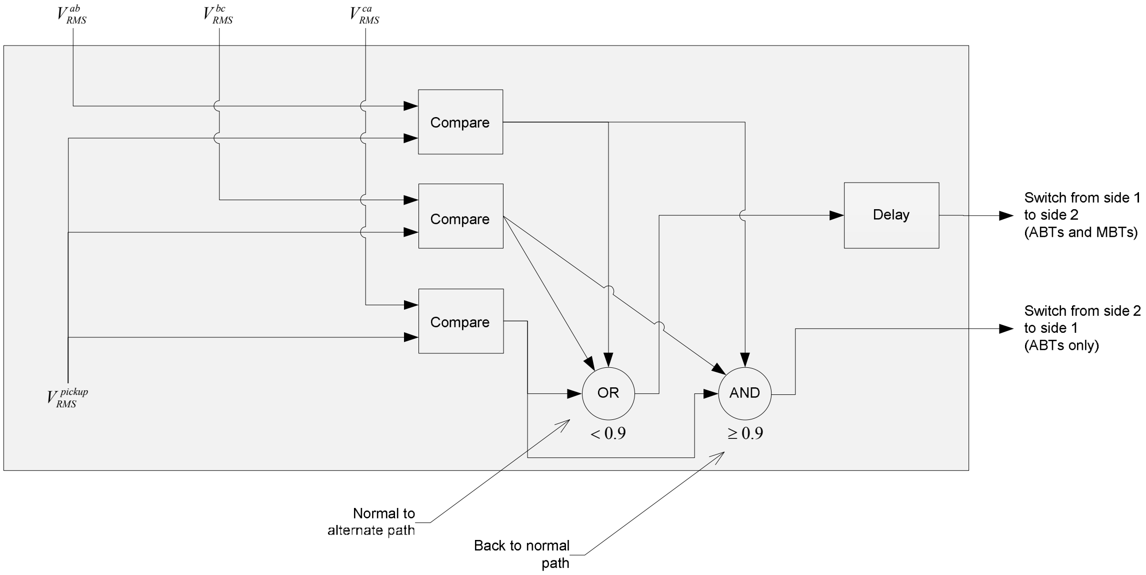


Fig. 2.4.20. Under-voltage relay logic for bus transfers (XBTs)

$$\begin{array}{l}\text{Under-voltage} \\ \text{relay logic}\end{array}\left\{\begin{array}{l}
\text{if}\left(\left(V_{RMS}^{ab} < 0.9*450\right) \text{ or } \left(V_{RMS}^{bc} < 0.9*450\right) \text{ or}\left(V_{RMS}^{ca} < 0.9*450\right)\right) \\
\qquad \text{if } \left(t_{now} - t_{fault}\right) > t_{delay} \\
\qquad\qquad \text{move contacts to side 2;} \\
\qquad \text{end} \\
\text{else} \\
\qquad \text{if } \left(\text{ABT}\right) \\
\qquad\qquad \text{if } \left(\text{voltage is restored}\right) \\
\qquad\qquad\qquad \text{move contacts to side 1;} \\
\qquad \text{else} \\
\qquad\qquad t_{fault} = t_{now}; \qquad \left(\text{clear fault time flag}\right) \\
\text{end}
\end{array}\right. \tag{2.40}$$

2.4.3 Interconnections

The previous section introduced the SPS components as stand-alone MTCs with exogenous inputs. To interconnect all MTCs and form a system of DAEs, voltage and current constraints at each node must be satisfied. At each node where two or more MTCs connect the line-to-line voltages must be the same for all MTCs at said node. Additionally, the net sum of currents entering and leaving the same node must equal zero.

MTC interconnections are illustrated via the connections shown in Fig. 2.4.21, where node 1 is reminiscent of a switchboard or load-center (bus node). To connect the cable to the over-current relay monitoring a breaker, the voltage and current algebraic equations in (2.41) and (2.42) are used. Equation (2.41) is Kirchhoff's second law (KVL), and (2.42) is Kirchhoff's first law (KCL).

$$\begin{array}{c}\text{Voltage}\\\text{constraints}\end{array}\rightarrow\begin{array}{l}\begin{cases}0=-v_{CBL1}^{AB2}+v_{BRK1}^{AB1}\\0=-v_{CBL1}^{BC2}+v_{BRK1}^{BC1}\end{cases}\\\begin{cases}0=-v_{CBL1}^{AB2}+v_{BRK2}^{AB1}\\0=-v_{CBL1}^{BC2}+v_{BRK2}^{BC1}\end{cases}\\\begin{cases}0=-v_{CBL1}^{AB2}+v_{BRK3}^{AB1}\\0=-v_{CBL1}^{BC2}+v_{BRK3}^{BC1}\end{cases}\end{array}\tag{2.41}$$

$$\begin{array}{c}\text{Current}\\\text{constraints}\end{array}\rightarrow\begin{cases}0=-i_{CBL1}^{A2}+i_{BRK1}^{A1}+i_{BRK2}^{A1}+i_{BRK3}^{A1}\\0=-i_{CBL}^{B2}+i_{BRK1}^{B1}+i_{BRK2}^{B1}+i_{BRK3}^{B1}\end{cases}\tag{2.42}$$

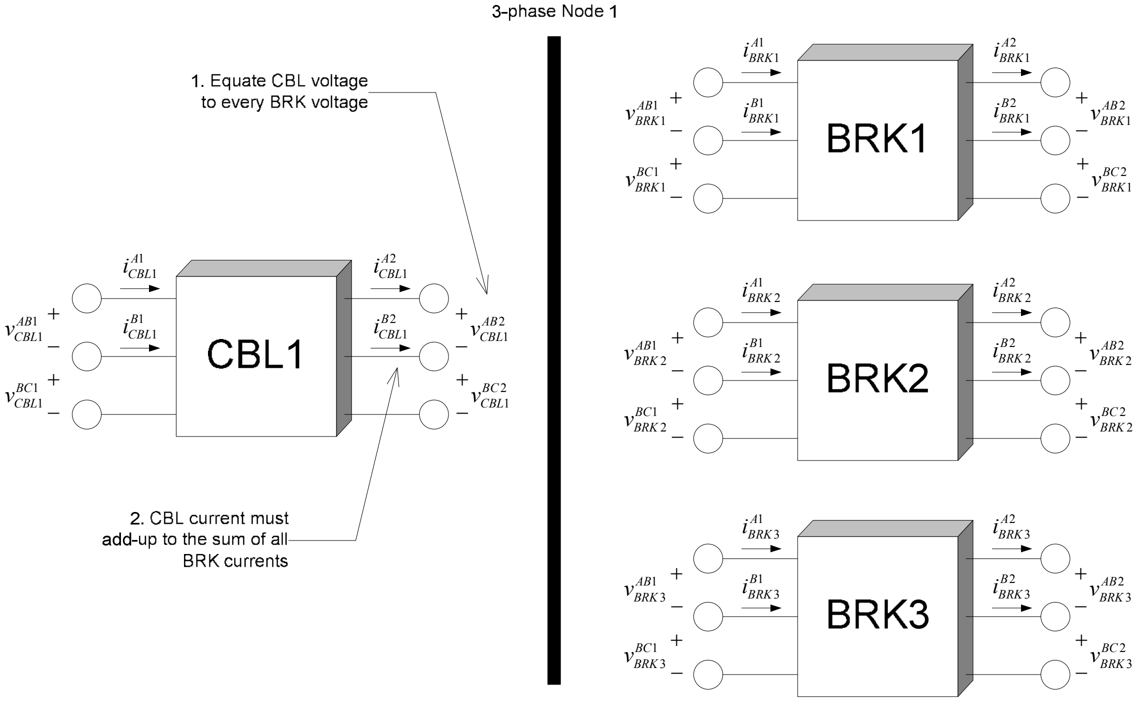


Fig. 2.4.21 . Example connection of a cable and transformer

The voltage and current algebraic constraints in (2.41) and (2.42) are repeated at each single-phase and three-phase node in the system. After writing differential and/or algebraic equations for each MTC, and after all nodes have been visited and described with KVL and KCL equations, the system is algebraically connected and the DAE formulation is complete.

2.4.4 System Equation Formulation

The differential and/or algebraic equations for each MTC were given in section 2.4.2, whereas the interconnection equations were given in section 2.4.3. The set of all MTC and connection equations was used to formulate a notional AC-Radial SPS DAE model.

Shipboard power systems can be represented by the DAEs in (2.43). In (2.43) $\dot{\mathbf{x}}$ is the system's state-vector containing all SPS MTCs' state-variables; $\dot{\mathbf{u}}$ is the input vector containing all SPS MTCs' inputs; $\mathbf{y}$ is the vector of measurements of interest (i.e., node voltages and branch currents). The functions (f, g, h) may be linear, or non-linear depending on each component model. The independent variable t represents time.

$$\begin{array}{c}\text{DAE}\\ \text{equation}\\ \text{formulation}\end{array} \rightarrow \begin{cases}\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u}, t)\\ \mathbf{0} = g(\mathbf{x}, \mathbf{u}, t)\\ \mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)\end{cases} \tag{2.43}$$

The equation $\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u}, t)$ represents the components' differential equations, $\mathbf{0} = g(\mathbf{x}, \mathbf{u}, t)$ represents components' algebraic equations and the voltage and current constraints at each node. Equation $\mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)$ specifies the variables of interest, which are the nodes' line-to-line voltages and select branch currents. The state vector $\mathbf{x}$ is shown in block-vector form in (2.44), where each sub-vector represents the state-variables of each group of components. For example, the vector $\mathbf{x}_{GEN} \in \mathbf{x}$ in (2.45) contains the state-variables for three generators. The first generators' subvector $\mathbf{x}_{GEN1} \in \mathbf{x}_{GEN}$ in (2.46) contains the state-variables corresponding to generator 1's windings (WND), prime-mover and governor (PMG), rotor (ROT), and voltage regulator and exciter (VRE) as introduced in section 2.4.2.1. Similarly for three-phase cables (CBL), the i^{th} three-phase CBL equations are found in $\mathbf{x}_{CBL1} \in \mathbf{x}_{CBL}$.

$$\mathbf{x} = \begin{bmatrix} \underbrace{\mathbf{x}_{GEN}}_{\text{generators}} & \underbrace{\mathbf{x}_{MOT}}_{\text{ind.mots.}} & \underbrace{\mathbf{x}_{Cbl}}_{1\varphi\text{ cables}} & \underbrace{\mathbf{x}_{CBL}}_{3\varphi\text{ cables}} & \underbrace{\mathbf{x}_{Lod}}_{1\varphi\text{ loads}} & \underbrace{\mathbf{x}_{LOD}}_{3\varphi\text{ loads}} & \underbrace{\mathbf{x}_{XFM}}_{\text{transformers}} \end{bmatrix}^{\mathrm{T}} \tag{2.44}$$

$$\mathbf{x}_{GEN} = \begin{bmatrix} \mathbf{x}_{GEN1} & \mathbf{x}_{GEN2} & \mathbf{x}_{GEN3} \end{bmatrix}^{\mathrm{T}} \tag{2.45}$$

$$\mathbf{x}_{GEN1} = \begin{bmatrix} \mathbf{x}_{WND1} & \mathbf{x}_{PMG1} & \mathbf{x}_{ROT1} & \mathbf{x}_{VRE1} \end{bmatrix}^{\mathrm{T}} \tag{2.46}$$

$$\mathbf{x}_{CBL} = \begin{bmatrix} \mathbf{x}_{CBL1} & \mathbf{x}_{CBL2} & \cdots & \mathbf{x}_{CBL114} \end{bmatrix}^{\mathrm{T}} \tag{2.47}$$

An illustration of a notional AC-Radial SPS is repeated in Fig. 2.4.22, where the description of the components and topology was given in section 2.2.1. The component models used in this work are summarized and shown with their state-variable count in Table II.4. The algebraic equation count is shown in . From Table II.4 and Table II.5 it is seen that the order of a SPS DAE simulation is nearly 3,000 equations of which ~1600 are state-variable equations, and ~1300 are algebraic equations.

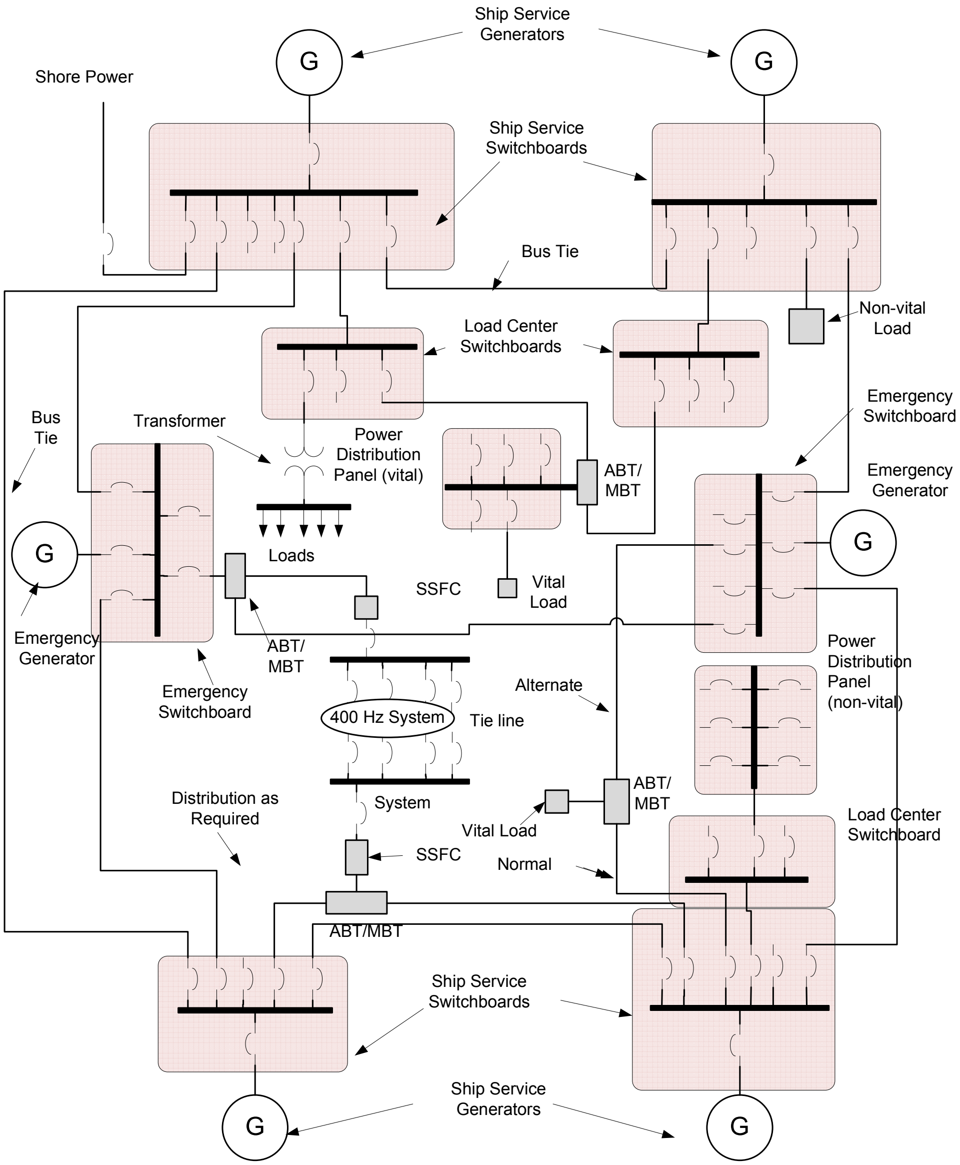


Fig. 2.4.22. Illustration of a notional AC-Radial SPS (repeated from Fig. 2.2.2)

TABLE II.4. DAE FORMULATION'S STATE-VARIABLE COUNT

Acronym	Component Description	Number of	No. State-Variables	Total
GEN	Synchronous generator	3	15	45
MOT	Induction motor	19	9	171
Cbl	Single-phase cable	33	4	132
CBL	Three-phase cable	108	6	648
Lod	Single-phase static load	33	1	33
LOD	Three-phase static load	13	3	39
XFM	Three-phase transformer	11	9	99
BRK	Over-current relay	83	3	249
XBT*	Bus transfer	28	3	84
LVX**	Low-voltage relay	19	3	57
	Totals	350		1,557

*15 Automatic (ABTs); 13 manual (MBTs)

** 2 Automatic (LVRs); 17 manual (LVPs)

TABLE II.5. DAE FORMULATION'S ALGEBRAIC EQUATION COUNT

Component Interconnections		No. Algebraic Equations	No. Connection Occurences	Total Number of Algebraic Equations
From	To			
Cbl	Lod	2	33	66
CBL	XFM	4	11	44
CBL	LVX	4	11	44
CBL	MOT's RCT	4	19	76
CBL	LOD	4	32	128
CBL	CBL	4	63	252
CBL	IRR	4	83	332
CBL	XBT	4	27	108
GEN PMG	GEN ROT	2	3	6
GEN VRE	GEN WND	2	3	6
GEN WND	GEN ROT	2	3	6
GEN WND	BRK	4	3	12
LVX	MOT RCT	11	4	44
MOT PWM	MOT WND	4	11	44
MOT RCT	MOT PWM	2	11	22
MOT ROT	MOT CTR	1	11	11
MOT WND	MOT ROT	1	11	11
XFM	Cbl	2	33	66
			Total	1,278

2.5 PROBLEM FORMULATION

The problem that this work addresses is to obtain, in reasonable time, the instantaneous node voltages and branch currents defined in $\mathbf{y} = h(\mathbf{x},\mathbf{u},t)$. Henceforth, to produce fast time domain simulations of AC-Radial SPSs an approach to parallelize the solution of $\dot{\mathbf{x}} = f(\mathbf{x},\mathbf{u},t)$, $\mathbf{0} = g(\mathbf{x},\mathbf{u},t)$ to obtain $\mathbf{y}$ using a multicore computer is sought .

Parallelizing an SPS simulation requires domain decomposition *a priori*. In this regard, an approach to partition SPSs as smaller sub-domains is required. Prominent challenges associated with this requirement are the introduction of singularities, inaccuracies, numerical stability, overwhelming simulation times, and ill-conditioning, all of which should be overcome in the end.

To partition a SPS, a formulation approach suitable for tearing should be developed first. The suitability of a formulation approach implies that it must be decomposable into smaller formulations of the same kind. With a suitable formulation approach, a partitioning approach to tear said formulation should be devised.

For the partitioning approach to be valid, partitioned SPS simulation results must agree with unpartitioned simulation results, and be obtained in less time. Multicore computers are suitable computers to parallelize the execution of tasks previously decomposed (i.e., partitioned). Using a multiprocessor computer SPS subsystems are sought to be solved concurrently, which implies facing the aforementioned challenges.

An issue that emerges as a result of parallelizing the simulation is the potential communication latency between subsystems. Subsystem communication is needed to exchange boundary voltages and current to other parts of a partitioned SPS. Keeping the communication between subsystems minimal is likely to counter-act the speeds in gain as only a few partitions could exist.

In summary, the problems this work addresses are obtaining a suitable formulation approach for which domain decomposition can be applied. Once a SPS is decomposed the SPS subsystems ought to be solved faster and concurrently using a multicore computer, without incurring overhead nor affecting the accuracy of the simulation.

2.6 CHAPTER SUMMARY

This chapter introduced the concept of time domain simulations. Useful books on the subject are [24],[45],[71],[83-84]. The reasons why time domain simulations demand vast computer resources were given, which led to stating the reasons that motivated this work. Relevant work in this area was presented and a literature review on current approaches to reduce simulation run-time was given.

This chapter also introduced and assessed the problem of large-scale SPS simulation. To assess the complexity of large-scale SPS simulation, a differential-algebraic equation formulation was presented. The DAE equation count was summarized in Table II.2 and Table II.3, which gives an idea of the order of AC-Radial SPS models and the complexity of their time domain simulation. The next chapter will present the solution methodology based on the same three stages previously listed: discretization, partitioning, and simulation.

CHAPTER III

SOLUTION METHODOLOGY

3.1 INTRODUCTION

This chapter presents the new methodology devised to parallelize AC-Radial SPS time domain simulation in three stages:

- Formulation of the system's mathematical representation
- Partition of the system and creation of its subsystems
- Simulation of the subsystems using a multithreaded approach.

The problem formulation stated that the solution of the set $\dot{\mathbf{x}} = f(\mathbf{x},\mathbf{u},t)$, $\mathbf{0} = g(\mathbf{x},\mathbf{u},t)$ is the mean to obtain $\mathbf{y} = h(\mathbf{x},\mathbf{u},t)$, which is of interest to a user. With the aim of producing fast time domain simulations and obtain $\mathbf{y} = h(\mathbf{x},\mathbf{u},t)$, a mathematical system representation which can be parallelized is sought. Said aim requires the reformulation in, preferably, less number of equations, and that the new formulation be decomposable with minimal subdomain inter-coupling. Discretization is the process of representing a system described in the time domain as a system described at discrete intervals of time, which is a necessary step for computer simulation.

To ready SPSs models for computer simulation, all SPS component models were discretized by replacing their inductors and capacitors (if any) with equivalent discretized branches. After each component model was discretized, the SPS system representation was mathematically re-formulated using discrete-time loop currents as variables, which is an alternate (and of reduced order) formulation to the DAE formulation presented in (2.43). The resulting discrete-time formulation is a system of linear algebraic equations that can be solved at discrete intervals of time.

The partitioning stage consists of tearing a SPS into subsystems to parallelize the simulations. To determine where to tear the SPS, a weighted graph representative of an SPS was created, where each graph vertex represents a (discretized) SPS component model, and each graph edge represents a single-phase or three-phase node. Weights were assigned to each vertex based on the estimated computational effort of solving the loop equations of each model. The partitioning stage partitions the representative graph using the mincut algorithm [2],[3] to create an initial graph segregation. To balance the graph partitions, balancing heuristics are used to move vertices across partitions. The final edge-cut resulting from the balancing heuristics corresponds to the points of disconnection on the SPS where tearing occurs.

When the points of disconnection of the SPS have been determined, a partitioning approach motivated by diakoptics [4] is used to tear the SPS into subsystems. The partitioning approach presented in this work uses capacitor loops as the points of disconnection. By shorting two (out of three) capacitors on three-phase cables, a large portion of the network matrix's off-diagonal region is depleted producing subsystem decoupling. This rapid off-diagonal depletion is a direct result of the formulation approach taken, which concentrates loop currents at bus node capacitors where most of disconnection points are.

The simulation stage is started by invoking threads from the Windows thread pool, where each thread calls the *solve* routine on each subsystem object. The loop current solution of each subsystem is used to find the boundary conditions of where the capacitor loops were torn. Knowledge of the boundary condition variables allows to *patch* the solution of each subsystem, which are naturally incorrect since subsystems are solved independently.

The following subsections present the details of the aforementioned stages. Details of programming implementation and techniques are given as references where they are thoroughly explained. The multithreaded synchronization approach and some of the object-oriented techniques used in this work can be found in the appendices.

3.2 MATHEMATICAL SYSTEM REPRESENTATION

To solve for the voltages and currents defined in $\mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)$, a discretization and re-formulation approach is needed. Discretization replaces the differential relationships of $\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u}, t)$ with algebraic difference equations that can be solved in time intervals of Δt (often referred to as the EMTP discretization approach [5],[24]). Once a power system is discretized, a system of linear algebraic equations is formulated in the form of (3.1). Several formulation approaches lead to the form in (3.1) which is why the general notation **A·x**=**b** is used.

$$\mathbf{A} \cdot \mathbf{x} = \mathbf{b} \tag{3.1}$$

where:

A = network coefficient matrix
x = network variables
b = network excitation (input) vector.

To discretize a SPS (and power systems in general), each component model's inductors and capacitors are replaced with discretized equivalent circuits derived from difference equations. After all component models are discretized the SPS becomes a purely resistive (algebraic) network and can be formulated as (3.1).

The trapezoidal rule is a commonly used discretization algorithm and the one used here due to its low truncation error (high accuracy). However, the trapezoidal rule suffers from a well-known drawback: numerical chatter is injected when inductive currents are interrupted (even at 0A crossings), among other reasons detailed [85-86]. To avoid numerical chatter, a technique known as the critical damping adjustment (CDA) [86]is implemented in this work. The CDA technique suggests the following actions during a switching discontinuity. When a switching instant is encountered (e.g., protective device opening), the time step size is divided by two (i.e., $\Delta t_{BE} = \Delta t_{TR} / 2$), the integration algorithm changed from the trapezoidal rule to the backward Euler, and two forward steps taken. Taking two forward steps at Δt_{BE} is equivalent to advancing one Δt_{TR} .

The trapezoidal rule is the default integration algorithm and is recommended for electrical networks where voltage and currents are sinusoidal; backward Euler integration is recommended for networks that are piecewise linear, frequently switching [85-86], or when there are many power electronic devices in a system [83],[87]. Since

SPSs exhibit both sinusoidal and piecewise linear behaviors, an adjustable integration algorithm [71] is presented next, which permits changing integration algorithms during run-time .

Considering the differential equation in (3.2), where $x(t)$ is the state-variable, and $u(t)$ the forcing function, backward Euler and trapezoidal integration of (3.2) result in (3.3) and (3.4), respectively. In (3.3) and (3.4) the super-script $k+1$ represents a value at the present time step, and k a value from the previous time step.

$$\dot{x} = h\left(x(t),u(t)\right), \qquad x(0) = x_0 \tag{3.2}$$

$$\frac{x^{k+1}-x^k}{\Delta t} = h\left(x^{k+1},u^{k+1}\right), \quad x(0) = x_0 \quad \begin{pmatrix}\text{backward}\\ \text{Euler}\end{pmatrix} \tag{3.3}$$

$$\frac{x^{k+1}-x^k}{\Delta t} = \frac{h\left(x^{k+1},u^{k+1}\right)+h\left(x^k,u^k\right)}{2}, \quad x(0) = x_0 \quad \begin{pmatrix}\text{trapezoidal}\\ \text{rule}\end{pmatrix} \tag{3.4}$$

The difference between (3.3) and (3.4) is an implicit right-hand side (RHS) coefficient. To control said coefficient a parameter γ is used to select between integration algorithms as given by (3.5).

$$\frac{x^{k+1}-x^k}{\Delta t} = \gamma \cdot h\left(x^{k+1},u^{k+1}\right)+(1-\gamma)h\left(x^k,u^k\right) \tag{3.5}$$

where $\gamma \rightarrow \begin{cases} =\dfrac{1}{2} & \text{for trapezoidal rule} \\ =1 & \text{for backward Euler} \end{cases}$

Using the tunable integration in (3.5), the discretization of inductors, capacitors, state-variable equations, and RMS measurements are introduced next. The discretized component models (with their inductors and capacitors replaced) are given in the Appendix.

3.2.1 Discretization of an Inductor

The inductor's fundamental differential equation is discretized in (3.6). In (3.6), v_L^{k+1} is the voltage across an inductor in Volts, L is the inductance in Henries, Δt is the discretization time step in seconds, γ is an adjustable parameter that determines the integration method [71] (i.e., $\gamma = \frac{1}{2}$ for trapezoidal rule, $\gamma = 1$ for backward Euler), i_L^{k+1} is the current through the inductor in Amps, and hist_L^{k+1} a voltage impression which is a function of the previous time step solution's values. The equivalent circuit for the discretized inductor equation is shown at the lower-left in Fig. 3.2.1.

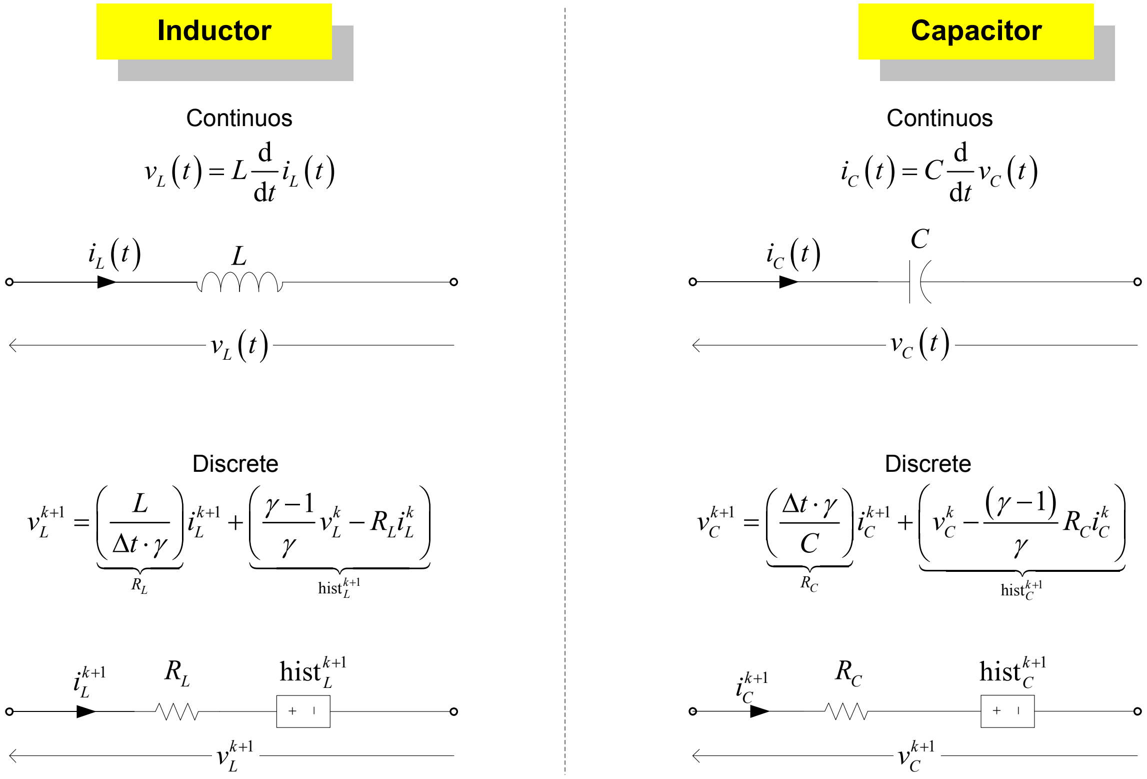
$$v_L(t) = L\frac{d}{dt}i_L(t) \qquad \Rightarrow \qquad v_L^{k+1} = \left(\frac{L}{\Delta t \cdot \gamma}\right)i_L^{k+1} + \underbrace{\left(\frac{\gamma - 1}{\gamma}v_L^k - \frac{L}{\Delta t \cdot \gamma}i_L^k\right)}_{\text{hist}_L^{k+1}} \tag{3.6}$$

3.2.2 Discretization of a Capacitor

The capacitor's fundamental differential equation is discretized in (3.7). In (3.7), v_C^{k+1} is the voltage across a capacitor in Volts, C is the capacitance in Farads, Δt is the discretization time step in seconds, i_C^{k+1} is the current through the capacitor in Amps, and hist_C^{k+1} is a voltage impression term, which is a function of the previous time step solution's values. The equivalent circuit for the discretized capacitor equation is shown at the lower-right in Fig. 3.2.1.

$$v_C(t) = \frac{1}{C}\int i_C(t)\mathrm{d}t \quad \Rightarrow \quad v_C^{k+1} = \left(\frac{\Delta t \cdot \gamma}{C}\right) i_C^{k+1} + \underbrace{\left(v_C^k + \frac{\Delta t(1-\gamma)}{C} i_C^k\right)}_{\text{hist}_C^{k+1}} \quad (3.7)$$

The discretization of inductors and capacitors have been introduced and discussed. The next subsection introduces the discretization of differential equations in state-variable form, which, in this work, are used to represent machine controllers and rotor dynamic equations.


Inductor
Capacitor
Continuos
$v_L(t) = L\frac{\mathrm{d}}{\mathrm{d}t}i_L(t)$
$i_L(t)$
L
$v_L(t)$
Continuos
$i_C(t) = C\frac{\mathrm{d}}{\mathrm{d}t}v_C(t)$
$i_C(t)$
C
$v_C(t)$
Discrete
$v_L^{k+1} = \underbrace{\left(\frac{L}{\Delta t \cdot \gamma}\right)}_{R_L} i_L^{k+1} + \underbrace{\left(\frac{\gamma - 1}{\gamma} v_L^k - R_L i_L^k\right)}_{\mathrm{hist}_L^{k+1}}$
i_L^{k+1}
R_L
hist_L^{k+1}
v_L^{k+1}
Discrete
$v_C^{k+1} = \underbrace{\left(\frac{\Delta t \cdot \gamma}{C}\right)}_{R_C} i_C^{k+1} + \underbrace{\left(v_C^k - \frac{(\gamma - 1)}{\gamma} R_C i_C^k\right)}_{\mathrm{hist}_C^{k+1}}$
i_C^{k+1}
R_C
hist_C^{k+1}
v_C^{k+1}

Trapezoidal Rule: $\gamma = \frac{1}{2}$
Backward Euler: $\gamma = 1$

Fig. 3.2.1. Equivalent circuits for discretized inductors and capacitors

3.2.3 Discretization of Controllers and Relays

Machine controllers and rotor dynamic equations were formulated using state-variable equations in (2.17), (2.18), (2.19), and (2.25), respectively, and have the form of (3.8). Discretization of (3.8) using tunable integration is given by (3.9)-(3.10) [88].

$$\mathbf{x}(t) = \mathbf{A} \cdot \mathbf{x} + \mathbf{B} \cdot \mathbf{u}(t) \tag{3.8}$$

$$\tfrac{1}{\Delta t}\left(\mathbf{x}^{k+1} - \mathbf{x}^k\right) = \mathbf{A}\left(\gamma \cdot \mathbf{x}^{k+1} + (1-\gamma)\mathbf{x}^k\right) + \mathbf{B}\left(\gamma \cdot \mathbf{u}^{k+1} + (1-\gamma)\mathbf{u}^k\right) \tag{3.9}$$

Solving for the state-variable vector $\mathbf{x}^{k+1}$:

$$\mathbf{x}^{k+1} = \underbrace{\overbrace{\left(\tfrac{1}{\Delta t}\mathbf{I} - \gamma\cdot\mathbf{A}\right)^{-1}}^{\mathbf{Q}} \left(\tfrac{1}{\Delta t}\mathbf{I}+\left(1-\gamma\right)\cdot\mathbf{A}\right)}_{\mathbf{M}}\mathbf{x}^{k} + \underbrace{\mathbf{Q}\cdot\mathbf{B}}_{\mathbf{N}}\left(\gamma\cdot\mathbf{u}^{k+1}+\left(1-\gamma\right)\mathbf{u}^{k}\right) \quad (3.10)$$

$$\begin{matrix}\text{Discretized state-}\\ \text{variable equations}\end{matrix} \rightarrow \begin{cases}\mathbf{x}^{k+1} = \mathbf{M}\cdot\mathbf{x}^{k} + \mathbf{N}\left(\gamma\cdot\mathbf{u}^{k+1}+\left(1-\gamma\right)\mathbf{u}^{k}\right)\\ \mathbf{y}^{k+1} = \mathbf{C}\cdot\mathbf{x}^{k+1} + \mathbf{D}\left(\gamma\cdot\mathbf{u}^{k+1}+\left(1-\gamma\right)\mathbf{u}^{k}\right)\end{cases} \quad (3.11)$$

where:

$\mathbf{x}^{k+1}$ = vector of state-variables at time step $k+1$

$\mathbf{x}^{k}$ = vector of state-variables at time step k

$\mathbf{u}^{k+1}$ = input vector at time step $k+1$

$\mathbf{u}^{k}$ = input vector at time step k

A = state-matrix; **B** = input matrix; **I** = identity matrix;

C = output-to-state matrix; **D** = output-to-input matrix

Δt = time step increment; $\gamma=\dfrac{1}{2}$ for trapezoidal rule; $\gamma=1$ for backward Euler.

In the discretization of inductors, capacitors, and state-variable equations, the time step increment Δ*t* was assumed constant. Though Δ*t* can be changed during run-time, in this work Δ*t* is fixed (Δ*t* is also fixed in commercial power system simulators such as [14],[26]). The reason to hold Δ*t* constant is due to the network matrix (matrix **A** in a system **A·x**=**b**), where the coefficients of **A** depend on Δ*t*. Referring to the equivalent circuits of inductors and capacitors in Fig. 3.2.1, each resistance is a function of Δ*t*. As resistance values are part of **A**, changing Δ*t* would require reforming and re-triangulating

A every time Δt changes [86]. Since in power system simulation the matrix **A** is large, reforming and re-triangulating is time-consuming and would increase run-time. Variable Δt solvers are better suited, perhaps, for the simulation of small circuits. In the simulation of small circuits, in contrast with power systems, frequent calculations of a Δt size [89] and changes of the network matrix are not as noticeable [90].

Relays constantly check their RMS measurements against pre-specified thresholds to determine whether they should signal a tripping signal. The continuous-time RMS introduced in (2.33) is repeated in (3.12) for convenience.

$$X_{RMS}^{y}\left(t\right)=\sqrt{\frac{1}{T_0}\int_{T_0}\left(x_y\left(t\right)\right)^2 dt} \tag{3.12}$$

where:
T_0 = fundamental period in seconds
$x_y\left(t\right)$ = instantaneous measurement (voltage or current) of phase y
$X_{RMS}^{y}\left(t\right)$ = RMS value of $x_y\left(t\right)$

The discretized RMS measurement of a continuous signal $x_y\left(t\right)$, sampled at every time step k (noted x^k), is given in (3.13). Use of (3.13) is computationally inefficient, for which a recursive RMS computation is derived instead.

$$\text{RMS}\left(x^k\right)=\sqrt{\frac{1}{N}\sum_{k-N+1}^{k}\left(x^k\right)^2} \tag{3.13}$$

where:

$N = ceil\left(\frac{T}{\Delta t}\right)$ = the number of samples in a running-window

Δt = the time step increment

$T = \frac{1}{60} = 16.67\text{ms}$ = the fundamental sampling period

Expanding (3.13) :

$$\text{RMS}\left(x^k\right) = \sqrt{\left(\frac{\left(x^{(k-N)+1}\right)^2}{N} + \frac{\left(x^{(k-N)+2}\right)^2}{N} + \cdots + \frac{\left(x^{k-1}\right)^2}{N} + \frac{\left(x^k\right)^2}{N}\right)} \tag{3.14}$$

Squaring both sides:

$$\text{RMS}^2\left(x^k\right) = \frac{\left(x^{(k-N)+1}\right)^2}{N} + \frac{\left(x^{(k-N)+2}\right)^2}{N} + \cdots + \frac{\left(x^{k-1}\right)^2}{N} + \frac{\left(x^k\right)^2}{N} \tag{3.15}$$

From (3.15), the next sample time at time step *k*+1 is:

$$\text{RMS}^2\left(x^{k+1}\right) = \frac{\left(x^{(k-N)+2}\right)^2}{N} + \frac{\left(x^{(k-N)+3}\right)^2}{N} + \cdots + \frac{\left(x^{k-2}\right)^2}{N} + \frac{\left(x^{k-1}\right)^2}{N} + \frac{\left(x^{k+1}\right)^2}{N} \tag{3.16}$$

Subtracting (3.15) from (3.16):

$$\text{RMS}^2\left(x^{k+1}\right) = \left(\text{RMS}^2\left(x^k\right) - \frac{\left(x^{(k-N)+1}\right)^2}{N}\right) + \frac{\left(x^{k+1}\right)^2}{N} \tag{3.17}$$

Taking the square-root of both sides:

$$\text{RMS}\left(x^{k+1}\right) = \sqrt{\text{RMS}^2\left(x^k\right) - \frac{\left(x^{(k-N)+1}\right)^2}{N} + \frac{\left(x^{k+1}\right)^2}{N}} \tag{3.18}$$

where:

$\mathrm{RMS}\left(x^{k+1}\right)$ = the RMS value at the present time step $k+1$

$\mathrm{RMS}^2\left(x^{k}\right)$ = the square of RMS value from the previous time step

x^{k} = the previous time step's sample

x^{k+1} = the present time step's sample

The notation used for an RMS current measurement (e.g., phase *a*) of protective device is illustrated with (3.19):

$$I_{aRMS}^{k+1}=\sqrt{\frac{-\left(i_a^{k+1-N}\right)^2}{N}+\left(I_{aRMS}^{k}\right)^2+\frac{\left(i_a^{k+1}\right)^2}{N}},\quad \text{where}\begin{pmatrix} i_a^{k+1-N}=0\\ \text{for }(k+1)<N\end{pmatrix}. \tag{3.19}$$

3.2.4 Formulation of Loop Currents for Electrical and Control Networks

The formulation approach in this work treats SPS models as purely ungrounded electrical networks; thus, datum nodes are not included despite implicit stray connections to the hull. To form the network equations of the form **A·x**=**b**, loop currents were chosen as variables. The choice of loop currents is due to three reasons: the first is that a formulation in loop currents as variables is suitable in the absence of datum nodes; the second is that there are generally less loop equations than node equations in power systems; and third, because the sparsity of loop resistance matrices when using meshes as the cycle basis is comparable to the nodal conductance matrix’s sparsity [91-92].

After the component models composing the electrical network are discretized, mesh current equations are used to obtain each model’s branch currents and terminal voltages. The interconnection of all components’ mesh equations results in a large interconnected system represented with non-planar loop current equations. The set of system-wide loop current equations is arranged in **A·x=b** form as given by (3.20), where $\mathbf{R}_{loop}^{k+1}$ is the time-varying loop resistance matrix of the system, $\mathbf{i}_{loop}^{k+1}$ is the vector of all loop currents, and $\mathbf{e}_{loop}^{k+1}$ is the vector of loop electromotive forces (EMFs). The EMFs are found as the contour sum of historical voltage sources in each loop.

A word on the notations of (3.20)-(3.21) is imperative. In (3.20), the vector $\mathbf{e}_{loop}^{k+1}$ contains only terms from the previous time step (i.e., historical sources due to inductors and capacitors); the notation $\mathbf{e}_{loop}^{k+1}$ is used over $\mathbf{e}_{\mathrm{loop}}^{k}$ because $\mathbf{e}_{\mathrm{loop}}^{k+1}$ represents the EMF impression at the *present* time step $k+1$, and not the EMF impression that was used at the *previous* time step k. Referring to (3.21), the coefficients in $\mathbf{R}_{loop}^{k+1}$ have upper-scripts *k*+1 to indicate that their values are time-varying and are valid during the present time step's solution. The coefficients in $\mathbf{R}_{loop}^{k+1}$ may be different during the next time step if a switch's state changes (e.g., faults are applied, protective devices operate, diodes commutate, and so on).

$$\mathbf{R}_{loop}^{k+1}\mathbf{i}_{loop}^{k+1} = \mathbf{e}_{loop}^{k+1} \tag{3.20}$$

$$\begin{bmatrix} R_{11}^{k+1} & R_{12}^{k+1} & \cdots & \cdots \\ R_{21}^{k+1} & R_{22}^{k+1} & \cdots & \cdots \\ \vdots & \vdots & \ddots & \cdots \\ \vdots & \vdots & \vdots & R_{\ell\ell}^{k+1} \end{bmatrix}_{\ell\times\ell} \begin{bmatrix} i_{\ell 1}^{k+1} \\ i_{\ell 2}^{k+1} \\ \vdots \\ i_{\ell\ell}^{k+1} \end{bmatrix}_{\ell\times 1} = \begin{bmatrix} e_{\ell 1}^{k+1} \\ e_{\ell 2}^{k+1} \\ \vdots \\ e_{\ell\ell}^{k+1} \end{bmatrix}_{\ell\times 1} \tag{3.21}$$

where:

$\ell =$ total number of loop current equations

$\ell i =$ the i^{th} loop current

$R_{ii}^{k+1} =$ contour sum of resistances in ℓi's path at time step $k+1$

$R_{ij}^{k+1} =$ resistance common to ℓi and ℓj at time step $k+1$

$k+1 =$ current simulation time step

$e_{\ell i}^{k+1} =$ contour voltage (EMF) sum in ℓi's path.

The non-zero structure of the symmetric positive-definite loop resistance matrix $\mathbf{R}_{loop}^{k+1}$ for a notional SPS model is shown in Fig. 3.2.2. The structure plot shows comparable sparsity to nodal conductance matrix. The dense square regions near the main diagonal are due to coupled loop currents at switchboard and load center capacitor loops (i.e., the right-side capacitor loop of the cable model shown in Fig. 2.4.10).

These dense regions are analogous to the situation (rare, and typically non-physical) of mutual inductances coupling dozens of branches in a nodal formulation [93]. The paths of the circulating currents were defined with this goal in mind. This dense condition is exploited during the partitioning approach by shoring the capacitors where said loop currents intersect, which results in a rapid depletion of the non-zero structure of $\mathbf{R}_{loop}^{k+1}$.

Rapid depletion of the non-zero structure of $\mathbf{R}_{loop}^{k+1}$ permits block-diagonalizing $\mathbf{R}_{loop}^{k+1}$ with minimal boundary equations. Keeping the number of boundary equations small implies tearing the least number of capacitor loops possible as will be shown later.

In section 3.5, it is shown that the computational cost per time step is proportional to the square of the number of capacitors torn (noted as r^2).

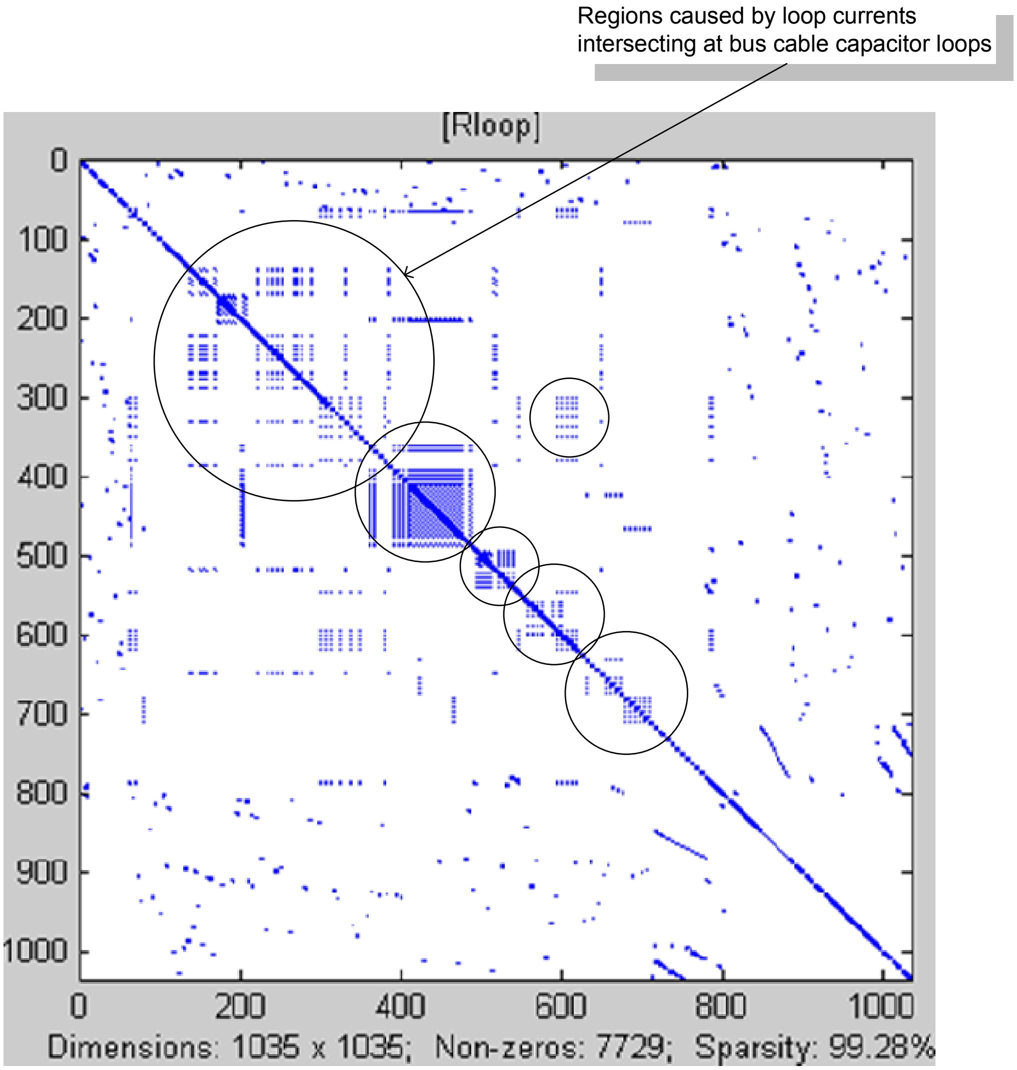


Fig. 3.2.2. Loop resistance matrix structure for an unpartioned AC-Radial SPS

After solving (3.21) at each time step all node voltages and branch currents can be found with (3.22) . Equation (3.22) states that the system's branch currents and node voltages are from the loop currents and the historical voltage sources. The discretized component models listed in Appendix A include expressions to find their terminal voltages and line current, which are of the form of (3.22). The solution of (3.22) using (3.23) is the same as the DAE output vector $\mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)$ introduced in (2.43), but obtained using a discretized loop current formulation approach instead of a DAE continuous formulation approach. A table summarizing the relation of the loop current solution to the DAE formulation's solution is given in Table III.1.

$$\mathbf{y}^{k+1} = \begin{bmatrix} \mathbf{i}_{branch}^{k+1} \\ \hdashline \mathbf{v}_{nodes}^{k+1} \end{bmatrix} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right) \tag{3.22}$$

$$\mathbf{i}_{branch}^{k+1} = f\left(\mathbf{i}_{loop}^{k+1}\right) \qquad \mathbf{v}_{nodes}^{k+1} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right) \tag{3.23}$$

where :

$\mathbf{y}^{k+1}$ = measurements of interest at time step $k+1$

$\mathbf{i}_{branch}^{k+1}$ = vector of all branch currents at time step $k+1$

$\mathbf{v}_{nodes}^{k+1}$ = vector of line-to-line voltages at every node at time step $k+1$

$\mathbf{f}$ = vector function of loop currents and historical sources.

The DAE output vector $\mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)$ is obtained by solving $\dot{\mathbf{x}} = f(\mathbf{x}, \mathbf{u}, t)$, $\mathbf{0} = g(\mathbf{x}, \mathbf{u}, t)$. The solution of $\mathbf{y}^{k+1} = \begin{bmatrix} \mathbf{i}_{branch}^{k+1} \\ \hdashline \mathbf{v}_{nodes}^{k+1} \end{bmatrix} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right)$, which is the same as $\mathbf{y} = h(\mathbf{x}, \mathbf{u}, t)$, is obtained by solving for the loop current vector $\mathbf{i}_{loop}^{k+1}$ in $\mathbf{R}_{loopi}^{k+1}\mathbf{i}_{loopi}^{k+1} = \mathbf{e}_{loopi}^{k+1}$.

TABLE III.1. RELATIONSHIP BETWEEN DAE AND LOOP CURRENT FORMULATIONS

	DAE Formulation	Loop Current Formulation
Equation Count	~3000	~1000
Equation(s) to Solve	$\dot{\mathbf{x}} = f(\mathbf{x},\mathbf{u},t)$ $\mathbf{0} = g(\mathbf{x},\mathbf{u},t)$	$\mathbf{R}_{loopi}^{k+1}\mathbf{i}_{loopi}^{k+1} = \mathbf{e}_{loopi}^{k+1}$
Output Variables	$\mathbf{y} = h(\mathbf{x},\mathbf{u},t)$	$\mathbf{y}^{k+1} = \begin{bmatrix} \mathbf{i}_{branch}^{k+1} \\ \hline \mathbf{v}_{nodes}^{k+1} \end{bmatrix} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right)$
Domain	Continous Time	Discrete Time

Power system discretization and the loop currents formulation was introduced in this section. The discretized component models with their inductors and capacitors (if any) replaced by the discretized equivalent circuits.

3.2.5 Electrical and Control Networks

To simulate a discretized SPS, the EMTP approach [5] is followed in this work, where an electrical network (EN) and a control network (CN) are defined as shown in Fig. 3.2.3. The EN is responsible for the solution of $\mathbf{R}_{loopi}^{k+1}\mathbf{i}_{loopi}^{k+1} = \mathbf{e}_{loopi}^{k+1}$, whereas the control network is responsible for the solution of $\mathbf{y}^{k+1} = \begin{bmatrix} \mathbf{i}_{branch}^{k+1} \\ \hline \mathbf{v}_{nodes}^{k+1} \end{bmatrix} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right)$.

The EN-CN solution is sequential, and is depictedin Fig. 3.2.4 [5]. The EN solution is found first and its results are passed to the CN. The CN uses the results from the EN to compute the voltages and current everywhere, solves machine controller equations, updates the historical sources of inductors and capacitors, updates $\mathbf{R}_{loop}^{k+1}$ (if necessary), and makes discrete RMS measurements. The state of the protective devices are based on the discretize RMS measurements, which are used to determine whether protective devices should operate (logic equations were introduced in (2.34), (2.35), and (2.40)). After the CN solution is complete, the simulation time is advanced and the EN solved again using the historical sources that were updated during the CN solution.

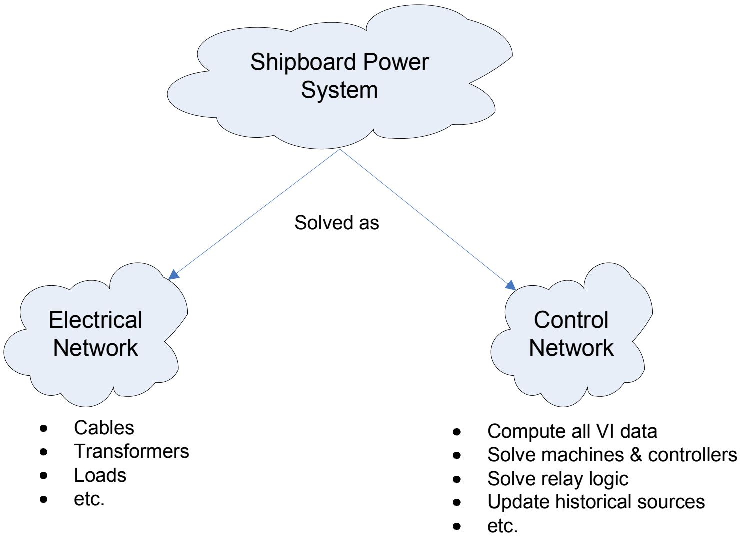


Fig. 3.2.3. Overview of electrical and control network

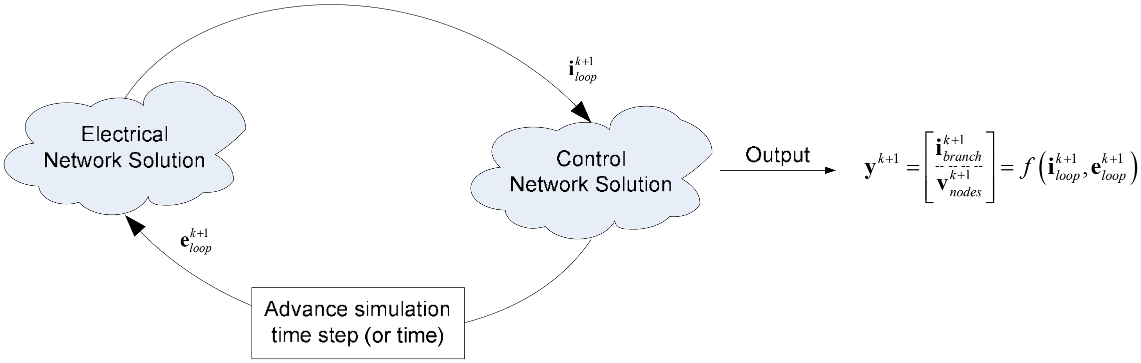

$\mathbf{i}_{loop}^{k+1}$
Electrical Network Solution
Control Network Solution
Output
$\mathbf{y}^{k+1} = \begin{bmatrix} \mathbf{i}_{branch}^{k+1} \\ \hdashline \mathbf{v}_{nodes}^{k+1} \end{bmatrix} = f\left(\mathbf{i}_{loop}^{k+1}, \mathbf{e}_{loop}^{k+1}\right)$
$\mathbf{e}_{loop}^{k+1}$
Advance simulation time step (or time)

Fig. 3.2.4. Solution of electrical and control networks [24]

A time-line illustration of Fig. 3.2.4 is given in Fig. 3.2.5. Starting with step 1 in Fig. 3.2.5, the EN is solved by finding $\mathbf{i}_{loop}^{k+1}$ in (3.20). After the loop currents are found, the CN computes (3.22) and other aforementioned operations shown as step 2 *before* advancing the time step. After the CN is solved the simulation time step is incremented in step 3 and the process is repeated throughout the entire simulation.

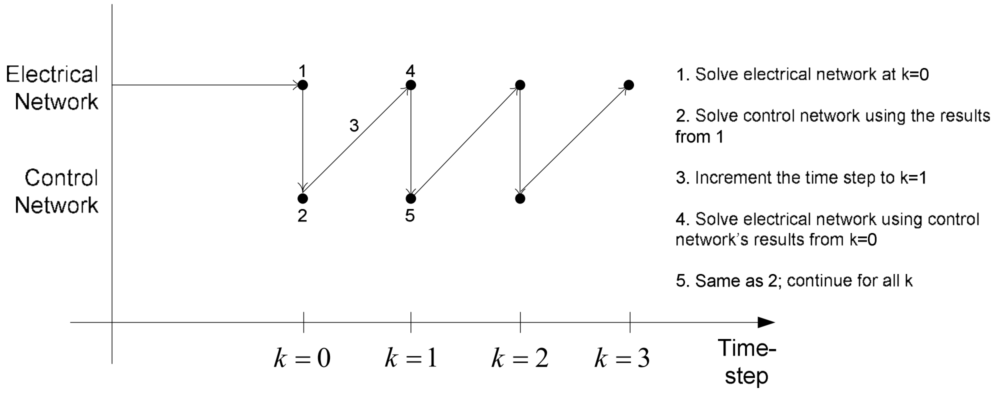

Electrical Network
Control Network
1
2
3
4
5
1. Solve electrical network at k=0
2. Solve control network using the results from 1
3. Increment the time step to k=1
4. Solve electrical network using control network's results from k=0
5. Same as 2; continue for all k
$k=0$
$k=1$
$k=2$
$k=3$
Time-step

Fig. 3.2.5. Time-line illustration of the electrical and control network interface [71]

The previous subsections presented the discretization (and formulation approach) used in this work, which is the first (out of three) stages that conforms the solution methodology. The following section presents the partitioning approach followed by the simulation approach, which is presented last.

3.3 ELECTRICAL NETWORK PARTITIONING AND GRAPH BALANCING

An approach based on diakoptics [4],[59],[94-95] is used to tear the electrical network of an AC-Radial SPS at selected capacitor loops. To determine which capacitors to tear in a manner that the subsystems are computationally balanced, graph theory is used. Using graph theory a representative SPS graph was created and partitioned first with mincut [3] algorithm. The mincut algorithm produces an initial graph segregation which serves as the initial condition before the balancing heuristics begin.

The heuristic balancing algorithm was developed to equally distribute the weights of the weighted vertices across the graph partitions. The vertices were assigned weights based on the computational effort [96] of the component they represent, which are used to determine if the graph partitions are balanced. After balancing the graph partitions, the edges interfacing any two partitions indicate which capacitors should be torn.

The partitioning approach in this work tears capacitor loops on three-phase cables to create SPS subsystems. To determine which cables to tear (i.e., 100s of cables exist on SPSs), graph theory is used. A representative graph of an SPS is used to partition and balance graph partitions. The resulting graph edge cut corresponds to the capacitor loops to be torn.

When the capacitor loops that are going to be torn are known, the cable models including said capacitor loops are replaced with a cable model that has said capacitors shorted; shorting out said capacitors permits obtaining a block-diagonal structure from the loop resistance matrix. The block-diagonal form of the loop resistance matrix can be solved as subsystems on a multicore computer. The remaining of this section is organized as follows:

1. Diakoptics and Capacitor Tearing
2. Graph Theory
    a. Weight assignment
    b. Graph creation
    c. Graph partitioning
    d. Partition balancing
    e. Capacitor Tearing

3.3.1 Diakoptics Theory and Capacitor Tearing

Diakoptics theory was introduced using general matrix notation **A·x**=**b** in (2.9)-(2.12) (section 2.3.3). In this section, diakoptics is re-derived using the variables and notation pertinent to this work. It is noted that there are two types of diakoptics-based tearing: *traversal* tearing and *longitudinal* tearing [97]. Traversal tearing is used when systems are formulated in node voltages as variables. Traversal tearing tears two *radially* attached networks by removing tie-lines (i.e., transmission lines interconnecting two geographical areas), solving each subsystem's node voltages, and injecting the tie-line currents back into each subsystem. Longitudinal tearing is used when systems are formulated using loop currents as variables. Longitudinal tearing tears two *adjacently* attached networks by shorting tie-lines, solving each subsystem's loop currents, and impressing the tie-line voltages back into each subsystem. The partitioning approach presented next makes use of longitudinal tearing, and is applied to cable capacitor loops.

The unpartitioned network's loop current equations, formerly introduced in (3.20), are repeated in (3.24).

$$\mathbf{R}_{loop}^{k+1}\mathbf{i}_{loop}^{k+1}=\mathbf{e}_{loop}^{k+1} \tag{3.24}$$

Removing the *k*+1 (redundant) notation for clarity:

$$\mathbf{R}_{loop}\mathbf{i}_{loop}=\mathbf{e}_{loop} \tag{3.25}$$

where:

$\ell =$ total number of loop currents

$\mathbf{R}_{loop} = \ell \times \ell$ loop resistance matrix (sparse, symmetric, positive-definite)

$$\mathbf{R}_{\ell oop}\left(i,j\right) \rightarrow \begin{cases} R_{ii}\text{:the sum of resistances in loop } i \\ R_{ij}\text{:the resistance common to } \ell_i \text{ and } \ell_j \end{cases}$$

$\mathbf{i}_{loop} = \ell \times 1$ vector of loop currents

$\mathbf{e}_{loop} = \ell \times 1$ vector of loop EMFs.

Decomposing (3.25) as the sum of two square matrices:

$$\left(\mathbf{R}_{loop}^{subs} + \mathbf{R}_{loop}^{off}\right)\mathbf{i}_{loop} = \mathbf{e}_{loop} \tag{3.26}$$

where:

$\mathbf{R}_{loop}^{subs} = \ell \times \ell$ block-diagonal matrix of subsystem loop resistance matrices

$$=\text{diag}\left(\mathbf{R}_{loop1}, \cdots, \mathbf{R}_{loopp}\right)$$

$$= \begin{bmatrix} \mathbf{R}_{loop1} & & & \\ & \mathbf{R}_{loop2} & & \\ & & \ddots & \\ & & & \mathbf{R}_{loopp} \end{bmatrix}$$

$\mathbf{R}_{loop}^{off} = \ell \times \ell$ matrix with the off-diagonals of $\mathbf{R}_{loop}$, where $R_{loop}^{off}\left(i,i\right) > 0 \ \forall \ell_i$.

At switchboards and load centers (i.e., buses), source cables supply components connected to said bus. As a result, many loop currents emanate from the *same* cable, a situation which is judiciously set up and exploited in this work. If many loop currents are incident at the same cable, the loop currents can be defined to circulate through the *same* boundary capacitors C_{ab} and C_{bc}. There is a deliberate intention in this approach; by defining all loop currents incidence at the *same* two capacitors, the loop resistance matrix exhibits dense areas due to the loop current couplings. To illustrate this situation, a generalized capacitor loop (reminiscent of a bus capacitor loop) is shown in Fig. 3.3.1. Fig. 3.3.1 shows how various ab and bc loop currents can be incident at the same two capacitors C_{ab} and C_{bc}, respectively. This situation causes the dense regions in $\mathbf{R}_{loopi}^{k+1}$ shown in Fig. 3.2.2, which off-diagonals are repeated values of the same discretized resistances for C_{ab} and C_{bc}, respectively.

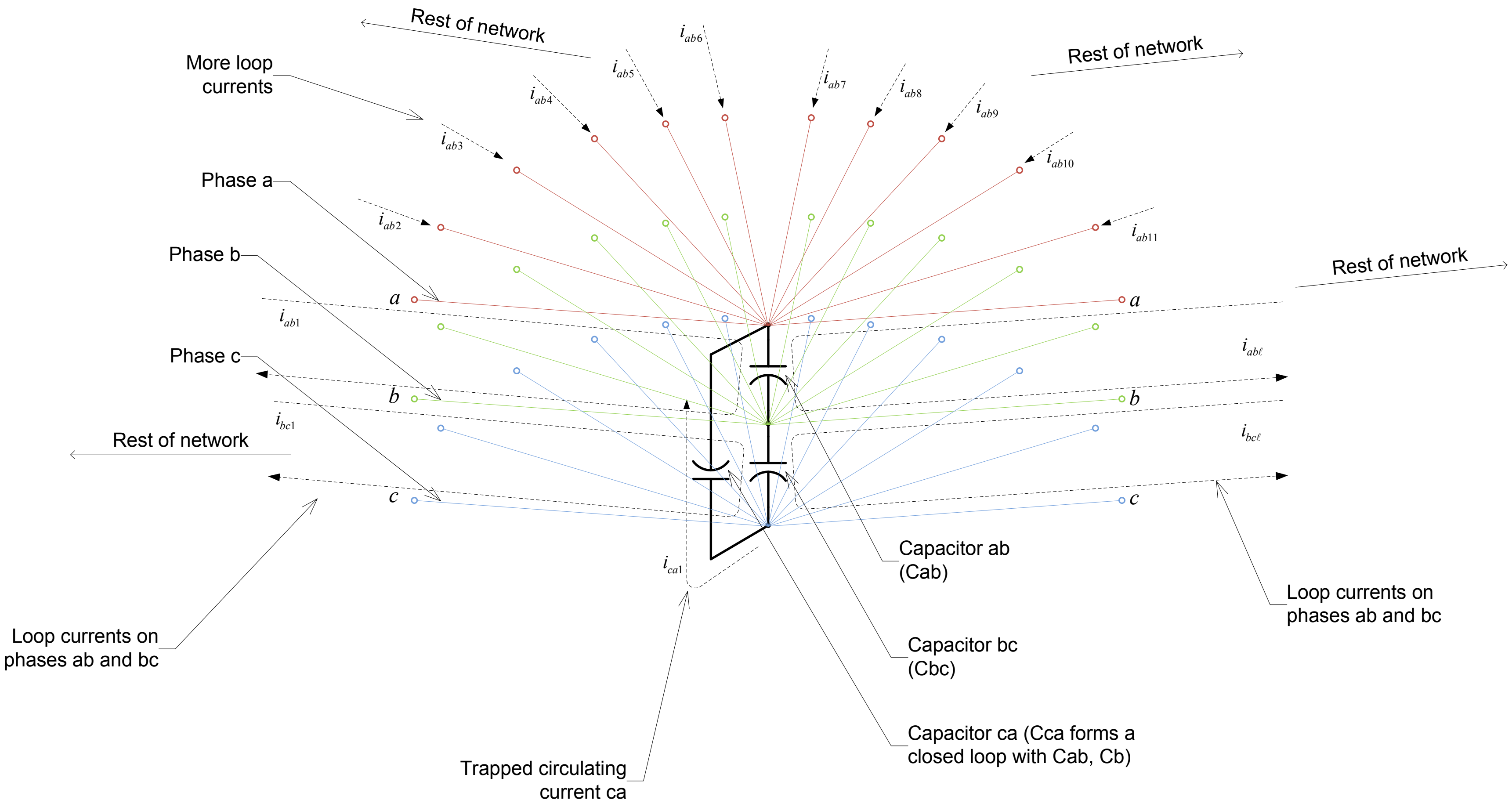


Fig. 3.3.1. Generalized cable capacitor loop (at switchboards and load centers)

The situation depicted in Fig. 3.3.1 suggests that the entries in $\mathbf{R}_{loop}^{off}$ consist (mainly) of the same bus capacitor discretized resistances. It is noted, however, that not *all* values in $\mathbf{R}_{loop}^{off}$ pertain to bus capacitor loops. Other values (lesser in number) pertain to loop current intersections elsewhere in the system. Since $\mathbf{R}_{loop}^{off}$ has only a few *unique* entries, said entries can be arranged in a diagonal matrix $\mathbf{R}_C$ and expressed as the tensor transformation[53],[98] in (3.27):

$$\mathbf{R}_{loop}^{off} = \mathbf{D}_{\ell \times r} \mathbf{R}_C \mathbf{D}_{r \times \ell}^{\mathrm{T}} \tag{3.27}$$

where:

$\ell =$ total number of loop currents in the electrical network

$r =$ total number of boundary capacitors $\left(r \ll \ell\right)$

$\mathbf{R}_C$ $= r \times r$ diagonal matrix of boundary capacitor resistances $\left(R_C\left(i,i\right) \in \mathbf{R}_{loop}^{off}\right)$

$\mathbf{D}$ $= \ell \times r$ transformation tensor:

$$\mathbf{D}\left(i,j\right) \rightarrow \begin{cases} = 1, & \text{if the } i^{\text{th}} \text{ loop current is in the same direction as} \\ & \text{the } j^{\text{th}} \text{ capacitor's voltage drop} \\ = -1, & \text{if the } i^{\text{th}} \text{ loop current is opposite in direction to} \\ & \text{the } j^{\text{th}} \text{ capacitor's voltage drop} \\ = 0, & \text{if the } i^{\text{th}} \text{ loop current does not traverse the } j^{\text{th}} \text{ capacitor.} \end{cases}$$

Substituting (3.27) in (3.26) results in:

$$\left(\mathbf{R}_{loop}^{subs} + \mathbf{D} \cdot \mathbf{R}_C \mathbf{D}^{\mathrm{T}}\right) \mathbf{i}_{loop} = \mathbf{e}_{loop} \tag{3.28}$$

$$\mathbf{R}_{loop}^{subs}\mathbf{i}_{loop}+\mathbf{D}\cdot\mathbf{R}_{C}\mathbf{D}^{\mathrm{T}}\mathbf{i}_{loop}=\mathbf{e}_{loop} \tag{3.29}$$

Referring to the discretized capacitor model in Fig. 3.2.1, the term $\mathbf{R}_{C}\mathbf{D}^{\mathrm{T}}\mathbf{i}_{loop}$ on the right of (3.29) corresponds to resistive voltage drops across $\{R_{Cab}, R_{Cbc}\}$ of all boundary capacitors $\{C_{ab}, C_{bc}\}$. The matrix $\mathbf{R}_{C}$ is a diagonal matrix of discretized boundary capacitor resistances, and the term $\mathbf{D}^{\mathrm{T}}\mathbf{i}_{loop}$ is the current (i.e., net loop current sum) through each capacitor. Referring to Fig. 3.2.1, the resistive voltage drop $\mathbf{R}_{C}\mathbf{D}^{\mathrm{T}}\mathbf{i}_{loop}$ can be expressed as the difference between the capacitors' across voltage and historical source as given by (3.30). Substitution of (3.30) into (3.29) results in (3.31).

$$\mathbf{R}_{C}\mathbf{D}^{\mathrm{T}}\mathbf{i}_{loop}=\mathbf{v}_{C}-\mathbf{hist}_{C} \tag{3.30}$$

$$\mathbf{R}_{loop}^{subs}\mathbf{i}_{loop}+\mathbf{D}\left(\mathbf{v}_{C}-\mathbf{hist}_{C}\right)=\mathbf{e}_{loop} \tag{3.31}$$

where:

$\mathbf{hist}_{C}=r\times 1$ vector of boundary (torn) capacitor historical sources

$\mathbf{v}_{C}=r\times 1$ vector of boundary (torn) capacitor across voltages.

Solving for $\mathbf{i}_{loop}$ in (3.31):

$$\mathbf{i}_{loop}=\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop}-\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\left(\mathbf{v}_{C}-\mathbf{hist}_{C}\right) \tag{3.32}$$

Substituting (3.32) in (3.30):

$$\mathbf{R}_{C}\mathbf{D}^{\mathrm{T}}\left(\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop}-\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\left(\mathbf{v}_{C}-\mathbf{hist}_{C}\right)\right)=\mathbf{v}_{C}-\mathbf{hist}_{C} \tag{3.33}$$

Solving for $\mathbf{v}_C$:

$$\mathbf{v}_C - \mathbf{hist}_C = \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop} - \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\left(\mathbf{v}_C - \mathbf{hist}_C\right) \quad (3.34)$$

$$\left(\mathbf{v}_C - \mathbf{hist}_C\right) + \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\left(\mathbf{v}_C - \mathbf{hist}_C\right) = \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop} \quad (3.35)$$

$$\left(\mathbf{I} + \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\right)\left(\mathbf{v}_C - \mathbf{hist}_C\right) = \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop} \quad (3.36)$$

$$\mathbf{v}_C = \left(\mathbf{I} + \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\right)^{-1}\left(\mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop}\right) + \mathbf{hist}_C \quad (3.37)$$

The sequential solution of (3.32) and (3.37) (repeated as (3.38)) is the solution approach used in this work to solve the electrical network as subsystems. In vector form, (3.38) is given by (3.39):

$$\begin{cases} \mathbf{i}_{loop} = \left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop} - \left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\cdot\mathbf{v}_C \\ \mathbf{v}_C = \underbrace{\left(\mathbf{I}_r + \mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{D}\right)^{-1}}_{\boldsymbol{\alpha}}\underbrace{\left(\mathbf{R}_C\mathbf{D}^{\mathrm{T}}\left(\mathbf{R}_{loop}^{subs}\right)^{-1}\mathbf{e}_{loop}\right)}_{\boldsymbol{\beta}} + \mathbf{hist}_C \end{cases} \quad (3.38)$$

$$\begin{bmatrix} \mathbf{i}_{loop1} \\ \mathbf{i}_{loop2} \\ \vdots \\ \mathbf{i}_{loopp} \end{bmatrix} = \underbrace{\begin{bmatrix} \mathbf{R}_{loop1}^{-1}\mathbf{e}_{loop1} \\ \mathbf{R}_{loop2}^{-1}\mathbf{e}_{loop2} \\ \vdots \\ \mathbf{R}_{loopp}^{-1}\mathbf{e}_{loopp} \end{bmatrix}}_{\text{subsystem solutions}} - \underbrace{\begin{bmatrix} \mathbf{R}_{loop1}^{-1}\mathbf{D}_1 \\ \mathbf{R}_{loop2}^{-1}\mathbf{D}_2 \\ \vdots \\ \mathbf{R}_{loopp}^{-1}\mathbf{D}_p \end{bmatrix}\overbrace{\mathbf{v}_C}^{\substack{\text{boundary} \\ \text{conditions}}}}_{\text{patch}} \quad (3.39)$$

Re-introducing *k*+1 notation for (3.38) and (3.39) results in (3.40)

$$\begin{array}{c}\text{Solved}\\ \text{using}\\ p\ \text{threads}\end{array}\left\{\begin{array}{l}
\begin{bmatrix} \mathbf{i}^{k+1}_{loop1} \\ \mathbf{i}^{k+1}_{loop2} \\ \vdots \\ \mathbf{i}^{k+1}_{loopp} \end{bmatrix} = \underbrace{\begin{bmatrix} \left(\mathbf{R}^{k+1}_{loop1}\right)^{-1}\mathbf{e}^{k+1}_{loop1} \\ \left(\mathbf{R}^{k+1}_{loop2}\right)^{-1}\mathbf{e}^{k+1}_{loop2} \\ \vdots \\ \left(\mathbf{R}^{k+1}_{loopp}\right)^{-1}\mathbf{e}^{k+1}_{loopp} \end{bmatrix}}_{\substack{\text{step 1:}\\ \text{subsystem solutions}}} - \underbrace{\begin{bmatrix} \left(\mathbf{R}^{k+1}_{loop1}\right)^{-1}\mathbf{D}_1 \\ \left(\mathbf{R}^{k+1}_{loop2}\right)^{-1}\mathbf{D}_2 \\ \vdots \\ \left(\mathbf{R}^{k+1}_{loopp}\right)^{-1}\mathbf{D}_p \end{bmatrix} \underbrace{\mathbf{v}^{k+1}_{C}}_{\substack{\text{step 2: boundary}\\ \text{conditions}}}}_{\text{step 3: patch}} \\
\\
\mathbf{v}^{k+1}_{C} = \boldsymbol{\alpha}^{-1}\boldsymbol{\beta}^{k+1} + \mathbf{hist}^{k+1}_{C} \\
\quad \boldsymbol{\alpha} = \mathbf{I}_r + \sum_{i=1}^{p}\left(\mathbf{D}_i^{\mathrm{T}}\left(\mathbf{R}^{k+1}_{loopi}\right)^{-1}\mathbf{D}_i\right) \qquad \left(\text{constant matrix}\right) \\
\boldsymbol{\beta}^{k+1} = \sum_{i=1}^{p}\mathbf{D}_i^{\mathrm{T}}\underbrace{\left(\mathbf{R}^{k+1}_{loopi}\right)^{-1}\mathbf{e}^{k+1}_{loopi}}_{\text{from step 1}} \qquad \begin{pmatrix}\text{vector updated at}\\ \text{every time step}\end{pmatrix}
\end{array}\right. \tag{3.40}$$

The 2nd term on the RHS atop (3.40) is called the *patch;* its computation becomes increasingly burdensome as p increases. When p increases, computing $\mathbf{v}^{k+1}_{C}$ governs the performance of the partitioning approach. The capacitor tearing partitioning approach creates subsystems by removing off-diagonals from the loop resistance matrix, but mainly those off-diagonal resistance values intentionally defined to exist as off-diagonal values. That is, the bus capacitor loop currents were intentionally defined to create dense couplings in the loop resistance matrix because it was known in advance that those resistance values would be removed (torn).

The three-phase cable model used in this work is shown in Fig. 3.3.2, which has capacitor loops on each side. In this work, only the right side capacitor loops are torn because they are on the side of bus nodes (i.e., a bus node is always immediately to the right of a cable). In physical terms, removing off-diagonals from $\mathbf{R}_{loop}^{k+1}$ is equivalent to replacing boundary capacitors $\{C_{ab},C_{bc}\}$with short-circuits. Consider the discretization of a cable's capacitor loop is shown in Fig. 3.3.3, where everything to the left-and-right is obfuscated. Replacing $\{C_{ab},C_{bc}\}$with short circuits results in the *new* cable model shown in Fig. 3.3.4.-Fig. 3.3.5 Where two or more subsystems interface, the cable to the left of said interface is *replaced* with the cable in Fig. 3.3.4.-Fig. 3.3.5. By interconnecting the meshes of all components, except those meshes adjacent to boundary cables, makes the resulting loop resistance block-diagonal and is how $\mathbf{R}_{loop}^{subs}$ is obtained.

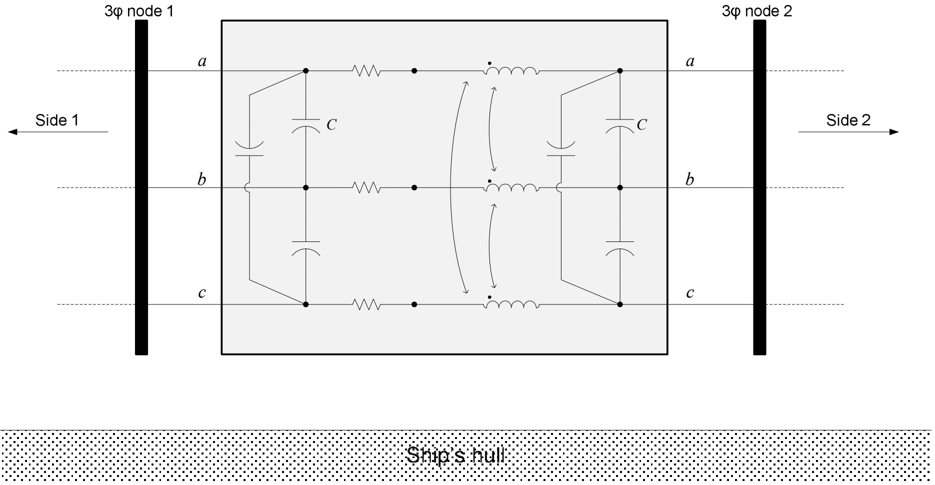


Fig. 3.3.2. Three-phase cable model

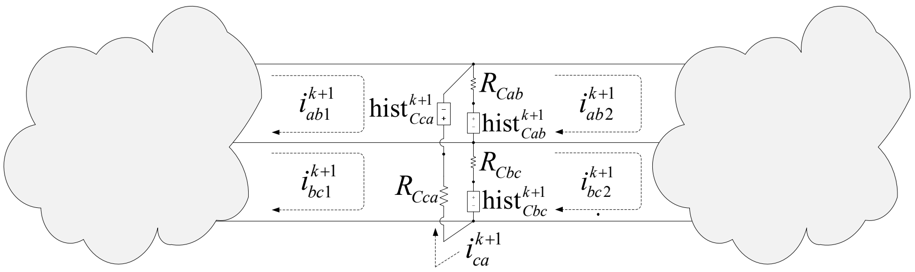


Fig. 3.3.3. A discretized capacitor loop

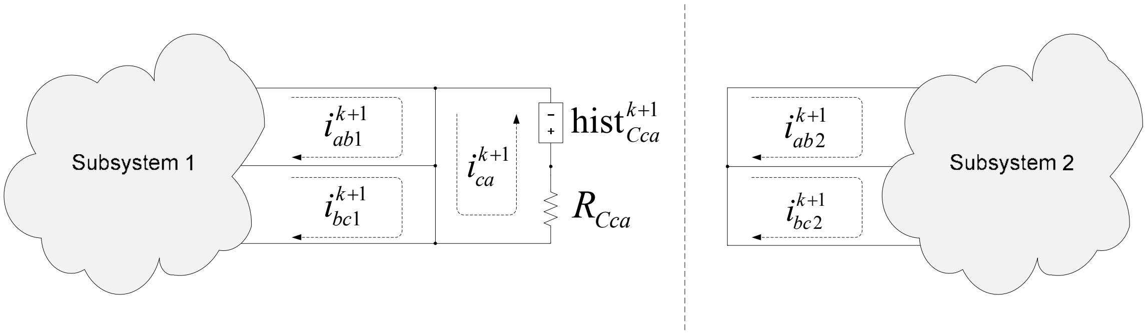
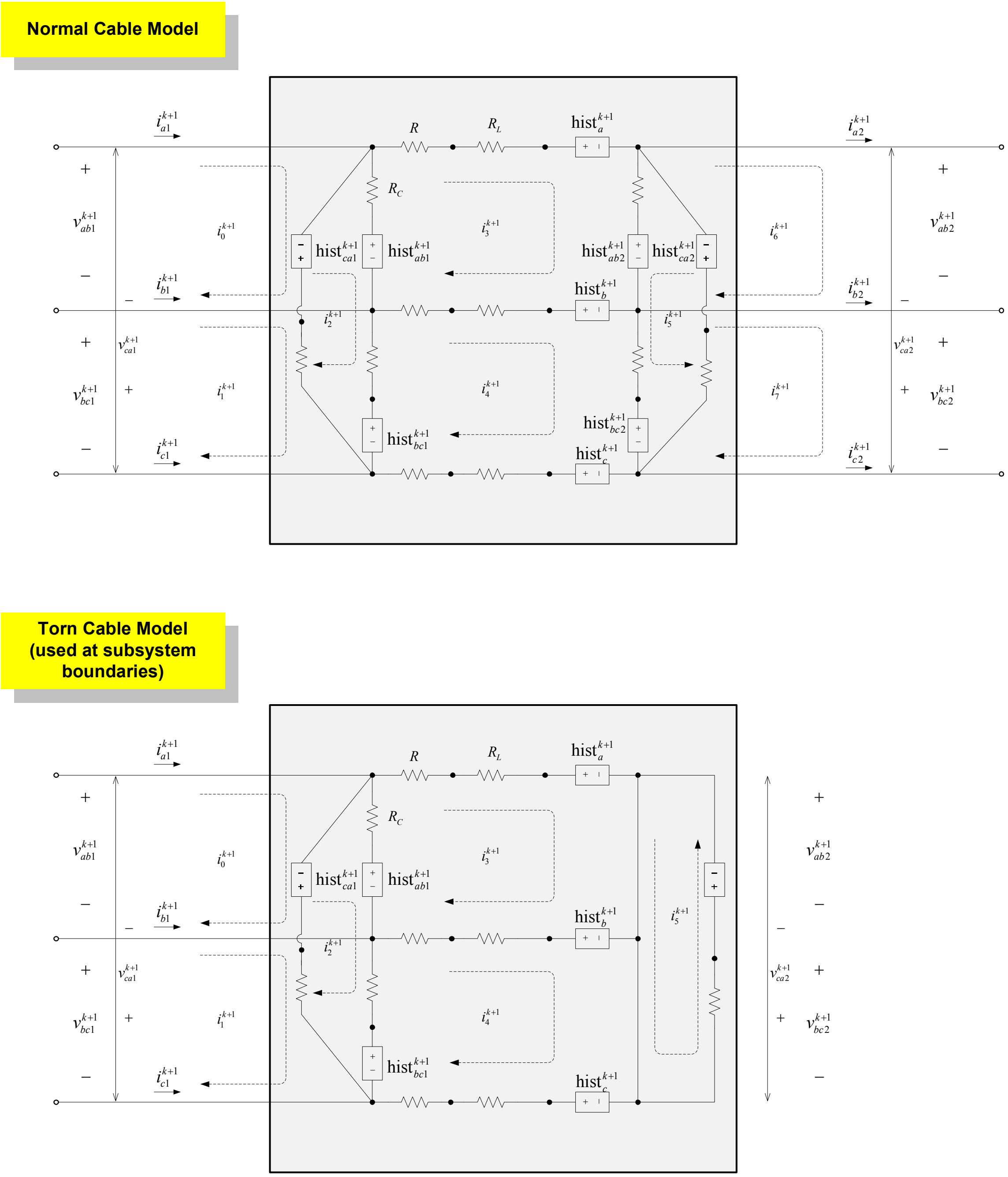


Fig. 3.3.4. Torn cable forms two subsystems



Normal Cable Model

Torn Cable Model (used at subsystem boundaries)

Fig. 3.3.5. Normal and torn cable model (replaced at boundaries)

This subsection presented the partitioning approach of tearing cable capacitor loops. By tearing two of three capacitors in a capacitor loop, two subsystems are created: subsystem 1 to the left and subsystem 2 to the right of a capacitor loop. To automate the process of tearing (i.e., to decide upon how many partitions and where to tear), graph theory is used. Each component model is represented by a weighted vertex in a SPS representative a graph. Each vertex is assigned a weight based on the estimated computational requirement of each component model. The details of how each component model is assigned a weight is presented next.

3.3.2 Flop Computations for Graph Vertices

A common measure of computer work is the floating-point arithmetic operation (flop) [45],[99],[96], and is used here to estimate the computational effort imposed by each component model. A flop is defined as a computer operation requiring floating-point arithmetic, such as a sum, subtraction, multiplication, or a division. The number of flops required to solve a component's electrical and control network equations is used as the component's weight when represented by a graph vertex. In the next subsections, the algebraic operations that were used to determine the vertex weights are presented.

3.3.2.1 Flops for Updating Inductor and Capacitor Historical Terms

Updating inductor and capacitor historical terms is the most frequently repeated operation. The historical terms for inductors and capacitors were presented in (3.6)-(3.7), and are repeated in (3.41)-(3.42) for convenience.

$$\text{hist}_L^{k+1} = \overbrace{\overbrace{\frac{\overbrace{\gamma-1}^{\text{2 flops}}}{\gamma} v_L^k}^{\text{1 flops}} - \overbrace{\frac{\overbrace{L}^{\text{2 flops}}}{\Delta t \cdot \gamma} i_L^k}^{\text{1 flops}}}^{\text{1 flops}} \tag{3.41}$$

$$\text{hist}_C^{k+1} = \overbrace{v_C^k + \overbrace{\frac{\overbrace{\Delta t\left(1-\gamma\right)}^{\text{3 flops}}}{C} i_C^k}^{\text{1 flops}}}^{\text{1 flops}} \tag{3.42}$$

The number of flops to update hist_L^{k+1} is $f_L = 7$ flops, and to update hist_C^{k+1} is $f_C = 5$ flops, which were obtained by counting the number of additions, subtractions, multiplications, and divisions as shown in (3.41)-(3.42).

3.3.2.2 Flops for Matrix Algebra

Consider the product of two rectangular matrices $\mathbf{G}$ and $\mathbf{D}$ given in (3.43).

$$\mathbf{G}_{m\times n}\mathbf{D}_{n\times k} = \begin{bmatrix} g_{11} & g_{12} & g_{13} & \cdots & g_{1n} \\ g_{21} & g_{22} & g_{23} & \cdots & g_{2n} \\ g_{31} & g_{32} & g_{33} & \cdots & g_{3n} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ g_{m1} & g_{m2} & g_{m3} & \cdots & g_{mn} \end{bmatrix}_{m\times n} \begin{bmatrix} d_{11} & d_{12} & d_{13} & \cdots & d_{1k} \\ d_{21} & d_{22} & d_{23} & \cdots & d_{2k} \\ d_{31} & d_{32} & d_{33} & \cdots & d_{3k} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ d_{n1} & d_{n2} & d_{n3} & \cdots & d_{nk} \end{bmatrix}_{n\times k} \tag{3.43}$$

The computational effort of the dot product between the first row of $\mathbf{G}$ and the first column of $\mathbf{D}$ is given by (3.44), where the multiplications and summations require:

$$g_{11}d_{11} + g_{12}d_{21} + g_{13}d_{31} + \ldots + g_{1n}d_{n1} \leftarrow \begin{cases} n \text{ multiplications} + \\ \underline{\quad n-1 \text{ summations} \quad} \\ = 2n-1 \text{ flops} \end{cases} \tag{3.44}$$

Since **D** has k columns, (3.44) is repeated k times for each of the m rows of **G** resulting in (3.45), where $f_{rect \cdot rect}^{mult}$ is the number of flops required to multiply two full rectangular matrices.

$$f_{rect \cdot rect}^{mult} = m(2n-1)k \tag{3.45}$$

If **G** and **D** in (3.43) are both square matrices of dimension n, then m=n=k and (3.45) becomes (3.46), where $f_{sq \cdot sq}^{mult}$ is the number of flops required to multiply to full square matrices.

$$f_{sq \cdot sq}^{mult} = n(2n-1)n = 2n^3 - n^2 \tag{3.46}$$

If $\mathbf{G}$ remains the same as defined in (3.43), and $\mathbf{D}$ is a $n \times 1$ vector, setting k=1 in (3.45) reduces to (3.47), where $f_{rect \cdot vct}^{mult}$ is the number of flops required for a matrix-vector multiplication.

$$f_{rect \cdot vct}^{mult} = m(2n-1) = 2mn - m \tag{3.47}$$

The sum of two full $m \times n$ rectangular matrices $\mathbf{G}$ and $\mathbf{D}$ requires $f_{rect+rect}^{sum}$ flops as given by (3.48).

$$f_{rect+rect}^{sum} = m \cdot n \tag{3.48}$$

If $\mathbf{G}$ and $\mathbf{D}$ are both vectors of dimensions $n\times 1$, the vector sum operation has $f^{sum}_{vct+vct}$ number of flops as given by (3.49).

$$f^{sum}_{vct+vct} = n \tag{3.49}$$

3.3.2.3 Flops for Solving State-Variable Equations

The discretization (and definition of terms) for a set of state-variable equations were given in (3.8)-(3.11) and were repeated in (3.50) for convenience. The number of flops required to find $\mathbf{x}^{k+1}$ and $\mathbf{y}^{k+1}$ are derived in (3.51)-(3.52).

$$\begin{cases} \mathbf{x}^{k+1} = \mathbf{M}\cdot\mathbf{x}^{k} + \mathbf{N}\left(\mathbf{u}^{k+1}+\mathbf{u}^{k}\right) \\ \mathbf{y}^{k+1} = \mathbf{C}\cdot\mathbf{x}^{k+1} + \mathbf{D}\cdot\mathbf{u}^{k+1} \end{cases} \tag{3.50}$$

$$\mathbf{x}^{k+1}_{n\times1} = \overbrace{\overbrace{\mathbf{M}_{m\times n}\cdot\mathbf{x}^{k}_{n\times1}}^{f^{mult}_{rect\cdot vct}=2mn-m} + \overbrace{\mathbf{N}_{m\times n}\overbrace{\left(\mathbf{u}^{k+1}_{n\times1}+\mathbf{u}^{k}_{n\times1}\right)}^{f^{sum}_{vct+vct}=n}}^{f^{mult}_{rect\cdot vct}=2mn-m}}^{f^{sum}_{vct+vct}=n} \quad \text{where } m=n \tag{3.51}$$

$$\mathbf{y}^{k+1}_{n\times1} = \overbrace{\mathbf{C}_{m\times n}\mathbf{x}^{k+1}_{n\times1}}^{f^{mult}_{rect\cdot vct}=2mn-m} + \overbrace{\mathbf{D}_{m\times n}\mathbf{u}^{k+1}_{n\times1}}^{f^{mult}_{rect\cdot vct}=2mn-m} \qquad \text{where } m=n \tag{3.52}$$

The number of flops required to find $\mathbf{x}^{k+1}$ is $2f^{sum}_{vct+vct} + 2f^{mult}_{rect\cdot vct}$, and the number of flops required to find $\mathbf{y}^{k+1}$ is $2f^{mult}_{rect\cdot vct}$. The combined number of flops required to find the state-variable vector $\mathbf{x}^{k+1}$ and the output vector $\mathbf{y}^{k+1}$ is given in (3.53), where *n* is the number of the state-variable equations.

$$\begin{aligned} f_{statespace} &= 2f^{sum}_{vct+vct} + 2f^{mult}_{rect\cdot vct} + 2f^{mult}_{rect\cdot vct} \\ &= 2f^{sum}_{vct+vct} + 4f^{mult}_{rect\cdot vct} \\ &= 2n + 4\left(2mn - m\right) \\ &= 8mn + 2n - 4m \\ &= 8n^2 - 2n \qquad \left(\text{for } m = n\right) \end{aligned} \tag{3.53}$$

3.3.2.4 Flops to obtain an RMS Measurement

$$\mathrm{RMS}\left(x^{k+1}\right) = \overbrace{\sqrt{\overbrace{\overbrace{\left(\mathrm{RMS}^2\left(x^k\right) - \frac{\left(x^{(k-N)+1}\right)^2}{N}\right)}^{\text{1 flop}} + \overbrace{\frac{\left(x^{k+1}\right)^2}{N}}^{\text{2 flops}}}^{\text{1 flop}}}}^{\text{1 flop}} \tag{3.54}$$

where:

$\mathrm{RMS}\left(x^{k+1}\right)$ = the RMS measurement computed at the present time step $k+1$
$\mathrm{RMS}\left(x^{k}\right)$ = the RMS measurement made at the previous time step k
x^k = the signal sample from N time steps ago
x^{k+1} = the signal sample at the present time step
N = the number of samples per RMS measurement.

Equation (3.18) is a recursive (and effective) way to obtain an RMS value. The first term under the square-root only requires one subtraction since the term subtracted from $\mathrm{RMS}^2\left(x^k\right)$ is already known. The number of flops f_{RMS} required to (recursively) make an RMS measurement is given by (3.55).

$$f_{RMS} = \overbrace{1}^{\substack{\text{Number of} \\ \text{negations}}} + \overbrace{3}^{\substack{\text{Number of} \\ \text{squared terms}}} + \overbrace{2}^{\substack{\text{Number of} \\ \text{additions}}} + \overbrace{2}^{\substack{\text{Number of} \\ \text{divisions by } N}} + \overbrace{1}^{\substack{\text{Number of} \\ \text{square-roots}}} = 9 \tag{3.55}$$

Table III.2 summarizes the flop-counts introduced in this section. Using Table III.2, the vertex weights of the representative graph were determined, which play an important role in determining to what partition a components belongs to.

TABLE III.2. SUMMARY OF COMMON FLOP OPERATIONS

Description of Operations	Numbers of Flops
Update inductor historical term	$f_L = 7$
Update capacitor historical term	$f_C = 5$
Multiplication of m x n matrices	$f_{rect\cdot rect}^{mult} = m\left(2n-1\right)k$
Multiplication of n x n matrices	$f_{sq\cdot sq}^{mult} = 2n^3 - n^2$
Multiplication of m x n matrix & n x1 vector	$f_{rect\cdot vct}^{mult} = 2mn - m$
Matrix sum of m x n matrices	$f_{rect+rect}^{sum} = m \cdot n$
Sum of n x1 vectors	$f_{vct+vct}^{sum} = n$
Solution of n th order state-variable equations	$f_{statespace} = 8n^2 - 2n$
Computation of an RMS value	$f_{RMS} = 9$

Table III.5 summarizes the weights for each component model based on the flop-counts listed in Table III.2. The number of flops required by each component is given as the sum of its electrical network (EN) and control network (CN) equations examined earlier. To illustrate how the component weights were determined, the weight calculation for a discretized three-phase cable is given in Table III.3.

TABLE III.3. EXAMPLE OF WEIGHT CALCULATION FOR A THREE-PHASE CABLE

Network	Description of Operation(s)	Arithmetic	Number of Flops
Electrical Network (EN)	Inverse of mesh matrix times right-hand-side eloop vector	fmult/rect.vect = 2n^2-n with n=8	120
	Compute inductor La current	iLa=i3	0
	Compute inductor Lb current	iLb=i4-i3	1
	Compute inductor Lc current	iLc=-i4	1
	Compute inductor La voltage	vLa=iLa*Ra+histLa	2
	Compute inductor Lb voltage	vLb=iLb*Rb+histLb	2
	Compute inductor Lc voltage	vLc=iLc*Rc+histLc	2
	Compute capacitor Cab1 current	iCab1=i0+i2-i3	2
	Compute capacitor Cbc1 current	iCbc1=i1+i2-i4	2
	Compute capacitor Cca1 current	iCca1=i2	0
	Compute capacitor Cab1 voltage	vCab1=iCab1*RCab1+histCab1	2
	Compute capacitor Cbc1 voltage	vCbc1=iCbc1*RCbc1+histCbc1	2
	Compute capacitor Cca1 voltage	vCca1=iCca1*RCca1+histCca1	2
	Compute capacitor Cab2 current	iCab2=i3+i5-i6	2
	Compute capacitor Cbc2 current	iCbc2=i4+i5-i7	2
	Compute capacitor Cca2 current	iCca2=i5	0
	Compute capacitor Cab2 voltage	vCab2=iCab2*RCab2+histCab2	2
	Compute capacitor Cbc2 voltage	vCbc2=iCbc2*RCbc2+histCbc2	2
	Compute capacitor Cca2 voltage	vCca2=iCca2*RCca2+histCca2	2
		Subtotal	148

Network	Description of Operation(s)	Arithmetic	Number of Flops
Control Network (CN)	Compute line-to-line voltages on side 1	3 * fRMS	27
	Compute line-to-line voltages on side 2	3 * fRMS	27
	Compute line currents entering side 1	3 * fRMS	27
	Compute line currents entering side 2	3 * fRMS	27
	Update inductor historical terms	3 * fL	21
	Update capacitor historical terms	6 * fC	30
	Stamp right-hand side vector due to i0	-histCab1	1
	Stamp right-hand side vector due to i1	-histCbc1	1
	Stamp right-hand side vector due to i2	-(histCab1+histCbc1+histCca1)	3
	Stamp right-hand side vector due to i3	-(histLa+histCab2-histLb-histCab1)	4
	Stamp right-hand side vector due to i4	-(histLb+histCbc2-histLc-histCbc1)	4
	Stamp right-hand side vector due to i5	-(histCab2+histCbc2+histCca2)	3
	Stamp right-hand side vector due to i6	histCab2	1
	Stamp right-hand side vector due to i7	histCbc2	1
		Subtotal	177
		Total	325

TABLE III.4. EXAMPLE OF WEIGHT CALCULATION FOR OVER-CURRENT RELAYS

Network	Description of Operation(s)	Arithmetic	Number of Flops
Electrical Network (EN)	Inverse of mesh matrix times right-hand-side eloop vector	fmult/rect.vect = 2n^2-n with n=2	6
	Compute phase a current	ia1=i0	1
	Compute phase b current	ib1=i1-i0	2
	Compute phase c current	ic1=-i1	1
		Subtotal	10

Network	Description of Operation(s)	Arithmetic	Number of Flops
Control Network (CN)	Compute line-to-line voltages on side 1	not measured directly	0
	Compute line currents entering side 1	not measured directly	0
	Compute line-to-line voltages on side 2	not measured directly	0
	Compute line currents leaving side 2	not measured directly	0
	Check if arcing is needed	IF (opening)	1
	Update arcing source ua	ua=Varc*sign(ia1)	2
	Update arcing source ub	ub=Varc*sign(ib1)	2
	Update arcing source uc	uc=Varc*sign(ic1)	2
	Check for overcurrent in phase a	IaRMS > Threshold current (x)	1
	Check for overcurrent in phase b	IbRMS > Threshold current (y)	1
	Check for overcurrent in phase c	IcRMS > Threshold current (z)	1
	Check OR condition for IabcRMS currents	x OR y OR z (w)	2
	Check IF condition for 'w'	IF (w)	1
	Check if pickup time delay has elapsed	Tdelay > (Tnow - Tfault)	2
	Change resistance of phase a	update Ra entries in mesh matrix	1
	Change resistance of phase b	update Rb entries in mesh matrix	4
	Change resistance of phase c	update Rc entries in mesh matrix	1
	Stamp right-hand side vector due to i0	-ua+ub	2
	Stamp right-hand side vector due to i1	-ub+uc	2
		Subtotal	25
		Total	35

TABLE III.5. SUMMARY OF VERTEX WEIGHTS PER COMPONENT

Acronym	Component Description	Electrical Network Flops	Control Network Flops	Total Number of Flops
GEN	Synchronous generator	23	320	343
PMG	*Prime-mover and governor*	0	68	
ROT	*Rotor swing equation*	0	28	
VRE	*Voltage regulator and exciter*	0	129	
WND	*Windings circuit*	23	95	
MOT	Induction motor and drive	182	428	610
CON	*Speed controller*	0	7	
INV	*Three-phase inverter*	59	108	
RCT	*Three-phase rectifier w/DC-link capacitor*	92	168	
ROT	*Rotor swing equation*	0	28	
WND	*Windings circuit*	31	117	
Cbl	1-phase Cable	26	78	104
CBL	3-phase Cable	148	177	325
Lod	1-phase Static Load	3	26	29
LOD	3-phase Static Load	23	80	103
XFM	Transformer	82	134	216
BRK	Over-current relays	10	25	35
LVX	Low-votlage relays controlling LVP or LVR	10	25	35
XBT	Bus transfer device with undervoltage relay (ABT or MBT)	35	99	134

From Table III.5, the most expensive (heaviest vertex) component model is the induction motor with drive. The motors have their effort concentrated in polling the diodes and transistors and determining whether their states should be toggled. It is noted though that the vertex weights are fixed (do not change during a simulation) and are only estimations of the true amount of floating point arithmetic required at the computer hardware level.

In the next subsection using the vertex weights summarized in Table III.5, the procedure of creating, balancing, and partitioning a graph is discussed. The weighted graph's vertices correspond to the SPSs component models. Using the weight of each vertex, the graph partitions are compared , and it is determined whether vertex migration is required to balance the partitions.

3.3.3 Creation of a Representative Graph

To automate the determination of where to partition the electrical network of an SPS model a representative weighed graph $\mathcal{G}(\mathcal{V},\mathcal{E})$ is used, where $\mathcal{V}$ represents the set of graph vertices and ε represents the set of graph edges. In $\mathcal{G}$, each weighed vertex represents a discretized component model which weight is the computational effort (in flops) required to solve each model as listed by Table III.5. Each graph edge (un-weighted) represents a single-phase or three-phase node (i.e., the junction where 2 or more MTCs interconnect).

To illustrate the mapping of an SPS electrical network to a representative graph, consider the components in Fig. 3.3.6. The arrows next to each component represent the power flow direction and define each component's input and output terminals. The black cross bars represent the junctions between two or more components, and are normally referred to as three-phase nodes (the cross bars for single-phase nodes are represented in the same way) . The representative graph for the network in Fig. 3.3.6 is shown in Fig. 3.3.7.

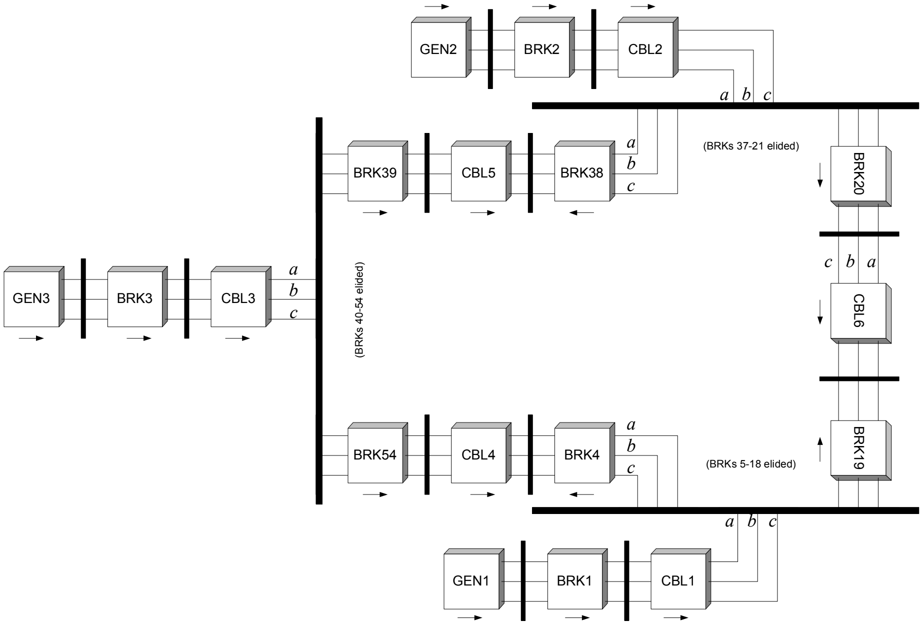


Fig. 3.3.6. A group of components to illustrate the representative graph

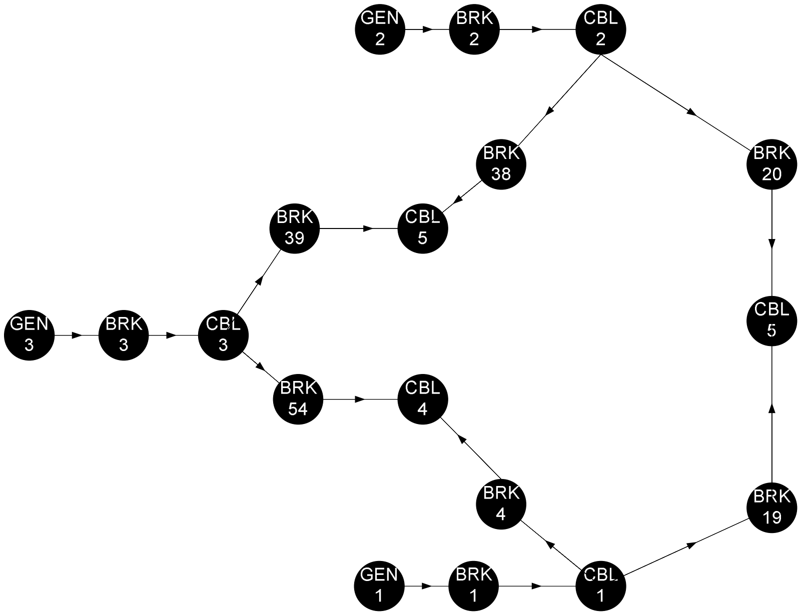


Fig. 3.3.7. Representative graph of electrical network in Fig. 3.3.6

With a representative graph $\mathcal{G}$ of an SPS model, graph theoretic algorithms can be used to find (automatically) and determine the locations where to tear the system. For example, if the graph in Fig. 3.3.7 was partitioned in p=2 partitions by tearing the edges in front of CBL2 and CBL3, the resulting partitions would appear as shown in Fig. 3.3.8. The electrical network subsystems corresponding to the graph partitions are shown in Fig. 3.3.9. Each removed edge from the graph corresponds to a disconnection point in the SPS model.

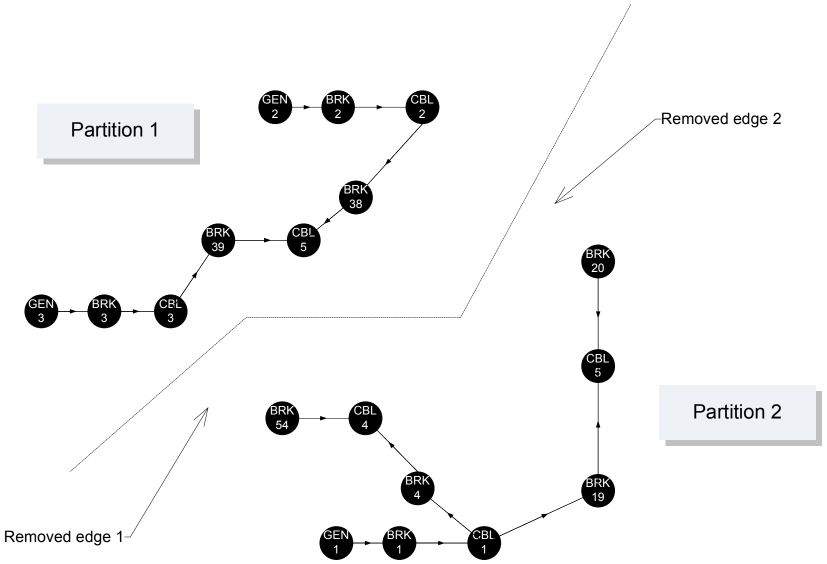


Fig. 3.3.8. A graph divided into two partitions

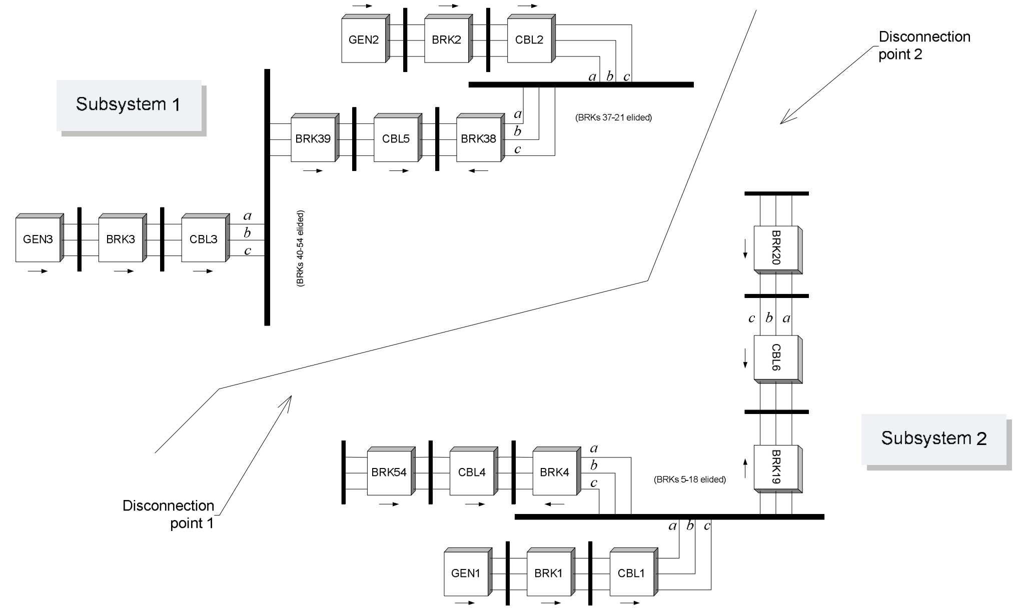


Fig. 3.3.9. Subsystems corresponding to graph partitions

To partition a large SPS model, the representative graph $\mathcal{G}$ is first partitioned using the mincut algorithm [3]. The mincut algorithm produces graph partitions where each partition has approximately the same vertex count (not vertex weight), and where the number of removed edges is minimal. Graph partitions with unequal weight correspond to SPSs of unequal computational effort. To mitigate the computational imbalance, a heuristic approach was used to balance the graph partition weights. Starting from the initial segregation created with the mincut algorithm, the vertices are heuristically migrated across partitions as explained next.

3.3.4 Graph Balancing Heuristics

The graph balancing heuristics used in this work are based on Kernighan and Lin's algorithm [100]. Kernighan and Lin's algorithm balances a set of pre-existing graph partitions by exchanging vertex *pairs* across partitions. The choice of vertex pairs is based on the gain equation in (3.56), where $k < n$ is chosen to minimize the partial sum $\sum_1^k g_i$, and where $\sum_1^n g_i = 0$ (i.e., some g_i's are negative unless all are zero). Each time the gain g_i of a potential vertex pair removal is computed, the vertex pair is removed from the graph partitions and the procedure of computing the gains is repeated for the remaining vertex pairs. Because Kernighan and Lin's algorithm aims to minimize the external cost of the graph partitions with (3.56) (i.e., minimize edge cost $\sum c_{ij},\ \ i,j = 1,...,n$, where the edge *ij* extends across partitions *A* and *B*), most of the vertex-pair exchanges occur at the boundary of *A* and *B* [101]

$$g_i = D_a + D_b - 2c_{ab} \qquad i = 1,...,n \tag{3.56}$$

where:

i = the i^{th} vertex-pair exchange
n = the number of vertices in each partition
g_i = the gain of exchanging vertices $a \leftrightarrow b$ across partitions $A \leftrightarrow B$, respectively
D_a = the difference between the external and interal costs of vertex a
D_b = the difference between the external and interal costs of vertex b
c_{ab} = the edge weight between vertices a and b

In this work, instead of assigning weights to edges extending across partitions, weights are assigned to vertices. Instead of exchanging vertex *pairs*, single vertices are allowed to move to another partition. The maximum weight imbalance $\Delta_{\max}$ for a partitioned graph is defined as the weight difference between the heaviest partition $\mathcal{G}_i$

and the lightest partition $\mathcal{G}_j$ as $\Delta_{\max} = \left(\max\left(\mathcal{W}_i\right) - \min\left(\mathcal{W}_j\right)\right)_{i \neq j}$, where $\Delta_{\max}$ varies according to how many times a graph is partitioned.

To reduce the graph imbalance the vertices are heuristically moved one-at-a-time across partitions, where after each move the graph partitions' are weighed again. To determine if the graph partitions are balanced after each move, the following metric should be satisfied: $\Delta_{\max} \leq \tau$, where $\Delta_{\max}^{new}$ is the new imbalance factor after vertices are moved across partitions, and $0 \leq \tau \leq 20\%$ is a specified tolerance factor. When there are more than two partitions, after $\Delta_{\max}$ is reduced for a pair of partitions $\left\{\mathcal{G}_i, \mathcal{G}_j\right\}_{i \neq j}$, $\Delta_{\max}$ is re-computed for a different pair of partitions $\left\{\mathcal{G}_x, \mathcal{G}_y\right\}_{x \neq y}$. The process is repeated until $\Delta_{\max} \leq \tau \; \forall \left\{\mathcal{G}_i, \mathcal{G}_j\right\}_{i \neq j}$. In case $\Delta_{\max}$ cannot be reduced to $\Delta_{\max} \leq \tau$ for a given pair of graph partitions $\left\{\mathcal{G}_i, \mathcal{G}_j\right\}_{i \neq j}$, partitions i and j are skipped and tried again after all other partitions pairs have been balanced. The graph partitioning and balancing steps are summarized below.

- Partition graph into *p* partitions $\mathcal{G} = \bigcup_{i=1}^{p} \mathcal{G}_i$ using mincut algorithm
- Compute graph partition weights $\{\mathcal{W}_1, \mathcal{W}_2, ..., \mathcal{W}_p\}$
- Balance partitions as follows:
    - i. Compute $\Delta_{\max} = \frac{100}{\max(\mathcal{W}_i)} \left| \max(\mathcal{W}_i) - \min(\mathcal{W}_j) \right|_{i \neq j}$
    - ii. If $\Delta_{\max} \leq \tau$,
        1. balancing is complete (or not needed)
        2. exit
    - iii. Else if $\Delta_{\max} > \tau$ for any two $\{\mathcal{G}_i, \mathcal{G}_j\}_{i \neq j}$, do:
        1. If $\mathcal{W}_i > \mathcal{W}_j$ move heaviest boundary vertex υ_j from $\mathcal{G}_j$ to $\mathcal{G}_i$ such that $|w_j| < (\mathcal{W}_i - \mathcal{W}_j)$, where $|w_j|$ is the weight of υ_j.
        2. Goto i)

After moving as many boundary vertices as are necessary to satisfy $\Delta_{\max} \leq \tau$, the graph partitions are considered balanced. It is noted that due to the constraint that only boundary vertices can be migrated, the tolerance factor τ might have to be increased. A larger τ means more imbalance, and is not desirable. This is a limitation of the balancing heuristic method used in this work. However, as will be shown in Chapter IV, computational imbalance in multicore computers is not as detrimental. Even with unbalanced partitions, acceptable speed gains are possible. Referring to the original work in [100], Table III.6 summarizes the differences between Kernighan and Lin's algorithm and the algorithm used here.

TABLE III.6 . COMPARISON OF GRAPH BALANCING HEURISTICS

	Kernighan and Lin’s Algorithm	As used in this Work
Assignment of a vertex weight	Sum of external and internal weights based on a vertex's degree	Weight based on computational effort or flops
Connectiviy matrix representation	Weighted edges represented as non-zero off-diagonals; diagonals are 0s	Weighted vertices represented as non-zero diagonals; off-diagonals are 1s
Gain from vertex exchange(s)	$g_i = D_a + D_b - 2c_{ab} \qquad i = 1,\ldots,n$	$\Delta_{\max} = \frac{100}{\max(\mathcal{W}_i)} \left\lvert \max\left(\mathcal{W}_i\right) - \min\left(\mathcal{W}_j\right) \right\rvert_{i \neq j}$
Initial graph segration	Varios suggested, mainly based on multilevel partitioning	Uses the mincut algorithm as the starting graph segration
Migration of vertices	By vertex pairs	By stand-alone vertices
Vertices considered	All vertex pairs	Only vertices at the boundaries

Two software programs are used for the graph creation, partitioning, and balancing stage as shown in Fig. 3.3.10. C# 3.0 is used to create the graph as an edge-list. Mathematica® [2] imports the edge-list, forms the graph $\mathcal{G}$ as an object, and partitions the graph with Mathematica’s built-in mincut algorithm. The mincut algorithm outputs $p_{\max}$ sets of partitions, where $p_{\max}$ is the maximum number of partitions desired (e.g., $p_{\max} = 12$ is used in Chapter IV). Each partition set p_i contains a subset of components, where the i^{th} subset contains the components of subsystem *i*. The component sets in the form of an output file are read back into C# where the balancing heuristics were programmed.

The mincut algorithm is run once per number of partition *p* desired. For example, to partition a graph into *p*={1,2,3,4,5,6,7,8} (i.e., $p_{\max} = 8$), the mincut algorithm is run eight times. For each *p*, each graph partition's weight is computed. If an imbalance exists, vertices are moved across partitions. A constraint of the aforementioned balancing approach is that when moving vertices across partitions, the vertices must be boundaries vertices as suggested by the activity diagram of Fig. 3.3.11.

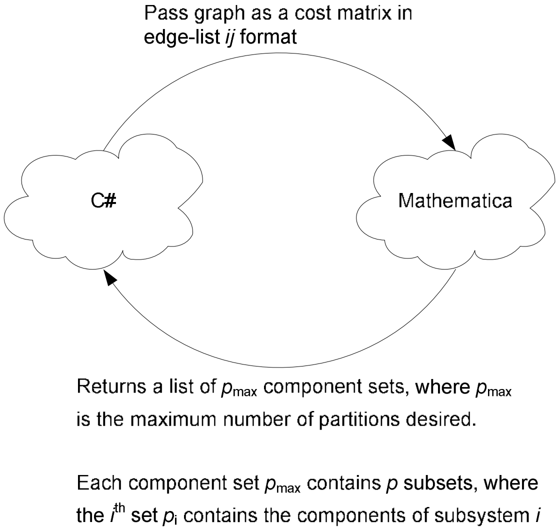

Pass graph as a cost matrix in edge-list *ij* format
C#
Mathematica
Returns a list of $p_{\max}$ component sets, where $p_{\max}$ is the maximum number of partitions desired.
Each component set $p_{\max}$ contains *p* subsets, where the i^{th} set p_i contains the components of subsystem *i*

Fig. 3.3.10. Interaction between C# and Mathematica

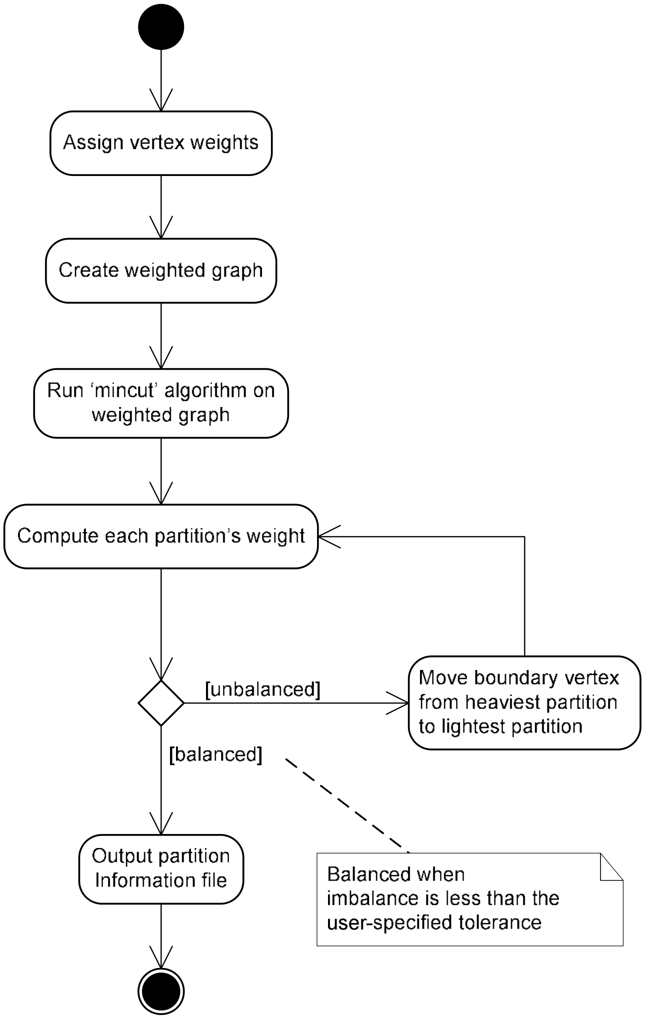
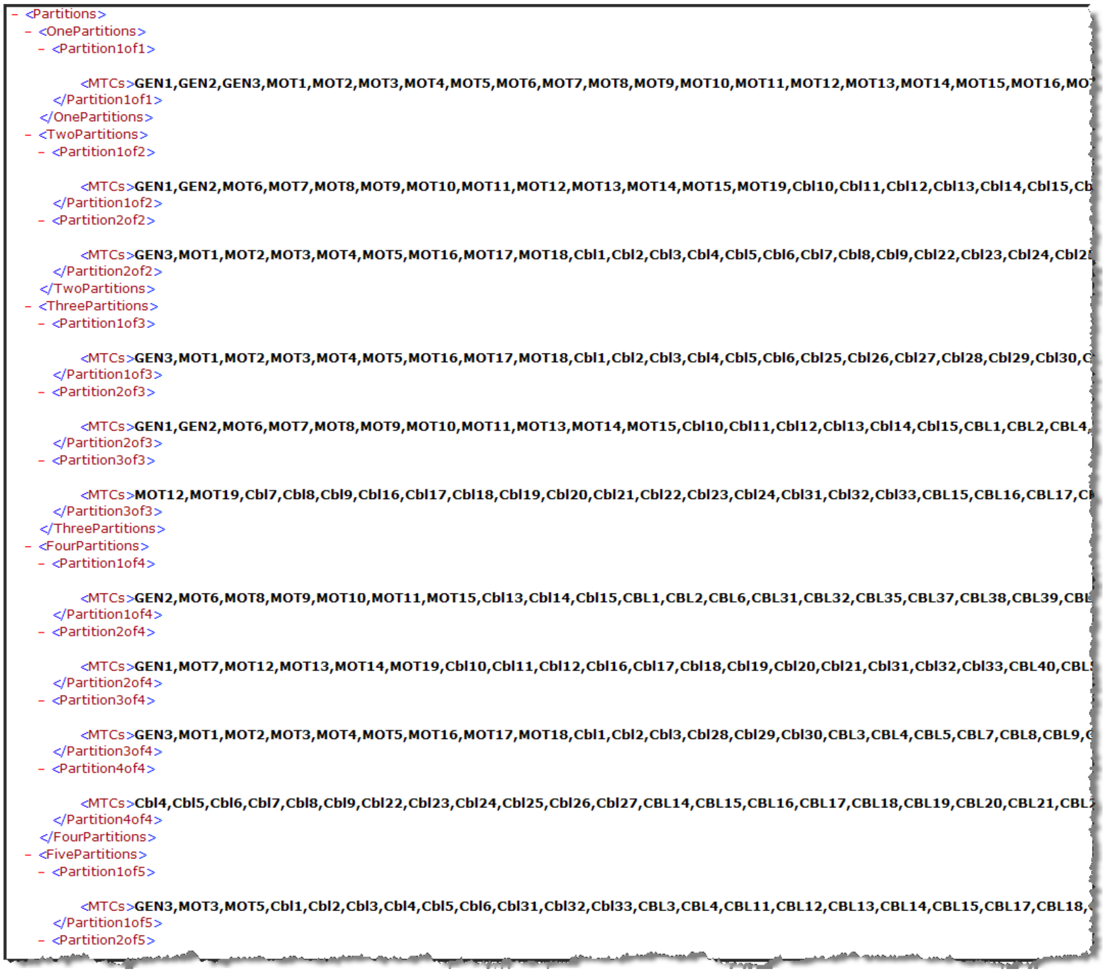

Assign vertex weights
Create weighted graph
Run 'mincut' algorithm on weighted graph
Compute each partition's weight
[unbalanced]
Move boundary vertex from heaviest partition to lightest partition
[balanced]
Output partition Information file
Balanced when imbalance is less than the user-specified tolerance

Fig. 3.3.11. Activity diagram illustrating steps to balance graph

A sample output file is provided in Fig. 3.3.12. The output file in Fig. 3.3.12 shows all components at the top for *p*=1. The components listed under "<Partition3of4>" are the components belonging to subsystem 3 when a power system is partitioned into *p*=4 subsystems.



```
- <Partitions>
  - <OnePartitions>
    - <Partition1of1>

        <MTCs>GEN1,GEN2,GEN3,MOT1,MOT2,MOT3,MOT4,MOT5,MOT6,MOT7,MOT8,MOT9,MOT10,MOT11,MOT12,MOT13,MOT14,MOT15,MOT16,MO
      </Partition1of1>
    </OnePartitions>
  - <TwoPartitions>
    - <Partition1of2>

        <MTCs>GEN1,GEN2,MOT6,MOT7,MOT8,MOT9,MOT10,MOT11,MOT12,MOT13,MOT14,MOT15,MOT19,Cbl10,Cbl11,Cbl12,Cbl13,Cbl14,Cbl15,Cb
      </Partition1of2>
    - <Partition2of2>

        <MTCs>GEN3,MOT1,MOT2,MOT3,MOT4,MOT5,MOT16,MOT17,MOT18,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,Cbl6,Cbl7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,Cbl2
      </Partition2of2>
    </TwoPartitions>
  - <ThreePartitions>
    - <Partition1of3>

        <MTCs>GEN3,MOT1,MOT2,MOT3,MOT4,MOT5,MOT16,MOT17,MOT18,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,Cbl6,Cbl25,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,C
      </Partition1of3>
    - <Partition2of3>

        <MTCs>GEN1,GEN2,MOT6,MOT7,MOT8,MOT9,MOT10,MOT11,MOT13,MOT14,MOT15,Cbl10,Cbl11,Cbl12,Cbl13,Cbl14,Cbl15,CBL1,CBL2,CBL4,
      </Partition2of3>
    - <Partition3of3>

        <MTCs>MOT12,MOT19,Cbl7,Cbl8,Cbl9,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl22,Cbl23,Cbl24,Cbl31,Cbl32,Cbl33,CBL15,CBL16,CBL17,C
      </Partition3of3>
    </ThreePartitions>
  - <FourPartitions>
    - <Partition1of4>

        <MTCs>GEN2,MOT6,MOT8,MOT9,MOT10,MOT11,MOT15,Cbl13,Cbl14,Cbl15,CBL1,CBL2,CBL6,CBL31,CBL32,CBL35,CBL37,CBL38,CBL39,CBL
      </Partition1of4>
    - <Partition2of4>

        <MTCs>GEN1,MOT7,MOT12,MOT13,MOT14,MOT19,Cbl10,Cbl11,Cbl12,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl31,Cbl32,Cbl33,CBL40,CBL
      </Partition2of4>
    - <Partition3of4>

        <MTCs>GEN3,MOT1,MOT2,MOT3,MOT4,MOT5,MOT16,MOT17,MOT18,Cbl1,Cbl2,Cbl3,Cbl28,Cbl29,Cbl30,CBL3,CBL4,CBL5,CBL7,CBL8,CBL9,C
      </Partition3of4>
    - <Partition4of4>

        <MTCs>Cbl4,Cbl5,Cbl6,Cbl7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,Cbl25,Cbl26,Cbl27,CBL14,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL
      </Partition4of4>
    </FourPartitions>
  - <FivePartitions>
    - <Partition1of5>

        <MTCs>GEN3,MOT3,MOT5,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,Cbl6,Cbl31,Cbl32,Cbl33,CBL3,CBL4,CBL11,CBL12,CBL13,CBL14,CBL15,CBL17,CBL18,
      </Partition1of5>
    - <Partition2of5>
```

Fig. 3.3.12. Component sets output file from Mathematica

Mathematica's output is a segregation of stand-alone components residing in each graph partition, which is the equivalent of an electrical network having all its components disconnected or isolated from each other [96],[102]. The stand-alone vertices correspond to the components in each subsystem and need to be interconnected to form the respective subsystem's loop resistance matrix. After all components are assigned a subsystem number as shown with the listing in Fig. 3.3.12, the first step is replace boundary three-phase cables with their torn equivalents as shown in Fig. 3.3.5. The second step is to form the i^{th} subsystem's loop resistance matrix $\mathbf{R}_{loopi}^{k+1}$ by equating the terminal meshes of adjacent components belong to the same partition.

3.3.5 Summary

Different software programs were used at the different stages of the program development. The software programs used were: MATLAB/Simulink as the drawing canvas to create the one-line diagram and Mathematica [2] to create and partition the SPS representative graph. A multithreaded simulation program was created in C# to balance the graph partitions, assign the subsystems to threads, and execute the threads on multicore computer. The partitioning stage takes place *once* per power system. Once a SPS is partitioned (i.e., subsystems are formed by interconnecting only those components in the same partition), the number of components in each subsystem remains constant and partitioning is not needed again. Re-partitioning of a power system would only be needed if/when re-adjusting the vertex weights, adding or removing components from a power system, or when changing the balancing tolerance factor τ.

3.4 SIMULATION AND MULTITHREADED SIMULATION

This section discusses the implementation of the SPS simulation approach. As introduced in section 2.5, an operating system *thread* is an independent path of code of execution commonly regarded as an asynchronous agent. Threads are asynchronous because threads do not inherently abide to synchronization rules, and therefore execute tasks regardless of what other threads are doing; as a result, data corruption, dead-locks, and contention for computer resources are common issues in multithreading programming [103-104].

Referring to Fig. 3.4.1, multiple subsystems can be created and each solved with a different thread. As of this writing, the number of subsystems that can be created exceeds the number of cores available on a multicore computer; hence, many threads will be appointed to the same core creating sequential work; the simultaneous execution of the threads, however, is a *parallel* task.

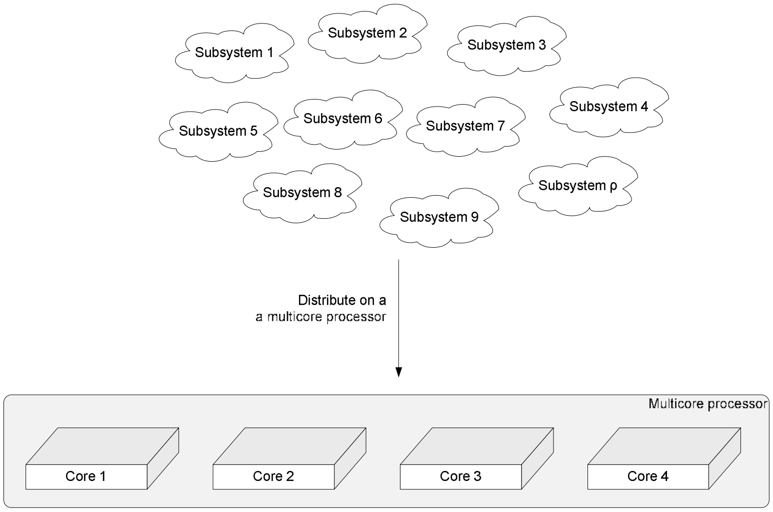


Fig. 3.4.1. Illustration of subsystem simulation on a multicore processor

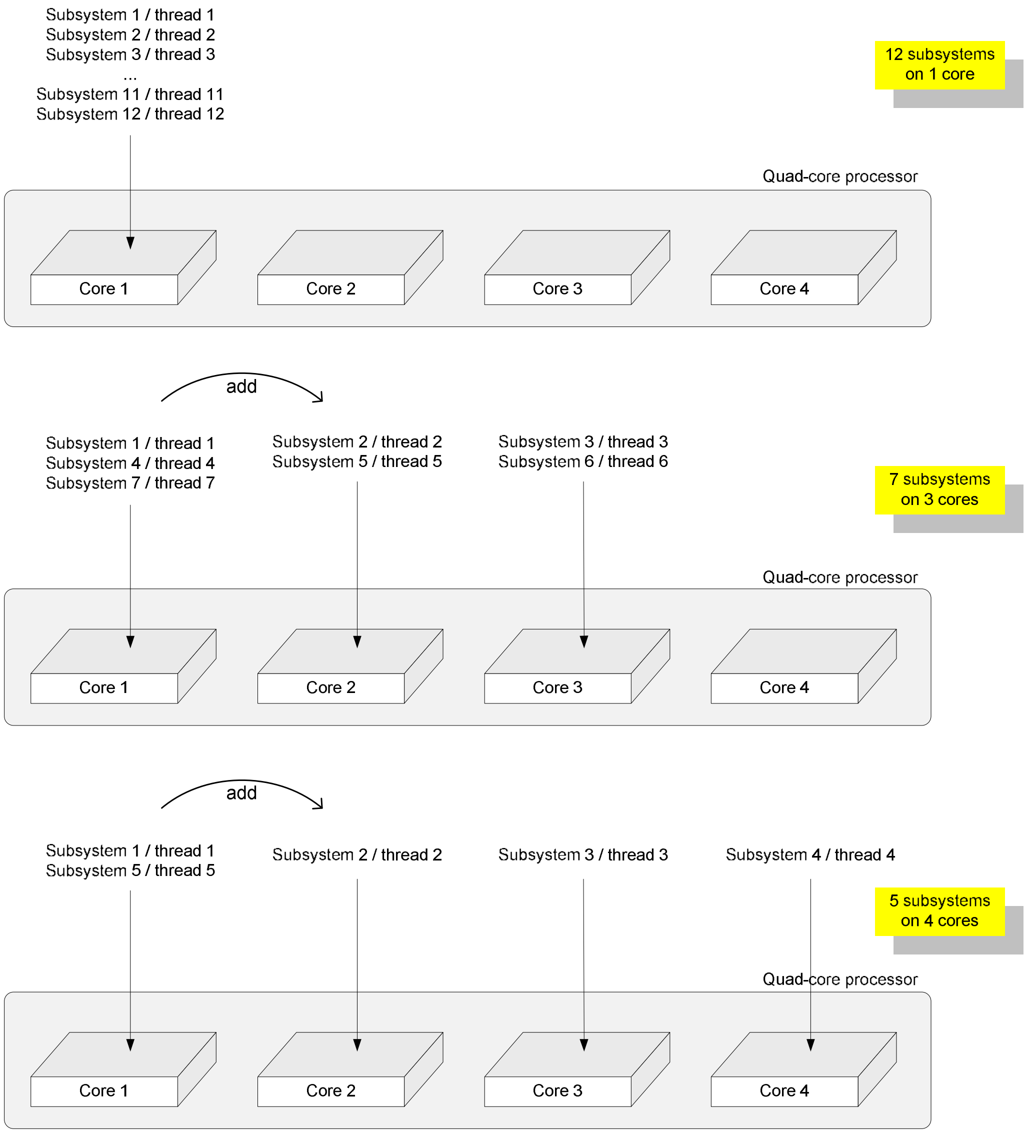


Fig. 3.4.2. Examples of various subsystem/thread distributions on four cores

The subsystems are distributed with the criteria that each core observes an equal, but minimal, number of subsystems. For example, to solve 7 subsystems on 3 cores, the subsystems are distributed as shown in the second row of Fig. 3.4.2. In the case of an odd number of subsystems (e.g., 5 subsystems on 4 cores), the left-over subsystem creates an imbalance as shown on the third row of Fig. 3.4.2.

Although it is possible to intentionally use fewer cores and leave computer resources for other applications thus under-utilizing a multicore processor, this deliberate option gives rise to inefficiency--computationally speaking. For example, a power system partitioned in p=12 can be solved using 1 core. However, with 3 unused cores a quad-core computer would not be fully exploited.

A Microsoft Windows-based program was developed in C# 3.0 with .NET 3.5 to perform the multithreaded parallel-sequential simulations. When the simulation starts, each thread solves the electrical and control networks of each subsystem as explained in section 3.2.5. A swim-lane showing the thread interactions at each time step is shown in Fig. 3.4.3 and explained in detail next.

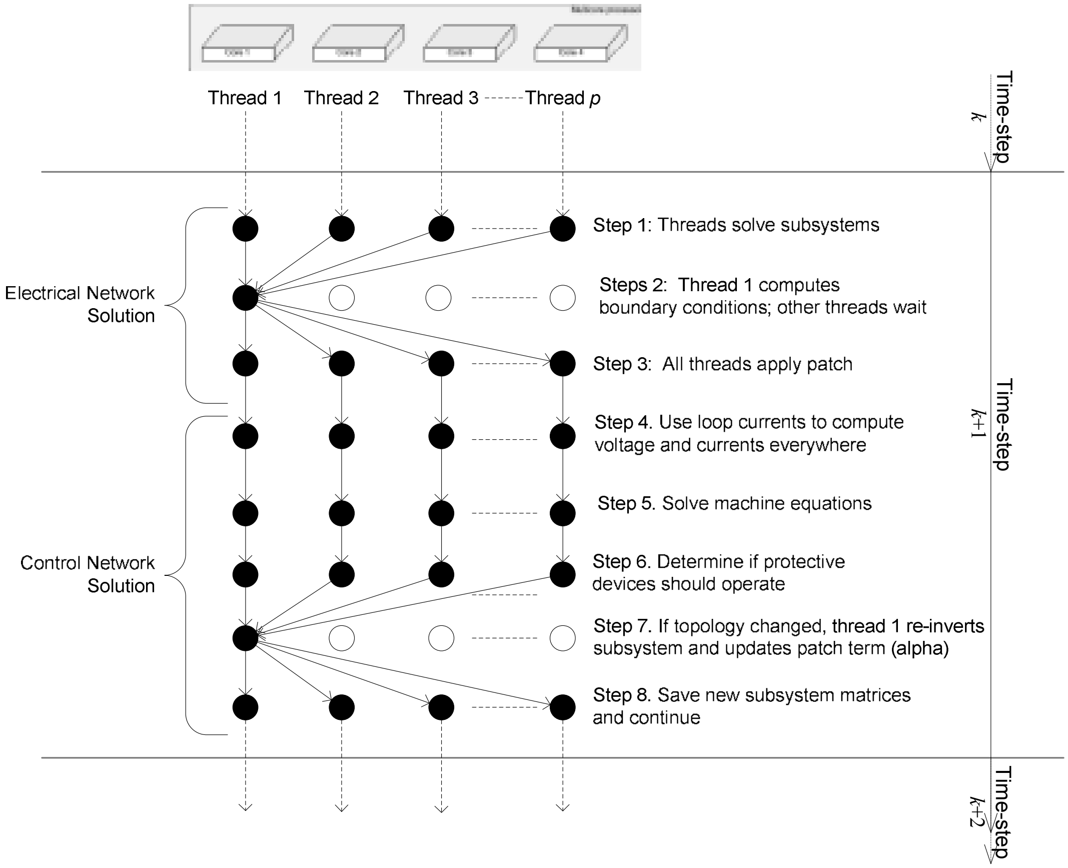

Thread 1
Thread 2
Thread 3
Thread *p*
Time-step *k*
Electrical Network Solution
Step 1: Threads solve subsystems
Steps 2: Thread 1 computes boundary conditions; other threads wait
Step 3: All threads apply patch
Time-step *k*+1
Step 4. Use loop currents to compute voltage and currents everywhere
Step 5. Solve machine equations
Control Network Solution
Step 6. Determine if protective devices should operate
Step 7. If topology changed, thread 1 re-inverts subsystem and updates patch term (alpha)
Step 8. Save new subsystem matrices and continue
Time-step *k*+2

Fig. 3.4.3. Thread swim-lane diagram: 1 thread-per-core shown

- Electrical Network Solution

    - Step 1: The threads (one per subsystem, though many per core are possible) solve the first term on the RHS of (3.57) using forward and backward substitutions. When there are multiple threads per core, each core switches among threads using time-slicing.

$$\begin{bmatrix} \mathbf{i}_{loop1}^{k+1} \\ \mathbf{i}_{loop2}^{k+1} \\ \vdots \\ \mathbf{i}_{loopp}^{k+1} \end{bmatrix} = \underbrace{\begin{bmatrix} \left(\mathbf{R}_{loop1}^{k+1}\right)^{-1} \mathbf{e}_{loop1}^{k+1} \\ \left(\mathbf{R}_{loop2}^{k+1}\right)^{-1} \mathbf{e}_{loop2}^{k+1} \\ \vdots \\ \left(\mathbf{R}_{loopp}^{k+1}\right)^{-1} \mathbf{e}_{loopp}^{k+1} \end{bmatrix}}_{\text{step 1: subsystem solutions}} \underbrace{- \begin{bmatrix} \left(\mathbf{R}_{loop1}^{k+1}\right)^{-1} \mathbf{D}_1 \\ \left(\mathbf{R}_{loop2}^{k+1}\right)^{-1} \mathbf{D}_2 \\ \vdots \\ \left(\mathbf{R}_{loopp}^{k+1}\right)^{-1} \mathbf{D}_p \end{bmatrix} \underbrace{\mathbf{v}_C^{k+1}}_{\text{step 2: boundary conditions}}}_{\text{step 3: patch}} \tag{3.57}$$

- ○ Step 2: using the p solutions from Step 1, thread 1 computes the boundary conditions $\mathbf{u}^{k+1}$ with (3.58). While thread 1 computes $\mathbf{v}_C^{k+1}$, the other threads await. The synchronization constructs used in C# to synchronize the threads are `AutoResetEvent` handles [103] and are explained in Appendix B. The term $\boldsymbol{\alpha}$ is a constant coefficient matrix and does not change unless the network topology changes. The term $\boldsymbol{\beta}^{k+1}$ changes at every time step of the simulation.

$$\begin{cases} \mathbf{v}_C^{k+1} = \boldsymbol{\alpha}^{-1}\boldsymbol{\beta}^{k+1} + \mathbf{hist}_C^{k+1} \\ \quad \boldsymbol{\alpha} = \mathbf{I}_r + \sum_{i=1}^{p} \left(\mathbf{D}_i^{\mathrm{T}} \left(\mathbf{R}_{loopi}^{k+1}\right)^{-1} \mathbf{D}_i \right) & (\text{constant matrix}) \\ \boldsymbol{\beta}^{k+1} = \sum_{i=1}^{p} \mathbf{D}_i^{\mathrm{T}} \underbrace{\left(\mathbf{R}_{loopi}^{k+1}\right)^{-1} \mathbf{e}_{loopi}^{k+1}}_{\text{from step 1}} & \begin{pmatrix} \text{vector updated at} \\ \text{every time step} \end{pmatrix} \end{cases} \tag{3.58}$$

- ○ Step 3: After thread 1 computes the boundary conditions, the threads patches their subsystems using the second term on the RHS of (3.57). The term $\mathbf{v}_C^{k+1}$ represents the capacitor voltages at the boundaries of disconnection. The superposition form in (3.57) suggest that the capacitors impress a voltage at the boundaries of disconnection to counter-act the short-circuit currents of each subsystem. After step 3, the control network (next step) *does not experience* (i.e., it is oblivious to) a partitioned electrical network.

- Control Network Solution

    - Step 4: The control network solution begins. Using the patched (corrected) loop currents of each subsystem, each thread computes the instantaneous voltages and currents for each component model. Using the components' terminal voltages and currents, all node RMS voltages and branch RMS currents are obtained. This step gives the solution to (3.22).

    - Step 5: If a subsystem has machines, it uses the stator voltages computed in Step 4 to find the field voltageand winding currents. With the winding currents, the electromagnetic torque is computed and the mechanical speed obtained.

    - Step 6: Using the RMS measurements from Step 4, each protective device determines if it needs to operate. If so, a signal is sent to the master thread indicating that re-triangularization of the appropriate subsystem's loop resistance matrix is needed.

    - Step 7: If there is a topology change (e.g., diode or transistor commutation, fault, or protective device), thread 1 re-triangulates the appropriate subsystem's matrix, and updates the static term of the boundary conditions (i.e., matrix $\boldsymbol{\alpha}$).

    - Step 8: After thread 1 completes re-triangulating any subsystem's matrix (if any), all threads continue into the next time step.

3.5 DETERMINING THE NUMBER OF PARTITIONS

This subsection discusses how to determine in general a good number of partitions p to minimize simulation run-time. A simulation's run-time is proportional to two components:

- the total number of time steps in a simulation $k_{tot} = t_{end} / \Delta t$, where t_{end} is the user-specified simulation end-time in seconds and Δ*t* is the time step increment in seconds, and
- the amount of time in seconds it takes to solve each time step *k*, which is proportional to the number of flops per time step

To reduce the amount of time it takes to solve each time step, the number of flops per *k* should be reduced. In terms of flops, the computational cost incurred at each time step is defined in (3.59), where C_{step} is the total and C_{stepi} is the cost of only the *i*th step, which was defined earlier for the swim-lane diagram in Fig. 3.4.3.

$$C_{step} = \overbrace{C_{step1} + C_{step2} + C_{step3}}^{\text{Electrical Network}} + \overbrace{C_{step4} + C_{step5} + C_{step6} + C_{step7} + C_{step8}}^{\text{Control Network}} \qquad (3.59)$$

Fig. 2.2.4 illustrated that the solution time is governed by the solution of **A·x**=**b**, which in (3.59) corresponds to the EN solution. The solution of the CN makes up for a smaller percentage of computational effort in each time step and is not used in determining the number of partitions *p*.

Although multiplications take longer than summations [83],[105], for simplicity both operations are assumed to cost one flop each. The cost of each of the terms $C_{step1} + C_{step2} + C_{step3}$ is presented next.

3.5.1 Cost of Step 1

Referring to (3.57), and assuming that the number of loop currents in subsystems 1 through p are the same (i.e., $\ell_1 = \ell_2 = ... = \ell_p$), the flop-cost of step 1 for the i^{th} subsystem is given by (3.60)

$$C_{step1} = \overbrace{\left(\mathbf{R}_{loopi}^{k+1}\right)^{-1} \mathbf{e}_{loopi}^{k+1}}^{f_{rect\text{-}vct}^{mult}=2mn-m} \quad . \tag{3.60}$$

Since $\mathbf{R}_{loopi}^{k+1}$ has dimensions $n_i \times n_i \Rightarrow m = n$, and $\mathbf{e}_{loopi}^{k+1}$ has dimensions $n_i \times 1$ where $n_i = \ell_i$, (3.60) becomes

$$C_{step1} = 2\ell_i^2 - \ell_i . \qquad \left(\text{parallel}\right) \tag{3.61}$$

The cost C_{step1} in (3.61) assumes subsystems 1 through p are solved in parallel, which is the best-case scenario. In the worst-case scenario, subsystems 1-p are all solved sequentially, which changes (3.61) to (3.62) [83]

$$C_{step1} = \sum_{i=1}^{i=p} 2\ell_i^2 - \ell_i . \qquad \left(\text{sequential}\right) \tag{3.62}$$

3.5.2 Cost of Step 2

Referring to (3.58), the cost of step 2 is broken down into the computation of $\boldsymbol{\beta}^{k+1}$ and $\mathbf{v}_C^{k+1}$, respectively (it is assumed that $\boldsymbol{\alpha}$ remains time-invariant)

$$\boldsymbol{\beta}^{k+1} = \sum_{i=1}^{p} \left. \overbrace{\overbrace{\mathbf{D}_i^{\mathrm{T}} \underbrace{\left(\mathbf{R}_{loopi}^{k+1}\right)^{-1} \mathbf{e}_{loopi}^{k+1}}_{\text{from step 1}}}^{f_{rect\cdot vct}^{mult}=2mn-m}}^{(p\text{–}1)\text{ summations}} \right|_{m=n=r} = r - p\cdot r - 2r^2 + 2p\cdot r^2 \tag{3.63}$$

$$\mathbf{v}_C^{k+1} = \left. \overbrace{\overbrace{\boldsymbol{\alpha}^{-1}\boldsymbol{\beta}^{k+1}}^{f_{rect\cdot vct}^{mult}=2mn-m} + \overbrace{\mathbf{hist}_C^{k+1}}^{f_C\times r=5r}}^{f_{vct+vct}^{sum}=n} \right|_{m=n=r} = 5r + 2r^2. \tag{3.64}$$

In (3.63), p is the number of partitions and r is the total number of torn capacitors for the entire system. The cost of step 2 is the sum of costs in (3.63) and (3.64). This summation is given in (3.65). Referring to Fig. 3.4.3, step 2 is the major bottleneck of diakoptics-based approaches and cannot not be parallelized [106]

$$C_{step2} = 6r - p\cdot r + 2p\cdot r^2. \qquad \text{(sequential)} \tag{3.65}$$

3.5.3 Cost of Step 3

Referring to (3.57), the cost of step 3 consists of a matrix-vector multiplication and a vector-vector summation as given in (3.66). It is assumed that the negative sign in (3.66) can be treated as a pure addition instead of, first, a multiplication by -1 and, then, an addition.

$$C_{step3} = \ldots - \left. \underbrace{\overbrace{\overbrace{\begin{bmatrix} \left(\mathbf{R}_{loop1}^{k+1}\right)^{-1}\mathbf{D}_1 \\ \left(\mathbf{R}_{loop2}^{k+1}\right)^{-1}\mathbf{D}_2 \\ \vdots \\ \left(\mathbf{R}_{loopp}^{k+1}\right)^{-1}\mathbf{D}_p \end{bmatrix} \underbrace{\mathbf{v}_C^{k+1}}_{\substack{\text{step 2: boundary}\\ \text{conditions}}}}^{f_{rect\cdot vct}^{mult}=2mn-m}}^{f_{vct+vct}^{sum}=m}}_{\text{step 3: patch}} \right|_{m=\ell_i;n=r} = 2r\cdot\ell_i \quad (\text{parallel}) \tag{3.66}$$

In (3.66) the product $\left(\mathbf{R}_{loopi}^{k+1}\right)^{-1}\mathbf{D}_i$ is constant and does not need to be computed at each time step. The dimensions of $\mathbf{v}_C^{k+1}$ are $r\times 1$, which when multiplied by $\left(\mathbf{R}_{loopi}^{k+1}\right)^{-1}\mathbf{D}_i$, gives a $\ell_i \times 1$ vector which in turn acts as a patch for the solution in step 1. The patch term is the summation of two vectors: one obtained from step 1 and the other obtained from step 3, which is a vector summation of $m = \ell_i^{\text{th}}$ order.

The cost in (3.66) assumes that subsystems 1 through p are solved in parallel, which is the best-case scenario. In the worst-case scenario, subsystems 1-p are all solved sequentially, which changes (3.66) into (3.62)

$$C_{step3} = \sum_{i=1}^{i=p} 2r\cdot\ell_i. \qquad (\text{sequential}) \tag{3.67}$$

3.5.4 Cost Function

The cost of $C_{step1} + C_{step2} + C_{step3}$ is given in (3.68), and represents the flop-cost at each time step k. Minimization of (3.68) is expressed as a cost function of three variables in (3.69), and is considered an NP-complete problem. The essence of the cost function resides in reducing the objective function without violating the inequality constraints.

In (3.69) the dominant variables are the subsystem's order ℓ_i, and the number of torn capacitors *r*. To minimize C_{tot}, both ℓ_i and *r* should be reduced which is a conflicting requirement. To decrease ℓ_i, *p* must increase; if *p* increases, so does *r*. There is an intrinsic (and intricate stochastic) relationship between *p* and *r* , which can reduce the cost function of (3.69) to be a function of two possible variables pair: ℓ_i and *p*, or ℓ_i and *r* .

$$\begin{aligned} C_{tot} &= C_{step1} + C_{step2} + C_{step3} \\ &= \left(2\ell_i^2 - \ell_i\right) + \left(6r - p \cdot r + 2p \cdot r^2\right) + \left(2r \cdot \ell_i\right) \\ &= (6-p)r + 2p \cdot r^2 + (-1+2r)\ell_i + 2\ell_i^2 \end{aligned} \tag{3.68}$$

$$\min\left\{C_{tot} = (6-p)r + 2p \cdot r^2 + (-1+2r)\ell_i + 2\ell_i^2\right\} \tag{3.69}$$

subject to:

$$\begin{cases} 2 \le p \le p_{\max} \\ 2 \le r \le r_{\max}; \qquad r = f\left(p\right) \\ \ell_i \approx \frac{\ell}{p} \end{cases}$$

where:

ℓ = the order of the unpartitioned system
ℓ_i = the order of the i^{th} subsystem
r = the number of torn capacitors
$r_{\max}$ = the maximum number of capacitors that can be torn
p = the number of partitions
$\mathrm{p}_{\max}$ = the maximum number of possible partitions
$f\left(p\right)$ = a function of *p*.

Minimization of the cost function (3.69) is an NP-complete problem and cannot be expressed in closed form [96],[107-108]. In (3.69), *p* is constrained on its upper-end to $p_{\max}$, which is unknown until a power system has been defined by the user. The number of torn capacitors *r* in this work is at least 2, and is related *p*, and cannot be expressed in closed form. The upper limit of *r* is $r_{\max}$, which is determined by the number of capacitor loops in a system. Once a power system (i.e., a SPS) is defined by the user and after the balancing heuristics is completed, the value of *r* is exposed. The number of loop currents in the i^{th} subsystem is unknown until the graph's balancing heuristics is complete.

Different values of *p* and *r* will be shown in Chapter IV, during the performance metric studies. When introducing (3.60), it was stated that ℓ_i represented the assumption that all subsystems have the same number of loop currents. Due to the heuristic solution requirement to minimize (3.69), and the possible $\left\{p, p_{\max}, r, \ell_i\right\}$ solutions, which depend on system order and topology, the cost function in (3.69) was not solved in this work. In Chapter IV, a good value for *p* was determined empirically.

3.6 CHAPTER SUMMARY

This chapter presented the discretization, partitioning, and simulation approaches used in this work. At the end of the chapter, a theoretical cost function was introduced to predict the best number of partitions. The interconnection of all discretized component models produced a large interconnected resistive network which is formulated using loop currents.

To partition a power system and reduce simulation run-time, a representative graph is created and partitioned according to the mincut algorithm. To balance the graph partitions, boundary vertices are moved across partitions heuristically. Once each component is assigned a partitioning number, each subsystem's loop resistance matrix can be formed by connecting only those components in the partition. When cables are the boundary of partitions, their RHS is left short-circuited (i.e., the capacitors do not form part of their equations).

The simulation approach was also presented in this chapter. Threads were taken from the Windows thread pool and used to invoke the *solve* method on each subsystem object. The thread synchronization approach used in this work is given in Appendix B. The swim-lane diagram in Fig. 3.4.3 presents the details of what occurs during each time step of the simulation.

Producing various subsystems from a large power system permits simulating the subsystems in a parallel-sequential fashion using multithreaded programming. When fewer threads than cores are used, the simulation is purely parallel. When there are more threads than cores, the simulation is partially sequential and partially concurrent.

CHAPTER IV

STUDIES AND PERFORMANCE ANALYSIS

4.1 INTRODUCTION

This chapter presents the performance metrics used to validate the solution methodology. The performance metrics (PMs) were assessed by repeatedly running a benchmark case study based on SPS battle damage scenario [8]. The section on results presents select simulation waveforms, and the results of evaluating the performance metrics. A summary of the performance metrics results and conclusions are presented in the last section of this chapter.

4.2 DESCRIPTION OF PERFORMANCE METRICS

4.2.1 Performance Metric 1

The first performance metric (PM1) evaluates the speed gain and accuracy of partitioned simulations using a fixed time step of Δt=50μs for all number of partitions p and number of cores c. The simulation speed gain was computed as the ratio of unpartitioned to partitioned simulation run-times using (4.1) [35], where $t_{\text{unpartitioned}}$ is the unpartitioned (i.e., p=1, c=1) simulation run-time in seconds, and $t_{\text{partitioned}}$ is any partitioned (p>1) simulation's run-time in seconds.

$$K_{speed} = \frac{t_{\text{unpartitioned}}}{t_{\text{partitioned}}} \tag{4.1}$$

Simulation accuracy was assessed by comparing the unpartitioned and partitioned simulation results at each time step of the simulation using (4.2), where $x_{\text{unpartitioned}}^{k+1}$ is a data sample from the unpartitioned simulation results (i.e., an instantaneous voltage or current measurement), and $x_{\text{partitioned}}^{k+1}$ is the same sample but taken from a partitioned simulation.

$$100\left|\frac{x_{\text{unpartitioned}}^{k+1}-x_{\text{partitioned}}^{k+1}}{x_{\text{unpartitioned}}^{k+1}}\right|\% \tag{4.2}$$

At each simulation time step, line-to-line voltages v_{ab}^{k+1}, v_{bc}^{k+1}, v_{ca}^{k+1} were saved for all 330 three-phase nodes, and currents i_{a}^{k+1}, i_{b}^{k+1}, i_{c}^{k+1} were saved for all 281 branches. For the simulation length of $t_{end}=1\text{s}$, a time step of Δt=50μs, and p=12 partitions, $\left((3\times 330)+(3\times 281)\right)\times\frac{1}{50\times 10^{-6}}\times 12=439.92\times 10^{6}$ data points were evaluated using (4.2).

The number of simulation runs to evaluate PM1 is illustrated with Fig. 4.2.1, where each block represents a unique p and c combination. The abscissa and ordinates show how p and c were swept to evaluate PM1, which resulted in a total of 42 simulation runs.

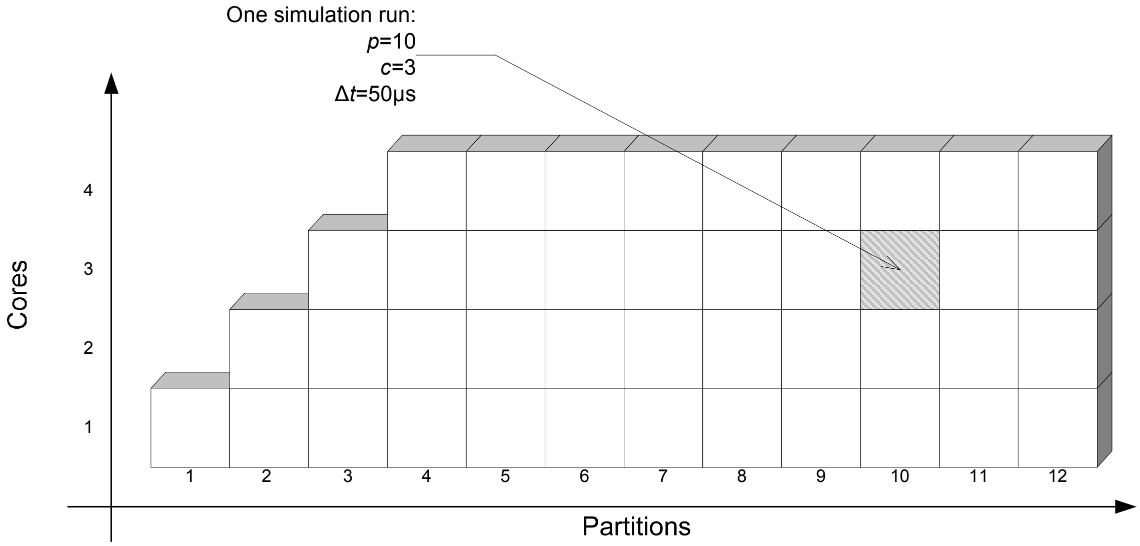


Fig. 4.2.1. Number of simulation runs (42) to evaluate performance metric 1

4.2.2 Performance Metric 2

The second performance metric (PM2) measures speed gain and accuracy, but additionally sweeps the time step as: $\Delta t = \{75, 100, 250, 500\}\,\mu\text{s}$. An illustration of the time steps sizes (relative to Δt=50μs) is shown in Fig. 4.2.2. The time step increase is non-linear, starting with a 1.5x size factor and ending with 10x size factor. The non-linear increase was chosen as such to observe if the error introduced from partitioning SPS simulations follows this trend.

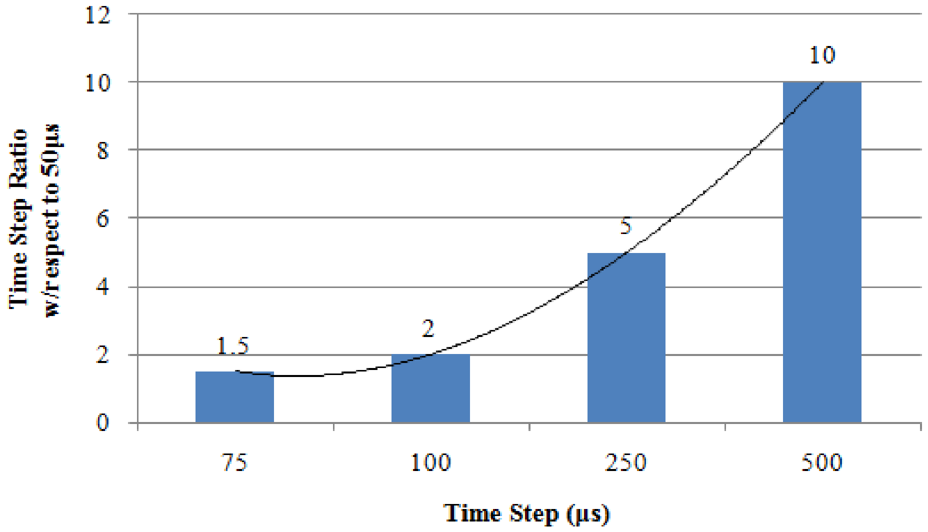


Fig. 4.2.2. Time step sizes used for performance metric 2

The evaluation of speed and accuracy for PM2 was conducted in the same way as was conducted for PM1. Equation (4.1) was used to assess the speed gain, and (4.2) to assess accuracy. The three dimensional sweeping of $p \in \{1,12\}$, $c \in \{1,4\}$, and $\Delta t = \{75, 100, 250, 500\}$ µs for PM2 required the as many simulation runs as depicted with Fig. 4.2.3. If $N_{dt} = 4$ is the number of different Δt sizes used, $N_{part} = 12$ is the maximum number of partitions created (i.e., $p_{\max}$), and $N_{cores} = 4$ is the number of cores on the multicore computer used, the total number of simulation runs for PM2 is given by (4.3).

$$\begin{matrix}\text{Total no.}\\ \text{runs}\end{matrix} = N_{dt}\left(N_{part}N_{cores} - \frac{N_{cores}\left(N_{cores}-1\right)}{2} \right)\Bigg|_{\substack{N_{part}=12\\ N_{cores}=4\\ N_{dt}=4}} = 168 \qquad (4.3)$$

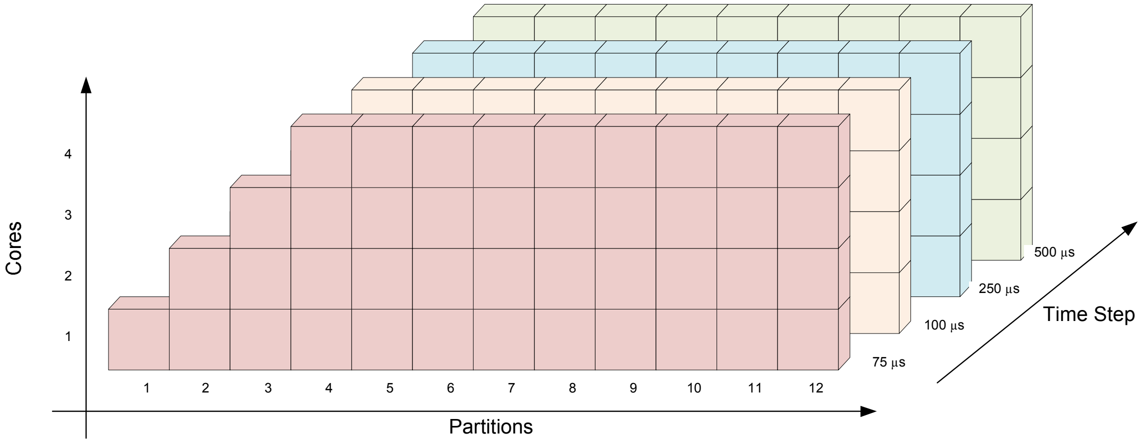


Fig. 4.2.3. Number of simulation runs (168) to evaluate performance metric 2

4.3 DESCRIPTION OF CASE STUDY

A case study was chosen to assess the aforementioned PMs. The simulations were conducted using a multithread program developed in C# 3.0 which ran on the computer listed in Table IV.1.

TABLE IV.1 . COMPUTER USED TO EVALUATE PERFORMANCE METRICS

Computer A	Dell Precision PWS690
Memory	3.25GB
Operating System	Windows XP Professional 2002 with Service Pack 3
Processor	Intel Xeon E5345 (quad-core)

The present case study simulates the battle damage scenario presented in [8] as three-phase cable faults causing the successive and simultaneous tripping of protective devices throughout the system. The one-line diagram of the notional AC-Radial SPS model used for the case study is shown Fig. 4.3.1, where acronyms and component count (as XYZ, 12) are provided in the legend.

The objectives, limitations, and assumptions, of the system model and case study are stated next.

Objectives:

- To observe system behavior under battle damage
- To measure the simulation speed gain after parallelizing the simulation
- To assess the accuracy of partitioned simulations

Limitations and Assumptions:

- The battle damage is modeled as nine three-phase cable faults
- The fault locations were obtained from the geographical information system (GIS) presented in [8]

- The SPS model in this work is the same as presented in [8]
- The nine faults (FLTs), 1 through 9, were applied as follows:

FLT1 applied at $t = 0.1$s
FLT2 applied at $t = 0.2$s
FLT3 applied at $t = 0.3$s
FLT4 applied at $t = 0.4$s
FLT5 applied at $t = 0.5$s
FLT6 applied at $t = 0.6$s
FLT7 applied at $t = 0.7$s
FLT8 applied at $t = 0.8$s
FLT9 applied at $t = 0.9$s

- The fault line-to-line resistance was $R_{fault} = 50\text{m}\Omega$
- All faults occurred on the 450V side of the system
- All faults occurred at the center (midway) of a cable
- The simulations ran for 60 cycles (t=0s to t_{end}=1s)
- The system was partitioned up to 12 times $\left(p \in \left[1,12\right]\right)$
- The system was ran on 1,2,3, and 4 cores $\left(c \in \left[1,4\right]\right)$
- Only generators 1 and 2 were online

Protective Device Initial States:

- All bus transfers started on their normal supply path (side 1)
- All over-current relays started in the closed position
- The emergency generator's relay was the only relay in the open position (i.e., GEN3 was offline)
- All low-voltage protective devices started in the closed position

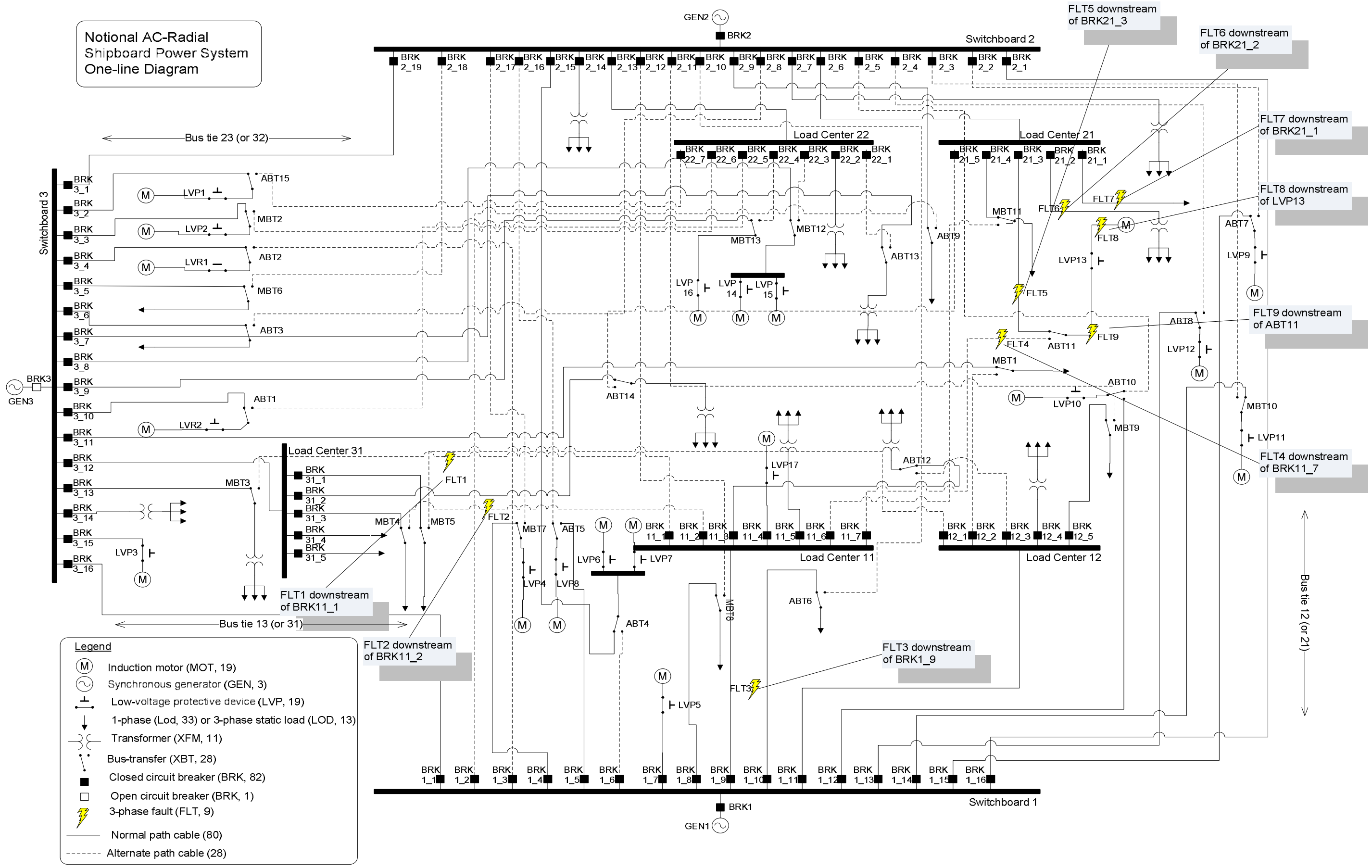


Fig. 4.3.1. Schematic of SPS used for case studies showing locations of the 9 faults

The system ratings and protective device settings are listed in Table IV.2 and Table IV.3, respectively. As noted, LVRs are the only protective devices without a time delay, which means LVRs operate instantaneously when any line-to-line voltage becomes $\leq$405V.

The average number of components per partition, the number of boundaries, and the number of capacitor loops torn are shown in Fig. 4.3.2. The exact component distribution in each partition (i.e., subsystem) is listed in Appendix C. It is noted that there is no direct relation between p and the number of boundaries. For example, when $p = 12$ there are 22 boundaries, which is less than when p=7 having 24 boundaries. This indirect relationship between the number of partitions and number of boundaries is due to two reasons: the first is the mincut algorithm, where the edge-cut depends on the graph connection matrix and p. The second reason is due to the graph balancing heuristics. When, and if, an internal vertex that is *not* at a boundary is moved to another partition, a new boundary is created to detach said vertex from its current graph partition.

TABLE IV.2 . NOTIONAL AC-RADIAL SPS MODEL BASE QUANTITIES

Description of Quantity	Symbol	Value	Units
Base 3-phase total power	$S_{3\varphi}$	3.125	MVA
Base 3-phase real power	$P_{3\varphi}$	2.500	MW
Base 3-phase reactive power	$Q_{3\varphi}$	1.875	Mvars
Power factor	PF	0.8	
Power angle	ϕ	36.87	degrees
Base frequency	f_{base}	60	Hz
Base voltage	V_{LL}	0.45	kV RMS line-to-line
Base 1-phase power	$S_{1\varphi}$	1.042	MVA
Base 1-phase current	I_p	2.31	kA RMS
Base line-current	I_L	4.009	kA RMS
Base per-phase impedance	Z_p	0.1944	Ohms

TABLE IV.3 . PROTECTIVE DEVICE SETTINGS

Protective Device	Pickup Condition	Pickup Time Delay (cycles)	Pickup Time Delay (secs)	Restore Time Delay (cycles)	Restore Time Delay (secs)
Overcurrent relays at load centers	Any phase current ≥ specified threshold	3	0.05	-	-
Overcurrent relays at switchboards	Any phase current ≥ specified threshold	6	0.1	-	-
Overcurrent relays on ring bus	Any phase current ≥ 2kA	12	0.2	-	-
Overcurrent relays at generators	Any phase current ≥ 4kA	15	0.25	-	-
Low voltage protective devices (LVPs)	Any line-to-line voltage ≤ 405V (90%)	3	0.05	-	-
Low voltage protective releases (LVRs)	Any line-to-line voltage ≤ 405V (90%)	0	0	2	0.033
Automatic bus transfers (ABTs)	Any line-to-line voltage ≤ 405V (90%)	2	0.033	2	0.033
Manual bus transfers (MBTs)	Any line-to-line voltage ≤ 405V (90%)	2	0.033	-	-

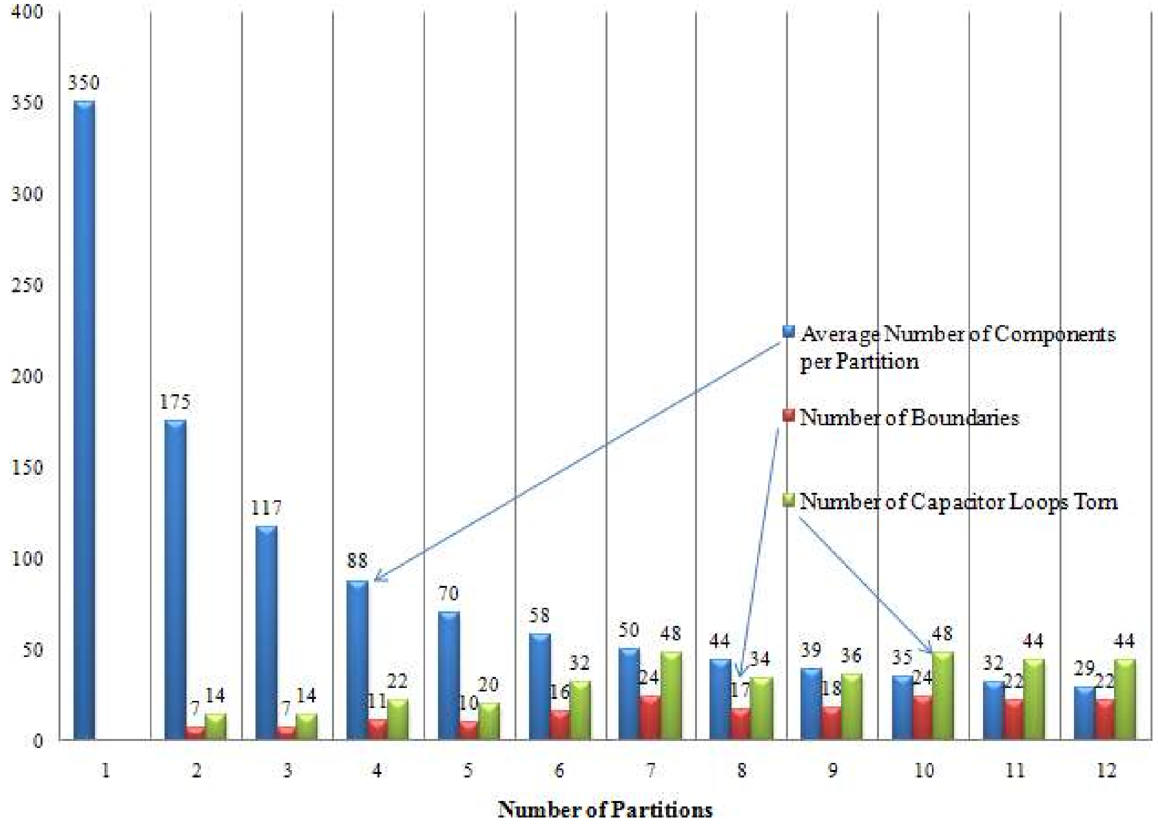


Fig. 4.3.2. Average component distribution per number of partitions

The model used for the faults is shown in Fig. 4.3.3, where $R_{fault} = 50\text{m}\Omega$ is the fault resistance during the fault, $R_{open} = 1\text{M}\Omega$ is the fault resistance before the fault, v_{abf}^{k+1} is the fault voltage across phase *ab*. To stage the three-phase faults, the three resistances in Fig. 4.3.3 simultaneously change their values from R_{open} to R_{fault}.

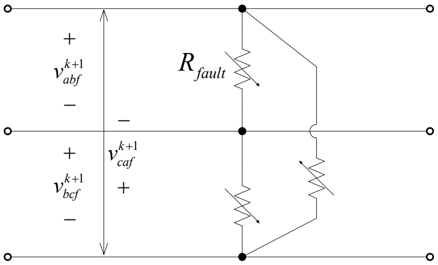


Fig. 4.3.3. Three-phase fault model (inside three-phase cables)

This section presented the PMs, their importance, the number of runs required to asses said PMs, the system model, an average component distribution in each partition, the number of capacitor loops torn, fault times, and an overview of the protective device settings. The following sections present select simulation waveforms and the performance metric results.

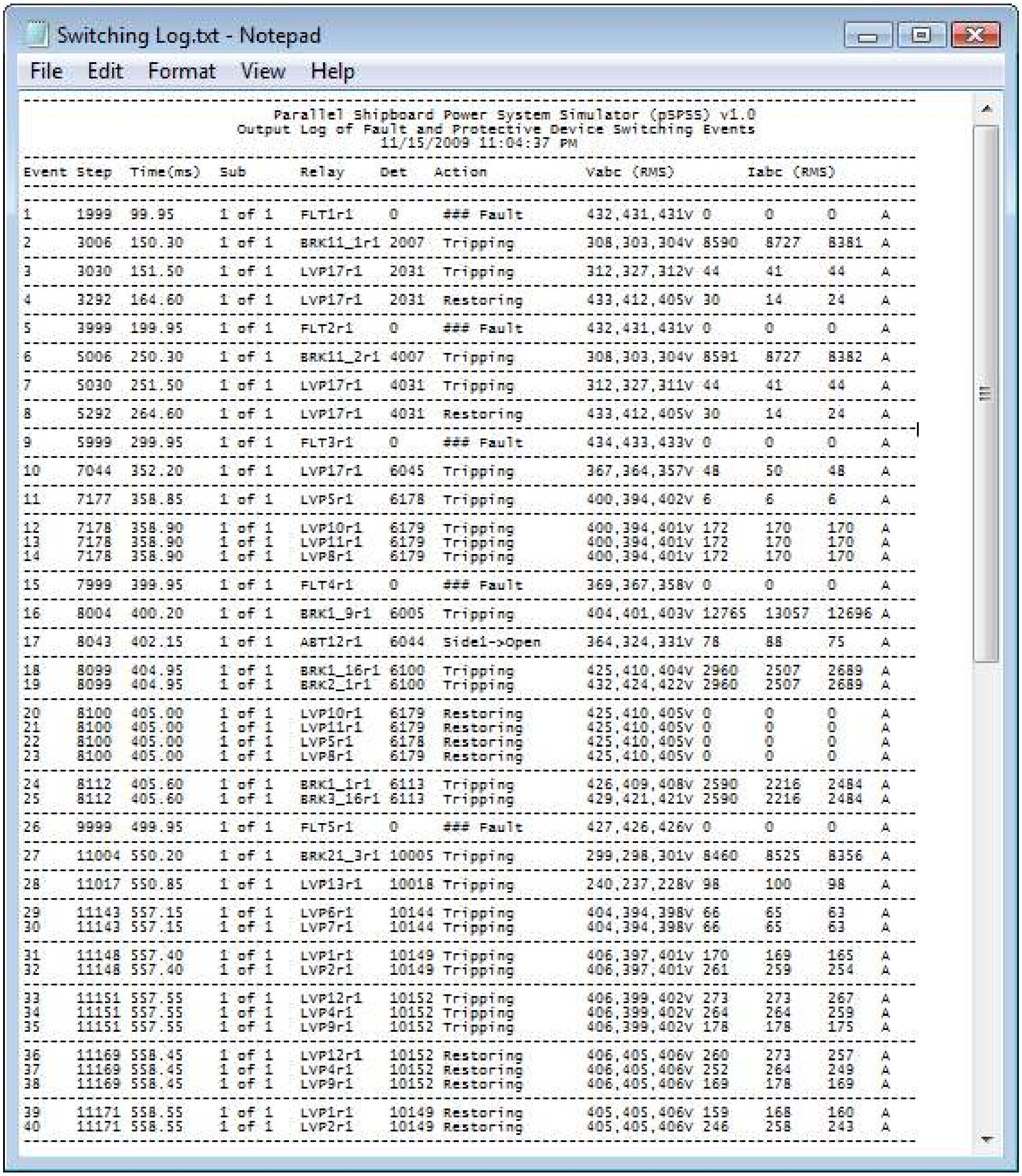
4.3.1 Simulation Waveforms

The battle damage scenario simulation produced (when Δt=50μs) 77 switching events: 68 protective device operations, and 9 faults; the switching events are listed in Fig. 4.3.4 and Fig. 4.3.5. The meaning of the column headers in Fig. 4.3.4 and Fig. 4.3.5 are given in Table IV.4. Select simulation waveforms are presented before the performance metrics results. The waveforms shown in this chapter are annotated to reduce their explanations.

TABLE IV.4 . COLUMN HEADER DESCRIPTIONS FOR SWITCHING EVENTS OUTPUT FILE

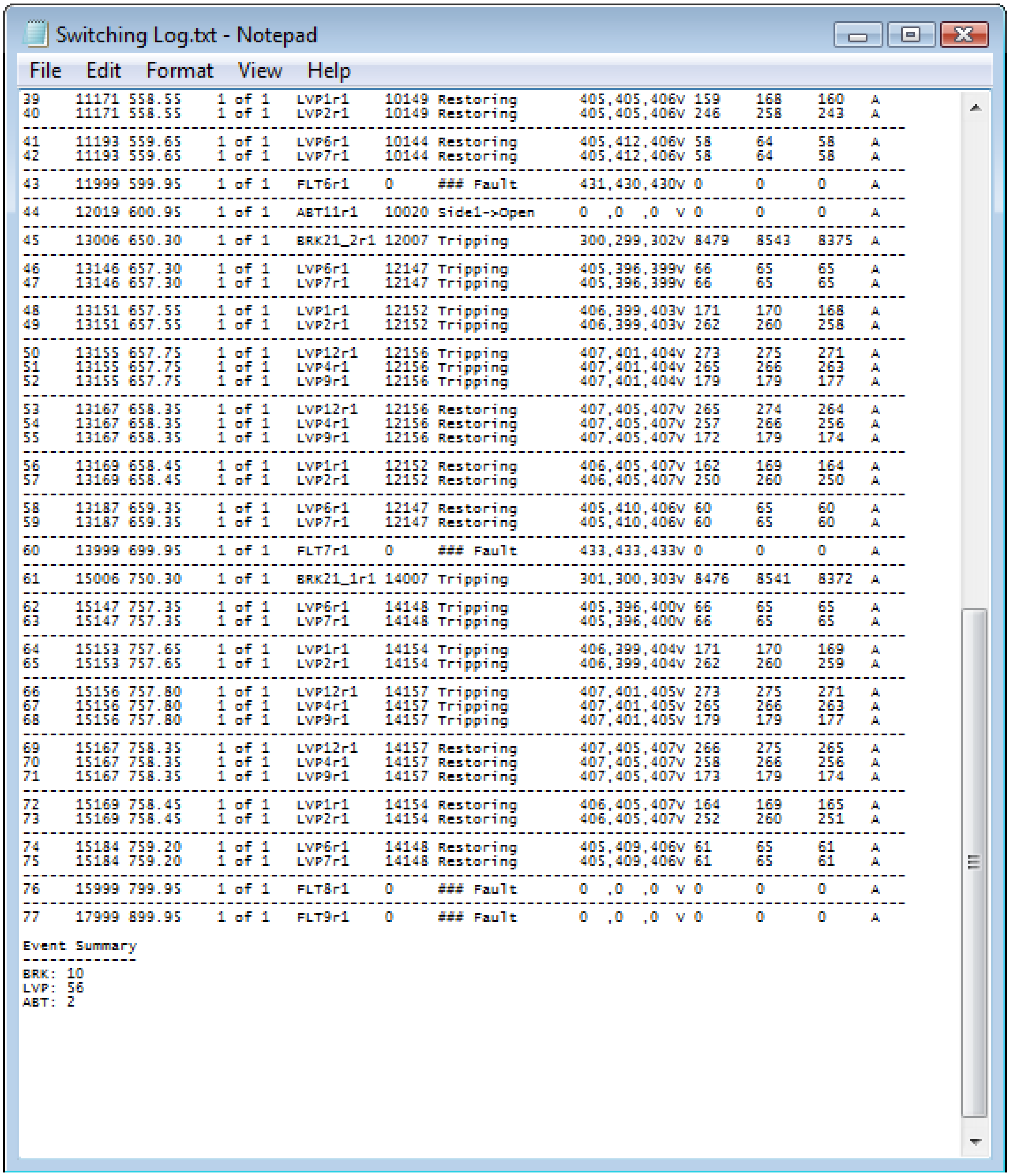
Column Header	Description
Event	Switching event number
Step	The time step number immediately before the event. At this time step the loop resistance matrix is updated
Time (ms)	The time corresponding to the time step number immediately before the event
Sub	The subsystem number where the event occurred
Relay	The relay number that operated (r 1 stands for side 1, r 2 for side 2, and r 3 for side 3)
Det	The time step number at which the overcurrent or undervoltage was detected by the relay
Action	The action that occurred at the present event
Vabc (RMS)	The last measured RMS voltage made by at the relay before the event occurred
Iabc (RMS)	The last measured RMS current made by at the relay before the event occurred

The simulation's voltage and current envelope for $t \in [0,1]\text{s}$, as measured at the terminals of generators 1 and 2 (GEN1 and GEN2) are shown in Fig. 4.3.6 and Fig. 4.3.7, respectively. Since generator 3 (GEN3) was disconnected, waveforms are not shown for GEN3. The three-phase waveforms in Fig. 4.3.6 and Fig. 4.3.7 show the system's response at a high-level, where the generator voltages and the total current injection into the system can be seen.



```
-----------------------------------------------------------------------------------------------------
                          Parallel Shipboard Power System Simulator (pSPSS) v1.0
                      Output Log of Fault and Protective Device Switching Events
                                       11/15/2009 11:04:37 PM
-----------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub        Relay      Det    Action            Vabc (RMS)       Iabc (RMS)
-----------------------------------------------------------------------------------------------------
-----------------------------------------------------------------------------------------------------
1      1999   99.95    1 of 1    FLT1r1      0      ### Fault        432,431,431v 0       0       0      A
-----------------------------------------------------------------------------------------------------
2      3006   150.30   1 of 1    BRK11_1r1  2007    Tripping         308,303,304v 8590    8727    8381   A
-----------------------------------------------------------------------------------------------------
3      3030   151.50   1 of 1    LVP17r1    2031    Tripping         312,327,312v 44      41      44     A
-----------------------------------------------------------------------------------------------------
4      3292   164.60   1 of 1    LVP17r1    2031    Restoring        433,412,405v 30      14      24     A
-----------------------------------------------------------------------------------------------------
5      3999   199.95   1 of 1    FLT2r1      0      ### Fault        432,431,431v 0       0       0      A
-----------------------------------------------------------------------------------------------------
6      5006   250.30   1 of 1    BRK11_2r1  4007    Tripping         308,303,304v 8591    8727    8382   A
-----------------------------------------------------------------------------------------------------
7      5030   251.50   1 of 1    LVP17r1    4031    Tripping         312,327,311v 44      41      44     A
-----------------------------------------------------------------------------------------------------
8      5292   264.60   1 of 1    LVP17r1    4031    Restoring        433,412,405v 30      14      24     A
-----------------------------------------------------------------------------------------------------
9      5999   299.95   1 of 1    FLT3r1      0      ### Fault        434,433,433v 0       0       0      A
-----------------------------------------------------------------------------------------------------
10     7044   352.20   1 of 1    LVP17r1    6045    Tripping         367,364,357v 48      50      48     A
-----------------------------------------------------------------------------------------------------
11     7177   358.85   1 of 1    LVP5r1     6178    Tripping         400,394,402v 6       6       6      A
-----------------------------------------------------------------------------------------------------
12     7178   358.90   1 of 1    LVP10r1    6179    Tripping         400,394,401v 172     170     170    A
13     7178   358.90   1 of 1    LVP11r1    6179    Tripping         400,394,401v 172     170     170    A
14     7178   358.90   1 of 1    LVP8r1     6179    Tripping         400,394,401v 172     170     170    A
-----------------------------------------------------------------------------------------------------
15     7999   399.95   1 of 1    FLT4r1      0      ### Fault        369,367,358v 0       0       0      A
-----------------------------------------------------------------------------------------------------
16     8004   400.20   1 of 1    BRK1_9r1   6005    Tripping         404,401,403v 12765   13057   12696  A
-----------------------------------------------------------------------------------------------------
17     8043   402.15   1 of 1    ABT12r1    6044    Side1->Open      364,324,331v 78      88      75     A
-----------------------------------------------------------------------------------------------------
18     8099   404.95   1 of 1    BRK1_16r1  6100    Tripping         425,410,404v 2960    2507    2689   A
19     8099   404.95   1 of 1    BRK2_1r1   6100    Tripping         432,424,422v 2960    2507    2689   A
-----------------------------------------------------------------------------------------------------
20     8100   405.00   1 of 1    LVP10r1    6179    Restoring        425,410,405v 0       0       0      A
21     8100   405.00   1 of 1    LVP11r1    6179    Restoring        425,410,405v 0       0       0      A
22     8100   405.00   1 of 1    LVP5r1     6178    Restoring        425,410,405v 0       0       0      A
23     8100   405.00   1 of 1    LVP8r1     6179    Restoring        425,410,405v 0       0       0      A
-----------------------------------------------------------------------------------------------------
24     8112   405.60   1 of 1    BRK1_1r1   6113    Tripping         426,409,408v 2590    2216    2484   A
25     8112   405.60   1 of 1    BRK3_16r1  6113    Tripping         429,421,421v 2590    2216    2484   A
-----------------------------------------------------------------------------------------------------
26     9999   499.95   1 of 1    FLT5r1      0      ### Fault        427,426,426v 0       0       0      A
-----------------------------------------------------------------------------------------------------
27     11004  550.20   1 of 1    BRK21_3r1  10005   Tripping         299,298,301v 8460    8525    8356   A
-----------------------------------------------------------------------------------------------------
28     11017  550.85   1 of 1    LVP13r1    10018   Tripping         240,237,228v 98      100     98     A
-----------------------------------------------------------------------------------------------------
29     11143  557.15   1 of 1    LVP6r1     10144   Tripping         404,394,398v 66      65      63     A
30     11143  557.15   1 of 1    LVP7r1     10144   Tripping         404,394,398v 66      65      63     A
-----------------------------------------------------------------------------------------------------
31     11148  557.40   1 of 1    LVP1r1     10149   Tripping         406,397,401v 170     169     165    A
32     11148  557.40   1 of 1    LVP2r1     10149   Tripping         406,397,401v 261     259     254    A
-----------------------------------------------------------------------------------------------------
33     11151  557.55   1 of 1    LVP12r1    10152   Tripping         406,399,402v 273     273     267    A
34     11151  557.55   1 of 1    LVP4r1     10152   Tripping         406,399,402v 264     264     259    A
35     11151  557.55   1 of 1    LVP9r1     10152   Tripping         406,399,402v 178     178     175    A
-----------------------------------------------------------------------------------------------------
36     11169  558.45   1 of 1    LVP12r1    10152   Restoring        406,405,406v 260     273     257    A
37     11169  558.45   1 of 1    LVP4r1     10152   Restoring        406,405,406v 252     264     249    A
38     11169  558.45   1 of 1    LVP9r1     10152   Restoring        406,405,406v 169     178     169    A
-----------------------------------------------------------------------------------------------------
39     11171  558.55   1 of 1    LVP1r1     10149   Restoring        405,405,406v 159     168     160    A
40     11171  558.55   1 of 1    LVP2r1     10149   Restoring        405,405,406v 246     258     243    A
-----------------------------------------------------------------------------------------------------
```

Fig. 4.3.4. Summary of switching events (1 of 2)



```
39    11171 558.55    1 of 1   LVP1r1    10149 Restoring      405,405,406v 159    168    160   A
40    11171 558.55    1 of 1   LVP2r1    10149 Restoring      405,405,406v 246    258    243   A
----------------------------------------------------------------------------------------------------
41    11193 559.65    1 of 1   LVP6r1    10144 Restoring      405,412,406v 58     64     58    A
42    11193 559.65    1 of 1   LVP7r1    10144 Restoring      405,412,406v 58     64     58    A
----------------------------------------------------------------------------------------------------
43    11999 599.95    1 of 1   FLT6r1    0     ### Fault      431,430,430v 0      0      0     A
----------------------------------------------------------------------------------------------------
44    12019 600.95    1 of 1   ABT11r1   10020 Side1->Open    0  ,0  ,0  v 0      0      0     A
----------------------------------------------------------------------------------------------------
45    13006 650.30    1 of 1   BRK21_2r1 12007 Tripping       300,299,302v 8479   8543   8375  A
----------------------------------------------------------------------------------------------------
46    13146 657.30    1 of 1   LVP6r1    12147 Tripping       405,396,399v 66     65     65    A
47    13146 657.30    1 of 1   LVP7r1    12147 Tripping       405,396,399v 66     65     65    A
----------------------------------------------------------------------------------------------------
48    13151 657.55    1 of 1   LVP1r1    12152 Tripping       406,399,403v 171    170    168   A
49    13151 657.55    1 of 1   LVP2r1    12152 Tripping       406,399,403v 262    260    258   A
----------------------------------------------------------------------------------------------------
50    13155 657.75    1 of 1   LVP12r1   12156 Tripping       407,401,404v 273    275    271   A
51    13155 657.75    1 of 1   LVP4r1    12156 Tripping       407,401,404v 265    266    263   A
52    13155 657.75    1 of 1   LVP9r1    12156 Tripping       407,401,404v 179    179    177   A
----------------------------------------------------------------------------------------------------
53    13167 658.35    1 of 1   LVP12r1   12156 Restoring      407,405,407v 265    274    264   A
54    13167 658.35    1 of 1   LVP4r1    12156 Restoring      407,405,407v 257    266    256   A
55    13167 658.35    1 of 1   LVP9r1    12156 Restoring      407,405,407v 172    179    174   A
----------------------------------------------------------------------------------------------------
56    13169 658.45    1 of 1   LVP1r1    12152 Restoring      406,405,407v 162    169    164   A
57    13169 658.45    1 of 1   LVP2r1    12152 Restoring      406,405,407v 250    260    250   A
----------------------------------------------------------------------------------------------------
58    13187 659.35    1 of 1   LVP6r1    12147 Restoring      405,410,406v 60     65     60    A
59    13187 659.35    1 of 1   LVP7r1    12147 Restoring      405,410,406v 60     65     60    A
----------------------------------------------------------------------------------------------------
60    13999 699.95    1 of 1   FLT7r1    0     ### Fault      433,433,433v 0      0      0     A
----------------------------------------------------------------------------------------------------
61    15006 750.30    1 of 1   BRK21_1r1 14007 Tripping       301,300,303v 8476   8541   8372  A
----------------------------------------------------------------------------------------------------
62    15147 757.35    1 of 1   LVP6r1    14148 Tripping       405,396,400v 66     65     65    A
63    15147 757.35    1 of 1   LVP7r1    14148 Tripping       405,396,400v 66     65     65    A
----------------------------------------------------------------------------------------------------
64    15153 757.65    1 of 1   LVP1r1    14154 Tripping       406,399,404v 171    170    169   A
65    15153 757.65    1 of 1   LVP2r1    14154 Tripping       406,399,404v 262    260    259   A
----------------------------------------------------------------------------------------------------
66    15156 757.80    1 of 1   LVP12r1   14157 Tripping       407,401,405v 273    275    271   A
67    15156 757.80    1 of 1   LVP4r1    14157 Tripping       407,401,405v 265    266    263   A
68    15156 757.80    1 of 1   LVP9r1    14157 Tripping       407,401,405v 179    179    177   A
----------------------------------------------------------------------------------------------------
69    15167 758.35    1 of 1   LVP12r1   14157 Restoring      407,405,407v 266    275    265   A
70    15167 758.35    1 of 1   LVP4r1    14157 Restoring      407,405,407v 258    266    256   A
71    15167 758.35    1 of 1   LVP9r1    14157 Restoring      407,405,407v 173    179    174   A
----------------------------------------------------------------------------------------------------
72    15169 758.45    1 of 1   LVP1r1    14154 Restoring      406,405,407v 164    169    165   A
73    15169 758.45    1 of 1   LVP2r1    14154 Restoring      406,405,407v 252    260    251   A
----------------------------------------------------------------------------------------------------
74    15184 759.20    1 of 1   LVP6r1    14148 Restoring      405,409,406v 61     65     61    A
75    15184 759.20    1 of 1   LVP7r1    14148 Restoring      405,409,406v 61     65     61    A
----------------------------------------------------------------------------------------------------
76    15999 799.95    1 of 1   FLT8r1    0     ### Fault      0  ,0  ,0  v 0      0      0     A
----------------------------------------------------------------------------------------------------
77    17999 899.95    1 of 1   FLT9r1    0     ### Fault      0  ,0  ,0  v 0      0      0     A

Event Summary
-------------
BRK: 10
LVP: 56
ABT: 2
```

Fig. 4.3.5. Summary of switching events (2 of 2)

The times at which the nine faults closed-in are labeled on the current plots. From the fault locations shown on the schematic in Fig. 4.3.1, and from the envelope response shown in Fig. 4.3.6, faults FLT 1, 2, 3, and 4 are closer to (and supplied mainly by) GEN1 except for FLT4. Fault location 4 (FLT4) was not supplied from any generator for long because its upstream breaker BRK1_9 on switchboard 1 (SB1) opened moments after FLT4 was applied. The list of switching events in Fig. 4.3.4 show that BRK1_9 tripped at $t = 400.2\text{ms}$, that is, briefly after FLT4 was applied at $t = 400\text{ms}$.

An overlay of bus tie 12 (p=1 vs. p=12; c=2; Δt=50μs) and bus tie 13's (p=1 vs. p=7; c=4; Δt=75μs) envelope waveforms are shown in Fig. 4.3.8 and Fig. 4.3.9, which show inter-switchboard flows during the first three faults near SB1. Before the faults were applied (i.e., $t < 0.1\text{s}$) the bus tie flows were small as expected from a ring bus topology. During the faults the bus ties served as paths from generators to faults and initiated the bus tie breakers timers. Ring breakers BRK1_16 and BRK2_1 tripped simultaneously at $t = 404.95\text{ms}$, which opened bus tie 21 and the supply from GEN2 to FLTs 1,2, 3, and 4 downstream of SB1. The ring breaker tripping are listed as events 18 and 19 in Fig. 4.3.4. Similarly for bus tie 31, breakers BRK1_1 and BRK3_16 opened the ring as given by events 24 and 25.

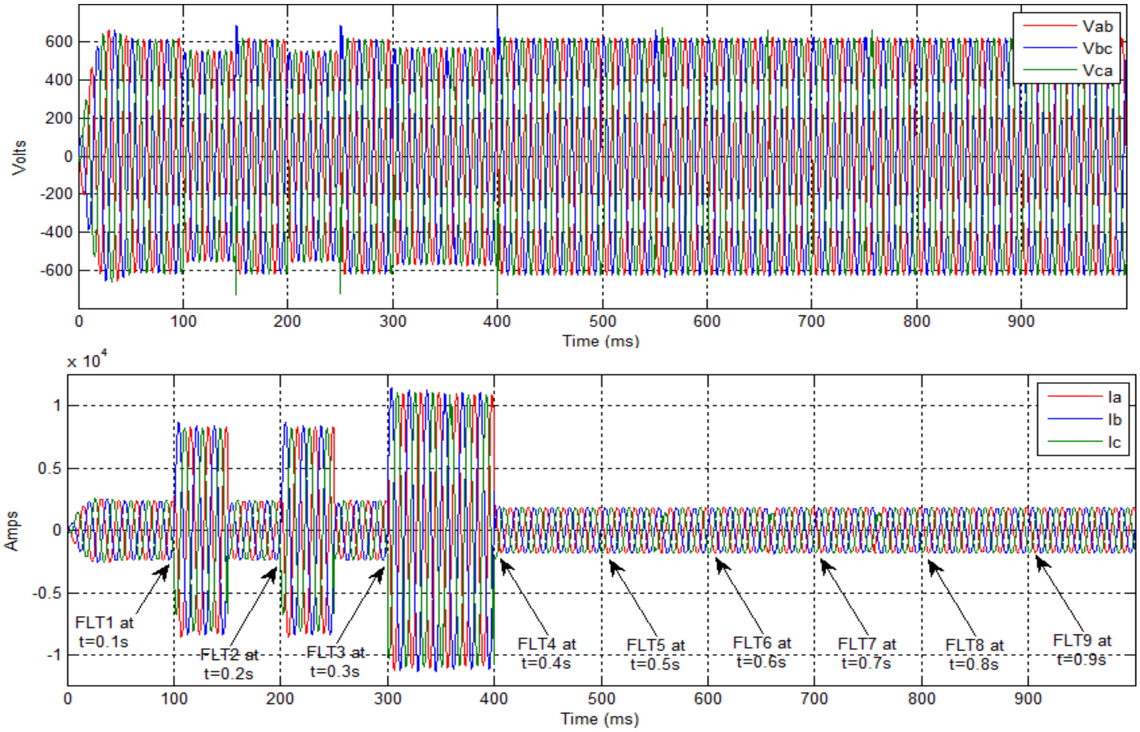


Fig. 4.3.6. Voltage and current measured from generator 1 {p=1; c=1; Δt=50μs}

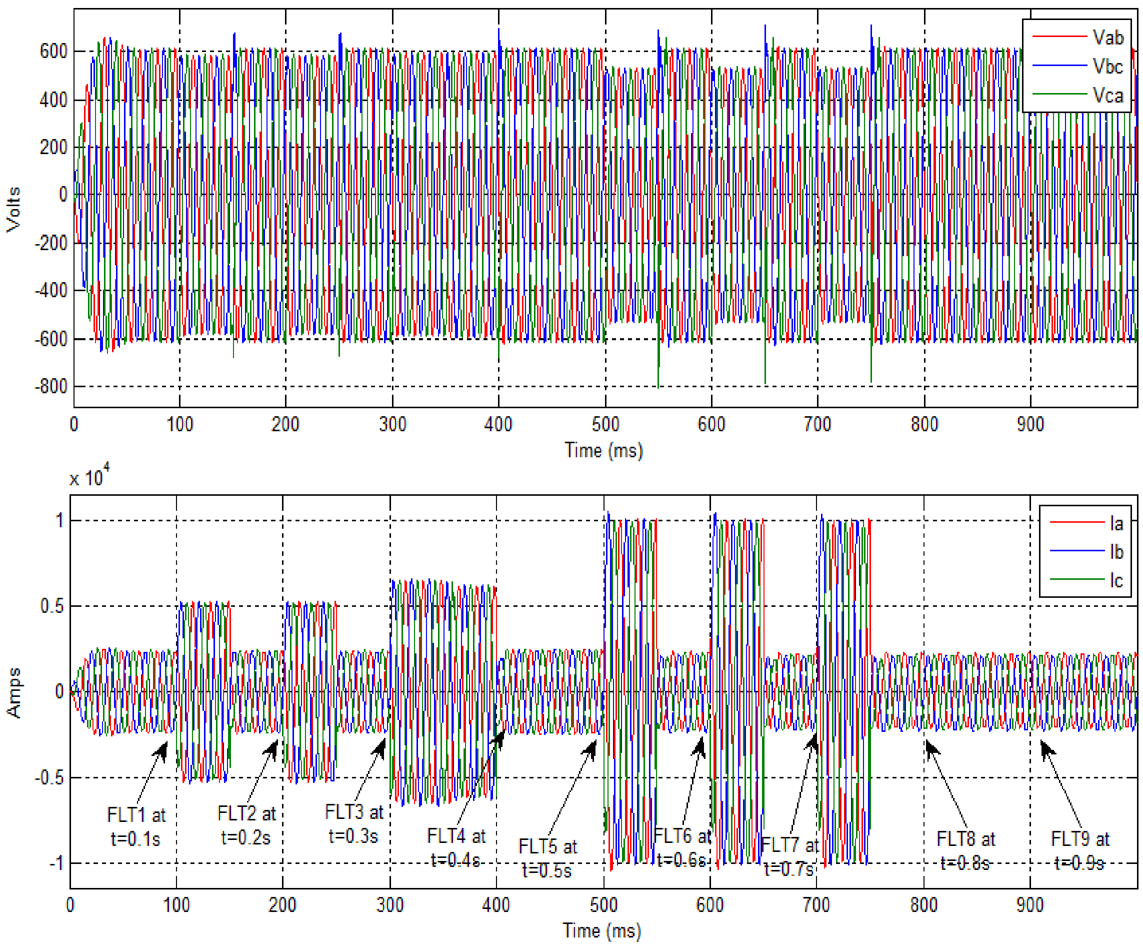


Fig. 4.3.7. Voltage and current measured from generator 2 {*p*=1; *c*=2; Δ*t*=50μs}

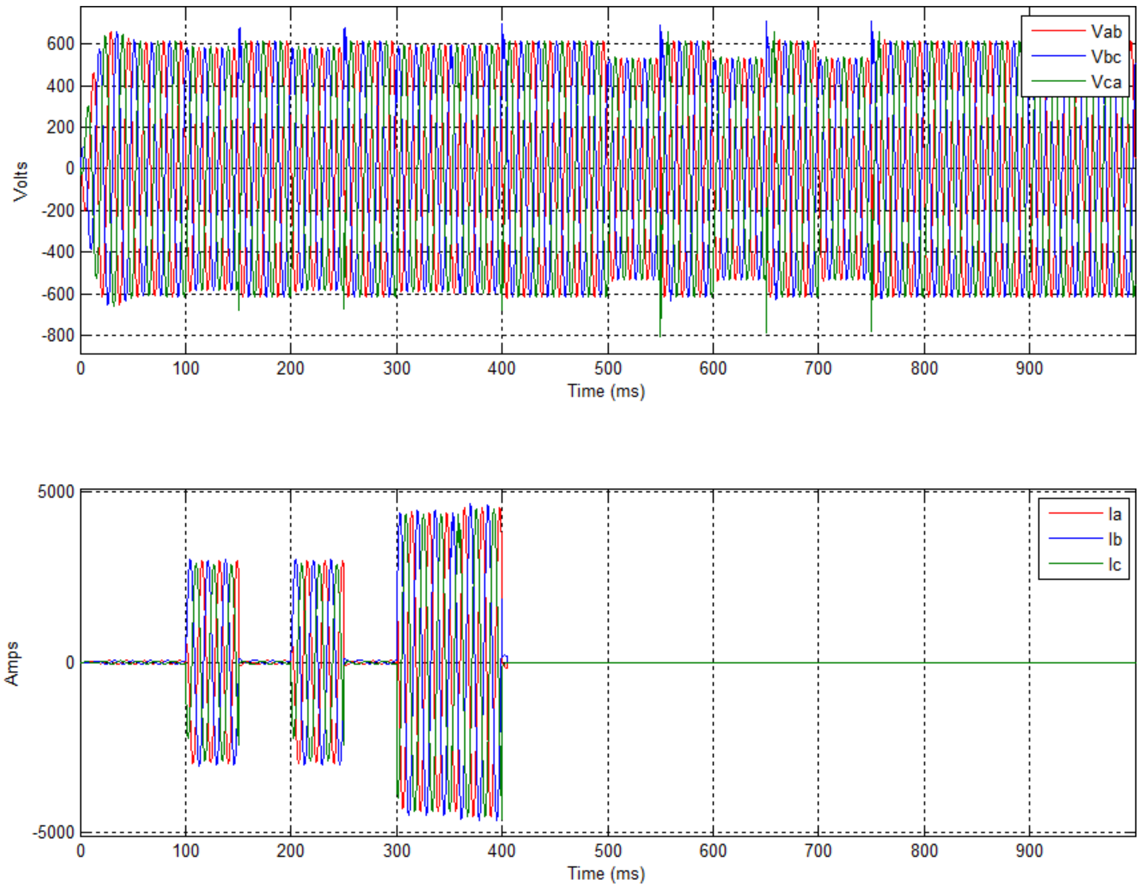


Fig. 4.3.8. Voltage and current: BRK2_1 (*p*=1 vs. *p*=12; *c*=3; Δ*t*=75μs)

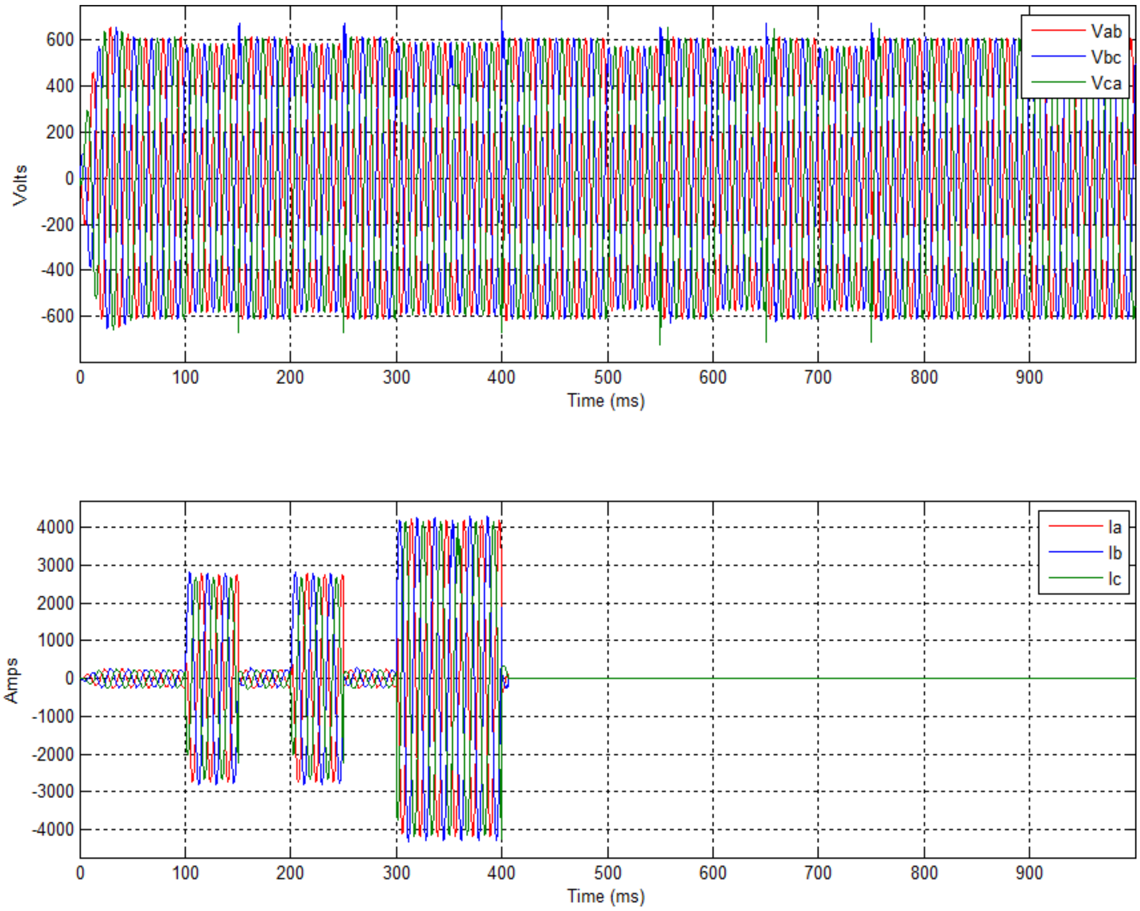


Fig. 4.3.9. Voltage and current: (*p*=1 vs. *p*=7; *c*=4; Δ*t*=75μs)

Application of FLT1 caused BRK11_1 operated at $t = 150.3$ms (event 2). The voltage and currents measured at load center 11 (LC11) due to said opening are overlaid in Fig. 4.3.10. The voltage transients due to BRK11_1's opening exhibit fast resonance due to the cables' small time constants. The voltage waveforms shown in Fig. 4.3.10.

are the common to all over-current relays connected from LC11. The current decay from BRK11's disconnection is shown on the lower part of Fig. 4.3.10. As BRK11_1 opened high resonant decaying currents were noted for a few milliseconds.

The resonant behavior shown in Fig. 4.3.10 is also common to other protective device openings throughout the system. At various points in the system, and every time a protective device opened, the same resonance was observed.

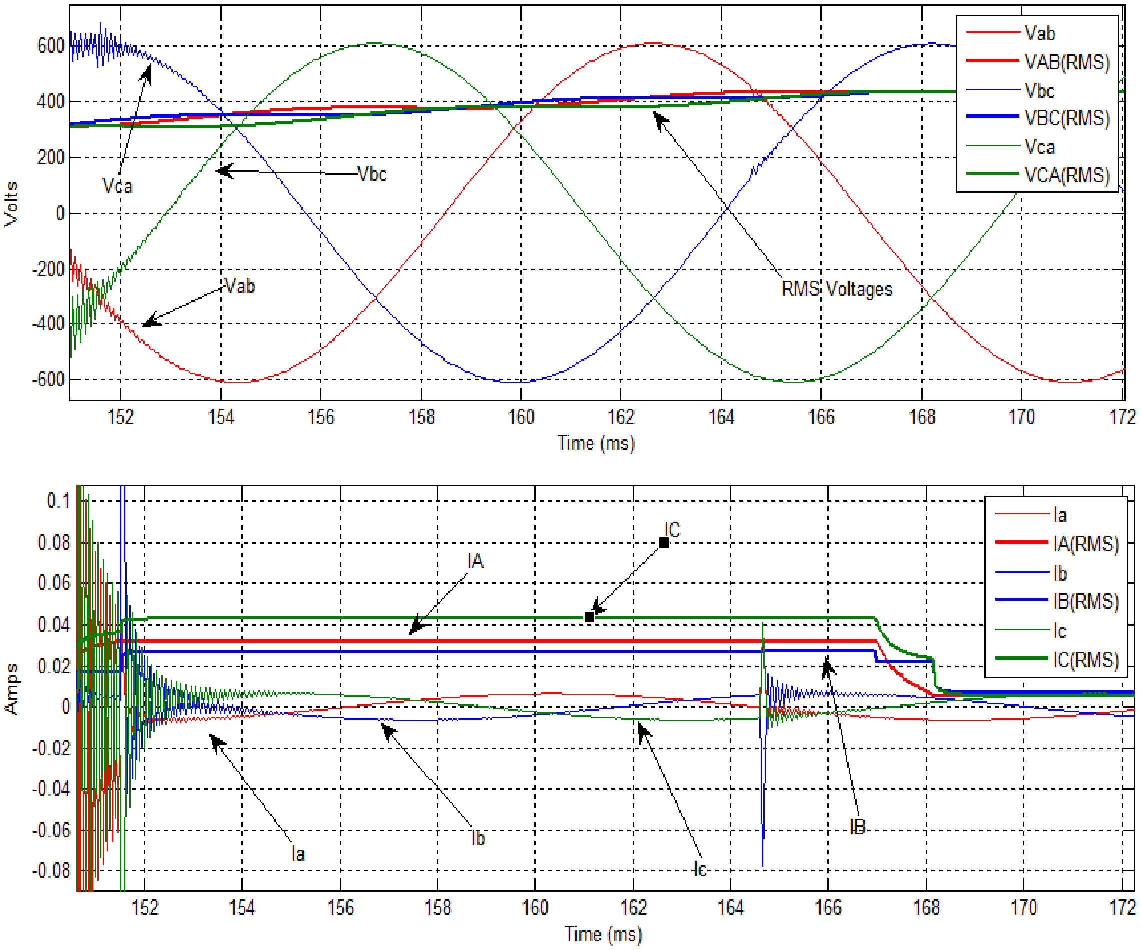


Fig. 4.3.10. Voltage and current: BRK11_1 as FLT1 was cleared

Shown in Fig. 4.3.11 are voltage overlays {p=1 vs. p=10; c=3; Δt=75μs} at LC11 and current through BRK11_2. The current through BRK11_2 is 0A prior to the fault because BRK11_2 is on MBT4's alternate path which is normally open. MBT4's normal path is connected from BRK31_3 on LC31. Also noted from Fig. 4.3.11 are the voltage dips caused by the faults.

Shown in Fig. 4.3.12 are voltage overlays {p=1 vs. p=6; c=2; Δt=50μs} for FLT3's voltage and the fault's line-to-line (LL) current. The current through FLT3 is 0A prior to the fault $\left(R_{fault} = 1\text{M}\Omega\right)$. When FLT3 was applied the fault LL current increased to a peak level of ~10kA as the fault resistance changed to $R_{fault} = 50\text{m}\Omega$. Also noted from Fig. 4.3.12 is the rate at which the RMS current increases. There are inherent delays in RMS computations which retards the moment when the relay detects the fault.

Shown in Fig. 4.3.13 are voltage overlays measured at SB1 {p=1 vs. p=5; c=1; Δt=500μs}and current overlays measured by BRK1_9. The current through BRK1_9 is the largest current detected during the simulation which occurs when FLT3 is applied. Faults FLT1 and FLT2 occurred downstream of LC11 and are electrically further from SB1 than FLT3 is. Fault 3 drew the largest current due to the proximity (electrically close) to SB1, and sunk in-feed current from GEN1 and GEN2.

Also noted from Fig. 4.3.13 are the voltage dips at SB1 due to the faults. The lengthiest voltage dip was caused by FLT3 because BRK1_9's time-delay setting is longer than for load-center relays (i.e., BRK1_9 took ~6 cycles (~0.1s) to react as shown by event 16).

From the select simulation waveforms presented, there is no apparent error between unpartitioned and partitioned simulation results. Following similar explanations as given for Fig. 4.3.6 through Fig. 4.3.13, voltage and current overlays for FLTs 4-9 are shown in Fig. 4.3.14 through Fig. 4.3.19, respectively. The generators response to each fault were labeled in Fig. 4.3.6 and Fig. 4.3.7, and the fault locations shown in Fig. 4.3.1.

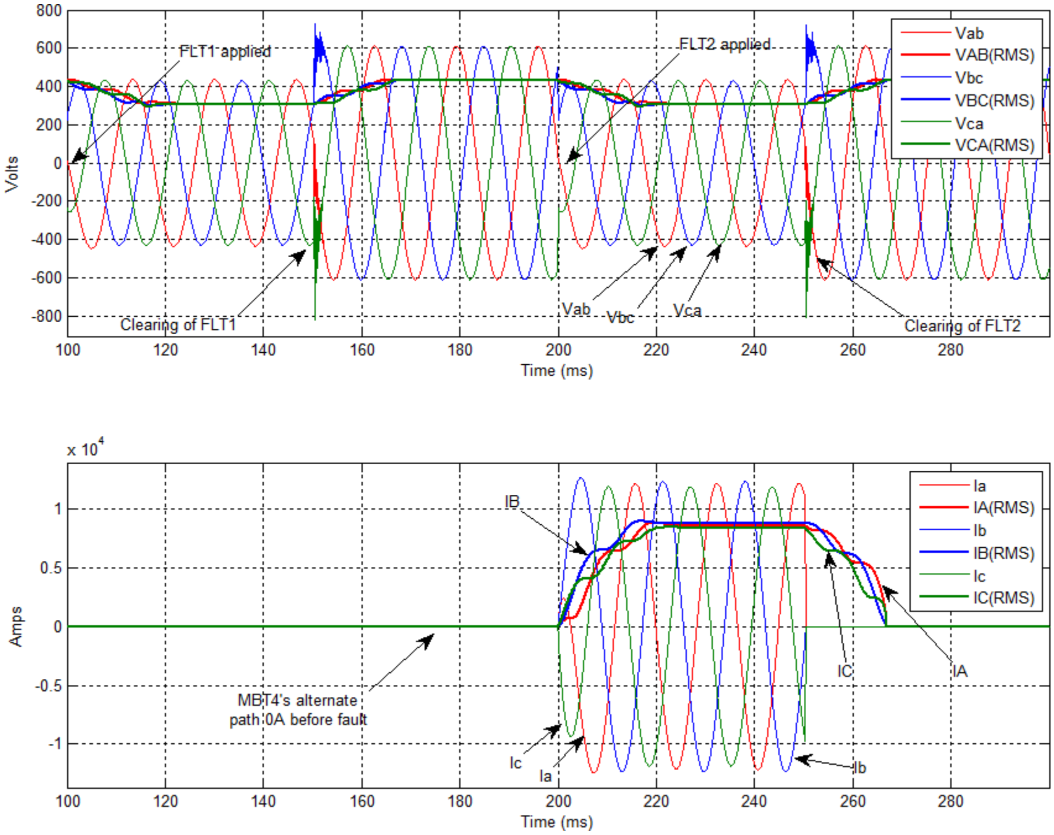


Fig. 4.3.11. Voltage and current: BRK11_2 (*p*=1 vs. *p*=3; *c*=2; Δ*t*=250μs)

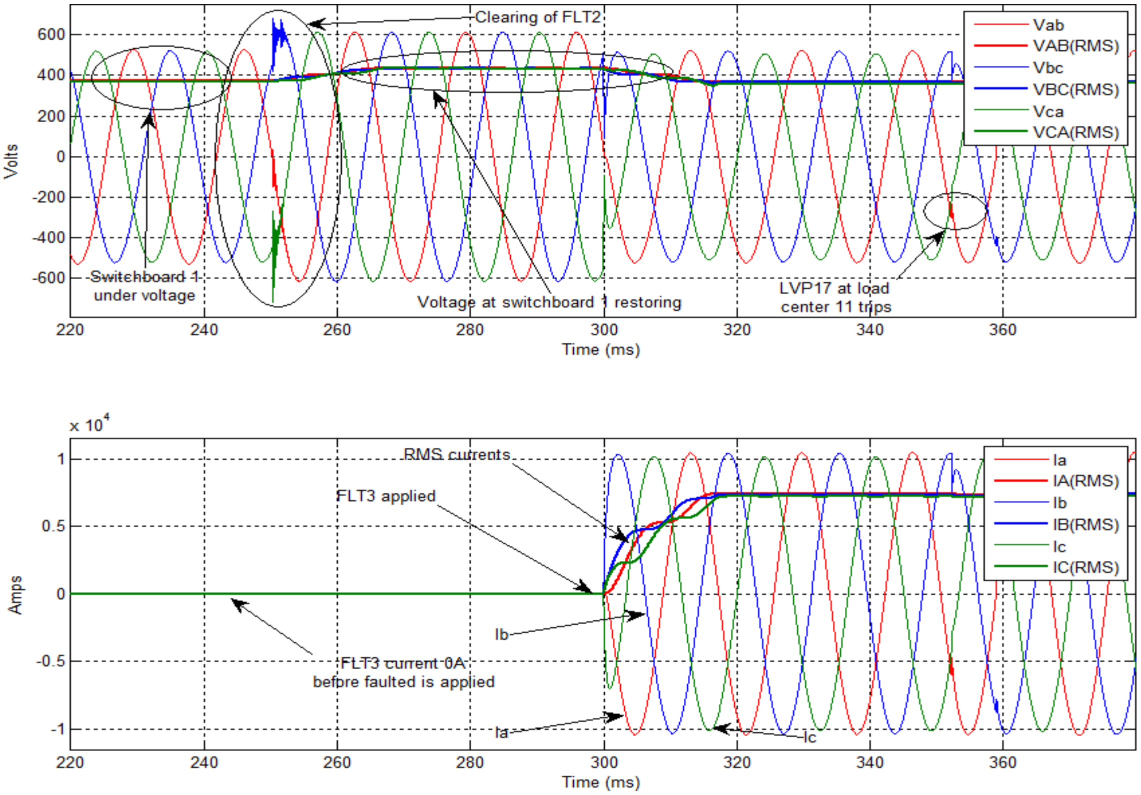


Fig. 4.3.12. Voltage and phase current: FLT3's (*p*=1 vs. *p*=6; *c*=2; Δ*t*=50μs)

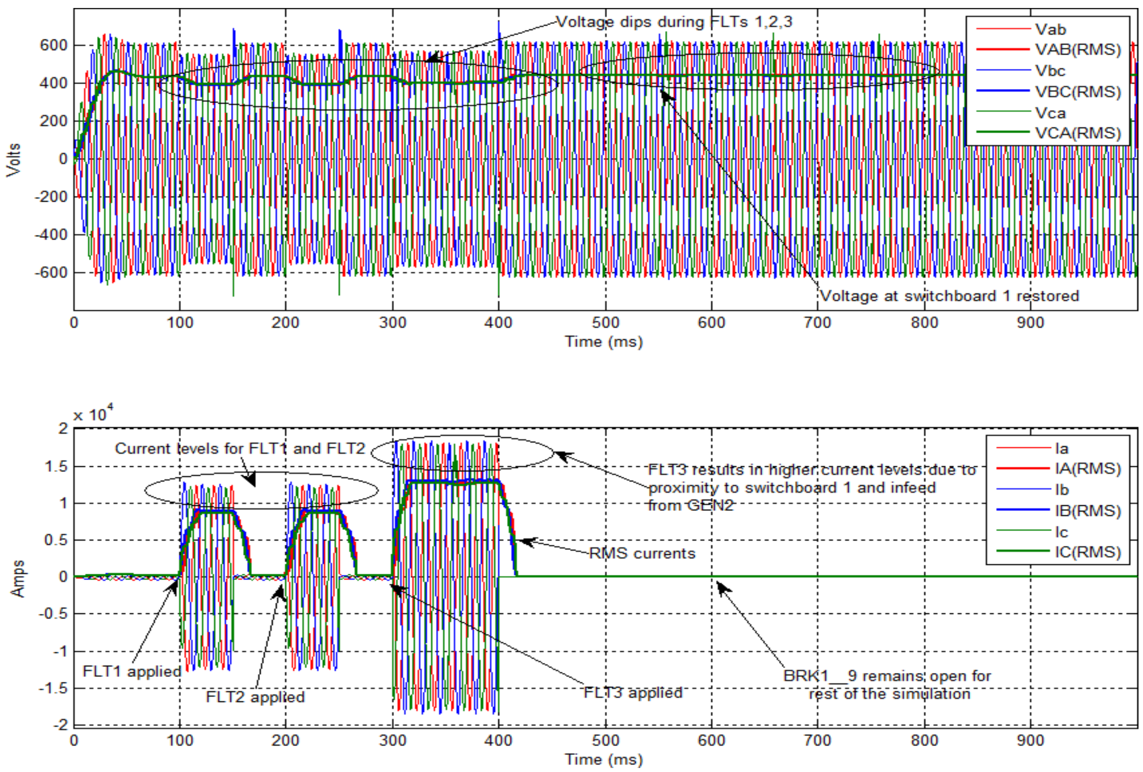


Fig. 4.3.13. Voltage and current: BRK1_9 (p=1 vs. p=5; c=1; Δt=500µs)

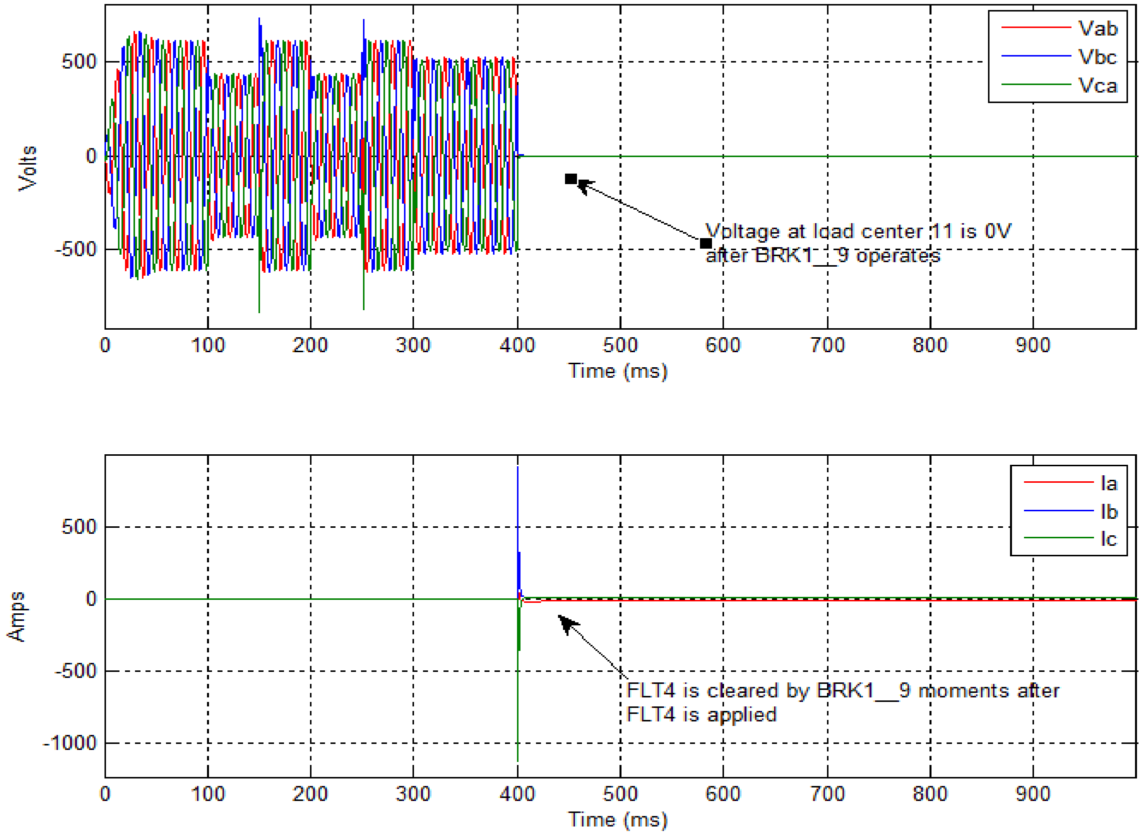


Fig. 4.3.14. Voltage and phase-current: FLT4's (*p*=1 vs. *p*=3; *c*=3; Δ*t*=100µs)

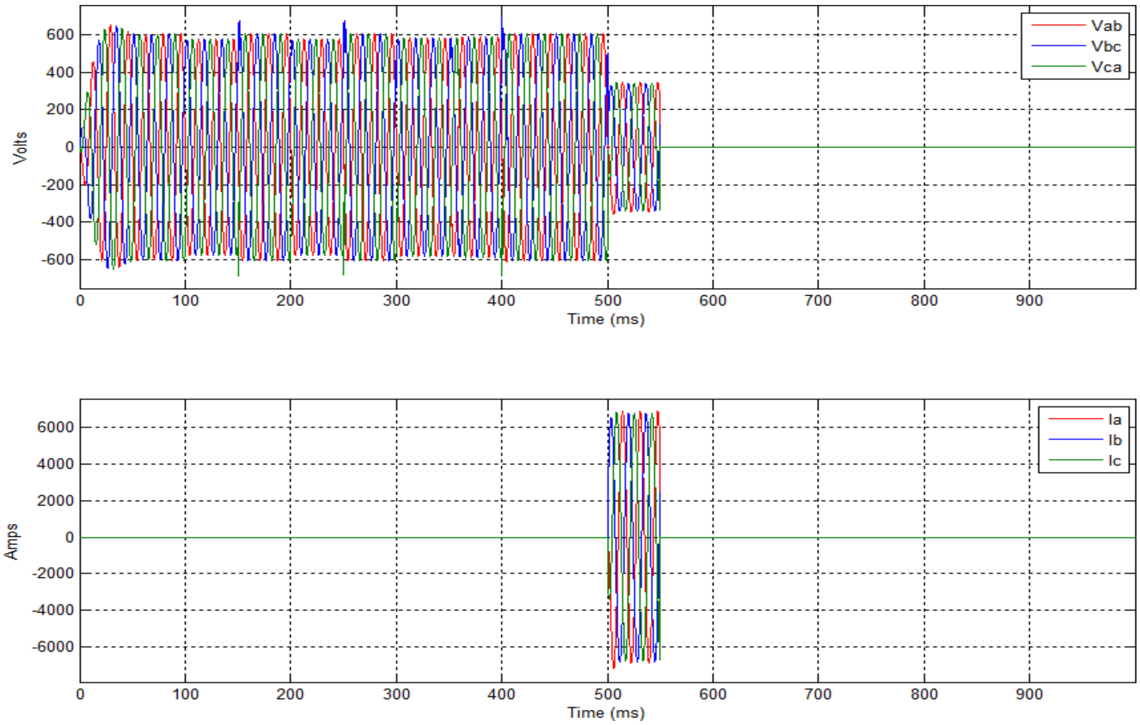


Fig. 4.3.15. Voltage and phase-current: FLT5 (p=1 vs. p=2; c=2; Δt=100μs)

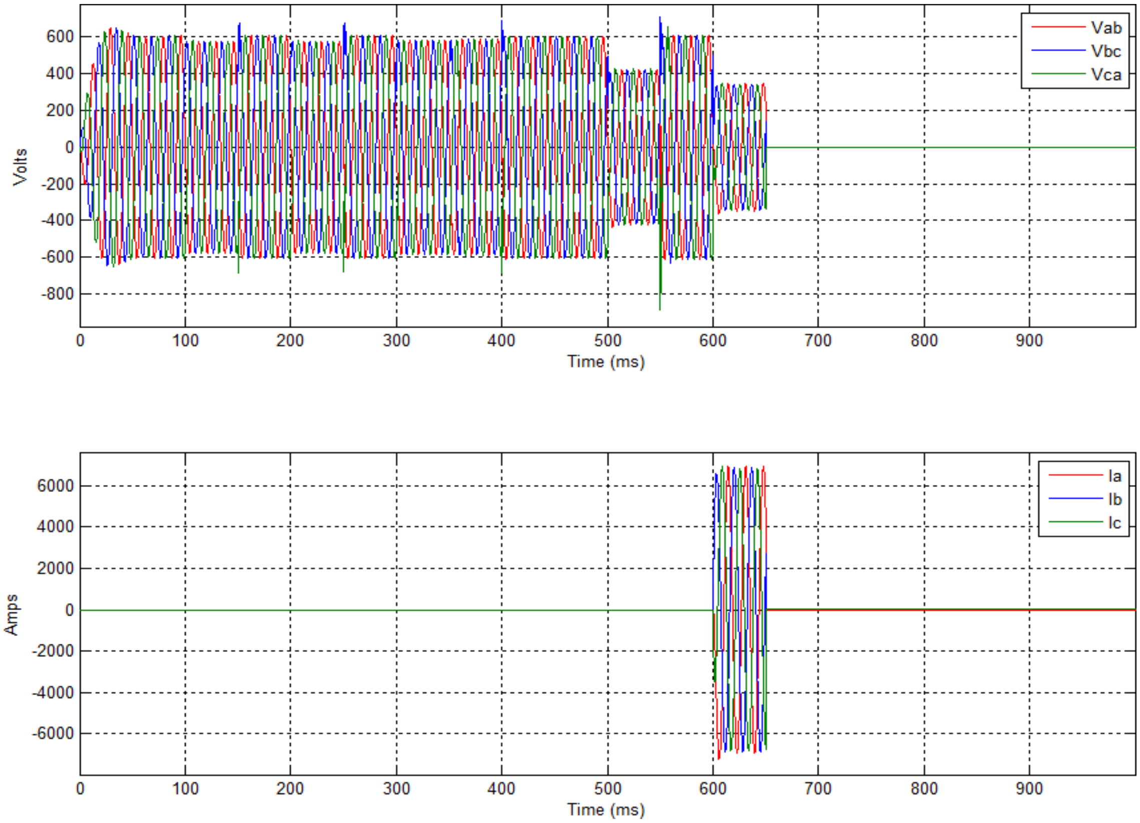


Fig. 4.3.16. Voltage and phase-current: FLT6 (*p*=1 vs. *p*=3; *c*=1; Δ*t*=75μs)

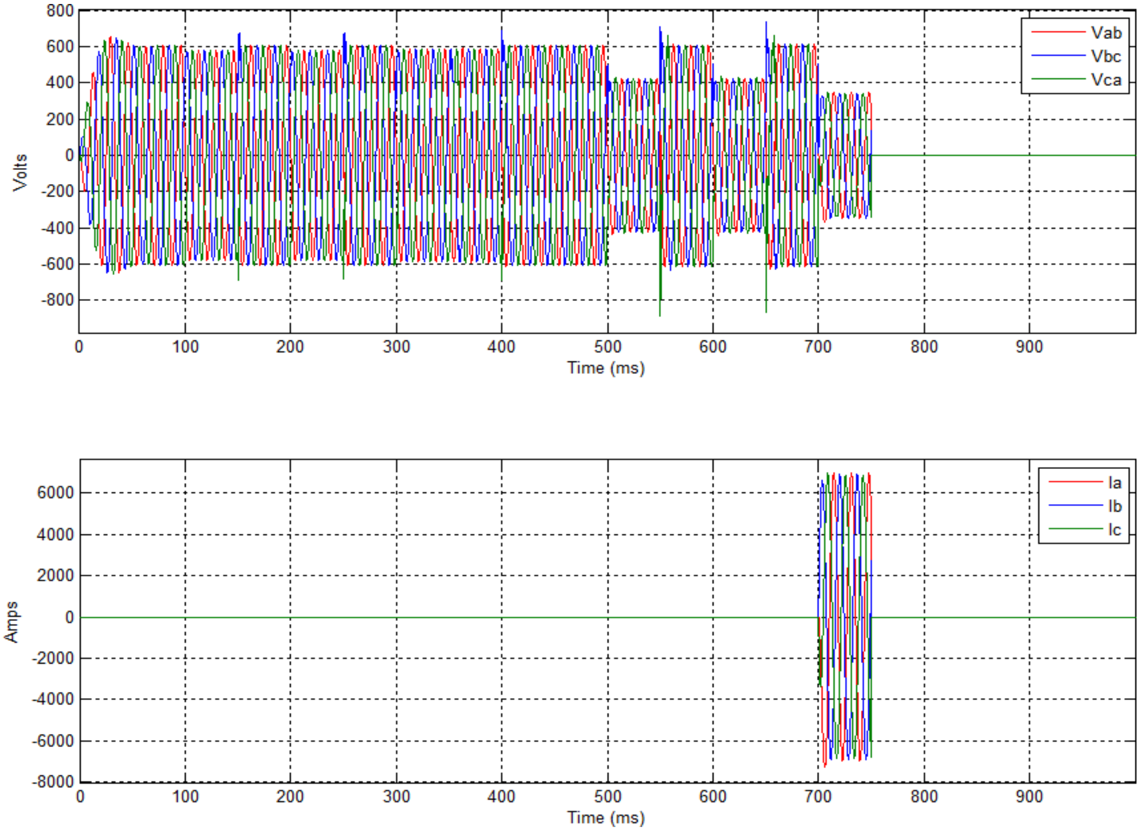


Fig. 4.3.17. Voltage and phase-current: FLT7 (p=1 vs. p=6; c=3; Δt=100μs)

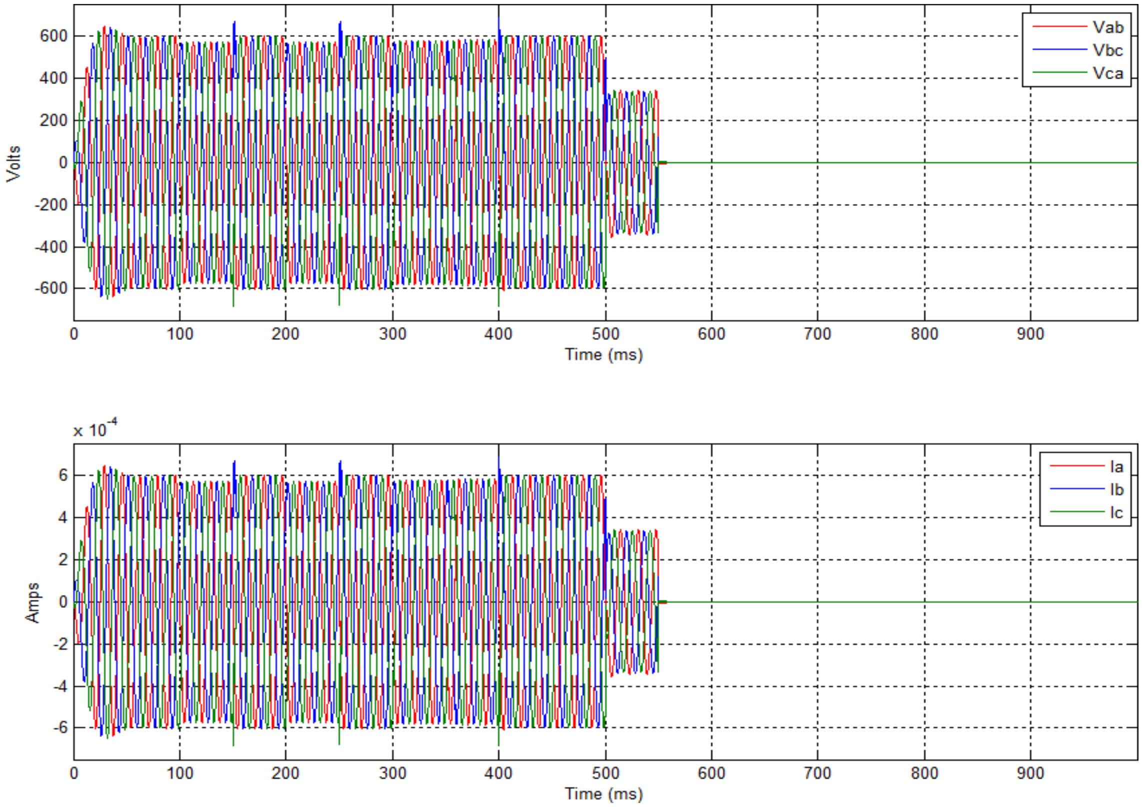


Fig. 4.3.18. Voltage and phase-current FLT8: (p=1 vs. p=12; c=4; Δt=50μs)

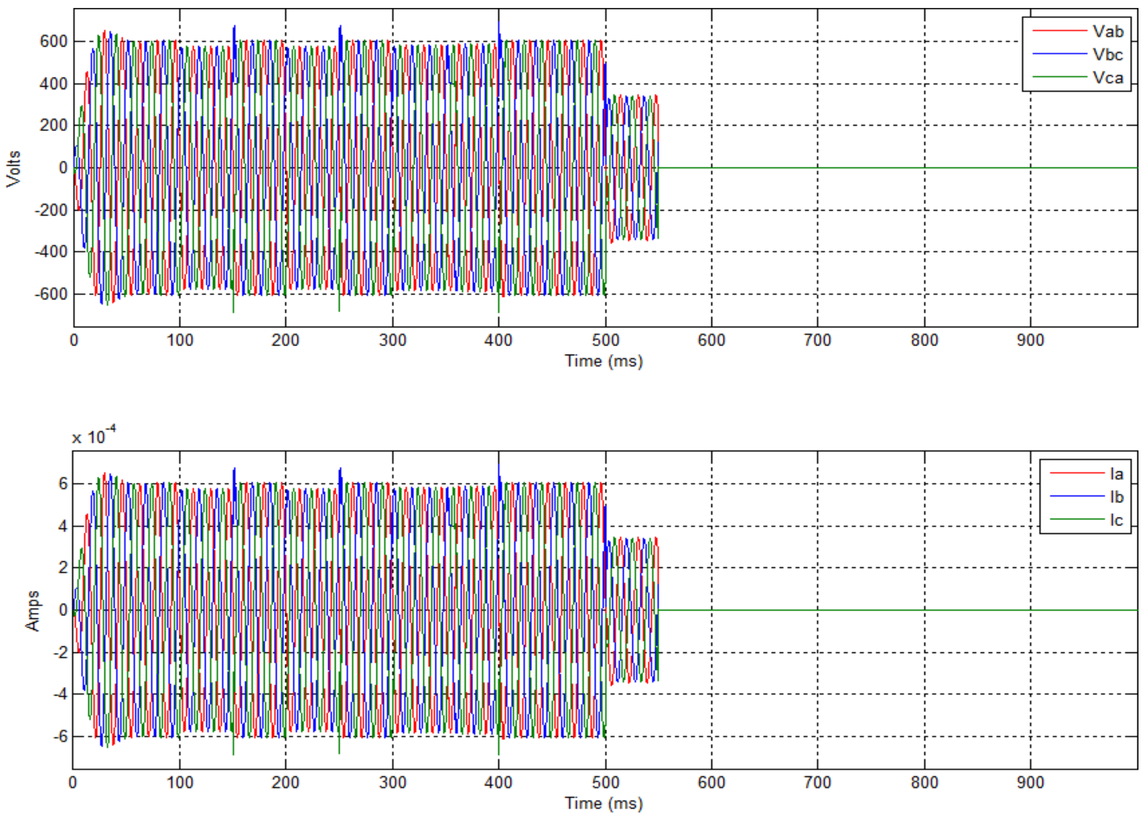


Fig. 4.3.19. Voltage and phase-current: FLT9 (p=1 vs. p=3; c=1; Δt=250μs)

4.3.2 Performance Metric 1 Results

4.3.2.1 Case Study Results

The simulation run-time and speed gain for the 42 simulations of PM1 are shown in Fig. 4.3.20. The unpartitioned (p=1) simulation's run-time was $t_{\text{unpartitioned}} = 2{,}709\text{s}$ (45mins; 09secs) when c=1. When p=2, the simulation's run- time reduced to 15 minutes 30 seconds for c=1, and to 10 minutes 12 seconds for c=2. It is interesting to note that partitioning alone (i.e., p=2 holding c=1 constant) decreased run-time by ~30 minutes. This result indicates that speed gain is possible without parallelizing simulations, and suggests that sequential simulations of partitioned power systems should be optimized before parallelizing the simulations. Following the run-time trend atop of Fig. 4.3.20, the shortest run-time was 2 minutes 18 seconds when p=11 and c=4. With Δt=50μs, and before partitioning the SPS, simulations took ~45 minutes; after partitioning, run-time reduced to ~2 minutes.

The smallest run-time of 2 minutes 18 seconds corresponds to a maximum speed gain of $K_{speed} = 19.63$. Since $K_{speed} > p$ the speed gain is said to be super-linear [35]. It is also noted that c=4 does not always result in the highest speed gain for all p, which is a counter intuitive result. There is a general belief that speed gains always increments if c does. For example, when p=4 a higher K_{speed} was obtained with c=2 and c=3 than with c=4. This result indicates that K_{speed} is not only a function of c, but of both of p and c. Referring to the lower part of Fig. 4.3.20, K_{speed} increased asymptotically for $p \in [2,11] \forall c$ but diminished when p>11 $\forall c$. This result indicates that p=11 is a good number, if not optimal, number of partitions for the AC-Radial SPS model used and the case study conducted.

The simulation error for PM1 was assessed using (4.2). The number of cores c does not influence the accuracy of the simulation; it only influences run-time. A summary of the errors obtained for PM1 are plotted using on a base-10 logarithmic scale in Fig. 4.3.21 and are tabulated in Table IV.5.

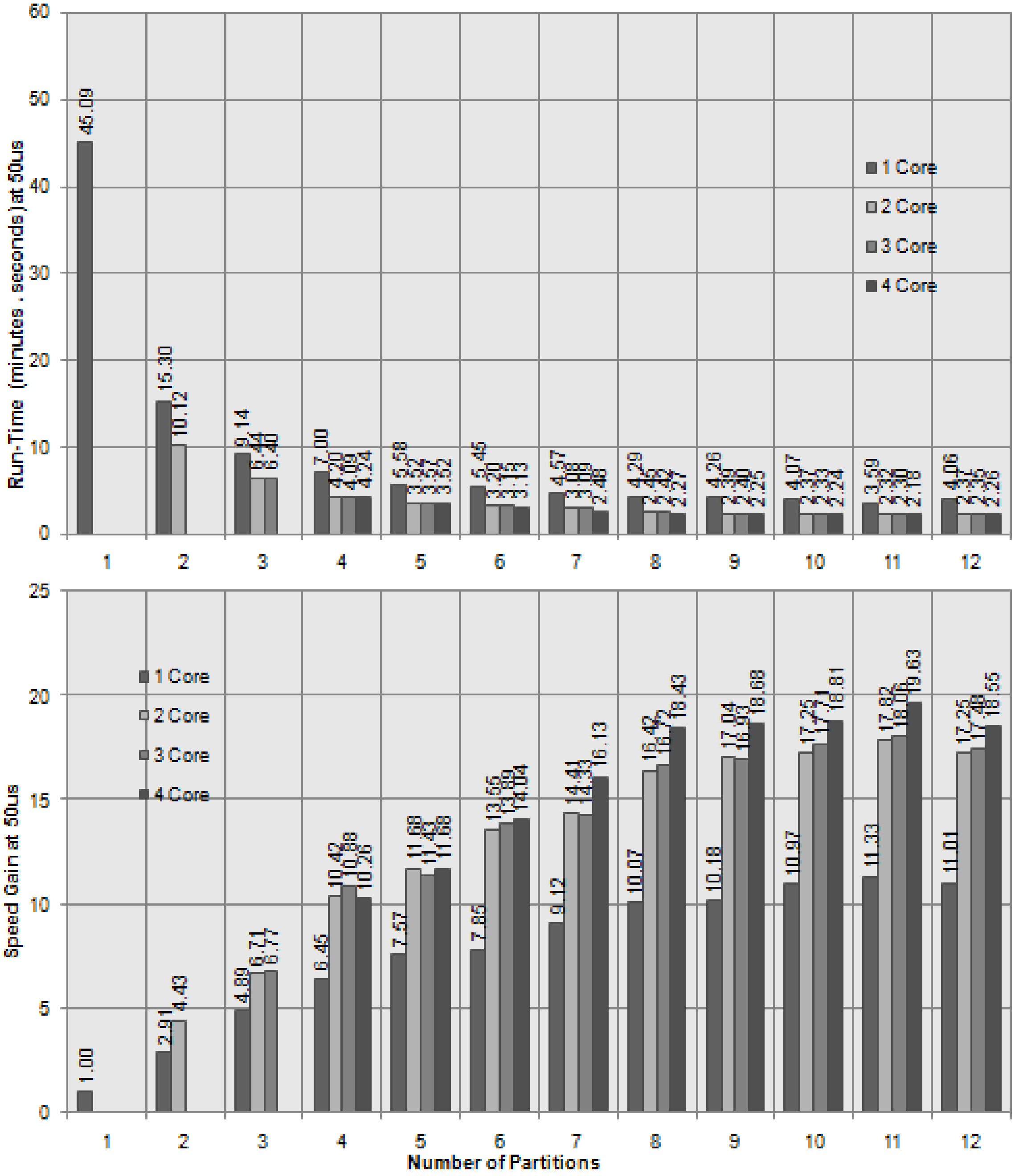
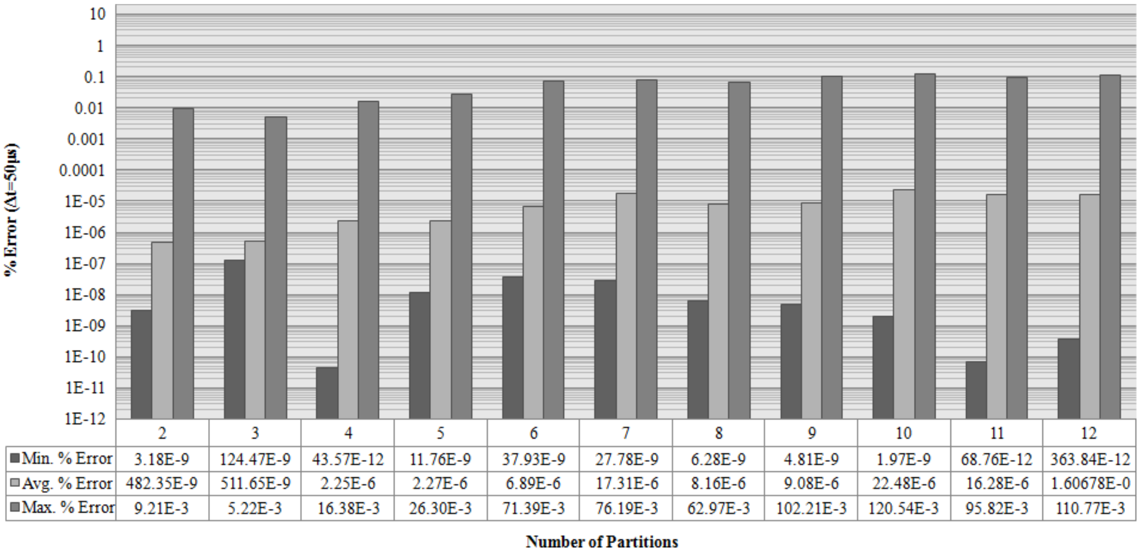


Fig. 4.3.20 . Simulation run-time (top) and speed gain (bottom) for Δ*t*=50μs



	2	3	4	5	6	7	8	9	10	11	12
■ Min. % Error	3.18E-9	124.47E-9	43.57E-12	11.76E-9	37.93E-9	27.78E-9	6.28E-9	4.81E-9	1.97E-9	68.76E-12	363.84E-12
□ Avg. % Error	482.35E-9	511.65E-9	2.25E-6	2.27E-6	6.89E-6	17.31E-6	8.16E-6	9.08E-6	22.48E-6	16.28E-6	1.60678E-0
■ Max. % Error	9.21E-3	5.22E-3	16.38E-3	26.30E-3	71.39E-3	76.19E-3	62.97E-3	102.21E-3	120.54E-3	95.82E-3	110.77E-3

Fig. 4.3.21 . Simulation errors for performance metric 1 (Δ*t*=50μs)

TABLE IV.5.SIMULATION ERRORS FOR PERFORMANCE METRIC 1 (Δ*T*=50 MICROSECONDS)

Minimum Error (Δt=50μs)								
No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	17.84E-9	17.84E-9	568.00E-21	3.18E-9	0.000050	BRK11_3r1 - Subsystem 1 of 2	Ia
3	7	-2.04E-9	-2.04E-9	2.53E-18	124.47E-9	0.000000	BRK12_4r1 - Subsystem 3 of 3	Ia
4	11	-65.64E-9	-65.64E-9	28.60E-21	43.57E-12	0.438200	BRK11_3r1 - Subsystem 1 of 4	Ia
5	10	6.49E-9	6.49E-9	762.42E-21	11.76E-9	0.000050	BRK21_5r1 - Subsystem 1 of 5	Ia
6	16	17.84E-9	17.84E-9	6.77E-18	37.93E-9	0.000050	ABT14r2 - Subsystem 6 of 6	Ia
7	24	-2.04E-9	-2.04E-9	565.53E-21	27.78E-9	0.000000	MBT11r2 - Subsystem 4 of 7	Ia
8	17	5.81E-12	5.81E-12	365.23E-24	6.28E-9	0.964500	MBT11r2 - Subsystem 7 of 8	Ia
9	18	10.02E-9	10.02E-9	481.70E-21	4.81E-9	0.000000	ABT14r2 - Subsystem 7 of 9	Ia
10	24	5.09E-12	5.09E-12	100.01E-24	1.97E-9	0.921000	BRK21_4r1 - Subsystem 10 of 10	Ib
11	22	-5.29E-6	-5.29E-6	3.64E-18	68.76E-12	0.479250	FLT2r1 - Subsystem 8 of 11	Vbc
12	22	-113.51E-9	-113.51E-9	413.01E-21	363.84E-12	0.597700	MBT11r2 - Subsystem 12 of 12	Ic

Average Error (Δt=50μs)		
No. Partitions	No. Boundaries	Avg. % Error
2	7	482.35E-9
3	7	511.65E-9
4	11	2.25E-6
5	10	2.27E-6
6	16	6.89E-6
7	24	17.31E-6
8	17	8.16E-6
9	18	9.08E-6
10	24	22.48E-6
11	22	16.28E-6
12	22	16.07E-6

Maximum Error (Δt=50μs)								
No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-196.83E+0	-196.81E+0	18.12E-3	9.21E-3	0.250350	BRK11_3r1 - Subsystem 1 of 2	Vca
3	7	341.61E+0	341.59E+0	17.82E-3	5.22E-3	0.400250	BRK12_4r1 - Subsystem 3 of 3	Vbc
4	11	-196.83E+0	-196.79E+0	32.23E-3	16.38E-3	0.250350	BRK11_3r1 - Subsystem 1 of 4	Vca
5	10	-159.46E+0	-159.42E+0	41.94E-3	26.30E-3	0.750350	BRK21_5r1 - Subsystem 1 of 5	Vca
6	16	-151.83E+0	-151.72E+0	108.39E-3	71.39E-3	0.750350	ABT14r2 - Subsystem 6 of 6	Vca
7	24	-189.86E+0	-189.71E+0	144.66E-3	76.19E-3	0.250350	MBT11r2 - Subsystem 4 of 7	Vca
8	17	-189.86E+0	-189.74E+0	119.55E-3	62.97E-3	0.250350	MBT11r2 - Subsystem 7 of 8	Vca
9	18	-151.83E+0	-151.68E+0	155.19E-3	102.21E-3	0.750350	ABT14r2 - Subsystem 7 of 9	Vca
10	24	-159.46E+0	-159.27E+0	192.21E-3	120.54E-3	0.750350	BRK21_4r1 - Subsystem 10 of 10	Vca
11	22	-171.41E+0	-171.24E+0	164.25E-3	95.82E-3	0.150350	FLT2r1 - Subsystem 8 of 11	Vca
12	22	-189.86E+0	-189.65E+0	210.31E-3	110.77E-3	0.250350	MBT11r2 - Subsystem 12 of 12	Vca

A plot of the maximum error against the number of partitions and boundaries is shown in Fig. 4.3.22. The exact relationship between the error, number of partitions, and number of boundaries was not investigated. From Fig. 4.3.23 and Table IV.5 the maximum error detected was when p=10 at relay 1 of BRK21_4 in subsystem 10 of 10. The maximum error occurred when the number of boundaries was maximum (24 boundaries), which suggests that the error has a relationship with the number of boundaries.

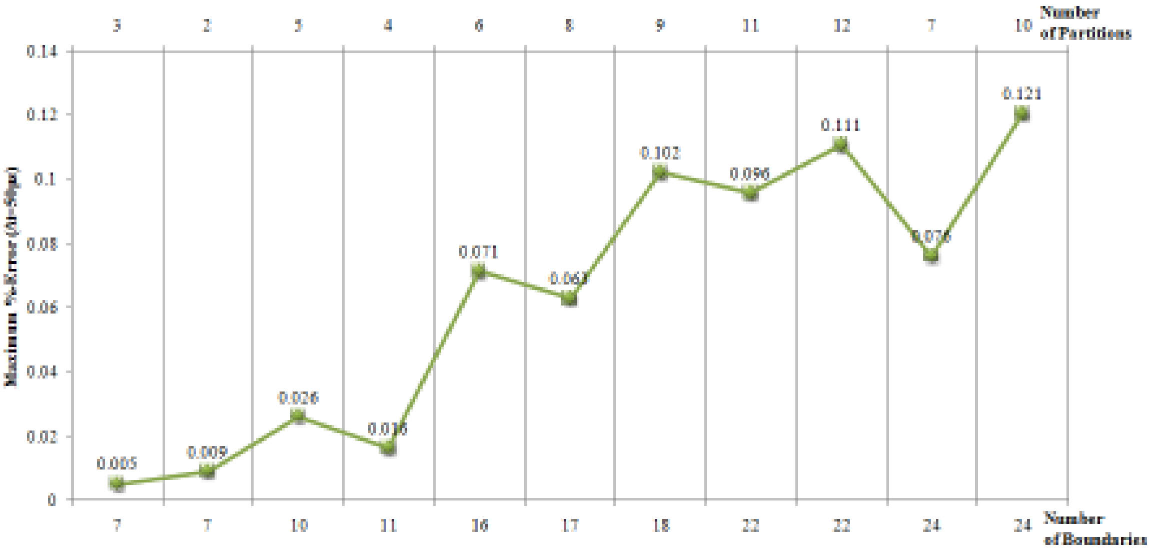


Fig. 4.3.22 . Maximum simulation error for Δ*t*=50μs

The time at which the maximum error occurred was $t = 0.750350\text{s}$, and occurred for variable v_{ca}^{k+1}. An overlay of the voltage waveform for BRK21_4 is shown in Fig. 4.3.23, where the maximum error is annotated. The abbreviation BRK21_4 stands for: switchboard 2, load center 1, circuit breaker 4, and can be located in the schematic shown in Fig. 4.3.1. A close-up of v_{ca}^{k+1} is shown on the lower part of Fig. 4.3.23 to show the maximum error value as indicated by Table IV.5. It is seen from the lower part of Fig. 4.3.23 that v_{ca}^{k+1} suffered from a magnitude deficiency when v_{ca}^{k+1}'s slope changed sign. The event that triggered the maximum error found in v_{ca}^{k+1} was event 61 as listed by Fig. 4.3.5, which corresponds to the tripping of BRK21_1.

The second largest error occurred at $t = 0.250350\text{s}$ when *p*=12, and also for v_{ca}^{k+1}. An overlay (*p*=1 and *p*=12) of the voltage waveforms for MBT11 are shown in Fig. 4.3.24, and annotated where the maximum error was reported. A close-up of v_{ca}^{k+1} is shown on the lower part of Fig. 4.3.24, which shows the maximum errors as indicated by Table IV.5. It can be seen again that the partitioned waveform also suffered at the peak where v_{ca}^{k+1}'s slope changed sign. The event that triggered this error is event 6 in Fig. 4.3.5, and occurred moments after BRK11_2 operated. There is no apparent difference between the unpartitioned and partitioned waveforms shown in Fig. 4.3.24 either, which indicates a good agreement of simulation results. As seen before the voltage transients occurred, the unpartitioned and partitioned waveforms appear to be exactly the same. To note the differences (if/when any), close-ups of the waveforms are necessary.

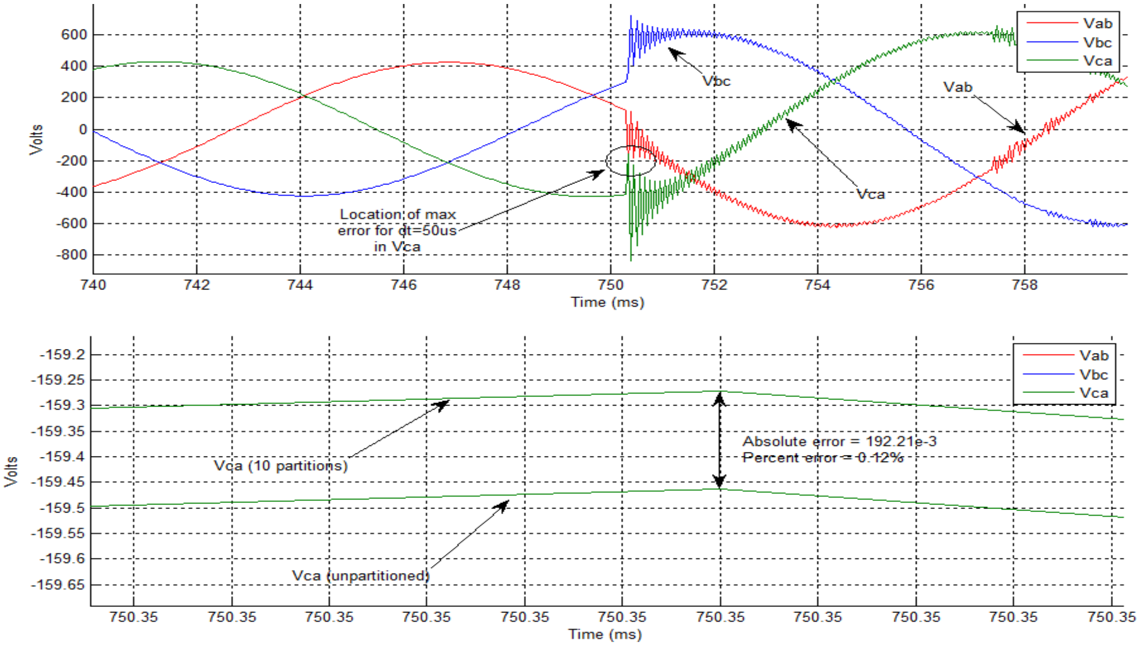


Fig. 4.3.23 . Maximum error: BRK21_4 for Δ*t*=50µs (bottom curve zooms top)

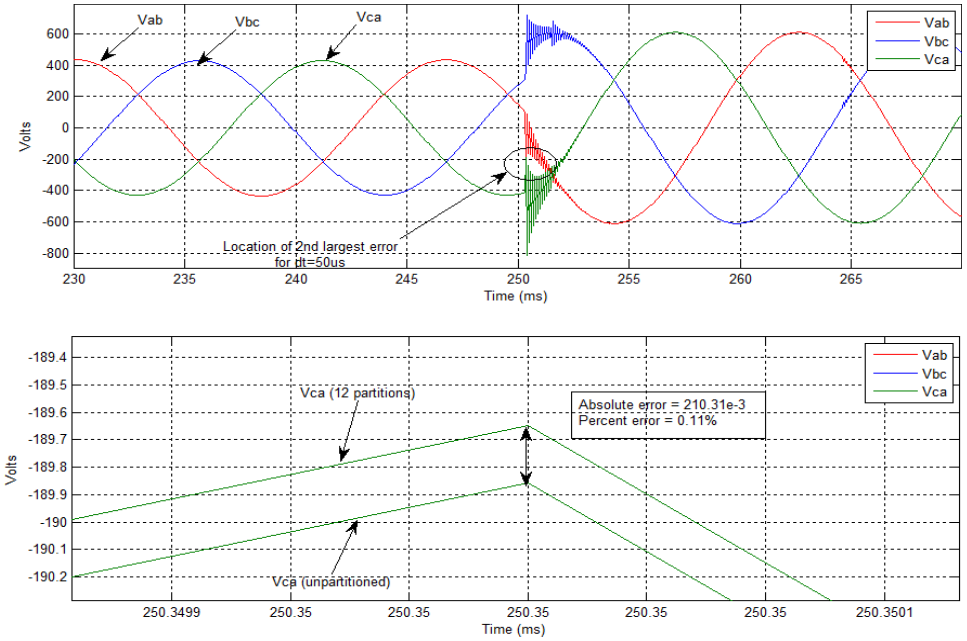


Fig. 4.3.24 . Second largest error: MBT11 for Δ*t*=50µs (bottom curve zooms top)

4.3.2.2 Summary of Results and Findings for PM1

Speed gains >11 were obtained when *c*=1. This result indicates that before going parallel, sequential simulations of partitioned SPSs should be optimized. The largest speed gain was $K_{speed} = 19.63$ corresponding to a run-time of 2 minutes 18 seconds. Comparing the slowest and fastest run-times, partitioning SPS simulations increments the number of simulations that can be ran per diem by a factor of ~20. These results can speed up the advancement of technology as *significantly more case studies* can be executed in the same amount of time.

The speed gains for $p = 12$, $c = \{2,3,4\}$ were almost the same. The reason for this unintuitive result is that when threads are manually assigned to the cores (i.e., unsafe programming) it leaves the operating system at an un-optimal operational state. If the operating system (Windows®) needs to give a time slice to the threads of another process, the threads of the SPS simulation are suspended until Windows lets them continue. This inherent thread suspension mitigates speed gain, causes undesirable dead-time, and a natural (uncontrollable) internal computational imbalance. In this regard, it is recommended that Windows handle the thread-to-core assignment (i.e., thread affinity) automatically based on computational resource information (not available to the user) [104].

The maximum error detected was 0.12%, when $p = 10$, for variable v_{ca}^{k+1}, and at over-current BRK21_4. The event that triggered the maximum error found in v_{ca}^{k+1} was event 61, which corresponds to the tripping of BRK21_1 as listed by Fig. 4.3.5. As seen from Fig. 4.3.1, both BRK21_1 (cause) and BRK21_4 (effect) are connected to the same load center. In this case, the tripping of BRK21_1 created a voltage transient local to BRK21_4. Both the cause and effect were in the same partition 10 of 10 as shown by the component distribution in Appendix C.

The second largest error also corresponded to v_{ca}^{k+1} but at MBT11, 0.5s earlier, and moments after BRK11_2r1 tripped. In this case, the transients from BRK11_2 tripping in partition 11 of 12 caused the second 2nd largest simulation error to occur at MBT11 in partition 12 of 12. The error locations may be produced and observed in the same partition as was noted for the largest error; however, this is not a necessary condition as was seen by the second largest error. All errors for Δt=50μs were fractional percentages and indicate general good agreement between unpartitioned and partitioned results. The switching of protective devices caused errors to be introduced during fast voltage transients.

A good way to show that the error incurred from partitioning SPS simulation is negligible is to compare the number of switching events (and their time instants) of unpartitioned (*p*=1) and partitioned simulations (*p*>1). If the simulation error would have been significant, the number of switching events (and RMS measurements) would have disagreed between *p*=1 and *p*>1. The consequences of wrong RMS measurements are a different number of protective device trippings, and switching events occurring at different time instants. Since the *number* and *times* of the protective devices for partitioned and unpartitioned simulations was the same, it is said that the error observed did not alter the simulation results.

Another way to assess the impact of the simulation error is by considering the average error in Table IV.5. The average error gives an idea of how close a partitioned value is to its true unpartitioned value. Since the average errors were in $O\left(10^{-6}\right)$, there is confidence in the partitioned simulation results.

4.3.3 Performance Metric 2 Results

The results descriptions of PM2 follows those of PM1. Since the graphics and tables of PM2 convey the same information as those of PM1, explanations for Fig. 4.3.25-Fig. 4.3.36 and Table IV.6-Table IV.9 are elided.

4.3.3.1 Case Study Results

4.3.3.1.1 Results for Performance Metric 2: Δt=75µs

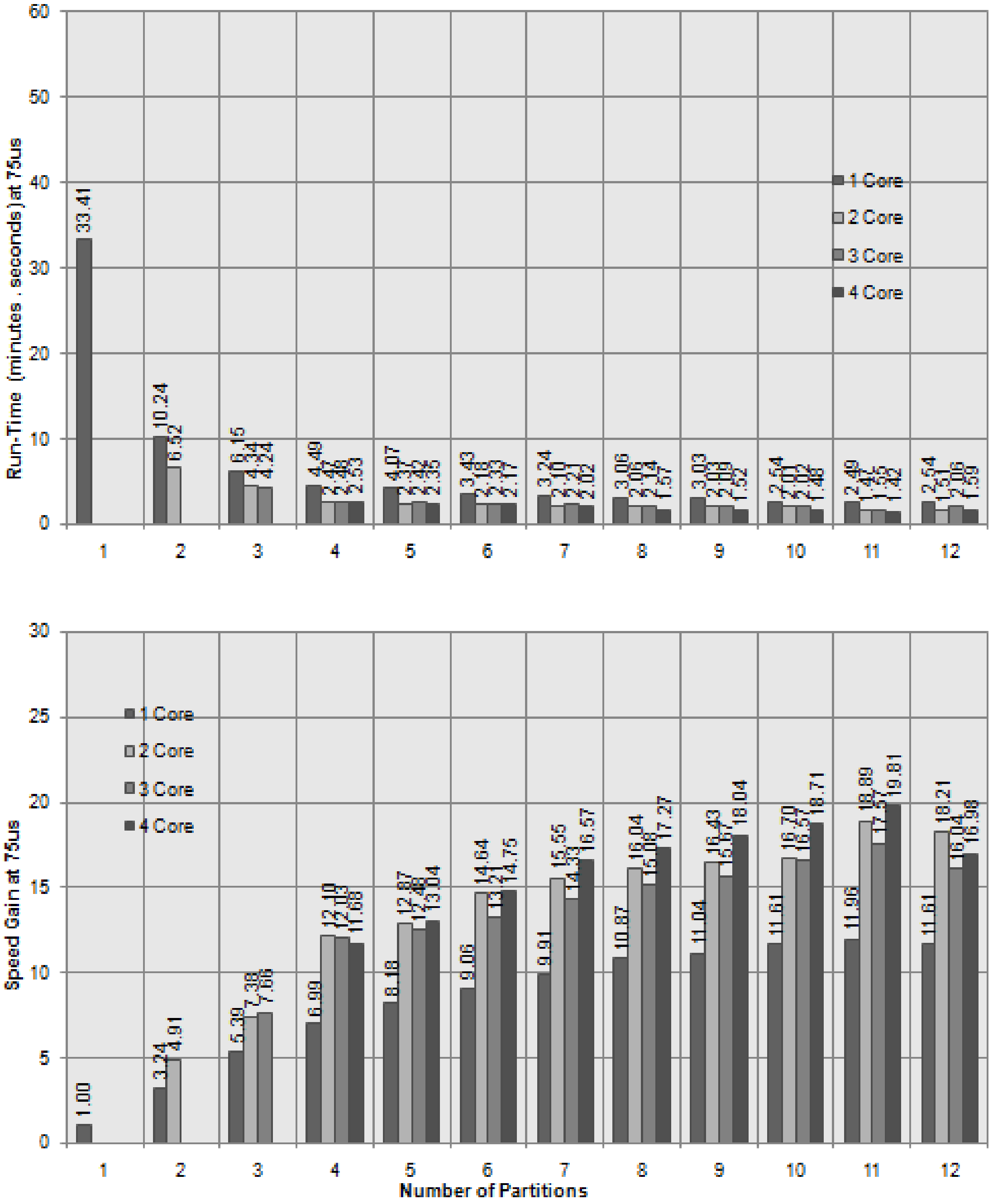
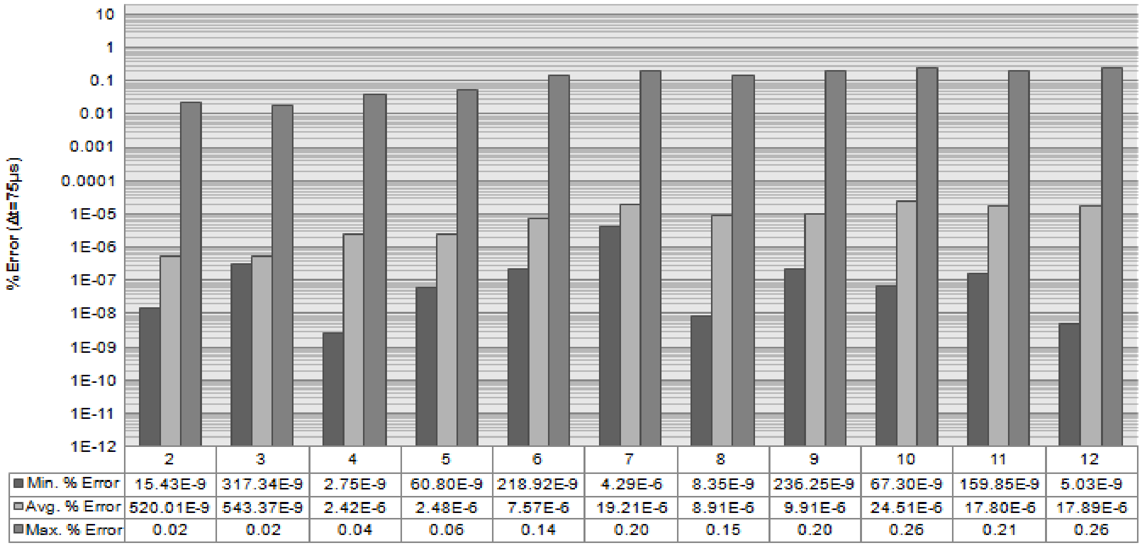


Fig. 4.3.25 . Simulation run-time (top) and speed gain (bottom) for Δ*t*=75µs



	2	3	4	5	6	7	8	9	10	11	12
■ Min. % Error	15.43E-9	317.34E-9	2.75E-9	60.80E-9	218.92E-9	4.29E-6	8.35E-9	236.25E-9	67.30E-9	159.85E-9	5.03E-9
□ Avg. % Error	520.01E-9	543.37E-9	2.42E-6	2.48E-6	7.57E-6	19.21E-6	8.91E-6	9.91E-6	24.51E-6	17.80E-6	17.89E-6
■ Max. % Error	0.02	0.02	0.04	0.06	0.14	0.20	0.15	0.20	0.26	0.21	0.26

Fig. 4.3.26 . Simulation errors for Δ*t*=75μs

TABLE IV.6.SIMULATION ERRORS FOR PERFORMANCE METRIC 2 (Δ*T*=75 MICROSECONDS)

Minimum Error (Δt=75µs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	26.49E-9	26.49E-9	4.09E-18	15.43E-9	0.000075	BRK11_3r1 - Subsystem 1 of 2	Ia
3	7	-2.24E-9	-2.24E-9	7.11E-18	317.34E-9	0.000000	BRK12_4r1 - Subsystem 3 of 3	Ia
4	11	-406.76E-9	-406.76E-9	11.19E-18	2.75E-9	0.498150	BRK11_3r1 - Subsystem 1 of 4	Ia
5	10	23.85E-9	23.85E-9	14.50E-18	60.80E-9	0.000075	BRK21_5r1 - Subsystem 1 of 5	Ia
6	16	8.76E-9	8.76E-9	19.19E-18	218.92E-9	0.000075	ABT14r2 - Subsystem 6 of 6	Ia
7	24	8.01E-9	8.01E-9	343.68E-18	4.29E-6	0.000000	ABT1r2 - Subsystem 6 of 7	Ia
8	17	-4.45E-12	-4.45E-12	371.96E-24	8.35E-9	0.929850	MBT11r2 - Subsystem 7 of 8	Ib
9	18	46.14E-9	46.14E-9	109.02E-18	236.25E-9	0.000075	ABT14r2 - Subsystem 7 of 9	Ia
10	24	5.90E-12	5.90E-12	3.97E-21	67.30E-9	0.930825	ABT15r2 - Subsystem 7 of 10	Ia
11	22	8.16E-9	8.16E-9	13.04E-18	159.85E-9	0.000000	FLT2r1 - Subsystem 8 of 11	Ia
12	22	-134.31E-9	-134.31E-9	6.75E-18	5.03E-9	0.620025	MBT11r2 - Subsystem 12 of 12	Ic

Average Error (Δt=75µs)

No. Partitions	No. Boundaries	Avg. % Error
2	7	520.01E-9
3	7	543.37E-9
4	11	2.42E-6
5	10	2.48E-6
6	16	7.57E-6
7	24	19.21E-6
8	17	8.91E-6
9	18	9.91E-6
10	24	24.51E-6
11	22	17.80E-6
12	22	17.89E-6

Maximum Error (Δt=75µs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-398.69E+0	-398.60E+0	89.11E-3	22.35E-3	0.250200	BRK11_3r1 - Subsystem 1 of 2	Vca
3	7	467.12E+0	467.04E+0	84.22E-3	18.03E-3	0.400200	BRK12_4r1 - Subsystem 3 of 3	Vbc
4	11	-398.69E+0	-398.53E+0	160.94E-3	40.37E-3	0.250200	BRK11_3r1 - Subsystem 1 of 4	Vca
5	10	-377.72E+0	-377.51E+0	209.89E-3	55.57E-3	0.750225	BRK21_5r1 - Subsystem 1 of 5	Vca
6	16	-375.33E+0	-374.79E+0	534.86E-3	142.50E-3	0.750225	ABT14r2 - Subsystem 6 of 6	Vca
7	24	-370.90E+0	-370.14E+0	756.32E-3	203.92E-3	0.750225	ABT1r2 - Subsystem 6 of 7	Vca
8	17	-396.49E+0	-395.91E+0	584.81E-3	147.50E-3	0.250200	MBT11r2 - Subsystem 7 of 8	Vca
9	18	-375.33E+0	-374.58E+0	752.05E-3	200.37E-3	0.750225	ABT14r2 - Subsystem 7 of 9	Vca
10	24	-370.90E+0	-369.94E+0	957.75E-3	258.22E-3	0.750225	ABT15r2 - Subsystem 7 of 10	Vca
11	22	-387.58E+0	-386.77E+0	810.74E-3	209.18E-3	0.150225	FLT2r1 - Subsystem 8 of 11	Vca
12	22	-396.49E+0	-395.47E+0	1.03E+0	259.03E-3	0.250200	MBT11r2 - Subsystem 12 of 12	Vca

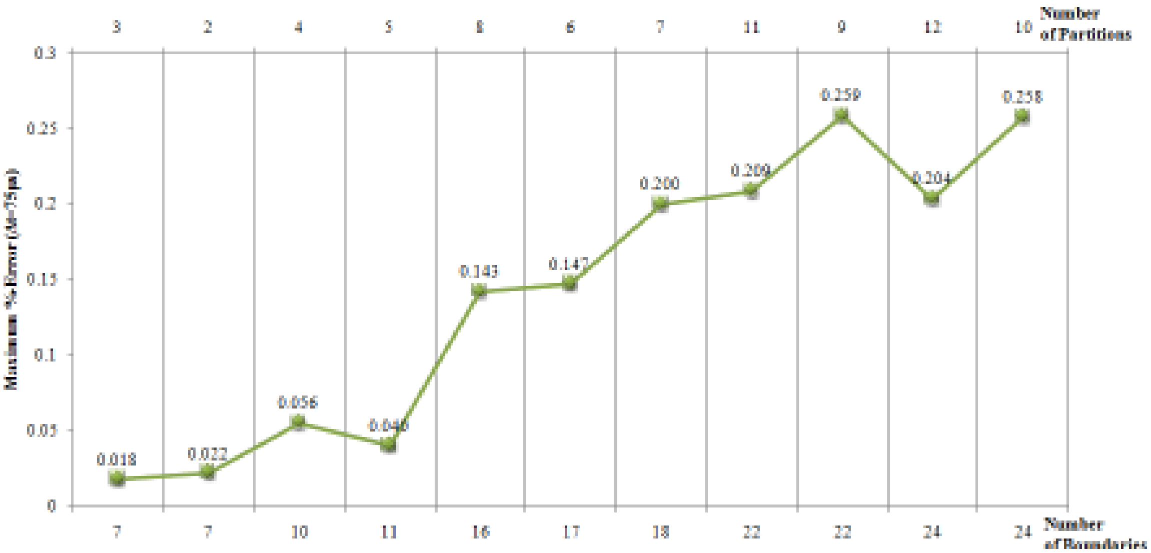


Fig. 4.3.27 . Maximum simulation error for Δ*t*=75μs

*4.3.3.1.2 Results for Performance Metric 2: Δt=100*μs

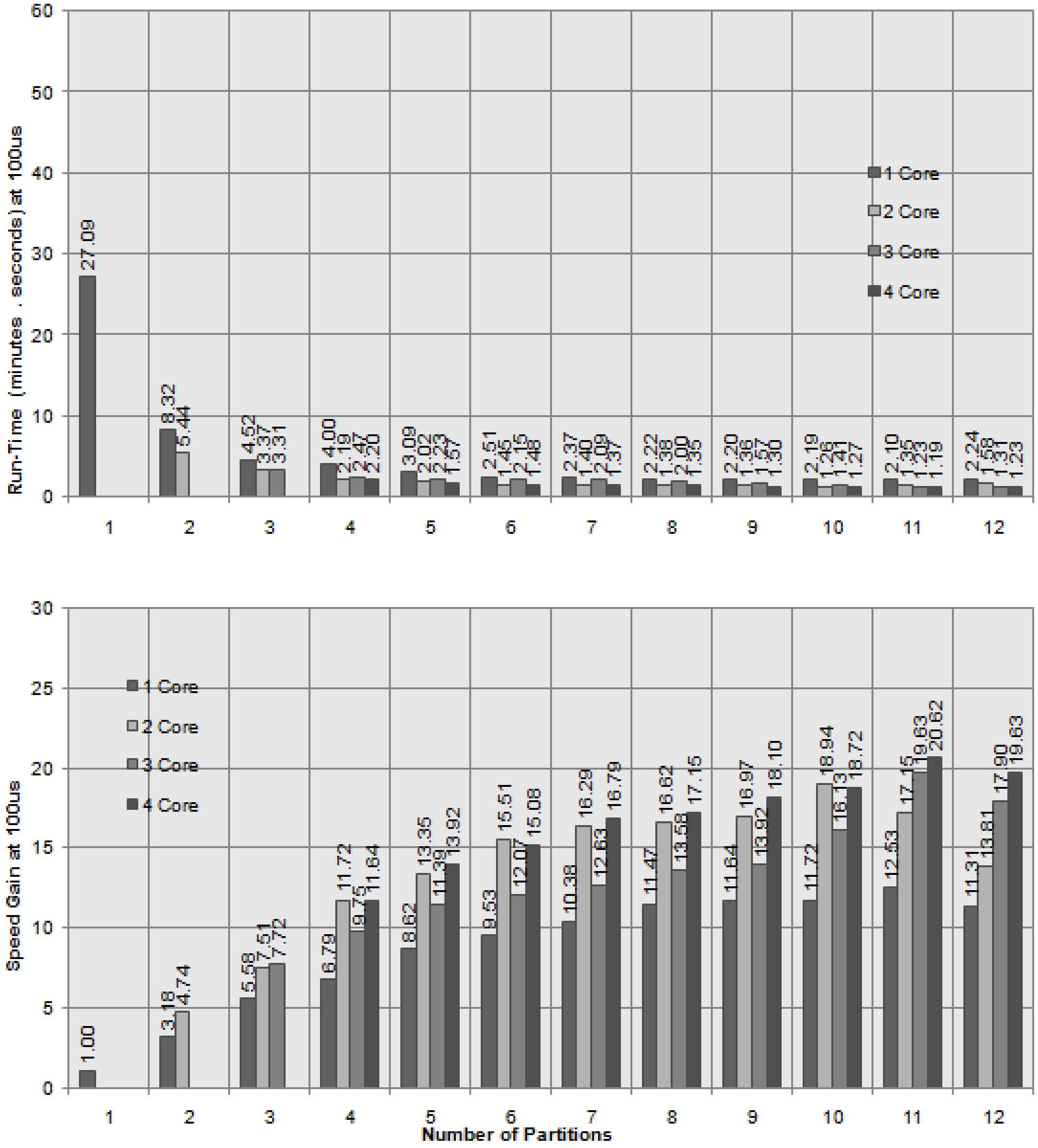
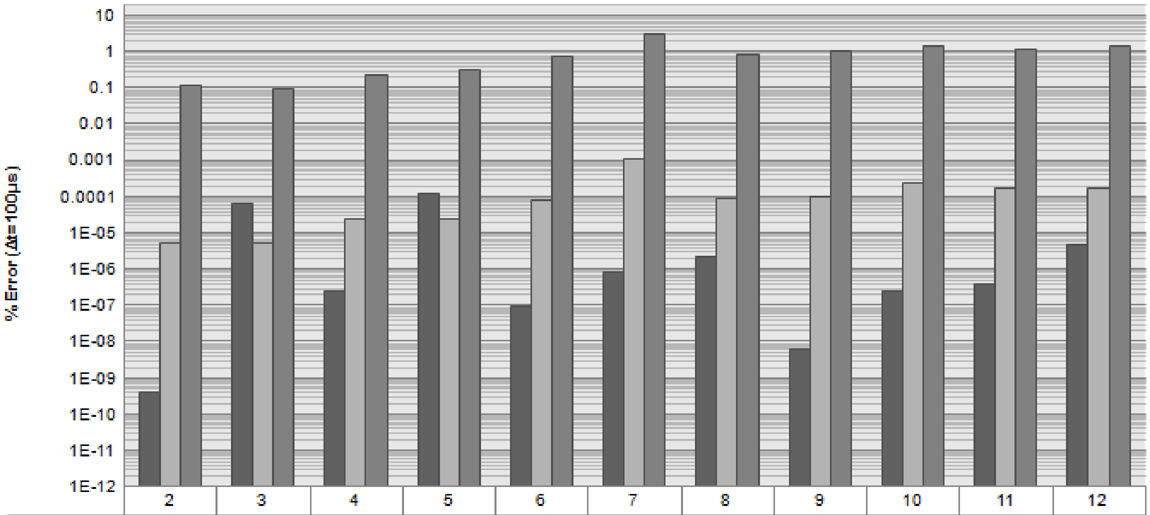


Fig. 4.3.28 . Simulation run-time (top) and speed gain for Δ*t*=100μs



	2	3	4	5	6	7	8	9	10	11	12
■ Min. % Error	398.17E-1	64.75E-6	264.70E-9	117.99E-6	99.43E-9	790.59E-9	2.26E-6	6.15E-9	244.56E-9	377.57E-9	4.68E-6
□ Avg. % Error	5.21E-6	5.40E-6	24.39E-6	25.08E-6	76.38E-6	1.10E-3	89.76E-6	99.01E-6	244.27E-6	178.22E-6	178.67E-6
■ Max. % Error	0.12	0.10	0.22	0.29	0.74	2.92	0.79	1.04	1.38	1.11	1.39

Fig. 4.3.29 . Simulation errors for Δ*t*=100μs

TABLE IV.7.SIMULATION ERRORS FOR PERFORMANCE METRIC 2 (ΔT=100 MICROSECONDS)

Minimum Error (Δt=100µs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	19.11E-6	19.11E-6	76.10E-18	398.17E-12	0.737400	BRK11_3r1 - Subsystem 1 of 2	Ib
3	7	-2.54E-9	-2.54E-9	1.65E-15	64.75E-6	0.000000	BRK12_4r1 - Subsystem 3 of 3	Ia
4	11	551.22E-9	551.22E-9	1.46E-15	264.70E-9	0.507600	BRK11_3r1 - Subsystem 1 of 4	Ib
5	10	3.40E-9	3.40E-9	4.01E-15	117.99E-6	0.000000	BRK21_5r1 - Subsystem 1 of 5	Ia
6	16	-2.86E-6	-2.86E-6	2.84E-15	99.43E-9	0.713400	ABT14r2 - Subsystem 6 of 6	Vbc
7	24	-264.56E-9	-264.56E-9	2.09E-15	790.59E-9	0.060500	FLT3r1 - Subsystem 1 of 7	Ic
8	17	1.75E-12	1.75E-12	39.58E-21	2.26E-6	0.911900	MBT11r2 - Subsystem 7 of 8	Ic
9	18	-1.99E-6	-1.99E-6	122.67E-18	6.15E-9	0.446900	ABT14r2 - Subsystem 7 of 9	Vbc
10	24	5.10E-12	5.10E-12	12.48E-21	244.56E-9	0.987700	ABT1r2 - Subsystem 7 of 10	Ib
11	22	-351.94E-9	-351.94E-9	1.33E-15	377.57E-9	0.623600	FLT2r1 - Subsystem 8 of 11	Ia
12	22	6.17E-9	6.17E-9	289.05E-18	4.68E-6	0.000000	MBT11r2 - Subsystem 12 of 12	Ia

Average Error (Δt=100µs)

No. Partitions	No. Boundaries	Avg. % Error
2	7	5.21E-6
3	7	5.40E-6
4	11	24.39E-6
5	10	25.08E-6
6	16	76.38E-6
7	24	1.10E-3
8	17	89.76E-6
9	18	99.01E-6
10	24	244.27E-6
11	22	178.22E-6
12	22	178.67E-6

Maximum Error (Δt=100µs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-440.74E+0	-440.20E+0	532.32E-3	120.78E-3	0.250300	BRK11_3r1 - Subsystem 1 of 2	Vca
3	7	508.15E+0	507.66E+0	490.19E-3	96.46E-3	0.400200	BRK12_4r1 - Subsystem 3 of 3	Vbc
4	11	-440.74E+0	-439.77E+0	969.79E-3	220.04E-3	0.250300	BRK11_3r1 - Subsystem 1 of 4	Vca
5	10	-431.24E+0	-429.98E+0	1.26E+0	293.27E-3	0.750300	BRK21_5r1 - Subsystem 1 of 5	Vca
6	16	-430.18E+0	-426.98E+0	3.20E+0	743.83E-3	0.750300	ABT14r2 - Subsystem 6 of 6	Vca
7	24	8.76E+3	8.50E+3	255.58E+0	2.92E+0	0.359000	FLT3r1 - Subsystem 1 of 7	Ic
8	17	-439.77E+0	-436.28E+0	3.48E+0	792.25E-3	0.250300	MBT11r2 - Subsystem 7 of 8	Vca
9	18	-430.18E+0	-425.73E+0	4.45E+0	1.04E+0	0.750300	ABT14r2 - Subsystem 7 of 9	Vca
10	24	-424.83E+0	-418.99E+0	5.84E+0	1.38E+0	0.750300	ABT1r2 - Subsystem 7 of 10	Vca
11	22	-437.08E+0	-432.24E+0	4.84E+0	1.11E+0	0.150300	FLT2r1 - Subsystem 8 of 11	Vca
12	22	-439.77E+0	-433.66E+0	6.11E+0	1.39E+0	0.250300	MBT11r2 - Subsystem 12 of 12	Vca

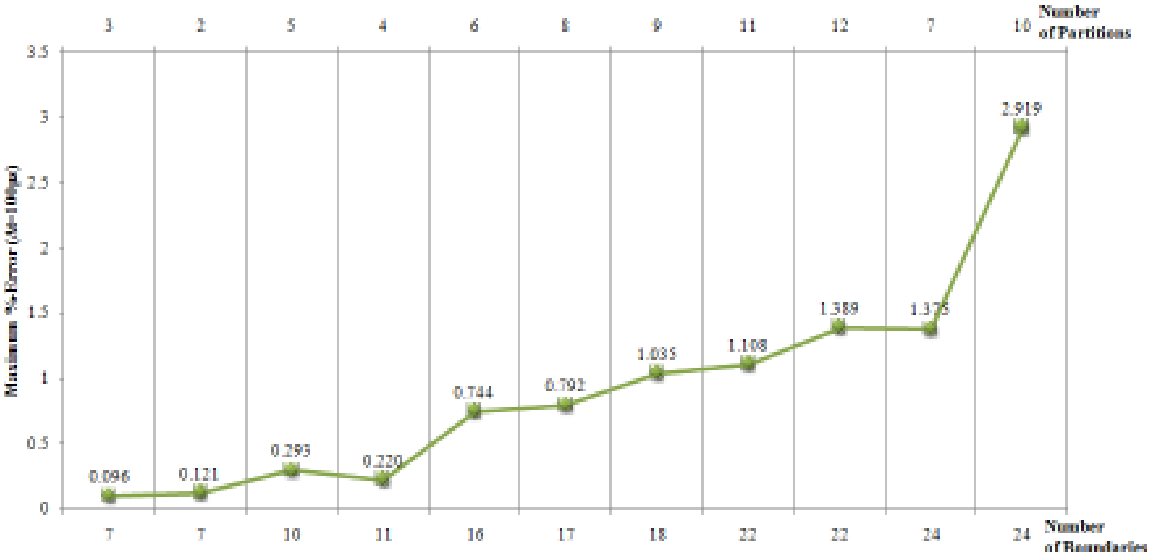


Fig. 4.3.30 . Maximum simulation for Δ*t*=100µs

4.3.3.1.3 Results for Performance Metric 2: Δt=250μs

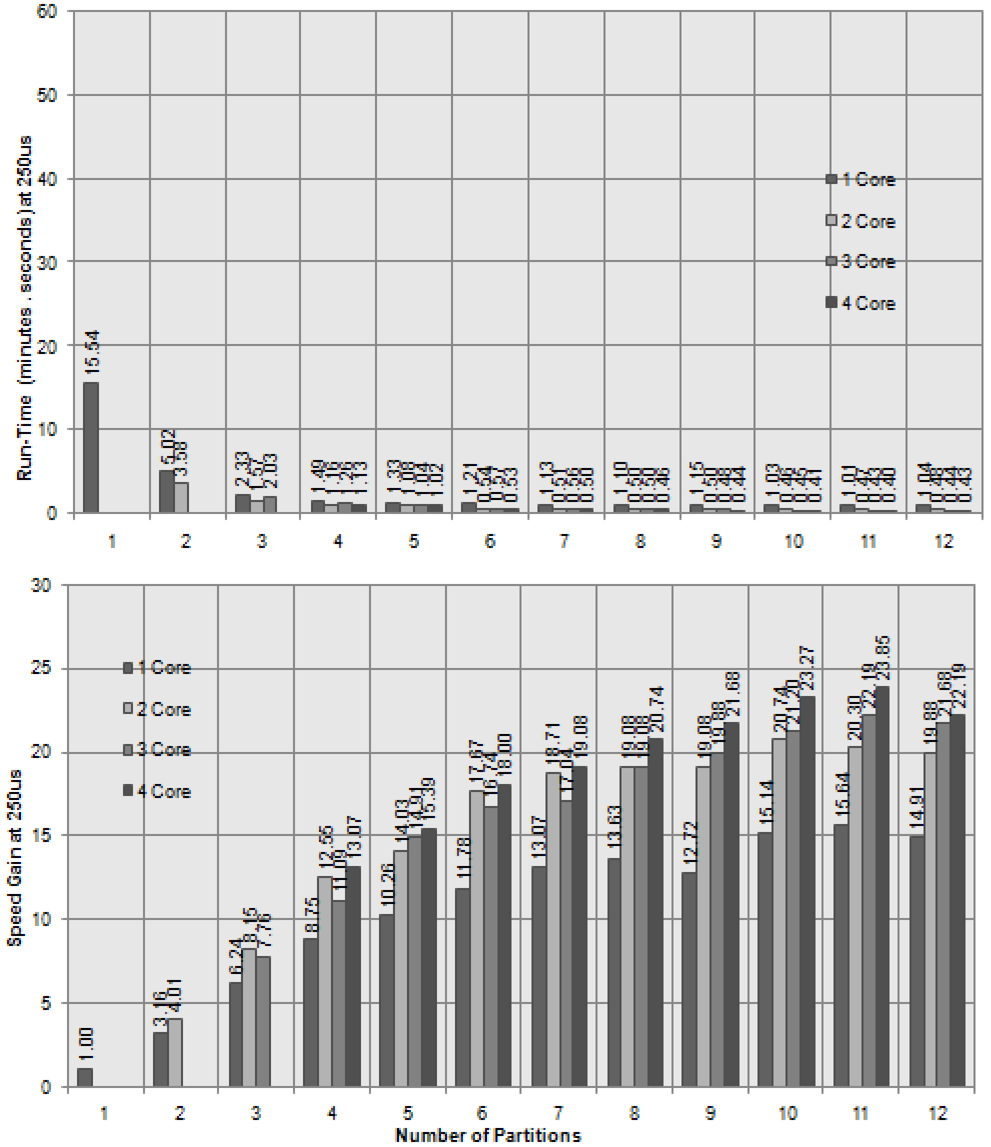
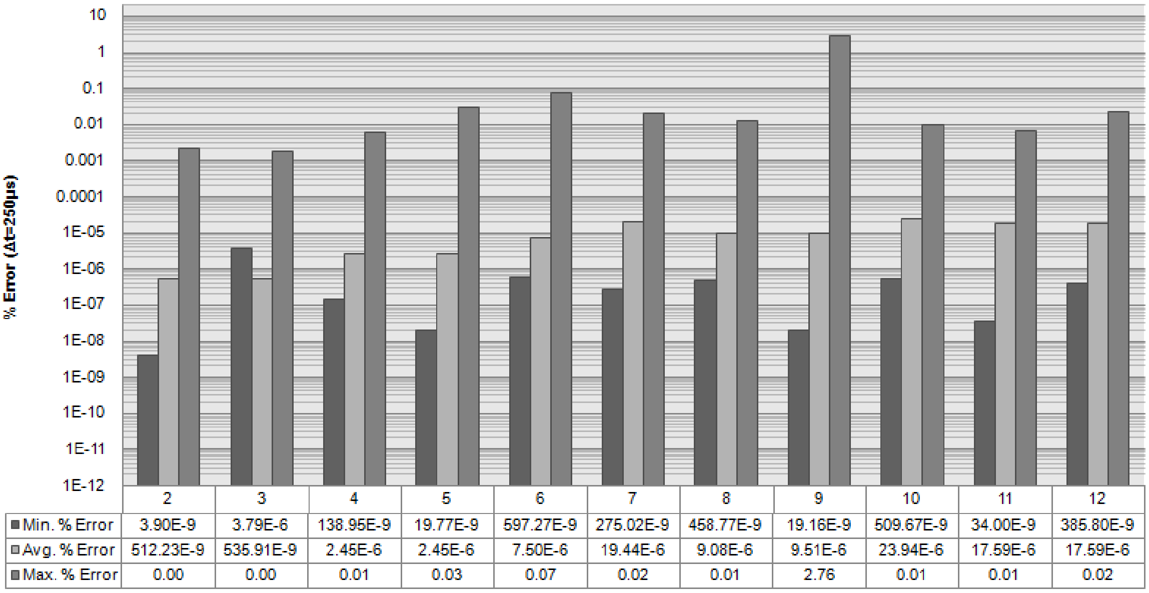


Fig. 4.3.31. Simulation run-time (top) and speed gain (bottom) Δ*t*=250μs



	2	3	4	5	6	7	8	9	10	11	12
■ Min. % Error	3.90E-9	3.79E-6	138.95E-9	19.77E-9	597.27E-9	275.02E-9	458.77E-9	19.16E-9	509.67E-9	34.00E-9	385.80E-9
□ Avg. % Error	512.23E-9	535.91E-9	2.45E-6	2.45E-6	7.50E-6	19.44E-6	9.08E-6	9.51E-6	23.94E-6	17.59E-6	17.59E-6
■ Max. % Error	0.00	0.00	0.01	0.03	0.07	0.02	0.01	2.76	0.01	0.01	0.02

Fig. 4.3.32 . Simulation errors for Δ*t*=250μs

Table IV.8.Simulation errors for performance metric 2 (Δ*T*=250 microseconds)

Minimum Error (Δt=250μs)								
No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-282.78E-9	-282.78E-9	11.04E-18	3.90E-9	0.450000	MBT5r1 - Subsystem 1 of 2	Ia
3	7	-4.16E-9	-4.16E-9	157.58E-18	3.79E-6	0.000000	BRK12_4r1 - Subsystem 3 of 3	Ia
4	11	-267.41E-9	-267.41E-9	371.57E-18	138.95E-9	0.805750	BRK3_12r1 - Subsystem 3 of 4	Ic
5	10	-322.02E-9	-322.02E-9	63.66E-18	19.77E-9	0.528750	BRK21_5r1 - Subsystem 1 of 5	Ic
6	16	16.56E-9	16.56E-9	98.93E-18	597.27E-9	0.000250	ABT14r2 - Subsystem 6 of 6	Ia
7	24	47.91E-9	47.91E-9	131.76E-18	275.02E-9	0.000000	ABT1r2 - Subsystem 6 of 7	Ia
8	17	-5.41E-12	-5.41E-12	24.82E-21	458.77E-9	0.957000	MBT11r2 - Subsystem 7 of 8	Ia
9	18	1.83E-6	1.83E-6	351.33E-18	19.16E-9	0.806500	ABT14r2 - Subsystem 7 of 9	Ic
10	24	-4.80E-12	-4.80E-12	24.47E-21	509.67E-9	0.904250	BRK1r1 - Subsystem 2 of 10	Ia
11	22	-302.80E-9	-302.80E-9	102.96E-18	34.00E-9	0.622750	BRK3r1 - Subsystem 11 of 11	Ic
12	22	73.74E-9	73.74E-9	284.50E-18	385.80E-9	0.000250	MBT11r2 - Subsystem 12 of 12	Ia

Average Error (Δt=250μs)		
No. Partitions	No. Boundaries	Avg. % Error
2	7	512.23E-9
3	7	535.91E-9
4	11	2.45E-6
5	10	2.45E-6
6	16	7.50E-6
7	24	19.44E-6
8	17	9.08E-6
9	18	9.51E-6
10	24	23.94E-6
11	22	17.59E-6
12	22	17.59E-6

Maximum Error (Δt=250μs)								
No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	558.03E+0	558.02E+0	11.57E-3	2.07E-3	0.251500	MBT5r1 - Subsystem 1 of 2	Vbc
3	7	567.61E+0	567.60E+0	9.83E-3	1.73E-3	0.251500	BRK12_4r1 - Subsystem 3 of 3	Vbc
4	11	-395.22E+0	-395.24E+0	24.52E-3	6.20E-3	0.028250	BRK3_12r1 - Subsystem 3 of 4	Ib
5	10	91.29E+0	91.32E+0	25.90E-3	28.37E-3	0.750000	BRK21_5r1 - Subsystem 1 of 5	Vab
6	16	91.35E+0	91.41E+0	66.11E-3	72.37E-3	0.750000	ABT14r2 - Subsystem 6 of 6	Vab
7	24	569.76E+0	569.65E+0	112.54E-3	19.75E-3	0.251500	ABT1r2 - Subsystem 6 of 7	Vbc
8	17	-506.88E+0	-506.81E+0	67.16E-3	13.25E-3	0.250000	MBT11r2 - Subsystem 7 of 8	Vca
9	18	91.35E+0	93.87E+0	2.52E+0	2.76E+0	0.750000	ABT14r2 - Subsystem 7 of 9	Vab
10	24	-2.33E+3	-2.33E+3	223.95E-3	9.61E-3	0.028250	BRK1r1 - Subsystem 2 of 10	Ib
11	22	-2.53E+3	-2.53E+3	167.49E-3	6.61E-3	0.028250	BRK3r1 - Subsystem 11 of 11	Ib
12	22	-506.88E+0	-506.76E+0	117.16E-3	23.11E-3	0.250000	MBT11r2 - Subsystem 12 of 12	Vca

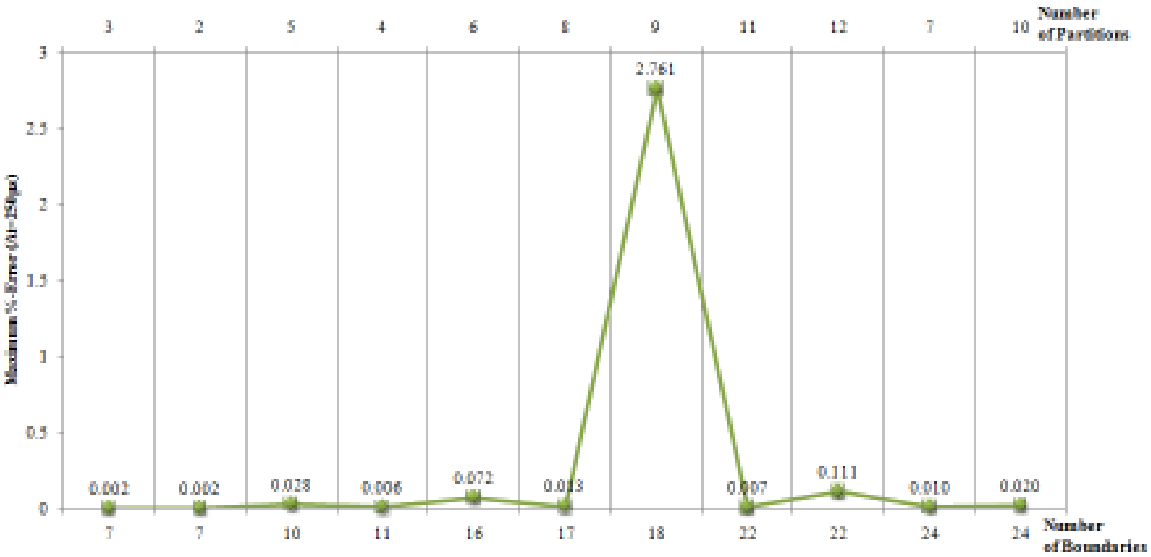


Fig. 4.3.33 . Maximum simulation error for Δ*t*=250μs

4.3.3.1.4 Results for Performance Metric 2: Δt=500μs

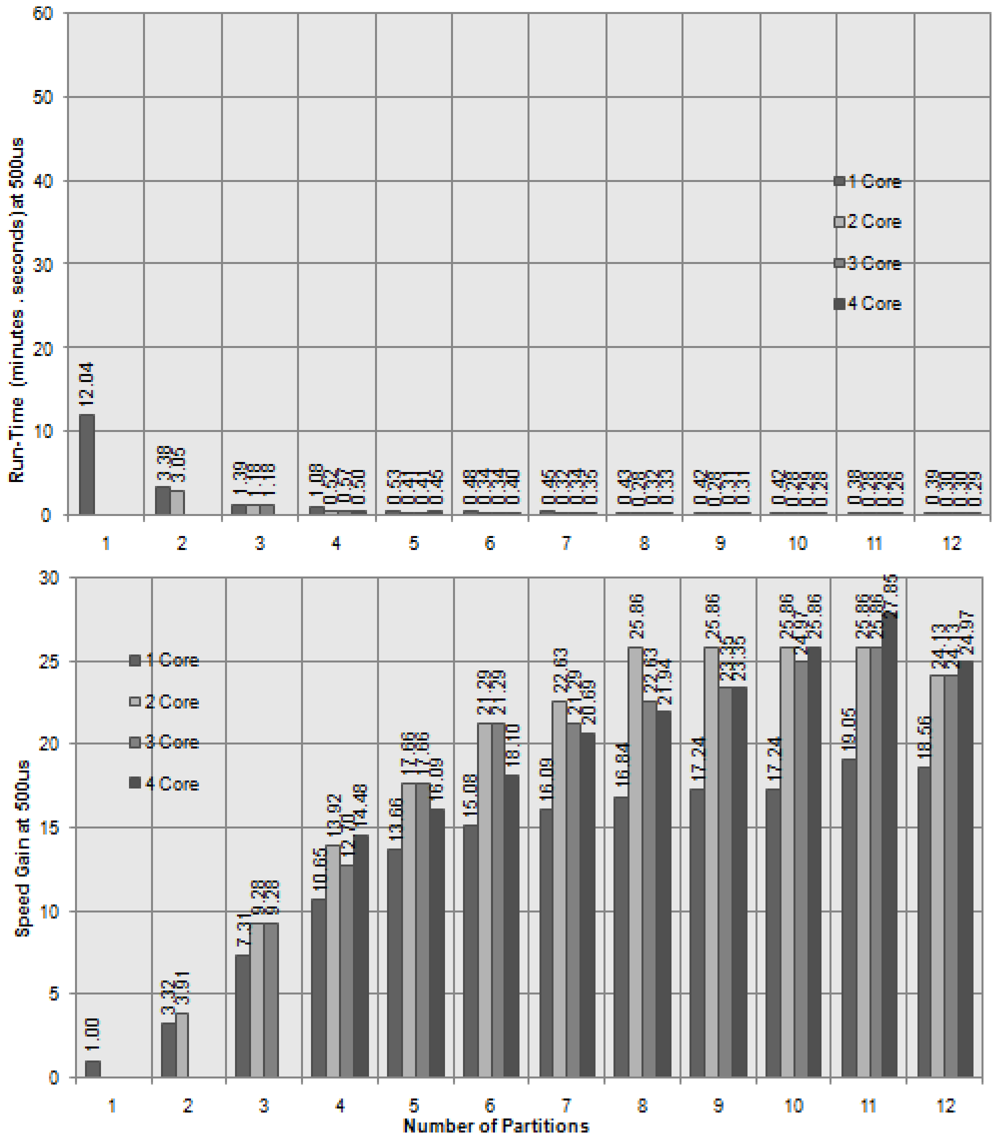
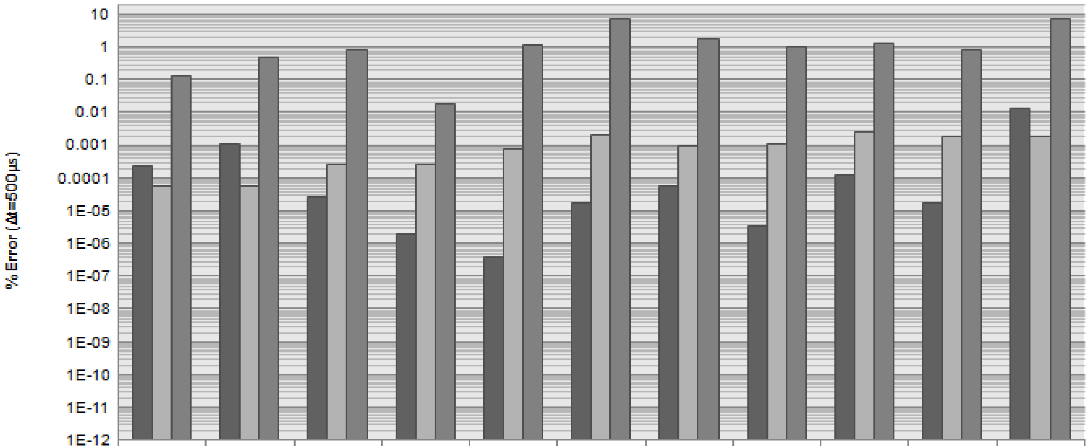


Fig. 4.3.34. Simulation run-time (top) and speed gain (bottom) for Δ*t*=500μs



	2	3	4	5	6	7	8	9	10	11	12
■ Min. % Error	245.76E-6	1.03E-3	26.58E-6	2.08E-6	370.25E-9	18.14E-6	56.29E-6	3.41E-6	126.71E-6	17.40E-6	12.60E-3
□ Avg. % Error	57.45E-6	60.70E-6	275.83E-6	274.50E-6	816.95E-6	2.01E-3	1.01E-3	1.03E-3	2.60E-3	1.90E-3	1.85E-3
■ Max. % Error	0.13	0.48	0.78	0.02	1.12	7.50	1.80	1.02	1.20	0.83	6.88

Fig. 4.3.35 . Simulation errors for Δ*t*=500µs

TABLE IV.9.SIMULATION ERRORS FOR PERFORMANCE METRIC 2 (Δ*T*=500 MICROSECONDS)

Minimum Error (Δt=500μs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-3.49E-9	-3.49E-9	8.58E-15	245.76E-6	0.000500	BRK2_7r1 - Subsystem 1 of 2	Ia
3	7	-4.87E-9	-4.87E-9	50.19E-15	1.03E-3	0.000000	BRK1_11r1 - Subsystem 1 of 3	Ia
4	11	-455.38E-9	-455.38E-9	121.05E-15	26.58E-6	0.584500	BRK3_12r1 - Subsystem 3 of 4	Ic
5	10	-379.21E-9	-379.21E-9	7.90E-15	2.08E-6	0.853500	BRK1_9r1 - Subsystem 2 of 5	Ic
6	16	-6.79E-6	-6.79E-6	25.13E-15	370.25E-9	0.457000	BRK3_12r1 - Subsystem 6 of 6	Vab
7	24	2.34E-6	2.34E-6	423.93E-15	18.14E-6	0.859500	BRK2_13r1 - Subsystem 7 of 7	Ic
8	17	2.38E-12	2.38E-12	1.34E-18	56.29E-6	0.962000	BRK3_12r1 - Subsystem 6 of 8	Ic
9	18	7.35E-6	7.35E-6	250.68E-15	3.41E-6	0.509500	BRK2_7r1 - Subsystem 3 of 9	Vca
10	24	5.38E-12	5.38E-12	6.81E-18	126.71E-6	0.954500	BRK1r1 - Subsystem 2 of 10	Ib
11	22	753.60E-9	753.61E-9	131.15E-15	17.40E-6	0.495500	BRK3r1 - Subsystem 11 of 11	Ib
12	22	2.92E-9	2.92E-9	368.36E-15	12.60E-3	0.000000	BRK2_13r1 - Subsystem 7 of 12	Ia

Average Error (Δt=500μs)

No. Partitions	No. Boundaries	Avg. % Error
2	7	57.45E-6
3	7	60.70E-6
4	11	275.83E-6
5	10	274.50E-6
6	16	816.95E-6
7	24	2.01E-3
8	17	1.01E-3
9	18	1.03E-3
10	24	2.60E-3
11	22	1.90E-3
12	22	1.85E-3

Maximum Error (Δt=500μs)

No. Partitions	No. Boundaries	Unpartitioned Value	Partitioned Value	Absolute Error	% Error	Time (secs)	Location of Error	Variable
2	7	-735.22E+0	-736.20E+0	976.38E-3	132.80E-3	0.028500	BRK2_7r1 - Subsystem 1 of 2	Ib
3	7	-207.87E+0	-208.86E+0	989.26E-3	475.90E-3	0.028500	BRK1_11r1 - Subsystem 1 of 3	Ib
4	11	-396.46E+0	-399.55E+0	3.08E+0	777.20E-3	0.028500	BRK3_12r1 - Subsystem 3 of 4	Ib
5	10	7.90E+3	7.90E+3	1.52E+0	19.20E-3	0.355500	BRK1_9r1 - Subsystem 2 of 5	Ib
6	16	-396.46E+0	-400.91E+0	4.45E+0	1.12E+0	0.028500	BRK3_12r1 - Subsystem 6 of 6	Ib
7	24	-136.07E+0	-146.27E+0	10.20E+0	7.50E+0	0.028500	BRK2_13r1 - Subsystem 7 of 7	Ib
8	17	-396.46E+0	-403.60E+0	7.13E+0	1.80E+0	0.028500	BRK3_12r1 - Subsystem 6 of 8	Ib
9	18	-735.22E+0	-742.68E+0	7.46E+0	1.02E+0	0.028500	BRK2_7r1 - Subsystem 3 of 9	Ib
10	24	-2.34E+3	-2.37E+3	28.14E+0	1.20E+0	0.028500	BRK1r1 - Subsystem 2 of 10	Ib
11	22	-2.54E+3	-2.56E+3	21.05E+0	827.83E-3	0.028500	BRK3r1 - Subsystem 11 of 11	Ib
12	22	-136.07E+0	-145.43E+0	9.36E+0	6.88E+0	0.028500	BRK2_13r1 - Subsystem 7 of 12	Ib

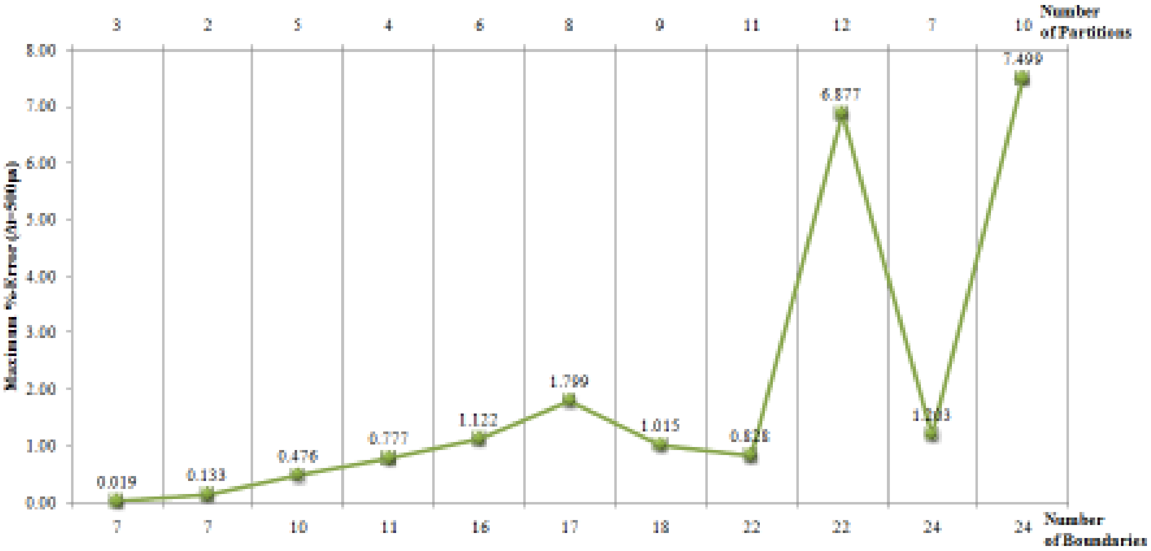


Fig. 4.3.36 . Maximum simulation error for Δ*t*=500µs

The maximum error for PM2 was found when Δ*t*=500µs, $p = 7$ at BRK2_13 as given by Table IV.9 as 7.50%. Waveform overlays of BRK2_13's current are shown in Fig. 4.3.37. From the upper overlay apparently there is good agreement between unpartitioned and partitioned (*p*=7) line currents. A close-up of i_b^{k+1} is shown on the lower part of Fig. 4.3.37, where a magnitude difference of 7.5% was detected at $t = 28.5\text{ms}$. The error shown occurred in the lower part of Fig. 4.3.37 is the largest error obtained for PM2, which also occurred when using the largest Δ*t*. Furthermore, no event triggered the error. This error was detected early during the simulation before any switching event took place. All switching events that occurred after $t = 28.5\text{ms}$ did not exceed this error.

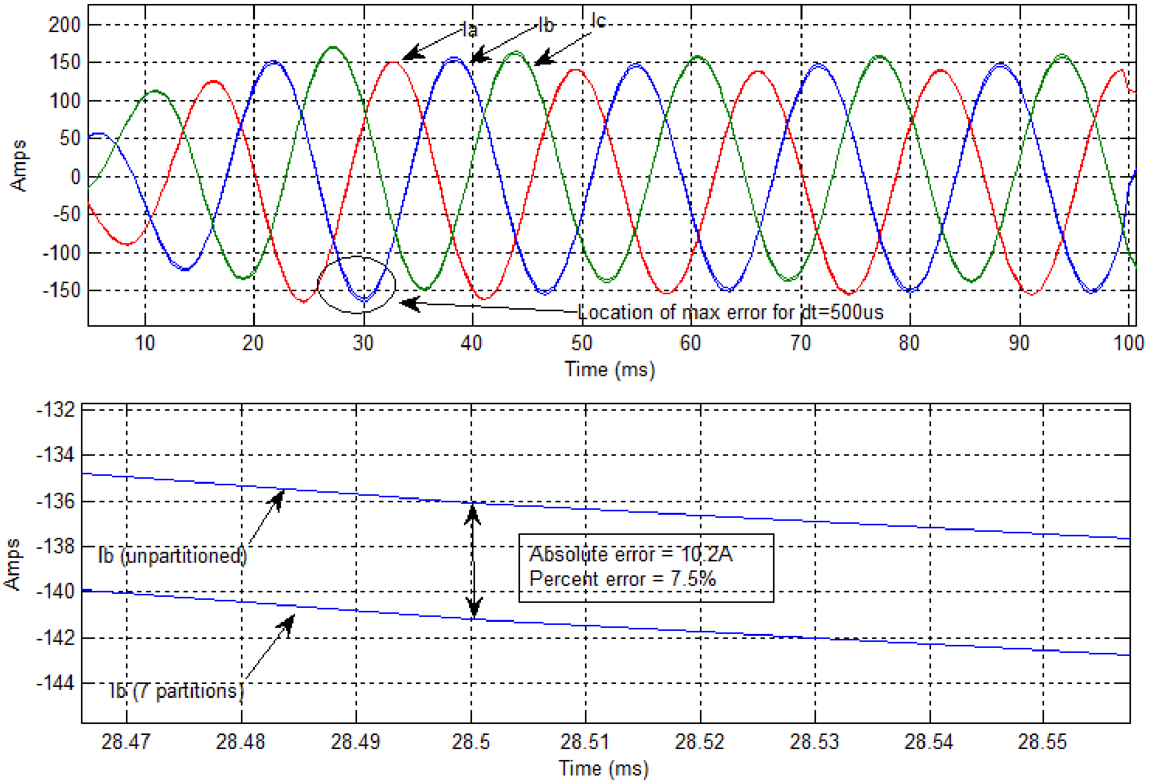


Fig. 4.3.37 . Current overlay of BRK2_13 showing largest error for PM2

4.3.3.2 Summary of Results and Findings for PM2

Over 200 simulations were conducted to obtain the results presented for PM2. The purpose of PM2 was to determine if variations in Δ*t* affected the speed gain and the accuracy and, if so, by how much. The largest error for PM2 occurred when Δ*t*=500μs, $p = 7$ at BRK2_13, was 7.50%. and occurred early during the simulation before any faults were applied. The maximum errors for all Δ*t* considered in PM2 increased similarly to the ratios in Fig. 4.2.2, which suggests that a correspondence between Δ*t* and error exists (i.e., the error from partitioning may accrue more significantly with a larger Δ*t*).

The largest error of 7.5% is considered acceptable because it neither changed the *values* of the RMS measurements nor the *number* of switching events. For example, when comparing p=1 and p=9 (both at Δt=500us), the number of switching events was in both cases as listed in the Appendix C. Henceforth, a user comparing the switching event log of unpartitioned and partitioned simulation results could not tell the difference between results.

The combined run-time, speed gain, and error per Δt for PM1 and PM2 are summarized in Fig. 4.3.38. Referring to the first set of columns in Fig. 4.3.38, the most accurate simulation was when Δt=50µs. Using the same Δt, the least run-time was 2 minutes and 18 seconds when partitioned as $p = 11$. The maximum error found with Δt=50µs was 0.12%. The peak error only occurred for the duration of one time step, which indicates that all subsequent errors (if any) are smaller than this peak.

Referring to the right-most set of columns in Fig. 4.3.38, the least run-time of 25 seconds (shown as 0.25), the largest speed gain of $K_{speed} = 27.85$, and largest error of 7.5% all occurred during PM2 with $\Delta t = 500\mu\text{s}$. The results for Δ$t$=75µs through Δ$t$=250µs are also shown in Fig. 4.3.38.

The run-time decreased as Δt increased because there were less number of time steps to execute. The maximum error increased with Δt, but not at a linear rate. The maximum errors shown in Fig. 4.3.38 are peak values, which mean that these errors occurred only once during the simulation and lasted for exactly one time step. More important than the maximum error is the *average* error, which is a good representation of the veracity of each partitioned simulation data point.

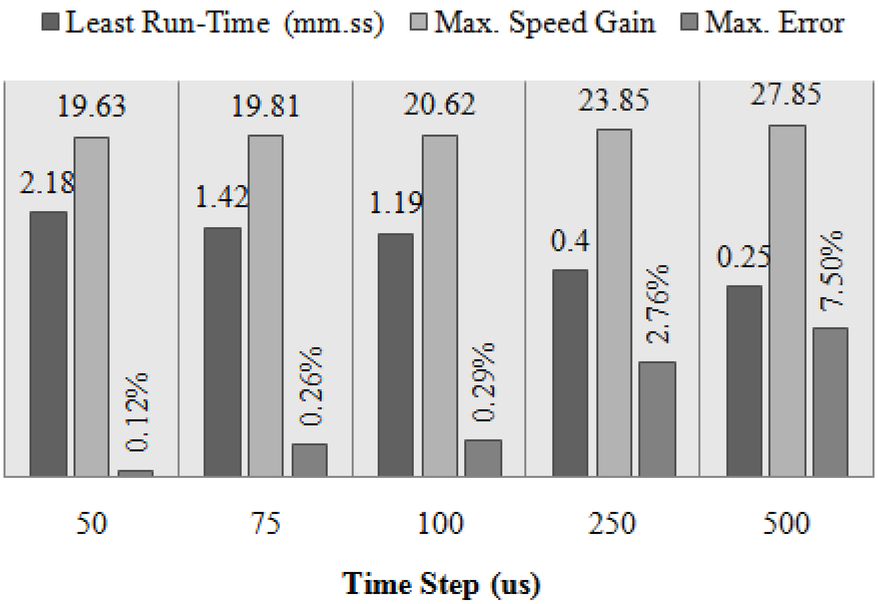


Fig. 4.3.38 . Run-time, speed gain, and maximum error per time step

The most important result is that the error from partitioning AC-Radial SPS simulations does not cause additional protective devices to operate. The reason the number of protective device operations was different for Δ*t*=50μs vs. Δ*t*=500μs (77 vs. 79 events, respectively) was the Δ*t* size, not the partitioning approach. The partitioning approach is validated by noticing that for the *same* Δ*t* the number of protective device operations does not change as exemplified for the Δ*t*=500μs case in the Appendix C.

The maximum speed gain obtained per each core is summarized with Fig. 4.3.39. The first column group represents the speed gains obtained when *c*=1 at different Δ*t*. For example, the maximum speed gain with *c*=1 occurred when Δ*t*=500μs and was $K_{speed} = 19.05$. Referring to the second column group, when $c = 2$ the maximum speed gain also occurd when Δ*t*=500μs and was $K_{speed} = 25.86$. Generally K_{speed} increases with both *c* and *p*, but not always. For example when *c*=3 at Δ*t*=75μs gave $K_{speed} = 17.57$ which is less gain than for Δ*t*=50μs of . In other words, larger Δ*t*'s tend to return higher gains than smaller Δ*t*'s but it is not guaranteed.

Another interesting result is observed from Fig. 4.3.39. When Δ*t*=50μs, the gain does not increase proportionally to *c*. For example, when using *c*=1 at Δ*t*=50μs the gain when using *c*=2 incrased by only $17.82/11.33 = 1.57$, and not =2 as may have been expected from using twice as many processors. Similary, when using *c*=4 the gain increase with respect to *c*=1 was $19.63/11.33 = 1.73$. More suprisingly is that the speed gain ratio between *c*=4 and *c*=2 was only $1.73/1.57 = 1.1$. This result implies that the gain of using 4 cores vs. 2 cores (on the quad-core machine used) is only 10%; an empiral, counter-intutive, and non-deterministic result at the same time.

Referring to the swim-lane diagram in Fig. 3.4.3, the dominant computation times at each time step (as *p* increases) are steps 2 and 7, which are the *serial* steps of the simulation approach. To estimate the influence of the serial steps on the *fastest* run-time of PM1 (depicted with Fig. 4.3.40), the *average* times to compute the serial steps were measured and tabulated in Table IV.10. For the simulation indicated in Fig. 4.3.40 the average time to compute the serial steps was ~2.2ms (per time step). The total time used to compute the serial steps (for the entire simulation) was ~45 seconds, and constitutes ~32% of the total run-time of 138 seconds. This result indicates that ~32% is likely to be the maximal affordable time that can be spent doing serial work over parallel-sequential work before diminishing returns are experienced. The serial-work computation time for other combinations or *p*, *c*, and Δ*t* was not investigated.

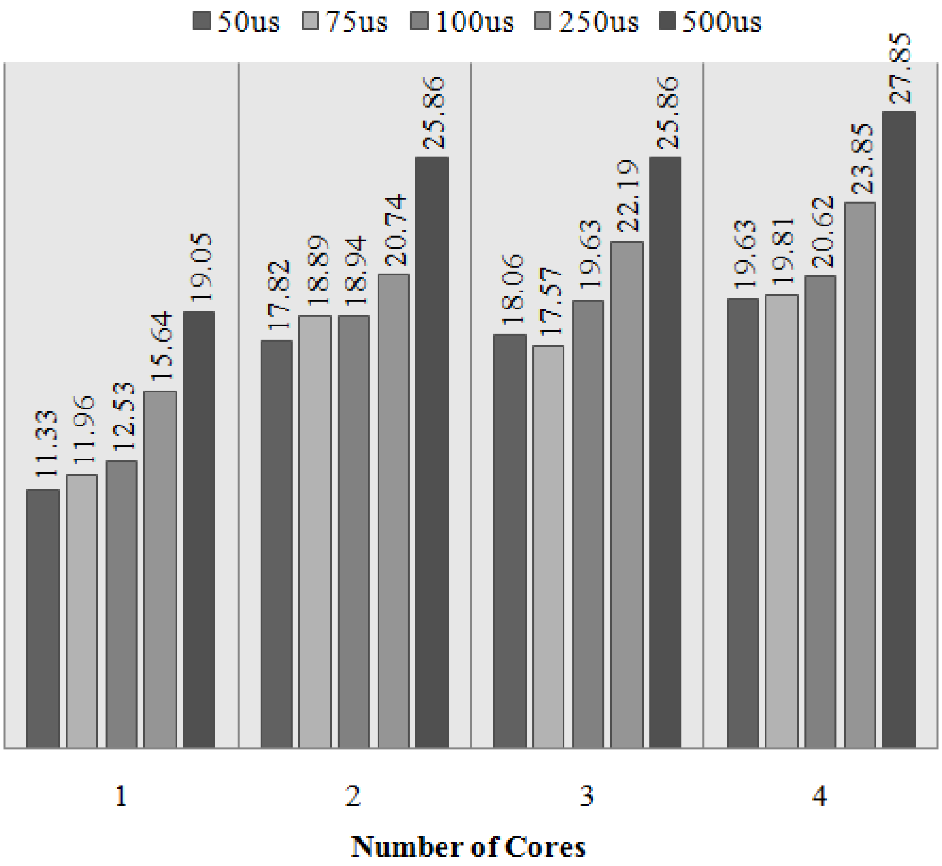


Fig. 4.3.39 . Summary of speed gain for each Δ*t* and *c*

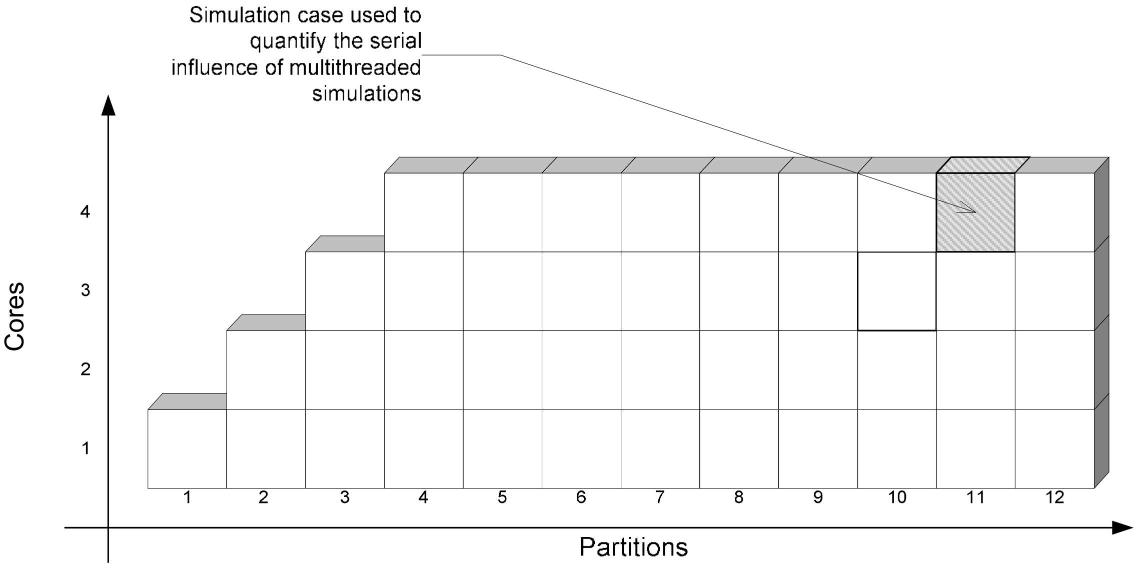

Simulation case used to quantify the serial influence of multithreaded simulations
Cores
1
2
3
4
1
2
3
4
5
6
7
8
9
10
11
12
Partitions

Fig. 4.3.40 . Simulation case to determine computation time of serial steps

TABLE IV.10.INFLUENCE OF SERIAL STEPS ON RUN-TIME

Average Time Spent on the Serial Steps		Totals	
Per Time Step (μs)	Whole Simulation (secs)	Simulation Run-Time (secs)	Influence of Serial Steps on Simulation Run-Time
2253.6	45.072	138	32.66%

4.4 CHAPTER SUMMARY

This chapter introduced, described, and discussed the performance metric results used to evaluate the solution methodology. To obtain the results of PM1 and PM2, ~250 simulations of the same SPS battle damage scenario were conducted.

The are several factors that limit the observed speed gain; some are: Windows background processes, computational imbalances, computation of the patch term or boundary conditions, the non-zero count and structure of the subsystem matrices, programming efficiency, processing power, memory cache, thread affinity, sequential simulation techniques, efficient switching models, interpolation techniques, etc.

The computation of the patch term is the major bottle neck of diakoptics-based approaches and becomes dominant as the simulations become finer-grained. Computational imbalance was present for two reasons: because the graph partitioning and balancing heuristics require that capacitors be present to form partitions and when $p>c$ the thread-to-core distribution is not even.

Errors in the partitioned simulation results were detected. Referring to the discretized capacitor circuit in Fig. 3.2.1, discretized capacitors have a series resistance and a series historical source. The partitioning approach in this work tore *active* branches (i.e., branches with sources), and further tore branches with rapidly-changing voltages (i.e., capacitor state-variables). The shorted capacitors at each boundary include the historical sources as part of the torn capacitors which influences the computations of the boundary conditions. The current through the capacitors is very small due to the high impedance of the capacitors. However, the capacitors' state-variable (their voltage) is oscillatory due to cable resonance. This high frequency (fast time constant) phenomenon caused fast voltage transients at load centers which is where the largest errors occurred.

The simulation speed gain increased as the number of partitions increased, but only through 11 partitions. Beyond 11 partitions, the computational burden of calculating the boundary conditions dominated the solution at each time step and produced diminishing speed gains. When using all four cores, the simulation speed gain does not increase linearly from its two- and three-core counterparts. This result occurs due to processor overwhelming. When Windows is left without resources for graphical rendering or other background process, the thread scheduler must suspend the simulation's threads and respond to other requests.

The observed errors were within acceptable reason because they did not change the RMS measurements, or the *number* of switching events in the partitioned simulations. The errors observed increased with Δt, occurred at difference time instances, and at different locations throughout the SPS. The errors reported were peak values, which mean that these errors only lasted for one time step. What is important to consider than the maximum error is the average the average error, which gives an idea of how accurate each partitioned simulation data point is with respect to its unpartitioned counterpart.

The amount of serial work was measured in terms of computational time for p=11, c=4, and Δt=50μs. It was found that, for this particular combination of p, c, and Δt the serial work amounts to ~32% of the total run-time. Other combinations of p, c, and Δt to measure the serial work were not investigated.

CHAPTER V

CONCLUSIONS AND FUTURE WORK

5.1 CONCLUSIONS

The work in this dissertation presented a formulation-partitioning approach to parallelize the simulation of AC-Radial SPSs using multicore computers. The solution methodology was validated with performance metrics, which assessed speed gain and accuracy. This chapter presents concluding remarks organized in two subsections: advantages and limitations of the solution methodology. The chapter ends focusing on central research topics to explain what seem likely to become useful future specific research work aimed at reducing simulation run-times while preserving accuracy in the process and outcomes.

5.1.1 Advantages of the Solution Methodology

The run-time of AC-Radial SPS simulation was reduced by ~30 times. This result indicated that significantly more case studies could be run in one day, which was the main purpose of this work. An example of said improvement was the run-time comparison of the unpartitioned run-time (Δt=50μs) of ~45mins vesus the partitioned run-time of ~2 minutes.

The hardware cost of using multicore computers is very low when compared to other existing hardware solutions (e.g., PC-clusters or dedicated real-time simulators). Further, since multicore computers are already ubiquitous, it is likely that hardware need not be bought to implement the simulation approach presented in this work. The simulation approach presented in this work does not demand additional hardware cost to implement it, which makes simulation an attractive option for investigators in need of conducting repeated parallel simulations of AC-Radial SPSs.

On the other hand, the accuracy of unpartitioned simulations was preserved when compared to partitioned simulations results. It was shown in Fig. 4.3.38 that the peak simulation error, when Δt=500μs, was barely 7.5%. This error was a peak one and only lasted for one time step. The error observed in the partitioned simulations nonetheless *did not* alter the number of switching events; that is, for a given combination $\{\Delta t, p, c\}$ the number of switching events was the same whether the simulation was unpartitioned or unpartitioned. Had the error impacted the results, protective device RMS measurements would have been erroneous, which was not the case in this work, according to the findings of the performance metrics explained earlier. Erroneous RMS measurements, however, may lead to a loss in protective device security [109] and did not occur here.

More important than the peak simulation errors observed in the partitioned simulations were the average errors listed in Table IV.5-Table IV.9. The average error shows the level of uncertainty that each partitioned simulation data point is incorrect. For instance, for a given random sample point an average error of $O\left(10^{6}\right)$ indicates that for a random sample point, the %-error between unpartitioned and partitioned simulation results is of this order. Chapter IV established that the average errors were of negligible concern.

Formulation of an AC-Radial SPS using loop currents variables is attractive in terms of equation count. Comparing the number of DAE equations versus the number of equations in $\mathbf{R}_{loopi}^{k+1}\mathbf{i}_{loopi}^{k+1} = \mathbf{e}_{loopi}^{k+1}$ (for p=1), the equation count of the latter is lower. Low equation-count simulation results in faster solution times. The same can be said of a formulation using node voltages as variables, where typically there are more node equations than loop equations. Another factor that results in fast computation times is the sparsity of the loop formulation. The loop current approach results in a system over 99% sparse, which is solved very effectively.

The simulation approach in this work is both single and/or multicore. The simulation approach was implemented by assigning one subsystem per thread instead of one subsystem per core. The latter method imposed a limitation on the maximum number of partitions since there are only four cores to a multicore PC (quad-core computers are readily available desktop computers; however, as of the writing dual-cores are more common). The simulation approach, by assigning threads to subsystems, permits simulating a partitioned SPS on a single core. From Fig. 4.3.39, the gain with a single core simulation neared 20x with Δt=500μs, which indicates that parallelism is not a necessary pre-requisite (though it is desired).

Due to the low-latency of shared-memory computers, thread synchronizations and subsystem overheads were found to be negligible. It was shown that for p=11, which gave the least run-time for all Δt, the amount of time spend in thread overhead was a fractional percent of the run-time. This result is due to the low-latency in data sharing, idle-time, and thread synchronization that in shared-memory computers is not pronounced. Although subsystem imbalances were not expected, their presence however was not detrimental overall.

5.1.2 Limitations of the Solution Methodology

The first limitation was that capacitor loops were required to implement partitioning approach. Not all SPS cables were modeled as having capacitor loops [81]; however, the inclusion of capacitors in cables of short length should be considered. Capacitor loops introduce complex eigenvalues causing oscillatory transients otherwise not observable in resistive-inductive networks [110]. Another motivation to include cable capacitance is to perform transient recovery voltage studies [30],[82].

It should be highlighted that for the partitioning method presented in this work to be effective, capacitor loops must exist at buses (i.e., switchboards or load centers). Buses produce dense off-diagonal regions in the loop resistance matrix because many loop currents are coupled to each other at the same two capacitors. By shorting two capacitors at a bus, much of the off-diagonal region in $\mathbf{R}_{loopi}^{k+1}$ becomes zero. This makes the partitioning method particularly effective as the number of flops per time step is proportional to the number of non-zeroes in $\mathbf{R}_{loopi}^{k+1}$.

Another limitation of the partitioning approach presented in this work is that a ground plane must not exist. The partitioning approach has only been validated on a system modeled as purely ungrounded, where two capacitors per capacitor loop were torn. The presence of ground capacitance would require additional tearing that have not been considered (i.e., tearing two capacitors per cable would no longer suffice).

An AC-Radial SPS model was used in this work. Although other, new, and emerging SPS architectures exists (e.g., the future all-electric ship), the partitioning approach has been tailored to an AC-Radial SPS. Complex SPS models employing both AC- and DC-side have not been tested while writing the work.

A shared memory machine was used to implement this work. Though the idea of a PC-cluster is plausible, said implementation is likely to result in less speed gain due to the communication delay of a physical network. Shared-memory machines are flexible in terms of permissible subsystem imbalance because incurred dead-time is recuperated by the speed at which the subsystems access shared memory. On a PC-cluster, if the computational nodes were imbalanced as a result of subsystem imbalance (as in this work), the combined dead-time and communication delay would influence the maximum speed gain.

In this work the capacitance between cable conductors was considered to be linear. While there was no motivation nor was the scope of this research to assume otherwise, tearing non-linear capacitances has not been considered. If component models with non-linear capacitors existed and a boundary created at said capacitors, the results might not be accurate with the presented approach. Finally, although non-linear processes are typically handled iteratively, the particular partitioning approach employed in this work did not take into account iterative techniques of any sort.

5.2 FUTURE WORK

Additional case studies and performance metrics may be created to further test and validate the solution methodology presented and examined in detail in this work. The case study provided in Chapter IV modeled nine sequential homogeneous three-phase faults. Another research work to look into is that is likely and expected that under different assumptions and applying the faults sequentially in lesser time-intervals different estimates may be obtained. Within the behavior and restrictions of the work presented, the interval between each fault was 6 cycles, which allowed the extinction of many transients before the next fault was applied.

Rigorisity and coverage of most possible scenarios--if not all—in setting up a case study is central to determining whether the partitioning approach is valid. Consequently, the degree of complexity the researcher engages in will determine the type of results he or she will obtain from a work similar to the one provided. Asides from sequential faults, one recommendation to further this work is to consider modification *inter alia* of faulting boundaries, simultaneous faults, combinations of single- and three-phase faults, and non-linear faults instead of linear ones.

Another recommendation has to do with gaining full knowledge of the emerged errors and average errors treated and analyzed in the work. It is desirable that the error behavior be completely understood. It was shown that the error accounted for followed or depended upon both the number of partitions *p* and the number of boundaries. But *no exact* relationship was found. If future investigation could predict the error in advance, corrective measures could be taken to damp (or even prevent) said error.

Optimizations at the programming level that can improve the speed gain are:

- Using *N*-core machines
- Reducing thread overhead times
- Exploit subsystem latency
- Automatic thread-to-core assignment
- Assessment of when it is justifiable to partition
- Sequential vs. simultaneous subsystem solution
- Choice of granularity
- Fill-in reduction
- Sparse matrix storage techniques
- Use existing hyper-graph partitioning software

Latency exploitation (i.e., multi-rate simulation) takes advantage of the fact that all subsystems may not require the same Δt to simulate. Subsystems with slow time constants can be simulated at larger integer multiples of a base Δt and allow subsystems with faster time constants to better utilize available computational resources. Work in power system simulation using multi-rate simulation techniques have been presented in [33],[60],[111].

Manual thread-assignment is unsafe. Hardware resources on computers are constantly changing and, thus, optimal resource availability cannot be determined analytically. In this regard, assigning one thread per core is not the worse strategy, but it is simplistic in its analysis [104]. Simulation runs have shown that in some cases Windows® is able to better allocate the threads to the cores based on the internal hardware information that it has; in some other cases, manual (unsafe programming) assignments may be better.

Standard sparse linear solvers permute coefficient matrices (say **A)** with a permutation matrix **P**. The permutation matrix is used to permute the rows and columns of **A** to minimize fill-ins during factorization. In this work, triangular factorization was performed without a permutation matrix which is inefficient. A typical (and recommended) approach is the minimum degree ordering (Tinney-II) proposed in [55].

Although the linear subsystems $\mathbf{A}\cdot\mathbf{x}=\mathbf{b}$ in this work are sparse, a sparse storage technique was not used. Speed gain can improve by only storing the non-zero structure of the network matrix. A good storage scheme is the compressed column storage [112], but others are possible. The flop count for component models were based on full-matrix computations. If a sparse storage scheme is used, the vertex weights and cost function that endeavors the best p should be revisited.

An alternative to using the mincut algorithm and create an iterative refinement approach customized to tear capacitor loops, would have been to use hMETIS [113]. The algorithms in hMETIS are targeted towards hyper-graphs arising from large-scale circuit integration (a.k.a., VLSI), are fast, and robust. hMETIS would have taken the representative graph of the SPS and used multilevel hyper-graph bisection to reduce the size of the edge cut. Further, the refinement process would have been more accurate as algorithms based on Kernighan and Lin's do not handle hyper-edges properly. In this work, graph hyper-edges were created due to the loop current couplings at buses.

5.3 CHAPTER SUMMARY

This chapter presented the conclusions of this work, and was organized as advantages and disadvantages of the solution methodology. The subsection on organization summarized each chapter in the order presented. The section on future work suggested that case studies with added complexity and additional performance metrics should be considered.

The multithreaded program developed in C# implemented the partitioning approach correctly, but not necessarily efficiently. An efficient implementation of partitioning theory [4-5],[53],[98] requires raising the importance of this pragmatic step. Lastly, several research topics were described and discussed and other likely research interests were itemized as future work. All in all, these topics concern, and are expected to increase speed gain without affecting accuracy. Several items were listed as future work and are expected to increase speed gain without affecting accuracy.

REFERENCES

[1] ONR Control Challenge Problem [Online]. Available: http: //www.usna.edu/EPNES/

[2] S. Wolfram, *The Mathematica Book.* 5th ed. Champaign: Wolfram Media / Cambridge University Press, 2003.

[3] M. Stoer and F. Wagner, "A Simple Min-Cut Algorithm," *Journal of the ACM,* vol. 44, pp. 585-591, Jul 1997.

[4] G. Kron, *Diakoptics: The Piecewise Solution of Large-Scale Systems.* London: MacDonald & Co., 1963.

[5] H. W. Dommel, "Digital Computer Solution of Electromagnetic Transients in Single- and Multiphase Networks," *IEEE Transactions on Power Apparatus and Systems,* vol. 4, pp. 388-399, 1969.

[6] K. L. Butler-Purry, "An ONR Young Investigator Project - Predictive Reconfiguration of Shipboard Power Systems," in *Proc. 2004 Power Engineering Society General Meeting*, p. 975.

[7] K. L. Butler-Purry and N. D. R. Sarma, "Visualization for Shipboard Power Systems," in *Proc. 2002 IEEE 36th Hawaii International Conference on System Sciences (HICSS'03).*

[8] K. L. Butler-Purry and N. D. R. Sarma, "Geographical Information Systems for Automation of Shipboard Power Systems," *Naval Engineers Journal,* vol. 118, pp. 63-75, 2006.

[9] K. L. Butler-Purry, N. D. R. Sarma, C. Whitcomb, H. D. Carmo, and H. Zhang, "Shipboard Systems Deploy Automated Protection," *IEEE Computer Applications in Power,* vol. 11, pp. 31-36, April, 1998.

[10] J. I. Ykema, "Protective Devices in Navy Shipboard Electrical Power Systems," *Naval Engineers Journal,* vol. 100, pp. 166-179.

[11] USS Monterey (CG 61) Homepage (Jan. 2010) [Online]. Available: http: //www.monterey.navy.mil/

[12] K. L. Butler-Purry, N. D. R. Sarma, C. Whitcomb, H. D. Carmo, and H. Zhang, "Shipboard Systems Deploy Automated Protection," *IEEE Computer Applications in Power,* vol. 11, pp. 31-36, 1998.

[13] Power Engineering Education Committee - Digital Educational Resources (Jan. 2010) [Online]. Available: http: //www.ece.mtu.edu/faculty/ljbohman/peec/Dig_Rsor.htm#Software

[14] Power System Simulator PSCAD (Jan. 2010) [Online]. Available: http: //pscad.com/

[15] Power System Simulator ETAP (Jan. 2010) [Online]. Available: http: //www.etap.com

[16] Power System Simulator EMTP-RV (Jan. 2010) [Online]. Available: http: //www.emtp.com

[17] PLECS (Jan. 2010) [Online]. Available: http://www.plexim.com

[18] MathWorks Inc. (Jan. 2010) [Online]. Available: http: //www.mathworks.com/products/simpower/

[19] Power Factory (Jan. 2010) [Online]. Available: http: //www.digsilent.com/

[20] PowerWorld Corporation's PowerWorld (Jan. 2010) [Online]. Available: http: //powerworld.com

[21] CanAm EMTP Users Group ATP (Jan. 2010) [Online]. Available: http: //www.ece.mtu.edu/atp/

[22] InterPSS (Jan. 2010) [Online]. Available: http: //www.interpss.org

[23] Virtual Test Bed 2003 (Jan. 2010) [Online]. Available: http: //vtb.ee.sc.edu/

[24] H. W. Dommel, *Electromagnetic Transients Program Theory Book (EMTP Theory Book).* Portland, OR: Bonneville Power Administration, 1986.

[25] PSCAD [Online]. Available: http://pscad.com/

[26] Manitoba HVDC Research Centre, Inc., *EMTDC User's Guide - A Comprehensive Resource for EMTDC.* Manitoba, Canada: Manitoba HVDC Research Centre, 2005.

[27] Opal-RT Video:A Multi-Core PC-based Simulator for the Hardware-In-the-Loop Testing of Modern Train and Ship Traction Systems (Jan. 2010) [Online]. Available: http: //www.opal-rt.com/technical-document/multi-core-pc-based-simulator-hardware-loop-testing-modern-train-and-ship

[28] J. R. Marti, L. R. Linares, J. Calviño, H. W. Dommel, and J. Lin, "OVNI: An Object Approach to Real-Time Power System Simulators," in *Proc. 1998*

International Conference on Power System Technology (Powercon'98), Beijing, China.

[29] Opal-RT Video: 330 Bus Large Scale Real-Time Power Systems Simulation (Jan. 2010) [Online]. Available: http: //www.planet-rt.com/video/330-bus-large-scale-real-time-power-systems-simulation-0?releaseId=963

[30] A. Greenwood, *Electrical Transients in Power Systems.* 2nd ed. New York: John Wiley & Sons, 1991.

[31] IEEE Power Systems Engineering Committee, "Parallel Processing in Power Systems Computation," *IEEE Transactions on Power Systems,* vol. 7, pp. 629-38, 1992.

[32] C. T. Liu and T. S. Yeh, "Parallel Simulation of Industrial Power System Transients by an Inherent Parallel Algorithm," *International Journal of Electrical Power & Energy Systems,* vol. 18, pp. 437-443, Oct 1996.

[33] G. Chen and X. Zhou, "Asynchronous Parallel Electromagnetic Transient Simulation of Large Scale Power System," *International Journal of Emerging Power Systems,* vol. 2, pp. 1-13, 2005.

[34] A. Y. Zomaya, *Parallel and Distributed Computing Handbook.* New York: McGraw-Hill, 1996.

[35] J. Duffy, *Concurrent Programming on Windows.* Upper Saddle River, NJ: Addison-Wesley, 2009.

[36] F. Zhe, Q. Feng, A. Kaufman, and S. Yoakum-Stover, "GPU Cluster for High Performance Computing," in *Proc. 2004 ACM/IEEE Conference on Supercomputing*, pp. 47-47.

[37] V. Kindratenko, J. Enos, G. Shi, M. Showerman, G. Arnold, J. Stone, and W. H. J. Phillips, "GPU Cluster for High Performance Computing," in *Proc. 2009 Workshop on Parallel Programming on Accelerator Clusters PPAC'09*, pp. 1-8.

[38] L. Bergeron, *Water Hammer in Hydraulics and Wave Surges in Electricity.* New York: John Wiley & Sons, 1961.

[39] D. M. Falcao, E. Kaszkurewicz, and H. L. S. Almeida, "Application of Parallel Processing Techniques to the Simulation of Power-System Electromagnetic Transients," *IEEE Transactions on Power Systems,* vol. 8, pp. 90-96, 1993.

[40] J. A. Hollman and J. R. Marti, "Real Time Network Simulation With PC-Cluster," *IEEE Transactions on Power Systems,* vol. 18, pp. 563-569, 2003.

[41] J. A. Hollman, "Real-Time Distributed Network Simulation with PC Clusters." M.S. thesis: University of British Columbia, 1999.

[42] J. R. Marti and L. R. Linares, "Real-Time EMTP-based Transients Simulation," *IEEE Transactions on Power Systems,* vol. PWRS-9, pp. 1309-1317, 1993.

[43] P. W. Sauer and M. A. Pai, *Power System Dynamics and Stability.* Upper Saddle River, N.J.: Prentice Hall, 1998.

[44] T. Noda and S. Sasaki, "Algorithms for Distributed Computation of Electromagnetic Transients toward PC Cluster Based Real-Time Simulations," in *Proc. 2003 International Conference on Power System Transients*, New Orleans, LA.

[45] T. L. Pillage, R. A. Rohrer, and C. Visweswariah, *Electronic Circuit & System Simulation Methods.* NY: McGraw-Hill, Inc., 1995.

[46] R. A. Rohrer, "Circuit Partitioning Simplified," *IEEE Transactions on Circuits and Systems,* vol. 35, pp. 2-5, 1988.

[47] J. Schutt-Aine, "Stability Analysis of the Latency Insertion Method Using a Block Matrix Formulation," in *Proc. 2008 Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, pp. 155-158.

[48] J. Schutt-Aine, "Latency Insertion Method (LIM) for the Fast Transient Simulation of Large Networks," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 48, pp. 81-89, 2001.

[49] T. Watanabe, Y. Tanji, H. Kubota, and H. Asai, "Fast Transient Simulation of Power Distribution Networks Containing Dispersion Based on Parallel-Distributed Leapfrog Algorithm," *IEICE Trans. Fundamentals,* vol. E90, pp. 388-397, 2007.

[50] J. Langston, S. Suryanarayanan, M. Steurer, M. Andrus, S. Woodruff, and P. F. Ribeiro, "Experiences with the Simulation of a Notional All-Electric Ship Integrated Power Systems on a Large-Scale High-Speed Electromagnetic Transients Simulator," in *Proc. 2007 Electric Ship Technologies Symposium*, Arlington, VA, pp. 1-5.

[51] G. D. C. Dufour, J-N. Paquin, J. Bélanger, (Jan. 2010), [Online]. Available: A Multi-Core PC-based Simulator for the Hardware-In-the-Loop Testing of Modern Train and Ship Traction Systems (http://www.opal-rt.com/technical-document/multi-core-pc-based-simulator-hardware-loop-testing-modern-train-and-ship)

[52] A. E. A. Araujo, H. W. Dommel, and J. R. Marti, "Simultaneous Solution of Power and Control Systems Equations," *IEEE Transaction on Power Systems,* vol. 8, pp. 1483-1489, 1993.

[53] G. Kron, *Tensor Analysis of Networks.* Schenectady, NY: John Wiley & Sons, Inc., 1939.

[54] G. Kron, "Tensorial Analysis of Integrated Transmission Systems," *AIEE,* vol. 71, pp. 814-822, 1952.

[55] W. F. Tinney and J. W. Walker, "Direct Solutions of Sparse Network Equations by Optimally Ordered Triangular Factorization," *Proc. of the IEEE,* vol. 55, pp. 1801-1809, 1967.

[56] C. W. Ho, A. E. Ruehli, and P. A. Brennan, "Modified Nodal Approach to Network Analysis," *IEEE Transactions on Circuits and Systems,* vol. Ca22, pp. 504-509, 1975.

[57] A. Brameller, M. N. John, and M. R. Scott, *Practical Diakoptics for Electrical Networks.* London: Chapman & Hall, 1969.

[58] H. H. Happ et. al, *Gabriel Kron and Systems Theory.* Schenectady, N.Y.: Union College Press, 1973.

[59] H. H. Happ, "Diakoptics: The Solution of System Problems by Tearing," *Proceedings of the IEEE,* vol. 62, pp. 930-940, 1974.

[60] J. R. Marti, L. Linares, J. A. Hollman, and F. A. Moreira, "OVNI: Integrated Software/Hardware Solution for Real-Time Simulation of Large Power Systems," in *Proc. 2002 Power Systems Computation Conference (PSCC'02)*, Sevilla, Spain, pp. 1-7.

[61] M. Armstrong, J. R. Marti, L. R. Linares, and P. Kundur, "Multilevel MATE for Efficient Simultaneous Solution of Control systems and Nonlinearities in the OVNI Simulator," *IEEE Transactions on Power Systems,* vol. 21, pp. 1250-1259, Aug 2006.

[62] K. W. Chan, R. C. Dai, and C. H. Cheung, "A Coarse Grain Parallel Solution Method for Solving Large Sets of Power System Network Equations," in *Proc. 2002 International Conference on Power System Technology (PowerCon '02)*, pp. 2640-2644.

[63] S. Jiwu, X. Wei, and Z. Weimin, "A Parallel Transient Stability Simulation for Power Systems," *IEEE Transactions on Power Systems,* vol. 20, p. 1709, 2005.

[64] A. Kalantari and S. M. Kouhsari, "An Exact Piecewise Method for Fault Studies in Interconnected Networks," *International Journal of Electrical Power & Energy Systems,* vol. 30, pp. 216-225, 2008.

[65] S. Esmaeili and S. M. Kouhsari, "A Distributed Simulation Based Approach for Detailed and Decentralized Power System Transient Stability Analysis," *Electric Power Systems Research,* vol. 77, pp. 673-684, 2007.

[66] H. V. Henderson and S. R. Searle, "On Deriving the Inverse of a Sum of Matrices," *SIAM Review,* vol. 23, pp. 53-60, 1981.

[67] I. S. Duff, A. M. Erisman, and J. K. Reid, *Direct Methods for Sparse Matrices.* Oxford: Oxford University Press, 1986.

[68] Z. Quming, S. Kai, K. Mohanram, and D. C. Sorensen, "Large Power Grid Analysis Using Domain Decomposition," in *Proc. 2006 Design, Automation and Test in Europe, 2006. DATE '06. Proceedings*, pp. 1-6.

[69] H. R. Martens and D. R. Allen, *Introduction to System Theory.* New York: Charles E. Merrill Publishing Company, 1969.

[70] J. G. Ciezki and R. W. Ashton, "The Resolution of Algebraic Loops in the Simulation of Finite-Inertia Power Systems," in *Proc. 1998 IEEE International Symposium on Circuits and Systems*, pp. 342-345.

[71] N. Watson and J. Arrillaga, *Power Systems Electromagnetic Transients Simulation.* 1st ed. London: IEE, 2003.

[72] IEEE Committee Report, "Computer Representation of Excitation Systems," *IEEE Transactions on Power Apparatus and Systems,* vol. PAS-87, pp. 1460–1464, 1967.

[73] Z. A. Yamayee and J. L. Bala, *Electromechanical Energy Devices and Power Systems.* New York: Wiley, 1994.

[74] P. M. Anderson, *Analysis of Faulted Power Systems.* 5th ed. New York: IEEE Press, 1995.

[75] P. M. Anderson and A. A. Fouad, *Power System Control and Stability.* 5th ed. New York: IEEE Press, 1994.

[76] J. Machowski, J. W. Bialek, and J. R. Bumby, *Power System Dynamics and Stability.* Chichester, NY: John Wiley, 1997.

[77] A. M. Gole, A. Keri, C. Nwankpa, E. W. Gunther, H. W. Dommel, I. Hassan, J. R. Marti, J. A. Martinez, K. G. Fehrle, L. Tang, M. F. McGranaghan, O. B. Nayak, P. F. Ribeiro, R. Iravani, and R. Lasseter, "Guidelines for Modeling Power Electronics in Electric Power Engineering Applications," *IEEE Transactions on Power Delivery,* vol. 12, pp. 505-514, Jan 1997.

[78] M. Rashid, *Power Electronics Circuits, Devices, and Applications.* 2nd ed. Pensacola, FL: Pearson Education, 1993.

[79] R. Krishnan, *Electric Motor Drives Modelling, Analysis, and Control.* Blacksburg, VA: Prentice Hall, 2001.

[80] B. K. Bose, *Modern Power Electronics and AC Drives.* Upper Saddle River, NJ: Prentice Hall, 2002.

[81] L. Qi and K. L. Butler-Purry, "Reformulated Model Based Modeling and Simulation of Ungrounded Stiffly Connected Power Systems," in *Proc. 2003 IEEE Power Engineering Society General Meeting*, pp. 725-730.

[82] R. D. Garzon, *High Voltage Circuit Breakers : Design and Applications.* 2nd ed. New York: Marcel Dekker, 2002.

[83] K. Strunz, *Numerical Methods for Real Time Simulation of Electromagnetics in AC/DC Network Systems.* Düsseldorf: VDI Verlag, 2002.

[84] J. Arrillaga and N. R. Watson, *Computer Modeling of Electrical Power Systems.* 2nd ed. Christchurch, New Zealand: John Wiley & Sons, LTD, 2001.

[85] T. Funaki, T. Takazaqa, T. Tada, A. Kurita, and X. Cao, "A Study on the Usage of CDA in EMTP Simulations," in *Proc. 2003 International Conference on Power Systems Transients*, New Orleans, pp. 1-6.

[86] J. R. Marti and J. Lin, "Suppression of Numerical Oscillations in the EMTP," *IEEE Transactions on Power Systems,* vol. 4, pp. 739-747, 1989.

[87] K. Strunz, "Flexible Numerical Integration for Efficient Representation of Switching in Real Time Electromagnetic Transients Simulation," *IEEE Transactions on Power Delivery,* vol. 19, pp. 1276-1283, Jul 2004.

[88] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics.* 3rd ed. New York: John Wiley & Sons, 2003.

[89] M. Crow, *Computational Methods for Electric Power Systems.* Rolla, MO: CRC Press, 2003.

[90] R. M. Kielkowski, *Inside SPICE.* 2nd ed. New York: McGraw-Hill, 1998.

[91] L. Chua and C. Li-Kuan, "On Optimally Sparse Cycle and Coboundary Basis for a Linear Graph," *Circuit Theory, IEEE Transactions on,* vol. 20, pp. 495-503, 1973.

[92] A. G. Exposito, E. R. Ramos, and M. D. Godino, "Two Algorithms for Obtaining Sparse Loop Matrices," *IEEE Transactions on Power Systems,* vol. 21, pp. 125-131, 2005.

[93] F. M. Uriarte and K. L. Butler-Purry, "Diakoptics in Shipboard Power System Simulation," in *Proc. September 17-19, 2006 North American Power Symposium (NAPS)*, Southern Illinois University, Carbondale.

[94] H. H. Happ, "Diakoptics and Piecewise Methods," *IEEE Transactions on Power Apparatus and Systems,* vol. PAS-89, pp. 1373-1382, 1970.

[95] A. Klos, "What Is Diakoptics?," *International Journal of Electrical Power & Energy Systems,* vol. 4, pp. 192-195, 1982.

[96] P. Zhang, J.R.Marti, and H. W. Dommel, "Network Partitioning for Real-Time Power System Simulation," in *Proc. June 19-23, 2005 The International Conference on Power System Transients*, Montreal, Canada, pp. 1-6.

[97] K. Wang, "Piecewise Method for Large-Scale Electrical Networks," *Circuits and Systems, IEEE Transactions on [Legacy, pre - 1988],* vol. 20, pp. 255-258, 1973.

[98] G. Kron, *Tensors for Circuits (formerly entitled A Short Course in Tensor Analysis for Electrical Engineers).* 2nd ed. Schenectady, NY: Dover Publications, Inc., 1959.

[99] G. T. Heydt, *Computer Analysis Methods for Power Systems.* 2nd ed. Chelsea, MI: Stars in a Circle Publications, 1996.

[100] B. W. Kernighan and S. Lin, "An Efficient Heuristic Procedure for Partitioning Graphs," *Bell Laboratories Record,* vol. 49, pp. 291-307, 1970.

[101] G. Karypis and V. Kumar, "Multilevel Graph Partitioning Schemes," in *Proc. 1995 Intl. Conference on Parallel Processing*, pp. 113-122.

[102] G. Cafaro and E. Margarita, "Method for Optimal Tearing of Electrical Networks," *International Journal of Electrical Power & Energy Systems,* vol. 4, pp. 185-191, 1982.

[103] J. Albahari and B. Albahari, *C# 3.0 in a Nutshell* 5th ed. Cambridge: O'Reilly, 2007.

[104] B. Wagner, *More Effective C# : 50 Specific Ways to Improve Your C#.* Upper Saddle River, NJ: Addison-Wesley, 2009.

[105] W. D. Passos, *Numerical Methods, Algorithms, and Tools in C#.* Boca Raton, FL: CRC Press, 2010.

[106] C. H. Lai, "Diakoptics, Domain Decoupling and Parallel Computing," *The Computer Journal,* vol. 37, pp. 840-846, 1994.

[107] H. Ding, A. A. Elkeib, and R. Smith, "Optimal Clustering of Power Networks Using Genetic Algorithms," *Electric Power Systems Research,* vol. 30, pp. 209-214, Sep 1994.

[108] C. S. Chang, L. R. Lu, and F. S. Wen, "Power System Network Partitioning Using Tabu Search," *Electric Power Systems Research,* vol. 49, pp. 55-61, Feb 15 1999.

[109] S. H. Horowitz and A. G. Phadke, *Power System Relaying.* 2nd ed. Blacksburg, VA: John Wiley & Sons, Inc., 1996.

[110] A. L. Shenkman, *Transient Analysis of Electric Power Circuits.* Holon, Israel: Springer, 2005.

[111] F. A. Moreira, J. R. Marti, and L. Linares, "Electromagnetic Transients Simulation with Different Time Steps: The Latency Approach," in *Proc. 2003 International Conference on Power System Transients (IPST)*, New Orleans, LA.

[112] T. A. Davis, *Direct Methods for Sparse Linear Systems.* Philadelphia: SIAM, 2006.

[113] G. Karypis, R. Aggarwal, V. Kumar, and S. Shekhar, "Multilevel Hypergraph Partitioning: Applications in VLSI Domain," in *Proc. 1997 Design and Automation Conference*, Minneapolis, pp. 526-529.

[114] J. R. Marti, "A Phase-Domain Synchronous Generator Model Including Saturation Effects," *IEEE Transactions on Power Systems,* vol. 12, pp. 222-229, 1997.

[115] K.-W. Louie, "Phase-domain Synchronous Generator Model for Transients Simulation," M.S. Thesis: University of British Columbia, 1995.

[116] X. Cao, A. Kurita, H. Mitsuma, Y. Tada, and H. Okamoto, "Improvements of Numerical Stability of Electromagnetic Transient Simulation by Use of Phase-Domain Synchronous Machine Models," *Electrical Engineering in Japan,* vol. 128, pp. 53-62, 1999.

[117] P. Kuffel, K. Kent, and G. Irwin, "The Implementation and Effectiveness of Linear Interpolation Within Digital Simulation," in *Proc. 1995 International Conference on Power System Transients*, Lisbon, pp. 499-504.

APPENDIX A

DISCRETIZED COMPONENT MODELS

A. Discretized Component Models

The discretized component models presented next are the discretized versions of the models introduced in Section 2.4.2, but use different notation. The voltages and currents for all component models are from the solution to $\mathbf{R}_{loopi}^{k+1}\mathbf{i}_{loopi}^{k+1} = \mathbf{e}_{loopi}^{k+1}$, where i represents the subsystem containing the component model.

Synchronous Generator Windings

Discretization of the generator's stator and rotor winding is based on [114-116].

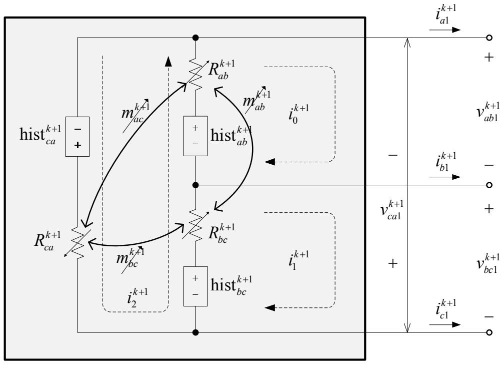


Fig. 5.3.1. Discretized generator stator and rotor windings

$$\begin{bmatrix} R_{ab}^{k+1} & m_{ab}^{k+1} & \begin{pmatrix} m_{ab}^{k+1}+m_{ac}^{k+1} \\ +R_{ab}^{k+1} \end{pmatrix} \\ m_{ab}^{k+1} & R_{bc}^{k+1} & \begin{pmatrix} m_{ab}^{k+1}+m_{bc}^{k+1} \\ +R_{bc}^{k+1} \end{pmatrix} \\ \begin{pmatrix} m_{ab}^{k+1}+m_{ac}^{k+1} \\ +R_{ab}^{k+1} \end{pmatrix} & \begin{pmatrix} m_{ab}^{k+1}+m_{bc}^{k+1} \\ +R_{bc}^{k+1} \end{pmatrix} & \begin{pmatrix} 2\left(m_{ab}^{k+1}+m_{ac}^{k+1}+m_{bc}^{k+1}\right) \\ +R_{ab}^{k+1}+R_{bc}^{k+1}+R_{ca}^{k+1} \end{pmatrix} \end{bmatrix} \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \end{bmatrix} = \begin{bmatrix} \text{hist}_{ab}^{k+1} \\ \text{hist}_{bc}^{k+1} \\ \text{hist}_{ab}^{k+1}+\text{hist}_{bc}^{k+1}\ \text{hist}_{ca}^{k+1} \end{bmatrix} \qquad \text{(A.1)}$$

Generator winding nomenclature:

$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\} = \text{terminal voltages } (\text{V})$

$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\} = \text{line currents out of terminals } (\text{A})$

$\left\{i_0^{k+1}, i_1^{k+1}, i_2^{k+1}\right\} = \text{mesh currents}(\text{A})$

$\left\{\text{hist}_{ab}^{k+1}, \text{hist}_{bc}^{k+1}, \text{hist}_{ca}^{k+1}\right\} = \text{discretized winding inductance}$

historical sources(V)

$m_{ab}^{k+1} = \text{time-varying mutual inductance between winding}$

ab and $bc(\text{H})$

$m_{ac}^{k+1} = \text{time-varying mutual inductance between winding}$

ab and $ca(\text{H})$

$m_{bc}^{k+1} = \text{time-varying mutual inductance between winding}$

bc and $ca(\text{H})$

$\left\{R_{ab}^{k+1}, R_{bc}^{k+1}, R_{ca}^{k+1}\right\} = \text{time-varying discretized winding}$

inductance resistances (Ω)

Synchronous Generator Prime-Mover and Governor

$$\begin{cases} \mathbf{x}_{PMG}^{k+1} = \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{PMG}\right)^{-1}\left(\mathbf{I} + \dfrac{\Delta t}{2}\mathbf{A}_{PMG}\right)\mathbf{x}^{k} + \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{PMG}\right)^{-1}\left(\dfrac{\Delta t}{2}\mathbf{B}_{PMG}\right)\left(\mathbf{u}_{PMG}^{k+1} + \mathbf{u}_{PMG}^{k}\right) \\ \mathbf{y}_{PMG}^{k+1} = \mathbf{C}_{PMG}\mathbf{x}_{PMG}^{k+1} + \mathbf{D}_{PMG}\mathbf{u}_{PMG}^{k+1} \end{cases} \qquad \text{(A.2)}$$

$$\mathbf{A}_{PMG} = \begin{bmatrix} \frac{-1}{T_{FT}} & \cdot & \frac{1}{T_{FT}} \\ \cdot & \cdot & \cdot \\ \cdot & \frac{-1}{T_{FV}} & \frac{-1}{T_{FV}} \end{bmatrix}; \qquad \mathbf{B}_{PMG} = \begin{bmatrix} \cdot & \cdot & \cdot & \cdot & \cdot \\ \dfrac{K_C}{T_C} & \dfrac{\frac{-K_C}{T_C} - \frac{K_C}{\Delta t}}{\omega_{base}^{elec}} & \dfrac{K_C}{\omega_{base}^{elec}\Delta t} & \cdot & \cdot \\ \cdot & \cdot & \cdot & \dfrac{-1}{T_{FV}} & \cdot \end{bmatrix}$$

$$\mathbf{C}_{PMG} = \left[-C_{GNGT} T_{base} \quad \cdot \quad \cdot \right]$$

$$\mathbf{D}_{PMG} = \left[-C_{GNGT} T_{base} \quad \frac{C_{GNGT} T_{base}}{\omega_{base}^{elec}} \quad \cdot \quad C_{1GT} T_{base} \right]$$

$$\mathbf{x}_{PMG}^{k+1} = \left[x_1 \quad x_2 \quad x_3 \right]^{\mathrm{T}}$$

$$\mathbf{u}_{PMG}^{k+1} = \left[\omega_{mech}^{\mathrm{pu}ref} \quad \left(\omega_{ROT}^{\mathrm{pu}mech} \right)^{k+1} \quad \left(\omega_{ROT}^{\mathrm{pu}mech} \right)^{k} \quad WF10s \quad C2GT \right]^{\mathrm{T}}$$

$$\mathbf{y}_{PMG}^{k+1} = T_{PMG}^{\mathrm{pu}mech}$$

Prime-mover and governor nomenclature:

$\left\{ T_{FT}, T_{FV}, W_{F10s}, C_{1GT}, C_{2GT}, C_{GNGT} \right\}$ = prime-mover constants

K_C = governor gain

T_C = governor time-constant

T_{base} = generator base torque

$\omega_{mech}^{\mathrm{pu}ref}$ = reference speed

$\omega_{ROT}^{\mathrm{pu}mech}$ = per-unit rotor speed

$\mathbf{y}_{PMG}^{k+1}$ = prime-mover's output torque

$$\begin{cases} \mathbf{x}_{ROT}^{k+1} = \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{ROT}\right)^{-1}\left(\mathbf{I} + \dfrac{\Delta t}{2}\mathbf{A}_{ROT}\right)\mathbf{x}^{k} \\ \qquad + \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{ROT}\right)^{-1}\left(\dfrac{\Delta t}{2}\mathbf{B}_{ROT}\right)\left(\mathbf{u}_{ROT}^{k+1} + \mathbf{u}_{ROT}^{k}\right) \\ \mathbf{y}_{ROT}^{k+1} = \mathbf{C}_{ROT}\mathbf{x}_{ROT}^{k+1} \end{cases} \tag{A.3}$$

$$\mathbf{A}_{ROT} = \begin{bmatrix} \cdot & 1 \\ \cdot & \dfrac{-D}{J} \end{bmatrix}; \qquad \mathbf{B}_{ROT} = \begin{bmatrix} \cdot & \cdot \\ \dfrac{1}{J} & \dfrac{-1}{J} \end{bmatrix}; \qquad \mathbf{C}_{ROT} = \mathrm{diag}\left(1,1\right);$$

$$\mathbf{x}_{ROT}^{k+1} = \left[\theta_{ROT}^{\mathrm{pu}mech} \quad \omega_{ROT}^{\mathrm{pu}mech}\right]^{\mathrm{T}}; \qquad \mathbf{u}_{ROT}^{k+1} = \left[T_{PMG}^{\mathrm{pu}mech} \quad T_{WND}^{\mathrm{pu}elec}\right]^{\mathrm{T}};$$

Rotor nomenclature:

$D =$ friction coefficient $\left(\text{N-m-s}\right)$

$\theta_{ROT}^{\mathrm{pu}mech} =$ instantaneous rotor position in per-unit

$J =$ moment of intertia in $\left(\text{kg-m}^2\right)$

$\omega_{ROT}^{\mathrm{pu}mech} =$ instantaneous rotor speed in per-unit

$T_{PMG}^{\mathrm{pu}mech} =$ applied mechanical torque $\left(\text{N-m}\right)$

$T_{WND}^{\mathrm{pu}elec} =$ electromagnetic counter-torque $\left(\text{N-m}\right)$

Synchronous Generator Voltage Regulator and Exciter

$$\begin{cases} \mathbf{x}_{VRE}^{k+1} = \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{VRE}\right)^{-1}\left(\mathbf{I} + \dfrac{\Delta t}{2}\mathbf{A}_{VRE}\right)\mathbf{x}^{k} \\ \qquad + \left(\mathbf{I} - \dfrac{\Delta t}{2}\mathbf{A}_{VRE}\right)^{-1}\left(\dfrac{\Delta t}{2}\mathbf{B}_{VRE}\right)\left(\mathbf{u}_{VRE}^{k+1} + \mathbf{u}_{VRE}^{k}\right) \\ \mathbf{y}_{VRE}^{k+1} = \mathbf{C}_{VRE}\mathbf{x}_{VRE}^{k+1} \end{cases} \tag{A.4}$$

$$\mathbf{A}_{VRE}=\begin{bmatrix}-\dfrac{K_E}{T_E} & \cdot & \cdot & \cdot\\ \cdot & -\dfrac{1}{T_{F1}} & \dfrac{1}{T_{F1}} & \cdot\\ \cdot & \cdot & -\dfrac{1}{T_{F2}} & \cdot\\ \cdot & -\dfrac{K_A}{T_A} & \cdot & -\dfrac{1}{T_A}\end{bmatrix};\mathbf{B}_{VRE}=\begin{bmatrix}\cdot & \cdot\\ \cdot & \cdot\\ \cdot & \cdot\\ \dfrac{K_A}{T_A} & \dfrac{-K_A}{T_A}\end{bmatrix};\ \mathbf{C}_{VRE}=\begin{bmatrix}\sqrt{2}V_{base}E_{VRE}^{FD} & 0 & 0 & 0\end{bmatrix}$$

$$\mathbf{x}_{VRE}^{k+1}=\begin{bmatrix}E_{VRE}^{FD} & V_{VRE}^{1} & V_{VRE}^{2} & V_{VRE}^{3}\end{bmatrix}^{\mathrm{T}};\quad \mathbf{u}_{VRE}^{k+1}=\begin{bmatrix}v_{VRE}^{\mathrm{pu}ref} & v_{VRE}^{\mathrm{pu}term}\end{bmatrix}^{\mathrm{T}};$$

Voltage regulator and exciter nomenclature:

$\left\{V_{VRE}^{1},V_{VRE}^{2},V_{VRE}^{3}\right\}$ = excitation system state-variables

$\left\{K_E,K_A,K_F\right\}$=gain coefficients

E_{VRE}^{FD} = field excitation voltage

$\left\{T_{F1},T_{F2},T_A,T_E\right\}$ = time-constants

$v_{VRE}^{\mathrm{pu}ref}$ = reference voltage in per-unit

$v_{VRE}^{\mathrm{pu}term}$ = stator voltage in per-unit

$\mathbf{y}_{VRE}^{k+1}$ = voltage applied to the field winding

Induction Motor

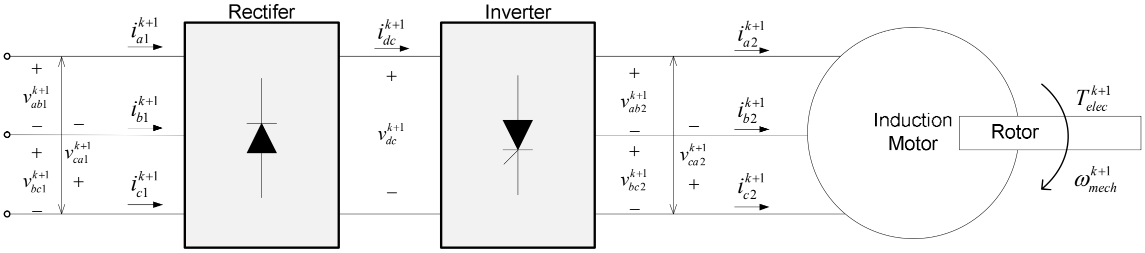


Fig. 5.3.2. Induction motor and drive

Induction Motor Rectifier

The instants of diode commutation are found by polling all diodes to determine whether commutation has occurred. If any diode requests a commutation according to (A.5), the simulation time is interpolated to the earliest diode commutation time and the EN and CNs solved again. Details of the interpolation technique can be found in [52],[117].

$$v_{Di}^{k+1} \rightarrow \begin{cases} > 1\text{V, turn diode on and make } V_{on} = 1\text{V} \\ < 1\text{V, turn diode off } V_{on} = 0\text{V} \\ = 1\text{V, do nothing} \end{cases} \tag{A.5}$$

The diode model are characteristics are shown in Fig. 5.3.3 and Fig. 5.3.4, respectively. Since the diode resistance is time-variant and the diode on-voltage varies between 0Vand 1V, diodes are modeled with the two equations as represent in Fig. 5.3.4.

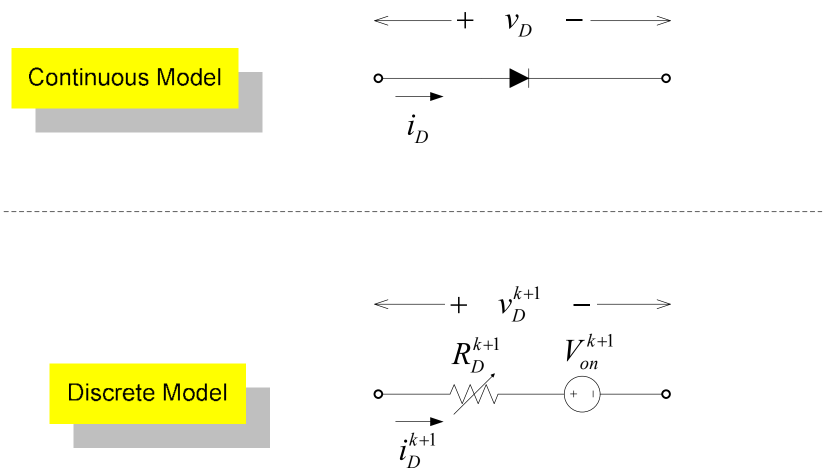


Fig. 5.3.3. Continuous and discretized diode model

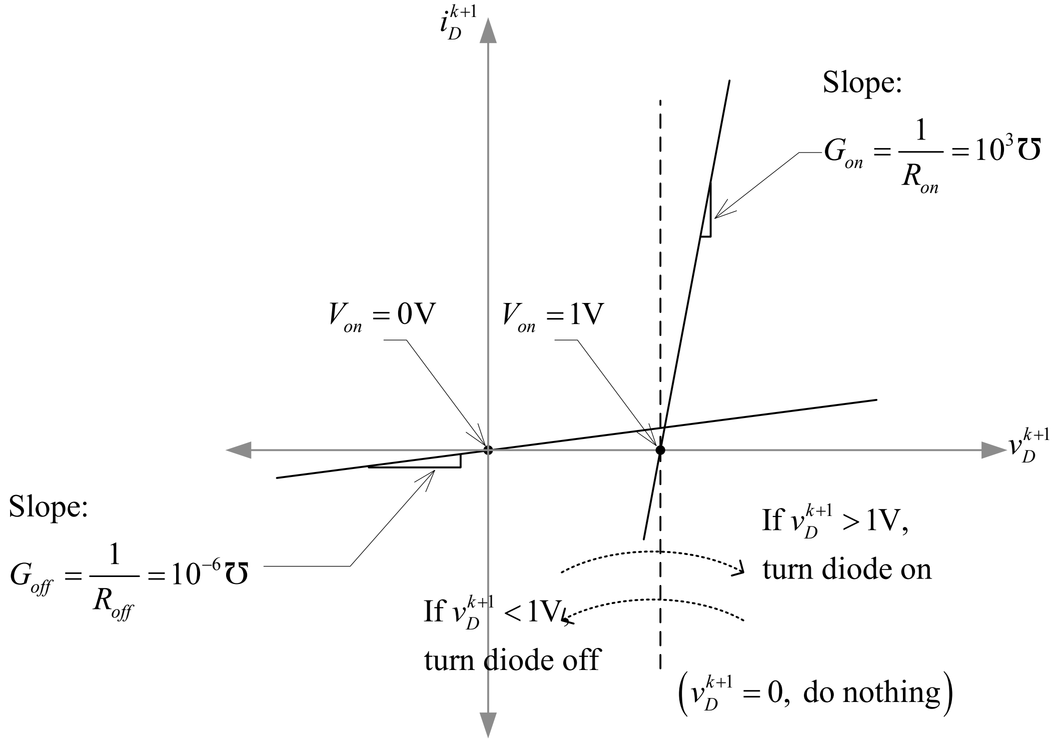


Fig. 5.3.4. Discretized diode voltage and current characteristic

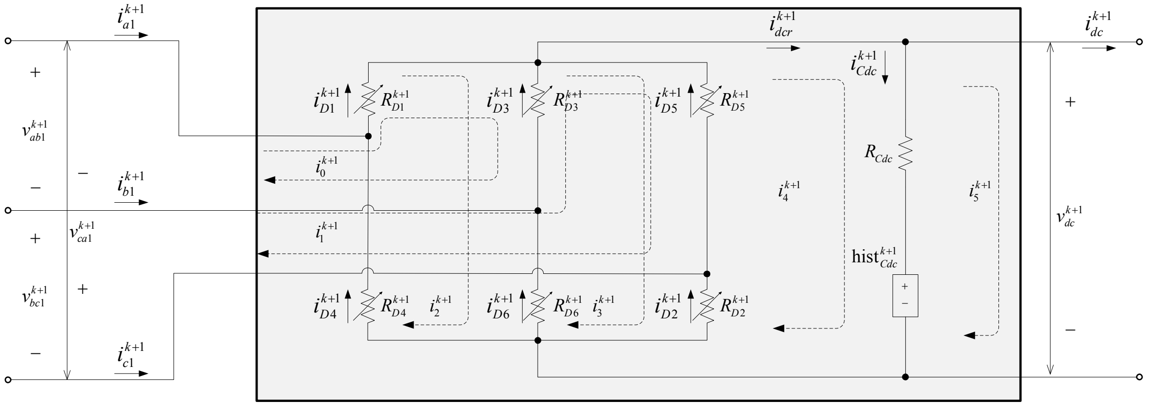


Fig. 5.3.5. Discretized induction motor rectifier model

$$\mathbf{R}_{RCT}^{k+1}\mathbf{i}_{RCT}^{k+1} = \mathbf{e}_{RCT}^{k+1} \tag{A.6}$$

$$\mathbf{R}_{RCT}^{k+1} =$$

$$\begin{bmatrix} R_{D1}^{k+1}+R_{D3}^{k+1} & -R_{D3}^{k+1} & R_{D1}^{k+1}+R_{D3}^{k+1} & -R_{D3}^{k+1} & \cdot & \cdot \\ -R_{D3}^{k+1} & R_{D3}^{k+1}+R_{D5}^{k+1} & -R_{D3}^{k+1} & R_{D3}^{k+1}+R_{D5}^{k+1} & -R_{D5}^{k+1} & \cdot \\ R_{D1}^{k+1}+R_{D3}^{k+1} & -R_{D3}^{k+1} & \left(\begin{matrix} R_{D1}^{k+1}+R_{D3}^{k+1} \\ +R_{D4}^{k+1}+R_{6} \end{matrix}\right) & -R_{D3}^{k+1}-R_{D6}^{k+1} & \cdot & \cdot \\ -R_{D3}^{k+1} & R_{D3}^{k+1}+R_{D5}^{k+1} & -R_{D3}^{k+1}-R_{D6}^{k+1} & \left(\begin{matrix} R_{D2}^{k+1}+R_{D3}^{k+1} \\ +R_{D5}^{k+1}+R_{D6}^{k+1} \end{matrix}\right) & -R_{D2}^{k+1}-R_{D5}^{k+1} & \cdot \\ \cdot & -R_{D5}^{k+1} & \cdot & -R_{D2}^{k+1}-R_{D5}^{k+1} & R_{D2}^{k+1}+R_{D5}^{k+1}+R_{Cdc} & -R_{Cdc} \\ \cdot & \cdot & \cdot & \cdot & -R_{Cdc} & R_{Cdc} \end{bmatrix}$$

$$\mathbf{i}_{RCT}^{k+1} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ i_3^{k+1} \\ i_4^{k+1} \\ i_5^{k+1} \end{bmatrix}; \quad \mathbf{e}_{RCT}^{k+1} = \begin{bmatrix} -V_{on1}^{k+1}+V_{on3}^{k+1} \\ -V_{on3}^{k+1}+V_{on5}^{k+1} \\ -V_{on1}^{k+1}+V_{on3}^{k+1}+V_{on6}^{k+1}-V_{on4}^{k+1} \\ -V_{on3}^{k+1}+V_{on5}^{k+1}+V_{on2}^{k+1}-V_{on6}^{k+1} \\ -V_{on2}^{k+1}-V_{on5}^{k+1}-\text{hist}_{Cdc}^{k+1} \\ \text{hist}_{Cdc}^{k+1} \end{bmatrix}$$

$$R_{Di}^{k+1} \rightarrow \begin{cases} =1\text{m}\Omega\text{, when diode is on} \\ =1\text{M}\Omega\text{, when diode is off} \end{cases}; \quad V_{oni}^{k+1} \rightarrow \begin{cases} =1\text{V, when diode is on} \\ =0\text{V, when diode is off} \end{cases}$$

$$\text{Node voltages} \rightarrow \begin{bmatrix} v_{ab1}^{k+1} \\ v_{bc1}^{k+1} \\ v_{ca1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_{D1}^{k+1}R_{D1}^{k+1}-i_{D3}^{k+1}R_{D3}^{k+1} \\ i_{D3}^{k+1}R_{D3}^{k+1}-i_{D5}^{k+1}R_{D5}^{k+1} \\ i_{D5}^{k+1}R_{D5}^{k+1}-i_{D1}^{k+1}R_{D1}^{k+1} \end{bmatrix}$$

$$\text{Diode currents} \rightarrow \begin{bmatrix} i_{D1}^{k+1} \\ i_{D2}^{k+1} \\ i_{D3}^{k+1} \\ i_{D4}^{k+1} \\ i_{D5}^{k+1} \\ i_{D6}^{k+1} \end{bmatrix} = \begin{bmatrix} 1 & \cdot & 1 & \cdot & \cdot \\ \cdot & \cdot & \cdot & -1 & 1 \\ -1 & 1 & -1 & 1 & \cdot \\ \cdot & \cdot & 1 & \cdot & \cdot \\ \cdot & -1 & \cdot & -1 & 1 \\ \cdot & \cdot & -1 & 1 & \cdot \end{bmatrix} \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ i_3^{k+1} \\ i_4^{k+1} \end{bmatrix}$$

$$\text{Branch currents} \rightarrow \begin{bmatrix} i_{a1}^{k+1} \\ i_{b1}^{k+1} \\ i_{c1}^{k+1} \\ i_{dc}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} - i_0^{k+1} \\ -i_1^{k+1} \\ i_5^{k+1} \end{bmatrix}$$

Induction motor rectifier nomenclature:

$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\}$ = terminal voltages on AC side

$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\}$ = line currents on AC side

$\left\{i_0^{k+1}, i_1^{k+1}, i_2^{k+1}, i_3^{k+1}, i_4^{k+1}\right\}$ = mesh currents (A)

i_{dc}^{k+1} = DC side current (A)

R_{Di}^{k+1} = the i^{th} diode's resistance (Ω)

v_{dc}^{k+1} = DC side output voltage (V)

V_{on} = series on-voltage (V)

Induction Motor Windings

The motor windings are modeled as approximate per-phase equivalent circuits referred to the rotor side [78], where due to slip *s* the winding equations are time-varying.

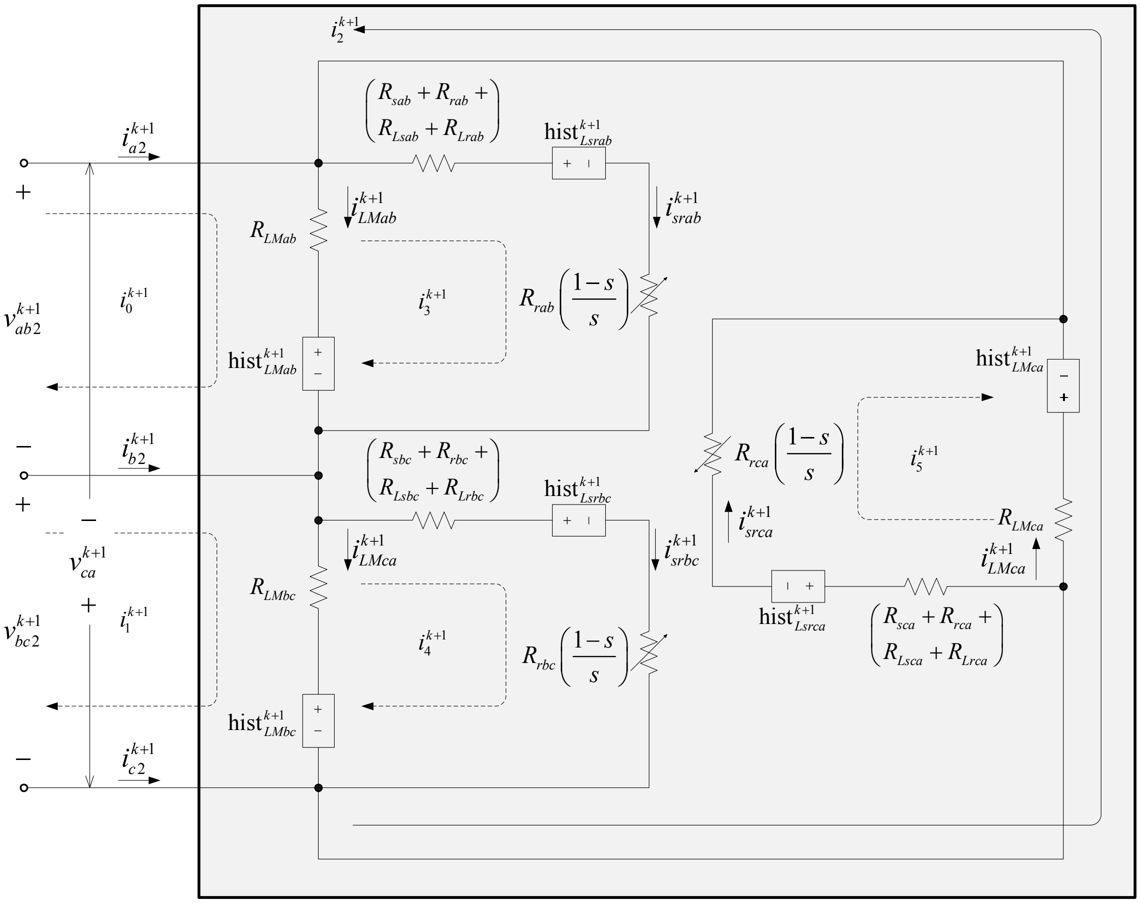

i_2^{k+1}
$\begin{pmatrix} R_{sab}+R_{rab}+ \\ R_{Lsab}+R_{Lrab} \end{pmatrix}$
i_{a2}^{k+1}
$\text{hist}_{Lsrab}^{k+1}$
+
i_{LMab}^{k+1}
i_{srab}^{k+1}
R_{LMab}
v_{ab2}^{k+1}
i_0^{k+1}
i_3^{k+1}
$R_{rab}\left(\frac{1-s}{s}\right)$
hist_{LMab}^{k+1}
hist_{LMca}^{k+1}
−
i_{b2}^{k+1}
$\begin{pmatrix} R_{sbc}+R_{rbc}+ \\ R_{Lsbc}+R_{Lrbc} \end{pmatrix}$
$R_{rca}\left(\frac{1-s}{s}\right)$
i_5^{k+1}
$\text{hist}_{Lsrbc}^{k+1}$
+
−
i_{srca}^{k+1}
R_{LMca}
v_{ca}^{k+1}
i_{LMca}^{k+1}
i_{srbc}^{k+1}
i_{LMca}^{k+1}
R_{LMbc}
+
$\text{hist}_{Lsrca}^{k+1}$
$\begin{pmatrix} R_{sca}+R_{rca}+ \\ R_{Lsca}+R_{Lrca} \end{pmatrix}$
v_{bc2}^{k+1}
i_1^{k+1}
i_4^{k+1}
$R_{rbc}\left(\frac{1-s}{s}\right)$
hist_{LMbc}^{k+1}
−
i_{c2}^{k+1}

Fig. 5.3.6. Discretized induction motor windings model

$$\mathbf{R}_{MOT}^{k+1}\mathbf{i}_{MOT}^{k+1}=\mathbf{e}_{MOT}^{k+1} \tag{A.7}$$

$$\mathbf{R}_{MOT}^{k+1}=\left[\begin{array}{ccc:ccc} R_{LMab} & \cdot & R_{LMab} & -R_{LMab} & \cdot & \cdot \\ \cdot & R_{LMbc} & R_{LMbc} & \cdot & -R_{LMbc} & \cdot \\ R_{LMab} & R_{LMbc} & \left(R_{LMab}+R_{LMbc}+R_{LMca}\right) & -R_{LMab} & -R_{LMbc} & -R_{LMca} \\ \hdashline -R_{LMab} & \cdot & -R_{LMab} & R_{(3,3)} & \cdot & \cdot \\ \cdot & -R_{LMbc} & -R_{LMbc} & \cdot & R_{(4,4)} & \cdot \\ \cdot & \cdot & -R_{LMca} & \cdot & \cdot & R_{(5,5)} \end{array}\right]$$

$$R_{(3,3)} = \begin{pmatrix} R_{sab} + R_{rab} + R_{LMab} \\ R_{Lsab} + R_{Lrab} + R_{rab}\left(\frac{1-s}{s}\right) \end{pmatrix}$$

$$R_{(4,4)} = \begin{pmatrix} R_{sbc} + R_{rbc} + R_{LMbc} \\ R_{Lsbc} + R_{Lrbc} + R_{rbc}\left(\frac{1-s}{s}\right) \end{pmatrix}$$

$$R_{(5,5)} = \begin{pmatrix} R_{sca} + R_{rca} + R_{LMca} \\ R_{Lsca} + R_{Lrca} + R_{rca}\left(\frac{1-s}{s}\right) \end{pmatrix}$$

$$\mathbf{i}_{MOT}^{k+1} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ i_3^{k+1} \\ i_4^{k+1} \\ i_5^{k+1} \end{bmatrix}; \qquad \mathbf{e}_{MOT}^{k+1} = \left[\begin{array}{c} -\mathrm{hist}_{LMab}^{k+1} \\ -\mathrm{hist}_{LMbc}^{k+1} \\ -\mathrm{hist}_{LMab}^{k+1} - \mathrm{hist}_{LMbc}^{k+1} - \mathrm{hist}_{LMca}^{k+1} \\ \hline \mathrm{hist}_{LMab}^{k+1} - \mathrm{hist}_{Lsrab}^{k+1} \\ \mathrm{hist}_{LMbc}^{k+1} - \mathrm{hist}_{Lsrbc}^{k+1} \\ \mathrm{hist}_{LMca}^{k+1} - \mathrm{hist}_{Lsrca}^{k+1} \end{array}\right]$$

$$\text{Magnetizing currents} \rightarrow \begin{bmatrix} i_{LMab}^{k+1} \\ i_{LMbc}^{k+1} \\ i_{LMca}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} + i_2^{k+1} - i_3^{k+1} \\ i_1^{k+1} + i_2^{k+1} - i_4^{k+1} \\ i_2^{k+1} - i_5^{k+1} \end{bmatrix}$$

$$\text{Winding currents} \rightarrow \begin{bmatrix} i_{srab}^{k+1} \\ i_{srbc}^{k+1} \\ i_{srca}^{k+1} \end{bmatrix} = \begin{bmatrix} i_3^{k+1} \\ i_4^{k+1} \\ i_5^{k+1} \end{bmatrix}$$

$$\text{Node voltages} \rightarrow \begin{bmatrix} v_{ab2}^{k+1} \\ v_{bc2}^{k+1} \\ v_{ca2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_{LMab}^{k+1} R_{LMab} + \mathrm{hist}_{LMab}^{k+1} \\ i_{LMbc}^{k+1} R_{LMbc} + \mathrm{hist}_{LMbc}^{k+1} \\ -v_{ab2}^{k+1} - v_{bc2}^{k+1} \end{bmatrix}$$

$$\text{Branch currents} \rightarrow \begin{bmatrix} i_{a2}^{k+1} \\ i_{b2}^{k+1} \\ i_{c2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} - i_0^{k+1} \\ -i_1^{k+1} \end{bmatrix}$$

Induction motor nomenclature:

$$\left\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\right\} = \text{motor windings' terminal voltages } (\text{V})$$

$$\left\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\right\} = \text{motor input line currents } (\text{A})$$

$$\left\{i_{0}^{k+1}, i_{1}^{k+1}, i_{2}^{k+1}, i_{3}^{k+1}, i_{4}^{k+1}, i_{5}^{k+1}\right\} = \text{mesh currents } (\text{A})$$

$$\left\{\text{hist}_{LMab}^{k+1}, \text{hist}_{LMbc}^{k+1}, \text{hist}_{LMca}^{k+1}\right\} = \text{magnetizing inductance historical sources } (\text{V})$$

$$\left\{\text{hist}_{Lsrab}^{k+1}, \text{hist}_{Lsrbc}^{k+1}, \text{hist}_{Lsrca}^{k+1}\right\} = \text{combined stator and rotor leakage inductance historical sources } (\text{V})$$

$$R_{sab} = \text{stator winding resistance of phase } ab \ (\Omega)$$

$$R_{rab} = \text{rotor winding resistance of phase } ab \ (\Omega)$$

$$R_{Lsab} = \text{stator leakage inductance resistance of phase } ab \ (\Omega)$$

$$R_{Lrab} = \text{rotor leakage inductance resistance of phase } ab \ (\Omega)$$

$$R_{LMab} = \text{discretized magnetizing inductance resistance of phase } ab \ (\Omega)$$

$$s = \text{slip coefficient}$$

Induction Motor Inverter

The inverter transistors are modeled as controlled (i.e., $1\text{m}\Omega, \text{or } 1\text{M}\Omega$) resistances and without a snubber circuit.

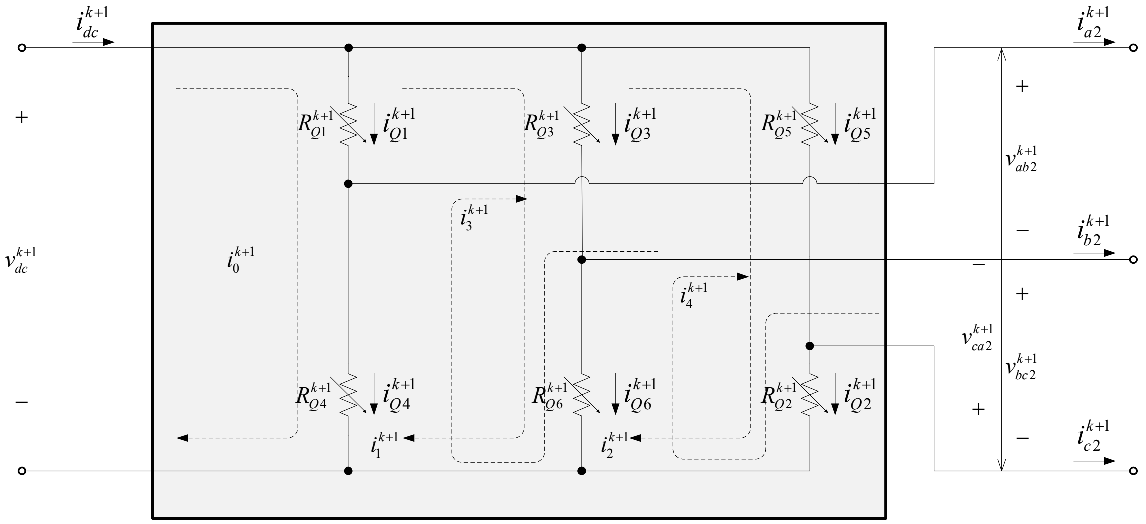


Fig. 5.3.7. Discretized induction motor inverter model

$$\begin{bmatrix} R_{Q1}^{k+1}+R_{Q4}^{k+1} & -R_{Q1}^{k+1}-R_{Q4}^{k+1} & \cdot & -R_{Q4}^{k+1} & \cdot \\ -R_{Q1}^{k+1}-R_{Q4}^{k+1} & \begin{pmatrix} R_{Q1}^{k+1}+R_{Q3}^{k+1} \\ +R_{Q4}^{k+1}+R_{Q6} \end{pmatrix} & -R_{Q3}^{k+1}-R_{Q6}^{k+1} & R_{Q6}^{k+1}+R_{Q4}^{k+1} & -R_{Q6}^{k+1} \\ \cdot & -R_{Q3}^{k+1}-R_{Q6}^{k+1} & \begin{pmatrix} R_{Q2}^{k+1}+R_{Q3}^{k+1} \\ +R_{Q5}+R_{Q6}^{k+1} \end{pmatrix} & -R_{Q6}^{k+1} & R_{Q2}^{k+1}+R_{Q6}^{k+1} \\ -R_{Q4}^{k+1} & R_{Q6}^{k+1}+R_{Q4}^{k+1} & -R_{Q6}^{k+1} & R_{Q4}^{k+1}+R_{Q6}^{k+1} & -R_{Q6}^{k+1} \\ \cdot & -R_{Q6}^{k+1} & R_{Q2}^{k+1}+R_{Q6}^{k+1} & -R_{Q6}^{k+1} & R_{Q2}^{k+1}+R_{Q6}^{k+1} \end{bmatrix} \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ i_3^{k+1} \\ i_4^{k+1} \end{bmatrix} = \begin{bmatrix} \cdot \\ \cdot \\ \cdot \\ \cdot \\ \cdot \end{bmatrix} \tag{A.8}$$

$$\text{Node voltages} \rightarrow \begin{bmatrix} v_{dc}^{k+1} \\ v_{ab2}^{k+1} \\ v_{bc2}^{k+1} \\ v_{ca2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_{Q1}^{k+1}R_{Q1}^{k+1}+i_{Q4}^{k+1}R_{Q4}^{k+1} \\ i_{Q4}^{k+1}R_{Q4}^{k+1}-i_{Q6}^{k+1}R_{Q6}^{k+1} \\ i_{Q6}^{k+1}R_{Q6}^{k+1}-i_{Q2}^{k+1}R_{Q2}^{k+1} \\ i_{Q2}^{k+1}R_{Q2}^{k+1}-i_{Q1}^{k+1}R_{Q1}^{k+1} \end{bmatrix}$$

$$\text{Branch currents} \rightarrow \begin{bmatrix} i_{a2}^{k+1} \\ i_{b2}^{k+1} \\ i_{c2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_3^{k+1} \\ i_4^{k+1} - i_3^{k+1} \\ -i_4^{k+1} \end{bmatrix};$$

Induction motor inverter nomenclature:

$$v_{dc}^{k+1} = \text{terminal voltages on rectifier side } (\text{V})$$

$$\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\} = \text{terminal voltages on motor side} (\text{V})$$

$$\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\} = \text{line currents on motor side} (\text{A})$$

$$\{i_0^{k+1}, i_1^{k+1}, i_2^{k+1}, i_3^{k+1}, i_4^{k+1}\} = \text{mesh currents} (\text{A})$$

$$i_{dc}^{k+1} = \text{DC current from rectifier } (\text{A})$$

$$i_{Qi}^{k+1} = \text{current through the } i^{\text{th}} \text{ transistor } (\text{A})$$

$$R_{Qi}^{k+1} = \text{the } i^{\text{th}} \text{ transistor's resistance } (\Omega)$$

Single-Phase Cable

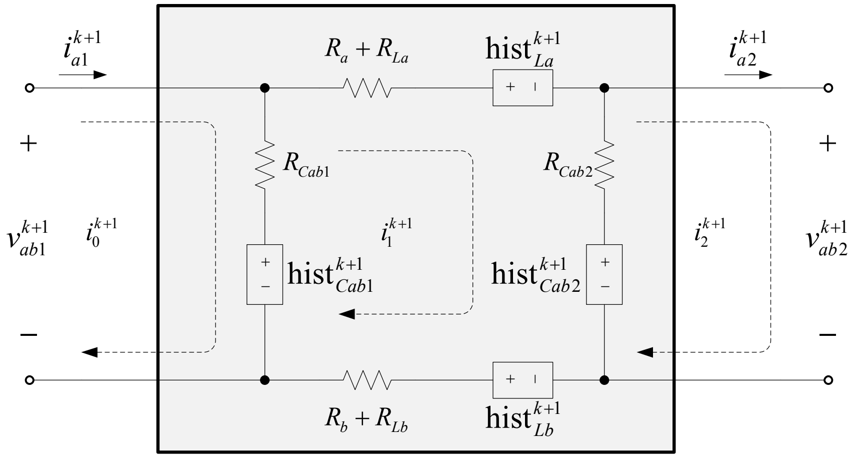


Fig. 5.3.8. Discretized single-phase cable model

$$\mathbf{R}_{Cbl}\mathbf{i}_{Cbl}^{k+1} = \mathbf{e}_{Cbl}^{k+1} \tag{A.9}$$

$$\mathbf{R}_{Cbl}=\begin{bmatrix} R_{Cab1} & -R_{Cab1} & \cdot \\ -R_{Cab1} & \begin{pmatrix} R_{Cab1}+R_a+R_{La}+ \\ R_{Cab2}+R_b+R_{Lb} \end{pmatrix} & -R_{Cab2} \\ \cdot & -R_{Cab2} & R_{Cab2} \end{bmatrix}$$

$$\mathbf{i}_{Cbl}^{k+1}=\begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \end{bmatrix}; \quad \mathbf{e}_{Cbl}^{k+1}=\begin{bmatrix} -\mathrm{hist}_{Cab1}^{k+1} \\ \mathrm{hist}_{Cab1}^{k+1}-\mathrm{hist}_{La}^{k+1}-\mathrm{hist}_{Cab2}^{k+1}+\mathrm{hist}_{Lb}^{k+1} \\ \mathrm{hist}_{Cab2}^{k+1} \end{bmatrix}$$

$$\text{Node voltages}\rightarrow\begin{bmatrix} v_{ab1}^{k+1} \\ v_{ab2}^{k+1} \end{bmatrix}=\begin{bmatrix} \left(i_0^{k+1}-i_1^{k+1}\right)R_{Cab1}+\mathrm{hist}_{Cab1}^{k+1} \\ \left(i_1^{k+1}-i_2^{k+1}\right)R_{Cab2}+\mathrm{hist}_{Cab2}^{k+1} \end{bmatrix}$$

$$\text{Branch currents}\rightarrow\begin{bmatrix} i_{a1}^{k+1} \\ i_{a2}^{k+1} \end{bmatrix}=\begin{bmatrix} i_0^{k+1} \\ i_2^{k+1} \end{bmatrix}$$

Single-phase cable nomenclature:

$\left\{v_{ab1}^{k+1},v_{ab2}^{k+1}\right\}=$ terminal voltages on sides 1 and 2 (V)

$\left\{i_{a1}^{k+1},i_{a2}^{k+1}\right\}=$ line currents on sides 1 and 2 (A)

$\left\{i_0^{k+1},i_1^{k+1},i_2^{k+1}\right\}=$ mesh currents (A)

$R_a=$ cable resistance of phase $a(\Omega)$

$R_{La}=$ discretized cable inductance resistance of phase a (Ω)

$R_{Cab1}=$ discretized cable capacitance resistance
of phase ab, side 1 (Ω)

$\left\{\mathrm{hist}_{Cab1}^{k+1},\mathrm{hist}_{Cab2}^{k+1}\right\}=$ capacitor historical sources on sides 1 and 2 (V)

$\left\{\mathrm{hist}_{La}^{k+1},\mathrm{hist}_{Lb}^{k+1}\right\}=$ inductor historical sources (V)

Three-Phase Cable

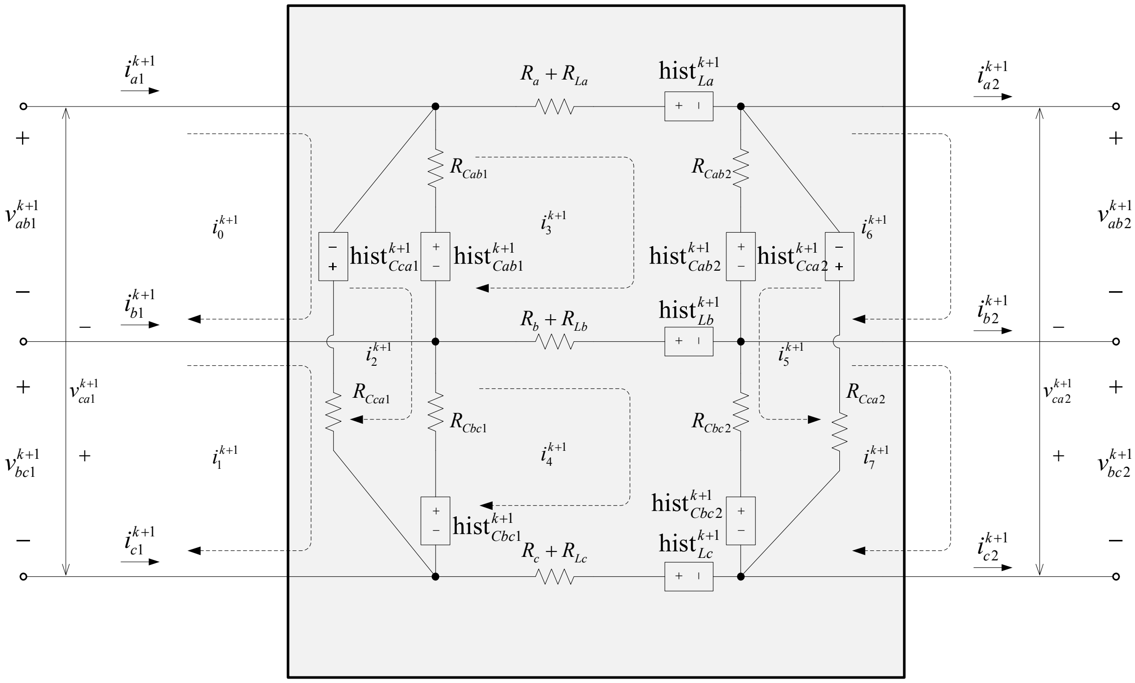


Fig. 5.3.9. Discretized three-phase cable model

$$\mathbf{R}_{CBL}\mathbf{i}_{CBL}^{k+1} = \mathbf{e}_{CBL}^{k+1} \tag{A.10}$$

$$\mathbf{R}_{CBL} =$$

$$\begin{bmatrix}
R_{Cab1} & \cdot & R_{Cab1} & -R_{Cab1} & \cdot & \cdot & \cdot & \cdot \\
\cdot & R_{Cbc1} & R_{Cbc1} & \cdot & -R_{Cbc1} & \cdot & \cdot & \cdot \\
R_{Cab1} & R_{Cbc1} & (R_{22}) & -R_{Cab1} & -R_{Cbc1} & \cdot & \cdot & \cdot \\
-R_{Cab1} & \cdot & -R_{Cab1} & (R_{33}) & -R_a - R_{La} & R_{Cab2} & -R_C & \cdot \\
\cdot & -R_{Cbc1} & -R_{Cbc1} & -R_a - R_{La} & (R_{44}) & R_{Cbc2} & \cdot & -R_C \\
\cdot & \cdot & \cdot & R_{Cab2} & R_{Cbc2} & (R_{55}) & -R_{Cab2} & -R_{Cbc2} \\
\cdot & \cdot & \cdot & -R_C & \cdot & -R_{Cab2} & R_{Cab2} & \cdot \\
\cdot & \cdot & \cdot & \cdot & -R_C & -R_{Cbc2} & \cdot & R_{Cbc2}
\end{bmatrix}$$

$$
\begin{aligned}
R_{22} &= \left(R_{Cab1} + R_{Cbc1} + R_{Cca1}\right)\\
R_{33} &= \left(R_{Cab1} + R_{a} + R_{La} + R_{Cab2} + R_{b} + R_{Lb}\right)\\
R_{44} &= \left(R_{Cab2} + R_{b} + R_{Lb} + R_{Cbc2} + R_{c} + R_{Lc}\right)\\
R_{55} &= \left(R_{Cab2} + R_{Cbc2} + R_{Cca2}\right)
\end{aligned}
$$

$$
\mathbf{i}_{CBL}^{k+1} = \begin{bmatrix} i_0^{k+1}\\ i_1^{k+1}\\ i_2^{k+1}\\ i_3^{k+1}\\ i_4^{k+1}\\ i_5^{k+1}\\ i_6^{k+1}\\ i_7^{k+1} \end{bmatrix}; \qquad
\mathbf{e}_{CBL}^{k+1} = \begin{bmatrix} -\text{hist}_{Cab1}^{k+1}\\ -\text{hist}_{Cbc1}^{k+1}\\ -\text{hist}_{Cab1}^{k+1} - \text{hist}_{Cbc1}^{k+1} - \text{hist}_{Cca1}^{k+1}\\ -\text{hist}_{La}^{k+1} - \text{hist}_{Cab2}^{k+1} + \text{hist}_{Lb}^{k+1} + \text{hist}_{Cab1}^{k+1}\\ -\text{hist}_{Lb}^{k+1} - \text{hist}_{Cbc2}^{k+1} + \text{hist}_{Lc}^{k+1} + \text{hist}_{Cbc1}^{k+1}\\ -\text{hist}_{Cab2}^{k+1} - \text{hist}_{Cbc2}^{k+1} - \text{hist}_{Cca2}^{k+1}\\ \text{hist}_{Cab2}^{k+1}\\ \text{hist}_{Cbc2}^{k+1} \end{bmatrix}
$$

$$
\begin{matrix}\text{Node voltages}\\ \text{side 1}\end{matrix} \rightarrow \begin{bmatrix} v_{ab1}^{k+1}\\ v_{bc1}^{k+1}\\ v_{ca1}^{k+1} \end{bmatrix} = \begin{bmatrix} \left(i_0^{k+1} + i_2^{k+1} - i_3^{k+1}\right) R_{Cab1} + \text{hist}_{Cab1}^{k+1}\\ \left(i_1^{k+1} + i_2^{k+1} - i_4^{k+1}\right) R_{Cbc1} + \text{hist}_{Cbc1}^{k+1}\\ -v_{ab1}^{k+1} - v_{bc1}^{k+1} \end{bmatrix}
$$

$$
\begin{matrix}\text{Node voltages}\\ \text{side 2}\end{matrix} \rightarrow \begin{bmatrix} v_{ab2}^{k+1}\\ v_{bc2}^{k+1}\\ v_{ca2}^{k+1} \end{bmatrix} = \begin{bmatrix} \left(i_3^{k+1} + i_5^{k+1} - i_6^{k+1}\right) R_{Cab2} + \text{hist}_{Cab2}^{k+1}\\ \left(i_4^{k+1} + i_5^{k+1} - i_7^{k+1}\right) R_{Cbc2} + \text{hist}_{Cbc2}^{k+1}\\ -v_{ab2}^{k+1} - v_{bc2}^{k+1} \end{bmatrix}
$$

$$
\text{Branch currents} \rightarrow \begin{bmatrix} i_{a1}^{k+1}\\ i_{b1}^{k+1}\\ i_{c1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1}\\ i_1^{k+1} - i_0^{k+1}\\ -i_2^{k+1} \end{bmatrix}; \qquad \begin{bmatrix} i_{a2}^{k+1}\\ i_{b2}^{k+1}\\ i_{c2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_6^{k+1}\\ i_7^{k+1} - i_6^{k+1}\\ -i_7^{k+1} \end{bmatrix}
$$

Three-phase cable nomenclature:

$$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\} = \text{terminal voltages on side 1 } (\text{A})$$

$$\left\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\right\} = \text{terminal voltages on side 2 } (\text{A})$$

$$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\} = \text{line currents on side 1 } (\text{A})$$

$$\left\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\right\} = \text{line currents on side 2 } (\text{A})$$

$$\left\{i_{0}^{k+1}, i_{1}^{k+1}, i_{2}^{k+1}, i_{3}^{k+1}, i_{4}^{k+1}, i_{5}^{k+1}, i_{6}^{k+1}, i_{7}^{k+1}\right\} = \text{mesh currents } (\text{A})$$

$$R = \text{cable series resistance } (\Omega)$$

$$R_L = \text{discretized inductance resistance } (\Omega)$$

$$R_C = \text{discretized capacitor resistance } (\Omega)$$

$$\left\{\text{hist}_{Cab1}^{k+1}, \text{hist}_{Cbc1}^{k+1}, \text{hist}_{Cca1}^{k+1}\right\} = \text{historical sources of cable capacitance on side 1 } (\text{V})$$

$$\left\{\text{hist}_{Cab2}^{k+1}, \text{hist}_{Cbc2}^{k+1}, \text{hist}_{Cca2}^{k+1}\right\} = \text{historical sources of cable capacitance on side 2 } (\text{V})$$

$$\left\{\text{hist}_{La}^{k+1}, \text{hist}_{Lb}^{k+1}, \text{hist}_{Lc}^{k+1}\right\} = \text{historical sources of cable inductance } (\text{V})$$

Single-Phase Static Load

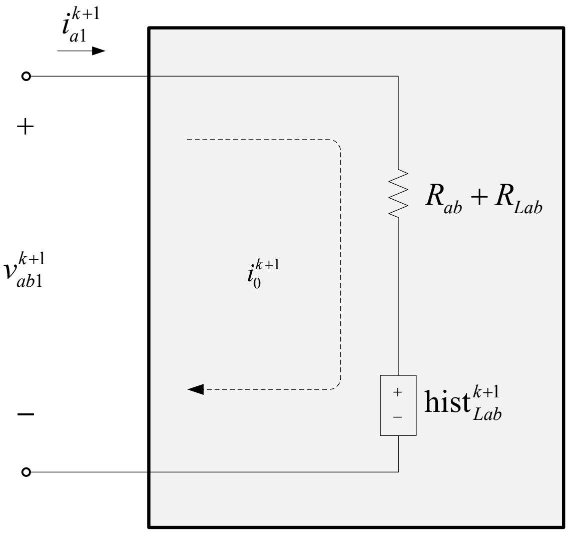


Fig. 5.3.10. Discretized single-phase static load model

$$\left(R_{ab} + R_{Lab}\right) i_0^{k+1} = -\text{hist}_{Lab}^{k+1} \tag{A.11}$$

Node voltages → $v_{ab1}^{k+1} = \left(R_{ab} + R_{Lab}\right) i_0^{k+1} + \text{hist}_{Lab}^{k+1}$
Branch currents → $i_{a1}^{k+1} = i_0^{k+1}$

Given the power rating of a single-phase load, the phase resistance and inductance are computed with (A.12).

$$R_{ab} = \frac{P_{1\varphi} V_{LL}^2}{P_{1\varphi}^2 + Q_{1\varphi}^2} \; (\Omega) \qquad L_{ab} = \frac{Q_{1\varphi} V_{LL}^2}{2\pi f \left(P_{1\varphi}^2 + Q_{1\varphi}^2\right)} \; (\text{H}) \tag{A.12}$$

Single-phase static load nomenclature:

v_{ab1}^{k+1} = terminal voltage (V)

i_{a1}^{k+1} = line current (A)

i_{0}^{k+1} = mesh current (A)

f = system frequency (Hz)

$\mathrm{hist}_{Lab}^{k+1}$ = inductor historical source (V)

L_{ab} = load inductance of phase *ab* (H)

$P_{1\varphi}$ = rated *real* power (W)

$Q_{1\varphi}$ = rated *reactive* power (VARs)

R_{ab} = load resistance of phase *ab* (Ω)

R_{Lab} = discretized load inductance resistance of phase *ab* (Ω)

V_{LL} = rated line-to-line voltage (RMS Volts)

Three-Phase Static Load

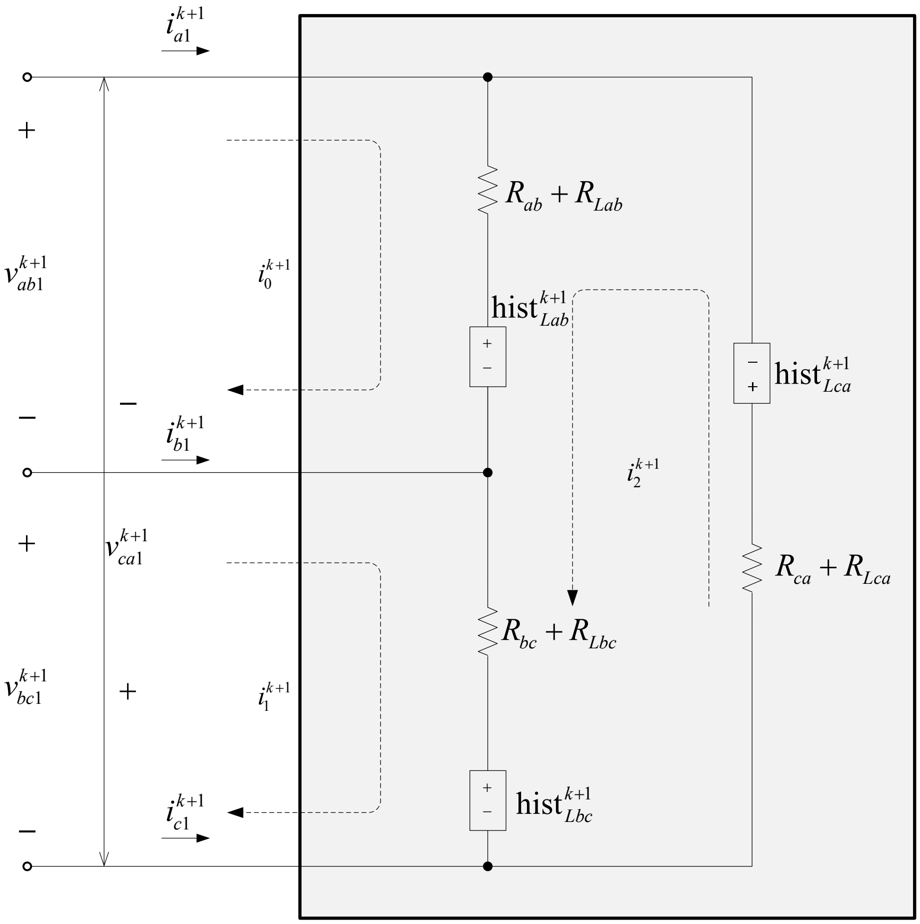


Fig. 5.3.11. Discretized three-phase static load model

$$\mathbf{R}_{LOD}\mathbf{i}_{LOD}^{k+1}=\mathbf{e}_{LOD}^{k+1} \tag{A.13}$$

$$\mathbf{R}_{LOD}=\begin{bmatrix} R_{ab}+R_{Lab} & \cdot & R_{ab}+R_{Lab} \\ \cdot & R_{bc}+R_{Lbc} & R_{bc}+R_{Lbc} \\ R_{ab}+R_{Lab} & R_{bc}+R_{Lbc} & \left(R_{ab}+R_{Lab}+R_{bc}+R_{Lbc}+R_{ca}+R_{Lca}\right) \end{bmatrix}$$

$$\mathbf{i}_{LOD}^{k+1} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \end{bmatrix}; \qquad \mathbf{e}_{LOD}^{k+1} = \begin{bmatrix} -\text{hist}_{Lab}^{k+1} \\ -\text{hist}_{Lbc}^{k+1} \\ -\text{hist}_{Lab}^{k+1} - \text{hist}_{Lbc}^{k+1} - \text{hist}_{Lca}^{k+1} \end{bmatrix}$$

$$\text{Node voltages} \rightarrow \begin{bmatrix} v_{ab1}^{k+1} \\ v_{bc1}^{k+1} \\ v_{ca1}^{k+1} \end{bmatrix} = \begin{bmatrix} \left(i_0^{k+1} + i_2^{k+1}\right)\left(R_{ab} + R_{Lab}\right) + \text{hist}_{Lab}^{k+1} \\ \left(i_1^{k+1} + i_2^{k+1}\right)\left(R_{bc} + R_{Lbc}\right) + \text{hist}_{Lbc}^{k+1} \\ i_2^{k+1}\left(R_{ca} + R_{Lca}\right) + \text{hist}_{Lca}^{k+1} \end{bmatrix}$$

$$\text{Branch currents} \rightarrow \begin{bmatrix} i_{a1}^{k+1} \\ i_{b1}^{k+1} \\ i_{c1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} - i_0^{k+1} \\ -i_2^{k+1} \end{bmatrix}$$

Given the per-phase power rating of a three-phase load, the per-phase resistance and inductance is also computed with (A.12).

Three-phase static load nomenclature:

$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\}$ = terminal voltages (V)

$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\}$ = line currents on side (A)

$\left\{i_0^{k+1}, i_1^{k+1}, i_2^{k+1}\right\}$ = mesh currents (A)

R_{ab} = phase resistance of phase $ab(\Omega)$

R_{Lab} = discretized inductance resistance of phase $ab(\Omega)$

$\left\{\text{hist}_{Lab}^{k+1}, \text{hist}_{Lbc}^{k+1}, \text{hist}_{Lca}^{k+1}\right\}$ = load inductance historical sources (V)

Three-Phase Transformer

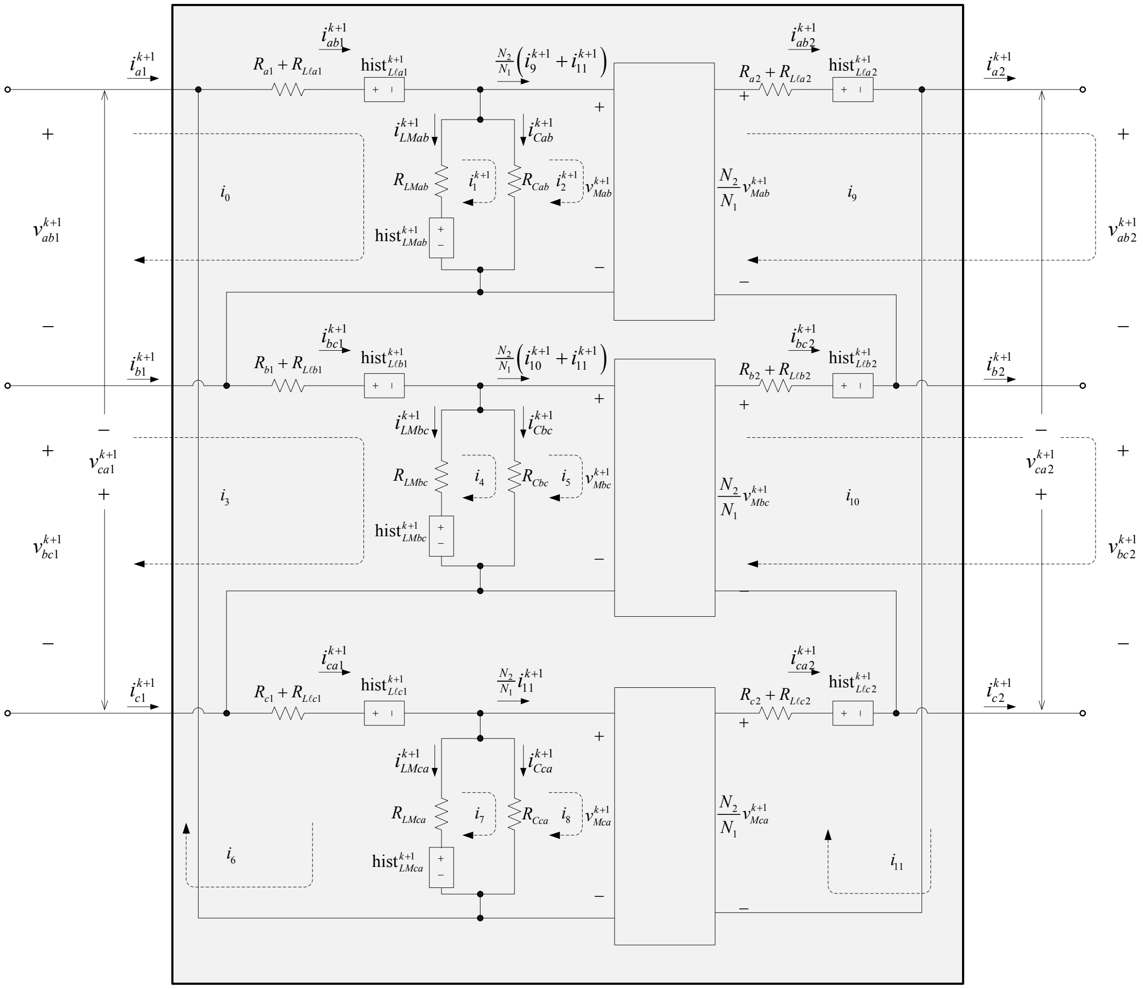


Fig. 5.3.12. Discretized three-phase transformer model (Δ-Δ)

$$\mathbf{R}_{XFM}^{k+1}\mathbf{i}_{XFM}^{k+1}=\mathbf{e}_{XFM}^{k+1} \tag{A.14}$$

$$\mathbf{R}_{XFM}^{k+1} =$$

$$\left[\left[\begin{array}{ccc|ccc|ccc|ccc|ccc}
R_{(0,0)} & -R_{LMab} & \cdot & \cdot & \cdot & \cdot & R_{a1}+R_{L\ell a1} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
-R_{LMab} & \begin{pmatrix} R_{LMab} \\ +R_{Cab} \end{pmatrix} & -R_{Cab} & \cdot & \cdot & \cdot & R_{Cab} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & -R_{Cab} & R_{Cab} & \cdot & \cdot & \cdot & -R_{Cab} & \cdot & \cdot & \cdot & \cdot & \cdot & 1 & \cdot & \cdot \\
\hline
\cdot & \cdot & \cdot & R_{(3,3)} & -R_{LMbc} & \cdot & R_{b1}+R_{L\ell b1} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & -R_{LMbc} & \begin{pmatrix} R_{LMbc} \\ +R_{Cbc} \end{pmatrix} & -R_{Cbc} & R_{Cbc} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & -R_{Cbc} & R_{Cbc} & -R_{Cbc} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & 1 & \cdot \\
\hline
R_{a1}+R_{L\ell a1} & R_{Cab} & -R_{Cab} & R_{b1}+R_{L\ell b1} & R_{Cbc} & -R_{Cbc} & R_{(6,6)} & R_{Cca} & -R_{Cca} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & R_{Cca} & \begin{pmatrix} R_{LMca} \\ +R_{Cca} \end{pmatrix} & -R_{Cca} & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & -R_{Cca} & -R_{Cca} & R_{Cca} & \cdot & \cdot & \cdot & \cdot & \cdot & 1 \\
\hline
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \begin{pmatrix} R_{a2} \\ +R_{L\ell a2} \end{pmatrix} & \cdot & \begin{pmatrix} R_{a2} \\ +R_{L\ell a2} \end{pmatrix} & \frac{-N_2}{N_1} & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \begin{pmatrix} R_{b2} \\ +R_{L\ell b2} \end{pmatrix} & \begin{pmatrix} R_{b2} \\ +R_{L\ell b2} \end{pmatrix} & \cdot & \frac{-N_2}{N_1} & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \begin{pmatrix} R_{a2} \\ +R_{L\ell a2} \end{pmatrix} & \begin{pmatrix} R_{b2} \\ +R_{L\ell b2} \end{pmatrix} & R_{(11,11)} & \frac{-N_2}{N_1} & \frac{-N_2}{N_1} & \frac{-N_2}{N_1} \\
\hline
\cdot & \cdot & 1 & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \frac{-N_2}{N_1} & \cdot & \frac{-N_2}{N_1} & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & 1 & \cdot & \cdot & \cdot & \cdot & \frac{-N_2}{N_1} & \frac{-N_2}{N_1} & \cdot & \cdot & \cdot \\
\cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & \cdot & 1 & \cdot & \cdot & \frac{-N_2}{N_1} & \cdot & \cdot & \cdot
\end{array}\right]\right]$$

$$R_{(0,0)} = R_{a1} + R_{L\ell a1} + R_{LMab}$$

$$R_{(3,3)} = R_{b1} + R_{L\ell b1} + R_{LMbc}$$

$$R_{(6,6)} = \left(R_{a1} + R_{L\ell a1} + R_{LMab} + R_{b1} + R_{L\ell b1} + R_{LMbc} + R_{c1} + R_{L\ell c1} + R_{LMca}\right)$$

$$R_{(11,11)} = \left(R_{a2} + R_{L\ell a2} + R_{b2} + R_{L\ell b2} + R_{c2} + R_{L\ell c2}\right)$$

$$\mathbf{i}_{XFM}^{k+1} = \left[\begin{array}{c} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ \hdashline i_3^{k+1} \\ i_4^{k+1} \\ i_5^{k+1} \\ \hdashline i_6^{k+1} \\ i_7^{k+1} \\ i_8^{k+1} \\ \hdashline i_9^{k+1} \\ i_{10}^{k+1} \\ i_{11}^{k+1} \\ \hdashline v_{Mab}^{k+1} \\ v_{Mbc}^{k+1} \\ v_{Mca}^{k+1} \end{array}\right] \qquad \mathbf{e}_{XFM}^{k+1} = \left[\begin{array}{c} -\mathrm{hist}_{L\ell a1}^{k+1} - \mathrm{hist}_{LMab}^{k+1} \\ \mathrm{hist}_{LMab}^{k+1} \\ . \\ \hdashline -\mathrm{hist}_{L\ell b1}^{k+1} - \mathrm{hist}_{LMbc}^{k+1} \\ \mathrm{hist}_{LMbc}^{k+1} \\ . \\ \hdashline -\mathrm{hist}_{L\ell a1}^{k+1} - \mathrm{hist}_{L\ell b1}^{k+1} - \mathrm{hist}_{L\ell c1}^{k+1} \\ \mathrm{hist}_{LMca}^{k+1} \\ . \\ \hdashline -\mathrm{hist}_{L\ell a2}^{k+1} \\ -\mathrm{hist}_{L\ell b1}^{k+1} \\ -\mathrm{hist}_{L\ell a2}^{k+1} - \mathrm{hist}_{L\ell b2}^{k+1} - \mathrm{hist}_{L\ell c1}^{k+1} \\ \hdashline . \\ . \\ . \end{array}\right]$$

$$\begin{array}{c}\text{Line currents}\\\text{side 1}\end{array} \rightarrow \begin{bmatrix} i_{a1}^{k+1} \\ i_{b1}^{k+1} \\ i_{c1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} \\ i_3^{k+1} - i_{10}^{k+1} \\ -i_3^{k+1} \end{bmatrix}; \quad \begin{array}{c}\text{Line currents}\\\text{side 2}\end{array} \rightarrow \begin{bmatrix} i_{a2}^{k+1} \\ i_{b2}^{k+1} \\ i_{c2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_9^{k+1} \\ i_{10}^{k+1} - i_9^{k+1} \\ -i_{10}^{k+1} \end{bmatrix}$$

$$\begin{array}{c}\text{Phase currents}\\\text{side 1}\end{array} \rightarrow \begin{bmatrix} i_{ab1}^{k+1} \\ i_{bc1}^{k+1} \\ i_{ca1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} + i_6^{k+1} \\ i_3^{k+1} + i_6^{k+1} \\ i_6^{k+1} \end{bmatrix}; \qquad \begin{array}{c}\text{Phase currents}\\\text{side 2}\end{array} \rightarrow \begin{bmatrix} i_{ab2}^{k+1} \\ i_{bc2}^{k+1} \\ i_{ca2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_9^{k+1} + i_{11}^{k+1} \\ i_{10}^{k+1} + i_{11}^{k+1} \\ i_{11}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Magnetizing}\\ \text{currents}\end{matrix}\rightarrow\begin{bmatrix} i_{LMab}^{k+1} \\ i_{LMbc}^{k+1} \\ i_{LMca}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{0}^{k+1}-i_{1}^{k+1} \\ i_{3}^{k+1}-i_{4}^{k+1} \\ -i_{7}^{k+1} \end{bmatrix};\ \begin{matrix}\text{Core-loss}\\ \text{currents}\end{matrix}\rightarrow\begin{bmatrix} i_{Cab}^{k+1} \\ i_{Cbc}^{k+1} \\ i_{Cca}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{1}^{k+1}+i_{6}^{k+1}-i_{2}^{k+1} \\ i_{4}^{k+1}+i_{6}^{k+1}-i_{5}^{k+1} \\ i_{7}^{k+1}+i_{6}^{k+1}-i_{8}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Magnetizing}\\ \text{voltages}\end{matrix}\rightarrow\begin{bmatrix} v_{Mab}^{k+1} \\ v_{Mbc}^{k+1} \\ v_{Mca}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{LMab}^{k+1}R_{LMab}+\text{hist}_{LMab}^{k+1} \\ i_{LMbc}^{k+1}R_{LMbc}+\text{hist}_{LMbc}^{k+1} \\ i_{LMca}^{k+1}R_{LMca}+\text{hist}_{LMca}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Node voltages}\\ \text{side 1}\end{matrix}\rightarrow\begin{bmatrix} v_{ab1}^{k+1} \\ v_{bc1}^{k+1} \\ v_{ca1}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{ab1}^{k+1}\left(R_{a1}+R_{L\ell a1}\right)+\text{hist}_{L\ell a1}^{k+1}+v_{Mab}^{k+1} \\ i_{bc1}^{k+1}\left(R_{b1}+R_{L\ell b1}\right)+\text{hist}_{L\ell b1}^{k+1}+v_{Mbc}^{k+1} \\ i_{ca1}^{k+1}\left(R_{c1}+R_{L\ell c1}\right)+\text{hist}_{L\ell c1}^{k+1}+v_{Mca}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Node voltages}\\ \text{side 2}\end{matrix}\rightarrow\begin{bmatrix} v_{ab2}^{k+1} \\ v_{bc2}^{k+1} \\ v_{ca2}^{k+1} \end{bmatrix}=\begin{bmatrix} \frac{N_2}{N_1}v_{Mab}^{k+1}-i_{ab2}^{k+1}\left(R_{a2}+R_{L\ell a2}\right)-\text{hist}_{L\ell a2}^{k+1} \\ \frac{N_2}{N_1}v_{Mbc}^{k+1}-i_{bc2}^{k+1}\left(R_{b2}+R_{L\ell b2}\right)-\text{hist}_{L\ell b2}^{k+1} \\ \frac{N_2}{N_1}v_{Mca}^{k+1}-i_{ca2}^{k+1}\left(R_{c2}+R_{L\ell c2}\right)-\text{hist}_{L\ell c2}^{k+1} \end{bmatrix}$$

Transformer nomenclature:

$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\}$ = terminal voltages on side 1 (V)

$\left\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\right\}$ = terminal voltages on side 2 (V)

$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\}$ = line currents on side 1 (A)

$\left\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\right\}$ = line currents on side 2 (A)

$\left\{i_{ab1}^{k+1}, i_{bc1}^{k+1}, i_{ca1}^{k+1}\right\}$ = phase currents on side 1 (A)

$\left\{i_{ab2}^{k+1}, i_{bc2}^{k+1}, i_{ca2}^{k+1}\right\}$ = phase currents on side 2 (A)

$\left\{i_{0}^{k+1}, \cdots, i_{11}^{k+1}\right\}$ = mesh currents (A)

$\left\{\mathrm{hist}_{LMab}^{k+1}, \mathrm{hist}_{LMbc}^{k+1}, \mathrm{hist}_{LMca}^{k+1}\right\}$ = magnetizing inductance historical sources (V)

$\left\{\mathrm{hist}_{L\ell a1}^{k+1}, \mathrm{hist}_{L\ell b1}^{k+1}, \mathrm{hist}_{L\ell c1}^{k+1}\right\}$ = leakge inductance historical sources on side 1 (V)

$\left\{\mathrm{hist}_{L\ell a2}^{k+1}, \mathrm{hist}_{L\ell b2}^{k+1}, \mathrm{hist}_{L\ell c2}^{k+1}\right\}$ = leakge inductance historical sources on side 2 (V)

$N_1 / N_2 = 450/120$ = winding turns ratio

$\left\{R_{a1}, R_{a2}\right\}$ = winding resistances of phase *ab* on sides 1 and 2, respectively (Ω)

R_{Cab} = core resistance for phase *ab* (Ω)

$\left\{R_{L\ell a1}, R_{L\ell a2}\right\}$ = discretized leakage inductance resistance of side 1 and 2, respectively (Ω)

$\left\{R_{LMab}, R_{LMbc}, R_{LMca}\right\}$ = discretized magnetizing inductance resistances for phases *ab*, *bc*, and *ca*, respectively (Ω)

Over-Current and Under-Voltage Relays

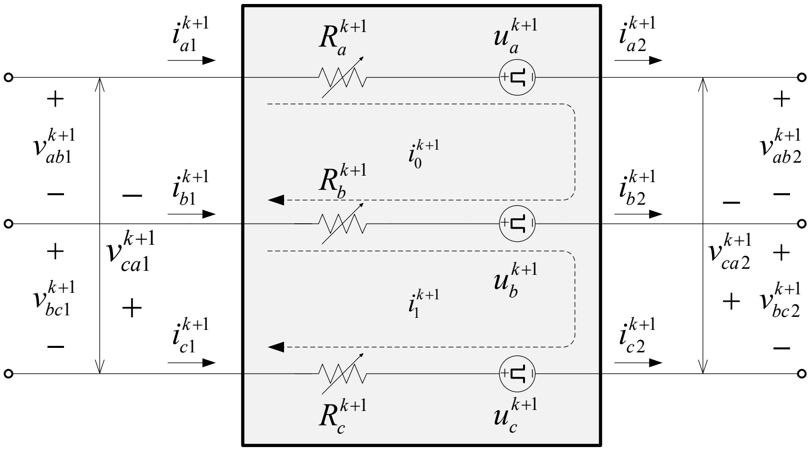


Fig. 5.3.13. Over-current relay

$$R_i^{k+1} \rightarrow \begin{cases} = 1\text{m}\Omega\text{, when the } i^{\text{th}} \text{ phase is closed or arcing} \\ = 1\text{M}\Omega\text{, when the } i^{\text{th}} \text{ phase is open} \end{cases}$$

$$\begin{bmatrix} R_a^{k+1} + R_b^{k+1} & -R_b^{k+1} \\ -R_b^{k+1} & R_b^{k+1} + R_c^{k+1} \end{bmatrix} \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \end{bmatrix} = \begin{bmatrix} -u_a^{k+1} + u_b^{k+1} \\ -u_b^{k+1} + u_c^{k+1} \end{bmatrix} \tag{A.15}$$

Since over-current and under-voltage relays do not have shunt branches between phases, the node (i.e., line-to-line) voltages are passed-in from the left-hand side's component (e.g., generator, or cable).

$$\text{Branch currents} \rightarrow \begin{bmatrix} i_{a1}^{k+1} \\ i_{b1}^{k+1} \\ i_{c1}^{k+1} \end{bmatrix} = \begin{bmatrix} i_{a2}^{k+1} \\ i_{b2}^{k+1} \\ i_{c2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} - i_0^{k+1} \\ -i_1^{k+1} \end{bmatrix}$$

$$\begin{array}{c}\text{Arcing}\\ \text{sources}\end{array} \rightarrow \begin{cases} u_a^{k+1} = V_{arc}\text{sign}\left(i_{a1}^k\right) \\ u_b^{k+1} = V_{arc}\text{sign}\left(i_{b1}^k\right); \quad \text{V}_{arc} \rightarrow \begin{cases} = 10\text{V, when arcing} \\ = 0\text{V, otherwise} \end{cases} \\ u_c^{k+1} = V_{arc}\text{sign}\left(i_{c1}^k\right) \end{cases}$$

Overcurrent/undervoltage relay nomenclature:

$$\begin{aligned}
\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\} &= \text{terminal voltages on side 1 } (\text{V}) \\
\left\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\right\} &= \text{terminal voltages on side 2 } (\text{V}) \\
\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\} &= \text{line currents on side 1 } (\text{A}) \\
\left\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\right\} &= \text{line currents on side 2 } (\text{A}) \\
\left\{i_0^{k+1}, i_1^{k+1}\right\} &= \text{mesh currents } (\text{A}) \\
\left\{u_a^{k+1}, u_b^{k+1}, u_c^{k+1}\right\} &= \text{arcing voltages } (\text{V}) \\
R_i^{k+1} &= \text{time-varying breaker resistance} \\
&\quad \text{of the } i^{\text{th}} \text{ phase } (\Omega) \\
V_{arc} &= \text{arcing voltage magnitude (=10V)}
\end{aligned}$$

Bus Transfer

The bus transfer model (automatic and manual) is shown on the next page.

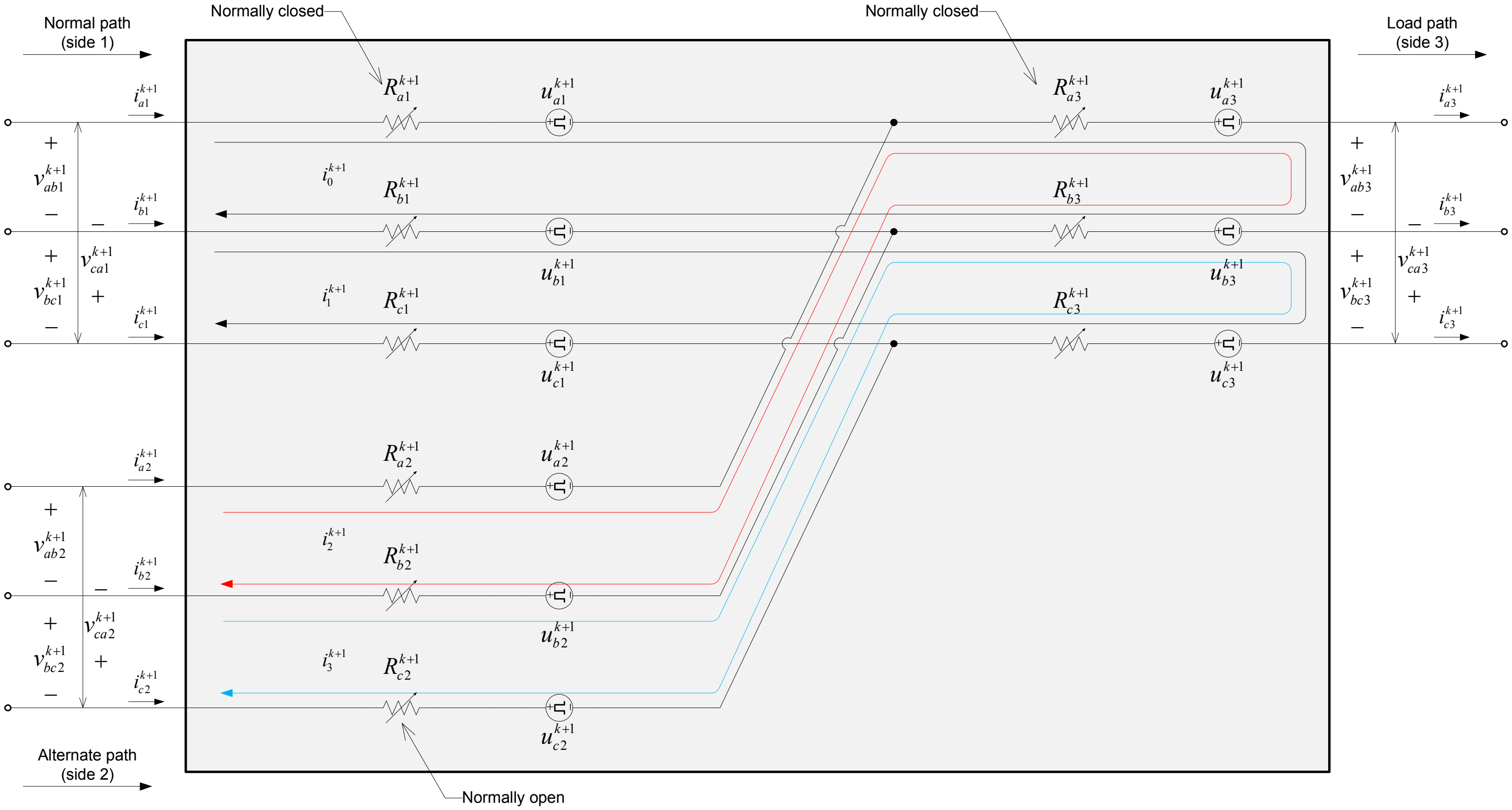


Fig. 5.3.14. Bus transfer model

The center-point (non-physical) shunt resistances of $1\text{M}\Omega$ each were added for the following reasons: to compute XBT terminal voltages easily, to avoid >1 output loop current per phase on the load side, and to be able to model XBTs with the load side open-circuited (i.e., removing the last two rows and columns of $\mathbf{R}_{XBT}^{k+1}$ makes $i_5^{k+1} = i_6^{k+1} = 0$). The peak leakage currents through R_{xab} and R_{xbc} are $450\sqrt{2}/10^6 = 636\times 10^{-6}\,\text{A}$, which are negligible.

$$\mathbf{R}_{XBT}^{k+1}\mathbf{i}_{XBT}^{k+1} = \mathbf{e}_{XBT}^{k+1} \tag{A.16}$$

$$\mathbf{R}_{XBT}^{k+1} = \left[\begin{array}{cc|cc|cc}
R_{(0,0)} & -R_{b1}^{k+1} & R_{xab} & \cdot & -R_{xab} & \cdot \\
-R_{b1}^{k+1} & R_{(1,1)} & \cdot & R_{xbc} & \cdot & -R_{xbc} \\
\hline
R_{xab} & \cdot & R_{(2,2)} & -R_{b2}^{k+1} & -R_{xab} & \cdot \\
\cdot & R_{xbc} & -R_{b2}^{k+1} & R_{(3,3)} & \cdot & -R_{xbc} \\
\hline
-R_{xab} & \cdot & -R_{xab} & \cdot & R_{(4,4)} & -R_{b3}^{k+1} \\
\cdot & -R_{xbc} & \cdot & -R_{xbc} & -R_{b3}^{k+1} & R_{(5,5)}
\end{array}\right]$$

$$\begin{aligned}
R_{(0,0)} &= \left(R_{a1}^{k+1} + R_{b1}^{k+1} + R_{xab}\right) \\
R_{(1,1)} &= \left(R_{b1}^{k+1} + R_{c1}^{k+1} + R_{xbc}\right) \\
R_{(2,2)} &= \left(R_{a2}^{k+1} + R_{b1}^{k+1} + R_{xab}\right) \\
R_{(3,3)} &= \left(R_{b2}^{k+1} + R_{c2}^{k+1} + R_{xbc}\right) \\
R_{(4,4)} &= \left(R_{a3}^{k+1} + R_{b3}^{k+1} + R_{xab}\right) \\
R_{(5,5)} &= \left(R_{b3}^{k+1} + R_{c3}^{k+1} + R_{xbc}\right)
\end{aligned}$$

$$\mathbf{i}_{XBT}^{k+1}=\begin{bmatrix} i_0^{k+1} \\ i_1^{k+1} \\ i_2^{k+1} \\ i_3^{k+1} \\ i_4^{k+1} \\ i_5^{k+1} \end{bmatrix}; \qquad \mathbf{e}_{XBT}^{k+1}=\begin{bmatrix} -u_{a1}^{k+1}+u_{b1}^{k+1} \\ -u_{b1}^{k+1}+u_{c1}^{k+1} \\ -u_{a2}^{k+1}+u_{b2}^{k+1} \\ -u_{b2}^{k+1}+u_{c2}^{k+1} \\ -u_{a3}^{k+1}+u_{b3}^{k+1} \\ -u_{b3}^{k+1}+u_{c3}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Branch} \\ \text{currents}\end{matrix} \rightarrow \begin{bmatrix} i_{a1}^{k+1} \\ i_{b1}^{k+1} \\ i_{c1}^{k+1} \end{bmatrix}=\begin{bmatrix} i_0^{k+1} \\ i_1^{k+1}-i_0^{k+1} \\ -i_1^{k+1} \end{bmatrix}; \quad \begin{bmatrix} i_{a2}^{k+1} \\ i_{b2}^{k+1} \\ i_{c2}^{k+1} \end{bmatrix}=\begin{bmatrix} i_2^{k+1} \\ i_3^{k+1}-i_2^{k+1} \\ -i_3^{k+1} \end{bmatrix}; \quad \begin{bmatrix} i_{a3}^{k+1} \\ i_{b3}^{k+1} \\ i_{c3}^{k+1} \end{bmatrix}=\begin{bmatrix} i_5^{k+1} \\ i_6^{k+1}-i_5^{k+1} \\ -i_6^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Center-point} \\ \text{currents}\end{matrix} \rightarrow \begin{bmatrix} i_{xab}^{k+1} \\ i_{xbc}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{a1}^{k+1}+i_{a2}^{k+1}-i_{a3}^{k+1} \\ i_{b1}^{k+1}+i_{b2}^{k+1}-i_{b3}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Center-point} \\ \text{voltages}\end{matrix} \rightarrow \begin{bmatrix} v_{xab}^{k+1} \\ v_{xbc}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{xab}^{k+1}R_{xab} \\ i_{xbc}^{k+1}R_{xbc} \end{bmatrix}$$

$$\begin{matrix}\text{Node voltages} \\ \text{side 1}\end{matrix} \rightarrow \begin{bmatrix} v_{ab1}^{k+1} \\ v_{bc1}^{k+1} \\ v_{ca1}^{k+1} \end{bmatrix}=\begin{bmatrix} i_{a1}^{k+1}R_{a1}^{k+1}+u_{a1}^{k+1}+v_{xab}^{k+1}-u_{b1}^{k+1}-i_{b1}^{k+1}R_{b1}^{k+1} \\ i_{b1}^{k+1}R_{b1}^{k+1}+u_{b1}^{k+1}+v_{xbc}^{k+1}-u_{c1}^{k+1}-i_{c1}^{k+1}R_{c1}^{k+1} \\ -v_{ab1}^{k+1}-v_{bc1}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Node voltages}\\ \text{side 2}\end{matrix} \rightarrow \begin{bmatrix} v_{ab2}^{k+1} \\ v_{bc2}^{k+1} \\ v_{ca2}^{k+1} \end{bmatrix} = \begin{bmatrix} i_{a2}^{k+1}R_{a2}^{k+1} + u_{a2}^{k+1} + v_{xab}^{k+1} - u_{b2}^{k+1} - i_{b2}^{k+1}R_{b2}^{k+1} \\ i_{b2}^{k+1}R_{b2}^{k+1} + u_{b2}^{k+1} + v_{xbc}^{k+1} - u_{c2}^{k+1} - i_{c2}^{k+1}R_{c2}^{k+1} \\ -v_{ab2}^{k+1} - v_{bc2}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Node voltages}\\ \text{side 3}\end{matrix} \rightarrow \begin{bmatrix} v_{ab3}^{k+1} \\ v_{bc3}^{k+1} \\ v_{ca3}^{k+1} \end{bmatrix} = \begin{bmatrix} -u_{a3}^{k+1} - i_{a3}^{k+1}R_{a3}^{k+1} + v_{xab}^{k+1} + i_{b3}^{k+1}R_{b3}^{k+1} + u_{b3}^{k+1} \\ -u_{b3}^{k+1} - i_{b3}^{k+1}R_{b3}^{k+1} + v_{xbc}^{k+1} + i_{c3}^{k+1}R_{c3}^{k+1} + u_{c3}^{k+1} \\ -v_{ab3}^{k+1} - v_{bc3}^{k+1} \end{bmatrix}$$

$$\begin{matrix}\text{Arcing sources}\\ \text{on normal path}\end{matrix} \rightarrow \begin{cases} u_{a1}^{k+1} = V_{arc}\text{sign}\left(i_{a1}^{k}\right) \\ u_{b1}^{k+1} = V_{arc}\text{sign}\left(i_{b1}^{k}\right); \\ u_{c1}^{k+1} = V_{arc}\text{sign}\left(i_{c1}^{k}\right) \end{cases} \qquad \text{V}_{arc} \rightarrow \begin{cases} = 10\text{V, when arcing} \\ = 0\text{V, otherwise} \end{cases}$$

$$\begin{matrix}\text{Arcing sources}\\ \text{on alternate path}\end{matrix} \rightarrow \begin{cases} u_{a2}^{k+1} = V_{arc}\text{sign}\left(i_{a2}^{k}\right) \\ u_{b2}^{k+1} = V_{arc}\text{sign}\left(i_{b2}^{k}\right); \\ u_{c2}^{k+1} = V_{arc}\text{sign}\left(i_{c2}^{k}\right) \end{cases} \qquad \text{V}_{arc} \rightarrow \begin{cases} = 10\text{V, when arcing} \\ = 0\text{V, otherwise} \end{cases}$$

$$\begin{matrix}\text{Arcing sources}\\ \text{on load path}\end{matrix} \rightarrow \begin{cases} u_{a3}^{k+1} = V_{arc}\text{sign}\left(i_{a3}^{k}\right) \\ u_{b3}^{k+1} = V_{arc}\text{sign}\left(i_{b3}^{k}\right); \\ u_{c3}^{k+1} = V_{arc}\text{sign}\left(i_{c3}^{k}\right) \end{cases} \qquad \text{V}_{arc} \rightarrow \begin{cases} = 10\text{V, when arcing} \\ = 0\text{V, otherwise} \end{cases}$$

Bus transfer nomenclature:

$\left\{v_{ab1}^{k+1}, v_{bc1}^{k+1}, v_{ca1}^{k+1}\right\}$ = terminal voltages on side 1 (normal path) (V)

$\left\{v_{ab2}^{k+1}, v_{bc2}^{k+1}, v_{ca2}^{k+1}\right\}$ = terminal voltages on side 2 (alternate path) (V)

$\left\{v_{ab3}^{k+1}, v_{bc3}^{k+1}, v_{ca3}^{k+1}\right\}$ = terminal voltages on side 3 (load path) (V)

$\left\{i_{a1}^{k+1}, i_{b1}^{k+1}, i_{c1}^{k+1}\right\}$ = normal path line currents (A)

$\left\{i_{a2}^{k+1}, i_{b2}^{k+1}, i_{c2}^{k+1}\right\}$ = alternate path line currents (A)

$\left\{i_{a3}^{k+1}, i_{b3}^{k+1}, i_{c3}^{k+1}\right\}$ = load path line currents (A)

$\left\{i_{0}^{k+1}, i_{1}^{k+1}, i_{2}^{k+1}, i_{3}^{k+1}, i_{4}^{k+1}, i_{5}^{k+1}\right\}$ = mesh currents (A)

$\left\{u_{a1}^{k+1}, u_{b1}^{k+1}, u_{c1}^{k+1}\right\}$ = normal path arcing sources (V)

$\left\{u_{a2}^{k+1}, u_{b2}^{k+1}, u_{c2}^{k+1}\right\}$ = alternate path arcing sources (V)

$\left\{u_{a3}^{k+1}, u_{b3}^{k+1}, u_{c3}^{k+1}\right\}$ = load path arcing sources (V)

$\left\{R_{a1}^{k+1}, R_{b1}^{k+1}, R_{c1}^{k+1}\right\}$ = normal path contact resistance (Ω)

$\left\{R_{a2}^{k+1}, R_{b2}^{k+1}, R_{c2}^{k+1}\right\}$ = alternate path contact resistance (Ω)

$\left\{R_{a3}^{k+1}, R_{b3}^{k+1}, R_{c3}^{k+1}\right\}$ = load path contact resistance (Ω)

V_{arc} = arcing voltage magnitude (=10V)

APPENDIX B

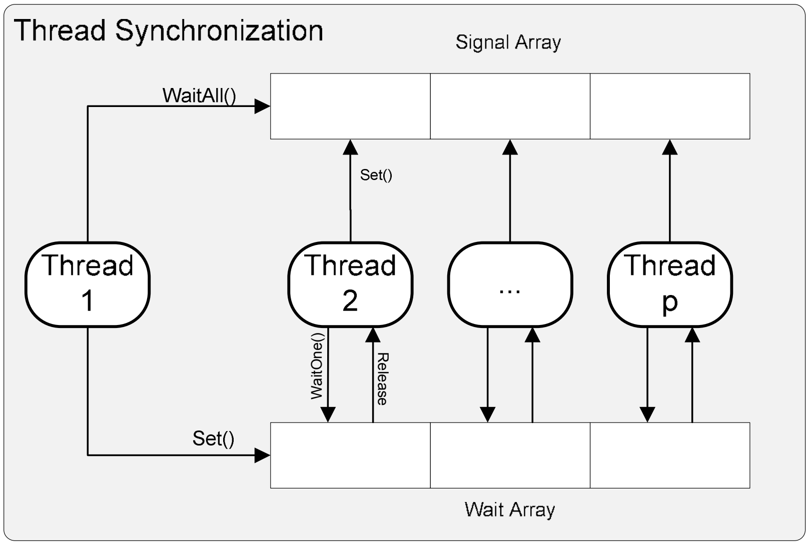
THREAD SYNCHRONIZATION

B. Thread Synchronization

The thread synchronization constructs in this work are based two-way signaling, which use auto-reset and wait-handle arrays (`AutoResetEvent[]` in C#). When solving *p* subsystems, *p* threads were invoked from the Windows thread pool. The first thread (thread 1) is designated the *master* thread. Thread 1 has two roles: as a master, and as a slave. When acting as a master thread, thread 1 is signals slave threads 2-*p* that they may continue working after being in the wait state. As a slave thread, thread 1 is responsible of solving subsystem 1. A high-level illustration of the thread synchronization scheme is shown in Fig. 5.3.15.

Two `AutoResetEvent[]` arrays are used: a signal array and a wait array. The signal array is used by the slave threads to signal the master thread of their readiness or work completion. The wait array is used so that the master thread can tell slaves 2-*p* to continue working (i.e., leave their wait states). The signal array works as follows. The master thread waits on this signal array by calling the `WaitHandle.WaitAll()` method. When all slave threads fully signal the signal array, the master thread can do work alone while slaves 2-*p* wait (i.e., serial work, or steps 2 and 7 in Fig. 3.4.3).

The wait array is used so that slave threads can wait for the master to finish the serial work. When the master finishes the serial work, the master calls the `Set()` method on the wait array and threads 2-*p* are released and can continue their work. The atomic operation in C# for said signaling and waiting is the `WaitHandle.SignalAndWait()` method.



1. All threads work concurrently
2. As slave threads finish, signal is signaled by each thread
3. After signal array is fully signaled, each slave waits on the wait array
4. When thread 1 finishes its serial work and notices the wait array fully signaled, thread 1 releases slave threads waiting on wait array
5. Goto 1

Fig. 5.3.15. Thread synchronization arrays and logic

The threads were assigned to each core using the following code snippet, where `processorNumber` is the integer that selects the core number.

```
foreach (ProcessThread thread in Process.GetCurrentProcess().Threads
      if (thread.Id == GetCurrentThreadId())
            thread.ProcessorAffinity = (IntPtr)processorNumber;
```

The thread priority was left at its default value of *Normal.* As the SPS simulations took place, other Windows background processes ran as well. The PCs booted normally into Window normally when running the simulations.

APPENDIX C

COMPONENT DISTRIBUTION

C. Component Distribution

```
<Partitions><Partition1of1
MTCs="ABT1,ABT2,ABT3,ABT4,ABT5,ABT6,ABT7,ABT8,ABT9,ABT10,ABT11,ABT12,AB
T13,ABT14,ABT15,BRK1,BRK1_1,BRK1_2,BRK1_3,BRK1_4,BRK1_5,BRK1_6,BRK1_7,B
RK1_8,BRK1_9,BRK1_10,BRK1_11,BRK1_12,BRK1_13,BRK1_14,BRK1_15,BRK1_16,BR
K2,BRK2_1,BRK2_2,BRK2_3,BRK2_4,BRK2_5,BRK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_
10,BRK2_11,BRK2_12,BRK2_13,BRK2_14,BRK2_15,BRK2_16,BRK2_17,BRK2_18,BRK2
_19,BRK3,BRK3_1,BRK3_2,BRK3_3,BRK3_4,BRK3_5,BRK3_6,BRK3_7,BRK3_8,BRK3_9
,BRK3_10,BRK3_11,BRK3_12,BRK3_13,BRK3_14,BRK3_15,BRK3_16,BRK11_1,BRK11_
2,BRK11_3,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK12_1,BRK12_2,BRK12_4,BRK12
_5,BRK13_3,BRK21_1,BRK21_2,BRK21_3,BRK21_4,BRK21_5,BRK22_1,BRK22_2,BRK2
2_3,BRK22_4,BRK22_5,BRK22_6,BRK22_7,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK
31_5,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,Cbl6,Cbl7,Cbl8,Cbl9,Cbl10,Cbl11,Cbl12,Cbl
13,Cbl14,Cbl15,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl22,Cbl23,Cbl24,Cb
l25,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,Cbl31,Cbl32,Cbl33,CBL1,CBL2,CBL3,CBL4
,CBL5,CBL6,CBL7,CBL8,CBL9,CBL10,CBL11,CBL12,CBL13,CBL14,CBL15,CBL16,CBL
17,CBL18,CBL19,CBL20,CBL21,CBL22,CBL23,CBL24,CBL25,CBL26,CBL27,CBL28,CB
L29,CBL30,CBL31,CBL32,CBL33,CBL34,CBL35,CBL36,CBL37,CBL38,CBL39,CBL40,C
BL41,CBL44,CBL45,CBL46,CBL47,CBL48,CBL49,CBL50,CBL51,CBL52,CBL53,CBL54,
CBL55,CBL56,CBL57,CBL58,CBL59,CBL60,CBL61,CBL62,CBL63,CBL64,CBL65,CBL66
,CBL67,CBL68,CBL69,CBL70,CBL71,CBL72,CBL73,CBL74,CBL75,CBL76,CBL77,CBL7
8,CBL79,CBL80,CBL81,CBL82,CBL83,CBL84,CBL85,CBL86,CBL87,CBL88,CBL89,CBL
90,CBL91,CBL92,CBL93,CBL94,CBL95,CBL96,CBL97,CBL98,CBL99,CBL100,CBL101,
CBL102,CBL103,CBL104,CBL105,CBL106,CBL107,CBL108,CBL109,CBL110,FLT1,FLT
2,FLT3,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,GEN1,GEN2,GEN3,Lod1,Lod2,Lod3,Lod4
,Lod5,Lod6,Lod7,Lod8,Lod9,Lod10,Lod11,Lod12,Lod13,Lod14,Lod15,Lod16,Lod
17,Lod18,Lod19,Lod20,Lod21,Lod22,Lod23,Lod24,Lod25,Lod26,Lod27,Lod28,Lo
d29,Lod30,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,LOD4,LOD5,LOD6,LOD7,LOD8,LOD
9,LOD10,LOD11,LOD12,LOD13,LVP1,LVP2,LVP3,LVP4,LVP5,LVP6,LVP7,LVP8,LVP9,
LVP10,LVP11,LVP12,LVP13,LVP14,LVP15,LVP16,LVP17,LVR1,LVR2,MBT1,MBT2,MBT
3,MBT4,MBT5,MBT6,MBT7,MBT8,MBT9,MBT10,MBT11,MBT12,MBT13,MOT_AcCpr2,MOT_
AcCpr4,MOT_ACcpr1,MOT_ACcpr3,MOT_Anchor,MOT_Fpmp1,MOT_Fpmp2,MOT_Fpmp3,M
OT_Fpmp4,MOT_Fpmp5,MOT_Fpmp6,MOT_Hpcpr2,MOT_HPcpr1,MOT_Steer1,MOT_Steer
2,MOT_WPmp1,MOT_WPmp2,MOT_WPmp3,MOT_WPmp4,XFM1,XFM2,XFM3,XFM4,XFM5,XFM6
,XFM7,XFM8,XFM9,XFM10,XFM11" />
```

```
<Partition1of2
MTCs="ABT2,ABT3,ABT4,ABT5,ABT6,ABT7,ABT8,ABT9,ABT10,ABT12,BRK1,BRK1_1,B
RK1_2,BRK1_3,BRK1_4,BRK1_5,BRK1_6,BRK1_7,BRK1_8,BRK1_9,BRK1_10,BRK1_11,
BRK1_12,BRK1_13,BRK1_14,BRK1_15,BRK1_16,BRK2,BRK2_1,BRK2_2,BRK2_3,BRK2_
4,BRK2_5,BRK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_10,BRK2_11,BRK2_12,BRK2_14,BR
K2_15,BRK2_16,BRK2_17,BRK2_18,BRK3_4,BRK3_5,BRK3_6,BRK3_16,BRK11_3,BRK1
2_1,BRK12_2,BRK12_4,BRK12_5,BRK13_3,Cbl7,Cbl8,Cbl9,Cbl10,Cbl11,Cbl12,Cb
```

```
l13,Cbl14,Cbl15,Cbl22,Cbl23,Cbl24,CBL1,CBL2,CBL4,CBL6,CBL22,CBL29,CBL30
,CBL31,CBL32,CBL33,CBL34,CBL35,CBL36,CBL37,CBL38,CBL39,CBL40,CBL41,CBL4
4,CBL45,CBL46,CBL47,CBL48,CBL49,CBL50,CBL51,CBL52,CBL53,CBL54,CBL56,CBL
57,CBL58,CBL59,CBL60,CBL62,CBL63,CBL64,CBL65,CBL67,CBL74,CBL75,CBL76,CB
L77,CBL78,CBL79,CBL80,CBL81,CBL82,CBL83,CBL84,CBL85,CBL86,CBL88,CBL89,C
BL101,CBL102,CBL103,CBL107,FLT3,GEN1,GEN2,Lod7,Lod8,Lod9,Lod10,Lod11,Lo
d12,Lod13,Lod14,Lod15,Lod22,Lod23,Lod24,LOD4,LOD5,LOD6,LOD7,LOD8,LOD9,L
OD10,LOD13,LVP4,LVP5,LVP6,LVP7,LVP8,LVP9,LVP10,LVP11,LVP12,LVR1,MBT1,MB
T5,MBT6,MBT7,MBT8,MBT9,MBT10,MOT_AcCpr2,MOT_ACcpr1,MOT_Fpmp2,MOT_Fpmp3,
MOT_Fpmp4,MOT_Fpmp5,MOT_HPcpr1,MOT_Steer2,MOT_WPmp1,MOT_WPmp2,XFM3,XFM4
,XFM5,XFM8" />

<Partition2of2
MTCs="ABT1,ABT11,ABT13,ABT14,ABT15,BRK2_13,BRK2_19,BRK3,BRK3_1,BRK3_2,B
RK3_3,BRK3_7,BRK3_8,BRK3_9,BRK3_10,BRK3_11,BRK3_12,BRK3_13,BRK3_14,BRK3
_15,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK21_1,BRK21_2,BRK
21_3,BRK21_4,BRK21_5,BRK22_1,BRK22_2,BRK22_3,BRK22_4,BRK22_5,BRK22_6,BR
K22_7,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_5,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,
Cbl6,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl25,Cbl26,Cbl27,Cbl28,Cbl29,
Cbl30,Cbl31,Cbl32,Cbl33,CBL3,CBL5,CBL7,CBL8,CBL9,CBL10,CBL11,CBL12,CBL1
3,CBL14,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL23,CBL24,CBL25,CBL
26,CBL27,CBL28,CBL55,CBL61,CBL66,CBL68,CBL69,CBL70,CBL71,CBL72,CBL73,CB
L87,CBL90,CBL91,CBL92,CBL93,CBL94,CBL95,CBL96,CBL97,CBL98,CBL99,CBL100,
CBL104,CBL105,CBL106,CBL108,CBL109,CBL110,FLT1,FLT2,FLT4,FLT5,FLT6,FLT7
,FLT8,FLT9,GEN3,Lod1,Lod2,Lod3,Lod4,Lod5,Lod6,Lod16,Lod17,Lod18,Lod19,L
od20,Lod21,Lod25,Lod26,Lod27,Lod28,Lod29,Lod30,Lod31,Lod32,Lod33,LOD1,L
OD2,LOD3,LOD11,LOD12,LVP1,LVP2,LVP3,LVP13,LVP14,LVP15,LVP16,LVP17,LVR2,
MBT2,MBT3,MBT4,MBT11,MBT12,MBT13,MOT_AcCpr4,MOT_ACcpr3,MOT_Anchor,MOT_F
pmp1,MOT_Fpmp6,MOT_Hpcpr2,MOT_Steer1,MOT_WPmp3,MOT_WPmp4,XFM1,XFM2,XFM6
,XFM7,XFM9,XFM10,XFM11" />
```

```
<Partition1of3
MTCs="ABT11,ABT12,ABT14,BRK1_11,BRK2_7,BRK3_12,BRK3_13,BRK11_1,BRK11_2,
BRK11_3,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK12_1,BRK12_2,BRK13_3,BRK21_1
,BRK21_2,BRK21_3,BRK21_4,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_
5,Cbl4,Cbl5,Cbl6,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl22,Cbl23,Cbl24,
Cbl31,Cbl32,Cbl33,CBL13,CBL14,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21
,CBL22,CBL55,CBL64,CBL66,CBL67,CBL68,CBL69,CBL70,CBL71,CBL72,CBL73,CBL7
6,CBL77,CBL78,CBL81,CBL87,CBL90,CBL91,CBL92,CBL93,CBL104,CBL105,CBL106,
CBL107,FLT1,FLT2,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,Lod4,Lod5,Lod6,Lod16,Lod
17,Lod18,Lod19,Lod20,Lod21,Lod22,Lod23,Lod24,Lod31,Lod32,Lod33,LOD1,LOD
2,LOD3,LOD4,LOD11,LOD12,LOD13,LVP13,LVP17,MBT1,MBT3,MBT4,MBT5,MBT11,MOT
_Anchor,MOT_Fpmp1,XFM2,XFM6,XFM7,XFM8,XFM11" />

<Partition2of3
MTCs="ABT4,ABT5,ABT6,ABT7,ABT8,ABT9,ABT10,BRK1,BRK1_1,BRK1_2,BRK1_4,BRK
1_5,BRK1_6,BRK1_7,BRK1_8,BRK1_9,BRK1_10,BRK1_12,BRK1_13,BRK1_14,BRK1_15
,BRK1_16,BRK2,BRK2_1,BRK2_2,BRK2_3,BRK2_4,BRK2_5,BRK2_6,BRK2_9,BRK2_10,
BRK2_11,BRK2_12,BRK2_14,BRK2_15,BRK2_16,BRK2_17,BRK12_5,Cbl10,Cbl11,Cbl
12,Cbl13,Cbl14,Cbl15,CBL1,CBL2,CBL6,CBL35,CBL37,CBL38,CBL39,CBL40,CBL41
,CBL44,CBL45,CBL46,CBL47,CBL48,CBL49,CBL50,CBL51,CBL52,CBL53,CBL56,CBL5
7,CBL58,CBL59,CBL60,CBL62,CBL63,CBL74,CBL75,CBL80,CBL82,CBL83,CBL84,CBL
85,CBL86,CBL88,CBL89,CBL101,CBL102,CBL103,FLT3,GEN1,GEN2,Lod10,Lod11,Lo
```

```
d12,Lod13,Lod14,Lod15,LOD7,LOD8,LOD9,LOD10,LVP4,LVP5,LVP6,LVP7,LVP8,LVP
9,LVP10,LVP11,LVP12,MBT7,MBT8,MBT9,MBT10,MOT_AcCpr2,MOT_ACcpr1,MOT_Fpmp
2,MOT_Fpmp3,MOT_Fpmp4,MOT_Fpmp5,MOT_HPcpr1,MOT_WPmp1,MOT_WPmp2,XFM4,XFM
5" />

<Partition3of3
MTCs="ABT1,ABT2,ABT3,ABT13,ABT15,BRK1_3,BRK2_8,BRK2_13,BRK2_18,BRK2_19,
BRK3,BRK3_1,BRK3_2,BRK3_3,BRK3_4,BRK3_5,BRK3_6,BRK3_7,BRK3_8,BRK3_9,BRK
3_10,BRK3_11,BRK3_14,BRK3_15,BRK3_16,BRK12_4,BRK22_1,BRK22_2,BRK22_3,BR
K22_4,BRK22_5,BRK22_6,BRK22_7,Cbl1,Cbl2,Cbl3,Cbl7,Cbl8,Cbl9,Cbl25,Cbl26
,Cbl27,Cbl28,Cbl29,Cbl30,CBL3,CBL4,CBL5,CBL7,CBL8,CBL9,CBL10,CBL11,CBL1
2,CBL23,CBL24,CBL25,CBL26,CBL27,CBL28,CBL29,CBL30,CBL31,CBL32,CBL33,CBL
34,CBL36,CBL54,CBL61,CBL65,CBL79,CBL94,CBL95,CBL96,CBL97,CBL98,CBL99,CB
L100,CBL108,CBL109,CBL110,GEN3,Lod1,Lod2,Lod3,Lod7,Lod8,Lod9,Lod25,Lod2
6,Lod27,Lod28,Lod29,Lod30,LOD5,LOD6,LVP1,LVP2,LVP3,LVP14,LVP15,LVP16,LV
R1,LVR2,MBT2,MBT6,MBT12,MBT13,MOT_AcCpr4,MOT_ACcpr3,MOT_Fpmp6,MOT_Hpcpr
2,MOT_Steer1,MOT_Steer2,MOT_WPmp3,MOT_WPmp4,XFM1,XFM3,XFM9,XFM10" />
```

```
<Partition1of4
MTCs="ABT3,ABT4,ABT5,ABT10,ABT12,BRK1_5,BRK1_6,BRK1_11,BRK1_12,BRK2_5,B
RK2_11,BRK2_14,BRK2_15,BRK2_16,BRK2_18,BRK3_5,BRK3_6,BRK11_3,BRK12_1,BR
K12_2,BRK12_4,BRK12_5,BRK13_3,Cbl7,Cbl8,Cbl9,Cbl13,Cbl14,Cbl15,Cbl22,Cb
l23,Cbl24,CBL22,CBL31,CBL32,CBL33,CBL34,CBL39,CBL41,CBL44,CBL45,CBL47,C
BL51,CBL54,CBL57,CBL62,CBL63,CBL64,CBL65,CBL67,CBL76,CBL77,CBL78,CBL79,
CBL80,CBL81,CBL82,CBL102,CBL103,CBL107,Lod7,Lod8,Lod9,Lod13,Lod14,Lod15
,Lod22,Lod23,Lod24,LOD4,LOD5,LOD6,LOD10,LOD13,LVP6,LVP7,LVP8,LVP10,MBT1
,MBT5,MBT6,MBT9,MOT_Fpmp2,MOT_Fpmp3,MOT_WPmp1,MOT_WPmp2,XFM3,XFM5,XFM8"
/>

<Partition2of4
MTCs="ABT2,ABT6,ABT7,ABT8,ABT9,BRK1,BRK1_1,BRK1_2,BRK1_3,BRK1_4,BRK1_7,
BRK1_8,BRK1_9,BRK1_10,BRK1_13,BRK1_14,BRK1_15,BRK1_16,BRK2,BRK2_1,BRK2_
2,BRK2_3,BRK2_4,BRK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_10,BRK2_12,BRK2_17,BRK
3_4,BRK3_16,Cbl10,Cbl11,Cbl12,CBL1,CBL2,CBL4,CBL6,CBL29,CBL30,CBL35,CBL
36,CBL37,CBL38,CBL40,CBL46,CBL48,CBL49,CBL50,CBL52,CBL53,CBL56,CBL58,CB
L59,CBL60,CBL74,CBL75,CBL83,CBL84,CBL85,CBL86,CBL88,CBL89,CBL101,FLT3,G
EN1,GEN2,Lod10,Lod11,Lod12,LOD7,LOD8,LOD9,LVP4,LVP5,LVP9,LVP11,LVP12,LV
R1,MBT7,MBT8,MBT10,MOT_AcCpr2,MOT_ACcpr1,MOT_Fpmp4,MOT_Fpmp5,MOT_HPcpr1
,MOT_Steer2,XFM4" />

<Partition3of4
MTCs="ABT1,ABT13,ABT15,BRK2_13,BRK2_19,BRK3,BRK3_1,BRK3_2,BRK3_3,BRK3_7
,BRK3_8,BRK3_9,BRK3_10,BRK3_11,BRK3_12,BRK3_13,BRK3_14,BRK3_15,BRK22_1,
BRK22_2,BRK22_3,BRK22_4,BRK22_5,BRK22_6,BRK22_7,Cbl1,Cbl2,Cbl3,Cbl25,Cb
l26,Cbl27,Cbl28,Cbl29,Cbl30,CBL3,CBL5,CBL7,CBL8,CBL9,CBL10,CBL11,CBL12,
CBL13,CBL23,CBL24,CBL25,CBL26,CBL27,CBL28,CBL61,CBL94,CBL95,CBL96,CBL97
,CBL98,CBL99,CBL100,CBL108,CBL109,CBL110,GEN3,Lod1,Lod2,Lod3,Lod25,Lod2
6,Lod27,Lod28,Lod29,Lod30,LVP1,LVP2,LVP3,LVP14,LVP15,LVP16,LVR2,MBT2,MB
T12,MBT13,MOT_AcCpr4,MOT_ACcpr3,MOT_Fpmp6,MOT_Hpcpr2,MOT_Steer1,MOT_WPm
p3,MOT_WPmp4,XFM1,XFM9,XFM10" />

<Partition4of4
MTCs="ABT11,ABT14,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK21
_1,BRK21_2,BRK21_3,BRK21_4,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK3
```

```
1_5,Cbl4,Cbl5,Cbl6,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,Cbl31,Cbl32,Cbl3
3,CBL14,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL55,CBL66,CBL68,CBL
69,CBL70,CBL71,CBL72,CBL73,CBL87,CBL90,CBL91,CBL92,CBL93,CBL104,CBL105,
CBL106,FLT1,FLT2,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,Lod4,Lod5,Lod6,Lod16,Lod
17,Lod18,Lod19,Lod20,Lod21,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,LOD11,LOD12
,LVP13,LVP17,MBT3,MBT4,MBT11,MOT_Anchor,MOT_Fpmp1,XFM2,XFM6,XFM7,XFM11"
/>
```

```
<Partition1of5
MTCs="ABT12,ABT14,BRK1_11,BRK2_11,BRK3_11,BRK3_12,BRK3_15,BRK11_3,BRK12
_1,BRK12_2,BRK12_4,BRK12_5,BRK13_3,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK3
1_4,BRK31_5,Cbl7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,Cbl31,Cbl32,Cbl33,CBL11,CB
L15,CBL16,CBL17,CBL19,CBL20,CBL22,CBL23,CBL51,CBL64,CBL67,CBL76,CBL77,C
BL78,CBL79,CBL80,CBL81,CBL87,CBL102,CBL106,CBL107,Lod7,Lod8,Lod9,Lod22,
Lod23,Lod24,Lod31,Lod32,Lod33,LOD1,LOD2,LOD4,LOD10,LOD13,LVP3,MBT1,MBT5
,MBT9,MOT_Hpcpr2,XFM3,XFM8,XFM11" />

<Partition2of5
MTCs="ABT11,BRK1_9,BRK2_7,BRK3_13,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11
_6,BRK11_7,BRK21_1,BRK21_2,BRK21_3,BRK21_4,Cbl4,Cbl5,Cbl6,Cbl16,Cbl17,C
bl18,Cbl19,Cbl20,Cbl21,CBL13,CBL14,CBL18,CBL21,CBL55,CBL66,CBL68,CBL69,
CBL70,CBL71,CBL72,CBL73,CBL90,CBL91,CBL92,CBL93,CBL104,CBL105,FLT1,FLT2
,FLT3,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,Lod4,Lod5,Lod6,Lod16,Lod17,Lod18,Lo
d19,Lod20,Lod21,LOD3,LOD11,LOD12,LVP13,LVP17,MBT3,MBT4,MBT11,MOT_Anchor
,MOT_Fpmp1,XFM2,XFM6,XFM7" />

<Partition3of5
MTCs="ABT1,ABT13,ABT15,BRK3_2,BRK3_3,BRK3_7,BRK3_9,BRK3_10,BRK3_14,BRK2
2_1,BRK22_2,BRK22_3,BRK22_4,BRK22_5,BRK22_6,BRK22_7,Cbl1,Cbl2,Cbl3,Cbl2
5,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,CBL7,CBL8,CBL9,CBL10,CBL12,CBL24,CBL25,
CBL26,CBL28,CBL61,CBL94,CBL95,CBL96,CBL97,CBL98,CBL99,CBL100,CBL108,CBL
109,CBL110,Lod1,Lod2,Lod3,Lod25,Lod26,Lod27,Lod28,Lod29,Lod30,LVP1,LVP2
,LVP14,LVP15,LVP16,LVR2,MBT2,MBT12,MBT13,MOT_AcCpr4,MOT_ACcpr3,MOT_Fpmp
6,MOT_Steer1,MOT_WPmp3,MOT_WPmp4,XFM1,XFM9,XFM10" />

<Partition4of5
MTCs="ABT4,ABT5,ABT6,ABT7,ABT8,ABT9,BRK1,BRK1_1,BRK1_2,BRK1_4,BRK1_5,BR
K1_6,BRK1_7,BRK1_8,BRK1_10,BRK1_13,BRK1_15,BRK1_16,BRK2_1,BRK2_2,BRK2_4
,BRK2_10,BRK2_12,BRK2_15,BRK2_16,BRK3_16,CBL1,CBL4,CBL6,CBL35,CBL37,CBL
38,CBL39,CBL40,CBL41,CBL44,CBL45,CBL47,CBL48,CBL49,CBL50,CBL52,CBL58,CB
L60,CBL63,CBL74,CBL75,CBL83,CBL85,CBL86,CBL89,CBL101,GEN1,LOD7,LOD8,LOD
9,LVP4,LVP5,LVP6,LVP7,LVP8,LVP9,LVP12,MBT7,MBT8,MOT_AcCpr2,MOT_ACcpr1,M
OT_Fpmp3,MOT_Fpmp5,MOT_HPcpr1,MOT_WPmp1,MOT_WPmp2" />

<Partition5of5
MTCs="ABT2,ABT3,ABT10,BRK1_3,BRK1_12,BRK1_14,BRK2,BRK2_3,BRK2_5,BRK2_6,
BRK2_8,BRK2_9,BRK2_13,BRK2_14,BRK2_17,BRK2_18,BRK2_19,BRK3,BRK3_1,BRK3_
4,BRK3_5,BRK3_6,BRK3_8,Cbl10,Cbl11,Cbl12,Cbl13,Cbl14,Cbl15,CBL2,CBL3,CB
L5,CBL27,CBL29,CBL30,CBL31,CBL32,CBL33,CBL34,CBL36,CBL46,CBL53,CBL54,CB
L56,CBL57,CBL59,CBL62,CBL65,CBL82,CBL84,CBL88,CBL103,GEN2,GEN3,Lod10,Lo
d11,Lod12,Lod13,Lod14,Lod15,LOD5,LOD6,LVP10,LVP11,LVR1,MBT6,MBT10,MOT_F
pmp2,MOT_Fpmp4,MOT_Steer2,XFM4,XFM5" />
```

```
<Partition1of6
MTCs="ABT3,ABT6,ABT12,BRK1_4,BRK1_10,BRK2_10,BRK2_17,BRK3_6,BRK11_3,BRK
12_1,BRK12_2,BRK12_4,BRK12_5,BRK13_3,Cbl7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,C
BL22,CBL33,CBL34,CBL37,CBL38,CBL46,CBL52,CBL54,CBL64,CBL67,CBL74,CBL75,
CBL76,CBL77,CBL78,CBL79,CBL80,CBL81,CBL102,CBL107,Lod7,Lod8,Lod9,Lod22,
Lod23,Lod24,LOD4,LOD6,LOD8,LOD10,LOD13,LVP4,MBT1,MBT5,MBT7,MBT9,MOT_ACc
pr1,XFM3,XFM8" />

<Partition2of6
MTCs="ABT2,ABT5,ABT8,ABT9,BRK1,BRK1_1,BRK1_2,BRK1_3,BRK1_5,BRK1_7,BRK1_
8,BRK1_9,BRK1_11,BRK1_13,BRK1_14,BRK1_16,BRK2_1,BRK2_3,BRK2_4,BRK2_9,BR
K2_12,BRK3_4,BRK3_16,CBL1,CBL4,CBL6,CBL29,CBL30,CBL35,CBL36,CBL39,CBL40
,CBL45,CBL48,CBL49,CBL50,CBL53,CBL58,CBL59,CBL83,CBL84,CBL88,CBL89,CBL1
01,FLT3,GEN1,LOD7,LOD9,LVP5,LVP8,LVP11,LVP12,LVR1,MBT8,MBT10,MOT_AcCpr2
,MOT_Fpmp3,MOT_Fpmp4,MOT_HPcpr1,MOT_Steer2" />

<Partition3of6
MTCs="ABT4,ABT7,ABT10,BRK1_6,BRK1_12,BRK1_15,BRK2,BRK2_2,BRK2_5,BRK2_6,
BRK2_7,BRK2_8,BRK2_11,BRK2_14,BRK2_15,BRK2_16,BRK2_18,BRK3_5,Cbl10,Cbl1
1,Cbl12,Cbl13,Cbl14,Cbl15,CBL2,CBL31,CBL32,CBL41,CBL44,CBL47,CBL51,CBL5
6,CBL57,CBL60,CBL62,CBL63,CBL65,CBL82,CBL85,CBL86,CBL103,GEN2,Lod10,Lod
11,Lod12,Lod13,Lod14,Lod15,LOD5,LVP6,LVP7,LVP9,LVP10,MBT6,MOT_Fpmp2,MOT
_Fpmp5,MOT_WPmp1,MOT_WPmp2,XFM4,XFM5" />

<Partition4of6
MTCs="ABT11,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK21_1,BRK
21_2,BRK21_3,BRK21_4,BRK21_5,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl21,CBL18,
CBL21,CBL55,CBL66,CBL68,CBL69,CBL70,CBL71,CBL72,CBL73,CBL87,CBL90,CBL91
,CBL92,CBL93,CBL104,CBL105,FLT1,FLT2,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,Lod1
6,Lod17,Lod18,Lod19,Lod20,Lod21,LOD3,LOD11,LOD12,LVP13,LVP17,MBT4,MBT11
,MOT_Anchor,MOT_Fpmp1,XFM6,XFM7" />

<Partition5of6
MTCs="ABT1,ABT13,ABT15,BRK2_13,BRK2_19,BRK3,BRK3_1,BRK3_2,BRK3_3,BRK3_7
,BRK3_8,BRK3_10,BRK3_11,BRK3_15,BRK22_1,BRK22_3,BRK22_5,BRK22_6,BRK22_7
,Cbl28,Cbl29,Cbl30,CBL3,CBL5,CBL7,CBL8,CBL9,CBL10,CBL11,CBL23,CBL24,CBL
25,CBL27,CBL28,CBL61,CBL94,CBL95,CBL96,CBL98,CBL100,CBL108,CBL109,GEN3,
Lod28,Lod29,Lod30,LVP1,LVP2,LVP3,LVP14,LVP15,LVR2,MBT2,MBT12,MOT_ACcpr3
,MOT_Fpmp6,MOT_Hpcpr2,MOT_Steer1,MOT_WPmp3,MOT_WPmp4,XFM10" />

<Partition6of6
MTCs="ABT14,BRK3_9,BRK3_12,BRK3_13,BRK3_14,BRK22_2,BRK22_4,BRK31_1,BRK3
1_2,BRK31_3,BRK31_4,BRK31_5,Cbl1,Cbl2,Cbl3,Cbl4,Cbl5,Cbl6,Cbl25,Cbl26,C
bl27,Cbl31,Cbl32,Cbl33,CBL12,CBL13,CBL14,CBL15,CBL16,CBL17,CBL19,CBL20,
CBL26,CBL97,CBL99,CBL106,CBL110,Lod1,Lod2,Lod3,Lod4,Lod5,Lod6,Lod25,Lod
26,Lod27,Lod31,Lod32,Lod33,LOD1,LOD2,LVP16,MBT3,MBT13,MOT_AcCpr4,XFM1,X
FM2,XFM9,XFM11" />
```

```
<Partition1of7
MTCs="ABT2,ABT5,ABT8,BRK1,BRK1_1,BRK1_2,BRK1_3,BRK1_4,BRK1_5,BRK1_6,BRK
1_7,BRK1_8,BRK1_9,BRK1_10,BRK1_13,BRK1_15,BRK2_4,BRK3_4,CBL1,CBL29,CBL3
0,CBL35,CBL36,CBL37,CBL38,CBL39,CBL40,CBL44,CBL45,CBL48,CBL49,CBL58,CBL
74,CBL83,CBL85,CBL89,FLT3,GEN1,LOD7,LVP4,LVP5,LVP8,LVP12,LVR1,MBT7,MBT8
,MOT_AcCpr2,MOT_ACcpr1,MOT_Fpmp3,MOT_HPcpr1,MOT_Steer2" />
```

```
<Partition2of7
MTCs="ABT3,ABT4,ABT6,ABT7,ABT9,ABT10,BRK1_12,BRK1_16,BRK2,BRK2_1,BRK2_2
,BRK2_5,BRK2_7,BRK2_8,BRK2_9,BRK2_10,BRK2_12,BRK2_15,BRK2_16,BRK2_17,BR
K2_18,BRK3_6,CBL2,CBL6,CBL33,CBL34,CBL41,CBL46,CBL47,CBL50,CBL52,CBL53,
CBL54,CBL57,CBL60,CBL63,CBL75,CBL82,CBL86,CBL101,CBL103,GEN2,LOD6,LOD8,
LOD9,LVP6,LVP7,LVP9,LVP10,MOT_Fpmp2,MOT_Fpmp5,MOT_WPmp1,MOT_WPmp2" />

<Partition3of7
MTCs="BRK1_11,BRK1_14,BRK2_3,BRK2_6,BRK2_11,BRK2_14,BRK12_2,BRK12_4,BRK
12_5,Cbl7,Cbl8,Cbl9,Cbl10,Cbl11,Cbl12,Cbl13,Cbl14,Cbl15,CBL51,CBL56,CBL
59,CBL62,CBL64,CBL77,CBL79,CBL80,CBL81,CBL84,CBL88,CBL102,Lod7,Lod8,Lod
9,Lod10,Lod11,Lod12,Lod13,Lod14,Lod15,LOD10,LOD13,LVP11,MBT1,MBT9,MBT10
,MOT_Fpmp4,XFM3,XFM4,XFM5" />

<Partition4of7
MTCs="ABT14,BRK3_12,BRK12_1,BRK21_1,BRK21_2,BRK21_3,BRK21_4,BRK21_5,BRK
31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_5,Cbl16,Cbl17,Cbl18,Cbl31,Cbl32,Cbl3
3,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL22,CBL55,CBL76,CBL87,CBL90,CBL
92,CBL93,CBL105,CBL106,FLT6,FLT7,Lod16,Lod17,Lod18,Lod31,Lod32,Lod33,LO
D1,LOD2,LOD4,LOD11,LOD12,MBT5,MBT11,XFM6,XFM11" />

<Partition5of7
MTCs="ABT11,ABT12,BRK3_13,BRK11_1,BRK11_2,BRK11_3,BRK11_4,BRK11_5,BRK11
_6,BRK11_7,BRK13_3,Cbl19,Cbl20,Cbl21,Cbl22,Cbl23,Cbl24,CBL13,CBL21,CBL6
6,CBL67,CBL68,CBL69,CBL70,CBL71,CBL72,CBL73,CBL78,CBL91,CBL104,CBL107,F
LT1,FLT2,FLT4,FLT5,FLT8,FLT9,Lod19,Lod20,Lod21,Lod22,Lod23,Lod24,LOD3,L
VP13,LVP17,MBT3,MBT4,MOT_Anchor,MOT_Fpmp1,XFM7,XFM8" />

<Partition6of7
MTCs="ABT1,ABT15,BRK2_19,BRK3,BRK3_1,BRK3_2,BRK3_5,BRK3_7,BRK3_9,BRK3_1
0,BRK3_11,BRK3_14,BRK3_15,BRK3_16,BRK22_4,Cbl1,Cbl2,Cbl3,CBL3,CBL4,CBL5
,CBL7,CBL8,CBL11,CBL12,CBL23,CBL24,CBL25,CBL26,CBL28,CBL31,CBL32,CBL65,
CBL97,CBL110,GEN3,Lod1,Lod2,Lod3,LOD5,LVP1,LVP3,LVP16,LVR2,MBT6,MBT13,M
OT_AcCpr4,MOT_Fpmp6,MOT_Hpcpr2,MOT_Steer1,XFM1" />

<Partition7of7
MTCs="ABT13,BRK2_13,BRK3_3,BRK3_8,BRK22_1,BRK22_2,BRK22_3,BRK22_5,BRK22
_6,BRK22_7,Cbl4,Cbl5,Cbl6,Cbl25,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,CBL9,CBL1
0,CBL14,CBL27,CBL61,CBL94,CBL95,CBL96,CBL98,CBL99,CBL100,CBL108,CBL109,
Lod4,Lod5,Lod6,Lod25,Lod26,Lod27,Lod28,Lod29,Lod30,LVP2,LVP14,LVP15,MBT
2,MBT12,MOT_ACcpr3,MOT_WPmp3,MOT_WPmp4,XFM2,XFM9,XFM10" />
```

```
<Partition1of8
MTCs="ABT3,ABT12,BRK1_11,BRK2_11,BRK3_6,BRK11_3,BRK12_1,BRK12_2,BRK12_4
,BRK12_5,BRK13_3,Cbl7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,CBL22,CBL33,CBL51,CBL
54,CBL64,CBL67,CBL76,CBL77,CBL78,CBL79,CBL80,CBL81,CBL102,CBL107,Lod7,L
od8,Lod9,Lod22,Lod23,Lod24,LOD4,LOD10,LOD13,MBT1,MBT5,MBT9,XFM3,XFM8"
/>

<Partition2of8
MTCs="ABT4,ABT5,ABT10,BRK1_5,BRK1_6,BRK1_12,BRK2_5,BRK2_14,BRK2_15,BRK2
_16,BRK2_18,BRK3_5,Cbl13,Cbl14,Cbl15,CBL31,CBL32,CBL34,CBL39,CBL41,CBL4
4,CBL45,CBL47,CBL57,CBL62,CBL63,CBL65,CBL82,CBL103,Lod13,Lod14,Lod15,LO
D5,LOD6,LVP6,LVP7,LVP8,LVP10,MBT6,MOT_Fpmp2,MOT_Fpmp3,MOT_WPmp1,MOT_WPm
p2,XFM5" />
```

```
<Partition3of8
MTCs="ABT2,ABT7,BRK1,BRK1_1,BRK1_3,BRK1_7,BRK1_8,BRK1_9,BRK1_10,BRK1_14
,BRK1_15,BRK2_2,BRK2_3,BRK2_12,BRK3_4,BRK3_16,CBL1,CBL4,CBL29,CBL30,CBL
36,CBL40,CBL48,CBL49,CBL50,CBL59,CBL60,CBL74,CBL84,CBL85,CBL86,CBL88,FL
T3,GEN1,LOD7,LVP5,LVP9,LVP11,LVR1,MBT8,MBT10,MOT_Fpmp4,MOT_Fpmp5,MOT_HP
cpr1,MOT_Steer2" />

<Partition4of8
MTCs="ABT6,ABT8,ABT9,BRK1_2,BRK1_4,BRK1_13,BRK1_16,BRK2,BRK2_1,BRK2_4,B
RK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_10,BRK2_17,Cbl10,Cbl11,Cbl12,CBL2,CBL6,
CBL35,CBL37,CBL38,CBL46,CBL52,CBL53,CBL56,CBL58,CBL75,CBL83,CBL89,CBL10
1,GEN2,Lod10,Lod11,Lod12,LOD8,LOD9,LVP4,LVP12,MBT7,MOT_AcCpr2,MOT_ACcpr
1,XFM4" />

<Partition5of8
MTCs="ABT1,ABT15,BRK2_13,BRK3_2,BRK3_3,BRK3_8,BRK3_10,BRK22_2,BRK22_3,B
RK22_5,BRK22_6,BRK22_7,Cbl25,Cbl26,Cbl27,CBL7,CBL8,CBL9,CBL10,CBL24,CBL
25,CBL27,CBL61,CBL94,CBL95,CBL96,CBL98,CBL99,CBL109,Lod25,Lod26,Lod27,L
VP1,LVP2,LVP14,LVP15,LVR2,MBT2,MBT12,MOT_ACcpr3,MOT_Fpmp6,MOT_Steer1,MO
T_WPmp3,MOT_WPmp4,XFM9" />

<Partition6of8
MTCs="ABT13,BRK2_19,BRK3,BRK3_1,BRK3_7,BRK3_9,BRK3_11,BRK3_12,BRK3_13,B
RK3_14,BRK3_15,BRK22_1,BRK22_4,Cbl1,Cbl2,Cbl3,Cbl28,Cbl29,Cbl30,CBL3,CB
L5,CBL11,CBL12,CBL13,CBL23,CBL26,CBL28,CBL97,CBL100,CBL108,CBL110,GEN3,
Lod1,Lod2,Lod3,Lod28,Lod29,Lod30,LVP3,LVP16,MBT13,MOT_AcCpr4,MOT_Hpcpr2
,XFM1,XFM10" />

<Partition7of8
MTCs="ABT14,BRK21_1,BRK21_2,BRK21_3,BRK21_4,BRK21_5,BRK31_1,BRK31_2,BRK
31_4,BRK31_5,Cbl16,Cbl17,Cbl18,Cbl31,Cbl32,Cbl33,CBL15,CBL16,CBL17,CBL1
9,CBL20,CBL55,CBL87,CBL90,CBL91,CBL92,CBL93,CBL105,CBL106,FLT5,FLT6,FLT
7,Lod16,Lod17,Lod18,Lod31,Lod32,Lod33,LOD1,LOD2,LOD11,LOD12,MBT11,XFM6,
XFM11" />

<Partition8of8
MTCs="ABT11,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11_6,BRK11_7,BRK31_3,Cbl
4,Cbl5,Cbl6,Cbl19,Cbl20,Cbl21,CBL14,CBL18,CBL21,CBL66,CBL68,CBL69,CBL70
,CBL71,CBL72,CBL73,CBL104,FLT1,FLT2,FLT4,FLT8,FLT9,Lod4,Lod5,Lod6,Lod19
,Lod20,Lod21,LOD3,LVP13,LVP17,MBT3,MBT4,MOT_Anchor,MOT_Fpmp1,XFM2,XFM7"
/>
```

```
<Partition1of9
MTCs="ABT2,ABT6,BRK1,BRK1_1,BRK1_3,BRK1_6,BRK1_7,BRK1_8,BRK1_9,BRK1_10,
BRK1_14,BRK1_16,BRK2_1,BRK2_3,BRK2_10,BRK3_4,CBL1,CBL6,CBL29,CBL30,CBL3
6,CBL40,CBL49,CBL52,CBL59,CBL74,CBL75,CBL84,CBL88,FLT3,GEN1,LOD8,LVP5,L
VP11,LVR1,MBT10,MOT_Fpmp4,MOT_HPcpr1,MOT_Steer2" />

<Partition2of9
MTCs="ABT4,ABT7,ABT8,ABT9,BRK1_2,BRK1_4,BRK1_13,BRK1_15,BRK2_2,BRK2_4,B
RK2_9,BRK2_15,BRK2_17,CBL35,CBL37,CBL38,CBL41,CBL44,CBL46,CBL53,CBL58,C
BL60,CBL63,CBL83,CBL85,CBL86,CBL89,CBL101,LOD9,LVP4,LVP6,LVP7,LVP9,LVP1
2,MBT7,MOT_AcCpr2,MOT_ACcpr1,MOT_Fpmp5,MOT_WPmp1,MOT_WPmp2" />

<Partition3of9
MTCs="ABT3,ABT5,ABT10,BRK1_5,BRK1_12,BRK2,BRK2_5,BRK2_6,BRK2_7,BRK2_8,B
```

```
RK2_16,BRK2_18,BRK3_6,Cbl10,Cbl11,Cbl12,CBL2,CBL32,CBL33,CBL34,CBL39,CB
L45,CBL47,CBL54,CBL56,CBL57,CBL65,CBL82,CBL103,GEN2,Lod10,Lod11,Lod12,L
OD5,LOD6,LVP8,LVP10,MBT6,MOT_Fpmp2,MOT_Fpmp3,XFM4" />

<Partition4of9
MTCs="BRK1_11,BRK2_11,BRK2_12,BRK2_14,BRK3_11,BRK12_2,BRK12_4,BRK12_5,C
bl7,Cbl8,Cbl9,Cbl13,Cbl14,Cbl15,CBL23,CBL48,CBL50,CBL51,CBL62,CBL64,CBL
77,CBL79,CBL80,CBL81,CBL102,Lod7,Lod8,Lod9,Lod13,Lod14,Lod15,LOD7,LOD10
,LOD13,MBT1,MBT8,MBT9,XFM3,XFM5" />

<Partition5of9
MTCs="ABT1,BRK2_19,BRK3,BRK3_1,BRK3_2,BRK3_5,BRK3_9,BRK3_10,BRK3_14,BRK
3_15,BRK3_16,BRK22_4,BRK22_5,Cbl1,Cbl2,Cbl3,CBL3,CBL4,CBL5,CBL11,CBL12,
CBL24,CBL25,CBL26,CBL31,CBL96,CBL97,CBL110,GEN3,Lod1,Lod2,Lod3,LVP3,LVP
16,LVR2,MBT13,MOT_AcCpr4,MOT_Hpcpr2,MOT_Steer1,XFM1" />

<Partition6of9
MTCs="ABT13,ABT15,BRK2_13,BRK3_3,BRK3_7,BRK22_1,BRK22_2,BRK22_3,BRK22_6
,BRK22_7,Cbl25,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,CBL7,CBL8,CBL9,CBL10,CBL28
,CBL61,CBL94,CBL95,CBL99,CBL100,CBL108,Lod25,Lod26,Lod27,Lod28,Lod29,Lo
d30,LVP1,LVP2,MBT2,MOT_ACcpr3,MOT_Fpmp6,XFM9,XFM10" />

<Partition7of9
MTCs="ABT14,BRK3_8,BRK3_12,BRK12_1,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK3
1_5,Cbl31,Cbl32,Cbl33,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL22,C
BL27,CBL76,CBL98,CBL106,CBL109,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,LOD4,LV
P14,LVP15,MBT4,MBT5,MBT12,MOT_WPmp3,MOT_WPmp4,XFM11" />

<Partition8of9
MTCs="ABT11,BRK3_13,BRK11_7,BRK21_1,BRK21_2,BRK21_3,BRK21_5,Cbl4,Cbl5,C
bl6,Cbl16,Cbl17,Cbl18,CBL13,CBL14,CBL55,CBL71,CBL87,CBL91,CBL92,CBL93,C
BL104,FLT4,FLT5,FLT6,FLT7,FLT8,FLT9,Lod4,Lod5,Lod6,Lod16,Lod17,Lod18,LO
D11,LVP13,MBT3,MOT_Fpmp1,XFM2,XFM6" />

<Partition9of9
MTCs="ABT12,BRK11_1,BRK11_2,BRK11_3,BRK11_4,BRK11_5,BRK11_6,BRK13_3,BRK
21_4,Cbl19,Cbl20,Cbl21,Cbl22,Cbl23,Cbl24,CBL66,CBL67,CBL68,CBL69,CBL70,
CBL72,CBL73,CBL78,CBL90,CBL105,CBL107,FLT1,FLT2,Lod19,Lod20,Lod21,Lod22
,Lod23,Lod24,LOD12,LVP17,MBT11,MOT_Anchor,XFM7,XFM8" />
```

```
<Partition1of10
MTCs="ABT12,BRK1_11,BRK11_3,BRK12_1,BRK12_2,BRK12_4,BRK12_5,BRK13_3,Cbl
7,Cbl8,Cbl9,Cbl22,Cbl23,Cbl24,CBL22,CBL64,CBL67,CBL76,CBL77,CBL78,CBL79
,CBL81,CBL107,Lod7,Lod8,Lod9,Lod22,Lod23,Lod24,LOD4,LOD13,MBT1,MBT5,XFM
3,XFM8" />

<Partition2of10
MTCs="ABT6,ABT8,BRK1,BRK1_7,BRK1_10,BRK1_13,BRK1_14,BRK2_3,BRK2_4,BRK2_
10,BRK2_11,CBL40,CBL51,CBL52,CBL58,CBL59,CBL74,CBL75,CBL80,CBL83,CBL84,
CBL88,CBL89,CBL102,GEN1,LOD8,LOD10,LVP5,LVP11,LVP12,MBT9,MBT10,MOT_AcCp
r2,MOT_Fpmp4,MOT_HPcpr1" />

<Partition3of10
MTCs="ABT3,BRK1_8,BRK2,BRK2_1,BRK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_12,BRK2_
18,BRK3_5,BRK3_6,Cbl10,Cbl11,Cbl12,CBL2,CBL31,CBL32,CBL33,CBL34,CBL48,C
```

```
BL49,CBL50,CBL54,CBL56,CBL65,GEN2,Lod10,Lod11,Lod12,LOD5,LOD6,LOD7,MBT6
,MBT8,XFM4" />

<Partition4of10
MTCs="ABT4,ABT7,ABT9,ABT10,BRK1_1,BRK1_2,BRK1_6,BRK1_12,BRK1_15,BRK1_16
,BRK2_2,BRK2_5,BRK2_15,CBL1,CBL6,CBL35,CBL41,CBL44,CBL53,CBL57,CBL60,CB
L63,CBL82,CBL85,CBL86,CBL101,CBL103,LOD9,LVP6,LVP7,LVP9,LVP10,MOT_Fpmp2
,MOT_Fpmp5,MOT_WPmp1,MOT_WPmp2" />

<Partition5of10
MTCs="ABT2,ABT5,BRK1_3,BRK1_4,BRK1_5,BRK1_9,BRK2_14,BRK2_16,BRK2_17,BRK
3_4,BRK3_16,Cbl13,Cbl14,Cbl15,CBL4,CBL29,CBL30,CBL36,CBL37,CBL38,CBL39,
CBL45,CBL46,CBL47,CBL62,FLT3,Lod13,Lod14,Lod15,LVP4,LVP8,LVR1,MBT7,MOT_
ACcpr1,MOT_Fpmp3,MOT_Steer2,XFM5" />

<Partition6of10
MTCs="ABT13,BRK2_13,BRK3_7,BRK22_1,BRK22_2,BRK22_3,BRK22_4,BRK22_5,BRK2
2_6,BRK22_7,Cbl25,Cbl26,Cbl27,Cbl28,Cbl29,Cbl30,CBL28,CBL61,CBL94,CBL96
,CBL97,CBL99,CBL100,CBL108,CBL110,Lod25,Lod26,Lod27,Lod28,Lod29,Lod30,L
VP16,MBT13,MOT_AcCpr4,XFM9,XFM10" />

<Partition7of10
MTCs="ABT1,ABT15,BRK2_19,BRK3,BRK3_1,BRK3_2,BRK3_3,BRK3_8,BRK3_9,BRK3_1
0,BRK3_11,BRK3_15,CBL3,CBL5,CBL7,CBL8,CBL11,CBL23,CBL24,CBL25,CBL26,CBL
27,CBL98,CBL109,GEN3,LVP1,LVP3,LVP14,LVP15,LVR2,MBT12,MOT_Fpmp6,MOT_Hpc
pr2,MOT_Steer1,MOT_WPmp3,MOT_WPmp4" />

<Partition8of10
MTCs="ABT14,BRK3_12,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_5,Cbl
31,Cbl32,Cbl33,CBL9,CBL10,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL
73,CBL87,CBL95,CBL106,FLT2,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,LVP2,MBT2,M
BT4,MOT_ACcpr3,XFM11" />

<Partition9of10
MTCs="ABT11,BRK3_13,BRK11_1,BRK11_2,BRK11_4,BRK11_5,BRK11_6,BRK11_7,Cbl
4,Cbl5,Cbl6,CBL13,CBL14,CBL66,CBL68,CBL70,CBL71,CBL72,CBL90,CBL104,CBL1
05,FLT1,FLT4,FLT8,FLT9,Lod4,Lod5,Lod6,LOD12,LVP13,LVP17,MBT3,MBT11,MOT_
Anchor,MOT_Fpmp1,XFM2" />

<Partition10of10
MTCs="BRK3_14,BRK21_1,BRK21_2,BRK21_3,BRK21_4,Cbl1,Cbl2,Cbl3,Cbl16,Cbl1
7,Cbl18,Cbl19,Cbl20,Cbl21,CBL12,CBL55,CBL69,CBL91,CBL92,CBL93,FLT5,FLT6
,FLT7,Lod1,Lod2,Lod3,Lod16,Lod17,Lod18,Lod19,Lod20,Lod21,LOD11,XFM1,XFM
6,XFM7" />
```

```
<Partition1of11
MTCs="ABT3,ABT8,ABT10,BRK1_16,BRK2,BRK2_1,BRK2_4,BRK2_5,BRK2_7,BRK2_8,B
RK2_10,BRK2_11,BRK2_12,BRK2_15,BRK3_6,CBL2,CBL6,CBL33,CBL34,CBL50,CBL54
,CBL57,CBL58,CBL63,CBL89,CBL103,GEN2,LOD6,LVP10,LVP12,MOT_AcCpr2,MOT_Fp
mp2" />

<Partition2of11
MTCs="ABT7,BRK1_15,BRK2_2,BRK2_6,BRK2_14,BRK2_18,BRK3_5,Cbl10,Cbl11,Cbl
12,Cbl13,Cbl14,Cbl15,CBL31,CBL32,CBL56,CBL60,CBL62,CBL65,CBL85,CBL86,Lo
d10,Lod11,Lod12,Lod13,Lod14,Lod15,LOD5,LVP9,MBT6,MOT_Fpmp5,XFM4,XFM5"
/>
```

```
<Partition3of11
MTCs="ABT2,BRK1_3,BRK1_11,BRK3_4,BRK3_11,BRK12_2,BRK12_4,BRK12_5,Cbl7,C
bl8,Cbl9,CBL23,CBL29,CBL30,CBL36,CBL51,CBL64,CBL77,CBL79,CBL80,CBL81,CB
L102,Lod7,Lod8,Lod9,LOD10,LOD13,LVR1,MBT1,MBT9,MOT_Steer2,XFM3" />

<Partition4of11
MTCs="ABT6,ABT9,BRK1,BRK1_1,BRK1_2,BRK1_7,BRK1_8,BRK1_9,BRK1_10,BRK1_12
,BRK1_13,BRK2_9,BRK3_16,CBL1,CBL4,CBL35,CBL40,CBL48,CBL49,CBL52,CBL53,C
BL74,CBL75,CBL82,CBL83,CBL101,FLT3,GEN1,LOD7,LOD8,LOD9,LVP5,MBT8,MOT_HP
cpr1" />

<Partition5of11
MTCs="ABT4,ABT5,BRK1_4,BRK1_5,BRK1_6,BRK1_14,BRK2_3,BRK2_16,BRK2_17,CBL
37,CBL38,CBL39,CBL41,CBL44,CBL45,CBL46,CBL47,CBL59,CBL84,CBL88,LVP4,LVP
6,LVP7,LVP8,LVP11,MBT7,MBT10,MOT_ACcpr1,MOT_Fpmp3,MOT_Fpmp4,MOT_WPmp1,M
OT_WPmp2" />

<Partition6of11
MTCs="ABT11,ABT12,BRK11_3,BRK11_5,BRK11_7,BRK13_3,Cbl19,Cbl20,Cbl21,Cbl
22,Cbl23,Cbl24,CBL67,CBL69,CBL71,CBL78,CBL104,CBL107,FLT4,FLT5,FLT8,FLT
9,Lod19,Lod20,Lod21,Lod22,Lod23,Lod24,LVP13,MOT_Fpmp1,XFM7,XFM8" />

<Partition7of11
MTCs="BRK11_1,BRK11_2,BRK11_4,BRK11_6,BRK21_1,BRK21_2,BRK21_3,BRK21_4,C
bl16,Cbl17,Cbl18,CBL55,CBL66,CBL68,CBL70,CBL72,CBL73,CBL90,CBL91,CBL92,
CBL93,CBL105,FLT6,FLT7,Lod16,Lod17,Lod18,LOD11,LOD12,LVP17,MBT11,MOT_An
chor,XFM6" />

<Partition8of11
MTCs="ABT14,BRK12_1,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_5,Cbl
31,Cbl32,Cbl33,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL22,CBL76,CB
L87,CBL106,FLT2,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,LOD4,MBT4,MBT5,XFM11"
/>

<Partition9of11
MTCs="ABT13,BRK2_13,BRK3_9,BRK22_1,BRK22_2,BRK22_4,BRK22_7,Cbl25,Cbl26,
Cbl27,Cbl28,Cbl29,Cbl30,CBL26,CBL61,CBL94,CBL97,CBL99,CBL100,CBL108,CBL
110,Lod25,Lod26,Lod27,Lod28,Lod29,Lod30,LVP16,MBT13,MOT_AcCpr4,XFM9,XFM
10" />

<Partition10of11
MTCs="ABT15,BRK2_19,BRK3_1,BRK3_2,BRK3_3,BRK3_7,BRK3_8,BRK3_15,BRK22_3,
BRK22_6,CBL3,CBL5,CBL7,CBL8,CBL9,CBL10,CBL11,CBL27,CBL28,CBL95,CBL98,CB
L109,LVP1,LVP2,LVP3,LVP14,LVP15,MBT2,MBT12,MOT_ACcpr3,MOT_Fpmp6,MOT_Hpc
pr2,MOT_WPmp3,MOT_WPmp4" />

<Partition11of11
MTCs="ABT1,BRK3,BRK3_10,BRK3_12,BRK3_13,BRK3_14,BRK22_5,Cbl1,Cbl2,Cbl3,
Cbl4,Cbl5,Cbl6,CBL12,CBL13,CBL14,CBL24,CBL25,CBL96,FLT1,GEN3,Lod1,Lod2,
Lod3,Lod4,Lod5,Lod6,LVR2,MBT3,MOT_Steer1,XFM1,XFM2" />
```

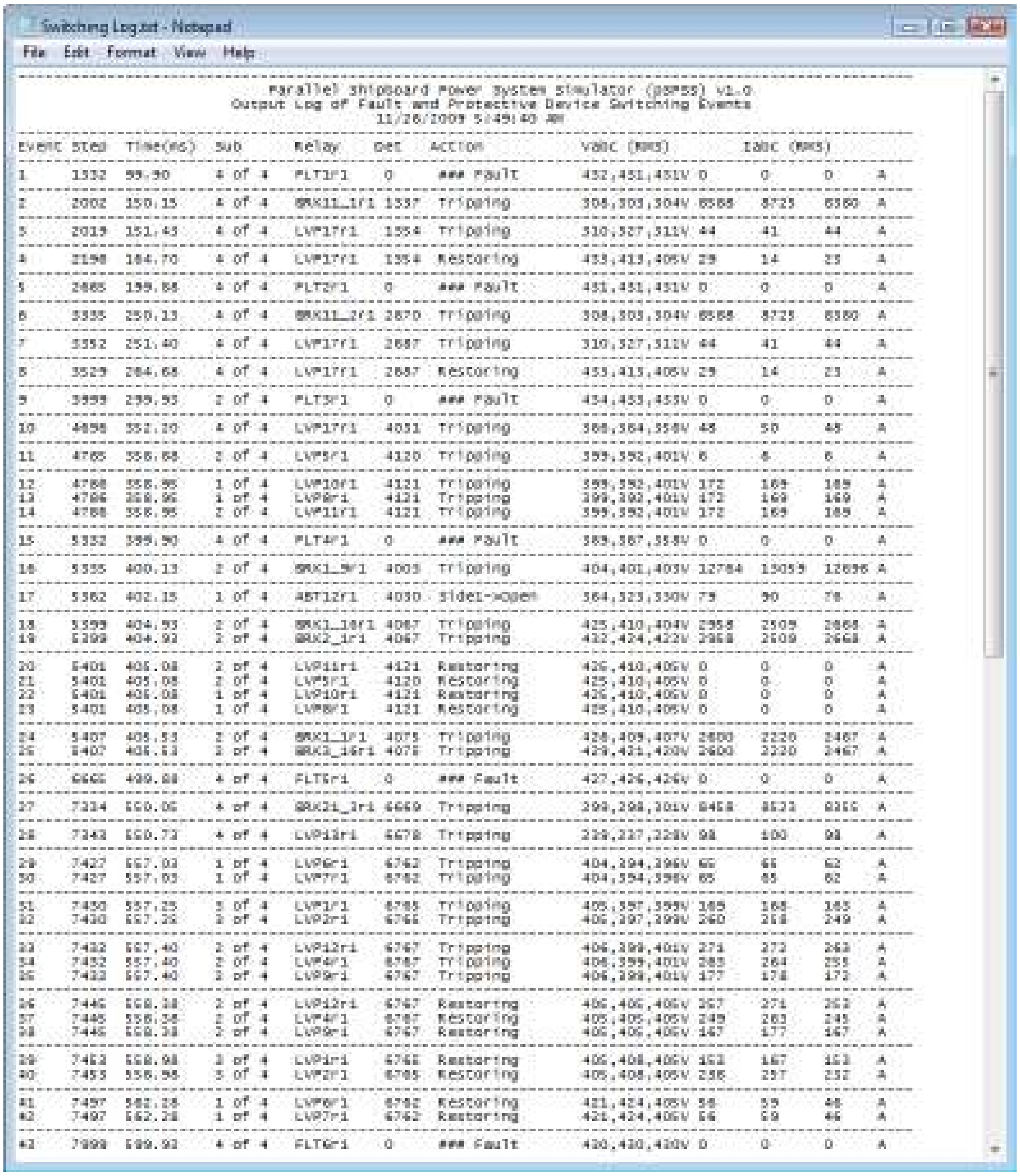
```
<Partition1of12
MTCs="ABT4,ABT10,BRK1_6,BRK1_12,BRK2_5,BRK2_14,BRK2_15,Cbl13,Cbl14,Cbl1
5,CBL41,CBL44,CBL57,CBL62,CBL63,CBL82,CBL103,Lod13,Lod14,Lod15,LVP6,LVP
7,LVP10,MOT_Fpmp2,MOT_WPmp1,MOT_WPmp2,XFM5" />
```

```
<Partition2of12
MTCs="ABT12,BRK1_11,BRK2_11,BRK11_3,BRK12_1,BRK12_2,BRK12_5,BRK13_3,Cbl
22,Cbl23,Cbl24,CBL22,CBL51,CBL64,CBL67,CBL76,CBL77,CBL78,CBL80,CBL81,CB
L102,CBL107,Lod22,Lod23,Lod24,LOD4,LOD10,LOD13,MBT1,MBT5,MBT9,XFM8" />

<Partition3of12
MTCs="ABT3,ABT5,BRK1_5,BRK2_16,BRK2_18,BRK3_5,BRK3_6,BRK12_4,Cbl7,Cbl8,
Cbl9,CBL31,CBL32,CBL33,CBL34,CBL39,CBL45,CBL47,CBL54,CBL65,CBL79,Lod7,L
od8,Lod9,LOD5,LOD6,LVP8,MBT6,MOT_Fpmp3,XFM3" />

<Partition4of12
MTCs="ABT6,ABT9,BRK1_10,BRK2,BRK2_6,BRK2_7,BRK2_8,BRK2_9,BRK2_10,BRK2_1
2,BRK2_17,Cbl10,Cbl11,Cbl12,CBL2,CBL46,CBL50,CBL52,CBL53,CBL56,CBL74,CB
L75,CBL101,GEN2,Lod10,Lod11,Lod12,LOD8,LOD9,XFM4" />

<Partition5of12
MTCs="ABT2,BRK1,BRK1_1,BRK1_3,BRK1_4,BRK1_7,BRK1_8,BRK1_9,BRK3_4,BRK3_1
6,CBL1,CBL4,CBL29,CBL30,CBL36,CBL37,CBL38,CBL40,CBL48,CBL49,FLT3,GEN1,L
OD7,LVP4,LVP5,LVR1,MBT7,MBT8,MOT_ACcpr1,MOT_HPcpr1,MOT_Steer2" />

<Partition6of12
MTCs="ABT7,ABT8,BRK1_2,BRK1_13,BRK1_14,BRK1_15,BRK1_16,BRK2_1,BRK2_2,BR
K2_3,BRK2_4,CBL6,CBL35,CBL58,CBL59,CBL60,CBL83,CBL84,CBL85,CBL86,CBL88,
CBL89,LVP9,LVP11,LVP12,MBT10,MOT_AcCpr2,MOT_Fpmp4,MOT_Fpmp5" />

<Partition7of12
MTCs="ABT15,BRK2_13,BRK3_2,BRK3_3,BRK22_2,BRK22_4,BRK22_5,BRK22_6,BRK22
_7,Cbl25,Cbl26,Cbl27,CBL7,CBL8,CBL9,CBL10,CBL61,CBL94,CBL95,CBL97,CBL99
,Lod25,Lod26,Lod27,LVP1,LVP2,MBT2,MOT_ACcpr3,MOT_Fpmp6,XFM9" />

<Partition8of12
MTCs="BRK2_19,BRK3,BRK3_1,BRK3_8,BRK3_9,BRK3_11,BRK3_12,BRK3_13,BRK3_15
,BRK22_3,CBL3,CBL5,CBL11,CBL13,CBL23,CBL26,CBL27,CBL98,CBL109,CBL110,GE
N3,LVP3,LVP14,LVP15,LVP16,MBT12,MBT13,MOT_AcCpr4,MOT_Hpcpr2,MOT_WPmp3,M
OT_WPmp4" />

<Partition9of12
MTCs="ABT1,ABT13,BRK3_7,BRK3_10,BRK3_14,BRK22_1,Cbl1,Cbl2,Cbl3,Cbl28,Cb
l29,Cbl30,CBL12,CBL24,CBL25,CBL28,CBL96,CBL100,CBL108,Lod1,Lod2,Lod3,Lo
d28,Lod29,Lod30,LVR2,MOT_Steer1,XFM1,XFM10" />

<Partition10of12
MTCs="ABT11,BRK11_1,BRK11_4,BRK11_5,BRK11_6,BRK11_7,Cbl4,Cbl5,Cbl6,CBL1
4,CBL66,CBL68,CBL70,CBL71,CBL72,CBL104,FLT1,FLT4,FLT5,FLT8,FLT9,Lod4,Lo
d5,Lod6,LVP13,LVP17,MBT3,MOT_Anchor,MOT_Fpmp1,XFM2" />

<Partition11of12
MTCs="ABT14,BRK11_2,BRK21_5,BRK31_1,BRK31_2,BRK31_3,BRK31_4,BRK31_5,Cbl
31,Cbl32,Cbl33,CBL15,CBL16,CBL17,CBL18,CBL19,CBL20,CBL21,CBL73,CBL87,CB
L106,FLT2,Lod31,Lod32,Lod33,LOD1,LOD2,LOD3,MBT4,XFM11" />

<Partition12of12
MTCs="BRK21_1,BRK21_2,BRK21_3,BRK21_4,Cbl16,Cbl17,Cbl18,Cbl19,Cbl20,Cbl
21,CBL55,CBL69,CBL90,CBL91,CBL92,CBL93,CBL105,FLT6,FLT7,Lod16,Lod17,Lod
18,Lod19,Lod20,Lod21,LOD11,LOD12,MBT11,XFM6,XFM7" />

     </Partitions>
```

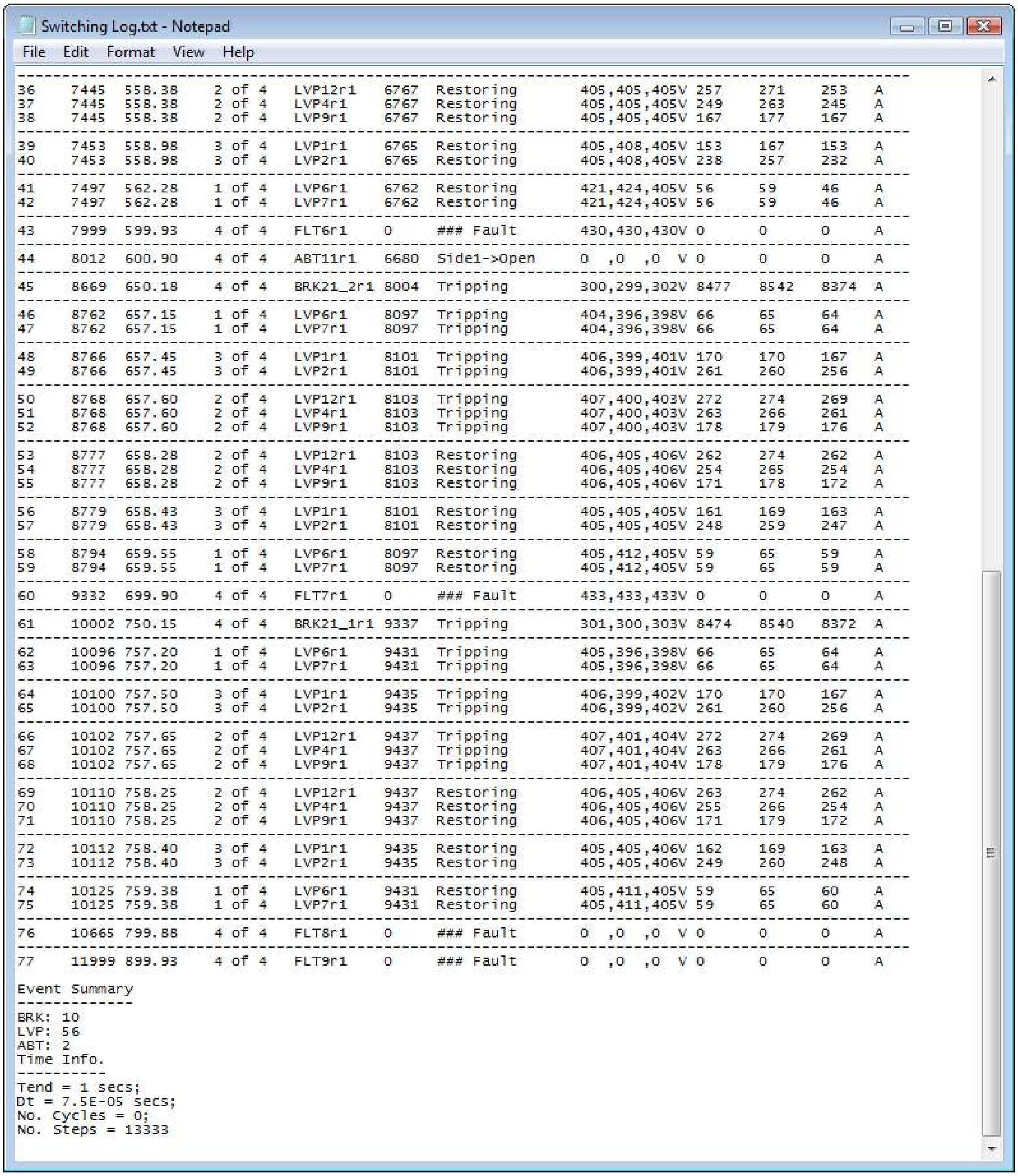
APPENDIX D

FAULT AND PROTECTIVE DEVICE EVENTS

Performance Metric 2: Δt=75μs

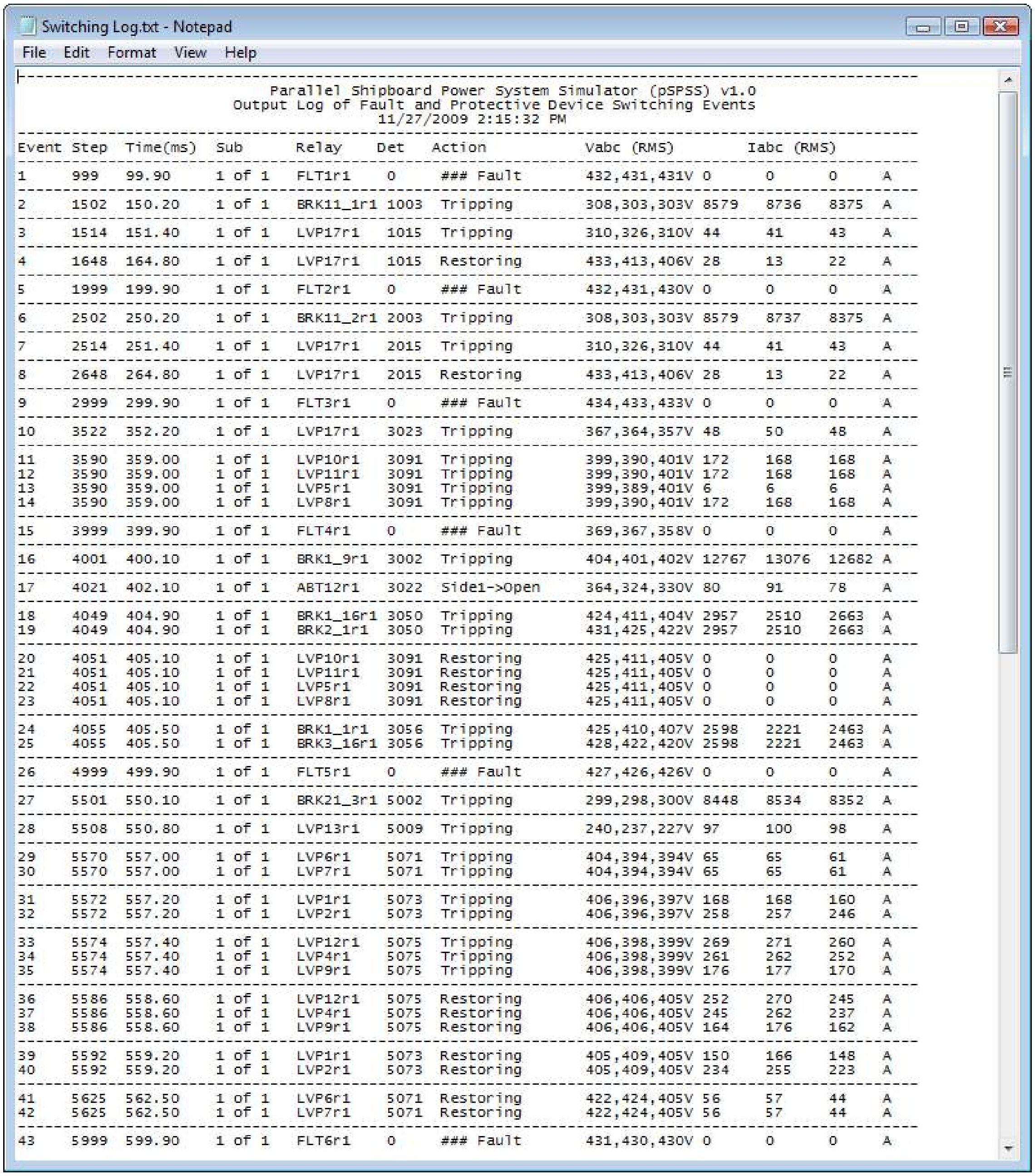


```
------------------------------------------------------------------------------------------------------
                     Parallel Shipboard Power System Simulator (PSPSS) v1.0
                   Output Log of Fault and Protective Device Switching Events
                                  11/26/2009 5:49:40 AM
------------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub     Relay     Det   Action            Vabc (RMS)         Iabc (RMS)
------------------------------------------------------------------------------------------------------
1     1332  99.90     4 of 4  FLT1r1    0     ### Fault         432,431,431V 0     0      0     A
------------------------------------------------------------------------------------------------------
2     2002  150.15    4 of 4  BRK11_1r1 1337  Tripping          308,303,304V 8588  8725   8580  A
------------------------------------------------------------------------------------------------------
3     2019  151.43    4 of 4  LVP17r1   1354  Tripping          310,327,311V 44    41     44    A
------------------------------------------------------------------------------------------------------
4     2196  164.70    4 of 4  LVP17r1   1354  Restoring         433,413,405V 29    14     23    A
------------------------------------------------------------------------------------------------------
5     2665  199.88    4 of 4  FLT2r1    0     ### Fault         431,431,431V 0     0      0     A
------------------------------------------------------------------------------------------------------
6     3335  250.13    4 of 4  BRK11_2r1 2670  Tripping          308,303,304V 8588  8725   8580  A
------------------------------------------------------------------------------------------------------
7     3352  251.40    4 of 4  LVP17r1   2687  Tripping          310,327,311V 44    41     44    A
------------------------------------------------------------------------------------------------------
8     3529  264.68    4 of 4  LVP17r1   2687  Restoring         433,413,405V 29    14     23    A
------------------------------------------------------------------------------------------------------
9     3999  299.93    2 of 4  FLT3r1    0     ### Fault         434,433,433V 0     0      0     A
------------------------------------------------------------------------------------------------------
10    4696  352.20    4 of 4  LVP17r1   4031  Tripping          368,364,358V 48    50     48    A
------------------------------------------------------------------------------------------------------
11    4785  358.88    2 of 4  LVP5r1    4120  Tripping          399,392,401V 6     6      6     A
------------------------------------------------------------------------------------------------------
12    4786  358.95    1 of 4  LVP10r1   4121  Tripping          399,392,401V 172   169    169   A
13    4786  358.95    1 of 4  LVP8r1    4121  Tripping          399,392,401V 172   169    169   A
14    4786  358.95    2 of 4  LVP11r1   4121  Tripping          399,392,401V 172   169    169   A
------------------------------------------------------------------------------------------------------
15    5332  399.90    4 of 4  FLT4r1    0     ### Fault         363,367,358V 0     0      0     A
------------------------------------------------------------------------------------------------------
16    5335  400.13    2 of 4  BRK1_9r1  4003  Tripping          404,401,403V 12784 13059  12696 A
------------------------------------------------------------------------------------------------------
17    5362  402.15    1 of 4  ABT12r1   4030  Side1->Open       364,323,330V 79    90     78    A
------------------------------------------------------------------------------------------------------
18    5399  404.93    2 of 4  BRK1_16r1 4067  Tripping          425,410,404V 2958  2509   2668  A
19    5399  404.93    2 of 4  BRK2_1r1  4067  Tripping          432,424,422V 2958  2509   2668  A
------------------------------------------------------------------------------------------------------
20    5401  405.08    2 of 4  LVP11r1   4121  Restoring         426,410,406V 0     0      0     A
21    5401  405.08    2 of 4  LVP5r1    4120  Restoring         425,410,405V 0     0      0     A
22    5401  405.08    1 of 4  LVP10r1   4121  Restoring         426,410,406V 0     0      0     A
23    5401  405.08    1 of 4  LVP8r1    4121  Restoring         425,410,405V 0     0      0     A
------------------------------------------------------------------------------------------------------
24    5407  405.53    2 of 4  BRK1_1r1  4075  Tripping          428,409,407V 2600  2220   2467  A
25    5407  405.53    2 of 4  BRK2_16r1 4075  Tripping          429,421,420V 2600  2220   2467  A
------------------------------------------------------------------------------------------------------
26    6666  499.95    4 of 4  FLT5r1    0     ### Fault         427,426,426V 0     0      0     A
------------------------------------------------------------------------------------------------------
27    7334  550.05    4 of 4  BRK21_3r1 6669  Tripping          299,298,301V 8458  8523   8356  A
------------------------------------------------------------------------------------------------------
28    7343  550.73    4 of 4  LVP13r1   6678  Tripping          229,227,228V 98    100    98    A
------------------------------------------------------------------------------------------------------
29    7427  557.03    1 of 4  LVP6r1    6762  Tripping          404,394,396V 66    66     62    A
30    7427  557.03    1 of 4  LVP7r1    6762  Tripping          404,394,398V 65    65     62    A
------------------------------------------------------------------------------------------------------
31    7430  557.25    3 of 4  LVP1r1    6765  Tripping          405,397,399V 165   168    163   A
32    7430  557.25    3 of 4  LVP2r1    6766  Tripping          406,397,399V 260   258    249   A
------------------------------------------------------------------------------------------------------
33    7432  557.40    2 of 4  LVP12r1   6767  Tripping          406,399,401V 271   272    262   A
34    7432  557.40    2 of 4  LVP4r1    6767  Tripping          406,399,401V 283   264    255   A
35    7432  557.40    2 of 4  LVP9r1    6767  Tripping          406,399,401V 177   178    172   A
------------------------------------------------------------------------------------------------------
36    7445  558.38    2 of 4  LVP12r1   6767  Restoring         406,406,406V 267   271    262   A
37    7445  558.38    2 of 4  LVP4r1    6767  Restoring         405,405,405V 249   263    245   A
38    7445  558.38    2 of 4  LVP9r1    6767  Restoring         406,406,406V 167   177    167   A
------------------------------------------------------------------------------------------------------
39    7453  558.98    3 of 4  LVP1r1    6766  Restoring         406,408,406V 162   167    163   A
40    7453  558.98    3 of 4  LVP2r1    6765  Restoring         405,408,405V 238   257    232   A
------------------------------------------------------------------------------------------------------
41    7497  562.28    1 of 4  LVP6r1    6762  Restoring         421,424,405V 56    59     46    A
42    7497  562.28    1 of 4  LVP7r1    6762  Restoring         421,424,406V 56    59     46    A
------------------------------------------------------------------------------------------------------
43    7999  599.93    4 of 4  FLT6r1    0     ### Fault         430,430,430V 0     0      0     A
```

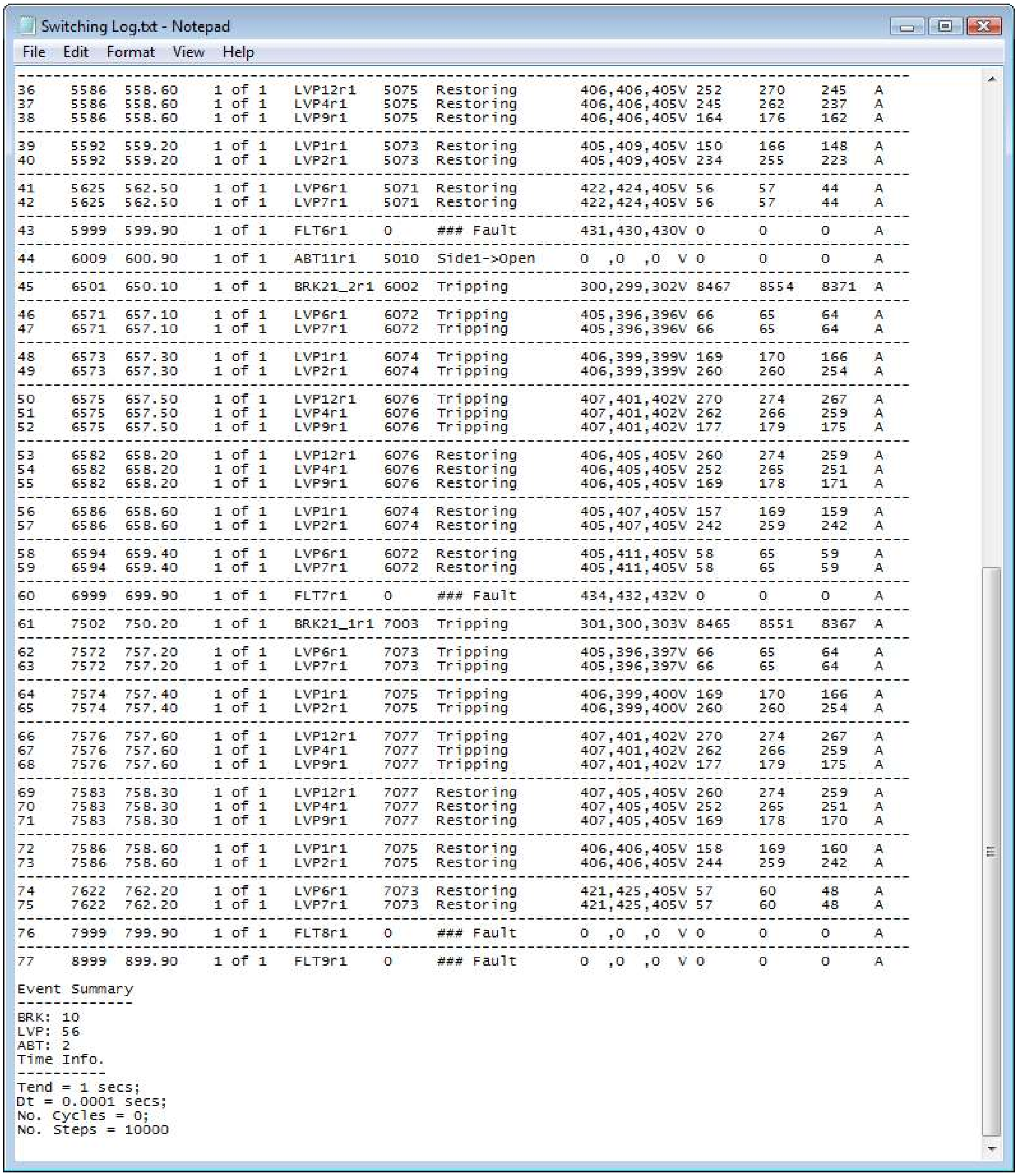


```
----------------------------------------------------------------------------------------------------
36    7445  558.38    2 of 4   LVP12r1   6767  Restoring       405,405,405V 257    271    253    A
37    7445  558.38    2 of 4   LVP4r1    6767  Restoring       405,405,405V 249    263    245    A
38    7445  558.38    2 of 4   LVP9r1    6767  Restoring       405,405,405V 167    177    167    A
----------------------------------------------------------------------------------------------------
39    7453  558.98    3 of 4   LVP1r1    6765  Restoring       405,408,405V 153    167    153    A
40    7453  558.98    3 of 4   LVP2r1    6765  Restoring       405,408,405V 238    257    232    A
----------------------------------------------------------------------------------------------------
41    7497  562.28    1 of 4   LVP6r1    6762  Restoring       421,424,405V 56     59     46     A
42    7497  562.28    1 of 4   LVP7r1    6762  Restoring       421,424,405V 56     59     46     A
----------------------------------------------------------------------------------------------------
43    7999  599.93    4 of 4   FLT6r1    0     ### Fault       430,430,430V 0      0      0      A
----------------------------------------------------------------------------------------------------
44    8012  600.90    4 of 4   ABT11r1   6680  Side1->Open     0  ,0  ,0  V 0      0      0      A
----------------------------------------------------------------------------------------------------
45    8669  650.18    4 of 4   BRK21_2r1 8004  Tripping        300,299,302V 8477   8542   8374   A
----------------------------------------------------------------------------------------------------
46    8762  657.15    1 of 4   LVP6r1    8097  Tripping        404,396,398V 66     65     64     A
47    8762  657.15    1 of 4   LVP7r1    8097  Tripping        404,396,398V 66     65     64     A
----------------------------------------------------------------------------------------------------
48    8766  657.45    3 of 4   LVP1r1    8101  Tripping        406,399,401V 170    170    167    A
49    8766  657.45    3 of 4   LVP2r1    8101  Tripping        406,399,401V 261    260    256    A
----------------------------------------------------------------------------------------------------
50    8768  657.60    2 of 4   LVP12r1   8103  Tripping        407,400,403V 272    274    269    A
51    8768  657.60    2 of 4   LVP4r1    8103  Tripping        407,400,403V 263    266    261    A
52    8768  657.60    2 of 4   LVP9r1    8103  Tripping        407,400,403V 178    179    176    A
----------------------------------------------------------------------------------------------------
53    8777  658.28    2 of 4   LVP12r1   8103  Restoring       406,405,406V 262    274    262    A
54    8777  658.28    2 of 4   LVP4r1    8103  Restoring       406,405,406V 254    265    254    A
55    8777  658.28    2 of 4   LVP9r1    8103  Restoring       406,405,406V 171    178    172    A
----------------------------------------------------------------------------------------------------
56    8779  658.43    3 of 4   LVP1r1    8101  Restoring       405,405,405V 161    169    163    A
57    8779  658.43    3 of 4   LVP2r1    8101  Restoring       405,405,405V 248    259    247    A
----------------------------------------------------------------------------------------------------
58    8794  659.55    1 of 4   LVP6r1    8097  Restoring       405,412,405V 59     65     59     A
59    8794  659.55    1 of 4   LVP7r1    8097  Restoring       405,412,405V 59     65     59     A
----------------------------------------------------------------------------------------------------
60    9332  699.90    4 of 4   FLT7r1    0     ### Fault       433,433,433V 0      0      0      A
----------------------------------------------------------------------------------------------------
61    10002 750.15    4 of 4   BRK21_1r1 9337  Tripping        301,300,303V 8474   8540   8372   A
----------------------------------------------------------------------------------------------------
62    10096 757.20    1 of 4   LVP6r1    9431  Tripping        405,396,398V 66     65     64     A
63    10096 757.20    1 of 4   LVP7r1    9431  Tripping        405,396,398V 66     65     64     A
----------------------------------------------------------------------------------------------------
64    10100 757.50    3 of 4   LVP1r1    9435  Tripping        406,399,402V 170    170    167    A
65    10100 757.50    3 of 4   LVP2r1    9435  Tripping        406,399,402V 261    260    256    A
----------------------------------------------------------------------------------------------------
66    10102 757.65    2 of 4   LVP12r1   9437  Tripping        407,401,404V 272    274    269    A
67    10102 757.65    2 of 4   LVP4r1    9437  Tripping        407,401,404V 263    266    261    A
68    10102 757.65    2 of 4   LVP9r1    9437  Tripping        407,401,404V 178    179    176    A
----------------------------------------------------------------------------------------------------
69    10110 758.25    2 of 4   LVP12r1   9437  Restoring       406,405,406V 263    274    262    A
70    10110 758.25    2 of 4   LVP4r1    9437  Restoring       406,405,406V 255    266    254    A
71    10110 758.25    2 of 4   LVP9r1    9437  Restoring       406,405,406V 171    179    172    A
----------------------------------------------------------------------------------------------------
72    10112 758.40    3 of 4   LVP1r1    9435  Restoring       405,405,406V 162    169    163    A
73    10112 758.40    3 of 4   LVP2r1    9435  Restoring       405,405,406V 249    260    248    A
----------------------------------------------------------------------------------------------------
74    10125 759.38    1 of 4   LVP6r1    9431  Restoring       405,411,405V 59     65     60     A
75    10125 759.38    1 of 4   LVP7r1    9431  Restoring       405,411,405V 59     65     60     A
----------------------------------------------------------------------------------------------------
76    10665 799.88    4 of 4   FLT8r1    0     ### Fault       0  ,0  ,0  V 0      0      0      A
----------------------------------------------------------------------------------------------------
77    11999 899.93    4 of 4   FLT9r1    0     ### Fault       0  ,0  ,0  V 0      0      0      A

Event Summary
-------------
BRK: 10
LVP: 56
ABT: 2
Time Info.
----------
Tend = 1 secs;
Dt = 7.5E-05 secs;
No. Cycles = 0;
No. Steps = 13333
```

Performance Metric 2: Δt=100μs

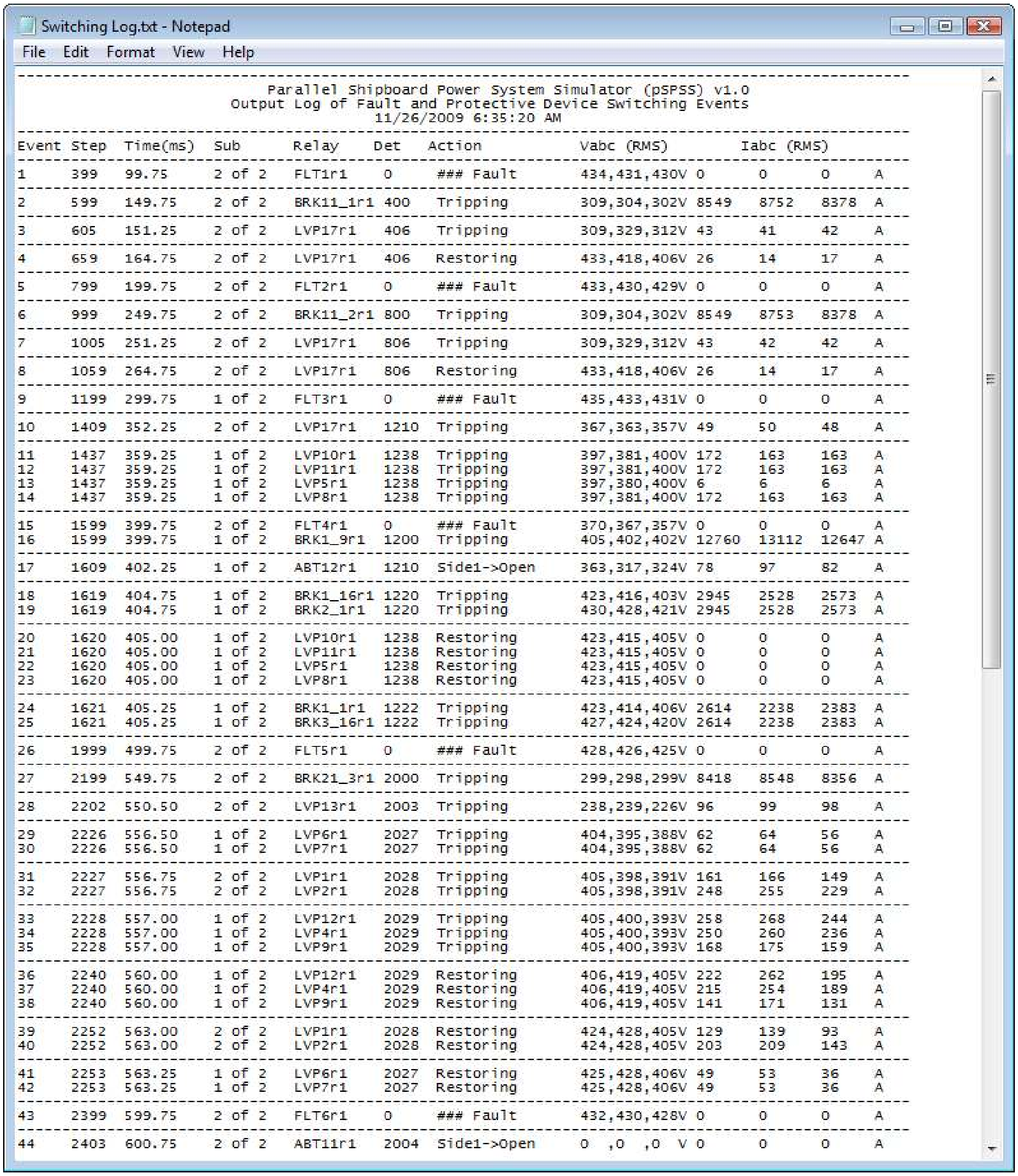


```
-----------------------------------------------------------------------------------------------------
                         Parallel Shipboard Power System Simulator (pSPSS) v1.0
                     Output Log of Fault and Protective Device Switching Events
                                        11/27/2009 2:15:32 PM
-----------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub      Relay     Det   Action        Vabc (RMS)       Iabc (RMS)
-----------------------------------------------------------------------------------------------------
1     999   99.90     1 of 1   FLT1r1    0     ### Fault     432,431,431V 0      0      0      A
-----------------------------------------------------------------------------------------------------
2     1502  150.20    1 of 1   BRK11_1r1 1003  Tripping      308,303,303V 8579   8736   8375   A
-----------------------------------------------------------------------------------------------------
3     1514  151.40    1 of 1   LVP17r1   1015  Tripping      310,326,310V 44     41     43     A
-----------------------------------------------------------------------------------------------------
4     1648  164.80    1 of 1   LVP17r1   1015  Restoring     433,413,406V 28     13     22     A
-----------------------------------------------------------------------------------------------------
5     1999  199.90    1 of 1   FLT2r1    0     ### Fault     432,431,430V 0      0      0      A
-----------------------------------------------------------------------------------------------------
6     2502  250.20    1 of 1   BRK11_2r1 2003  Tripping      308,303,303V 8579   8737   8375   A
-----------------------------------------------------------------------------------------------------
7     2514  251.40    1 of 1   LVP17r1   2015  Tripping      310,326,310V 44     41     43     A
-----------------------------------------------------------------------------------------------------
8     2648  264.80    1 of 1   LVP17r1   2015  Restoring     433,413,406V 28     13     22     A
-----------------------------------------------------------------------------------------------------
9     2999  299.90    1 of 1   FLT3r1    0     ### Fault     434,433,433V 0      0      0      A
-----------------------------------------------------------------------------------------------------
10    3522  352.20    1 of 1   LVP17r1   3023  Tripping      367,364,357V 48     50     48     A
-----------------------------------------------------------------------------------------------------
11    3590  359.00    1 of 1   LVP10r1   3091  Tripping      399,390,401V 172    168    168    A
12    3590  359.00    1 of 1   LVP11r1   3091  Tripping      399,390,401V 172    168    168    A
13    3590  359.00    1 of 1   LVP5r1    3091  Tripping      399,389,401V 6      6      6      A
14    3590  359.00    1 of 1   LVP8r1    3091  Tripping      399,390,401V 172    168    168    A
-----------------------------------------------------------------------------------------------------
15    3999  399.90    1 of 1   FLT4r1    0     ### Fault     369,367,358V 0      0      0      A
-----------------------------------------------------------------------------------------------------
16    4001  400.10    1 of 1   BRK1_9r1  3002  Tripping      404,401,402V 12767  13076  12682  A
-----------------------------------------------------------------------------------------------------
17    4021  402.10    1 of 1   ABT12r1   3022  Side1->Open   364,324,330V 80     91     78     A
-----------------------------------------------------------------------------------------------------
18    4049  404.90    1 of 1   BRK1_16r1 3050  Tripping      424,411,404V 2957   2510   2663   A
19    4049  404.90    1 of 1   BRK2_1r1  3050  Tripping      431,425,422V 2957   2510   2663   A
-----------------------------------------------------------------------------------------------------
20    4051  405.10    1 of 1   LVP10r1   3091  Restoring     425,411,405V 0      0      0      A
21    4051  405.10    1 of 1   LVP11r1   3091  Restoring     425,411,405V 0      0      0      A
22    4051  405.10    1 of 1   LVP5r1    3091  Restoring     425,411,405V 0      0      0      A
23    4051  405.10    1 of 1   LVP8r1    3091  Restoring     425,411,405V 0      0      0      A
-----------------------------------------------------------------------------------------------------
24    4055  405.50    1 of 1   BRK1_1r1  3056  Tripping      425,410,407V 2598   2221   2463   A
25    4055  405.50    1 of 1   BRK3_16r1 3056  Tripping      428,422,420V 2598   2221   2463   A
-----------------------------------------------------------------------------------------------------
26    4999  499.90    1 of 1   FLT5r1    0     ### Fault     427,426,426V 0      0      0      A
-----------------------------------------------------------------------------------------------------
27    5501  550.10    1 of 1   BRK21_3r1 5002  Tripping      299,298,300V 8448   8534   8352   A
-----------------------------------------------------------------------------------------------------
28    5508  550.80    1 of 1   LVP13r1   5009  Tripping      240,237,227V 97     100    98     A
-----------------------------------------------------------------------------------------------------
29    5570  557.00    1 of 1   LVP6r1    5071  Tripping      404,394,394V 65     65     61     A
30    5570  557.00    1 of 1   LVP7r1    5071  Tripping      404,394,394V 65     65     61     A
-----------------------------------------------------------------------------------------------------
31    5572  557.20    1 of 1   LVP1r1    5073  Tripping      406,396,397V 168    168    160    A
32    5572  557.20    1 of 1   LVP2r1    5073  Tripping      406,396,397V 258    257    246    A
-----------------------------------------------------------------------------------------------------
33    5574  557.40    1 of 1   LVP12r1   5075  Tripping      406,398,399V 269    271    260    A
34    5574  557.40    1 of 1   LVP4r1    5075  Tripping      406,398,399V 261    262    252    A
35    5574  557.40    1 of 1   LVP9r1    5075  Tripping      406,398,399V 176    177    170    A
-----------------------------------------------------------------------------------------------------
36    5586  558.60    1 of 1   LVP12r1   5075  Restoring     406,406,405V 252    270    245    A
37    5586  558.60    1 of 1   LVP4r1    5075  Restoring     406,406,405V 245    262    237    A
38    5586  558.60    1 of 1   LVP9r1    5075  Restoring     406,406,405V 164    176    162    A
-----------------------------------------------------------------------------------------------------
39    5592  559.20    1 of 1   LVP1r1    5073  Restoring     405,409,405V 150    166    148    A
40    5592  559.20    1 of 1   LVP2r1    5073  Restoring     405,409,405V 234    255    223    A
-----------------------------------------------------------------------------------------------------
41    5625  562.50    1 of 1   LVP6r1    5071  Restoring     422,424,405V 56     57     44     A
42    5625  562.50    1 of 1   LVP7r1    5071  Restoring     422,424,405V 56     57     44     A
-----------------------------------------------------------------------------------------------------
43    5999  599.90    1 of 1   FLT6r1    0     ### Fault     431,430,430V 0      0      0      A
```

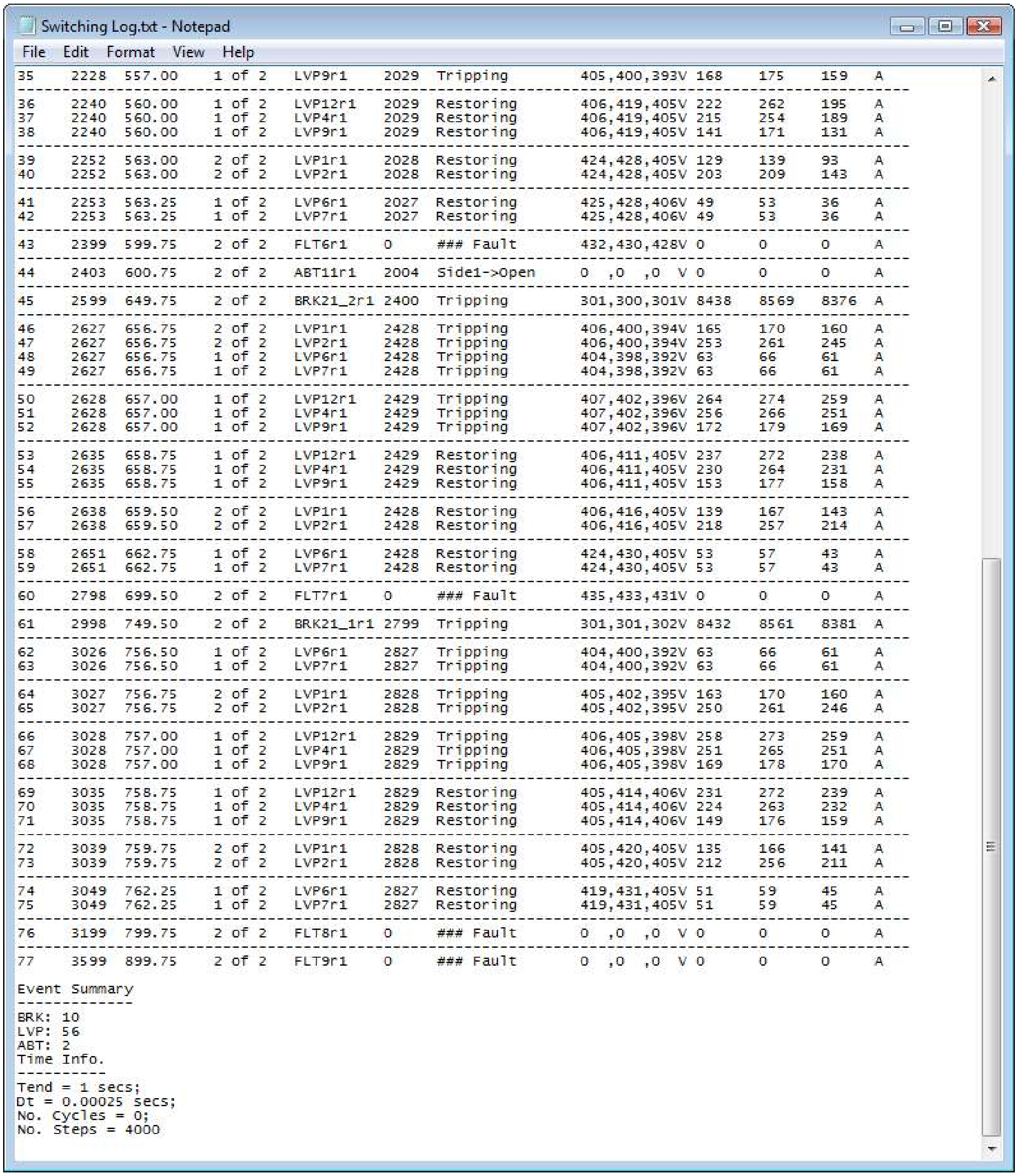


```
-------------------------------------------------------------------------------------------------
36    5586  558.60    1 of 1   LVP12r1   5075  Restoring       406,406,405V 252    270    245    A
37    5586  558.60    1 of 1   LVP4r1    5075  Restoring       406,406,405V 245    262    237    A
38    5586  558.60    1 of 1   LVP9r1    5075  Restoring       406,406,405V 164    176    162    A
-------------------------------------------------------------------------------------------------
39    5592  559.20    1 of 1   LVP1r1    5073  Restoring       405,409,405V 150    166    148    A
40    5592  559.20    1 of 1   LVP2r1    5073  Restoring       405,409,405V 234    255    223    A
-------------------------------------------------------------------------------------------------
41    5625  562.50    1 of 1   LVP6r1    5071  Restoring       422,424,405V 56     57     44     A
42    5625  562.50    1 of 1   LVP7r1    5071  Restoring       422,424,405V 56     57     44     A
-------------------------------------------------------------------------------------------------
43    5999  599.90    1 of 1   FLT6r1    0     ### Fault       431,430,430V 0      0      0      A
-------------------------------------------------------------------------------------------------
44    6009  600.90    1 of 1   ABT11r1   5010  Side1->Open     0  ,0  ,0  V 0      0      0      A
-------------------------------------------------------------------------------------------------
45    6501  650.10    1 of 1   BRK21_2r1 6002  Tripping        300,299,302V 8467   8554   8371   A
-------------------------------------------------------------------------------------------------
46    6571  657.10    1 of 1   LVP6r1    6072  Tripping        405,396,396V 66     65     64     A
47    6571  657.10    1 of 1   LVP7r1    6072  Tripping        405,396,396V 66     65     64     A
-------------------------------------------------------------------------------------------------
48    6573  657.30    1 of 1   LVP1r1    6074  Tripping        406,399,399V 169    170    166    A
49    6573  657.30    1 of 1   LVP2r1    6074  Tripping        406,399,399V 260    260    254    A
-------------------------------------------------------------------------------------------------
50    6575  657.50    1 of 1   LVP12r1   6076  Tripping        407,401,402V 270    274    267    A
51    6575  657.50    1 of 1   LVP4r1    6076  Tripping        407,401,402V 262    266    259    A
52    6575  657.50    1 of 1   LVP9r1    6076  Tripping        407,401,402V 177    179    175    A
-------------------------------------------------------------------------------------------------
53    6582  658.20    1 of 1   LVP12r1   6076  Restoring       406,405,405V 260    274    259    A
54    6582  658.20    1 of 1   LVP4r1    6076  Restoring       406,405,405V 252    265    251    A
55    6582  658.20    1 of 1   LVP9r1    6076  Restoring       406,405,405V 169    178    171    A
-------------------------------------------------------------------------------------------------
56    6586  658.60    1 of 1   LVP1r1    6074  Restoring       405,407,405V 157    169    159    A
57    6586  658.60    1 of 1   LVP2r1    6074  Restoring       405,407,405V 242    259    242    A
-------------------------------------------------------------------------------------------------
58    6594  659.40    1 of 1   LVP6r1    6072  Restoring       405,411,405V 58     65     59     A
59    6594  659.40    1 of 1   LVP7r1    6072  Restoring       405,411,405V 58     65     59     A
-------------------------------------------------------------------------------------------------
60    6999  699.90    1 of 1   FLT7r1    0     ### Fault       434,432,432V 0      0      0      A
-------------------------------------------------------------------------------------------------
61    7502  750.20    1 of 1   BRK21_1r1 7003  Tripping        301,300,303V 8465   8551   8367   A
-------------------------------------------------------------------------------------------------
62    7572  757.20    1 of 1   LVP6r1    7073  Tripping        405,396,397V 66     65     64     A
63    7572  757.20    1 of 1   LVP7r1    7073  Tripping        405,396,397V 66     65     64     A
-------------------------------------------------------------------------------------------------
64    7574  757.40    1 of 1   LVP1r1    7075  Tripping        406,399,400V 169    170    166    A
65    7574  757.40    1 of 1   LVP2r1    7075  Tripping        406,399,400V 260    260    254    A
-------------------------------------------------------------------------------------------------
66    7576  757.60    1 of 1   LVP12r1   7077  Tripping        407,401,402V 270    274    267    A
67    7576  757.60    1 of 1   LVP4r1    7077  Tripping        407,401,402V 262    266    259    A
68    7576  757.60    1 of 1   LVP9r1    7077  Tripping        407,401,402V 177    179    175    A
-------------------------------------------------------------------------------------------------
69    7583  758.30    1 of 1   LVP12r1   7077  Restoring       407,405,405V 260    274    259    A
70    7583  758.30    1 of 1   LVP4r1    7077  Restoring       407,405,405V 252    265    251    A
71    7583  758.30    1 of 1   LVP9r1    7077  Restoring       407,405,405V 169    178    170    A
-------------------------------------------------------------------------------------------------
72    7586  758.60    1 of 1   LVP1r1    7075  Restoring       406,406,405V 158    169    160    A
73    7586  758.60    1 of 1   LVP2r1    7075  Restoring       406,406,405V 244    259    242    A
-------------------------------------------------------------------------------------------------
74    7622  762.20    1 of 1   LVP6r1    7073  Restoring       421,425,405V 57     60     48     A
75    7622  762.20    1 of 1   LVP7r1    7073  Restoring       421,425,405V 57     60     48     A
-------------------------------------------------------------------------------------------------
76    7999  799.90    1 of 1   FLT8r1    0     ### Fault       0  ,0  ,0  V 0      0      0      A
-------------------------------------------------------------------------------------------------
77    8999  899.90    1 of 1   FLT9r1    0     ### Fault       0  ,0  ,0  V 0      0      0      A

Event Summary
-------------
BRK: 10
LVP: 56
ABT: 2
Time Info.
----------
Tend = 1 secs;
Dt = 0.0001 secs;
No. Cycles = 0;
No. Steps = 10000
```

Performance Metric 2: Δt=250μs

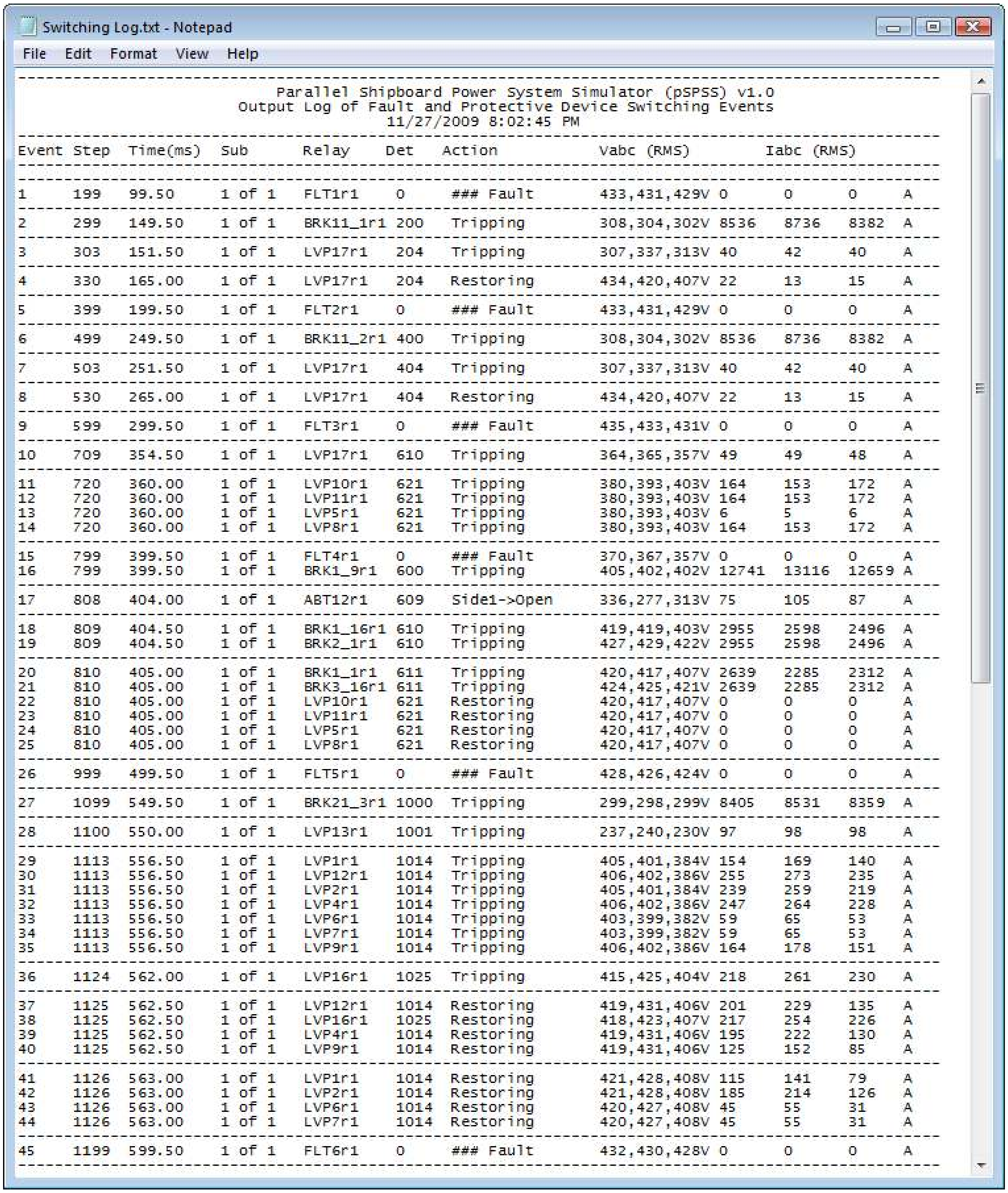


```
-------------------------------------------------------------------------------------------------------
                              Parallel Shipboard Power System Simulator (pSPSS) v1.0
                          Output Log of Fault and Protective Device Switching Events
                                            11/26/2009 6:35:20 AM
-------------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub      Relay    Det   Action             Vabc (RMS)         Iabc (RMS)
-------------------------------------------------------------------------------------------------------
1     399   99.75     2 of 2   FLT1r1    0     ### Fault         434,431,430V 0      0      0      A
-------------------------------------------------------------------------------------------------------
2     599   149.75    2 of 2   BRK11_1r1 400   Tripping          309,304,302V 8549   8752   8378   A
-------------------------------------------------------------------------------------------------------
3     605   151.25    2 of 2   LVP17r1   406   Tripping          309,329,312V 43     41     42     A
-------------------------------------------------------------------------------------------------------
4     659   164.75    2 of 2   LVP17r1   406   Restoring         433,418,406V 26     14     17     A
-------------------------------------------------------------------------------------------------------
5     799   199.75    2 of 2   FLT2r1    0     ### Fault         433,430,429V 0      0      0      A
-------------------------------------------------------------------------------------------------------
6     999   249.75    2 of 2   BRK11_2r1 800   Tripping          309,304,302V 8549   8753   8378   A
-------------------------------------------------------------------------------------------------------
7     1005  251.25    2 of 2   LVP17r1   806   Tripping          309,329,312V 43     42     42     A
-------------------------------------------------------------------------------------------------------
8     1059  264.75    2 of 2   LVP17r1   806   Restoring         433,418,406V 26     14     17     A
-------------------------------------------------------------------------------------------------------
9     1199  299.75    1 of 2   FLT3r1    0     ### Fault         435,433,431V 0      0      0      A
-------------------------------------------------------------------------------------------------------
10    1409  352.25    2 of 2   LVP17r1   1210  Tripping          367,363,357V 49     50     48     A
-------------------------------------------------------------------------------------------------------
11    1437  359.25    1 of 2   LVP10r1   1238  Tripping          397,381,400V 172    163    163    A
12    1437  359.25    1 of 2   LVP11r1   1238  Tripping          397,381,400V 172    163    163    A
13    1437  359.25    1 of 2   LVP5r1    1238  Tripping          397,380,400V 6      6      6      A
14    1437  359.25    1 of 2   LVP8r1    1238  Tripping          397,381,400V 172    163    163    A
-------------------------------------------------------------------------------------------------------
15    1599  399.75    2 of 2   FLT4r1    0     ### Fault         370,367,357V 0      0      0      A
16    1599  399.75    1 of 2   BRK1_9r1  1200  Tripping          405,402,402V 12760  13112  12647  A
-------------------------------------------------------------------------------------------------------
17    1609  402.25    1 of 2   ABT12r1   1210  Side1->Open       363,317,324V 78     97     82     A
-------------------------------------------------------------------------------------------------------
18    1619  404.75    1 of 2   BRK1_16r1 1220  Tripping          423,416,403V 2945   2528   2573   A
19    1619  404.75    1 of 2   BRK2_1r1  1220  Tripping          430,428,421V 2945   2528   2573   A
-------------------------------------------------------------------------------------------------------
20    1620  405.00    1 of 2   LVP10r1   1238  Restoring         423,415,405V 0      0      0      A
21    1620  405.00    1 of 2   LVP11r1   1238  Restoring         423,415,405V 0      0      0      A
22    1620  405.00    1 of 2   LVP5r1    1238  Restoring         423,415,405V 0      0      0      A
23    1620  405.00    1 of 2   LVP8r1    1238  Restoring         423,415,405V 0      0      0      A
-------------------------------------------------------------------------------------------------------
24    1621  405.25    1 of 2   BRK1_1r1  1222  Tripping          423,414,406V 2614   2238   2383   A
25    1621  405.25    1 of 2   BRK3_16r1 1222  Tripping          427,424,420V 2614   2238   2383   A
-------------------------------------------------------------------------------------------------------
26    1999  499.75    2 of 2   FLT5r1    0     ### Fault         428,426,425V 0      0      0      A
-------------------------------------------------------------------------------------------------------
27    2199  549.75    2 of 2   BRK21_3r1 2000  Tripping          299,298,299V 8418   8548   8356   A
-------------------------------------------------------------------------------------------------------
28    2202  550.50    2 of 2   LVP13r1   2003  Tripping          238,239,226V 96     99     98     A
-------------------------------------------------------------------------------------------------------
29    2226  556.50    1 of 2   LVP6r1    2027  Tripping          404,395,388V 62     64     56     A
30    2226  556.50    1 of 2   LVP7r1    2027  Tripping          404,395,388V 62     64     56     A
-------------------------------------------------------------------------------------------------------
31    2227  556.75    2 of 2   LVP1r1    2028  Tripping          405,398,391V 161    166    149    A
32    2227  556.75    2 of 2   LVP2r1    2028  Tripping          405,398,391V 248    255    229    A
-------------------------------------------------------------------------------------------------------
33    2228  557.00    1 of 2   LVP12r1   2029  Tripping          405,400,393V 258    268    244    A
34    2228  557.00    1 of 2   LVP4r1    2029  Tripping          405,400,393V 250    260    236    A
35    2228  557.00    1 of 2   LVP9r1    2029  Tripping          405,400,393V 168    175    159    A
-------------------------------------------------------------------------------------------------------
36    2240  560.00    1 of 2   LVP12r1   2029  Restoring         406,419,405V 222    262    195    A
37    2240  560.00    1 of 2   LVP4r1    2029  Restoring         406,419,405V 215    254    189    A
38    2240  560.00    1 of 2   LVP9r1    2029  Restoring         406,419,405V 141    171    131    A
-------------------------------------------------------------------------------------------------------
39    2252  563.00    2 of 2   LVP1r1    2028  Restoring         424,428,405V 129    139    93     A
40    2252  563.00    2 of 2   LVP2r1    2028  Restoring         424,428,405V 203    209    143    A
-------------------------------------------------------------------------------------------------------
41    2253  563.25    1 of 2   LVP6r1    2027  Restoring         425,428,406V 49     53     36     A
42    2253  563.25    1 of 2   LVP7r1    2027  Restoring         425,428,406V 49     53     36     A
-------------------------------------------------------------------------------------------------------
43    2399  599.75    2 of 2   FLT6r1    0     ### Fault         432,430,428V 0      0      0      A
-------------------------------------------------------------------------------------------------------
44    2403  600.75    2 of 2   ABT11r1   2004  Side1->Open       0  ,0  ,0  V 0      0      0      A
```

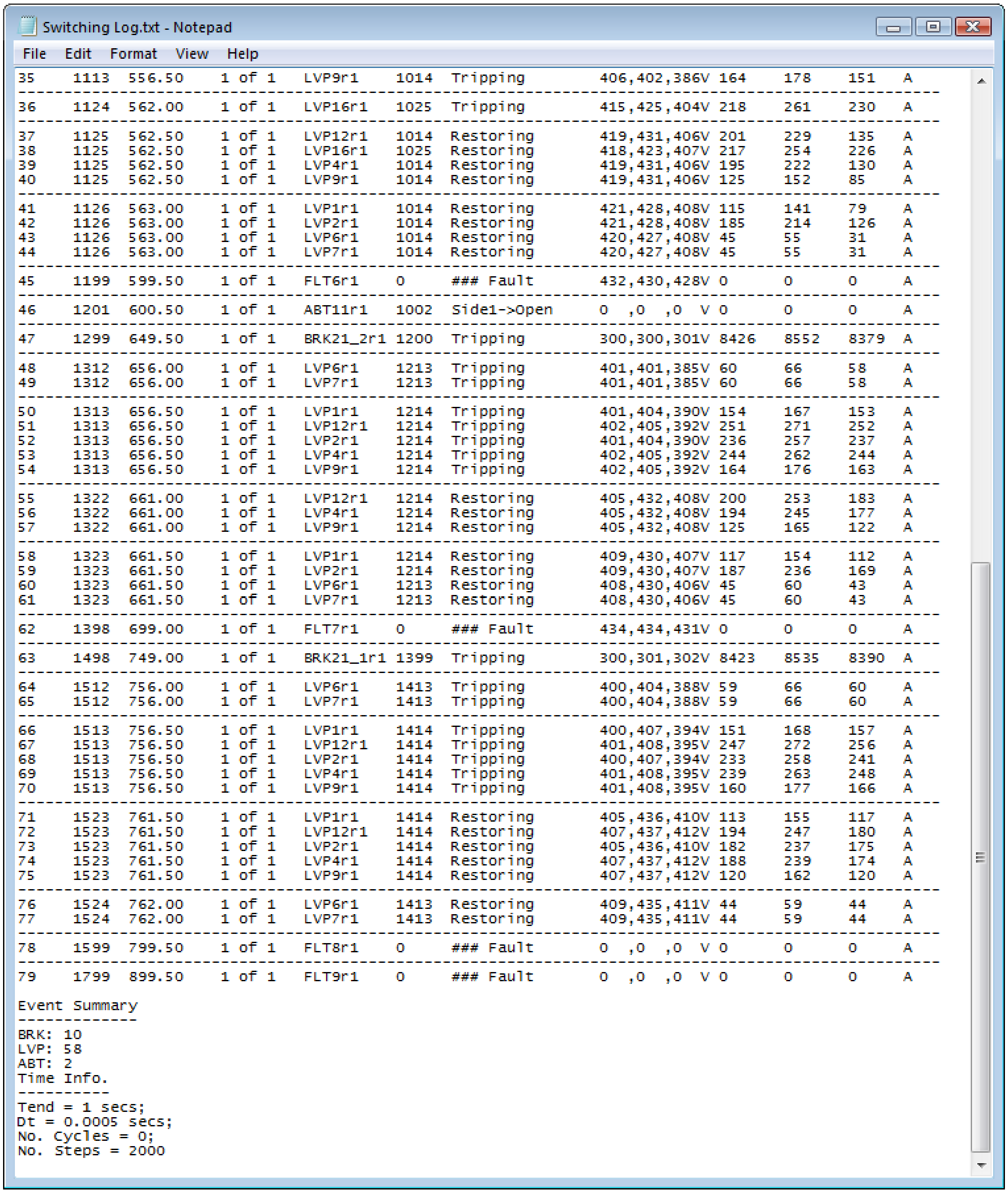


```
35     2228  557.00    1 of 2   LVP9r1    2029  Tripping        405,400,393V 168     175     159    A
----------------------------------------------------------------------------------------------------
36     2240  560.00    1 of 2   LVP12r1   2029  Restoring       406,419,405V 222     262     195    A
37     2240  560.00    1 of 2   LVP4r1    2029  Restoring       406,419,405V 215     254     189    A
38     2240  560.00    1 of 2   LVP9r1    2029  Restoring       406,419,405V 141     171     131    A
----------------------------------------------------------------------------------------------------
39     2252  563.00    2 of 2   LVP1r1    2028  Restoring       424,428,405V 129     139     93     A
40     2252  563.00    2 of 2   LVP2r1    2028  Restoring       424,428,405V 203     209     143    A
----------------------------------------------------------------------------------------------------
41     2253  563.25    1 of 2   LVP6r1    2027  Restoring       425,428,406V 49      53      36     A
42     2253  563.25    1 of 2   LVP7r1    2027  Restoring       425,428,406V 49      53      36     A
----------------------------------------------------------------------------------------------------
43     2399  599.75    2 of 2   FLT6r1    0     ### Fault       432,430,428V 0       0       0      A
----------------------------------------------------------------------------------------------------
44     2403  600.75    2 of 2   ABT11r1   2004  Side1->Open     0  ,0  ,0  V 0       0       0      A
----------------------------------------------------------------------------------------------------
45     2599  649.75    2 of 2   BRK21_2r1 2400  Tripping        301,300,301V 8438    8569    8376   A
----------------------------------------------------------------------------------------------------
46     2627  656.75    2 of 2   LVP1r1    2428  Tripping        406,400,394V 165     170     160    A
47     2627  656.75    2 of 2   LVP2r1    2428  Tripping        406,400,394V 253     261     245    A
48     2627  656.75    1 of 2   LVP6r1    2428  Tripping        404,398,392V 63      66      61     A
49     2627  656.75    1 of 2   LVP7r1    2428  Tripping        404,398,392V 63      66      61     A
----------------------------------------------------------------------------------------------------
50     2628  657.00    1 of 2   LVP12r1   2429  Tripping        407,402,396V 264     274     259    A
51     2628  657.00    1 of 2   LVP4r1    2429  Tripping        407,402,396V 256     266     251    A
52     2628  657.00    1 of 2   LVP9r1    2429  Tripping        407,402,396V 172     179     169    A
----------------------------------------------------------------------------------------------------
53     2635  658.75    1 of 2   LVP12r1   2429  Restoring       406,411,405V 237     272     238    A
54     2635  658.75    1 of 2   LVP4r1    2429  Restoring       406,411,405V 230     264     231    A
55     2635  658.75    1 of 2   LVP9r1    2429  Restoring       406,411,405V 153     177     158    A
----------------------------------------------------------------------------------------------------
56     2638  659.50    2 of 2   LVP1r1    2428  Restoring       406,416,405V 139     167     143    A
57     2638  659.50    2 of 2   LVP2r1    2428  Restoring       406,416,405V 218     257     214    A
----------------------------------------------------------------------------------------------------
58     2651  662.75    1 of 2   LVP6r1    2428  Restoring       424,430,405V 53      57      43     A
59     2651  662.75    1 of 2   LVP7r1    2428  Restoring       424,430,405V 53      57      43     A
----------------------------------------------------------------------------------------------------
60     2798  699.50    2 of 2   FLT7r1    0     ### Fault       435,433,431V 0       0       0      A
----------------------------------------------------------------------------------------------------
61     2998  749.50    2 of 2   BRK21_1r1 2799  Tripping        301,301,302V 8432    8561    8381   A
----------------------------------------------------------------------------------------------------
62     3026  756.50    1 of 2   LVP6r1    2827  Tripping        404,400,392V 63      66      61     A
63     3026  756.50    1 of 2   LVP7r1    2827  Tripping        404,400,392V 63      66      61     A
----------------------------------------------------------------------------------------------------
64     3027  756.75    2 of 2   LVP1r1    2828  Tripping        405,402,395V 163     170     160    A
65     3027  756.75    2 of 2   LVP2r1    2828  Tripping        405,402,395V 250     261     246    A
----------------------------------------------------------------------------------------------------
66     3028  757.00    1 of 2   LVP12r1   2829  Tripping        406,405,398V 258     273     259    A
67     3028  757.00    1 of 2   LVP4r1    2829  Tripping        406,405,398V 251     265     251    A
68     3028  757.00    1 of 2   LVP9r1    2829  Tripping        406,405,398V 169     178     170    A
----------------------------------------------------------------------------------------------------
69     3035  758.75    1 of 2   LVP12r1   2829  Restoring       405,414,406V 231     272     239    A
70     3035  758.75    1 of 2   LVP4r1    2829  Restoring       405,414,406V 224     263     232    A
71     3035  758.75    1 of 2   LVP9r1    2829  Restoring       405,414,406V 149     176     159    A
----------------------------------------------------------------------------------------------------
72     3039  759.75    2 of 2   LVP1r1    2828  Restoring       405,420,405V 135     166     141    A
73     3039  759.75    2 of 2   LVP2r1    2828  Restoring       405,420,405V 212     256     211    A
----------------------------------------------------------------------------------------------------
74     3049  762.25    1 of 2   LVP6r1    2827  Restoring       419,431,405V 51      59      45     A
75     3049  762.25    1 of 2   LVP7r1    2827  Restoring       419,431,405V 51      59      45     A
----------------------------------------------------------------------------------------------------
76     3199  799.75    2 of 2   FLT8r1    0     ### Fault       0  ,0  ,0  V 0       0       0      A
----------------------------------------------------------------------------------------------------
77     3599  899.75    2 of 2   FLT9r1    0     ### Fault       0  ,0  ,0  V 0       0       0      A

Event Summary
-------------
BRK: 10
LVP: 56
ABT: 2
Time Info.
----------
Tend = 1 secs;
Dt = 0.00025 secs;
No. Cycles = 0;
No. Steps = 4000
```

Performance Metric 2: Δt=500μs (p=1)

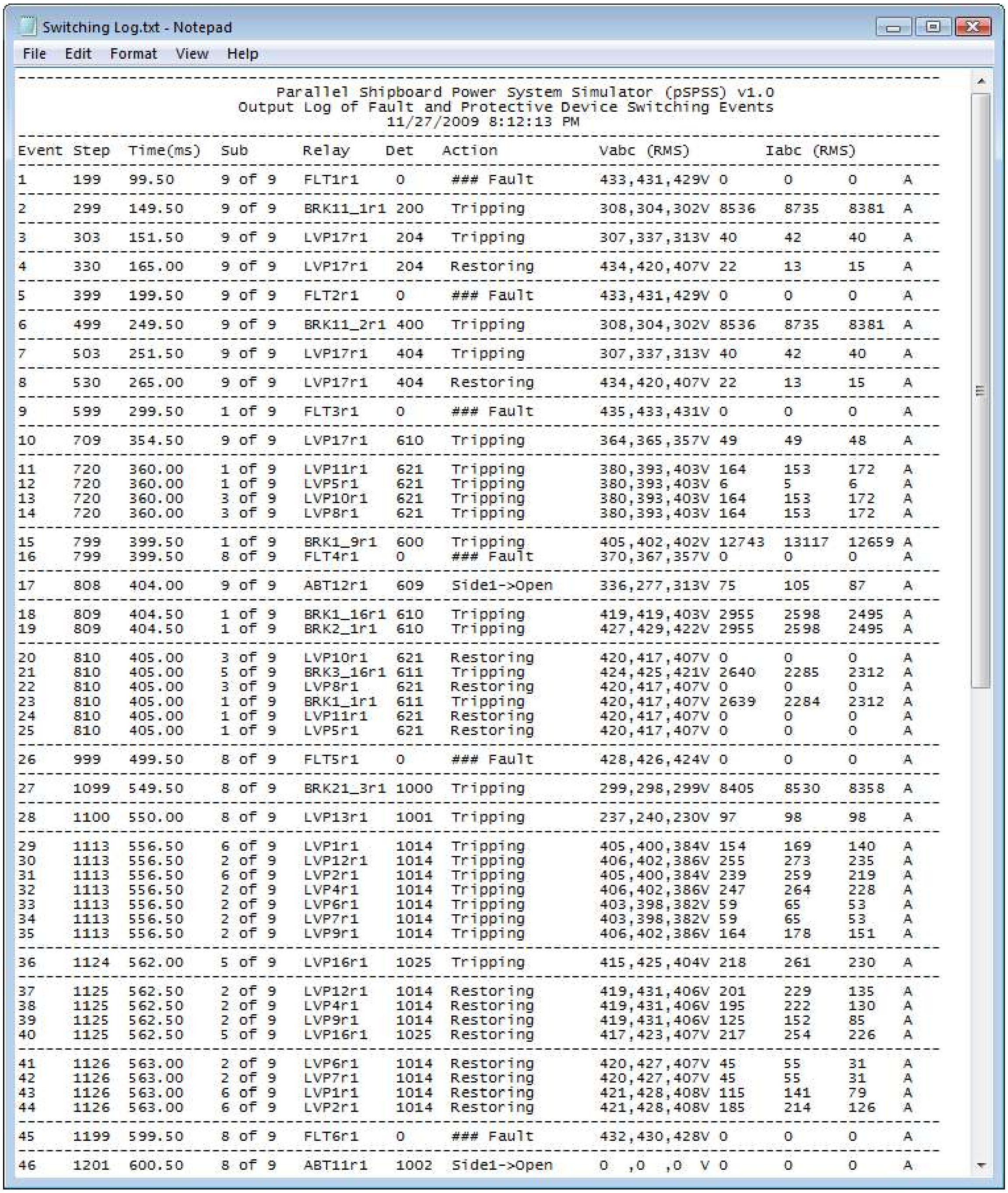


```
----------------------------------------------------------------------------------------------------
                            Parallel Shipboard Power System Simulator (pSPSS) v1.0
                        Output Log of Fault and Protective Device Switching Events
                                        11/27/2009 8:02:45 PM
----------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub      Relay     Det  Action           Vabc (RMS)        Iabc (RMS)
----------------------------------------------------------------------------------------------------
----------------------------------------------------------------------------------------------------
1     199   99.50     1 of 1   FLT1r1    0     ### Fault       433,431,429V 0      0      0     A
----------------------------------------------------------------------------------------------------
2     299   149.50    1 of 1   BRK11_1r1 200   Tripping        308,304,302V 8536   8736   8382  A
----------------------------------------------------------------------------------------------------
3     303   151.50    1 of 1   LVP17r1   204   Tripping        307,337,313V 40     42     40    A
----------------------------------------------------------------------------------------------------
4     330   165.00    1 of 1   LVP17r1   204   Restoring       434,420,407V 22     13     15    A
----------------------------------------------------------------------------------------------------
5     399   199.50    1 of 1   FLT2r1    0     ### Fault       433,431,429V 0      0      0     A
----------------------------------------------------------------------------------------------------
6     499   249.50    1 of 1   BRK11_2r1 400   Tripping        308,304,302V 8536   8736   8382  A
----------------------------------------------------------------------------------------------------
7     503   251.50    1 of 1   LVP17r1   404   Tripping        307,337,313V 40     42     40    A
----------------------------------------------------------------------------------------------------
8     530   265.00    1 of 1   LVP17r1   404   Restoring       434,420,407V 22     13     15    A
----------------------------------------------------------------------------------------------------
9     599   299.50    1 of 1   FLT3r1    0     ### Fault       435,433,431V 0      0      0     A
----------------------------------------------------------------------------------------------------
10    709   354.50    1 of 1   LVP17r1   610   Tripping        364,365,357V 49     49     48    A
----------------------------------------------------------------------------------------------------
11    720   360.00    1 of 1   LVP10r1   621   Tripping        380,393,403V 164    153    172   A
12    720   360.00    1 of 1   LVP11r1   621   Tripping        380,393,403V 164    153    172   A
13    720   360.00    1 of 1   LVP5r1    621   Tripping        380,393,403V 6      5      6     A
14    720   360.00    1 of 1   LVP8r1    621   Tripping        380,393,403V 164    153    172   A
----------------------------------------------------------------------------------------------------
15    799   399.50    1 of 1   FLT4r1    0     ### Fault       370,367,357V 0      0      0     A
16    799   399.50    1 of 1   BRK1_9r1  600   Tripping        405,402,402V 12741  13116  12659 A
----------------------------------------------------------------------------------------------------
17    808   404.00    1 of 1   ABT12r1   609   Side1->Open     336,277,313V 75     105    87    A
----------------------------------------------------------------------------------------------------
18    809   404.50    1 of 1   BRK1_16r1 610   Tripping        419,419,403V 2955   2598   2496  A
19    809   404.50    1 of 1   BRK2_1r1  610   Tripping        427,429,422V 2955   2598   2496  A
----------------------------------------------------------------------------------------------------
20    810   405.00    1 of 1   BRK1_1r1  611   Tripping        420,417,407V 2639   2285   2312  A
21    810   405.00    1 of 1   BRK3_16r1 611   Tripping        424,425,421V 2639   2285   2312  A
22    810   405.00    1 of 1   LVP10r1   621   Restoring       420,417,407V 0      0      0     A
23    810   405.00    1 of 1   LVP11r1   621   Restoring       420,417,407V 0      0      0     A
24    810   405.00    1 of 1   LVP5r1    621   Restoring       420,417,407V 0      0      0     A
25    810   405.00    1 of 1   LVP8r1    621   Restoring       420,417,407V 0      0      0     A
----------------------------------------------------------------------------------------------------
26    999   499.50    1 of 1   FLT5r1    0     ### Fault       428,426,424V 0      0      0     A
----------------------------------------------------------------------------------------------------
27    1099  549.50    1 of 1   BRK21_3r1 1000  Tripping        299,298,299V 8405   8531   8359  A
----------------------------------------------------------------------------------------------------
28    1100  550.00    1 of 1   LVP13r1   1001  Tripping        237,240,230V 97     98     98    A
----------------------------------------------------------------------------------------------------
29    1113  556.50    1 of 1   LVP1r1    1014  Tripping        405,401,384V 154    169    140   A
30    1113  556.50    1 of 1   LVP12r1   1014  Tripping        406,402,386V 255    273    235   A
31    1113  556.50    1 of 1   LVP2r1    1014  Tripping        405,401,384V 239    259    219   A
32    1113  556.50    1 of 1   LVP4r1    1014  Tripping        406,402,386V 247    264    228   A
33    1113  556.50    1 of 1   LVP6r1    1014  Tripping        403,399,382V 59     65     53    A
34    1113  556.50    1 of 1   LVP7r1    1014  Tripping        403,399,382V 59     65     53    A
35    1113  556.50    1 of 1   LVP9r1    1014  Tripping        406,402,386V 164    178    151   A
----------------------------------------------------------------------------------------------------
36    1124  562.00    1 of 1   LVP16r1   1025  Tripping        415,425,404V 218    261    230   A
----------------------------------------------------------------------------------------------------
37    1125  562.50    1 of 1   LVP12r1   1014  Restoring       419,431,406V 201    229    135   A
38    1125  562.50    1 of 1   LVP16r1   1025  Restoring       418,423,407V 217    254    226   A
39    1125  562.50    1 of 1   LVP4r1    1014  Restoring       419,431,406V 195    222    130   A
40    1125  562.50    1 of 1   LVP9r1    1014  Restoring       419,431,406V 125    152    85    A
----------------------------------------------------------------------------------------------------
41    1126  563.00    1 of 1   LVP1r1    1014  Restoring       421,428,408V 115    141    79    A
42    1126  563.00    1 of 1   LVP2r1    1014  Restoring       421,428,408V 185    214    126   A
43    1126  563.00    1 of 1   LVP6r1    1014  Restoring       420,427,408V 45     55     31    A
44    1126  563.00    1 of 1   LVP7r1    1014  Restoring       420,427,408V 45     55     31    A
----------------------------------------------------------------------------------------------------
45    1199  599.50    1 of 1   FLT6r1    0     ### Fault       432,430,428V 0      0      0     A
----------------------------------------------------------------------------------------------------
```
]

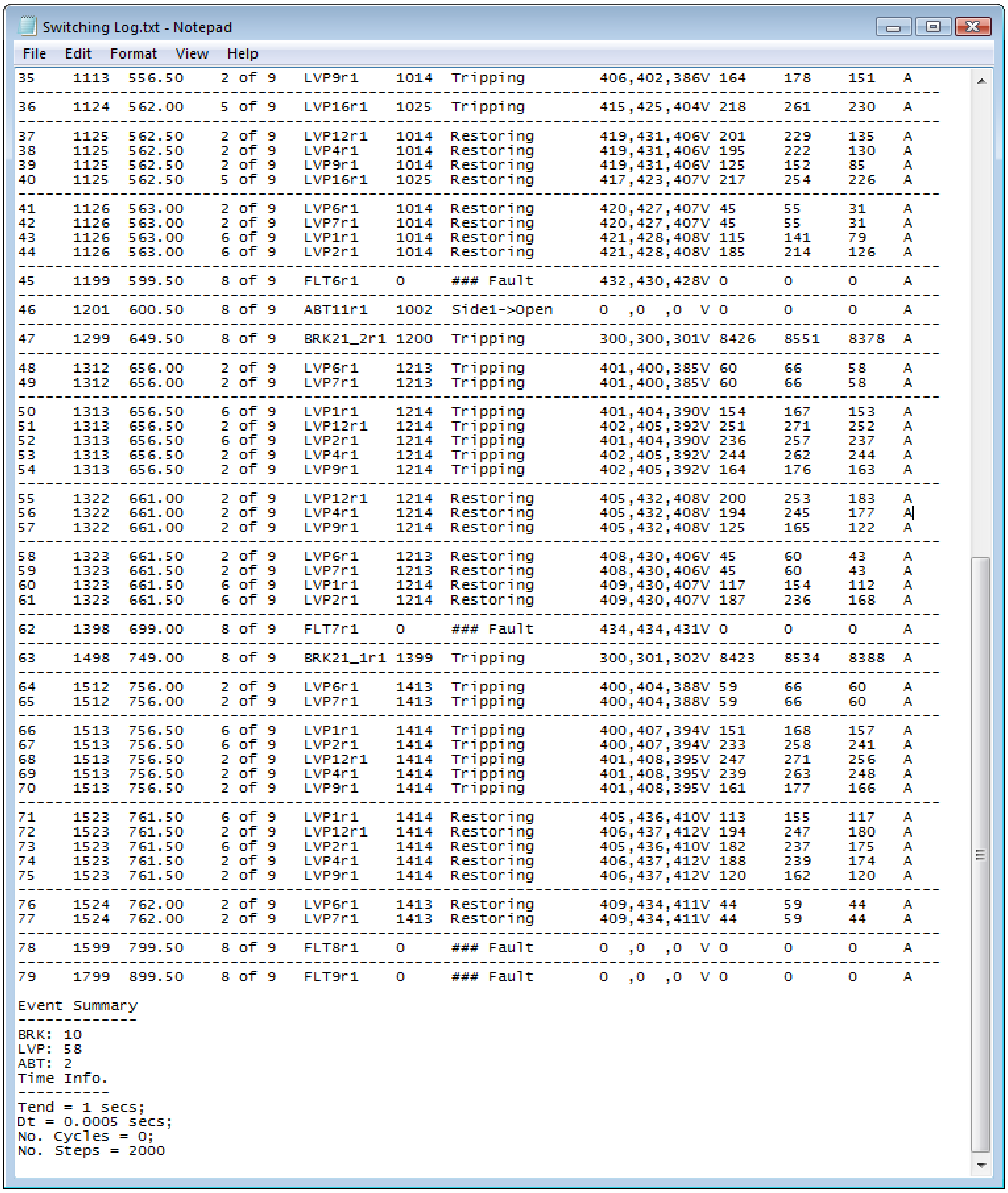


```
35    1113  556.50    1 of 1   LVP9r1    1014  Tripping        406,402,386V 164    178    151   A
----------------------------------------------------------------------------------------------------
36    1124  562.00    1 of 1   LVP16r1   1025  Tripping        415,425,404V 218    261    230   A
----------------------------------------------------------------------------------------------------
37    1125  562.50    1 of 1   LVP12r1   1014  Restoring       419,431,406V 201    229    135   A
38    1125  562.50    1 of 1   LVP16r1   1025  Restoring       418,423,407V 217    254    226   A
39    1125  562.50    1 of 1   LVP4r1    1014  Restoring       419,431,406V 195    222    130   A
40    1125  562.50    1 of 1   LVP9r1    1014  Restoring       419,431,406V 125    152    85    A
----------------------------------------------------------------------------------------------------
41    1126  563.00    1 of 1   LVP1r1    1014  Restoring       421,428,408V 115    141    79    A
42    1126  563.00    1 of 1   LVP2r1    1014  Restoring       421,428,408V 185    214    126   A
43    1126  563.00    1 of 1   LVP6r1    1014  Restoring       420,427,408V 45     55     31    A
44    1126  563.00    1 of 1   LVP7r1    1014  Restoring       420,427,408V 45     55     31    A
----------------------------------------------------------------------------------------------------
45    1199  599.50    1 of 1   FLT6r1    0     ### Fault       432,430,428V 0      0      0     A
----------------------------------------------------------------------------------------------------
46    1201  600.50    1 of 1   ABT11r1   1002  Side1->Open     0  ,0  ,0  V 0      0      0     A
----------------------------------------------------------------------------------------------------
47    1299  649.50    1 of 1   BRK21_2r1 1200  Tripping        300,300,301V 8426   8552   8379  A
----------------------------------------------------------------------------------------------------
48    1312  656.00    1 of 1   LVP6r1    1213  Tripping        401,401,385V 60     66     58    A
49    1312  656.00    1 of 1   LVP7r1    1213  Tripping        401,401,385V 60     66     58    A
----------------------------------------------------------------------------------------------------
50    1313  656.50    1 of 1   LVP1r1    1214  Tripping        401,404,390V 154    167    153   A
51    1313  656.50    1 of 1   LVP12r1   1214  Tripping        402,405,392V 251    271    252   A
52    1313  656.50    1 of 1   LVP2r1    1214  Tripping        401,404,390V 236    257    237   A
53    1313  656.50    1 of 1   LVP4r1    1214  Tripping        402,405,392V 244    262    244   A
54    1313  656.50    1 of 1   LVP9r1    1214  Tripping        402,405,392V 164    176    163   A
----------------------------------------------------------------------------------------------------
55    1322  661.00    1 of 1   LVP12r1   1214  Restoring       405,432,408V 200    253    183   A
56    1322  661.00    1 of 1   LVP4r1    1214  Restoring       405,432,408V 194    245    177   A
57    1322  661.00    1 of 1   LVP9r1    1214  Restoring       405,432,408V 125    165    122   A
----------------------------------------------------------------------------------------------------
58    1323  661.50    1 of 1   LVP1r1    1214  Restoring       409,430,407V 117    154    112   A
59    1323  661.50    1 of 1   LVP2r1    1214  Restoring       409,430,407V 187    236    169   A
60    1323  661.50    1 of 1   LVP6r1    1213  Restoring       408,430,406V 45     60     43    A
61    1323  661.50    1 of 1   LVP7r1    1213  Restoring       408,430,406V 45     60     43    A
----------------------------------------------------------------------------------------------------
62    1398  699.00    1 of 1   FLT7r1    0     ### Fault       434,434,431V 0      0      0     A
----------------------------------------------------------------------------------------------------
63    1498  749.00    1 of 1   BRK21_1r1 1399  Tripping        300,301,302V 8423   8535   8390  A
----------------------------------------------------------------------------------------------------
64    1512  756.00    1 of 1   LVP6r1    1413  Tripping        400,404,388V 59     66     60    A
65    1512  756.00    1 of 1   LVP7r1    1413  Tripping        400,404,388V 59     66     60    A
----------------------------------------------------------------------------------------------------
66    1513  756.50    1 of 1   LVP1r1    1414  Tripping        400,407,394V 151    168    157   A
67    1513  756.50    1 of 1   LVP12r1   1414  Tripping        401,408,395V 247    272    256   A
68    1513  756.50    1 of 1   LVP2r1    1414  Tripping        400,407,394V 233    258    241   A
69    1513  756.50    1 of 1   LVP4r1    1414  Tripping        401,408,395V 239    263    248   A
70    1513  756.50    1 of 1   LVP9r1    1414  Tripping        401,408,395V 160    177    166   A
----------------------------------------------------------------------------------------------------
71    1523  761.50    1 of 1   LVP1r1    1414  Restoring       405,436,410V 113    155    117   A
72    1523  761.50    1 of 1   LVP12r1   1414  Restoring       407,437,412V 194    247    180   A
73    1523  761.50    1 of 1   LVP2r1    1414  Restoring       405,436,410V 182    237    175   A
74    1523  761.50    1 of 1   LVP4r1    1414  Restoring       407,437,412V 188    239    174   A
75    1523  761.50    1 of 1   LVP9r1    1414  Restoring       407,437,412V 120    162    120   A
----------------------------------------------------------------------------------------------------
76    1524  762.00    1 of 1   LVP6r1    1413  Restoring       409,435,411V 44     59     44    A
77    1524  762.00    1 of 1   LVP7r1    1413  Restoring       409,435,411V 44     59     44    A
----------------------------------------------------------------------------------------------------
78    1599  799.50    1 of 1   FLT8r1    0     ### Fault       0  ,0  ,0  V 0      0      0     A
----------------------------------------------------------------------------------------------------
79    1799  899.50    1 of 1   FLT9r1    0     ### Fault       0  ,0  ,0  V 0      0      0     A

Event Summary
-------------
BRK: 10
LVP: 58
ABT: 2
Time Info.
----------
Tend = 1 secs;
Dt = 0.0005 secs;
No. Cycles = 0;
No. Steps = 2000
```

Performance Metric 2: Δt=500μs (p=9)



```
----------------------------------------------------------------------------------------------------
                            Parallel Shipboard Power System Simulator (pSPSS) v1.0
                        Output Log of Fault and Protective Device Switching Events
                                        11/27/2009 8:12:13 PM
----------------------------------------------------------------------------------------------------
Event Step  Time(ms)  Sub      Relay     Det  Action          Vabc (RMS)         Iabc (RMS)
----------------------------------------------------------------------------------------------------
1     199   99.50     9 of 9   FLT1r1    0     ### Fault       433,431,429V 0      0       0     A
----------------------------------------------------------------------------------------------------
2     299   149.50    9 of 9   BRK11_1r1 200   Tripping        308,304,302V 8536   8735    8381  A
----------------------------------------------------------------------------------------------------
3     303   151.50    9 of 9   LVP17r1   204   Tripping        307,337,313V 40     42      40    A
----------------------------------------------------------------------------------------------------
4     330   165.00    9 of 9   LVP17r1   204   Restoring       434,420,407V 22     13      15    A
----------------------------------------------------------------------------------------------------
5     399   199.50    9 of 9   FLT2r1    0     ### Fault       433,431,429V 0      0       0     A
----------------------------------------------------------------------------------------------------
6     499   249.50    9 of 9   BRK11_2r1 400   Tripping        308,304,302V 8536   8735    8381  A
----------------------------------------------------------------------------------------------------
7     503   251.50    9 of 9   LVP17r1   404   Tripping        307,337,313V 40     42      40    A
----------------------------------------------------------------------------------------------------
8     530   265.00    9 of 9   LVP17r1   404   Restoring       434,420,407V 22     13      15    A
----------------------------------------------------------------------------------------------------
9     599   299.50    1 of 9   FLT3r1    0     ### Fault       435,433,431V 0      0       0     A
----------------------------------------------------------------------------------------------------
10    709   354.50    9 of 9   LVP17r1   610   Tripping        364,365,357V 49     49      48    A
----------------------------------------------------------------------------------------------------
11    720   360.00    1 of 9   LVP11r1   621   Tripping        380,393,403V 164    153     172   A
12    720   360.00    1 of 9   LVP5r1    621   Tripping        380,393,403V 6      5       6     A
13    720   360.00    3 of 9   LVP10r1   621   Tripping        380,393,403V 164    153     172   A
14    720   360.00    3 of 9   LVP8r1    621   Tripping        380,393,403V 164    153     172   A
----------------------------------------------------------------------------------------------------
15    799   399.50    1 of 9   BRK1_9r1  600   Tripping        405,402,402V 12743  13117   12659 A
16    799   399.50    8 of 9   FLT4r1    0     ### Fault       370,367,357V 0      0       0     A
----------------------------------------------------------------------------------------------------
17    808   404.00    9 of 9   ABT12r1   609   Side1->Open     336,277,313V 75     105     87    A
----------------------------------------------------------------------------------------------------
18    809   404.50    1 of 9   BRK1_16r1 610   Tripping        419,419,403V 2955   2598    2495  A
19    809   404.50    1 of 9   BRK2_1r1  610   Tripping        427,429,422V 2955   2598    2495  A
----------------------------------------------------------------------------------------------------
20    810   405.00    3 of 9   LVP10r1   621   Restoring       420,417,407V 0      0       0     A
21    810   405.00    5 of 9   BRK3_16r1 611   Tripping        424,425,421V 2640   2285    2312  A
22    810   405.00    3 of 9   LVP8r1    621   Restoring       420,417,407V 0      0       0     A
23    810   405.00    1 of 9   BRK1_1r1  611   Tripping        420,417,407V 2639   2284    2312  A
24    810   405.00    1 of 9   LVP11r1   621   Restoring       420,417,407V 0      0       0     A
25    810   405.00    1 of 9   LVP5r1    621   Restoring       420,417,407V 0      0       0     A
----------------------------------------------------------------------------------------------------
26    999   499.50    8 of 9   FLT5r1    0     ### Fault       428,426,424V 0      0       0     A
----------------------------------------------------------------------------------------------------
27    1099  549.50    8 of 9   BRK21_3r1 1000  Tripping        299,298,299V 8405   8530    8358  A
----------------------------------------------------------------------------------------------------
28    1100  550.00    8 of 9   LVP13r1   1001  Tripping        237,240,230V 97     98      98    A
----------------------------------------------------------------------------------------------------
29    1113  556.50    6 of 9   LVP1r1    1014  Tripping        405,400,384V 154    169     140   A
30    1113  556.50    2 of 9   LVP12r1   1014  Tripping        406,402,386V 255    273     235   A
31    1113  556.50    6 of 9   LVP2r1    1014  Tripping        405,400,384V 239    259     219   A
32    1113  556.50    2 of 9   LVP4r1    1014  Tripping        406,402,386V 247    264     228   A
33    1113  556.50    2 of 9   LVP6r1    1014  Tripping        403,398,382V 59     65      53    A
34    1113  556.50    2 of 9   LVP7r1    1014  Tripping        403,398,382V 59     65      53    A
35    1113  556.50    2 of 9   LVP9r1    1014  Tripping        406,402,386V 164    178     151   A
----------------------------------------------------------------------------------------------------
36    1124  562.00    5 of 9   LVP16r1   1025  Tripping        415,425,404V 218    261     230   A
----------------------------------------------------------------------------------------------------
37    1125  562.50    2 of 9   LVP12r1   1014  Restoring       419,431,406V 201    229     135   A
38    1125  562.50    2 of 9   LVP4r1    1014  Restoring       419,431,406V 195    222     130   A
39    1125  562.50    2 of 9   LVP9r1    1014  Restoring       419,431,406V 125    152     85    A
40    1125  562.50    5 of 9   LVP16r1   1025  Restoring       417,423,407V 217    254     226   A
----------------------------------------------------------------------------------------------------
41    1126  563.00    2 of 9   LVP6r1    1014  Restoring       420,427,407V 45     55      31    A
42    1126  563.00    2 of 9   LVP7r1    1014  Restoring       420,427,407V 45     55      31    A
43    1126  563.00    6 of 9   LVP1r1    1014  Restoring       421,428,408V 115    141     79    A
44    1126  563.00    6 of 9   LVP2r1    1014  Restoring       421,428,408V 185    214     126   A
----------------------------------------------------------------------------------------------------
45    1199  599.50    8 of 9   FLT6r1    0     ### Fault       432,430,428V 0      0       0     A
----------------------------------------------------------------------------------------------------
46    1201  600.50    8 of 9   ABT11r1   1002  Side1->Open     0  ,0  ,0  V 0      0       0     A
```



```
35    1113  556.50    2 of 9   LVP9r1    1014  Tripping        406,402,386V 164    178    151   A
----------------------------------------------------------------------------------------------------
36    1124  562.00    5 of 9   LVP16r1   1025  Tripping        415,425,404V 218    261    230   A
----------------------------------------------------------------------------------------------------
37    1125  562.50    2 of 9   LVP12r1   1014  Restoring       419,431,406V 201    229    135   A
38    1125  562.50    2 of 9   LVP4r1    1014  Restoring       419,431,406V 195    222    130   A
39    1125  562.50    2 of 9   LVP9r1    1014  Restoring       419,431,406V 125    152    85    A
40    1125  562.50    5 of 9   LVP16r1   1025  Restoring       417,423,407V 217    254    226   A
----------------------------------------------------------------------------------------------------
41    1126  563.00    2 of 9   LVP6r1    1014  Restoring       420,427,407V 45     55     31    A
42    1126  563.00    2 of 9   LVP7r1    1014  Restoring       420,427,407V 45     55     31    A
43    1126  563.00    6 of 9   LVP1r1    1014  Restoring       421,428,408V 115    141    79    A
44    1126  563.00    6 of 9   LVP2r1    1014  Restoring       421,428,408V 185    214    126   A
----------------------------------------------------------------------------------------------------
45    1199  599.50    8 of 9   FLT6r1    0     ### Fault       432,430,428V 0      0      0     A
----------------------------------------------------------------------------------------------------
46    1201  600.50    8 of 9   ABT11r1   1002  Side1->Open     0  ,0  ,0  V 0      0      0     A
----------------------------------------------------------------------------------------------------
47    1299  649.50    8 of 9   BRK21_2r1 1200  Tripping        300,300,301V 8426   8551   8378  A
----------------------------------------------------------------------------------------------------
48    1312  656.00    2 of 9   LVP6r1    1213  Tripping        401,400,385V 60     66     58    A
49    1312  656.00    2 of 9   LVP7r1    1213  Tripping        401,400,385V 60     66     58    A
----------------------------------------------------------------------------------------------------
50    1313  656.50    6 of 9   LVP1r1    1214  Tripping        401,404,390V 154    167    153   A
51    1313  656.50    2 of 9   LVP12r1   1214  Tripping        402,405,392V 251    271    252   A
52    1313  656.50    6 of 9   LVP2r1    1214  Tripping        401,404,390V 236    257    237   A
53    1313  656.50    2 of 9   LVP4r1    1214  Tripping        402,405,392V 244    262    244   A
54    1313  656.50    2 of 9   LVP9r1    1214  Tripping        402,405,392V 164    176    163   A
----------------------------------------------------------------------------------------------------
55    1322  661.00    2 of 9   LVP12r1   1214  Restoring       405,432,408V 200    253    183   A
56    1322  661.00    2 of 9   LVP4r1    1214  Restoring       405,432,408V 194    245    177   A
57    1322  661.00    2 of 9   LVP9r1    1214  Restoring       405,432,408V 125    165    122   A
----------------------------------------------------------------------------------------------------
58    1323  661.50    2 of 9   LVP6r1    1213  Restoring       408,430,406V 45     60     43    A
59    1323  661.50    2 of 9   LVP7r1    1213  Restoring       408,430,406V 45     60     43    A
60    1323  661.50    6 of 9   LVP1r1    1214  Restoring       409,430,407V 117    154    112   A
61    1323  661.50    6 of 9   LVP2r1    1214  Restoring       409,430,407V 187    236    168   A
----------------------------------------------------------------------------------------------------
62    1398  699.00    8 of 9   FLT7r1    0     ### Fault       434,434,431V 0      0      0     A
----------------------------------------------------------------------------------------------------
63    1498  749.00    8 of 9   BRK21_1r1 1399  Tripping        300,301,302V 8423   8534   8388  A
----------------------------------------------------------------------------------------------------
64    1512  756.00    2 of 9   LVP6r1    1413  Tripping        400,404,388V 59     66     60    A
65    1512  756.00    2 of 9   LVP7r1    1413  Tripping        400,404,388V 59     66     60    A
----------------------------------------------------------------------------------------------------
66    1513  756.50    6 of 9   LVP1r1    1414  Tripping        400,407,394V 151    168    157   A
67    1513  756.50    6 of 9   LVP2r1    1414  Tripping        400,407,394V 233    258    241   A
68    1513  756.50    2 of 9   LVP12r1   1414  Tripping        401,408,395V 247    271    256   A
69    1513  756.50    2 of 9   LVP4r1    1414  Tripping        401,408,395V 239    263    248   A
70    1513  756.50    2 of 9   LVP9r1    1414  Tripping        401,408,395V 161    177    166   A
----------------------------------------------------------------------------------------------------
71    1523  761.50    6 of 9   LVP1r1    1414  Restoring       405,436,410V 113    155    117   A
72    1523  761.50    2 of 9   LVP12r1   1414  Restoring       406,437,412V 194    247    180   A
73    1523  761.50    6 of 9   LVP2r1    1414  Restoring       405,436,410V 182    237    175   A
74    1523  761.50    2 of 9   LVP4r1    1414  Restoring       406,437,412V 188    239    174   A
75    1523  761.50    2 of 9   LVP9r1    1414  Restoring       406,437,412V 120    162    120   A
----------------------------------------------------------------------------------------------------
76    1524  762.00    2 of 9   LVP6r1    1413  Restoring       409,434,411V 44     59     44    A
77    1524  762.00    2 of 9   LVP7r1    1413  Restoring       409,434,411V 44     59     44    A
----------------------------------------------------------------------------------------------------
78    1599  799.50    8 of 9   FLT8r1    0     ### Fault       0  ,0  ,0  V 0      0      0     A
----------------------------------------------------------------------------------------------------
79    1799  899.50    8 of 9   FLT9r1    0     ### Fault       0  ,0  ,0  V 0      0      0     A

Event Summary
-------------
BRK: 10
LVP: 58
ABT: 2
Time Info.
----------
Tend = 1 secs;
Dt = 0.0005 secs;
No. Cycles = 0;
No. Steps = 2000
```

VITA

Fabian Marcel Uriarte obtained his B.S. and M.S. in electrical engineering from Virginia Tech in July 2002 and December 2003, respectively and his Ph.D. in electrical engineering from Texas A&M University in May 2010. His research interests are in modeling and simulation of power systems and power electronics, parallel computational methods, and object-oriented programming.

Dr. Uriarte was recognized with the following awards as a doctoral student:

- An Alfred P. Sloan Foundation Graduate Scholarship in December 2004
- 3rd place at Texas A&M University Student Research Week's (SRW) oral presentation sessions in May 2005
- 2nd best graduate student poster at the IEEE Transmission and Distribution (T&D) Conference in Dallas, TX in May 2006
- A travel grant to present a research paper on current transformer saturation at the Ph.D. Research in Microelectronics (PRIME) conference in Otranto, Italy in June 2006
- 1st place research paper presentation at the North American Power Symposium (NAPS) student conference held in Carbondale, IL in September 2006
- 1st place at Texas A&M University Student Research Week's (SRW) oral presentation sessions in March 2008

Dr. Uriarte can be reached at the Department of Electrical and Computer Engineering at Texas A&M University, College Station, TX 77843-3128. His email address is: fabian@tamu.edu.