DESIGN OF A LOW POWER 70MHZ-110MHZ HARMONIC REJECTION FILTER WITH CLASS-AB OUTPUT STAGE

A Thesis

by

SHAN HUANG

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2010

Major Subject: Electrical Engineering

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ABSTRACT

Design of A Low Power 70MHz-110MHz Harmonic Rejection Filter with Class-AB Output Stage. (May 2010)

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An FM transmitter becomes the new feature in recent portable electronic development. A low power, integrable FM transmitter filter IC is required to meet the demand of FM transmitting feature. A low pass filter using harmonic rejection technique along with a low power class-AB output buffer is designed to meet the current market requirements on the FM transmitter chip.

A harmonic rejection filter is designed to filter FM square wave signal from 70MHz to 110MHz into FM sine wave signal. Based on Fourier series, the harmonic rejection technique adds the phase shifted square waves to achieve better THD and less high frequency harmonics. The phase shifting is realized through a frequency divider, and the summation is implemented through a current summation circuit. A RC low pass filter with automatic tuning is designed to further attenuate unwanted harmonics. In this work, the filter's post layout simulation shows -53dB THD and harmonics above 800MHz attenuation of -99dB. The power consumption of the filter is less than 0.7mW.

Output buffer stage is implemented through a resistor degenerated transconductor and a class-AB amplifier. Feedforward frequency compensation is applied to

compensate the output class-AB stage, which extends the amplifier's operating bandwidth. A fully balanced class-AB driver is proposed to unleash the driving capability of common source output transistors. The output buffer reaches -43dB THD at 110MHz with 0.63Vpp output swing and drives 1mW into 50Ω load. The power consumption of the output buffer is 7.25mW.

By using harmonic rejection technique, this work realizes the 70MHz-110MHz FM carrier filtering using TSMC 0.18um nominal process. Above 800MHz harmonics are attenuated to below -95dB. With 1.2V supply, the total power consumption including output buffer is 7.95mW. The total die area is 0.946mm^2.

DEDICATION

To Mom and Dad

ACKNOWLEDGEMENTS

I would like to thank my mother Yang Xu and father Fei Huang for their endless support and great encouragement throughout my early education and my pursuit of this degree. I am forever grateful for their personal sacrifice toward my education and career development.

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CHAPTER I

INTRODUCTION

1.1 The Motivation and Background of the Research

Nowadays many portable electronic devices are equipped with MP3 music play capability. One of the problems in these portable devices is that people have to use a pair of earphones or headset. Most often, the music could only be enjoyed by one single person at a time. A pair of external speakers could help solve the problem, but the extra wiring and the size of the equipment make speakers less popular. In fact, many people would like to enjoy music from their MP3 players while driving. The conventional way of using MP3 players in car is to use an adapter which transfers the music to either the AUX input or the cassette player of a car. However, it is usually inconvenient to connect and disconnect MP3 players. In addition, many cars are not equipped with AUX inputs and cassette players. In fact, 90% of cars manufactured after year 2000 are only equipped with CD player and FM/AM radio. So, FM radios become an obvious choice for broadcasting music from portable devices. FM transmitter converts the audio output from a MP3 player into an FM radio signal, which can then be picked up by in-car radios. There are FM transmitters for portable device application available in the market. The size of a typical transmitter is comparable to an MP3 player. Some FM transmitters use power directly from the MP3 player's battery, which shortens the device music

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This thesis follows the style of *IEEE Journal of Solid-State Circuits.*

playback time. The size and power prevent transmitters from integrating into mobile devices. A power efficient and integrable FM transmitter is needed.

In December 2008, Broadcom Corp rolled out 802.11n, Bluetooth, FM transmitter and receiver in handset chip, which is the first to integrate these receiving and transmitting capabilities. Broadcom stated that it is the smallest dual-band Wi-Fi device and it has the lowest power consumption. Texas Instruments also has a competing chip that integrates Wi-Fi, Bluetooth, and FM transmitter and receiver. It has been shown that the current market demands FM transmitter circuit for mobile devices with low power consumption and integrable capability.

1.2 Research Goals

In this work, a low power and integrated low-pass filter for FM signal with a high performance Class-AB buffer stage is designed as shown in Figure 1.

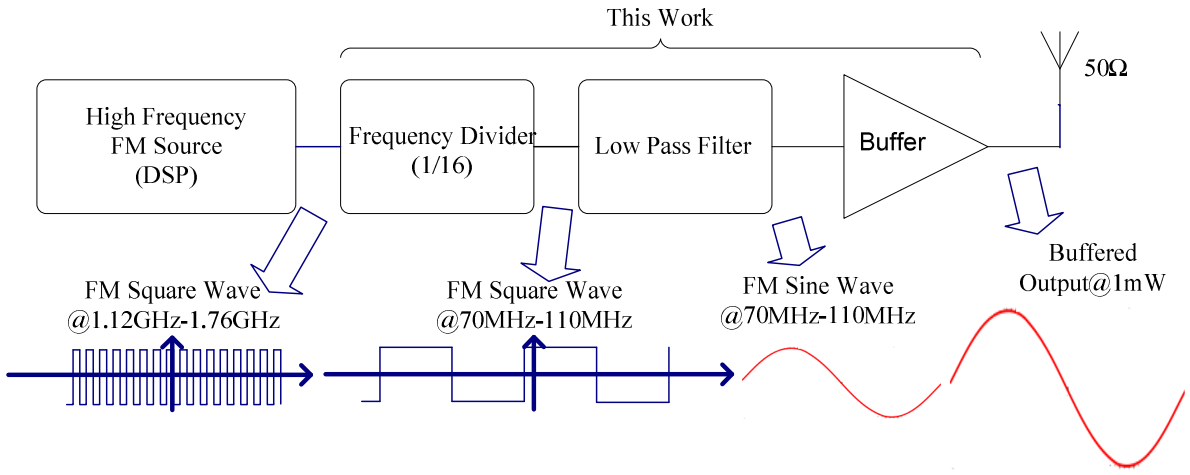

Figure 1 FM transmitter system level architecture

The first objective of this research is to design a low-pass filter that can remove harmonics of a square wave FM signal with 70MHz-110MHz carrier frequency and attenuate its high frequency harmonics (above 800MHz) by 110dB. The FM signal is obtained through a divide-by-16 frequency divider. The undivided FM signal of 1.12GHz to 1.76GHz is generated from DSP block. Attenuation of harmonics above 800MHz is required to eliminate their interference in RF band. The second objective is to minimize the power consumption. This work is going to be used in handheld device. Minimizing power consumption is the key value for this work. The filter power consumption is aimed at 0.5mW. The third objective is to design an efficient buffer stage that drives The filtered FM signal into a 50Ω resistive load at 0.63Vpp and consumes no more than 1.5mW. The ultimate goal of this project is to realize an integrated ultra low power FM transmitter for handheld devices. The detailed specifications are listed in Table 1.

Table 1 Specifications of the FM filter

Parameter	Min	Nom	Max
Supply Voltage	1V	1.2V	1.4V
FM Carrier Frequency	70MHz		110MHz
Frequency Deviation		100KHz	
SNR	65dB	70dB	
Attenuation above 800MHz	110dB		
Power Consumption		2mW	3mW
THD(Both carrier and signal)			46dB
Settling Time			50ms
Load		50Ω	
Output Power		1mW	
Technology		TSMC 0.18um	

1.3 Thesis Organization

This thesis consists of eight chapters. Chapter II will discuss basic filter design and operational amplifier design. The harmonic rejection concept will be discussed in Chapter III including proposed system level architecture. Chapter IV will cover the harmonic rejection circuit. Chapter V will focus on RC low pass filter and the automatic tuning circuit. In Chapter VI, transimpedance output buffer stage will be discussed and analyzed. Chapter VII will discuss post layout simulation results. Finally, Chapter VIII will draw some conclusions based on the research presented and propose some future research directions.

CHAPTER II

GENERAL DESIGN CONSIDERATIONS OF TRADITIONAL FILTER AND AMPLIFIER

2.1 General Design Considerations of Traditional Filter

A high performance filter and a high performance output buffer are the key building blocks of this research. Many design aspects such as linearity, high frequency attenuation, power consumption, tunability, etc. have to be taken into consideration.

2.1.1 Total Harmonic Distortion and High Frequency Harmonic Attenuation

THD is the ratio of the sum of the powers of all harmonics to the power of the fundamental signal, and it is usually expressed in dB. Typically, only the first few harmonics are significant.

$$THD = 10\log\left(\frac{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 \ldots}{V_f^2}\right) \tag{2.1}$$

A square wave contains odd number of harmonics, where 3rd, 5th, 7th and 9th affect THD most. Square wave THD is given by

$$THD = 10\log\left(\frac{V_3^2 + V_5^2 + V_7^2 + V_9^2 + \cdots}{V_f^2}\right) \tag{2.2}$$

For THD to be less than -46dB, the highest V_3 signal level is calculated by

$$THD = 10\log\left(\frac{V_3^2 + V_5^2 + V_7^2 + V_9^2 + \cdots}{V_f^2}\right) < -46dB \tag{2.3}$$

$$\frac{V_3^2 + V_5^2 + V_7^2 + V_9^2 + \cdots}{V_f^2} < 10^{-46dB/10} \tag{2.4}$$

$$V_3 < -46dB \tag{2.5}$$

where V_5, V_7, V_9 etc are assumed to be at lower signal level of V_3. FM square wave's third harmonic level is at -9.54dB compared to fundamental signal. It is desired to be attenuated by 36.5dB in order to meet THD requirement. So, a low pass filter with pass-band at 110MHz and stop-band at 210MHz with attenuation of 180dB per decade is needed. 110MHz is the highest input fundamental frequency, and 210MHz is the lowest third harmonic frequency. Figure 2 illustrates the filter specifications. The solid line is the desired low pass filter ac response curve based on THD requirement. Attenuation of high frequency harmonics reduces the interference to the adjacent systems such as Bluetooth, 802.11n Rx/Tx. For the harmonics above 800MHz, a low pass filter with pass-band at 110MHz and stop-band at 800MHz with 130dB per decade attenuation is needed. In Figure 2, the dashed line shows the desired filter attenuation level across frequency.

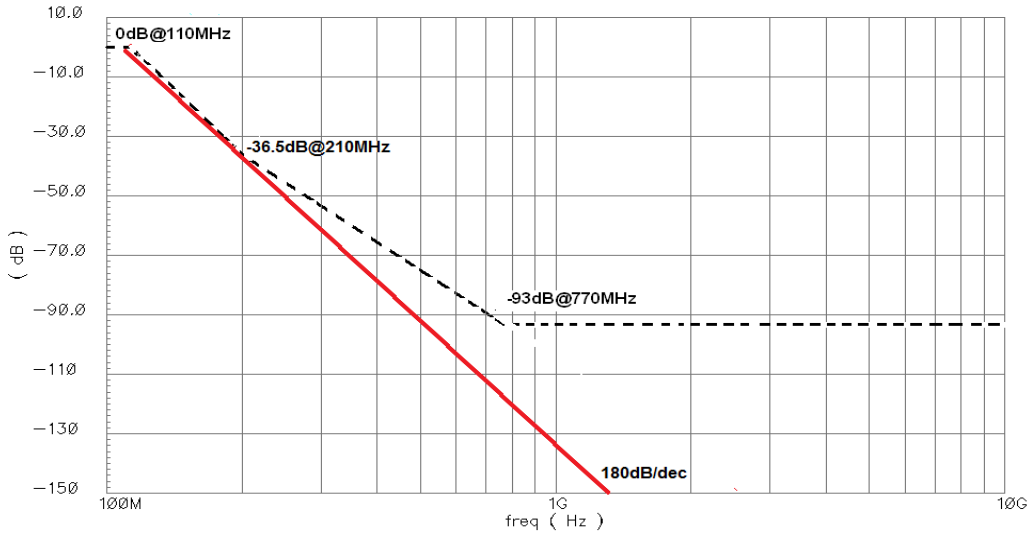

Figure 2 Filter specifications in frequency domain

Table 2 shows the low pass filter's desired attenuation specification based on the FM signal's THD and high frequency harmonic level specifications with respect to each FM harmonic tone. Filter's attenuation at 3^{rd}-7^{th} harmonic is based on THD specification. In order to meet THD requirement, the attenuation of 3^{rd}, 5^{th}, and 7^{th} harmonics should be more than 36.5dB. Filter's attenuation above 9^{th} harmonic is based on FM signal's harmonic attenuation specification. For 9^{th}, 11^{th} and higher harmonics, the attenuation has to be greater than 90dB.

Table 2 Specifications of FM filter on each harmonic tone

Harmonic	Frequency	FM Signal Level	Spec. Level	Desired Filter Attenuation
1^{st}	70MHz-110MHz	0dB	0dB	0dB
3^{rd}	210MHz-330MHz	-9.54dB	-46dB	36.5dB
5^{th}	350MHz-550MHz	-13.98dB	<-46dB	36.5dB
7^{th}	490MHz-770MHz	-16.90dB	<-46dB	36.5dB
9^{th}	630MHz-990MHz	-19.08dB	<-110dB	90dB
11^{th} and up	770MHz-1.21GHz and up	-20.83dB	<-110dB	90dB

2.1.2 Filter Order

The order of the filter is estimated based on the specification. The pass band frequency is 110MHz. The pass band ripple is not given in the specification explicitly, but it is expected to be small and estimated to be 1.5dB. The stop band frequency is at 800MHz and its attenuation is 90dB as shown in Table 2. Based on the specification, the filter order using Butterworth response is calculated as

$$n = \frac{log\left(\frac{10^{0.1\alpha_{min}} - 1}{10^{0.1\alpha_{max}} - 1}\right)}{2log\left(\frac{\omega_s}{\omega_p}\right)} = 5.4 \approx 6 \tag{2.6}$$

where ω_p is the pass band frequency, ω_s is the stop band frequency, α_{min} is the stop band minimum attenuation, and α_{max} is the pass band maximum ripple. The filter order using Chebyshev response is calculated as

$$n = \frac{\cosh^{-1}\sqrt{\left(\frac{10^{0.1\alpha_{min}} - 1}{10^{0.1\alpha_{max}} - 1}\right)}}{\cosh^{-1}\left(\frac{\omega_s}{\omega_p}\right)} = 4.3 \approx 5 \tag{2.7}$$

2.1.3 Group Delay

Group delay is particularly important for pulse transmission in digital domain. Group delay variation causes signal distortion during transmission. In this research, although FM carrier square wave signal contains several frequency components with 100KHz deviation from the carrier, this square wave is not transmitted to the output, only the fundamental tone is passed through. For the FM 100KHz deviation, the frequency range is small enough that the group delay variation is insignificant. Therefore, group delay is not the main concern in this research.

2.1.4 Passive vs. Active Filter

Passive filters consist of resistors, inductors, and capacitors, minimizing power consumption and providing very high linearity. Due to the higher cost of inductor fabrication, in this work, passive filter design is limited to passive RC filter. The

absolute value of passive devices in modern IC technology is heavily process dependent. One way to minimize the process variation is to use tuning circuit.

Active filters use active components such as amplifiers, transconductance cells along with passive elements to realize filter function. Power consumption and linearity are the two main issues for active filter. For a low pass active RC filter operating at 110MHz, its op-amp's power consumption could easily exceed the total power budget. Therefore, it is not a suitable filter type for this work. A 5th order Gm-C filter operating at 110MHz with rail-to-rail input signal swing has both linearity and power problems [1]. Switched-capacitor filter, as another type of active filters, is widely used. However, its op-amp's dc gain, unity-gain frequency, and slew rate requirements at 110MHz operating frequency affect the practical implementation of switched-capacitor technique. Thereby, it could not be implemented in this work either.

Table 3 shows the performance comparison of 5 basic filter types. In terms of power consumption, signal linearity, chip area and tuning requirement, passive RC low pass filter is the most suitable type for this research. It consumes minimum amount of power, introduces minimum amount of distortion, and occupies reasonable amount of chip area. However, passive RC low pass filter is heavily process dependent. A tuning circuit is required in order to implement a realistic RC low pass filter. The design of a low pass filter with automatic tuning will be discussed in Chapter V.

Table 3 Comparison of different filter types

Filter Type	Power	Linearity	Area	Frequency	Tuning
RC Passive	None	High	***Large***	High	Required
Gm-C	Medium	***LOW***	Medium	Medium	Required
Active RC	***High***	Medium	Medium	Medium	Required
RLC Passive	None	High	***Giant***	High	Required
Switched-Cap	***High***	Medium	Medium	***Low***	Not Required

2.1.5 Tunability and Tuning Method

FM carrier signal frequency is from 70MHz-110MHz. It is more efficient to design a tunable filter which follows FM signal's carrier frequency. Without tunability, the low pass filter's cut-off frequency has to be designed at 110MHz and it has to attenuate harmonics at 800MHz down to -110dB, resulting in over designed filter. Furthermore, for a continuous time filter, process, voltage and temperature variations could reduce the accuracy of these design parameters. For this reason, a tuning circuit is also required to compensate these variations.

2.2 General Design Considerations of Output Buffer

2.2.1 Class-AB Output Buffer

The output signal is delivered into a 50Ω antenna load with -46dB THD. An output buffer stage is desired to provide sufficient output power and to avoid distorting signal. One way to drive a low resistive load is to use a Class A output stage, which is shown in Figure 3(a). The efficiency of the Class A amplifier is calculated as

$$Efficiency = \frac{Power_{deliver}}{Power_{supply}} = \left(\frac{V_{OUT}(peak)}{V_{DD} - V_{SS}}\right)^2 \tag{2.8}$$

where the maximum value of V_{out}(peak) is the half of the supply voltage. Although the linearity is good for Class A amplifier, its maximum efficiency is only 25%. Alternatively, Class B can be used to deliver power onto low resistive load shown in Figure 3(b). Class B amplifier has better efficiency through controlling push-pull common source stage which conducts half of the signal period. The efficiency of a Class B amplifier is given by

$$Efficiency = \frac{Power_{deliver}}{Power_{supply}} = \frac{\pi}{2}\frac{V_{out}(peak)}{V_{DD} - V_{SS}} \tag{2.9}$$

where the maximum efficiency is 78.5% with the largest V_{out}(peak). However Class B amplifier shows crossover distortion. In order to improve linearity and maintain good efficiency, Class-AB amplifier is used in this research, where the output transistors conduct current during the entire signal period. Class-AB efficiency is between Class A and Class B. The design of Class-AB output stage is discussed in Chapter VI.

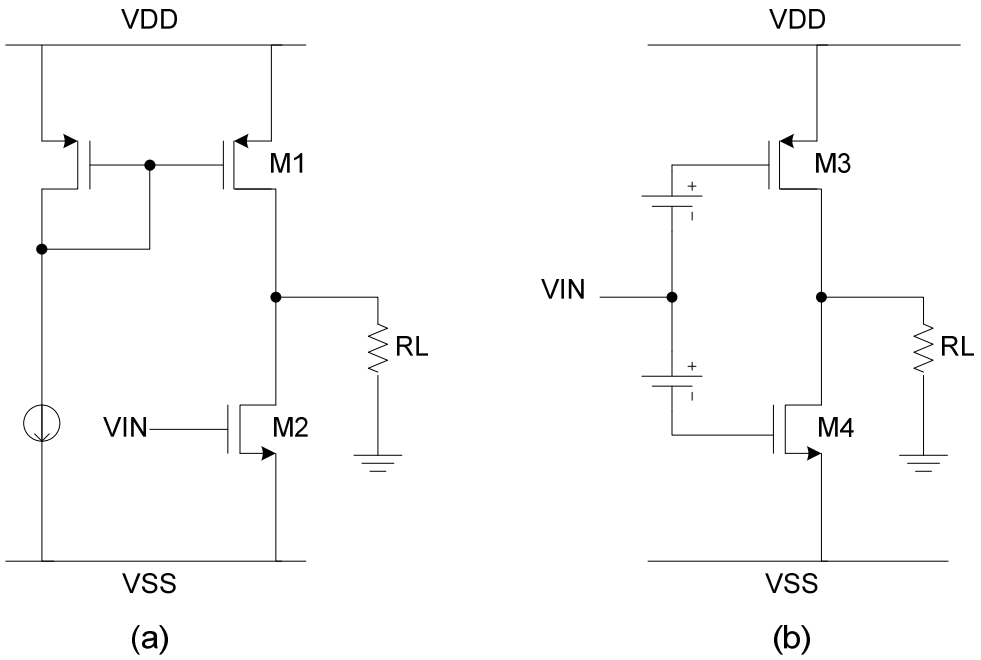

Figure 3 (a) Common source class A amplifier (b) push-pull class B or class-AB amplifier

2.2.2 Open Loop or Closed Loop

Open loop output buffer consumes less power than its equivalent closed loop output buffer. Due to the lack of feedback loop, it does not operate linearly especially for large signal swing and its output gain is process dependent. For the output signal's linearity consideration, closed loop output buffer is chosen.

2.2.3 High Frequency Output Buffer Issue

Closed loop Class-AB buffer operating at 110MHz frequency is challenging to design. For example, 40dB dc gain with 110MHz bandwidth is translated into 10GHz GBW, which is impossible to implement in 0.18um technology. Most of the output

buffer stages are designed in sub 10MHz operating range. However, with a good compensation scheme [2], an op-amp could operate at 110MHz with GBW in 1GHz range. Table 4 summarizes the general specifications for the output buffer stage.

Table 4 Output buffer stage specifications

Buffer Specifications	
Output load	50Ω
Output Power	1mW
Output Swing	0.63Vpp
Operating Frequency	70MHz-110MHz
Output THD	-46dB
Supply Voltage	1.2V
Slew Rate	140V/us
Power Consumption	1.5mW

CHAPTER III

HARMONIC REJECTION TECHNIQUE

3.1 Harmonic Rejection Method

The unique feature of this research is that input FM signal is a square wave. One way to filter this FM signal is to use harmonic rejection technique. Other applications of this method have been reported in mixer design and oscillator design [3] [4].

3.1.1 45º Phase Shift Harmonic Rejection

Basically, square waves could be added together with certain phase shifts and different amplitudes to eliminate some of the square wave's harmonics. Figure 4 shows harmonic rejection method graphically. All square waves should have the same frequency. P_2 and P_3 have to be shifted by 45º and 90º, respectively, and P_2 is amplified by $\sqrt{2}$. All three square waves P_1, P_2, and P_3 are added together to remove 3^{rd} and 5^{th} harmonics.

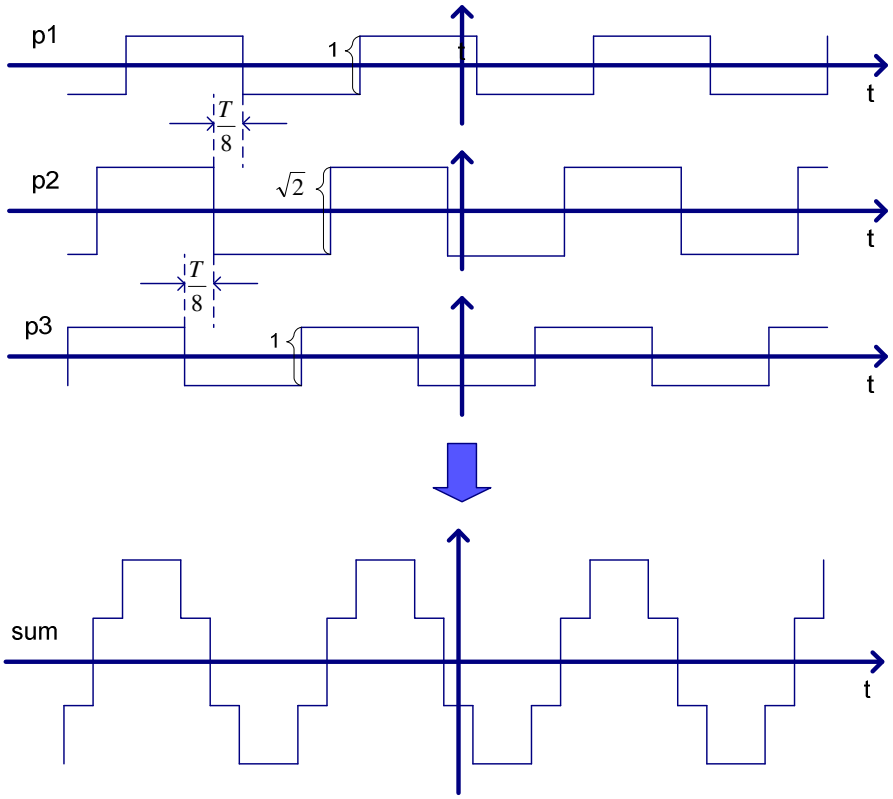

Figure 4 45° phase shift harmonic rejection method

Mathematically, the square wave can be expressed as

$$\text{square wave} = \frac{4}{\pi}\sum_{n}^{\infty}\frac{1}{n}\sin(n\omega t) \quad n=\text{odd} \tag{3.1}$$

P_1, P_2, and P_3 can be expressed as,

$$P_1(t) = \frac{4}{\pi}\sum_{n}^{\infty}\frac{1}{n}\sin\left(n\omega t + n\frac{\pi}{4}\right) \tag{3.2}$$

$$P_2(t) = \frac{4\sqrt{2}}{\pi}\sum_{n}^{\infty}\frac{1}{n}\sin(n\omega t) \tag{3.3}$$

$$P_3(t) = \frac{4}{\pi}\sum_{n}^{\infty}\frac{1}{n}\sin\left(n\omega t - n\frac{\pi}{4}\right) \tag{3.4}$$

where P_1, P_2, and P_3 are three individual 45 ° phase shifted square waves. They can also be expanded into

$$P_1(t) = \frac{4}{\pi}\left\{\sin\left(\omega t + \frac{\pi}{4}\right) + \frac{1}{3}\sin\left(3\omega t + 3\frac{\pi}{4}\right) + \frac{1}{5}\sin\left(5\omega t + 5\frac{\pi}{4}\right) + \frac{1}{7}\sin\left(7\omega t + 7\frac{\pi}{4}\right) + \ldots\right\} \tag{3.5}$$

$$P_2(t) = \frac{4\sqrt{2}}{\pi}\left\{\sin(\omega t + 0) + \frac{1}{3}\sin(3\omega t + 3 * 0) + \frac{1}{5}\sin(5\omega t + 5 * 0) + \frac{1}{7}\sin(7\omega t + 7 * 0) + \ldots\right\} \tag{3.6}$$

$$P_3(t) = \frac{4}{\pi}\left\{\sin\left(\omega t - \frac{\pi}{4}\right) + \frac{1}{3}\sin\left(3\omega t - 3\frac{\pi}{4}\right) + \frac{1}{5}\sin\left(5\omega t - 5\frac{\pi}{4}\right) + \frac{1}{7}\sin\left(7\omega t - 7\frac{\pi}{4}\right) + \ldots\right\} \tag{3.7}$$

where P_1 square wave can be further expanded into,

$$P_1(t) = \frac{4}{\pi}\Big\{\sin(\omega t)\cos\left(\frac{\pi}{4}\right) + \cos(\omega t)\sin\left(\frac{\pi}{4}\right) + \frac{1}{3}\sin(3\omega t)\cos\left(3\frac{\pi}{4}\right) + \frac{1}{3}\cos(3\omega t)\sin\left(3\frac{\pi}{4}\right) + \frac{1}{5}\sin(5\omega t)\cos\left(5\frac{\pi}{4}\right) + \frac{1}{5}\cos(5\omega t)\sin\left(5\frac{\pi}{4}\right) + \frac{1}{7}\sin(7\omega t)\cos\left(7\frac{\pi}{4}\right) + \frac{1}{7}\cos(7\omega t)\sin\left(7\frac{\pi}{4}\right) + \ldots\Big\} \tag{3.8}$$

$$P_1(t) = \frac{4}{\pi} * \frac{1}{\sqrt{2}}\Big\{\sin(\omega t) + \cos(\omega t) - \frac{1}{3}\sin(3\omega t) + \frac{1}{3}\cos(3\omega t) - \frac{1}{5}\sin(5\omega t) - \frac{1}{5}\cos(5\omega t) + \frac{1}{7}\sin(7\omega t) - \frac{1}{7}\cos(7\omega t) + \ldots\Big\} \tag{3.9}$$

P_3 is again expanded into,

$$P_3(t) = \frac{4}{\pi}\Big\{\sin(\omega t)\cos\left(\frac{\pi}{4}\right) - \cos(\omega t)\sin\left(\frac{\pi}{4}\right) + \frac{1}{3}\sin(3\omega t)\cos\left(3\frac{\pi}{4}\right) - \frac{1}{3}\cos(3\omega t)\sin\left(3\frac{\pi}{4}\right) + \frac{1}{5}\sin(5\omega t)\cos\left(5\frac{\pi}{4}\right) - \frac{1}{5}\cos(5\omega t)\sin\left(5\frac{\pi}{4}\right) + \frac{1}{7}\sin(7\omega t)\cos\left(7\frac{\pi}{4}\right) - \frac{1}{7}\cos(7\omega t)\sin\left(7\frac{\pi}{4}\right) + \ldots\Big\} \tag{3.10}$$

$$P_3(t) = \frac{4}{\pi} * \frac{1}{\sqrt{2}}\Big\{\sin(\omega t) - \cos(\omega t) - \frac{1}{3}\sin(3\omega t) - \frac{1}{3}\cos(3\omega t) - \frac{1}{5}\sin(5\omega t) + \frac{1}{5}\cos(5\omega t) + \frac{1}{7}\sin(7\omega t) + \frac{1}{7}\cos(7\omega t) + \ldots\Big\} \tag{3.11}$$

All three phase shifted square waves are added together as

$$Sum = P_1(t) + P_2(t) + P_3(t) \tag{3.12}$$

where the sum of these three square waves contains only 7th, 9th, 15th, 17th, etc harmonics. The 3rd and 5th harmonics are mathematically cancelled. The sum of the square waves can be expressed as,

$$Sum = \frac{8\sqrt{2}}{\pi}\Big\{\sin(\omega t) + \frac{1}{7}\sin(7\omega t) + \frac{1}{9}\sin(9\omega t) + \frac{1}{15}\sin(15\omega t) + \frac{1}{17}\sin(17\omega t) \ldots\Big\} \tag{3.13}$$

45° phase shift harmonic rejection technique improves FM carrier THD value and reduces some harmonics. However, 7th, 9th harmonics with amplitude about -20dB are still untouched. Removing those harmonics will require a 120dB/dec low pass filter. Designing a 120dB/dec low pass filter with good linearity and low power consumption is not a trivial task. Based on the aforementioned issues, it has been shown that 45° phase shift harmonic does not meet the specifications in this research.

3.1.2 22.5 º Phase Shift Harmonic Rejection

22.5 º phase shift harmonic rejection technique could be used to remove 3rd, 5th, 7th, 9th, 11th and 13th harmonics. It generates smaller THD and lowers high frequency harmonics better than the 45º phase shift harmonic rejection technique. With the cancellation of higher frequency harmonics which are not cancelled by 45º phase shift harmonic rejection filter, only a 60dB/dec low pass filter is needed instead of a 120dB/dec low pass filter. To realize a 22.5º harmonic rejection filter, seven shifted square waves are needed. Each square wave has its own weighting factor with 22.5º phase shift to each other. Each phase shifted square wave can be expressed as

$$P_1(t) = k_1 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t - n\frac{3\pi}{8}\right) \tag{3.14}$$

$$P_2(t) = k_2 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t - n\frac{2\pi}{8}\right) \tag{3.15}$$

$$P_3(t) = k_3 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t - n\frac{\pi}{8}\right) \tag{3.16}$$

$$P_4(t) = k_4 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin(n\omega t) \tag{3.17}$$

$$P_5(t) = k_5 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t + n\frac{\pi}{8}\right) \tag{3.18}$$

$$P_6(t) = k_6 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t + n\frac{2\pi}{8}\right) \tag{3.19}$$

$$P_7(t) = k_7 \frac{4}{\pi} \sum_{n}^{\infty} \frac{1}{n} \sin\left(n\omega t + n\frac{3\pi}{8}\right) \tag{3.20}$$

where k_1-k_7 are square waves' magnitudes or weighting factors. The weighting factor for each of the square wave can be expressed as

$$k_1 = \frac{1}{2}\left[\sin\left(\frac{7}{16}\right) - \sin\left(\frac{5}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{3}{8}\pi\right) \tag{3.21}$$

$$k_2 = \frac{1}{2}\left[\sin\left(\frac{5}{16}\right) - \sin\left(\frac{3}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{1}{4}\pi\right) \tag{3.22}$$

$$k_3 = \frac{1}{2}\left[\sin\left(\frac{3}{16}\right) - \sin\left(\frac{1}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{1}{8}\pi\right) \tag{3.23}$$

$$k_4 = \sin\left(\frac{1}{16}\pi\right)\cos(0) \tag{3.24}$$

$$k_5 = \frac{1}{2}\left[\sin\left(\frac{7}{16}\right) - \sin\left(\frac{5}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{3}{8}\pi\right) \tag{3.25}$$

$$k_6 = \frac{1}{2}\left[\sin\left(\frac{5}{16}\right) - \sin\left(\frac{3}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{1}{4}\pi\right) \tag{3.26}$$

$$k_7 = \frac{1}{2}\left[\sin\left(\frac{3}{16}\right) - \sin\left(\frac{1}{16}\right)\right] = \sin\left(\frac{1}{16}\pi\right)\cos\left(\frac{1}{8}\pi\right) \tag{3.27}$$

where k_1=k_7, k_2=k_6, and k_3=k_5. The summation of these seven square waves is given as

$$Sum = P_1 + P_2 + P_3 + P_4 + P_5 + P_6 + P_7 \tag{3.28}$$

$$Sum = \frac{4}{\pi}\left\{\sin(\omega t) + \frac{1}{15}\sin(15\omega t) + \frac{1}{17}\sin(17\omega t) + \frac{1}{31}\sin(31\omega) + \frac{1}{33}\sin(33\omega) + \cdots\right\} \tag{3.29}$$

It has been shown that it is possible to completely cancel certain harmonics of a square wave. The capability of this harmonic cancellation aligns perfectly with the THD specification and higher frequency harmonics attenuation requirement. Using this

method also has the benefit of very low power consumption. Compared with 45º harmonic rejection, it further relaxes the design margin for the next stage low pass filter, which reduces the low pass filter attenuation requirement. It is identified as a better option than 45º phase shift harmonic rejection technique.

3.2 System Level Verification of FM Signal Harmonic Rejection Filter

3.2.1 Harmonic Rejection Behavioral Model

Behavioral model was built in Cadence to show the harmonic rejection technique. Transient simulation and FFT results of the harmonic rejection behavioral model output signal are shown in Figure 5 and Figure 6. With 22.5º phase shift, 3rd-13th harmonics are all cancelled out perfectly.

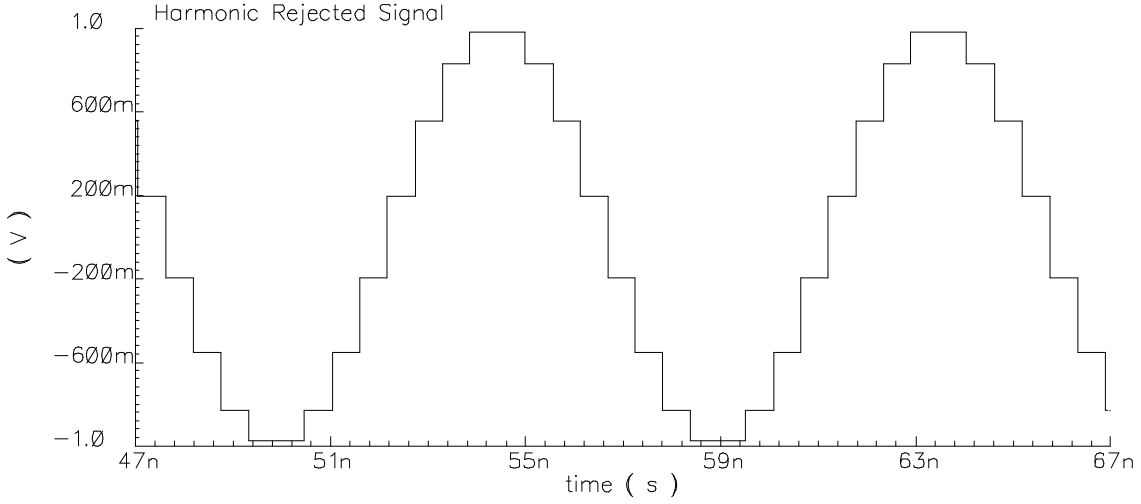

Figure 5 Transient simulation of the 22.5º harmonic rejection behavioral model output signal

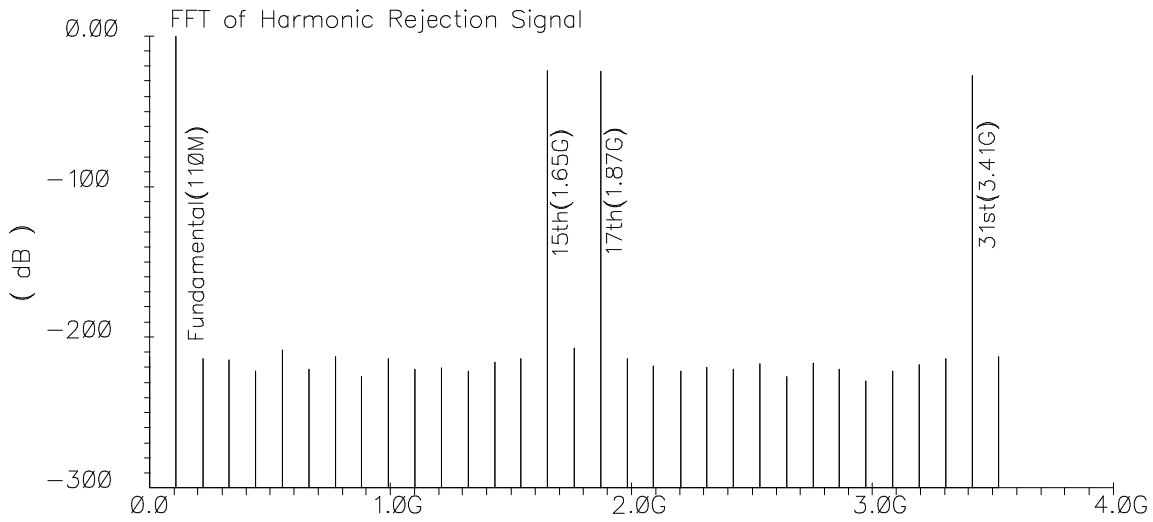

Figure 6 FFT of the 22.5º harmonic rejection behavioral model output signal

3.2.2 FM Signal Demodulation

A system level Matlab model was written to verify harmonic rejection filter's effect on FM signal (Appendix A). The system level architecture is illustrated in Figure 7. 110MHz FM square wave signal is first created in Matlab. Then, harmonic rejection technique is applied to the FM wave. An ideal brick wall low pass filter function is used during the simulation to model the RC low pass filter effect. The FM signal is demodulated using Matlab built-in FM demodulator function. The simulation result in Figure 8 shows the demodulated 1MHz signal from 110MHz FM signal. This simulation verifies that the harmonic rejection circuit can preserve an FM signal. Due to the size of simulation data and the simulation time, 1MHz modulating signal frequency and 1MHz

deviation frequency are chosen instead of 1KHz modulating signal and 100KHz deviation in the specification.

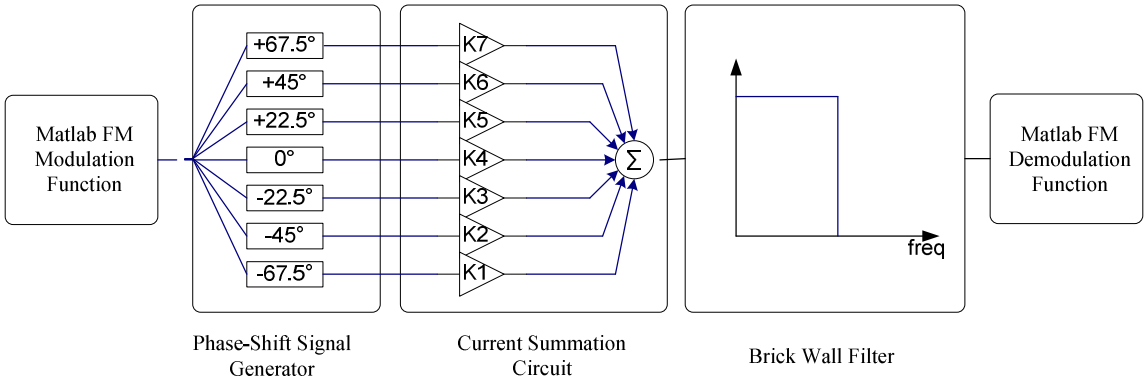

Figure 7 Block diagram of harmonic rejection filter

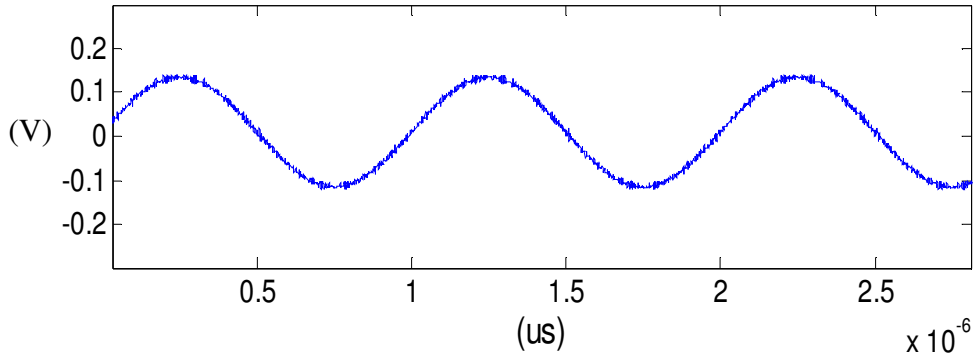

Figure 8 Demodulated FM signal using harmonic rejection filter in Matlab simulation

3.2.3 Non-ideal Effects Verification

In actual circuit realization, the weighting factors k_1-k_7 are implemented through CMOS current sources. Small mismatches among these current sources affect the

performance of harmonic rejection. The mismatch is modeled in Matlab to simulate the non-ideal effect on the harmonic rejection circuit (Appendix B).

The spectrum of a square wave contains the fundamental frequency and odd harmonics. For 22.5º harmonic rejection, seven shifted and scaled square waves are added together. It is the output of the current summation circuit as shown in Figure 7. The output f(t) is expressed as

$$fs(t) = square\ wave = \frac{4}{\pi}\sum_{n}^{\infty}\frac{1}{n}\sin(n\omega t)\ \ n = odd \tag{3.30}$$

$$\begin{aligned} f(t) = {} & k_3 fs(t - t_d) + k_5 fs(t + t_d) + k_2 fs(t - 2t_d) + k_6 fs(t + 2t_d) \\ & + k_1 fs(t - 3t_d) + k_7 fs(t + 3t_d) + k_4 fs \end{aligned} \tag{3.31}$$

where t_d is the square wave timing delay which is 1/16 of the square wave period. For $k_{1,7}=k_1=k_7$, $k_{2,6}= k_2=k_6$, and $k_{3,5}=k_3=k_5$, the above equation becomes

$$\begin{aligned} f(t) = {} & k_{3,5} fs(t - t_d) + k_{3,5} fs(t + t_d) + k_{2,6} fs(t - 2t_d) \\ & + k_{2,6} fs(t + 2t_d) + k_{1,7} fs(t - 3t_d) + k_{1,7} fs(t + 3t_d) \\ & + k_4 fs \end{aligned} \tag{3.32}$$

Fourier transform of (3.32) yields

$$\begin{aligned} F(\omega) &= H(\omega)F_s(\omega) \\ &= \left[k_4 + 2k_{3,5}\cos(t_d\omega) + 2k_{2,6}\cos(2t_d\omega)\right. \\ &\quad \left. + 2k_{1,7}\cos(3t_d\omega)\right]F_s(\omega) \end{aligned} \tag{3.33}$$

$$\begin{aligned} H(\omega) &= \frac{F(\omega)}{F_s(\omega)} \\ &= \left[k_4 + 2k_{3,5}\cos(t_d\omega) + 2k_{2,6}\cos(2t_d\omega)\right. \\ &\quad \left. + 2k_{1,7}\cos(3t_d\omega)\right] \end{aligned} \tag{3.34}$$

where $F_s(\omega)$ is the Fourier transform of the square wave $fs(t)$. $H(\omega)$ is the transfer function for 22.5º harmonic rejection. To obtain the nth harmonic rejection magnitude transfer function, In $H(\omega)$, ω could be replaced by $n\omega_0$. Here, n represents the number of harmonics, ω_0 is used as the fundamental frequency, and $n\omega_o$ represents nth harmonic frequency. Harmonic rejection happens when $H(\omega)$ is equal to zero. Harmonic rejection magnitude transfer function are shown as follows

$$\begin{aligned} H((2n+1)\omega_0) \\ &= k_4 + 2\left(k_{3,5}\right)\cos(t_d(2n+1)\omega_0) \\ &+ 2\left(k_{2,6}\right)\cos(2t_d(2n+1)\omega_o) \\ &+ 2(k_{1,7})\cos(3t_d(2n+1)\omega_0) \quad \text{n} = 1, 2, 3, 4, \ldots \end{aligned} \tag{3.35}$$

In order to estimate non ideality, 2% current source mismatch is added into the ideal weighing factors k_1-k_7. Assuming k_1-k_7 are considered as seven uncorrelated random current sources, each individual current source's standard deviation can be calculated as follows:

$$\sigma_{k1-k7} = 2\% = \sqrt{\sigma_{k1}^2 + \sigma_{k2}^2 + \sigma_{k3}^2 + \sigma_{k4}^2 + \sigma_{k5}^2 + \sigma_{k6}^2 + \sigma_{k7}^2} \tag{3.36}$$

$$\sigma_{k1} = \sigma_{k2} = \sigma_{k3} = \sigma_{k4} = \sigma_{k5} = \sigma_{k6} = \sigma_{k7} = 0.76\% \tag{3.37}$$

Since k_1=k_7, k_2=k_6, and k_3=k_5, the combined current sources standard deviation can be calculated as follows:

$$\sigma_{k1,7} = \sqrt{\sigma_{k1}^2 + \sigma_{k7}^2} = 1.07\% \tag{3.38}$$

$$\sigma_{k2,6} = \sqrt{\sigma_{k2}^2 + \sigma_{k6}^2} = 1.07\% \tag{3.39}$$

$$\sigma_{k3,5} = \sqrt{\sigma_{k3}^2 + \sigma_{k5}^2} = 1.07\% \tag{3.40}$$

Harmonic rejection magnitude transfer function with non ideal weighting factors are expressed as

$$\begin{aligned} H((2n+1)\omega_0) &= (k_4 + \Delta k_4) + 2\left(k_{3,5} + \Delta k_{3,5}\right)\cos(t_d(2n+1)\omega_0) \\ &+ 2\left(k_{2,6} + \Delta k_{2,6}\right)\cos(2t_d(2n+1)\omega_o) + 2(k_{1,7} \\ &+ \Delta k_{1,7})\cos(3t_d(2n+1)\omega_0) \\ &\text{n=1, 2, 3, 4 …} \end{aligned} \tag{3.41}$$

Using Matlab random function, the value for each rejected harmonic coefficient (3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th}, and 13^{th} harmonic) is calculated and plotted in Figure 9. These histograms show the harmonic tone rejection level with 2% standard deviation among current sources (weighting factors) assuming square wave's phase shifts are ideal. Each figure shows the statistical distribution of nth harmonic tone's rejected level in the presence of current source mismatch with 10,000 test runs.

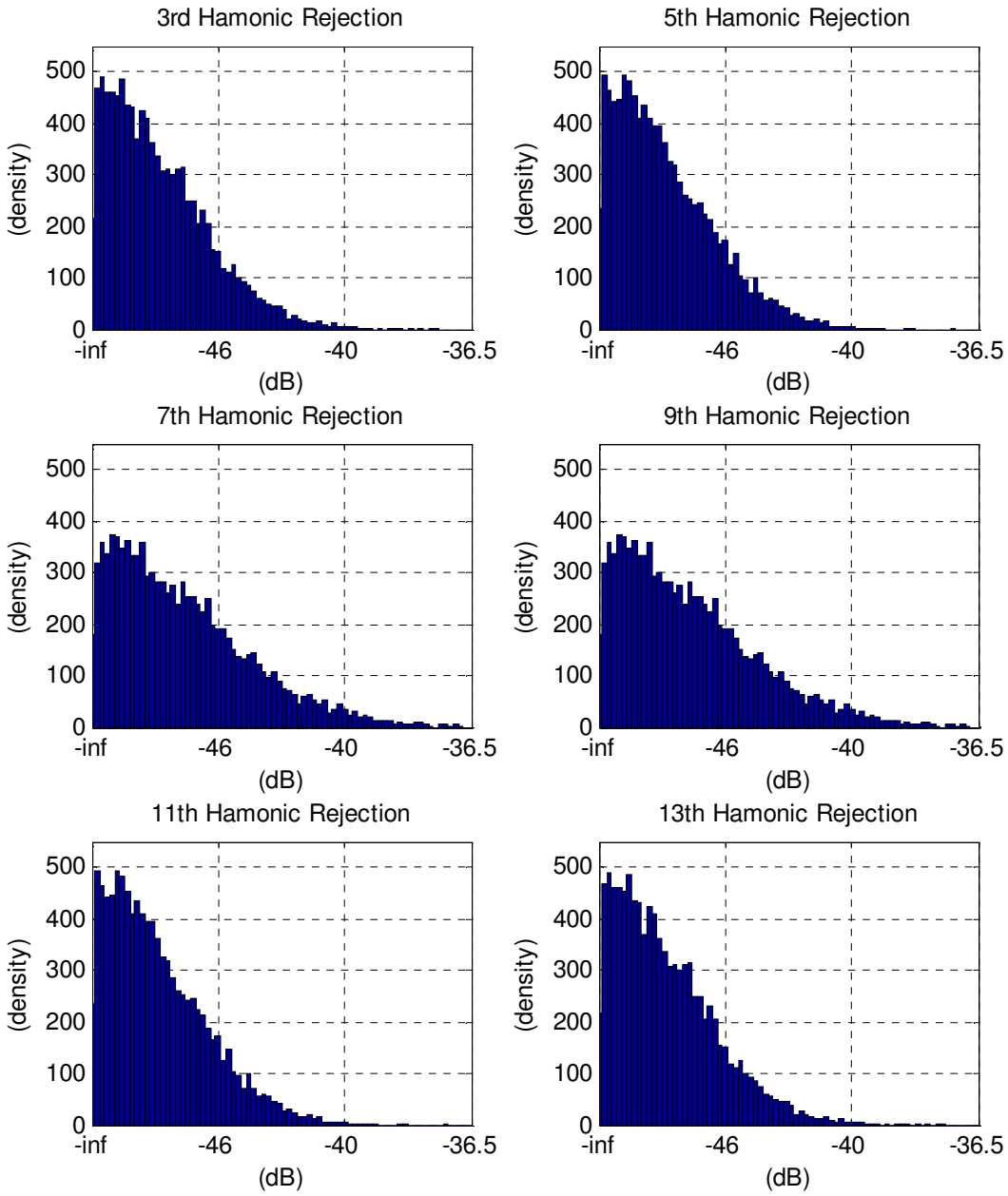

Figure 9 Nth harmonic tone's rejection level histograms in the presence of current source mismatch

Table 5 List of estimated harmonic tone's rejection level within three σ current source mismatch

Within Two Sigma	
Harmonic Tone	Rejection Level
3rd	-43.6dB or less
5th	-43.6dB or less
7th	-41.1dB or less
9th	-41.1dB or less
11th	-43.6dB or less
13th	-43.6dB or less

Table 5 shows each harmonic tone's rejection level within two σs. It has been shown that within two sigma or 97% chance harmonics from 3^{rd} to 13^{th} are rejected by at least 41dB. In Figure 10, Matlab is used to plot the worst case harmonic transfer function with 2% standard deviation among square wave weighting factors. After 4000 runs, odd harmonics 3^{rd}-13^{th} could be attenuated at least by 37-40dB.

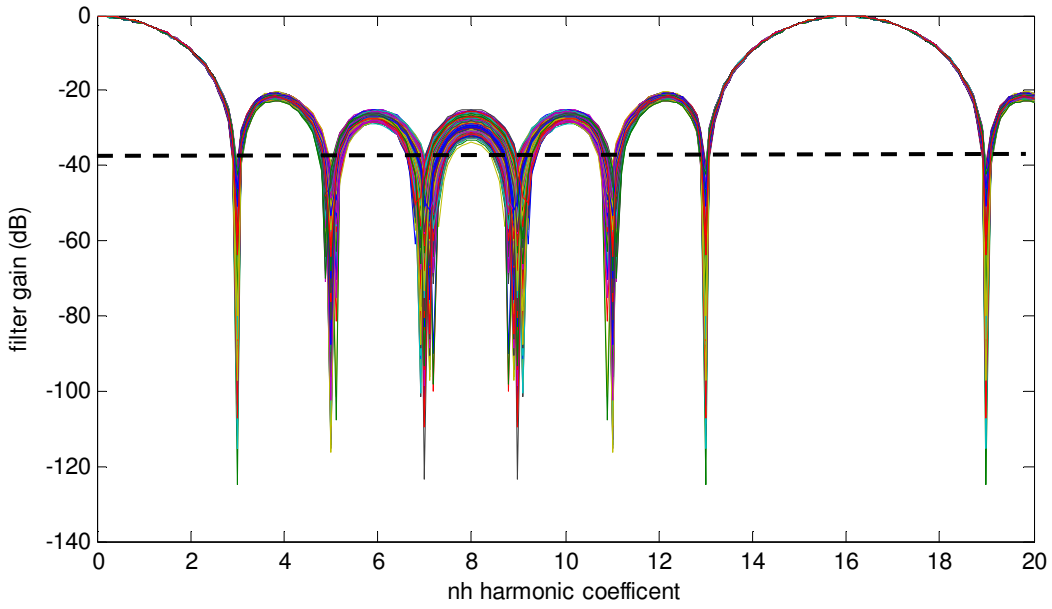

Figure 10 Worst case harmonic transfer function with 2% standard deviation

The phase error (or timing error) is also modeled through Matlab with 0.5% standard deviation among all seven square waves. Figure 11 shows the non-ideality histograms of harmonic tone rejection level with 0.5% standard deviation among timing mismatch and 1% standard deviation among current sources (weighting factors). Each figure shows the statistical distribution of each harmonic tone's rejection level in the presence of timing shift mismatch and current source mismatch with 10,000 runs.

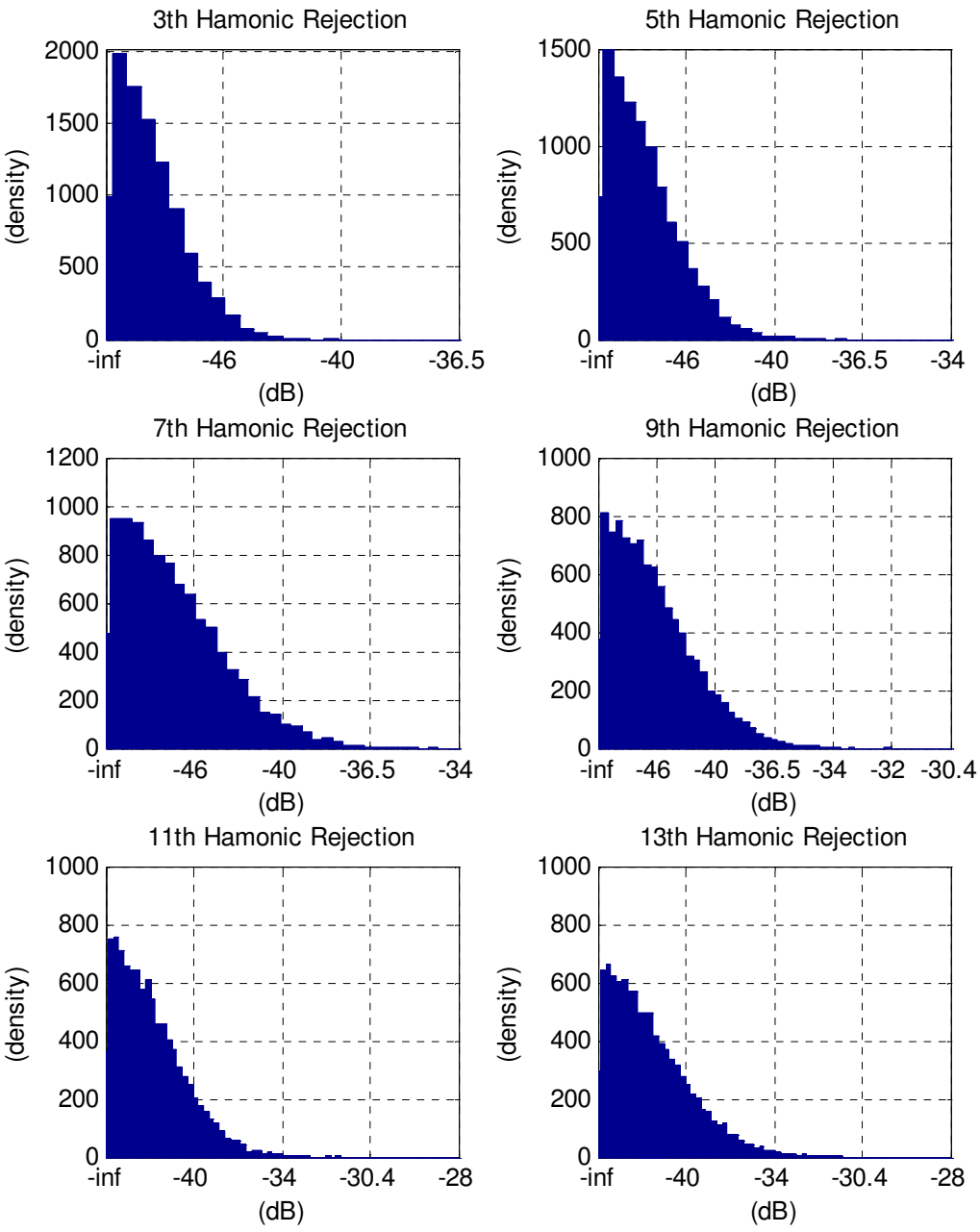

Figure 11 Nth harmonic tone's rejection coefficient value histograms in the presence of timing mismatch and current source mismatch

Table 6 shows rejection level of each harmonic tone within two σ. It shows that with 97% chance 3rd and 5th harmonics are rejected by at least -46dB and -43.7dB respectively. With timing mismatch, the higher frequency harmonics get less rejected. This is due to the smaller time period at high frequency. So, for 7th, 9th, and 11th harmonics, within two sigma or 97% chance, they are rejected by 36dB.

.

Table 6 List of estimated harmonic rejection level within two σ timing mismatch

Within Two Sigma	
Harmonic	Rejection Level
3rd	-46.4dB or less
5th	-43.6dB or less
7th	-40.4dB or less
9th	-38.6dB or less
11th	-37.7dB or less
13th	-36.4dB or less

Although harmonics may not be perfectly cancelled and rejection depends on circuit matching, attenuation of 30dB-40dB on signal's harmonics, greatly improves the signal's linearity and lowers the higher frequency harmonics. This result indicates that harmonic rejection concept is a feasible solution. Matlab simulation validates this concept for FM signal filtering. System level harmonic rejection architecture is proposed in the section 3.3.

3.3 Proposed Harmonic Rejection Scheme

The proposed system level harmonic rejection filter is shown in Figure 12. The whole system consists of a phase-shift signal generator, a current summation circuit, a RC filter, and an output buffer.

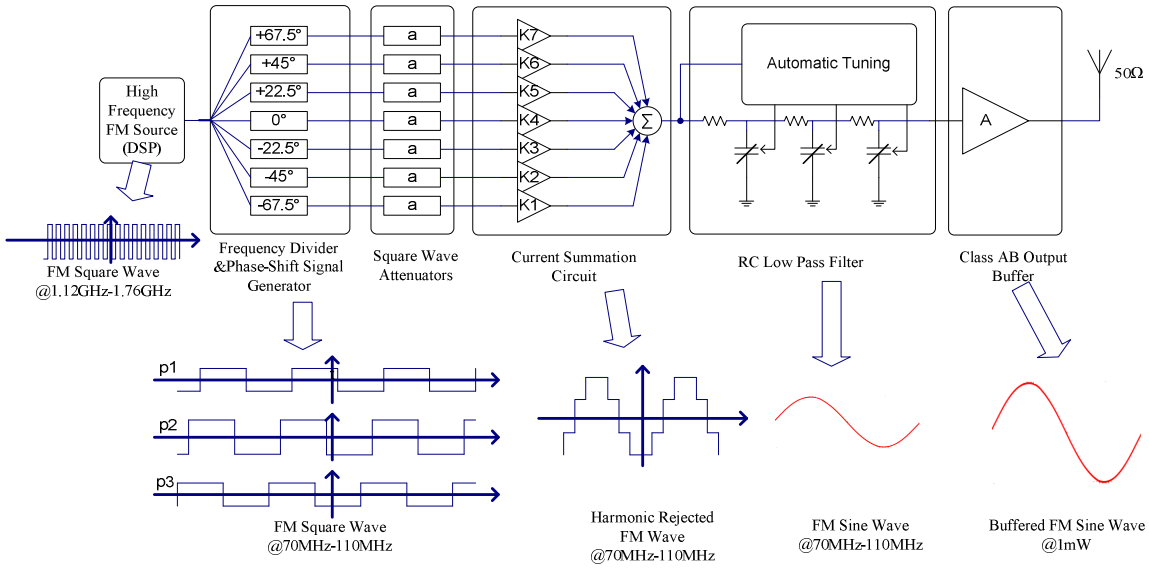

Figure 12 Proposed system level harmonic rejection filter

3.3.1 Phase-shift Signal Generator

A phase-shift signal generator could be built to generate phase shifted square waves from 70MHz to 110MHz. The phase-shift signal generator should track the input signal frequency independent of process, voltage and temperature. A delay lock loop scheme could be used to generate required phase shifts [5]. A conventional frequency divider is used in this research. Its design will be discussed in Chapter IV.

3.3.2 Current Summation Block

A summation circuit can be built to add phase shifted square waves together. Adding voltage is neither very easy nor accurate. However, current could be added relatively easy. A current summation circuit could be built using a traditional current steering circuit as shown in Figure 13.

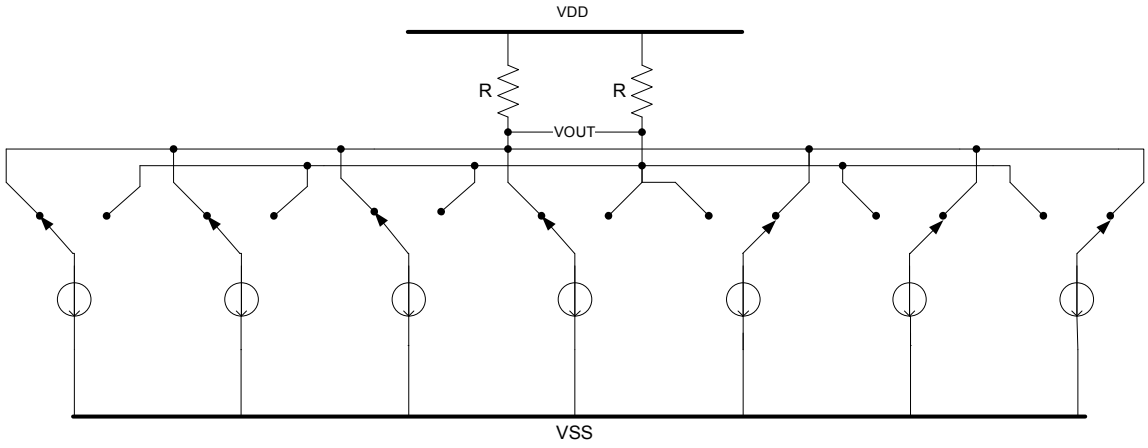

Figure 13 Current summation circuit

The phase shift square waves are used as switches' control signals. The weighting factors are generated by dc current values. Currents are added and loaded onto a resistor. The detailed circuit realization will be discussed in Chapter IV.

3.3.3 RC Filter

A passive low pass RC filter as shown in Figure 14 can be used to attenuate un-cancelled 15th and 17th harmonics. RC low pass filter does not introduce any distortion and does not consume power. In addition, RC low pass filter further attenuates any

unwanted harmonics which are not totally cancelled due to circuit mismatch. However, RC passive filter's time constant deviates considerably from the design value due to process variation. Both resistor's and capacitor's value can be ±15% away from design parameters. The estimated overall time constant variation is ±25%. Therefore, automatic-tuning circuit is needed for this RC low pass filter. RC filter with automatic tuning design will be presented in Chapter V.

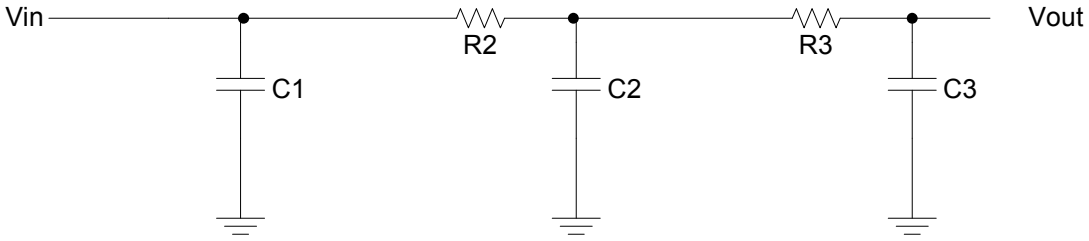

Figure 14 RC low pass filter

3.3.4 Output Buffer

An output buffer is needed to drive the filtered sine wave onto 50Ω resistive load delivering 1mW power. A balanced Class-AB output stage is designed. In order to maintain signal linearity, the output stage operates in closed loop as shown in Figure 15. The design of output buffer will be discussed in Chapter VI.

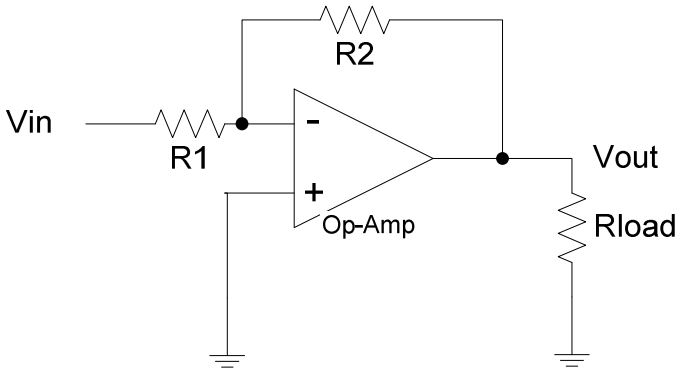

Figure 15 Output buffer stage

CHAPTER IV

HARMONIC REJECTION FILTER

4.1 DLL Harmonic Rejection

Delay Locked Loop shown in Figure 16 has been widely used to change the phase of a clock signal in a digital circuit. Compared to PLL, DLL is a first-order loop without an oscillator. A DLL compares the phase of its output to the input clock to generate an error signal which is then integrated and fed back to control all of the delay elements. The integration allows the error to go to zero while keeping the control signal, and thus the delays, where they need to be for phase lock. Since it is first-order feedback loop, it is inherently stable. It could be used as a phase shift generator. FM signal is in digital domain which could act as a clock signal for DLL. DLL also tracks FM signal from 70MHz to 110MHz along with 100 KHz deviation. At the same time, it generates a set of phase shift signals ready for the harmonic rejection process.

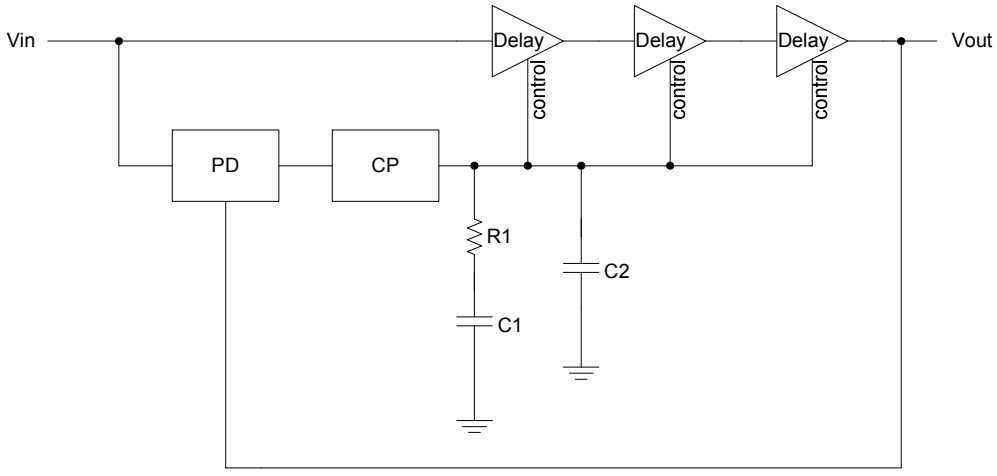

Figure 16 Block diagram of delay lock loop

However, delay element design is crucial for the performance of DLL [6]. Although the total phase shift from the first delay element to the last delay element is very well controlled, the phase shifts from delay elements may not be evenly distributed. Since the function of delay element is based on RC time constant, the phase shift (delay) for each delay element is circuit design, process, and supply voltage variation dependent. Any variation among delay elements creates inaccurate phase shift. The total phase shift is given by

$$\begin{aligned} Total\ Phase\ Shift\ (180^0) &= (22.5^0 + \Delta 1) + (22.5^0 + \Delta 2) + (22.5^0 + \Delta 3) \\ &+ (22.5^0 + \Delta 4) + (22.5^0 + \Delta 5) + (22.5^0 + \Delta 6) \\ &+ (22.5^0 + \Delta 7) + (22.5^0 + \Delta 8) \end{aligned} \tag{4.1}$$

where $\Delta 1$- $\Delta 7$ are the delay mismatch. With the fixed total phase shift, a single delay element's delay variation will induce delay variations among other delay elements. Due to the delay accuracy performance concern, the delay lock loop is not an ideal candidate for harmonic rejection technique application.

4.2 Digital Frequency Divider

The traditional frequency divider divides the frequency of 1.12GHz-1.76GHz down to 70MHz-110MHz as shown in Figure 17. It does not provide phase shifted square waves.

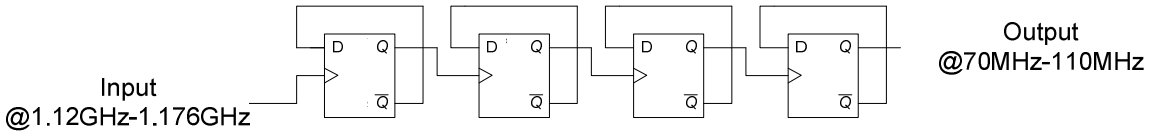

Figure 17 Conventional divider circuit topology

In order to realize harmonic rejection filter, frequency divider shown in Figure 18 is used. This digital circuit provides better phase shift accuracy than DLL. The phase shift is generated through dividing input clock, but in DLL the phase depends on RC time constant. Therefore, the digital frequency divider is less sensitive across process, voltage, and temperature.

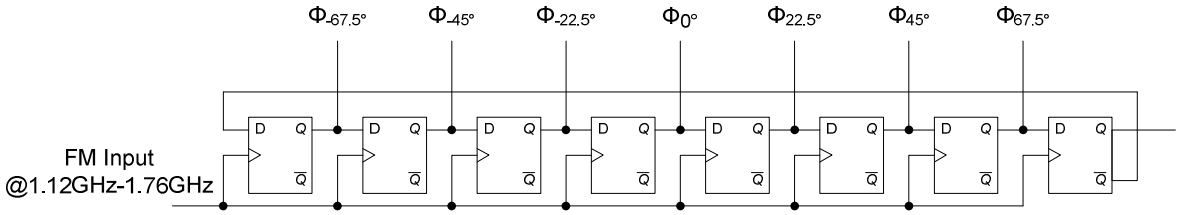

Figure 18 Phase shifted frequency divider

4.2.1 D Flip-flop Circuit Implementation

D flip-flop is the basic building block of synchronous circuits [7]. Figure 19 shows a non-inverting static flip flop. However, at high clock frequency, a pair of non-overlapping clocks is required for its operation. Also, the outputs of the flip-flops are not true differential signals. There is always one inverting delay between Q and $\bar{Q}$.

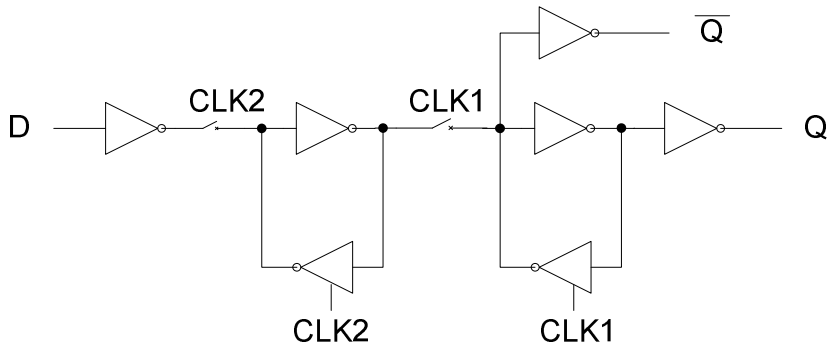

Figure 19 Conventional static flip-flop [7]

Differential flip-flop takes complementary inputs and produce true complementary outputs. A sense amplifier is built into the flip flop to respond to small differential input rapidly. It is better than conventional static flip flop in terms of true differential outputs. However, due to its complexity, voltage headroom and speed limitation, it is not suitable for this research.

Conventional D flip-flop (Figure 20) consumes very little static power and shows its robustness and tolerance for low operating frequency. Using TSMC 0.18um technology, at 1.76GHz input, this D flip-flop reaches its operating frequency limit. With large number of transistors, propagation delay causes the static D flip-flop to fail. Therefore, it is not chosen as the divider's D flip-flop.

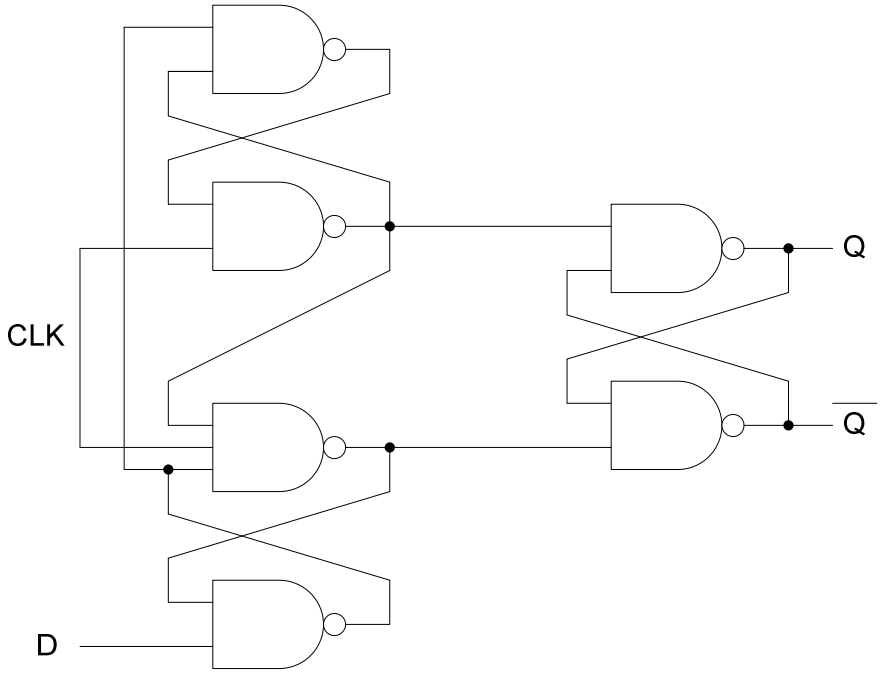

Figure 20 Conventional D flip-flop

Dynamic D-flip-flops are essential to high performance frequency synthesizer [8]. Dynamic logic gates are used to decrease circuit complexity, increase operating speed and lower power consumption. True-Single-Phase clocking (TSPC) D flip flop shown in Figure 21 is used in the frequency divider, due to its high speed performance [9] [10]. The drawback of not having precise complementary outputs is compensated through using additional 8 flip-flops for the frequency divider.

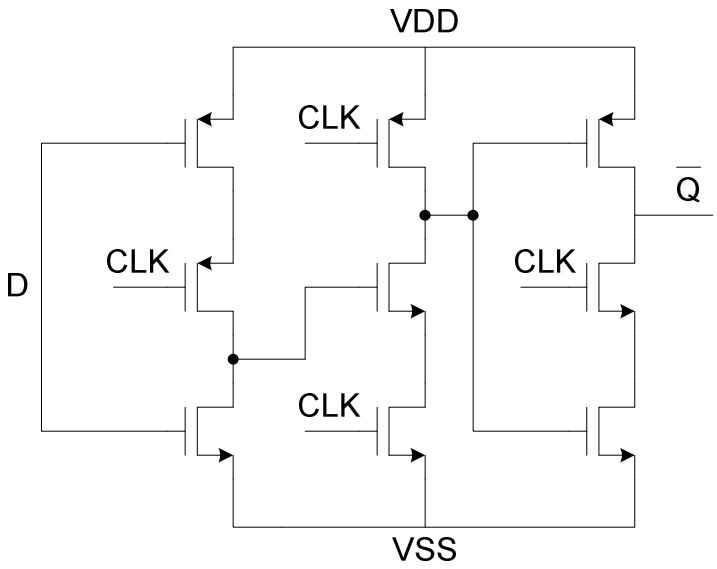

Figure 21 True-single-phase clocking d flip flop

4.2.2 Divider Circuit Implementation

Eight TSPC D flip-flops are used to build a divide-by-16 frequency divider as shown in Figure 18. TSPC D flip-flop carries pseudo differential outputs which are not desired for controlling current summation circuit as shown in Figure 13. The delay creates phase shift error of about 60ps as shown in Figure 22, which causes charge accumulation effect on the current summation circuit's current sources. The accumulated charge distorts its output signal.

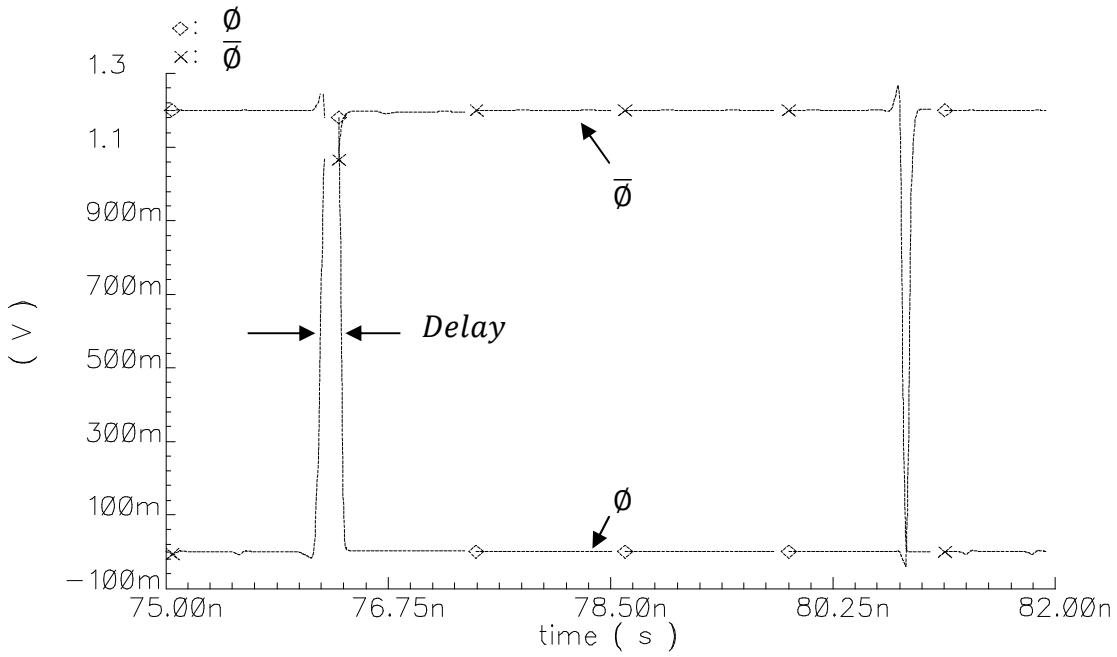

Figure 22 Conventional frequency divider pseudo differential outputs

The schematic in Figure 23 shows a divide-by-two circuit with complementary outputs. Every other input clock rising edge triggers one of the D flip-flops. This circuit generates outputs at half of the input frequency. The waveforms are shown in Figure 24.

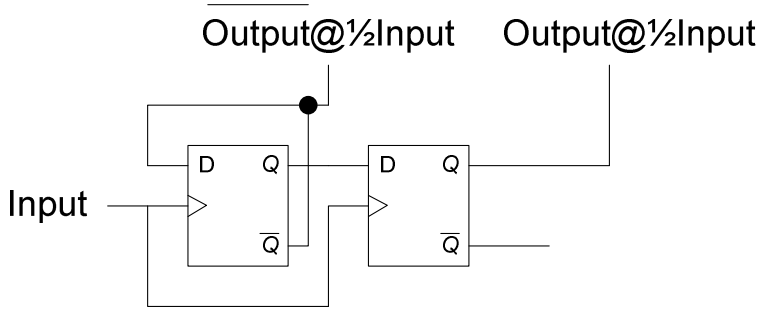

Figure 23 Divide-by-two circuit with complementary outputs

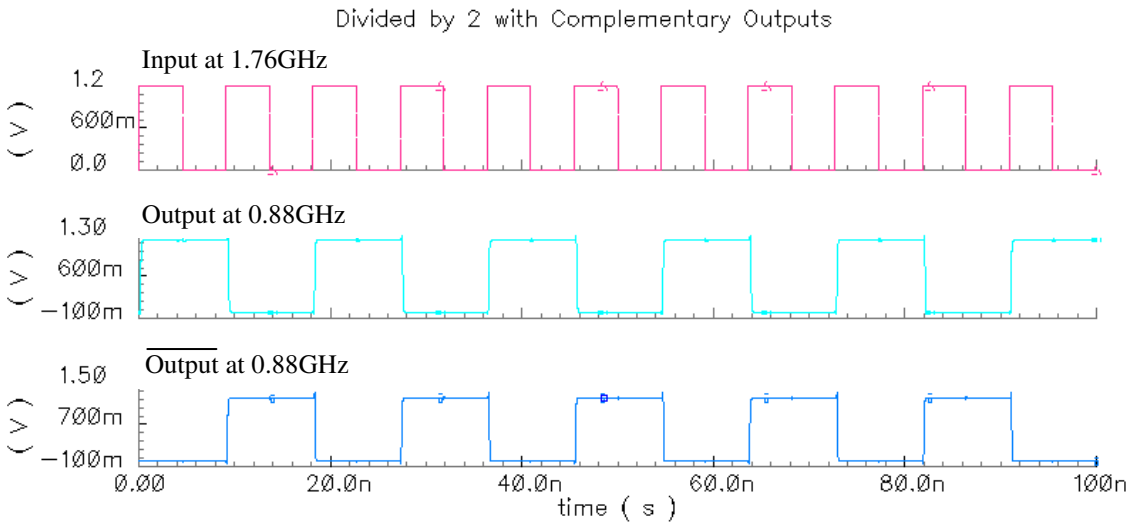

Figure 24 Circuit simulation results for divide-by-two complementary output circuit

By adding eight D flip-flops D9-D16 into the frequency divider in Figure 18, a set of complementary phase shifted square waves is obtained. The modified frequency divider circuit is shown in Figure 25. All D-flip flops D1-D16 are triggered simultaneously, so, there is no delay between complementary square waves. The transient simulation result of $\emptyset$ and $\overline{\emptyset}$ is shown in Figure 26. The inverter delay in Figure 22 is eliminated as shown in Figure 26. Figure 27 shows the layout of the modified frequency divider with die area of $0.001mm^2$. 16 D flip-flops are implemented in this layout using common centroid topology. The distance between two complementary output signals is about 15um. The delay time between two complementary output signals which is caused by circuit mismatch is only a fraction of one inverter delay time (60ps).

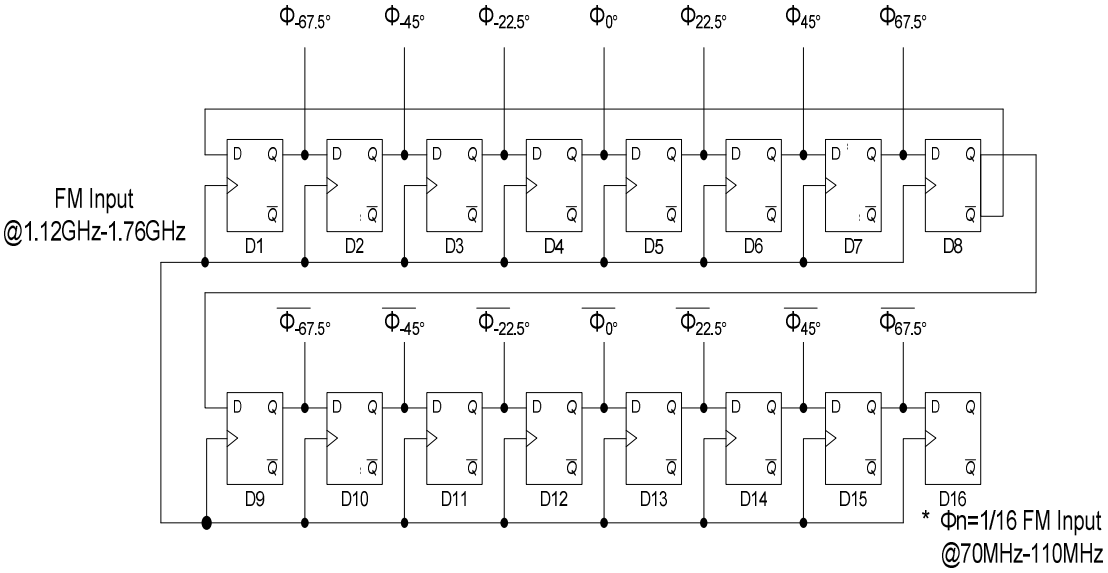

Figure 25 Proposed balanced phase shift generator

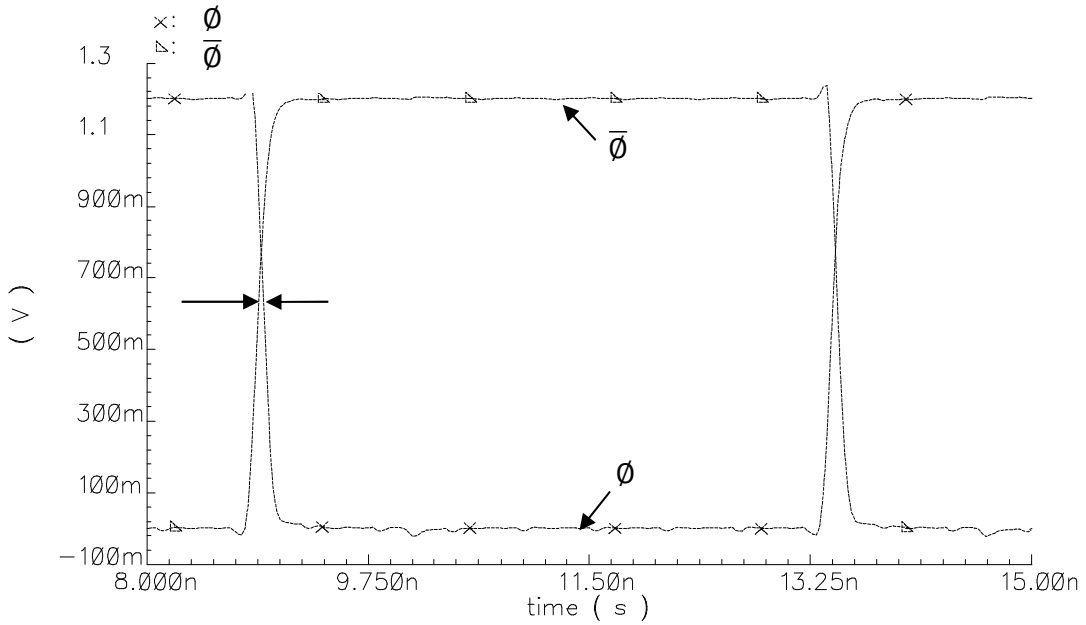

Figure 26 Modified frequency divider's differential output

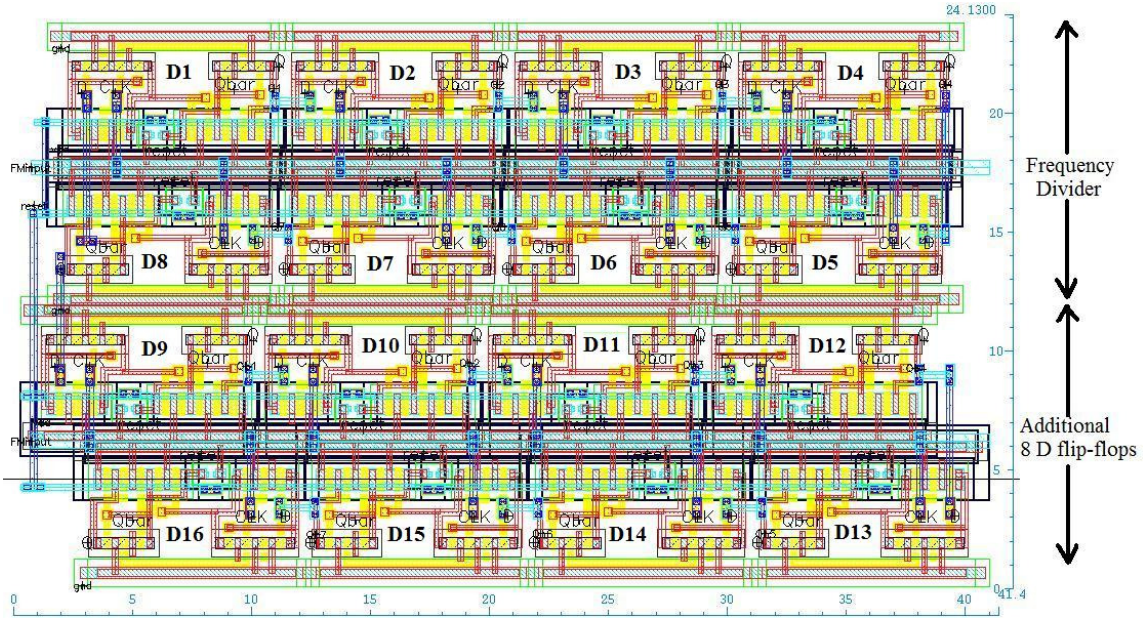

Figure 27 Layout of divided by 16 frequency divider with die area of 0.001mm^2

4.3 Current Summation Circuit Design and Implementation

4.3.1 Current Steering Cell

Current steering cell is chosen to realize the summation of phase shifted square waves in current. It is commonly used in high-accuracy and high-speed D/A converters [11]. Two usual topologies for the current steering cell are shown in Figure 28. Topology (a) includes a cascode transistor MC2 that enhances the output impedance of the current source. However, for 1.2V power supply using TSMC 0.18um technology nominal threshold voltage transistor, the cascode current source occupies too much voltage head room. A non-cascode current source is used for the current steering cell as

shown in Figure 28 (b). Figure 29 shows the current summation circuit schematic using 7 current steering cells.

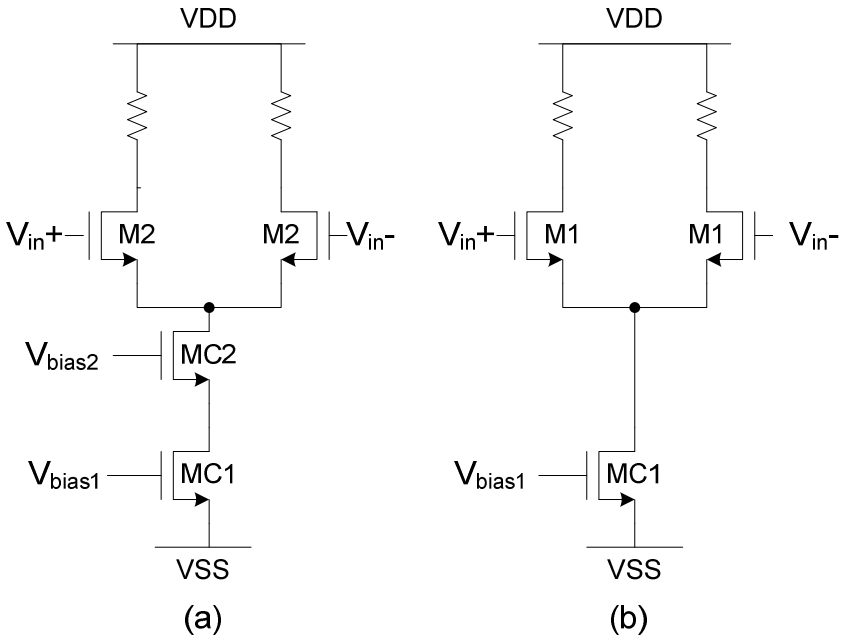

Figure 28 Current steering cell (a) conventional (b) cascode

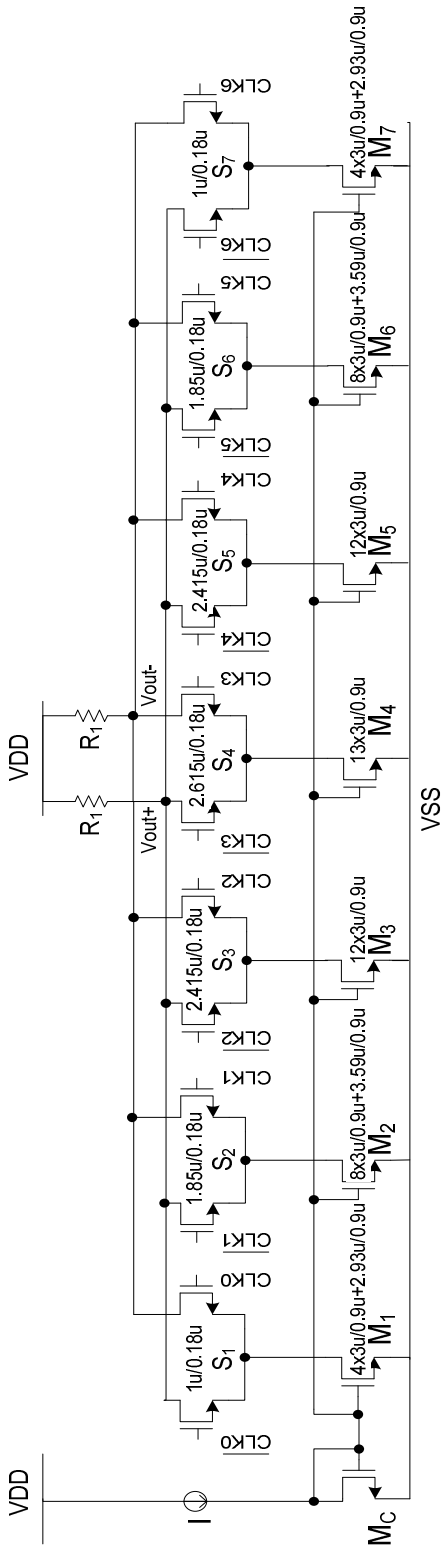

Figure 29 Schematic of current summation circuit

4.3.2 Matching

Harmonic rejection technique uses current sources M_1-M_7 as shown in Figure 29 to realize weighting factors. In Chapter III, mismatch effect is modeled in Matlab to show the relation between weighting factor variation and output harmonic rejection performance.

Although the absolute transistor size is not guaranteed in CMOS process, the ratio among transistor sizes could be within 0.5% depending on layout. In order to minimize mismatch, large transistor size and multiple finger are used in the design. The detailed transistor sizes M_1-M_7 are shown in Table 7. 0.9um length instead of 0.18um is used for all current source transistors. Using multiple fingers, about less than ±0.1% discrepancy with respect to exact harmonic rejection coefficient has been achieved.

Table 7 Ideal harmonic rejection weighting factor vs. current source transistor sizes

Weighting Factor	Exact Value	MOS	Current Source Sizes (finger*W/L)	Discrepancy
K_4	$\sin(11.25^o)\cos(0^o)$	M_4	13x3um/0.9um	0.0462975%
$K_{3,5}$	$\sin(11.25^o)\cos(22.5^o)$	M_3/M_5	12x3um/0.9um	0.1331311%
$K_{2,6}$	$\sin(11.25^o)\cos(45^o)$	M_2/M_6	8x3um/0.9um+3.59um/0.9um	0.0002250%
$K_{1,7}$	$\sin(11.25^o)\cos(67.5^o)$	M_1/M_7	4x3um/0.9um+2.93um/0.9um	0.0104933%

Figure 30(a) shows the ideal harmonic rejection transfer function where all the harmonics from 3^{rd} to 13^{th} are rejected. In Figure 30(b), the actual current source transistor ratio is used to generate the transfer function. It shows that with actual current source transistor ratio the harmonics are attenuated by about 50dB, which is better than

Matlab estimation with 2% STD among current sources as shown in Figure 9. With the real current source design values and 2% STD among current sources, the harmonic tone's rejection coefficient value histograms are obtained as shown in Figure 31. It has been shown that within two sigma, or 97% chance, harmonics from 3rd to 13th are rejected by at least 41dB which is the same level as using ideal current source ratio. Hence, there is no need to design more precise current sources. The random mismatch limits the maximum rejection level.

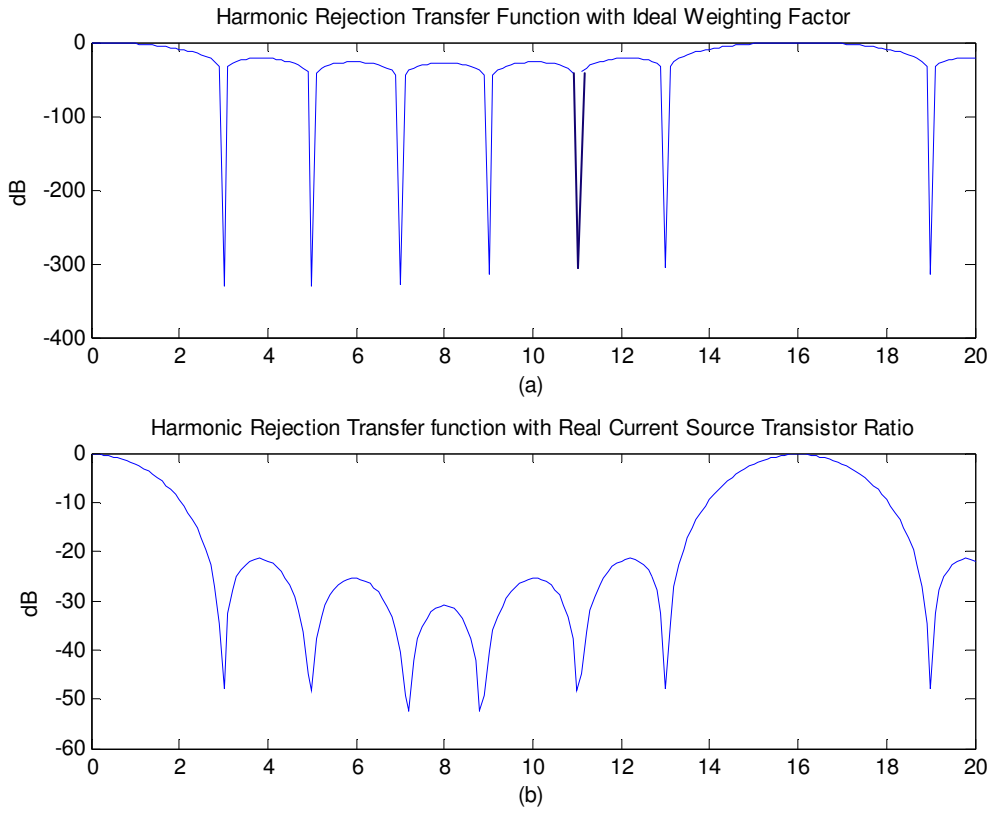

Figure 30 Harmonic rejection ideal transfer function (a) with ideal current source vs. nth harmonic (b) with actual current source vs. nth harmonic

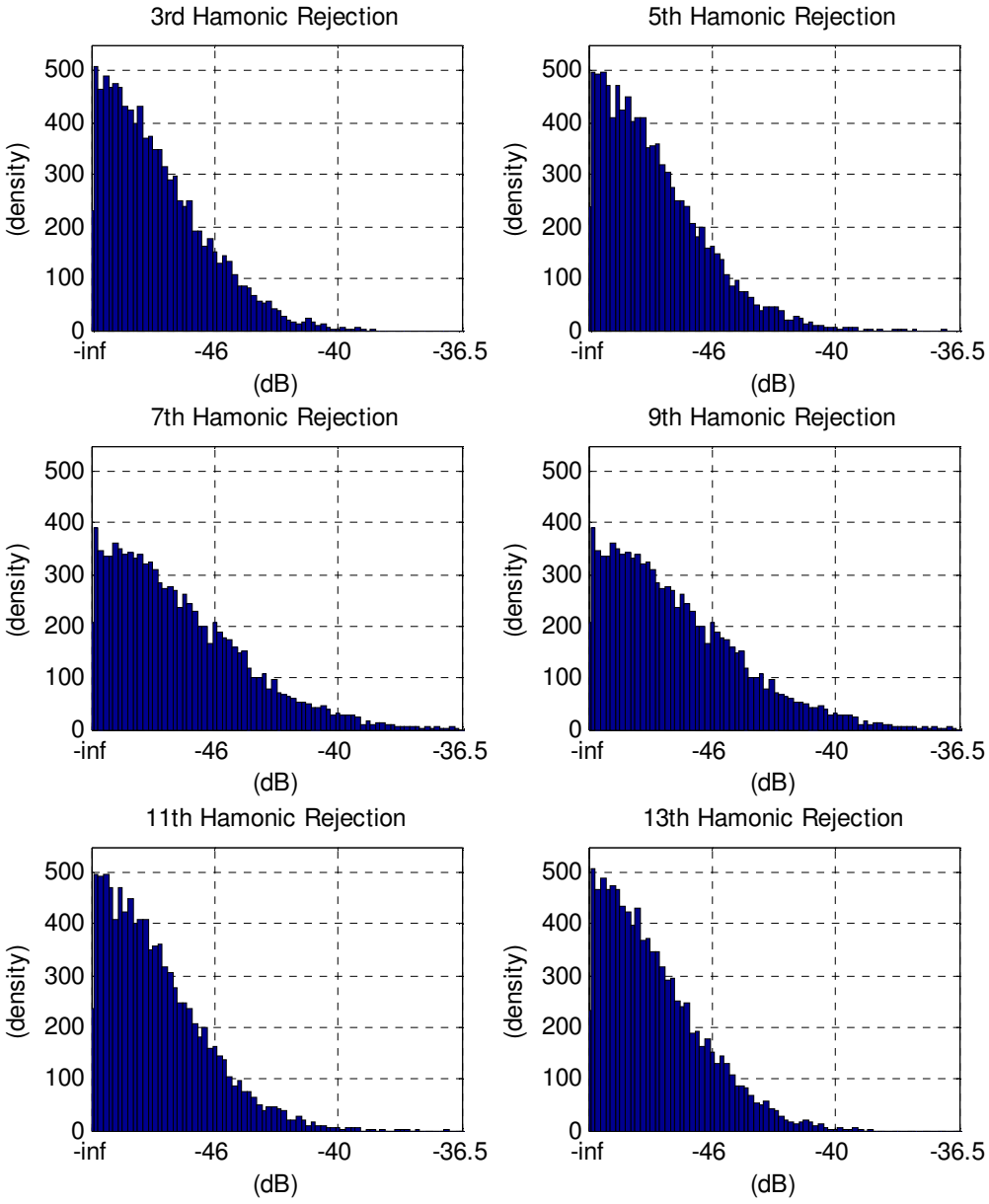

Figure 31 Nth harmonic tone's rejection coefficient value histograms in the presence of current source mismatch and actual current source design values

4.3.3 Power Consumption and Linearity

The power consumption of current steering cells is specified within 0.5mW. The current steering cells drive a 1900Ω resistive load R1 to realize current to voltage conversion as shown in Figure 29. The value of load resistor R1 is determined by the RC low pass filter's time constant which will be discussed in Chapter V. The output swing is proportional to output current and resistor's value. Large output signal swing gives good output signal to noise ratio but it may degrade signal linearity. For linear operation of current to voltage conversion, the maximum output swing is calculated as follows:

$$Output\ Swing < Supply\ Voltage - 2 * V_{ov} \cong 0.8V \tag{4.2}$$

where V_{ov} is the overdrive voltage of the current supply M1-M7 and current switch S1-S7. The total current can be calculated through maximum output swing divided by R1. The output swing is calculated as

$$Output\ Swing = Total\ Current * R1 \tag{4.3}$$

$$0.8V_{max} = Total\ Current * 1900\Omega \tag{4.4}$$

$$Total\ Current = \frac{0.8V_{max}}{1900\Omega} = 421uA \tag{4.5}$$

where the total current is the estimated maximum value. Based on the estimation, the current sources are designed and shown in Table 8. Transistors M1-M7 and, switches S1-M7 are scaled accordingly to maintain the constant V_{ov}.

Table 8 Current source and transistor sizings of current summation circuit

Current Source	Design Current	Transistor Sizes
M1	24.883uA	4x3um/0.9um+2.93um/0.9um
M2	45.983uA	8x3um/0.9um+3.59um/0.9um
M3	60uA	12x3um/0.9um
M4	65uA	13x3um/0.9um
M5	60uA	12x3um/0.9um
M6	45.983uA	8x3um/0.9um+3.59um/0.9um
M7	24.883uA	4x3um/0.9um+2.93um/0.9um
Total	326.732uA	

4.3.4 Current Source Layout

Layout plays a very critical role in the realization of design. Seven current sources (M1-M7) of Figure 29 are grouped together with common centroid distribution. The floor plan is shown in Figure 32 “D” represents dummy transistors. S1-S7 are current steering cells’ switches whose performance is not affected by mismatch. Transistor length of M1-M7 is 5 times of minimum length. Layout of the current summation circuit is shown in Figure 33.

		S1	S7	S2	S6	S3	S5	S4						
	D	M5	M5	M6	M7	MC	M2	M3	M3	D				
	D	M5	M4	M6	M1	MC	M2	M4	M3	D	D	M6	M2	D
D	M3	M3	M4	M2	MC	M7	M6	M4	M5	M5	D			
D	D	M3	M4	M2	MC	M1	M6	M4	M5	M4	M4	M1	M7	D

Figure 32 Layout floor plan of current source transistors

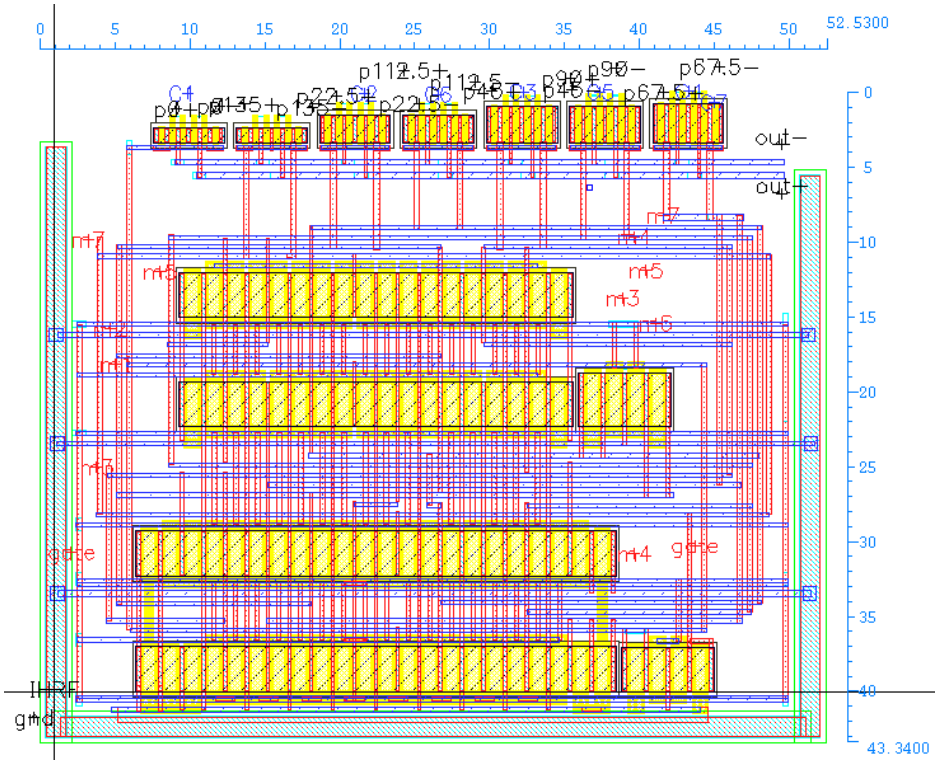

Figure 33 Layout of current summation circuit with area of 0.00224mm^2

4.3.5 Switching Signal Feedthrough

The coupling between the current steering cell's inputs and outputs through the parasitic capacitors of the switches M1a and M1b causes glitches at the output when switching signals are applied. The schematic of current steering cell with switches' parasitic capacitors is shown in Figure 34 (a). The illustration of input switch signal and output glitch though the coupling is shown in Figure 34 (b). The voltage glitch at the output of the current steering cell is estimated by

$$V_{glitch} = \frac{C_{gd}}{C_{gd} + C_{dtotal}} V_{in} \tag{4.6}$$

where V_{in} is the switching input voltage, C_{dtotal} is the total parasitic capacitance associated with M1a/M1b's drain and output node with respect to VSS, and C_{gd} is the M1a/M1b's parasitic capacitance from gate to drain. When V_{in} is large, a noticeable amount of voltage glitch appears on the output of current steering cell, which reduces linearity of the harmonic rejected signal.

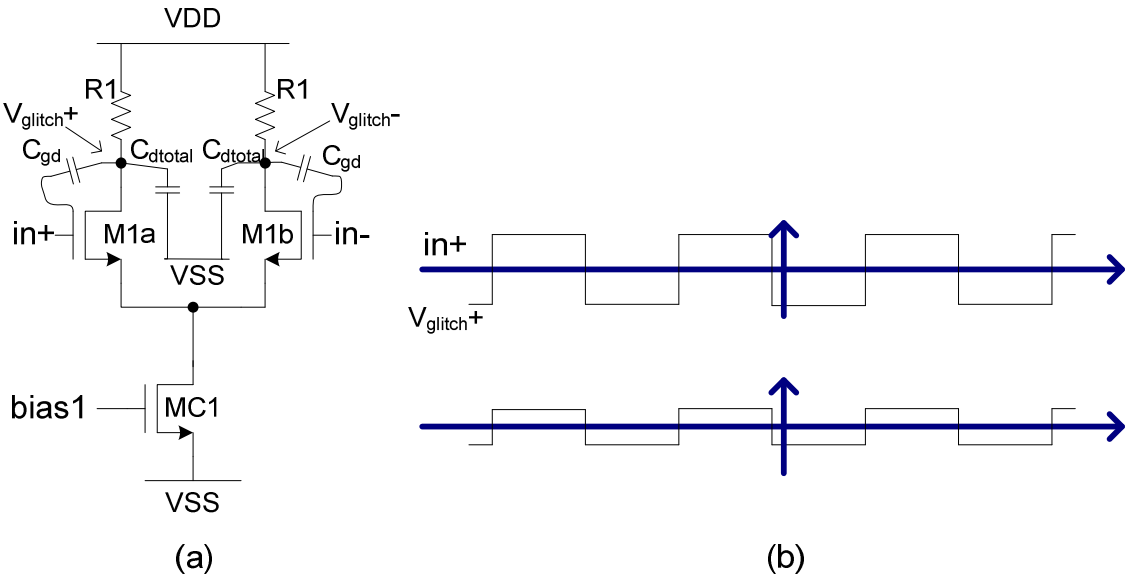

Figure 34 (a) Schematic of current steering cell with parasitic capacitors shown (b) switching input signal and feedthrough glitch

Some techniques were proposed to reduce the switch feedthrough [12]. An extra transistor could be added on top of the switch transistor in order to isolate the output node from the drain of the switch transistor, though this technique reduces output swing headroom. The second solution is to connect a dummy transistor in parallel with the

switch transistor. A complementary control signal is used to switch the dummy transistor in order to compensate the signal feedthrough.

In this work, a third solution is used, which is to limit the switching signal amplitude. The circuit is shown in Figure 35. The switching amplitude is set to $\sqrt{2}$ of transistor S1a and S1b's overdrive voltage, which is just necessary to completely turn off and on the switches. The minimum voltage swing becomes,

$$V_{in} \cong \sqrt{2}V_{ov2} = \sqrt{\frac{2I}{\frac{k_n}{2}\frac{W}{L}}} \tag{4.7}$$

where, k_n is NMOS transconductance parameter, and I is the DC current flowing through S1a/S1b. Switch transistors S1-S7 shown in Figure 29 are scaled proportional to the current values shown in Table 9 in order to carry the same overdrive voltage.

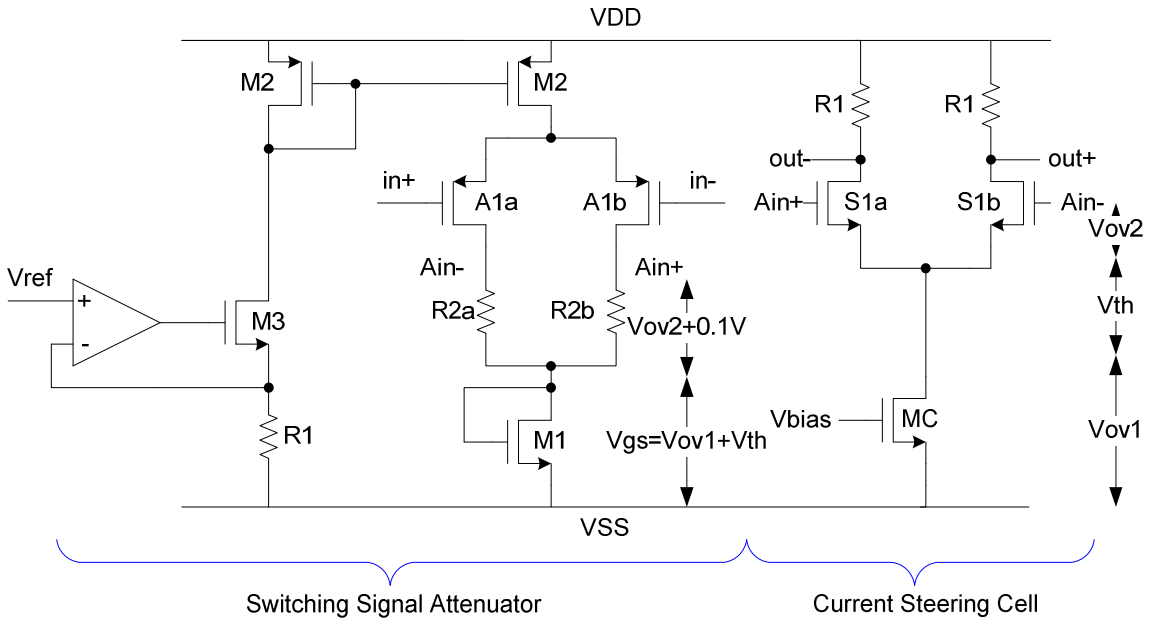

Figure 35 Schematic of switching signal attenuator and error correction circuit

Table 9 Current summation switch transistor sizes

Switch	Current	Transistor Sizes	V_{ov}
S1	24.8uA	1u/0.18u	250mV
S2	45.9uA	1.85u/0.18u	250mV
S3	60.0uA	2.415u/0.18u	250mV
S4	65.0uA	2.615u/0.18u	250mV
S5	60.0uA	2.415u/0.18u	250mV
S6	45.9uA	1.85u/0.18u	250mV
S7	24.8uA	1u/0.18u	250mV

The desired switching signal's swing is realized through voltage attenuators as shown in Figure 35. A simple differential pair type attenuator is designed to provide the desired swing for the current steering cells. Two resistors R2a and R2b are used as the differential pair's load, which limits the attenuator's upper output swing level. Under these two resistors, a diode connected transistor M1 is placed, which limits the lower output swing level. The voltage drop across M1's source and drain is given by

$$V_{gs} = V_{th} + V_{ov1} \tag{4.8}$$

where V_{ov1} is designed to be around the same overdrive voltage of MC and the V_{th} is about the same threshold voltage of the steering cell's switches S1a and S1b. The attenuated voltage swing is approximated to be the minimum turn on/off voltage of S1-S7.

The voltage drop across R2a and R2b is used to set the upper signal swing limit. However, these resistors are heavily process dependent elements. A simple tuning circuit is designed to cancel any resistance process variation effect. It is shown in Figure 35.

The simple feedback amplifier determines the current in M2, which is inversely proportional to R1's value. This current is mirrored into attenuator's resistance load R2, which creates a constant voltage drop regardless of the resistance process variation. Figure 36 shows the layout of the switching signal attenuator, which occupies 0.0028mm^2 die area.

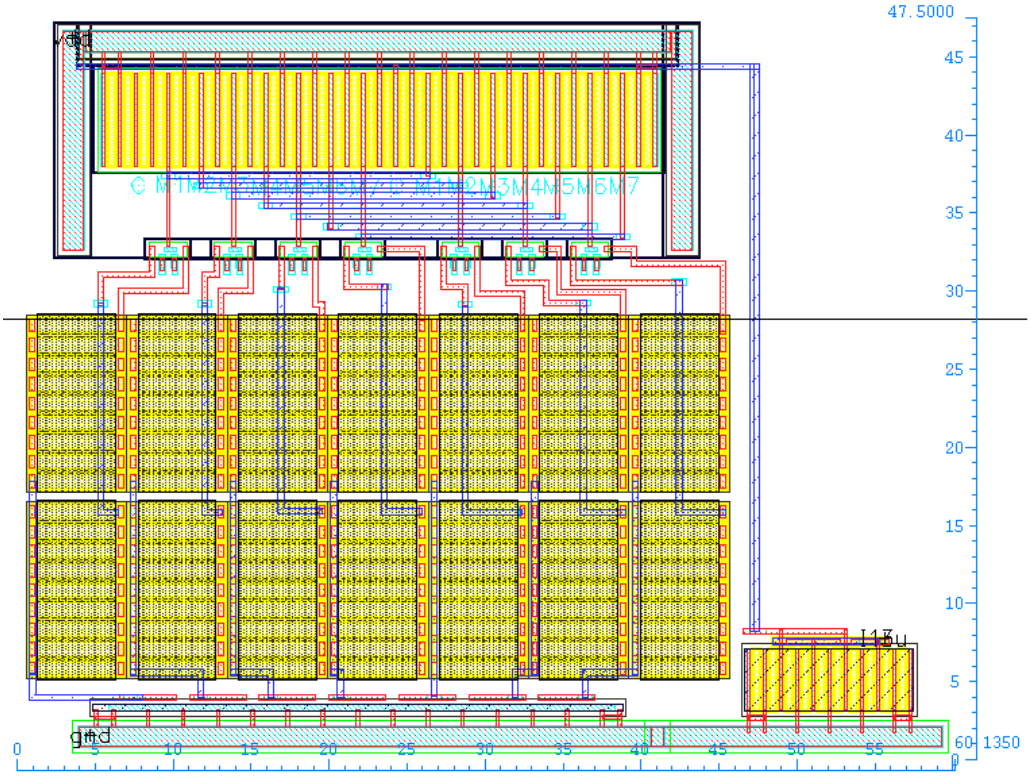

Figure 36 Layout of switching signal attenuator with die area of 0.0028mm^2

4.4 Post Layout Simulation Results

The harmonic rejection filter's performance is measured during the post layout simulation. The transient simulation given in Figure 37 shows the differential output

signals with 15th and 17th harmonics that are not rejected. The total harmonic distortion is -17.5dB. The differential output signal's frequency spectrum is measured through Cadence calculator. The 15th and 17th harmonics are at -31dB and -35.5dB, respectively. The frequency spectrum is shown in Figure 38.

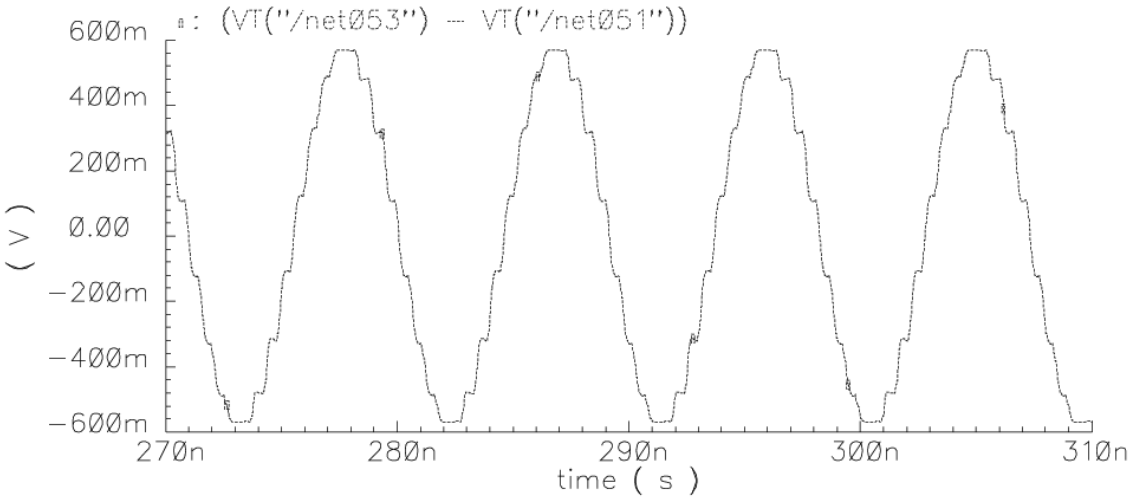

Figure 37 Post layout simulation of harmonic rejection filter's output

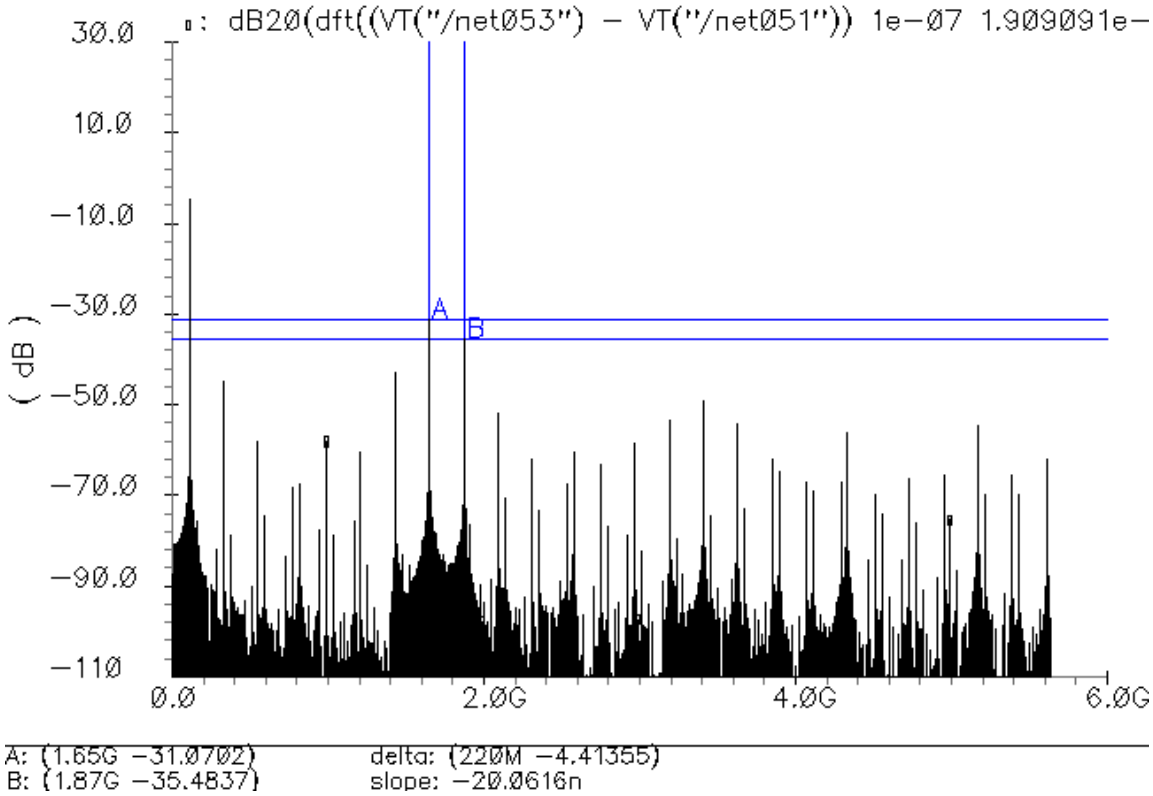

Figure 38 Post layout FFT simulation of harmonic rejection filter's output

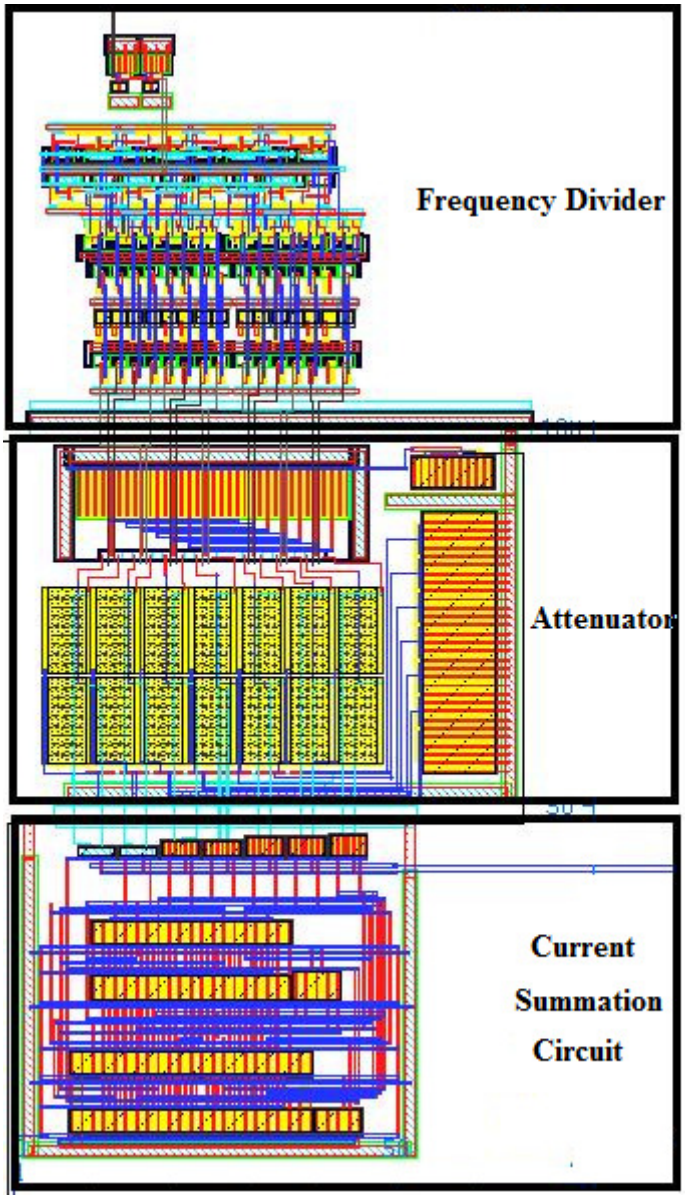

Figure 39 Layout of harmonic rejection filter including frequency divider, attenuator, and Current Summation Circuit with total area of 0.0112mm^2

The harmonic rejection filter is laid out in TSMC 0.18um technology. The total area of the filter is 0.0112mm^2. It is shown in Figure 39. In theory, the harmonic rejection filter could achieve -19.2dB THD with high frequency harmonics at -20.8dB.

In this design, post layout simulation shows -17.5dB THD with -31dB high frequency harmonics. The higher THD is caused by 3^{rd}, 5^{th}, 7^{th}, 9^{th} harmonics which are not rejected completely due to the use of finite resolution of W/L in current source transistors. These harmonics are further attenuated by the next stage RC low pass filter. The lower than expected high frequency harmonics amplitudes are mainly due to transistors' and layout interconnects' parasitic resistance and capacitance's low pass filter effect. The total power consumption is under 0.4mW. Table 10 shows harmonic rejection filter's results based on mathematical model and post layout simulation.

Table 10 Harmonic rejection filter's post layout simulation results

Performance Parameter	Mathematical Calculation	Post Layout Simulation
THD	-19.2dB	-17.5dB
Frequency Range	70MHz-110MHz	70MHz-110MHz
Output Swing	550mV	550mV
High Frequency Harmonics	-20.8dB	-31dB
Power	0.525mV	0.525mV
Area	N/A	$0.0112mm^2$

CHAPTER V

RC FILTER WITH AUTOMATIC TUNING

5.1 RC Low Pass Filter Specifications

The output signal of the harmonic rejection filter carries 15^{th} and 17^{th} harmonics with the highest amplitude at about -24dB. The THD of this output signal is -17.2dB. Based on this harmonic rejection filter's attenuation performance and the project's specifications, RC low pass filter's desired attenuation with respect to FM carrier harmonics is estimated as shown in Table 11. In addition, both 3^{rd} and 4^{th} order RC low pass filters' attenuation across the specified frequency spectrum are shown in the table. The RC filters' RC time constants are set to be the same as FM fundamental frequency The table shows that 4^{th}-order RC low pass filter meets the desired attenuation for the harmonics, but it also attenuates the fundamental tone. In the mean time, 3^{rd}-order RC low pass filter has less fundamental tone attenuation, but it is about 20dB less than the desired 15^{th} and 17^{th} harmonic tones attenuation.

Table 11 Desired, 3rd-order, and 4th –order rc filter attenuation based on harmonic rejection attenuation and output signal specifications

FM Carrier Harmonic & Amplitude	Estimated Harmonic Rejection Attenuation	Output Signal Harmonic Level Specifications	Desired RC Filter Attenuation	3rd-Order RC Filter Attenuation	4th-Order RC Filter Attenuation
1st @0dB	-3dB	-4dB	0	12.8dB	18.1dB
3rd @-9.5dB	-49.4dB	-50dB	>0dB	27.5dB	36.9dB
5th @-14.0dB	-46.7dB	-50dB	>0dB	37.4dB	49.4dB
7th @-16.9dB	-43.2 dB	-50dB	>0dB	44.7dB	59.1dB
9th @-19.1dB	-41.3dB	-110dB	>49.6dB	50.4dB	67.0dB
11th @-20.8dB	-40.9dB	-110dB	>48.3dB	55.3dB	73.2dB
13th @-22.3dB	-39.2dB	-110dB	>48.5dB	59.0dB	78.7dB
15th @-23.5dB	-3dB	-110dB	>86.5dB	62.9dB	83.7dB
17th @-24.6dB	-3dB	-110dB	>85.4dB	65.6dB	87.5dB
…@<-25.6dB	-34dB	-110dB	>50.4dB	67.0dB	89.4dB

5.2 Design Consideration of RC Filter with Automatic Tuning

5.2.1 Cascade First-Order RC Passive Low Pass Filters

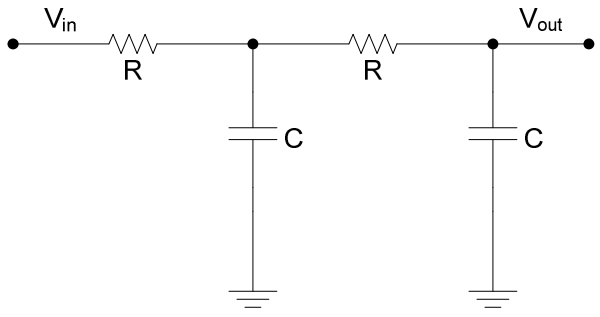

Figure 40 Second Order RC low pass filter

n^{th}-order RC passive low pass filter is constructed through cascading n number of first-order RC passive low pass filters. A second-order RC low pass filter is shown in Figure 40, its transfer function can be expressed as

$$\frac{V_{out}}{V_{in}} = \frac{\left(R + \frac{1}{SC}\right) // \frac{1}{SC}}{R + \left(R + \frac{1}{SC}\right) // \frac{1}{SC}} * \frac{\frac{1}{SC}}{R + \frac{1}{SC}} \tag{5.1}$$

$$= \frac{SRC + 1}{(S^2R^2C^2 + 3SRC + 1)(SRC + 1)}$$

$$\frac{V_{out}}{V_{in}} = \frac{1}{S^2R^2C^2 + 3SRC + 1} \tag{5.2}$$

This transfer function shows that by cascading two first-order RC low pass filters the gain at *1/RC* attenuates more than 6dB. Nonetheless, at higher frequency where $\omega >> 1/RC$ the transfer function is estimated as

$$\frac{V_{out}}{V_{in}} = \frac{1}{S^2R^2C^2 + 3SRC + 1} \cong \frac{1}{(SRC)^2} \tag{5.3}$$

where the transfer function is approximately the same as the product of two first-order low pass filters. This example shows that increasing RC low pass filter's order not only attenuates unwanted high frequency harmonics, but also decreases the gain at frequency of 1/RC. Increasing the order of the RC passive low pass filter is not the ideal solution for this project's filter design.

5.2.2 Order of Low Pass RC Filter

4^{th}-order low pass filter has better high frequency attenuation than 3^{rd}-order low pass filter. However, the designed output buffer generates distortions as large as -95dB at higher frequency. It is not necessary to use 4^{th}-order low pass filter to reach -110dB at 800MHz. In addition, the fundamental tone's attenuation of a 4^{th}-order low pass filter reduces the output signal to noise ratio. Therefore, a 3^{rd}-order low pass filter is chosen in this work. In fact, at the output side, a matching network will be added which provides additional attenuation of 20dB for the output FM carrier.

5.3 RC Filter Circuit Implementation

5.3.1 RC Filter Circuit Transistor Level Implementation

Differential RC low pass filter is implemented using TSMC 0.18um poly resistors and metal-insulator-metal capacitors. The single-ended filter schematic is shown in Figure 41. In order to compensate process variation, the filter's minimum time constant is designed to be 50MHz, which is 75% of 70MHz input frequency. The filter's maximum time constant is designed to be 140MHz, which is about 125% of 110MHz input frequency. 4-bit capacitor banks are used to tune RC time constant.

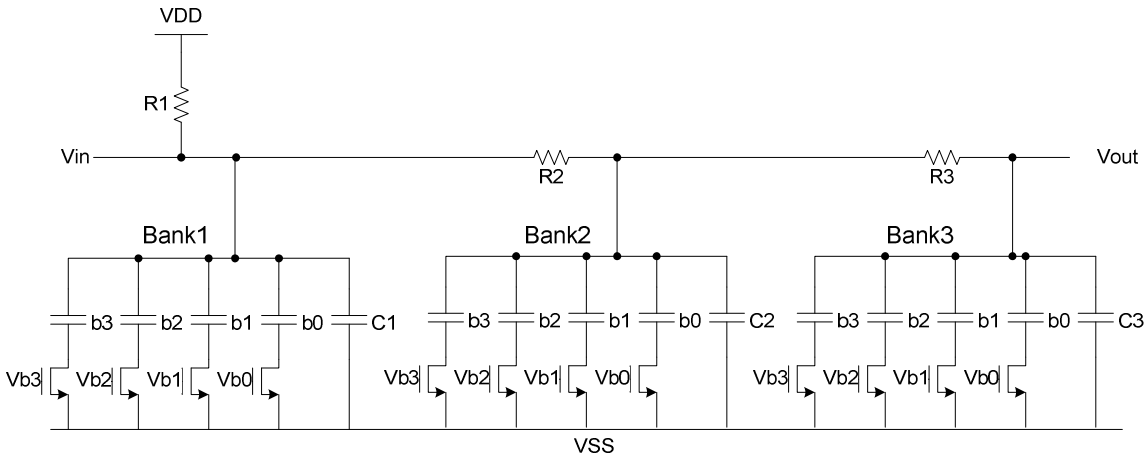

Figure 41 Schematic of third-order RC low pass filter with capacitor banks

In Figure 42 resistor R1 acts like a load for the current steering cells, which converts harmonic rejection output current into voltage. However, process variation of resistors causes the output voltage swing deviation. Due to 1.2V supply headroom, too large swing would distort V_{out}+/V_{out}-. Too small swing reduces signal to noise ratio. This process variation issue is cancelled through an error correction circuit as shown in Figure 42. It is the same concept as the attenuator's resistor process variation compensation as shown in Figure 35. With a matching resistor R1, the process variation is cancelled. Table 12 shows the RC filter's design parameters. These values are designed to compensate the maximum RC process deviation of ±25%.

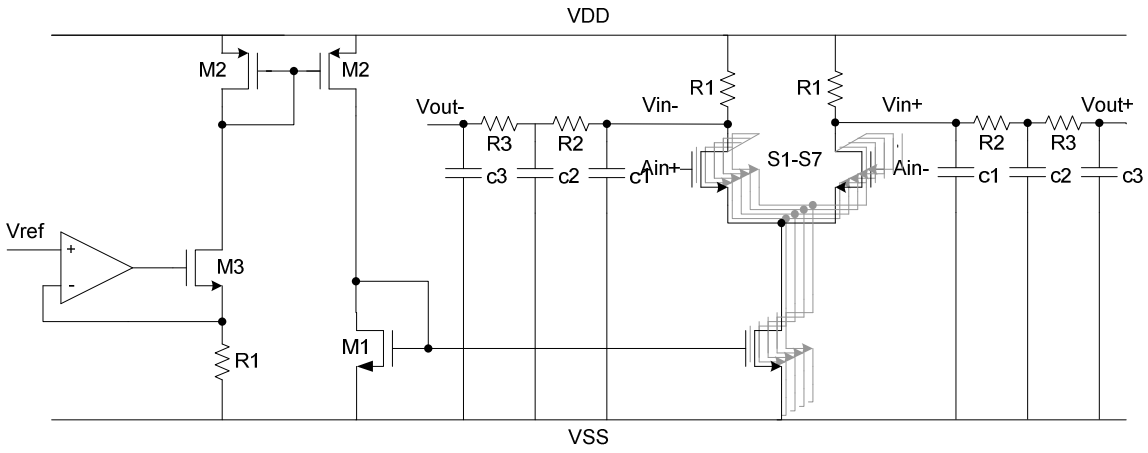

Figure 42 Schematic of current summation circuit's error correction circuit

Table 12 RC low pass filter components value

Resistor	Design Value	Capacitor	Design Value
R1	1926Ω	C1-C3	480fF
R2	1926 Ω	b0	80fF
R3	1926 Ω	b1	160fF
		b2	320fF
		b3	640fF

5.3.2 RC Low Pass Filter Layout

Common centroid topology is used in order to minimize circuit mismatch. Unity capacitor of 80fF is used during the layout. Figure 43 shows the layout of RC low pass filter. The die area is 0.0954mm^2.

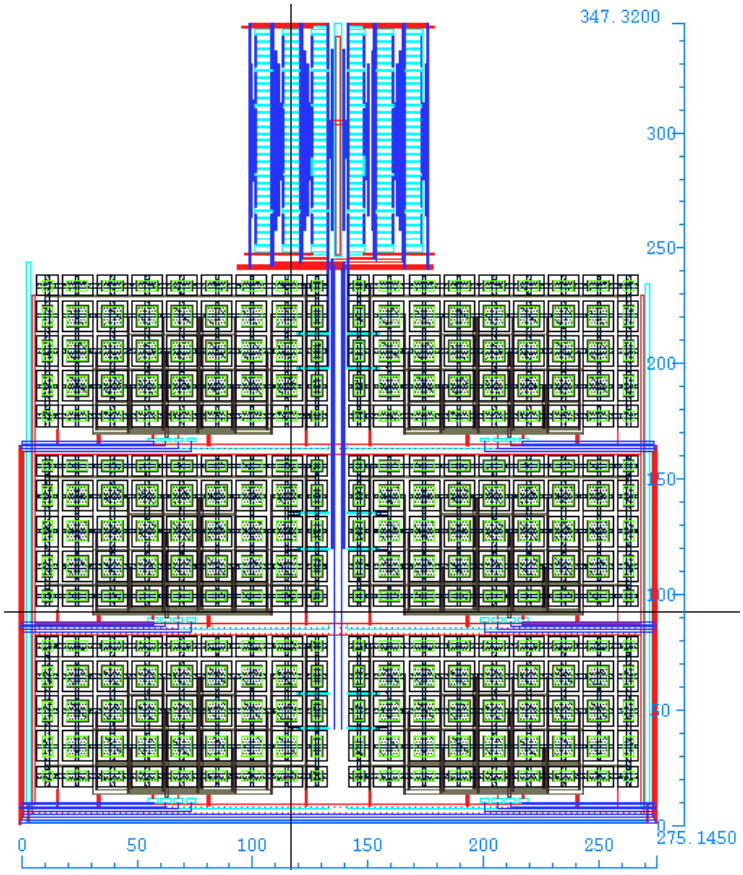

Figure 43 Layout of third-order differential RC low pass filter with area of 0.0954mm^2

5.4 Design and Implementation of Automatic Tuning Circuit

The RC passive low pass filter automatic tuning scheme based on the phase was introduced in 2004 [13]. In this work, a magnitude base automatic tuning scheme is proposed for the RC passive low pass filter. This tuning scheme follows the input frequency and process variation to tune RC time constant automatically. It does not require any external reference signal. The FM input signal itself provides the tuning

reference. To save area and reduce circuit mismatch, on-line tuning scheme is adopted instead of master-slave tuning.

5.4.1 Magnitude Tuning

The tuning is based on the passive filter's magnitude transfer function. A first-order RC low pass filter's transfer function can be expressed as

$$T(j\omega) = \frac{1}{1 + j\omega RC} \tag{5.4}$$

where at input frequency of 1/RC, the magnitude of the transfer function is calculated as

$$Mag\big(T(j\omega)\big) = 20\log\left(\frac{1}{\sqrt{1 + \omega RC^2}}\right) = 20\log\left(\frac{1}{\sqrt{2}}\right) = -3dB \tag{5.5}$$

Based on the magnitude of the filter transfer function at the frequency of 1/RC, RC filter can be tuned. For a third-order RC passive low pass filter, when output's magnitude is 1/3 (-9.5dB) of input signal's magnitude, the input frequency is at about 80% of the filter's actual cut-off frequency. Figure 44 shows a tunable third order RC low pass filter's frequency response tuning from 50MHz to 150MHz.

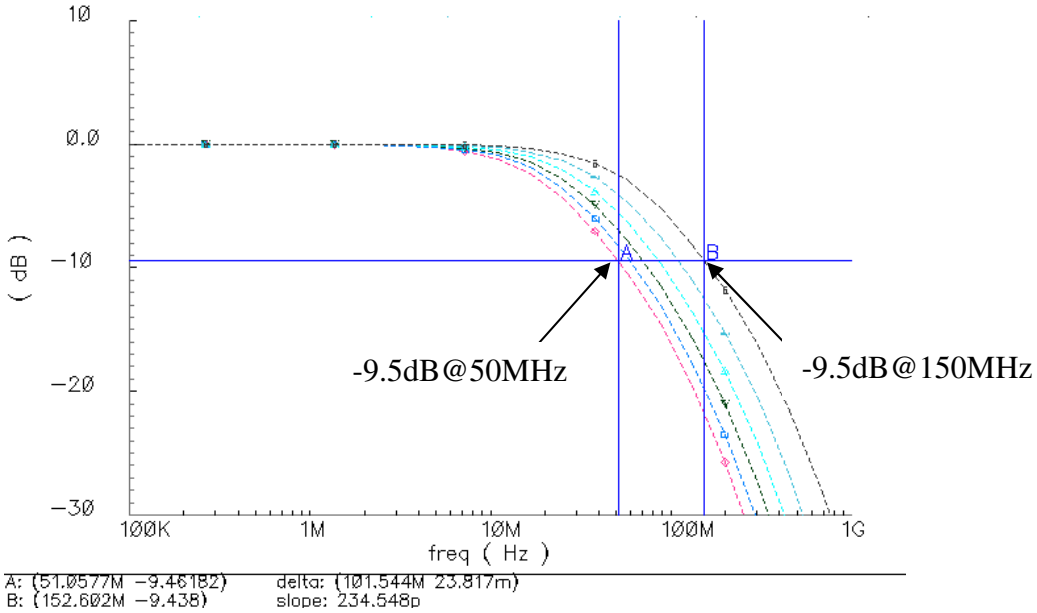

Figure 44 A tunable 3rd RC low pass filter frequency response tuning from 50MHz to 110MHz

5.4.2 Automatic Tuning Circuit Realization

Figure 45 shows the block diagram of the automatic tuning. *ref1* and *ref2* are 1/3 of *input* and 4/15 of *input* respectively. They are generated through resistor divider as shown in Figure 46. FM is divided by 1024 to function as a clock signal for the tuning circuit. Peak detectors are used to measure the peak amplitude of ref1, ref2 and out. Their amplitudes are compared with each other by comparators to determine the RC filter's RC time constant with respect to FM frequency. When RC low pass filter is not tuned, the output signal's amplitude falls out of ref1 and ref2 window. An enable signal and an up/down signal are generated through a NAND gate and comparators, which controls the 4-bit counter. Depending on the RC corner frequency's location, 4-bit

counter either counts up/down or stops counting. b0-b3 which are the output of the counter control RC low pass filter's capacitor banks. Maximum of 16 clock steps is required to finish the tuning. Once the filter is tuned, the 4-bit counter will stop at the present number automatically. The counter remains disabled until a change of FM carrier input signal frequency is detected.

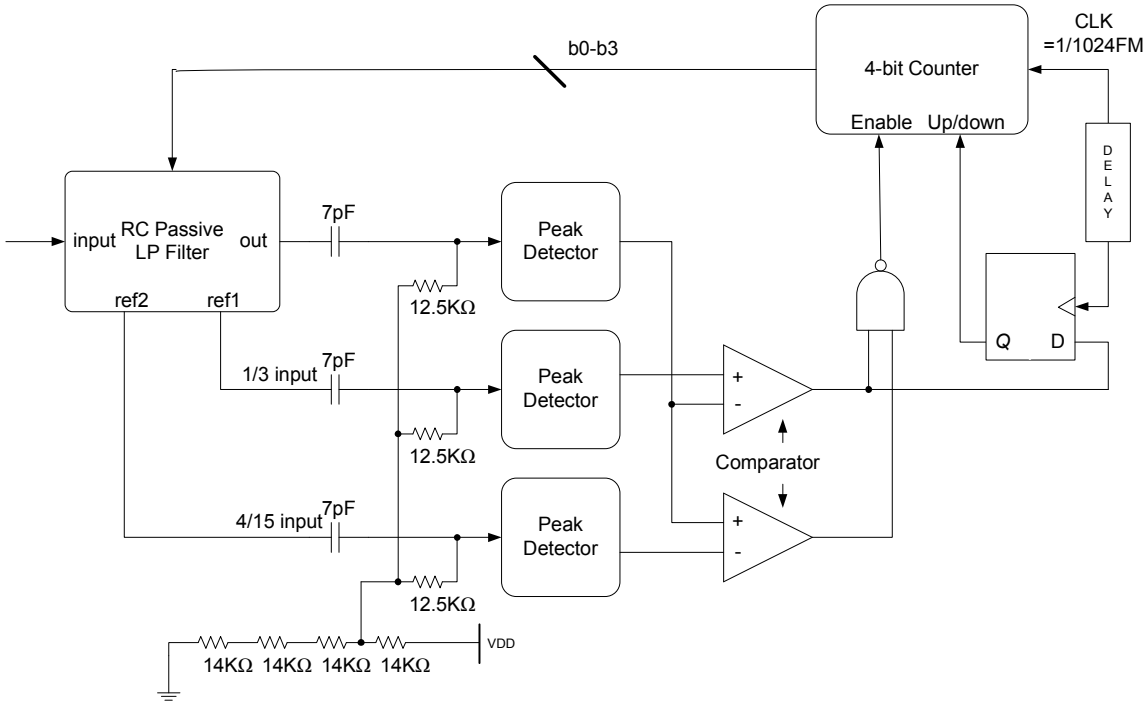

Figure 45 Proposed magnitude tuning flow chart

Figure 46 shows the resistor divider implementation. R1 is divided into 15 equal value resistors. ref1 and ref2 are generated and are independent of process variation. The reference signals are coupled into the peak detector through 7pF capacitor. The DC voltage level of ref1, ref2, and out are provided by a resistor divider circuit.

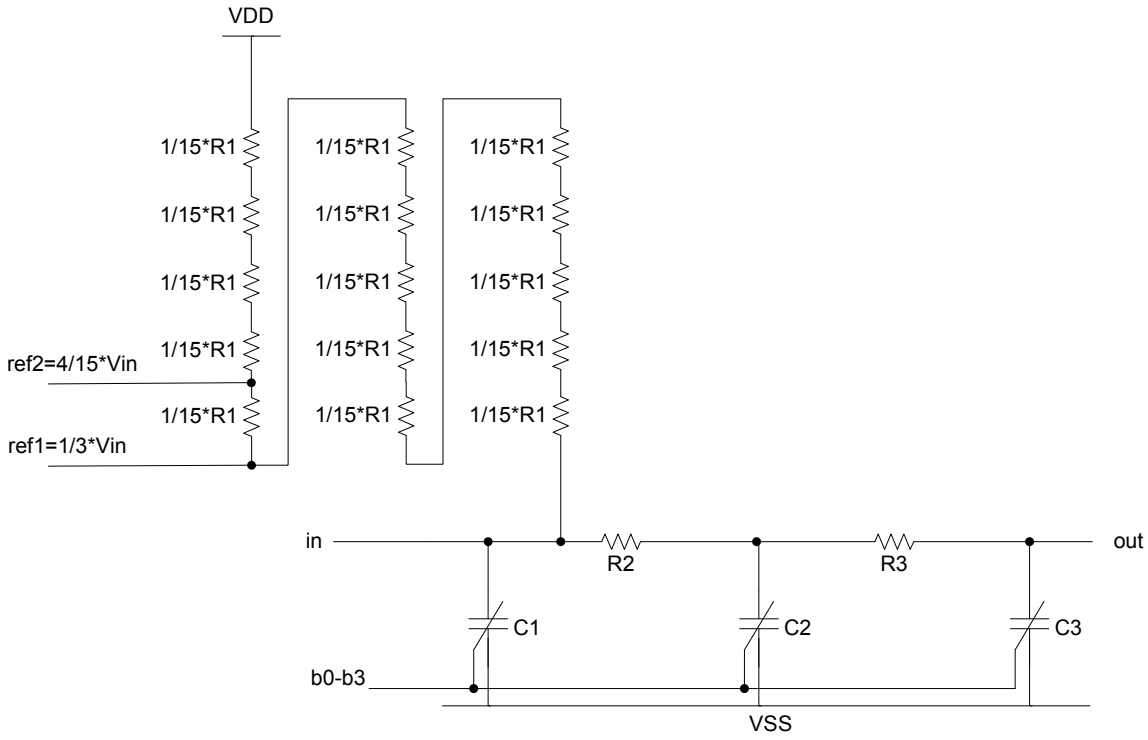

Figure 46 RC low pass filter with resistor divider

5.4.3 Tuning Circuit Timing Diagram

Figure 47 shows the timing diagram of RC filter's automatic tuning signals. Initially, the capacitor banks C1-C3 are all turned off and the RC filter is not tuned. b0-b3 are all zero. The comparator and NAND gate will generate up-down and enable control signals for the counter based on the filter's RC time constant. As the sampling clock starts to sample the output of the latch, the counter starts to count up/down through b0-b3. The counter increases or decreases in binary format and its outputs b0-b3 control capacitor bank's switches in order to lock FM carrier frequency. The tuning process stops when the output signal's magnitude falls between ref1 and ref2. The comparator

turns off the counter, and the tuning is stopped. The counter will restart tuning automatically when FM carrier frequency changes.

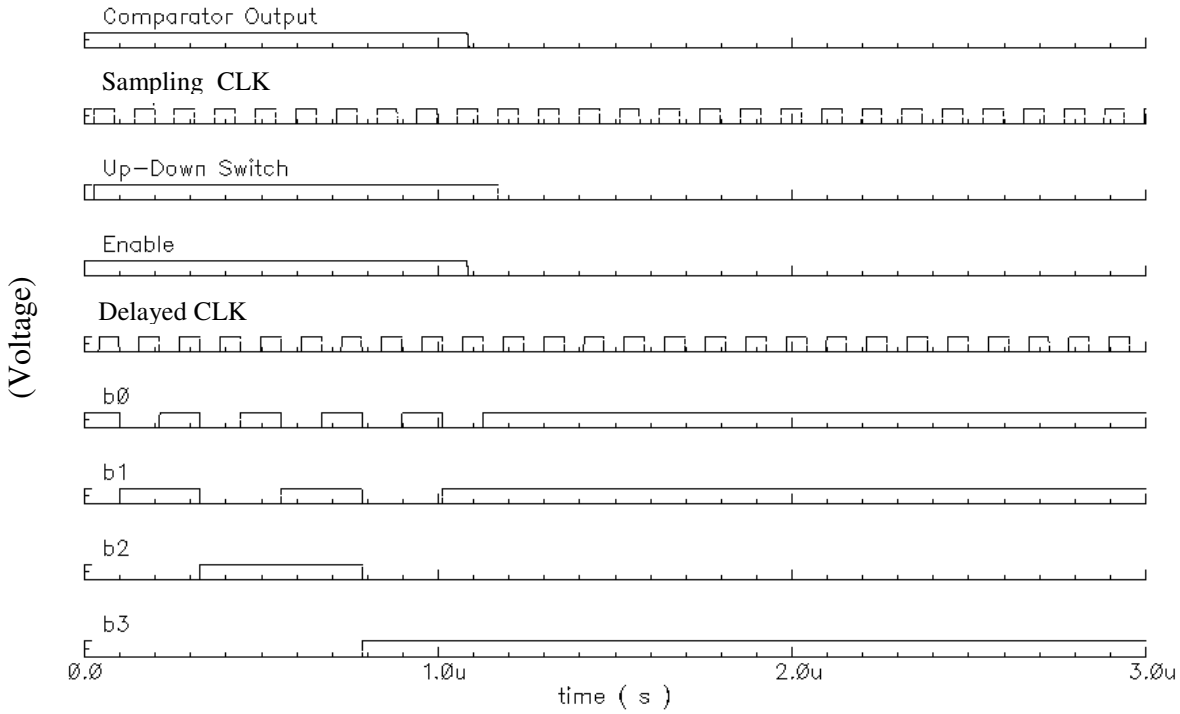

Figure 47 Timing diagram of automatic tuning

5.4.4 Design of Peak Detector

Signal level detectors are widely used in electronic systems [14]. Conventional peak detector as shown in Figure 48 uses an amplifier and a diode in feedback configuration to realize precision peak detection. The peak detector's input signal frequency is limited below amplifier gain bandwidth product. The incoming signal's frequency is in the range of 70MHz to 110MHz. An amplifier with more than 100MHz gain bandwidth product could easily consume more than 1mW power. Based on the

power consumption requirement, the conventional peak detector could not be used in this research.

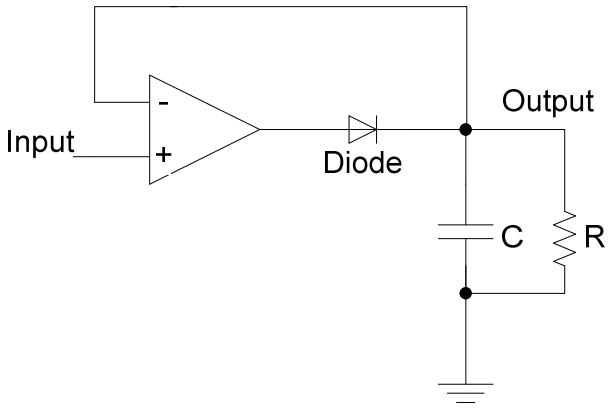

Figure 48 Schematic of conventional peak detector

Current mode peak detector in Figure 49 [15] is commonly used for high frequency applications. An OTA is used to realize voltage to current conversion. It is followed by a precision rectifier and a current mode peak detector. Since the OTA operates in open loop configuration, the peak detector consumes less power than the amplifier based peak detector. However, three peak detectors are needed for filter tuning. Based on our power budget, the total power consumption of the peak detectors are expected to be less than 100uW. Therefore, the power consumption of the current mode peak detector operating at 100MHz is still high compared to our power budget.

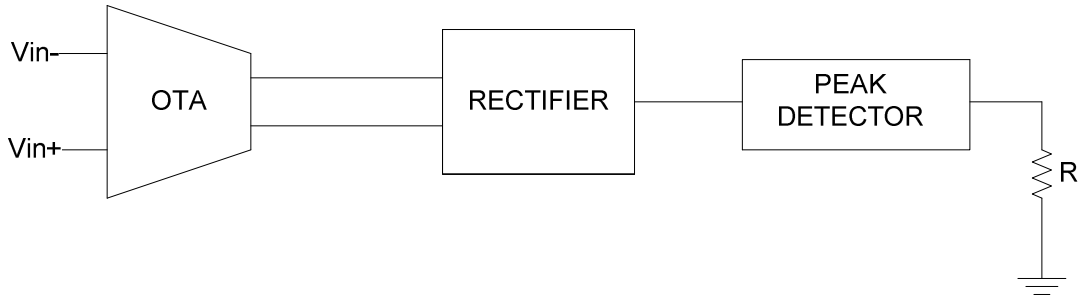

Figure 49 Schematic of current mode peak detector

Alternatively, a simpler source follower peak detector as shown in Figure 50 (a) is use. This peak detector contains only two transistor and one capacitor. It can track the signal magnitude at high frequency without consuming lots of power. With large input signal swing, the transistor acts like a diode. During the positive input signal cycle, the transistor charges up the load capacitor. Since differential RC low pass filter is implemented, a differential mode peak detector is used to take differential input signals as shown in Figure 50 (b).

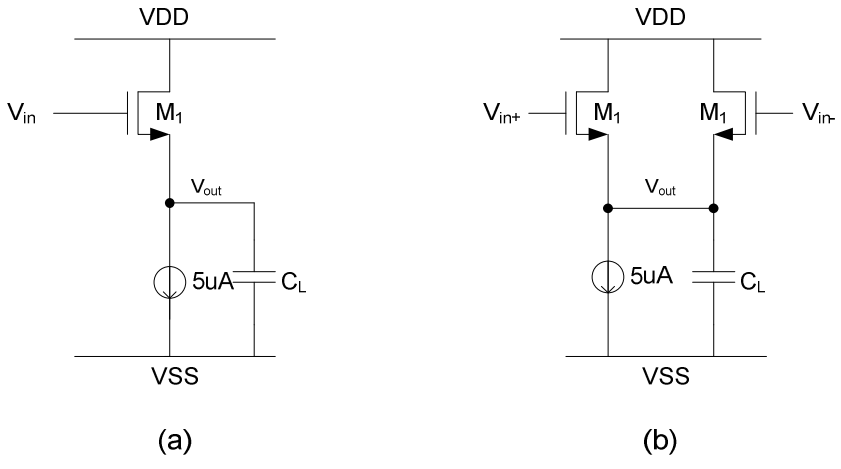

Figure 50 Schematic of 6uW peak detectors (a) Single-ended (b) Differential

The peak detector in Figure 50 (b) consumes only 6uW. The output ripple is around 0.6mV when V_{in}=200mV_{pp}. The DC transfer characteristic is shown in Figure 51 with input frequency of 70MHz. Peak detector's transient response is shown in Figure 52 with input frequency of 70MHz and amplitude sweeping from 100mV to 250mV.

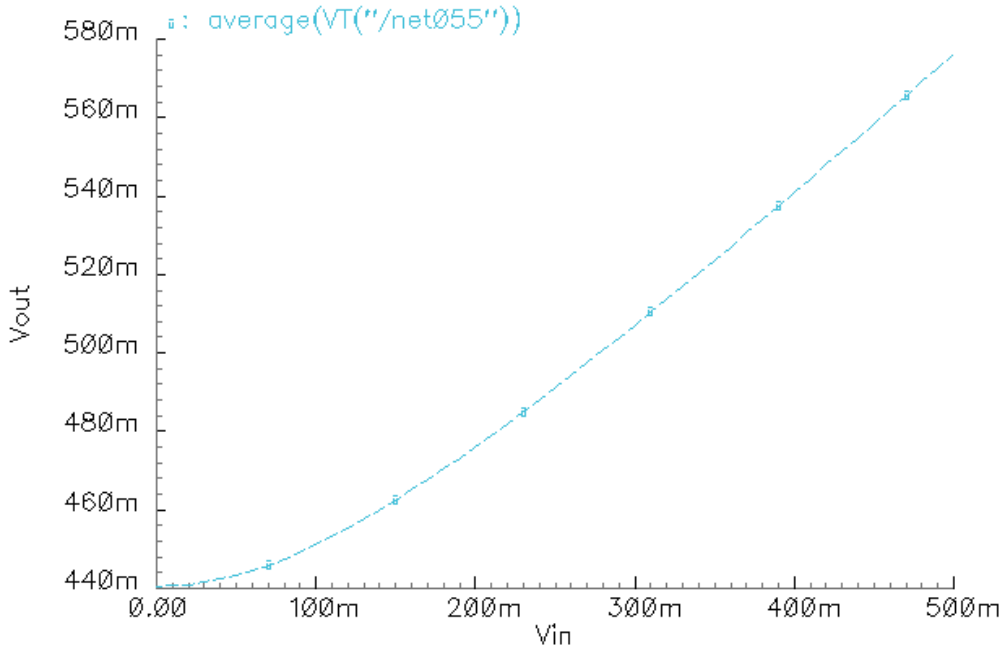

Figure 51 DC transfer characteristic of the peak detector

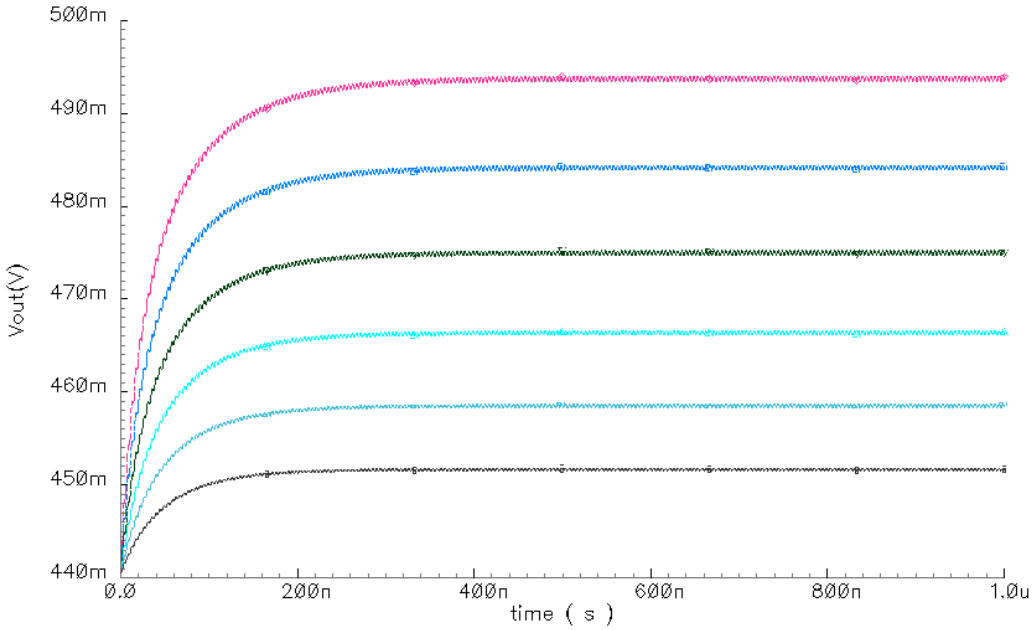

Figure 52 Transient response of 6uW peak detector with input amplitude sweeping from 100mV to 250mV

Although the peak detector is not a high precision and fast tracking detector, using only 6uW power this peak detector design gives the required performance. Figure 53 shows the layout of three peak detectors with area of 0.0261mm^2.

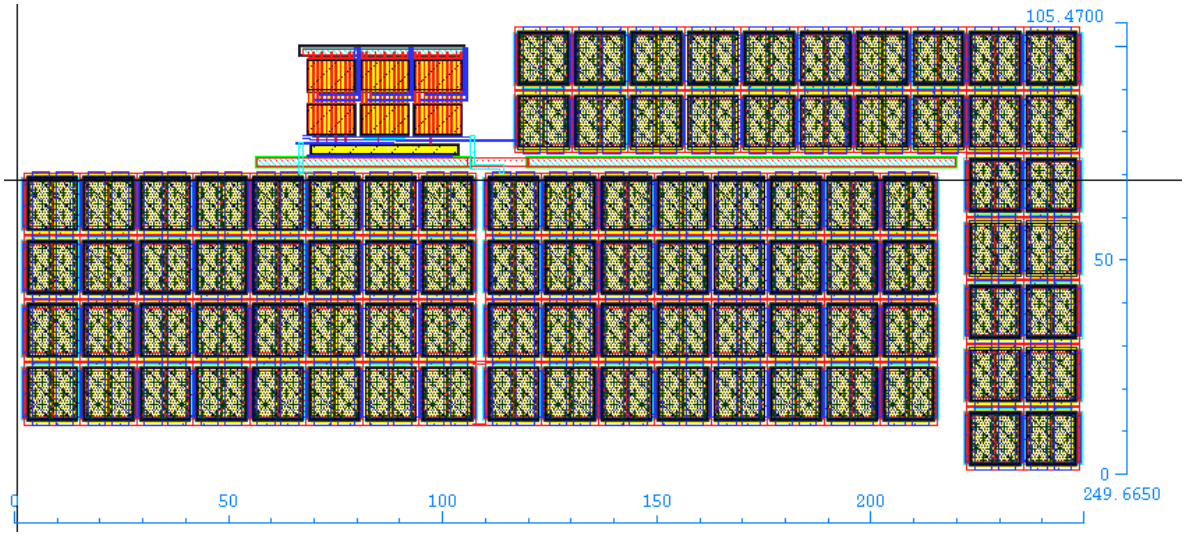

Figure 53 Layout of 6uW peak detector with area of 0.0261mm^2

5.4.5 Design of 3-stage Open Loop Comparator

Comparators are widely used in analog-to-digital converter circuits. There are two main comparator types: open-loop comparator and regenerative comparator. The open-loop comparator is an op-amp based topology without frequency compensation. Regenerative comparators use positive feedback to accomplish the comparison of input signals, which generates a very fast output. Nevertheless, the speed of this automatic tuning circuit is not a main issue due to the specified FM radio tuning time of 50ms. Moreover, this type of comparator requires two phases of operation, which increases the circuit complexity. Hence, the open-loop comparator design is chosen. The transfer function of a two-stage open-loop comparator is estimated by

$$A(s) = \frac{A}{(s/p_1 + 1)(s/p_2 + 1)} \tag{5.6}$$

where p_1 and p_2 are the dominant and second pole. Here, the speed of an open-loop comparator is first estimated through its dominant pole. The final design value is obtained through circuit simulation. It is estimated by

$$A(s) \approx \frac{A}{(s/p_1 + 1)} \tag{5.7}$$

The single pole system's propagation delay time with respect to a small step input is estimated by

$$t_p = 1/p_1 \ln(2) \tag{5.8}$$

where t_p is the propagation delay time. The automatic tuning circuit's clock frequency is from 136.25KHz to 212.5KHz. Based on tuning circuit clock period, the required t_p is estimated, which is chosen to be 7% of the clock period. Based on (5.8), the dominant pole is calculated to be around 2MHz. Our comparator simulation indicates that the speed of the comparator is slew limited. One way is to use a push-pull inverter, which relaxes the slew rate limitation. So, two-stage open-loop amplifier with a push-pull inverter is used as shown in Figure 54.

Input offset voltage is a very important performance characteristic for a comparator. The random mismatch of the input differential stage transistors introduces the input-offset voltage. Large input transistor sizes are used to reduce mismatch. Figure 55 shows the layout of the comparator with die area of 0.0028mm^2.

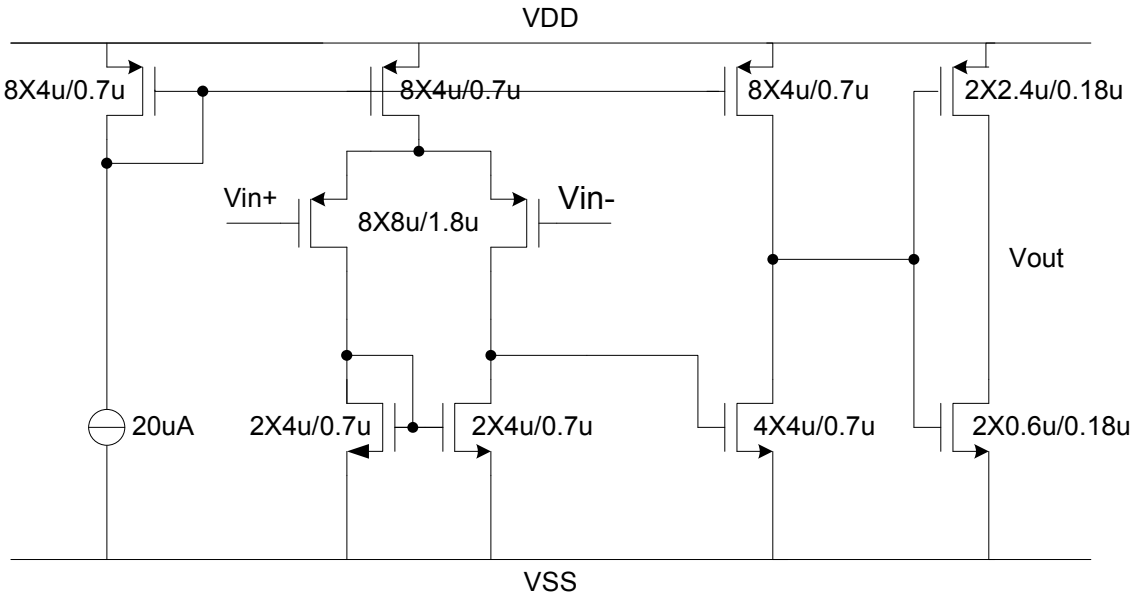

Figure 54 Schematic of 2-stage open loop comparator with a push-pull inverter

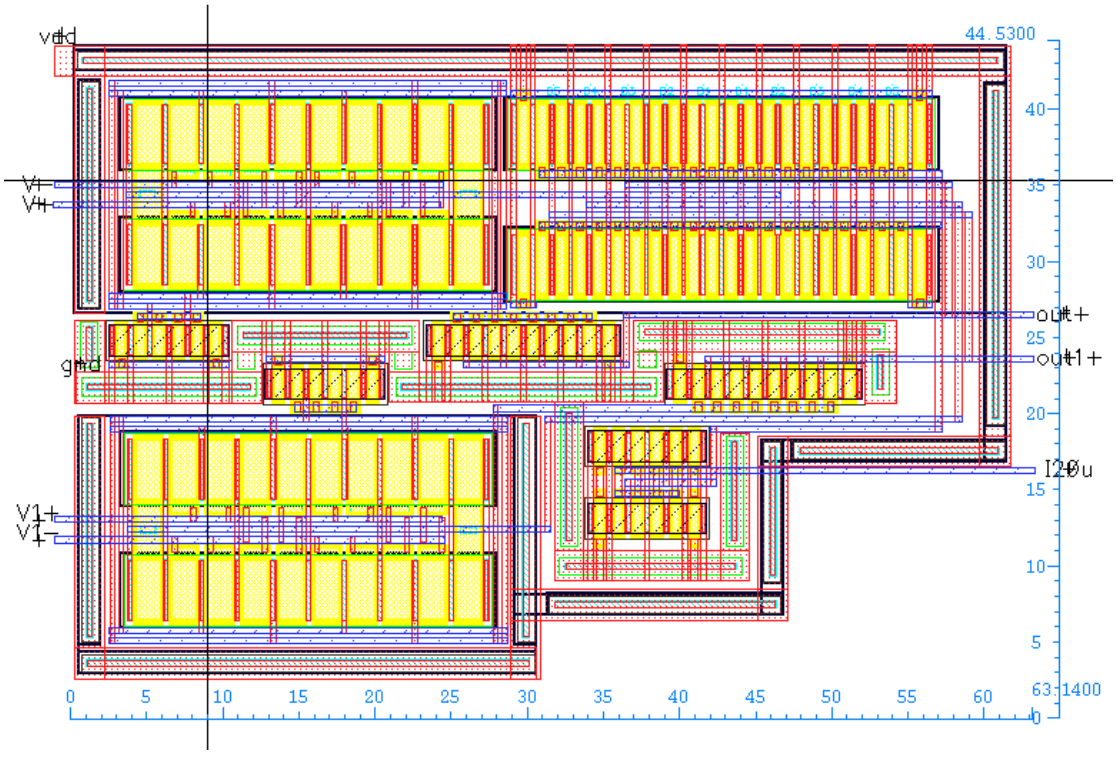

Figure 55 Layout of the 2-stage open loop comparator with area of 0.0028mm^2

5.5 Post Layout Simulation Results

The RC low pass filter connected to the harmonic rejection filter is measured together during the post layout simulation. Figure 56 shows the filtered differential FM signals with 110mV$_{PP}$ input from the RC low pass filter. The FM carrier's THD is -53dB. The highest harmonic above 800MHz is at -99dB as shown in Figure 57.

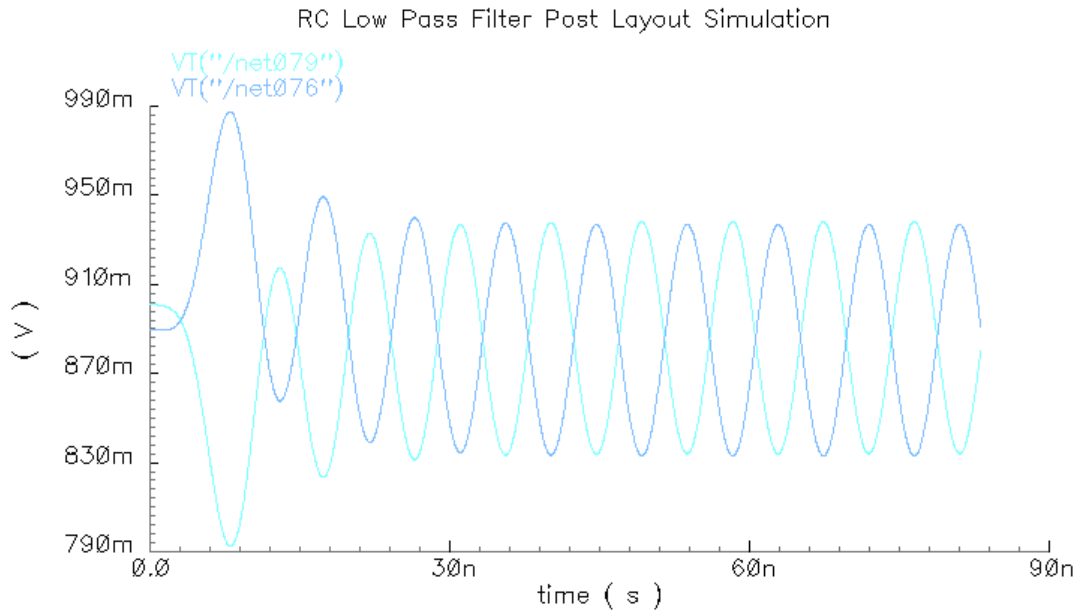

Figure 56 Post layout transient simulation of RC low pass filter's differential outputs with -53dB THD

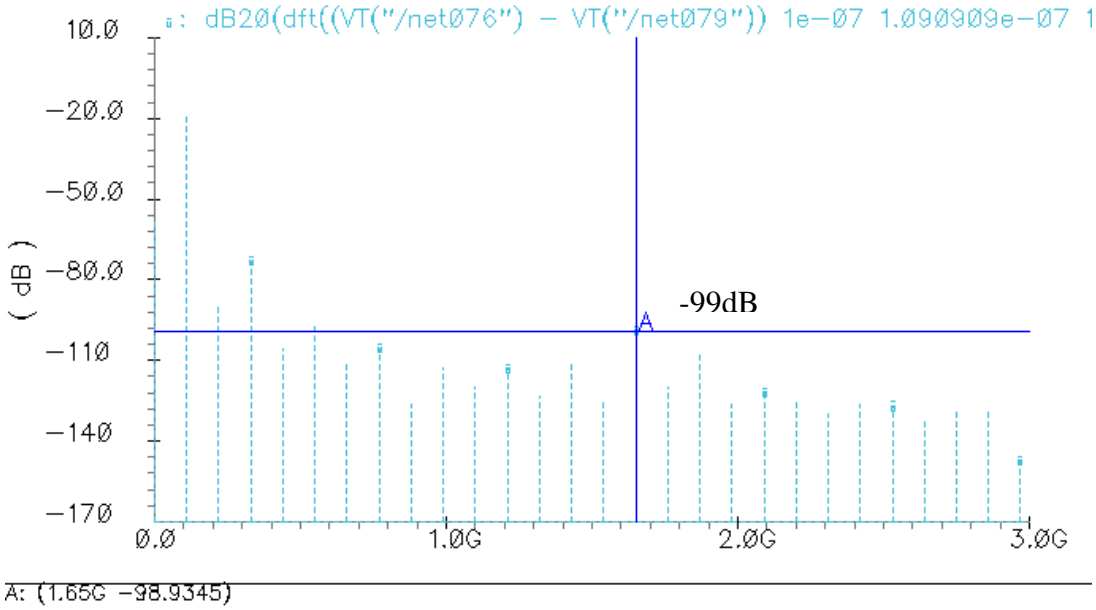

Figure 57 Post layout FFT simulation of RC low pass filter's differential outputs

RC filter's automatic tuning is tested during the post layout simulation. Using 110MHz FM frequency, the filter requires 1.3us to finish tuning as shown in Figure 58. The layout (Figure 59) of the RC low pass filter with the tuning circuit occupies 0.282mm^2 die area. Due to the size of the capacitors, it is the largest building block in this work.

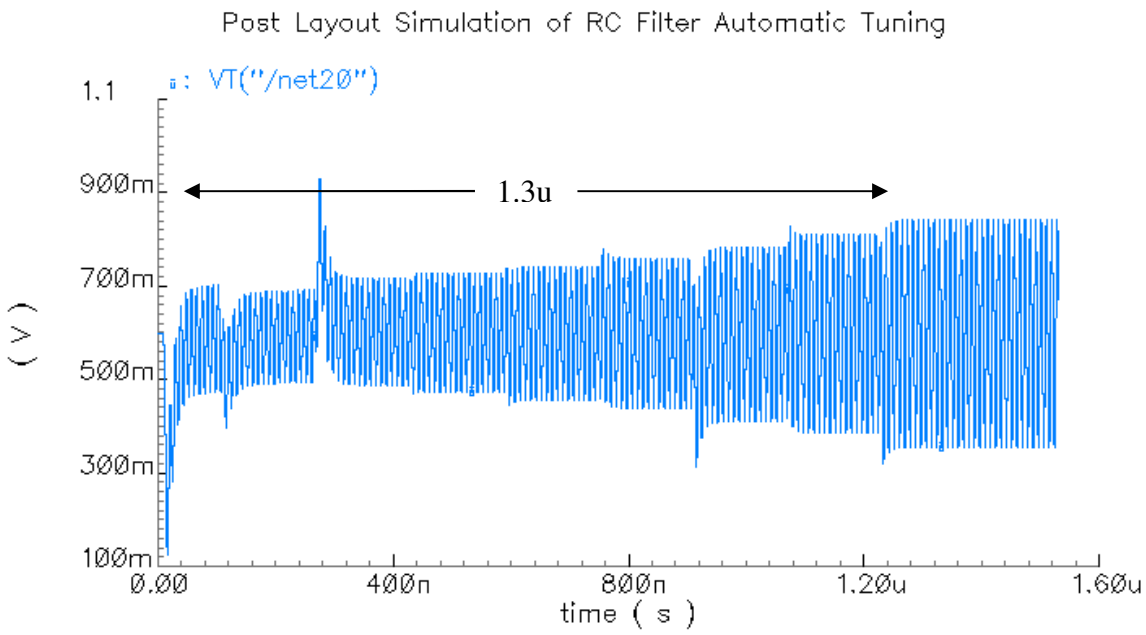

Figure 58 Post layout simulation result of RC filter tuning process

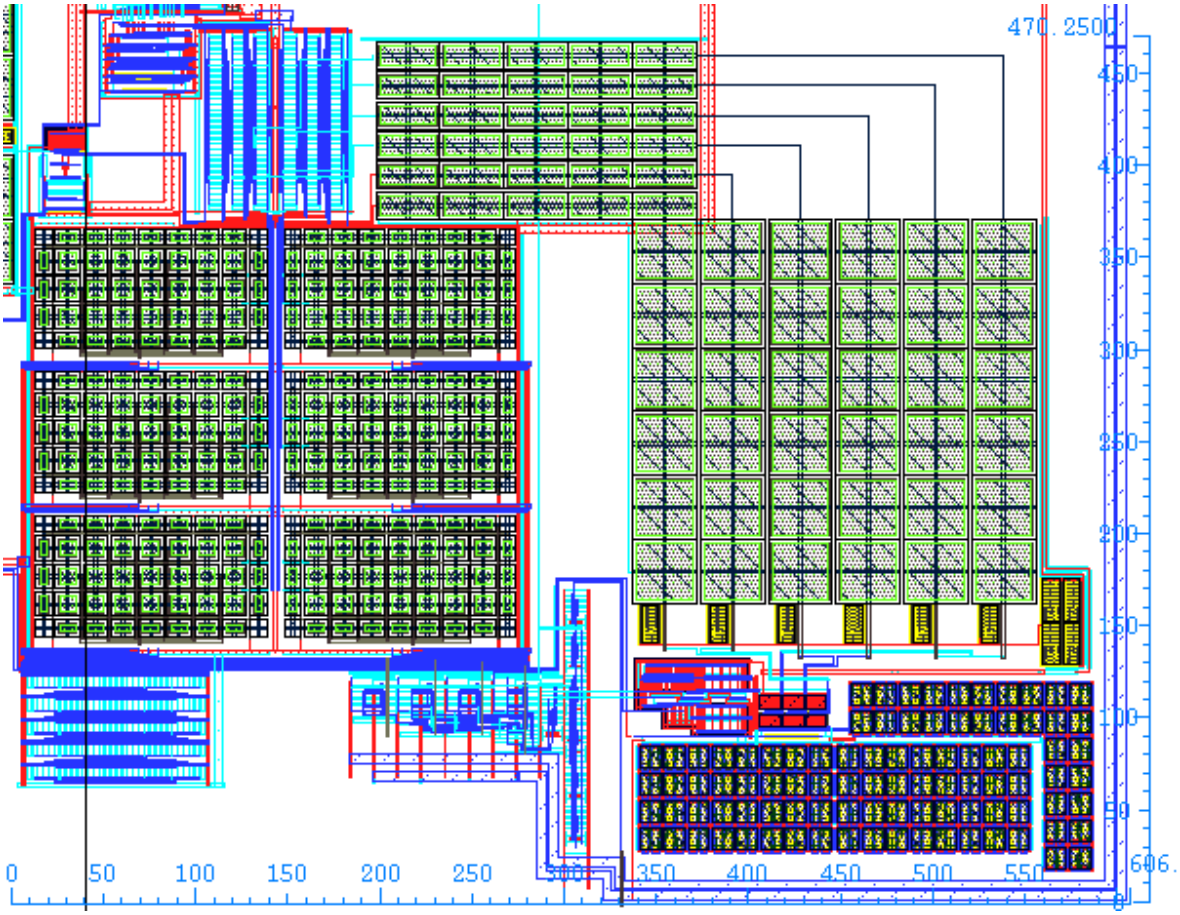

Figure 59 Layout of RC low pass filter with automatic tuning with area of 0.282mm^2

Third-order RC filter post layout simulation meets the design expectation in terms of linearity. The final output signal's linearity is limited by output buffer stage.

Table 13 shows the performance results of the RC automatic tuning filter with harmonic rejection input signal.

Table 13 RC automatic tuning filter post layout simulation

Performance Parameter	Value
THD	-53dB
High Frequency Harmonics	-99dB
Tuning Time	1.3us
Resolution	6MHz
Power	0.25mW
Area	0.282 mm^2

CHAPTER VI

CLASS-AB OUTPUT STAGE

6.1 Differential to Single-ended Conversion Using A Transconductor

An output buffer stage is designed to drive the differential output signals from the outputs of RC passive low pass filter onto a 50Ω resistive load. Theoretically, a differential amplifier could be used to convert differential signals into single-ended output as shown in Figure 60. Using this topology, the non-inverting input node $V_{in}+$ changes the common mode voltage V_{cm}. An amplifier in closed loop operation needs to burn a lot of power in order to track the fast common mode voltage fluctuation which is at 110MHz in this design. With the limited power budget, a more efficient circuit implementation is desired.

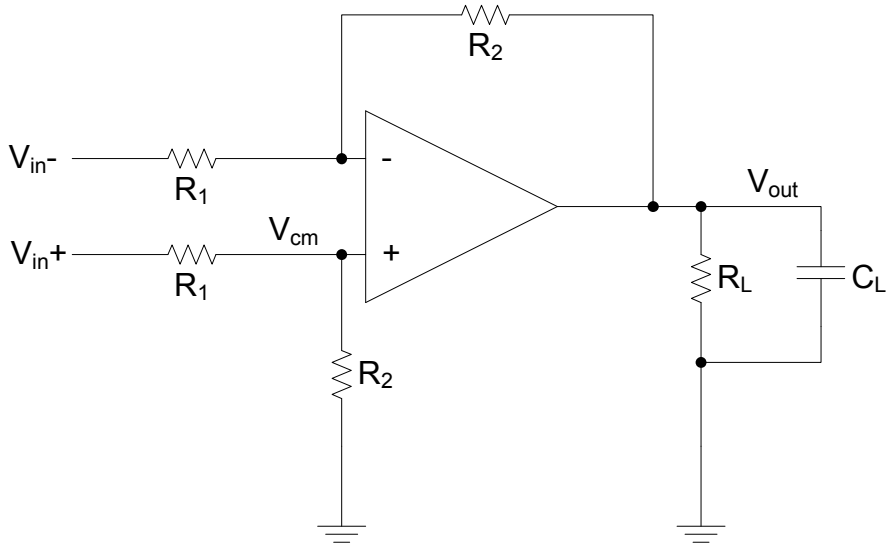

Figure 60 Differential input single-ended output buffer stage

A transimpedance amplifier topology is proposed for this project in order to handle high frequency differential to single-ended conversion as shown in Figure 61. An output transconductor is designed to convert differential input signals into current, which is driven into a transimpedance amplifier. In order to maintain signal's linearity, a transconductor with degeneration resistor is chosen. In addition, the transconductor also acts like a buffer, which provides the RC passive low pass filter stage a high impedance load. In addition, RC filter's differential signals' DC bias is transferred from 0.9V down to 0.6V. 0.9V is designed in the current summation circuit to give the maximum output voltage swing. 0.6V is a perfect DC voltage for 1.2V supply class-AB op-amp complementary input stages.

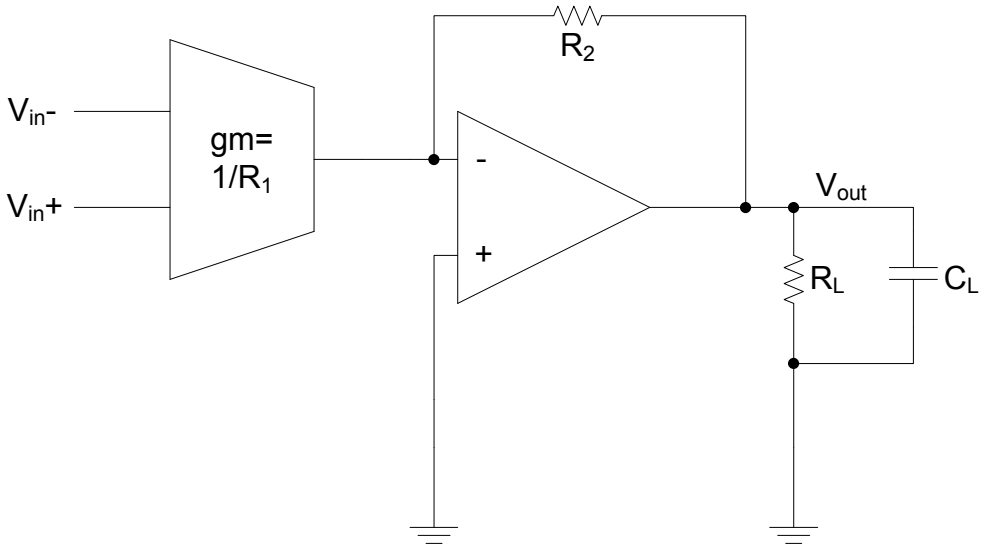

Figure 61 Transconductor with degeneration resistor and transimpedance class-AB amplifier

6.1.1 Design of Resistor Degenerated Transconductor

One of the most commonly used CMOS voltage to current converters is the source degenerated differential transconductor as shown in Figure 62. Its transconductance is estimated by

$$gm = \frac{gm_{1,2}}{1 + gm_{1,2} * 0.5 * R_1} \tag{6.1}$$

where R_1 is the degeneration resistor and $gm_{1,2}$ is the small signal transconductance of transistors $M_{1,2}$. Assuming $gm_{1,2}R_1 >> 1$, the overall transconductance is determined by the degeneration resistance R_1, and is approximated by

$$gm \approx \frac{1}{0.5R_1} \tag{6.2}$$

where gm's dependence on M_1 and M_2 is reduced. The degeneration factor of gm_1R_1 is designed to be 7. Thus, the transconductor behaves more linearly than a regular non-degenerated differential transconductor. In some applications, a MOS transistor in triode region is used to replace degeneration resistor in order to save chip area and have tunable transconductance. In this application, chip area is not the main concern and the transconductance is fixed. The degeneration resistor R_1 is matched with the output stage feedback resistor R_2 in the layout. The resistance process variation is cancelled by matching of the degeneration resistor R_1 and feedback resistor R_2.

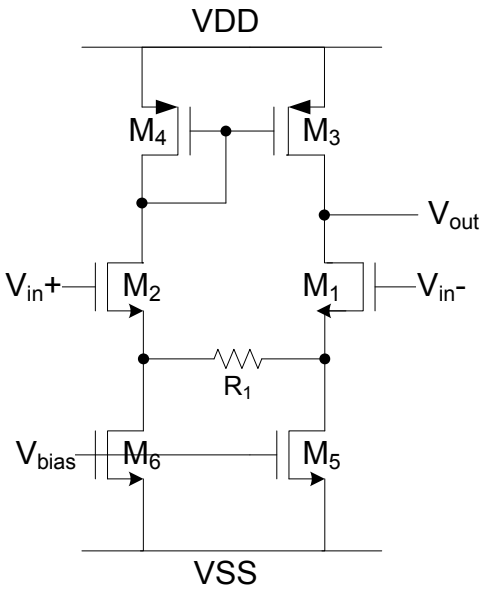

Figure 62 Schematic of the transconductor with degeneration resistor

6.1.2 Transconductor with Degeneration Resistor Simulation Results

The circuit transconductance is measured during the post layout simulation. Within $80mV_{pp}$ input swing, the transconductance varies within 0.02% as shown in Figure 63.

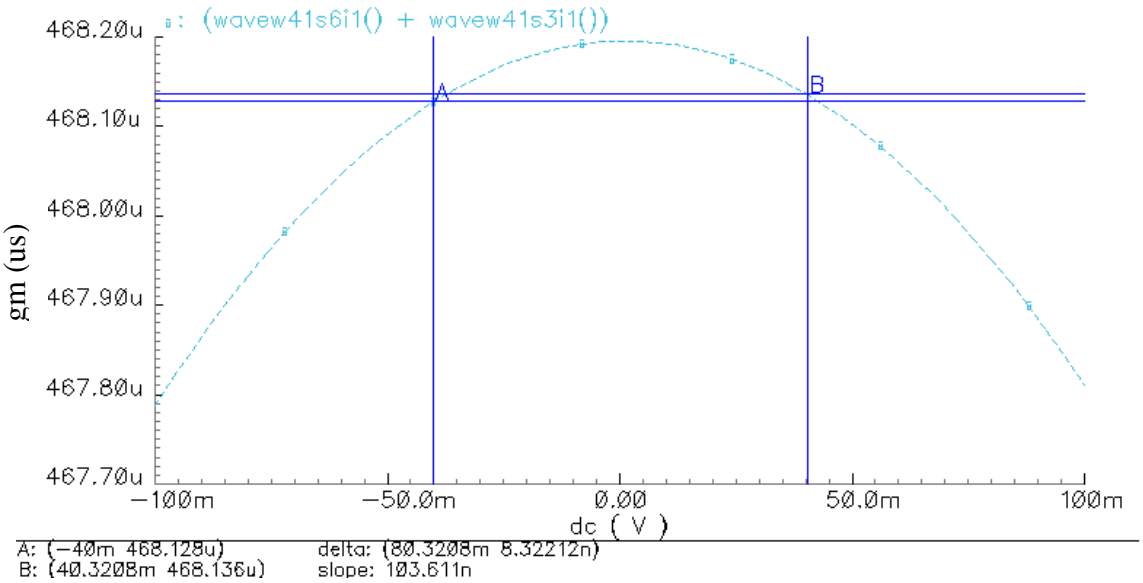

Figure 63 Output transconductor's gm vs. input voltage swing

The linearity of the transconductor is measured by feeding ideal $66mV_{pp}$ differential inputs at 110MHz to the transconductor's input and connecting an ideal transimpedance amplifier to its output. $66mV_{pp}$ differential inputs are RC passive low pass filter's output signal level. The measured amplifier's output THD is -61dB. Figure 64 shows the frequency spectrum of the output signal. Measured high frequency harmonics level is below -110dB. IM3 is also simulated with the actual designed output buffer and transconductor using 110MHz and 120MHz signals. IM3 is measured to be 47dBc. Figure 66 shows the result of IM3 simulation. The simulations show that the transconductor with degeneration resistor does not introduce significant distortion across the frequency of the interest. Both THD and high frequency harmonic level have met the specification. In fact, the class-AB amplifier's linearity performance will be the limiting

factor for signal linearity. The performance of the class-AB amplifier will be discussed in the end of this Chapter.

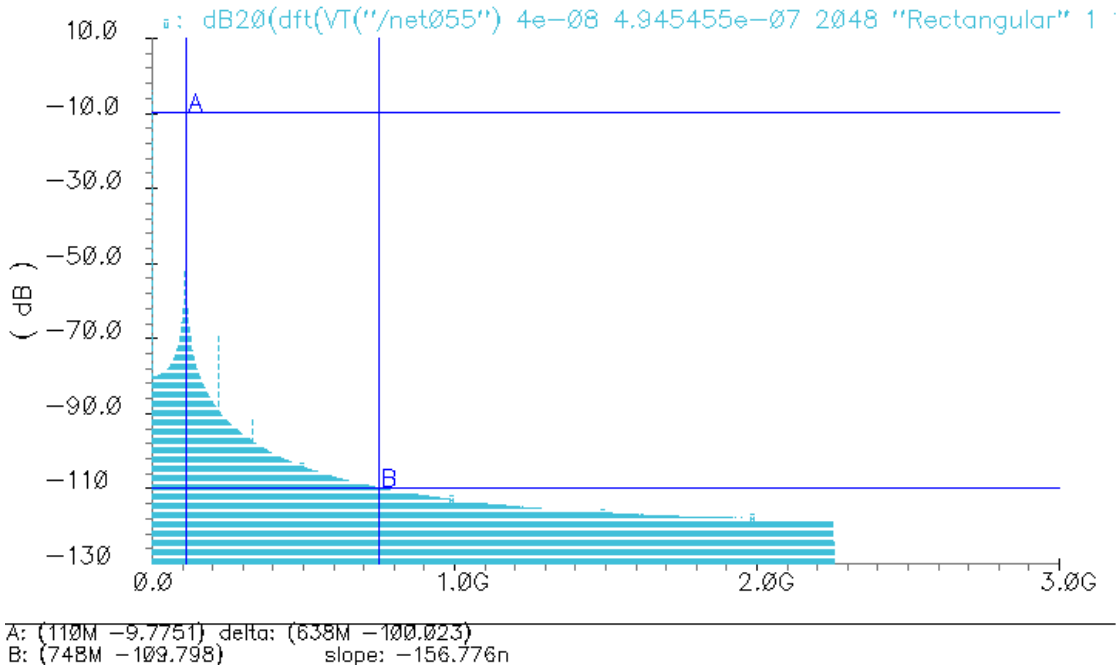

Figure 64 Frequency spectrum of ideal buffer's output signal with the transconductor

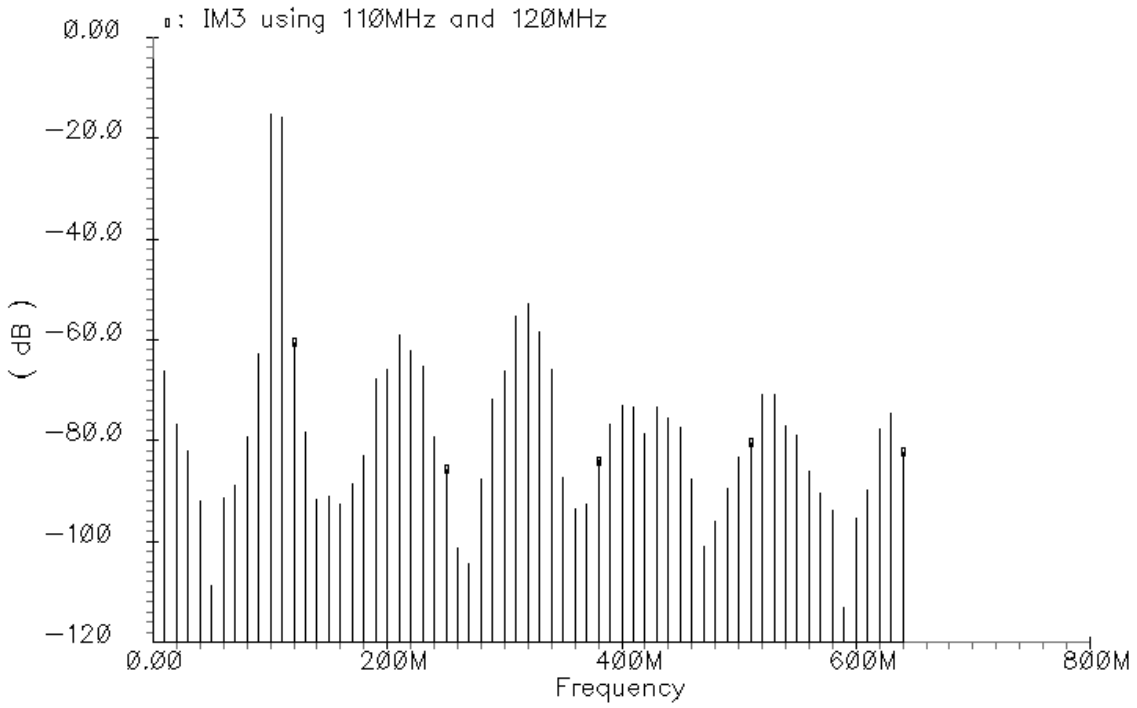

Figure 65 IM3 of the buffer with the transconductor's output signal

The transconductor is designed and laid out in TSMC 0.18um technology as shown in Figure 66. In order to minimize circuit mismatch, common centroid topology was used during the layout, and minimum transistor length was avoided. Total die area of the transconductor is $0.00115 mm^2$. Table 14 shows the simulated performance parameter for the transconductor.

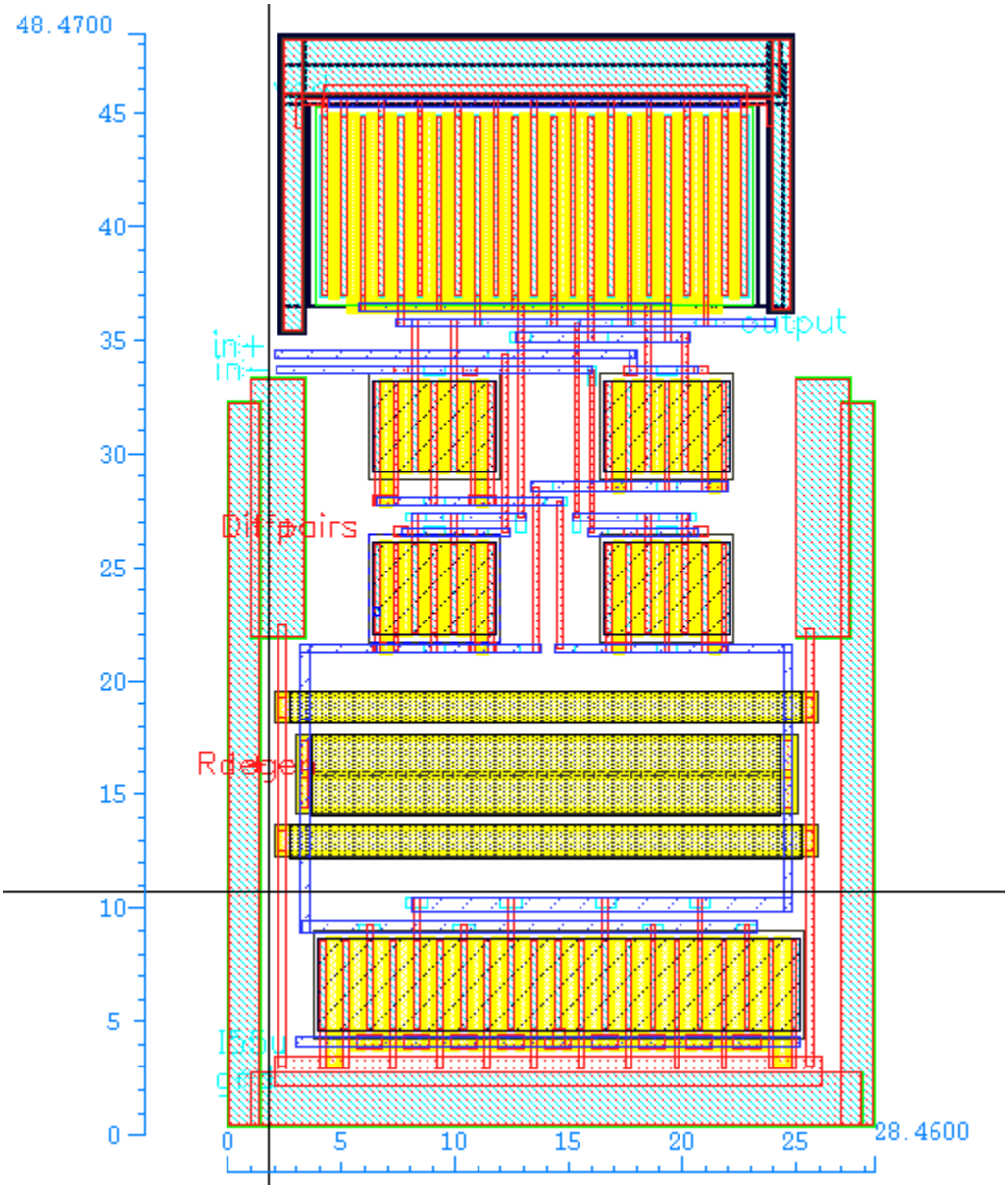

Figure 66 Layout of the transconductor with degeneration resistor with area of $0.00115mm^2$

Table 14 Post layout simulation performance of degenerated transconductor

Parameter	Post Layout Simulation
gm variation (Vin=80mVpp)	0.02%
Power	0.509mW
Area	0.00115mm^2
Technology	TSMC 0.18um

6.2 Design of Output Buffer Stage

6.2.1 Background

Driving a 50Ω load at 110MHz requires a high performance output stage featuring high efficiency, good current drive capability, and excellent frequency response. High efficiency is defined as the ratio of the output power vs. the average power drawn from supplies [2]. Good current driving capability is described as the ability to drive a low resistive load and preserve signal linearity.

Class-AB output stage has good balance of current driving capability and power efficiency. Many different class-AB output stages have been proposed [16][17][18][19]. Many of them were developed before the low voltage CMOS era. For those output stages designed for the low voltage supply [20][21][22][23], very few of them could handle high frequency operation. The complexity of the output stages degrades the high frequency performance of output stages. Usually, simpler circuit design gives better high frequency performance [24]. Many of output stages use internal feedback loop to control output transistors' quiescent current [20]. This is very effective for low frequency application where the amplifier operating frequency is low compared to the bandwidth

of its class-AB output stage's internal feedback control loop. However, for high frequency application, it is very difficult to design a class-AB output stage's internal feedback control loop.

Source followers and common-source topologies are widely used in design of output stages. Source followers exhibit low output impedance, compared to the common-source output stages. However, source followers' voltage headroom is limited by two threshold voltages, so they are not suitable for low voltage application. Therefore, common source output stage as shown in Figure 67 (b) is used in this research.

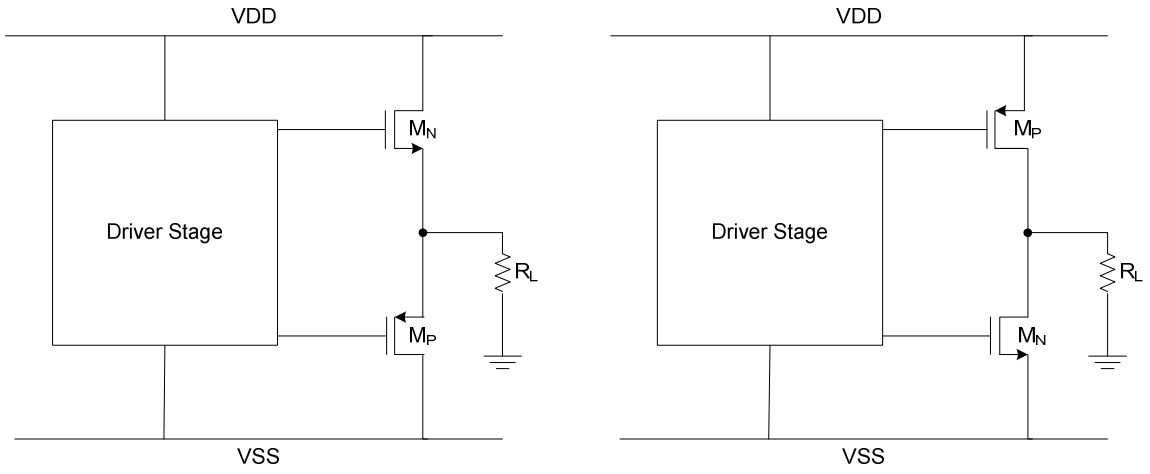

Figure 67 Class-AB output stage (a) source followers and (b) common source

Theoretically, the maximum efficiency of a class-AB amplifier is 78.6% [25]. It is calculated based on the output stage's maximum output power vs. average power

drawn from its supplies. The power consumed by the input stages and frequency compensation stages is not counted into the class-AB efficiency calculation. Therefore, in this work, the efficiency is calculated based on the output stage only.

6.2.2 Class-AB Stage with Adaptive Load

A class-AB stage with adaptive load was proposed in [26] as shown in Figure 68. It has better high frequency performance than the class-AB output stage's internal feedback loop design [24].

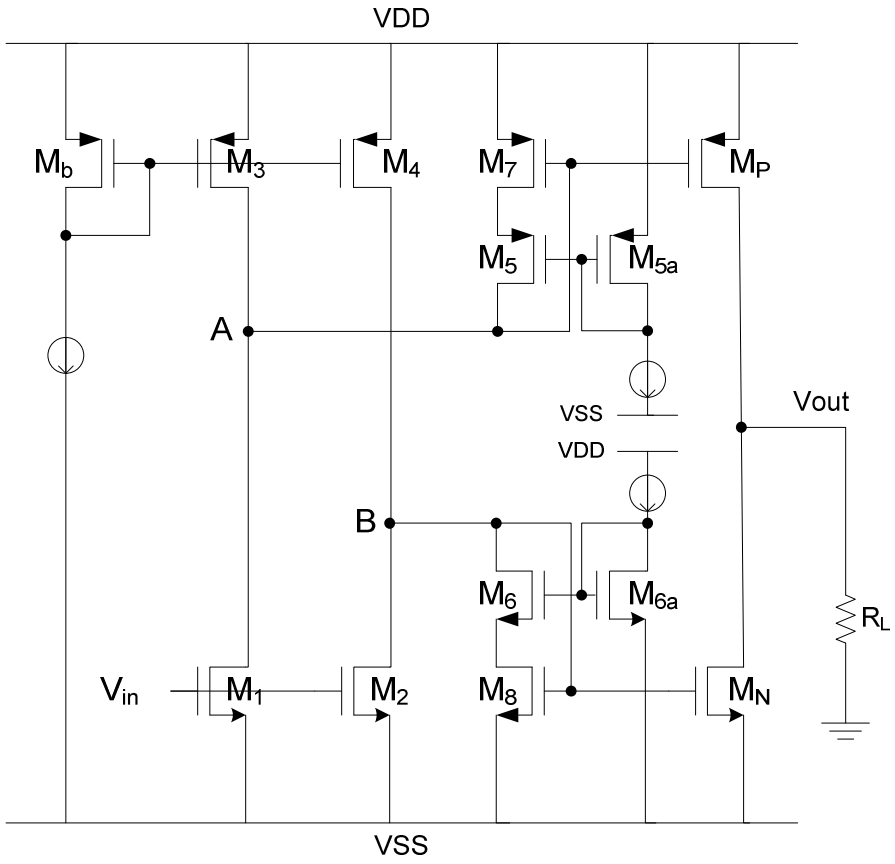

Figure 68 Schematic of a class-AB adaptive load output stage [26]

MP and MN in Figure 68 are controlled by the adaptive load M_5/ M_7 and M_6/M_8 transistors. Diode-connected transistors M_7 and M_8 are used to control output quiescent current. Cascode transistors M_6 and M_5 are used to increase the output impedance of the diode connected transistors M_7 and M_8. At the quiescent point, the output impedance looking into the drain of M_6 as shown in Figure 69 (b) is calculated as

$$r_{out} = \frac{r_{o6} + r_{o8} + r_{o6}r_{o8}gm_6}{1 + gm_8gm_6r_{o6}r_{o8} + gm_8r_{o8}} \approx \frac{1}{gm_8} \tag{6.3}$$

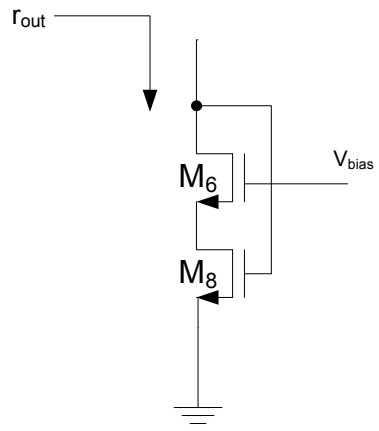

Figure 69 Cascade diode connected load

However, during class B mode (operating mode), due to the cascode transistor M_5/M_6 as shown in Figure 68, M_7/M_8 is forced into linear region, the output impedance looking into the drain of M_5/M_6 increases as the driving signal swing increases, which increases the driving capability of the intermediate stage M_1-M_4. In class B mode, r_{out} is estimated by

$$r_{out} = \frac{1}{\mu_n C_{ox} \frac{W}{L} V_{DS8}} > \frac{1}{gm_8} \tag{6.4}$$

At the quiescent point, the two diode-connected transistors M_8 and M_7 with MN and MP can be viewed as two current mirrors, where the quiescent current in MN and MP is controlled. It may not be the most efficient class-AB output stage control method and cannot minimize the quiescent current in MP and MN, but higher quiescent current is needed for high frequency operation. The quiescent current in MP and MN not only reduces crossover distortion, but also improves the high frequency performance of the output stage. During the class B mode operation, with the cascode transistor M_6/M_5, the diode connected output impedance looking into the drain of M_5/M_6 is boosted to higher value. Due to the boosted output impedance, the current driving capability of M_1 and M_2 is improved.

In order to maximize the performance of the output stage, the output transistors M_N and M_P in Figure 68 should be matched in terms of that transconductances. For the driver stage, M_1 and M_2 in Figure 68 should provide the same amount of gain to M_N and M_P. Considering only small signal analysis, pmos and nmos paths which are highlighted in Figure 70 can be carefully designed to give the same transconductance, assuming matching is perfect. The transconductance of each path is estimated by

$$gm_{pmos\,path} = gm_1 \left(r_{o1} // r_{o3} // \frac{1}{gm_7} \right) gm_p \tag{6.5}$$

$$gm_{nmos\,path} = gm_2 \left(r_{o2} // r_{o4} // \frac{1}{gm_8} \right) gm_n \tag{6.6}$$

However, during large signal operation, pmos and nmos paths as shown in Figure 70 are inherently unbalanced in the design. M_1 and M_2 function as a pair of pull-down transistors. Both M_1 and M_2 have the high driving capability when pulling down the node A and node B. In a well designed class-AB output stage, a pulling down transistor is to drive PMOS and a pushing up transistor is to drive NMOS. Here, M_2 is used to drive M_N, where the path transconductance is not maximized. The nmos path is equivalent to the driving path in a two-stage amplifier with M_1 and M_6 as a driver as shown in Figure 71.

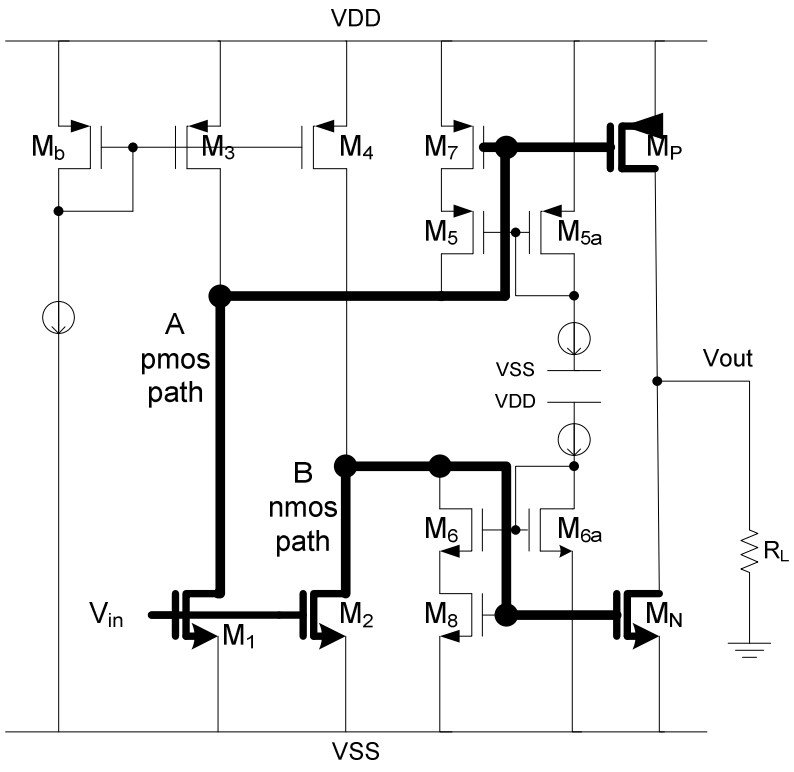

Figure 70 Schematic of the class-AB adaptive load output stage [26] with highlighted pmos path and nmos path

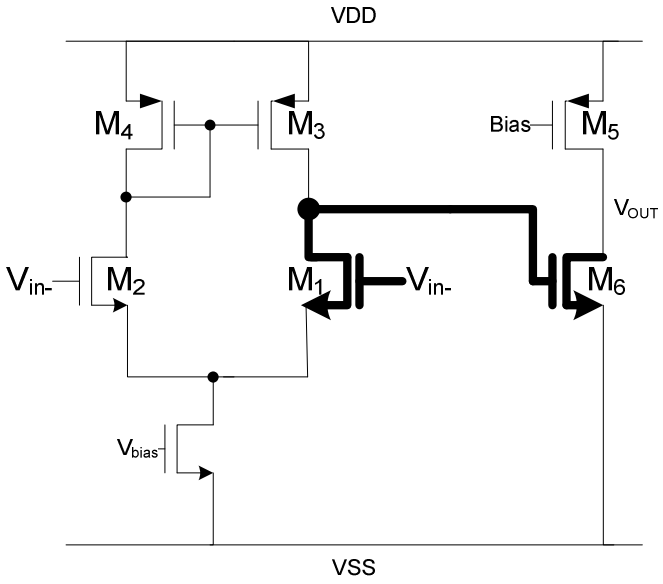

Figure 71 Two-stage amplifier with two NMOS as drivers

In Figure 70, M_1 and M_2 do not drive the adaptive loads equally. When M_2's gate voltage lowers down, the voltage at node B cannot increase to VDD-$V_{dsat}(M_4)$. The adaptive load M_6 and M_8 conducts current, which pull the node B voltage lower than VDD-$V_{dsat}(M_4)$. The adaptive load M_6 and M_8 works against M_2 to drive M_N. On the other hand, the adaptive load M_5 and M_7 nicely follows driver M_1 to drive M_P. Due to this unbalanced design, it is very difficult to design the pmos and nmos driving paths. In fact, with M_N and M_P in balanced $\beta_{pmos}/\beta_{nmos}$ ratio, M_N is always weaker than M_P, which is opposite to a balanced output stage. This unbalanced design greatly weakens the performance of the whole output buffer and introduces design confusion.

6.2.3 Proposed Fully Balanced Class-AB Output Stage Solution

A symmetric driver stage is proposed to provide the balanced driving capability for both M_N and M_P as shown in Figure 72. The intermediate driver transistors M_1 and M_4 provide balanced driving capability. Originally, both M_N and M_P are driven by two nmos transistors, which are pull-down transistors. In this design, M_N's driver in Figure 70 is replaced by a PMOS transistor M_4 as shown in Figure 72. The nmos and pmos driving paths are complementary where M_N output transistor is driven by M_4 and M_P output transistor is driven by M_1. By using this complementary structure, the output stage is balanced. Current driving capability of the output stage M_n and M_p is improved through their complementary drivers M_1 and M_4.

For the input stage of the class-AB amplifier, complementary differential pairs are used to drive pmos path and nmos path as shown in Figure 73. Using both nmos and pmos differential pairs not only maintains the balanced pmos and nmos paths, but also increases the class-AB amplifier input common mode range.

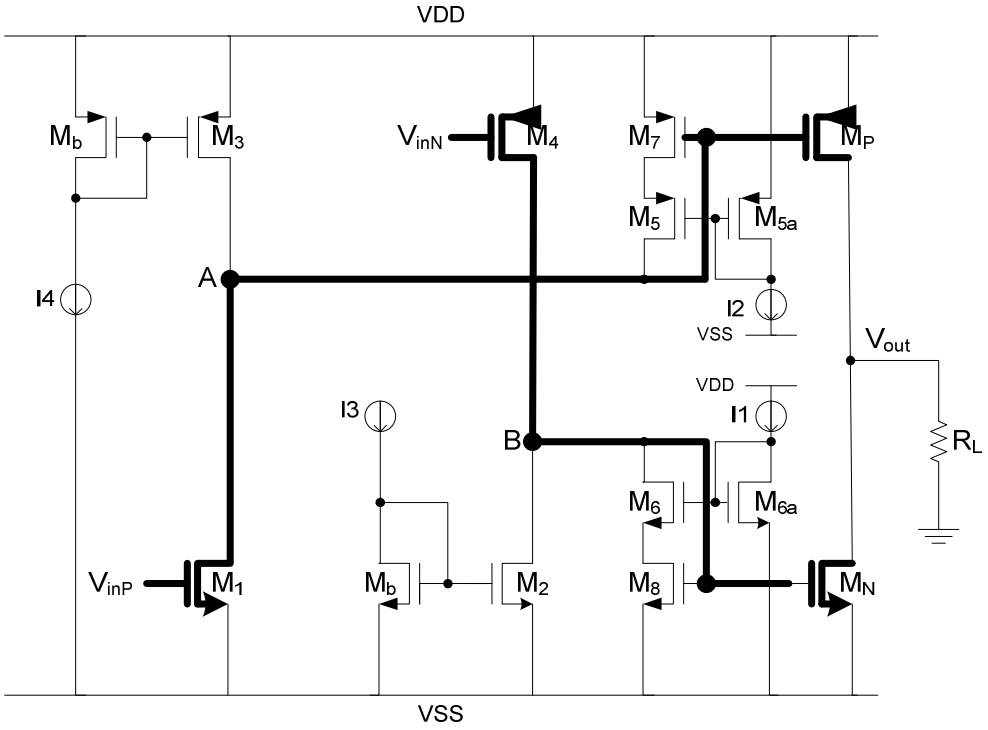

Figure 72 Proposed fully balanced class-AB output stage

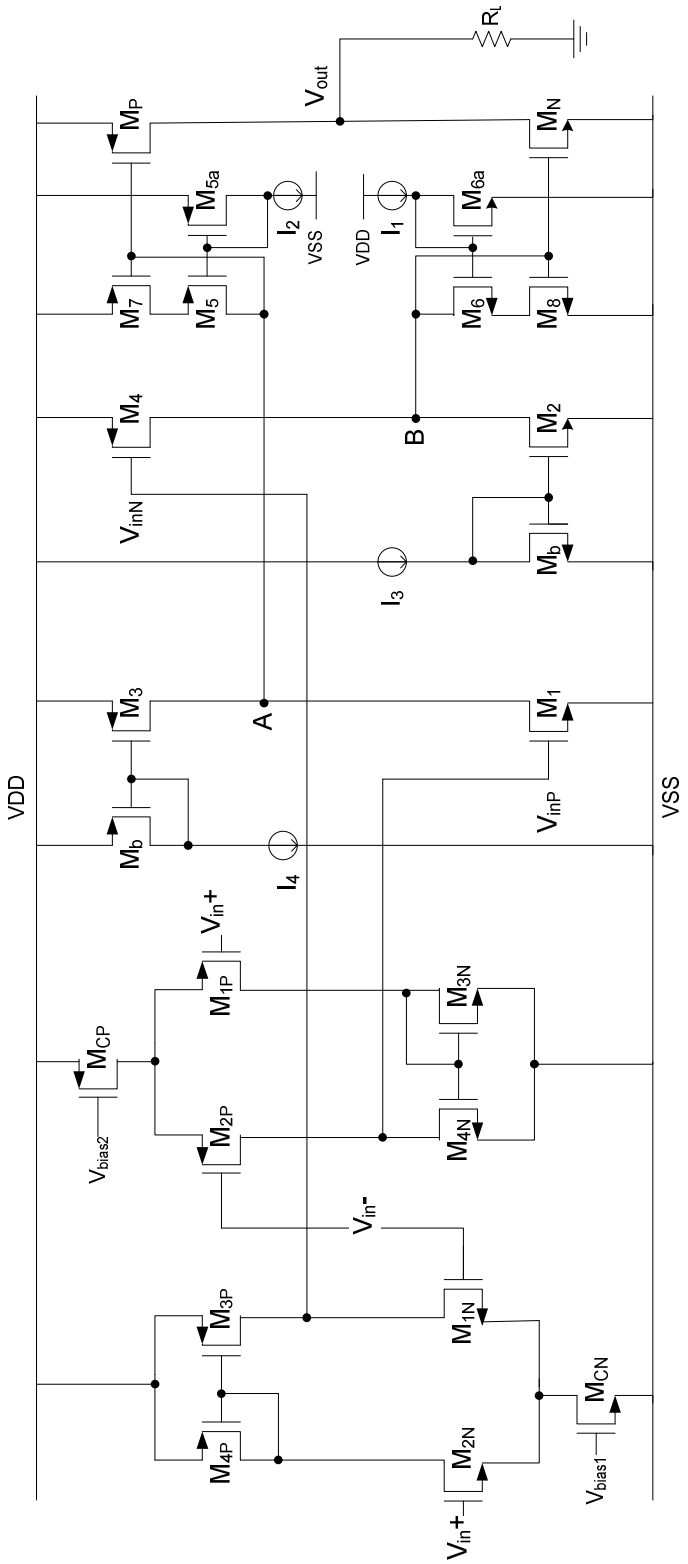

Figure 73 Proposed fully balanced class-AB operational amplifier (uncompensated)

6.3 Design of Class-AB Amplifier Frequency Compensation Circuit

For multi stage amplifier, many frequency compensation techniques have been proposed in order to extend the op-amp operating frequency. It is very important for this project to use the right compensation scheme to realize high frequency and low power performance. Three-stage amplifier is illustrated in Figure 74. The first two stages are for amplification. The third-stage provides low resistive driving capability.

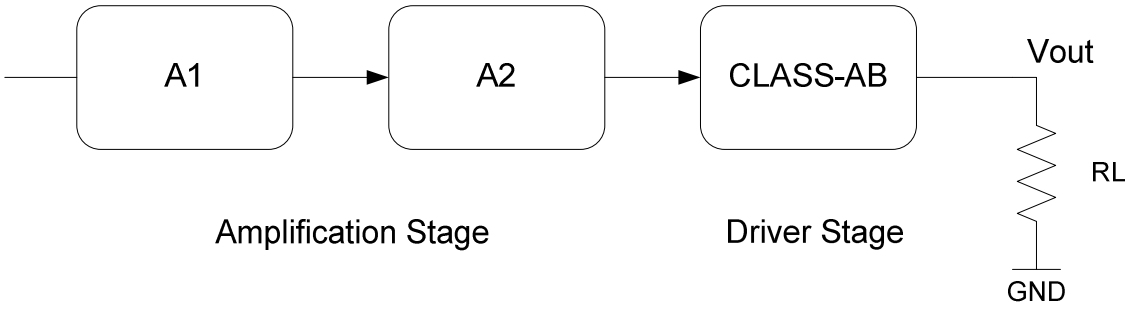

Figure 74 Block diagram of an operational amplifier

6.3.1 Miller Capacitor Compensation

Miller capacitor compensation is the most effective and widely used compensation technique. An uncompensated two-stage op-amp as shown in Figure 75 contains two poles. Those two poles are given by the following equations:

$$p_1 = \frac{-1}{r_1 C_1} \tag{6.7}$$

$$p_2 = \frac{-1}{r_2 C_2} \tag{6.8}$$

where r_1 and r_2 are the resistance seen from the output nodes of the first and second stages and C_1 and C_2 are the capacitances associated to the first and second stage output nodes. In most cases, those two poles are close to each other, which make the phase margin of the op-amp less than 45º.

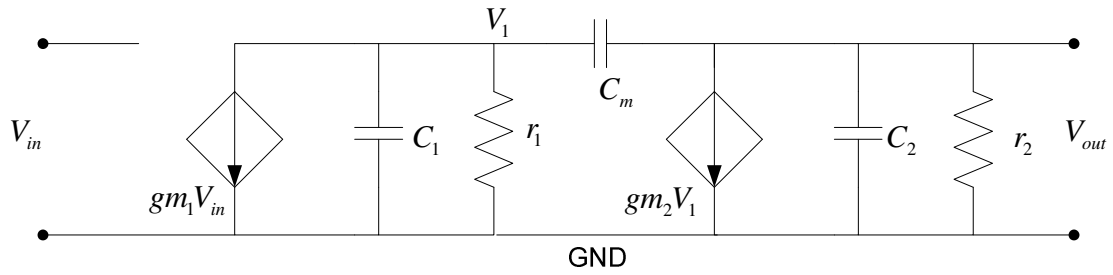

Figure 75 Small signal equivalent circuit of two-stage OTA

Miller effect is used for compensation by applying a capacitor between the first stage output and the second stage output. The effective added capacitance seen at the output of the first and second stage is estimated by

$$C_{1st\ stage} = C_m(1 + A_2) \tag{6.9}$$

$$C_{2st\ stage} = C_m(1 - A_2{}^{-1}) \tag{6.10}$$

where C_m is the miller capacitor and A_2 is the second stage amplification. With the miller capacitor effect, the first stage pole is shifted close to DC frequency and it is estimated by

$$p_1 \approx \frac{-1}{r_1 * A_2 * C_m} = \frac{-1}{r_1 * gm_2 * r_2 * C_m} \tag{6.11}$$

The second pole of the two-stage amplifier is pushed away from the previous location due to the effective diode connected second stage caused by the miller capacitor, which reduces resistance seen from the output to 1/gm. The second pole with miller capacitance effect is estimated by

$$p_2 \approx \frac{-gm_2}{C_2} \tag{6.12}$$

where C_2 is equal to load capacitance, which is assumed to be greater than C_m. Due to the miller capacitance effect, a RHP zero is created. The RHP zero comes from the output signal cancellation through two signal paths. Basically, the miller capacitor functions as a feedforward path across the output stage, which cancels the output signal at the frequency of the zero. It is estimated by

$$Z_1 \approx \frac{gm_2}{C_m} \tag{6.13}$$

This undesired RHP zero can be pushed away from origin through a nulling resistor in series with miller capacitor. The new zero is estimated by

$$Z_1' \approx \frac{1}{C_m\left(\frac{1}{gm2} - R_{null}\right)} \tag{6.14}$$

Miller compensation is very effective for two-stage op-amp frequency compensation, but it sacrifices GBW for better phase margin.

6.3.2 Nested Miller Compensation

Nested Miller Compensation (NMC) as shown in Figure 76 [27] is one of the most effective multi-stage compensation schemes. The unity-gain frequency of NMC multi-stage amplifier is set by the first stage transconductance. This unity-gain frequency is half of the two-stage amplifier's unity-gain frequency in order to maintain 60º phase margin. The bandwidth of a three-stage amplifier is one quarter of the limiting pole's frequency. The NMC is a robust way to compensate a multi-stage amplifier without using pole-zero cancellation techniques. However, due to the bandwidth reduction, it needs to consume much more power than a two-stage amplifier to reach the specified operating frequency.

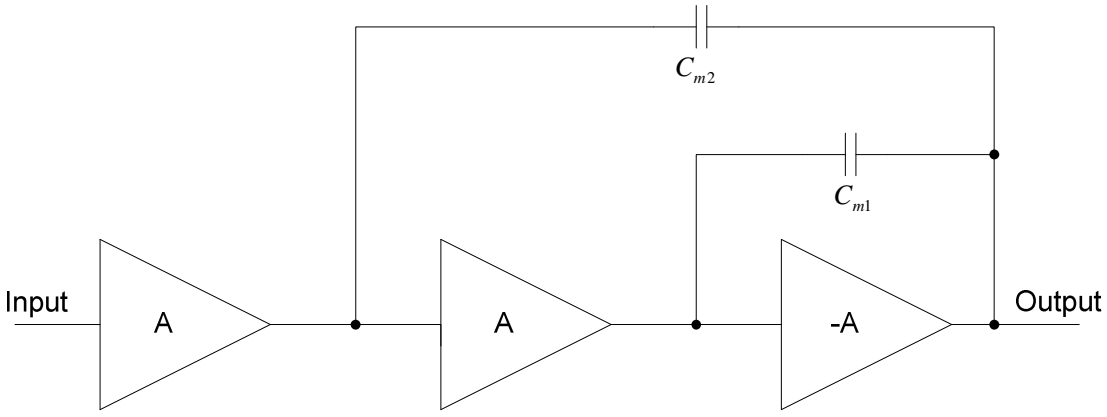

Figure 76 Nested miller compensation (NMC)

6.3.3 Multipath Nested Miller Compensation

Due to NMC's reduction of gain-bandwidth product, the multipath nested miller compensation (MNMC) as shown in Figure 77 [28] was developed in order to regain the loss of the bandwidth.

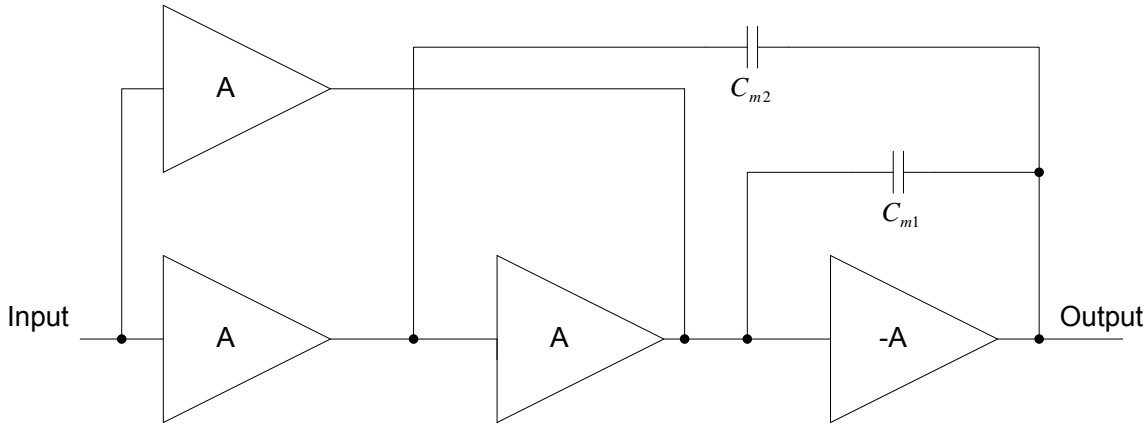

Figure 77 Multipath nested miller compensation (MNMC)

A second input stage is used to form a two-stage amplifier which is in parallel with three-stage NMC amplifier. At low frequency, three-stage NMC provides large gain, while at high frequency, the two-stage amplifier extends the high frequency gain and gain bandwidth product. However, the crossover point between three-stage and two-stage creates pole-zero doublet which may affect the settling time of the op-amp. Perfect matching between first two input stages and two miller capacitors can determine the pole-zero cancellation effect, which is estimated by:

$$\frac{gm_{11}}{Cm_1} = \frac{gm_{12}}{Cm_2} \tag{6.15}$$

where gm_{11} is the three-stage amplifier's first stage transconductance and gm_{12} is the two-stage amplifier's first stage transconductance and Cm_1 and Cm_2 are NMC's miller capacitors. Although MNMC extends the bandwidth of a three-stage amplifier, its GBW is still half of the limiting pole frequency.

6.3.4 Nested Gm-C Compensation

Both NMC and MNMC use miller capacitance pole splitting effect to improve phase margin. However, zeros generated through miller capacitors are not taken into consideration, which reduce NMC and MNMC's performance and make them more complicated to design. Nested Gm-C compensation (NGCC) topology as shown in Figure 78 [29] was proposed to use gm feedforward paths to cancel multiple miller RHP zeros effect. Although NGCC extends the bandwidth further, the bandwidth of the amplifier is still limited by the miller capacitor's effect. In addition, the miller capacitance compensation does not function well for the output stage which has very little gain. Consequently, a compensation technique which does not rely on miller capacitance compensation is needed.

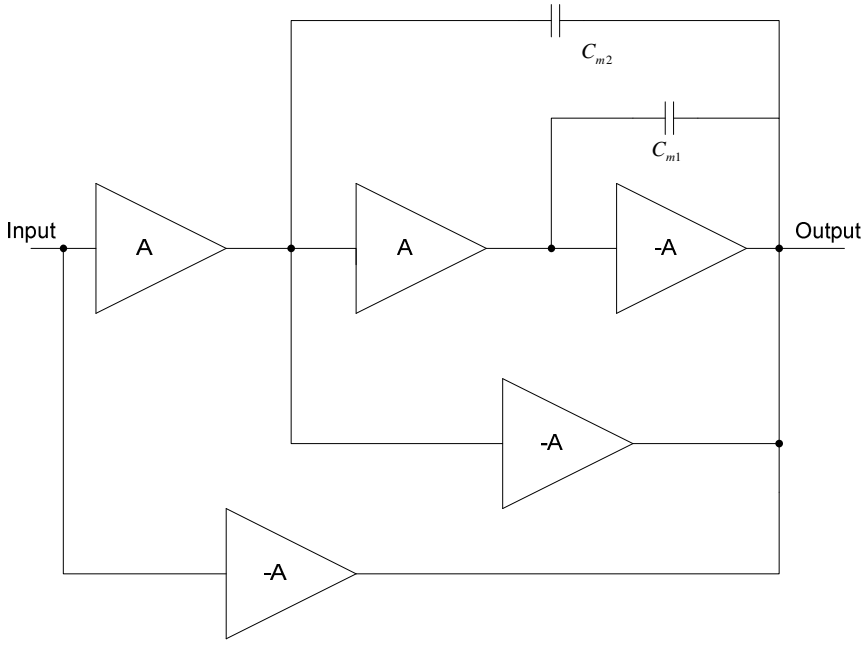

Figure 78 Nested gm-C compensation (NGCC)

6.3.5 No-capacitor Feedforward Compensation

Feedforward compensation technique [30] has been used for high frequency compensation for many years. No-capacitor Feedforward (NCFF) as shown in Figure 79 [31] employs a feedforward path to create LHP zero to cancel the effect of second dominant pole. It does not rely on Miller capacitor's pole splitting effect, which reduces the gain-bandwidth product of an op-amp.

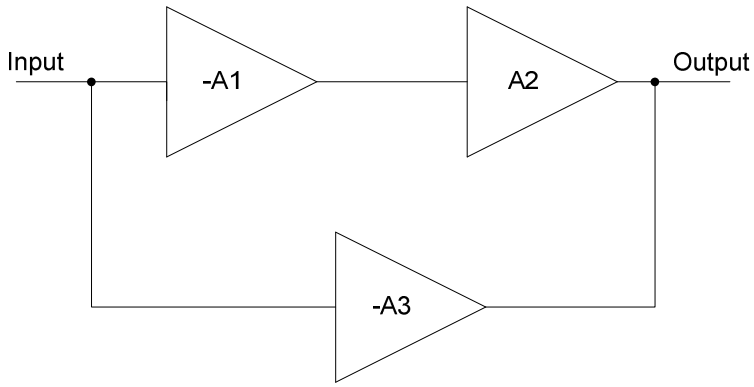

Figure 79 No-capacitor feed forward (NCFF)

A two-stage amplifier carries two dominant poles at frequencies of ω_1 and ω_2. Without any frequency compensation, those two poles are relatively close to each other and generate very little phase margin for an amplifier. Miller capacitor compensation pushes the first stage pole close to origin and pulls the second stage pole away from origin in order to increase the phase margin. For NCFF, instead of pushing the first pole to lower frequency, the feedforward path creates a positive phase shift LHP zero and cancels out the second dominant pole's negative phase shift effect. The pole zero cancellation effect [32] happens at high frequency, higher than GBW, which has minimum impact on the amplifier's settling time. The amplifier transfer function is

$$H(s) = H_{two-stage}(s) + H_{feedforward}(s) \tag{6.16}$$

$$H(s) = \frac{-A1 * A2}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_2}\right)} + \frac{-A3}{\left(1 + \frac{S}{\omega_3}\right)} \tag{6.17}$$

where the feedforward path is added into the uncompensated two-stage amplifier. For the pole-zero cancellation, the pole of the feedforward path is set to be the same location as the second stage amplifier's pole. The transfer function is simplified into

$$H(s) = \frac{-A1 * A2}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_2}\right)} + \frac{-A3}{\left(1 + \frac{S}{\omega_2}\right)} \tag{6.18}$$

$$H(s) = -\frac{A1 * A2 + A3\left(1 + \frac{S}{\omega_1}\right)}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_2}\right)}$$

$$= -\frac{(A1 * A2 + A3)\left(1 + \frac{A3 * S}{(A1 * A2 + A3)\omega_1}\right)}{\left(1 + \frac{S}{\omega_1}\right)\left(1 + \frac{S}{\omega_2}\right)} \tag{6.19}$$

where the DC gain of the two-stage NCFF is $A_1A_2+A_3$ and the feedforward path creates a LHP zero. The LHP zero can be expressed as

$$Z = -\frac{(A1 * A2 + A3)\omega_1}{A3} = -\frac{1}{R_1C_1}\left(1 + gm_1R_1\frac{gm_2R_2}{gm_3R_2}\right)$$

$$\approx -\frac{gm_1}{C_1}\frac{gm_2}{gm_3} \tag{6.20}$$

where gm_1 and gm_2 are the first and second stage transconductances respectively, and gm_3 is the feedforward stage transconductance. It is shown in Figure 80. R_1 and C_1 are the first stage resistive and capacitive output impedances. R_2 is the output resistive load off the circuit. No capacitor feedforward has better high frequency performance and consumes less power than the aforementioned methods.

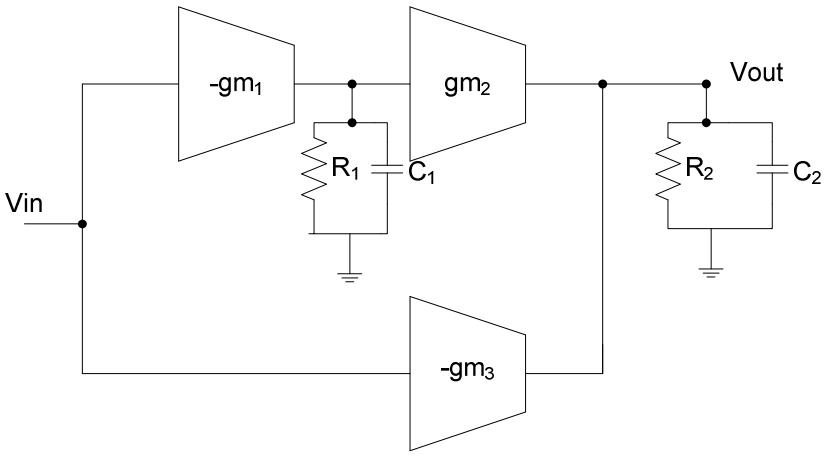

Figure 80 No-capacitor feed forward (NCFF) with poles

6.3.6 Other Multi-stage Compensation Technique

In order to extend bandwidth, many other frequency compensation techniques have been proposed since late 1990's. Reversed nested miller compensation [33][34] implements NMC in reversed fashion to extend the amplifier's bandwidth. Active-feedback frequency-compensation (AFFC) [35][36] separates the low-frequency high-gain path and high-frequency low gain signal path to achieve wide bandwidth. Single Miller capacitor compensation (SMC) and single Miller capacitor feedforward compensation (SMFFC) [37] combine pole-splitting and feedforward techniques to achieve better high frequency performance. Feedforward reversed nested miller compensation technique [38] employs double feedforward paths to reach high frequency bandwidth. Active reversed nested miller compensation .

[39] [40] was introduced to remove RHP zero through the existing active stage. All these frequency compensation method are actually based on NMC, NGCC and feedforward compensation technique.

6.3.7 Summary

Based on the high frequency performance as shown in Table 15 of fundamental compensation techniques and available process technology of the project, NCFF is believed to be the excellent candidate for this project's multi stage class-AB amplifier's frequency compensation. It uses the least amount of power and extends op-amp's bandwidth beyond the traditional miller compensation.

Table 15 Comparison of multi-stage frequency compensation scheme

	GBW	POWER	POLE-ZERO Cancellation
Nested Miller Comp.	Low	High	No
Multipath Nested Miller Comp.	Medium	Medium	Yes
Nested Gm-C Comp	Medium	Medium	No
No Capacitor Feed Forward	High	Medium	Yes(high frequency)

6.4 Frequency Compensation Design

Based on the discussion in the previous section about high frequency and settling time requirements, no-capacitor feedforward is chosen to compensate the class-AB amplifier. For a three-stage amplifier, usually two feedforward paths are used to completely cancel out the second and third poles through introducing two LHP zeros. Figure 81 shows the no-capacitor feed forward three-stage amplifier.

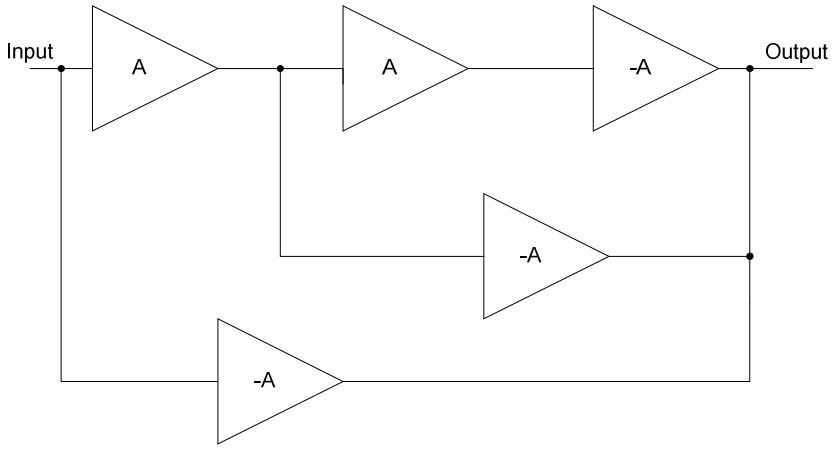

Figure 81 Three-stage amplifier with two no-capacitor feed forward stages

However, to save power, the inner feedforward path is not implemented in this amplifier design. Instead, single feedforward path is adopted in this three–stage amplifier design as shown in Figure 82.

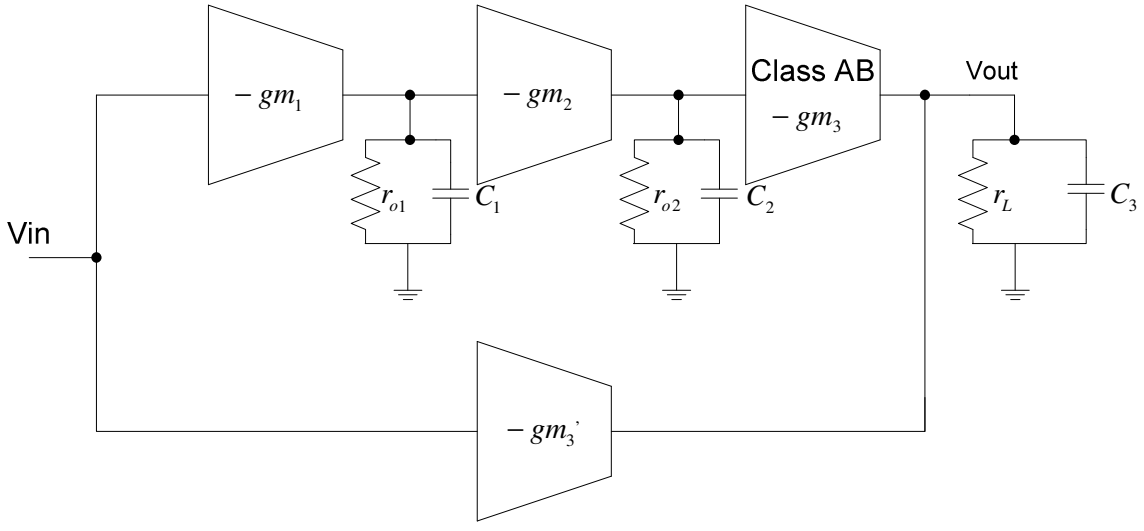

Figure 82 Three-stage amplifier with single no-capacitor feed forward stage

There are three dominant poles for this three-stage amplifier. First pole is associated with the differential input stage. Second pole is associated with the diode connected adaptive load as shown in Figure 69. The third pole is at node of class-AB stage the output. These poles locations are estimated by

$$\omega_1 = \frac{1}{r_{o1}C_1} \tag{6.21}$$

$$\omega_2 = \frac{1}{r_{o2}C_2} = \frac{gm_2}{C_2} \tag{6.22}$$

$$\omega_3 = \frac{1}{r_L C_3} \tag{6.23}$$

where r_{o1} is the output impedance of the input stage differential pair, C_1 is the first stage output parasitic capacitor, r_{o2} is approximately the diode connected adaptive load's transconductance, C_2 is the adaptive load parasitic capacitance, and the third pole is determined by the output resistor load r_L and the output driver's parasitic capacitance C_3. Without any compensation, three-stage amplifier's transfer function is estimated by

$$H(s)_{uncompensated} = \frac{A_1 A_2 A_3}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{6.24}$$

By using no-capacitor feedforward technique, the transfer function is modified into

$$H(s)_{NCFF} = \frac{A_1 A_2 A_3}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} + \frac{A_4}{\left(1+\frac{s}{\omega_3}\right)} \tag{6.25}$$

where A_4 is the gain of the feedforward stage, and the feedforward stage has the same pole location as the class-AB output stage. In fact, the feedforward stage transconductance needs to be as much as the output transistor transconductance at

quiescent condition in order to achieve the design stability. The small signal ac gain of the class-AB output stage is approximately equal to the feedforward stage small signal ac gain. With this approximation, the transfer function is simplified into

$$H(s)_{NCFF} = \frac{A_3\left(A_1A_2 + \left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\right)}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{6.26}$$

$$H(s)_{NCFF} = \frac{\frac{A_3}{\omega_1\omega_2}(A_1A_2\omega_1\omega_2 + \omega_1\omega_2 + (\omega_1+\omega_2)s + s^2)}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{6.27}$$

where the transfer function has three poles and two zeros. The zeros could be estimated through solving the second-order polynomial of the numerator. They are estimated by

$$\begin{aligned} Z_1 &= \frac{-(\omega_1+\omega_2) + \sqrt{(\omega_1+\omega_2)^2 - 4(A_1A_2\omega_1\omega_2 + \omega_1\omega_2)}}{2} \\ &= \frac{-(\omega_1+\omega_2) + \sqrt{(\omega_1-\omega_2)^2 - 4(A_1A_2\omega_1\omega_2)}}{2} \end{aligned} \tag{6.28}$$

$$\begin{aligned} Z_2 &= \frac{-(\omega_1+\omega_2) - \sqrt{(\omega_1+\omega_2)^2 - 4(A_1A_2\omega_1\omega_2 + \omega_1\omega_2)}}{2} \\ &= \frac{-(\omega_1+\omega_2) - \sqrt{(\omega_1-\omega_2)^2 - 4(A_1A_2\omega_1\omega_2)}}{2} \end{aligned} \tag{6.29}$$

The zeros are in LHP, and $\omega_1 \approx \omega_2$ is assumed. The zeros are complex conjugates and estimated by

$$\omega_1 \approx \omega_2 \quad \rightarrow \quad (\omega_1-\omega_2)^2 - 4(A_1A_2\omega_1\omega_2) \approx -4(A_1A_2\omega_1\omega_2) < 0 \tag{6.30}$$

$$Z_1 = \frac{-(\omega_1+\omega_2) + j\sqrt{4(A_1A_2\omega_1\omega_2)}}{2} \tag{6.31}$$

$$Z_2 = \frac{-(\omega_1+\omega_2) - j\sqrt{4(A_1A_2\omega_1\omega_2)}}{2} \tag{6.32}$$

Matlab is used to analyze the third-order transfer function frequency response. Pole locations are estimated based on the circuit design and simulation results. They are estimated at

$$\omega_1 = 2\pi * 70MHz \tag{6.33}$$

$$\omega_2 = 2\pi * 120MHz \tag{6.34}$$

$$\omega_3 = 2\pi * 1000MHz \tag{6.35}$$

Each stage gain is estimated to be

$$A_1 = 30dB, A_2 = 10dB, A_3 = 7dB \tag{0.1}$$

The transfer function of this amplifier is approximated by

$$H(s)_{NCFF} = \frac{A_3\left(A_1A_2 + \left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\right)}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)\left(1+\frac{s}{\omega_3}\right)} \tag{6.36}$$

$$= \frac{[(1.153e-017)\,s^2 + (8.028e-009)s + 213.6]}{[(4.799e-028)s^3 + (3.588e-018)\,s^2 + (3.759e-009)\,s + 1]}$$

Figure 83 shows the proposed feedforward compensation frequency response using Matlab. With two LHP zeros, phase margin of this three-stage amplifier is compensated. At lower frequencies, the phase decreases due to two lower frequency poles at ω_1 and ω_2. At the higher frequencies, the pole-zero cancellation effect happens, where the phase margin is compensated. The feedforward stage creates two complex LHP zeros, which extends the amplifier's phase margin considerably.

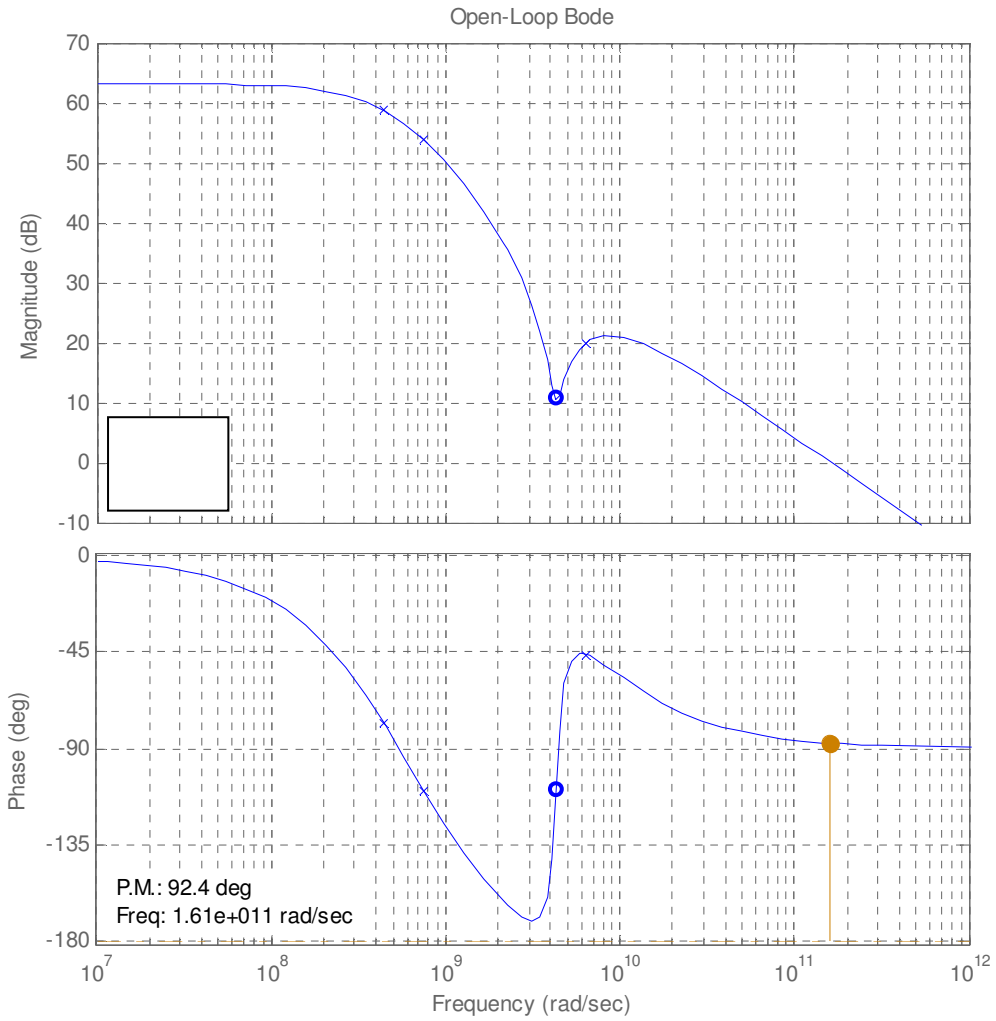

Figure 83 Frequency response and phase response of proposed feedforward compensation

The performance of the amplifier is also discussed in the unity-feedback closed-loop configuration as shown in Figure 84. The characteristic equation can be expressed as

$$1 + A_3 H(S) = 0 \tag{0.2}$$

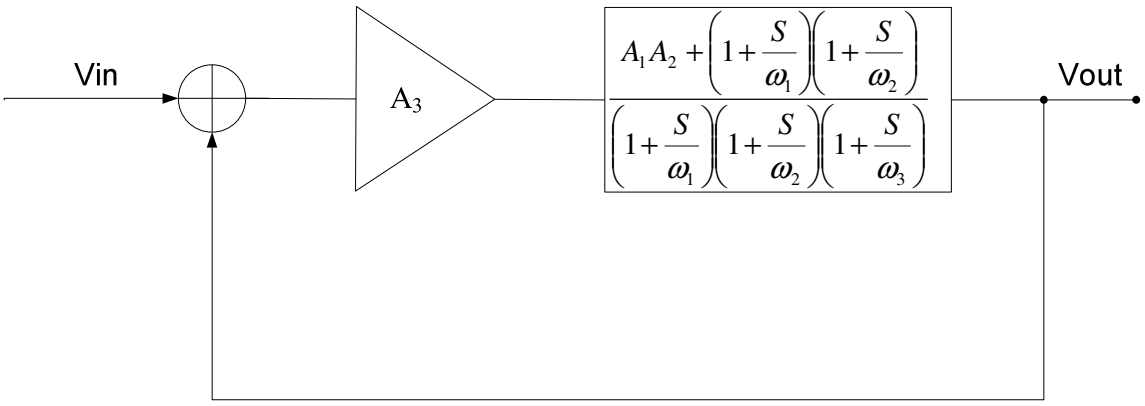

Figure 84 Three-stage amplifier with single feedforward compensation path in unity gain feedback loop

where A_3 is the feedforward stage as well as output stage small signal gain. Using Matlab root locus function, the roots and zeros are shown in Figure 85 with A_3 varying from 0 to infinity. As the gain of feedforward stage increases, the poles of the closed-loop transfer function enter into the RHP briefly. Once the feedforward gain is sufficiently large, the poles of the closed loop function come back to LHP. When A_3 is greater than 6dB, the poles enters the LHP. To ensure stability of the unity-feedback closed-loop function, it has been shown that the feedforward stage gain A_3 should be greater than 6dB. In general, the simulation shows that the closed-loop system is stable with moderate feedforward gain.

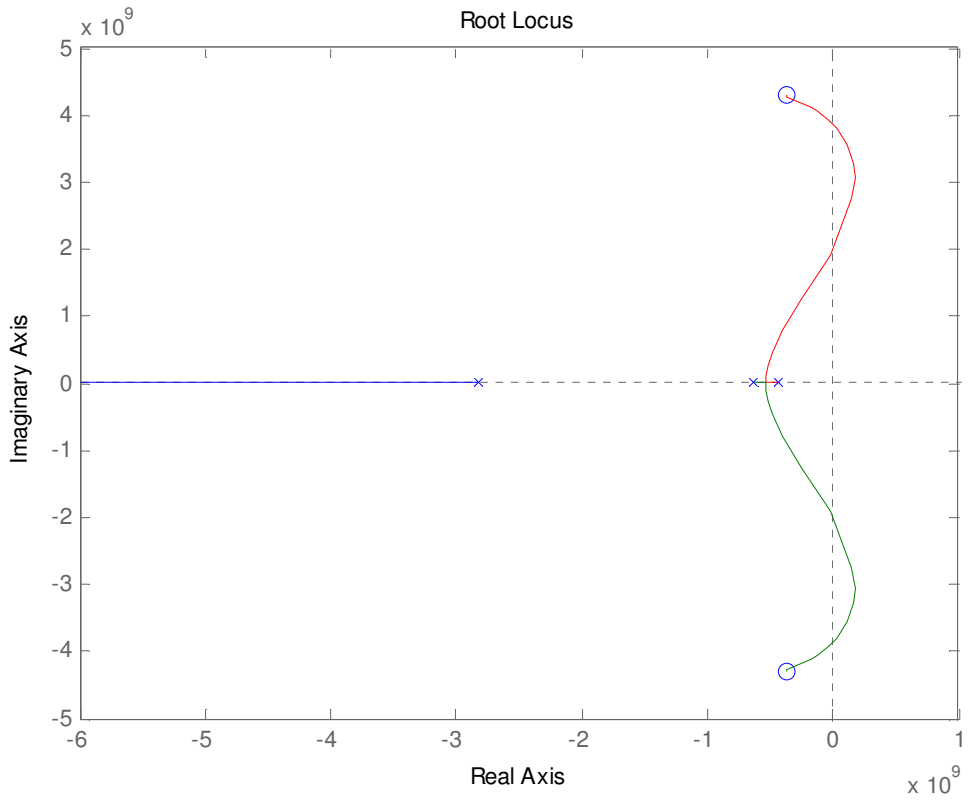

Figure 85 Matlab root locus simulation of three-stage amplifier single feedforward compensation path in unity gain feedback loop

6.5 Frequency Compensation Circuit Implementation

The single path feedforward stage is implemented using two simple feedforward transistors M_{PF} and M_{NF} as shown in Figure 86. In order to better control the transconductances of these feedforward transistors, their gate voltages are controlled individually through two reference voltages V_{bias1} and V_{bias2} generated from current biasing circuit. Two coupling capacitors of 7pF are used for ac signal coupling.

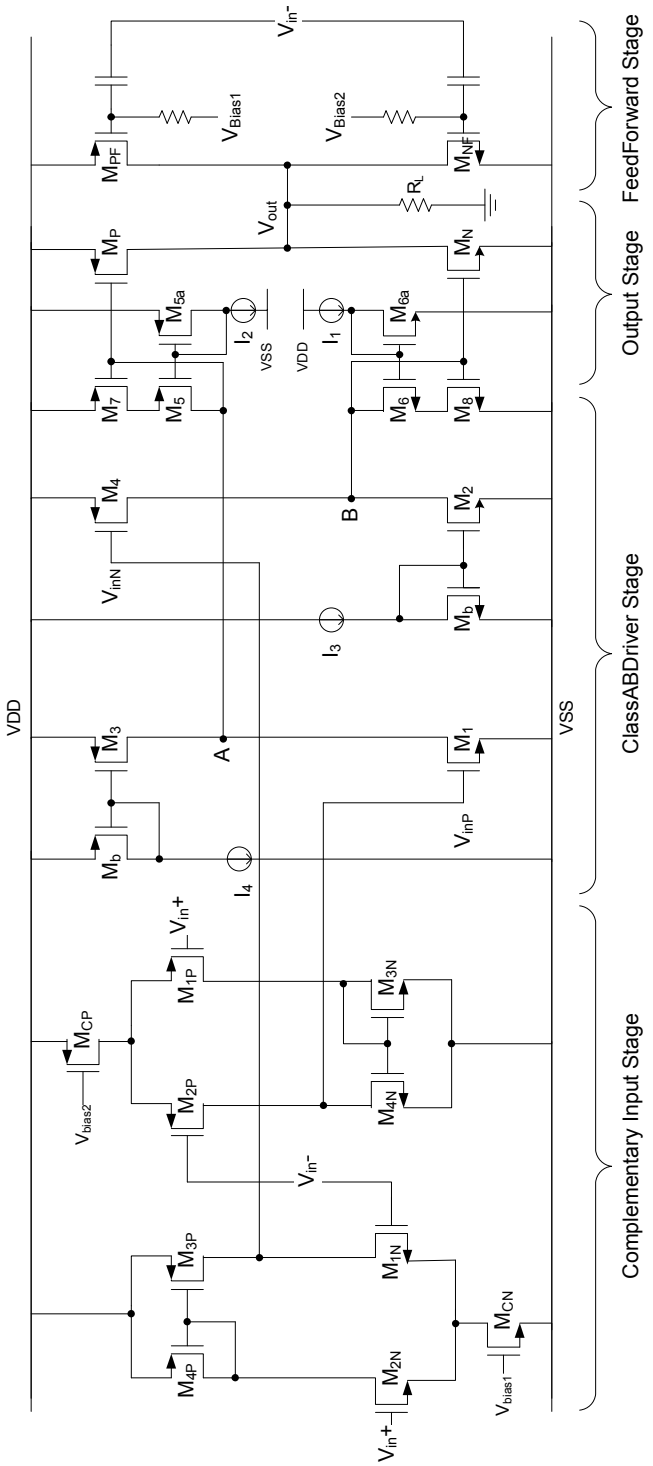

Figure 86 Schematic of propose fully balanced class-AB amplifier with single feedforward compensation path

6.6 Post Layout Simulation Performance

The Class-AB Op-Amp's layout is simulated using Cadence Spectre. This amplifier is operating in closed-loop configuration with loop gain of 6v/v. The loop gain and loop phase margin is simulated using the circuit shown in Figure 87.

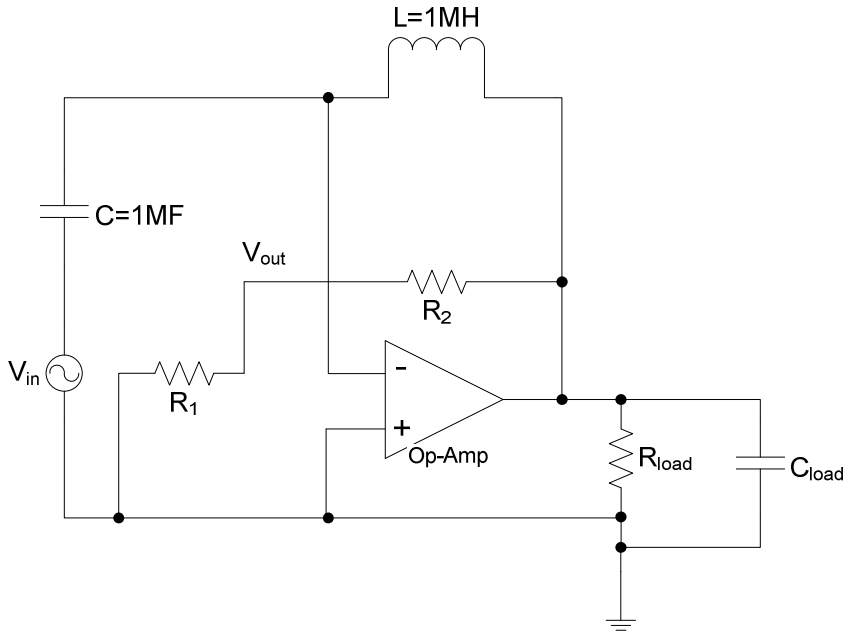

Figure 87 Schematic of fully balanced class-AB amplifier for AC response simulation

The post layout simulation in Figure 88 shows that the loop gain is 33dB at DC and 30-23dB at 70-110MHz. The loop phase margin is about 45º. The phase shape is similar to Matlab simulation result. The phase decreases as a two pole system until it hits the high frequency pole zero cancellation frequency. Due to two complex LHP zeros created by the feedforward stage, the phase margin is compensated to 45º.

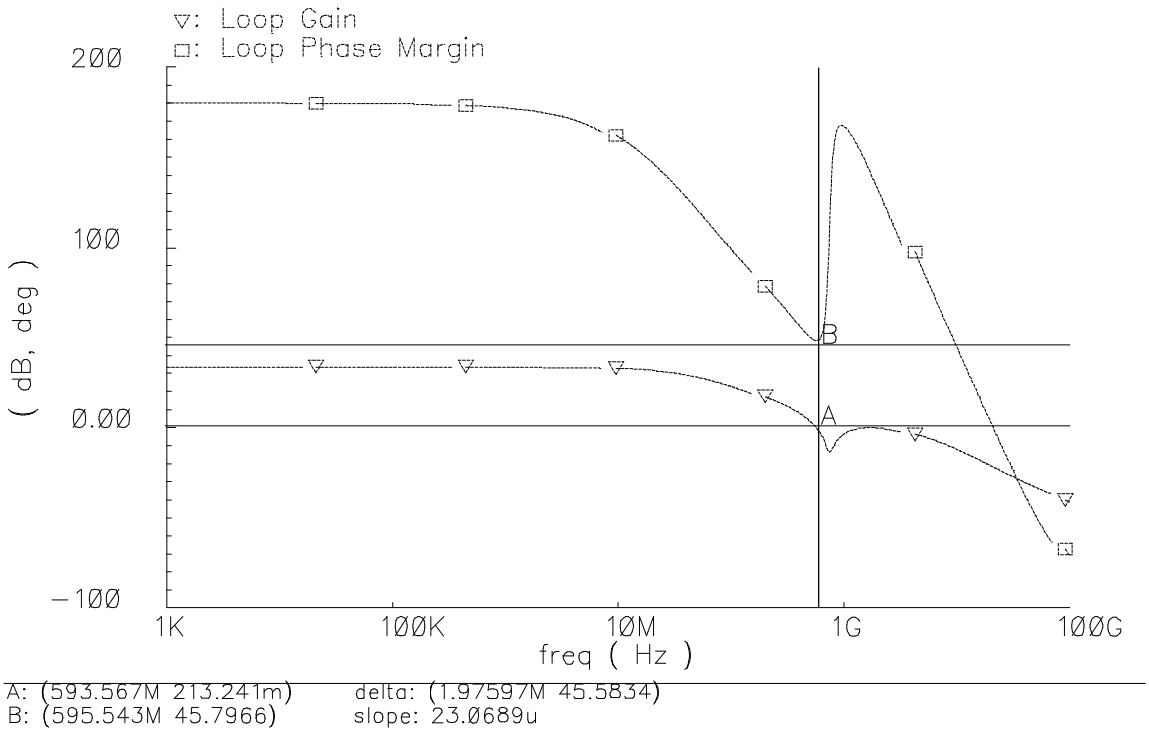

Figure 88 Post layout AC simulation of fully balanced class-AB amplifier with 593MHz gain bandwidth product and 45^{o} phase margin

Transient simulation is performed on the class-AB amplifier's layout with 50Ω load in parallel with 1pF parasitic capacitor. Figure 89 shows output signal transient simulation. With output peak-peak amplitude of 0.63V at 110MHz, the output signal has 0.7% total harmonic distortion.

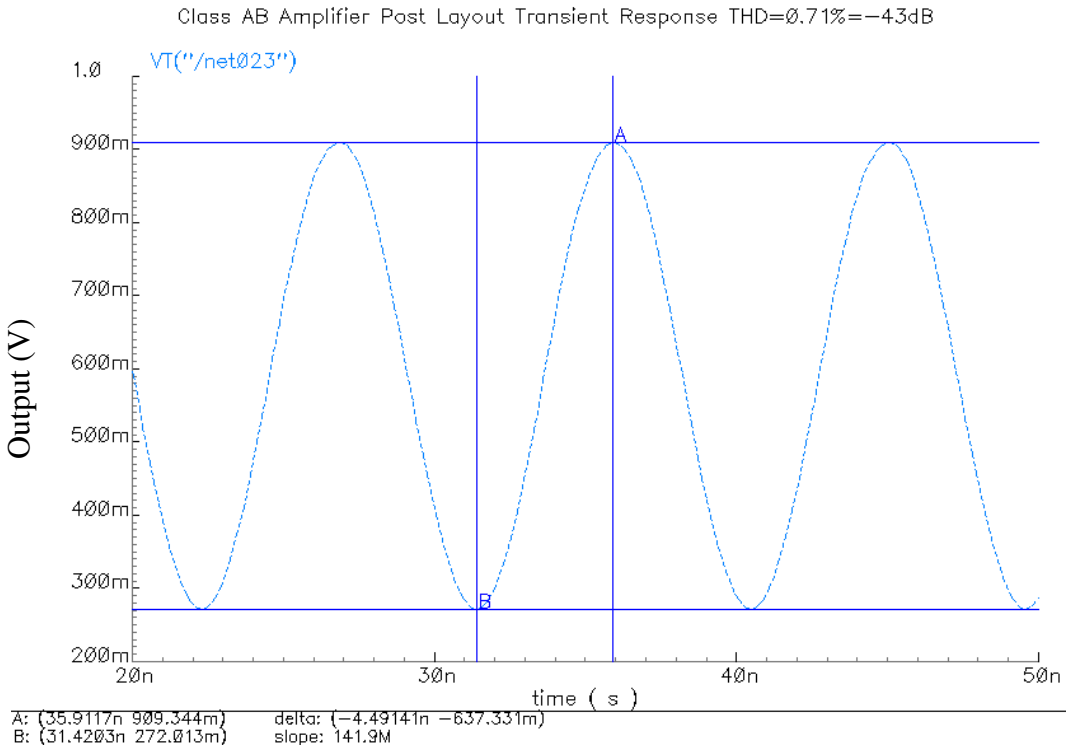

Figure 89 Post layout transient simulation of fully balanced class-AB amplifier output signal with $0.63V_{pp}$

Discrete Fourier transform is used to calculate the output signal's high frequency harmonics. With peak-to-peak amplitude of 0.63V and 110MHz signal frequency, the harmonics above 990MHz frequency are less than -94dB as shown in Figure 90. Although not reaching the 110dB specifications, it is an accepted result.

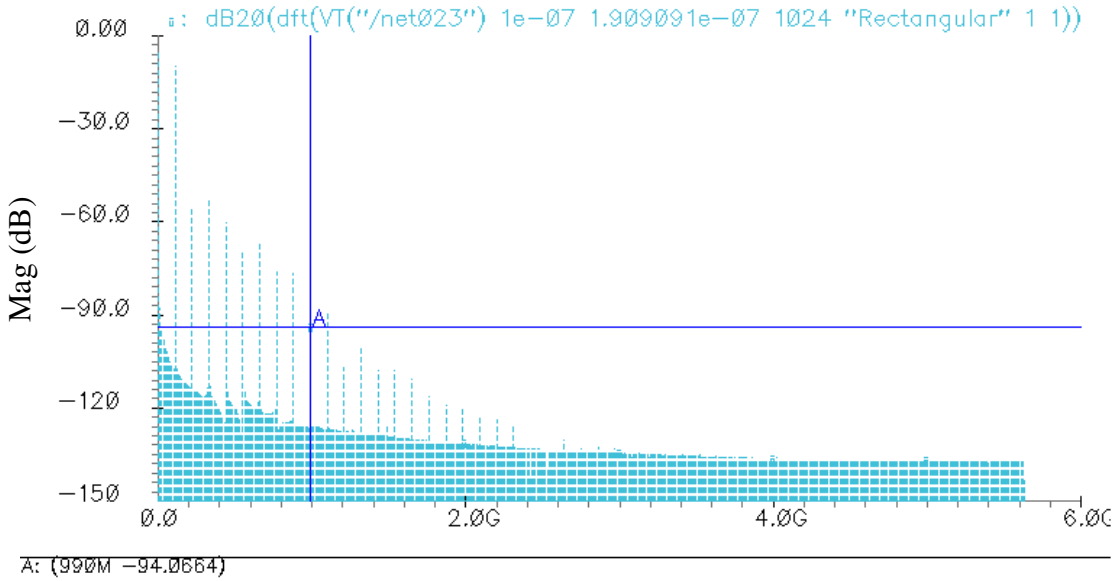

Figure 90 Frequency spectrum of fully balanced class-AB amplifier's output signal with 0.63Vpp at 110MHz

Two-tone test is conducted on the class-AB amplifier, where 100MHz and 110MHz sine waves are injected into the amplifier. The measured IM3 is 46dB as shown in Figure 91.

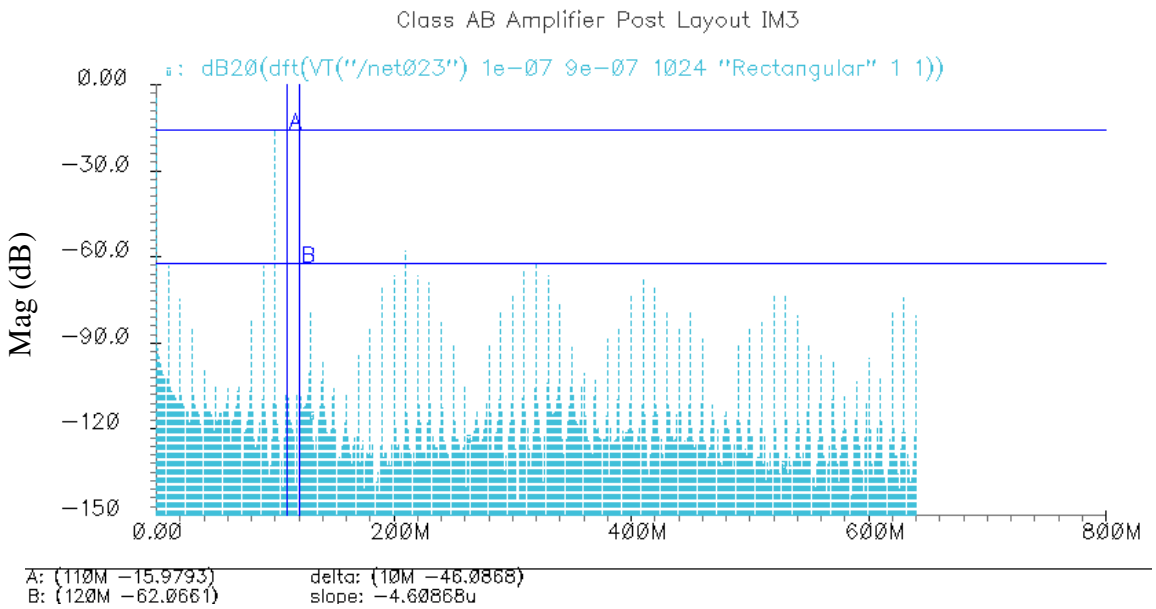

Figure 91 Frequency spectrum of fully balanced class-AB amplifier's output signal with two-tone test with IM3 of -46dB

Input common mode voltage range and the output-voltage swing of the class-AB amplifier are measured in post layout simulation. The input common mode range is 0.8V as shown in Figure 92. Figure 93 shows the output voltage swing of 0.9V.

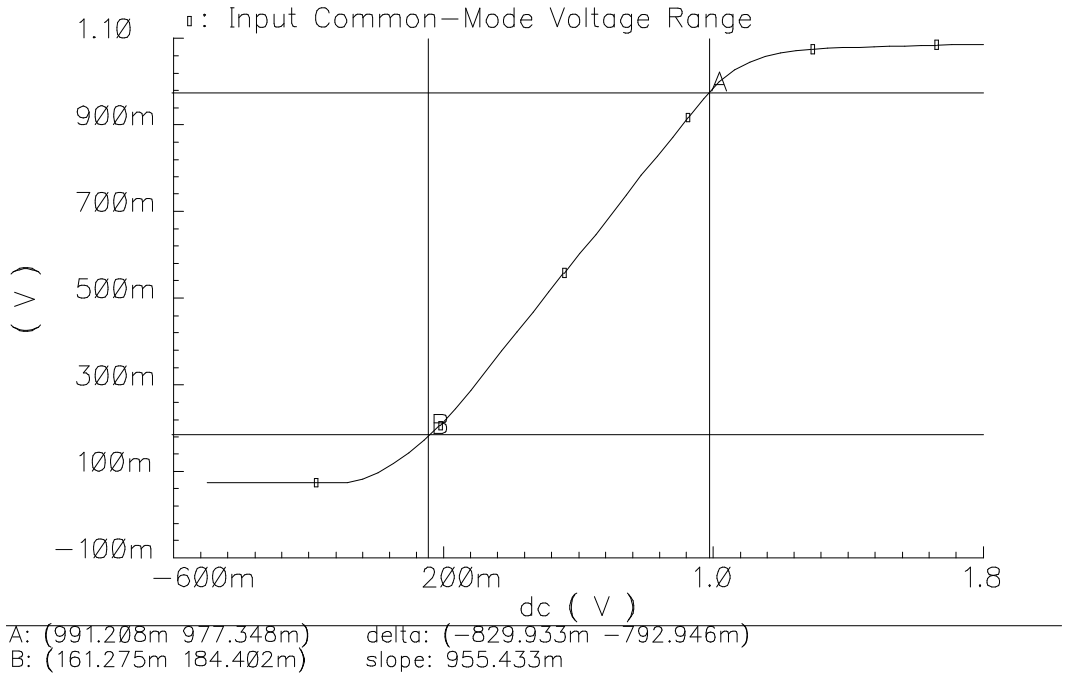

Figure 92 The proposed class-AB input common-mode voltage range

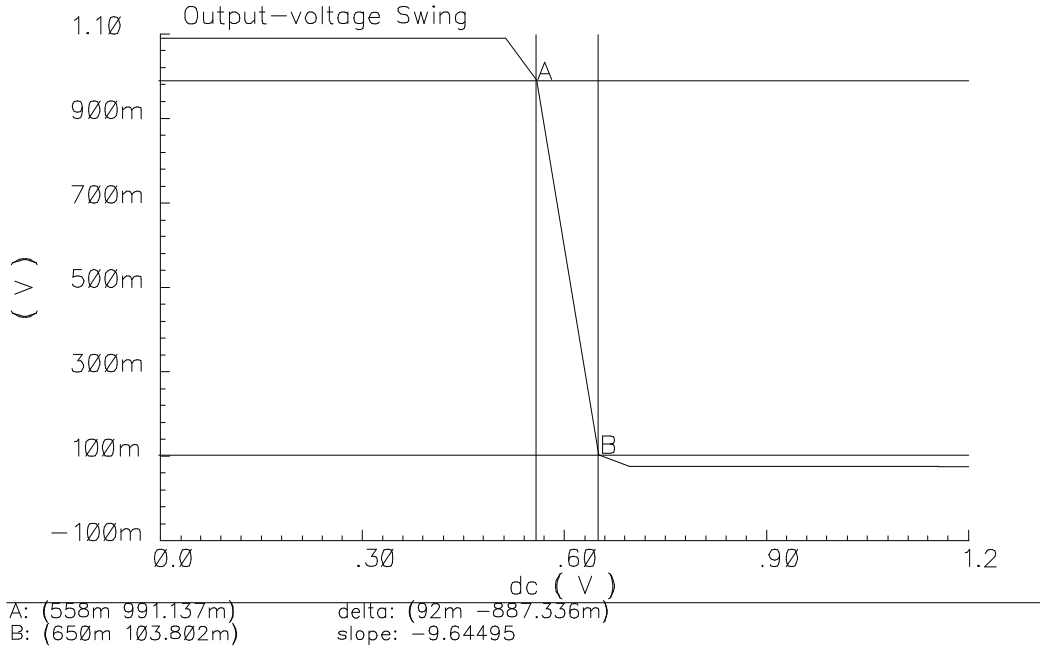

Figure 93 The proposed class-AB Output voltage swing

The slew rate of this class-AB op-amp is measured during the post layout simulation. In order to drive a 50Ω load at 1mW with 110MHz frequency, the minimum slew rate is estimated by

$$Slew\ Rate = 4 * 110MHz * \sqrt{2 * 1mW * 50\Omega} = 139V/us \tag{6.37}$$

The measured minimum slew rate is 420V/us with 50Ω load and 0.5pF load capacitance, which is 3 times higher than the minimum slew rate requirement. Figure 94 shows the positive slew rate result, and Figure 95 shows the negative slew rate result.

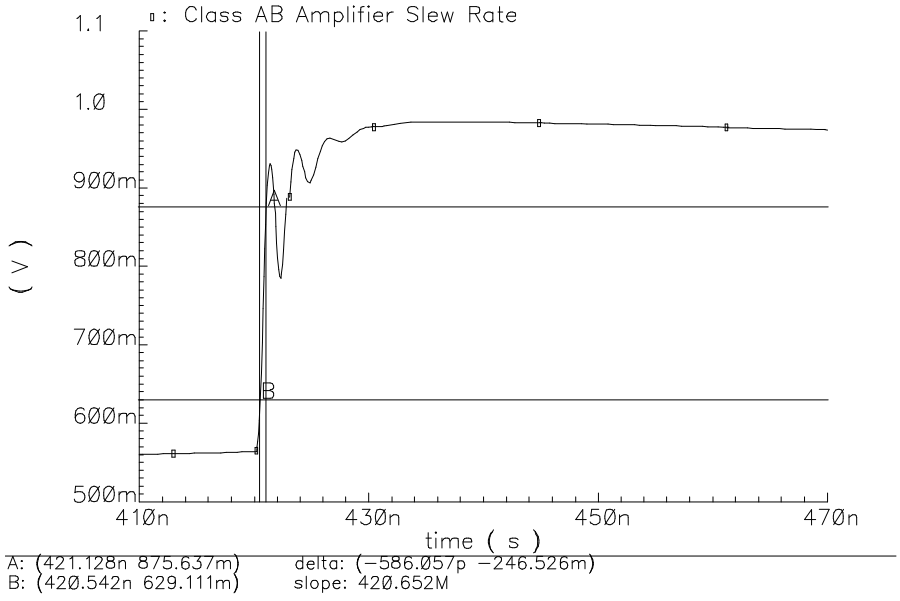

Figure 94 Post layout simulation of fully balanced class-AB amplifier's positive slew rate of 420V/us

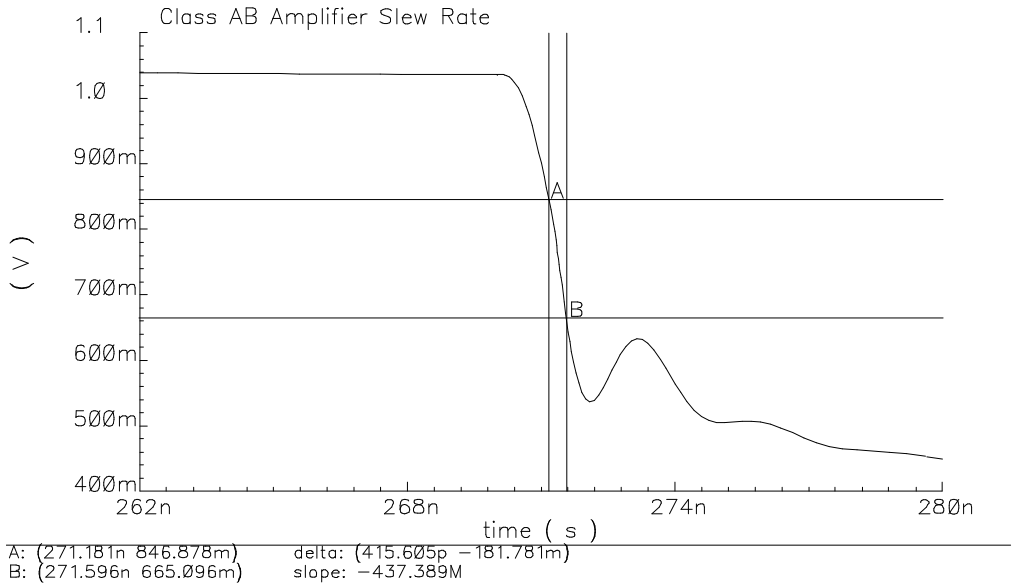

Figure 95 Post layout simulation of fully balanced class-AB amplifier's negative slew rate of 437V/us

6.7 Output Buffer Stage Efficiency

The most important feature of a class-AB buffer is its efficiency. The power consumption of the designed buffer is 6.75mW and the output power is 1mW. Based on this simulation result, the efficiency of the buffer seems to be very low. The conventional class-AB 78.6% efficiency calculation is based on rail-to-rail output signal amplitude and does not take the input stage and frequency compensation stage power consumption into account. Based on the conventional efficiency definition and specified output signal amplitude, maximum efficiency of the designed class-AB output stage is calculated as

$$\eta_{classA} = \frac{P_{load}}{P_{supply}} = \frac{\pi * V_{out}}{2 * Vdd} = \frac{\pi * 0.316}{2 * 1.2} = 41.36\% \quad (6.38)$$

where Vout is the output signal zero-to-peak swing, and Vdd is the supply voltage. Due to the output signal's maximum allowed amplitude, this maximum achievable efficiency is a lot lower than the ideal class-AB output efficiency.

If a class A buffer stage were used in this work, it would consume more power and have lower efficiency. In order to deliver 1mW power on a 50Ω load, the output stage has to maintain at least 6.32mA DC current, which is 7.58mW at 1.2V supply. The ideal class A output stage's maximum efficiency is 25%. Since the actual class A efficiency depends on the value of R_{load} and the swing of output, in our case, the maximum achievable efficiency of the class A output stage is calculated as

$$\eta_{classA} = \frac{P_{load}}{P_{supply}} = \frac{1mW}{\left(\sqrt{1mW/50\Omega}\right) * \sqrt{2} * 1.2V} = 13.18\% \quad (6.39)$$

where the P_{supply} is the minimum power supply of the output stage. In addition to the power consumed in the output stage, the class A buffer also needs to consume power in its input stage and frequency compensation stage, which could easily exceed 2~3mW. In practice, a well designed class A output buffer would consume more than 10mW DC power, which is 4mW more than the class-AB buffer designed.

Based on the simulation, the actual designed output stage efficiency is calculated by

$$\eta_{classA} = \frac{P_{load}}{P_{supply}} = \frac{P_{load}}{P_{supplyAC} + P_{supplyDC}} = \frac{1mW}{2.41mW + 2.4mW} = 20.8\% \quad (6.40)$$

where $P_{supplyAC}$ is defined to be the supply power in order to drive the resistive load and $P_{supplyDC}$ is defined to be the power due to quiescent current in the output stage. In this case, the quiescent power takes considerable portion of total supply power due to the need of keeping output stage's pole at high frequency domain.

Table 16 shows the efficiency comparison between class A and class-AB. Based on the theoretical calculation and simulation result, it has been shown that class-AB amplifier fits the efficiency requirement of the project and outperforms class A amplifier.

Table 16 Efficiency comparison of class-A amplifier and class-AB amplifier

Parameter	Class-A	Class-AB
Ideal Efficiency	25.0%	78.6%
Max. Achievable Efficiency	13.2%	41.4%
Actual Simulated Efficiency	<13.2%	20.8%
Amplifier DC Power	>10mW	6.75mW

6.8 Output Buffer Stage Performance Summary

A transimpedance output buffer stage is successfully designed. The degenerated transconductance cell minimized the output signal distortion during the voltage to current conversion. The fully balanced class-AB output stage with feedforward path

achieves the 50Ω load current driving capability at 110MHz. Table 17 shows the summary of post layout simulation performance of the fully balance class-AB amplifier.

Table 17 Post layout simulation summary of fully balanced class-AB amplifier

Parameter	Post layout Simulation
GBW	597MHz
DC Gain	45dB
Phase Margin	45.8º
IM3 110MHz&120MHz	-46dBc
THD@110MHz 0.63Vpp	-43dB
IIP3	23dBm
Input Common Mode Range	0.8V
Output Swing Range	0.9V
Slew Rate	420V/us
Output Stage Efficiency	20.8%
Power	6.75mW
Supply	1.2V
Area	$0.0288mm^2$
Technology	TSMC 0.18um

6.9 Class-AB Amplifier Layout

This class-AB amplifier is designed and laid out in TSMC 0.18um technology as shown in Figure 96. In order to minimize the mismatch, common centroid topology is used during the layout, and minimum transistor length is avoided. The total area of the amplifier is $0.0288mm^2$.

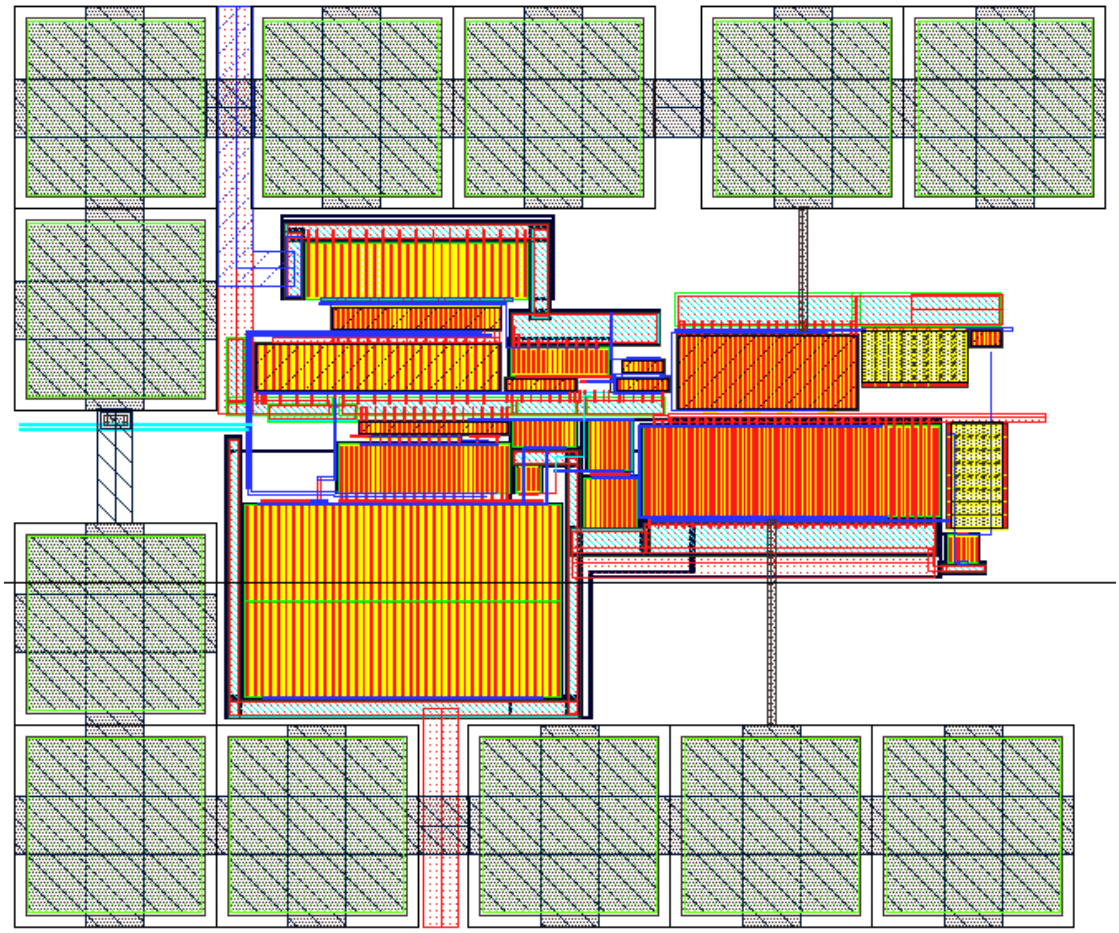

Figure 96 Layout of propose fully balanced class-AB amplifier with single feedforward compensation path with area of 0.0288mm^2

CHAPTER VII

POST LAYOUT SIMULATION RESULTS

The complete harmonic rejection filter is designed, laid out and simulated in TSMC 0.18um technology. The total chip area is 0.819mm^2. This chapter describes the filter test setup, the post layout simulation results, and the circuit layout.

7.1 Test Setup

The complete layout of harmonic rejection filter is simulated. In order to mimic the testing lab environment, 1.76GHz sine wave is used instead of square wave. An on-chip three-stage buffer using inverters is designed to convert the sine wave into a square wave. Figure 97 shows the testing circuit setup. In the test bench, a reset signal source is used for global digital circuit reset. A low speed automatic tuning clock is used to provide clock to tuning circuitry. Although the tuning circuitry clock could be provided through the internal frequency divider circuit, a separate clock signal is used for testing purpose. Digital and analog power supplies are isolated in order to minimize noise coupling between them. An off-chip resistor is used to control bias current. All the DC bias voltages are realized through current bias circuit. A 50Ω resistive load and 1 pF capacitive load are used as the filter output loads. The 1pF capacitor is used to simulate the pad's parasitic capacitance. 4-bit tuning pins are created during the layout, but they are not connected during the simulation. They could be used to override the automatic tuning signal in order to reduce simulation time. During the actual chip testing, 4-bit tuning pins are left unconnected. In the event of tuning failure, these pins could be used for the lab testing and debugging. All the pin assignments are shown in Figure 106.

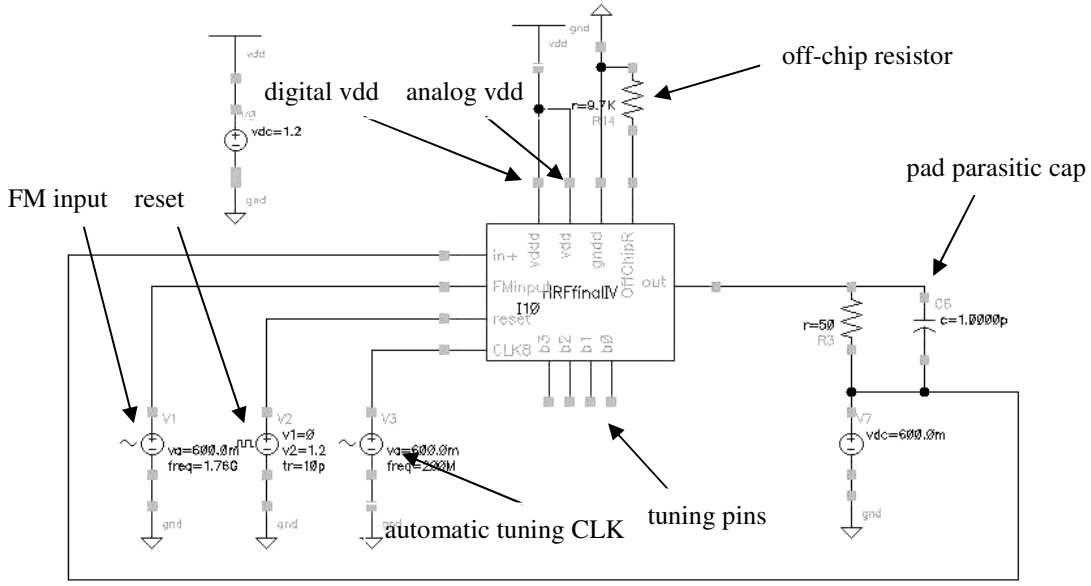

Figure 97 Schematic of testing circuit setup

7.2 Simulation Results

The harmonic rejection filter is simulated using transient simulation. With an input of 1.76GHz square FM signal, the 110MHz output signal has 0.815% or -42dB THD as shown in Figure 98.

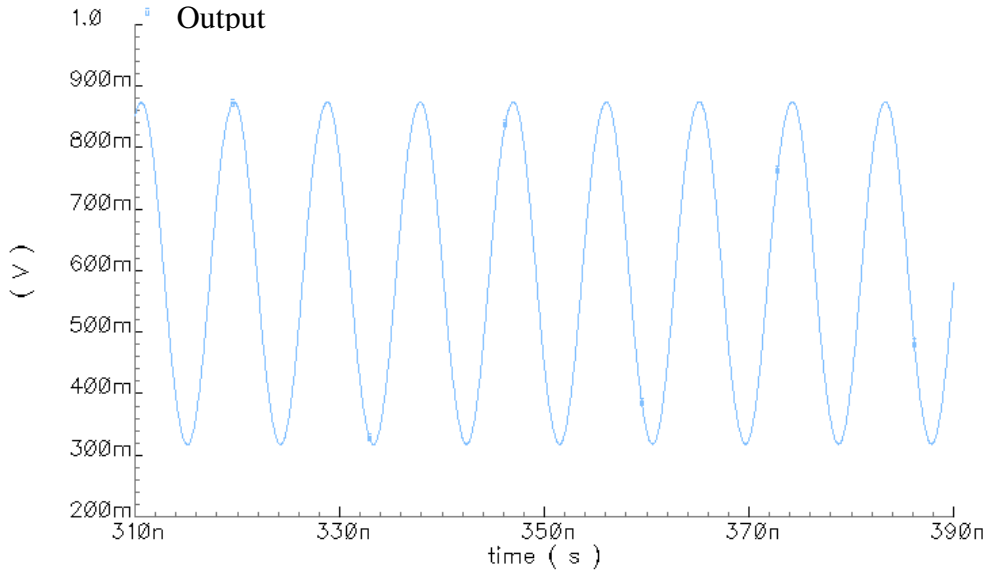

Figure 98 Post layout simulation of harmonic rejection filter with 110MHz output

The output signal frequency spectrum is obtained through Cadence Calculator FFT function. The Cadence FFT setup is based on the tutorial in [41] in order to minimize calculation error. The post layout simulation shows that the high frequency harmonics are below -90dB with 110MHz FM carrier frequency as shown in Figure 99. With the FM frequency of 80MHz, the high frequency harmonics are below -100dB as shown in Figure 100.

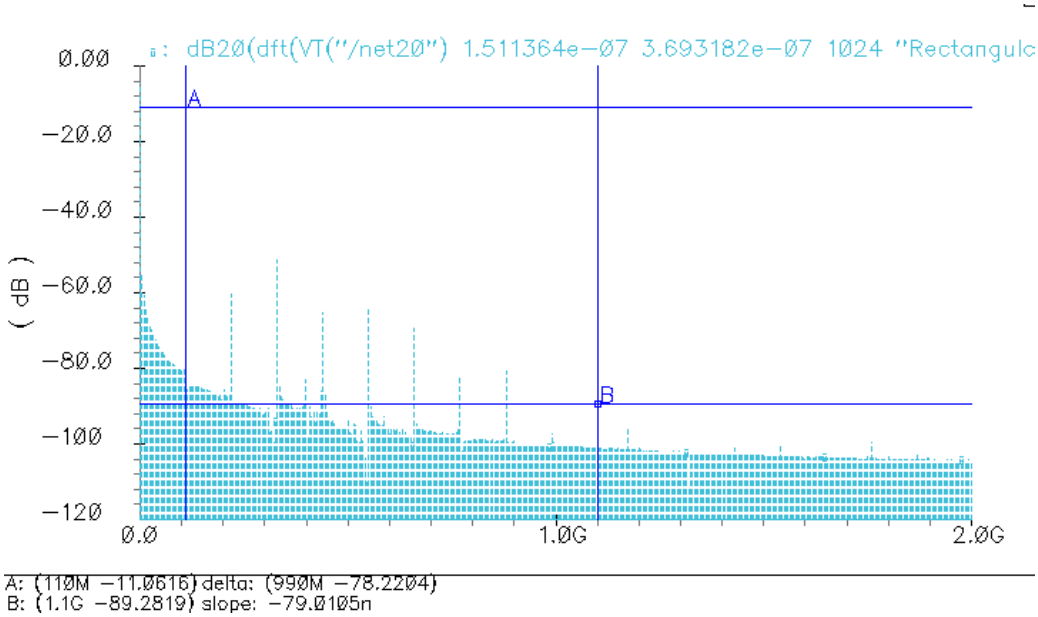

Figure 99 Post layout DFT simulation of harmonic rejection filter with 110MHz output

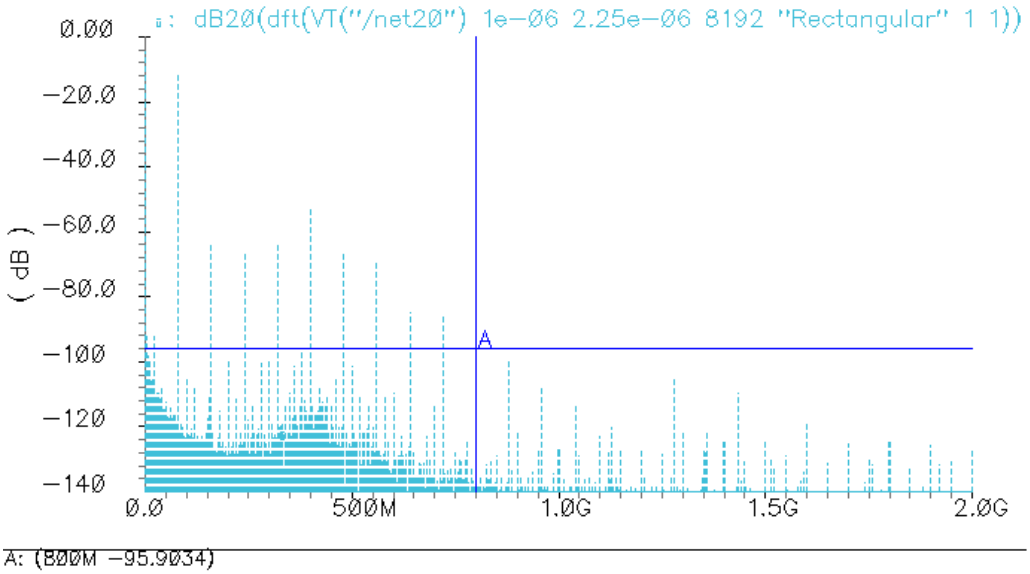

Figure 100 Post layout DFT simulation of harmonic rejection filter with 80MHz output

Post layout simulation is performed on the harmonic rejection filter. With 1.28GHz FM input signal, the automatic tuning circuit could finish the tuning within 4 tuning clock cycle as shown in Figure 101. With 1.76GHz FM input signal, the automatic tuning could be finished in 10 tuning clock cycles as shown in Figure 102 and Figure 103. In addition, the tuning clock speed is externally controlled for testing purposes.

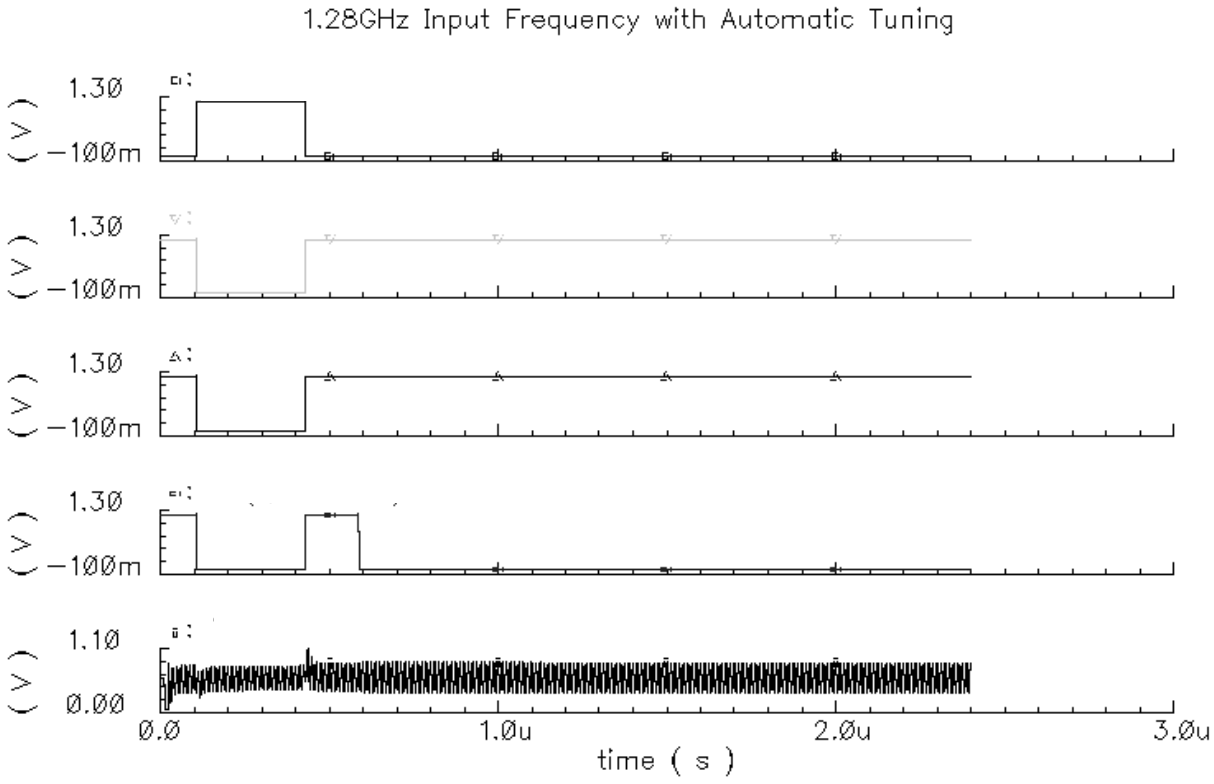

Figure 101 Post layout simulation of automatic tuning with 1.28GHz input

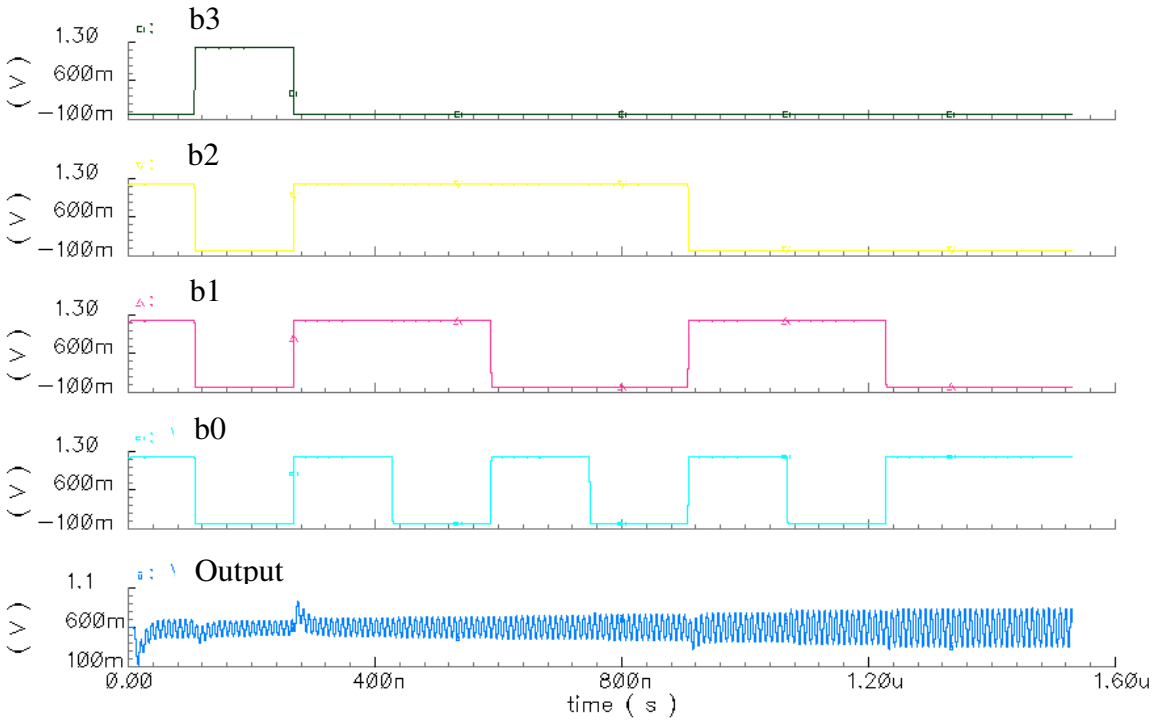

Figure 102 Post layout simulation of automatic tuning with 1.76GHz input

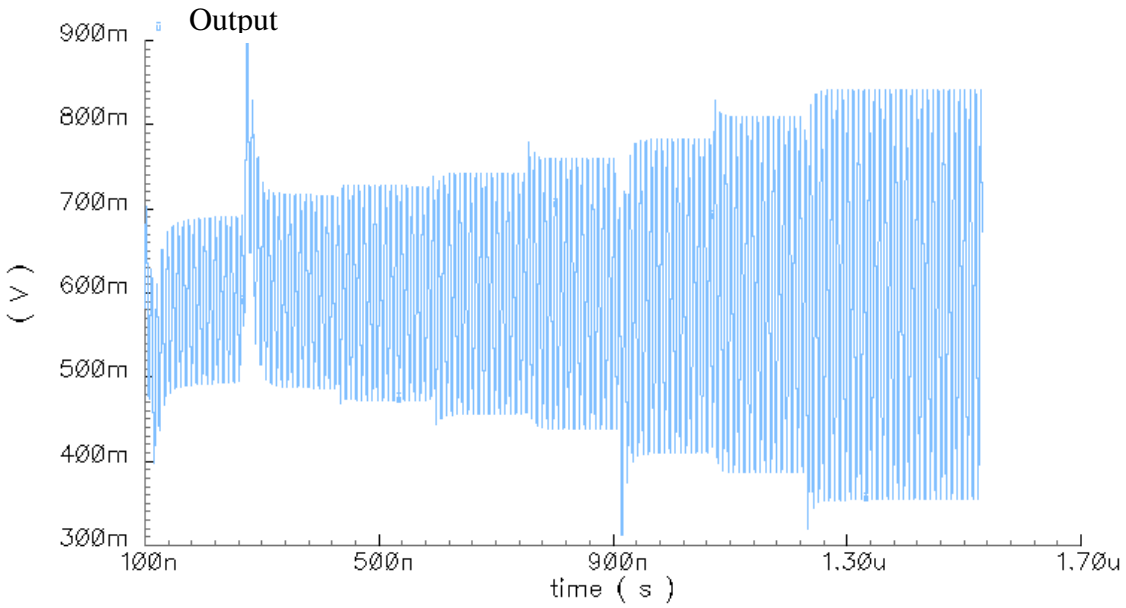

Figure 103 Post layout simulation of automatic tuning 110MHz output

Monte Carlo statistical simulation was performed on the harmonic rejection filter's current summation circuit. Mismatch effect and process variation are added onto the seven current sources. Final output signal's THD histogram is plotted as shown in Figure 104. 100 test runs were performed on the circuit. The output THD mean value is 0.875% (-42dB) with STD of 0.032%.

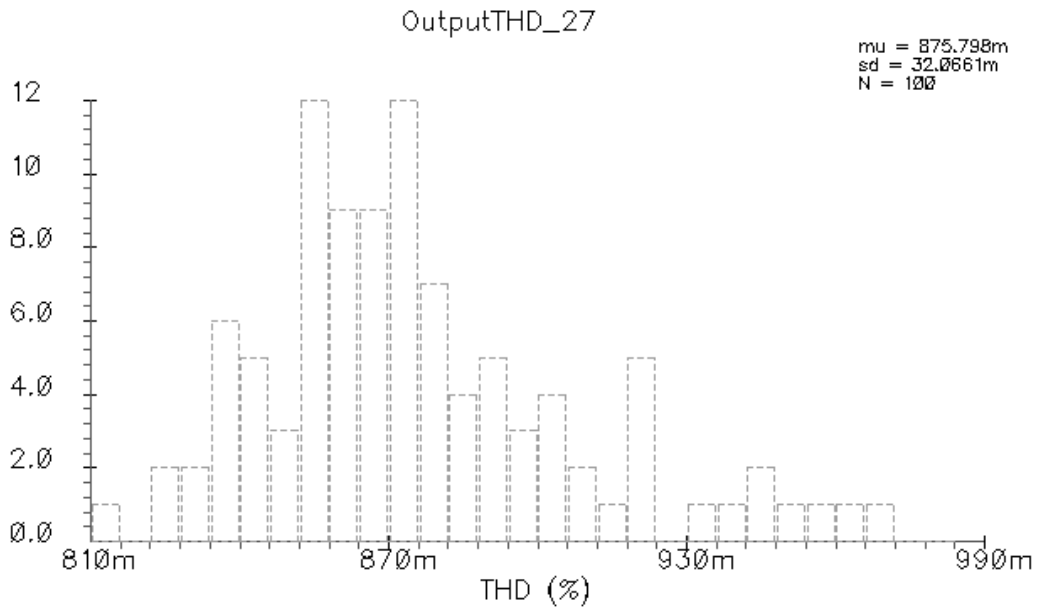

Figure 104 Histogram of output THD Monte Carlo simulation

Figure 105 shows the post layout simulation of the filter's FM signal demodulation. The demodulated signal's THD is -43dB. The glitch is caused by the PLL demodulator, which is not part of this research.

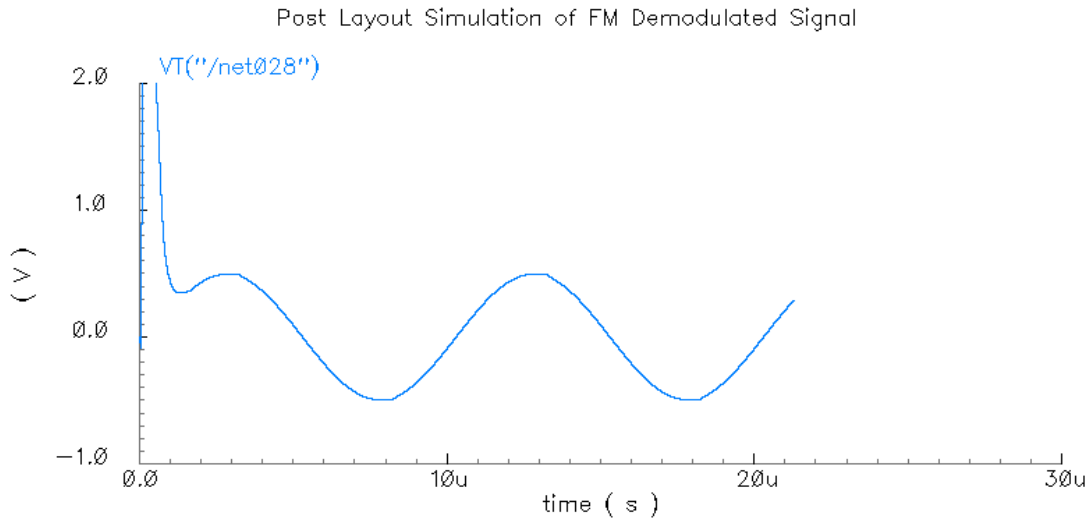

Figure 105 Post layout simulation of demodulated FM signal with -42dB THD

Harmonic rejection FM filter simulation results are summarized in Table 18. Table 19 shows a comparison to other recently published low pass filters. It shows that harmonic rejection filter has higher power efficiency per pole than these previous works.

Table 18 Performance summary of FM harmonic rejection filter

Performance Parameter	Value
Supply Voltage	1.2V
Frequency Range	70MHz-110MHz
SNR	70dB
Attenuation above 800MHz	95dB
Current Consumption (Filter+Buffer)	7.95mW
THD(Carrier)	-43dB
THD(Signal)	-42dB
Settling	<1mS
Total Area	0.946mm^2
Technology	TSMC 0.18um

Table 19 Comparison to recently published works

Reference	[42]	[43]	[44]	[45]	This work
CMOS technology	0.18um	0.12um	65nm	0.13um	0.18um
Supply voltage	1.8V	1V	1.2V	0.55V	1.2V
Topology	source follower	active-RC	gm-C	source follower	harmonic rejection
Order	4	5	5	4	6
3dB frequency	10MHz	5MHz	275MHz	11.3MHz	>110MHz
Power consumption (no buffer)	4.1mW	6.1mW	36mW	3.5mW	0.775mW
Active chip area	0.52mm^2	0.25 mm^2	0.21 mm^2	0.43 mm^2	0.64 mm^2

7.3 Harmonic Rejection Filter Layout

The harmonic rejection filter is laid out in TSMC 0.18um technology. The total chip area is 0.946mm^2. In the harmonic rejection filter design, the layout plays a very important role. First, the layout affects the matching for the harmonic rejection technique, which could alter the circuit performance. Interdigitization and common centroid techniques are used throughout the layout in order to minimize mismatch. Second, digital circuit block could interfere the analog circuit block.

Frequency divider receives the input signal and divides it by 16. As a high frequency digital circuit, it is isolated by guard rings from other analog circuitry in order to reduce its interference on the die. Its layout is also symmetrically designed in order to reduce any phase-shifted output signals mismatch. Also, every D flip-flop is loaded with approximately equal length of metal lines in order to reduce parasitic loading mismatch. For the current summation circuit, interdigitization is used for current source layout in

order to reduce mismatch on the weighting factor. To minimize noise, the block is isolated by guard rings and uses analog power supplies which are isolated from the frequency divider power supplies. Class-AB amplifier is operating at 100MHz range. Any additional layout parasitic degrades its post layout performance from schematic simulation results. During its layout, drain source sharing technique is used extensively in order to minimize any extra amount of parasitic capacitance. Wider metal width is used to reduce current density.

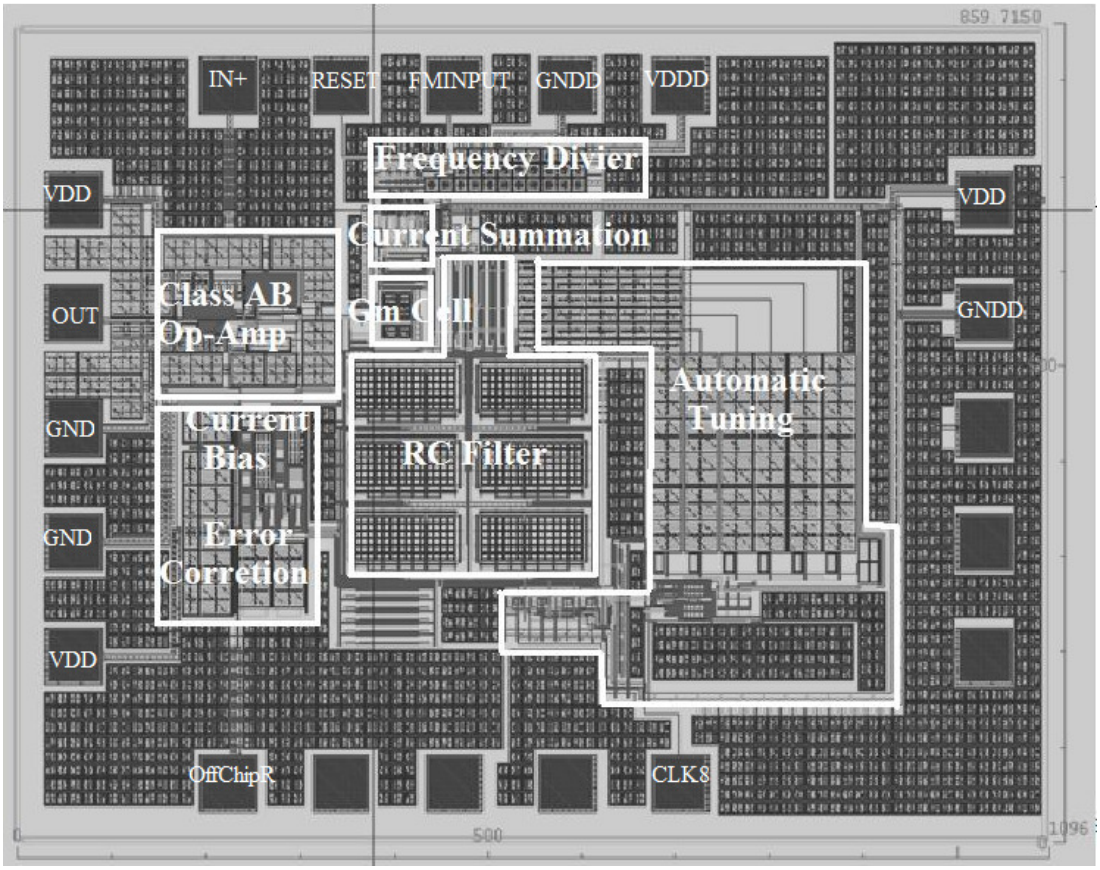

Figure 106 Layout of the complete FM harmonic rejection filter

CHAPTER VIII

CONCLUSION AND FUTURE WORK

8.1 Conclusion

Harmonic rejection filter is designed to filter FM square wave signal from 70MHz to 110MHz into FM sine wave signal. Based on Fourier series, the harmonic rejection technique adds the phase shifted square waves to achieve better THD and less high frequency harmonics. The phase shifting is realized through a frequency divider, and the summation is implemented through a current summation circuit. A RC low pass filter with automatic tuning is designed to further attenuate unwanted harmonics. Through using harmonic rejection technique along with third-order low pass filter, this work has achieved -53dB THD and harmonics above 800MHz attenuation of -99dB. The power consumption of the harmonic rejection filter and RC low pass filter is less than 0.7mW.

Output buffer stage is implemented through a resistor degenerated transconductor and a class-AB amplifier. Feedforward frequency compensation is applied to compensate the output class-AB stage, which extends the amplifier's operating bandwidth. A fully balanced class-AB driver is proposed to improve the driving capability of common source output transistors. The output buffer reaches -43dB THD at 110MHz with 0.63Vpp output swing and drives 1mW power on 50Ω load. The power consumption of the output buffer is 7.25mW.

8.2 Future Work and Directions

This harmonic rejection filter is designed to minimize total power consumption under low voltage supply. A newer and more advanced technology such as 90nm may give larger design margin in terms of speed, power, voltage headroom, etc. Using advanced technology, the frequency divider could easily operate at 1.76GHz frequency and generate higher yield rate than using TSMC 0.18um. With the advanced technology's low threshold voltage and high Ft, it could potentially increase the linearity of the output buffer stage without sacrificing the power budget.

Current steering cell is used for this harmonic rejection filter project. The mismatch effect causes the reduction of harmonic rejection. A rotary type of current summation circuit could be used in the future to systematically reduce the random mismatch among the current sources.

A two-stage polyphase harmonic rejection method [46] could be used in the future to realize rational weighting factor values. It could greatly improve the harmonic rejection method accuracy.

If more advanced technology were available, the buffer stage with better high frequency performance could be realized. The differential output buffer could be used directly to convert differential outputs from RC filter into the resistive load. Hence, transimpedance stage could be removed for further power saving.

REFERENCES

[1] M.S. Qureshi, and P.E. Allen, "70 MHz CMOS gm-C IF filter," in *Proc. IEEE ISCAS'05,* Kobe, Japan, May 2005, vol. 6, pp. 5946-5949.

[2] J.H. Huijsing, *Operational Amplifiers: Theory and Design.* Boston, MA: Kluwer, 2001.

[3] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and F. P. R. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE J. Solid-State Circuits*, vol. 36, pp. 2003–2015, Dec. 2001.

[4] S.W. Park, J.L. Ausin, F. Bahmani, and E. Sanchez-Sinencio, "Nonlinear shaping SC oscillator with enhanced linearity," *IEEE J. Solid-State Circuits*, vol.42, pp.2421-2431, Nov. 2007.

[5] H.H. Chang, J.Y.Chang, C.Y. Kuo, and S.I. Liu, "A 0.7-2-GHz self-calibrated multiphase delay-locked loop," *IEEE J. Solid-State Circuits*, vol.41, pp. 1051-1061, May 2006.

[6] G. Kim, M.K. Kim, B.S. Chang, and W. Kim, "A low-voltage, low-power CMOS delay element," *IEEE J. Solid-State Circuits*, vol.31, pp.966-971, Jul 1996.

[7] N.H.E Weste, and D. Harris, *CMOS VLSI Design A Circuits and Systems Perspective*, Boston, MA: Pearson/Addison-Wesley, 2005.

[8] J. Yuan and C. Svensson, "High speed CMOS circuit technique." *IEEE J. Solid-State Circuits*, vol.24, pp. 62-70, Feb. 1989.

[9] J. Yuan and C. Svensson, "New single-clock CMOS latches and flipflops with improved speed and power savings," *IEEE J. Solid-State Circuits*, vol.32, pp.62-69, Jan. 1997.

[10] Q. Huang and R. Rogenmoser, "A glitch-free single-phase CMOS DFF for gigahertz applications," in *Proc. IEEE ISCAS'94*, London, England, May 1994, vol.4, pp.11-14.

[11] N. Ghittori, A. Vigna, P. Malcovati, A. Baschirotto, and S. D'Amico, "A low-distortion 1.2 V DAC+filter for transmitters in wireless applications," in *Proc. IEEE ISCAS'05,* Kobe, Japan, May 2005, vol.1, pp. 776-779.

[12] J. Bastos, A.M. Marques, M.S.J. Steyaert, and W. Sansen, "A 12-bit intrinsic accuracy high-speed CMOS DAC," *IEEE J. Solid-State Circuits*, vol.33, pp.1959-1969, Dec. 1998.

[13] T. Oshima, K. Maio, W. Hioe, and Y. Shibahara, "Novel automatic tuning method of RC filters using a digital-DLL technique," *IEEE J. Solid-State Circuits*, vol.39, pp. 2052-2054, Nov. 2004.

[14] R.G. Meyer, "Low-power monolithic RF peak detector analysis," *IEEE J. Solid-State Circuits*, vol.30, pp.65-67, Jan 1995.

[15] S.M. Zhak, M.W. Baker, and R. Sarpeshkar, "A low-power wide dynamic range envelope detector," *IEEE J. Solid-State Circuits,* vol.38, pp. 1750-1753, Oct. 2003.

[16] D.M. Monticelli, "A quad CMOS single-supply op-amp with rail-to-rail output swing," *IEEE J. Solid-State Circuits*, vol.21, pp. 1026-1034, Dec. 1986.

[17] J.A. Fisher, "A high-performance CMOS power amplifier," *IEEE J. Solid-State Circuits*, vol.20, pp. 1200-1205, Dec. 1985.

[18] R. Hogervorst, J.P. Tero, R.G.H. Eschauzier, and J.H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol.29, pp.1505-1513, Dec. 1994.

[19] C.W. Lu, "High-speed driving scheme and compact high-speed low-power rail-to-rail class-B buffer amplifier for LCD applications," *IEEE J. Solid-State Circuits*, vol.39, pp. 1938-1947, Nov. 2004.

[20] G.A. Rincon-Mora, and R. Stair, "A low voltage, rail-to-rail, class-AB CMOS amplifier with high drive and low output impedance characteristics," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.,* vol.48, pp.753-761, Aug 2001.

[21] G. Palmisano, G. Palumbo, and R. Salerno, "CMOS output stages for low-voltage power supplies," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.,* vol.47, pp.96-104, Feb 2000.

[22] A. Torralba, R.G. Carvajal, J. Martinez-Heredia, and J. Ramirez-Angulo, "Class-AB output stage for low voltage CMOS op-amps with accurate quiescent current control," *Electron. Lett.*, vol.36, pp.1753-1754, Oct 2000.

[23] T. Stockstad, and H. Yoshizawa, "A 0.9-V 0.5-μA rail-to-rail CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol.37, pp.286-292, Mar 2002.

[24] W. Aloisi, G. Giustolisi, and G. Palumbo, "Design and comparison of very low-voltage CMOS output stages," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.52, pp. 1545-1556, Aug. 2005.

[25] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York: Wiley, 2001, pp.365-366.

[26] F. You; S.H.K. Embabi, and E. Sanchez-Sinencio, "Low-voltage class-AB buffers with quiescent current control," *IEEE J. Solid-State Circuits*, vol.33, pp.915-920, Jun 1998.

[27] J. H. Huijsing. “Multi-stage amplifier with capacitive nesting for frequency compensation.” U.S. Patent Appl. Ser. 602234, filed Apr. 19, 1984.

[28] R.G.H. Eschauzier, L.P.T. Kerklaan, and J.H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits*, vol.27, pp.1709-1717, Dec. 1992.

[29] F. You, S.H.K. Embabi, and E. Sanchez-Sinencio, "Multi-stage amplifier topologies with nested G_m-C compensation," *IEEE J. Solid-State Circuits*, vol.32, pp.2000-2011, Dec. 1997.

[30] W. Sansen, and Z.Y. Chang, "Feedforward compensation techniques for high-frequency CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol.25, pp.1590-1595, Dec. 1990.

[31] B.K. Thandri, and J. Silva-Martinez, "A robust feedforward compensation scheme for multi-stage operational transconductance amplifiers with no Miller capacitors," *IEEE J. Solid-State Circuits*, vol.38, pp. 237-243, Feb. 2003.

[32] B.Y.T. Kamath, R.G. Meyer, and P.R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits*, vol.9, pp. 347-352, Dec. 1974.

[33] R. G. H. Eschauzier and J. H. Huijsing, *Freqeucny Compensation Techniques for Low-Power Operational Amplifiers*. Norwell, MA: Kulwer, 1995.

[34] G. Di Cataldo, R. Mita, G. Palumbo, and S. Pennisi, "Reversed nested Miller compensation with voltage follower," in *Proc. IEEE ISCAS'02,* Scottsdale, AZ, May 2002 vol.2, pp. II-827-II-830.

[35] H. Lee, and P.K.T. Mok, "Active-feedback frequency-compensation technique for low-power multi-stage amplifiers," *IEEE J. Solid-State Circuits*, vol.38, pp. 511-520, Mar. 2003.

[36] H. Lee, and P.K.T. Mok, "Advances in active-feedback frequency compensation with power optimization and transient improvement," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol.51, pp. 1690-1696, Sept. 2004.

[37] X. Fan, C. Mishra, and E. Sanchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multi-stage amplifiers," *IEEE J. Solid-State Circuits*, vol.40, pp. 584-592, Mar. 2005.

[38] F. Zhu, S. Yan, J. Hu, and E. Sanchez-Sinencio, "Feedforward reversed nested Miller compensation techniques for three-stage amplifiers," in *Proc. IEEE ISCAS'05,* Kobe, Japan, May 2005, Vol. 3, pp. 2575-2578.

[39] A.D. Grasso, G. Palumbo, and S. Pennisi, "Active reversed nested Miller compensation for three-stage amplifiers," in *Proc. IEEE ISCAS'06* Island of Kos, Greece, May 2005, pp. 4.

[40] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in reversed nested miller compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.54, no.7, pp. 1459–1470, July 2007.

[41] B. Kelleci, *Practical Usage of Fast Fourier Transform (FFT)*, Nov. 2004.

[42] S. D'Amico, M. Conta, and A. Baschirotto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2713–2719, Dec. 2006.

[43] A. Vasilopoulos, G. Vitzilaios, G. Theodoratos, and Y. Papananos, "A low-power wideband reconfigurable integrated active-RC filter with 73dB SFDR," *IEEE J. Solid-State Circuits*, vol. 41, pp. 1997–2008, Sep. 2006.

[44] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, and K.A.I. Halonen, "A 240-MHz low-pass filter with variable gain in 65-nm CMOS for a UWB radio receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.56, no.7, pp. 1488-1499, July 2009.

[45] M. De Matteis, S. D'Amico, and A. Baschirotto, "A 0.55 V 60 dB-DR fourth-order analog baseband filter," *IEEE J. Solid-State Circuits*, vol.44, no.9, pp.2525-2534, Sept. 2009.

[46] Z. Ru, N. A. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *IEEE J. Solid-State Circuits,* vol.44, no.12, pp.3359-3375, Dec. 2009.

APPENDIX A

MATLAB HARMONIC REJECTION CIRCUIT MACROMODEL CODE

```
clear;clc;
samp=10 Me9;
dev=10e6;
t=[0:1/samp:3e-6-1/samp];
x=sin(2*pi*1e6*t);
y=fmmod(x,110e6,samp,dev);
square=2*((y>=0)-0.5);
%%z=fmdemod(square,1.76e9,40e9,2e6);
%%mag=abs(fft(z));
%%figure;plot(20*log10(mag));
clk=square;
D1=-1;D2=-1;D3=-1;D4=-1;
Q1=-1;Q2=-1;Q3=-1;Q4=-1;
Qbar1=1;Qbar2=1;Qbar3=1;Qbar4=1;
h1(1)=-1;h2(1)=-1;h3(1)=-1;h4(1)=-1;
for i=1:length(clk)-4;

[Q1,Qbar1] = stamp_DFF(clk(i+0),clk(i+1),D1,h1(i),(-h1(i)));
h1(i+1)=Q1;

[Q2,Qbar2] = stamp_DFF(clk(i+0),clk(i+1),h1(i),h2(i),(-h2(i)));
h2(i+1)=Q2;

[Q3,Qbar3] = stamp_DFF(clk(i+0),clk(i+1),h2(i),h3(i),(-h3(i)));
h3(i+1)=Q3;

[Q4,Qbar4] = stamp_DFF(clk(i+0),clk(i+1),h3(i),h4(i),(-h4(i)));
h4(i+1)=Q4;

D1=Qbar4;
end

htotal=h1+(2^0.5)*h2+h3;
% plot(htotal)
mag=fft(htotal);

figure;plot(20*log10(abs(mag)));
mag(1600:end-1600)=0;

filtered=real(ifft(mag));
z=fmdemod(filtered,110e6,samp,dev);
figure(2);
plot(z)

function [new_Q,new_Qbar]=stamp_DFF(clkI,clkII,D,new_Q,new_Qbar)
%persistent new_Q;
```

```
if  clkI<0 && clkII>=0
    new_Q=D;
    new_Qbar=-new_Q;
end
```

APPENDIX B

MATLAB HARMONIC REJECTION FILTER CIRCUIT MISMATCH EFFECT SIMULATION CODE

```
clc,
%%hist(1+0.05*randn(10000,1));
r1=1+1*0.028*randn(10000,1);
r2=1+1*0.028*randn(10000,1);
r3=1+1*0.028*randn(10000,1);
freq=110e6;
T=1/freq;
x=1/T;
td=T/16;
%%n=[0:0.01:20];
%%n=[1,3,5,7,9,11,13,15,17,19,21];
n=[3,5,7,9,11,13];
%%k0=sin(pi/16)*cos(0);
%%k1=sin(pi/16)*cos(pi/8*1)*r1;
%%k2=sin(pi/16)*cos(pi/8*2)*r2;
%%k3=sin(pi/16)*cos(pi/8*3)*r3;
k0=sin(pi/16)*cos(0)*(1-0.0004629);
k1=sin(pi/16)*cos(pi/8*1)*r1*(1-0.0013313);
k2=sin(pi/16)*cos(pi/8*2)*r2*(1-0.00000225);
k3=sin(pi/16)*cos(pi/8*3)*r3*(1-0.00010449);
y=k0+2*k1*cos(n*td*2*pi*x)+2*k2*cos(n*2*td*2*pi*x)+2*k3*cos(n*3*td*2*pi
*x);
%%db=20*log(sqrt(y.^2));
db=20*log10(abs(y));
scale=(0:0.001:0.04);
%%[scaler,out]=hist(y,scale);
i=0
for i=1:6
    dev(i)=std(y(:,i))

    i=i+1;
end

figure(1);
subplot(2,3,1);
hist(abs(y(:,1)),scale);
title('3rd Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);
%%surf(n,out,scaler);
subplot(2,3,2);
hist(abs(y(:,2)),scale);
```

```
title('5th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);
subplot(2,3,3);
hist(abs(y(:,3)),scale);
title('7th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);
subplot(2,3,4);
hist(abs(y(:,4)),scale);
title('9th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);
subplot(2,3,5);
hist(abs(y(:,5)),scale);
title('11th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);
subplot(2,3,6);
hist(abs(y(:,6)),scale);
title('13th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.04);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1200]);

w1=sin(pi/16)*cos(pi/8*1);
w2=sin(pi/16)*cos(pi/8*2);
w3=sin(pi/16)*cos(pi/8*3);

r4=1+1*0.01*randn(10000,1);
r5=1+1*0.01*randn(10000,1);
r6=1+1*0.01*randn(10000,1);

td1=r4*T/16;
```

```
td2=r5*T/16;
td3=r6*T/16;

n2=[3,5,7,9,11,13];

y2phase=k0+2*w1*cos(td1*2*pi*x*n2)+2*w2*cos(2*td2*2*pi*x*n2)+2*w3*cos(3
*td3*2*pi*x*n2);
%%db=20*log(sqrt(y.^2));
db=20*log10(abs(y2phase));
scale=(-0.2:0.001:0.2);
%%[scaler,out]=hist(y,scale);

for i=7:12
    dev(i)=std(y2phase(:,i-6))
    i=i+1;
end

figure(2);
subplot(3,2,1);
hist(abs(y2phase(:,1)),scale);
title('3th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.4);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
%%set(gca, 'XTickLabel',{'inf','-34','-28','-24.4','-22','-20'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,1350]);
%%surf(n,out,scaler);
subplot(3,2,2);
hist(abs(y2phase(:,2)),scale);
title('5th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.01:0.4);
set(gca, 'XTickLabel',{'inf','-40','-34','-30','-28'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.04,0,800]);
subplot(3,2,3);
hist(abs(y2phase(:,3)),scale);
title('7th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.02:0.1);
set(gca, 'XTickLabel',{'inf','-34','-28','-24.4','-22','-20'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.1,0,600]);
subplot(3,2,4);
hist(abs(y2phase(:,4)),scale);
title('9th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.02:0.1);
set(gca, 'XTickLabel',{'inf','-34','-28','-24.4','-22','-20'});
```

```
xlabel('(dB)');
ylabel('(density)');
axis([0,0.1,0,400]);
subplot(3,2,5);
hist(abs(y2phase(:,5)),scale);
title('11th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.02:0.1);
set(gca, 'XTickLabel',{'inf','-34','-28','-24.4','-22','-20'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.1,0,400]);
subplot(3,2,6);
hist(abs(y2phase(:,6)),scale);
title('13th Hamonic Rejection');
grid on
set(gca, 'XTick', 0:0.02:0.1);
set(gca, 'XTickLabel',{'inf','-34','-28','-24.4','-22','-20'});
xlabel('(dB)');
ylabel('(density)');
axis([0,0.1,0,400]);

figure(3);
scale2=(-120:2:0);
hist(db,scale2);

r4=1+1*0.05*randn(100000,1);
k4=cos(pi/4)*r4;
y2=k0*(1+2*k4*cos(n*2*td*2*pi*x));
figure(4); plot(y2)
```

VITA

Shan Huang was born in Tianjin China. He received the B.Sc.Eng. degree in electrical engineering from University of Alberta, Edmonton, Canada in 2006. In 2010, he received the M.S. degree in electrical engineering from Texas A&M University in College Station, Texas. His master research was on low power filters, high performance class-AB amplifiers, and automatic tuning design. From January 2009 to August 2009, he interned in Broadcom Inc, Andover, MA, where he was involved in the performance characterization and design of a new generation network processor chip (part# BCM88025).

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