A 3RD-ORDER CONTINUOUS-TIME LOW-PASS SIGMA-DELTA (ΣΔ) ANALOG-TO-DIGITAL CONVERTER FOR WIDEBAND APPLICATIONS

An Honors Fellows Thesis

by

KUN MO KIM

Submitted to the Honors Programs Office
Texas A&M University
in partial fulfillment of the requirements for the designation as

HONORS UNDERGRADUATE RESEARCH FELLOW

April 2011

Major: Electrical Engineering

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Approved by:

Research Advisor: Jose Silva-Martinez
Associate Director of the Honors Programs Office: Dave A. Louis

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ABSTRACT

A 3rd-order Continuous-Time Low-Pass Sigma-Delta (ΣΔ) Analog-to-Digital Converter for Wideband Applications. (April 2011)

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This thesis presents the design of a 20 MHz bandwidth 3rd-order continuous-time low-pass sigma-delta analog-to-digital converter with low-noise and low-power consumption using TSMC 0.18 μm CMOS technology. The bandwidth of the system is selected to be able to accommodate WiMAX and other wireless network standards. A 3rd-order filter with feed-forward architecture is selected to achieve low-power consumption as well as less complexity. The system uses 3-bit flash quantizer to provide fast data conversion. The current-steering DAC not only achieves low-power and less current sensitivity, but also it helps directly inject the feedback signal without additional circuitries. In order to avoid degradation of the overall performance, cross-coupled transistors are adopted to reduce the current glitches.

The proposed system achieves a peak SNDR of 65.9 dB in 20 MHz bandwidth, and consumes 31.735 mW from a 1.8 V supply. The entire circuit is driven by a sampling

rate at 500 MHz. The measured in-band IM3 of this thesis is -69 dB with 600 mV_{p-p} two tone signal peak-to-peak voltage.

DEDICATION

I would like to dedicate this Honors thesis to my family, who has mentally supported me throughout my life. I would also like to give great thanks to my fiancé, Jessica Kim, who has been with me through the good times and bad times, and supporting me while I was going through hardships during my college career. I appreciate my mentors, Jong Rak Hyun, Junghoon Lee, Kyu ha Choe, Keytaek Lee, and Jusung Kim, for being there when I needed them as well.

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I firstly would like to thank my advisor, Dr. Jose Silva-Martinez, for providing support and encouragement throughout this research work. He not only agreed to be my research advisor, but also gave me technical advice whenever I faced obstacles. His broad knowledge of theory of ΣΔ modulator and design methodology of ADC significantly helped me to successfully realize and simulate this work. Throughout his support of this work, I learned different aspects of analog circuit design as well as a broad knowledge of problem solving skills and graduate level study.

I also greatly appreciate Dr. Samuel Palermo for his close mentorship and also for providing me with various research opportunities throughout my sophomore and junior years. He has been my research advisor since I was a sophomore. He has always encouraged me to keep studying in analog and mixed-signal circuit design, and guided me to be an expert of analog circuit design by sharing his academic experiences. The filter design is successfully done with his fruitful comments and suggestions.

Moreover, I would like to thank my colleagues, Mohan Geddada, Jusung Kim, Chang Joon Park, Arun Sundar, Yang Su, and Lakshminarasimhan Krishnan, for spending their time to discuss with me and helping me to design and simulate the system I implemented. Without their help, I would not have been able to finish this thesis.

NOMENCLATURE

ADC	Analog-to-Digital Converter
BP	Band-Pass
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DR	Dynamic Range
HP	High-Pass
LP	Low-Pass
LSB	Least-Significant Bit
MSB	Most-Significant Bit
NMOS	Negative-Channel Metal-Oxide-Semiconductor
OSR	Oversampling Ratio
PMOS	Positive-Channel Metal-Oxide-Semiconductor
ΣΔ	Sigma-Delta
SNDR	Signal-to-Noise Distortion Ratio
SNR	Signal-to-Noise Ratio
SQNR	Signal-to-Quantization Noise Ratio
t	Time
T	Temperature

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CHAPTER I

INTRODUCTION

This thesis introduces the basic theory of a ΣΔ modulator and describes the design methodology of a 3rd-order Low-Pass ΣΔ ADC (Sigma-Delta Analog-to-Digital Converter) for wideband applications. The design methodology contains various design considerations, which the system needs to tolerate. In a sense of system implementations, the circuits including a 3rd-order low-pass filter, a summing amplifier, a 3-bit quantizer, and a DAC (Digital-to-Analog Converter) are implemented at the transistor level to ensure whether the system satisfies the given specifications. This paper also presents several other techniques that are used in previous publications to achieve a low-power, a high linearity, and a high dynamic range.

Motivation

As wireless networks are being rapidly developed, the network transceivers demand a faster data transfer rate and a wider bandwidth of communication. Recent developments in mobile computing and wireless internet have led to exponential growth in demand for portable computers and smart phones that require low-power and low-cost specifications, which accommodate 802.11 a/b/g/n WLAN (Wireless Local Area Network) standards.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

Currently, WiMAX (Worldwide Interoperability for Microwave Access) protocol, which is denoted as IEEE 802.16e WLAN standards, is a hot issue in the telecommunication research area. Not only is WiMAX able to provide broadband wireless access as an alternative to cable and DSL, but also is a possible replacement candidate for cellular phone technology such as GSM and CDMA. The design of the transceiver chip for WiMAX, however, is not that simple due to the required high-frequency bandwidth, fast data transfer rates, and strict noise specifications. In addition, providing this wide of a bandwidth is a huge burden to an analog circuit designer because of the performance degradation from parasitic capacitances and other external/internal process variations existing on the chip.

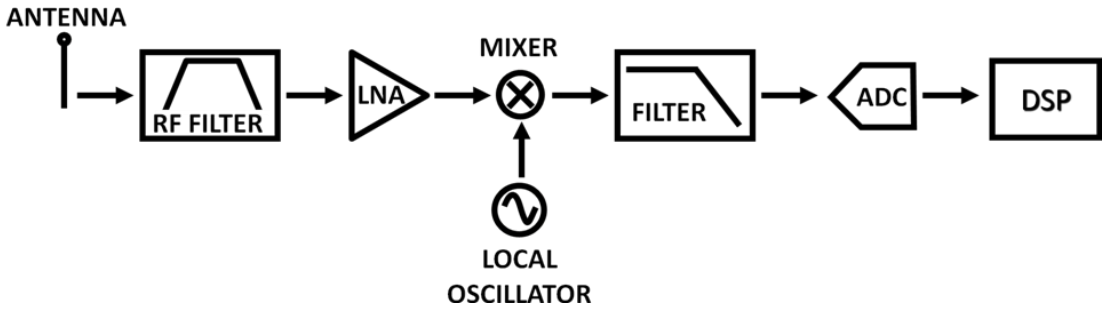

Figure 1. Basic system block diagram of a wireless receiver.

Fig. 1 illustrates the system block diagrams of a wireless receiver. This is a very generic diagram, and most of wireless network devices employ the structure shown in Fig. 1. It is critically important to place an ADC close to an antenna, so that the signal processing can be taken in digital domain as soon as possible. The signals converted into digital domain will further boost up the speed and flexibility of the system while reducing the

complexity. Furthermore, depending on the architecture of the receiver, the ADC will be asked to digitize different signals, such as Radio Frequency (RF), Intermediate-Frequency (IF), or base-band signal [1]. Therefore, the ADC will significantly affect the overall performance of receiver in terms of power consumption, complexity, and cost.

Due to the importance of the ADC in the wireless transceivers, ΣΔ ADCs (Sigma-Delta Analog-to-Digital Converter) has been attracting great attention. ΣΔ ADCs have been developed along with the development of digital communication. ΣΔ ADCs are considered one of the high performance ADCs due to its characteristics of low-power consumption, low-noise performance, wide bandwidth, and high dynamic range. Because of these various advantages of ΣΔ ADCs, most wireless network devices prefer to employ ΣΔ ADCs for efficient data conversion.

The objective of this work is to implement a 3^{rd}-order Continuous-Time Low-Pass ΣΔ ADC accommodating wideband, which is 20 MHz to adopt WiMAX protocol. TSMC 0.18 μm CMOS technology is used in order to implement the system at the transistor level. Not only would this system be suitable to accommodate WiMAX wireless standards, but also be feasible to adopt applications of the next generation.

Overview of analog-to-digital converter architecture

The ADC architectures can be separated into two groups based on the sampling frequency and the bandwidth of the input signal: Nyquist-rate and Oversampling. The

Nyquist-rate ADC architecture has low-resolution and low-bandwidth, but very fast speed. Flash ADCs, for instance, are categorized under the Nyquist-rate ADC architecture. In contrast, oversampling ADC architecture has characteristics of high resolutions and low-noise due to the noise shaping. The ΣΔ ADC is often considered a representative of oversampling ADC architectures.

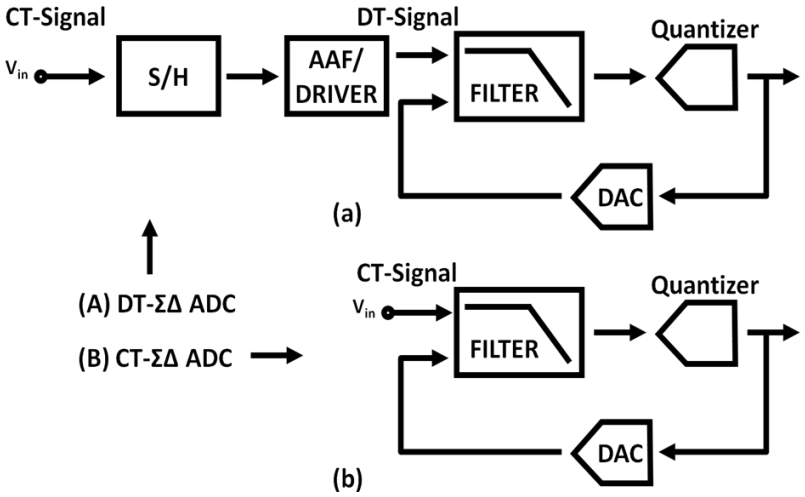

Figure 2. (a) Discrete-Time ΣΔ ADC has additional circuitries, such as a sample-and-hold circuit, an anti-aliasing filter, and a driver circuit, whereas (b) Continuous-Time ΣΔ ADC directly receives continuous-time signals into the filter.

As shown in Fig. 2, ΣΔ ADC generally operates in two different domains: Discrete-Time (DT) and Continuous-Time (CT) domain. Since both of the DT ΣΔ ADC and the CT ΣΔ ADC share the same building blocks within the loop, the way how to distinguish one from the other is analyzing the loop filter characteristics. In previous years, ΣΔ ADC has been implemented in discrete-time domain, which mostly employed switched-capacitor technique. Since the DT ΣΔ ADC takes the advantages of the digital domain, they result in a fast speed and a high flexibility. However, the anti-alias filter (AAF) is needed to

prevent signals around multiples of the output sampling rate from aliasing down in-band. The sampling rate, therefore, can be at least twice the fundamental frequency of the signal of interest. Moreover, driver circuit is also needed to isolate CT signals from the switched-capacitor stage. Consequently, the DT ΣΔ ADC has been suffering from the hungry of power, and the inherent complexity due to the additional circuitries. In contrast, CT ΣΔ ADC recently reported impressive performance due to its wide bandwidth by help from the rapid development of the CMOS technology [2]. The CT ΣΔ ADC directly accepts CT signals, thus the system no longer needs the AAF and driver circuit. Although aliasing still occurs when sampling takes place, the sampling and the injection of quantization error occur simultaneously. In other words, the alias can be attenuated at least as much as the quantization noise. These advantages consequently reduce the complexity and the power consumption of the system, which are indispensible to optimize the performance of the wireless transceivers. Because of these advantages of the CT ΣΔ ADC, the recent researches of ΣΔ ADC for wideband applications are more focused on the continuous-time domain, and are introduced in the next subsection.

Literature review

Table 1 shows the measured performance of several ΣΔ ADCs for wideband applications (BW ≥ 10 MHz) published in the past five years (2006 ~ 2011). From the list below, previously published ADCs mostly adopted CT type filter. It can be obviously observed that the DT ΣΔ ADC is only used when the sampling frequency and bandwidth are lower

than 10 MHz. Moreover, for high sampling frequency systems, they often employed 1-bit quantizer. This is because using a single-bit quantizer can alleviate the mismatch issues. By doing so, the system can achieve low-power system while it does not necessarily require dynamic element matching (DEM) devices. The CMOS technology is dominantly used for most of wideband ΣΔ ADCs, while the SiG technology is used to achieve ultra-wide bandwidth (≥ 20 MHz) or very high clock frequency (≥ 1 GHz). The SiGe technology, however consumes more power than the CMOS technology does.

This work, the 3rd-order continuous-time low-pass ΣΔ modulator, is compared with the previously published works to observe which aspects the 3rd-order filter leads or losses. As Table 1 shows, 3rd-order or 2nd-order system consume less power than the higher-order system. Comparing this work with previously reported works, this work does not show the best performance among the list, but is highly competitive. Since this work does not require DEM, and employed 3rd-order filter, it can be seen that the proposed system has relatively less complexity than any other system shown in Table 1. Moreover, the proposed work also has very efficient power consumption with respect to SNDR and bandwidth among 3rd-order systems shown in the table. Comparing this work with 3rd-order system using 0.18 μm technology, the proposed work shows almost the best performance among the competitors.

Table 1. Literature survey of previously published ΣΔ ADCs for wideband (≥ 10 MHz)

Ref	Type of ΣΔ ADC	Fs (MHz)	BW (MHz)	SNDR (dB)	Power (mW)	Technology
[3]	5^{th} CT 3bit LP	400	25	67.7	48	0.18 μm CMOS
[4]	3^{rd} CT 1bit LP	640	10	66	7.5	0.18 μm CMOS
[5]	5^{th} CT 4bit LP	400	25/20	52/56	18	0.18 μm CMOS
[6]	3^{rd} CT 4-bit LP	640	20	63.9	58	0.13 μm CMOS
[7]	2^{nd} CT 2-bit LP	640	20	51.4	6	0.13 μm CMOS
[8]	3^{rd} CT 4bit LP	640	20	74	20	0.13 μm CMOS
[9]	3^{rd} CT N-bit	250	20	60	10.5	65 nm CMOS
[10]	3^{rd} DT 3.5-bit	26-400	0.1-20	86-70	2-34	0.13 μm CMOS
[11]	4^{th} CT VCO (N-bit)	900	20	78	87	0.13 μm CMOS
[12]	2^{nd} CT VCO (5-bit)	900/1000	10/20	72/67	40	0.13 μm CMOS
[13]	3^{rd} CT 4-bit LP	200	20	49	103	0.18 μm CMOS
[14]	4^{th} CT 1-bit BP	40000	60	55	1600	0.13 μm SiGe
[15]	2^{nd} CT 1-bit LP	40000	500	37	350	0.13 μm SiGe
This work	3^{rd} CT 3-bit LP	500	20	65.9	31.735	0.18 μm CMOS

Another survey has been taken to display the research tendency in ΣΔ ADC. The survey in Fig. 3 shows the DT and CT ΣΔ ADC results of publications from 1999 to 2011. The recent publications, which are published from 2009 to 2011, are emphasized by green triangle symbols and purple circle symbols. The results are displayed in terms of the bandwidth of systems and their SNDR in dB scale. As figure shows, the SNDR and bandwidth increase as technology develops, but there is still a trade-off between bandwidth and SNDR. Most recent works published from 2009 to 2011 are concentrated in the region where bandwidth is from 100 kHz to 20 MHz, and SNDR is from 60 dB to 81 dB. This work concentrates on the region where a peak SNDR is from 60 dB to 70dB

with a bandwidth of 20 MHz. The literature survey also illustrates that using 0.18 μm technology, the implementation of our target specification is highly competitive in terms of power consumption and SNR.

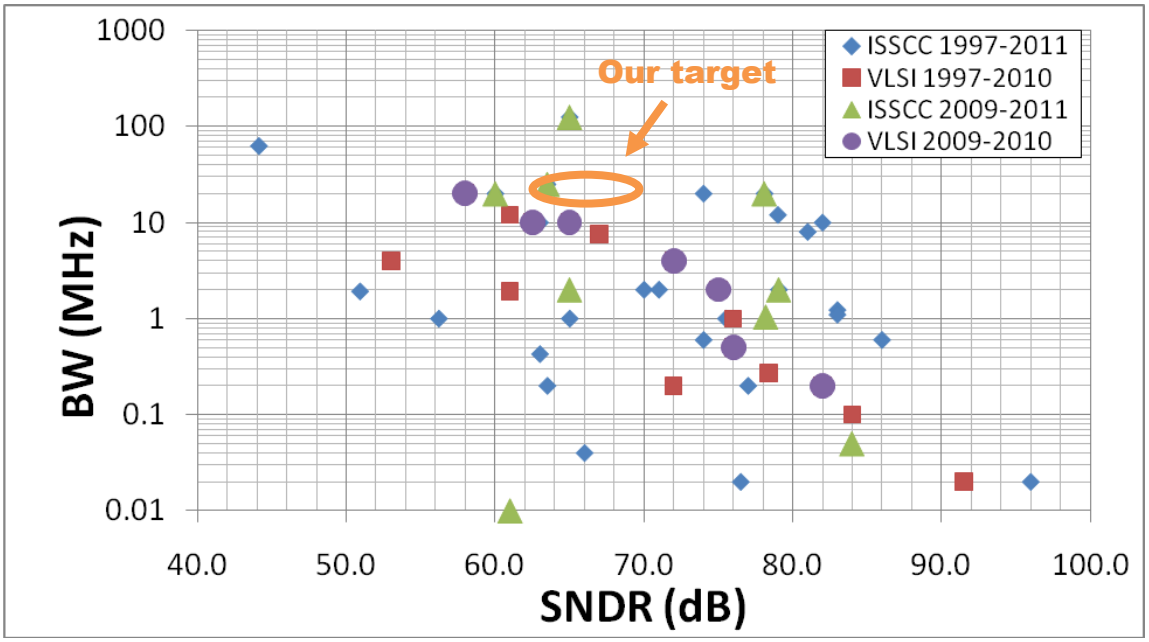

Figure 3. ADC performance survey from 1997 to 2011. Data is provided from [16].

Organization of the thesis

There are total of four chapters in this thesis, which provides introduction, overview of sigma-delta modulator, circuit implementations, and summary and conclusion. Chapter I provides the motivation of the thesis as well as the brief introduction of ADC architecture. The ADC architecture part covers the history of ADCs and important design considerations for ADCs.

Chapter II provides basic background knowledge about ΣΔ ADCs. The information covered in this chapter will further help readers to understand about what the sigma-delta is, and how the ΣΔ ADCs work.

Chapter III presents detailed information about circuit implementations at the system level and the transistor level. The system level simulation exhibits the expected simulation results of the ΣΔ ADC. The transistor level analysis provides the actual circuit implementation of each system block and simulated results. The circuit implementations include a 3^{rd}-order Low-Pass filter, a summing amplifier, a 3-bit flash ADC, and a current steering DAC. The chapter also covers the correlation between the system level design and the transistor level design.

In Chapter IV, the results of the design of a 3^{rd}-order Low-Pass ΣΔ ADC system is discussed. The discussion is mainly based on the simulation results obtained from Chapter III. Overall performances, such as linearity and stability, are evaluated in this chapter. Summarizations, conclusions, and future work are discussed.

CHAPTER II

OVERVIEW OF SIGMA-DELTA MODULATOR

This chapter gives an overview of the operation and basic theory of the sigma-delta modulator, which includes sigma-delta modulation, quantization, and noise-shaping. Critical parameters of the sigma-delta modulator will also be introduced with system implementations.

Oversampling data converter vs. Nyquist-rate data converter

Data converters, such as ADC and DAC, can be categorized into two main groups: Nyquist-rate and oversampling. The Nyquist-rate is a classic sampling theory that states the minimum sampling rate needs to be equal to twice the highest frequency contained within the signal in order to avoid aliasing. Thus, Nyquist sampling rate can be expressed as

$$f_{Nyquist} = 2 \cdot f_{signal}$$

By doing so, the Nyquist-rate ensures that the reconstructed signal is not corrupted by aliasing. However, the problem existing on the Nyquist-rate data converter is the linearity issue and the speed issue. The linearity of the Nyquist-rate data converter is dominantly determined by matching the accuracy of the analog components, such as resistors, capacitors, and current sources. Moreover, because of low sampling rates, the Nyquist-rate data converter is somewhat unfeasible for many applications requiring high-speed and high-linearity.

The oversampling, however, is another sampling theory that states the sampling rate is higher than the Nyquist sampling rate by a factor of oversampling ratio (OSR). The OSR is typically chosen between 8 and 512, and can be expressed as

$$OSR = \frac{f_{sampling}}{2 f_{signal}}$$

The advantages of the oversampling data converters are that the oversampling not only helps avoid aliasing, but also provides high resolution and low quantization noise. In addition, due to its high sampling rate, the oversampling data converter is suitable for many applications requiring high-speed. However, oversampling does not necessarily increase the linearity of the data converter. Therefore, the linearity of the oversampling data converter can be defined by the linearity of the loop filter within the data converter.

Sigma-delta modulation

The two main types of oversampling modulator are the Delta and the Sigma-Delta modulator. The Delta modulator simply generates output based on the difference between a sample of the input and an expected value of the sample. The analysis of the Delta-modulator gives

$$v(n) = u(n) - u(n-1) + e(n) - e(n-1)$$

The advantage of the Delta modulator is that the difference signal of input and output of the integrator (*u(n)-u(n-1)*) from the above equation is much smaller than the input signal, thus, the modulator allows a larger input signal [17]. In addition to the advantage of the Delta modulator, the implementation is relatively easier than other modulators for

the ADC system. However, the critical problem of the Delta modulator is that due to the high gain of the filter, the filter also amplifies the non-linear distortion of the DAC. Thus, the Delta modulator is no longer suitable for the current wireless network standards, which requires high bandwidth and low noise systems.

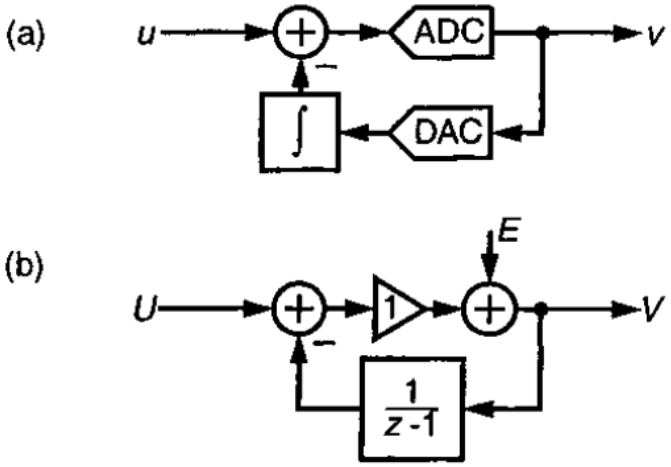

Figure 4. (a) Delta modulator used as an ADC and (b) its linear z-domain model [17].

The Sigma-Delta modulator is inspired by the Delta modulator shown in Fig. 4. The name of the Sigma-Delta modulator is derived from the fact that the output is the sum of the differences between an actual sample of the input and an expected value of the sample [17]. As shown in Fig. 5, the Sigma-Delta modulator is simply derived from the Delta modulator by moving the integrator from the output of DAC to the input of the ADC. By doing so, the amplification of in-band noise and distortion does not take place. Moreover, if the loop filter has a high gain, the in-band quantization noise is strongly attenuated. With higher order filters, the noise is even more attenuated. This noise attenuation is generally called noise-shaping, which will be discussed in the next sub-

sections. Generally, a ΣΔ modulator shapes the noise in a high-pass form, so that the low-pass filter can highly suppress the noise accumulated over high frequency band.

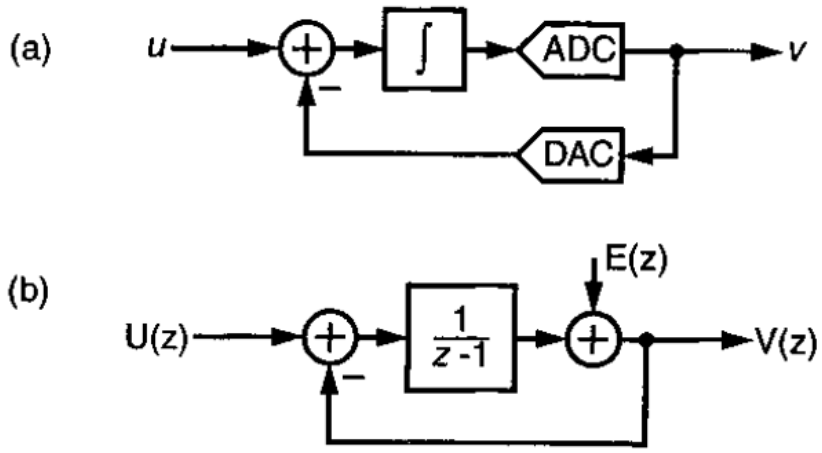

Figure 5. (a) Sigma-delta modulator used as an ADC and (b) its linear z-domain model [17].

The analysis of the Sigma-Delta modulator gives

$$v(n) = u(n-1) + e(n) - e(n-1)$$

From the expression, we can see that the digital output contains a delayed input signal *u* as well as the quantization error *e*. The above equations will be further analyzed in the next sub-sections.

Quantization error and noise shaping

One of the critical noises resulting from the ΣΔ modulator is quantization error. It is often called quantization noise as well. The Sigma-Delta modulator contains two blocks generating the most dominant noise over the system: ADC and DAC. The signals converted by ADCs most suffer from a quantization noise. Literally, the quantization

error is simply a difference between the original signal and a quantized signal. Fig. 6 displays the quantization error in a 3-bit flash ADC. As the figure shows, the quantization error is uniformly distributed between -1/2 LSB and +1/2 LSB. Therefore, the quantization error is treated as additive white noise at the system level.

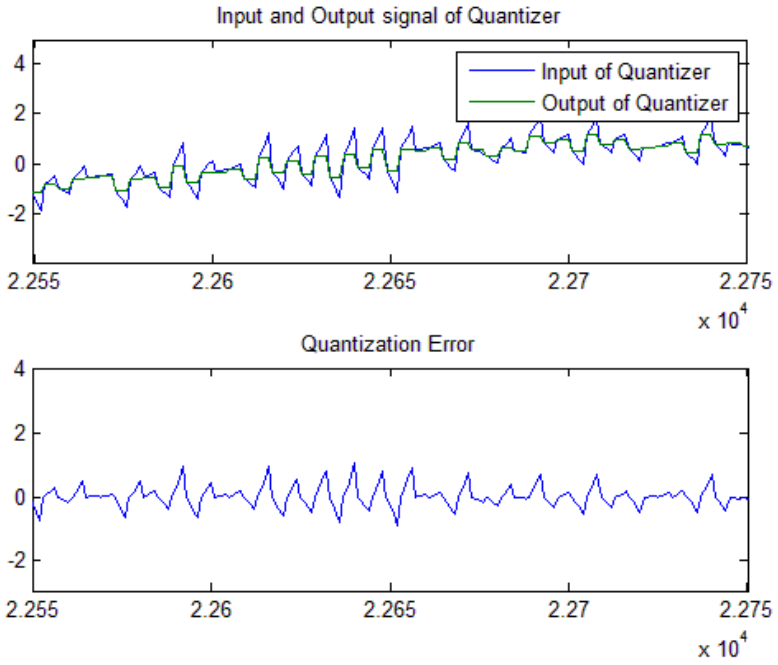

Figure 6. Quantization noise for a 3-bit flash ADC.

The output noise of the 1st-order Sigma-Delta modulator due to the quantization error can also be expressed as

$$q(n) = e(n) - e(n-1)$$

In Z-domain, this expression becomes

$$Q(z) = (1 - z^{-1})E(z)$$

The coefficient, $1-z^{-1}$, is called the noise-transfer function (NTF), and it has a high-pass frequency response, which suppress the quantization noise at the low-frequency band. This plays an important role in the Sigma-Delta modulator, and is called noise-shaping. The noise-shaping works by putting the quantization error in a feedback loop. Fig. 7 displays the NTF having a high-pass frequency response. Therefore, the Sigma-Delta modulator can attenuate the quantization noise lying on the baseband by noise-shaping without affecting the desired signal band.

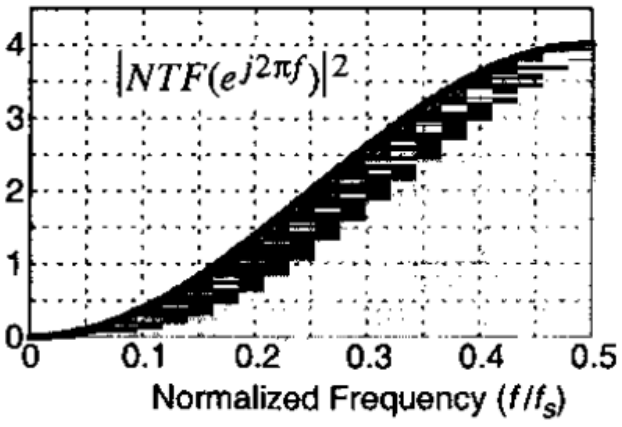

Figure 7. Noise transfer function of the 1st-order sigma-delta modulator [17].

Performance parameters of sigma-delta modulator

Several performance parameters should be measured in order to ensure the quality of the Sigma-Delta modulator. These performance parameters include Dynamic Range, Signal-to-Noise Ratio, Signal-to-Noise and Distortion Ratio, Effective Number of Bits, and Power Consumption. These of parameters are directly related to the accuracy of the system. Most ΣΔ modulators are operating in a very high clock frequency, thus the

system needs to qualify how much distortion the system itself can tolerate. The follow subsections briefly introduce what kind of parameters the designer needs to be aware of and how they can be measured. In exception, power consumption is not dealt with in this chapter. It will be discussed in detail in Chapter III.

Dynamic range

The dynamic range (DR) of a Sigma-Delta modulator is defined as the ratio of the maximum input signal to the minimum input signal. In other words, the DR represents how much of the input signal the Sigma-Delta modulator can allow.

Signal-to-noise ratio

The Signal-to-Noise Ratio (SNR) is a measure that shows how much a signal has been corrupted by noise. This noise is mainly composed of the noise from transistors, such as thermal noise and flicker noise. The concepts of SNR and DR are closely related.

Signal-to-noise and distortion ratio

Not only the SNR and the DR of the system is important to the Sigma-Delta modulator, but also the Signal-to-Noise and Distortion Ratio (SNDR) is another critical aspect. In the ideal Sigma-Delta modulator, the total noise and distortion power is equal to the quantization noise power. However, in a real world, the size of transistors will not be perfectly matched, hence it causes distortion in the system, which corresponds to the Signal-to-Distortion Ratio (SDR). Moreover, due to the nature of the CMOS transistors,

the system implemented by CMOS always suffers from the flicker noise and the thermal noise produced from transistors. These internal noises affect the SNDR of the system. Consequently, the SNDR is simply composed of SNR + SDR.

Effective number of bits

A general way to measure the accuracy of the Sigma-Delta modulator is measuring the Effective Number of Bits (ENOB), which is also known as the resolution. Since the Sigma-Delta modulator is operating in a very fast speed, the accuracy is one of the most important parameters that need to be ensured. The relationship between ENOB and Signal-to-Noise Ratio (SNR) is expressed as

$$ENOB = \frac{SNR - 1.76}{6.02}$$

CHAPTER III

SYSTEM LEVEL ANALYSIS AND CIRCUIT IMPLEMENTATION

This chapter provides the design methodology of a 3rd-order continuous-time low-pass ΣΔ ADC at the system level and the transistor level. It is important for the circuit designers to be familiar with the correlation between the system level and transistor level.

System level design and analysis

This work presents a 3rd-order continuous-time low-pass ΣΔ modulator that achieves over 60 dB SNDR with 20 MHz bandwidth. The architecture shown in Fig. 8 contains a 3-bit flash type quantizer and a 3-bit current-steering DAC. The 3rd-order filter is implemented using a biquad filter, and a single-pole lossy-integrator. Since the amplifier employed the feed-forward architecture, the summing amplifier is needed to ensure the stability of the 3rd-order loop filter, and to provide direct path to the 3-bit quantizer.

In addition to the filter design, comparing with a 5th-order filter, the 3rd-order filter is selected for this work to reduce the power consumption and the complexity. Although the 5th-order filter definitely has a much steeper roll-off than the 3rd-order filter, the out-of-band signal is not in our interest. Therefore, the steeper roll-off would not affect too much to the overall system performance. Furthermore, a low-pass ΣΔ modulator usually employs an odd-order filter in order to make the baseband as flat as possible. Having an even-order filter would not be able to make the baseband flat because the filter would

more likely function as bandpass filters. Thereby signal peaks would appear on the frequency response, which is not desired in our low-pass filter system.

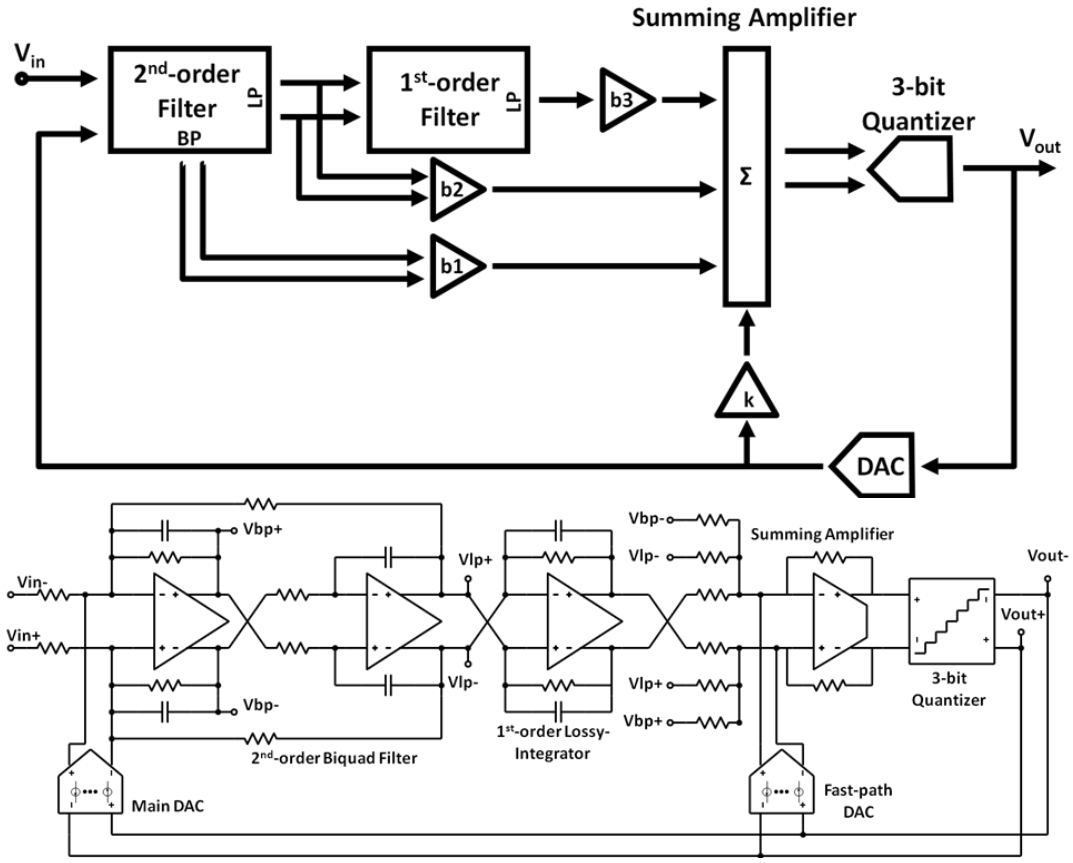

Figure 8. System architecture of the 3rd-order sigma-delta ADC.

The system level analysis assumes that the ΣΔ ADC is composed of ideal system blocks. Throughout the system level analysis, the designer can expect what the ideal results would be and how to make the systems properly function. The system architecture of the proposed work is shown in Fig. 8. As shown in the figure, the system includes 3rd-order filter with one biquad filter and one lossy-integrator. Since the filter is using the feed-

forward architecture for its stability compensator, the summing amplifier is placed at the end of filters. A 3-bit quantizer provides 7 digital levels from the analog input signal, and DAC provides two different feedback paths, one for main feedback signal, and another one for stability. Table 2 shows the design parameters for Matlab simulation.

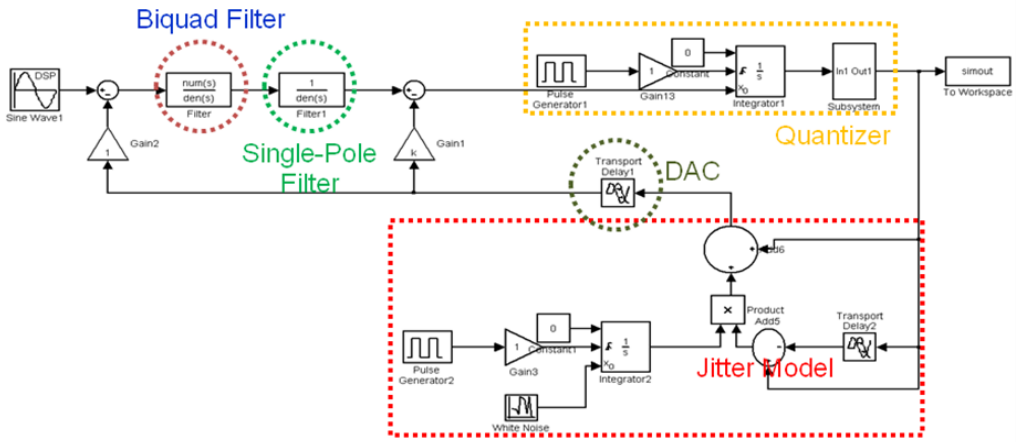

Figure 9. Simulation configuration of a 3rd-order sigma-delta ADC with jitter model inserted.

Table 2. System level design parameters for 3rd-order continuous-time low-pass ΣΔ modulator

Design parameter	Value
Bandwidth	20 MHz
Sampling Frequency	500 MHz
Out-of-band Gain	2.8
Oversampling Ratio (OSR)	12.5
Order of the filter system	3rd order
Quantizer resolution	3 bits
Targeted resolution	10 bits (61.96 dB)

The simulation configuration in Matlab is shown in Fig. 9. In this schematic, the sinusoidal input with a frequency of 7.1 MHz is injected to the system. In Fig. 9, summing amplifier is simply ignored and replaced with a simple adder. This is because the system transfer function of the biquad filter and the single-pole filter already includes the system transfer function of the summing amplifier. The 3-bit quantizer simply converts the analog signal into 3-bit digital form. The digital-to-analog (DAC) block can be simply illustrated as a delay element on the Simulink. Jitter model is also implemented on the Simulink to observe how it affects to the SNDR of the system.

Figs. 10 and 11 show the AC responses of the biquad filter and the single-pole filter, respectively. The biquad filter has a low frequency gain of 20 dB, and a center frequency of 15.4 MHz. The single-pole filter has a low frequency gain of 23.8 dB, and a dominant pole at 4.08 MHz. After these two systems are cascaded, the AC response gives the low frequency gain of 45.9 dB, center frequency of 15.4 MHz, and phase margin of 76 º while the Gain Bandwidth Product is at 164 MHz. The result is shown in Fig. 12. The system level simulation generally shows the expected result of the circuit level system.

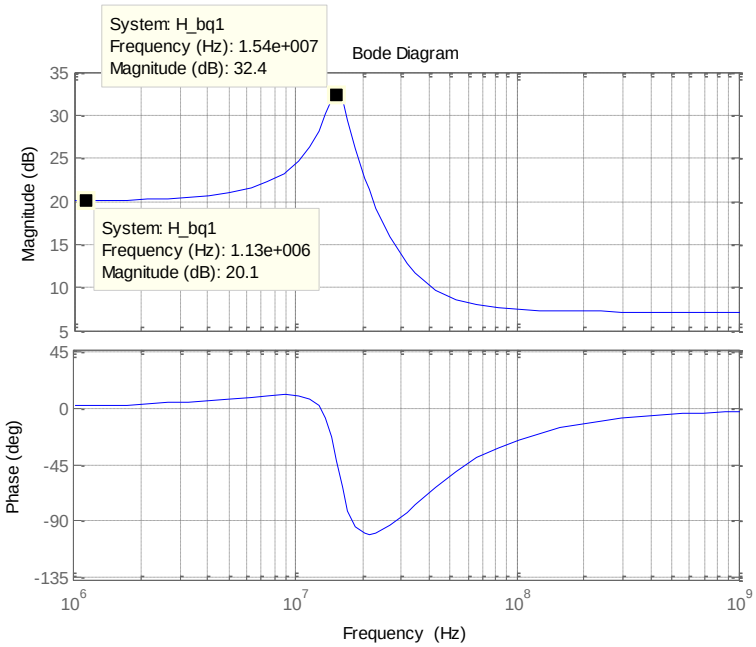

Figure 10. AC response of the biquad filter at the system level.

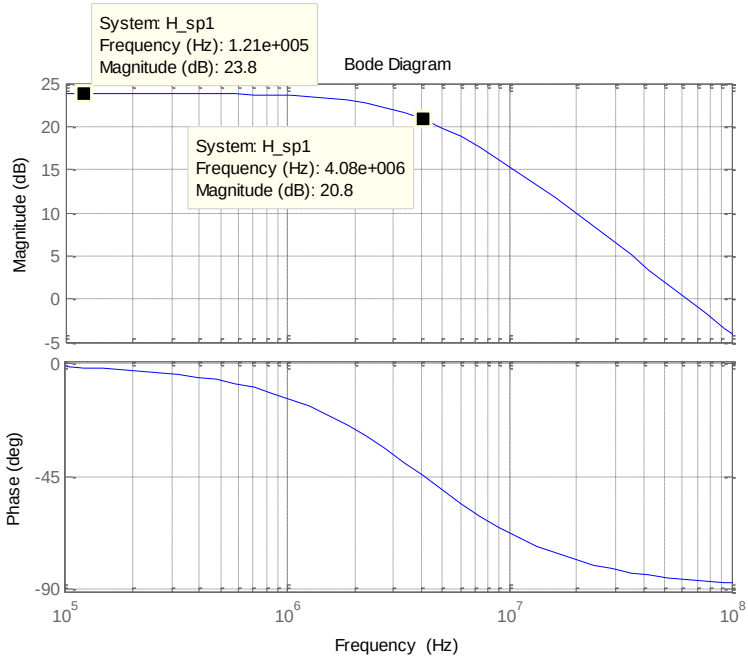

Figure 11. AC response of the lossy-integrator at the system level.

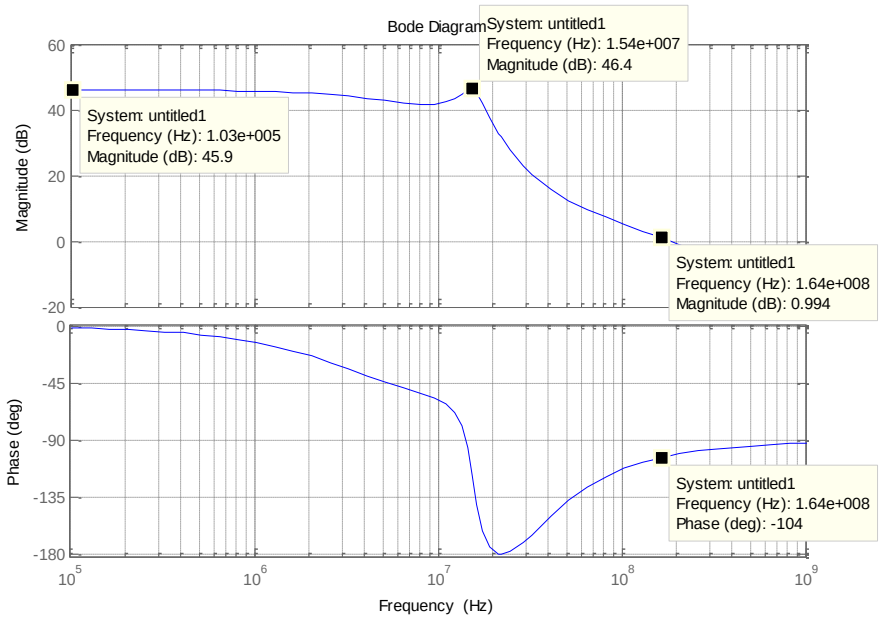

Figure 12. AC response of the 3rd-order low-pass filter.

Considering the design of a high-resolution ΣΔ ADC, the linearity performance of the DAC feedback at the quantizer input becomes a limiting factor of the overall performance. This is because non-linearity errors on DACs cannot be noise-shaped by the ΣΔ dynamics. In order to adjust the gain of DAC feedback, which is also known as a feed-forward gain, designers can trade off a feed-forward gain with the oversampling ratio (OSR) and the out-of-band gain (OBG). For this particular ΣΔ ADC project, feed-forward gain needs to be less than 2. With an OSR of 12.5, signal bandwidth of 20 MHz, and an out-of-band gain of 2.8, the optimized SNR value, the maximum noise transfer function (NTF) gain, and the dynamic range (DR) are shown in Fig. 13. From Fig. 13, the expected DR is 65 dB. When the input signal is injected with a frequency of 7.1 MHz, the system gives a SNDR of 70.8 dB (Fig. 14). Considering the high bandwidth of

the system, this SNR value is sufficiently high enough to endure external/internal noises and variations. The signal to distortion ratio (SDR) is ignored in the Matlab simulation.

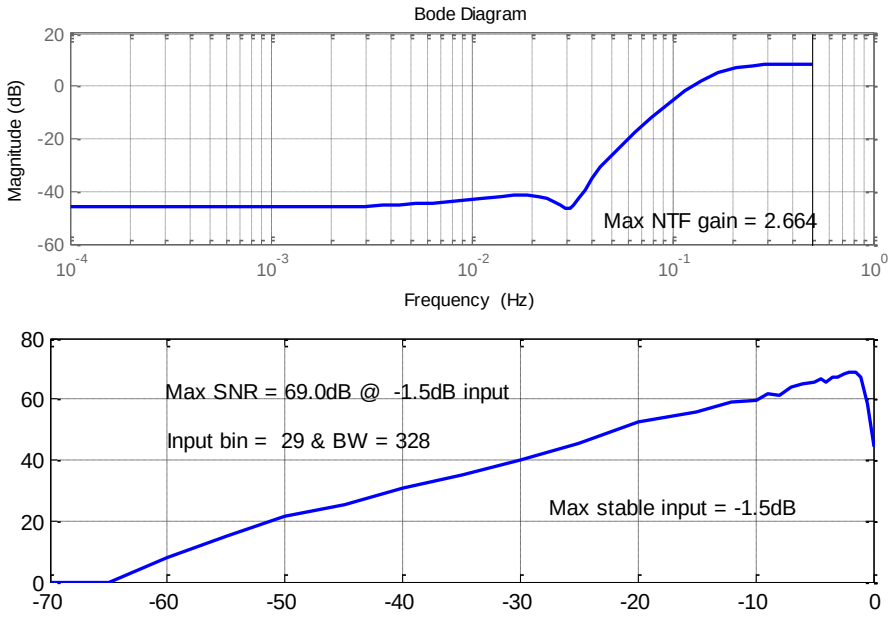

Figure 13. A noise transfer function and a dynamic range of the ΣΔ modulator.

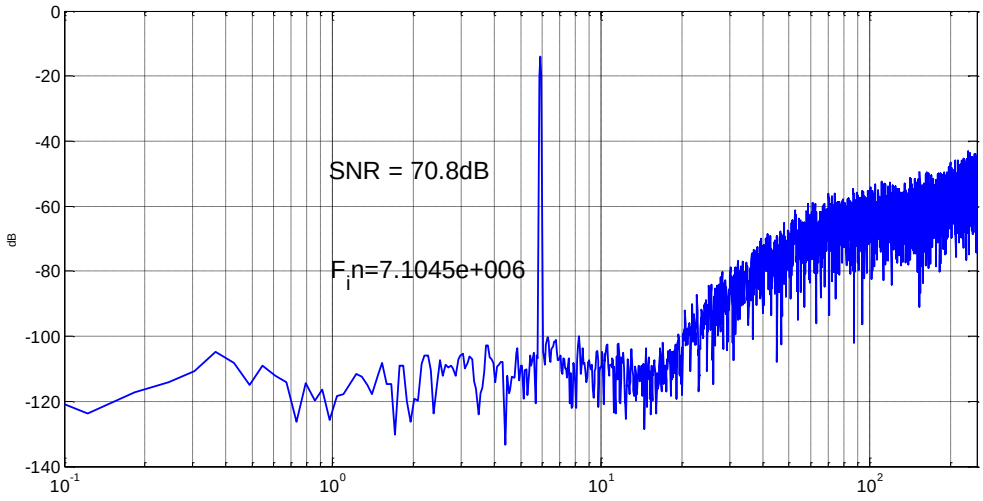

Figure 14. Simulated SNR with an input frequency of 7.1 MHz. SDR is ignored in the Matlab simulation.

When the phase noise (jitter) is considered in the ΣΔ ADC as shown in Fig. 15, the SNR decreases significantly depending on the power level of the jitter. Since the entire design is running along with very fast clock frequency, a small amount of phase noise can critically ruin the synchronization and thus, distort the linearity of the system. Hence, if the system cannot tolerate a certain level of jitter, the system will not be able to meet the required SNR (≥ 60 dB) in the real world. The simulation result shows that when the variance of jitter noise is $20*10^{-6}$, the SNDR stays around 60 dB (Fig. 16), but once the jitter power goes above, performance drastically decreases.

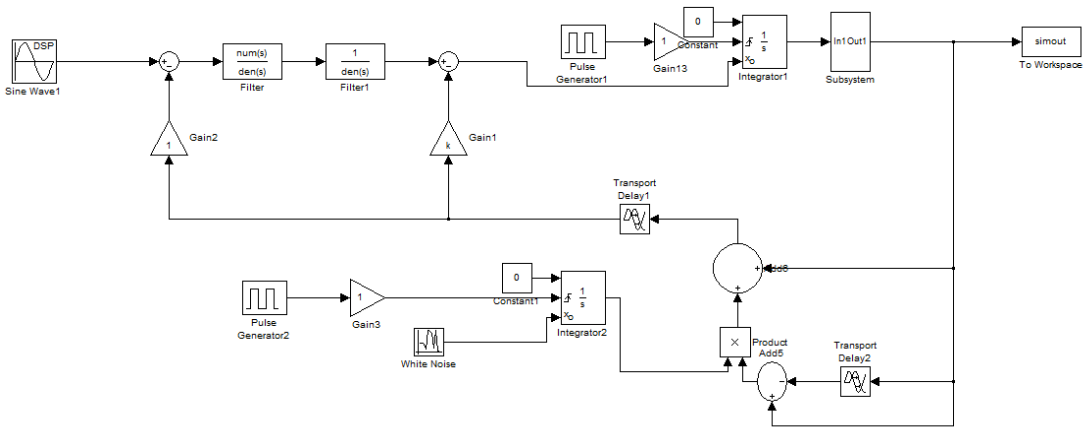

Figure 15. Matlab configuration for jitter simulation.

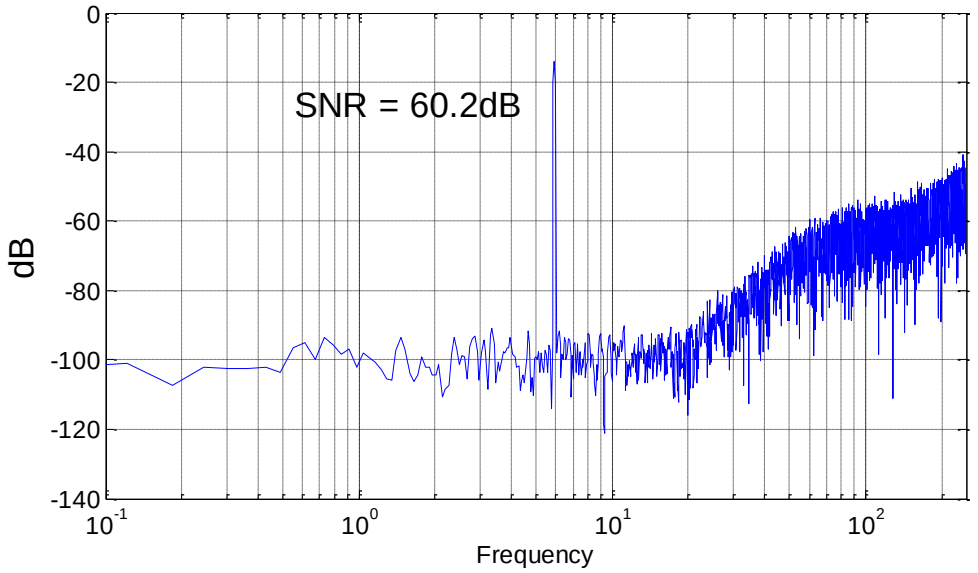

Figure 16. The peak SNR of the system when the jitter is injected (with $\sigma^2 = 20*10^{-6}$).

Transistor level design and analysis

The design of the circuit blocks which are used in this wideband CT ΣΔ ADC modulator is presented in detail. Each circuit is realized using TSMC 0.18 μm CMOS technology. Cadence is used as a circuit simulation tool to simulate the implementations.

TSMC 0.18 μm CMOS technology is used in order to provide wide signal bandwidth up to 20 MHz. Using small length of transistors are less affected by parasitic capacitors. However, the gain of transistor will be reduced because small transistors exhibit higher leakage currents, lower output resistance, and lower transconductance [18]. As transistor size decreases, the sensitivity of CMOS current to drain voltage increases. Due to the increment of current leakages, drain-to-source voltage drastically drops, hence the current through CMOS significantly changes. As a result of the change of the current,

the output impedance decreases and this results in decrement of the gain. In addition to the effect of a smaller transistor, the transconductance of CMOS is proportional to electron mobility. As transistor size decreases, the fields in the channel and dopant impurity increase. Thus, electron mobility decreases.

Two types of compensators are generally used in ΣΔ ADCs: Feedback and feed-forward. The feedback architecture provides more robust and better sensitivity to PVT variations, but consumes more power than the feed-forward architecture. The feed-forward architecture is highly sensitive to DAC errors, but provides low power consumption, high linearity, and less complexity. Since one of the most important objectives of this work is the low-power system, feed-forward architecture is preferred to be used. Simple flash type of quantizer is used to implement the 3-bit quantizer for conversion from analog to digital. Flash type of quantizer is the most general implementation for quantizer because of its fast speed and easy implementation. Current-steering type of DAC is used to realize DAC. The advantage of current-steering DAC is that it can directly inject feedback signal from the DAC without any additional circuitries. Moreover, current-steering DAC has less current sensitivity, and less power consumption. However, glitches at each input signal transition degrades the overall performance.

Biquad filter

In this section, the specifications and the simulation results of the biquad filter are provided. The biquad filter is a two-pole filter topology that can be available in Low-Pass, High-Pass, Band-Pass, and Notch responses. Moreover, using the fully-differential input and output, the number of Op-Amps (Operational Amplifiers) required is reduced from 3 to 2. Usually, an odd-order filter is generally preferred to be employed in a LP ΣΔ ADC because it has less number of poles than an even-order filter, while the performance is almost the same in a pass-band region. An even-order filter can also be used if the system requires a steeper roll-off and if the band-pass filter is desired. However, most low-pass ΣΔ ADC systems only interest in a pass-band region, thus the steeper roll-off does not have a significant effect on the overall performance.

Specifications

Specifications for the 2^{nd}-order filter are shown in Table 3.

Table 3. Specification of the biquad filter

Objects	Specifications
Technology	TSMC 0.18 μm CMOS Technology
Power supply	V_{DD} = 0.18 V, V_{SS} = GND
Bandwidth	20 MHz
Low-frequency gain	20 dB
Power	≤ 10 mW
3^{rd} intermodulation distortion (IM3)	≤ -68 dB (400 mV_{p-p})
Quality factor	4
Input referred integrated noise	≤ 100 μV/√ Hz

In order to provide a low-frequency gain of 20 dB, each amplifier may need to have more than a 40 dB gain. This is because the system performance is decreased by noise, non-linearity, and offset requirements. In addition, since the first stage amplifier would be significantly suffer from these non-idealities, strict design procedure and noise/variation specifications may need to be carefully specified.

As it is mentioned above, the recent mobile computing requires a low-power system. The power consumption of the biquad filter part, therefore, should be less than 10 mW to configure the low-power consumption system. In addition to the description of the listed specifications, when the implementation comes to a real situation, one of the critical issues that mainly degrade the linearity of the system is the 3rd harmonic intermodulation distortion (IM3). Since the IM3 are located at very close to the fundamental frequency, elimination of these harmonics is significantly challenged. Therefore, these harmonics would be the most critical distortion that reduces the signal-to-noise ratio (SNR) of the entire system. As shown in Table 1, IM3 less than -68 dB at 20 MHz would be reasonable to prevent further decrement of the linearity from the intermodulation distortion.

The quality factor, which is typically denoted as Q, is selected to be 4 for the biquad filter. Having Q of 4 would not only attenuate the impact of additional high-frequency power components, but also reduce a ringing at the output [19]. Since the system is implemented in 2nd-order, the output signal might contain a peak at 3-dB frequency in

the frequency response. However, due to the small amount of Q, this peak would not be a serious problem.

Operational amplifier

Fig. 17 illustrates the schematic of the Operational-Amplifier (Op-Amp) at the transistor level. In Fig. 17, the two-stage Op-Amps with a common-mode feedback (CMFB) network are selected in order to provide high gain at the low-frequency. This two-stage Op-Amp would provide sufficient gain to achieve at least 40 dB DC-gain, but stability and low-bandwidth are potential problems. Table 4 includes its design parameters.

To enhance the stability of the amplifier, two different CMFB techniques are applied. The first CMFB stage can be found in the first stage of the amplifier. Two R1 resistors connected in parallel with transistors simply detect the common-mode signal [20]. For instance, when the common-mode signal at V_{g1} increases, then the voltage between R1s reduces the V_{sg} of MP_1s. As a result of the reduction of V_{sg}, the current flowing through MP_1 and MN_1 decreases, hence it eventually decreases the common-mode signal.

In perspective of differential-mode, since the center of R_1s is AC ground, the output impedance is dominated by the R_1s. In order to keep the gain high enough, high resistance of R_1 needs to be selected. In this design, R_1 of 80 kΩ is selected.

The common-mode level of the second stage output is controlled by a CFMB circuit consisting of R2, C, MN4, and MP4. The output common-mode level is detected by using resistive averaging (R2). The common-mode signal at the output of second stage is fed back into the node V_{CMFB} for DC level regulation. Stability is also enhanced by adding two small capacitors (C).

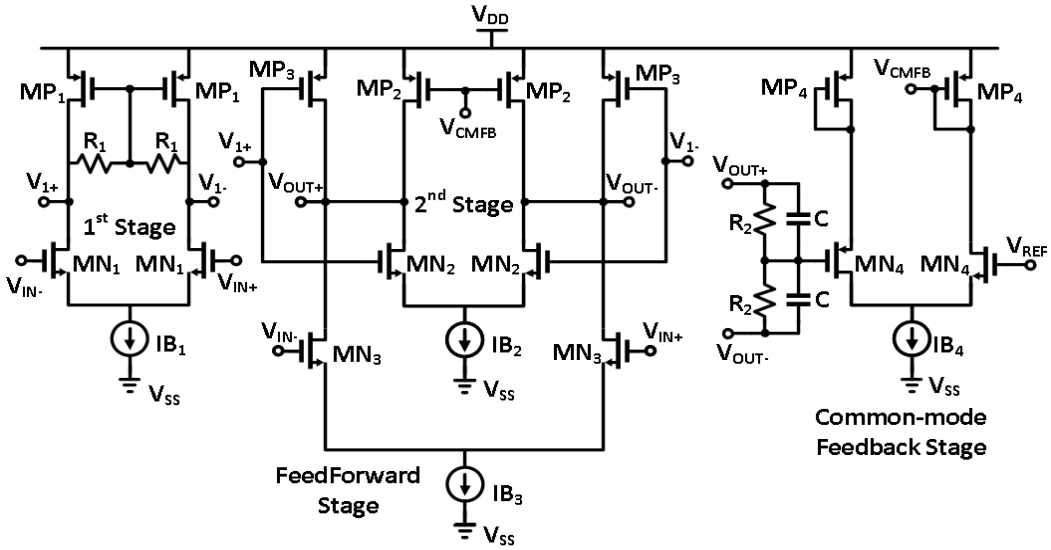

Figure 17. Schematic of the amplifier at the transistor level.

Table 4. Transistor dimentions and device values for the amplifier.

Device	Dimensions (μm)	Device	Dimensions
MN_1	150 / 0.6	IB_1	450 μA
MP_1	63 / 0.4	IB_2	800 μA
MN_2	28 / 0.4	IB_3	600 μA
MP_2	36 / 0.4	IB_4	600 μA
MN_3	60 / 0.3	R_1	80 kΩ
MP_3	90 / 0.4	R_2	80 kΩ
MN_4	120 / 0.3	C	100 fF
MP_4	36 / 0.4		

To provide bandwidth of 20 MHz, the Gain Bandwidth Product (GBW) also needs to be high enough. According to [21], pole-zero cancellation technique would efficiently designers to further increase GBW. This technique generates a zero on the left-half-plane (LHP) at the same location as the second pole, thus it cancels the effect of second pole, which decreases GBW. Using this pole-zero cancellation technique, GBW of the amplifier is able to achieve 2.3 GHz.

To maximize the output swing of this amplifier, cascode design is intentionally avoided. Since the TSMC 0.18 μm technology uses V_{DD} of 1.8 V and V_{SS} of 0 V, using the cascode structure would not allow the circuit to provide enough voltage output swings.

Table 5 presents the transistor dimensions, device values, and other bias conditions for the amplifier. The dimensions used in this amplifier are almost the same as the ones used in [1], though the simulation results and specifications are different.

The first stage of the amplifier is designed to achieve high gain and dominant pole at its output. The gain of the first stage is determined by the transconductance of MN_1 and output impedance of MN_1 and MP_1. The dominant pole location is determined by the parasitic capacitances of MN_1 and MP_1. Output swing of the first stage does not need to be concerned because the signal will be further amplified by the gain of the second stage. The combination of the second stage (MN_2, MP_2) and feed-forward stage (MN_3, MP_3) are optimized to produce wide bandwidth (20 MHz). As I mentioned above, having a

LHP zero right at the location where the second pole lies would further increase the GBW, thus the filter obtains broad bandwidth. Furthermore, for better linearity, MN_2 and MP_2 are designed to have high V_{DSAT}. High-selected V_{DSAT} greatly contributes to produce high signal output voltage swing. Further mathematical analysis of the amplifier is given in the next sub-section.

Table 5. Summary of the performance of the amplifier

Parameters	Values
Low-frequency gain (DC gain)	67.11 dB
Bandwidth	4.713 MHz
Gain Bandwidth Product (GBW)	2.3 GHz
Phase Margin (PM)	56.3 °
Power Consumption	4.6 mW
Input referred integrated noise (in 20 MHz)	15.06 uV

Detailed information of the biquad filter

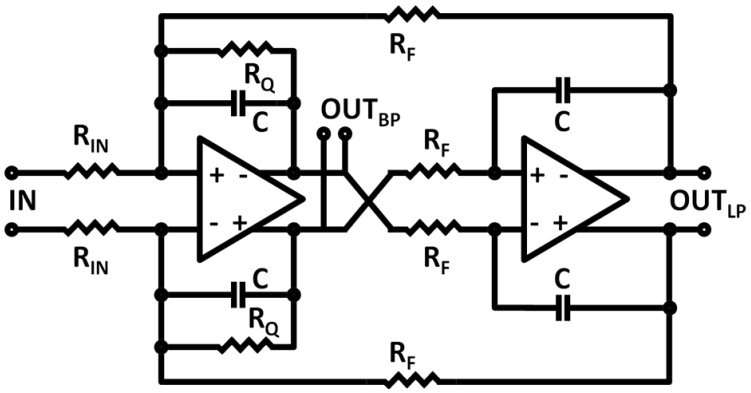

Figure 18. Macro-model of the biquad filter.

Table 6. Component values used in the implementation

Parameters	Values
R_{IN}	1 kΩ
R_F	10 kΩ
R_Q	40.5 kΩ
C	970 fF

The macro-model of the proposed biquad filter is shown in Fig. 18. As it is shown in the figure, the system is operating in fully differential input and output, and schematic of Fig. 17 is applied to configure each amplifier. Table 6 shows the component values used in the biquad filter implementation. The system transfer function of the biquad filter is given below.

$$H_{BP} = \frac{s/(R_{in}C)}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} = \frac{1}{R_{in}C}\frac{s}{s^2 + s\frac{1}{R_QC} + \frac{1}{R_FC}^2}$$

$$H_{LP} = H_{LP0}\frac{\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} = \frac{R_F}{R_{in}}\frac{1/(R_FC)^2}{s^2 + s\frac{1}{R_QC} + \frac{1}{R_FC}^2}$$

$$\omega_0 = \frac{1}{R_FC}$$

$$Q = \frac{R_Q}{R_F}$$

$$H_{BP}(\omega_0) = \frac{R_Q}{R_{in}}$$

$$H_{LP}(0) = \frac{R_F}{R_{in}}$$

According to [19] and the above equation, low-frequency gain, center frequency, and Q factor of the biquad filter are determined by $R_F/R_{IN,}$ $1/(R_FC)$, and R_Q/R_F, respectively. In other words, once the value of R_{IN} is determined, the rest of the components will be automatically configured. Therefore, determining the value of RIN is the critical procedure in the biquad filter design. The input-referred noise of the biquad filter can be expressed as

$$V_{in,n}^2 = 4kTR_{in}[1 + \frac{R_{in}}{R_F} + \frac{R_{in}}{R_Q}] + 4kTR_F \mid sCR_F \mid^2$$

$$+ [V_{n,a1}^2 + V_{n,a2}^2 \mid sCR_F \mid^2] \mid \frac{R_{in}}{R_Q} + sCR_{in} \mid^2$$

In the above equation, $V^2_{n,a1}$ and $V^2_{n,a2}$ represent the input-referred noise of the first and second amplifier, respectively. Moreover, by looking at the equations, it can easily be

observed that the main noise contribution, especially low-frequency noise, comes from the first stage amplifier and input resistor R_{IN}. The parameters used in the implementation of Fig. 18 are listed below.

In the actual implementation, the center-frequency (peak frequency) and a Q factor are not exactly defined by $1/(R_F C)$, but a slightly lower due to the external and internal variations, and mainly parasitic capacitances. Thus, the values shown in Table 2 are slightly off from the expected value, which are R_Q = 40 kΩ and C = 1.0193 pF.

Simulation results

Figs. 19 and 20 displays the AC responses of the amplifier and its loop gain. DC-gain of the stand-alone amplifier is measured as 67.11 dB, and the dominant pole is located at 4.713 MHz. Phase margin is 56.3 °at unity gain frequency of 2.3 GHz.

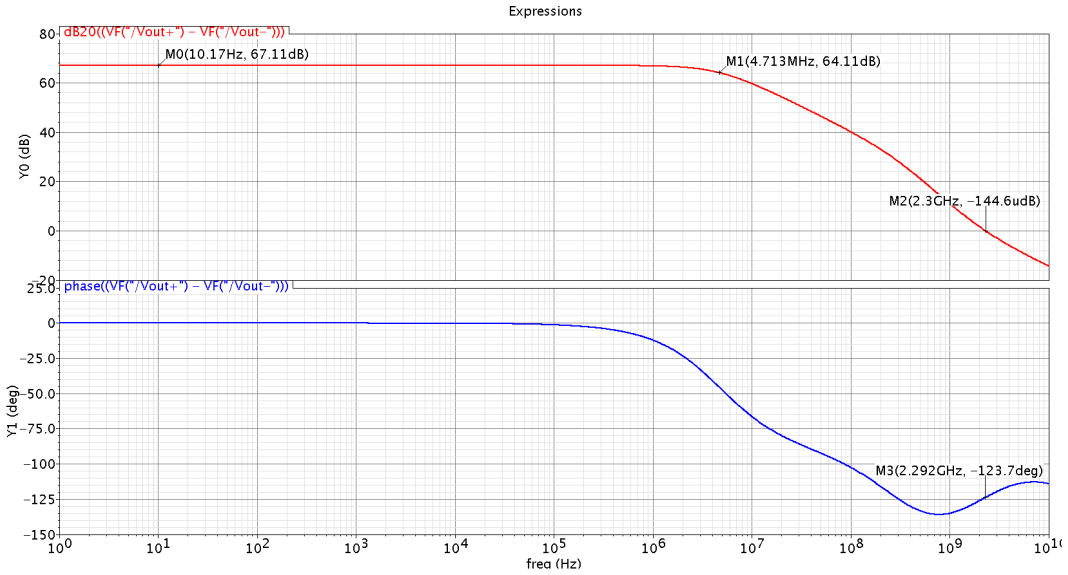

Figure 19. AC response of the amplifier. Av0=67.11dB, fp1=4.71 MHz, GBW=2.3 GHz.

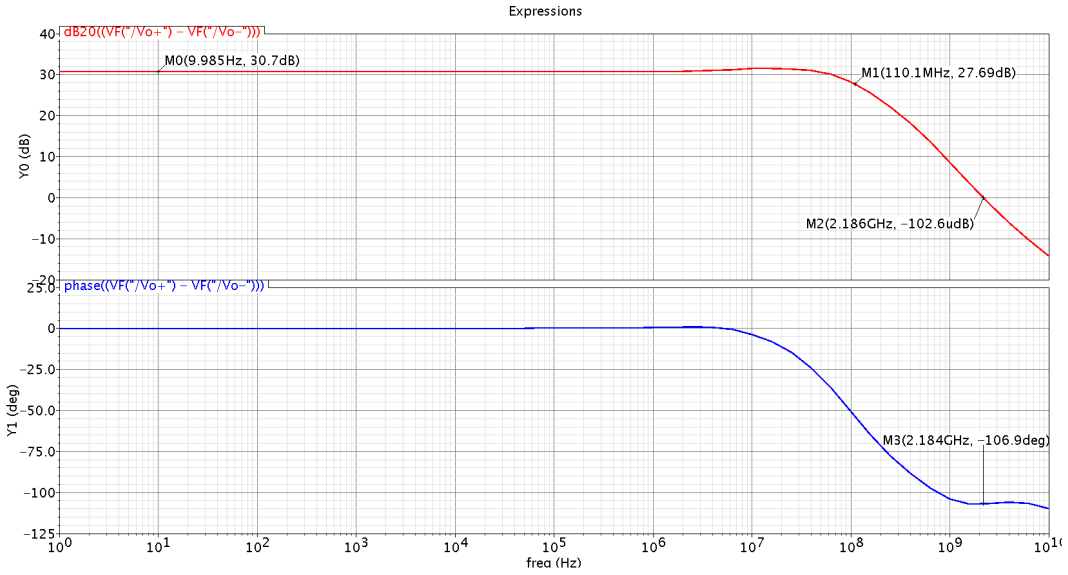

Figure 20. Loop gain of the amplifier. fp1=110 MHz and PM =73.1 º.

Since the amplifier is used in the biquad filter, the loop gain of the amplifier needs to be considered for analyzing the stability. The load effect of this loop gain includes the R_Q,

R_F, C, and R_F. Hence, the loop gain is expressed as the product of amplifier open-loop transfer function and the feedback factor. Measured DC gain of the loop gain is 30.7 dB, and it has a dominant pole at 4.713 MHz. It also achieved 73.1 ºphase margin at the unity gain frequency of 2.186 GHz. Thus, the result proves that the enough stability of the amplifier is secured. To further check the stability of the entire system, the loop gain of biquad filter is measured as well.

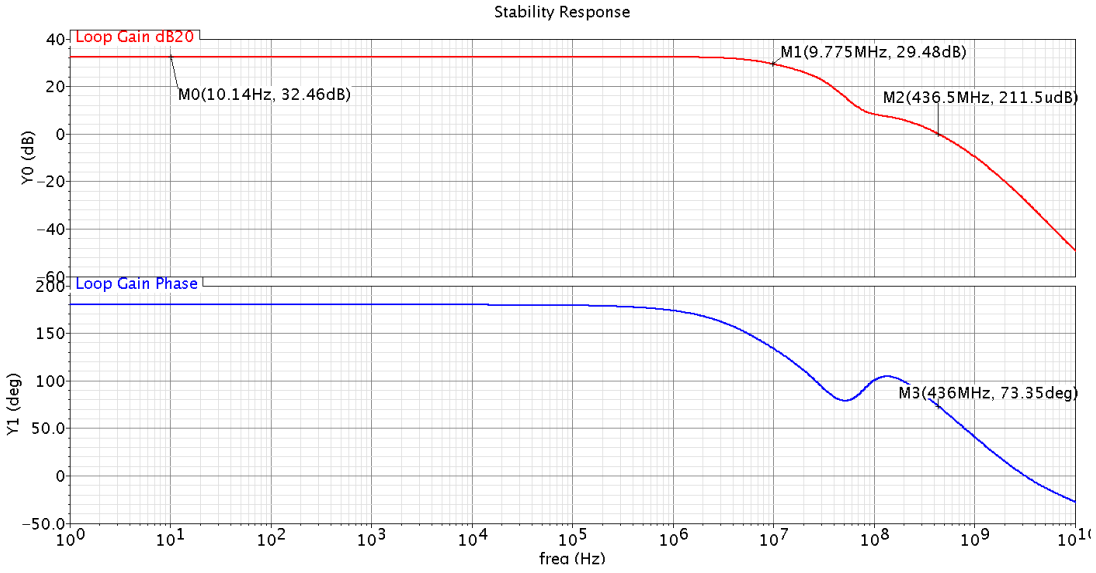

Figure 21. AC response of the CMFB loop. Av0=32.46dB, fp1=9.775 MHz, and GBW= 436 MHz.

The AC response of the CMFB loop is shown in Fig. 21. In this figure, the important aspects are bandwidth, phase margin, GBW, and its loop gain at center frequency. The phase margin of CMFB loop is 73.35 ºat GBW of 436 MHz. In addition, its loop gain at 20 MHz is 26.61 dB. The bandwidth of CMFB loop is 9.775 MHz.

The input spot noise spectral density plot for the amplifier is given in Fig. 22. The measured spot noise at 20 MHz of the amplifier is 2.585 nV/√Hz, and the calculated input integrated referred noise is 15.06 μV.

Fig. 23 displays the AC response of the loop gain of the biquad filter. This simulation is performed to ensure the phase margin of the biquad filter when the load effect is included. Measured phase margin of the loop gain of the biquad filter is 73 °.

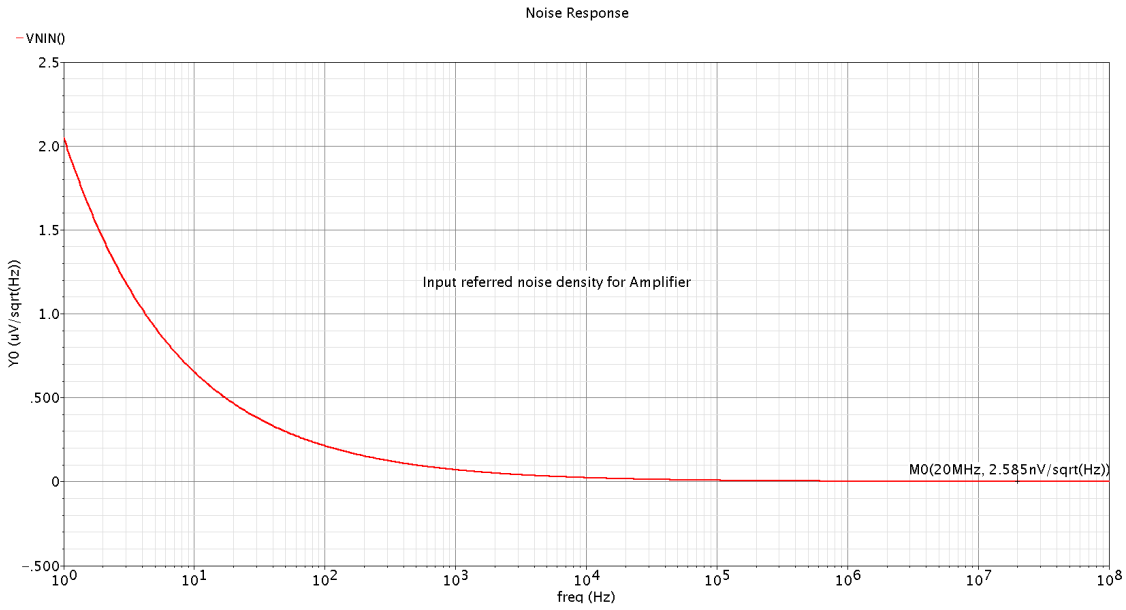

Figure 22. Input referred noise density of amplifier at 20 MHz. Spot noise at 20 MHz is 2.585 nV/√Hz.

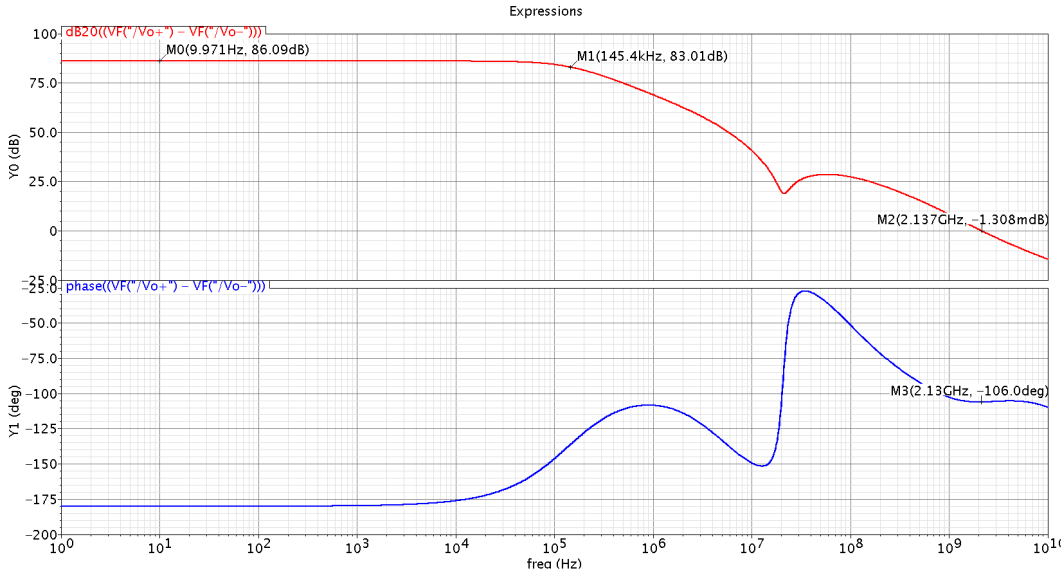

Figure 23. Loop gain of the biquad filter. Av0=86.08dB, fp1=145.4 kHz, and GBW=2.137 GHz.

The simulation result of the biquad filter is shown in Fig. 24 and Fig. 25. Two different filter responses are tested; Low-pass AC response and Band-pass AC response. The low-pass AC response shown in Fig. 17 has DC-gain of 20 dB and center frequency at 15.61 MHz. In the low-pass frequency response, Q factor can be approximated by using the equation below [19]:

$$Q = A_{peak} - A_{v0}$$

where A_{peak} is 32.1 dB and A_{vo} is 20 dB. Using the above equation, measured Q factor is 4.02. In order to obtain more accurate Q factor, band-pass frequency response is observed in Fig. 18. In the band-pass frequency response, Q factor can be expressed as:

$$Q = \frac{\omega_0}{Bandwidth}$$

where f_0 is 15.61 MHz, and bandwidth is (17.88 – 13.99) MHz = 3.89 MHz. Using the equation above, Q factor obtained in band-pass AC response is 4.012.

The spot input-referred noise density of the biquad filter is also shown in Fig. 26. At 15.61 MHz, the spot input-referred noise density is 7.056 nV/√Hz, and the integrated input-referred noise voltage is 29.268 μV.

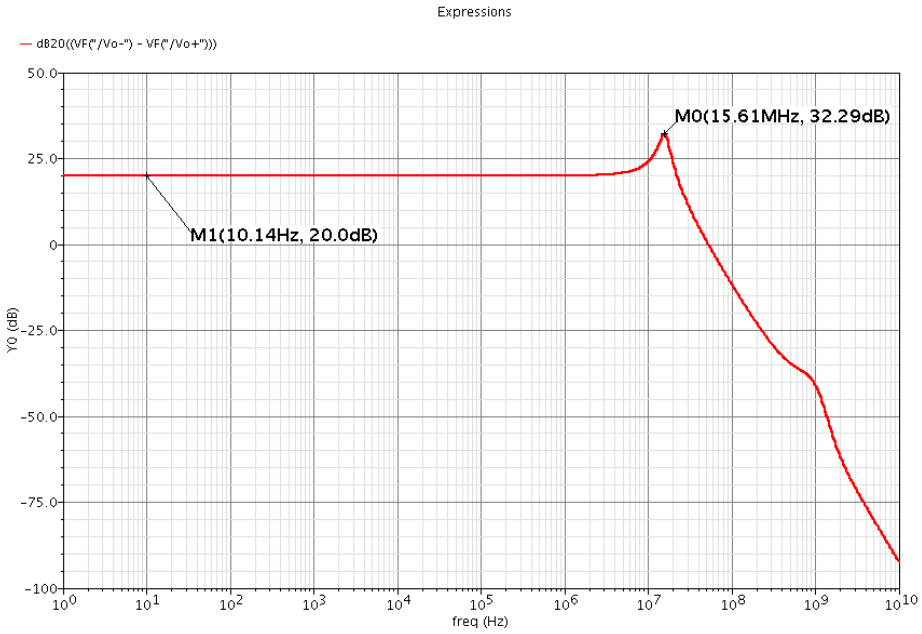

Figure 24. Low-pass AC response of the biquad filter. Av0=20dB and f_{p1}=20MHz.

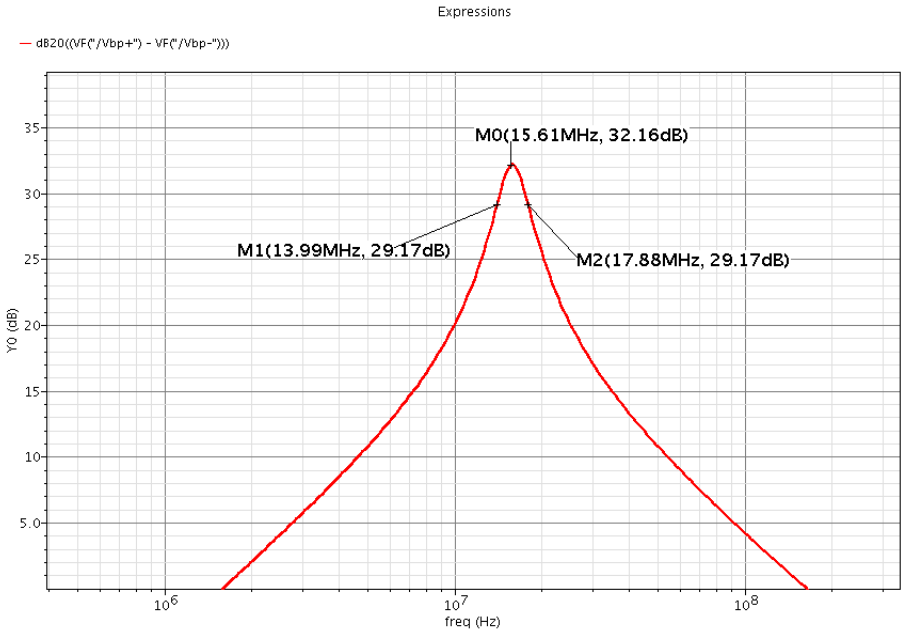

Figure 25. Band-pass AC response of the biquad filter. f_0=20MHz and Q = 4.012.

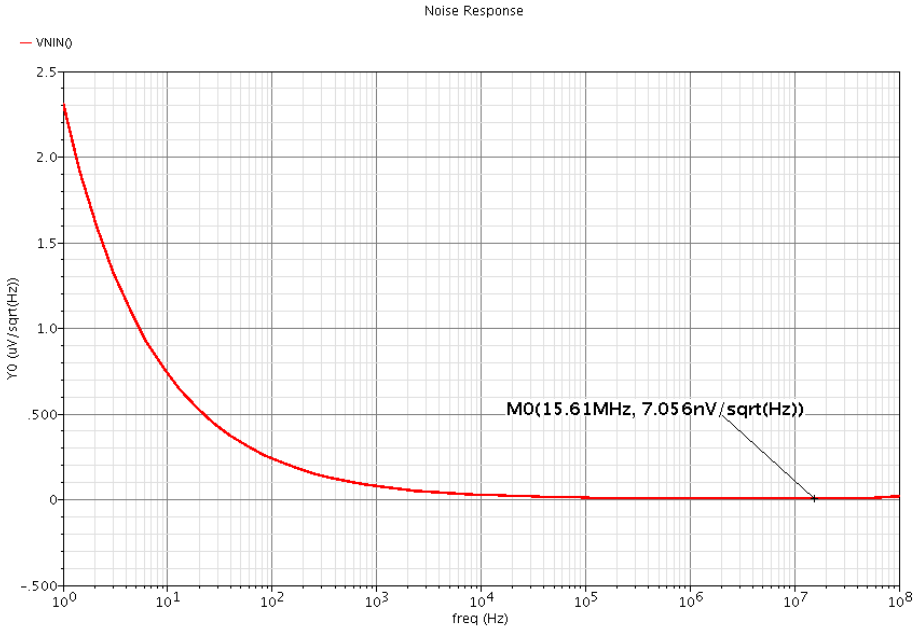

Figure 26. Input referred noise density of biquad filter. Spot noise at 20 MHz is 7.056 nV/√Hz.

The 3rd-order intermodulation distortion (IM3) is measured to ensure the linearity of the biquad filter in two different ways and shown in Fig. 27. The IM3 shown in Fig. 27 is measured by injecting two different tones located at 14 MHz and 16 MHz, with output voltage swing of ± 300 mV. The output voltage swing of ± 300 mV is reasonable in terms of the power supply of 1.8 V. The measured in-band IM3 is -85.98 dB.

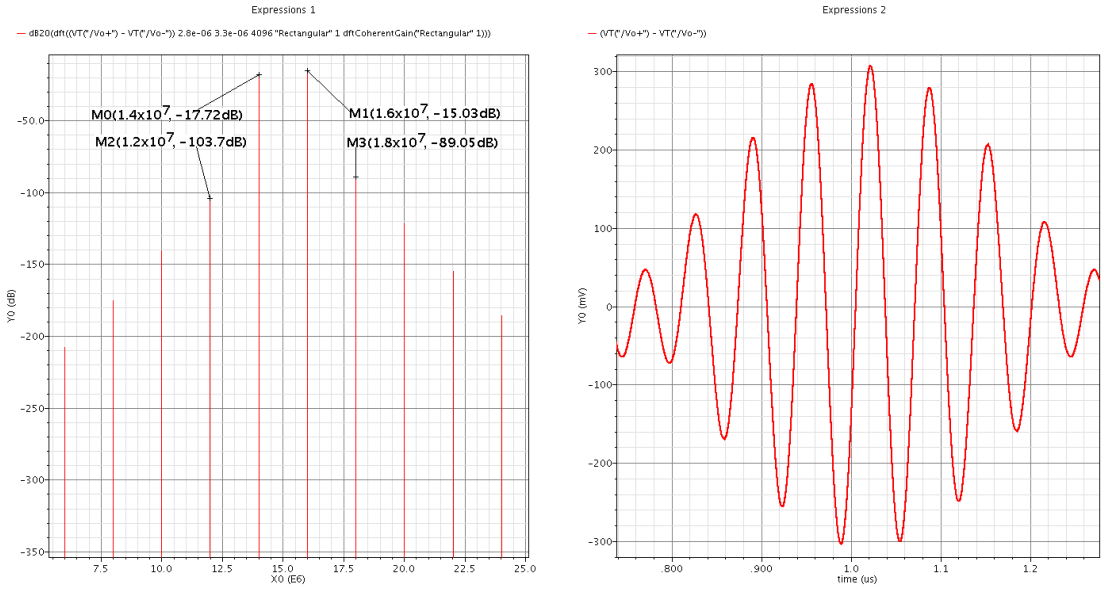

Figure 27. Measured IM3 using DFT function is -85.98 dB.

Table 7 shows the summarization of simulation results. Comparing Table 7 with Table 3, the simulation results show that all the specifications required are successfully satisfied. We can also see that power consumptions can also be further reduced with proper trade-off strategy.

Table 7. Summary of simulation results.

Objects	Simulation Results
Power supply	V_{DD} = 1.8 V, V_{SS} = 0 V
Bandwidth (f_0)	15.6 MHz
Low-frequency gain (A_{v0})	20 dB
Open-loop gain	86.08 dB
Open-loop PM	74 °
Open-loop GBW	2.3 GHz
Power consumption	8.81 mW
IM3	In-band:-85.98 dB
Q factor	4.013
Input referred integrated noise in 20 MHz	29.268 uV

Single-pole filter

The single-pole filter shown in Fig. 28 is used to realize a third stage of the filter. A simple lossy-integrator circuit is used. Values for R_1, R_2, and C are provided in Table 8.

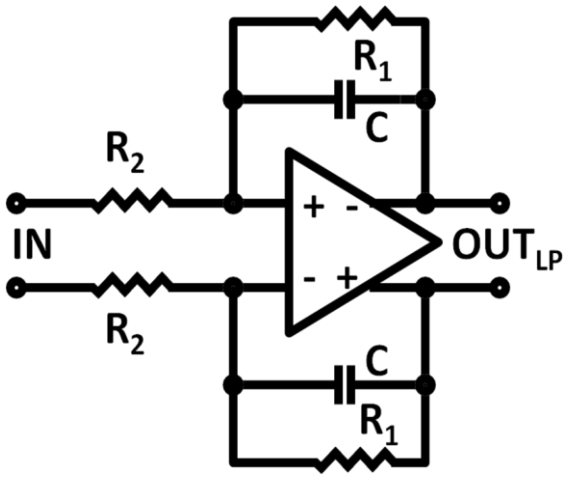

Figure 28. Macro model of a 1st-order lossy-integrator.

$$\frac{V_{out}}{V_{in}} = \frac{R_1}{R_2}\frac{1}{1+sR_1C}$$

From the above equations, the bandwidth and the gain of the circuits can be obtained as,

$$\omega_0 = \frac{1}{R_1C}$$

$$K = \frac{R_1}{R_2}$$

where K is defined as DC gain and ω_0 is defined as the bandwidth of the integrator. Therefore, the resistors R_1 and R_2, and a capacitor C is chosen to have a DC gain of 20 dB and a bandwidth of 18 MHz. Table 9 shows the simulation results of the lossy-integrator. Figs. 29, 30, and 31 display the simulation results of AC response, input referred spot noise, and IM3 of the lossy-integrator.

Table 8. Component values of lossy-integrator

Parameter	Value
R1	19.676 kΩ
R2	1 kΩ
C	1.95 pF

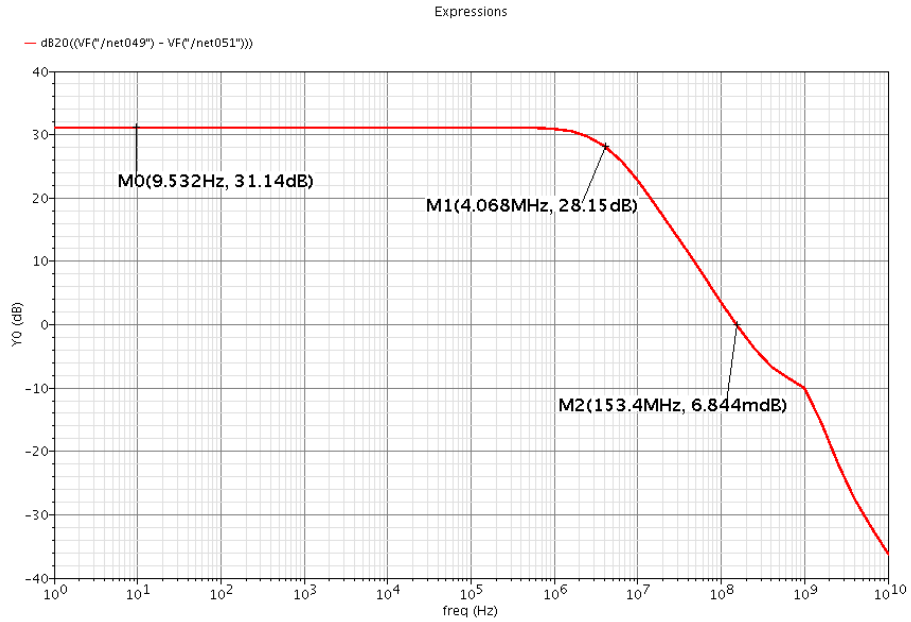

Figure 29. AC response of the lossy-integrator. A_{v0} = 31.14 dB, f_0 = 4.068 MHz, and GBW = 153.4 MHz.

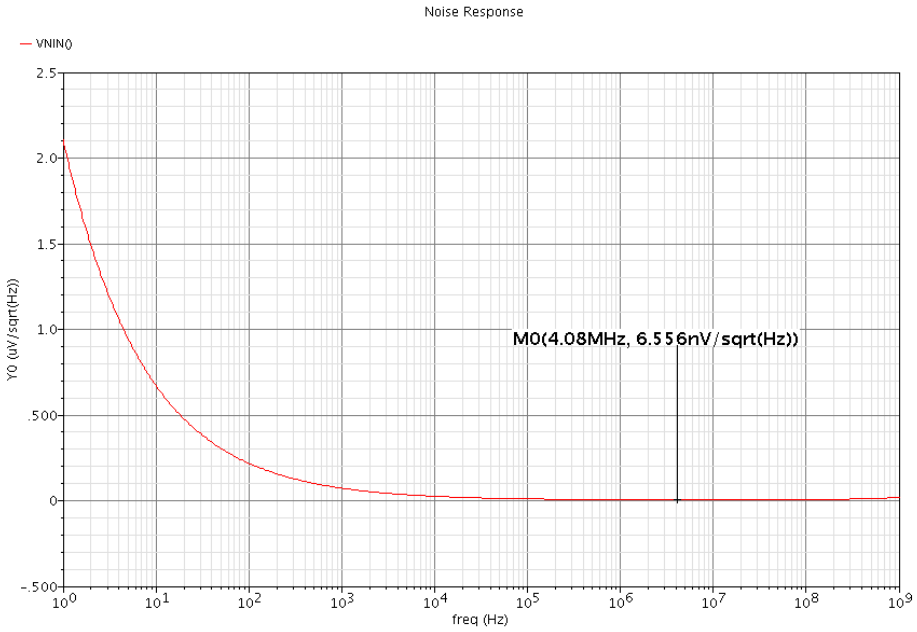

Figure 30. Input referred noise density of the lossy-integrator. Spot input-referred noise density @ 4.08 MHz is 6.56 nV/√Hz.

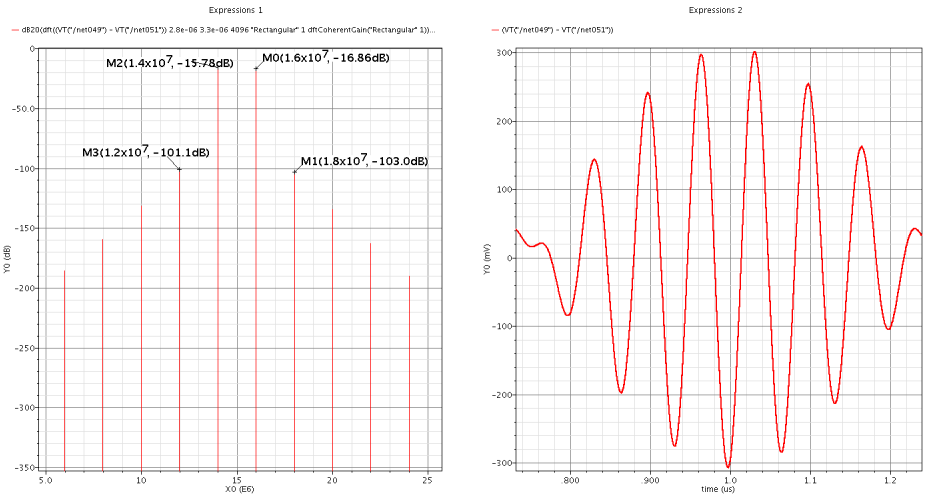

Figure 31. IM3 of the lossy-integrator is -82.91 dB.

Table 9. Summarization of the simulation results of the lossy-integrator

Objects	Simulation results
Low-frequency gain	31.14 dB
Bandwidth (f_0)	4.068 MHz
Input referred integrated noise	1.6074 μV
IM3 @ Vp-p 600 mV	82.41 dB
Power consumption	4.4 mW

Summing amplifier and 3rd-order filter with feed-forward architecture

The summing amplifier plays an important role in the feed-forward ΣΔ architecture. For the precise equivalence between discrete and continuous-time loop transfer function, it is required to maintain exactly one sampling clock delay in the direct feedback path. This issue raises stringent requirements for the design of the summing amplifier. In order to

provide exact one sampling clock delay, the speed of the summing amplifier is the most critical aspects. Hence, the main concern of the design of the summing-amplifier is a large bandwidth requirement. Since the large bandwidth is directly related to the speed, having a large bandwidth secures the high speed summing amplifier. In contrast to the filter design, noise and linearity is not a critical issue because those will be noise-shaped once the closed-loop system is achieved. Fig. 32 and Table 10 show the schematic of the amplifier for the summing amplifier and its device parameters. MB_1 is used to attenuate kick-back noise, i.e. digital glitches from the comparators that couple back to the filter. To satisfy the large bandwidth requirements, a single stage amplifier is used. The circuit for the summing amplifier is originally implemented in [1]. The configuration of the summing amplifier is shown in Fig. 33. Figs. 34 and 35 display the frequency response and IM3 simulation results of the summing amplifier. Tables 11 and 12 show the resistor values and the summarized performance of the summing amplifier, respectively.

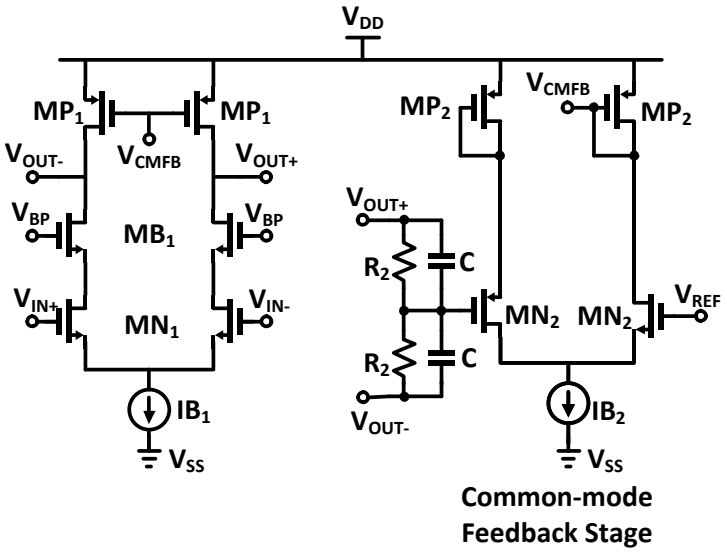

Figure 32. Schematic of op-amp for summing amplifier.

Table 10. Transistor dimentions and device values for the summing amplifier.

Device	Dimensions (μm/μm)	Device	Values
MN_1	100/0.18	R_2	80 kΩ
MB_1	96/0.2	C	100 fF
MP_1	126/0.2	IB_1	5 mA
MN_2	96/0.3	IB_2	600 μA
MP_2	126/0.2		

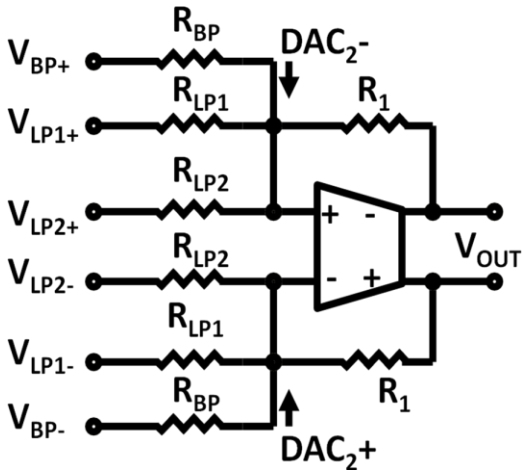

Figure 33. Macro model of a summing amplifier.

Table 11. Component values of summing amplifier stage of loop filter

Parameter	Value
R_{BP}	10.3 kΩ
R_{LP1}	5.5 kΩ
R_{LP2}	8 kΩ
R_1	10 kΩ

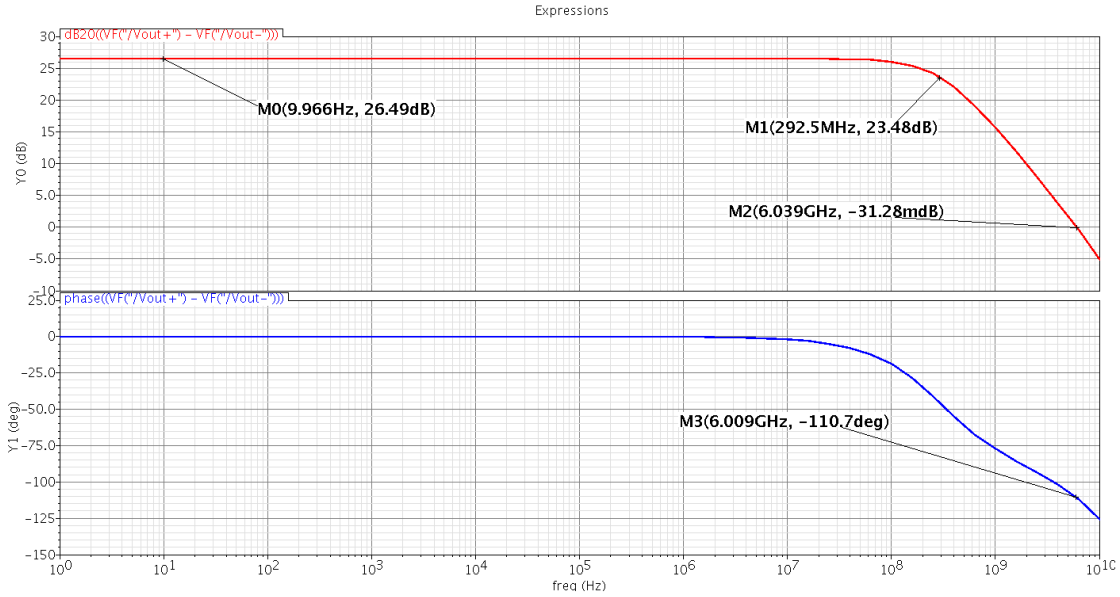

Figure 34. AC response of the summing amplifier. DC gain of 26.59 dB, GBW of 6.039 GHz, and PM of 69.3 °are observed.

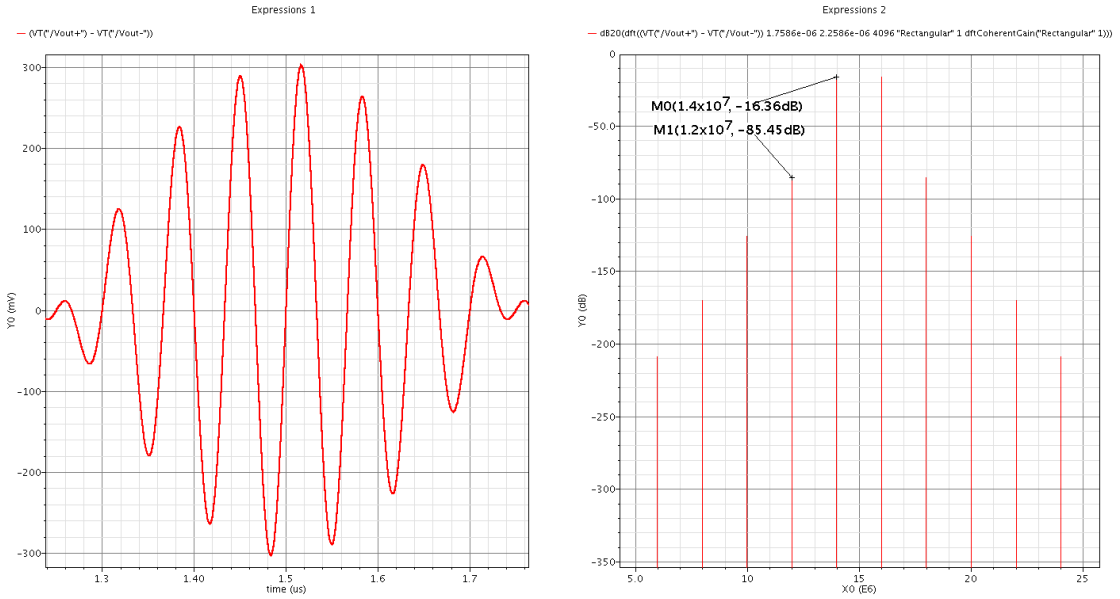

Figure 35. IM3 of the summing amplifier. IM3 of -69 dB is measured.

Table 12. Important performance parameters of the summing amplifier.

Performance parameter	Value
DC-gain	26.49 dB
Gain Bandwidth Product	6.039 GHz
Input referred integrated noise (in 20 MHz)	23.563 μV
IM3 (600 mV_{p-p})	-69 dB
Power consumption	10.008 mW

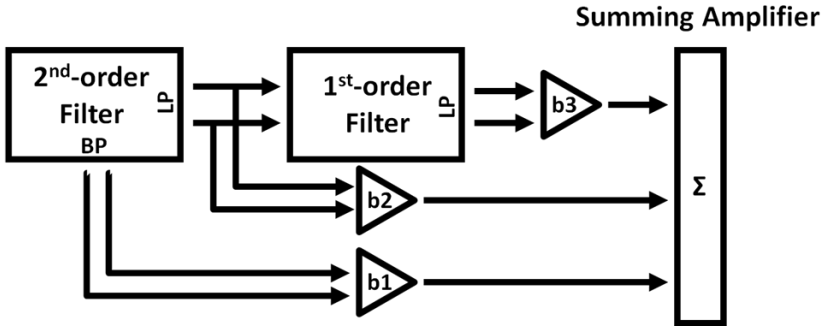

Figure 36. Feed-forward coefficient for stability of the system

Since the stability of the loop filter is defined by the summing amplifier and its feed-forward coefficients, it is significantly critical to set the proper values for each resistor in the summing amplifier. The ratio of R_{BP} to R_1, R_{LP2} to R_1, and R_{LP1} to R_1 defines the value of b1, b2, and b2 shown in Fig. 36. In order to set the values of each resistor, the coefficient values must be known. These values can be simply be calculated from Matlab with the assumption that the system works in the ideal case. From the Matlab code attached in Appendix A, the system transfer function for the filter system can be calculated simply by using d2c function.

$$H_{Filter}(s) = \frac{635084931.7407 \cdot (s^2 + 4.047 \cdot 10^8 \cdot s + 7.717 \cdot 10^{16})}{(s + 2.565 * 10^7) \cdot (s^2 + 2.453 \cdot 10^7 \cdot s + 9.625 \cdot 10^{15})}$$

Using the given specifications and simulation results from Matlab, the transfer function of the band-pass output and low-pass output of the biquad filter and lossy-integrator can be obtained.

$$H_{Biquad\_BP}(s) = \frac{s \cdot 9.81071 \cdot 10^8}{s^2 + 2.453 \cdot 10^7 \cdot s + 9.625 \cdot 10^{15}}$$

$$H_{Biquad\_LP}(s) = \frac{9.625 \cdot 10^{16}}{s^2 + 2.453 \cdot 10^7 \cdot s + 9.625 \cdot 10^{15}}$$

$$H_{Lossy\_LP}(s) = \frac{5.047 \cdot 10^8}{s + 2.565 \cdot 10^7}$$

The transfer function of the entire filter is defined by

$$H_{Filter}(s) = b_1 \cdot H_{Biquad\_BP} + b_2 \cdot H_{Biquad\_LP} + b_3 \cdot H_{Biquad\_LP} \cdot H_{Lossy\_LP}$$

After some algebra, the values of the feed-forward coefficient can be calculated.

$$b_1 = 1.164,\ b_2 = 3.193,\ b_3 = 0.8378$$

However, due to the parasitic capacitances that exist on the real circuit systems, the designer needs to adjust those values until the system becomes stable.

Figs. 37 and 38 displays the simulation results of frequency response and IM3 consisting of the biquad filter, the lossy-integrator, and the summing amplifier. After some calibration of the feed-forward coefficients, the phase margin of the entire system achieved 69.8 °. The entire filter also achieved IM3 of -69 dB.

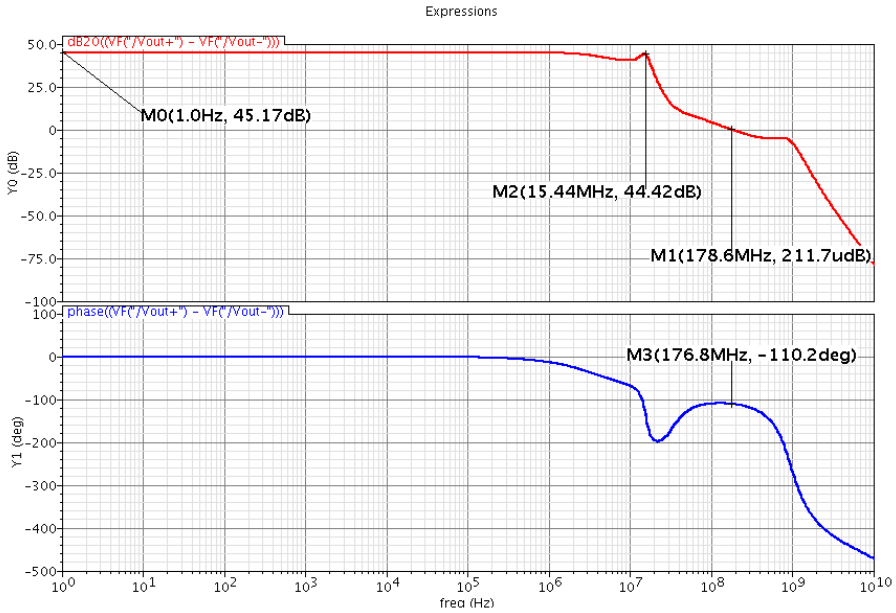

Figure 37. AC response of the 3rd-order continuous-time low-pass filter with summing amplifier. The load capacitors of 250 fF are connected in order to take account into the loading effect of the quantizer.

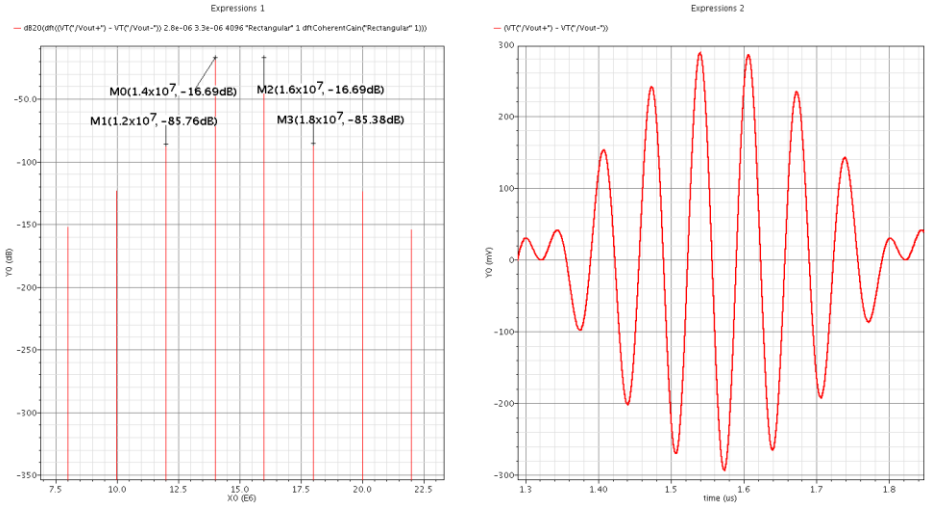

Figure 38. IM3 of the 3rd-order filter with the summing amplifier. In-band IM3 of -69 dB is achieved

3-bit flash quantizer

The 3-bit flash quantizer is composed of comparator cores, latches, and D flip-flops. Sample-and-hold block portrayed in the system level simulation does the same function as the comparator cores in a flash type quantizer. Eight resistors are connected in a series in order to generate seven reference voltage levels. Since the system has a power supply voltage of 1.8 V, we assume that the linear region of the system would be from 0.6 V to 1.2 V, which is a ±300 mV full-scale output voltage swing. Therefore, the MSB size is set to 600 mV, and the LSB size is determined by MSB/7, which is 85.714 mV.

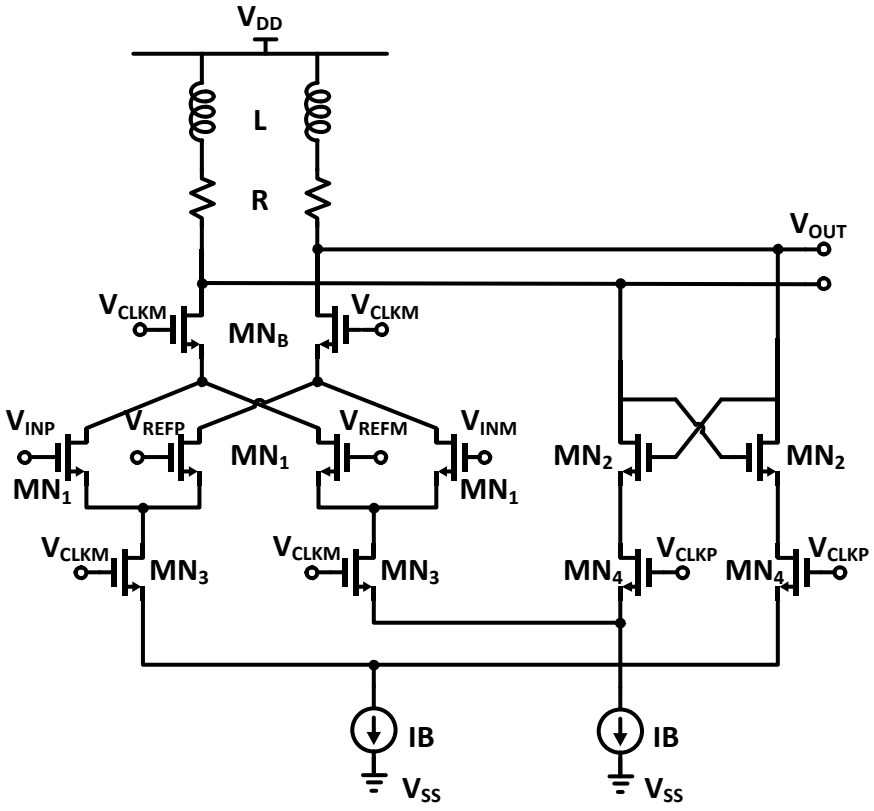

Figure 39. Comparator core [22].

Table 13. Dimension of the transistors and bias conditions for the comparator core.

Device	Dimensions (μm/μm)	Device	Dimensions
MN_1	10/0.18	IB	450 μA
MN_2	6/0.18	R	500 Ω
MN_3	4/0.18	L	11.88 nH
MN_4	4/0.18		
MN_B	6/0.18		

Fig. 39 shows the transistor level design of the comparator core, and Table 13 displays the transistor dimensions and device values for each comparator core. The comparator core has the following two different functions: pre-amplifier and latch. The differential output V_{OUT} of the comparator core is decided based on the voltage difference between V_{IN} and V_{REF}. The next two figures, Figs. 40 and 41, illustrate how the comparator core operates. At the rising edge of the V_{CLKM}, the comparator core is operating in tracking mode. During this mode, the latch circuit, which is MN_2, is disabled. Simultaneously, the pre-amplifier circuitry (MN_1) is enabled, and then it tracks the voltage difference between input and reference. At the rising edge of V_{CLKP}, the comparator core is operating in regenerative mode. During the regenerative mode, the latch circuit is enabled while the pre-amplifier circuit is disabled, thus it holds the data until the next track mode. Since the latch circuit generates a positive feedback, the comparator core during the regenerative mode makes the latch to operate in the saturation region shown in Fig. 42.

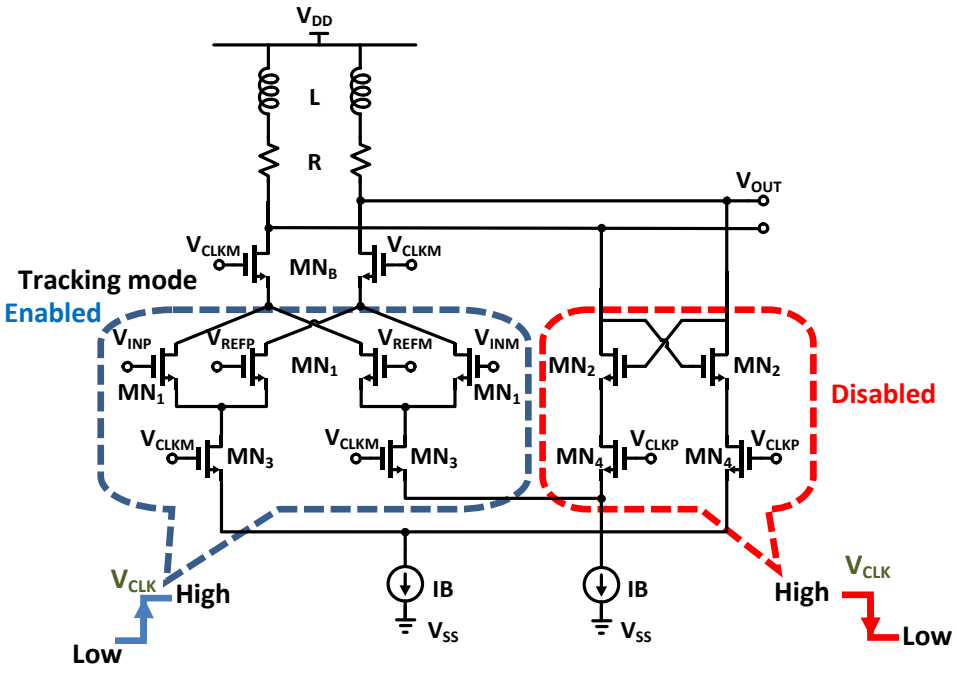

Figure 40. Tracking mode of the comparator core.

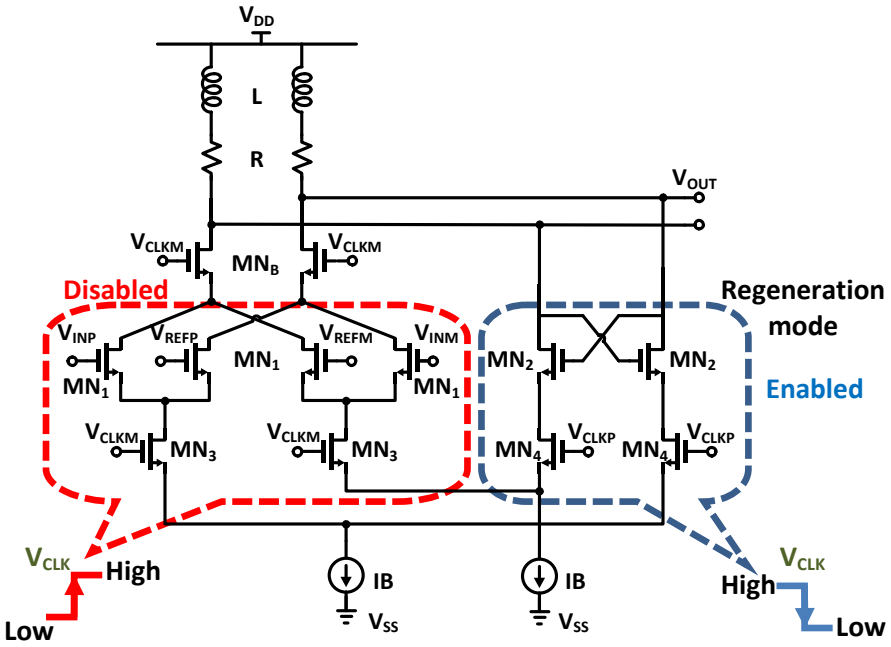

Figure 41. Regeneration mode of the comparator core

The cascode devices, which are MN_B, are used to reduce the parasitic capacitances and kick-back noise. This cascode structure in the comparator is originally used in [22]. By having less parasitic capacitances, the comparator has a larger bandwidth during the tracking mode and constant smaller regenerative mode time during the regenerative mode. The regeneration mode time and the tracking mode time can be reduced by placing inductors in a series with resistors in the comparator core, thereby the maximum sampling speed increases for a given power consumption [22]. Furthermore, each differential inductor has a parasitic resistance. In our case, it is 408 Ω.

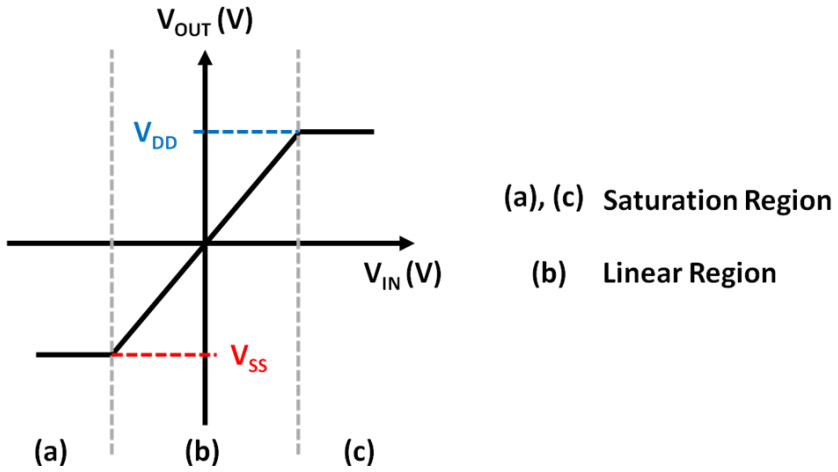

Figure 42. Plot of V_{in} vs V_{out}. The plot shows where the saturation and linear regions are located.

The comparator core, however, needs another supportive circuit to generate rail-to-rail signals. Therefore, an additional SR latch device is added next to the comparator core [23]. The schematic of the second latch is shown in Fig. 43. The detailed operation of the SR latch is portrayed in Fig. 44. The transistor dimensions and device values are presented in Table 14.

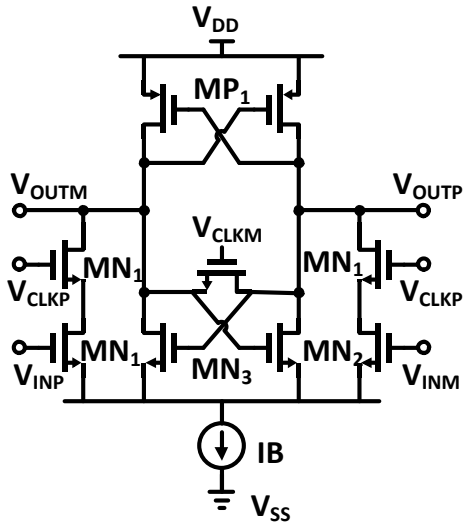

Figure 43. Latch [23].

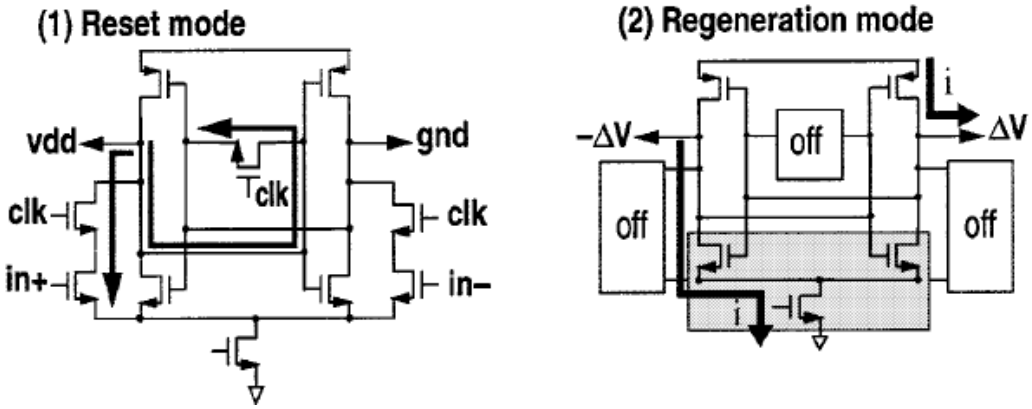

Figure 44. Detailed operation of the SR latch [23].

Table 14. Transistor dimensions and device values for the latch circuit

Device	Dimensions (μm)	Device	Values
MN_1	2/0.18	IB	450 μA
MP_1	2/0.18		
MN_2	3/0.18		
MN_3	2/0.18		

As it is mentioned above, the second latch circuit shown in Fig. 43 is used to generate rail-to-rail output to the digital part of the quantizer. The output of the comparator is evaluated when the V_{CLKM} is on, so that the output of the latch can either be V_{DD} or V_{SS}. While V_{CLKP} is on, the output voltage is forced to be zero as the transistor MN_1 is turned on.

The Fig. 45 illustrates the configuration of the 3-bit flash quantizer. The comparator cores and latches have fully-differential input and output ports. The comparator core simply compares the input and reference voltages, and the latch circuit takes the output of the comparator, and generates rail-to-rail output. The D type of flip-flop stores the output of the comparator-latch circuits, and digitizes them by the clock signal. Fig. 46 exhibits the output of each system block in the 3-bit flash quantizer. The output of D-FF is delayed by Ts/2 with respect to the input signal. Fig. 47 shows the comparison between continuous-time input signal and discrete-time output signal of the quantizer.

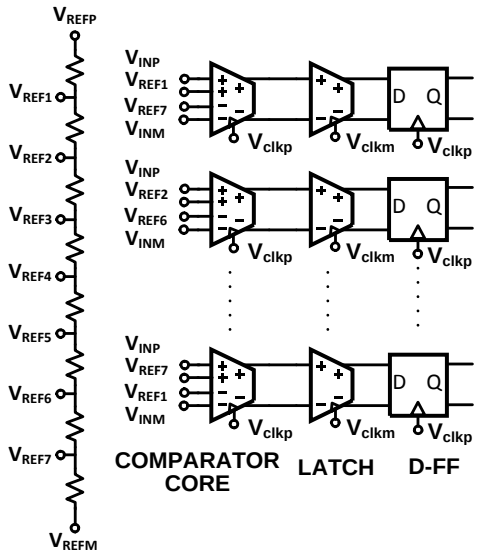

Figure 45. Configuration of the 3-bit flash quantizer.

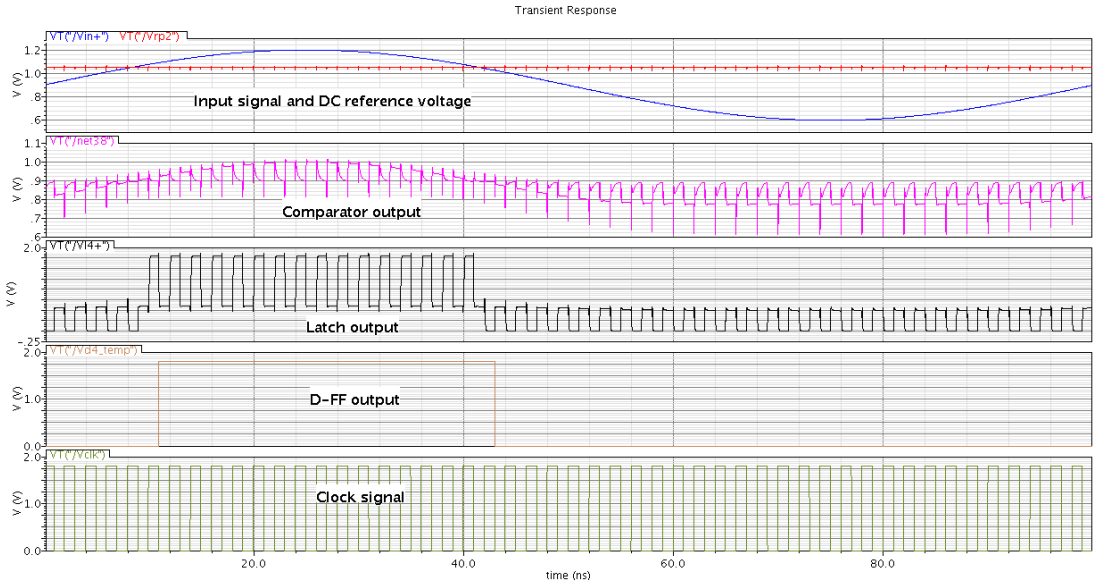

Figure 46. Transient simulation of the 3-bit flash quantizer.

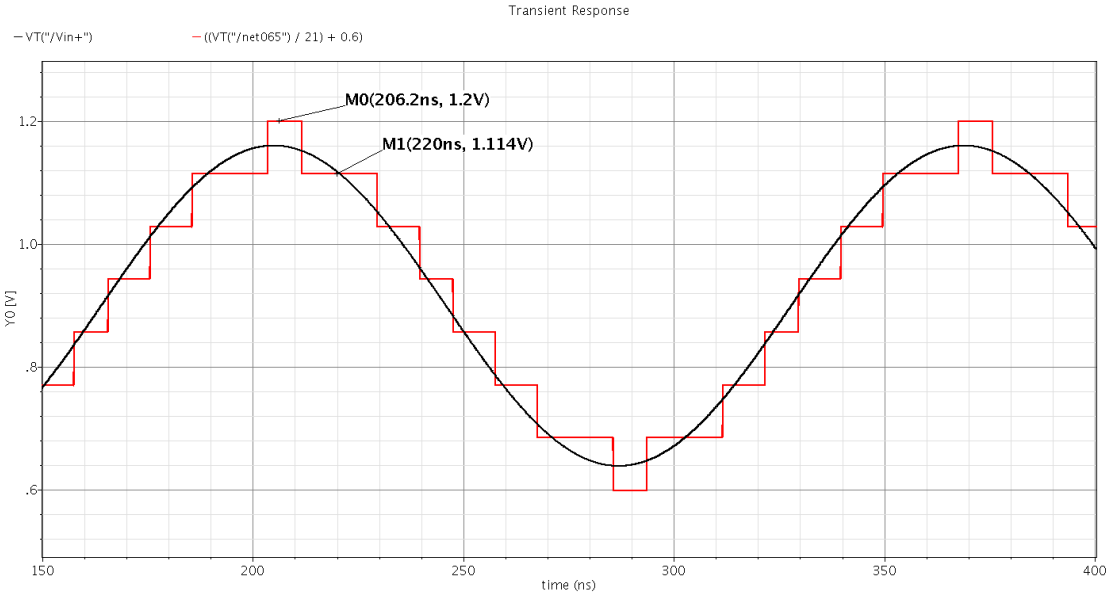

Figure 47. Input and output of the 3-bit flash quantizer. LSB is set to 85.714 mV and MSB is set to 600 mV. Black line indicates continuous-time input signal, and red line indicates discrete-time output signal.

Current steering digital-to-analog converter

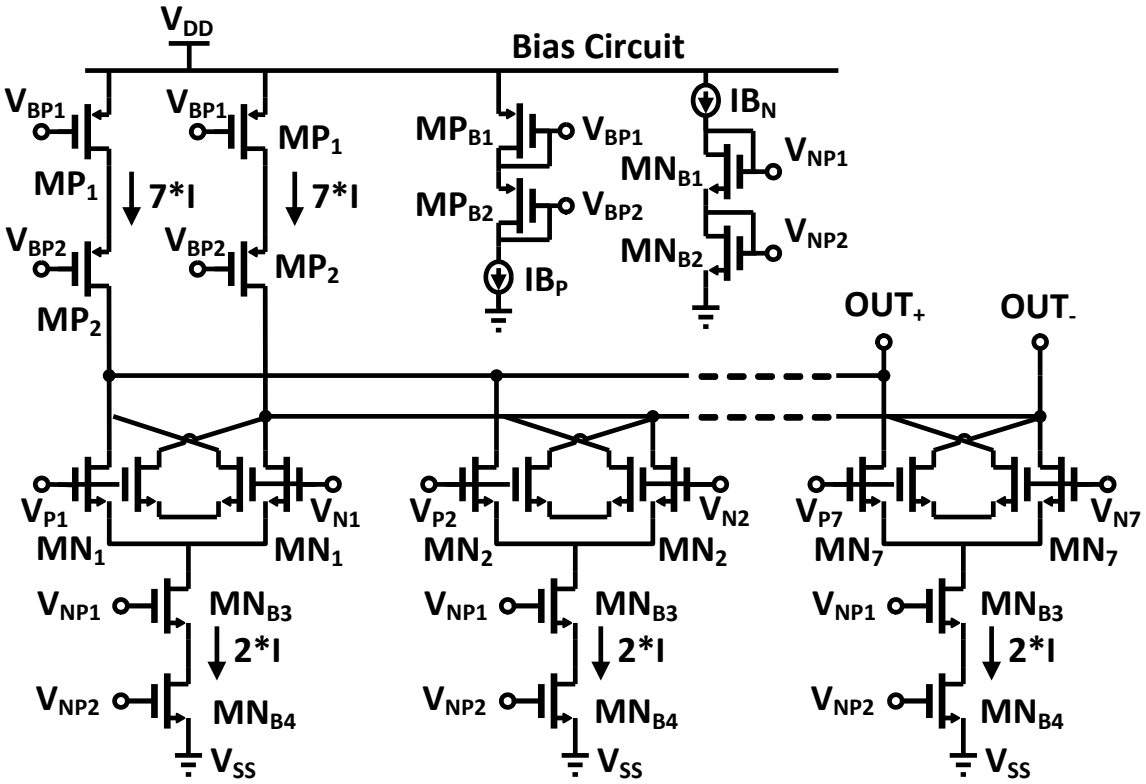

Figure 48. Schematic of current-steering DAC (7 cells).

Table 15. Transistor dimentions and device values for the main DAC.

Device	Dimension (µm/µm)	Device	Dimension (µm/µm)	Device	Values
MP_1	110/0.8	MP_{B1}	110/0.8	IB_P	300.6 µA
MP_2	20/0.3	MP_{B2}	25/0.3	IB_N	86.9 µA
MN_1	0.5/0.18	MN_{B1}	5/0.3		
MN_{B3}	1/0.2	MN_{B2}	13/1.2		
MN_{B4}	13/1.2				

Table 16. Transistor dimentions and device values for fast-path DAC

Device	Dimension (μm/μm)	Device	Dimension (μm/μm)	Device	Values
MP_1	30/1.8	MP_{B1}	30/1.8	IB_P	52.7 μA
MP_2	4/0.3	MP_{B2}	10/0.3	IB_N	15.06 μA
MN_1	0.5/0.18	MN_{B1}	45/1.5		
MN_{B3}	2/1.5	MN_{B2}	11/5		
MN_{B4}	11/5				

Fig. 48 displays the schematic of seven cells of current-steering DAC. Tables 15 and 16 show the device parameters for the main DAC and the fast-path DAC, respectively. The current-steering DAC is commonly used in ΣΔ modulators because of its less complexity and power consumption. The current flowing through MP1 and MP2 can be calculated by the equation below.

$$I_{MP1,2} = \textit{(peak value of the voltage output swing) / (}R_{IN}\textit{ of the biquad filter)}$$

In the case of our design, the equation would be

$$I_{MP1,2} = (300\ mV_{pk}) / (1\ k\Omega) = 300\ \mu A$$

$$I_{MNB_{1,2}} = \frac{I_{MP1,2} \cdot 2}{7} = 85.714 \mu A$$

The cascode current mirror is used to provide stable current of 300 μA to MP_1 and MP_2. Another cascode current mirror is used for NMOS transistors, which are MN_{B3} and MN_{B4}. Since the output swing is not in our design concern, the cascode structure is a good approach to provide a stable current to transistors. High V_{DSAT} for each transistor is required in order to generate fast current transitions.

Two different DACs using the same architecture are used in this work: One for the main feedback path, and another for the fast-path feedback. Since maximum sampling rate of a ΣΔ ADC is limited by the quantizer delay, which is also denoted as excess loop delay (ELD), the most conventional compensation technique is using a fast-path DAC with less than an one clock cycle delay [24]. To make modulators less sensitive to process variation, most ΣΔ ADCs compensate for only half a clock cycle of ELD. From the Matlab simulation attached in Appendix A, the gain of the fast-path DAC, denoted as 'k', is chosen to be 1.7594. The current driving the fast-path DAC can be calculated as

$I_{MP1,2}$ = *(peak value of the voltage output swing) k / (R_1 of the summing amplifier)*

$$= \frac{300mV \cdot 1.7594}{10k\Omega} = 52.782\mu A$$

$$I_{MNB_{1,2}} = \frac{I_{MP1,2} \cdot 2}{7} = 15.081\mu A$$

Fig. 49 displays the effect of noise cancellation. The noise cancellation works by adding and cross-coupling extra NMOS transistors. The gates of these extra transistors are connected to the input, but their drains are connected to the other side (cross-coupling). The sources of these transistors should be floating. The glitch arises at the transition of input voltage. This is because the C_{gd} of the input transistors store charge from the input voltage, and when the voltage transition rises, these parasitic capacitances release their stored charge, thus this extra charge generates undesired additional current. Therefore, by adding these extra transistors, the cross-coupled C_{gd} of these extra transistors can simply cancel the effect of the C_{gd} of the input transistors.

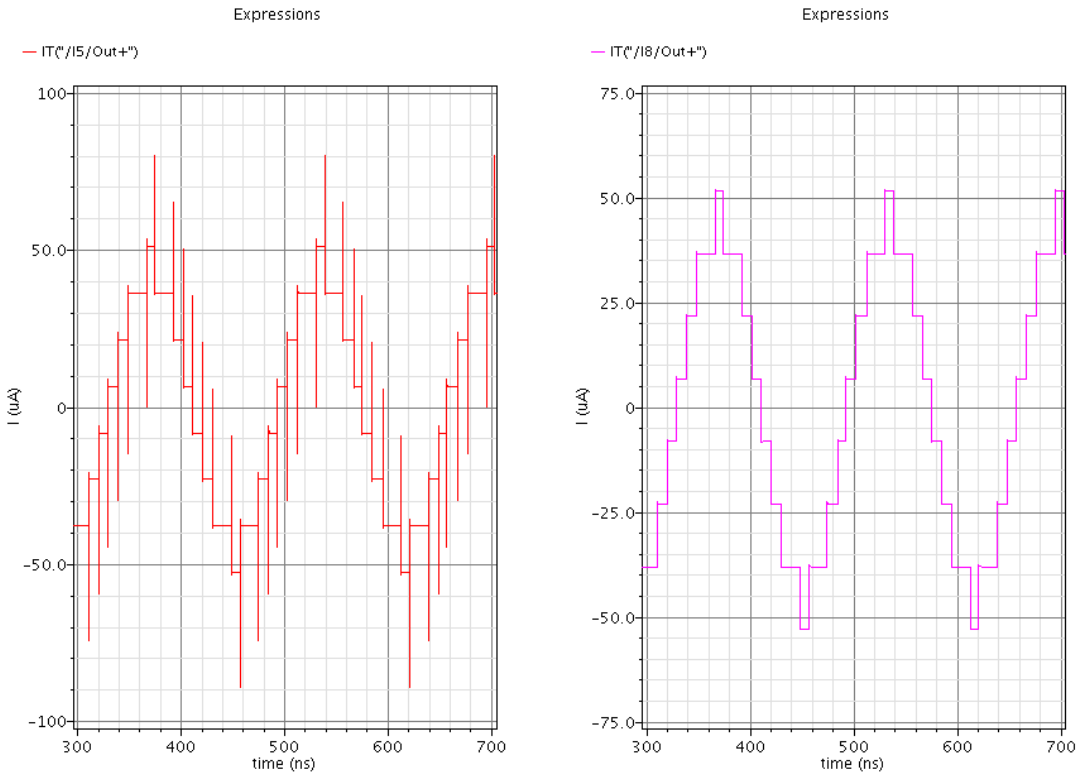

Figure 49. Noise Cancellation of the fast-path DAC

Closed-loop sigma-delta analog-to-digital converter

Once the loop is closed, numerous effects arise that the designer did not expect in the open-loop system. The most critical effect of the closed-loop system is the input impedance of the quantizer. Especially in a flash quantizer, due to the large number of comparators, the input parasitic capacitance of the flash quantizer significantly degrades the stability of the system.

Fig. 50 shows the output of the closed-loop ΣΔ ADC. The left figure of Fig. 50 displays the analog input signal, and the figure on the right hand side shows the converted discrete-time output signal. The digitized output signal contains 7 different levels.

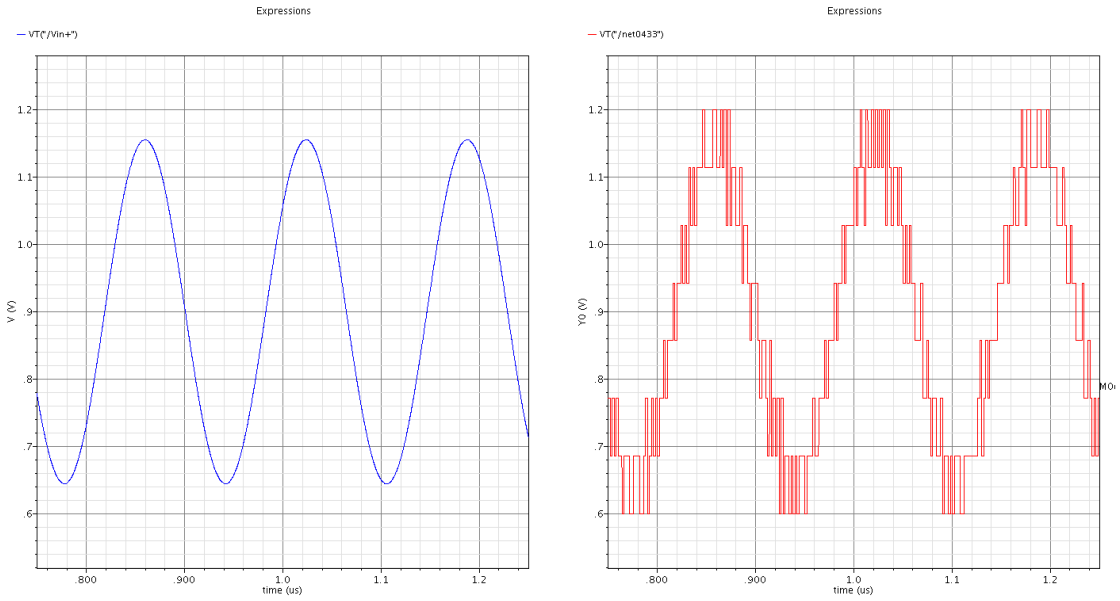

Figure 50. ΣΔ-ADC output. Left: continuous-time input signal. Right: discrete-time output signal.

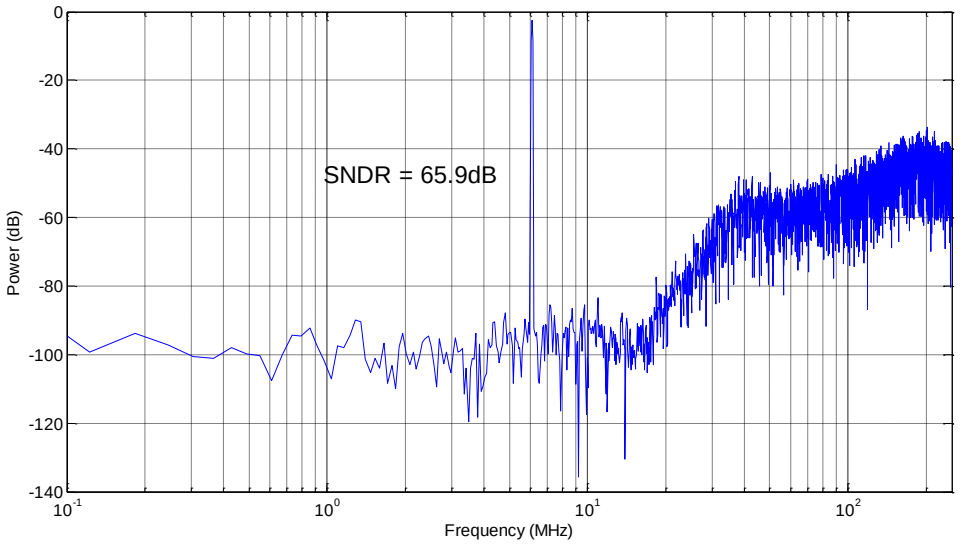

Figure 51. Measured output spectrum of the modulator. The peak SNDR of the system is 65.9 dB.

Table 17 summarizes the measured results of the proposed 3rd-order CT LP ΣΔ ADC in this work. The system uses clock frequency of 500 MHz, and the overall system is

designed to achieve a bandwidth of 20 MHz to accommodate WiMAX and other wideband applications. As shown in Fig. 51, the measured peak SNDR of this work is 65.9 dB. Due to the nature characteristics of a flash quantizer, the 3-bit quantizer used in this work consumes the most of power. After the circuits are properly biased, the 3rd-order low-pass filter with a summing amplifier consumes 22.3 mW. The quantizer consumes 8.16 mW. The main and fast-path DACs consume 1.08 mW and 0.19 mW, respectively. Hence, the total power consumption is 31.735 mW. In ΣΔ modulators, the figure-of-merit (FoM) is generally used to measure the overall performance of the system. The FoM is expressed as

$$FoM = \frac{Power}{2^{ENOB} \cdot (2 \cdot Bandwidth)} = 487 \text{ in fJ/bit}$$

Table 17. Summarization of the proposed 3rd-order CT LP ΣΔ ADC.

Parameter	Value
Power supply	1.8 V
Clock frequency	500 MHz
Bandwidth	20 MHz
Peak SNDR	65.9 dB
Dynamic range	59 dB
IM3 (600 mV_{p-p})	< -69 dB
Power consumption	31.735 mW

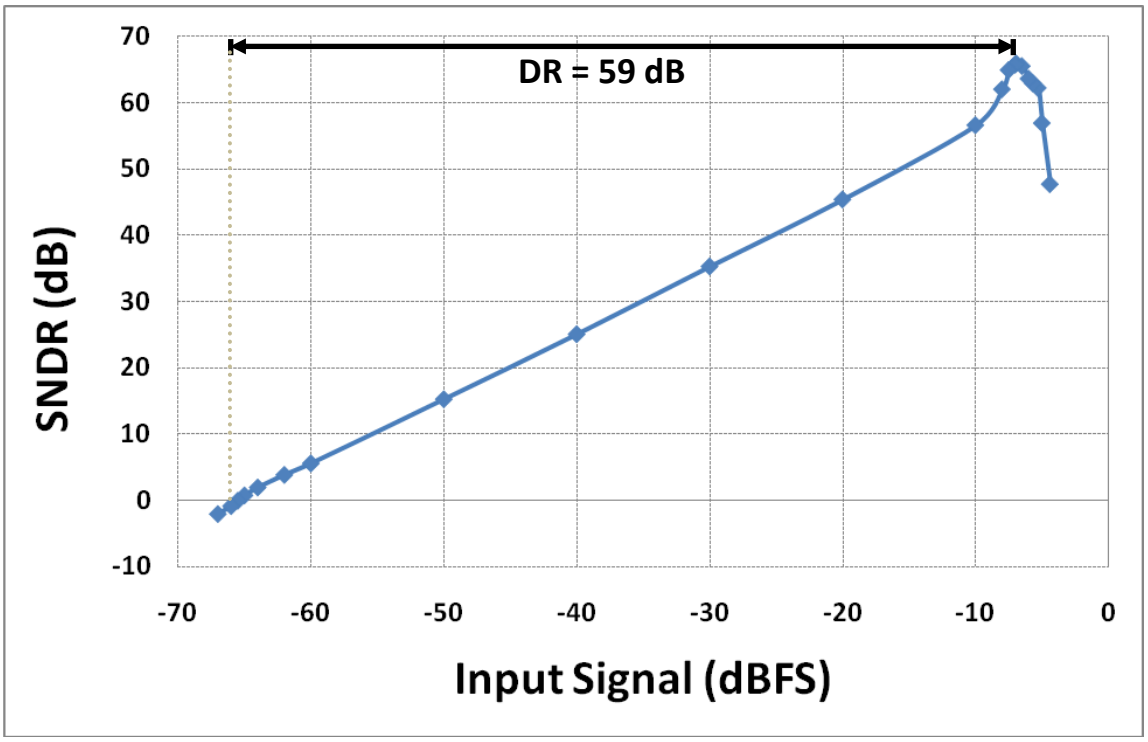

Figure 52. Measured SNDR versus input signal power. A dynamic range of 59 dB is achieved.

The measured SNDR for different input signal powers are plotted in Fig. 52, in which the 59 dB dynamic range (DR) is annotated. From the figure, the peak SNDR of the system is 65.9 dB with -7 dBFS input power. Overall, the simulation results covered in this section are nearly matched with the Matlab simulation shown in Fig. 13.

CHAPTER IV

SUMMARY AND CONCLUSIONS

Summary

In this work, the design of a 3rd-order continuous-time low-pass Sigma-Delta (ΣΔ) Analog-to-Digital Converter (ADC) is presented. The entire system was implemented using TSMC 0.18 μm CMOS technology. Throughout the paper, the system level design was analyzed by using Matlab, and the transistor level design was simulated using Cadence. A 3rd-order continuous-time low-pass filter with a 20 MHz bandwidth was designed by using an active-RC topology, and achieved specifications given by Matlab system simulations. Feed-forward architecture was used as a compensator to take advantage of its high linearity. A 3-bit quantizer was employed to achieve fast data conversion. However, a flash type quantizer has large power consumption due to its large number of comparators. A current-steering DAC was also used to directly inject feedback signal without additional circuitries. Two different DACs were designed to provide fast-path feedback signal and main feedback signal. Noise cancellation technique was also employed in the fast-path DAC design. After each system block was analyzed, the entire closed-loop system was simulated. The measured peak SNDR of the proposed system with 20 MHz bandwidth was 65.9 dB. The system consumes power of 31.735 mW from a 1.8 V supply. 22.3 mW of power is dissipated in the 3rd-order filter including the summing amplifier, 8.16 mW in the quantizer, and 1.08 mW and 0.19 mW in the main DAC and fast-path DAC, respectively.

Performance comparison

Table 18. A performance comparison by bandwidth (≥ 20 MHz).

Ref	Type of ΣΔ ADC	Fs (MHz)	**BW (MHz)**	SNDR (dB)	P(mW)	Technology	FOM (fJ/bit)
[3]	5th CT 3bit LP	400	**25**	67.7	48	0.18 µm CMOS	484
[5]	5th CT 4bit LP	400	**25/20**	52/56	18	0.18 µm CMOS	873
[6]	3rd CT 4-bit LP	640	**20**	63.9	58	0.13 µm CMOS	1132
[7]	2nd CT 2-bit LP	640	**20**	51.4	6	0.13 µm CMOS	494
[8]	3rd CT 4bit LP	640	**20**	74	20	0.13 µm CMOS	122
[9]	3rd CT N-bit	250	**20**	60	10.5	65 nm CMOS	321
[11]	4th CT VCO (N-bit)	900	**20**	78	87	0.13 µm CMOS	335
[12]	2nd CT VCO (5-bit)	1000	**20**	67	40	0.13 µm CMOS	546
[13]	3rd CT 4-bit LP	200	**20**	49	103	0.18 µm CMOS	11182
This work	3rd CT 3-bit LP	500	**20**	65.9	31.735	0.18 µm CMOS	487

Table 19. A performance comparison by a type of filters (3rd-order filter)

Ref	**Type of ΣΔ ADC**	Fs (MHz)	BW (MHz)	SNDR (dB)	P(mW)	Technology	FoM (fJ/bit)
[4]	**3rd CT 1bit LP**	640	10	66	7.5	0.18 µm CMOS	230
[6]	**3rd CT 4-bit LP**	640	20	63.9	58	0.13 µm CMOS	1132
[8]	**3rd CT 4bit LP**	640	20	74	20	0.13 µm CMOS	122
[9]	**3rd CT N-bit**	250	20	60	10.5	65 nm CMOS	321
[10]	**3rd DT 3.5-bit**	400	20	70	34	0.13 µm CMOS	329
[13]	**3rd CT 4-bit LP**	200	20	49	103	0.18 µm CMOS	11182
This work	**3rd CT 3-bit LP**	500	20	65.9	31.735	0.18 µm CMOS	487

Table 20. A performance comparison by technology (0.18 μm CMOS)

Ref	Type of ΣΔ ADC	Fs (MHz)	BW (MHz)	SNDR (dB)	P(mW)	**Technology**	FoM (fJ/bit)
[3]	5th CT 3bit LP	400	25	67.7	48	**0.18 μm CMOS**	484
[4]	3rd CT 1bit LP	640	10	66	7.5	**0.18 μm CMOS**	229
[5]	5th CT 4bit LP	400	25/20	52/56	18	**0.18 μm CMOS**	872
[13]	3rd CT 4-bit LP	200	20	49	103	**0.18 μm CMOS**	11182
This work	3rd CT 3-bit LP	500	20	65.9	31.735	**0.18 μm CMOS**	487

Tables 18, 19, and 20 show the performance comparison by bandwidth, filter type, and technology, respectively. The overall performance of the systems was measured based on the value of FoM, which was a function of power consumption, bandwidth, and effective number of bits. Smaller values of FoM indicate a better overall system performance. First of all, compared by bandwidth, the proposed system was ranked fifth in the list. To analyze in a more accurate way, the system was compared by other 3rd order filters, and was ranked fifth again. Comparison by technology is also taken to check if the system performs properly on 0.18 μm CMOS technology. By looking at the comparison in Table 20, the proposed system is ranked third, which indicates the decent performance among other competitors. Overall, although the proposed work is not showing the best performance, considering the situation that the proposed system is constructed only by one person, it can be seen that the system is highly competitive.

Conclusion

The proposed 3rd-order continuous-time low-pass ΣΔ analog-to-digital converter is successfully implemented in this work. Since this work was not fabricated, it was quite

hard to compare the exact performance of this and other works, but Cadence simulation is frequently considered sufficient to be compared. Compared by previously published work shown in Table 1, the performance of the proposed system is highly competitive. This work achieved relatively low power consumption while the bandwidth and the measured SNDR peak show sufficiently high performance. Moreover, among the group using 0.18 μm technology, the proposed work especially show the highly competitive results with respect to bandwidth and power consumption. Not many innovative techniques are used, but the combination of numerous techniques for reduction of complexity and power are implemented in the design of the system.

Future work

Since the optimization of the filter system has not been started yet, there are high possibilities that the optimization can further reduce the power consumption and increase a peak SNDR. Changing the type of quantizer can also increase the performance of SNDR and power consumption, but since a new design of quantizer would take a considerable amount of time, it is less expected. In addition, some techniques would have to be added in order to reduce the clock jitter sensitivity further.

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APPENDIX A

MATLAB SIMULATION CODE

```
clear
clc
set(cstprefs.tbxprefs,'FrequencyUnits','Hz')

Fbw = 20e6;
OSR = 12.5;
order = 3;
nlev = 7;    %   3-bit
OBG = 2.8;   %   out-of-band gain
Tone = 97;

Fsamp = 2*OSR*Fbw;

% %% Schreier's synthesis function
ntf1 = synthesizeNTF(order,OSR,1,OBG);
ntf_ideal = ntf1

%   Get the zero
[ntf_magn ntf_phase ntf_w] = bode(ntf1);
[ntf_zero_mag ntf_zero_ix] = sort(ntf_magn);
ntf_zero_freq1 = ntf_w(ntf_zero_ix(1));
            %ntf_zero_ix(1) holds the minimum value of mag
            %ntf_zero_freq1 holds the index of that min mag

beta1 = ntf_zero_freq1;     % freq of conjucate zeros

q_biquad1 = 4;
[b1,a1] = tfdata(ntf1,'v'); %numerator data -> b1
                            %denomenator data -> a1

alpha1 = -beta1/sqrt(4*q_biquad1^2-1);
r1 = exp(alpha1);
b1 = conv([1 -0.95],[1 -2*r1*cos(beta1) r1^2]);

ntf1 = filt(b1,a1,1);    %digital filter H(z^-1)=b1(z^-1)./(a1(z^-1)
                         %with sampling time 1
ntf1 = zpk(ntf1);
ntf_finiteQ = ntf1

ntf_mag = bode(ntf1,pi);
figure;
grid on
subplot(2,1,1)
bodemag(ntf1)
s = sprintf('Max NTF gain = %4.3f \n',ntf_mag);
text(0.15,-50,s);
```

```
N = 8192; % No of points in the FFT
fB = ceil(N/(2*OSR)); % Signal bandwidth
% Input tone
f = 29;

amp1 = [-80:5:-15 -12 -10:1:-6 -5:.5:0];

% Code to obtain SNR at various amplitudes
npoints = length(amp1);
snr1 = zeros(1,npoints);
maxsnr = snr1(1);
inp_maxsnr = amp1(1);
stability = 1;

for i=1:npoints
   ampl = 10^(amp1(i)/20);
%    ampl = 10^(-3.5/20);
   u = ampl*(nlev-1)*sin(2*pi*f/N*[0:N-1]);
   v = simulateDSM(u,ntf1,nlev);
   spec = fft(v.*ds_hann(N))/(N/4);
   snr1(i) = calculateSNR(spec(1:fB),f);
   if isinf(snr1(i))
       maxsnr = 0;
       snr1(i) = 0;
       inp_maxsnr = amp1(i);
       maxstabin = 0;
   else
       if snr1(i) > maxsnr
           maxsnr = snr1(i);
           inp_maxsnr = amp1(i);
       end
   end
   if (i>3)
   if (snr1(i)<(snr1(i-1)))&&(snr1(i-1)<(snr1(i-
2)))&&(stability==1)&&(i>12)
       stability = 0;
       maxstabin = amp1(i-2);
   end
   end
end

subplot(2,1,2)
plot(amp1,snr1)%,'b-d')
s = sprintf('Max SNR = %4.1fdB @ %5.1fdB input\n',maxsnr,inp_maxsnr);
text(-70,60,s)
s = sprintf('Input bin = %3d & BW = %3d\n',f,fB);
text(-70,40,s)
s = sprintf('Max stable input = %4.1fdB',maxstabin);
text(-70,-10,s)

%%%%% Discrete to continuous transformation %%%%%%%
```

```
ntf1 = filt(b1,a1,1/Fsamp);          %It changes nothing, but sampling
time
ntf1 = zpk(ntf1)

% %%%%% Loop filter computation from NTF
L1 = filt(1,1,1/Fsamp) - inv(ntf1);

d2c(-L1)        %Discrete to Continuous (Loop Transfer function : -L1)

[b1,a1]=tfdata(-L1,'v');
org=tf(b1,a1,1/Fsamp)

for i=1:3
    b2(i)=b1(i+1);
end

b2(4)=0;
L2 = tf(b2,a1,1/Fsamp); %Loop filter with ELD compensation, L2 will be
                        %different for different sampling frequency

d2c(L2)         % Loop transfer function L2 (s-domain)
Adc = evalfr(d2c(L2),0)
Adc_db = 20*log10(Adc)

%Partial fraction expansion of Loop filter with ELD compensation
[num1,den1] = tfdata(d2c(L2));
b_coeff = num1{1,1};
a_coeff = den1{1,1};
[r,p,k] = residue(b_coeff,a_coeff)

%Biquad coefficients
b_bq = r(1)*conv([1 -p(2)], [1 -p(3)])+ r(2)*conv([1 -p(1)], [1 -p(3)])
+ r(3)*conv([1 -p(1)], [1 -p(2)]);
a_bq = conv([1 -p(1)], [1 -p(2)]);

%Lossy-Integrator coefficients
a_rc = [1, -p(3)];

figure(2)   %SNR plot
f=Tone;
Fsim=Fsamp*4;
amp=-1.75;
Nfft=4*8192;
sim_time=(Nfft-1)/Fsim;
Ts=1/Fsamp;
sim('LP_ADC2');          %   this step consumes most of the time.
out = downsample(simout, 4)';
len_out = length(out);
dec=Fsim/Fsamp;
fB=ceil(len_out/OSR/2);
```

```
spec=fft(out.*ds_hann(len_out)/len_out);
semilogx(((0:(len_out/2-1))/len_out*Fsamp)/1e6,dbv(spec(1:len_out/2)));
xlim([0.1 250]);
grid on;
ylabel('dB');

snr = calculateSNR(spec(1:fB),Tone);
s = sprintf('SNR = %4.1fdB\n',snr);
text(1,-20,s);
s = sprintf('F_in=%0.5g',Tone/len_out*600e6);
text(1,-140,s);
```

APPENDIX B

MATLAB SIMULATION CODE FOR SNR CALCULATION

```
% Fourth order 4 bit
clear all
f = 100;
N = 8192;
OSR = 12.5;
fB = ceil(N/(2*OSR));

it_hdac = importdata('SD_out_diff.csv',' ');
yout1 = it_hdac(:,2);

for i=1:N
    yout_1(i) = (yout1(i))/0.6;
end

figure
spec1 = fft(yout_1.*ds_hann(N))/(N/4); % Hann windowed sequence
semilogx(linspace(0,1,N/2)*.25e9/1e6, dbv(spec1(1:N/2)),'b');

grid on
xlabel('Frequency (MHz)');
ylabel('Power (dB)');
spec1(1:10) = 0;
snr = calculateSNR(spec1(1:fB),f);
s = sprintf('SNR = %4.1fdB\n',snr);
text(4,0,s);
s = sprintf('NBW=%7.5f',1.5/N);
text(4,-114,s);
```

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