Parameterization of Metallic Grids on Transparent Conductive Electrodes for the Scaling of Organic Solar Cells

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Intense research interest in organic photovoltaic (OPV) devices has resulted in steadily improving figures of merit in recent years. Typically, these devices are fabricated by processing active and buffer layers on transparent conductive electrodes (TCEs). Superlative OPV devices are small (<≈0.1 cm²). The sheet resistance of available monolithic transparent conductive oxide (TCO) materials limits the performance of larger devices and hence the practically attainable cell area. Here, the use of metallic grids in combination with TCOs to create composite TCEs as a means of scaling solution-processed photovoltaics devices to practical sizes is parameterized. Finite element modeling is used to investigate the relevant design parameters and to estimate figures of merit for realistic organic solar cells. It is shown that the scalability of devices with metallic grids improves significantly when grids are implemented at micrometer scales. Representative silver grids are fabricated and the optical and electrical properties of the resulting structures are measured. Overall, these findings indicate that metallic grids can be designed to develop large-area solution-processed solar cells with currently available fabrication techniques.

1. Introduction

The development of solution-processable optoelectronic materials and the push toward mass-producible, low-cost, scalable devices such as light-emitting diodes (LEDs) and photovoltaics (PV) has resulted in success in both academic and commercial settings.[1–6] Commercial successes have included organic light-emitting diodes (OLEDs) for display applications.[3] However, the pixel size of these devices tends to be small (<1 μm) and technological challenges in producing larger-scale OLED panels

for lighting applications remain considerable.[7–9] Similarly, organic photovoltaic devices with impressive efficiencies have been demonstrated at laboratory scales (cell areas <0.2 cm²), whereas large-area organic solar cells (OSCs) remain a technical challenge and are critical for their commercial viability.[10–14]

Most solution-processed devices, including organic and perovskite solar cells (PSCs), are produced on a transparent conductive electrode (TCE) to allow light to enter (or exit) the device while providing conformal electrical contact. Two key parameters that are important in choosing a TCE are its sheet resistance (R_{sheet}) and optical transmittance. Of these, R_{sheet} is the limiting factor in the production of high efficiency, large-scale, solution-processable PV. This issue is common to all material systems for solution-processable PV including OSCs, PSCs and nanocrystals, which are produced atop (typically inorganic) TCE materials such as transparent conductive oxides (TCOs). State-of-the-art high-quality TCE materials such as indium tin oxide (ITO) and fluorine-doped tin oxide (FTO) can provide $R_{sheet} \approx 8\ \Omega\ \square^{-1}$.[15] FTO is commonly used in mesoporous thin film PV and are used in amorphous Si, CdTe, and PSCs.[16] ITO thin films are currently used as the TCEs for most organic optoelectronic devices.[17,18] The dominance of this material over possible alternatives is due to its properties such as large bandgap (3.5–4.3 eV), high work function (≈4.5 eV), conductivity (10³ S cm⁻¹), and optical transmittance (>84%) in the visible region.[19,20] However, although the conductivity of ITO electrodes is sufficient for small-scale research and development work, it presents a developmental barrier for highly efficient large-area OSC devices. Several promising alternatives to ITO as monolithic TCE materials have been developed in recent years. Notable mentions are transparent conducting polymers,[21–23] carbon nanotube films,[24–26] metal nanowires,[21,27,28] and graphene.[28–30] These materials have shown R_{sheet} in the ranges of 6–182, 5–1000, 6–91, and 14–1100 Ω □⁻¹, respectively. Additionally, the materials have shown average visible transmission (%AVT) of 71–95, 75–90, 72–94, and 80–94, respectively. Advanced monolithic TCEs are thus an area of noteworthy technological developments but are still incapable of providing suitable figures of merit for large-area OSCs. Other developments of note include the use of ultrathin aluminum-doped silver films,[31] and the use of nanoscale metallic grids for optoelectronic applications,[32] including LEDs.[33–35]

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The synergistic use of metallic grids with transparent conductive materials is an attractive proposition for reducing the effective R_{sheet} of TCEs while maintaining optical transparency.[7] Metal lines can be printed using conductive inks, which are suitable for flexible substrates.[36] Higher feature resolution can be achieved using semiconductor processing techniques, such as microfabrication methods, particularly to produce prototype devices. In R&D environments, the tools to produce micrometer-scale grids are frequently available, for example, photolithography and metal deposition, which are available at many university cleanroom facilities. Using microlithography to produce metal grids on ITO is an attractive option for R&D work, as designs can be rapidly prototyped and implemented at scale on commercially available ITO. This offers an efficient route to realize large-scale prototype optoelectronic devices with good figures of merit on rigid substrates. The rapid developments in the field of flexible electronics also require that TCE materials maintain their conductivity after bending. The presence of metal grids on brittle TCOs may also ameliorate cracking and other defects on flexible substrates, as demonstrated in TCO/metal/TCO electrodes.[37] The use of nanoimprinted grids has also been reported on both rigid and flexible substrates, although challenges such as surface roughness remain.[17,38]

At commercial scales, the use of metallic grids and replacing ITO with other materials may offer advantages in terms of cost, device reproducibility, and environmental advantages. The scarcity of indium is a concern for the long-term use of ITO in TCEs. As a byproduct of zinc production, and relatively scarce in the Earth's crust, the production capacity of indium is limited.[39] The use of metallic grids can be a route to TCEs produced with Earth-abundant elements and offer other advantages such as the choice of work function and resistance to chemical erosion. In parallel, this can be combined with material efficient thin layer TCO deposition techniques, for example using atomic layer deposition compatible materials such as aluminum-doped zinc oxide.[40]

Solution-processed OSCs are anticipated to be lightweight, low-cost, and affordable components of PV panels with added functionality compared to existing technologies. For example, OSCs are being developed for use in flexible PV or building-integrated photovoltaics (BIPV).[41,42] In practice, the overall solar module area may be on the order of tens to hundreds of centimeters for mobile or embedded PV power generation, to hundreds of square meters for BIPV. To create suitably sized modules, OSCs can be assembled into smaller "sub-module" cells with interconnects, or alternatively, the cells can be created on larger monolithic substrates. The TCE upon which the OSC is fabricated must be suitable for low-cost applications for these devices to be practical.

In this work, the relevant parameters for enhancing TCE characteristics with metallic grids for OSCs are introduced. The findings can be extrapolated in any other solution-processed PV technology such as perovskites and nanocrystals. Finite element modeling (FEM) is used to simulate the behavior of large-area OSCs and the utility of metallic grids is shown as the figures of merit offered by monolithic materials demonstrate poor performance at large cell areas. The effect of varying the dimensions of the metallic grids is simulated, demonstrating the motiva-

tion for micrometer-scale grid structures. Exemplary grid structures on ITO are fabricated using microfabrication techniques and relevant optical and electrical parameters are measured. Finally, technologically feasible scenarios for the incorporation of metallic grids into realistic OSC panels are reviewed. From these results, high-performance TCEs with metallic grids are presented as a facile means of creating large-area OSC devices; first at R&D scales, and subsequently moving to large-volume manufacturing as processing techniques mature.

2. Results

2.1. Motivation for the Incorporation of Metallic Grids

Commercially available high-quality ITO substrates with an acceptable %AVT (> 80%) typically have R_{sheet} on the order of 10 Ω □$^{-1}$. It is therefore instructive to explore the effects of R_{sheet} of the TCE on the practical cell size. OSCs were simulated with varying cell areas to investigate the scalability of high-quality ITO for large cell applications. Results from FEM of OSCs with 10 Ω □$^{-1}$ TCEs are shown in **Figure 1** (see the Experimental Section). Current density–voltage (JV) characteristics from simulated OSCs with varying cell areas are shown in Figure 1a. The fill factors (FFs, inset graph) do not vary significantly for the smallest sizes (0.1, 1 cm side lengths), but reduce significantly with side lengths above 5 cm. The reason for this can be seen from the potential contour plots varying with pixel size. Small (0.01 cm², Figure 1c) cells show little variance in potential across the TCE during operation when the bus-barred device is biased at maximum power point voltage (V_{MPP}, 0.73 V). In comparison, there is a significant potential drop at larger areas (100 cm², Figure 1d), in which case a large proportion of the OSC device is operating close to the open-circuit voltage ($V_{OC} \approx 0.92$ V), not the maximum power point ($V_{MPP} \approx 0.56$ V), hence generating low power. Cell areas <1 cm² are typical for OSC devices in research literature.[12] Comparing the performance at different cell sizes, small-area OSC devices do not scale when typical TCE materials are used. Devices fabricated on the best-performing monolithic materials thus have a practical maximum cell size on the order of 1 cm².

Next, the effect of the R_{sheet} of the TCE on large-area OSC device performance is considered. Simulated JV characteristics from 5 cm × 5 cm pixels with varying R_{sheet} are shown in Figure 1b. In this work, cell areas of 5 cm × 5 cm are referred to as "large," and this is taken as the minimum area that a monolithic OSC can be a practical alternative to established PV technologies. The FF (inset graph) for cells with TCE R_{sheet} of 0.1 and 1 Ω □$^{-1}$ are around 0.7 and decrease significantly with R_{sheet} > 5 Ω □$^{-1}$. For large-area cells, there is a significant potential drop with a TCE of R_{sheet} = 10 Ω □$^{-1}$ (Figure 1f), compared to an identical cell with R_{sheet} = 1 Ω □$^{-1}$ (Figure 1e). For the fabrication of large-area OSCs, a TCE with R_{sheet} < 1 Ω □$^{-1}$ is required for practical devices.

As it has been shown that the performance of an OSC depends on its pixel size, it is useful to define the *scalability* of a given structure. This can be defined as the ratio of the large-scale maximum power density to the maximum power density of a small-area cell
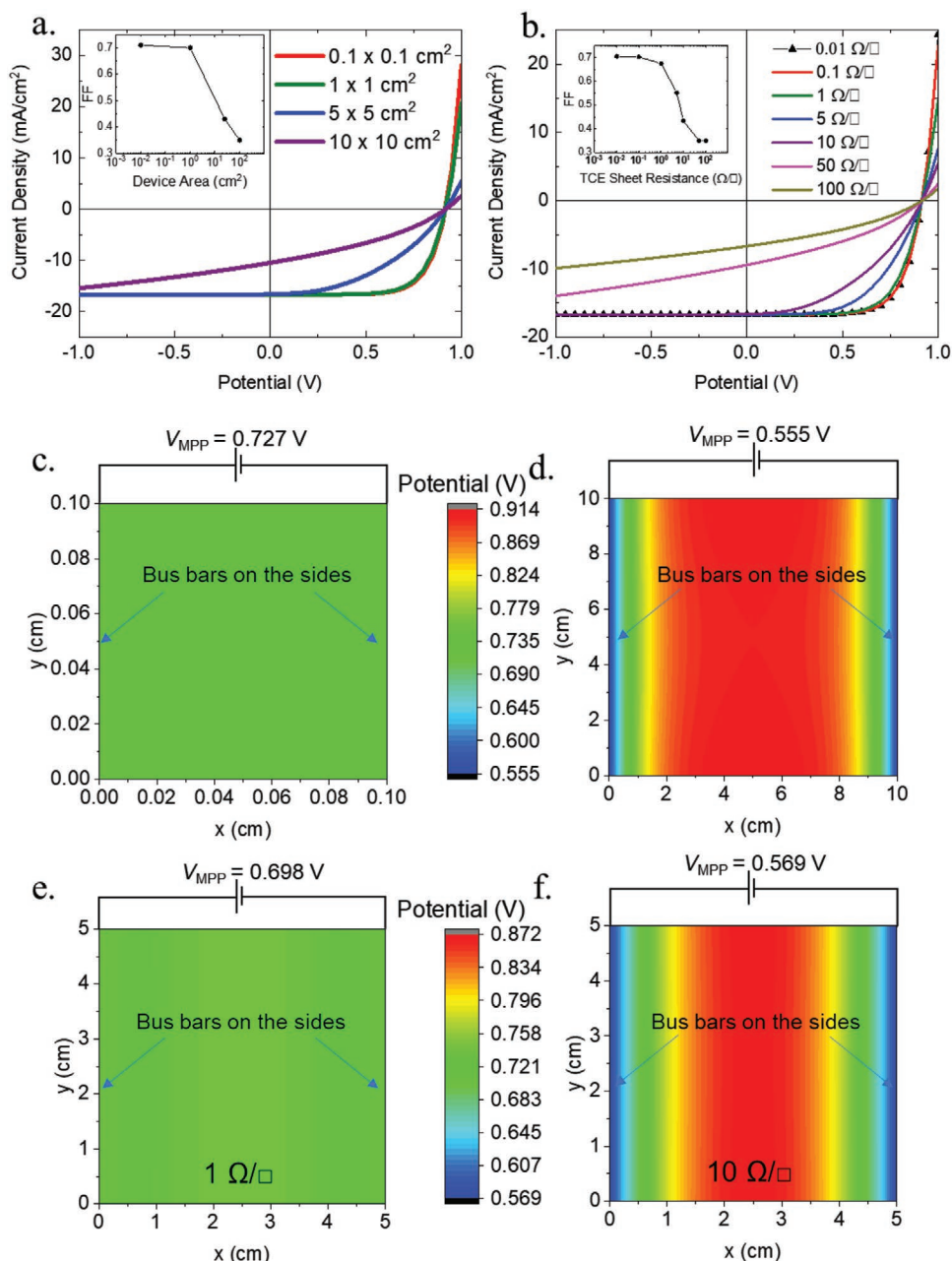
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Figure 1. The effect of device area and TCE sheet resistance on monolithic solar cell performance. Each simulated cell is based on a PDBD-T:IT-M device (see the Experimental Section) with $V_{OC} = 0.92$ V (2 s.f.). In panel (a) the JV characteristics for various cell sizes are drawn with TCE $R_{sheet} = 10$ Ω $\square^{-1}$, with an inset of the FF dependence on device area. Panel (b) shows JV characteristics for cells at varying TCE sheet resistances for 5 cm × 5 cm devices, with an inset of the FF dependence on the TCE sheet resistance. Panels (c) and (d) show the potential distribution at V_{MPP} across a small area (0.01 cm²) and large area (10 cm²) solar cell with TCE $R_{sheet} = 10$ Ω $\square^{-1}$. e,f) The effect of increasing TCE sheet resistance on device performance for 5 cm × 5 cm devices. (e) The potential distribution is seen for a TCE sheet resistance of 1 Ω $\square^{-1}$ for a 5 cm × 5 cm device. Panel (f) shows the same, with a sheet resistance of 10 Ω $\square^{-1}$.

$$s = \frac{P_{\text{max,large}}}{P_{\text{max,small}}} \quad (1)$$

where $P_{\text{max,large}}$ is the maximum power density produced in a large-area device and $P_{\text{max,small}}$ is the power density produced by a small-area device. The effect of R_{sheet} on device scalability is plotted in **Figure 2** for devices with 0.1, 1, 10, and 100 Ω $\square^{-1}$-

based OSCs as a function of device size. With 10 Ω $\square^{-1}$ TCEs, device scalability is poor for practical device sizes (>5 cm). R_{sheet} on the order of 100 Ω $\square^{-1}$ is typical for TCEs on flexible substrates, which are seen to scale poorly with device size.

As no monolithic materials currently exist that can produce <1 Ω $\square^{-1}$ TCEs with a satisfactory optical transmittance, a practical alternative is to reduce the effective R_{sheet} of a monolithic
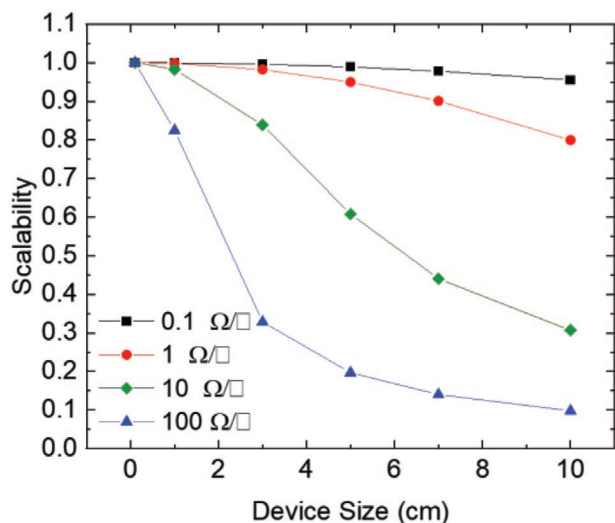
Figure 2. Scalability as a function of device size (equal width and length) with a TCE R_{sheet} of 100 Ω □$^{-1}$ (blue triangles), 10 Ω □$^{-1}$ (green diamonds), 1 Ω □$^{-1}$ (red circles), and 0.1 Ω □$^{-1}$ (black squares).

material with the addition of metallic grids. The effect of adding hexagonal metallic grids to 5 cm × 5 cm OSCs ("MG-OSCs") is shown in **Figure 3**. With 10 and 100 Ω □$^{-1}$ monolithic TCEs ("ITO-OSCs", Figure 3b), poor FFs are achieved at this pixel
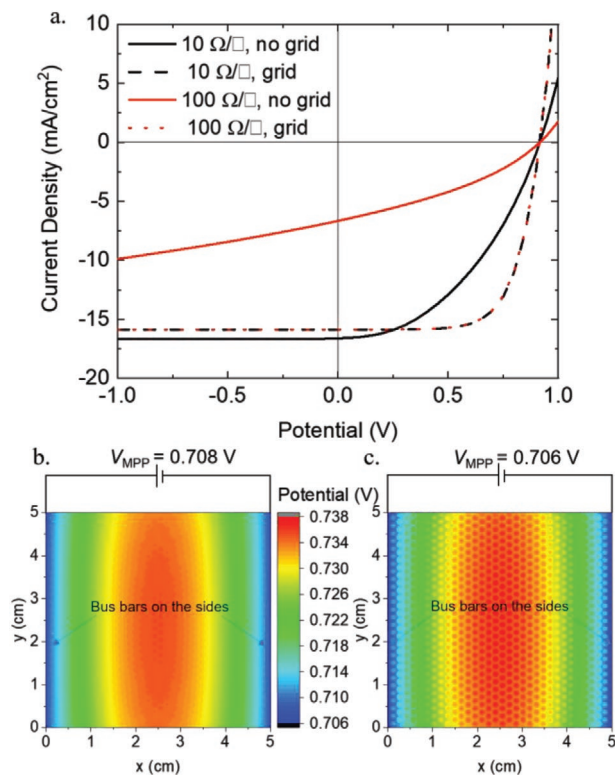

Figure 3. The effect of the addition of hexagonal metallic grids to OSCs. Panel (a) shows JV characteristics for simulated ITO- and MG-OSCs. Panels (b) and (c) show the potential distribution at the respective V_{MPP} for MG-OSCs with R_{sheet} = 10 Ω □$^{-1}$ (black dashed curve in (a)) and R_{sheet} = 100 Ω □$^{-1}$ (red dotted curve in (a)).
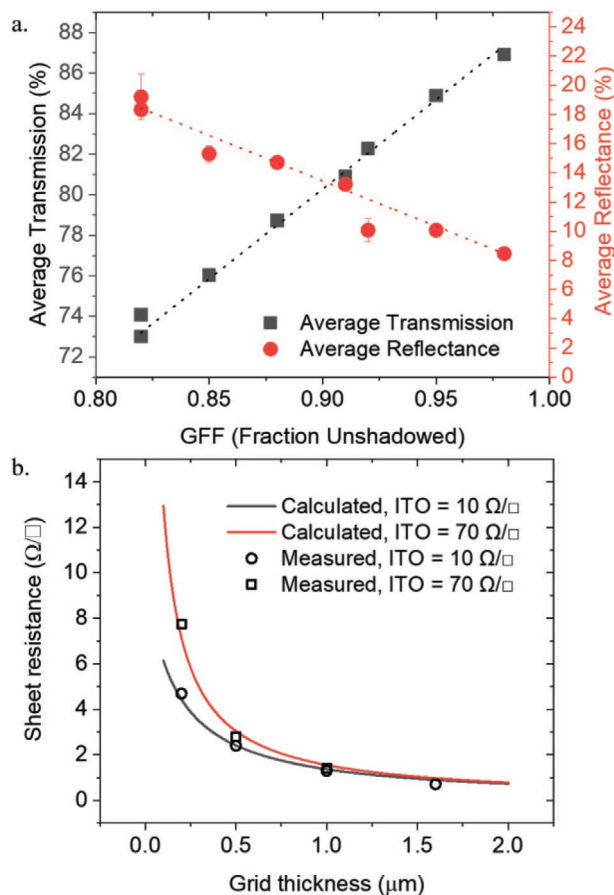

Figure 4. a) Average (400–1300 nm) transmission (black squares) and average reflectance (red circles) measured for grids with varying geometric fill factor (GFF) on glass substrates. b) Effective sheet resistance of transparent conductive electrodes with varying grid thickness. Circles = TCEs fabricated on 10 Ω □$^{-1}$ ITO, Squares = TCEs fabricated on 70 Ω □$^{-1}$ ITO. Solid lines are generated from a parallel resistor model.

size. Upon adding metal grids to the TCE, FFs are significantly improved and the JV profiles are similar, independent of initial TCE R_{sheet}. The short circuit current density (J_{sc}) is seen to drop in the MG-OSCs, consistent with the shading from the metal grid structures. Potential contours of the TCE demonstrate how the addition of metallic grids (Figure 3c) provides an equipotential surface compared to a monolithic TCE, which shows a significant voltage drop toward the edge busbars of the device, associated with the TCE R_{sheet}.

2.2. Exemplification of TCO/Grid TCEs

To verify that the simulated TCE structures could be created practically, a range of metallic grid structures on ITO/glass were fabricated using semiconductor fabrication techniques (see the Supporting Information). The resulting average optical transmission and reflection (400–1300 nm) is plotted with varying geometric fill factor (GFF), or fraction unshadowed, and demonstrated linear behavior (**Figure 4**a). This indicates that the shadowing of the grids is accurately predicted by the design of the grid structures, as calculated by their GFF. The GFF of

the grid structures were varied by varying the pitch (0.5–1 mm) and wire width (20–100 µm) of hexagonal grid structures.

The effective R_{sheet} of ITO substrates with metal grids of varying thickness is shown in Figure 4b. Grid structures were added to ITO with starting R_{sheet} of 10 and 70 Ω □$^{-1}$. This was fitted to a parallel resistor model (solid curves), which accurately predicts the effective R_{sheet} of the gridded TCE, which is defined here as the equivalent "sheet resistance" of the overall grid/ITO structure as measured using a four-point probe technique. Understood as a parallel resistance, at a critical thickness of the grid geometry, the R_{sheet} of the ITO layer has a diminishing effect on the equivalent R_{sheet} of the overall structure.

2.3. Design Considerations of Metallic Grids

The design of grids for use as components of TCEs must consider two competing effects. First, the presence of opaque metal grids on the TCE will shadow the light entering the active layer of an OSC device, reducing the generated photocurrent. At the same time, the overall resistance of the grids decreases with the covered area. The GFF is thus an important figure of merit for designing MG-OSC architectures. However, a given value of GFF can be achieved with vastly different grid geometries. The effect of varying hexagonal grid dimensions while keeping the GFF constant is summarized in **Figure 5**. Potential contours from 5 cm × 5 cm devices demonstrate how the surface potential across the OSC TCE varies considerably depending on grid geometry. For coarse geometries (r = 2.2 cm, w = 0.2 cm)

a considerable difference in surface potential is seen between the center of the cell and the edges. In this extreme case, the area of the cell circumscribed by the hexagonal grid structure is in effect a sub-cell, whose performance is determined by the R_{sheet} of the underlying ITO. The surface potential is less varied as the grids are finer (r = 2.2 mm, w = 200 µm and r = 220 µm, w = 20 µm), although the improvement to scalability does not change substantially at these dimensions. This motivates the production of metallic grids for TCE applications with critical dimensions on the order of tens of micrometers.

2.4. Thickness and Conductivity of Metallic Grids

Even if highly conductive metals such as silver are used to produce grids for TCEs, the grids must have some finite thickness to substantially reduce the effective R_{sheet}. The effect of varying the thickness of the applied grids with a constant lateral geometry is shown in **Figure 6**. The thickness of the metal grids is simulated for 10 µm, 1 µm, and 100 nm (Figure 6b–d). With thick, 10 µm grids, the TCE surface potential is uniform, with very little variation across the surface. Some voltage drop can be seen for 1 µm grids, but a considerable drop is seen when the grids are only 100 nm thick. There are limits to the thickness of grids that are practical in TCEs. As finer grid dimensions are preferred laterally, increasing the grid thickness will produce grid structures with very high aspect ratios, which may be difficult to manufacture, or may not be mechanically robust to solution processing.
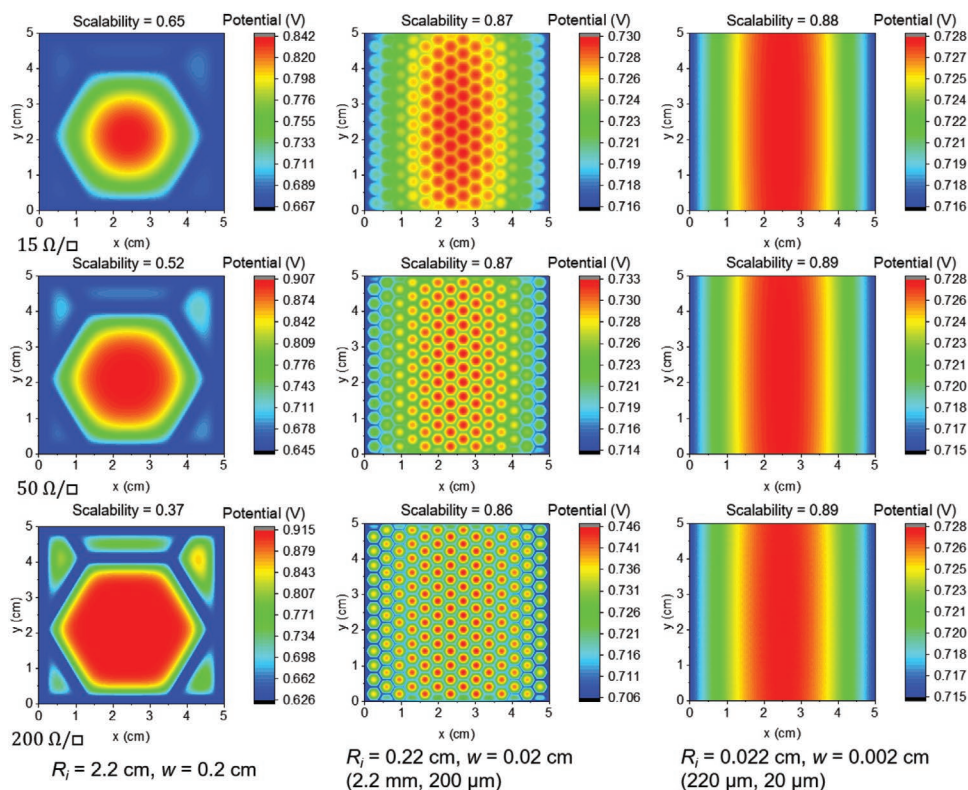

Figure 5. Potential contours of 5 cm × 5 cm solar cell devices with varying values of R_{sheet} and grid geometries. However, the GFF of the grid was constant. All potential contours were extracted at V_{MPP} (to 3 s.f.) for each respective device, which is the lowest labeled potential on each of the color scales.
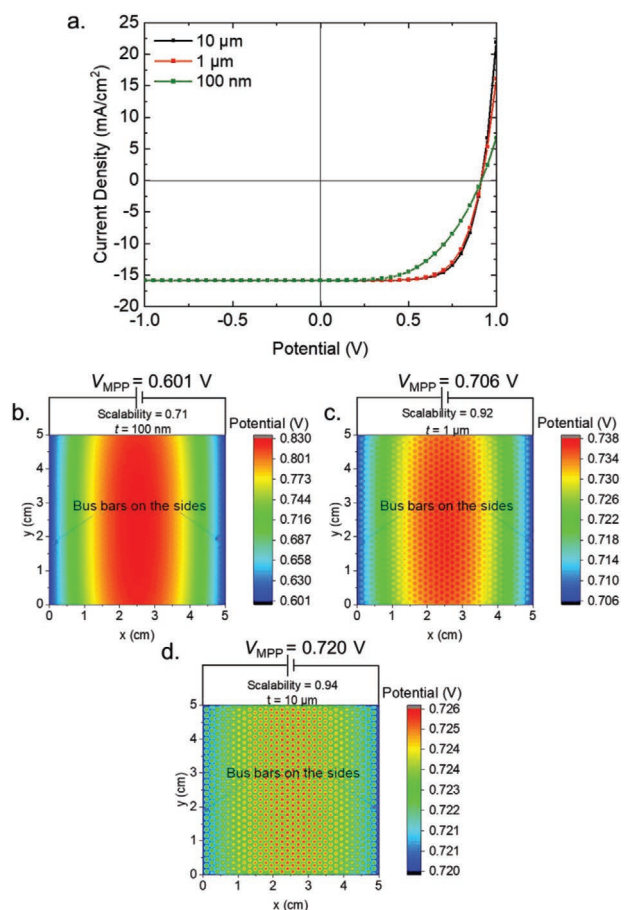
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Figure 6. a) JV curves for solar cell devices with varying thicknesses (out of plane) of Ag, hexagonal grids used in conjunction with ITO of $R_{sheet} = 100\ \Omega\ \square^{-1}$. b–d) Potential contours were plotted at the respective V_{MPP} (to 3 d.p.) for these devices. The hexagonal radius was 1 mm and the track width was 40 μm. The bulk resistivity of Ag was used for the calculation of the metallic grid sheet resistance.

As silver is a highly conductive metal, it is a good candidate material to produce grids on TCEs. However, real silver structures produced by common fabrication techniques do not have the same conductivity as the bulk material. Further, when comparing the resistivities of thin films, Matthiessen's rule should be considered, which states that the electrical resistivity of metals can be written as the sum of its intrinsic resistivity (or phonon part of the resistivity) and the residual resistivity attributed to scattering by impurities and imperfections.[43] A correction factor can be used to compare deposited material to the reference bulk value ($\rho_{Ag} = 1.59 \times 10^{-8}\ \Omega m\ @20\ °C$[44])

$$\zeta = \frac{\rho_{measured}}{\rho_{bulk}} \tag{2}$$

With this expression, silver deposited using different methods can be compared and are shown in Table S1 in the Supporting Information.

The equivalent R_{sheet} of ITO with sputtered silver grids can be seen in Figure S1 in the Supporting Information. As the grid thickness is increased, the R_{sheet} of the underlying ITO has little effect, as $R_{Grid} \ll R_{ITO}$.

2.5. Equivalent Circuit Approximations

It is illustrative to compare the FEM results to that of an equivalent circuit model to see the limits of a lumped matter approximation for large-area devices. **Figure 7** shows a comparison between these simulation methods. With 10 μm thick metallic grids (Figure 7a, $R_{sheet} \approx 60\ m\Omega\ \square^{-1}$), the behavior of the 5 cm × 5 cm cell can be approximated by an equivalent circuit model which includes series resistance terms. However, as the grid thickness is reduced (TCE resistance increased), this becomes a poor approximation, as the distribution of the potential across the TCE is not included in the lumped equivalent circuit model. With 1 μm grids ($R_{sheet} \approx 0.5\ \Omega\ \square^{-1}$, Figure 7b), the general behavior is modeled, but the FF is overestimated by the equivalent circuit. However, with 100 nm grids ($R_{sheet} \approx 4\ \Omega\ \square^{-1}$, Figure 7c), the large-area JV behavior of the cell is poorly predicted by an equivalent circuit model. This can be understood by observing the voltages across the surface of these cells in Figure 6b–d at V_{MPP}. As the grid thickness is decreased, a larger proportion of the cell area operates close to the V_{OC}. This is reflected in the decrease in scalability (defined in Equation (1)), as less power is generated in these devices.

2.6. Influence of the OSC Active Layer on Scalability

Charge extraction in OSCs is often limited by charge transport and recombination. A modified Shockley equation has been introduced by Neher et al.[45] to parameterize the JV characteristics of transport-limited solar cells.

$$J = J_G \left\{ \exp\left[\frac{q(V_{ext} - V_{OC})}{k_B T (1 + \alpha)} \right] - 1, \right\} \tag{3}$$

in which J_G is the photocurrent, V_{ext} is the applied voltage, k_B is the Boltzmann constant, q is the unit charge, and T is the absolute temperature of the junction. This model can be used to approximate the JV characteristics of OSCs through parameterizing the bimolecular recombination rate constant (β), electron and hole mobility (μ_n and μ_p) and thickness (d) into one dimensionless figure of merit, α,

$$\alpha^2 = \frac{q \beta J_G d^3}{4 \mu_n \mu_p (k_B T)^2} \tag{4}$$

Here we show the effect of varying α on scalability and power conversion efficiency (PCE) for an exemplary device in **Figure 8** and the resulting line profiles of the potentials across the devices are shown in Figure S2 in the Supporting Information. ITO-OSCs demonstrate poor scalability at low values of α, i.e., for more efficient, Shockley-type devices with nearly perfect charge extraction. This indicates that the TCE-related losses are more critical for the most efficient solar cells. OSC-related material developments such as improved/balanced carrier mobilities or reducing bimolecular recombination demonstrated at small-scale do not translate to better performance in large-area devices with monolithic TCEs such as ITO. This presents a developmental barrier to large-area cells with good figures of merit. In contrast, as α is varied, the scalability of MG-OSCs

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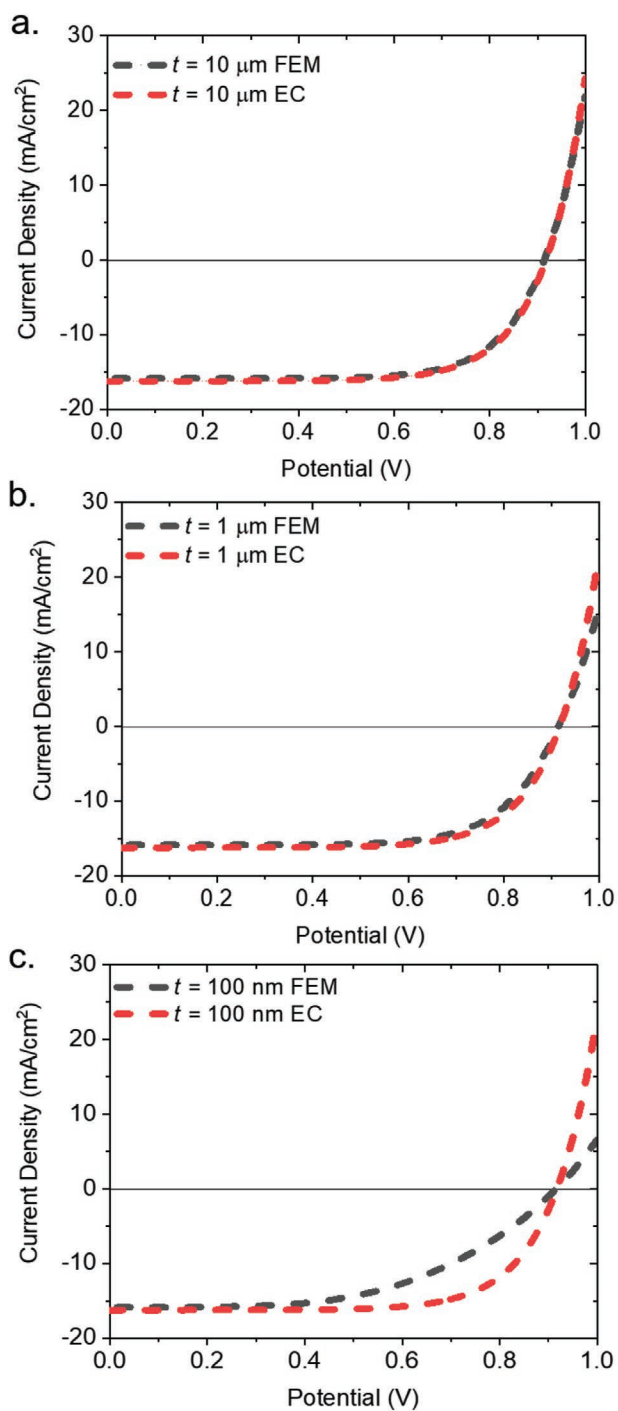MATERIALS**

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Figure 7. Comparison of 5 cm × 5 cm device JV profiles with varying metal grid thicknesses t generated from a finite element model (FEM, black curves) and an equivalent circuit model (EC, red curves) for a): 10 μm grids, b) 1 μm grids, and c) 100 nm grids.

remains consistently >0.85 (Figure 8a). The PCEs (Figure 8b) of large-area MG-OSCs are significantly greater than ITO-OSCs at all values of α. At low values of α, the large-area MG-OSCs produce PCEs close to that given by the analytical description of the FF (black line, see the Experimental Section). Accounting

for a finite series resistance (red dashed line) more closely predicts the performance of MG-OSCs as compared to FEM-simulated devices, which is only slightly below the idealized material performance. High-performance TCE structures with metal grids that demonstrate good scalability are thus capable of exploiting these material developments at scale.

2.7. Grid Fabrication Technologies

Having established the potential utility of the grid approach, it is instructive to consider technologies to produce grids on OSCs, and the relative performance associated with these technologies. Simulations of 5 cm × 5 cm OSCs produced with different technologies are summarized in **Figure 9** and the line profiles of the potentials of these devices are shown in Figure S3 in the Supporting Information. Additionally, the potential contours for these devices are shown in Figure S4 in the Supporting Information. The grid geometries in all cases were selected to have a constant GFF of 0.95. For producing OSCs,
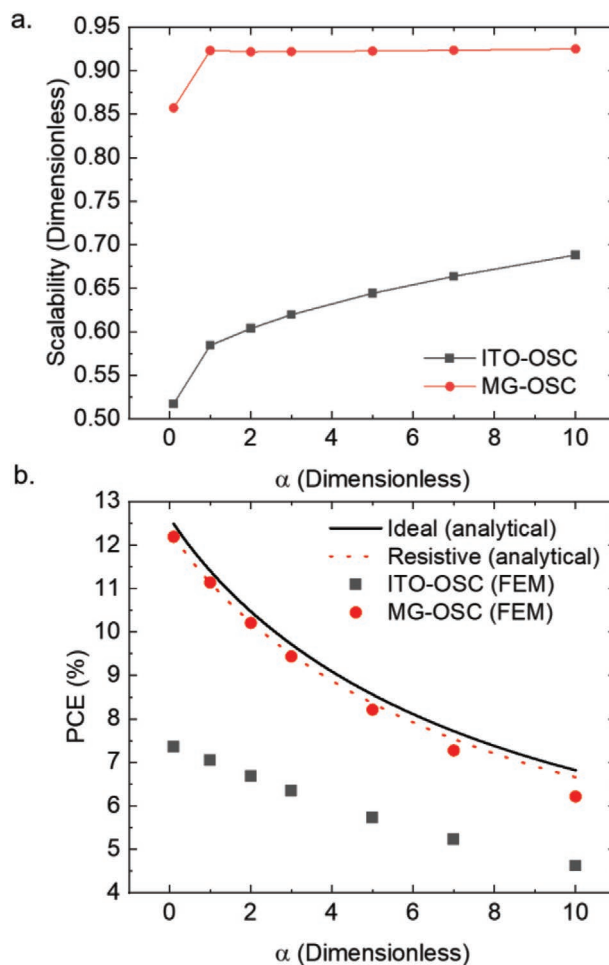

Figure 8. Dependence of a) scalability and b) PCE for varying extraction figure of merit (ideality factor) for 5 cm x 5 cm ITO- (black squares) and MG-OSCs (red circles). Analytical calculation for PCE for an ideal device is shown in the solid black line and with resistance terms in the dashed red line.
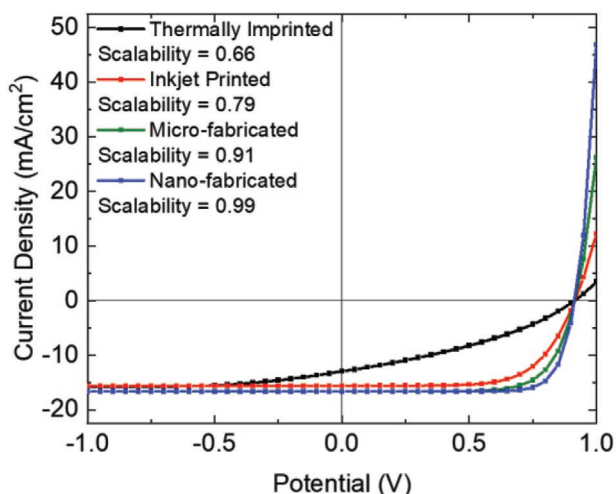
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Figure 9. JV characteristics from the simulations of MG-OSC devices, with varying methods of fabrication of the metallic grids. Potential contours and simulation parameters can be found in Figure S3 in the Supporting Information.

printing technologies will tend to produce the lowest cost per unit area. Reported methods for the development of flexible TCEs include thermal imprinting, flexographic, and inkjet roll-to-roll processing.[46] These methods vary in terms of cost, resolution, and roughness of the electrode. A simulated JV curve for an MG-OSC containing a thermally imprinted TCE is shown in Figure 9 (black curve). Current solution-processable flexible TCEs have R_{sheet} on the order of 100 Ω □$^{-1}$, and the reproducible print resolution of conductive structures on large-area substrates (for example, roll-to-roll processing), is on the order of 100 μm. In a fully printed OSC, the active layer will tend to be thicker (>500 nm) to avoid issues related to thin printed layers, such as point defects and thickness uniformity. This will tend to cause α to be higher than for an ideal device. In this example, R_{sheet} = 100 Ω □$^{-1}$, grid width = 18 μm, hexagonal radius = 370 μm, ζ = 2.89, α = 2.25.

Another roll-to-roll technique for depositing metallic grids is inkjet printing, offering a similar printing resolution on the order of 100 μm, with higher-resolution techniques being reported in the literature.[47,48] An example JV characteristic is shown for an inkjet fabricated MG-OSC in Figure 9 (red curve). In this example, R_{sheet} = 100 Ω □$^{-1}$, grid width = 132.5 μm, hexagonal radius = 2.67 mm, ζ = 2.3, α = 2.25.

More established semiconductor processing methods, such as micro and nanofabrication, can also be used to fabricate metallic grids. An example JV curve for a microfabricated MG-OSC is shown in Figure 9 (green curve). In this example, R_{sheet} = 10 Ω □$^{-1}$, grid width = 2 μm, hexagonal radius = 1 mm, ζ = 1.5, α = 2. Additionally, the JV characteristic for a nanofabricated MG-OSC is shown in Figure 9 (blue curve). In this example, R_{sheet} = 5 Ω □$^{-1}$, grid width = 100 nm, hexagonal radius = 2.05 μm, ζ = 1, α = 1. In the last two examples an equivalent R_{sheet} was calculated instead of simulating grid geometries, due to the computational expense of performing FEM simulations with the required resolution.

Overall, Figure 9 demonstrates that the greater the fabrication resolution of MG-OSCs, the greater the FF. This is due

to the decrease in TCE R_{sheet}, as shown in Figure 1b (inset). Increasing FF lends to greater scalability, where MG-OSCs have the advantage over ITO-OSCs. The use of metallic grids is therefore a valuable option for developing scalable and high efficiency monolithic OSCs, which must be balanced with the cost of producing TCEs with these fabrication techniques in real-world manufacturing settings.

3. Discussion

3.1. Operating Regimes of TCEs with Metallic Grids

To aid the understanding of the effect of adding metal grids to a TCE, the current density of the device can be split into sub-"cells," as defined by the grid geometry. The overall device current density is given by the sum across n domains

$$J_{device} = \frac{1}{A} \sum_{k=1}^{n} \left\{ \sum_{x,y=0}^{max(x,y)} \hat{i}_k \left[V(x,y) \right] \right\} \tag{5}$$

where J_{device} is the current density of the OSC as measured at its terminals, A is the sub-cell area, and $\hat{i}_k[V(x,y)]$ is the current at sub-module k resulting from potential at point (x, y). With this expression, three distinct regimes can be defined. First, in the case of highly conductive grid structures, the metal grids provide an equipotential surface across the TCE. In this case, the behavior of the device is approximated by summing across the cells, which are all at the same potential

$$J_{device} \approx \frac{1}{A} \sum_{k=1}^{n} I_{cell}(k) \tag{6}$$

$$J_{device} \approx \frac{n}{A} I_{cell}(V) \tag{7}$$

This regime will correspond to device architectures with high scalabilities (>0.9), meaning that the large-area behavior of the OSC will be consistent with those made at a smaller scale. In practical terms, a large proportion of the cell area will operate at V_{MPP}, as there is little variation in potential across the TCE. This also corresponds to devices that can be accurately modeled using an equivalent circuit approximation.

Another operating regime is defined where the voltage across the surface of the TCE is varying, but there is no significant voltage variation within the sub-cell. This can be approximated by defining the voltage of the cell as the voltage at its node at that point in the grid

$$J_{device} \approx \frac{1}{A} \sum_{k=1}^{n} I_{cell}(V(i)) \tag{8}$$

where $V(i)$ is the voltage at the node of that cell. Most realistic designs of metallic grids on TCEs with practical dimensions will operate in this regime, as some finite R_{sheet} will remain (≈1 Ω □$^{-1}$) with realistic grid structures. The potential variation may be small but will tend to reduce the FF and PCE of the large-area cell.

Lastly, an operating regime is defined where the grids are not conductive enough to provide points of equal potential across
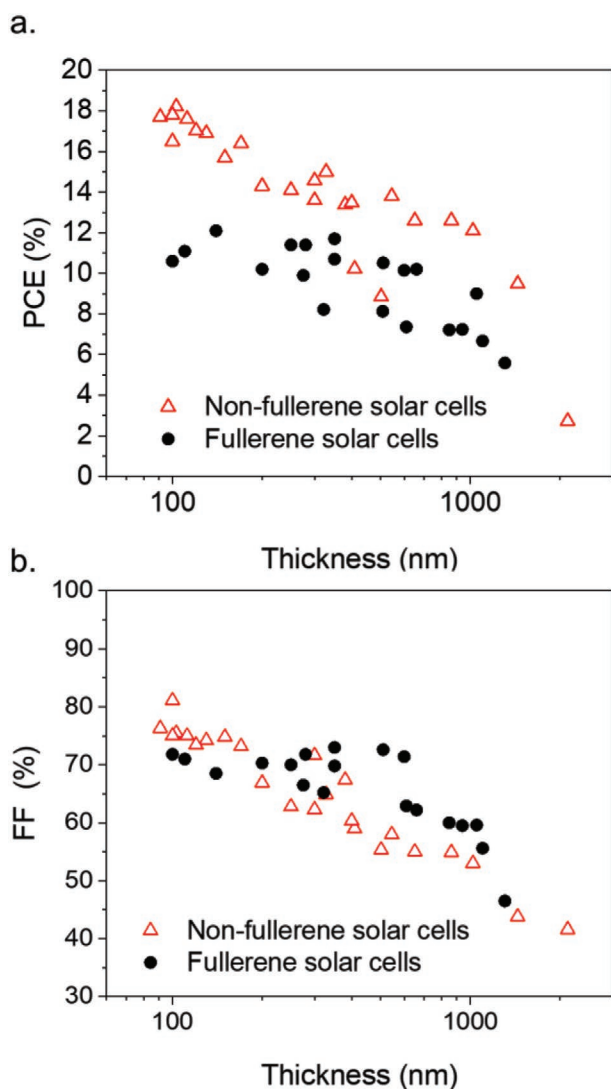
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a.

b.

Figure 10. A literature survey figure for record a) PCEs and b) FFs of fullerene (black circles) and nonfullerene (red triangles) devices for varying reported junction thicknesses.

the TCE. This can be approximated by considering a monolithic material with a slightly reduced equivalent R_{sheet} of the grid and TCO in parallel. In this scenario, the device performance of large-area cells will typically improve compared to a monolithic TCE, but will be poor compared to a highly conductive structure.

3.2. Active Layer Thickness and Conformal Coating of Grids

Due to the low carrier mobilities of organic semiconductor materials, OSCs with high PCEs are typically generated with thin (< 100 nm) active layers. Losses in FFs and PCEs of OSCs are observed when active layers are thicker than 150 nm. These losses are primarily due to imbalanced mobilities that originate from recombination where space charges can be built up because of the low mobility of the slower carriers. However, for a practical OSC at scale, the use of thick junctions (> 500 nm) is

encouraged, not only for absorbing more photons but also for large-scale solution printing technology. The use of thick junctions is advantageous in reducing the number of point defects, improving thickness uniformity and improved electro-optical properties. The suitability of organic materials to produce thick devices varies with the behavior of charge carriers in the material. A survey figure summarizing the performance metrics of OSCs with various junction thicknesses is shown in **Figure 10**. Although PCEs and FFs tend to decrease with increasing junction thickness, encouragingly PCEs over 10% and 13% have been realized in fullerene and nonfullerene acceptor (NFA) based solar cells with a thickness of 500 nm, respectively.[1] In particular, the use of NFAs is a promising recent development for thick bulk heterojunction OSCs. This new class of acceptor materials has demonstrated examples with reduced bimolecular recombination, which is beneficial for the scaling of thick junction devices. Further, NFA-containing OSCs have demonstrated greater thermal and photochemical stability and longer lifetimes.[49]

3.3. Technological Outlook for Grid Incorporation

The practicality of conformally coating grid structures with solution-processed organic layers should be considered for their applicability to OSC device architecture and fabrication. During the film-forming process through solution methods, the wetting ability of the processed solution with the grid structures should be considered first. As shown in Figure S5 in the Supporting Information, it can be found that the commonly used solutions such as poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) exhibit low contact angles to the grid substrate. The wetting ability of these solutions indicates that grid structures can be used in common solution processing coating techniques (spin-coating, bar-coating, spray-coating, and slot-die) and has promising prospects as a conductive substrate in the application of organic electronics. It should also be noted that the substrate for film-coating has been demonstrated to be an important factor in determining the morphology of organic semiconducting films. The physical and chemical interactions between the substrate and the solution could affect the molecular organization during the film-forming process. This does not result in different crystallinity and phase separation in organic semiconducting films but could modulate the component distribution in the vertical direction in the active layers of OSCs.[50–52] Compared to traditional ITO substrates, the addition of metal grids endows more flexibility with morphology optimization in organic semiconducting films. Furthermore, the type of coating technology will determine the degree of conformality that can be achieved on structures with high topography. Spin-coating methods, which are common for small-scale R&D devices, may not be suitable for these applications. Coating methods such as rotary screen printing, in which the direction of the shear force is normal to the surface may have more suitability for coating these types of structures, especially when the substrate is rough.[18] Another consideration is the presence of undesirable features such as spikes in grid structures, which may cause shorting behavior in an assembled device.

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Microfabrication techniques, such as those used in the TCEs produced in this work, are useful for the rapid prototyping of structures with micrometer-scale features. Direct-write or "mask-less" methods such as laser lithography are useful for the rapid prototyping of new designs. Mask aligners or steppers can be used when designs are being tested at scale. Thin-film deposition methods, such as evaporation or sputtering are also commonly used in these facilities. Combined, high-performance TCE structures can be produced using these techniques for research purposes. The feature sizes required to produce good scalability are easily attainable even with older generation equipment and without extensive process optimization. However, these techniques are best suited for rigid substrates (such as glass) intended to tackle the challenge of large-area, monolithic OSC devices. They are less appropriate for the development of flexible, high-performance TCEs. The development of suitable printed, flexible grid structures is therefore necessary for the development of high-performance, flexible OSC devices.[46] Recent reports of TCEs produced using techniques such as offset printing and electrohydrodynamic inkjet printing have demonstrated line widths below 10 µm with high optical transmittances and applicability to flexible devices.[47,48]

Nanolithography techniques could also be considered for the future development of high-performance TCEs. While this may be prohibitively expensive for most intended OSC devices, certain niche applications, particularly those requiring high specific power, may benefit from such structures. Direct-write techniques such as electron beam lithography can produce structures well below the diffraction limit of light and may also be available at R&D facilities. At scale, the use of nanoimprint techniques may be capable of producing application suitable, high-performance TCE structures as technical challenges such as surface roughness are addressed.[15,16]

4. Conclusions

In this work, key parameters in the design and implementation of metallic grids on TCEs for use in large-area OSC devices have been presented. The motivation for producing TCEs with metallic grids is given by the lack of TCE materials that offer a satisfactory R_{sheet} for creating monolithic OSCs at practical sizes. Metallic grids can first be parameterized by their GFF, or fraction unshadowed—this is a compromise between reduced photocurrent resulting from shading and R_{sheet}. GFF alone is not sufficient to predict OSC behavior—grids with finer lateral resolution demonstrate improved scalability. The thickness of the grids must also be optimized to be thick enough to reduce the R_{sheet} of the TCE, but the ability to conformally coat the grid structures with solution-processed layers should also be considered.

In the limit of highly conductive micrometer-scale grid structures, the performance of large-area OSCs approaches that of a small-area device. In this limit, equivalent circuit models can be used to predict the behavior of the large-area device, as there is no significant potential variation across the TCE.

OSC designs incorporating metallic grids should balance device performance with manufacturing costs for commercially relevant technologies to be realized. Various technologies can be considered for the addition of metallic grids and the appropriate techniques must be selected for the manufactured device to be technologically competitive. For R&D purposes, the use of microlithographic patterned metallic grids on glass substrates offers a facile route toward high-performance TCEs. Methods of printing high conductivity metallic grid structures on flexible substrates are similarly an area of strategic research interest in the demonstration of flexible OSC panels. In summary, the use of metal grids in TCEs is a credible route to large-area OSC devices and taken together with the recent demonstration of new material systems, offers a promising route toward large-area organic PV.

5. Experimental Section

Representative Small-Area Organic Solar Cells: Small-area OSCs with 0.04 cm² pixel sizes were fabricated from PBDB-T (poly[(2,6-(4,8-bis(5-(2-ethylhexyl)thiophen-2-yl)benzo[1,2-b:4,5-b']dithiophene)-co-(1,3-di(5-thiophene-2-yl)-5,7-bis(2-ethylhexyl)benzo[1,2-c:4,5-c']dithiophene-4,8-dione)) and the nonfullerene acceptor 3,9-bis(2-methylene-(3-(1,1-dicyanomethylene)-5-methylindanone))-5,5,11,11-tetra(4-hexylphenyl)dithieno[2,3-d:2',3'-d']sindaceno[1,2-b:5,6-b']dithiophene (IT-M), on commercial ITO/glass substrates and were used as representative OSC devices. The device structure was as follows: glass/ITO/TiO₂ (30 nm, spin-coated)/PBDB-T:IT-M (100 nm, spin-coated)/MoO₃(10 nm, thermally evaporated)/Ag(100 nm, thermally evaporated). The JV curves of the devices were measured through a shadow mask using a Newport 3A solar simulator and a Keithley 2612B source meter unit. The simulator was calibrated by a standard silicon reference cell certified by the National Renewable Energy Laboratory.

Representative JV curves were measured in the light and dark, (V_{OC} = 0.915 V, J_{sc} = 16.6 mA cm⁻², FF = 70.5%, PCE = 10.7%) (Figure S6, Supporting Information) and were parameterized using the modified Shockley equation from Neher et al.[45] which was explained above.

Fitting Equation (3) to the measured data gave a value of the dimensionless parameter $\alpha \approx 2.47$, indicating that the currents are strongly transport-limited. This parameterized JV profile is used as a representative OSC material in this work. Predictions of device performance were derived from expressions for FF and normalized V_{OC} from the same work.[45]

Finite Element Simulations: ITO- and MG-OSCs were simulated using the commercially available Large Area Organic Solar Simulator (Fluxim AG) software. The TCE was defined as a 100 nm thick layer of ITO, with additional hexagonal silver grid structures added on top of the ITO layer. Unless otherwise stated, the thickness of the grid structures was 1 µm, the hexagonal radius was 1 mm and the track width was 40 µm, providing a GFF of 0.96 (2 s.f.). OSC devices were modeled as a 2D + 1D + 2D system, with a TCE, photovoltaic layer, and metallic electrode. 1D electrical coupling laws connected the 2D regions, which for this work were parameterized from the light and dark JV characteristics of small area PBDB-T:IT-M devices, discussed previously. Values for the R_{sheet} of ITO = 10 Ω □⁻¹, Ag electrode = 0.159 Ω □⁻¹, unless otherwise stated. The R_{sheet} of the grid was calculated using a corrected R_{sheet} relationship that accounted for different resistivities of deposited metal, so that $R_{sheet} = \frac{\zeta \rho_G}{t_g}$ in the grid regions.

Meshing conditions were chosen to balance between runtime and mesh density due to the increased density required to cover the microgrids. Boundary conditions were setup to replicate a standard busbar setup used to test real devices; with biasing voltage applied to parallel sides on one electrode and between the orthogonal parallel sides on the other electrode. Potential difference sweeps were applied to the TCE between −1 and 1 V, in 0.05 V steps, to generate the JV characteristic for each device. Additionally, the potential contour across the TCE at V_{MPP} was simulated to observe the uniformity in potential distribution. V_{MPP} was quoted by the software after a full potential sweep and the potential contours swept over a 3 mV range, with V_{MPP} in the center

of the sweep. This allowed for higher resolution simulations (using mesh refinement iterations) to be ran in an acceptable time. The high-performance solver settings were chosen in all simulations to reduce simulation runtime and improve the accuracy of results. Finally, the JVs and potential contours allowed comparison between simulations, physical devices, and the equivalent circuit model described in this work.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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