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A Two-Dimension Time-Domain Comparator for Low Power SAR ADCs

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Abstract: This paper presents a two-dimension time-domain comparator suitable for low power successive-approximation register (SAR) analog-to-digital converters (ADCs). The proposed two-dimension time-domain comparator consists of a ring oscillator collapse-based comparator and a counter. The propagation delay of a voltage controlled ring oscillator depends on the input. Thus, the comparator can automatically change the comparison time according to its input difference, which can adjust the power consumption of the comparator dynamically without any control logic. And a counter is utilized to count the cycle needed to finish a comparison when the input difference is small. Thus, the proposed comparator can not only provide the polarity of the input, but also the amount information of the input, which helps to skip most of the SAR cycles when the initial input is small. Thus, most energy can be saved when the initial input is small. The proposed time-domain comparator is designed in 0.18 μm CMOS technology. Simulation results demonstrate that the comparator can not only save power consumption, but also give the design flexibility, and the current is only nA level when the supply voltage is 0.6 V.

Keywords: Time-domain comparator, two dimensions, low power.

1 Introduction

With the development of Internet of Things (IoTs), there are growing demands for power-limited applications, such as wireless sensor networks, RFID systems, wearable devices, biometrics [Verma and Chandrakasan (2007); Su, Sheng, Xie et al. (2019); Chang, Wang and Wang (2007); Su, Sheng, Liu et al. (2019); Lee, Park, Park et al. (2011); Zhu and Liang (2015); Su, Sheng, Leung et al. (2019); Elzakker, Tuijl, Geraedts et al. (2010); Wang, Gu, Liu et al. (2019)]. The analog-to-digital converter (ADC), as a critical block for sensor interface, should meet the stringent power budget in these power limited systems. The successive approximation register (SAR) ADC is the most preferred candidate for those energy-limited applications because of its medium resolution, medium speed, low power,

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low design complexity and friendly technology scaling [Liu, Sheng and Zhu (2016); Chang and Hsieh (2018); Chung, Yen, Tsai et al. (2018); Fu and Pun (2018)].

SAR ADC mainly consists of three blocks: comparator, digital-to-analog converter (DAC) and SAR control logic. In most SAR ADC designs, the comparator is in voltage domain [Hsieh and Hsieh (2018); Liu, Chang, Huang et al. (2010); Wang, Liu, Sheng et al. (2018); Zhu, Qiu, Liu et al. (2015); Ahmadi and Namgoong (2015); Yu, Gao, Liu et al. (2019)]. The power consumption of these voltage domain comparators is determined by the resolution of ADC, and it cannot be adjusted dynamically according to the input difference, which wastes lots of energy when the input signal difference becomes larger. In order to reduce the power consumption, comparator energy scaling techniques have been developed [Lee, Park, Park et al. (2011); Tai, Hu, Chen et al. (2014); Liu (2016)]. Two comparator architecture in Tai et al. [Tai, Hu, Chen et al. (2014); Liu (2016)] uses one comparator for coarse comparisons, and the other for fine comparisons. And time-domain comparators have also been proposed to reduce the power consumption [Lee, Park, Park et al. (2011); Shim, Jeong, Myers et al. (2017)]. However, these techniques complex the design of SAR ADC by extra control logic, which increases the design complexity. The ring oscillator collapse-based comparator in time-domain can achieve automatic energy scaling according to the input difference [Shim, Jeong, Myers et al. (2017)], but the delay cells in the comparator stacked four MOS transistors, which increases the power supply voltage.

This paper proposes a two-dimension time-domain comparator, which can achieve automatic energy scaling according to the input difference. Furthermore, a counter is utilized to detect the edge cycles needed to finish a comparison cycle, which makes the comparator provide additional information. Thus, the comparator can not only provide the polarity of the input, but also the amount of the input difference, which helps to skip most of the SAR cycles when the initial input is small. The rest of the paper is organized as follows. Section 2 presents the structure and operation principle of the proposed comparator. Section 3 analyzes the performance of the comparator. Simulation results are given in Section 4. And Section 5 concludes this paper.

2 Structure and operation principle of the proposed comparator

Fig. 1 shows the structure of the two-dimension time-domain comparator, which consists of inverter delay cells, two NAND gates and a counter. Each delay cell has two inverters, and each inverter has one input voltage: one is PMOS input and the other is NMOS input. Compared with the comparator in Shim et al. [Shim, Jeong, Myers, et al. (2017)], the proposed delay cell can achieve a lower supply voltage, which helps to reduce the power consumption. The operation principle is illustrated in Fig. 2. As the counter does not influence the oscillation of the inverter loop, the counter is omitted in Fig. 2 for simplification. As shown in Fig. 2(a), when the start signal ST is low, the comparator is in a reset state, the output OUT is logic high, and the number of CNT is zero. The oscillation loop is in a disabled state. When ST goes from low to high, the comparator starts to work. As Fig. 2(b) shows, NAND gates A and B will produce a rising edge, the outputs of the NAND gates will be a falling edge, and these two falling edges will propagate through delay cells. Supposing Vip>Vin, the edge originating from NAND gate A travels faster than the edge of NAND gate B. When the edge of gate A catches up with the edge of gate

B, the oscillation of the inverter loop will stop, and the comparison is finished. As Vip is larger than Vin, OUT is high when the comparison is finished. Otherwise, OUT is low.

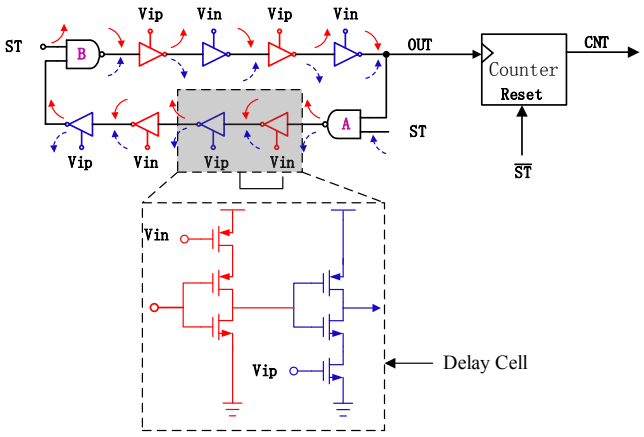

Figure 1: Schematic of the proposed comparator

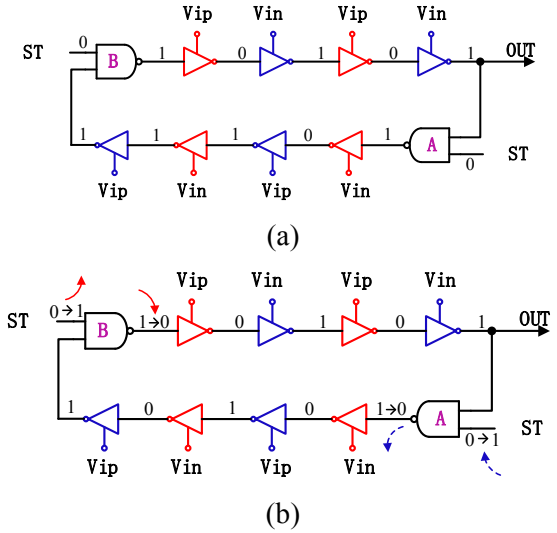

Figure 2: Operation principle of the comparator. (a) Reset state. (b) Comparison state

When Vip is larger than Vin, the comparison result OUT is a high level, and the oscillation cycle depends on the input difference. If Vip is larger than Vin with a large amount, the edge coming from NAND B propagates much faster than that of NAND A, and the comparison will finish in a short time as shown in Fig. 3(a). When Vip is only a little larger than Vin, then the edge coming from NAND B travels at a speed very close to that of NAND A, and it will take a long time to finish the comparison as Fig. 3(b) illustrates. In this case, the cycles needed are larger than those in Fig. 3(a), and the number CNT of the counter is larger than that of Fig. 3(a). When Vip is smaller than Vin,

OUT will be low. Thus, the comparison time depends on the input difference, which can be regarded as the energy consumption during a comparison cycle that can automatically adjust according to the input difference. The number CNT of the counter can indicate the amount of the input difference, which gives additional information of the comparator.

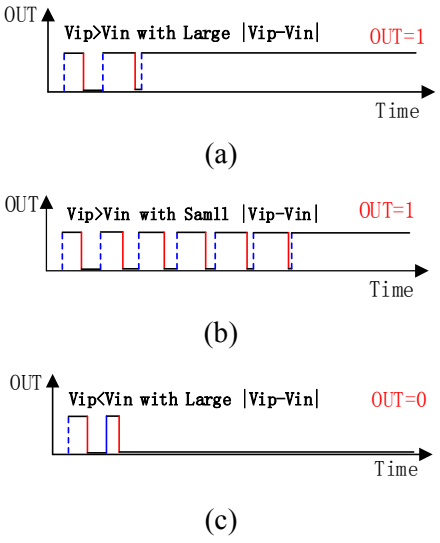

Figure 3: Comparison result *vs.* time. (a) Vip>Vin with a large amount of the input difference. (b) Vin>Vin with a small amount of the input difference. (c) Vip<Vin with a large amount of the input difference

3 Analysis of the comparator performance

3.1 Comparison time and power consumption

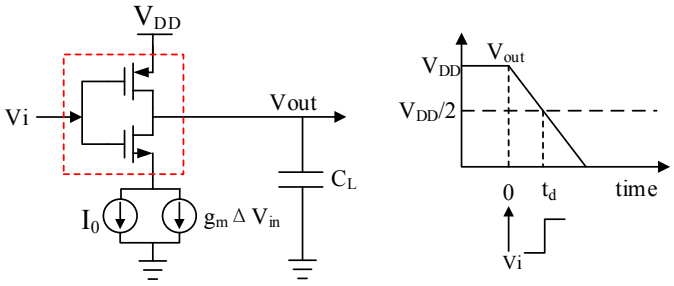

Figure 4: Simplified model of the unit delay stage

As shown in Fig. 2, the inverter loop consists of the inverter cell with alternated NMOS-gated and PMOS-gated current starved delay cells. For simplicity, the inverter loop can be modeled as a chain of multiple identical units NMOS-gated current starved delay cell. Fig. 4 shows the model of the unit delay cell with defined parameters. Assuming the load of each inverter cell is much larger than parasitic capacitors of MOS transistors, the delay of NAND gates in Fig. 2 and noise of MOS transistors with a red line in Fig. 4 can be

neglected. Then the unit delay cell can be modeled as a switch with a threshold of $V_{DD}/2$. When the input of the inverter goes from low to high, the output V_{out} starts to discharge through the current source controlled by one of the differential inputs. Assuming the input difference voltage is ΔV_{in}, the time needed to discharge V_{out} to $V_{DD}/2$ can be expressed as

$$t_d = \frac{C_L V_{DD}}{2I_0}, \tag{1}$$

where I_0 denotes the current when ΔV_{in} equals to 0, C_L is the load capacitance. The time delay between the two edges originating from NAND gates A and B can be written as

$$\begin{aligned} \Delta t_d &= \frac{C_L V_{DD}}{2}\left(\frac{1}{I_0 - g_m \Delta V_{in}/2} - \frac{1}{I_0 + g_m \Delta V_{in}/2}\right) \\ &\cong \frac{C_L V_{DD}}{2I_0^{\,2}} g_m \Delta V_{in}, \end{aligned} \tag{2}$$

where g_m is the small-signal transconductance of the transistor when the bias voltage is around $V_{DD}/2$. Then the gain of voltage to time conversion of N stages is

$$Gain\_N = N \cdot \frac{t_d}{\Delta V_{in}} = \frac{NC_L V_{DD}}{2I_0^{\,2}} g_m. \tag{3}$$

And the propagation delay of each edge can be expressed as (Vip>Vin)

$$\begin{aligned} t_A &= \frac{C_L V_{DD}}{2}\left(\frac{1}{I_0 - g_m \Delta V_{in}/2}\right) \\ t_B &= \frac{C_L V_{DD}}{2}\left(\frac{1}{I_0 + g_m \Delta V_{in}/2}\right) \end{aligned} \tag{4}$$

where t_A and t_B are the propagation delay of each unit delay cell. As shown in Fig. 2, the working principle can be regarded as two edges coming from NAND gates A and B chase each other. When the edge with faster propagating speed catches up with the lower one, the comparison is finished. Thus, the time of a comparison cycle can be considered as a chase problem. Assuming there are N unit delay cells in the inverter loop, the initial distance of these two edges is N/2 (neglecting the delay of two NAND gates), and the comparison time t_{comp} approximately satisfies

$$\frac{t_{comp}}{t_A} + \frac{N}{2} = \frac{t_{comp}}{t_B}. \tag{5}$$

Substituting Eq. (4) into Eq. (5)

$$t_{comp} = \frac{NV_{DD}C_L}{4g_m \Delta V_{in}}. \tag{6}$$

And the cycles the counter detected can be expressed as

$$CNT = \frac{t_{comp}}{N \cdot t_A} = \left\lfloor \frac{I_0}{2g_m \Delta V_{in}} - \frac{1}{4} \right\rfloor. \tag{7}$$

The amount of the input difference is reflected by CNT. Thus, the comparator can not only provide the polarity information of the inputs but also the amount of the input difference. The average current of the unit delay cell drawn from V_{DD} is I_0, the power consumption for a comparison cycle is

$$P = 2V_{DD} I_0 t_{comp} = \frac{I_0 N V_{DD}^2 C_L}{2g_m \Delta V_{in}}. \tag{8}$$

3.2 Noise analysis

The noise of the comparator can be analyzed using the noise model shown in Fig. 5. The MOS transistor can be modeled as a parallel current source with a power of i_n^2. The noise current will cause Gaussian distribution on t_d with a standard deviation of $\overline{\Delta t_d}$. The output noise power $\overline{\Delta V_{out}^2}$ can be expressed as Lee et al. [Lee, Park, Park et al. (2011)]

$$\overline{\Delta V_{out}^2} = \frac{g_m r_o \gamma kT}{C_L}, \tag{9}$$

where r_o is the output resistance, and γ the noise factor, k is the Boltzmann constant, T is the absolute temperature. The delay fluctuation $\overline{\Delta t_d}$ due to the noise can be expressed as

$$\overline{\Delta t_d} = \frac{\overline{\Delta V_{out}}}{Slew\ rate} = \frac{t_d}{V_{DD}/2} \cdot \overline{\Delta V_{out}} = \frac{C_L}{I_0} \cdot \overline{\Delta V_{out}}. \tag{10}$$

By substituting Eq. (9) into Eq. (10),

$$\overline{\Delta t_d} = \sqrt{C_L} \frac{\sqrt{g_m r_o \gamma kT}}{I_0}. \tag{11}$$

Since the comparator output accumulates the noise effect of every delay stage, which are statistically independent, the standard deviation of time error of the whole comparator $\overline{\Delta t_{d\_N}}$ can be derived as

$$\overline{\Delta t_{d\_N}} = \sqrt{N \cdot C_L} \cdot \frac{\sqrt{g_m r_o \gamma kT}}{I_0}. \tag{12}$$

By substituting Eq. (12) to Eq. (3), the input voltage noise can be derived

$$\overline{V_{input\_noise}} = \frac{2I_0 \sqrt{g_m r_o \gamma kT}}{V_{DD} g_m \sqrt{NC_L}}. \tag{13}$$

From Eq. (13), the input-referred noise can be adjusted by N and C_L, which make the design more flexible.

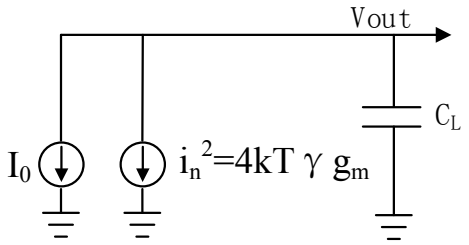

Figure 5: Noise model of the unit delay cell

3.2 Offset voltage analysis

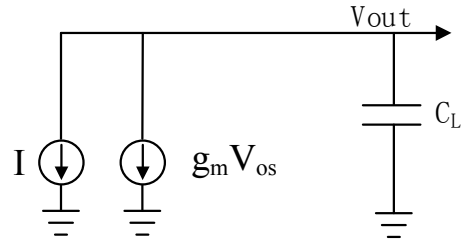

Figure 6: Model of the unit delay cell with an input-referred offset voltage

Fig. 6 shows the unit delay cell model of an input-referred offset voltage. According to Eq. (2), the timing error of a unit stage caused by the offset voltage is

$$\Delta t_{offset} = \frac{C_L V_{DD}}{2I_0^{\,2}} g_m V_{os}, \tag{14}$$

where V_{os} is the offset voltage. As each unit cell is independent, the deviation of the offset due to N-stage is

$$\Delta t_{\text{offset\_}N} = \sqrt{N}\,\frac{C_L V_{DD}}{2I_0^{\,2}} g_m V_{os}. \tag{15}$$

Thus, the input offset voltage V_{os_N} can be derived by Eq. (14) and Eq. (15):

$$V_{os\_N} = \frac{V_{os}}{\sqrt{N}}. \tag{16}$$

4 Simulation results

The proposed comparator is designed in 0.18 μm TSMC CMOS technology, and simulations are carried out by Cadence Spectre. The aspect ratio of all PMOS transistors is set to 4 μm/5 μm and that of all NMOS transistors is set to 1 μm/5 μm. The current against input under different VDD is shown in Fig. 7 when 20 delay cells are included in the inverter loop. The power consumption can be adjusted automatically according to the

input voltage difference. During simulations, the input difference is from 1 μV to the corresponding full-scale voltage. The current consumption decreases as the input difference increases when the input difference is small, and the current consumption is well satisfied with the analysis in Section 3 as the model used in the analysis is a small-signal model. When the input difference becomes larger, the circuit should be considered as a large signal mode, and the current consumption increases sharply with the input voltage as can been seen from Fig. 7. The knee points are about tens of mV.

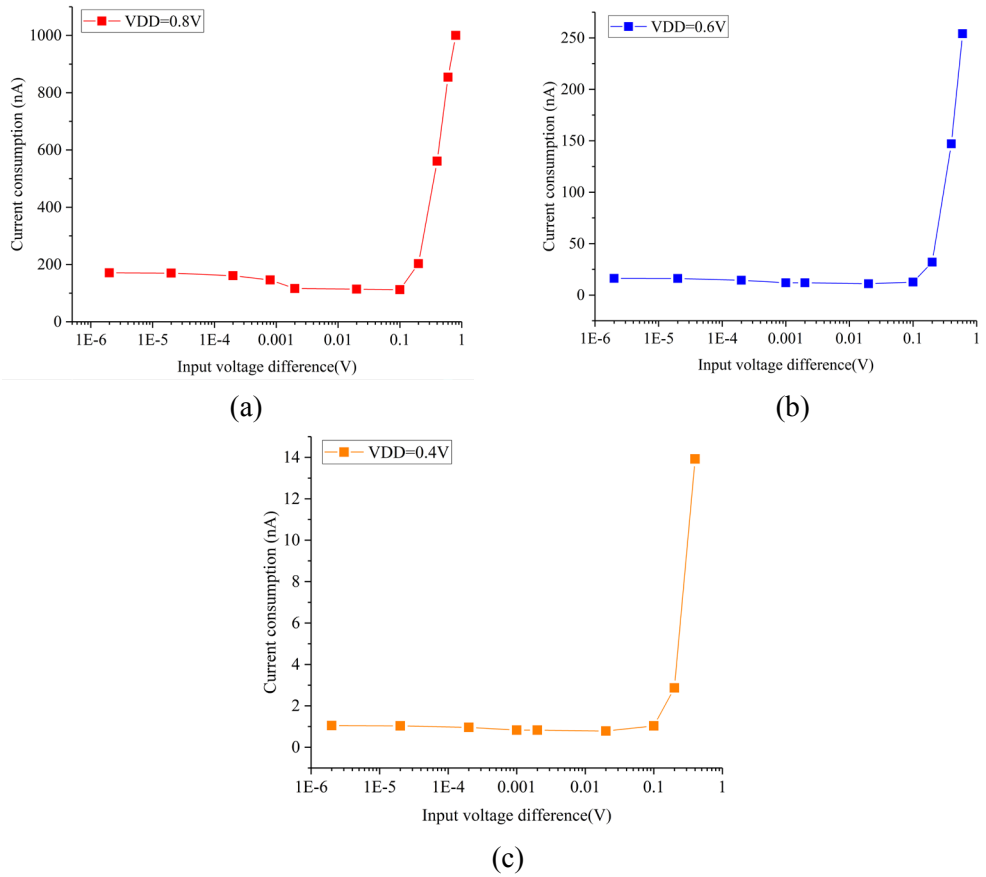

Figure 7: Current against input voltage under different supply voltages: (a) VDD=0.8 V, (b) VDD=0.6 V and (c) VDD=0.4 V

The comparison time against the input voltage is illustrated in Fig. 8. The comparison time decreases when the input voltage becomes larger. This is because when the input voltage difference becomes large, the edge generated from one of the NAND gates propagates much faster than the other one, then the oscillation will collapse more quickly.

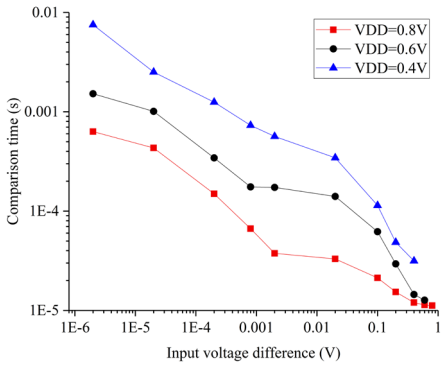

Figure 8: Comparison time against input voltage under different supply voltages

Tab. 1 shows the number CNT of the counter against the input voltage under different VDD when the delay cell stages are 20. When the input voltage is larger than 0.1 mV, the CNT is always 1. And the CNT will change with a certain amount of the input voltage difference. The lower the supply voltage is, the more the CNT changes with the input voltage.

Table 1: CNT under different supply voltage

Input	CNT (Delay cell=20)		
voltage (mV)	VDD=0.4 V	VDD=0.6 V	VDD=0.8 V
>0.1	1	1	1
0.1	2	2	5
0.01	4	6	15
0.001	6	9	22

The impact of delay cells on CNT is also evaluated and simulation results are shown in Tab. 2. It can be seen that the stages of delay cell have an impact on CNT, when more delay cell stages are incorporated, CNT is larger under the same input voltage. Thus, the sensitivity of CNT can be adjusted by the supply voltage and the stages of the delay cell. This characteristic of the comparator enables the ability of detecting week signals.

Table 2: CNT under difference delay cell stages

Input	CNT (VDD = 0.6 V)			
voltage (mV)	8 delay cells	12 delay cells	16 delay cells	20 delay cells
>0.1	1	1	1	1
0.1	2	2	2	2
0.01	3	4	5	6
0.001	3	5	6	9

5 Conclusion

A time-domain comparator is presented in this paper. The comparator consists of a ring-oscillator collapse-based comparator and a counter, which can provide not only the

polarity of the input but also the amount of the input difference. And the power consumption of the comparator can be adjusted automatically according to the input, which saves the power consumption when applied to SAR ADC. Designed in 0.18 μm CMOS technology, the current consumption of a comparison cycle is at the nA level when the supply voltage is 0.6 V.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

References

Ahmadi, M.; Namgoong, W. (2015): Comparator power minimization analysis for SAR ADC using multiple comparators. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 10, pp. 2369-2379.

Chang, K. H.; Hsieh, C. C. (2018): A 12-bit 150-MS/s sub-radix-3 SAR ADC with switching miller capacitance reduction. *IEEE Journal of Solid-State Circuits*, vol. 53, no. 6, pp. 1755-1764.

Chang, Y. K.; Wang, C. S.; Wang, C. K. (2007): A 8-bit 500-KS/s low power SAR ADC for bio-medical applications. *IEEE Asian Solid-State Circuits Conference*, pp. 228-231.

Chung, Y. H.; Yen, C. W.; Tsai, P. K.; Chen, B. W. (2018): A 12-bit 40-MS/s SAR ADC with a fast-binary-window DAC switching scheme. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 1989-1998.

Elzakker, M. V.; Tuijl, E. V.; Geraedts, P.; Schinkel, D.; Klumperink, E. A. M. et al. (2010): A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s. *IEEE Journal of Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1015.

Fu, Z.; Pun, K. P. (2018): An SAR ADC switching scheme with MSB prediction for a wide input range and reduced reference voltage. *IEEE Transactions on Very Large Scale Integration Systems*, vol. 26, no. 12, pp. 2863-2872.

Hsieh, S. E.; Hsieh, C. C. (2018): A 0.44-fJ/conversion-step 11-bit 600-kS/s SAR ADC with semi-resting DAC. *IEEE Journal of Solid-State Circuits*, vol. 53, no. 9, pp. 2595-2603.

Lee, S. K.; Park, S. J.; Park, H. J.; Sim, J. Y. (2011): A 21 fJ/conversion-step 100 kS/s 10-bit ADC with a low-noise time-domain comparator for low-power sensor interface. *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 651-659.

Liu, C. C. (2016): A 0.35mW 12b 100MS/s SAR-assisted digital slope ADC in 28nm CMOS. *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 462-463.

Liu, C. C.; Chang, S. J.; Huang, G. Y.; Lin, Y. Z. (2010): A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure. *IEEE Journal of Solid-State Circuits*, vol. 45, no. 4, pp. 731-740.

Liu, S.; Shen, Y.; Zhu, Z. (2016): A 12-bit 10 MS/s SAR ADC with high linearity and energy-efficient switching. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 10, pp. 1616-1627.

Shim, M.; Jeong, S.; Myers, P. D.; Bang, S.; Shen, J. et al. (2017): Edge-pursuit comparator: an energy-scalable oscillator collapse-based comparator with application in a 74.1 dB SNDR and 20 kS/s 15 b SAR ADC. *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1077-1090.

Su, J.; Sheng, Z.; Leung, V. C. M.; Chen, Y. (2019): Energy efficient tag identification algorithms for RFID: survey, motivation and new design. *IEEE Wireless Communications*, vol. 26, no. 3, pp. 118-124.

Su, J.; Sheng, Z.; Liu, A.; Han, Y.; Chen, Y. (2019): A group-based binary splitting algorithm for UHF RFID anti-collision systems. *IEEE Transactions on Communications*, pp. 1-14.

Su, J.; Sheng, Z.; Xie, L.; Li, G.; Liu, A. (2019): Fast splitting based tag identification algorithm for anti-collsion in UHF RFID system. *IEEE Transactions on Communications*, vol. 67, no. 3, pp. 2527-2538.

Tai, H. Y.; Hu, Y. S.; Chen, H. W.; Chen, H. S. (2014): A 0.85fJ/conversionstep 10b 200kS/s subranging SAR ADC in 40nm CMOS. *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 198-199.

Verma, N.; Chandrakasan, A. P. (2007): An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes. *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1196-1205.

Wang, J.; Gu, X. J.; Liu, W.; Sangaiah, A. K.; Kim, H. J. (2019): An empower hamilton loop based data collection algorithm with mobile agent for WSNs. *Human-Centric Computing and Information Sciences*, vol. 9, no. 1, pp. 1-14.

Wang, J.; Liu, S.; Shen, Y.; Zhu, Z. (2018): Low-power single-ended SAR ADC using symmetrical DAC switching for image sensors with passive CDS and PGA technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 8, pp. 2378-2388.

Yu, F.; Gao, L.; Liu, L.; Qian, S.; Cai, S. et al. (2019): A 1 V, 0.53 ns, 59 μW current comparator using standard 0.18 μm CMOS technology. *Wireless Personal Communications*, vol. 111, pp. 843-851.

Zhu, Z.; Liang, Y. (2015): A 0.6-V 38-nW 9.4-ENOB 20-kS/s SAR ADC in 0.18-μm CMOS for medical implant devices. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2167-2176.

Zhu, Z.; Qiu, Z.; Liu, M.; Ding, R. (2015): A 6-to-10-bit 0.5V-to-0.9V reconfigurable 2MS/s power scalable SAR ADC in 0.18μm CMOS. *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 689-696.