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Developing A Medium-Voltage Three-Phase Current Compensator Using Modular Switching Positions

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Developing A Medium-Voltage Three-Phase Current Compensator Using Modular Switching Positions

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by

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ABSTRACT

The objective of this thesis is to present the context, application, theory, design, construction, and testing of a proposed solution to unbalanced current loading on three-phase four-wire systems. This solution, known as the Medium-Voltage Unbalanced Current Static Compensator or MV-UCSC, is designed to recirculate currents between the three phases of a distribution system. Through this redistribution of the currents negative- and zero-sequence current components are eliminated and a balanced load is seen upstream from the point of installation. The MV-UCSC as it operates in the distribution system is presented followed by its effect on traditional compensation equipment. The construction of the MV-UCSC as well as 13.8 kV simulations are then shown. Development of the switching positions required by the MV-UCSC is then given followed by a variation on this switching position with the intent to reduce part count. Finally, the testing the 13.8 kV three-phase four-wire, neutral-point-clamped, eleven-level, flying-capacitor-based MV-UCSC connected directly to the grid is presented.

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF PUBLICATIONS

Chapter 2 V. Jones, J. C. Balda, and R. Adapa, "Current Compensators for Unbalanced Electric Distribution Systems," in 2018 IEEE Electronic Power Grid (eGrid), 2018, pp. 1-6.
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Chapter 3 V. Jones and J. C. Balda, "The Impact of a Current Imbalance Compensator on Feeder Compensation Equipment Operation," in 2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2020, pp. 463-469.
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CHAPTER 1

INTRODUCTION

1.1 Unbalanced Currents in Distribution Systems: The Problem and Motivation

An electric power transmission system normally consists of three phases and three-wires or conductors, but it becomes a four-wire one in the United States once the voltage is stepped down to voltages at the distribution system level. Though some of the customers in distribution systems utilize three-phase power, this is not economical for the vast majority of a given utility's service area. As a result single-phase feeders are used to service residential areas [1]. Single-phase loading leads to an inherent imbalance in the three-phase currents. The imbalances can cause several issues including overheating of neutral conductors, increased losses in generators, torque ripples in electric machines and excessive losses in the holding tank for ungrounded wye-connected transformers [2-7]. The entire system may also see a drop in efficiency [8, 9]. Recently, the use of rooftop solar panels in some areas has exacerbated current imbalances [10, 11].

Traditionally, utilities use balanced three-phase fixed and switched capacitor banks to compensate for this. These capacitor banks are sold in standard reactive power units normally 50 or 100 producing kVAR increments per phase for the distribution system. Imbalances can also make compensating for the power factor at the head of a feeder more difficult since not all phases would have the same power factor. Thus, the ability of the utility to adjust unbalanced reactive currents more closely and thus achieve an appropriate power factor is reduced.

The seasonality of loads can also play a role in this. For example, a tourist location supplied with a largely underground distribution feeder could experience overcompensation of the power factor in the off-season due to the increased capacitances of underground systems.

Overcompensation to a leading power factor can cause over-voltages on the distribution feeder. The utility then might have to also install shunt reactors seasonally to fix this issue [1].

Additionally, the use of non-linear power-electronics-based front-end converters on many loads can contribute to harmonic distortion in the currents drawn from the grid [10]. These currents drawn through the upstream impedances cause harmonic voltage distortions along the feeder, contribute to additional losses, and can cause overheating of fixed and switched capacitor banks because of their relatively low impedance at the harmonic frequencies.

Hence major problems associated with distribution feeders described above are:

- Load current imbalances,
- Voltage Regulation,
- Power factor correction, and
- Current harmonics.

1.2 Existing Current Compensation Solutions

The predominant distribution system configuration in the United States, the region of interest, is a three-phase four-wire system, so the focus of the considered solutions are for such a system. Existing solutions and their benefits are presented next.

1.2.1 Passive Solutions

Passives are cheap and simple to use relative to active solutions. As mentioned above, capacitor banks can correct for lagging power factors and adjust to increases in load or under-voltage conditions, but they are limited by the coarse nature of their taps. They also provide some decoupling of the upstream system from the downstream load harmonics; however, they

are normally not designed for this function. Additionally, these may induce additional system resonances and do not compensate for load imbalances [1].

Among passive solutions that compensate for unbalanced currents is the zig-zag transformer [12]. Through a modified winding configuration, this three-phase transformer is connected between each of the phases and the neutral wire. This transformer presents high-impedance to differential phase currents but presents very little impedance to common-mode currents. In the context of three-phase current component theory, the common-mode currents are equivalent to the zero-sequence currents or the currents in the neutral conductor. By providing a low-impedance current path for the zero-sequence components the magnitude of these currents seen upstream from the zig-zag transformer is reduced. This can reduce the imbalances seen at the head of the feeder. The drawbacks with this method are the need for another large, and potentially custom, line-frequency transformer and the need to be installed near the load, reducing the amount of load for which any one zig-zag transformer can compensate.

1.2.2 Active Solutions

Active solutions based on power electronics and closed-loop control tend to be more expensive and more complex, but these solutions provide improved performance and functionality over the passives-based solutions. A first step towards an active solution would be thyristor-switched reactor and capacitor banks [13]. By controlling the firing angle of a thyristor, the current through a shunt-connected network of reactive components can be controlled and the equivalent power factor of the load can be compensated. The control for this type of compensator is relatively simple and it can be effective, but it also can produce significant harmonic currents and does not compensate for unbalanced currents. An example of this converter is in Figure 1-1.

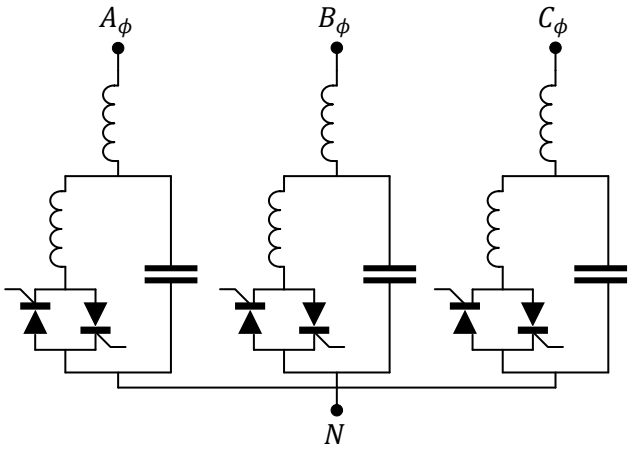


Figure 1-1. Thyristor-switched inductor and capacitor bank.

Voltage-Source Converters (VSCs)

Three-phase, three-leg converters can compensate for power factor, negative-sequence current, and non-zero-sequence harmonics [14]. These can be used to keep the power factor at a desired value under any loading (within their power rating). This allows the converter to act as a switched capacitor bank with very small kVAr steps. However, the disadvantage with this topology is the inability to compensate for zero-sequence currents and thus cannot compensate for all the load current imbalances. A diagram of the converter is displayed in Figure 1-2.

Three single-phase converters that share the same dc bus can be used to compensate for all the above problems. This setup requires the use of a full-bridge converter for each phase. The drawback with this topology is the requirement of single-phase transformers for interfacing with the load due to the need for three separate neutral wire connections. This converter is given in Figure 1-3.

A three-phase four-wire converter with a neutral point clamped (NPC) dc bus can compensate for all unbalanced load currents, power factor, and all harmonics [15]. However, the dc-bus voltage for this converter is 15% higher than those for three-phase three-wire and three

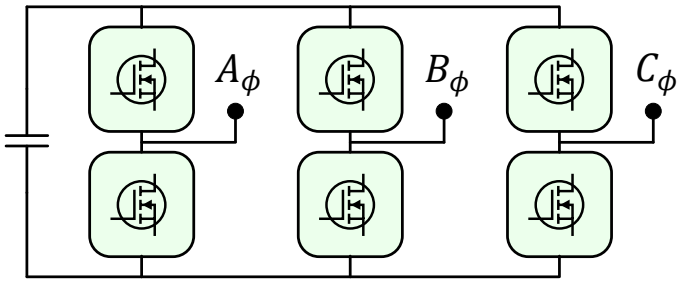


Figure 1-2. Three-phase three-wire converter

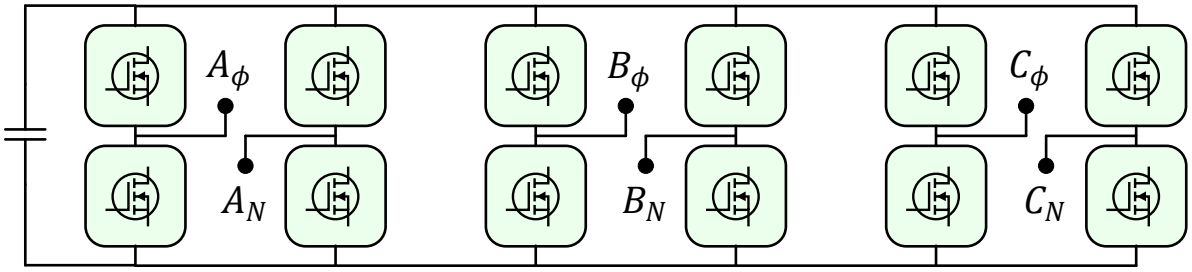
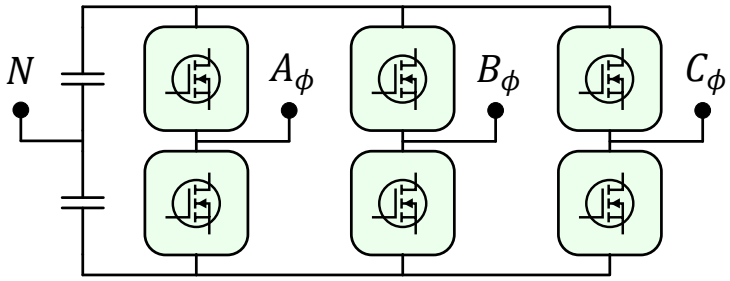


Figure 1-3. Three single-phase converters

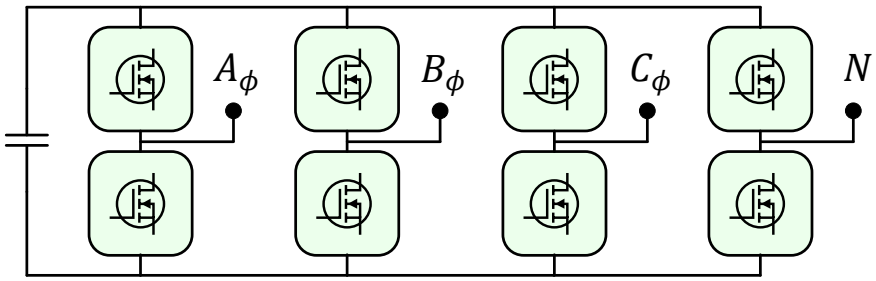
single-phase converters for the same grid voltage, and thus it may require higher rated semiconductor devices. There is the potential to reduce the required dc-bus voltage by utilizing more complex modulation techniques and a four-leg variant of this converter. Though the voltage stress may be reduced, this variant requires more semiconductor devices. Both converter types are shown in Figure 1-4. A summary of all the above solutions is given in Table 1-1.

Direct Connection to Distribution Systems

Usually a shunt active compensator at distribution system level voltages would be rated for lower voltages (e.g., 480 V) and a step-up transformer would interface with the feeder [16-18]. This requirement remains a barrier for the use of these converters because of their ease-of-use can be diminished by the need for a transformer. Also, though relatively uncostly, line-frequency transformers require a significant amount of space, which can affect the deployment of these equipment along the distribution feeder. Active compensators connected directly to



(a)



(b)

Figure 1-4. Three-phase four-wire (a) neutral point clamped (b) four-leg converter.

Table 1-1. Summary of common current compensation solutions

Solution	**Power Factor Compensation**	**Negative-Sequence Current Compensation**	**Zero-Sequence Current Compensation**	**Harmonic Current Compensation**
Passive Solutions				
Shunt Capacitors	✓	×	×	✓[1]
Zig-zag Transformer	×	×	✓	✓[2]
Active Solutions				
Thyristor Switched Inductor and Capacitor	✓	×	×	×
3-leg VSC	✓	✓	×	✓
6-leg VSC	✓	✓	✓	✓
3-leg NPC VSC	✓	✓	✓	✓
4-leg VSC	✓	✓	✓	✓

✓ indicates that the solution has the ability
× indicates that the solution does not have the ability
[1] not normally intended for this purpose
[2] can only compensate zero-sequence harmonic components

medium voltages have the potential to occupy less space and distribution system planners may use them more easily as with other equipment (e.g., shunt capacitors, voltage regulators).

Multilevel Converters

Multilevel converters have been suggested to achieve higher effective output voltages from the use of relatively low-voltage rated devices [19]. The breakdown voltages of semiconductor devices for high-voltage applications are reaching near 15 kV but the commercially available devices remain under 3.3 kV. Through special configurations of the low-voltage devices, these converters can achieve higher voltages by stacking these devices to form different "levels." There are many topologies available for active power exchange with the grid [19]. The three main topologies to consider are: The Diode-Clamped Multilevel Converter (DCMC), the Modular Multilevel Converter (MMC), and the Flying-Capacitor Multilevel Converter (FCMC).

The DCMC has the main advantage over the other two in that it does not require additional passives when adding levels to the converter. The main disadvantage is that the number of diodes increases exponentially with the number of required levels and the conduction losses can increase drastically as a result [20].

The MMC's main advantage is its modularity, lending itself to greater serviceability of the converter and can increase its reliability [21]. The main disadvantages are the number and size of the required capacitive components [22].

The FCMC has the main advantage of size reduction since the required capacitive energy storage is inversely proportional to the switching frequency [23, 24]. When compared to the MMC, which has a required energy storage inversely proportional to the line frequency, the FCMC has an obvious advantage. Like the MMC, this converter does not require the use of any

additional semiconductor devices and does not require any additional inductors. The main disadvantage of the FCMC is the complexity. The levels of the flying capacitor are not completely modular and balancing of the different capacitor levels may require additional control [25-33]. Five-level examples of these three converters in NPC configurations are shown in Figure 1-5.

1.3 Challenges of Multilevel Converters

As the voltage produced by the converter increases some challenges can arise such as an increase in isolation and dv/dt immunity requirements [34-36]. When employing higher voltages in a converter, clearance and creepage distances must be increased at all levels of the design [37]. These issues together can increase the size of the converter. The use of isolation materials with high-voltage withstand capability must be used. This leads to the second potential result of these challenges, higher cost. In addition to the higher price of high-performance materials, custom power supply circuit configurations that can withstand the required voltage ratings in addition to the required dv/dt's must be used, which increases the cost. Even with the choice of more robust materials and topologies, the dv/dt experienced across an isolation barrier can still contribute to the degradation of the isolating material, resulting in a third challenge, reliability of the converter.

One area of particular concern where all these challenges converge are the power supplies for supplying power to the converter switching positions. Parasitic currents due to the switching behavior of the power semiconductor devices can, unless mitigated, flow through the parasitic capacitances of the power supply, gate driver ICs, and other isolating chips. These current transients have the ability to degrade the small digital-level signals and cause false

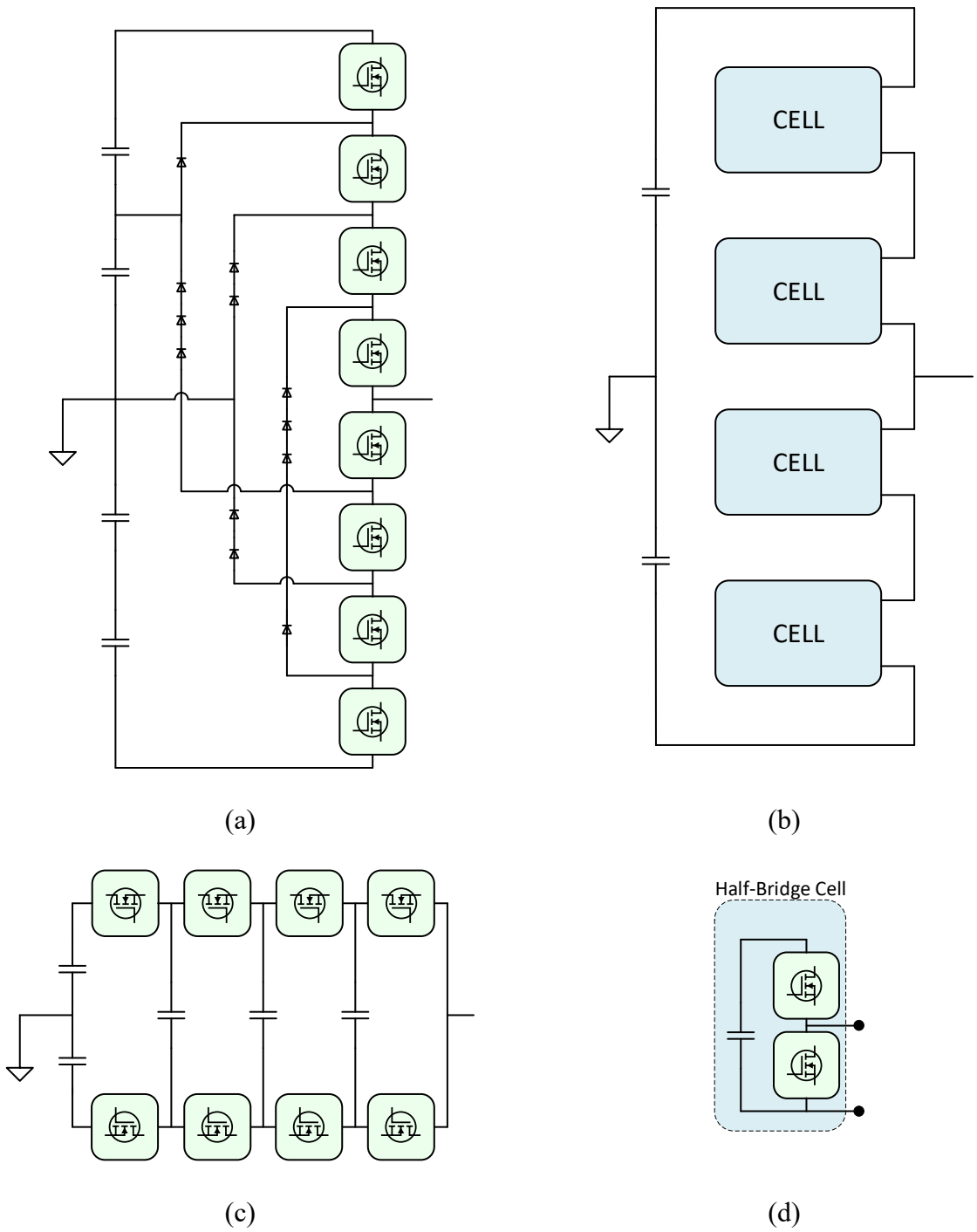


Figure 1-5. Main multilevel converter types: (a) DCMC (b) MMC (c) FCMC (d) MMC cell

triggering of digital logic or corruption of analog measurements [34]. These issues can lead to unwanted turn-ON of power semiconductor devices or drive undesired controller behavior in the converter. For the voltage isolation requirement of ±12 kV_{dc} and 7.9 kV_{ac} and a dv/dt withstand

requirement of 100-150 kV/µs required by this project commercially available "off-the-shelf" power supplies are often not available. Table 1-2 shows some commercially available supplies that target high-voltage applications.

As previously mentioned, the commercial availability of semiconductor devices with appropriate breakdown voltage ratings decreases as the required breakdown voltage increases. Equipment manufacturers then assume a much larger risk in their supply chain when attempting to use higher voltage rating devices. A solution is using several low-voltage semiconductor devices connected in series to form a switching position with a higher effective breakdown voltage [38-40]. This type of scheme increases the complexity of each switching position in the converter but decreases the complexity of the converter topology [38-51].

1.4 Proposed Solution for Unbalanced Current Static Compensation

A current compensator is suggested in this dissertation in the interest of alleviating the current imbalances experienced on distribution feeders. The following logic is used to derive an appropriate solution:

Table 1-2 Commercially available power supplies

Part Number/Series	Manufacturer	Isolation Voltage Rating	Coupling Capacitance
RHV3	Recom	12.5 kV_{ac}, 20 kV_{dc}	3.5 pF (4.0 pF max.)
ISO5125I-120	Power Integrations	12.5 kV_{pk}	4.0 pF
REC6	Recom	5 kV_{ac}, 10 kV_{dc}	20.0 pF
DCHBA1-XXXXH8	Wall Industries, Inc	8 kV_{dc}	10.0 pF
30EFL	HVP	30 kV_{dc}	40.0 pF max.
PWR	Murata	4 kV_{dc}, 8 kV_{pk}	10.0 pF
XE1000	AEB Sapphire	15 kV_{dc}, 10 kV_{ac}	-
SW25-25G	Siebel Elektronik GmbH	25kV_{ac}	10 pF

- An active solution utilizing high-speed power semiconductor devices must be chosen for current compensation due to the enhanced functions and versatility compared to passive or hybrid solutions.
- A three-phase four-wire converter is required because of the applicability to unbalanced distribution systems in the United States.
- Eliminate the use of a step-up transformer to reduce a barrier to adoption by the electric utilities. Thus, connecting directly to the distribution system voltages requires the use of a multilevel converter.
- Solve the set of challenges, particularly with the availability of high-voltage semiconductor devices and the power supplies that can be used to drive them, that come with multilevel converters based on fast-switching semiconductor devices.

With all of this in mind, the solution chosen for this paper is a Medium-Voltage Unbalanced Current Static Compensator (MV-UCSC) that consists of a 13.8 kV three-phase four-wire, neutral-point-clamped, eleven-level, flying-capacitor converter.

In [52] and [53], FCCs with a high number of levels have been demonstrated at low voltages to produce efficient and compact designs. The use of the flying capacitor converter at medium-voltages has not been shown. Overall, there are very few experimental examples of multilevel medium-voltage converters of any kind in the literature [54, 55].

The MV-UCSC is made from 3.3 kV switching positions by utilizing two modular stackable 1.7 kV switching positions connected in series. These switching positions have self-powering ability, which allows them to provide on-board power to themselves for the gate drives and other auxiliary circuitry from the voltage across the switching position in the OFF state [56-58]. This eliminates the need for an external isolated power supply meeting the isolation and

dv/dt requirements. They also utilize voltage-balancing circuits that allows for series-connection of an arbitrary number of these switching positions to form an effectively higher voltage switching position.

1.5 Objectives of the Dissertation

The objectives of the dissertation are as follows:

1. Provide an overview of the primary functions of the proposed MV-UCSC,
2. Show the effects of adding the MV-UCSC to existing conventional regulating equipment,
3. Describe the construction of the MV-UCSC and its the control algorithms,
4. Present the modular stackable switching positions used in the MV-UCSC,
5. Introduce an enhanced variant of the modular switching position, and
6. Lay out the final testing results from operation of the constructed MV-UCSC prototype at the NCREPT test facility.

1.6 Organization of the Dissertation

The structure of this dissertation comes in three major tiers. The first one addresses the MV-UCSC functionality at the distribution system level. The operation of the MV-UCSC along with some non-obvious applications are provided in Chapter 2. The consequence of a MV-UCSC installation with respect to the function of traditional compensation equipment that is installed at the substation is demonstrated in Chapter 3.

The second tier narrows the focus onto the converter itself as reflected in Chapter 4 where the construction and simulation of the MV-UCSC as a non-ideal system are presented.

The third tier narrows the focus even further to the development of a modular stackable switching position for use within the MV-UCSC. The design theory, simulation, and testing of this modular stackable switching position as well as modification required for its use in half-bridge configurations are presented in Chapter 5. The switching position concept and variation of the switching position in Chapter 5 are given in Chapter 6. All these analyses are experimentally verified in Chapter 7 where the testing results of the proposed MV-UCSC as a grid-connected current compensator utilizing the switching positions from Chapter 5 are shown.

Finally, major conclusions from this work along with suggestions for future work are provided in Chapter 8. Appendices have been included to enable easier recreation of the work described in this dissertation.

1.7 Major Contributions of this Research

The major contributions are the development of a modular stackable switching position and the design and implementation of this modular switching position within a medium-voltage converter. Table 1-3 summarizes the details of each of these contributions.

Table 1-3 Contributions of this research

Modular Switching Position	MV-UCSC with the Switching Position
• Improved a voltage balancing circuit such that it is suitable for half-bridge operation [59]. • Provided a previously non-existent quantitative design methodology for choosing component values for the voltage balancing circuit of series-connected devices [59]. • Reconfigured an existing self-powered circuit to allow for self-powering at any voltage and thus a soft-starting mechanism using a simplified implementation [59]. • Developed a start-up routine for a half-bridge configuration of the modular stackable switching positions by leveraging the proposed soft-start mechanism of the switching position [59].	• Designed and built a 13.8 kV, 11-level NPC FCC (Chapter 4). • Combined two instances of the 1.7 kV switching position in series to form an effective 3.3 kV switching position [59]. • Demonstrated the use of a modular stackable switching positions within a half-bridge configuration (Chapter 7). • Confirmed the operation of custom ride-through, voltage regulating and fault handling of the switching position with the MV-UCSC (Chapter 7). • Connected the MV-UCSC directly to a medium-voltage system with unbalanced loading and confirmed upstream current balancing (Chapter 7).

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CHAPTER 2

CURRENT COMPENSATORS FOR UNBALANCED ELECTRIC DISTRIBUTION SYSTEMS

V. Jones, J. C. Balda and R. Adapa, "Current Compensators for Unbalanced Electric Distribution Systems," *2018 IEEE Electronic Power Grid (eGrid)*, Charleston, SC, 2018, pp. 1-6.

2.1 Abstract

Inherent current imbalances are often present in electric distribution systems due to the increase of single-phase generation in the form of renewables and the existence of single-phase loads. The continued expansion of non-linear load usage is also increasing the levels of harmonics through the power transformers servicing these distribution systems. The issues that arise from these operating conditions are widely known and standard solutions used by utilities are as well. However, they are often bulky and do not provide a level of control or versatility appropriate for these challenges. This paper gives an overview of many of the problems that are faced on distribution systems and how an active shunt compensator may be used to mitigate or eliminate them.

2.2 Introduction

Distribution systems normally operate under certain amount of unbalanced loading, especially for residential systems, due to single-phase loads. The issue is exacerbated by single-phase generation in the form of rooftop solar which has seen significant increase in certain areas. Though large-scale three-phase solar generation remains by and large the majority of solar generation this does not eliminate the unbalanced nature of the loading. The issues associated with the negative- and zero-sequence current resulting from unbalanced loads are well documented [1-6]. For example: overheating of a generator, improper sizing of neutral

conductors, MMF ripples inside the generator due to negative-sequence MMFs and overheating of the holding tank for ungrounded wye-connected transformers. Efficiency of the total system is also adversely affected [7, 8].

One of the most prominent issues is the voltage profile along the feeder. Utilities use load rebalancing, load-tap changers, and reactive FACTS devices to meet voltage standards. At the three-phase feeder level, there is extensive research into techniques that can be used to optimize tap scheduling and the allocation of load among the available feeders, many of which are summarized in [9]. These algorithms are used to optimize a set of variables, not just load distribution, and many do not consider the effects of load imbalance which can greatly affect the analysis [10]. They also rely heavily on the prediction of the loading curve. This can be difficult when trying to design for new load centers, especially in rural areas [11, 12].

FACTS devices are currently used to augment the existing transmission systems; however, the use of power-electronics-based FACTS at the distribution level is still in its infancy. In this paper, the application of a shunt "unbalanced current static compensator" (UCSC) will be evaluated with respect to (1) the issues mentioned above, (2) a modernizing grid with increasing distributed generation, and (3) an expanding interest in a microgrid-based distribution system.

The remainder of this paper is organized as follows: the main and secondary applications of a shunt compensator are presented in sections 2.3 and 2.4, respectively. Simulation results and main implementation challenges for the proposed compensator are given in sections 2.5 and 2.6. Last thoughts are given in section 2.7.

2.3 Primary Applications of a Shunt Compensator

Reliability of service is a crucial criterion because customers expect consistent and limitless power availability. This requires a certain amount of margin between the nominal load and maximum feeder ratings at any given time to allow for contingencies. Unbalanced load currents add another level of complexity to the problem because any optimization effort needs to consider each phase of the feeder separately to achieve the true system-level optimal.

An UCSC installed near a distribution substation is shown in Figure 2-1. In this configuration on a traditional feeder, a shunt compensator can balance the currents seen by the substation, bring unity power factor (leveraging existing shunt capacitor banks), potentially dampen power oscillations during transient events, and compensate for harmonic currents that are produced by non-linear loads [13, 14].

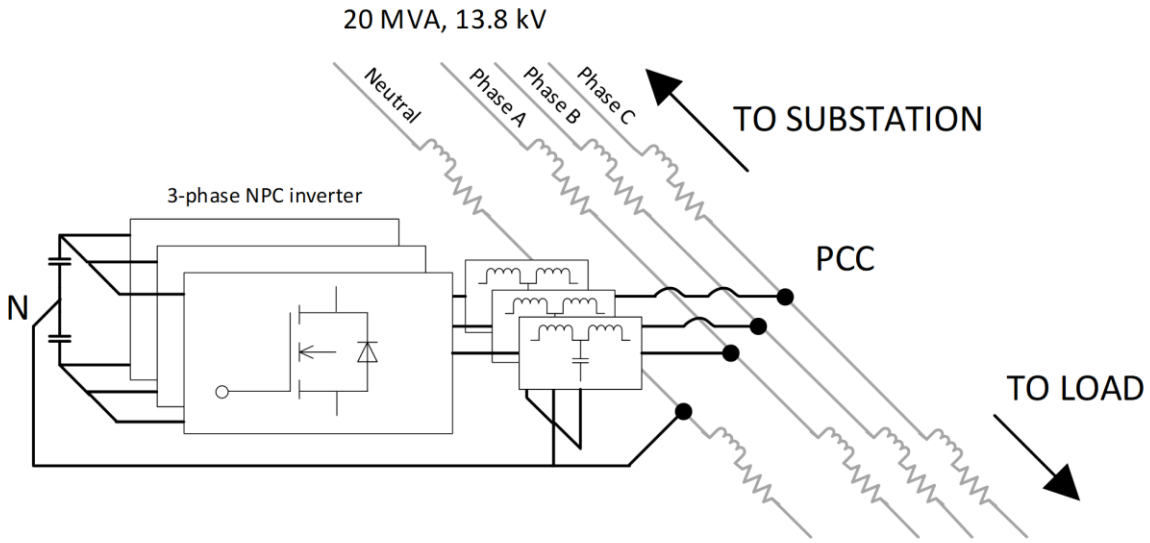

Figure 2-1. Connection of the UCSC to a three-phase feeder.

2.3.1 Current Balancing

When each phase of the feeder is carrying different and varying currents the UCSC can draw additional current from the less loaded phases and circulate that current onto phases that are more heavily loaded. This forces the current seen upstream to the average of the three phases, helping to eliminate any upstream fundamental frequency neutral current. This improves the efficiency of electric machines connected to the grid, can improve the efficiency of the system, and can improve the voltage balance at the point of common coupling by balancing the voltage drop across the upstream impedance [4].

Around 7.7% of billable energy was lost in transmission and distribution systems in the United States in 2016 [15]. Using the average retail price that implies approximately $31.5 billion dollars in lost revenue. Taking a transmission line with equal line resistance and an average current unbalance term, γ, the three-phase currents can be defined as:

$$I_{abc,rms} = \begin{bmatrix} I_{avg}(1+\gamma) \\ I_{avg}(1-\gamma) \\ I_{avg} \end{bmatrix} \quad , \quad 0 \leq \gamma \leq 1 \tag{1}$$

where Iavg is the average RMS current of the phases. The proportional energy loss in the transmission line can be expressed as:

$$E_{3\phi} \propto I_{avg}^2(2\gamma^2 + 3) \tag{2}$$

In Figure 2-2 the lost revenue due to transmission losses is plotted against varying γ for the cases in which transmission line losses amount to 1%, 2%, and 3% of the total billable energy. For the sake of argument, transmission lines were assumed to be operating at a γ of 0.25 for the 7.7% losses quoted above.

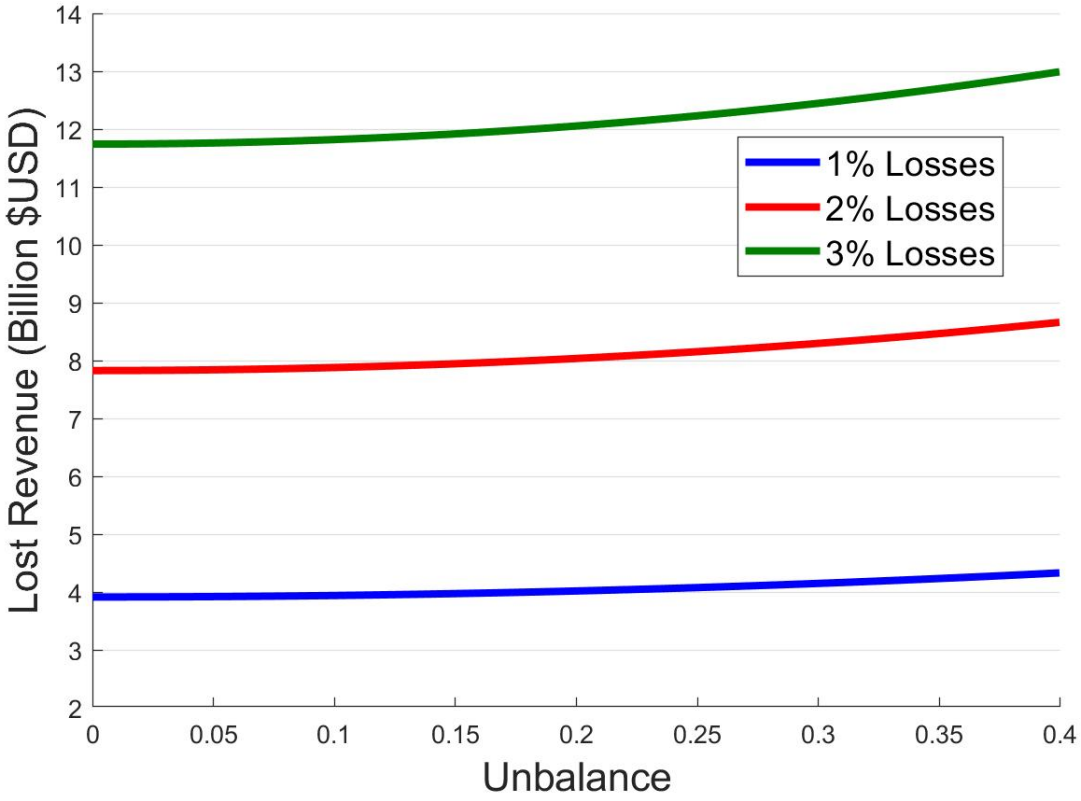

Figure 2-2. Lost revenue due to unbalances.

These calculations are simple averages that do not reflect the varying nature of loading or $/MWh for the electric power grid, but they do reflect the potential savings for utilities that experience unbalanced loading conditions.

2.3.2 Power Factor Regulation

Regulating the power factor to unity helps to improve the total system efficiency by reducing losses accrued in the upstream transmission lines through reactive current reduction. When used in conjunction with relatively cheap and well-known switched shunt capacitor banks the rating of the UCSC can be significantly reduced. While the shunt capacitor banks compensate for most of the reactive power they can only be switched in units of around 50

kVAR per phase [16]. The UCSC can provide nearly infinite steps of reactive power within a smaller range. This

- maintains unity power factor at all operating points,
- reduces potentially the number of operations for the switched capacitor bank and thus, reduces the number transient events from the changing taps in a capacitor bank, and
- can decrease any variations in the voltage profile of the feeder.

This operation could be extended to a fault ride-through type operation where the UCSC remains active and provides VAR support for the grid [17].

2.3.3 Harmonic Compensation

The UCSC can eliminate the voltage distortion that would otherwise propagate back into the transmission system and other feeders by compensating for harmonic currents. Harmonic voltages can overheat shunt capacitors (decreasing their lifetime), cause increased distortion in other grid-connected converters that are not equipped with harmonic voltage compensation [18], and could excite grid resonant frequencies [16]. Harmonics currents can also over-heat power transformers, creating hot-spots and deteriorating the insulation which reduces the lifetime of the transformer [19].

2.4 Secondary Applications of a Shunt Compensator

In addition to the direct benefits discussed above, there are several secondary benefits as listed below:

2.4.1 Complements Load Redistribution Practices

By extending the operating range of the upstream equipment, the conditions for load reconfiguration algorithms are laxed and thus provides more flexibility in the solution. This can help to reduce the number of reconfigurations. Currently, utilities manage current imbalances by first attempting to predict the growth of new loads and selectively add new single-phase loads, and secondly, mitigate any imbalances that occur later by moving single-phase loads to other phases as needed. This type of solution decreases the imbalance of the system but does not provide a fine-tuning of the resulting currents, because it does not account for the intermittency of the loads. The presence of the UCSC can extend the amount of time between load reconfigurations. The UCSC also maintains low neutral current at the substation for any intermittent loads. In addition, there may be instances in which there is a fault on one of the loads and a downstream fuse may open. This could cause a significant change in the loading of any phase resulting in an imbalance for which the utility cannot anticipate.

2.4.2 Inter-feeder Current Sharing

Multiple UCSCs installed at a bus that services several feeders can share a dc-link, providing current redistribution between adjacent substation transformers as in Figure 2-3. In this scenario, the total power available to a feeder is no longer limited absolutely by the rating of the transformer servicing it, but by the combined rating of its UCSC and transformer. Or, to approach the problem from a more practical direction, the stress across a transformer can be reduced from near-peak conditions to help prolong its lifetime [20].

If there is a three-phase fault on Feeder #2 and a large current begins to flow through T2, instead of the UCSC on Feeder #2 deactivating, the linked UCSCs can help to distribute some of the current stress of T2 to T1.

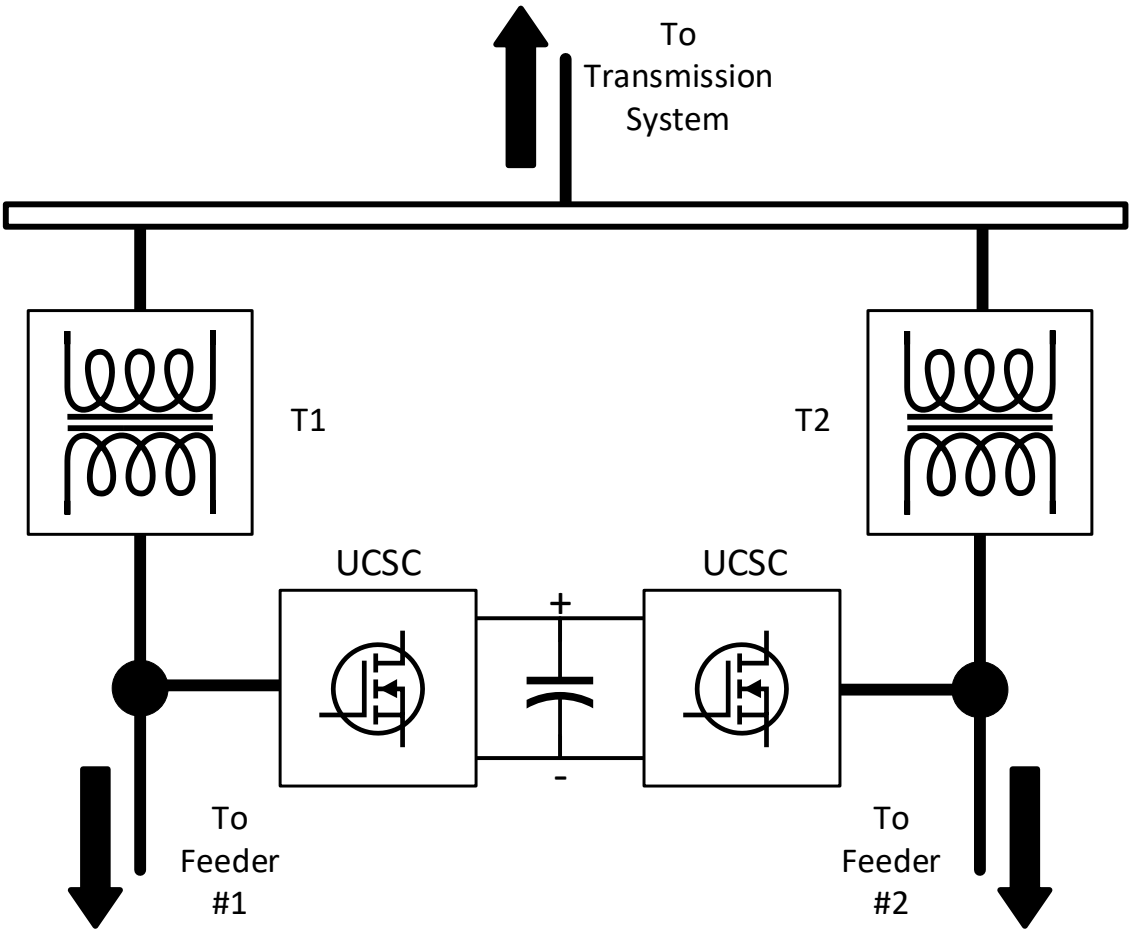

Figure 2-3. DC-link sharing between UCSC on adjacent feeders.

2.4.3 Microgrid Augmentation

In the context of feeders used as microgrids, the UCSC helps to decouple the effects of loads in any one microgrid on the system during grid-connected mode, and in islanded mode the UCSC can operate as a significant STATCOM resource that can help with voltage regulation and sub-synchronous resonances [21]. The compensation capability of the UCSC needs not be limited to the currents directly upstream from the point of installation. Tertiary level controllers for the microgrid can dictate the current references for the UCSC to achieve the goals at other nodes of interest.

2.4.4 Compact Installation

HV SiC devices enable direct connection to the medium voltages of distribution feeders with significantly less complexity. This eliminates the need for low-frequency transformers and the increased achievable switching frequencies allow for a large reduction in passive components in the power-stage of the device. This enhances the modularity of the UCSC and lends itself to the possibility of incrementally adding UCSC resources to new and existing installations as dictated by load growth or changing optimization criterion for the distribution system.

Component volume reduction and elimination of the low-frequency transformer is important for the cost of the converter, but also for the cost of installation. In [16] the cost of new substation installations in 2008 were as low as $36/kW or as high as $110/kW, so being able to eliminate the need for new installations or to be able to pole-mount a FACTS device could remove much of these secondary costs.

2.4.5 Energy Storage and Delivery

Though conceived as an energy circulating device, if the UCSC was connected to energy storage or generation it can, with minor changes to its control criterion, supply energy to the load in addition to its other objectives. In the case of energy storage, the UCSC can be used as a peak-shaving device for high-load conditions by storing energy during times of lower cost. And in the presence of renewables like solar and wind this can be used to control the intermittency of loads seen upstream from the point of installation [22].

2.5 UCSC Simulation Results

The abilities of the UCSC to balance currents and compensate for power factor are demonstrated Figure 2-4 using the control strategy presented in [23] with the UCSC connected

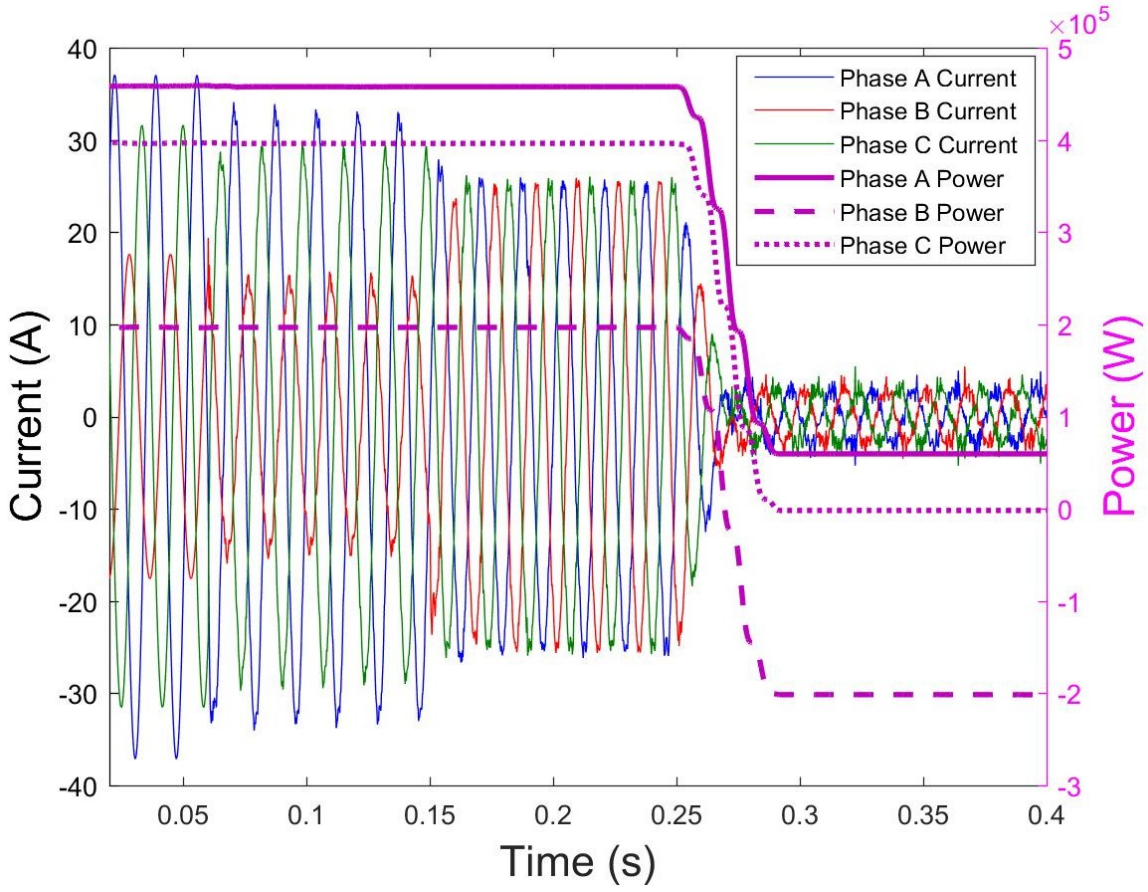

Figure 2-4. Substation currents and real power demand during UCSC and solar farm operation.

directly to a 13.8 kV feeder just downstream from a substation. At t = 0.05 s the UCSC starts to compensate for the reactive component of the load and the current magnitudes reduce accordingly. The power factor is improved from 0.88 lagging to 1.0. At t = 0.15 s current balancing operation begins and the currents of each phase are all brought to the same magnitude. The Unbalance Factor is reduced from 23.5% to 0.15%, and defined by:

$$\text{UBF} = \frac{|negative\ sequence|}{|postive\ sequence|} x100\% \tag{3}$$

Though the merits of the shunt compensator for a traditional feeder are firmly established, their place in a microgrid-based distribution system with significant generation and bi-directional power flows is not as obvious. One can consider a large solar plant installed at the

end of the feeder in Figure 2-1. At times there may be enough generation on the feeder itself that power flow reverses in one, two, or three phases. The UCSC can still balance the current seen by the substation up to the point and past where the averaged three-phase power flow has reversed. Figure 2-4 shows the UCSC operating while connected to an unbalanced load while three-phase generation at the end of the feeder increases starting at t = 0.25 s, eventually reversing real power flow in one phase.

The UCSC acting as an active filter for harmonics is shown in Figure 2-5, Figure 2-6, and Figure 2-7 using the control strategy proposed in [24]. The UCSC in Figure 2-5 activates at t = 0.03 s and begins compensation at t = 0.04 s.

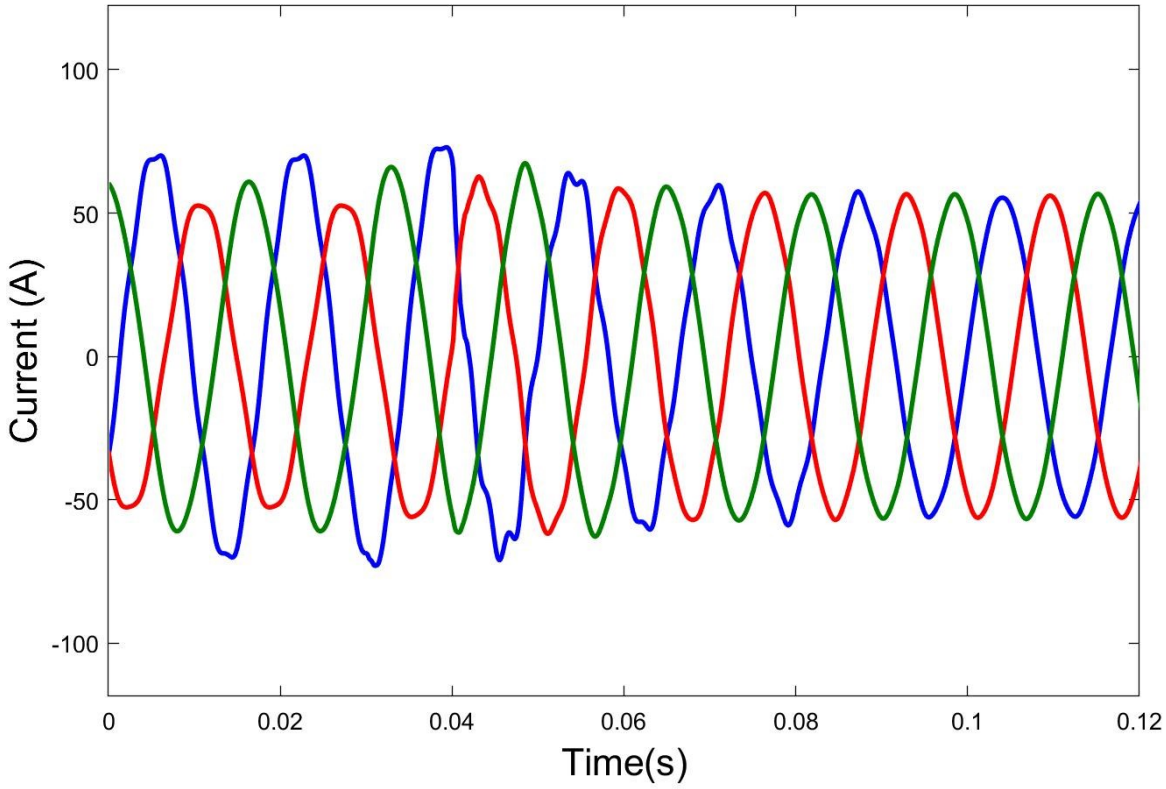

Figure 2-5. Substation currents before and after harmonic compensation.

Figure 2-6 shows the harmonic content of each substation phase current before compensation begins. The substation harmonics after imbalance and harmonic compensation begins is illustrated in Figure 2-7. The 7th harmonic was reduced from 2.2 A to 0.4 A in Phase A. The 5th harmonic was reduced from 1.8 A to 0.2 A in Phase B. And the 3rd harmonic was reduced from 1.9 A to 0.2 A in Phase C. The ability of an active filter to eliminate harmonics is a function of the switching frequency, sampling frequency, and computational power [25, 26].

2.6 UCSC Technical Challenges

Aside from the issues that any power-electronic-based solution faces (e.g., stability, THD, efficiency), any power electronic solution for the grid faces the same issues of any piece of

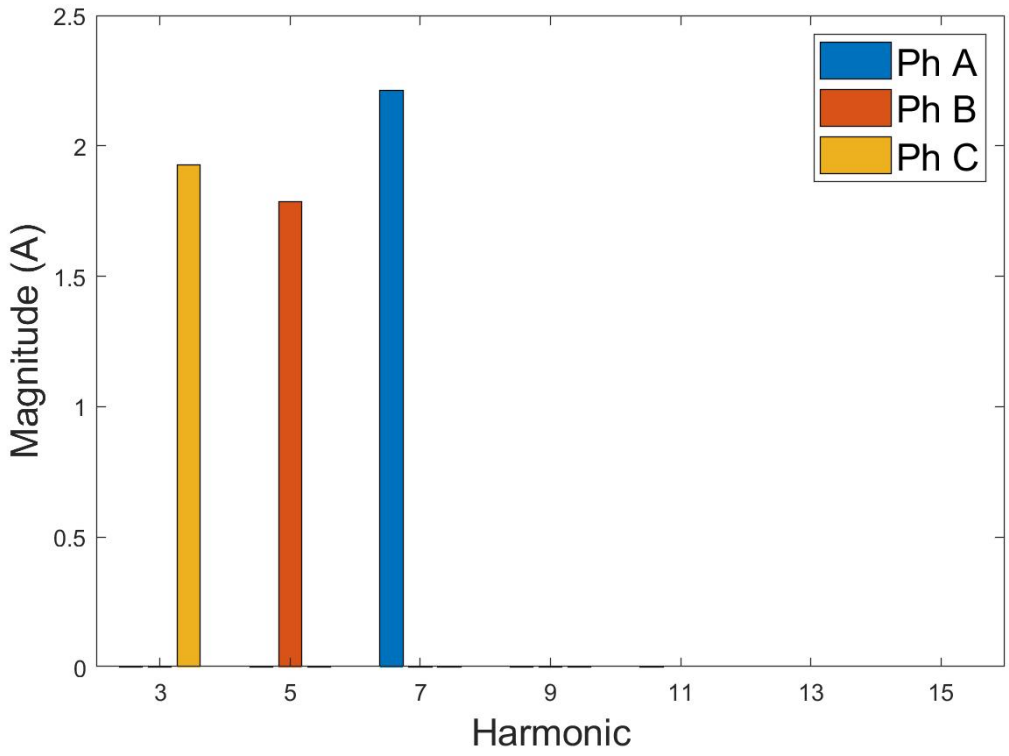

Figure 2-6. Substation harmonics before compensation.

passive utility equipment: (1) grid transients and (2) internal faults due to these transients. Semiconductor devices do not have the same overvoltage and overcurrent capabilities of traditional utility equipment. Thus, the protection of power electronic based equipment is a prominent research topic. Fortunately, as a supplementary and shunt-connected device, the UCSC avoids many issues that would be faced by equipment like a solid-state substation [27] such as providing fault current in the event of a grid fault and accompanying voltage-sag since the UCSC can quickly deactivate or compensate and wait for the grid to recover.

2.6.1 Over-Voltage Events

Significant voltage swells can occur on the grid and these types of events can destroy

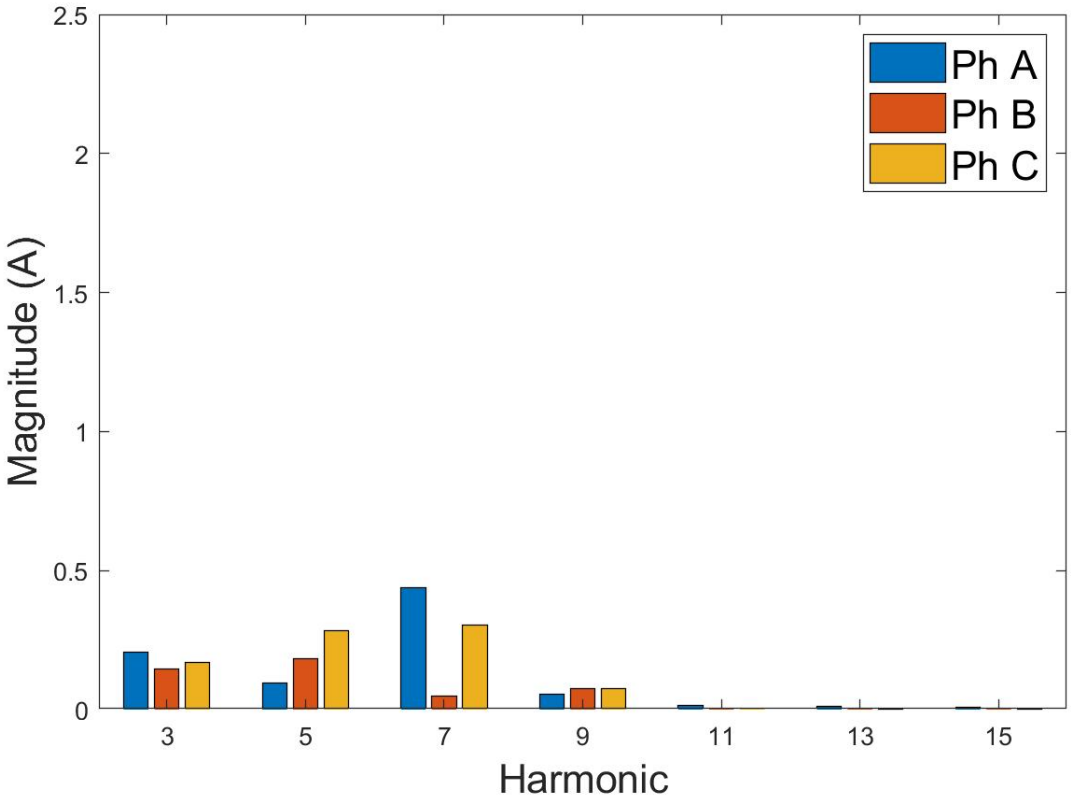

Figure 2-7. Substation harmonics after compensation.

power electronics if the voltage across any of the semiconductor devices rises above their breakdown limit. A worst-case scenario is lightning striking the distribution line near the UCSC. Reference [27] evaluates protections against the lightning strikes. These can include MOVs, solid-state circuit breakers, fault-current limiters, and ac crowbars. Reference [28] evaluates the selected grounding method of a grid-connected converter and its filter components for protection of the converter against lightning strikes using the IEEE 60060 1.2/50μs impulse voltage to approximate the lightning strike on the feeder. With these various solutions there are tradeoffs between cost, voltage surge levels, current surge levels, and any effect the solution may have on the grid.

2.6.2 Internal Faults

There are more points of failure due to the complexity and component count of these converters. An important area of research is in improving reliability and providing the ability to ride-through the fault of semiconductor devices or capacitors in the converter. Reference [29] outlines the use of redundant switching cells in modular multilevel converters (MMC) to improve reliability in the event of a device failing open or short. Reference [30] evaluates the ability of the flying capacitor converter (FCC, FCMLC) and presents solutions for continued operating after switch faults. “Hot-swapping” of submodule units in multilevel converters like in [31] paired with redundant switches or switch over-ratings can also enable smaller or eliminate down-time for power electronic equipment.

Another point of failure in most converters is the capacitor. Electrolytic capacitors can be a major limiting factor when it comes to the lifetime of the converter. Reference [32] addresses the reliability of capacitor banks based on electrolytic and film type capacitors. Film capacitors generally have greater reliability than electrolytic capacitors, but a lower energy density leading

to an inherent tradeoff between cost, size, and reliability. However, the higher switching frequencies enabled by SiC devices can shrink the capacitance required in some converters, which can make this trade-off optimization effort easier.

Though SiC is an enabling technology for direct MV connection, it brings new cabinet- and PCB-level design challenges. Powering gate drive circuitry at 10-30 kV bias with dv/dt of 100 kV/μs requires careful design of power supplies [33, 34]. Self-powered gate driving architectures may also be a suitable solution [35]. The selection of isolation materials is also important [36]. Reference [31] uses a solid polyurethane dielectric for a reduction in direct clearance between components, and thus converter volume, and as mechanical support for each submodule in the MMC.

2.6.3 Converter Start-up

In general, power converters require a start-up procedure and additional equipment to avoid high in-rush currents leading to power device failures. This actuality, like in grid transient protection schemes, requires some trade-offs between complexity, cost, and volume in the solution. As suggested in [37] a pre-charge resistance can be used to charge the capacitors in the converter safely, by limiting the in-rush current when the breaker is closed. This requires the use of an additional medium-voltage switch across this resistance to short it out during normal converter operation, which all together is relatively cheap, but can take up a lot of volume. The other common method is the use of an auxiliary power supply that charges the capacitors using energy from the grid in a controlled manor [38]. This can be implemented with semiconductor devices with potentially less volume than the shunt resistor method, though it is more complex and expensive. In both scenarios there is the potential for a mismatch in the capacitor voltages.

Balancing resistors and PWM techniques can be used to eliminate this mismatch during the start-up transient and steady-state operation as suggested in [39].

2.7 Conclusions

The use of an Unbalanced Current Static Compensator as a shunt compensator was evaluated for its use in electric distribution systems. The UCSC's primary functions as current balancing and power-factor correcting device were shown in simulations of a 13.8 kV feeder. The UCSC was able to achieve negligible neutral current and unity power factor for each phase. In addition, simulations of the UCSC acting as an active filter for harmonic currents were also included. The amplitudes of the 3rd, 5th, and 7th harmonics were reduced by around 80%. Potential secondary functionality of the UCSC and their benefits to the distribution system and the utility were discussed.

Current challenges associated with the implementation of grid-connected power electronics and more specifically multi-level converter structures based on SiC were presented along with solutions that have been proposed to solve these problems. This shows that the underlying technologies required to make a medium-voltage active compensator plausible exist. Though further research into reliability, cabinet-level design and proof-of-concept testing at medium-voltages approaching the 15 kV-class distribution voltages like in [40] are needed to increase confidence in the viability of FACTS implemented at the distribution system level.

2.8 Acknowledgments

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CHAPTER 3

THE IMPACT OF A CURRENT IMBALANCE COMPENSATOR ON FEEDER COMPENSATION EQUIPMENT OPERATION

V. Jones and J. C. Balda, "The Impact of a Current Imbalance Compensator on Feeder Compensation Equipment Operation," *2020 11th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Dubrovnik, Croatia, 2020, pp. 1-6.

3.1 Abstract

Typically, a feeder in a distribution system is operating with unbalanced currents. Furthermore, single-phase load-side generation can worsen this current imbalance. The use of an active current compensator has been suggested in literature as a solution because traditional compensation equipment used by electric utilities cannot fully address this issue. This paper looks at the effect that an unbalanced current compensator will have on the conventional compensation equipment installed at the substation. In addition, the positioning of this compensator relative to the other equipment is discussed. Using data from an existing distribution feeder the findings show that in most cases the use of this compensator can reduce the number of operations experienced by voltage regulators and switched capacitor banks.

3.2 Introduction

It is common for feeders in distribution systems to supply unbalanced loads. The economics of electricity supply force the use of single-phase taps from the three-phase main feeder to service loads and make this condition unavoidable. The load imbalance is worsened by the proliferation of single-phase rooftop solar installations affecting nominal load levels and potentially increasing load variability. As a result several issues can arise due to negative- and zero-sequence current components in feeder currents [1-6]. These include holding-tank

overheating, overloading of the neutral conductor and magnetomotive force (MMF) ripples in grid connected electric machines in addition to reduced system efficiency [7, 8].

To overcome this imbalance issue a shunt-connected compensator has been suggested to supply the negative- and zero-sequence currents on three-phase four-wire systems, and thus, give the appearance of a balanced load to all upstream equipment [9-14]. Many of these converters can also compensate for the load reactive power, and maybe, harmonic currents from non-linear loads. These compensators provide more benefit to the feeder when installed close to load because this eliminates unwanted current components before they can distort the feeder voltage profile. The disadvantage is that this does not compensate for as much load and thus requires many more installations. For this reason, this paper looks at the installation of a current compensator herein referred to as the Unbalanced Current Static Compensator (UCSC) at the head of the feeder within the substation.

More specifically this paper analyzes the effects that the UCSC at the substation may have on the voltage profile at the head of the feeder and preexisting traditional compensation equipment. Traditional regulating equipment on a feeder consists of Load Tap Changers (LTCs), (single- and three-phase) Voltage Regulators (VRs) and (switched and fixed) Power Factor Correction (PFC) Capacitors. LTCs and VRs are outfitted with mechanical tap-changing apparatuses that become worn over time and require preventative maintenance [15]. Coordination between reactive power compensators and LTCs is shown in [16] and others for balanced three-phase systems. This paper analyzes the effect of single-phase load imbalance correction in addition to reactive power compensation on the number of operations for these traditional regulating equipment by using data derived from an existing feeder and discusses the logistics of the positioning of the UCSC on preexisting substation installations.

The remainder of this paper is organized as follows: An overview of the conventional regulating equipment as well as the system derivations are in section II. The effect of the UCSC is analyzed in section III. Conclusions are given in section IV.

3.3 Conventional Regulating Equipment

Apparent-power data measured at 15-minute increments at a distribution feeder is shown in Figure 3-1. The implicit unbalance in the phase currents is obvious. A power factor of 0.80 lagging for each phase is assumed because the phase data was not provided. Uncompensated, these currents result in total winding conduction energy loss inside the transformer of 0.05405 pu-h or an average power loss of 0.00225 pu during the 24-hour period. In addition, a voltage Regulating equipment seen on the feeder traditionally consists of LTCs within the power

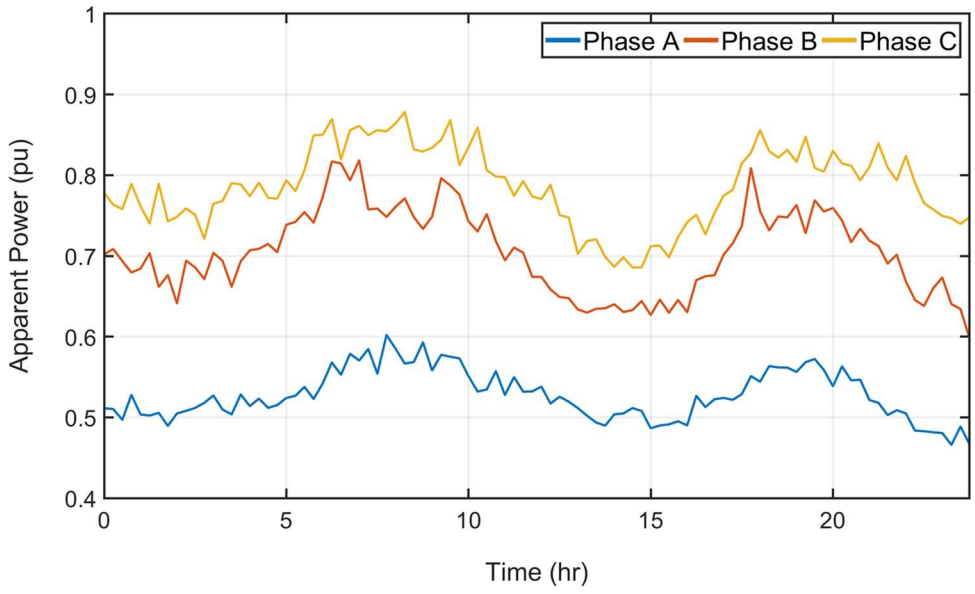


Figure 3-1. Feeder apparent power over a 24 hr period.

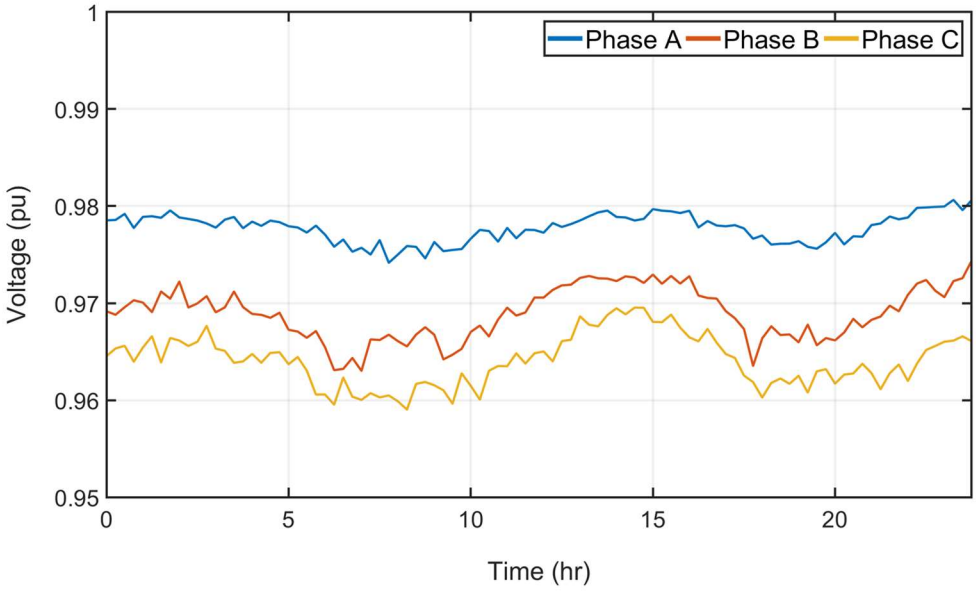


Figure 3-2. Voltage drop at the head of the feeder over a 24 hr period.

Table 3-1 Feeder characteristics

Parameter	Value
Transformer Reactance	0.065673 pu
Transformer Resistance	0.004827 pu
Feeder Source Reactance	0.01 pu
Load Power Factor	0.80 lag

transformers, single- and three-phase VRs and PFC capacitor banks (switched and fixed). LTCs and VRs typically have the option to enable Load-Drop Compensation (LDC). These can help to compensate for the voltage profile of the feeder and improve the feeder efficiency.

The equivalent one-line circuit diagrams for the feeder are shown in Figure 3-3. To increase the versatility of the model, a constant impedance load, I_{CIL}, a constant current load, I_{CCL}, and a constant power load, I_{CPL}, were considered when evaluating at the performance of the compensating equipment. The currents drawn from each of these sources are defined by:

$$\overrightarrow{I_{CILx}} = \frac{\left(K_{p1x}P_L + jK_{q1x}Q_{Lx}\right)^* \overrightarrow{V_{ux}}}{|V_o|^2}, \quad (1)$$

$$\overrightarrow{I_{CCLx}} = \frac{\left(K_{p2x}P_{Lx} + jK_{q2x}Q_{Lx}\right)^*}{|V_o|}\,, \tag{2}$$

$$\overrightarrow{I_{CPLx}} = \frac{\left(K_{p3x}P_{Lx} + jK_{q3x}Q_{Lx}\right)^*}{\overrightarrow{V_{ux}}}\,, \tag{3}$$

$$K_{p1x} + K_{p2x} + K_{p3x} = 1\,, \tag{4}$$

$$K_{q1x} + K_{q2x} + K_{q3x} = 1\,. \tag{5}$$

The variables whose subscripts are amended by "x" are quantities that are specific to a phase (a, b, or c) of the distribution feeder. The voltage just downstream from the power transformer is V_u. The real power of the load at the nominal voltage is P_L, V_o, and the reactive power of the load at V_o is Q_L. The percentages of P_L and Q_L constituted by the constant impedance load, the constant current load and the constant power load are K_{p1} and K_{q1}, K_{p2} and K_{q2}, and K_{p3} and K_{q3}, respectively. The voltage source for the grid is V_g, the equivalent transmission system impedance is Z_S and the power transformer impedance is Z_{XF}.

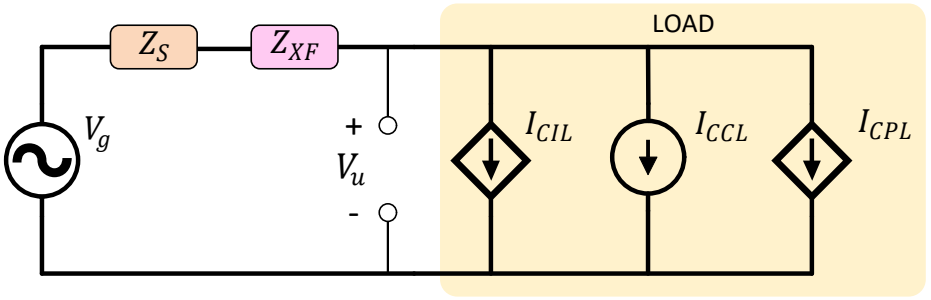
The basic one-line diagram with no compensating equipment is in Figure 3-3(a). A circuit approximating the VR is added in Figure 3-3(b) and a PFC capacitor bank is placed downstream from the VR in Figure 3-3(c). To solve the system at each data point the equations for the system had to be derived for each scenario.

3.3.1 Uncompensated System

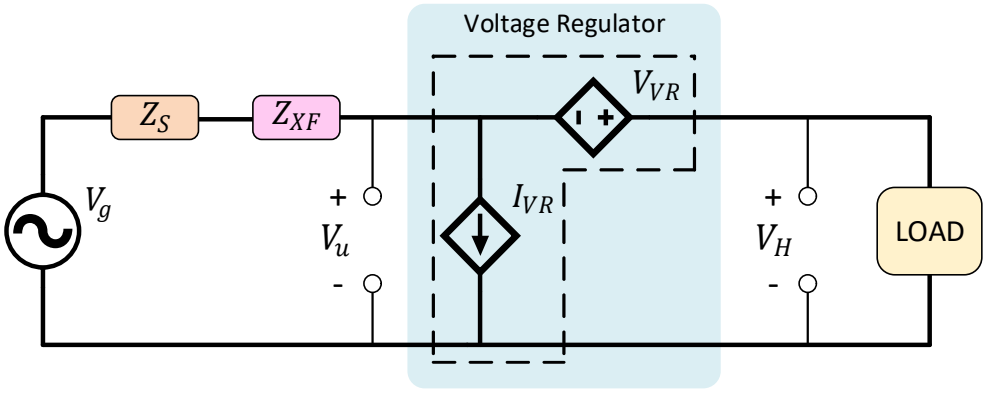
Using KCL at the downstream node of Z_{XF} results in:

$$\frac{1}{\overline{Z_{XF}}}\left(\overrightarrow{V_{gx}} - |V_{ux}|\right) = \left(\frac{K_{p3x}P_{Lx} + jK_{q3x}Q_{Lx}}{|V_{ux}|}\right)^* + \left(\frac{K_{p2x}P_{Lx} + jK_{q2x}Q_{Lx}}{|V_o|}\right)^* + \frac{|V_{ux}|}{\overrightarrow{Z_{Lx}}}, \tag{6}$$

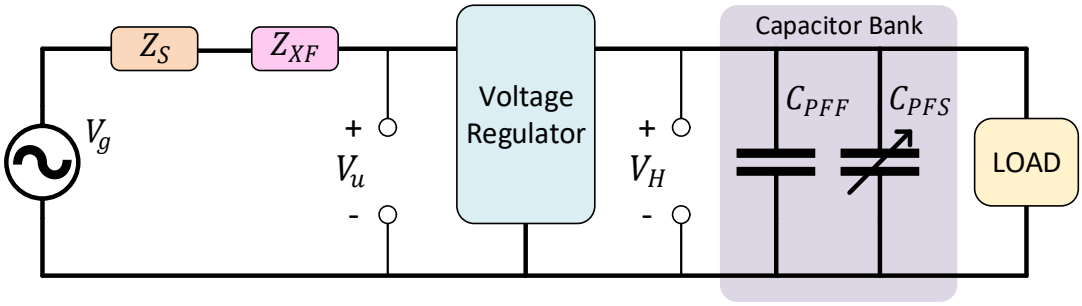
$$\overrightarrow{Z_{Lx}} = \frac{|V_o|^2}{\left(K_{p1x}P_L + jK_{q1x}Q_{Lx}\right)^*}, \tag{7}$$



(a)



(b)



(c)

Figure 3-3. Connection of the UCSC to a three-phase feeder.

$$\theta_{V_{gx}} = \sin^{-1}\left(\left[\left(-\frac{K_{q3x}Q_{Lx}}{|V_{ux}|}-\frac{K_{q2x}Q_{Lx}}{|V_o|}-\frac{|V_{ux}|\sin(\theta_{Z_{Lx}})}{|Z_{Lx}|}\right)|Z_{XF}|\right.\right.$$
$$\left.\left.-\sin(\theta_{Z_{XF}})\,|V_{ux}|\right]\left(\frac{1}{|V_g|}\right)\right)+\theta_{Z_{XF}}\,, \tag{8}$$

$$\frac{|V_g|\sin(\theta_{Z_{XF}})\sin\left(\theta_{V_{gx}}\right)+\cos(\theta_{Z_{XF}})\left(|V_g|\cos\left(\theta_{V_{gx}}\right)-|V_{ux}|\right)}{|Z_{XF}|} = \frac{K_{q3x}P_{Lx}}{|V_{ux}|}+\frac{K_{q2x}P_{Lx}}{|V_o|}+\frac{|V_{ux}|\cos(\theta_{Z_{Lx}})}{|Z_{Lx}|}. \quad (9)$$

Z_{LX} is the impedance for the constant-impedance load. $\theta_{Z_{XF}}$ is the impedance angle of the transformer. θ_{V_g} is the angle of V_g. V_u is chosen to be the 0 rad reference for the system. The magnitude of V_g is chosen to be 1.0146 pu. By iterating V_u and θ_{V_g} to satisfy (9) the solution of the system is determined.

3.3.2 System with Traditional Compensation

For the feeder in Figure 3-3(b), applying KCL at the downstream node of Z_{XF} results in the following system equations:

$$\frac{1}{\overline{Z_{XF}}}(\overline{V_{gx}}-|V_{ux}|)=\left[\left(\frac{K_{p3x}P_{Lx}}{|aV_{ux}|}-\frac{jK_{q3x}Q_{Lx}}{|aV_{ux}|}\right)+\left(\frac{K_{p3x}P_{Lx}}{|V_o|}-\frac{jK_{q3x}Q_{Lx}}{|V_o|}\right)+\frac{|aV_{ux}|(\cos(\theta_{Z_{Lx}})-j\sin(\theta_{Z_{Lx}}))}{|Z_{Lx}|}\right]a, \quad (10)$$

$$\theta_{V_{gx}}=\sin^{-1}\left(\left[a\left(-\frac{K_{q3x}Q_{Lx}}{|aV_{ux}|}-\frac{K_{q2x}Q_{Lx}}{|V_o|}-\frac{|aV_{ux}|\sin(\theta_{Z_Lx})}{|Z_{Lx}|}\right)|Z_{XF}|-\sin(\theta_{Z_{XF}})|V_{ux}|\right]\left(\frac{1}{|V_g|}\right)\right)+\theta_{Z_{XF}}, \quad (11)$$

$$\frac{|V_g|\sin(\theta_{Z_{XF}})\sin\left(\theta_{V_gx}\right)+\cos(\theta_{Z_{XF}})\left(|V_g|\cos\left(\theta_{V_gx}\right)-|V_u|\right)}{|Z_{XF}|} = a\left(\frac{K_{q3x}P_{Lx}}{|aV_{ux}|}+\frac{K_{q2x}P_{Lx}}{|V_o|}+\frac{|aV_{ux}|\cos(\theta_{Z_Lx})}{|Z_{Lx}|}\right), \quad (12)$$

$$V_{Hx}=aV_{ux} \quad (13)$$

a is a scalar that corresponds to the tap location on the VR. PFC capacitors are added to the constant impedance load Z_{Lx}.

The system equations are iteratively solved using a script. The flowchart for the script is shown in Figure 3-4. For each apparent power datapoint from Figure 3-1 the system equations are solved for each phase (Steps 1 - 3). For the uncompensated system steps 4 through 8 are skipped. When using an LTC or a VR the system, it must be determined if V_H is within

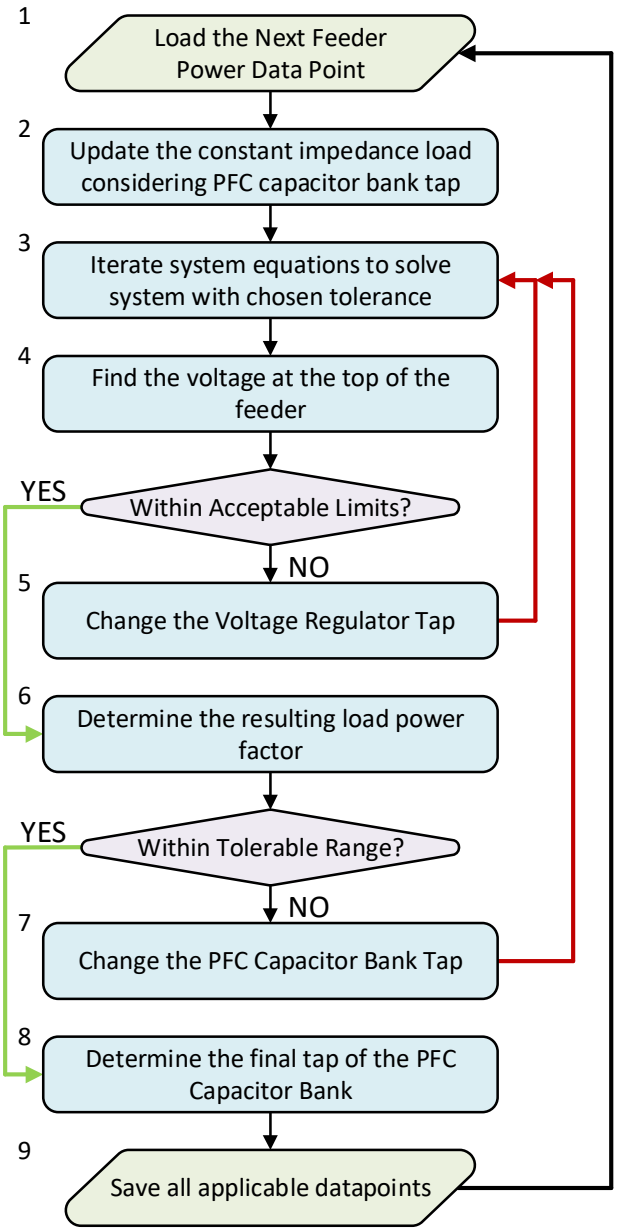


Figure 3-4. Connection of the UCSC to a three-phase feeder.

acceptable limits (Step 4). If not, the tap must be changed, and Step 3 is performed again. The VR is assumed to be a +/- 5% regulator with 16 taps. This results in steps of 0.625%. Based on section 4.c.(4).(a) of [17] an LDC with a K value of 3.2125 is chosen with a compensation voltage of 4 V.

If PFC capacitors are not used, then steps 6 through 8 are skipped. If PFC capacitors are used, then Step 6 is performed. If the level of reactive power is not within tolerable limits, then the switch PFC capacitor tap must be changed, and Step 3 must be performed again. For this paper a fixed capacitor bank is installed that achieves close to unity power factor for the lightest load of the day. In addition, it is assumed that a switched PFC capacitor bank as large as needed to achieve unity power factor at any amount of reactive power is also installed. Accomplishing unity power factor may not be cost effective to the utility. However, the "economical power factor" can increase from around 0.95 lagging closer to unity when the price of new installations and fuel rises [18]. However, the relative performance is of interest for the purposes of this paper so unity power factor was chosen.

There are numerous types of tap control schemes for switched PFC capacitor banks [19]. For this paper, the capacitor bank is operating with VAR control with the setpoint being unity power factor. In the continuous time system there would most likely be a time-delay feature on each piece of equipment [17].

In the case of increasing the tap (increasing the PFC capacitance), the requirements for a tap was 101% of the VAR_{pu} of a tap. This means that for a 0.0125 VAR_{pu} tap the PFC capacitor bank would have to detect a need of an additional 0.01375 VAR_{pu}. For a downward tap change (decreasing the PFC capacitance), an excess of 0.01 VAR_{pu} is required to trigger a tap change. It is typically not desired to run a feeder at a leading power factor because of the possibility for

voltage swells and resonances [18]. This increased margin for operation is to avoid nuisance tap changing around the boundary conditions.

3.4 Effect of Adding the UCSC

3.4.1 Placement of the UCSC

The order in which the equipment comes on the feeder can affect the performance of the total system. For example, it is best to place PFC capacitor banks downstream from the voltage regulator because in this configuration they better compensate the voltage at the head of the feeder [17]. This indicates that the location of the UCSC may affect its performance and as the UCSC is intended to be added to existing substations not all locations for the UCSC may be feasible. For this reason, the position of the UCSC among the preexisting equipment (PFC capacitor bank, VRs and transformers with integrated LTCs) was considered. The cases considered are given below and named for the order in which they appear along the feeder.

1) UCSC, Voltage Regulator, PFC Capacitor Bank: This is the most natural positioning for the UCSC. This allows for the UCSC to compensate for the current without any additional calculation. The voltage difference due to the upstream impedance and the transformer are compensated and the PFC banks are part of the load. This placement of the UCSC is shown in Figure 3-5. The current out of the UCSC is I_{uC}, I_{uL} the load current seen by the UCSC, and I_{VR} the CT measurement for the VR LDC.
2) Voltage Regulator, UCSC, PFC Capacitor Bank: Without the LDC enabled on the voltage regulator this positioning of the UCSC performs the same as in Case 1. This configuration is displayed in Figure 3-6. However, if the LDC is enabled this creates a problem for the voltage profile along the feeder. The currents the LDC uses to

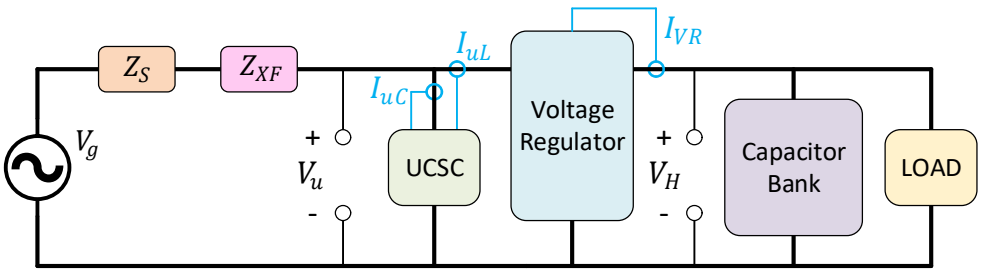


Figure 3-5. UCSC placement for Configuration 1 with current sensor locations.

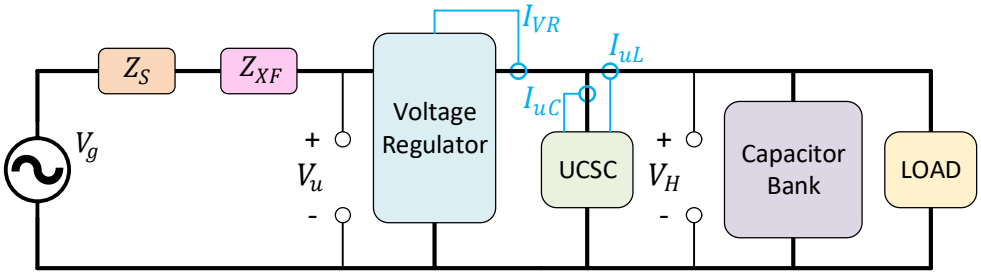


Figure 3-6. UCSC placement for Configuration 2 with current sensor locations.

perform its compensation would be incorrect, as they are compensated currents. If the CT for the LDC could be moved to measure the current downstream from the UCSC then this problem is eliminated. But most voltage regulators have the CT installed within the same tank as the tap-changing mechanism and makes this modification unlikely and/or unreasonable.

3) Voltage Regulator, PFC Capacitor Bank, UCSC: This positioning might come about if there is no space at the substation for additional installations. This has the same issues as Case 2. In addition, the UCSC then requires knowledge of tap position of the PFC capacitor bank so that it can appropriately compensate the power factor. Otherwise, it will attempt to compensate for the total reactive VARs of the load. One advantage of this positioning is that the UCSC is now inherently equipped to compensate for the harmonics that might otherwise cause increased current in the

PFC capacitor bank. To achieve this task in Case 1 & 2 the UCSC would need a current sensor downstream from the PFC capacitor. Otherwise, it can only compensate for harmonic currents seen upstream.

4) Load Tap Changer, UCSC, PFC Capacitor Bank: Assuming that the LTC similarly to a three-phase VR, and the impedance changes of the transformer are negligible with tap changes as in the VR; so, this case is identical to Case 2. The LTC is built into the transformer and the use of an LDC would most likely result in a deterioration of the feeder voltage at the intended load center for which the LDC is enabled.

Considering the UCSC, VR with LDC, and PFC Capacitor bank as distinct installations, not all advantages of the UCSC can be obtained with any one configuration. Through a reconfiguration of the UCSC current sensors from Figure 3-7 the current balancing, reactive current compensation functionalities of the UCSC can be performed as intended using I_{uS}, the upstream current seen by the UCSC, rather than I_{uL}. Then, the measurement I_{uL}, which has been moved downstream from the capacitor banks can be used to eliminate the lower-order harmonic currents seen by the PFC capacitor banks.

3.4.2 Effect of the UCSC

For comparisons of the voltage unbalance between the phases and the number of operations of the VRs and PFCs, the "UCSC, Voltage Regulator, PFC Capacitor Bank" case from the previous section was chosen. The results of the different scenarios are summarized in Table 3-2 – Table 3-8. The Average Maximum Voltage Unbalance (AMVU) metric used here to determine the affect the UCSC has on the balance of V_H on each phase is defined as:

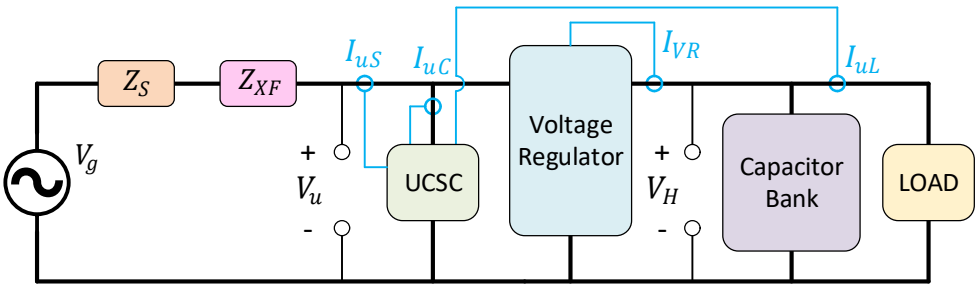


Figure 3-7. UCSC current sensor reconfiguration.

$$\frac{\sum_{1}^{n}\left[max\left(\left|V_{Hx}-V_{H}^{avg}\right|, x=\{a,b,c\}\right)\right]}{n}, \tag{14}$$

where n is the number of datapoints in the day and V_H^{avg} is the average of V_H between the three phases, at each value of n.

Though current source loading can be a good approximation of a feeder with mixed type loading (industrial, residential) this is not the case for many feeders. For this reason, the feeder wassolved separately for the cases of mostly industrial loads and mostly residential loads. For

Table 3-2 Scenario descriptions

Scenario	VR	LDC	Load Type	VR Settings (V_{pu})	PFC Settings
1	3 x 1-ph	YES	Industrial	1.0167 (± 0.0125)	1% Hysteresis
2	3 x 1-ph	YES	Residential	1.0167(± 0.0125)	1% Hysteresis
3	1 x 3-ph	YES	Industrial	1.0167(± 0.0125)	1% Hysteresis
4	1 x 3-ph	YES	Residential	1.0167(± 0.0125)	1% Hysteresis
5	1 x 3-ph	NO	Industrial	1.0417(±0.0167)	1% Hysteresis
6	1 x 3-ph	NO	Residential	1.0417(±0.0167)	1% Hysteresis
7	1 x 3-ph	NO	Industrial	1.0417(±0.0167)	10% Hystersis
8	1 x 3-ph	NO	Residential	1.0417(±0.0167)	10% Hystersis

Table 3-3 Scenario 1

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	76	9	0.004632
	YES	71	1	0.004166
0.0250	NO	29	9	0.005213
	YES	27	1	0.004166
0.0375	NO	29	9	0.005088
	YES	22	1	0.004166
0.0500	NO	10	11	0.005402
	YES	8	1	0.004166

Table 3-4 Scenario 2

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	87	6	0.00509
	YES	83	2	0.00467
0.0250	NO	29	6	0.00507
	YES	29	2	0.00467
0.0375	NO	20	6	0.00511
	YES	20	0	0.00417
0.0500	NO	19	10	0.00547
	YES	19	0	0.00417

Table 3-5 Scenario 3

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	74	5	0.00898
	YES	71	0	0.00000
0.0250	NO	27	5	0.00899
	YES	27	0	0.00000
0.0375	NO	29	5	0.00899
	YES	22	0	0.00000
0.0500	NO	10	5	0.00899
	YES	19	0	0.00000

Table 3-6 Scenario 4

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	87	2	0.00914
	YES	81	0	0.00000
0.0250	NO	29	2	0.00913
	YES	29	0	0.00000
0.0375	NO	20	2	0.00913
	YES	20	0	0.00000
0.0500	NO	19	2	0.00913
	YES	19	0	0.00000

Table 3-7 Scenario 5

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	77	0	0.00901
	YES	77	0	0.00000
0.0250	NO	27	0	0.00901
	YES	38	0	0.00000
0.0375	NO	26	0	0.00901
	YES	20	0	0.00000
0.0500	NO	8	0	0.00900
	YES	20	0	0.00000

Table 3-8 Scenario 6

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	87	0	0.00916
	YES	83	0	0.00000
0.0250	NO	29	0	0.00915
	YES	44	0	0.00000
0.0375	NO	20	0	0.00915
	YES	23	0	0.00000
0.0500	NO	19	2	0.00914
	YES	16	0	0.00000

Scenarios 5 and 6 the LDC is disabled and thus the voltage band tap settings have been changed to maintain the feeder voltage around 1.0417 pu. This would be the case for a UCSC installed downstream from the VR or LTC.

In scenarios with three single-phase VRs, the steps total includes the steps for every phase. In scenarios with one, three-phase VR the step total is equivalent to a step of all three phases, so those totals need to be multiplied by a factor of 3 when comparing numbers. In all scenarios the sensors for the PFC capacitors are on the most heavily loaded phase. For the 1 x 3-ph VR scenarios the most heavily loaded phase is also used.

In almost every case, the number of operations of the VRs has been reduced with the introduction of the UCSC. Similarly, the AMVU was also reduced for each case in which the UCSC was used.

With regards to the switch PFC capacitor banks, the benefits are not so inherent. In some cases, like in Scenario 3 with 0.05 VAR_{pu} PFC capacitor taps, the number of tap changes significantly increased. To overcome this effect, better coordination between the UCSC and the PFC capacitor banks is required. A simple approach would be a larger hysteresis placed for PFC capacitor tap changes. Two more scenarios are run with an increase in the hysteresis for an upward tap change. The downward tap hysteresis is left unchanged.

Table 3-9 and Table 3-10 show the number of operations using a larger hysteresis. In these scenarios the number of operations for the PFC capacitors banks either remained the same or reduced. This comparison demonstrates that the installation of a UCSC may not simply be a "plug-and-play" solution and may require additional analysis of the interaction between compensation equipment.

Because no assumptions can be made about the data between each of the 15-minute

Table 3-9 Scenario 7

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	74	5	0.00898
	YES	71	0	0.00000
0.0250	NO	27	5	0.00898
	YES	27	0	0.00000
0.0375	NO	25	5	0.00899
	YES	22	0	0.00000
0.0500	NO	8	5	0.00899
	YES	8	0	0.00000

Table 3-10 Scenario 8

PFC Steps (pu VARs)	UCSC	PFC Capacitor steps	# VR steps	Avg. Maximum Voltage Unbalance
0.0125	NO	87	2	0.00914
	YES	81	0	0.00000
0.0250	NO	29	2	0.00913
	YES	29	0	0.00000
0.0375	NO	18	2	0.00913
	YES	18	0	0.00000
0.0500	NO	17	2	0.00912
	YES	17	0	0.00000

increments, the data provided does not fully account for the number of operations that might occur with continuous-time data. The delay settings for VRs can be anywhere from 30 seconds to 60 seconds depending on the volatility of the voltage profile. From this, it can be assumed that the maximum number of operations from one increment to the next could be $(15\ min/(0.5\ min/operation) - 1)$ or 29.

3.4.3 Effect on the Power Transformer

Perfectly balanced loading would produce a slight decrease in the winding losses and core losses (around 1-2%), but this in of itself might not provide an economical motivation for

installation of a UCSC. Temperature dependent end-of-life analysis of the transformer winding and insulation like in [20] would be required to determine benefits that might be derived from a UCSC. Assuming a forced cooling method, the difference in average oil temperature in the holding tank between unbalanced and balanced load conditions may be negligible; however, the hot-spot temperature of the heavily loaded lines may age one winding more than the other two.

3.5 Conclusions

The effect of adding a shunt current compensator for phase current balancing and reactive power compensation on a traditional feeder was evaluated. More specifically, the effect that this compensator, referred to as the Unbalance Current Static Compensator (UCSC), had on the voltage imbalance and preexisting equipment installed at the head of the feeder.

A feeder model was developed to include input impedance, voltage regulators, power-factor correction capacitor banks and the UCSC. Based on voltage data at the head of a real feeder, the numbers of operations required by VRs and switched PFC capacitor banks were determined. In general, the numbers of operations for both VRs and PFC capacitor banks were reduced in the presence of the UCSC. Reduction in VR operations up to 100% was achieved. At best, the operations for the PFC capacitor banks was reduced by 28%. However, in some cases, the settings for a tap changing condition may need to be relaxed to avoid an increase in the number of operations in the presence of the UCSC.

3.6 References

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CHAPTER 4

CONSTRUCTION AND SIMULATION OF THE MV-UCSC PROTOTYPE

The theoretical understanding, simulation, and construction of a 13.8 kV neutral-point-clamped (NPC) flying capacitor converter (FCC), referred to as the MV-UCSC, that utilizes the developed modular stackable switching positions to be analyzed in Chapter 5 are presented in this chapter.

4.1 MV-UCSC Prototype Design

The envisioned connection of the FCMC, that is the MV-UCSC, to the grid is illustrated in Figure 4-1. The MV-UCSC is connected in parallel with the downstream feeder at the point of common coupling (PCC). A diagram of the basic structure for a single phase of the converter is shown in Figure 4-2. Each phase consists of 11-level utilizing 3.3 kV switching positions (with ~70% voltage utilization). This voltage level was chosen to reduce the required complexity of the converter since 10 kV and 6.5 kV power semiconductor devices are still in their early developmental stages. The ratings used for the development of the MV-UCSC are displayed in Table 4-1.

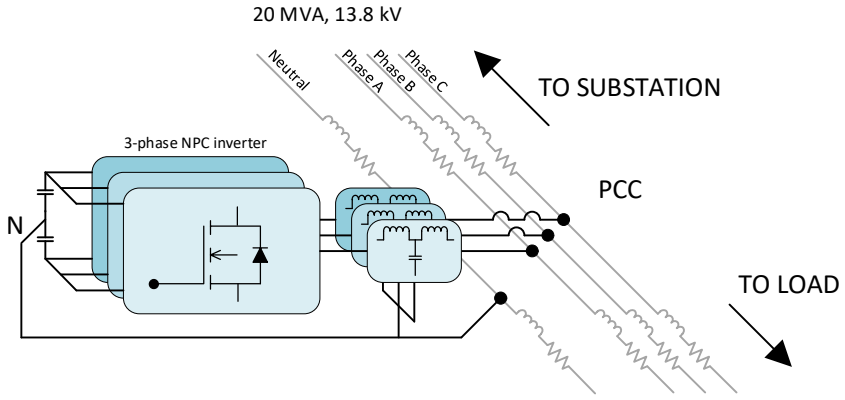


Figure 4-1. Connection of the MV-UCSC to a three-phase feeder.

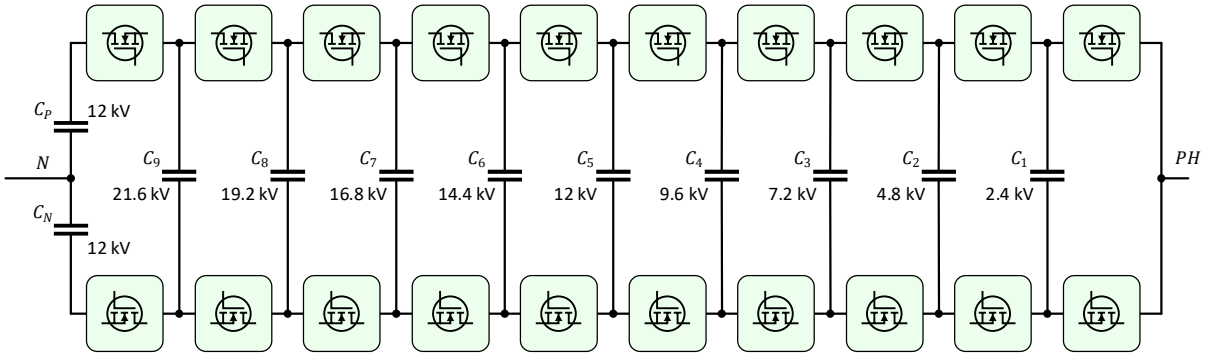


Figure 4-2. The topology for one phase of the MV-UCSC.

Table 4-1. MV-UCSC design specifications

Parameter	Value
Power Rating	750 kVA (250 kVA per phase)
Voltage Rating	13.8 kV (line-to-line)
Current Rating	~ 30 A
Position Switching Frequency	10 kHz

4.1.1 The 3.3 kV Switching Position

Cost and availability of 3.3 kV SiC devices made it unfeasible to develop the 3.3 kV switching position utilizing these devices. Therefore, two series-connected 1.7 kV SiC MOSFETs were used to form an effective 3.3 kV switching position [1]. The design of the 3.3 kV switching position was presented in [1]. The switching position as it fits into the converter is demonstrated in Figure 4-3. These switching positions avoid the need for an isolated power supply to provide auxiliary power using a self-powered circuit [2-4]. In addition, a voltage balancing circuit is placed across each switch to ensure dynamic and static voltage sharing among the series-connected devices.

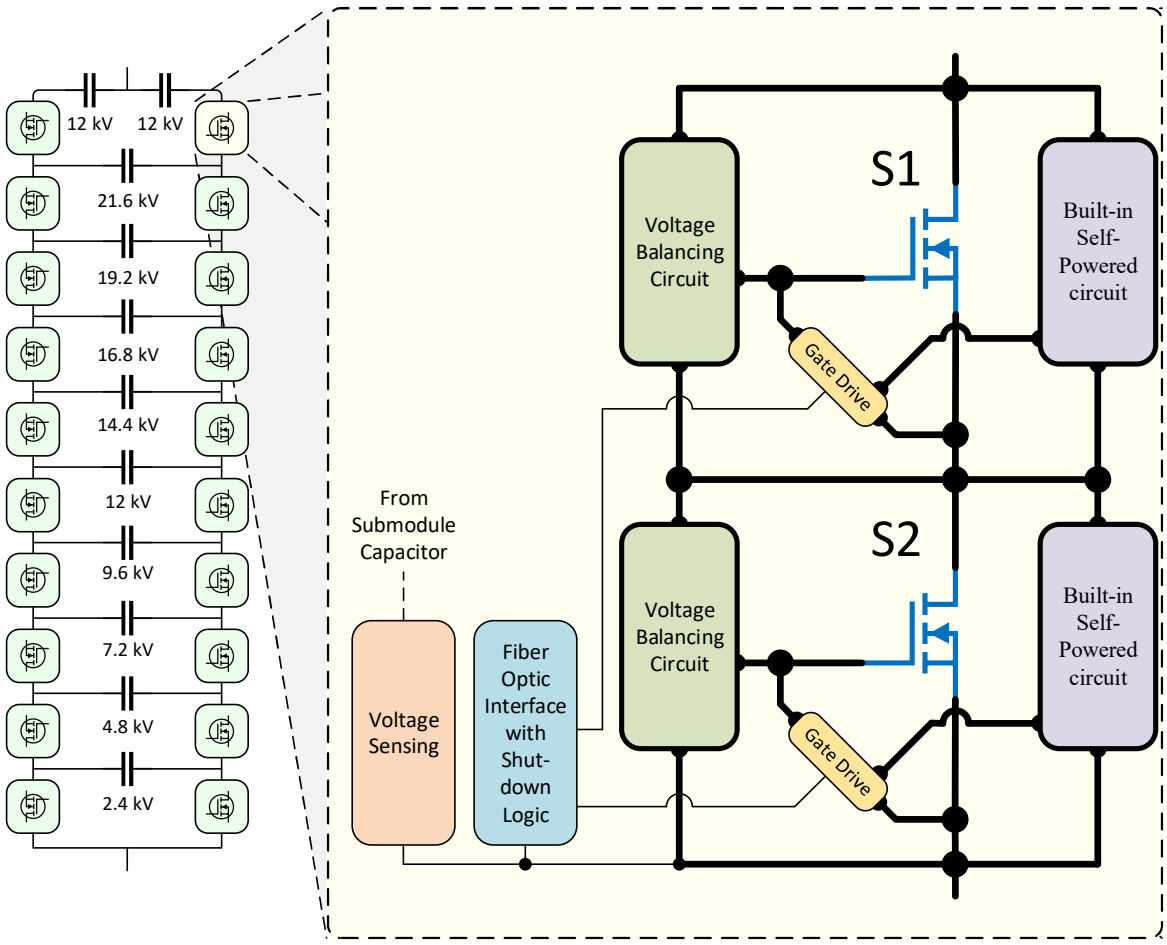


Figure 4-3. The switching position placement in a converter phase.

4.1.2 Flying and DC-Bus Capacitors

The major components along with their values are given in Table 4-2. The minimum required capacitance for each capacitor unit of the flying capacitors is from [5]:

$$C_{fc} \geq \frac{1}{\Delta V_{fc}} \hat{I}_s \frac{1}{2f_{sw}} (1 - m)\,. \tag{1}$$

where ΔV_{fc} is the desired ripple voltage across one unit, $\hat{I}_s$ is the peak of the sinusoidal current, f_{sw} if the switching frequency of a submodule, and m is the modulation index. The flying capacitor unit C_{fc} for the MV-UCSC would be calculated as

Table 4-2. MV-UCSC components and values

Component	Value	Selected Product
DC-Bus Capacitance		
Capacitors	3900 µF 550 V	Kemet A4075_ALS70_71
Shunt resistance	40 kΩ	
Connection	PCB	2-layer, 1 oz, FR-4
Flying Capacitors		
Capacitors	5 µF, 1300 V	TDK MKP_B32774_778
Connections	PCB	2-layer, 1 oz, FR-4
LCL Filter Capacitance		
Capacitors	3 uF	CDE SCRN235R-F
Damping resistance	10 Ω 100 W	Ohmite L25J10RE
Filter Inductance		
Cores	2.3 mH	Amorphous C-Core MetGlas AMCC-1000
Wire	Litz Wire 4-AWG, 38 AWG strands	New England Wire Technolgies NELD2625_38SPDN
Air gap spacer	PLA	
Grid Voltage Sensing		
Voltage sensor	Hall Effect Transducer	LEM 25-P
Burden resistance	75 kΩ, 7 W	Yageo SQM700JB-75K
DC-Bus Voltage Sensing		
Voltage sensor	Hall Effect Transducer	LEM 25-P
Burden resistance	75 kΩ, 7 W	Yageo SQM700JB-75K
Current Sensing		
Current sensor	Hall Effect Transducer	LA 100-P
EMI shield	Copper Braid	Electriduct 1/2" EMI RFI Shielding
Cabling		
Hook-up wire	10 AWG, 15 kV	AWC 3239-10-15KV
Sensing Signal wire	22 AWG, 3-conductor	Alpha Wire 57003
Fiber optic	1 mm Plastic Optical Fiber	Broadcom HFBR series

$$C_{fc} \geq \frac{1}{(240\ V)}(43\ \text{A})\frac{1}{2(10\ \text{kHz})}(1-0.8) = 3.0\ \mu\text{F}\,.$$

The minimum capacitance for the dc-link capacitors is given in [6] as:

$$C_{dc} \geq \frac{I_s}{\Delta V_{dc}\omega_s}. \tag{2}$$

where ΔV_{dc} is the desired voltage ripple of the dc bus and ω_s is the angular frequency of the grid. The required dc-bus capacitance for the MV-UCSC is

$$C_{dc} \geq \frac{(43\ A)}{(600\ V)\left(377\frac{rad}{s}\right)} = 180\ \mu F.$$

The use of balance-boosting resistors across each switch was considered based on the analysis in [7]. The boosting resistance that is desired is one that is small to keep the voltage drift due to dead-time and switching delay offsets to less than 1% of the nominal voltage. The voltage offset due to switching delays, V_{off}, can be calculated using

$$V_{off} = \frac{\sigma t_s I_L}{4C_{fc}\left[1 - e^{\left(-\frac{\alpha T'}{2}\right)}\left(\frac{\alpha}{\omega}\sin\left(\frac{\alpha T'}{2}\right) + \cos\left(\frac{\alpha T'}{2}\right)\right)\right]} \tag{3}$$

with

$$\alpha = \frac{R}{2L} \tag{4}$$

$$\omega = \sqrt{\frac{R^2}{(2L)^2} - \frac{1}{LC_{fc}}} \tag{5}$$

where I_L is the load current, t_s is the total of all switching delays, and σ is a percentage of the total possible switching delay that results in a switching mismatch. The voltage across the switch is V_d, the capacitance of the flying capacitor is C_{fc}, and T' is the duty cycle. The load resistance is R and the load inductance is L. The offset for the MV-UCSC is then given by:

$$\omega = \sqrt{\frac{(250\ \Omega)^2}{(2 * 4.6\ mH)^2} - \frac{1}{(4.6\ mH)(6.5\ \mu F)}} = 20099\ ,$$

$$\alpha = \frac{250\ \Omega}{2 * 4.6\ mH} = 27174\ ,$$

$$V_{off} = (2400\ V) - \frac{(200\ ns)(43\ A)}{4(6.5\ \mu F)\left[1 - e^{\left(-\frac{27174\ (0.5)}{2}\right)}\left(\frac{27174}{20099}\sin\left(\frac{27174\ (0.5)}{2}\right) + \cos\left(\frac{27174\ (0.5)}{2}\right)\right)\right]}\ ,$$

$$V_{fc} = 10.23\ V\ .$$

The voltage offset with no boosting resistance is still within the desired 1% or 24 V due to the low switching delays of the SiC MOSFETs.

4.1.3 Converter Output Filter

There is an LCL filter at the output of the converter that is designed using the methods in [8-10] to meet IEEE 1547-2003 requirements. The steps for determining the ratings for the LCL filter are as follows:

1. Choose the percentage of base capacitance for the filter capacitance. This is based on the power rating of the converter and should normally not go beyond 2%. The filter capacitance C_f is then selected using

$$C_f = \frac{0.02 S_\phi}{{V_g}^2 \omega_s}\ , \tag{6}$$

where S_ϕ is the single-phase power of the converter, V_g is the line-to-neutral grid voltage and ω_s is the angular frequency of the grid. The target MV-UCSC capacitance is then

$$C_f = \frac{0.02(250\ kVA)}{(7.96\ kV)^2\left(377\ \frac{rad}{s}\right)} = 209\ nF\ .$$

2. Determine the converter-side inductance, L_c using:

$$L_c = \frac{V_{DC}}{\Delta i_c I_L f_{eff}}, \tag{7}$$

where V_{DC} is the voltage of one level of the MV-UCSC, Δi_c is the chosen output current ripple percentage, I_L is the load current rating, and f_{eff} is the effective output frequency of the MV-UCSC. The target converter-side inductance for the MV-UCSC is then given by:

$$L_c = \frac{(2.4\ kV)}{(0.3)(31\ A)(100\ kHz)} = 2.5\ mH\ .$$

3. The grid-side inductance, L_g, is then chosen empirically by satisfying the following

$$\Delta i_g = \frac{1}{\left|1 + r\left(1 - L_c C_f \left(2\pi f_{eff}\right)^2\right)\right|}, \tag{8}$$

$$L_g = r L_c\ , \tag{9}$$

where r is the ratio between L_g and L_c and Δi_g is the percent current ripple reduction of the of the grid-side inductor. The target grid-side inductance for the MV-UCSC is then calculated iteratively in a Matlab™ script using:

$$0.17 = \frac{1}{\left|1 + r\left(1 - (2.5\ mH)(209\ nF)\left(2\pi(100\ kHz)\right)^2\right)\right|}\ .$$

and solving for r. The value of r is 0.35 to bring the total ripple to [(0.3)(0.17) * 100%] ≈ 5 % requiring a grid-side inductance of 764 µH. For simplicity of construction and lower THD at initially lower test currents, the L_g was made identical to L_c (r = 1).

4. Calculate the required damping resistance, R_f, using

$$R_f = \frac{1}{3\omega_{res}C_f}\ , \tag{10}$$

$$\omega_{res} = \sqrt{\frac{L_g + L_g}{L_c L_g C_f}}\ , \tag{11}$$

where ω_{res} is the angular resonant frequency for the LCL filter. The damping resistance for the MV-UCSC is

$$\omega_{res} = \sqrt{\frac{(2.3\ mH) + (320\ \mu H)}{(2.3\ mH)(320\ \mu H)(209\ nF)}} = 131\ \frac{krad}{s},$$

$$R_f = \frac{1}{3\left(131\ \frac{krad}{s}\right)(209\ nF)} \approx 17\ \Omega\,.$$

which is higher than the 10 Ω resistance in Table 4-2. This is because the film capacitors used for the filter capacitance have a non-negligible equivalent series resistance (ESR). Adding the ESR of the capacitors brings this equivalent resistance closer to the desired 17 Ω.

4.2 MV-UCSC Prototype Construction

4.2.1 Submodule Capacitors

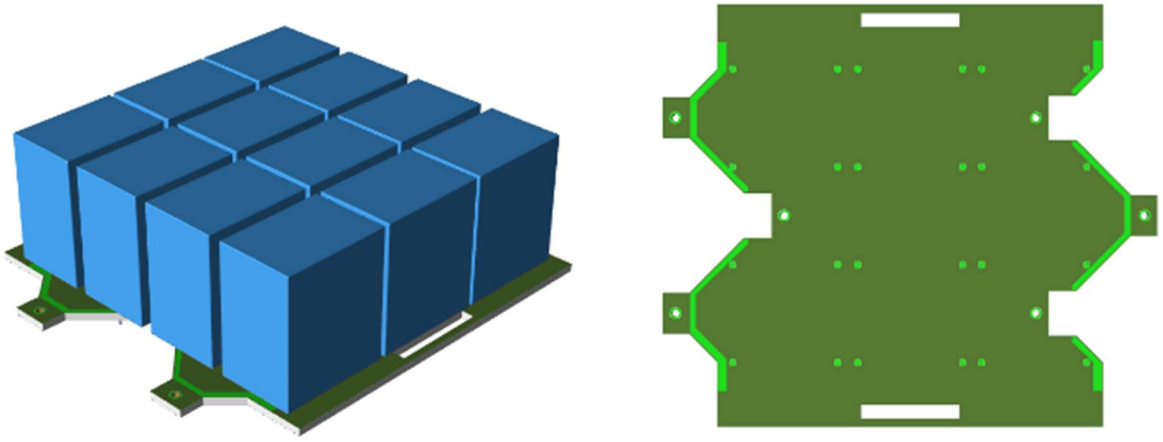
Film capacitor technology was chosen for the submodule capacitance. Though, they have a relatively low energy density compared with electrolytic capacitors, and have higher parasitic ESL relative to ceramic technologies, they do have better reliability than either electrolytic or ceramic capacitors. Metallized film capacitors can "self-heal" after large current transients and tend to fail in an open state rather than failing short like ceramic capacitors [11]. Considering the semi-modular nature of the FCMC, where each module depends on the others' voltage, it is important that no capacitor stacks fail short.

Additionally, the inverse relationship with the switching frequency and the laxer power density requirements of grid-connected equipment (relative to traction inverters or UPSs) allows for the use of less energy dense capacitor technologies [12]. The 1300 V, 5 μF film capacitors from TDK in Table 4-2 were chosen for the MV-UCSC.

The ESL of the capacitors stacks is an important factor for many reasons including voltage spikes across the devices, output voltage distortion, EMI, and voltage balancing. Keeping this value low is crucial, yet difficult due to the high voltage requirements. Paralleling capacitors is effective but can be costly in terms money and space. By paralleling "n" strings of capacitors, the ESL of the total stack can be reduced theoretically by "1/n". Paralleling multiple capacitors with smaller ratings also gives more control over the form factor of the capacitor stacks. However, the return vs cost/space does have a diminishing benefit as the percent reduction of ESL become less and less with each paralleled stack. For example, the change in ESL from 4 to 5 strings is only 5% of the original value of ESL for one stack. A model of each flying capacitor unit is shown in Figure 4-4(a). The film capacitors were arranged in series-connected strings of 3 with 4 of these strings connected in parallel which forms an equivalent capacitance of approximately 6.5 μF, satisfying the 4.5 μF minimum requirement.

Because of the orientation within the cabinet, the PCBs for these capacitors were designed with interlocking teeth and are soldered together to provide extra strength when placing several in series. This method was chosen as a cheaper alternative to custom busbar design. A top view of the PCB is given in Figure 4-4(b).

To avoid a large loop area associated with these capacitors, each of the stacks was folded in half with the positive and negative terminals being brought back together as shown in Figure 4-5. This design reduces the stray inductances of the capacitor units and helps to avoid radiated



(a) (b)

Figure 4-4. Model of the submodule capacitor unit (a), and a top-down view of the submodule capacitor unit PCB (b).

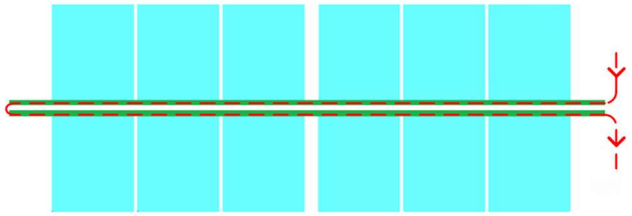


Figure 4-5. Current path for submodule capacitor stacks.

EMI from the experienced switching frequency currents [13]. Unfortunately, this design also places traces with very high voltage differences together. This means that an isolation material is required to meet clearance standards. A 6 mm thick sheet of GP03 fiberglass was used for this purpose. The soldered capacitor leads on the back of the PCB were also sanded down to eliminate any sharp points to avoid electric field focusing and unnecessary height to allow for the PCB to be placed closer together [14, 15].

4.2.2 DC-Link Capacitors

The choice of capacitor for the dc-link capacitance was mostly dependent on the energy density. A large capacitance is needed because of the selected standard NPC type converter. This requirement lends itself to the use of electrolytic capacitors that despite being not as reliable and

not having as low parasitics relative to film or ceramic capacitors they do have great energy densities as well as significant current capabilities at large values of capacitance [11]. Film capacitors equal to 0.5% of the total bus capacitance were placed in parallel with the electrolytic capacitors to act as decoupling capacitors for the bus. The dc bus capacitors are shown in Figure 4-6 where 26 of the 3900 µF capacitors from Table 4-2 were connected in series to achieve a reasonable overvoltage margin of 14 kV for both the top and bottom dc-bus capacitances.

4.2.3 Filter Capacitors

Fourteen of the 3.5 µF capacitors chosen for the filter in Table 4-2 are placed in series to give a total capacitance of 214 nF. A model of the filter capacitors is given in Figure 4-7.

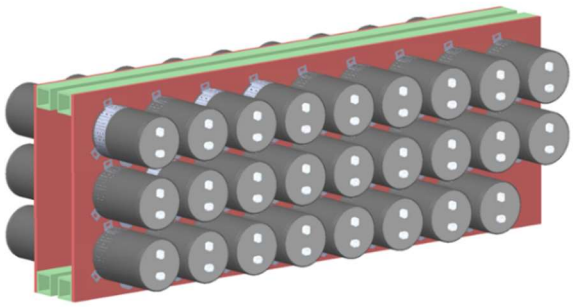


Figure 4-6. Model of the dc-bus capacitance.

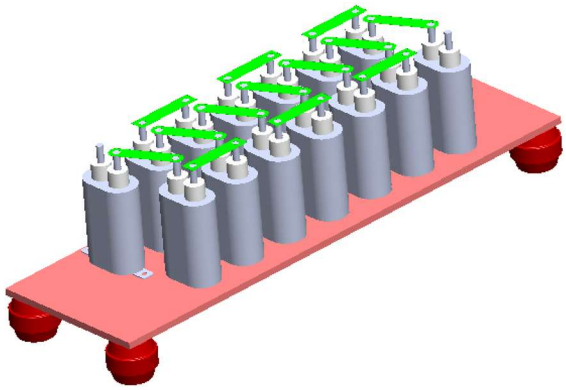


Figure 4-7. Model of the filter capacitance.

4.2.4 Filter Inductors

The filter inductors were designed based on [16] per the following:

1. Determine the power rating of the inductor, S_L . The MV-UCSC has a current rating, I, of 30 A. The voltage developed across the inductor, V, with a 30 A sinusoidal waveform and a target inductance, L, of 2.3 mH is

$$(30\ A)\left(377\ \frac{rad}{s}\right)(2.3\ mH) = 26\ V\ ,$$

and the apparent power rating of the inductor is then

$$S_L = (30\ A)(26\ V) = 780\ VA\ .$$

2. Calculate the area product, A_P, using

$$A_P = \frac{S_L}{K_f K_u f_g B_{ac} J} * 10^4\ , \tag{12}$$

where K_f, is the waveform factor, K_u is the window utilization factor, f_g is the current frequency, B_{ac} is the target flux density, and J is the chosen current density. The area product for the inductors of the MV-UCSC is then given by

$$A_P = \frac{780\ VA}{(4.44)(0.4)(60\ Hz)(1.3\ T)\left(200\ \frac{A}{cm^2}\right)} * 10^4\ = 281.67\ cm^4.$$

3. Select a core with an equal or greater area product, which is given by

$$A_P = A_C W_A\ , \tag{13}$$

where A_c is the cross sectional area of the core and W_A is the window area encompassed by the core. The Amorphous C-Core pair in Table 4-2 was chosen for the MV-UCSC inductors because the area product of this core is

$$A_P = (23\ cm^2)(42\ cm^2) = 966\ cm^4$$

4. Calculate the number of turns, N, using

$$N = \frac{V}{K_f A_C f_g B_{ac}} * 10^4 = \left\lfloor \frac{(26\ V)}{(4.44)(23\ cm^2)(60\ Hz)(1.3\ T)} * 10^4 \right\rfloor = 33\ turns \quad (14)$$

$$N =.$$

5. Determine the required air gap, l_{ag} using

$$l_{ag} = \frac{0.4\pi N^2 A_C}{L} * 10^{-8} = \frac{0.4\pi 33^2 (23\ cm^2)}{(2.3\ mH)} * 10^{-8} = 0.13\ cm\ . \quad (15)$$

6. Calculate the fringing flux factor, F_{ff} using

$$F_{ff} = 1 + \frac{l_{ag}}{\sqrt{A_C}} ln\left(\frac{2l_C}{l_{ag}}\right) = 1 + \frac{0.13\ cm}{\sqrt{23\ cm^2}} ln\left(\frac{2(10.5\ cm)}{0.13\ cm}\right) = 1.141\ . \quad (16)$$

7. Modify the number of turns to avoid saturation and losses due to fringing flux. The new number of turns, N_n, is the calculated as follows:

$$N_n = \sqrt{\frac{l_{ag} L}{0.4\pi A_C F_{ff}}} * 10^{-8} = \left\lfloor \sqrt{\frac{(0.13\ cm)(2.3\ mH)}{0.4\pi(23\ cm^2)(1.141)}} * 10^{-8} \right\rfloor = 31\ . \quad (17)$$

8. Check the flux density to make sure that it is near the target using

$$B = \frac{V}{K_f N A_C f_g} * 10^4 = \frac{(26\ V)}{(4.44)(31\ turns)(23\ cm^2)(60\ Hz)} * 10^4 = 1.388\ T\ . \quad (18)$$

This is close enough to the B_{ac} target of 1.3 to move forward.

9. Determine the bare wire area, A_{BW}, needed for the current rating using

$$A_{BW} = \frac{I}{J} = \frac{30\ A}{200\ \frac{A}{cm^2}} = 0.15\ cm^2\ . \tag{19}$$

An American Wire Gauge (AWG) equivalent wire rating of 4 AWG was chosen.

10. Use the chosen wire to calculate switching losses. The power loss is given by:

$$P_W = I^2 R_W\ , \tag{20}$$

where R_W is the equivalent resistance of the wire. The skin effect places a positive modifier on the dc resistance of a wire, so it is important to choose a Litz wire that will mitigate the skin effect. The skin depth for copper with an equivalent switching frequency of 100 kHz is 0.021 cm. The strands of the Litz wire need to be chosen such that the radius of the wire is equal to or less than the skin depth. This results in 38 AWG wire for the MV-UCSC inductor Litz wire. This is summarized in the inductor section of Table 4-2. The power loss in the Litz wire is the given by:

$$P_W = (30\ A)^2(0.0086348\ \Omega) = 7.77\ W.$$

11. Determine the losses in the core, P_C, using

$$P_C = K_C {f_g}^{\alpha} {B_{ac}}^{\beta} M_C\ , \tag{21}$$

where K_C, α, and β are constants given by the core material manufacturer based on curve fitting. M_C is the mass of the core. The power loss in the MV-UCSC inductor cores is

$$P_C = (6.5)(0.060\ kHz)^{1.51}(1.4\ T)^{1.74}(7.109\ kg) = 1.17\ W\ .$$

12. Calculate the losses due to the air gap using

$$P_G = K_l l_D l_g f_g {B_{ac}}^2\ , \tag{22}$$

where K_I is the thickness of the laminations and l_D is the width of the laminations. These losses for the MV-UCSC inductor are

$$P_G = (0.0023\ cm)(8.5\ cm)(0.134\ cm)(60\ Hz)(1.4\ T)^2 = 0.30\ W\ .$$

13. Determine the temperature rise, T_R using

$$T_R = 450\left(\frac{(P_W + P_C + P_G)}{A_S}\right)^{0.826}\ , \tag{23}$$

where A_S is the surface area of the core. The factor of 450 and exponent 0.826 are based on empirical analysis of iron based magnetic cores [16]. The temperature rise for the MV-UCSC inductors is

$$T_R = 450\left(\frac{(7.77\ W + 1.17\ W + 0.30\ W)}{1220\ cm^2}\right)^{0.826} = 8\ ℃.$$

14. Confirm that the chosen wire design will fit within the window area of the core. The estimated window utilization, $K_u{}^*$ is calculated using

$$K_u{}^* = \frac{N\pi}{0.9W_A}\left(\frac{D_W}{2}\right)^2\ , \tag{24}$$

where D_W is the diameter of the chosen wire from its datasheet. The insulation thickness must be considered. The 0.9 factor is included because the maximum area coverage achievable by circular cross sections of identical size is around 90%. The predicted window utilization for the MV-UCSC inductors is

$$K_u{}^* = \frac{N\pi}{0.9(42\ cm^2)}\left(\frac{0.812\ cm}{2}\right)^2 = 0.42\ .$$

15. Determine the length of the wire needed for the design. The length is calculated using

$$L_W = (MLT)N \ , \tag{25}$$

where MLT is the mean length of each turn of wire. For each new layer of wire this needs to be modified to reflect the added. The MLT for the MV-UCSC was multiplied by roughly 10 % to compensate for this increase. The length of wire required for each MV-UCSC inductor is roughly

$$L_W = 1.1(34.65\ cm)(31\ turns) = 1059\ cm\ .$$

A model of the inductor is shown in Figure 4-8. The cores are held together by two 16-cm long, 1-cm thick steel brackets on the top and bottom which clamp the C-cores together in conjunction with 20-cm long, M10 bolts. All of the aforementioned components and their designs were built and assembled within a 1 x 2 x 0.6 m standard equipment enclosure. A photo of the constructed prototype is shown in Figure 4-9.

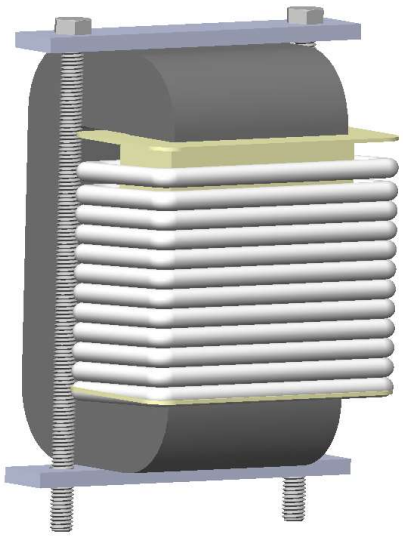


Figure 4-8. Model of the filter inductor.

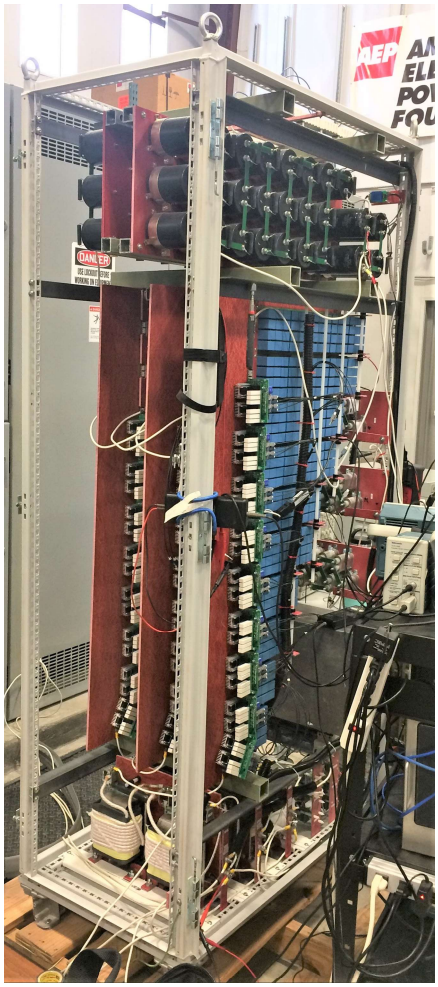


Figure 4-9. Photograph of the constructed MV-UCSC prototype.

4.2.5 Creepage and Clearance Requirements

Creepage and clearance requirements became of large concern due to the converter's high voltages and then need to fit all components in an enclosure of standard dimensions (1 x 2 x 0.6 m). Table 4-3 contains an overview of the required clearance requirements for 1 kV to 22 kV 60 Hz voltages [17]. IEC 60664-1 distinguishes between Inhomogeneous Fields and Homogeneous Fields. A homogeneous field is an electric field that is uniformly distributed between electrodes. This implies the use of two planes as the electrodes or two spheres with large radii relative to the distance between them. The use of the Homogeneous Field column is not applicable for most

cases. More likely is that there will be field focusing due to the shape of the electrode, whether this be a trace on a PCB or the corner of a screw terminal. Where possible, corners or sharp point in conductors should be rounded if clearance could be an issue.

Where clearance refers to the shortest distance between two points regardless of direction, creepage refers to the shortest distance between two points along the surfaces that connect them. Table 4-4 contains creepage distances for voltage between 0.1 kV and 25 kV. Pollution degrees (PD) included in this table refer to the type and level of environment contamination or pollution in which the electronics maybe be operating.

Table 4-3 Clearance distances versus voltage (kV)

	Inhomogeneous Field			**Homogeneous Field**	
Clearance (mm)	V_{RMS} (60 Hz)	V_{PEAK}	V_{PEAK} (Impulse)	V_{RMS} (60 Hz)	V_{PEAK} (Impulse)
1.0	1.06	1.50	1.95	2.47	3.50
3.0	2.21	3.13	4.07	6.32	8.94
10	4.95	7.00	9.10	17.7	25.0
25	10.8	15.3	19.9	41.2	58.3
40	16.2	22.9	29.8	63.6	90.0
60	22.8	32.3	42.0	92.6	131.0

Table 4-4. Creepage distance versus voltage

	Minimum Creepage Distance (mm)								
RMS Voltage (kV)	PWM		Other						
	Pollution Degree								
	1	2	1	2			3		
	All Material Groups	All Except IIIb	All Material Groups	Material Group I	Material Group II	Material Group III	Material Group I	Material Group II	Material Group III
0.1	0.10	0.16	0.25	0.71	1.00	1.40	1.80	2.00	2.20
0.25	0.56	1.00	0.56	1.25	1.80	2.50	3.20	3.60	4.00
0.63	1.8	3.2	1.8	3.2	4.5	6.3	8.0	9.0	10.0
1.0	3.2	5.0	3.2	5.0	7.1	10.0	12.5	14.0	16.0
2.0	-	-	7.5	10.0	14.0	20.0	25.0	28.0	32.0
6.3	-	-	25.0	32.0	45.0	63.0	80.0	90.0	100.0
12.5	-	-	50.0	63.0	90.0	125.0	-	-	-
20.0	-	-	80.0	100.0	140.0	200.0	-	-	-
25.0	-	-	100.0	125.0	180.0	250.0	-	-	-

The higher the pollution degree the higher the creepage and clearance distances that will be required. PWM in this case stand for Printed Wiring Material which is the category in which PCBs fall. The values for PWM creepage requirement disappear after 1 kV. This is because the creepage requirements after 1 kV converge to those of PD 1 in the "Others" category.

Also introduced are Material Groups that are arranged according to that materials comparative tracking index (CTI) in either group I, II, IIIa, or IIIb. The CTI of a material is a measure of the breakdown voltage of a material and the level of conductive carbon "tracks" that form on the material in the presence of heat produced from electrical arcing. These tracks can make the material a worse insulator over time. The CTI of a material is measured using a standardized process as in IEC 60601-1:2005.

The MV-UCSC design has a selected pollution degree of 2 which is defined as "Only non-conductive pollution occurs except that occasionally a temporary conductivity caused by condensation is to be expected." This was chosen because the location for the MV-UCSC was indoor at a testing facility that can sometimes experience elevated relative humidity levels and dust. The material group that was chosen was Material Group I as the majority of structural and insulative materials chosen were variations of fiberglass. For example, GPO-3 fiberglass has a CTI of at least 600 which puts it in that category.

Examples from [17] for creepage and clearance paths are shown in Figure 4-10. In Figure 4-10(a) the most basic example is shown with two electrodes on the same flat surface. The clearance is shown in blue and the creepage is shown in green; they are the same distance in this case. Using a notch to increase the creepage distance is demonstrated in Figure 4-10(b). However, there is a minimum hole size, in red, that can count towards creepage based on the PD. This means that the use of microscopic slots in a surface do not contribute to creepage in

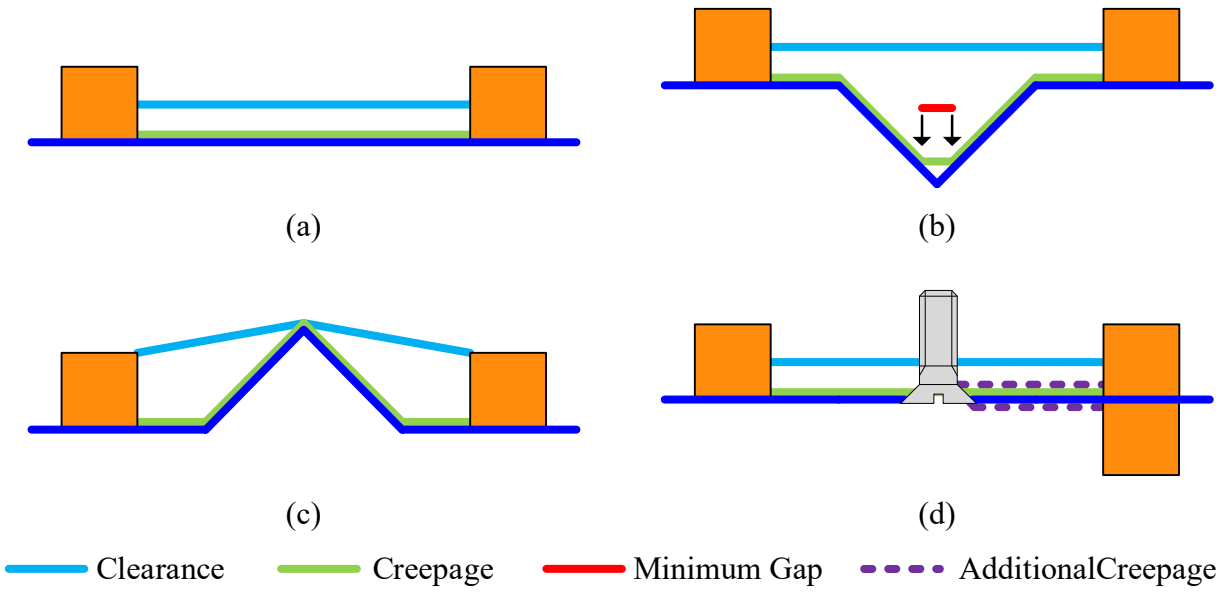


Figure 4-10. Clearance and creepage examples.

practice. The third example of increasing creepage and clearance is given in Figure 4-10(c). This partition only works if it has a dielectric withstand voltage rating that is higher than the voltage between the two electrodes, otherwise an arc might travel through the insulating partition. Care must be taken with mounting hardware as well. Highly conductive materials like aluminum, copper, and various steel alloys will not contribute to either the clearance or the creepage distances between two objects as shown in Figure 4-10(d). Additionally, the bolt in this figure now provides an additional clearance and creepage path to electrodes on the other side of the material on which the electrodes are mounted, shown in a dotted purple line.

4.3 MV-UCSC Controller Design

The controller of the MV-UCSC must perform the following functions:

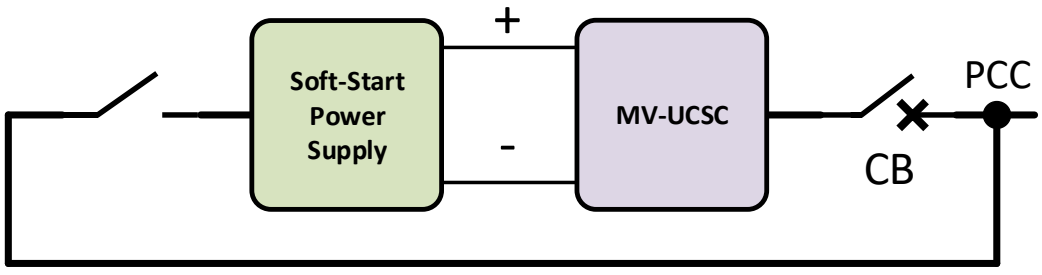
4.3.1 Converter Start-up

The converter is initially completely discharged and disconnected from the grid by a medium-voltage grid-tie breaker. An external low-power supply is used to ramp the dc bus to a

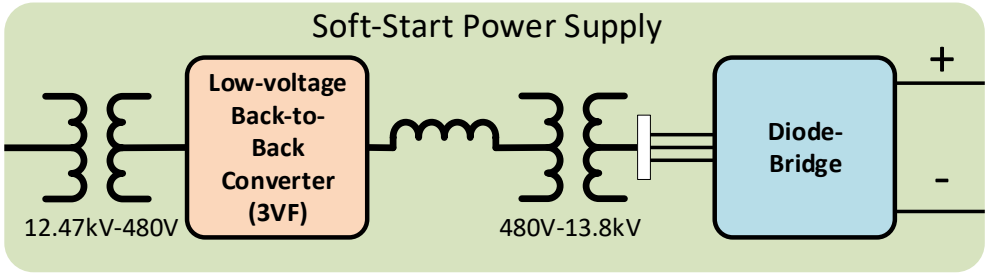
voltage close to its nominal value. While the dc-bus voltage increases the soft-start functionality of the switching positions is initiated (i.e. Mode 2 in Appendix B). The start-up circuitry as it relates to the MV-UCSC is illustrated in Figure 4-11.

Using the capabilities available at NCREPT, a power transformer is used to step the grid voltage down from 12.47 kV to 480 V. Then, a back-to-back converter (3VF) is used to ramp the voltage from 0 to 500 V_{LL}. This ramped voltage is then stepped-up by another power transformer from 480 V to 13.8 kV and rectified by a medium-voltage 24 kV_{dc} diode bridge that was built for this project. The required power for the start-up circuit is relatively low (less than 3 kW) so the size of this circuit can be relatively small. This setup is displayed in Figure 4-11.

Before the instant of grid-connection of the converter, the current controller is run using the sensed grid voltage and a virtual impedance that matches the LCL filter plant (Mode 2). This biases the controller to an appropriate operating point before connecting to the grid and helps to



(a)



(b)

Figure 4-11. The configuration of the soft-start mechanism for the MV-UCSC.

reduce the inrush current at the time of grid-connection. Upon signaling to the grid-tie breaker to close, the controller waits for the "close" delay time of the breaker and then switches from current predicted from the virtual filter and then begins to use the sensed output current. The converter is now under steady-state operation (Mode 4 in Appendix B).

4.3.2 Steady-state Operation of the MV-UCSC

The MV-UCSC Current Controller

Control of the converter was done in the stationary α-β reference frame on a single-phase basis using a proportional-resonant controller (PR) [18]. This is equivalent to a PI controller in the d-q rotating reference frame [19]. The PR controller transfer function is defined in the z-domain as follows:

$$G_{PR}(z) = k_p\left(1 + \frac{a}{T_r}\frac{z^2 - 1}{z^2 - 2z\cos\left(\frac{2\pi\omega_0}{\omega_s}\right) + 1}\right), \tag{26}$$

where

$$a = \frac{\sin(\omega_0 T_s)}{2\omega_0}, \tag{27}$$

$$\omega_s = \frac{2\pi}{T_s}. \tag{28}$$

and k_p is the proportional term, T_r is the resonant gain term, T_s is the sampling period, and ω_0 is the frequency of the grid voltage as measured by a frequency-lock-loop (FLL) [20]. This keeps the PR controller tuned to the appropriate frequency when the grid frequency varies from nominal.

The optimum value for k_p and T_r based on a desired phase margin of 45 degrees at a crossover frequency of $\omega_s/12$ are

$$k_p = \frac{\omega_s L_T}{12}, \tag{29}$$

$$T_r = \frac{120}{\omega_s}. \tag{30}$$

where L_T is the total inductance of the LCL filter. For the MV-UCSC, the value of k_p, T_r, and L_T are 0.144517, 0.318302, and 0.0046, respectively. The simplified control block diagram of the PR controller is shown in the z-domain in Figure 4-12, where the plant is an approximation of the LCL output filter.

The Frequency-Lock Loop

The FLL is based on a Double Second Order Generalized Integrator Quadrature Signal Generator (DSOGI-QSG) [20]. The three-phase voltages are transformed to the α-β domain using the Clarke Transform as follows:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ 0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{31}$$

where v_a, v_b, v_c are the grid voltage for phases A, B, and C, respectively.

The v_α waveform is fed through one SOGI-QSG and the v_β waveform is fed through

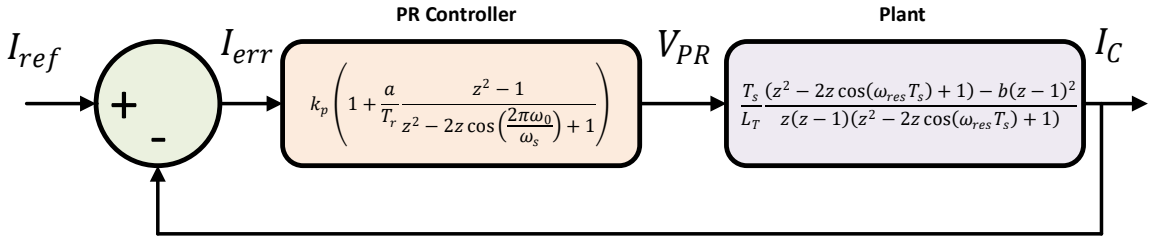


Figure 4-12. Block diagram for PR-based current controller.

another. Using the quadrature outputs, q_α and q_β and the error of the direct components ε_α and ε_β, the angular frequency of the grid, ω_0, is estimated and fed back into the SOGI-QSGs to tune them based on frequency shifts. This feedback gives the ability to lock onto the grid-angular frequency. The estimated angular frequency ω_0 is biased by ω_s, the nominal angular grid frequency, to speed up the FLL. The block diagram for the DSOGI-QSG FLL is shown in Figure 4-13. The direct outputs v_α' and v_β' can be used in an inverse Clarke transform to give filtered grid voltages. For the MV-UCSC, a value of $K = \sqrt{2}$ was chosen and a value of 50 was used for Γ.

The transfer functions in the z-domain for the SOGI-QSG direct and quadrature outputs are from [21]:

$$G_{SOGI,d}(z) = \frac{b_0 + b_2 z^{-2}}{1 - a_1 z^{-1} + a_2 z^{-2}}, \tag{32}$$

$$G_{SOGI,q}(z) = \frac{b_0 + b_2 z^{-2}}{1 - a_1 z^{-1} + a_2 z^{-2}}, \tag{33}$$

$$b_0 = \frac{x}{(x + y + 4)}, \tag{34}$$

$$b_2 = \frac{-x}{(x + y + 4)}, \tag{35}$$

$$a_1 = \frac{2(4 - y)}{(x + y + 4)}, \tag{36}$$

$$a_2 = \frac{x - y - 4}{(x + y + 4)}, \tag{37}$$

$$qb_0 \frac{ky}{(x + y + 4)}, \tag{38}$$

$$qb_1 = \frac{2ky}{(x + y + 4)}, \tag{39}$$

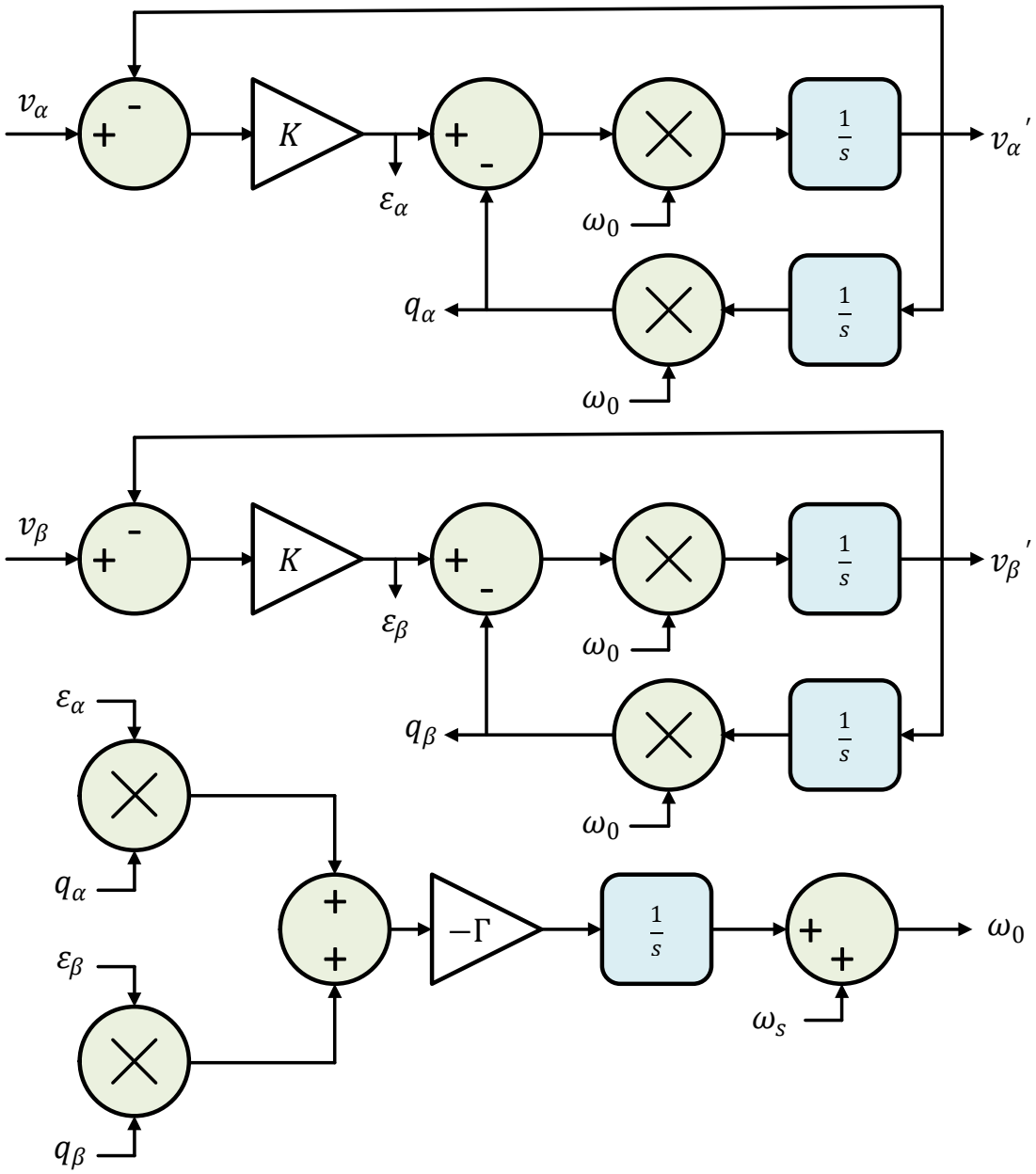


Figure 4-13. Block diagram for DSOGI-QSG FLL.

$$qb_2 = \frac{ky}{(x+y+4)}, \tag{40}$$

$$x = 2k\omega_0 T_s\,, \tag{41}$$

$$y = (\omega_0 T_s)^2 \,, \tag{42}$$

where k is a chosen constant to determine the SOGI-QSG response time and selectivity and T_s is the sampling period. For the MV-UCSC, the constant $k = \sqrt{2}$ and $T_s = 0.0001$ s.

The MV-UCSC DC-Bus Voltage Controller

The dc-bus voltage controller is enabled using the value of the dc-bus voltage measured at the connection as the initial reference. If needed, the dc-bus reference is then ramped to a higher value. Because of the split dc-bus and potential mismatch in passive component values, a dc-bus voltage offset controller is used to correct any minor deviations that may occur in the dc-bus capacitor voltages. The dc-offset control block diagram is shown in Figure 4-14. The plant was derived to give the response in voltage of the bottom dc capacitor, V_{busN}, to changes in the dc offset of the PWM control waveform, d^*. For the MV-UCSC, $k_p = 0.0002$ and $k_i = 0.001$.

A filtering function $F(s)$ was used to prevent this controller from reacting to normal dc-bus voltage ripples. The function $F(s)$ is made up of notch filters at the nominal grid frequency, ω_s, and $2\omega_s$ as well as a low-pass filter at $5\omega_s$. The transfer function for the notch filters and low-pass filters are

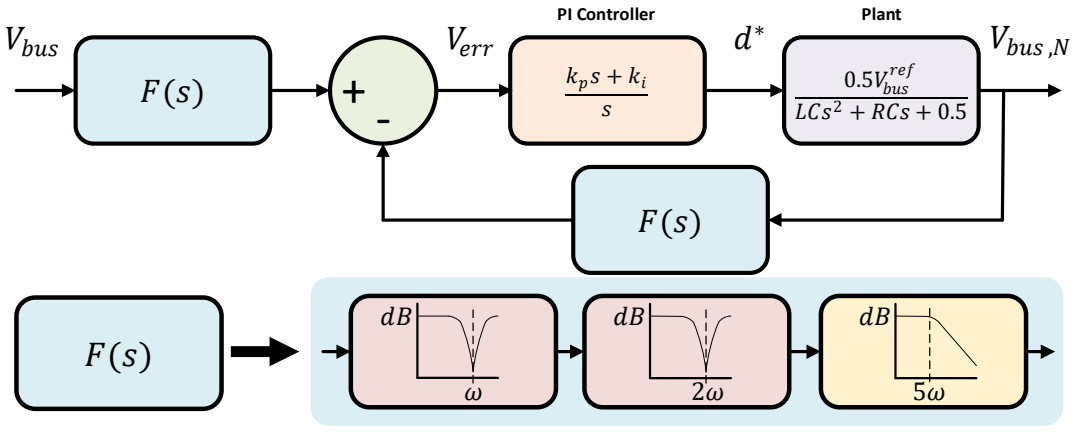


Figure 4-14. Model of the dc-offset controller.

$$G_{nf}(s) = \frac{s^2 + 2\zeta_2 \omega s + \omega^2}{s^2 + 2\zeta_1 \omega s + \omega^2}, \tag{43}$$

$$G_{lp}(s) = \frac{1}{\tau s + 1}, \tag{44}$$

where $\zeta_2 << \zeta_1$, ω is the frequency to be eliminated by the notch filter, and τ is the inverse of the cutoff angular frequency for the low-pass filter. For the MV-UCSC, ζ_2 = 0.00001, ζ_1 = 0.1. ω for the first notch filter is 377 rad/s and 754 rad/s for the second, τ takes the value of 0.0005305.

These transfer functions in the z-domain become

$$G_{nf}(s) = \frac{z^2 + (2\zeta_2 \omega T_s - 2)z + \left(-2\zeta_2 \omega T_s + \omega^2 {T_s}^2 + 1\right)}{z^2 + (2\zeta_1 \omega T_s - 2)z + \left(-2\zeta_1 \omega T_s + \omega^2 {T_s}^2 + 1\right)}, \tag{45}$$

$$G_{lp}(s) = \frac{\left(1 - e^{-\frac{T_s}{\tau}}\right) z}{z - e^{-\frac{T_s}{\tau}}}. \tag{46}$$

4.3.3 The Control Module

A photo of the control module is shown in Figure 4-15. High-level and primary control is performed by a TMS320F28379D DSP controlCARD™ from Texas Instruments Incorporated. Fault signal monitoring was performed by a MachXO3L/LF-6900C FPGA from Lattice Semiconductor. VHDL code to emulate the TI C2000 DSP's ePWM architecture was developed to perform the PWM inside another FPGA (MachXO2/LCMXO2-7000HC from Lattice Semiconductor). Serial communication was used between an external computer and the DSP. Because of the required data transfer rates involved, a 21-bit parallel port handshaking protocol (5 address bits and 16 data bits) was developed for faster communication between the DSP and the FPGA. Appendix B gives a deeper overview of the control code.

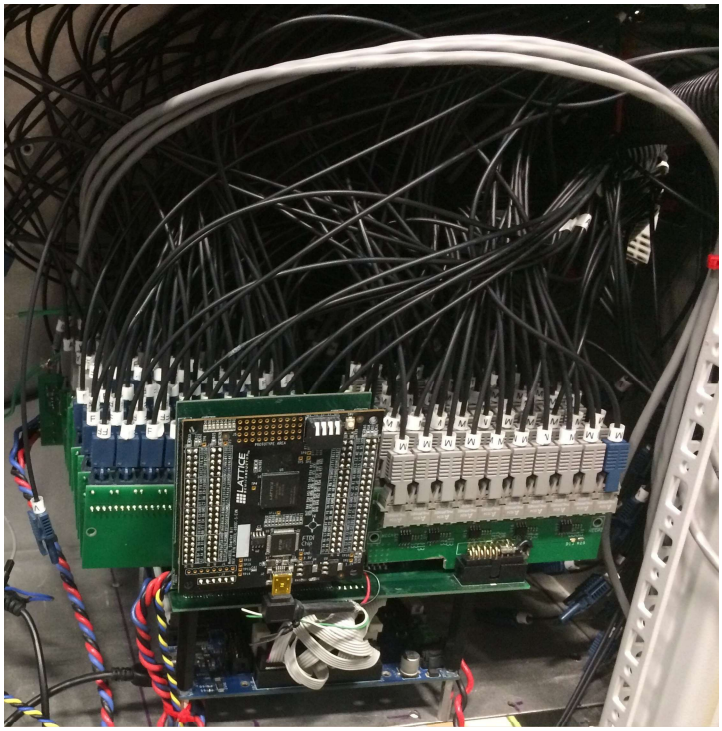


Figure 4-15. Photograph of the control module.

To remove the isolation requirements for a voltage sensor, each switching position was outfitted with a duty-cycle encoded voltage sensing circuit. This duty-cycle encoded signal is transmitted by fiber optic to the FPGA with a duty-cycle detector to decode the voltage measurement.

A carrier frequency of 32 kHz for this encoding was chosen considering the trade-offs between precision and bandwidth. This feedback mechanism allows for closed-loop compensation of the flying capacitor voltages [22, 23]. The control architecture for the control module presented in Figure 4-16 provides an idea of magnitudes of the control tasks. There are 60 PWM signals to the main switches and another 60 PWM signals to the auxiliary switches in the self-powered circuits from Figure 4-3. The flowchart for the operation of the DSP as well as primary and secondary FPGAs are given in Figure 4-17 and Figure 4-18, respectively.

4.4 Grid-Connected Simulations of the MV-UCSC Prototype

The 13.8 kV feeder presented in Figure 4-1 was simulated with Matlab/Simulink™ using a C-code based controller that matches the code used in the prototype. The system as constructed within Simulink™ is displayed in Figure 4-19. As described in Figure 4-1, a three-phase grid provides power to a load with the MV-UCSC connected in parallel.

The c-code controller and other supporting blocks that together make the control system for the simulation are shown in Figure 4-20. On the left are the sensor inputs to the MV-UCSC

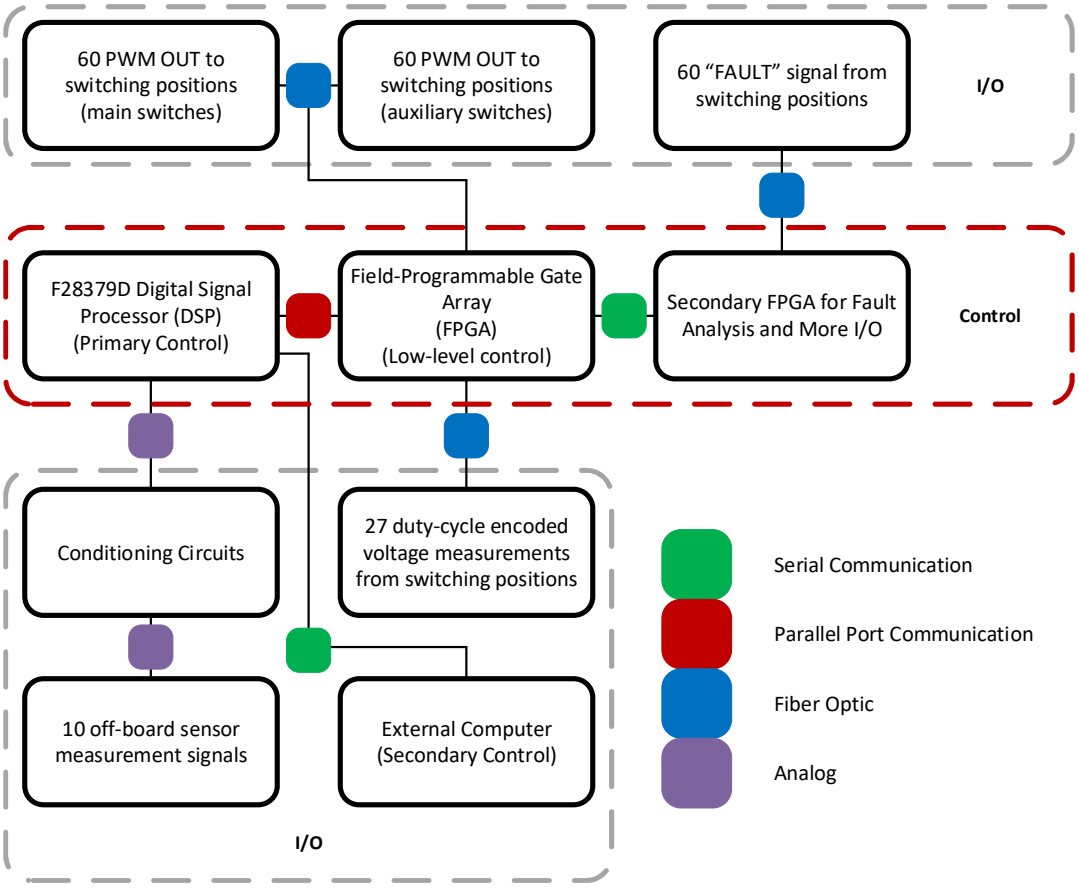


Figure 4-16. The controller architecture of the control module.

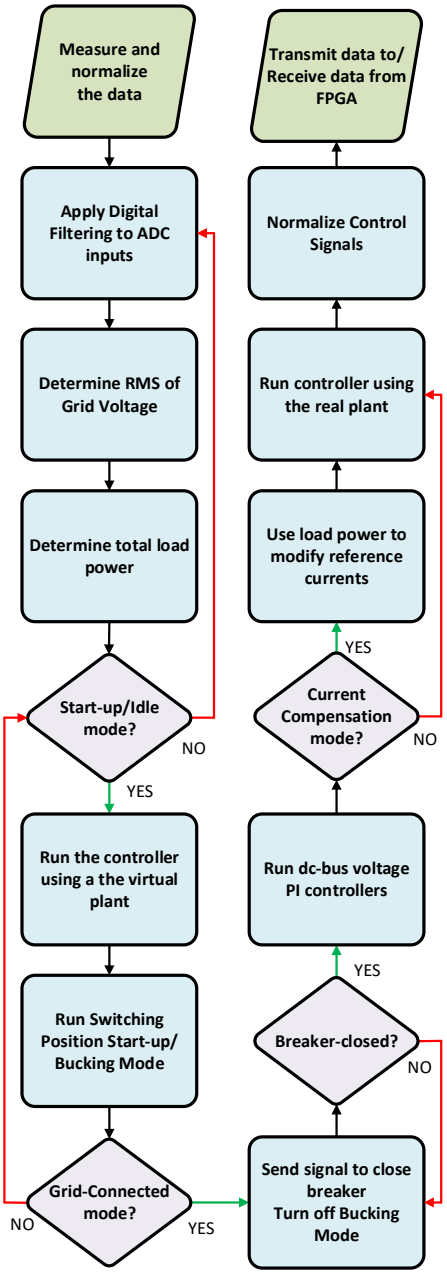


Figure 4-17. The control architecture of control module.

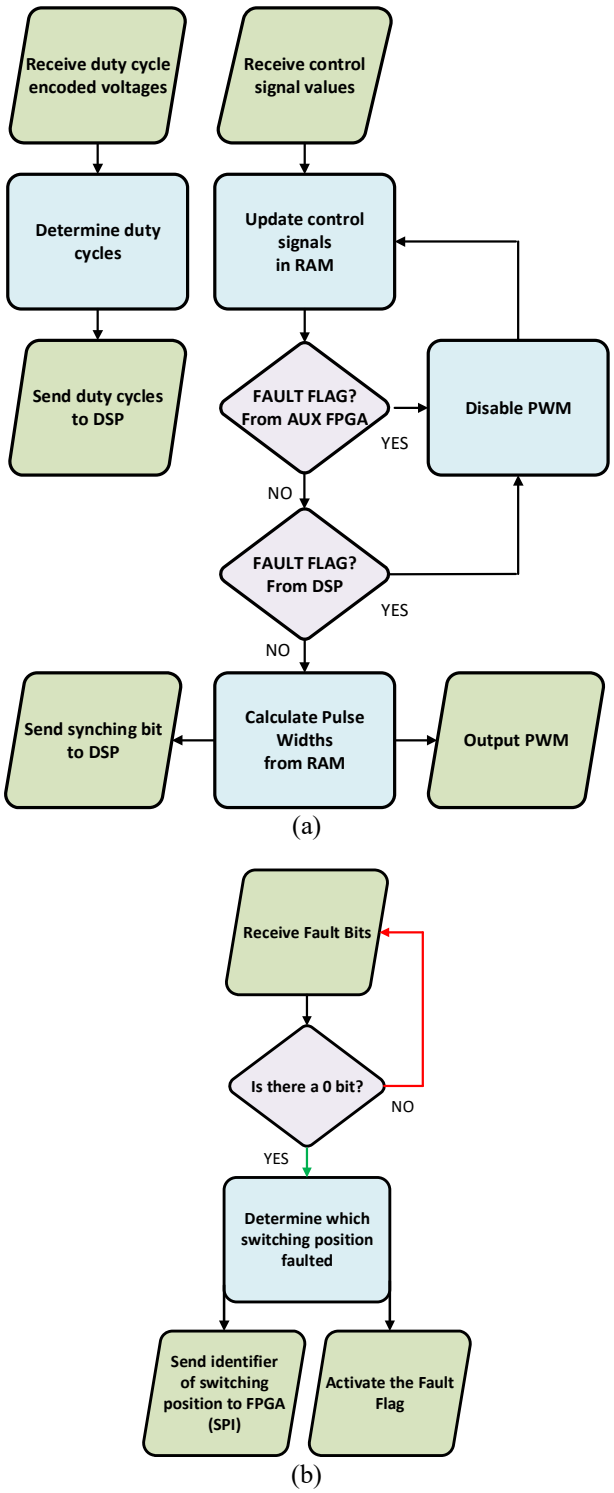


Figure 4-18. Flowchart for (a) the primary FPGA and (b) the secondary FPGA.

controller. A signal conditioning block performs the function of the external conditioning circuit as well as emulating the quantization and resolution of the DSP ADC. External “Start” and “Connect” signals are also routed to the C-code controller to represent the serial-communication-based mode changes that would occur in the actual prototype. The controller block then acts as the DSP and outputs a compare value for the PWM module, a PWM “enable” signal, a signal to trigger the closing of the breaker and some DEBUG outputs for testing modifications to the controller.

The DSP-PWM emulates the hardware PWM modules that were built in an external FPGA. In the actual system, the DSP sends a PWM “enable” signal to the FPGA to turn-on or

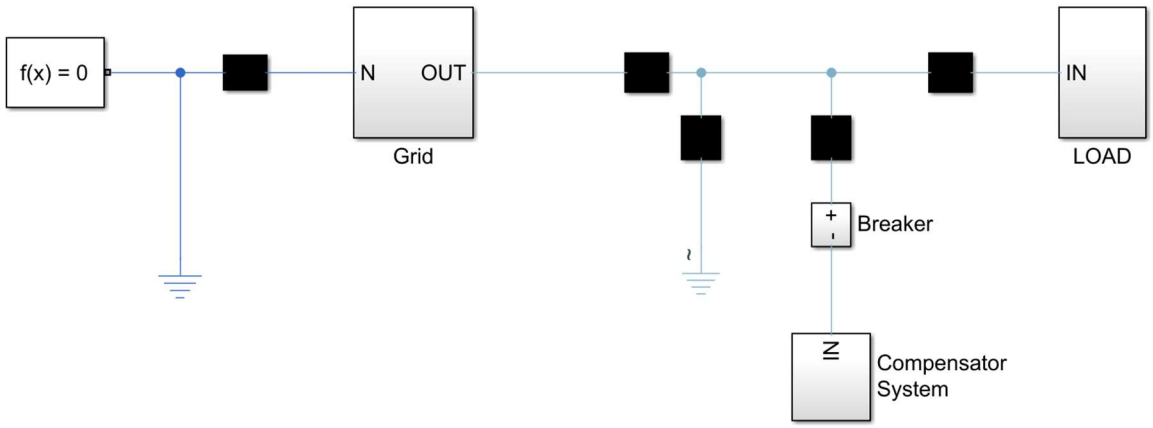


Figure 4-19. The MV-UCSC test feeder in Simulink™.

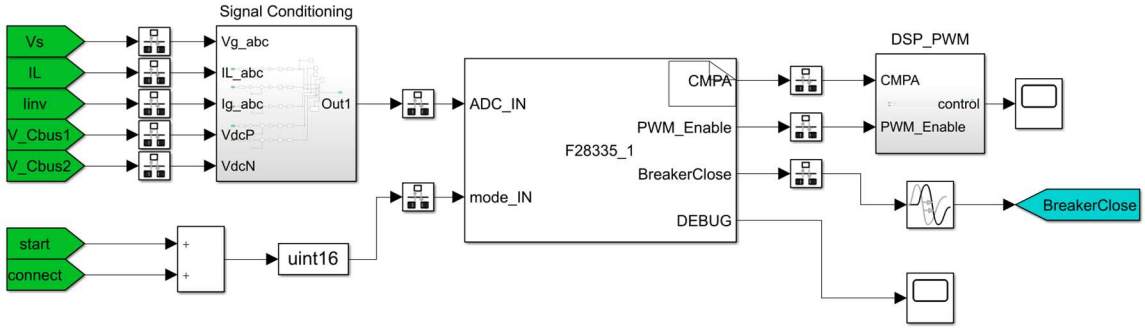


Figure 4-20. The MV-UCSC controller in Simulink™.

turn-off the PWM signal to the MV-UCSC switching positions and the “BreakerClose” signal is routed to a relay that controls the MV breaker that ties the MV-UCSC to the grid.

The load currents are given in Figure 4-21. Each phase is loaded with 3 A of reactive current and phase A has an additional loading of 20 A of active current while the loads on phases B and C absorb no real power. These currents result in negative-sequence current component of 9.4 A and zero-sequence current component of 9.4 A. The steady-state behavior of the MV-UCSC phase currents is shown in Figure 4-22. These currents are unbalanced and out of phase such that the upstream currents are balanced. The resulting substation currents are in Figure 4-23. The neutral current seen by the substation has been reduced from a peak of 24 A_{peak} to effectively zero reflecting a reduction of the zero-sequence current to a negligible value. The negative-sequence current have also been reduced to negligible values.

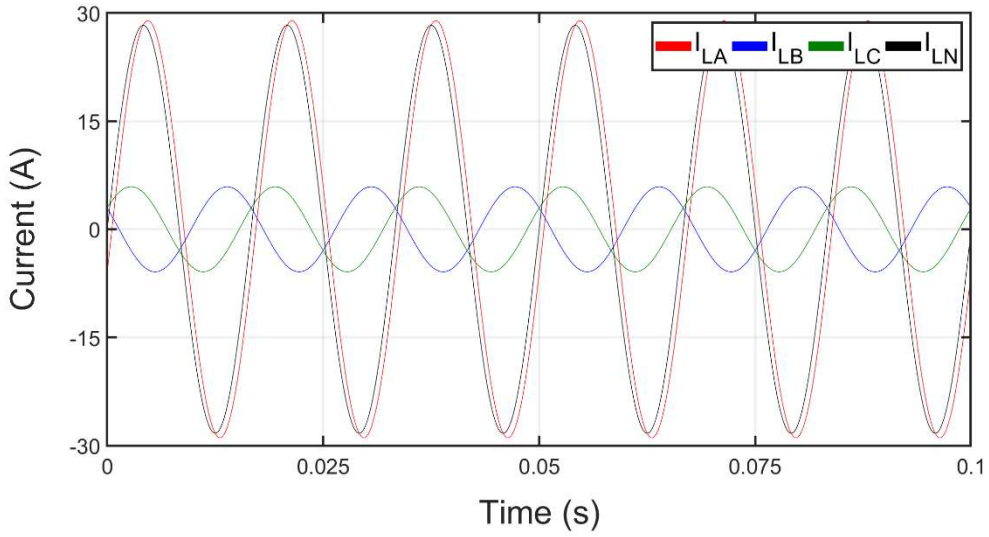


Figure 4-21. Load currents during MV-UCSC compensation.

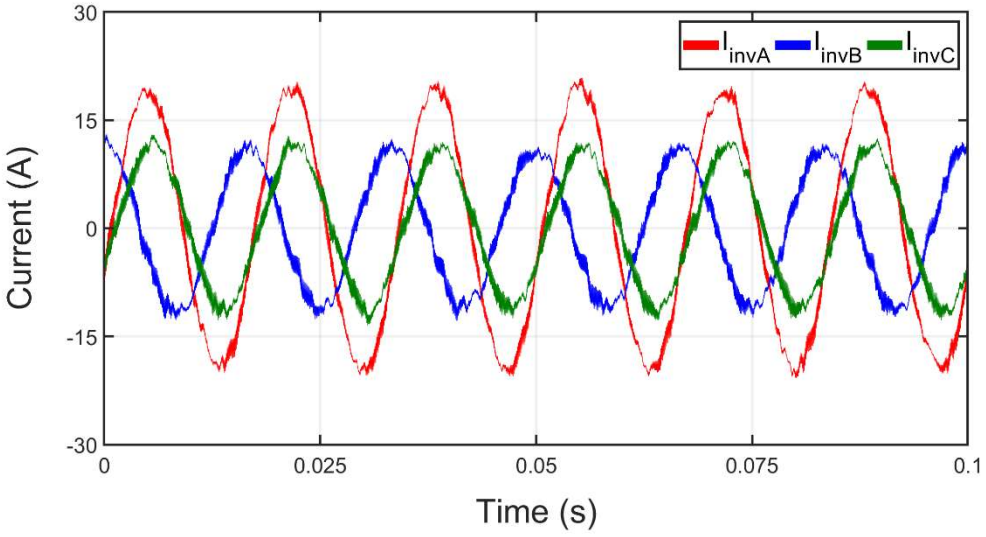


Figure 4-22. Steady-state currents of the MV-UCSC during MV-UCSC compensation.

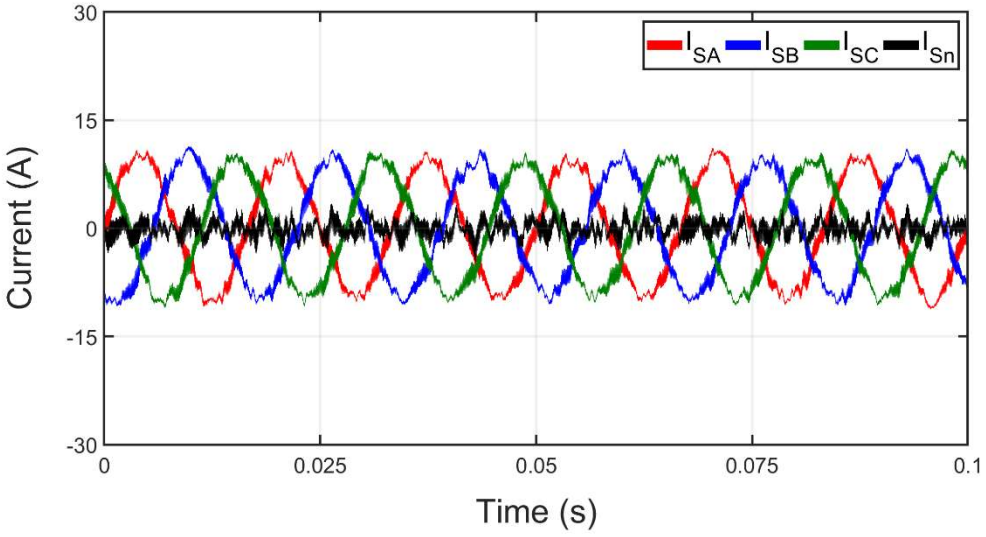


Figure 4-23. Steady-state substation currents during MV-UCSC compensation.

In addition, the power factor of the substation currents has been compensated to unity. In these simulations, the entirety of the load currents are processed by the UCSC, so the THD of the

substation currents is essentially equivalent to that of the MV-UCSC. Normally, the UCSC would process a fraction of the total load current.

The voltage balance between the flying capacitors of each level is illustrated in Figure 4-24. Each voltage level stays nearly constant with an acceptable ripple of ±5%. In Figure 4-25, the converter voltage before the filter (in red) and the grid voltage (in black) are compared to give context to the converter output waveforms. An FFT of the output current of the MV-UCSC is given in Figure 4-27 showing that the converter as designed has a THD less than 5% at 100% of the designed current rating which meets the overall total-demand-distortion (TDD) requirements for grid-connected equipment from IEEE 1547-2003 [24]. The height of each bar in the FFT represents the peak value.

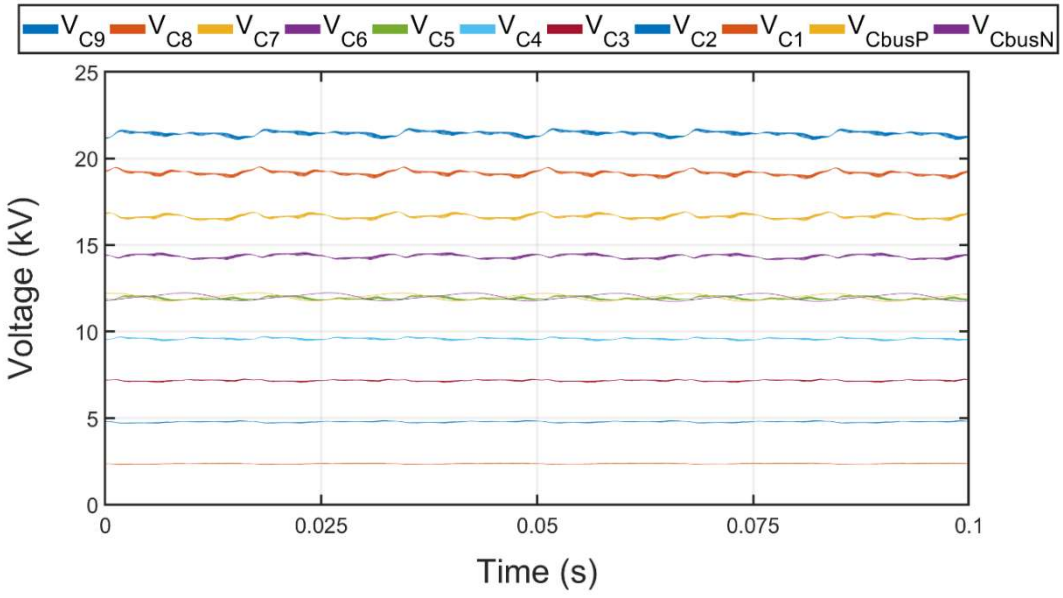


Figure 4-24. Steady-state flying capacitor voltages during MV-UCSC compensation.

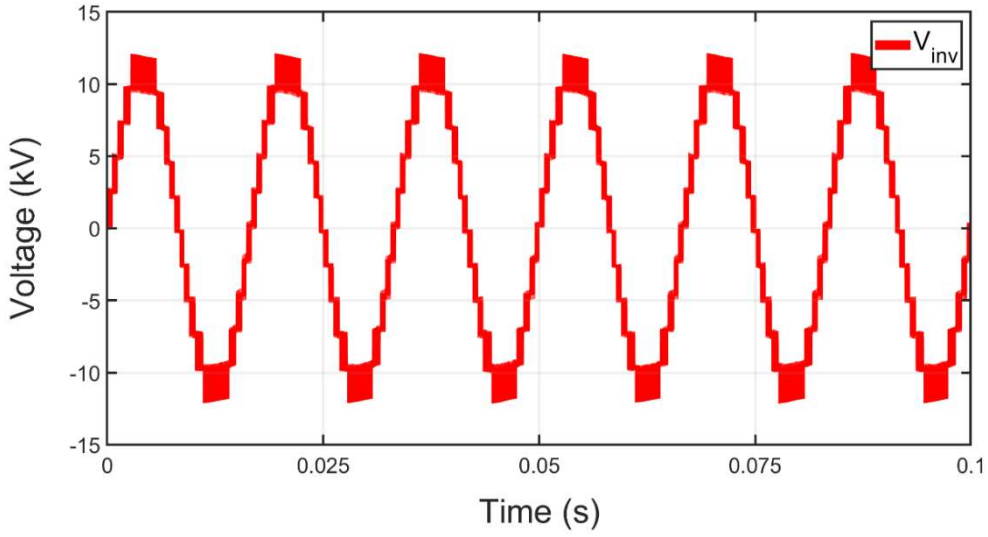


Figure 4-25. Steady-state MV-UCSC output voltage line-to neutral during compensation.

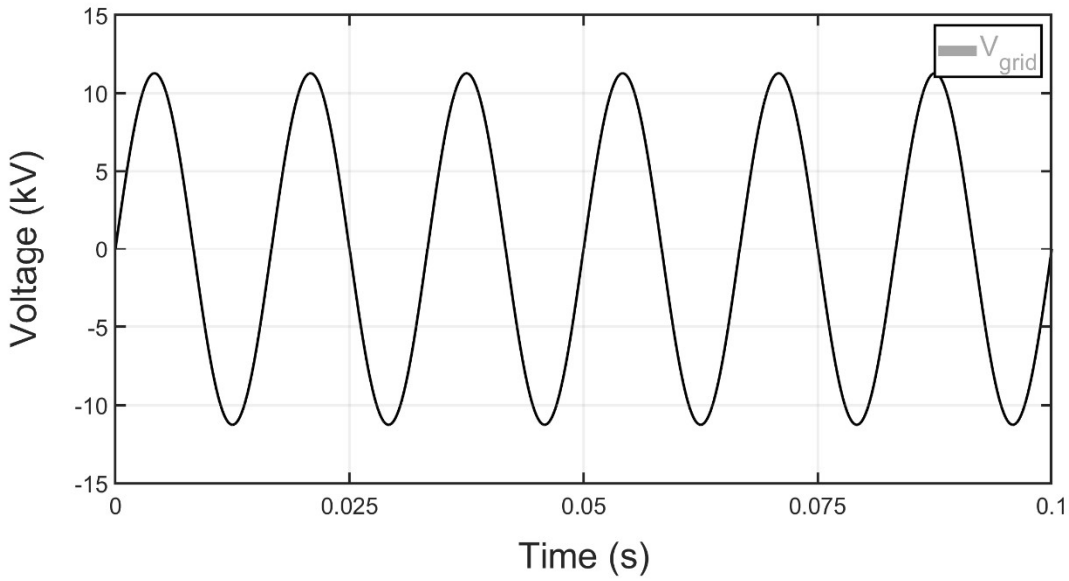


Figure 4-26. Grid voltage line-to-neutral during MV-UCSC compensation.

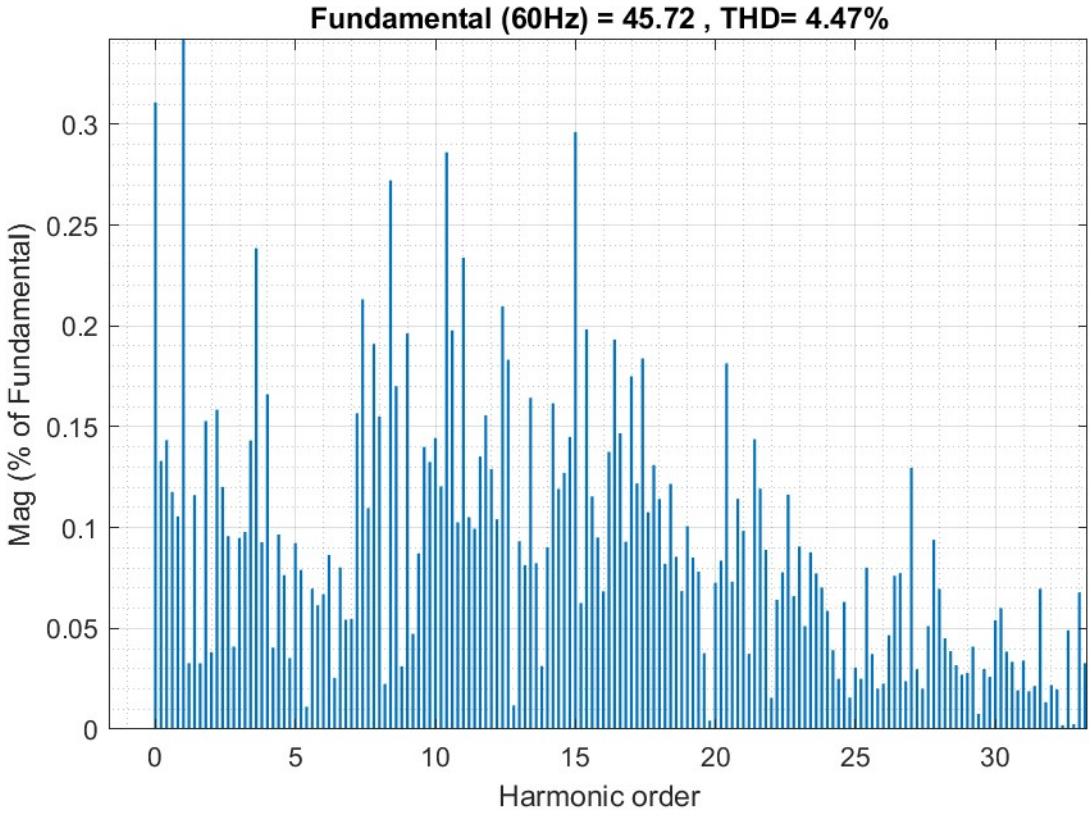


Figure 4-27. FFT of the steady-state converter current.

4.5 Concluding Remarks

This chapter presented each major aspect of the design, control architecture, simulations and construction of an 11-level 13.8 kV, 750 kVA flying capacitor converter for current compensation of distribution feeders. Simulation results for the MV-UCSC were provided to demonstrate its ability to compensate for negative- and zero-sequence currents as well as reactive currents upstream from the PCC. The control functions within these simulations were done using C-code to reflect the real-world implementation in the DSP-based controller.

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CHAPTER 5

A MODULAR SWITCHING POSITION WITH VOLTAGE-BALANCING AND SELF-POWERING FOR SERIES DEVICE CONNECTION

V. Jones, R. A. Fantino, and J. C. Balda, " A Modulat Switching Position with Voltage-Balancing and Self-Power for Series Device Connection," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

5.1 Abstract

Medium-voltage converters, especially those making use of SiC devices, require high common-mode voltage immunity and resilience against associated high dv/dt across multiple isolation barriers. A truly modular and common-mode immune switching position could be beneficial for these applications. The design of a modular switching position is presented here for series connection of power semiconductors with voltage-balancing and self-powered-gate capabilities. The designs of the voltage-balancing and self-powered circuits are described followed by simulations and testing of a 3.3-kV switching position formed by two 1.7-kV SiC MOSFETs in series. Testing results demonstrate the ability of the proposed switching position to balance the voltage across series-connected MOSFETs even if the gate signals of the series-connected devices are not perfectly synchronized, while powering themselves directly from the $_{OFF}$-state voltage across them. Additionally, a start-up circuit for the switching position is proposed and experimentally confirmed.

5.2 Introduction

Continued advances in high-voltage SiC devices, and the move towards medium-voltage converters with multilevel topologies using these devices, call for a truly modular switching position. In this paper a switching position is defined as a power semiconductor device used in

the primary power processing of a converter along with all the associated circuitry required for this device's operation. Connecting devices in series to realize a high-voltage switching position can make it possible to increase the switching frequency and reduce the position on-state voltage drops at the expense of higher complexity [1, 2]. Such a switching position requires mitigation of the common-mode current issues for power and control signals [3]. It also requires compensation for imperfect static and dynamic voltage sharing between series-connected devices [1].

Traditional methods by which the gate driver power supplies are designed becomes a challenge at medium-voltage levels (e.g., 13.8 kV) because the isolation required can be greater than 25 kV and may need to withstand dv/dt's across this isolation barrier greater than 100 kV/μs. This performance requires careful design of galvanically isolated power supplies and sometimes non-traditional supply configurations that can result in large and expensive solutions.

This problem has been reported extensively in literature [3-5]. Power-over-fiber (POF) systems can be used but these are large and relatively inefficient [6, 7]. Photonically-switched power devices have also been explored, but this does not provide power for any diagnostic circuitry surrounding the device [8]. Reference [9] proposes a bootstrapping method to provide power to all upper devices in a stack by using a single power supply on the lower switch. This method removes the need for a power supply at each power device for gating but doesn't eliminate the common-mode parasitic current paths due to the bootstrap diode capacitances. Inductive power transfer for power switch positions is used in [10] with an emphasis on low cost and reliability. The drawback for this method is low efficiency as the distance between primary and secondary windings increases and thus requires an optimization between efficiency and insulation/size.

Self-powered gate driver topologies have been suggested in [11-13]. This allows for the removal of the common-mode voltage issue with optical isolation being used for control signals. Reference [11] uses the natural switching of the power device to provide power by pairing a resonant circuit with a resonant gate-drive to minimize the power consumption. However, the resonant gate-drive may not be suited for active gate control as discusses below. A linear-regulator-based self-powered mechanism is proposed in [12] which has low efficiency, but its snubber-like properties can be used to decrease switching losses.

The most obvious power solution for a modular switching position would be to place an external high step-down commercial power supply across each power device along with a snubber which acts as an input filter. Such a setup is suggested in [14]. The drawback is the constant-power-load nature of an off-the-shelf power supply which may contribute to static voltage imbalance between devices in a leg. Therefore, that work suggests a compensating algorithm to overcome this effect, though this requires voltage sensing of the input filter for each power supply in a stack. A similar solution is given in [15] for a modular multilevel converter (MMC) building block with self-powering. This type of solution is elegant for the MMC but can suffer from the same constant-power load problem due to the local feedback mechanism and extrapolation of the solution to other converter applications is not obvious.

References [1, 2, 16-21] proposed several different voltage-balancing circuits for connecting devices in series. Passive snubber circuits was used in [2] to form a 6.5-kV SiC MOSFET switching position with four series-connected 1.7-kV SiC MOSFETs. A super-cascode configuration SiC JFETs to form a 5kV switch was explored in [22] and SiC MOSFETs were used to form a 7.2 kV switch in [23]. These can provide low on-resistance and fast switching times, but commercially are still limited to relatively low voltages.

A quasi-active gate control is introduced in [21] which uses balancing resistors and bootstraps a low-side gate signal to trigger all devices in a stack and ensure similar gate signal. Though the circuit is simple it requires care to design against circuit resonances and provides a common-mode current path through the RC networks to the gate drive circuitry. Similar solutions are presented in [24, 25].

An active gate driver with an FPGA-based closed-loop gate-current controller in [16] adjusts the switching speeds based on the voltage detected across the power switch. Reference [17] presented a similar solution but using an analog feedback mechanism rather than digital. This sort of feedback requires clean on-board voltage measurements and may be susceptible to excess delays.

A resonant network with coupled inductors is presented in [18] for voltage balancing two series-connected devices. Reference [19] suggests using coupled inductors to guarantee the same gate pulses. The drawbacks are the introduction of leakage or parasitic inductance into the gate path, and the economics of custom transformer design for each application.

Voltage balancing, loss minimization, and modularization were the focus of [26] which suggests a resonant snubber that is clamped by a voltage source paired with a gate signal sharing network. The disadvantages involve the introduction of an extra series inductance in the load current path, and the "daisy chain" constructed for the gate signals that may decrease the switch fault resiliency of a stack of power devices.

Reference [27] uses an open-loop active circuit to inject current into the gate when an overvoltage condition occurs. The active component of this circuit allows for low losses when the voltages are balanced but additional semiconductors may make the circuit less reliable. In an attempt to make a completely modular and "stackable" switching position, [27] suggested a

combination of a self-powered circuit and a voltage-balancing circuit. To achieve the goal of a fully modular switching position with low part count, simple control and soft-start capability, a combination of a modified configuration of the voltage balancing circuit in [1] so this approach could be used in multilevel converters, and a new built-in self-powered circuit is proposed in this paper building from the work presented in [28]. In particular, the following new contributions.

A procedure for determining the component values of the voltage-balancing circuit for inductive loading is shown and an analysis of its use in half-bridge circuits. A new soft-start circuit that takes advantage of the used components to reduce part count is proposed to provide power to the switch when the voltage across it is much lower than nominal value. Lastly, a method for pre-charging the voltage-balancing circuitry by taking advantage of this newly presented start-up circuit for half-bridge applications is shown.

The paper is structured as follows: The proposed switching position is described in Section 5.3. A novel design methodology for determining the components for the voltage-balancing circuit is given in Section 5.4. Defining equations for design of the self-powered circuitry are addressed in Section 5.5. The novel start-up configuration is given in Section 5.6. Simulation results for the circuit designs are illustrated in Section 5.7 and experimental results are evaluated in Section 5.8. An appendix provides a design example.

5.3 The Proposed Modular Switching Position

The circuit configuration of the proposed modular switching position is given in Figure 5-1. The function of the voltage-balancing circuit is to ensure dynamic and static voltage balance between series connected devices. The built-in self-powered gate circuit uses the switching of the power semiconductor device to provide power to the gate and other auxiliary circuitry. These

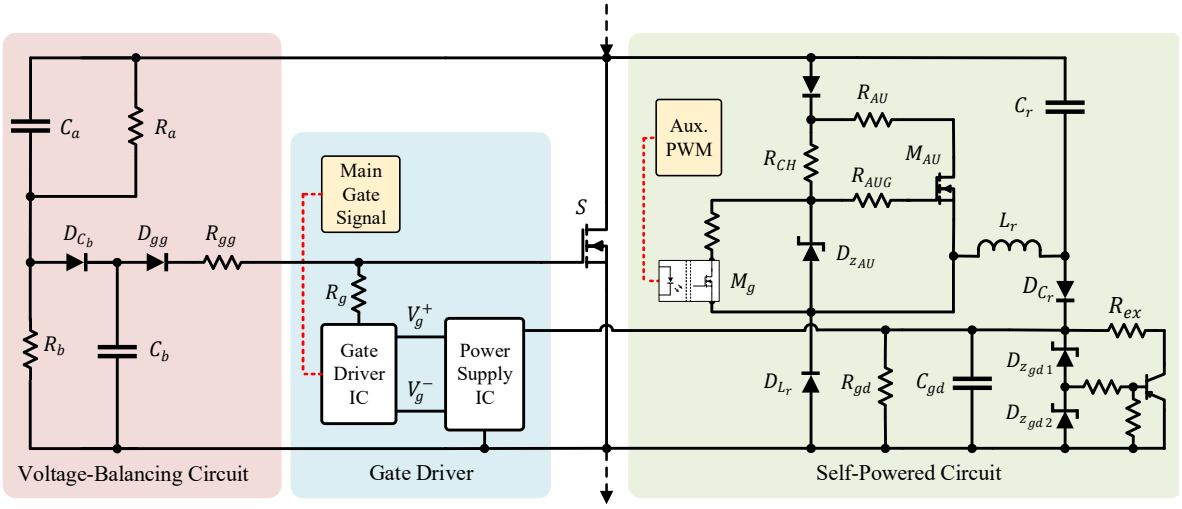

Figure 5-1. The proposed modular switching position.

two circuits are shown across a power semiconductor device along with a simple gate driver circuit.

All that is needed to interface with the switching position is the gate signal fiber optic cabling, making it ideal for use in multilevel converters in which size, common-mode voltage and dv/dt immunity are problematic. Just one switching position would be designed for the required current and voltage ratings of a more-readily-available power semiconductor device and then simply stacked to achieve the desired voltage rating. The voltage-balancing circuit and the built-in self-powered circuit are not involved in processing the *main* power flowing through the switching position.

From Figure 5-1, the proposed voltage-balancing circuit requires only passive components and diodes. This can be compared to the common series-connection approach from [2]. That approach uses RC snubbers to keep the voltages dynamically and statically balanced. The use of these snubbers is proven to be effective, but unfortunately, these circuits can cause

additional static and switching losses in the circuit. The voltage-balancing circuit in this paper avoids these losses because it can have very little static losses and does not contribute much to switching losses.

The self-powered circuit replaces the high-voltage-transient immune power supply and all the associated magnetics and components [7]. All of these circuits' components could be integrated into a singular module like it is done in typical commercially available isolated power supplies. So, the commercial power supplies should not be considered a singular component when making comparisons. And, unlike the traditional external power supplies, the built-in self-powered structure does not require an increase in size or a change in isolation material as the common-mode voltage of the application increases. Only a change in the voltage across the switch S or current rating would require a redesign. In summary, the proposed solution allows for reaching higher converter voltages more easily and could contribute to the reduction in size of the converter cabinet.

5.4 Design Methodology for the Voltage-Balancing Circuitry

The voltage-balancing circuit in [1] was modified so it could be operated as a half bridge (e.g., the addition of diode D_{C_b}). The modifications and the reasoning behind it are given in subsection 5.4.3. A switch S from a stack of series-connected switching positions is shown with the voltage-balancing circuit in Figure 5-2. Resistances R_a and R_b maintain the static balancing of the voltage between each switch position in the stack. However, this is not adequate during switching transients, so capacitors C_a and C_b are added to provide dynamic voltage- balancing.

Under normal operation C_a is charged to the nominal OFF-state voltage, V_S, of S. Because $C_a >> C_b$, any excess voltage when the voltage across S rises sharply will appear mostly across C_b. This current path is shown in blue. Simultaneously, the voltage across C_b results in a current,

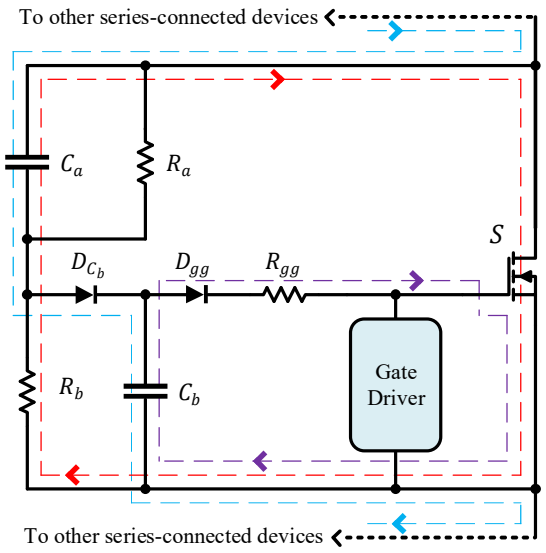

Figure 5-2. The voltage-balancing circuit across a power device.

shown in purple, into the gate of the power device, S, which charges its gate capacitance, C_g, and begins to turn the device ON. This mechanism protects S from overvoltage events that occur when one or more devices in a stack of devices turns ON before S (or when S turns-OFF before the others). Excess energy that may be accrued by C_a during a compensation event is expended by R_b when S is ON. This current path is shown red.

Though the basis for the circuit was suggested in [1], only a "rule-of-thumb" process for selecting the component values was given. The following two subsections present a new methodology for choosing the components for the voltage-balancing circuit with resistive [28] and also current-source (charged inductor) loadings. In addition, the modification to the voltage-balancing circuit from [1] and the reasoning behind it are given in a third subsection.

Consider that switches $S1$ and $S2$ in Figure 5-3 are initially OFF and have balanced voltages across them. Assume that $S1$ begins to turn-ON before $S2$. The voltage across $C_{a_{S2}}$ is V_S, and $C_{a_{S2}}$

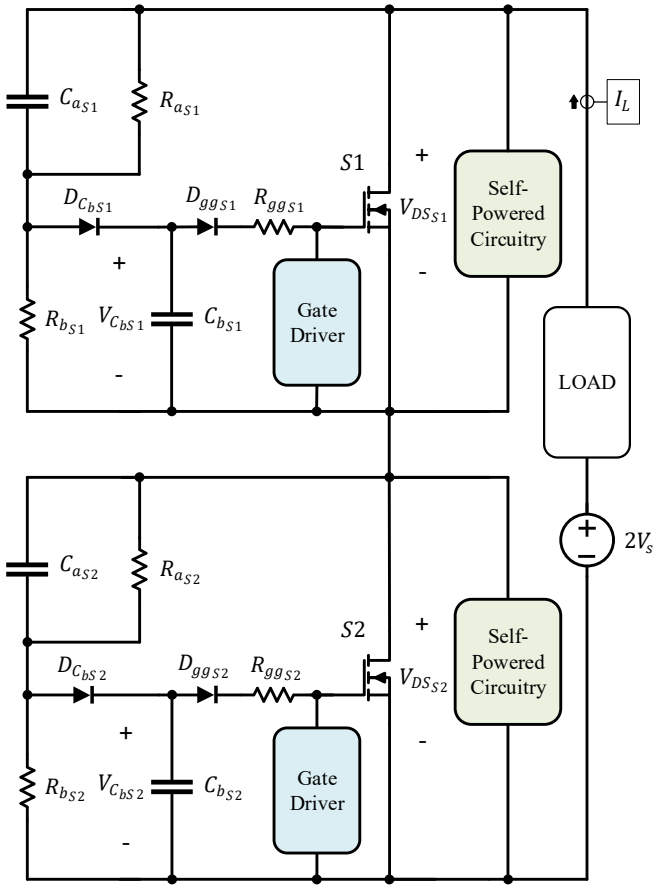

Figure 5-3. A series connection of two modular switching positions.

>> $C_{b_{S2}}$, so as the voltage across $S2$, $V_{DS_{S2}}$, begins to increase almost all of this voltage increase appears across $C_{b_{S2}}$. This charges the gate capacitance of $S2$, $C_{g_{S2}}$, turning $S2$ ON before it is destroyed.

The design process developed here assumes a worst-case scenario in which the gate pulse offset, t_{off}, between $S1$ and $S2$ is larger than the turn-ON time of $S1$ and the turn-OFF time of $S2$ combined. This means that $S1$ can completely turn ON before $S2$ begins to turn ON. It is expected that t_{off} is normally much smaller.

The processes below give a starting point for selecting the component parameters for $S2$ and thus $S1$, since they are identical. So, the "2" subscript is removed when applicable.

5.4.1 Resistive Loading Conditions

The process for choosing the component values is as follows:

1. Design the gate drive using normal methods [29-31]. This determines R_g, V_g^+, V_g^-.
2. Choose the maximum voltage overshoot, ΔV_{DS}, for the switch S. Then the resistance R_{gg} is calculated by

$$R_{gg} < \frac{\Delta V_{DS} R_g}{V_{g,on} - V_g^-} \tag{1}$$

   where $V_{g,on}$ is the gate voltage at which the device begins to turn ON (approximated from the datasheet), R_g is the gate resistance and V_g^- is the designed OFF-state gate voltage from Step 1.
3. Determine the dynamic behavior of C_b and C_g. The voltages V_{C_b} and V_{C_g} across C_b and C_g, are respectively defined in the Laplace domain as follows:

$$V_{C_b}(s) = \left(\frac{N_1}{D_1}\right)[V(s) - V_2(s)] + V_2(s) \tag{2}$$

$$N_1 = C_g R_g R_{gg} s + R_g + R_{gg} \tag{3}$$

$$\begin{aligned} D_1 &= C_b C_g R_L R_g R_{gg} s^2 + \ldots \\ &\ldots R_L\left(R_g + R_{gg}\right)\left(C_b + C_g\right)s + R_L + R_g + R_{gg} \end{aligned} \tag{4}$$

$$V_2(s) = \frac{N_2}{D_2}, \tag{5}$$

$$N_2 = R_g R_{gg} C_b C_g V_{C_b}(0) s^2 + R_g C_b V_{C_b}(0) s \ldots + R_g C_g V_{C_g}(0) s + R_{gg} C_b V_{C_b}(0) s + V_g^- , \quad (6)$$

$$D_2 = s\left(R_g R_{gg} C_b C_g s^2 + R_g C_b s + \ldots \ldots R_g C_g s + R_{gg} C_b s + 1\right) , \quad (7)$$

$$V_{C_g}(s) = \left(\frac{R_g}{C_g R_g R_{gg} s + R_g + R_{gg}}\right) \ldots \ldots \left[V_{C_b}(s) - V_1(s)\right] + V_1(s) , \quad (8)$$

$$V_1(s) = \frac{R_g C_g V_{C_g}(0) s + V_g^-}{R_g C_g s^2 + s} , \quad (9)$$

with $V_{C_b}(0)$ and $V_{C_g}(0)$ as initial conditions, and R_L and R_g as the load and gate resistances. Capacitor C_g is approximated by the C_{ISS} specified in the datasheet for switches $S1$ and $S2$.

The equivalent circuit for voltage-balancing action with a resistive load is drawn in Figure 5-4. The voltage drops across the diodes are neglected. The compensation event can be divided into three periods or "modes." A piecewise approximation of the compensation event can be constructed using the inverse Laplace transformation of (2) and (8) during each mode.

MODE I begins when $S1$ begins to turn ON before $S2$. Both C_b and C_g begin to charge, but V_{C_g} remains below $V_{g,on}$. Voltage $V(s)$ from (2) is given in the Laplace domain as

$$V(s) = \frac{V_S}{t_r s^2} \tag{10}$$

where t_r is the fall time of the device.

MODE II begins after t_r has elapsed. Capacitors C_b and C_g are still charging and V_{C_g} remains below $V_{g,on}$. However, $V(s)$ from (2) is now given by:

$$V(s) = \frac{V_S}{s} \tag{11}$$

because $S1$ is fully ON.

MODE III begins once $V_{C_g} = V_{g,on}$. Capacitor C_b is no longer charging because $S2$ has

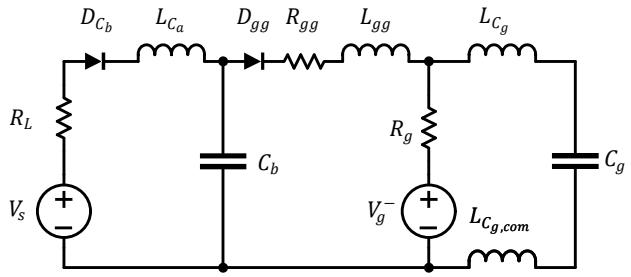

Figure 5-4. Equivalent circuit for voltage-balancing action with resistive load.

begun to turn ON, the voltage across C_a prevents any further charging of C_b and $V(s)$ from (2) is then

$$V(s) = V_2(s) \tag{12}$$

so that the first term in (2) is zero. Capacitor C_g may continue to accrue charge for a time because C_b is discharging into it. It then discharges into C_g and the gate drive.

Table I describes each of the three modes I-III of the compensation action for a resistive load including the value of $V(s)$ from (2) during each mode and their durations. The

Table 5-1. Values of $V(s)$ and $I(s)$ during each mode

RESISTIVE LOADING					
MODE	$V_{Cg} > V_{g,on}$[a]	C_b[b]	C_g[b]	$V(s)$	Duration
I	X	+	+	$\frac{V_S}{t_r s^2}$	t_r
II	X	+	+	$\frac{V_S}{s}$	$t_{V_g=V_{g,on}} - t_r$
III	✓	-	+ or -	$V_2(s)$	$t_{off} - t_{MODE\ II}$
CURRENT SOURCE LOADING					
MODE	$V_{Cg} > V_{g,ss}$[a]	C_b[b]	C_g[b]	$I_1(s)$	Duration
I	x	+	+	$\frac{I_L}{t_r s^2}$	$t_{V_g=V_{g,on}}$
II	✓	- or =	- or =	$\frac{V_{C_b,ss} + V_g^-}{s(R_{gg} + R_g)}$	$t_{off} - t_{MODE\ I}$

[a]Indicates if the given condition is TRUE (✓) or FALSE (x)
[b]Indicates if the given capacitance is charging (+) or discharging (-) or remaining the same (=)

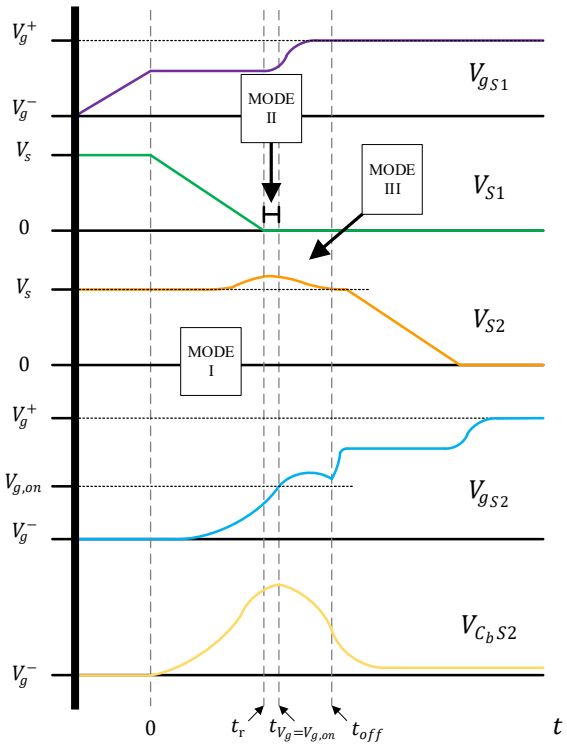

Figure 5-5. Theoretical waveforms for resistive loading.

modes occur in order. The time $t_{V_g=V_{g,on}}$ is at which $V_g = V_{g,on}$. And $t_{MODE\ II}$ is the time when MODE II ends. The theoretical waveforms for these modes are shown in Figure 5-5.

4. Choose C_b such that the circuit is operating in MODE III when $S2$'s gate driver begins to apply its ON-state voltage.

   Capacitor C_a is then chosen to be $100C_b$. Resistance R_a can be chosen as a static balancing resistance for the switching position if needed. Using a shunt resistance like R_a to compensate for leakage current mismatch is a well-known subject and is not covered in this paper [32].

5. Calculate the extra energy, ΔE_{C_a}, that is absorbed by C_a. This energy needs to be removed, otherwise V_{C_a} will become unbalanced for as long as $|t_{off}| > 0$. Resistance R_b should be chosen such that this energy is drained from C_a when $S2$ is ON. ΔE_{C_a} is determined from the current into C_a during the compensation event (the blue path in Figure 5-2). ΔE_{C_a} from each event can be integrated over a period to give an equivalent power P_{C_a} that R_b should dissipate. For a constant switching frequency, f_{sw}, this power is defined as

$$P_{C_a} = \Delta E_{C_{a,avg}} f_{sw} \tag{13}$$

   where $\Delta E_{C_{a,avg}}$ is the average expected ΔE_{C_a}. With P_{C_a}, R_b can be chosen according to

$$R_b < \frac{{V_s}^2}{P_{C_a}} d_{avg} \tag{14}$$

   d_{avg} is the average duty cycle applied to $S2$.

5.4.2 Current Source Loading Conditions

The process with a current-source load is as follows:

1. Follow Steps 1 and 2 from Section 5.4.2.
2. Determine the behavior of C_b and C_g. The voltage across C_b and the gate capacitance, C_g, are defined in the Laplace domain as

$$V_{C_b}(s) = \frac{N_3}{D_3} + I_1(s)\frac{N_4}{D_4}, \tag{15}$$

$$N_3 = R_g R_{gg} C_b C_g V_{C_b}(0)s^2 + V_g^- + \ldots \\ \ldots \left(C_b R_g V_{C_b}(0) + C_b R_{gg} V_{C_b}(0) + R_g C_g V_{C_g}(0)\right)s\,, \tag{16}$$

$$D_3 = R_g R_{gg} C_b C_g s^3 + \ldots \\ \ldots \left(C_b R_g + C_b R_{gg} + C_b R_g\right)s^2 + s\,, \tag{17}$$

$$N_4 = \left(R_g + R_{gg} + C_g R_g R_{gg} s\right), \tag{18}$$

$$D_4 = C_b C_g R_g R_{gg} s^2 + \ldots \\ \ldots \left(C_b R_g + C_b R_{gg} + C_g R_g\right)s + 1\,, \tag{19}$$

$$V_{C_g}(s) = \frac{V_g^- + C_g R_g V_{C_g}(0)s}{C_g R_g s^2 + s} + \ldots \\ \ldots \frac{R_g\left(V_{C_b}(s) + \dfrac{V_g^- + C_g R_g V_{C_g}(0)s}{C_g R_g s^2 + s}\right)}{\left(R_{gg} C_g R_g s + 1 + R_g\right)}, \tag{20}$$

where I_1 from (15) is the current through D_{C_b}.

3. Determine the current balance between I_1 and the current through R_{S2}, $I_{R_{S2}}$. The equivalent circuit for the current-source load is illustrated in Figure 5-6. Through device

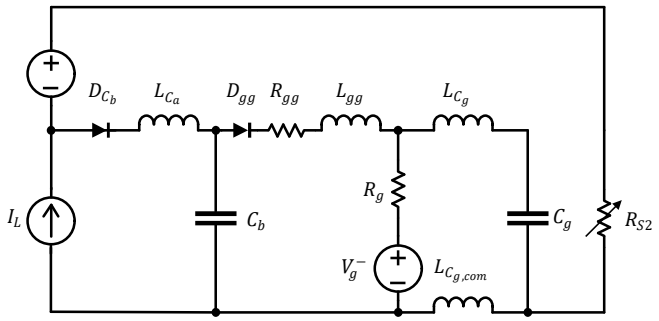

Figure 5-6. Equivalent circuit for the voltage-balancing action with a current-source load.

characterization, an equivalent resistance can be derived for switch $S2$ based on V_{C_g}. An equilibrium between the current going through the branch containing R_{gg} and the branch containing R_{S2} can be predicted based on this equivalent resistance. The relationship is defined by

$$I_L = \frac{V_{C_g,ss} - V_g^-}{R_g} + \frac{V_{C_b,ss} + V_S}{R_{S2}} \tag{21}$$

$$R_{S2} = f\left(V_{C_g}\right), \tag{22}$$

where $V_{C_g,ss}$ and $V_{C_b,ss}$ are the steady-state values of v_{C_g} and v_{C_b}, at the end of the compensation event, respectively, and I_L is the load current. The compensation event can be divided into two periods or "modes." Like with the resistive loading, this can be used to form a piecewise function approximation of the compensation event by using the inverse Laplace transforms of (15) and (20).

MODE I begins when $S1$ starts to turn ON before $S2$. Both C_b and C_g begin to charge, but V_{C_g} remains below $V_{g,on}$. Current $I_1(s)$ from (15) is given in the Laplace domain as

$$I_1(s) = \frac{I_L}{t_r s^2}. \tag{23}$$

MODE II begins when $V_{C_g} = V_{g,on}$. Voltages v_{C_g} and v_{C_b} converge to $V_{C_g,ss}$ and $V_{C_b,ss}$ and stay there until the end of MODE II when the gate driver for $S2$ takes over after t_{off}. $I_1(s)$ from (15) for this mode is

$$I_1(s) = \frac{V_{C_b,ss} + V_g^-}{s\left(R_{gg} + R_g\right)}. \tag{24}$$

Values for R_{S2}, $V_{C_g,ss}$ and $V_{C_b,ss}$ can be calculated manually for the worst-case load current. Table I describes both of these modes of the compensation action for a current source load including the value of $I_1(s)$ from (15) during each mode and their durations. $t_{MODE\ I}$ is the time when MODE I ends. The theoretical waveforms for these modes are shown in Figure 5-7.

4. Choosing I_L and t_{off} determine the value of C_b. Because of the low-pass RC network formed by (R_{gg} + R_g) and C_g, some overshoots above $V_{C_b,ss}$ and $V_{C_g,ss}$ may be experienced. This may lead to oscillations in v_{C_g} and thus in i_1.

   From the inverse Laplace of (13)-(18) and the value of I_1 from Table I, choose a C_b value in which v_{C_b} is greater than $V_{C_b,ss}$ at the end of MODE I. Capacitance C_a is then chosen to be $100C_b$ and R_a can be chosen as a static balancing resistance for the switching position if needed.

5. Follow Steps 5 from Section 5.4.1 to determine R_b.

It is important to note that R_b will discharge C_a regardless of the value of t_{off}. This will result in a voltage drop on C_a that is dependent upon the time the switch is ON. When two of these modular switching positions are connected in a half-bridge configuration, a non-negligible

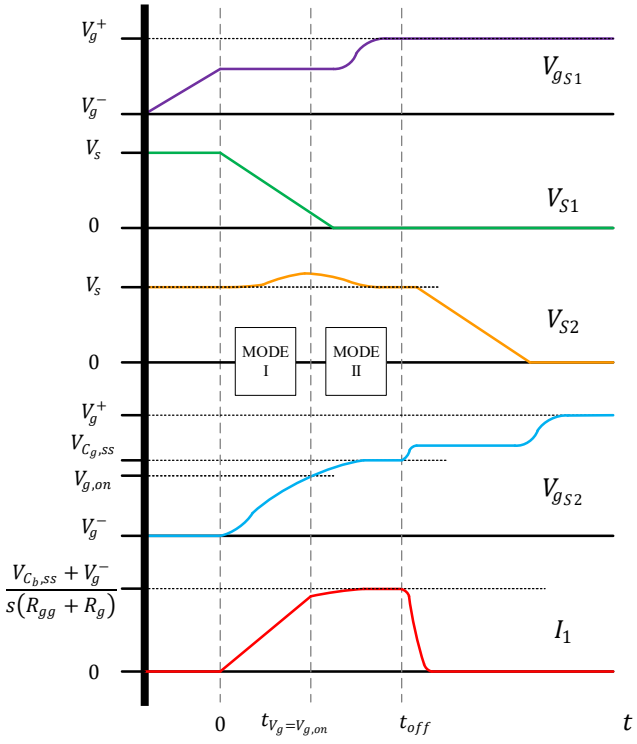

Figure 5-7. Theoretical waveforms for a current-source load.

charging current will be added to the load current experienced by each switching position during turn-ON, which will increase turn-ON losses. If t_{off} can be kept small, then the value of R_b can be increased and the reduction of V_{C_a} can be made negligible.

5.4.3 Voltage-Balancing Modification for Half-Bridge Operation

The effect of adding the voltage-balancing snubber from [1] needs to be evaluated for application in a half-bridge circuit. For simplicity only one of the proposed modular switching positions is used for the top and bottom switch locations, respectively. The addition of D_{C_bP} and D_{C_bN} is highlighted in green. Without D_{C_bP}, as is the case in [1], each time S_P turns ON it incurs additional losses associated with C_{bP} as it charges from 0 V to -2V_S [33]. This current path is shown red with D_{ggP} blocking the reverse charge of the gate. The resulting power loss is defined as

$$P_{C_b} = \frac{1}{2} C_{bP} (2V_S)^2 f_{sw} \,, \tag{25}$$

with f_{sw} as the switching frequency of S_P.

Another source of losses comes from the discharge of C_{bP}. When S_P turns OFF, the load current, I_L, as indicated in Figure 5-8 clamps the voltage across S_P to nearly 0 V by conducting through the anti-parallel diode. This keeps C_{bP} charged to -$2V_S$. When S_N turns ON after the switching deadtime capacitor C_{bP} will discharge into S_N resulting in additional turn-ON losses for S_N. This current path is shown in blue. The losses associated with this event are also given by (25).

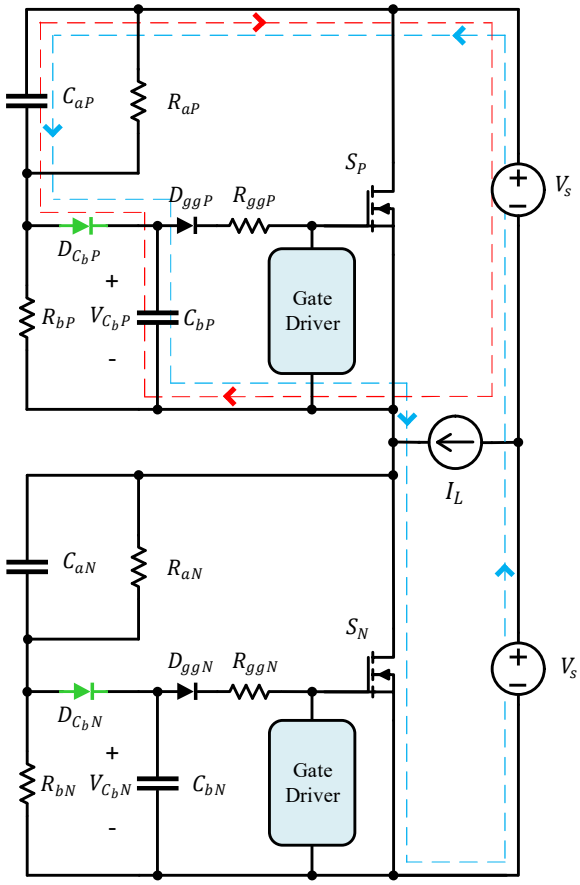

Figure 5-8. The voltage-balancing circuit used in a half-bridge application.

With the introduction of D_{C_bP} and D_{C_bN} the path indicated in red is blocked for both switching positions so C_{bP} and C_{bN} can never be charged by C_{aP} and C_{aN}, respectively and thus, these loss sources are eliminated. Another advantage of D_{C_bP} and D_{C_bN} is that they clamp resonance between the voltage- balancing circuit capacitors and inductive elements in the path of the load current.

5.5 Design of the Self-Powered Circuitry

The circuit designed to power the gate driver using power drawn from across the power device is illustrated in Figure 5-9. When the device S is OFF, capacitor C_r charges from -$V_{C_{gd}}$ to $\left(V_S - V_{C_{gd}}\right)$ through the blue current path shown in Figure 5-9. Again, V_S is the expected OFF-state voltage across the MOSFET. This current also helps to charge C_{gd}. The energy delivered to C_{gd} is

$$E_1 = V_{C_{gd}}(C_r V_S)\,. \tag{26}$$

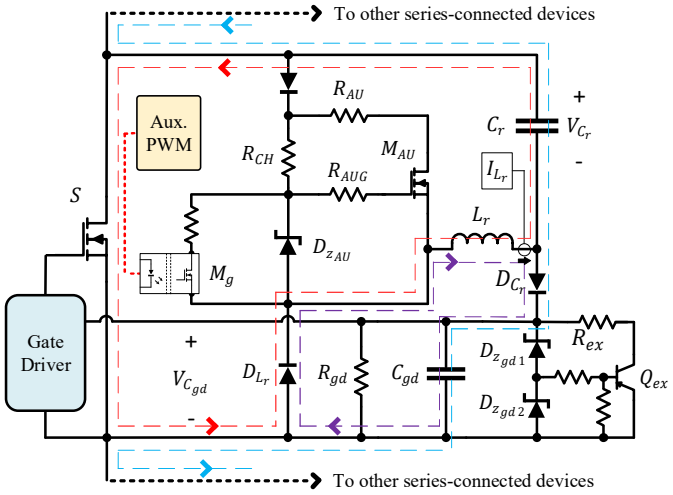

Figure 5-9. Current commutations during the ON- and OFF-times of the power MOSFET.

This charging current when used with resistive loading as in Figure 5-3 is defined by

$$i_1(t) = \left(\frac{V_S}{R_L}\right) e^{-t/C_r R_L}\,, \tag{27}$$

$$t_{TOT1} \approx 5C_r R_L\,, \tag{28}$$

where t_{TOT1} is the total amount of time to charge C_r. The current is constant when using a current-source load and the charging time is then given by

$$t_{TOT2} = \mathrm{C}_r \frac{V_S}{I_L}. \tag{29}$$

In (26) and (29) the assumption is that C_r is the only capacitance being charged. If there are other parallel capacitances across the switch S then the effect of this capacitive current divider must be included.

Upon turn-ON of S, the current resonates from C_r through L_r as shown in Figure 5-9 in red. This current, i_{L_r1}, is defined by

$$i_{L_r1}(t) = \frac{V_{C_r} - V_{C_{gd}}}{\sqrt{\frac{L_r}{C_r} - \frac{R_{eq}^2}{4}}} e^{-\delta t} \sin(\omega t)\,, \tag{27}$$

$$\omega = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_{eq}}{2L_r}\right)^2}\,, \tag{28}$$

$$\delta = \frac{R_{eq}}{2L_r}\,, \tag{32}$$

where V_{C_r} is the voltage across C_r, $V_{C_{gd}}$ is the voltage across C_{gd}, and R_{eq} is the equivalent series resistance of the current path. The value of R_{eq} could be approximated using the dc resistances from the datasheet for each component involved in conducting the current

(e.g., C_r, L_r, D_{L_r}). The current peak coincides with the discharging of C_r to 0 V, resulting in the total energy given by

$$E_2 = \frac{1}{2} L_r I_{pk1}^2 , \tag{33}$$

where I_{pk1}^2 is the peak value of i_{L_r1}. The peak occurs at

$$t_{pk1} = \frac{\tan^{-1}\left(\frac{\omega}{\delta}\right)}{\omega} . \tag{34}$$

After t_{pk1} the voltage across L_r reverses to maintain the flow of current and the energy in L_r then resonates into C_{gd} which is demonstrated in Figure 5-9 in purple. This discharge slope is a function of $V_{C_{gd}}$ and L_r. The time needed to reduce the current through L_r to 0 (neglecting series resistance and voltage drop across D_{L_r} and D_{C_r}) is calculated by

$$t_{TOT3} = L_r \frac{I_{pk1}}{V_{C_{gd}}} . \tag{35}$$

The total power delivered to C_{gd}, P_T, is given by

$$P_T = \frac{1}{2}\left(E_2 - C_r V_{C_{gd}}^2 + E_1\right) f_{sw} . \tag{36}$$

Capacitor C_r is effectively in parallel with C_{gd} when the MOSFET is ON and thus the existence of the $C_r V_{C_{gd}}^2$ term in (33). The existence of the f_{sw} term in (36) means that a change in switching frequency causes a change in delivered power. This can allow P_T to scale up with the increased power needed by the gate driver circuitry, but considering the baseline power needed by the auxiliary/diagnostic circuitry of the switching position this relationship sets a lower limit for a frequency change. So this self-powered circuity is not effective in applications requiring always-ON operation of a device. Thus, this self-powered scheme is most useful in applications that do not require large variations in switching frequency.

Assuming a relatively low power consumption of the on-board circuitry, the value of C_r will be such that this resonant circuit does not contribute significantly to the turn-ON or conduction losses incurred by the switch upon which it is installed. However, C_r does contribute to the effective C_{OSS} of $S1$ and $S2$. This means that if C_r has a value comparable to C_{OSS} of $S1$ or $S2$, this can then contribute to the turn-ON losses when these modular switching positions are connected in a half-bridge configuration. Thus, there is a trade-off between the power supplied by the self-powered gate circuitry and the turn-ON losses in the devices, unless the charging current is otherwise limited, such as with a resistor in series with C_r.

As implied by the preceding analysis, this circuit, like the voltage balancing circuit, is required to support the entirety of the power device voltage. Depending on the voltage, this requires some relatively large clearance and creepage distances between components when using conventional PCB technology [34]. However, the intended application is to develop a higher density module that can be potted with an isolation material like it is done with commercial power supply modules.

5.6 Start-Up of the Switching Position

5.6.1 Overview

The switching position may not have power in some self-powered schemes until nominal voltage occurs across the switch, and thus any diagnostics that may be desirable for centralized control are inaccessible. Hence, special consideration needs to be given to the start-up procedure required in any application because the power for the switching position is derived from the voltage across the switch which will be at much lower than nominal at startup. To prevent this undesirable operating condition, the start-up circuit in Figure 5-10 was added. In this configuration, L_r and its corresponding blocking diode are positioned to form a buck converter

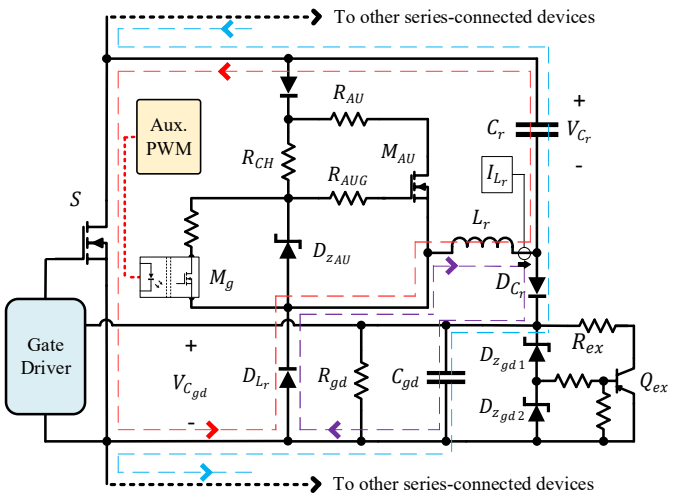

Figure 5-10. Proposed modified self-powered circuit with start-up circuitry.

along with M_{AU} and C_{gd}.

Components M_{AU}, L_r, D_{L_r}, and C_{gd} are used as a buck converter to provide power to the switching position at all voltages between the intended operating voltage of C_{gd}, $V_{C_{gd}}^*$, and V_S. The gate of M_{AU} is charged to the zener voltage of $D_{z_{AU}}$ through a large resistance value R_{CH}. This is the green current path. Switch M_g is used to modulate the voltage at the gate of M_{AU} according to a central controller. Through this bucking action, any diagnostics performed by the switching position are active starting slightly above $V_{C_{gd}}^*$, far below the nominal voltage V_S. Resistance R_{AU} remains as an initial current limiter as M_{AU} is in a "normally ON" configuration. The current path for the ON-time bucking action is shown in blue in Figure 5-10. When M_{AU} turns-OFF the current path is identical to the purple path in Figure 5-9.

Central/Identical duty cycle control of M_g for each switching position helps to keep the voltage balanced across each switch. The current paths in Figure 5-10 indicate the dependency of each switching position on the ones above and below it. When the M_{AU} of a switching position is ON it depends on the M_{AU} in the adjacent switching positions to be ON as well. If each switching

position was controlled independently, such as with an onboard voltage controller IC, they would operate as individual constant-power loads and possibly contribute to any voltage imbalance across the series-connected devices; so, this option was not selected.

To avoid any voltage imbalances that may occur from individual self-control of each switching position, the switching positions are controlled with a semi-open-loop central control method. From 0 V to 1.6 kV the required duty-cycle for this bucking mechanism is empirically determined at 10 V increments. The resultant Duty Cycle vs Switching Position Voltage curve from this characterization is presented in Figure 5-11. This data is then broken into different sections and a curve fitting tool is used to fit curves to each section. From the individual curves a piecewise function is built into the start-up control that automatically adjusts the duty cycle for all switching positions based on the number of switching positions used and the total dc-bus voltage. The duty-cycle chosen at each increment can be chosen larger than required to compensate for any component parameter variation between different switching positions.

Instead of a simple Zener-diode-based regulator for C_{gd}, a Zener-BJT-based voltage regulator is used. This voltage regulator consists of $D_{z_{gd}1}$, $D_{z_{gd}2}$, R_{ex}, Q_{ex}, and small resistor network. Transistor Q_{ex} begins to turn-ON when $v_{C_{gd}}$ becomes greater than the breakdown

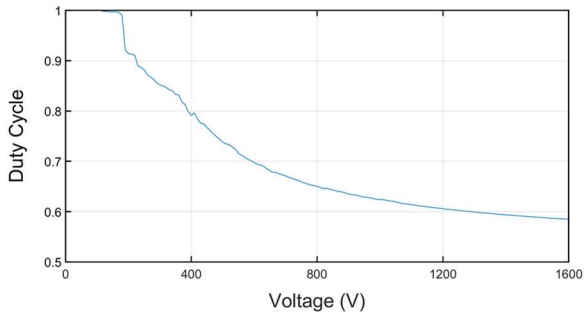

Figure 5-11. Proposed modified self-powered circuit with start-up circuitry.

voltage for D_{zgd1} plus the base-emitter voltage of Q_{ex}. This alleviates some of the current that would normally be shunted purely through the Zener diode. This allows for the selection of C_r for nominal bus voltage while allowing for voltage (and correspondingly power) swells across the power device to be dissipated by a more resilient power resistor. Or conversely, it is a simple way to lower the minimum operating voltage of the self-powered gate driver by oversizing C_r if the application requires operation during voltage sags.

5.6.2 Half-Bridge Operation

A basic half-bridge converter implemented with two modular switching positions is shown in Figure 5-12, where the self-powered snubber circuit is neglected. The converter is connected to a resistive load through an LC filter. When the dc bus is initially charged to the nominal value, the voltages across C_{aP} and C_{aN}, $V_{C_{aP}}$ and $V_{C_{aN}}$ respectively, are half of the total bus voltage, $2V_s$. In fact, when S_P and S_N are not operating, the snubbers across both switches effectively form a resistor divider. This start-up condition presents two problems. When S_P turns ON, there is a charging current that goes through it, in addition to the load current. The current paths are shown in blue in Figure 5-12.

The first problem is that a large positive dv/dt appearing across S_N can trigger the snubber balancing action. As a result, S_N could be forced ON causing a catastrophic shoot-through current event. Assuming some auxiliary switches S_{bP} and S_{bN} could be closed during this condition, the first problem can be avoided. However, this does not solve the following second problem. Due to the design requirements of the voltage-balancing snubber, the values of C_{aP} and C_{aN} will most likely far exceed the output capacitances of S_P and S_N. This means that S_P will be switching with a relatively large capacitive load, potentially resulting in a damaging overcurrent event.

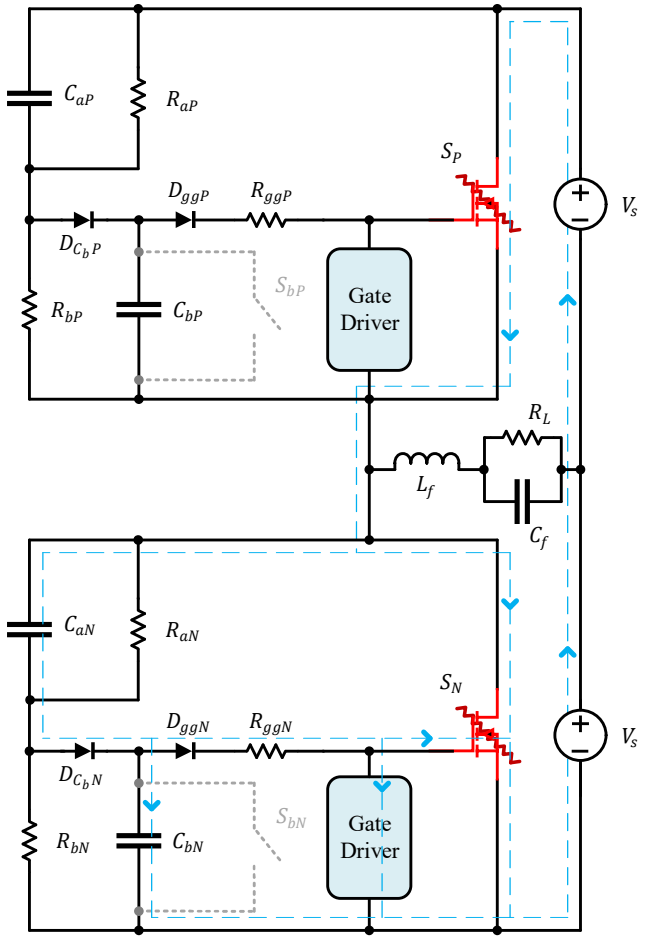

Figure 5-12. Proposed modified self-powered circuit with start-up circuitry.

Capacitors C_{aP} and C_{aN} must be charged to $2V_s$ before either S_P or S_N turn ON to avoid this condition. This can be achieved by utilizing the soft-starting capabilities of the self-powered snubber. When M_{auP} and M_{auN} are switched with the same pulses (in-phase), there is no net charge provided to C_{aP} or C_{aN} and the problem mentioned above persists. This is shown by the green path in Figure 5-13(a). However, if the control pulses for M_{auP} and M_{auN} are offset (out-of-phase), this allows for the charging of C_{aP} and C_{aN} to nearly $2V_s$. The current path in this case is illustrated in blue in Figure 5-13. The pulses for M_g are shown in Figure 5-13(b). Then v_s can

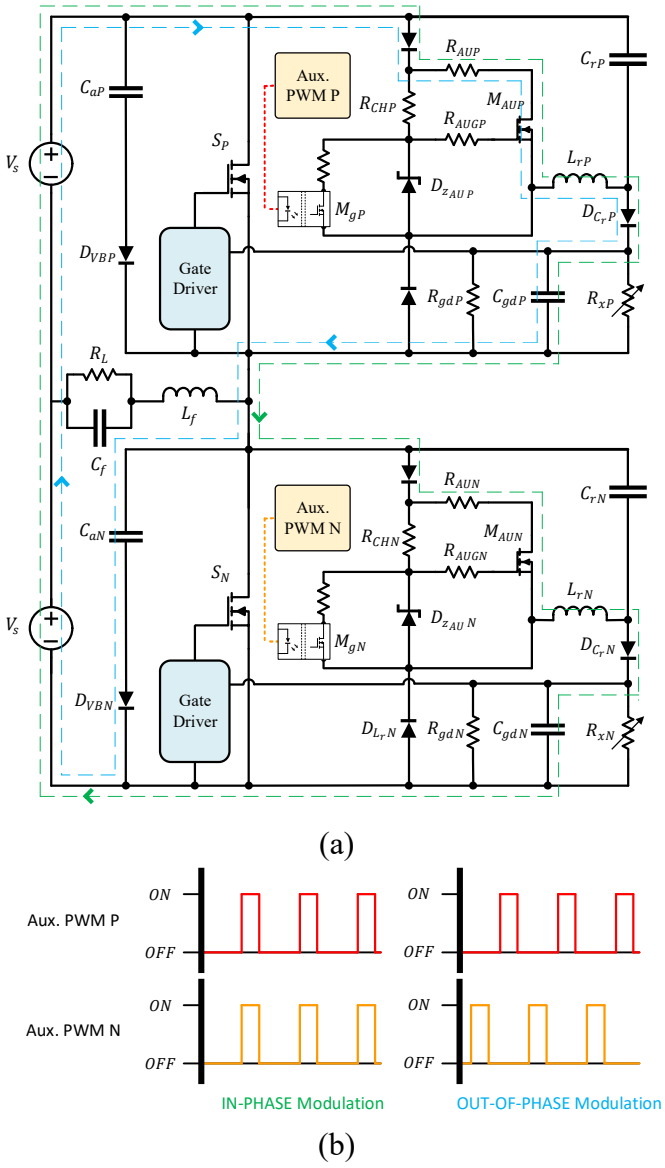

Figure 5-13. (a) Start-up currents with in-phase and out-of-phase bucking pulses. (b) The in-phase and out-of-phase modulation pulses.

be ramped from 0 V to nominal voltage and C_{aP} and C_{aN} remain charged near $2V_s$; the main self-powered mechanism can then take over. The voltage-balancing snubber is just approximated by C_{aP} and C_{aN}, and their respective blocking diodes, because it is assumed that the currents involved are relatively small. The excess-power circuit components D_{zgd1}, D_{zgd2}, R_{ex}, and Q_{ex} are approximated as the variable resistance R_x.

5.7 Circuit Simulation Results

The setup provided in Figure 5-3 was used in the simulations with a V_S = 1.2 kV and a current source load of 10 A. The following two sections present the operation of the two proposed circuits.

5.7.1 Voltage Balancing Circuit

The parameters of the simulated switching position are shown in Table 5-2. The voltage balancing action of the circuit was simulated using OrCAD® PSpice®. Simulations were done utilizing Wolfspeed® SiC MOSFET PSpice® models with the turn-ON of $S2$ modeled with a ramp function. The calculated and simulated values for $v_{C_b}/10$ and v_{C_g} during the turn-on compensation event with 2.4 kV across $S1$ and $S2$ and 10 A of resistive load are shown in Figure 5-14. The comparison between the two is not without some difference, but this does indicate a

Table 5-2. Circuit Parameters

Parameter	Value	Rating
C_a	33 nF	2 kV, 19 mΩ
C_b	0.33 nF	1 kV,
R_{gg}	10 Ω	0.5 W
C_{gd}	10 µF	35 V
V_g^-	-5 V	n/a
$R_{g,on}$	5 Ω	0.25 W
L_r	10 mH	0.5 A
C_r	0.220 nF	2 kV
$S1$, $S2$	C2M0045170D	1.7 kV, 72 A
M_{AU}	SCT2750NYTB	1.7 kV, 6 A
V_g^+	20 V	n/a
$R_{g,off}$	2.5 Ω	0.5 W
$D_{L_r}, D_{C_r}, D_{C_b}, D_{gg}$	CD214A-R12000	2 kV, 2 A

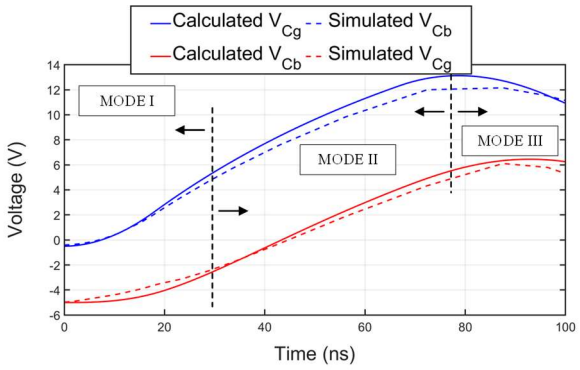

Figure 5-14. Calculated vs simulation values of $V_{Cb}/10$ and V_g for a resistive load.

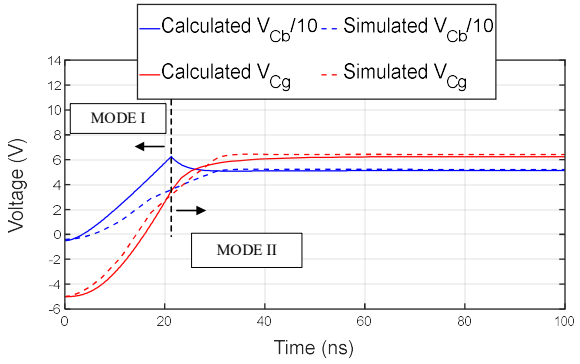

Figure 5-15. Calculated vs simulation values of $V_{C_b}/10$ and V_g for a current-source load.

good starting point for choosing the parameter values of the circuit. In Figure 5-15, the calculated and simulated values for $v_{C_b}/10$ and v_{C_g} during the turn-on compensation event with 2.4 kV across $S1$ and $S2$ and 10 A of current-source load are shown.

In this case, the equilibrium value for the calculations from Section 5.4.2 step 3 was chosen based on the MOSFET PSpice® model. The circuit shown in Figure 5-6 can be used for this purpose. By injecting the load current into the compensation network, the model will naturally come to the steady-state value. Here, a non-conservative value of C_b was chosen. The peak shown in the calculated values of $v_{C_b}/10$ comes from assuming two different values for $i_1(t)$ $(\mathcal{L}^{-1}\{I_1(s)\})$ in Section 5.4.2.

During MODE I the value of $i_1(t)$ ramps from 0 A at a rate determined the rise time of the MOSFET (i.e., 333 A/μs). Once $t_{V_g=V_{g,on}}$ a steady state value of $i_1(t) = 5.0$ A is used. This is a large percentage of the load current for this particular design, however, this equilibrium value is highly dependent upon the values of $R_{g,off}$ and V_g^- and can be significantly reduced. For example, the use of $R_{g,off} = 5\ \Omega$ and $V_g^- =$ -3 V would require a MODE II value of $i_1(t) =$ 1.9 A. Also worth noting is that the $i_1(t)$ does not increase linearly with the load current, so a factor of 2 increase of I_L does not require a factor of 2 increase of $i_1(t)$ as described by the defining equation for MOSFET current in the saturation region.

It should be noted that the gate voltages during these transients is above the threshold, but much lower than typical ON-state drive voltages. This would result in operation of the MOSFET in the saturation region for a small time. Operating in the saturation conduction region will induce higher switching losses in the switched that is being forced ON by the voltage- balancing circuit which in the case of Figure 5-16 and Figure 5-17 is $S1$. However, this voltage-balancing scenario should not occur at every switching cycle. This example is also demonstrating a worst-case scenario. With this circuit, care should still be taken to match the ON and OFF behavior of all MOSFETs that are series-connected. The simple voltage rise delay associated with the charging of C_b is enough to guarantee a safe operating voltage when t_{off} is relatively small (< 10 ns).

5.7.2 Self-Power Circuit

Simulations of the novel self-powered circuitry from Figure 5-10 were performed with a setup as shown in Figure 5-3. The switching frequency for $S1$ and $S2$ were chosen as 10 kHz. In Figure 5-18, $v_{C_{gd}}$, and the current through L_r, i_{L_r}, are shown during the 10 kHz operation. The bucking

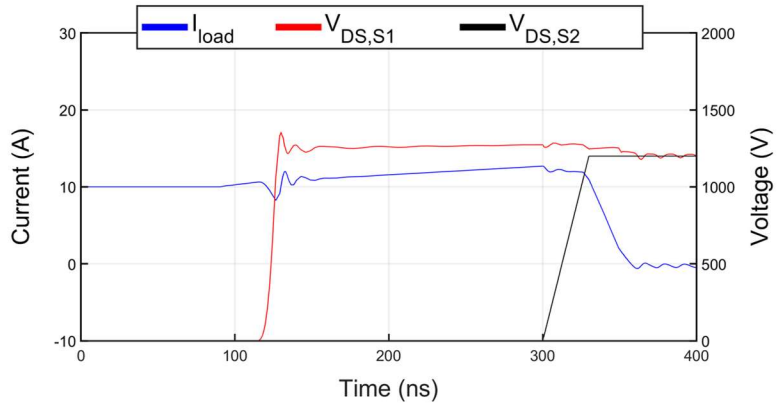

Figure 5-16. Simulation results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-OFF with a 200 ns delay in offset time with a current-source load.

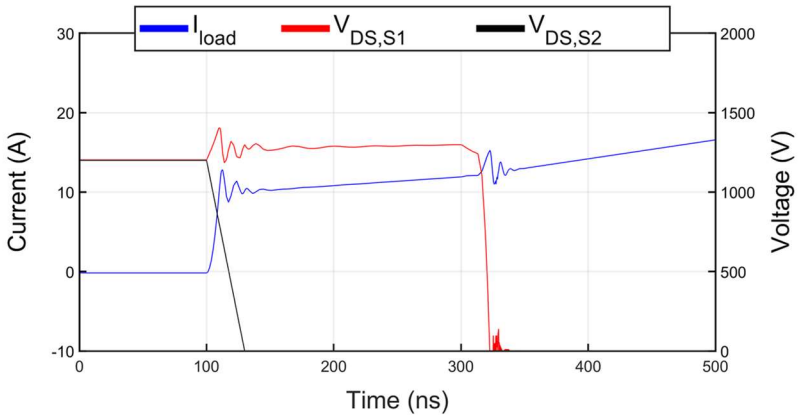

Figure 5-17. Simulation results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-ON with a 200 ns delay in offset time with a current-source load.

mode start-up i_{L_r} waveforms is nearly identical in shape to that in Figure 5-18 but may differ in magnitude and frequency.

5.8 Circuit Experimental Results

The tested 3.3-kV switching position formed by the series connection of two 1.7 kV SiC MOSFETs is presented in Figure 5-19. Though each switch would theoretically be a separate installation with its own fiber optic signaling, this switching position was designed to operate using a single gate signal for simplicity. A high-side driver was used to gate the top switch using the same signals as the low-side circuit.

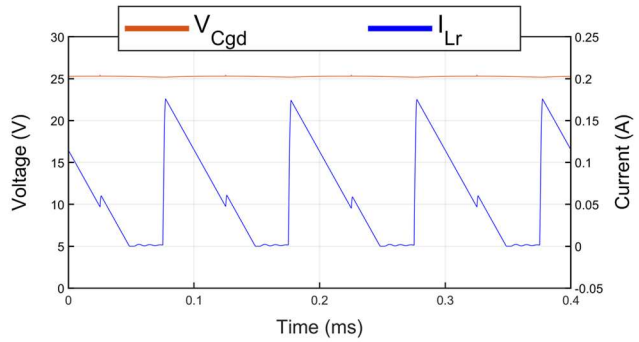

Figure 5-18. I_{L_r}, and V_{Cgd} during turn ON and turn OFF of $S2$.

Figure 5-19. Photograph of 3.3 kV switching position prototype.

This configuration is a good representation of another possible trade-off for this type of module switching position. It may be more cost effective to pre-package series devices up to the limits for conventional high-side ICs and then stack these higher-voltage units together. However, this does reintroduce common-mode current within the shared PCBs.

5.8.1 Voltage-Balancing Circuit

The testing configuration is shown in Figure 5-3 with V_S = 1.2 kV. The clamped inductive load current is 10 A. Like the simulation results in Figure 5-14, Figure 5-20 shows experimental waveforms for the $v_{C_b}/10$ and v_{C_g} for $S2$ when it is delayed relative to $S1$ by around 200 ns as well as the full turn-ON transient. This delay emulates either a false turn-ON signal on one of the devices or a large difference in dv/dt values between series-connected devices. At t = 0 s, $S1$ begins to turn ON. The voltage across C_b rises until v_{C_g} increases to the point where $S2$ begins to take significant current and then both stay around a constant voltage until the gate driver for $S2$ takes over at t = 220 ns; at which point, v_{C_g} starts to rise to the nominal ON-state gate voltage of 20 V. The starting voltage of C_b differs from the V_g^- predicted by the simulations due to the reverse-recovery charge of D_{C_b} within the voltage-balancing circuit. This allows C_b to be

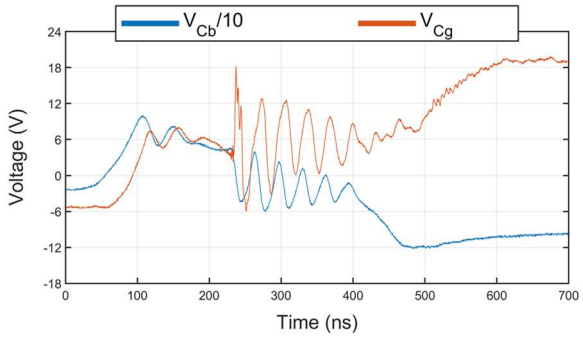

Figure 5-20. Experimental results of $V_{Cb}/10$ and V_g with $S2$ delayed by 220ns.

charged by C_a during a short time. The recovery charge of D_{gg} also contributes to some of the ringing observed in v_{C_g} at t = 220 ns. These affects could be minimized with the use of low reverse recovery diodes and low-inductance components and layout.

The voltage across $S1$, $v_{DS_{S1}}$, and $v_{DS_{S2}}$ are shown in Figure 5-21 along with the load current through the switching position for various values of t_{off} during the turn-OFF transient. There is an initial overvoltage event in $v_{DS_{S2}}$ above 1.2 kV followed by a convergence onto 1.2 kV, which is the voltage of C_a. As discussed in Section 5.3 and demonstrated in Section 5.4 a

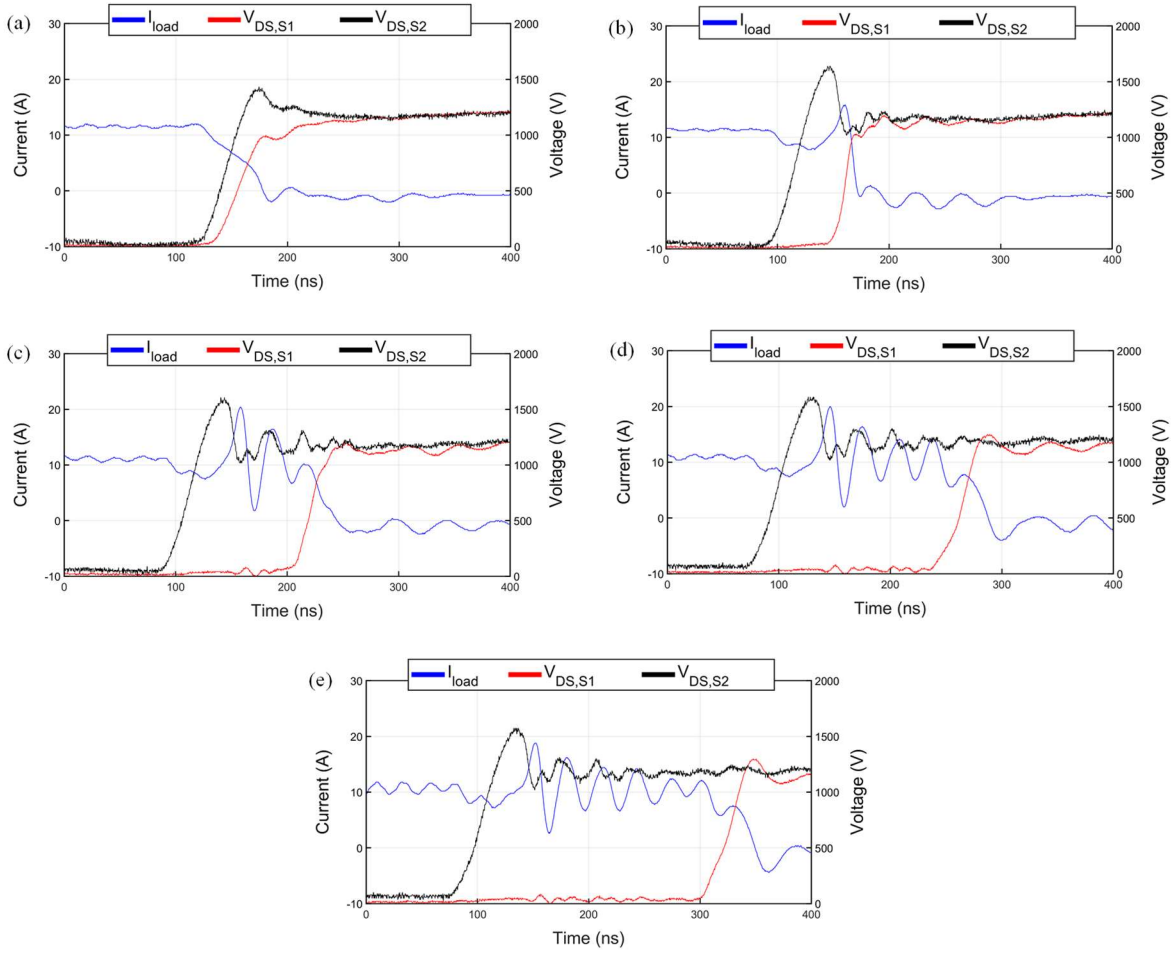

Figure 5-21. Experimental results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-OFF for (a) 10 ns (b) 50 ns (c) 100 ns (d) 150 ns (e) 200 ns offset time.

small percentage of the load current is diverted from $S2$ to the voltage balancing circuit. This small diverted current keeps C_g charged to a steady-state value during the transient and forces $S2$ into the saturation conduction region for a short period of time rather than experiencing a catastrophic overvoltage.

The turn-ON transient is illustrated in Figure 5-22. These voltages were measured with TPP0850 probe from Tektronix® utilizing tip-to-BNC adapters and the voltage was stepped down using techniques suggested in [35] for an approximate bandwidth of 300 MHz. A 1.6 kV spike in $v_{DS_{S2}}$ from Figure 5-21 comes from a slight under-sizing of C_a and C_b and inductance in the compensation and measurement paths. This is known because the voltage across C_b in Figure 5-21 should account for the majority of the voltage overshoot across $S2$.

5.8.2 Self-Powered Circuit

The waveforms for i_{L_r} and $v_{C_{gd}}$ during the bucking operation of the start-up circuit are shown in Figure 5-23. These waveforms were taken at nominal bus voltage (i.e., 2.4 kV). The operating duty cycle at lower voltages would be larger and thus the positive slope section of the

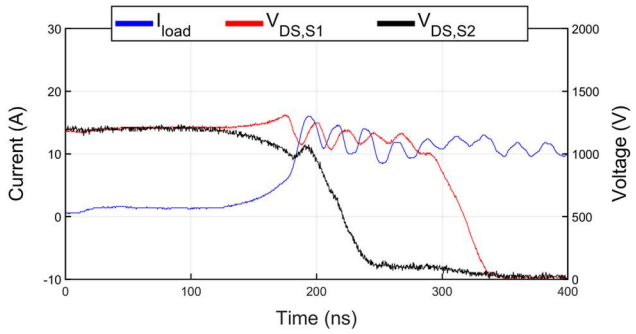

Figure 5-22. Experimental results of $V_{DS,S1}$ and $V_{DS,S2}$ during turn-ON with a 200 ns delay in offset time.

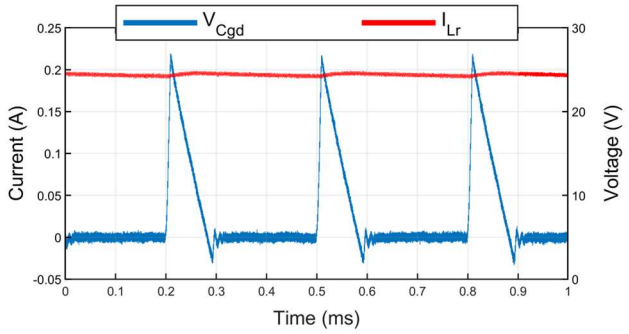

Figure 5-23. Experimental waveforms of I_{L_r} and $V_{C_{gd}}$ during bucking start-up operation.

waveforms would be longer. A noticeable ripple in $v_{C_{gd}}$ can be seen. This can obviously be reduced by increasing C_{gd}, but this amount of ripple is acceptable for this application because C_{gd} is buffered by a variable input voltage power supply ICs. For these waveforms, the switching frequency of the bucking, and thus M_{AU}, is 3 kHz. During normal operation, this same waveform shape is seen in L_r when C_r resonates into L_r and M_{AU} is OFF; however, the peak and frequency of i_{L_r} may change depending on the operating frequency of $S1$ and $S2$ as was the case in Figure 5-18. For the tested prototype a switching frequency of 3 kHz was chosen to reduce the thermal management requirements of M_{AU}.

It is important to choose a value of L_r and a switching frequency that results in a discontinuous conduction mode for the inductor. This ensures that M_{AU} operates with quasi-ZCS at turn-ON and reduces the required thermal management. Also, this avoids the problem with diode reverse recovery of D_{C_r} affecting the energy transfer from C_r to L_r. The effect of the reverse recovery can be seen in Figure 5-24 where L_r is operating in a semi-continuous conduction mode. The reverse recovery charge depleted C_r and this results in a lower energy transfer to L_r. This can be seen in the relative peaks of the current at t ≈ 0.0 ms and t ≈ 0.1 ms. Because the discharging current slope of L_r is a function of its inductance and $V_{C_{gd}}^*$, this sets the upper limit of the buck

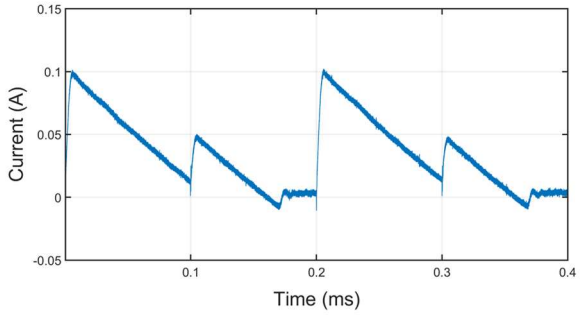

Figure 5-24. Experimental waveforms of I_{L_r} where L_r operating in continuous conduction mode.

converter switching frequency.

5.8.3 Start-Up for a Half-Bridge Application

The half-bridge test circuit is shown in Figure 5-25. The top and bottom devices of the half- bridge circuit are formed using two stackable switching positions. The performance of the half-bridge start-up procedure explained in Section 5.6 appears in Figure 5-26 and Figure 5-27 where waveforms for v_{C_a1} and v_{C_a2} and i_{L_r} are shown. The in-phase bucking modulation results in a constant C_a equal to V_s. The out-of-phase bucking modulation results in a C_a much closer to

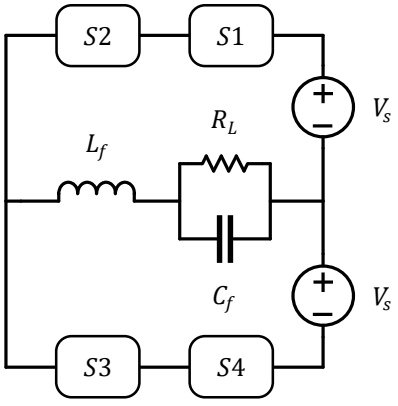

Figure 5-25. Half-bridge testing configuration.

the desired value of $2V_s$. A voltage ripple in v_{C_a} can be seen in Figure 5-27. This is due to the discharging of C_a through R_b. To reduce the voltage ripple across C_a, a larger value of R_b can be used or the switching frequency of M_{AU} can be increased.

5.9 Protection Concerns

It is important that the switching position reacts appropriately if the switching position is operating incorrectly or is experiencing an undesired condition. For this reason the switching position was designed with the following protection capabilities:

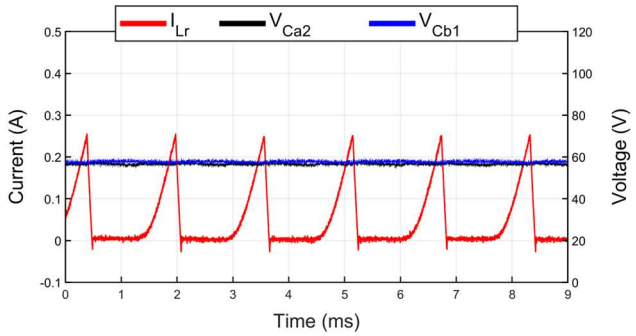

Figure 5-26. Voltage-balancing circuit capacitor voltage and self-power inductor current with in-phase start-up modulation.

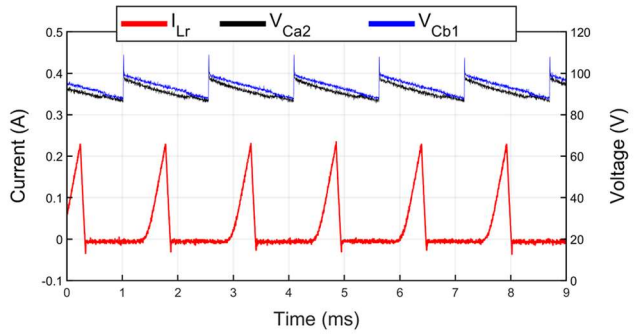

Figure 5-27. Voltage-balancing circuit capacitor voltage and self-power inductor current with in-phase start-up modulation.

1. Desaturation - An overcurrent condition turns the power semiconductor S OFF and generates a TTL error flag.
2. Gate Driver Undervoltage – The switching position will detect a malfunction of the gate drive power supply IC or a low
   voltage across C_{gd}, generating an error flag.
3. Device Overvoltage - A resistor divider and voltage comparator are used to monitor the voltage across the power semiconductor device to detect a static voltage imbalance. If the voltage is too high, then this implies the voltage is no longer being properly shared by series con nected switching positions.
4. PWM Interlocks – Open-collector logic is used with the auxiliary and main PWM to ensure that neither are ON at the same time. This prevents spurious tripping and damage to the start-up circuit if these signals are malfunctioning.
5. Auxiliary PWM Ride-Through – In the event that the converter in which this switching position is used requires an emergency shut-down, the switching position must be able to survive for a short time without any possibility to power itself. This is due to the normally-ON configuration of the start-up circuit. To provide this ride-through capability, the power rail for the auxiliary PWM fiber optic receiver circuit has been isolated through a diode from the main power rail for the gate drive and diagnostic circuitry. On this isolated power rail, a large reservoir of energy is placed. For the switching position in this paper a 1.5 F supercapacitor is used. This means, if power on the board is lost then the supercapacitor can drive M_g without having to provide power to the rest of the circuits. This energy reservoir can then be sized based on the drive current for M_g and amount of time required to discharge the energy storage in the converter.

The error signals from the desaturation, gate-driver undervoltage, and device overvoltage are all combined with TTL logic gates and then trigger an active-low master fault flag. This single flag is sent by fiber optic back to the controller. This is important because if one of the series connected switching positions has a fault the controller needs to quickly shut-down the converter.

5.10 Conclusions

A novel self-powered modular switching position with voltage-balancing ability for series-connected MOSFETs was presented. A new step-by-step procedure for choosing the components for the new configuration of the voltage-balancing circuit as well as the equations defining the self-powered behavior were also given. In addition, a novel start-up scheme for the self-powering circuitry was introduced. Lastly, the protection circuitry needed for the switching position is presented.

The behavior of the circuitry was confirmed by simulations. The voltage-balancing behavior of a 3.3-kV switching position made up of two 1.7-kV SiC MOSFETs was experimentally verified under current-source loading demonstrating the feasibility of the proposed ideas. In particular, the prototype was also experimentally shown to be capable of powering itself from the voltage across it.

5.11 Appendix

Below is an example design of the voltage-balancing circuit for the circuit in Figure 5-3 with a current-source load:

1. Decide on the gate driver parameters. They are chosen to be

$$R_g = 2.5\ \Omega\,,$$

$$V_g^+ = 20\ \text{V}\,,$$

$$V_g^- = -5\ \text{V}\,.$$

2. Choose the maximum voltage overshoot, ΔV_{DS}, for the switch S. The value is chosen to be

$$\Delta V_{DS} = 200\ \text{V}\,.$$

Then, R_{gg} is calculated as

$$R_{gg} < \frac{(200\ \text{V})(2.5\ \Omega)}{(3\ \text{V}) - (-5\ \text{V})},$$

$$R_{gg} < 30\ \Omega\,,$$

with $V_{g,on} \approx 3$ V. An R_{gg} of 10 Ω is chosen.

3. Determine the current balance between i_1 and $i_{\text{R}_{S_2}}$ during MODE II. The circuit parameters are

$$I_L = 10\ \text{A}\,,$$

$$V_s = 1200\ \text{V}\,.$$

The steady-state values of V_{C_g} and V_{C_b} from the model simulations are

$$V_{C_g,ss} = 6.5\ \text{V}\,,$$

$$V_{C_b,ss} = 50\ \text{V}\,.$$

The value of i_1 and $i_{\text{R}_{S_2}}$ are the given by

$$i_1 = \frac{6.5\ \text{V} - (-5\ \text{V})}{2.5\ \Omega},$$

$$i_1 \approx 5\ \text{A}\,,$$

$$i_{\text{R}_{S_2}} = 10\ \text{A} - 5\ \text{A} = 5\ \text{A}\,.$$

4. Determine the value of C_b. The worst-case gate pulse offset is chosen as

$$t_{off} = 200 \text{ ns}.$$

The calculated waveforms for v_{C_g} and $v_{C_b}/10$ for different values of C_b is shown in Figure 5-28.

When C_b is 100 nF, v_{C_g} takes almost the entire t_{off} to charge to $V_{g,on}$. This indicates an oversizing of C_b. At 0.33 nF, v_{C_b} charges above $V_{C_b,ss}$ before $v_{C_g} = V_{g,on}$. This indicates an appropriate value of C_b. From this analysis the chosen capacitor values are

$$C_b = 0.33 \text{ nF},$$

$$C_a = 100C_b = 33 \text{ nF}.$$

5. Calculate the extra energy absorbed by C_a. From gate drive components datasheets, a mismatch in propagation delay can be predicted between any two devices connected in series. An average value of t_{off} = 20 ns is assumed. From the calculated waveforms, the RMS current into C_a is 2.9 A. The average energy absorbed by C_a is then

$$\Delta E_{C_{a,avg}} = (1200 \text{ V})(2.9 \text{ A})(20 \text{ ns}) = 70 \text{ µJ}.$$

The power required to be dissipated by R_b is

$$P_{C_a} = (70 \, \mu\text{J})(10 \text{ kHz}) = 0.8 \text{ W}.$$

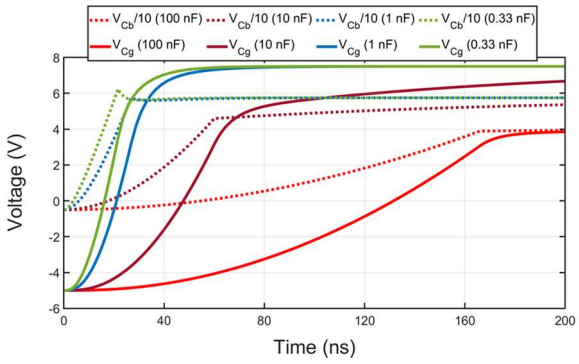

Figure 5-28. V_{C_g} and $V_{C_b}/10$ for different values of C_b.

$$R_b < \frac{(1200\ \text{V})^2}{0.8\ \text{W}}(0.5)$$

$$R_b < 900\ \text{k}\Omega$$

Assuming a mismatch in OFF-state leakage current of 12 µA between the power devices R_a can be determined by

$$R_a = \frac{1200\ \text{V}}{10(12\ \mu\text{A})}$$

$$R_b = 10\ \text{M}\Omega$$

5.12 Acknowledgments

Testing was conducted at the National Center for Reliable Electric Power Transmission (NCREPT), the University of Arkansas' High-Power Test Facility.

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CHAPTER 6

A HYBRID SNUBBER FOR VOLTAGE-BALANCING AND SELF-POWERING OF SERIES-CONNECTED DEVICES

V. Jones, J. C. Balda, and R. Adapu, "A Hybrid Snubber for Voltage-Balancing and Self-Powering of Series-Connected Devices," presented at the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, 2019.

6.1 Abstract

With SiC devices enabling much higher voltage converters with lower complexity, a modular switching position that eliminates some of the issues with medium-voltage converters (e.g., high isolation voltages and dv/dt's) would be valuable. Full modularity requires the ability to stack any arbitrary number of units in series. A requirement for this functionality is voltage balancing between all series switches. This paper introduces a hybrid snubber that attempts to solve these dynamic and static voltage balancing issues as well as providing power for each switch from the bus to which it is connected. A method for determining the required component values is developed and simulations are used to test the viability of the circuit. Then, a 600 V prototype is constructed using two MOSFETs in series to confirm the functionality of the snubber.

6.2 Introduction

Continued advances in high-voltage SiC devices and the push towards medium-voltage converters with multilevel topologies using these devices calls for a truly modular switching position. This requires the elimination of common-mode voltage issues for power and control signals as well as compensation for imperfect voltage sharing between series devices. The traditional methods by which the gate driver power supplies are designed becomes a challenge at medium voltages because the level of isolation required can be greater than 25 kV with dv/dt's

across this isolation barrier greater than 100 kV/µs. This type of performance requires careful design of a galvanically isolated power supply and sometimes non-traditional supply configurations that can result in large and expensive solutions; this same problem is seen in cascode and series connected switches [1-3]. Power-over-fiber (POF) systems can be used but these are large and relatively inefficient [4]. Self-powered gate driver topologies have been suggested in [5-8] to remove the common-mode voltage issue. Fiber optic cable can then be used for control signals.

Several different voltage-balancing circuit were proposed [9-12]. In an attempt to make a completely modular and "stack-able" switch position, [13] suggested a combined self-powered and voltage-balancing circuit. To achieve the same goal but eliminating losses in the quiescent power resistors, a hybrid of the snubber in [12] and a novel self-powered circuit are proposed.

6.3 Design of the Voltage Balancing Circuit

The circuitry associated with the voltage balancing is shown in Figure 6-1. With switches S1 and S2 initially off and with balanced voltages across them, assume that S2 begins to turn-on before S1. Capacitor Ca >> Cb so as VDS1 begins to increase almost all voltage appears across Cb which then charges Cg turning on the device before it is destroyed. Though the snubber was suggested in [12], a process for selecting the component values was not given. The design process developed here assumes a worst-case scenario in which the gate pulse offset, toff, between S1 and S2 is larger than the turn-off time of S2 and the turn-on time of S1 combined. To give a starting point for selecting component parameters by approximating the device behavior, the process is as follows:

1. Design the gate drivers using normal methods [14-16].

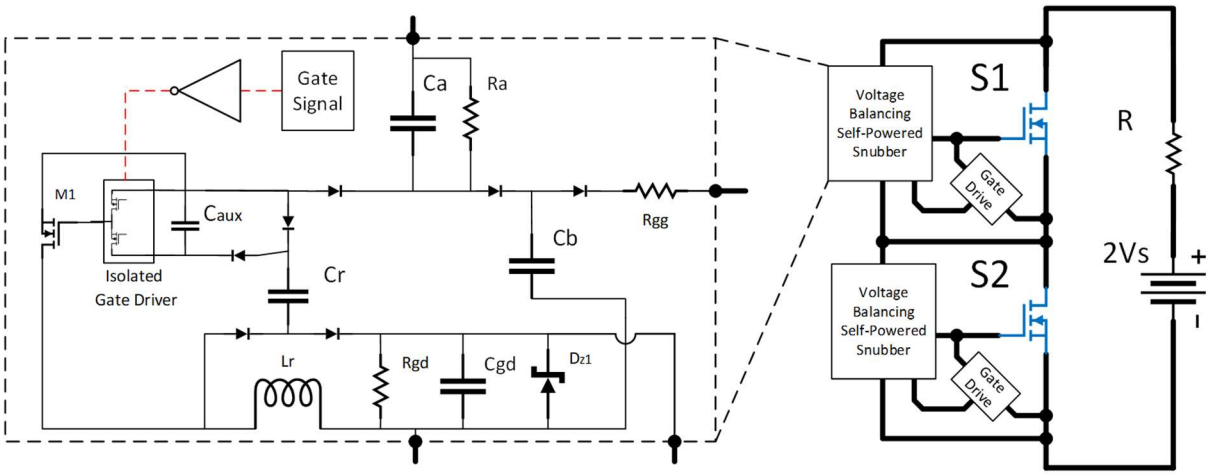

Figure 6-1. Proposed voltage balancing self-powered gate driver.

2. Choose maximum overshoot ΔV_{DS} for S1. R_{gg} is chosen using:

$$R_{gg} = \frac{R_g\left(\Delta V_{DS} - \left(V_{g,on} - V_g^-\right)\right)}{V_{g,on}} \tag{1}$$

with $V_{g,on}$ as the gate voltage at which the device begins to turn on (approximated from the datasheet) and V_g^- the designed off-state gate voltage from Step 1.

3. Determine the value of C_b. The voltage across C_b and the gate capacitance, C_g, are defined in the Laplace domain as:

$$V_{C_b}(s) = \left(\frac{N_1}{D_1}\right)(V(s) - V_2(s)) + V_2(s) \tag{2}$$

$$N_1 = C_g R_g R_{gg} s + R_g + R_{gg} \tag{3}$$

$$D_1 = C_b C_g R R_g R_{gg} s^2 + \ldots \\ R\left(R_g + R_{gg}\right)\left(C_b + C_g\right)s + R + R_g + R_{gg} \tag{4}$$

$$V_2(s) = \frac{N_2}{D_2} \tag{5}$$

$$N_2 = R_g R_{gg} C_b C_g V_{C_b}(0)s^2 + R_g C_b V_{C_b}(0)s + \ldots \\ R_g C_g V_{C_g}(0)s + R_{gg} C_b V_{C_b}(0)s + V_g^- \tag{6}$$

$$D_2 = s\big(R_g R_{gg} C_b C_g s^2 + R_g C_b s + \ldots \\ R_g C_g s + R_{gg} C_b s + 1\big) \tag{7}$$

$$V_{C_g}(s) = \left(\frac{R_g}{C_g R_g R_{gg} s + R_g + R_{gg}}\right) \ldots \\ \Big(V_{C_b}(s) - V_1(s)\Big) + V_1(s) \tag{8}$$

$$V_1(s) = \frac{R_g C_g V_{C_g}(0)s + V_g^-}{R_g C_g s^2 + s} \tag{9}$$

with $V_{Cb}(0)$ and $V_{Ciss}(0)$ as initial conditions, and R and R_g as the load and gate resistances. Capacitor C_g is approximated by the C_{iss} specified in the datasheet. Table 6-1 describes the value of $V(s)$ during each mode of the compensation action. Times t_f and t_r are the fall and rise times of the MOSFET, and V_S is the nominal off-state switch voltage. Using the inverse Laplace of (2)-(5), C_b is chosen such that the circuit is operating in MODE IV at the point of the turn-off time toff. This minimizes C_b and

Table 6-1. Values of $V(s)$ during each period of the turn-on compensation action

MODE	$V_{Cb} > V_{g,on}$	C_b [a.]	C_g [a.]	$V(s)$	Duration
I	X	+	+	$\frac{V_S}{t_r s^2}$	t_r
II	X	+	+	$\frac{V_S}{s}$	$t(V_g = V_{g,on}) - t_r$
III	✓	-	+	$\frac{V_S}{s} - \frac{V_S}{t_f s^2}$	t_f
IV	✓	-	-	0	$t_{off} - t(MODE\ I, II, III)$

a. Indicates whether the given capacitor is charging (+) or discharging (-)

thus C_a while assuring there is no on-off device oscillations.

4. Calculate the extra energy, ΔE_{Ca}, that is absorbed by C_a. This energy needs to be removed, otherwise V_{Ca} will continue to fluctuate for as long as $|t_{off}| > 0$.

6.4 Design of the Self-Powered Circuit

In the interest of reducing the net losses of the snubber, a resonant self-powered gate driver circuit in Figure 6-1 was constructed around using the excess energy from C_a. Upon turn-on of the switch, current resonates from C_a through L_r and into C_r as shown in Figure 6-2(a). This current, i_{Lr1} is defined by:

$$i_{Lr1}(t) = \frac{V_{C_a} - V_{C_{gd}}}{\sqrt{\frac{L_r}{C_r} - \frac{R_{eq}^2}{4}}} e^{-\delta t} \sin(\omega t) \tag{10}$$

$$\omega = \sqrt{\frac{1}{L_r C_r} - \left(\frac{R_{eq}}{2L_r}\right)^2} \tag{11}$$

$$\delta = \frac{R_{eq}}{2L_r} \tag{12}$$

where V_{Ca} is the voltage across C_a, V_{Cgd} is the voltage across C_{gd}, and R_{eq} is the equivalent series resistance of the current path. The peak of this current coincides with the charging of C_r to V_{Ca} resulting in a total energy given by:

$$E_T = \frac{1}{2}\left(L_r I_{pk1}^2 + C_r V_{C_a}^2\right) \tag{13}$$

$C_{aux} >> C_r$ so most of the voltage is seen across C_r.

The voltage across L_r reverses to maintain the flow of current and the energy in L_r then resonates into C_{gd} which is demonstrated in Figure 6-2(b). Once the main switch turns off a

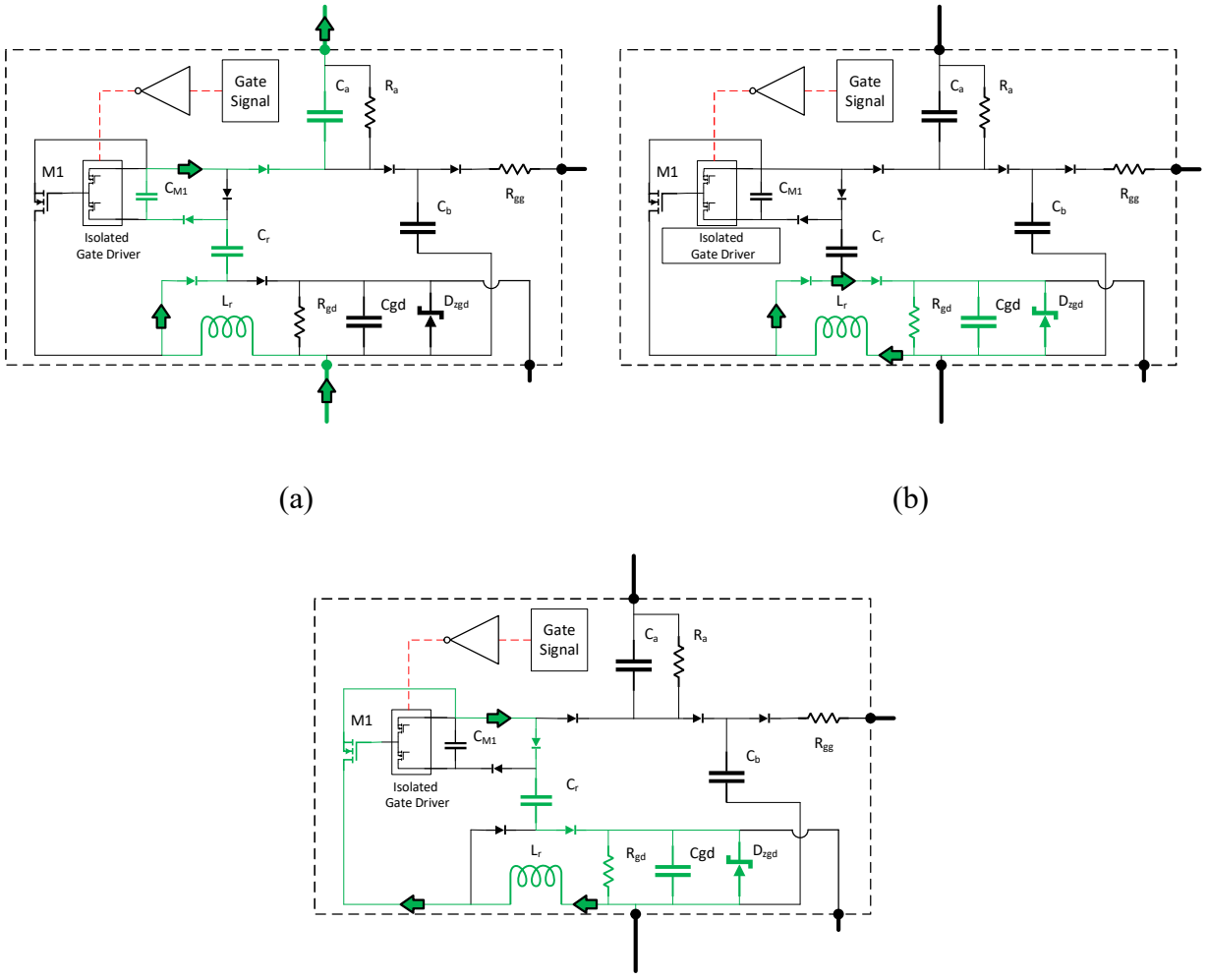

Figure 6-2. Current commutations during the on- and off-times of S2.

secondary gate driver uses the energy in C_{aux} to turn on M1 and resonate the energy in C_r through C_{gd} and L_r until the voltage across C_r reaches V_{Cgd}.

This current can be defined again with (6), however V_{Ca} becomes V_{Cr} and R_{eq} must be adjusted accordingly. This can be seen in Figure 6-2(c). At this point the voltage across L_r reverses and its energy is again resonated into C_{gd} (Figure 6-2(b)). This process assures that most of the energy removed from C_a is delivered to C_{gd}.

6.5 Snubber Simulation Results

The parameters of the simulated switching position are shown in Table 6-2. The voltage balancing action of the snubber was simulated using OrCAD® PSpice®. The calculated values for V_{cb}/10 and V_g during the turn-on compensation event with 1,200 V across S1 and S2 and 10 A of resistive load is shown in Figure 6-3. Simulations were done utilizing Wolfspeed SiC MOSFET spice models with the turn-on of S2 modeled with a ramp function. The comparison between the

Table 6-2. Snubber Parameters

Parameter	Value	Parameter	Value
Ca	100 nF	Lr	2.2 mH
Cb	1 nF	Cr	1 nF
Ra	1 MΩ	Caux	88 nF
Rgg	60 Ω	S1	C2M0025120
Cgd	10 µF	M1	C2M0025120

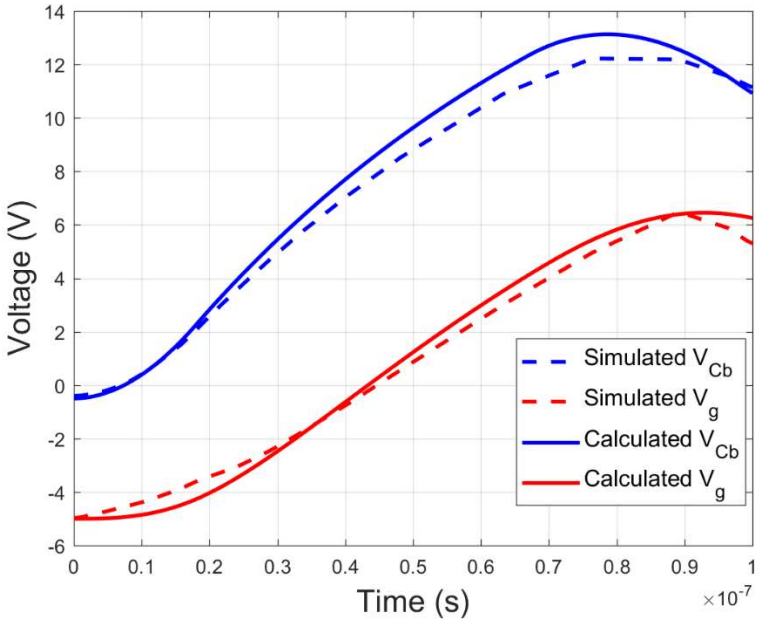

Figure 6-3. Calculated vs simulation values of V_{cb}/10 and V_g.

two is not without some error, but this does indicate a good starting point for choosing the parameter values of the snubber.

Simulations of the self-powered circuitry were performed in Matlab/Simulink® using the 2018a Simscape™ library components. In Figure 6-4 the voltage at the gate of S2 (V_{gate}), the voltage across C_{aux} (V_{Caux}), V_{Cgd}, and the current through L_r (I_{Lr}) are shown at 300 V bus with 0.15 A of resistive load. The slope of I_{Lr} during the discharge period of the "off-time" of S2 is different due to the additional conduction path formed by C_b and R_{gg} and the gate driver resistances. This current path is shown in Figure 6-5. The proportion of the energy lost to this additional conduction path and thus the efficiency of the "off-time" resonance is a function of the value of C_b and R_{gg}. With a smaller C_b, less energy will be drawn from L_r; a larger R_{gg} will have the same effect. If R_{gg} is small enough, potentially none of the energy stored in L_r is transferred to C_{gd}. Thus, it is important to minimize C_b during the voltage balancing circuit design and

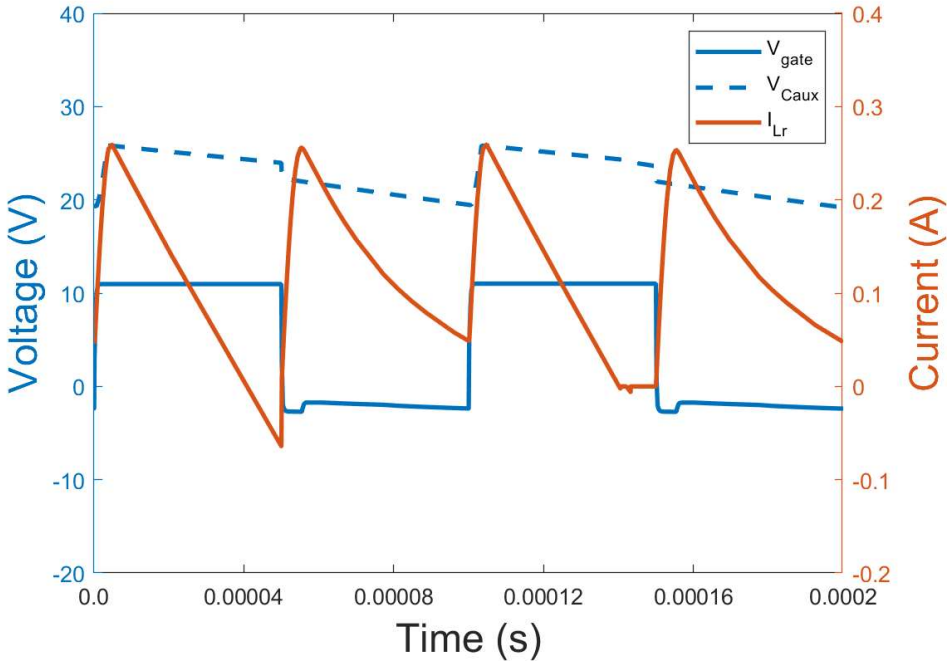

Figure 6-4. V_{gate}, V_{Caux}, and I_{Lr} during turn on and turn-off of S2.

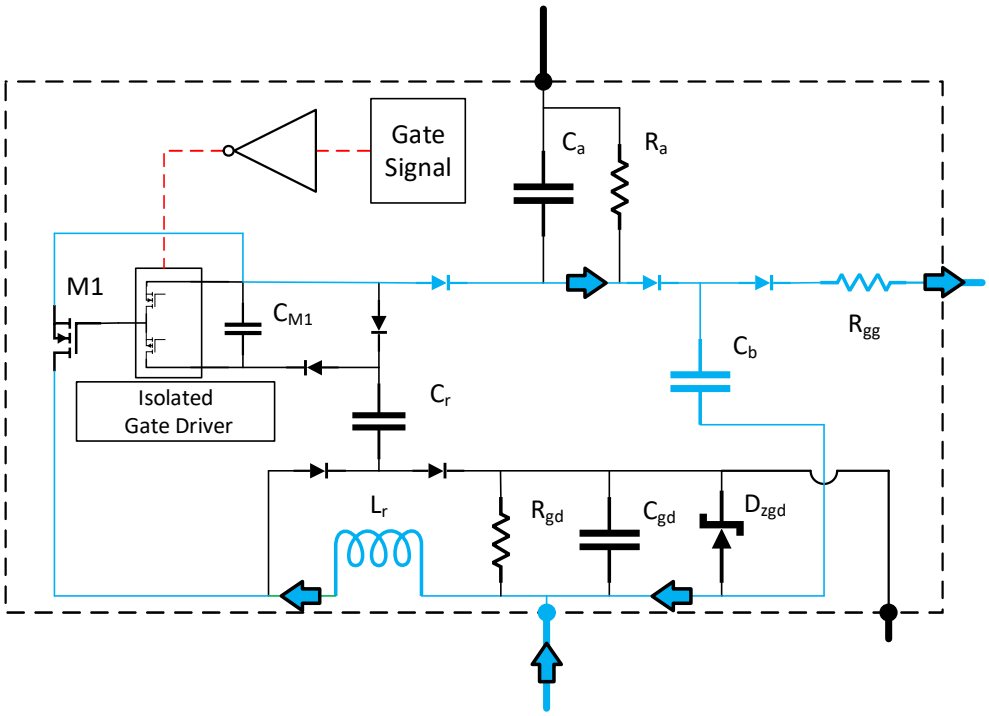

Figure 6-5. Additional current paths during the off-time of S2.

realize the trade-off between over-voltage across S2 and this efficiency (i.e., the selection of R_{gg}). The same waveforms as Figure 6-4 are displayed in Figure 6-6, but with a much larger R_{gg}. The effect is a slope of I_{Lr} that is nearly identical to its slope during the "on-time" of S2.

6.6 Snubber Experimental Results

The gate- and drain-source voltage for S1 and S2 during a turn-on event are illustrated in Figure 6-7 for a 625 V, 0.3 A test setup. The gate signal for S1 is delayed with respect to S2 by 200 ns. An overshoot at the turn-off of S1 of 50 V results in a 16 % overshoot. A decrease in R_a would decrease the voltage difference between the two switches when open but would result in higher losses.

The self-powered circuitry helps to bring balance when one switch begins to have a larger applied voltage than the other because the energy removed from C_a has a positive relationship to the voltage magnitude across it. Therefore, more energy is drawn from the capacitance when the

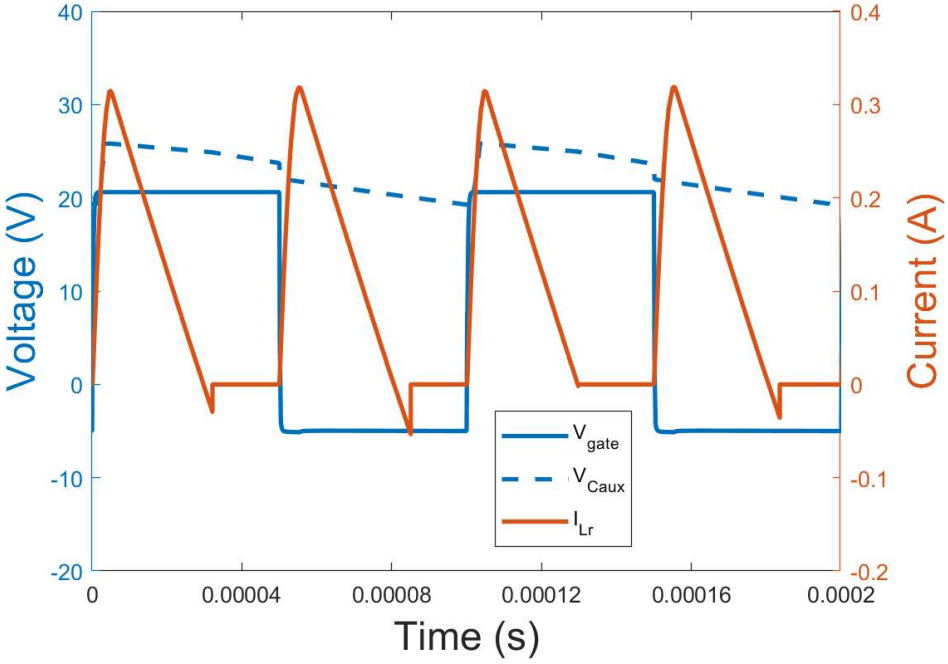

Figure 6-6. V_{gate}, V_{Caux}, and I_{Lr} during turn on and turn-off of S2.

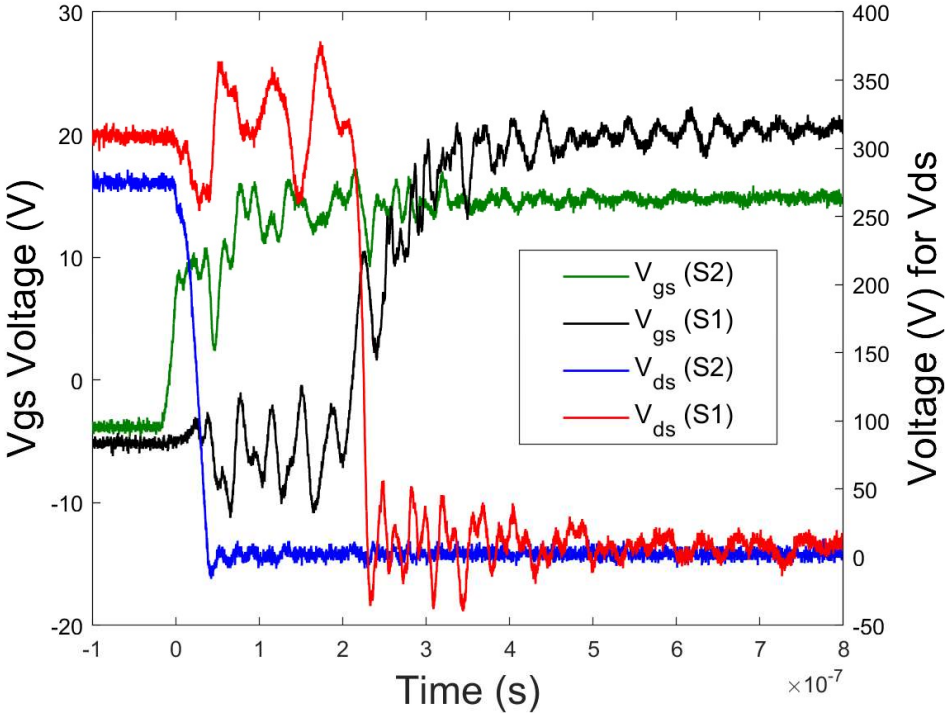

Figure 6-7. V_{ds} and V_{gs} for S1 and S2 during a turn-on event.

voltage across it rises.

The relative effect of this corrective action is dependent upon the proportion of energy that is stored in C_a (a function of the load current and the chosen voltage-balancing circuitry) and the amount of energy removed by the self-powered circuitry.

The same waveforms as shown in Figure 6-4 for a prototype with the same parameters as in Table 6-2 and the addition of V_{Cgd} are in Figure 6-8. An increased R_{gg} like in Figure 6-6 is used in Figure 6-9. The corresponding steady-state V_{Cgd} is higher due to the increased proportional energy transfer to C_{gd}.

When compared to the simulation results I_{Lr} is reduced approximately 50%. As per (6) the way to reduce this peak current is an increase in L_r or a decrease in C_r, both of which are unlikely for the selected prototype components. More likely is that a slower turn-on for the

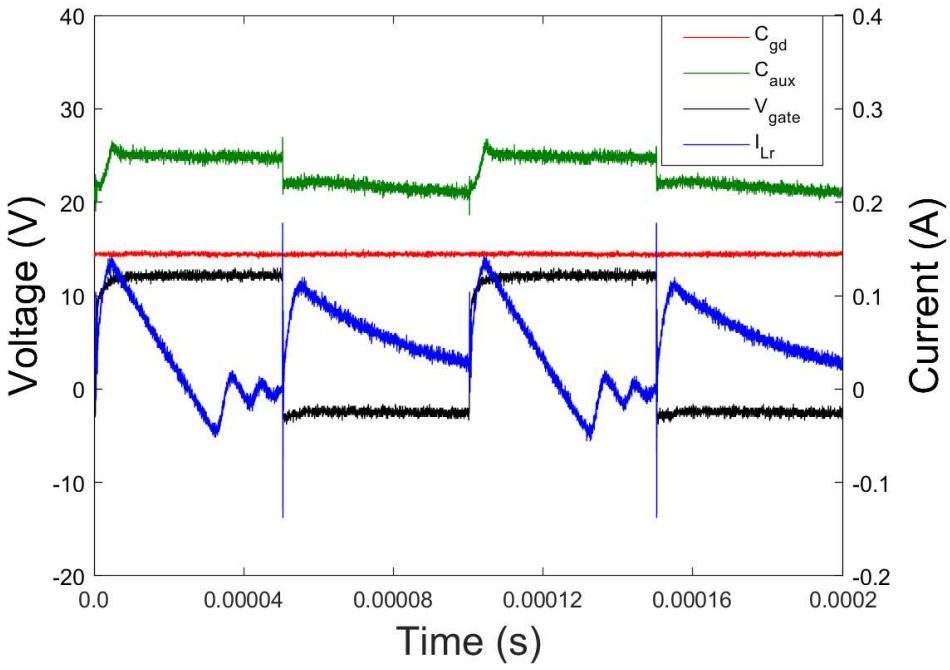

Figure 6-8. V_{gate}, V_{Caux}, and I_{Lr} during turn on and turn-off of S2.

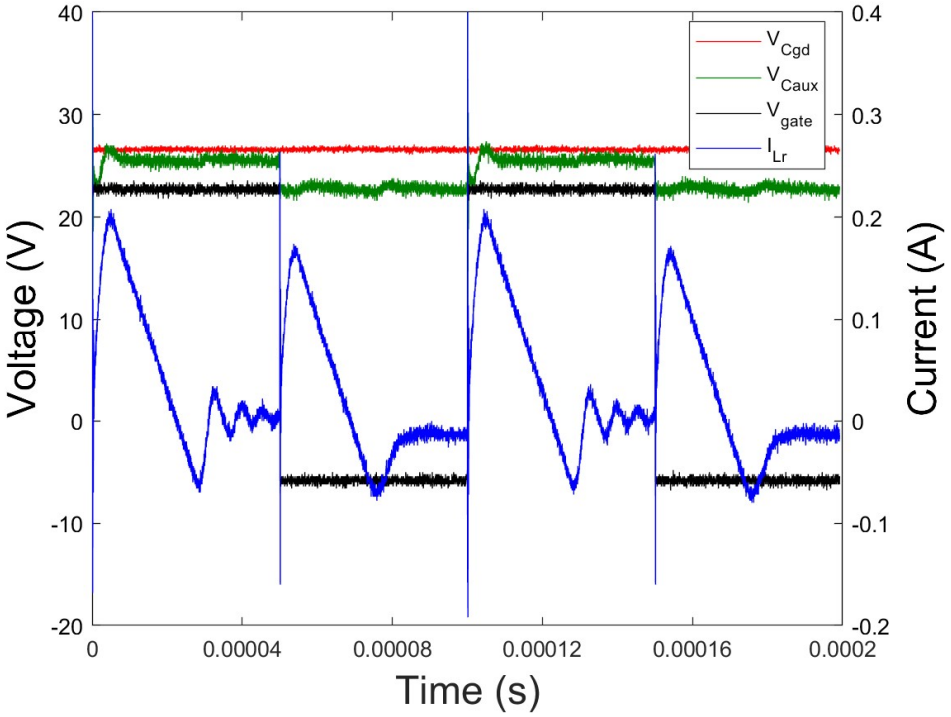

Figure 6-9. V_{gate}, V_{Caux}, and I_{Lr} during turn on and turn-off of S2 with large R_{gg}.

power MOSFETs than that used in the simulation deteriorates the practicality of the step voltage approximation used to derive (6) as well as other losses.

There are also negative currents and oscillations in I_{Lr} and V_{Caux} that are not seen in the simulation results. There are due to the parasitic capacitances of the components as well as the reverse recovery of the diodes.

6.7 Conclusions

A novel self-powered gate driver voltage-balancing hybrid snubber for series connected switches was presented. The voltage-balancing circuit has been shown to statically and dynamically balance the voltages across series-connected switches due to unbalances because of gate signal and component mismatch. The excess energy absorbed by the voltage-balancing snubber as a result of compensation was removed using the resonant self-powered gate driver

circuit where it can be utilized for other tasks instead of dissipating the energy in a shunt resistor. In addition, by combining both functions into one circuit the total efficiency of the system increased versus using two snubbers separately. A process was shown for choosing the voltage-balancing and self-powered gate driver components.

This setup paired with a fiber optic signaling scheme eliminated the common-mode currents from high-side devices that would distort supply voltages and degrade signal integrity. This allows for fully modular device "stacking." The snubber has the added benefit of absorbing energy from parasitic inductances during switching transitions as in a traditional RCD snubber.

This type of solution lends itself to solutions where there is always a voltage across the switch like in back-to-back converters and grid-connected inverters. This would be the only way to assure that the switch will always have power and can be controlled. This may limit some soft-start schemes that require control of the devices before full voltage is applied across the switch as well as any converters that utilize zero-voltage switching.

6.8 Acknowledgments

The authors are grateful for initial financial support from the NSF I/UCRC Grid-Connected Advanced Power Electronic Systems (GRAPES) under grant IIP-1439700. The authors are also grateful for the financial support through a tailored collaboration project between EPRI, Southern Company and Arkansas Electric Cooperative Corp.

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CHAPTER 7

TESTING RESULTS OF THE MV-UCSC PROTOTYPE

7.1 Experimental Setup for the MV-UCSC Prototype

The MV-UCSC prototype was tested with direct connection to the medium-voltage (MV) grid available at NCREPT under different operating conditions. The various test configurations are described in Appendix A. The first test consisted of evaluating the start-up procedure at ±12 kV dc bus voltage. Then, two MV load tests were carried out. The first test has an 11-level MV-UCSC connected to a 1.8 kV_{LL} ac grid that was formed using a 480V-13.8kV/4.16kV three-phase transformer with the 4.16 kV tap energized with 208 V_{LL} on the 480V_{LL} side. The second test has a reconfigured 5-level MV-UCSC connected to a 4.16 kV_{LL} ac grid; the 4.16 kV tap of the transformer was used.

A single phase is loaded with a power factor of approximately 1.0 using the 750 kW resistive load bank in both tests. The other phases carry no current. Lastly, the efficacy of the voltage-balancing circuit with the 3.3 kV switching position was verified by carrying out a test when connected to a 480 V_{LL} ac grid due to the limitation of the available instrumentation for measuring signals with common-mode voltages higher than 2 kV.

There are three major operating modes in each test. Appendix B gives an overview of these different modes (i.e., M2, M4, and M5). The first one is the idling/bucking mode (M2) where the self-powered switching positions use their soft-start capability to provide power to the switching positions while the MV-UCSC grid tie breaker is open. A 24 kV low-power supply was built to perform this mode; using a variable ac input voltage the dc output can be ramped from 0 V to 24 kV as needed by a particular test. The second one is the grid-connected mode (M4) where the MV-UCSC maintains its dc-bus voltage by replenishing converter energy loss

using the grid. Lastly, the third one is the compensation mode (M5) where the MV-UCSC compensates for the current imbalance and reactive power of the load.

7.2 Start-Up Using the Modular Switching Positions

The converter initially is completely discharged and disconnected from the grid by a 13.8 kV grid-tie breaker. The external 24 kV power supply is used to ramp the dc-bus voltage to its nominal value of ±12 kV. While the dc-bus voltage increases, the soft-start functionality of the switching positions is initiated; that is, mode M2. The start-up scheme used by the modular stackable switching positions was outlined in Chapters 4 and 5 [1]. In this scheme, the auxiliary switch within the self-powered gate drive circuit is used to form a buck converter equivalent which allows the switching position to power itself at any voltage up to the nominal OFF-state voltage. The auxiliary PWMs used during the start-up procedure are synced between the submodules of the converter. With the start-up circuit enabled the resulting currents are shown in Figure 7-1 in red. The dc-bus voltages, a resonant inductor current from one of the switching positions, and the voltage of flying capacitor C6 are all shown in Figure 7-2. With each switching position consuming essentially the same power, this modulation maintains the balance between the flying capacitor voltages during the start-up period while providing power to the switching positions at below the nominal dc-bus voltage. The voltage of capacitor C6 has small ripple around 14.4 kV which matches the predicted voltage of [24 kV/(11-1)*6 = 14.4 kV] for this capacitor. The square-wave voltage ripple and voltage spikes shown in Figure 7-2 are exaggerated due to the configuration and type of probe (Tektronix® P6015A) used to measure these voltages.

7.3 Testing of the MV-UCSC with 11-Levels and 1.8 kV AC Grid

During this test, the MV-UCSC is configured with 11-levels (20 switching positions per phase) and a dc-bus voltage of ±2.9 kV. Figure 7-3 displays the load currents where phase A is

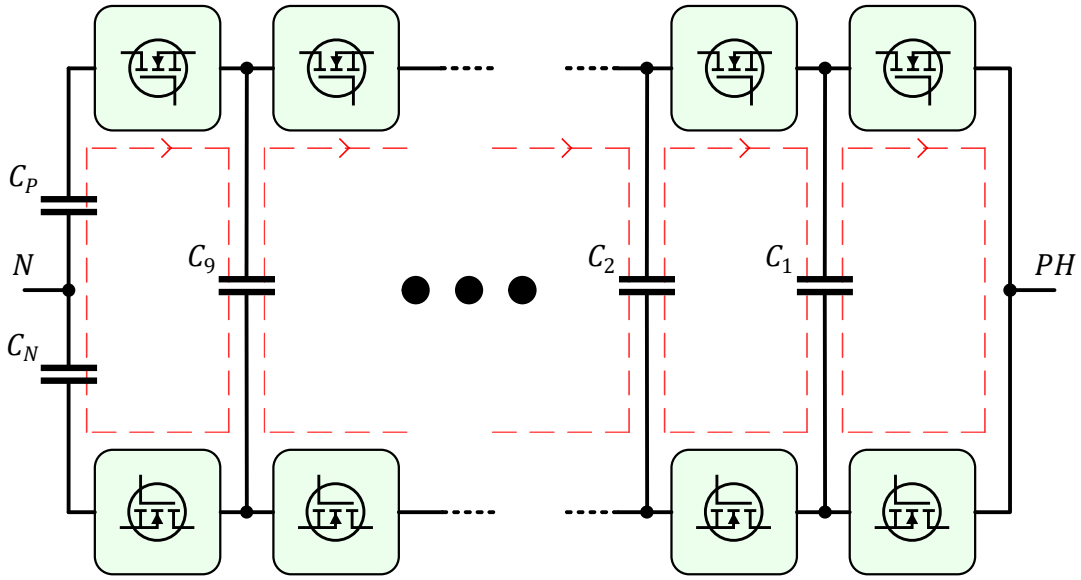


Figure 7-1. MV-UCSC start-up current paths.

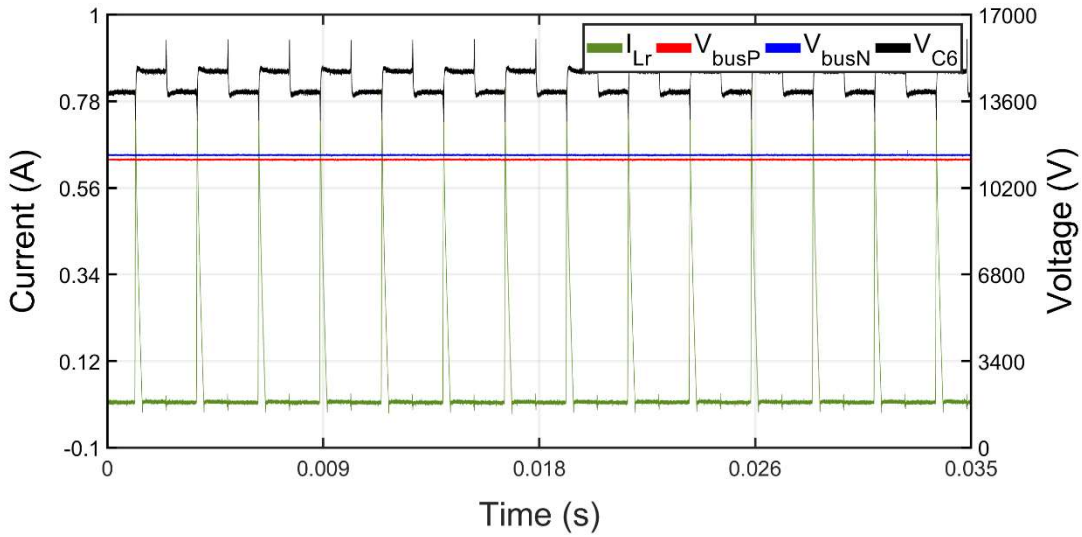


Figure 7-2. DC-bus voltages, resonant inductor current, and flying capacitor voltage during the start-up interval of the 11-level MV-UCSC at ±12 kV bus.

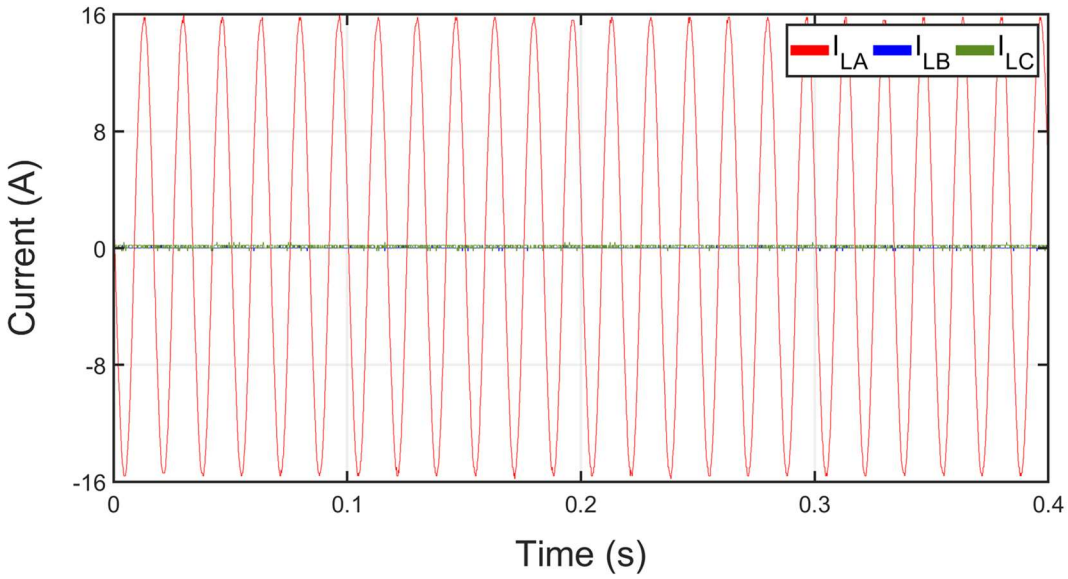


Figure 7-3. Three-phase unbalanced load currents; only phase A has a load.

loaded with approximately 10 A_{rms} and the other two phases carry no current. This current imbalance results in a negative- and zero-sequence current magnitudes of 3.3 A (after applying Clarke's transformation).

The MV-UCSC output currents are shown in Figure 7-4. From t = 0.00 s to t = 0.04 s, the converter is in idle/bucking mode (M2) and the switching positions are performing the self-powering bucking action described in Section 7.2.1 (M2). At t = 0.04 s, the grid-tie breaker closes and the control algorithm stabilizes the various voltages in the MV-UCSC; that is, mode M4.

At t = 0.13 s, the compensation for the load current imbalance starts; the beginning of M5. The compensation current references are ramped from 0 to 100% over 0.05 s. At t = 0.32 s, the grid-tie breaker opens and the converter switching positions go back to idle/bucking mode M2.

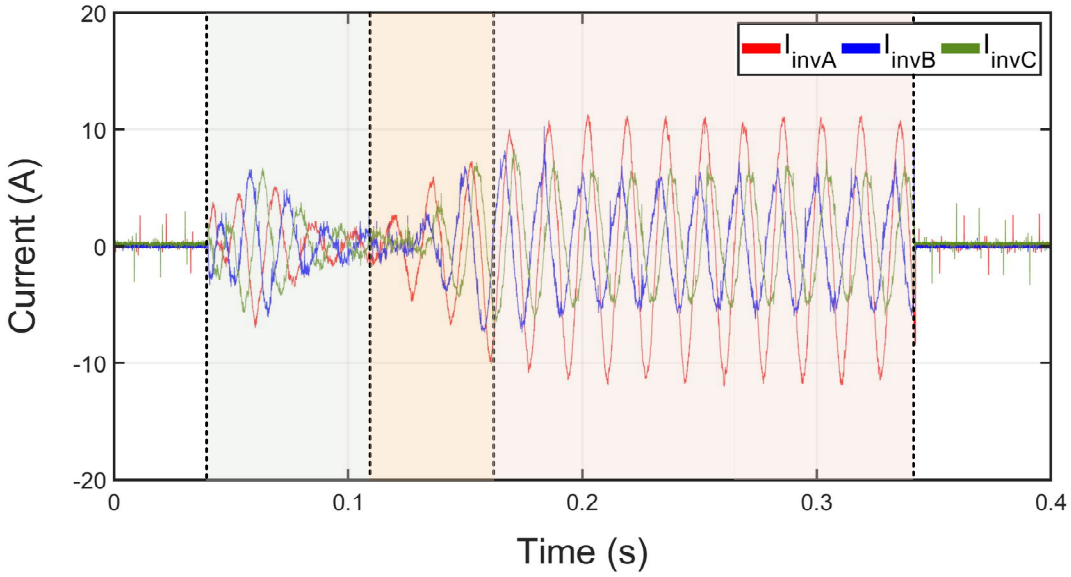


Figure 7-4. MV-UCSC experimental output currents with the 1.8 kV ac grid.

At t = 0.04 s, a small initial inrush current can be seen in the current, but then the currents converge to nearly zero as the converter is only replenishing converter losses to maintain the dc-bus voltage (during M4). At t = 0.13 s, the current in each phase of the converter begin to increase as the compensation action ramps up (during M5). These currents then immediately cease when the breaker opens at t = 0.32 s (returning to M2). These periods are indicated by colored zones within Figure 7-4.

The substation currents given in Figure 7-5 experience similar behavior. The substation currents separated by phase is presented in Figure 7-6. Starting at approximately t = 0.18 s, the MV-UCSC has fully balanced the substation currents and maintains this operation until the opening of the breaker at t = 0.32 s. The upstream negative- and zero-sequence current components have been reduced from 3.3 A to negligible values. It is observed in Figure 7-5 that the substation supplies unbalanced currents after disconnecting the MV-UCSC.

The positive and negative dc-bus rails are given in Figure 7-7 along with the voltage of one of the flying capacitors in Figure 7-8. The dc bus has a ripple of ±50 V or 3.3%, which

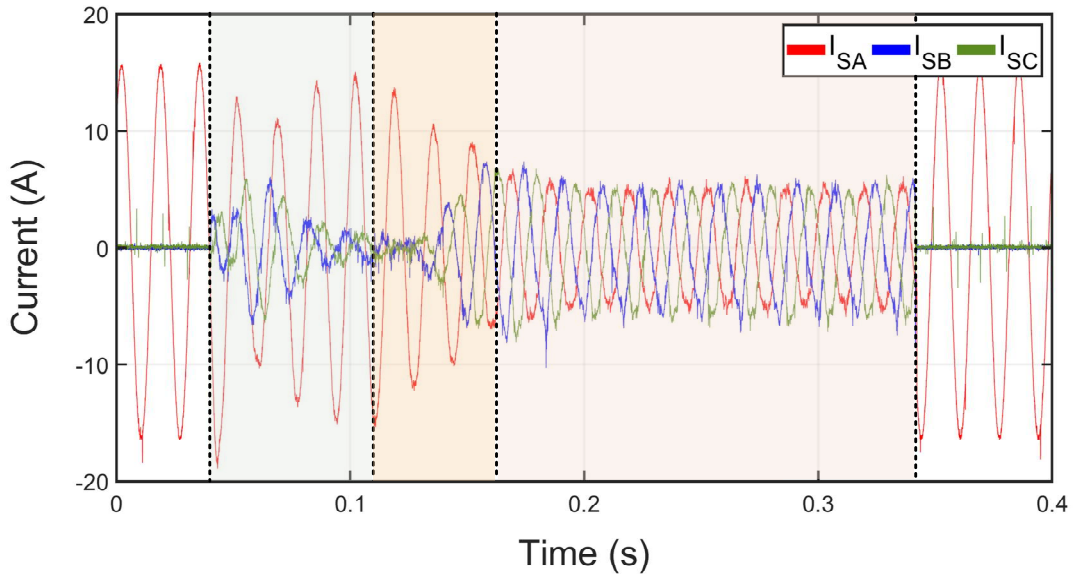


Figure 7-5. Experimental substation currents with the 1.8 kV ac grid.

for this reduced voltage level is within the 5% ripple expected at these current levels. The voltage of the flying capacitor which is the closest to the dc bus is at a dc value of approximately 5.1 kV. This is close to the expected value of [5.8 kV/(11 – 1)*9 = 5.2 kV]. The ripple is ±200 $V_{pk\text{-}pk}$ or ±5.1% which is close to the expected ripple of ±5% for the MV-UCSC with these operating conditions [2].

The dc-bus voltages are effectively controlled by the MV-UCSC and the flying capacitor voltage remains stable as well due to the self-balancing nature of the flying capacitor converter [3].

Figure 7-9 contains the resonant inductor current for one of the switching positions (red waveform) as well as $V_{C_{gd}}$, the voltage of the self-powered gate driver output capacitor (blue waveform). This bucking action occurs at a frequency of 0.8 kHz, but the main power switching frequency is 10 kHz, which causes the difference in the resonant inductor peak currents between Idle/Bucking (M2) and Run/Grid-Connected modes (M4 and M5). It can be seen that the voltage

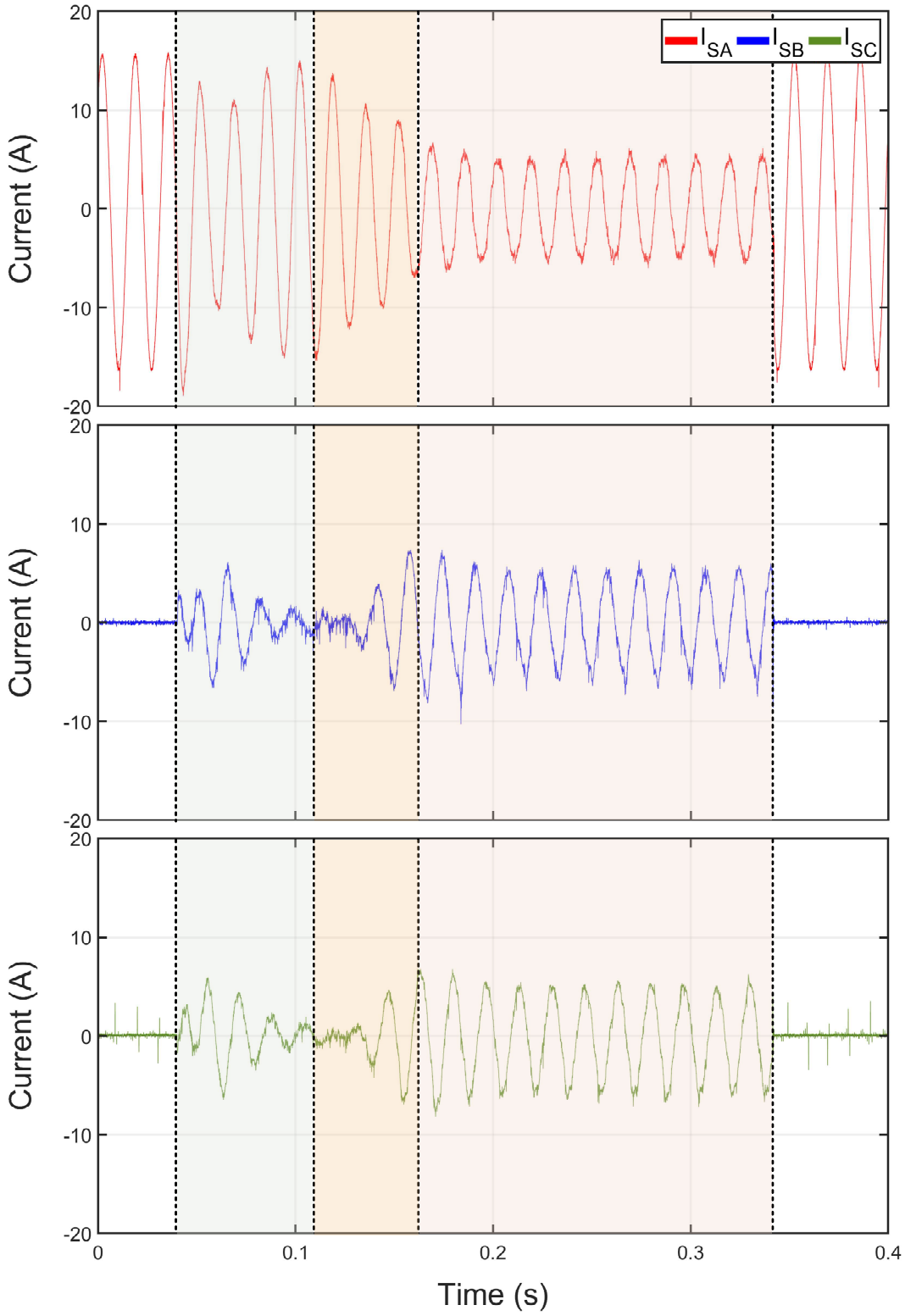


Figure 7-6. Experimental substation currents separated by phase with the 1.8 kV ac grid.

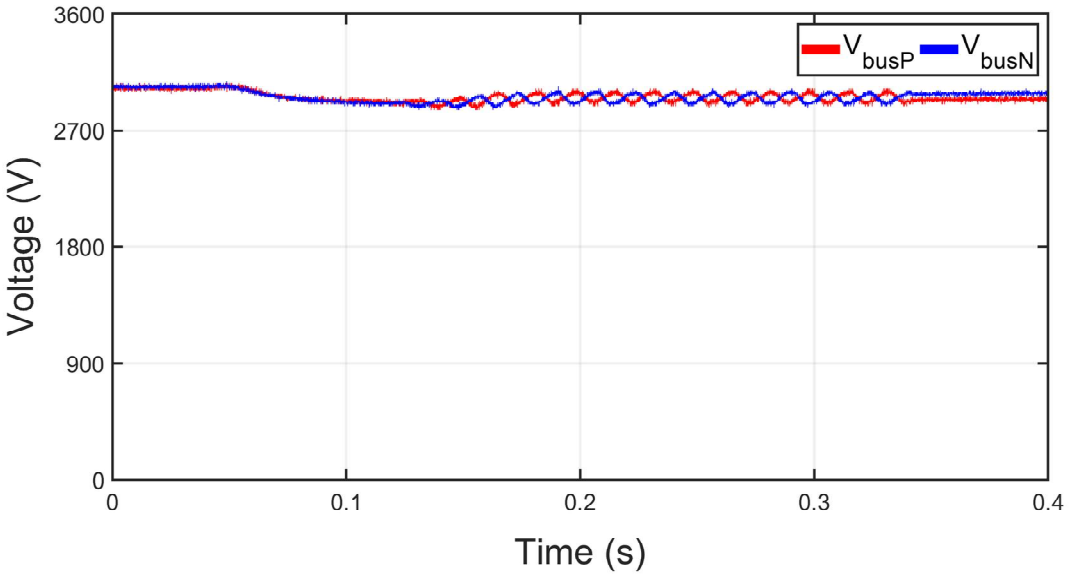


Figure 7-7. MV-UCSC experimental dc-bus capacitance voltages with the 1.8 kV ac grid.

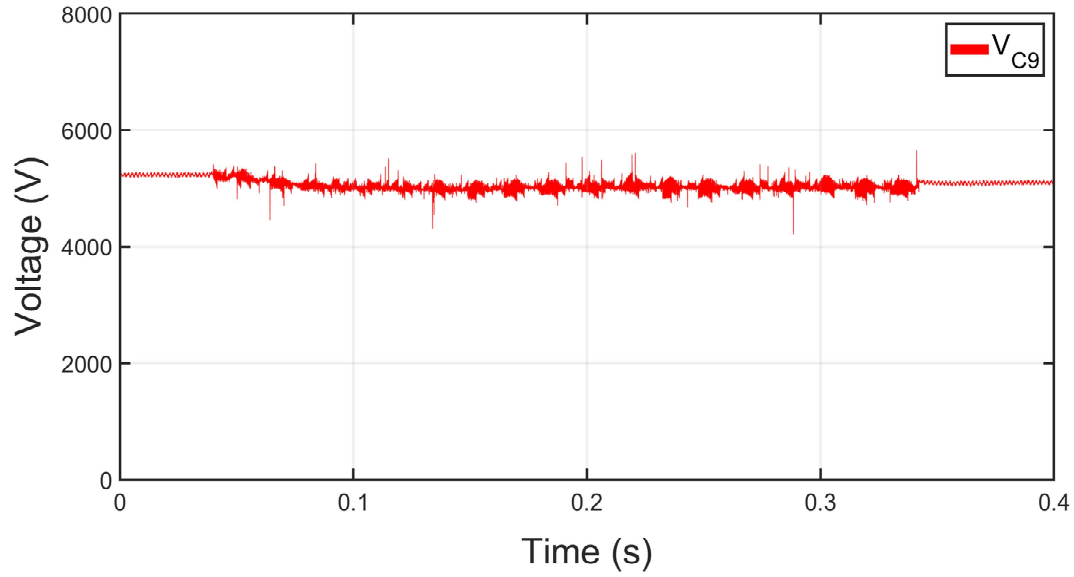


Figure 7-8. MV-UCSC experimental flying capacitor voltage with the 1.8 kV ac grid.

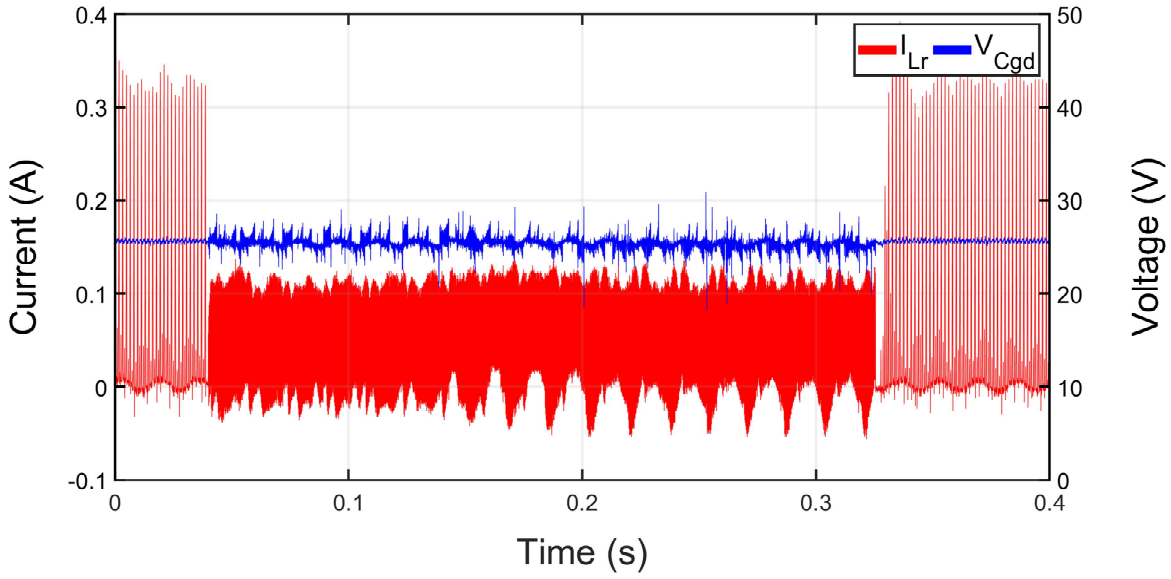


Figure 7-9. Experimental resonant inductor current and output capacitor voltage within the self-powered circuit with the 1.8 kV ac grid.

$V_{C_{gd}}$ remains constant at around 24 V, and thus, the switching positions are effectively powering themselves.

7.4 Testing of the MV-UCSC with 5-Levels and 4.16 kV AC Grid

For this test, the MV-UCSC is configured with 5-levels (8 switching positions per phase) and a dc-bus voltage of ±5.05 kV. This results in an effective voltage of 2.5 kV across each switching position. Phase A is loaded with approximately 14 A and the other two phases have no current as can be seen in Figure 7-10. This results in negative- and zero-sequence references that are ramped from 0 to 100% over 0.05 s. At t = 0.30 s, the grid-tie breaker opens and the converter switching positions go back to idle/bucking mode (M2).

At t = 0.04 s, small initial inrush currents flow but these currents converge to nearly zero as the converter is only maintaining the dc-bus voltage (M4). At t = 0.20 s, the current in each

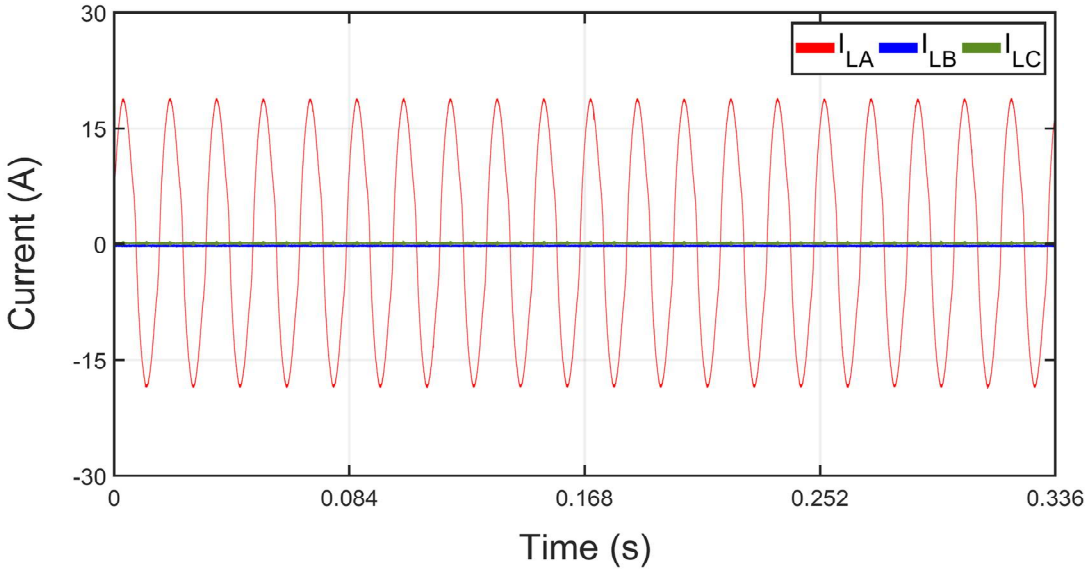


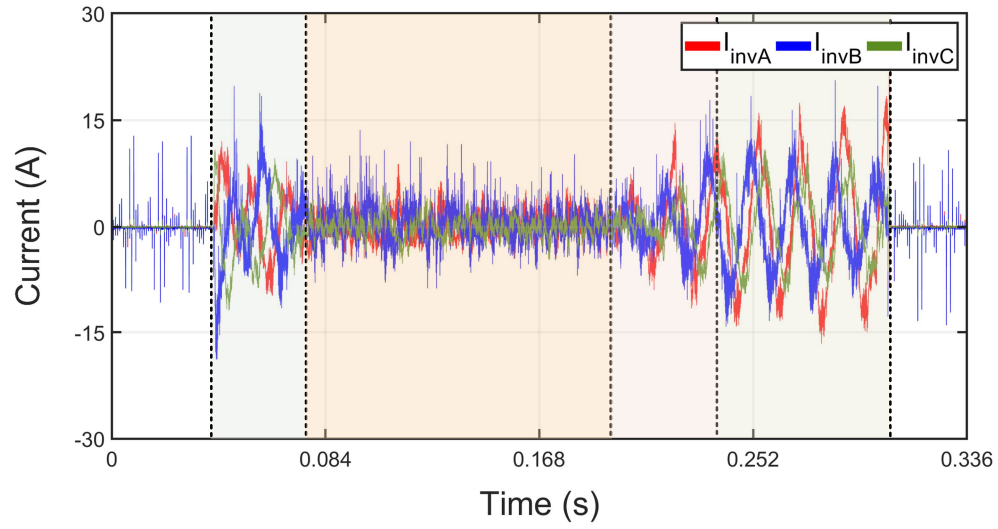
Figure 7-10. Experimental unbalanced load currents with the 4.16 kV ac grid.

phase of the converter begins to increase as the compensation action ramps up (M5). These current then immediately cease when the breaker opens at t = 0.30 s and the MV-UCSC returns to M2. These periods are indicated by the colored zones within Figure 7-11. The performance is very similar to what was expected from the simulations.

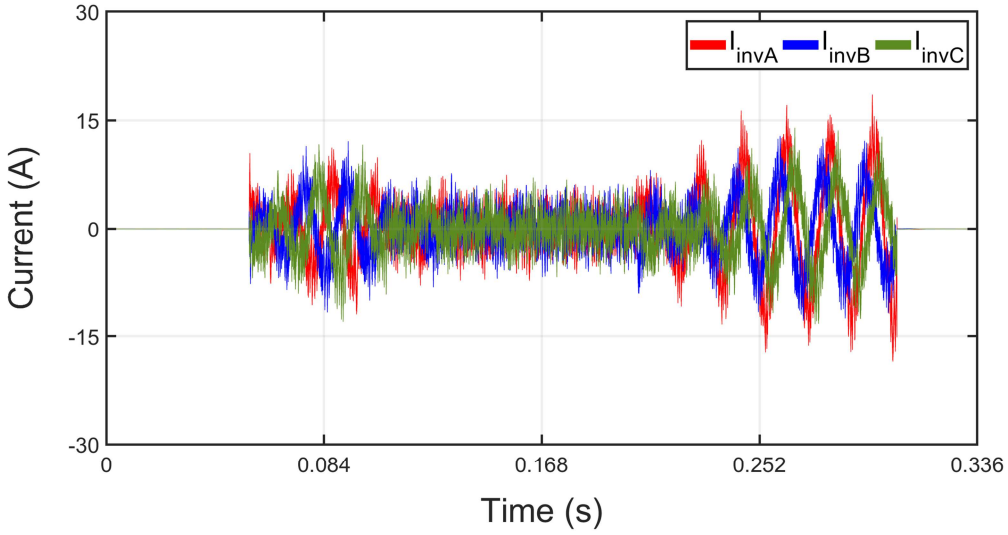
Similar behavior takes place in the substation currents given in Figure 7-12. Starting at approximately t = 0.20 s, the MV-UCSC has fully balanced the substation currents and maintains this until the opening of the breaker at t = 0.30 s. The upstream negative- and zero-sequence current components are reduced from 4.6 A to negligible values during the compensation period (M5). For comparison purposes, simulation results for this operating condition are included. The experimental results match closely what was expected from the simulation results. The experimental converter currents separated by phase is presented in Figure 7-13.

Relative to the 11-level, the THD of each converter current in the 4.16 kV ac grid is much higher. This is partly due to the increase in voltage of each level (0.2 kV vs. 2.5 kV) and partly due to the lower effective frequency (100 kHz at 11-levels vs. 40 kHz at 5-levels) [4].

The positive and negative dc-bus rails are given in Figure 7-14 along with the voltage of one of the Figure 7-15. The voltage ripple is ±115 $V_{pk\text{-}pk}$ or 2.3% which is near the predicted ±110 V. The voltage of the flying capacitor nearest to the dc-bus is at a dc value of approximately 7.75 kV which is close to the expected value of [10.5 kV/(11 – 1)*9 = 7.8 kV]. The voltage ripple is ±250 $V_{pk\text{-}pk}$ or ±3.2 % which is under the designed ripple value of ±5% for



(a)

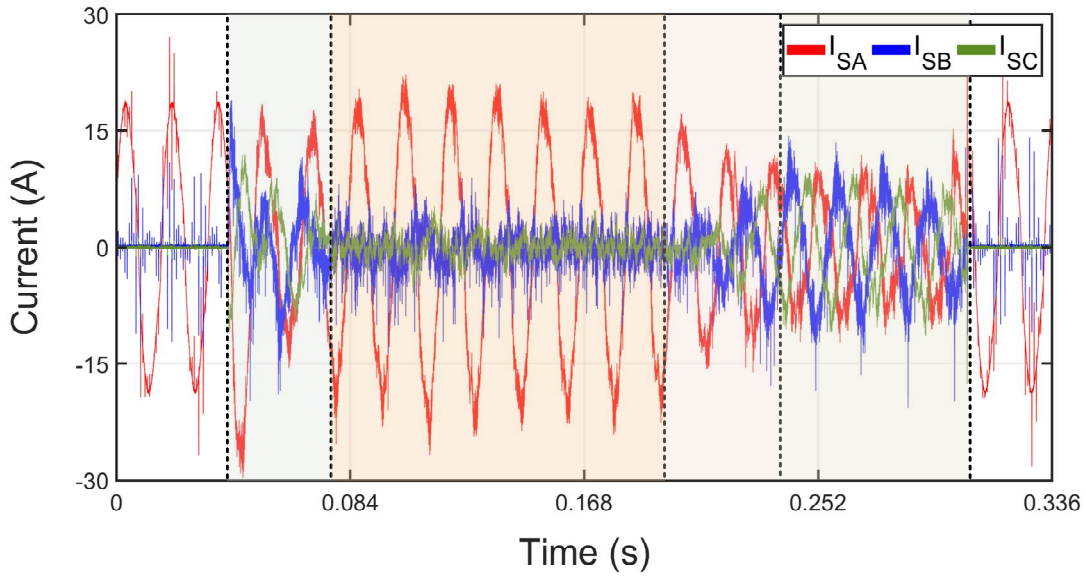


(b)

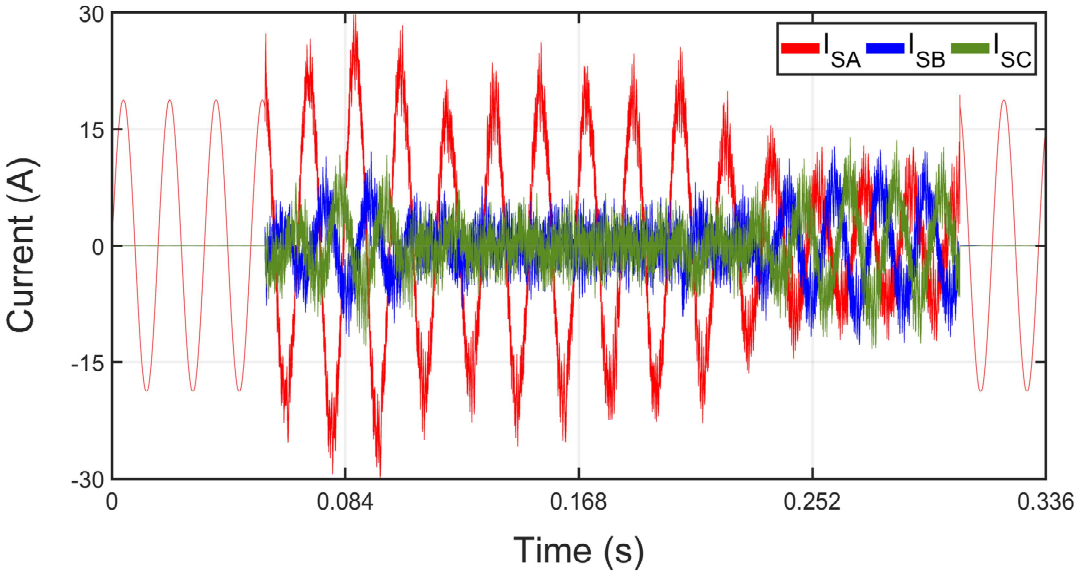
Figure 7-11. MV-UCSC experimental (a) and simulation (b) output currents with the 4.16 kV ac grid.

the MV-UCSC. The dc-bus voltages are effectively controlled by the MV-UCSC and the flying capacitor voltage remains stable as well. Figure 7-16 has the resonant inductor current for one of the switching positions.

Due to measurement limitation at these large common-mode voltages (± 5 kV), the



(a)



(b)

Figure 7-12. Simulation (a) and experimental (b) substation currents with the 4.16 kV ac grid.

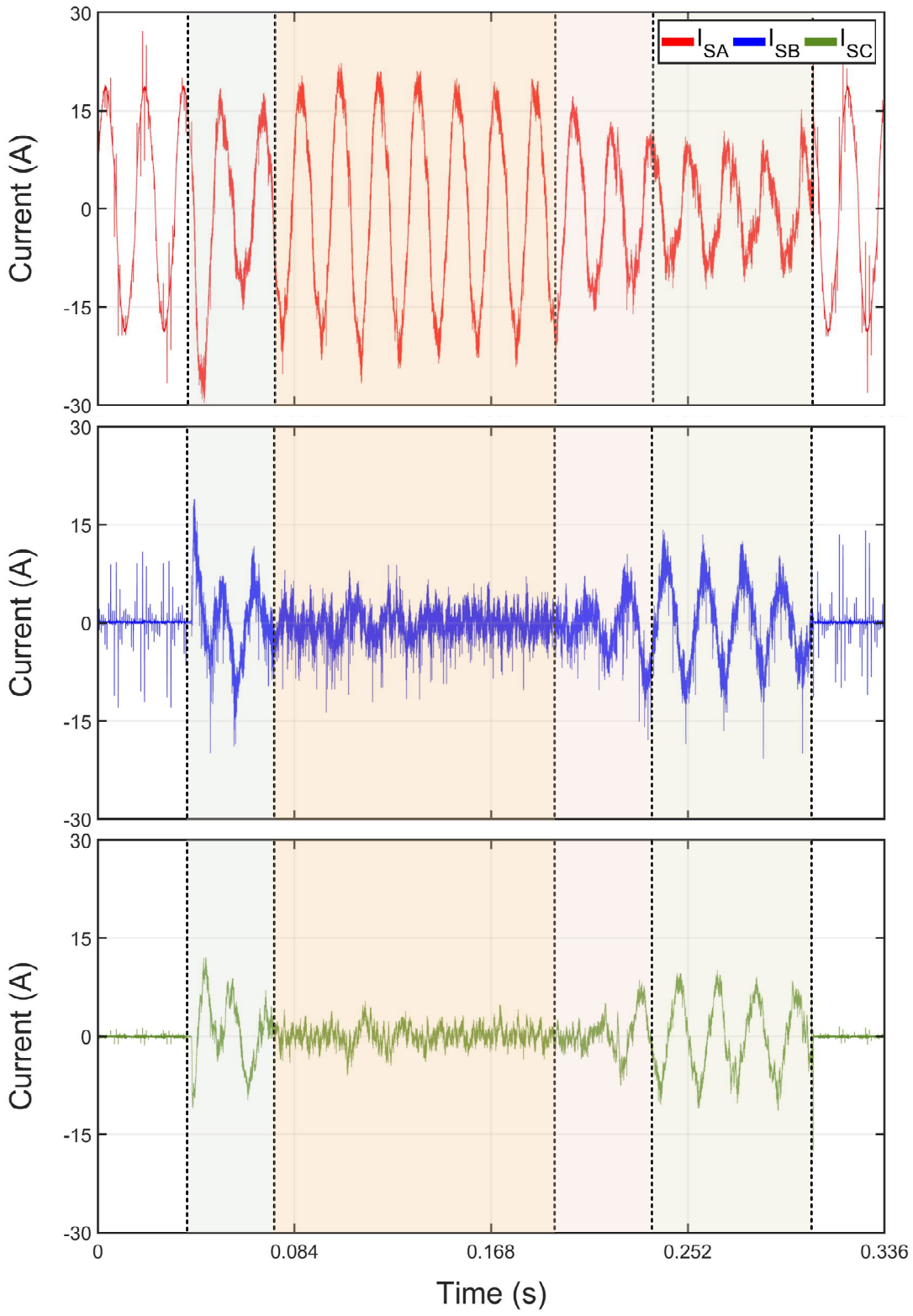


Figure 7-13. Experimental substation currents separated by phase with the 4.16 kV ac grid.

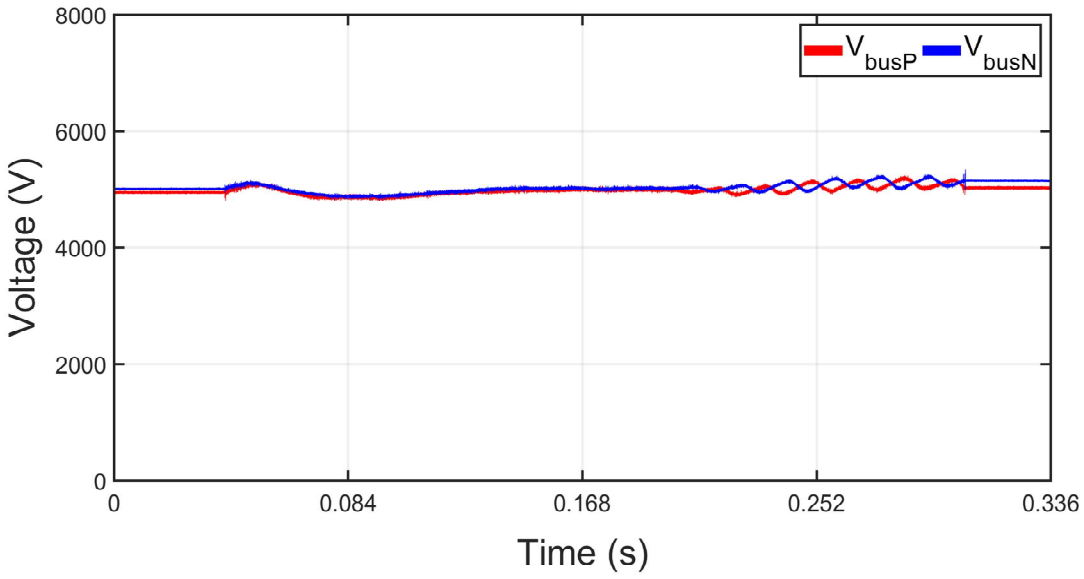


Figure 7-14. MV-UCSC experimental dc-bus capacitance voltages with the 4.16 kV ac grid.

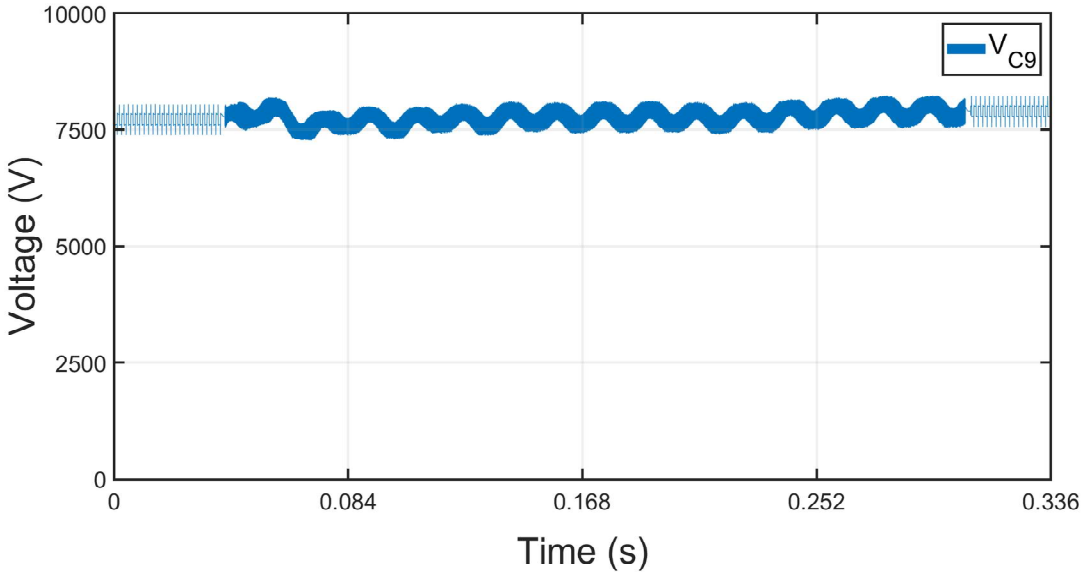


Figure 7-15. MV-UCSC experimental flying capacitor voltage with the 4.16 kV ac grid.

ability to measure $V_{C_{gd}}$ with acceptable efficacy is not possible, so this voltage is not included here as it was with the ± 1 kV grid experimental results above. As with the previous test, the bucking frequency is 0.8 kHz and the main power switching frequency is 10 kHz.

7.5 Performance of the Voltage Balancing Circuit within the 3.3 kV Switching Position

The voltage of the top voltage-balancing capacitor, V_{C_a} from the voltage-balancing circuit within the modular stackable switching positions with the resonant inductor current as context are given in Figure 7-17 [1]. These measurements were not possible at the 1.8 kV ac grid test or the 4.16 kV ac grid test due to the high common-mode voltage, so this measurement was performed with a dc-bus voltage of ±1 kV and an ac grid of 480 V. The voltage-balancing capacitor voltage remains at 100 V. For a 11-level flying capacitor converter with a ±1 kV bus each switching position should have a voltage around ½ of the submodule voltage or [2 kV/(11 – 1)/2 = 100 V] which matches the experimental value from Figure 7-17.

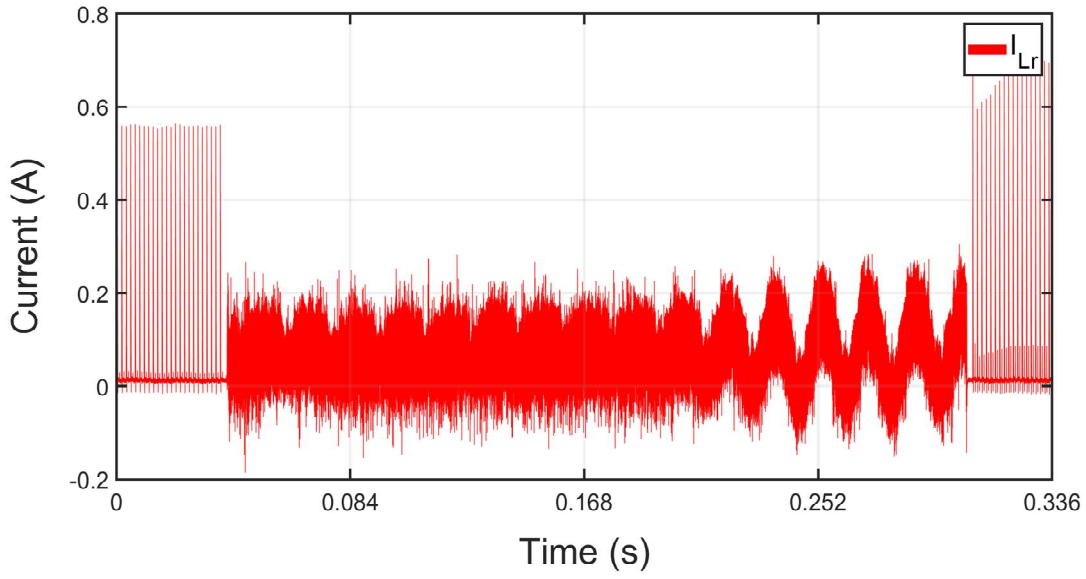


Figure 7-16. Experiment resonant inductor current with the 4.16 kV ac grid.

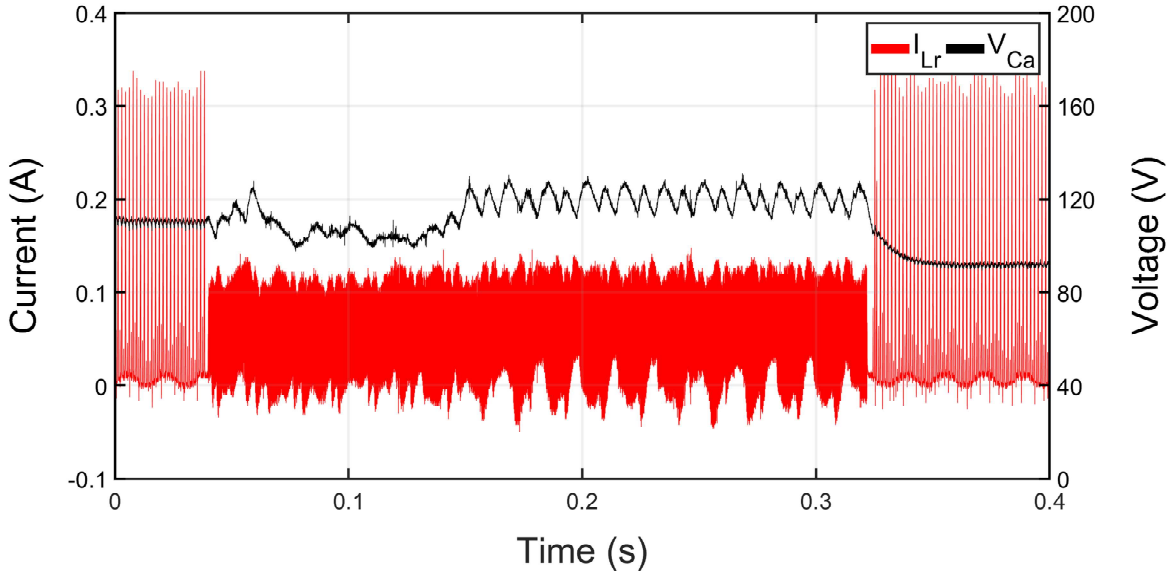


Figure 7-17. Experimental resonant inductor current and voltage-balancing capacitor voltage at a dc-bus voltage ±1 kV.

7.6 References

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CHAPTER 8

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

8.1 Conclusions

This dissertation addressed the issue of unbalanced currents in distribution systems due to load imbalances. It is anticipated that the increasing penetration rates of distributed generation, particularly residential single-phase PV arrays, will exacerbate this issue. To this end, several shunt-connected active and passive compensators were first analyzed eliminating those solutions not capable of compensating for unbalanced currents in distribution systems. The final topology was one connecting directly to medium voltages and based on the NPC arrangement (i.e., a four-wire system). This solution was referred to as the Medium-Voltage Unbalanced Current Static Compensator (MV-UCSC). The system-level functionality of the MV-UCSC when placed in a distribution system was explored along with its effect on the existing regulating equipment at distribution substations [1]. Furthermore, two other functions were added to the MV-UCSC; namely, (a) reactive power injection to optimize the compensation provide by shunt capacitor banks, and (b) harmonic minimization. These functions demonstrate the flexibility of the proposed MV-UCSC.

Subsequent research activities focused to the equipment level from the system level. That is, the design, simulation, and construction of the 13.8 kV eleven-level MV-UCSC prototype based on 3.3 kV modular switching positions were presented. The main issues associated with multilevel converters were identified. Specifically, isolation on the order of 12 kV for the a 13.8 kV distribution system, dv/dt on the order of 100 kV/μs, common-mode voltage as well as creepage distance/clearance requirements. The research work then focused on the switching positions that are used in the MV-UCSC prototype [2].

The 3.3 kV modular stackable switching position consisted of two 1.7 kV SiC MOSFETs connected in series to address the prohibitive cost to the researchers of the 3.3 kV SiC half-bridge power modules. This also provided a potential solution to equipment manufacturers who want to utilize higher-voltage switching positions but cannot accept the supply-chain risk of using higher-voltage SiC semiconductor devices that suffer from low availability and lack of secondary distributors.

The modularity of the switching positions was provided using voltage-balancing and self-powered circuitry. This potentially allows for the arbitrary stacking of "n" number of switching positions in series as well as eliminating voltage isolation problems of the gate-driver power supply.

To accomplish this the following contributions were made [2]:

- Improvements were made to voltage-balancing circuit to make it suitable for half-bridge operation.
- A new quantitative methodology for choosing component values for the voltage-balancing circuit was developed.
- A self-power circuit was reconfigured to allow for self-powering of the switching position at any voltage which provides a soft-starting mechanism.
- Additionally, a novel variant of this 3.3 kV switching position developed as a recombination of the existing circuits was evaluated [3].
- Lastly, medium-voltage test results of the MV-UCSC prototype as a grid-connected current compensator utilizing the 3.3 kV modular stackable switching positions were presented (Chapter 7). To accomplish this the following contributions were made:

In addition, the author had to perform the following:

- A new start-up routine was developed that leverages the soft-start capabilities of the self-powered circuitry to pre-charge the voltage-balancing circuitry and enable half-bridge operation of the modular stackable switching positions.
- Custom ride-through, voltage-regulating, and fault handling functions of the switching positions were created to make them more robust and reliable for use in converter.
- An 11-level three-phase neutral-point-clamped flying capacitor converter was designed, built, and tested with direct connection to a medium-voltage grid. To the author's knowledge, experimental results of a flying capacitor converter at medium-voltage with a high number of levels or grid-connected had not yet been shown in literature.

While working towards the objectives of this dissertation, the following conclusions were drawn:

- The MV-UCSC is capable of negative- and zero-sequence current component compensation as well as reactive power and harmonic current compensation.
- The MV-UCSC has other secondary features as a shunt connected compensator including inter-feeder current sharing from back-to-back connection, STATCOM functionality in the event a feeder is operating as a microgrid, and can also be used in conjunction with energy storage to provide peak-shaving or ride-through capability.
- The MV-UCSC installed at a substation can have a positive effect on the number of operations experienced by voltage regulators and power-factor correction capacitor banks. However, these pieces of equipment might need a coordination study in some configurations to ensure this benefit.

- The developed 3.3 kV modular stackable switching positions can balance the voltage among series connected power semiconductor devices and can provide power for themselves by utilizing the voltage across the switching position in the OFF-state. This eliminates the need for an external power supply and the associated parasitic common-mode currents and isolation requirements.
- A variation of the modular stackable switching position that provides power to itself by utilizing energy that would normally be lost in the voltage-balancing circuitry was also shown to be able to balance the voltage across series connected devices in addition to provide power to itself by utilizing energy that would normally be lost by the voltage-balancing circuitry.
- The use of an 11-level flying capacitor converter utilizing these 3.3 kV modular switching positions for direct connection to medium-voltage distribution feeders is a viable solution for the MV-UCSC. Testing of the MV-UCSC prototype confirmed its ability to compensate for unbalanced load currents and present a balanced load upstream from the point of installation.

8.2 Recommendations for Future Work

There are several future research thrusts that are broached by the work within this dissertation. Many of these lie within the context of the MV-UCSC as a future product. Within this context are reliability, application, and efficiency. Below are several recommendations within each of these categories.

8.2.1 Reliability

- The flying capacitor topology does not have the same obvious redundancies that exist for other multilevel converters like the MMC and the Cascaded Multilevel converter

[4]. The redundancy available to the MMC means a submodule failure can be easily shorted out and maybe even replaced during operation which allows the converter to continue functioning. However, further work is required to find internal fault recovery options for the flying capacitor converter.

- The MV-UCSC installed at a 13.8 kV distribution level must meet the basic insulation level (BIL) of a 95 kV pulse, such as those experienced from lightning strikes [5]. Determining a commercially viable protection scheme for the converter would be of great value.
- The designed modular stackable switching positions were all analyzed based the assumption that no switch fails. Determining how to recover from a failure when considering the use of these switching positions is not obvious [6, 7]. This adds another dimension to any converter fault analysis.
- Due to the high voltages and high dv/dt's in the MV-UCSC, the use of passive cooling and ungrounded heatsinks were employed. For higher power levels passive cooling becomes ineffective. Establishing a forced liquid cooling method like heat pipes that can be used in applications like the MV-UCSC would be very useful.

8.2.2 Applications

- The flying capacitor converter designed in this work is used as a current compensation tool, but as mentioned earlier most voltage-source converters have the potential to be adapted to an energy storage front-end or act as dc sources [8]. Expanding the applicability of the presented solution will contribute towards adoption by manufacturers and utilities.

- The number of capacitor links within the flying capacitor converter immediately lend themselves to dc sources, however, it is not obvious if this is feasible. It is important to maintain balance between the capacitors and voltage isolation may also hinder this type of use.
- The flying capacitor cannot maintain self-balance at lower power factors, and thus there may exist an operating point required of the MV-UCSC that may not be suitable [9]. Determining a solution for operating the flying capacitor converter at lower power factors could expand the operating range of the MV-UCSC.
- The self-powered solution for the switching positions presented in this paper is effective for this application but may not work under other operating conditions. The start-up mechanism needs to be tailored to the topology in which the switching position is installed. Further analysis can be applied to this self-powered circuit to determine the effects of converter switching dead-time and circulating currents on its operation.
- If the self-powering solution is to be used with other modulation strategies aside from the phase-shifted pulse-width modulation (PSPWM) used in this work, the effect on the self-powered circuitry needs to be evaluated [9].

8.2.3 Efficiency

- Most multilevel converter structures are hard-switched topologies. The use of SiC devices can reduce the switching energy, but converter energy efficiency is still relatively low compared to soft-switched topologies. The auxiliary resonant commutated pole (ARCP) variation on the flying capacitor converter provide the ability to soft-switch the flying capacitor converter but requires the use of high-

voltage semiconductors [7]. The development of new soft-switching variations of multilevel converters would be of high value.

- Efficiency of converter volume is a concern. Some applications may be lost if the converter topology requires too large of a volume. The flying capacitor converter has the advantage that its required energy storage reduces with the switching frequency which can allow for significant reductions in size. Though, it is more difficult to take advantage of this volume reduction due to the lack of true modularity of the flying capacitor cells. A more modular design of the flying capacitor converter could enhance its application.
- Volume reductions can also be accomplished at the switching position level by taking advantage of the elimination of the gate driver power supply enabled by the self-powered circuitry within the modular stackable switching position. With its relatively low power requirements, the self-powered circuitry could be combined within a power module with the power semiconductor or consolidated within a single integrated circuit.
- At the switching position level, the self-powering mechanism may be improved. Though the stored energy is resonated at turn-ON of the switch, efficiency of the self-powered circuit is capped at 50% due to the non-resonant charging of the self-powered circuit at turn-OFF. This can be disregarded when small amounts of power are required but can cause PCB- and system-level thermal management problems if a larger amount of power is required.

8.3 References

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APPENDICES

APPENDIX A

TESTING SETUP FOR THE MV-UCSC PROTOTYPE

A.1 Introduction

The MV-UCSC was tested at the National Center for Reliable Electric Power Transmission (NCREPT) because of its medium-voltage capabilities. This Appendix goes over the setup used at this facility to test the MV-UCSC.

A.2 Test Setup

There are three major setups used depending on the ac grid voltage levels used in the tests. These are 1) 208 V_{ac} & 480 V_{ac}, 2) 1.8 kV_{ac} & 6 kV_{ac}, and 3) 4.16 V_{ac} & 13.8 V_{ac}.

A.2.1 208 V & 480 V AC Grids

The test setup for ac grid voltages below 480 V is shown in Figure A-1. The pre-charge for the dc bus is performed using a 208 V variac that is attached through an external filter reactor to the terminals of circuit breaker (CB) F18. This CB is closed provides continuity to T6 which supplies a three-phase voltage to a diode-bridge rectifier. This allows the dc bus to be ramped from 0 V to the required nominal bus voltage.

The grid is formed either directly by a 208 V or 480 V source, or through a 0-560 V variac. This grid is connected to the MV-UCSC cabinet from the terminals at the back of CB MV13. This current is then routed back to the same CB cabinet to the terminal of T4. The MV-

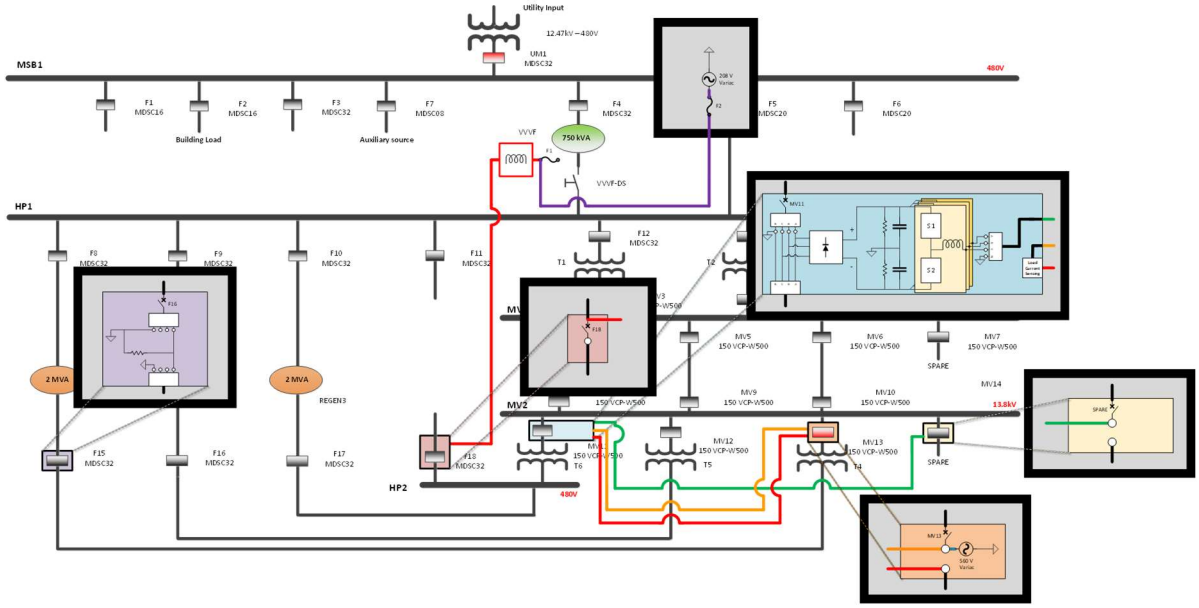

Figure A-1. Test setup for ≤ 480 V ac grid.

UCSC uses this to sense the load current flowing through T4 to the 750 kW load bank that is installed at the terminals of CB F15. The output of the MV-UCSC are routed to CB MV14 (spare). This CB is controlled directly by the MV-UCSC controller to connect to the grid.

A.2.2 1.8 kV & 6 kV AC Grids

These connections are demonstrated in Figure A-2. A grid is formed in this configuration by first routing the 480 V from the bus HP1 through an external 225 kVA 480Δ/208Y V transformer to produce 208 V. This 208 V is routed to CB F16 that is then closed to connect to CB MV13 through T5. With T5 at the 480Δ/4160Y V tap, an ac grid voltage of 1.8 kV is produced at the CB MV2 bus when CB MV13 is closed. Using the 480Δ/13800Y V tap for T5 results in an ac grid of 6 kV. The converter connection remains the same as in Section A.2.1. However, the dc bus pre-charge variac must be changed to a 0 – 560 V variac.

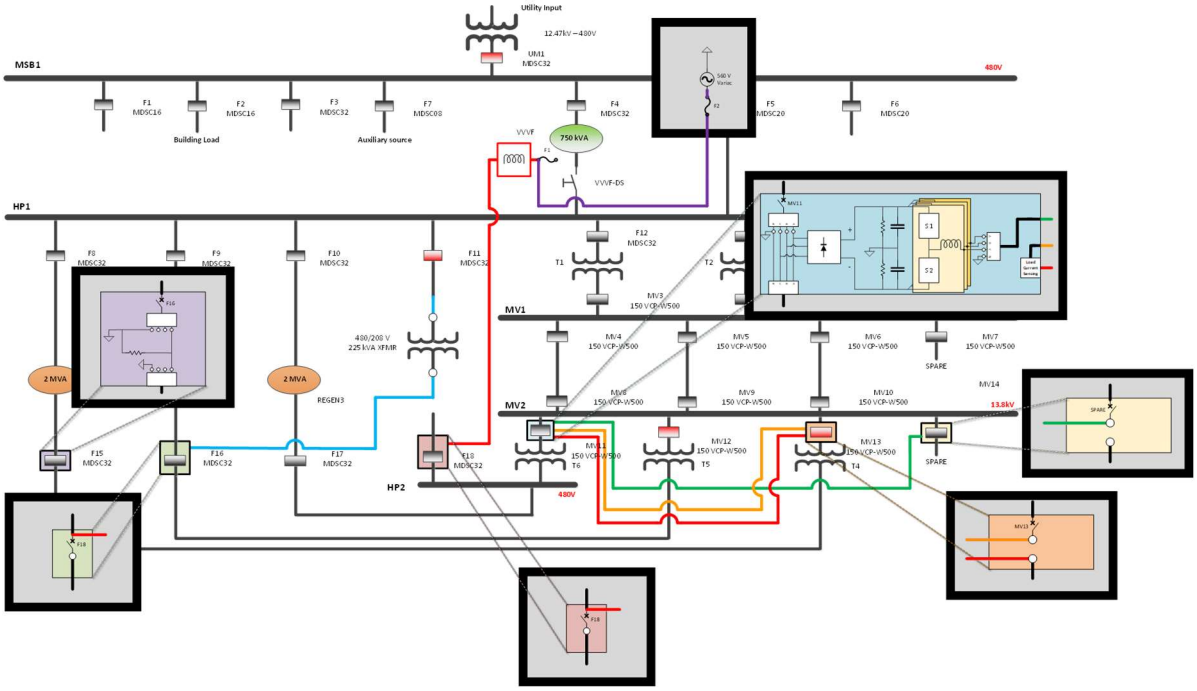

Figure A-2. Test setup for 1800 V & 6000 V ac grid.

A.2.1 4.16 kV & 13.8 kV AC Grids

The grid here is derived directly from the available mains at NCREPT as shown in Figure A-3. CBs F5, F12, MV3, MV8 and MV13 are closed. To form the 4.16 kV and 13.8 kV at the CB MV2 bus the taps for the transformers can be changed accordingly. The converter connection remains the same as in Section A.2.1. Again, the dc bus pre-charge variac must be changed to a 0 – 560 V variac.

A.3 Communication and Control

Mode control of the converter is accomplished through isolated RS-232 communication protocols. Figure A-4 shows the serial interface that is used to communicate with the DSP on the control board. This communication is performed over fiber optic USB to isolate the laptop from the system. The baud rate expected by the DSP is 9600. An externally powered USB hub provides additional power for the converter-side fiberoptic receiver.

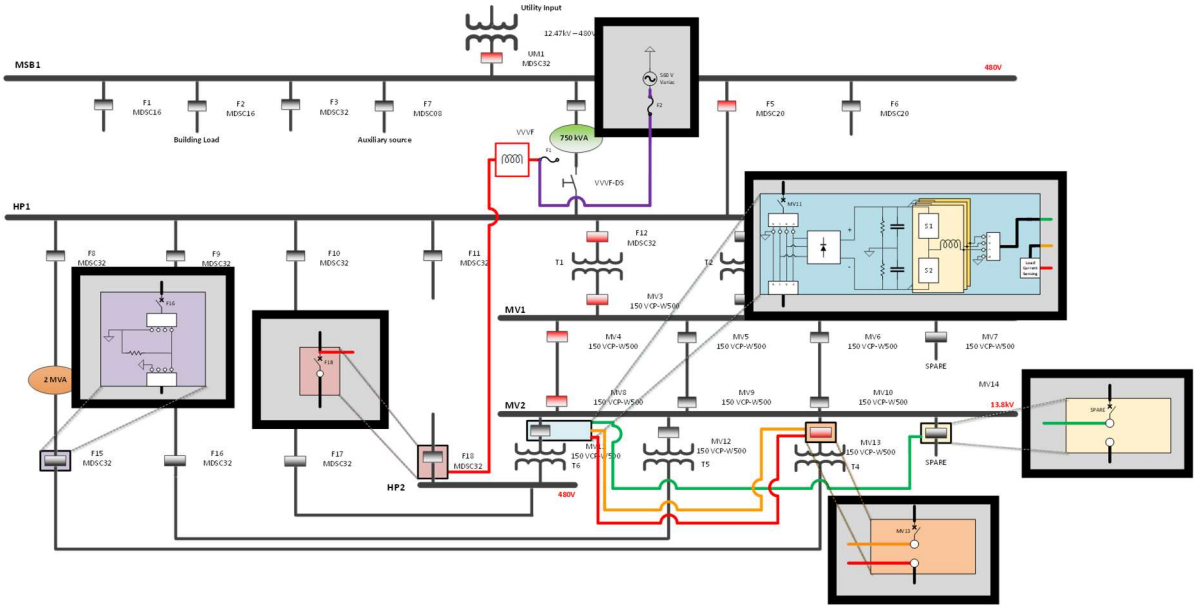

Figure A-3. Test setup for 4160 V & 13800 V ac grid.

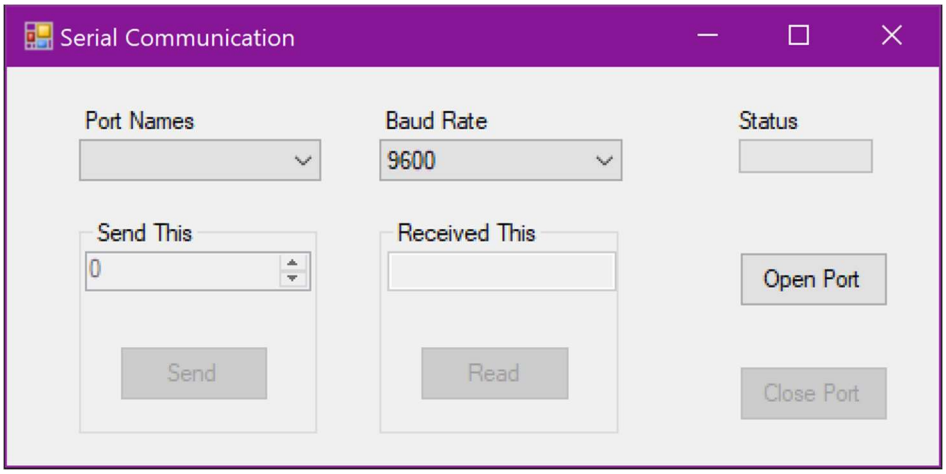

Figure A-4. Serial Interface from laptop to the DSP.

A.4 Test Procedure

Testing of the MV-UCSC consists of three parts: start-up procedure, steady-state operation, and shutdown procedure.

A.4.1 DSP Modes of Operation

The use of 5 different operating modes are used to encompass these three separate parts; that is:

- Mode 1 – None of the PWM are enabled. This is essentially a faulted mode where the converter has been shut-off completely to prevent further damage or faults.
- Mode 2 – The auxiliary/bucking PWM signals are enabled to power the switching position at low voltage as the dc bus is ramped.
- Mode 3 – This is a transitional mode. This disables the auxiliary/bucking PWM signals and enables the main PWM signals in accordance with the timing required by the CB behavior. At the end of this mode the converter is grid connected.
- Mode 4 – This mode switches from the currents predicted by the virtual filter plant to the actual measured currents. The dc bus is then maintained by regular converter operation. No compensation is performed.
- Mode 5 – This mode modifies the current references for the converter phases to compensate for the substation current imbalances as well as the reactive current. This reference can be further modified to compensate for harmonics or to provide real power if energy storage was available within the MV-UCSC.

A.4.2 Start-up Procedure

Upon turn-on of the control module the converter begins acquiring the necessary signals and ADC measurements while priming the FLL/PLL and PR controllers using the virtual filter plant. CB MV14 (spare) remains open and the DSP continuously sends an active-high open signal to the CB. With the open-loop control of the start-up bucking action within the self-power circuit enabled (Mode 2), the variac and diode bridge are used to ramp the dc bus from 0 V to the

required nominal voltage. Once at the nominal voltage, the converter is remains in the start-up/bucking mode for 90 seconds to charge the ride-through supercapacitors aboard each of the switching positions.

A.4.3 Steady-State Operation

Once ready to connect to the grid a value of 3 (unsigned integer) is sent to the DSP to change the operating mode to Mode 3. The DSP then automatically enter Mode 4 once the CB MV14 has successfully closed. The converter remains in Mode 4 for the preprogrammed amount of time. With the dc-bus voltage controlled and the converter successfully maintaining connection to the grid the DSP then automatically enters Mode 5 for a preprogrammed amount of time. Infinite operation in Mode 5 can also be chosen by a simple switch variable that bypasses the Mode 5 timeout.

A.4.4 Shutdown Procedure

If any of the switching positions send a fault signal or an overvoltage, undervoltage, or overcurrent condition occurs then the converter will enter Mode 1 and the signal to open CB MV14 (spare) is sent and then the converter dc bus voltage can be quickly reduce with a high-voltage contactor and energy resistors. Otherwise, at the end of Mode 5 the converter will then revert back to Mode 2 and the dc-bus voltage will naturally decay as the switching positions dissipate the energy stored within the dc-bus and flying capacitors.

A.5 Referenced Equipment

Photos of the equipment setup are shown below. The 0-560 V variac is in Figure A-5. The connections made within the CB MV13 cabinet are shown in Figure A-6. The connections within the CB MV14 (spare) cabinet are in Figure A-7. Figure A-8 illustrates are the connections

within the CB MV11 cabinet. The CB F15 cabinet and its connections are in Figure A-9. The connections within the CB F18 cabinet are shown in Figure A-10. The Variable-Voltage Variable-Frequency Drive (3VF) cabinet where the variac connection are made is in Figure A-11. The connections within the CB F16 Cabinet are shown in Figure A-12.

Figure A-5. 0-560 V variac.

Figure A-6. CB MV13 cabinet.

Figure A-7. CB MV14 cabinet.

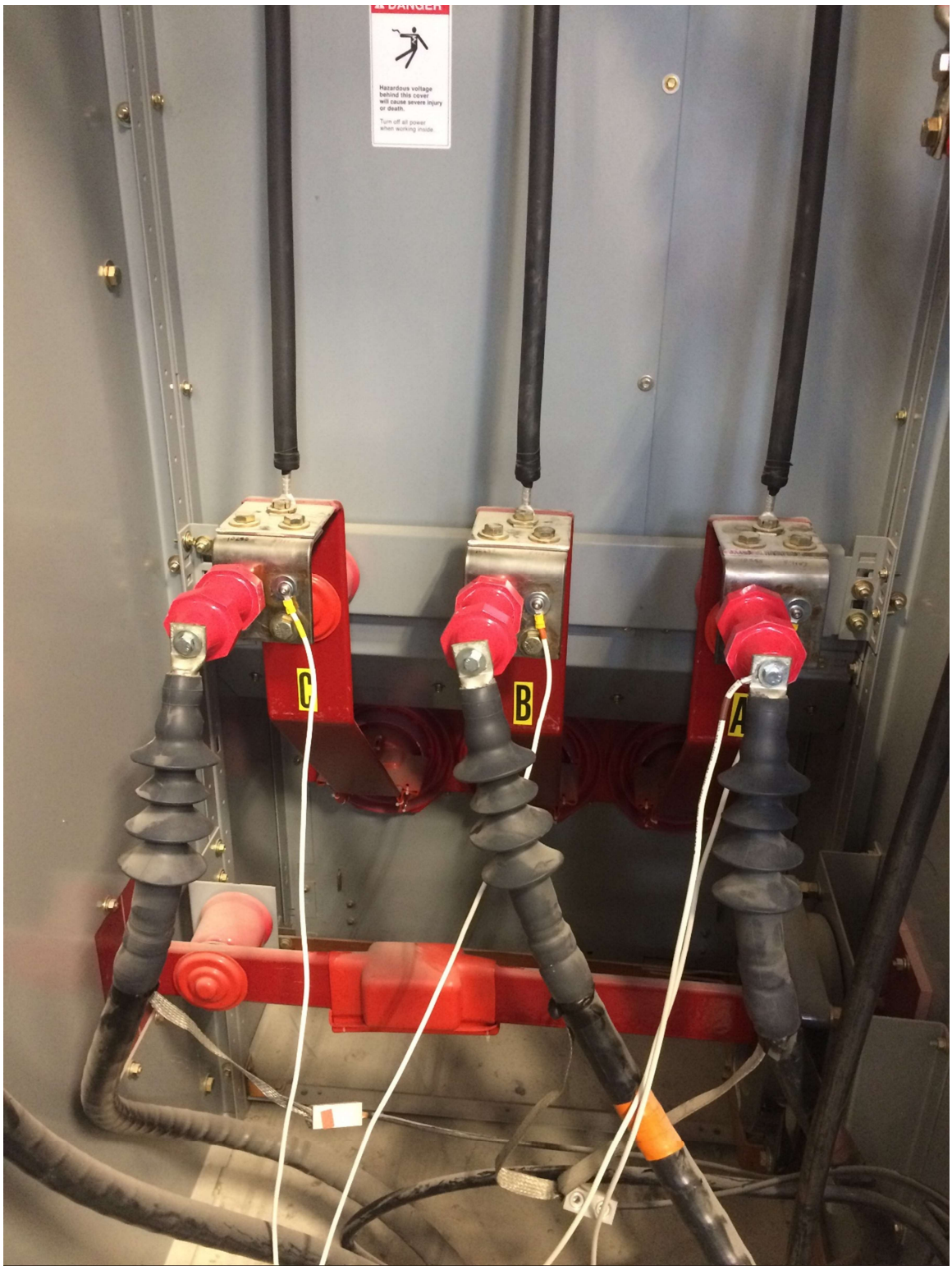

Figure A-8. CB MV11 cabinet.

Figure A-9. CB F15 cabinet.

Figure A-10. CB F18 cabinet.

Figure A-11. The 3VF cabinet.

Figure A-12. CB F16 Cabinet.

A.6 Instrumentation Used for MV-UCSC Testing

The instrumentation used for this dissertation is presented in Table A-1. The table presents the type of probe, the manufacturer, the relevant ratings, and the purpose of its use.

Table A-1. Instrumentation used for this dissertation

Type	Manufacturer	Rating	Purpose
THDP0100[1]	Tektronix	6 kV differential, 2.3 kV common	Flying capacitors voltages, self-power gate driver capacitor voltages
A622[2]	Tektronix	70 A	Grid and MV-UCSC Currents
TCPA300[3]	Tektronix	n/a	Current Sensing Amplifier
TPA-BNC[3]	Tektronix	n/a	Adaptor for probes
P6015A[1]	Tektronix	20 kV	Use 2 to differentially measure high common-mode voltage signals
TCP312A[2]	Tektronix	30 A	Self-Power Resonant Inductor currents
P5200[1]	Tektronix	1.3 kV differential, 1 kV common	PLC signal voltages
TPP0850[1]	Tektronix	1000 V_{rms}, 2.5 V_{pk}	Drain-to-source voltages
PP-150[1]	Hantek	600 V	DC-bus capacitor voltages, Embedded system signals

[1]Voltage Probe
[2]Current Probe
[3]Probe Utility

APPENDIX B

EMBEDDED SYSTEM CODE

B.1 Introduction

The use of a digital signal processor (DSP) and two field programmable gate arrays (FPGA) was required for control of the MV-UCSC. Below is an overview of the code that was used to control the prototype. C-code was used for the DSP programming and VHDL was used for the FPGA programming.

B.2 The Digital Signal Processor (DSP)

B.2.1 Interrupt service routines

Within the interrupt service routine (ISR) responsible for the primary control of the converter is the below code. This interrupt in the DSP is triggered externally by the PWM modules on the FPGA. First, all of the signals measured by the analog to digital converter read into the ADC structure.

```
261 // ADC Ports for UCSC Cabinet 1.00955
262 ADC.Iainv = CurrentMax*((float)(AdcbResultRegs.ADCRESULT4) - 2038.0f)/2048.0f;
263 ADC.Ibinv = CurrentMax*((float)(AdcbResultRegs.ADCRESULT2) - 2044.0f)/2048.0f;
264 ADC.Icinv = CurrentMax*((float)(AdcbResultRegs.ADCRESULT3) - 2045.0f)/2048.0f;
265 ADC.IaL = CurrentMax*((float)AdccResultRegs.ADCRESULT3 - 2044.0f)/2048.0f;
266 ADC.IbL = CurrentMax*((float)AdccResultRegs.ADCRESULT2 - 2042.0f)/2048.0f;
267 ADC.IcL = CurrentMax*((float)AdcaResultRegs.ADCRESULT5 - 2045.0f)/2048.0f;
268 ADC.Va = ((float)(AdcdResultRegs.ADCRESULT1) - 2050.0f)/2048.0f;
269 ADC.Vb = ((float)(AdcdResultRegs.ADCRESULT0) - 2043.0f)/2048.0f;
270 ADC.Vc = ((float)(AdcbResultRegs.ADCRESULT5) - 2049.0f)/2048.0f;
271 ADC.VbusP = BusVoltageMax*((float)(AdcbResultRegs.ADCRESULT0))/4096.0f;
272 ADC.VbusN = BusVoltageMax*((float)(AdcbResultRegs.ADCRESULT1))/4096.0f;
273 ADC.Vbus = ADC.VbusP + ADC.VbusN;
```

Figure B-1. Reading the ADC data.

```
275 Filt_Va.x[0] = ADC.Va;
276 Inv_SPTF_FUNC(&Filt_Va);
277 Filt_Vb.x[0] = ADC.Vb;
278 Inv_SPTF_FUNC(&Filt_Vb);
279 Filt_Vc.x[0] = ADC.Vc;
280 Inv_SPTF_FUNC(&Filt_Vc);
281 Filt_Vbus.x[0] = ADC.Vbus;
282 Inv_SPTF_FUNC(&Filt_Vbus);
283 Filt_IaL.x[0] = ADC.IaL;
284 Inv_SPTF_FUNC(&Filt_IaL);
285 Filt_IbL.x[0] = ADC.IbL;
286 Inv_SPTF_FUNC(&Filt_IbL);
287 Filt_IcL.x[0] = ADC.IcL;
288 Inv_SPTF_FUNC(&Filt_IcL);
289 Filt_IaINV.x[0] = ADC.Iainv;
290 Inv_SPTF_FUNC(&Filt_IaINV);
291 Filt_IbINV.x[0] = ADC.Ibinv;
292 Inv_SPTF_FUNC(&Filt_IbINV);
293 Filt_IcINV.x[0] = ADC.Icinv;
294 Inv_SPTF_FUNC(&Filt_IcINV);
```

Figure B-2. Inverse function calls to remove phase delays.

```
296 PP_receive();
```

Figure B-3. Parallel port function call.

Inverse functions are used to remove the phase delays from external filtering on the DSP's ADC signals. Any signals needed from the FPGA are received using a custom parallel port function.

The phase-lock-loop algorithm is run using the three phases voltages. Grid-frequency based variables used for tuning the controller are generated.

A sine-wave analyzer function from Texas Instruments' (TI's) solar application library was used to calculate the RMS of the grid voltage.

```
298 //---------------------- PLL -------------------------//
299
300 SOGI_PLL_FUNC(&VgPLL, Filt_Va.y[0], Filt_Vb.y[0], Filt_Vc.y[0]);
301 temp = VgPLL.w[0]/MEASUREFREQ;
302 K_wTs = 2*cosf(temp);
303 K_2wTs = 2*cosf(2*temp);
304 K_wTsSIN = sinf(temp)/(2*VgPLL.w[0]);
```

Figure B-4. Phase-Lock Loop function call.

```
306 //--------- Sine-Wave Analyzer (Used for RMS) ----------//
307
308 sineanalyzer_diff1.Vin = VgPLL.Va*GridVoltageMax;
309 SINEANALYZER_DIFF_F_FUNC(&sineanalyzer_diff1);
310 if(sineanalyzer_diff1.Vrms < 5.0){sineanalyzer_diff1.Vrms = 5.0;}
```

Figure B-5. Sine-wave RMS function call.

```
312 //--------- The normalized pos. seq. voltages ----------//
313
314 temp = 0.91743*sqrtf((VgPLL.Va*VgPLL.Va + VgPLL.Vb*VgPLL.Vb + VgPLL.Vc*VgPLL.Vc)/1.5);
315 if(temp > 2.0){temp = 2.0;} // saturation block
316 if(temp < 0.001){temp = 0.001;} // avoid dividing by zero
317 Filter1_FUNC(&FIL1_w_NORM, K_wTs, K_2wTs, temp, &Vpos_norm_den);
318 Vpos_norm_a= VgPLL.Va/Vpos_norm_den;
319 Vpos_norm_b= VgPLL.Vb/Vpos_norm_den;
320 Vpos_norm_c= VgPLL.Vc/Vpos_norm_den;
```

Figure B-6. Normalized voltage vector generation.

The normalized positive sequence phase voltage vectors are created from the voltage measurements.

Filtering of the bus voltages and load power is performed for better performance by the proportional-integrator (PI) controllers and the proportional-resonant (PR) controllers.

The virtual plant is run continuously to prime the PI and PR controllers for grid-connection when needed.

```
322 //-------------------- Filtering ----------------------//
323
324 Filter1_FUNC(&FIL1_w_Bus, K_wTs, K_2wTs, Filt_Vbus.y[0], &temp);
325 filtereddcbus = temp;
326
327 PI_Vbus.term.Ref = dcbusval;
328 PI_Vbus.term.Fbk = filtereddcbus;
329
330 Filter1_FUNC(&FIL1_w_VbusN, K_wTs, K_2wTs, ADC.VbusN, &temp);
331 PI_Vbus_NP.term.Ref = filtereddcbus*0.5;
332 PI_Vbus_NP.term.Fbk = temp;
333
334 temp = Vpos_norm_a*Filt_IaL.y[0] + Vpos_norm_b*Filt_IbL.y[0] + Vpos_norm_c*Filt_IcL.y[0];
335 Filter1_FUNC(&FIL1_w_Power, K_wTs, K_2wTs, temp, &LoadPower);
```

Figure B-7. Dc-bus measurement filtering.

```
337 //---------------- Run plant for idle mode -------------//
338
339 Lfil_plant_a.x = (COMP1.ya + Filt_Va.y[0]*GridVoltageMax);
340 singlepole_TF_FUNC(&Lfil_plant_a);
341 Lfil_plant_b.x = (COMP1.yb + Filt_Vb.y[0]*GridVoltageMax);
342 singlepole_TF_FUNC(&Lfil_plant_b);
343 Lfil_plant_c.x = (COMP1.yc + Filt_Vc.y[0]*GridVoltageMax);
344 singlepole_TF_FUNC(&Lfil_plant_c);
```

Figure B-8. Virtual plant function call.

```
362 if(filtereddcbus > 25000.0)
363 { // Check if there is an overvoltage on the dc bus
364 State_Ptr = &M1;
365 overvoltage_flag = 1;
366 deletethis = PI_Vbus.term.Out*((Filt_Vbus.y[0]/2.0)/3.0/sineanalyzer_diff1.Vrms);
367 }
368 if ( (ADC.Iainv > 20.0) || (ADC.Iainv < -20.0) || (ADC.Ibinv > 20.0) ||
369 (ADC.Ibinv < -20.0) || (ADC.Icinv > 20.0) || (ADC.Icinv < -20.0) ) {
370 State_Ptr = &M1;
371 overcurrent_flag = 1;
372 deletethis = PI_Vbus.term.Out*((Filt_Vbus.y[0]/2.0)/3.0/sineanalyzer_diff1.Vrms);
373 }
```

Figure B-9. Overvoltage and overcurrent tripping.

The overvoltage and overcurrent trips force the controller into Mode 1 (M1) when the either of these conditions occur.

The relevant Mode function is then run. Then data required by the FPGA is loaded into the appropriate registers. The parallel port transmit function is then called and the data is sent to the FPGA. The number of values that can be sent depends on the clock speed of the communicating devices and the ISR period. Lastly, ISR maintenance is performed, clearing the ADC interrupt flag and the peripheral interrupt flag.

```
375 (*State_Ptr)(); // perform the selected MODE function
```

Figure B-10. Mode function pointer call.

```
387 Reg[0] = (unsigned int)((float)(PWMaux_TIMER_TBPRD*PWM.CMP_AUX));
388 Reg[1] = (unsigned int)(PWM_TIMER_TBPRD*PWM.CMP_A1);
389 Reg[2] = (unsigned int)(PWM_TIMER_TBPRD*PWM.CMP_B1);
390 Reg[3] = (unsigned int)(PWM_TIMER_TBPRD*PWM.CMP_C1);
391 Reg[4] = (unsigned int)(PWMaux_TIMER_TBPRD);
```

Figure B-11. Register loading.

```
410 PP_transmit();
411
412 AdcaRegs.ADCINTFLGCLR.bit.ADCINT1 = 1; //clear INT1 flag
413 PieCtrlRegs.PIEACK.all = PIEACK_GROUP1;
```

Figure B-12. Phase-Lock Loop function call.

Changing the modes is performed through a separate ISR that is triggered by the SCI port on the DSP. When a mode change communication is received by the DSP this ISR is triggered and the function pointer that changes the mode of operation is reassigned based on the desired mode.

```
417 interrupt void SCIA_isr()
418 {
419
420 command = SciaRegs.SCIRXBUF.all; // Read data
421
422 if (command == 1)
423 {
424 breakercount = 0;
425 State_Ptr = &M1;
426 }
427
428 if (command == 2)
429 {
430 breakercount = 0;
431 State_Ptr = &M2;
432 }
433
434 if (command == 3)
435 {
436 GpioDataRegs.GPBSET.bit.GPIO40 = 1; // send signal to close the breaker.
437 State_Ptr = &M3;
438 }
439
440 if (command == 4)
441 {
442 State_Ptr = &M5;
443 }
444
445 SciaRegs.SCIFFRX.bit.RXFFOVRCLR=1; // Clear Overflow flag
446 SciaRegs.SCIFFRX.bit.RXFFINTCLR=1; // Clear Interrupt flag
447
448 PieCtrlRegs.PIEACK.all|=0x100; // Issue PIE ack
449
450 }
```

Figure B-13. SCI Port ISR code.

B.2.2 The Mode Functions

These functions run the code associated with the various modes as described in Appendix A.

Mode 1:

- Disable the Main PWMs
- Disable the Auxiliary PWMs
- Open the gird-tie breaker
- Set the converter current references to 0 A.
- Load the current controller PR controller error
- Run the current controller based on the virtual plant
- Set the Auxiliary PWMs to an OFF value (slightly redundant)

```
 86 void M1(void)
 87 {
 96 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
 97 GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;
 98 GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1; // send signal to open the breakers.
 99
100
101 // Set the reference to zero for the virtual plant control
102 Iref_a = 0.0;
103 Iref_b = 0.0;
104 Iref_c = 0.0;
105
106
107 cc_err_a = Iref_a - Lfil_plant_a.y[0];
108 cc_err_b = Iref_b - Lfil_plant_b.y[0];
109 cc_err_c = Iref_c - Lfil_plant_c.y[0];
110
111 CurrentControl();
112
113 // SET the PWMs to OFF (Active-Low)
114 PWM.CMP_AUX = 1.0;
115
116
117
118 }
```

Figure B-14. Mode 1 code.

Mode 2:

- Disable the Main PWMs
- Open the grid-tie breaker
- Set the converter current references to 0 A.
- Load the current controller PR controller error
- Run the current controller based on the virtual plant
- Run the Look-Up Table (LUT) function to determine the Auxiliary PWM duty cycles based on the voltage of the dc bus. Limit the outputs of this function to avoid useless duty cycle values.

```
120 void M2(void)
121 {
122
...
129 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
130 GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1; // send signal to open the breakers.
131
132 // Set the reference to zero for the virtual plant control
133 Iref_a = 0.0;
134 Iref_b = 0.0;
135 Iref_c = 0.0;
136
137
138 cc_err_a = Iref_a - Lfil_plant_a.y[0];
139 cc_err_b = Iref_b - Lfil_plant_b.y[0];
140 cc_err_c = Iref_c - Lfil_plant_c.y[0];
141
142 CurrentControl();
143
144 // Set the Aux PWM duty cycle
145
146 aux_duty_cycle_LUTcurve();
147
148 if (PWM.CMP_AUX > 1.0){PWM.CMP_AUX = 1.0;} // bounds protection
149 if (PWM.CMP_AUX < 0.0){PWM.CMP_AUX = 0.0;}
150
151 // Turn on the aux PWM
152 GpioDataRegs.GPASET.bit.GPIO11 = 1; // CBC TRIP 2 output to FPGA
153
154 }
```

Figure B-15. Mode 2 code.

- Enable the Auxiliary PWMs

Mode 3:

Upon transitioning to Mode 3, the signal to close the grid-tie breaker is sent.

- Check the grid-connect time to determine if the breaker should be opened.
- Set the converter current references to 0 A.
- Load the current controller PR controller error
- Run the current controller based on the virtual plant
- Once the DSP senses that the "Breaker Open" signal goes low the DSP performs a timing procedure to compensate for delay between breaker signals and physical operation.
- Run the Look-Up Table (LUT) function to determine the Auxiliary PWM duty cycles

```
156 void M3(void)
157 {
158
...
169 if (GpioDataRegs.GPBDAT.bit.GPIO40 && (breakercount2 < (unsigned long)
    (grid_connect_time*MEASUREFREQ)))
170 {
171 breakercount2++;
172 }
173 else
174 {
175 GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1;
176 breakercount2 = 0;
177 }
178
179
180 // Set the reference to zero for the virtual plant control
181 Iref_a = 0.0;
182 Iref_b = 0.0;
183 Iref_c = 0.0;
184
185
186 cc_err_a = Iref_a - Lfil_plant_a.y[0];
187 cc_err_b = Iref_b - Lfil_plant_b.y[0];
188 cc_err_c = Iref_c - Lfil_plant_c.y[0];
```

Figure B-16. Mode 3 code.

```
189
190 CurrentControl();
191
192 if (GpioDataRegs.GPBDAT.bit.GPIO52)
193 {
194 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
195
196 aux_duty_cycle_LUTcurve();
197 if (PWM.CMP_AUX > 1.0){PWM.CMP_AUX = 1.0;} // bounds protection
198 if (PWM.CMP_AUX < 0.0){PWM.CMP_AUX = 0.0;}
199
200 }
201 else
202 {
203 if (breakercount < (unsigned long)(0.0028*MEASUREFREQ))
204 {
205 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
206
207 aux_duty_cycle_LUTcurve();
208 if (PWM.CMP_AUX > 1.0){PWM.CMP_AUX = 1.0;} // bounds protection
209 if (PWM.CMP_AUX < 0.0){PWM.CMP_AUX = 0.0;}
210
211 breakercount++;
212 }
213 else
214 {
215 if (breakercount < (unsigned long)(0.0038*MEASUREFREQ))
216 {
217 // Turn off the main PWM
218 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
219 // Turn off the aux PWM
220 GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;
221
222
223 breakercount++;
224 }
225 else
226 {
227 // Turn on the main PWM
228 GpioDataRegs.GPASET.bit.GPIO8 = 1; // CBC TRIP 1 output to FPGA
229
230 dcbusval = Filt_Vbus.y[0];
231 State_Ptr = &M4;
232 breakercount = 0; // reset breakercount counter variable.
233 }
234 }
235 } // after the time delays, allow the MAIN PWM to change.
236
237 }
```

Figure B-16. Mode 3 code (Continued).

Mode 4:

- Check the grid-connect time to determine if the breaker should be opened.
- Begin to ramp the dc bus reference if necessary.

- Enable the bus voltage controllers
- Load the current controller PR controller error
- Run the current controller based on the measured output current
- After set time transition to Mode 5 or go back to Mode 2.

```
239 void M4(void)
240 {
241
...
250 if (GpioDataRegs.GPBDAT.bit.GPIO40 && (breakercount2 < (unsigned long)
    (grid_connect_time*MEASUREFREQ)))
251 {
252 breakercount2++;
253 }
254 else
255 {
256 GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1;
257 breakercount2 = 0;
258 }
259
260
261 if(dcbusval < dcbusref) // ramp the dc-bus reference to a higher value
262 {
263 dcbusval += 0.15; // 1 V/cycle = (0.005 ms ramp time)/(0.0001 s/cycle)
264 }
265
266 // Set the reference to maintain the dc bus voltage
267 // PI_cont_FUNC(&PI_Vbus);
268 PI_GRANDO_F_FUNC(&PI_Vbus);
269 PI_Vbus.term.Out *= (Filt_Vbus.y[0]/2.0)/3.0/sineanalyzer_diff1.Vrms/1.0;
270
271 Iref_a = (Curr_CMD_A + PI_Vbus.term.Out)*Vpos_norm_a;
272 Iref_b = (Curr_CMD_B + PI_Vbus.term.Out)*Vpos_norm_b;
273 Iref_c = (Curr_CMD_C + PI_Vbus.term.Out)*Vpos_norm_c;
274
275
276 // Run the neutral point voltage controller PI
277 PI_GRANDO_F_FUNC(&PI_Vbus_NP);
278 PI_Vbus_NP.term.Out /= 3.0;
279
280 // after the breaker closes switch the current controller error
281 // load the current controller error based on the actual current output
282 cc_err_a = Iref_a - Filt_IaINV.y[0];
283 cc_err_b = Iref_b - Filt_IbINV.y[0];
284 cc_err_c = Iref_c - Filt_IcINV.y[0];
285
286 CurrentControl();
```

Figure B-17. Mode 4 code.

```
287
288 if (breakercount < (unsigned long)(0.003*MEASUREFREQ))
289 {
290 breakercount++; // increment the counter variable
291 }
292 else
293 {
294 if(GpioDataRegs.GPBDAT.bit.GPIO59) // if the BreakerClosed signal is ON
295 {
296 // keep working as normal
297 breakercount++; // increment the counter variable
298 if(breakercount > (unsigned long)(maintain_mode_time*MEASUREFREQ))
299 {
300 State_Ptr = &M5;
301 }
302
303 }
304 else // if the BreakerClosed signal is OFF
305 {
306 if (breakercount3 < (unsigned long)(0.001*MEASUREFREQ))
307 {
308 // Turn off the main PWM
309 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
310 // Turn off the aux PWM
311 GpioDataRegs.GPACLEAR.bit.GPIO11 = 1;
312
313 breakercount3++;
314 }
315 else
316 {
...
320
321 // To go back to idle mode after M4
322 State_Ptr = &M2;
323
324 // Turn off the main PWM
325 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1;
326
327 // To go to M5 and do compensation
328 // State_Ptr = &M5;
329
330 // Clear the breakercount variables to reset the timing.
331 breakercount = 0;
332 breakercount3 = 0;
333 }
334 }
335
336
337 }
338
339 if(!GpioDataRegs.GPBDAT.bit.GPIO32)
340 {
341 fault_flag = 1; // Raise the fault flag
342
343 // Go back to MODE 1 where all PWM is OFF
344 State_Ptr = &M1;
345 }
349 undervoltage_flag = 1; // Raise the undervoltage flag
```

Figure B-17. Mode 4 code (Continued).

```
346
347 if(ADC.Vbus < 5700.0)
348 {
350
351 // Go back to MODE 1 where all PWM is OFF
352 State_Ptr = &M1;
353 }
354
355 }
```

Figure B-17. Mode 4 code (Continued).

Mode 5:

- Check the grid-connect time to determine if the breaker should be opened.
- Continue to ramp the dc bus reference if necessary.
- Run the bus voltage controllers
- Ramp the current compensation reference
- Load the current controller PR controller error
- Run the current controller based on the measured output current
- After set time transition to Mode 2 while compensating for breaker delays.

```
357 void M5(void)
358 {
359
...
368 if (GpioDataRegs.GPBDAT.bit.GPIO40 && breakercount2 < (unsigned long)
    (grid_connect_time*MEASUREFREQ))
369 {
370 breakercount2++;
371 }
372 else
373 {
374 GpioDataRegs.GPBCLEAR.bit.GPIO40 = 1;
375 breakercount2 = 0;
376 }
377
378 if(dcbusval < dcbusref) // ramp the dc-bus reference to a higher value
379 {
380 dcbusval += 0.15; // ((s/cycle)/(ramp time))*(dcbusref - dcbusval(0))
381 }
382
383 if(k < 1.0){k += (1.0/(0.050*MEASUREFREQ));}
384
```

Figure B-18. Mode 5 code.

```
385
386 PI_GRANDO_F_FUNC(&PI_Vbus);
387 PI_Vbus.term.Out *= (Filt_Vbus.y[0]/2.0)/3.0/sineanalyzer_diff1.Vrms/1.0;
388
389 Iref_a = (Curr_CMD_A + PI_Vbus.term.Out)*Vpos_norm_a +
    (LoadPower/3.0*Vpos_norm_a - Filt_IaL.y[0])*k;
390 Iref_b = (Curr_CMD_B + PI_Vbus.term.Out)*Vpos_norm_b +
    (LoadPower/3.0*Vpos_norm_b - Filt_IbL.y[0])*k;
391 Iref_c = (Curr_CMD_C + PI_Vbus.term.Out)*Vpos_norm_c +
    (LoadPower/3.0*Vpos_norm_c - Filt_IcL.y[0])*k;
392
393 PI_GRANDO_F_FUNC(&PI_Vbus_NP);
394 PI_Vbus_NP.term.Out /= 3.0;
395
396 // after the breaker closes switch the current controller error
397 // load the current controller error based on the actual current output
398 cc_err_a = Iref_a - Filt_IaINV.y[0];
399 cc_err_b = Iref_b - Filt_IbINV.y[0];
400 cc_err_c = Iref_c - Filt_IcINV.y[0];
401
402 CurrentControl();
403
404 if(GpioDataRegs.GPBDAT.bit.GPIO59) // if the BreakerClosed signal is ON
405 {
406 // keep working as normal
407
408 }
409 else // if the BreakerClosed signal is OFF
410 {
411 if (breakercount3 < (unsigned long)(0.001*MEASUREFREQ))
412 {
413 // Turn off the main PWM
414 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1; // CBC TRIP 1 output to FPGA
415 // Turn off the aux PWM
416 GpioDataRegs.GPACLEAR.bit.GPIO11 = 1; // CBC TRIP 2 output to FPGA
417
418 breakercount3++;
419 }
420 else
421 {
...
425
426 // To go back to idle mode after M4
427 State_Ptr = &M2;
428
429 // Turn off the main PWM
430 GpioDataRegs.GPACLEAR.bit.GPIO8 = 1; // CBC TRIP 1 output to FPGA
...
437 // Clear the breakercount variable to reset the timing.
438 breakercount = 0;
439 breakercount3 = 0;
440 k = 0.0;
441 }
442 }
443
444 if(!GpioDataRegs.GPBDAT.bit.GPIO32)
445 {
446 fault_flag = 1; // Raise the fault flag
```

Figure B-19. Mode 5 code (Continued).

```
447
448 // Go back to MODE 1 where all PWM is OFF
449 State_Ptr = &M1;
450 }
451
452 if(ADC.Vbus < 5700.0)
453 {
454 undervoltage_flag = 1; // Raise the undervoltage flag
455
456 // Go back to MODE 1 where all PWM is OFF
457 State_Ptr = &M1;
458 }
459 }
```

Figure B-20. Mode 5 code (Continued).

B.2.3 Compensator Functions

Current Controller:

- Load the compensator errors
- Run the compensator

```
461 void CurrentControl()
462 {
463
464 float norm_denom = 2.0*(Filt_Vbus.y[0]/2.0); // normalizing denominator
factor for developing the PWM control signal;
465
466 //--------------- Run the compensator ---------------//
467
468 COMP1.xa = cc_err_a;
469 COMP1.xb = cc_err_b;
470 COMP1.xc = cc_err_c;
471 Compensator_FUNC(&COMP1, K_wTs);
472
473 //---------------- Develop the PWM -----------------//
474
475 PWM.CMP_A1 = COMP1.ya/norm_denom + 0.5 - PI_Vbus_NP.term.Out;
476 if(PWM.CMP_A1 > 1){PWM.CMP_A1 = 1;}
477 if(PWM.CMP_A1 < 0){PWM.CMP_A1 = 0;}
478
479 PWM.CMP_B1 = COMP1.yb/norm_denom + 0.5 - PI_Vbus_NP.term.Out;
480 if(PWM.CMP_B1 > 1){PWM.CMP_B1 = 1;}
481 if(PWM.CMP_B1 < 0){PWM.CMP_B1 = 0;}
482
483 PWM.CMP_C1 = COMP1.yc/norm_denom + 0.5 - PI_Vbus_NP.term.Out;
484 if(PWM.CMP_C1 > 1){PWM.CMP_C1 = 1;}
485 if(PWM.CMP_C1 < 0){PWM.CMP_C1 = 0;}
486
487 }// end bracket for Controller Function
```

Figure B-21. Current controller function code.

```
534 void Compensator_FUNC(COMP *comp, float K_wTs)
535 {
536 // The transfer function for each phase
537 float comp_temp1 = (float)(TWO_PI*MEASUREFREQ*FilterL/12.0*0.9);
538 float comp_temp2 = (float)(120.0/(TWO_PI*MEASUREFREQ));
539
540 comp->SOGI_w_a.x[0] = comp->xa;
541 comp->SOGI_w_a.K = (comp_temp1/comp_temp2)*K_wTsSIN;
542 SOGI_FUNC(&comp->SOGI_w_a, K_wTs); // SOGI at w
543
544 comp->SOGI_w_b.x[0] = comp->xb;
545 comp->SOGI_w_b.K = (comp_temp1/comp_temp2)*K_wTsSIN;
546 SOGI_FUNC(&comp->SOGI_w_b, K_wTs); // SOGI at w
547
548 comp->SOGI_w_c.x[0] = comp->xc;
549 comp->SOGI_w_c.K = (comp_temp1/comp_temp2)*K_wTsSIN;
550 SOGI_FUNC(&comp->SOGI_w_c, K_wTs); // SOGI at w
551
552 comp->ya = comp->SOGI_w_a.y[0] + comp_temp1*comp->xa;
553 comp->yb = comp->SOGI_w_b.y[0] + comp_temp1*comp->xb;
554 comp->yc = comp->SOGI_w_c.y[0] + comp_temp1*comp->xc;
555
556 }
```

Figure B-22. The compensator function code.

- Form the modulation waveforms for the PWM modules.

The compensator function performs the PR controller functionality (See Figure B-22).

B.3 The Field Programmable Gate Array (FPGA)

For simplicity only the top-level VHDL code is shown here. The instantiated components used are:

- OSCH: Internal oscillator component to produce the main timing clock
- PLL_CLK: A phase-lock-loop component to produce a higher frequency clock
- Bus_Master: A data bus manager that regulates access to the shared block memory instantiated with the FPGA.
- ePWM_Master: Higher-level component that contains all the instantiated ePWM modules which mimic the Texas Instruments C2000 DSP ePWM modules.

- ParallelPort: Custom parallel data port that allows faster communication with the DSP.

These components are shown in Figure B-23 to Figure B-27.

```
71 component OSCH
72 generic(
73 NOM_FREQ : string := "8.31"
74 );
75 port(
76 STDBY : in std_logic;
77 OSC : out std_logic;
78 SEDSTDBY : out std_logic
79 );
80 end component;
```

Figure B-23. Internal oscillator component.

```
83 component PLL_Clk
84 PORT(
85 ClkI : in std_logic;
86 ClkOP : out std_logic;
87 Lock : out std_logic
88 );
89 end component;
```

Figure B-24. Phase-Lock Loop component.

```
92  component Bus_Master
93  PORT(
94  clk : in std_logic;
95  rst : in std_logic;
96  Data : inout std_logic_vector(15 downto 0);
97  Addr : in std_logic_vector(15 downto 0);
98  Xrqst : in std_logic;
99  XDat : out std_logic;
100 YDat : in std_logic;
101 BusRqst : in std_logic_vector(9 downto 0);
102 BusCtrl : out std_logic_vector(9 downto 0)
103 );
104 end component;
```

Figure B-25. Data bus manager component.

```
107 component ePWM_Master is
108 port(
109 clk : in std_logic; -- timer clock
110 rst : in std_logic;
111 SyncIN : in std_logic; -- external input synching signal
112 tripCBC_main: in std_logic; -- trip indicator bit for main pwm
113 tripCBC_aux : in std_logic; -- trip indicator bit for au
114 tripOSHT : in std_logic; -- trip indicator bit
115 ClearOSHT : in std_logic; -- clearing bit for one-shot tripping
116 CtrIsPrd : out std_logic;
117 CtrIsZero : out std_logic;
118 IsTripped : out std_logic;
119 ePWMMAIN : out std_logic_vector(59 downto 0);
120 ePWMAUX : out std_logic_vector(19 downto 0);
121 Data : inout std_logic_vector(15 downto 0);
122 Addr : out std_logic_vector(15 downto 0);
123 Xrqst : out std_logic;
124 XDat : in std_logic;
125 YDat : out std_logic;
126 BusRqst : out std_logic;
127 BusCtrl : in std_logic
128 );
129 end component;
```

Figure B-26. High-level ePWM component.

```
145 component ParallelPort is
146 port(
147 clk : in std_logic; -- timer clock
148 rst : in std_logic;
149 CtrIsZero : in std_logic;
150 PP_AddrIN : in std_logic_vector(5 downto 0);
151 PP_AddrOUT : out std_logic_vector(5 downto 0);
152 PP_DataIN : in std_logic_vector(15 downto 0);
153 PP_DataOUT : out std_logic_vector(15 downto 0);
154 PP_Xdat : in std_logic;
155 PP_Xrqst : in std_logic;
156 PP_Ydat : out std_logic;
157 PP_Yrqst : out std_logic;
158 PP_DirCont : in std_logic; -- allows external master to enable CPLD tri-state
159 Data : inout std_logic_vector(15 downto 0);
160 Addr : out std_logic_vector(15 downto 0);
161 Xrqst : out std_logic;
162 XDat : in std_logic;
163 YDat : out std_logic;
164 BusRqst : out std_logic;
165 BusCtrl : in std_logic;
166 LED_1 : out std_logic;
...
174 debug1 : out std_logic;
175 debug2 : out std_logic
176 );
177 end component;
```

Figure B-27. Custom parallel port component.

All design and reference files for this dissertation can be found in the “Vinson Jones” folder on the research group share drive (N:).