A 10GB/S FULL ON-CHIP BANG-BANG CLOCK AND DATA RECOVERY SYSTEM USING AN ADAPTIVE LOOP BANDWIDTH STRATEGY

A Thesis

by

HYUNG-JOON JEON

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
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ABSTRACT

A 10Gb/s Full On-chip Bang-Bang Clock and Data Recovery System Using an Adaptive Loop Bandwidth Strategy.

(August 2009)

Hyung-Joon Jeon,

B.S., Seoul National University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

As demand for higher bandwidth I/O grows, the front end design of serial link becomes significant to overcome stringent timing requirements on noisy and bandwidth-limited channels. As a clock reconstructing module in a receiver, the recovered clock quality of Clock and Data Recovery is the main issue of the receiver performance. However, from unknown incoming jitter, it is difficult to optimize loop dynamics to minimize steady-state and dynamic jitter.

In this thesis a 10 Gb/s adaptive loop bandwidth clock and data recovery circuit with on-chip loop filter is presented. The proposed system optimizes the loop bandwidth adaptively to minimize jitter so that it leads to an improved jitter tolerance performance. This architecture tunes the loop bandwidth by a factor of eight based on the phase information of incoming data. The resulting architecture performs as good as a maximum fixed loop bandwidth CDR while tracking high speed input jitter and as good as a minimum fixed bandwidth CDR while suppressing wide bandwidth steady-state

jitter. By employing a mixed mode predictor, high updating rate loop bandwidth adaptation is achieved with low power consumption. Another relevant feature is that it integrates a typically large off-chip filter using a capacitance multiplication technique that employs dual charge pumps.

The functionality of the proposed architecture has been verified through schematic and behavioral model simulations. In the simulation, the performance of jitter tolerance is confirmed that the proposed solution provides improved results and robustness to the variation of jitter profile. Its applicability to industrial standards is also verified by the jitter tolerance passing SONET OC-192 successfully.

To my parents and sister

ACKNOWLEDGEMENTS

Since the summer of 2006, I have enjoyed studying in the AMSC group. One of my best moments in the past three years was when I began to work with my advisor, Dr. J.Silva-martinez. His advice enriched my academic knowledge and his support encouraged me to focus on what I really love to study. Thanks to him, I now see myself much better than when I started my degree.

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CHAPTER I

INTRODUCTION

1. Overview of Clock and Data Recovery in Serial Link

As demand on technology becomes higher in the every part of life, the volume of information to be processed by computing devices also increases. Communication and network industry has confronted wide bandwidth requirement for supporting people to enjoy the advanced computing technology without the limitation of time and places. Those trends also have driven the wide bandwidth technology for hardware-to-hardware communication such as video network, device I/O network and chip-to-chip network.

As the requirement is becoming more stringent, the front end of wireline communication applications must enable high data rate transportation between the devices along the channel with finite bandwidth. Although employing multiple channels might be able to simply increase the bandwidth requirement, it will drastically draw high cost for the hardware implementation as data rate increases. Serial link has been spotlighted as a solution because it saves the implementation cost. With low swing-high data rate signaling by multiplexing, the serial link requires fewer number of the channel material.

Figure 1.1 shows the general example of the front end in the serial link application.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

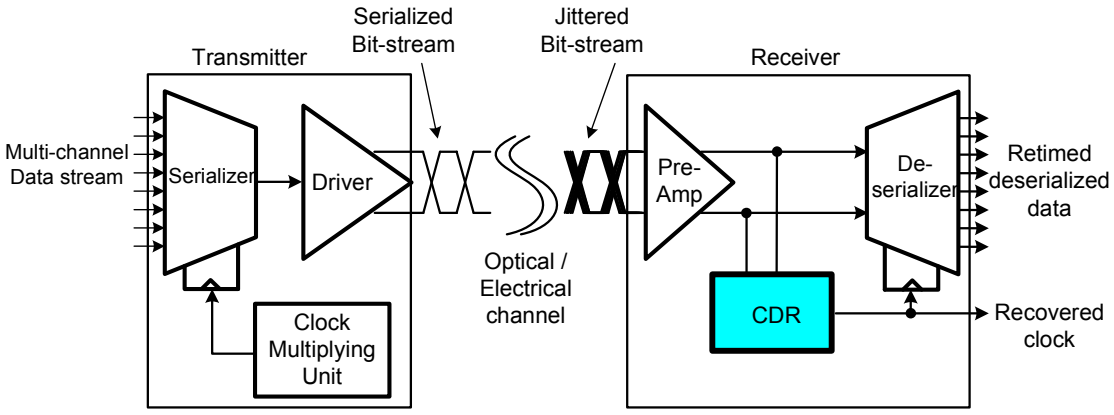


Figure 1. 1 Front end in serial link application

A serializer generates high speed digital data stream by multiplexing with Clock Multiplying Unit (CMU). The serialized data stream is attenuated at the end of the channel after delivered by output driver in a transmitter. The data is regenerated to certain level after pre-amplifier stages. Since the data is transported in the absence of a clock, a receiver should recover the clock to retime the data at the right instant. Synchronized by the recovered clock, a de-serializer parallelizes the input data stream to several slow rate data streams into digital computing systems.

Low pass characteristic of the channel not only attenuates the amplitude of the signal but also distorts the shape of data transition. Noise also reduces timing margin from various sources. Supply noise and thermal noise from the transmitter, and cross-talk between the channels affects the shape of the data transition. The distorted data transition reduces timing margin to make a correct data level decision. The loss of timing margin is called *jitter* which is defined as *the timing variation of digital signal from its ideal points* in[1].

While the attenuated data amplitude can be easily recovered by using a comparator, the jitter is hardly corrected by a simple circuitry because the exact time deviation needs to be compensated. Therefore, a special module is required to recover the clock from timing distortion.

Clock and data recovery (CDR) circuits are the clock reconstructing module of a receiver. It extracts the clock at the optimal point from the random input data stream in spite of the presence of jitter. As the data rate increases up to more than 10Gb/s on single channel, the tolerable timing jitter decreases to maintain bit-error rate below certain level that the data level decision on the incoming data is more sensitive to the quality of the recovered clock. Thus, CDR becomes a crucial component for the overall receiver performance.

High quality recovered clock and data is the primary goal of CDR. CDR should recover the clock in the presence of frequency offset, jitter and the randomness of data pattern. The clock frequency offset will be presented between devices if the frequency of CMU in a transmitter is slightly different from the recovered clock of a receiver. CDR should detect the offset and adjust the frequency of the recovered clock as early as possible. As afore-mentioned, jitter is the main issue of recovering clock and data. CDR needs to filter the jitter to increase timing margin. The CDR recovers the clock from non-periodic random data. Due to the absence of frequency information in the random data, the CDR must equip special frequency and phase extraction scheme [2].

Cost optimization for implementation is another goal of CDR design. Industry faces the design trend of low power and low area. However, due to high speed operation,

most of CDR consumes high power more than 100mW for multi-Gb/s applications in >0.18um CMOS technology [3-6]. Moreover, for jitter filtering, large passive elements are required for narrow bandwidth implementation with the high data rate operation. Thus, the power and area need to be optimized for the CDR design as it can be a bottle neck of the overall receiver implementation.

2. Topologies of Clock and Data Recovery

To recover the high quality clock with less implementation cost, various approaches have been proposed for CDR applications. Most of previously proposed CDRs can be classified into *open loop type CDR* and *feedback type CDR* [7]. The open loop CDR is a very attractive solution for burst mode data communication because this type of CDR can achieve fast locking and high stability due to its open loop architecture. Phase oversampling[8], gated VCO and high Q band-pass filter have been adopted to implement the open loop CDR. Limited frequency tracking is the common drawback of this open loop CDR because frequency extraction is generally hard to be accomplished without a feedback. The other problems of the open loop type CDR are low jitter suppression (Gated VCO) and high implementation cost (high Q band-pass filter). The feedback type CDRs are based on Phase-Locked Loop (PLL) or Delay-Locked Loop (DLL) structures. Many different types of topology have been suggested by means of phase interpolator [9], injection locking scheme, and the combination of PLL and DLL [10, 11]. Long lock time and stability have been pointed as the inherent problems of this type of CDR. Nevertheless, the feedback type CDR is most widely used because it

demonstrates superior performance for bit-rate variation, frequency offset and jitter suppression.

The feedback type CDR is divided into three different types of topology, analog based PLL[3, 5, 6], digital based PLL[12] and semi-digital based PLL/DLL[9, 13, 14], according to the implementation. Analog PLL based CDR transfers all information as continuous analog form of time, voltage and current between the building blocks. As shown in figure 1.2, PD, CP and analog loop filter generate the continuous control voltage of VCO in order to adjust the phase and frequency of recovered clock. The advantage of this topology is high speed implementation in limited technology. However, it generally experiences the leakage in the loop filter and is susceptible to supply noise.

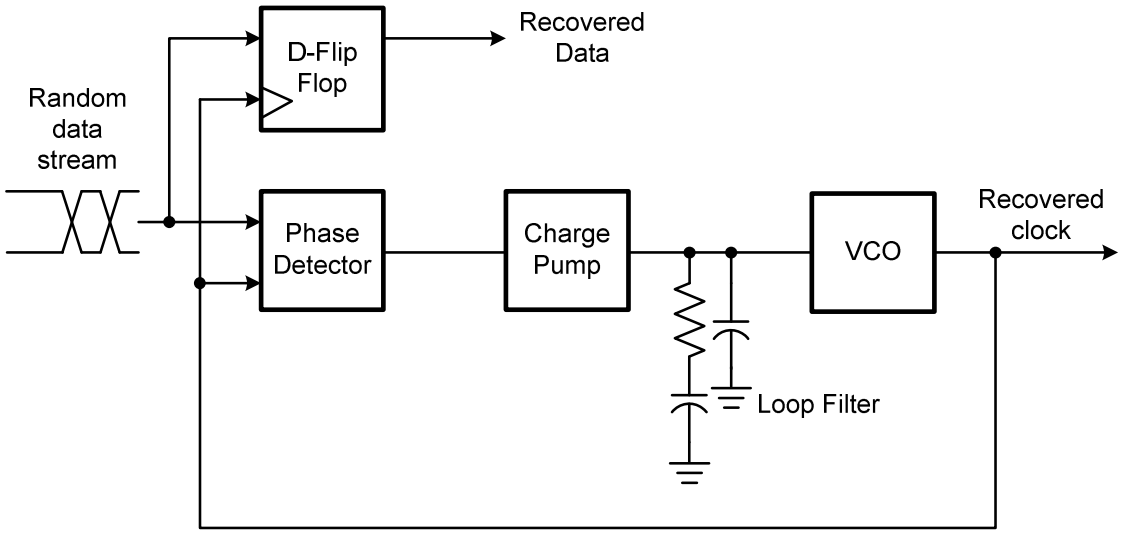


Figure 1. 2 Analog PLL based CDR

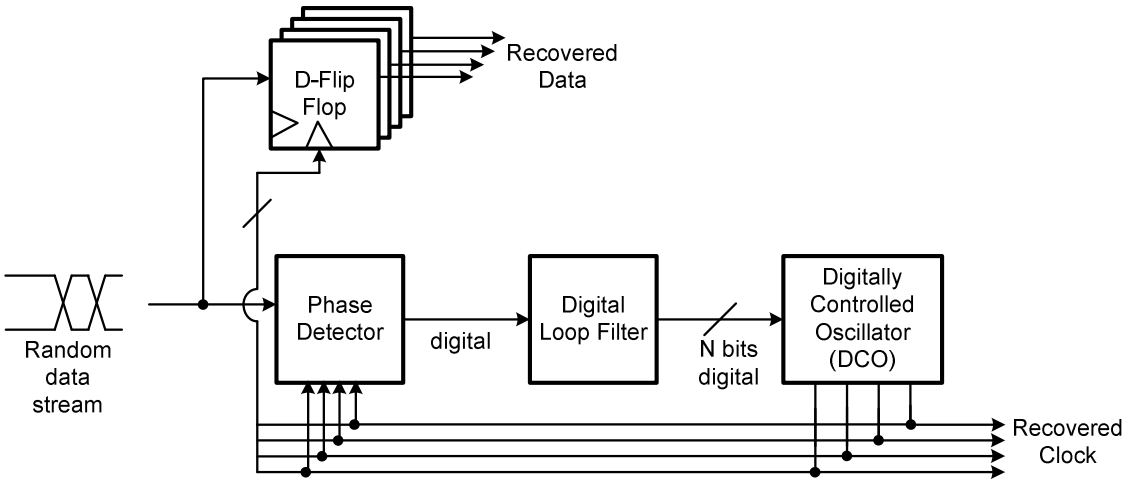


Figure 1. 3 Digital PLL based CDR

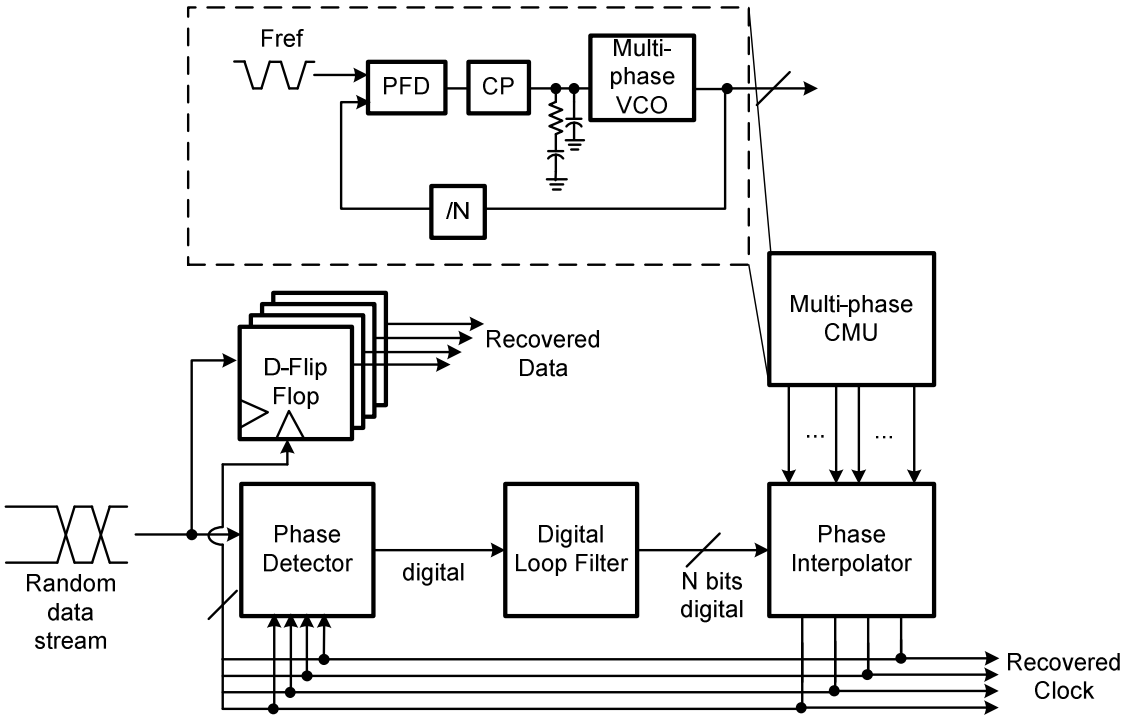


Figure 1. 4 Semi-digital type CDR

In the digital PLL based CDR in figure 1.3, the most of building blocks utilize digital I/Os to control loop dynamics while it still presents the behavior of general PLL [12, 15]. This type of system provides the flexibility of the design because it can be implemented with automatic design procedure as general digital system. This topology, however, is hard to be implemented in high speed application due to the timing requirement of CMOS logic design. The semi-digital PLL/DLL based CDR is implemented with the combination of both types [9, 13]. Generally, main signal path is built with digital components from PD to control voltage while multi-phase generating components are implemented with analog circuitry as shown in figure 1.4. The semi-digital topology provides more design flexibility than the digital based PLL in high speed applications. Nevertheless, the speed limitation of digital circuitry still results in degraded performance in >10Gb/s applications.

Despite of its limitation, the analog PLL is still widely preferred to implement high speed clock and data recovery over the digital or semi-digital topologies. The main reason is that analog loop filter implementation is not limited by input data rate due to its passive-only elements while a digital loop filter implementation is dependent on input data rate. It is necessary to implement high depth digital logic for the digital loop filter in order to recover a clock with high resolution phase step. Since more timing margin is required for higher logic depth, the limit of clock frequency of the filter is determined by the requirement of the clock phase step resolution and f_t of its technology. Since the maximum updating rate of overall PLL loop is limited by loop filter frequency, the ratio of input data rate to loop-updating rate increases for very high data rate application in

low f_t technology. Then, additional timing jitter is introduced associated with an inherent digital feedback system behavior, *limit cycle*. The limit cycle will be discussed in the chapter II. To minimize the jitter from the limit cycle, the digital loop filter should be functional at even more than 1GHz clock for >10Gb/s applications. Due to the limited f_t in 0.18um CMOS technology, it is hard to implement 1GHz high depth digital filter with general CMOS logic design. Although CML design may achieve high speed requirement, it is not appropriate for high depth logic design due to its excessive power consumption. Pipe-lined design approach may be able to realize a high speed-high depth digital loop filter. However, it also increases loop delay that the effect of limit cycle will be seriously magnified. As it is free from the afore-mentioned issues of loop filter implementation, an analog PLL based CDR will be considered as the best topology for high input data rate application in low f_t CMOS technology.

3. Organization

This thesis is composed of 5 separate chapters to discuss the motivation, implementation and verification of proposed novel clock ad data recovery.

This chapter introduces the overall architecture of a serial link transceiver and various CDR topologies.

Chapter II reviews the property of Bang-Bang CDR and its jitter performance. Identifying the problem of conventional structures, the trade-off in jitter tolerance will be discussed for loop bandwidth setup. With the comparison of previous solutions, it is justified the necessity of novel CDR

In Chapter III, the proposed solution will be described. The main idea will be discussed and relevant issues will be verified by graphical and mathematical analysis. Describing the implementation in detail, overall design procedure will be discussed.

The proposed solution will be verified by performing Cadence simulation in chapter IV. After summarizing all the features, conclusion is made in chapter V.

CHAPTER II

ANALYSIS OF ANALOG BANG-BANG PHASE LOCKED LOOP FOR CLOCK AND DATA RECOVERY APPLICATION

1. Background of Analog Bang-Bang PLL

As previously shown in figure 1.2, the conventional analog PLL is generally composed of phase detector (PD), charge pump (CP), loop filter and voltage-controlled oscillator (VCO). PD detects phase difference between input data and recovered clock, and produces the corresponding information. CP simply carries out the conversion of the information from PD to be appropriate to the loop filter. The VCO transforms the information to the form of phase. Other components can be required for interfaces, noise immunity and other improvement.

Analog PLLs are categorized by the type of PD. A linear PLL is simply represented as a linear feedback system with a linear type PD. On the other hand, a binary or Bang-Bang PLL exhibits similar behavior to digital system by utilizing a binary type PD (or Bang-Bang PD). The conceptual illustration of the analog PLL is shown in figure 2.1. Note that other components are simply represented as gain (CP), poles/zeros (loop filter) and integrator (VCO), respectively.

While the linear PD produces its output proportional to the phase error, Bang-Bang PD (BBPD) returns its output from the polarity of the phase error. BBPD generates additional timing jitter due to quantization error. Despite of the disadvantage, BBPD is more advantageous than linear PD for high-speed application because of following

reasons. Firstly, BBPD effectively produces the output even with very small phase error. Since the PD generally presents the phase error as output pulse width, the linear PD must generate very small pulse width when the PLL is locked and the phase error is very small. On the other hand, BBPD holds the output for one clock period irrespective of the size of phase error due to its binary nature. Higher f_t is generally required for linear PD than Bang-Bang PD. Thus, BBPD is power efficient over the linear PD in high speed applications.

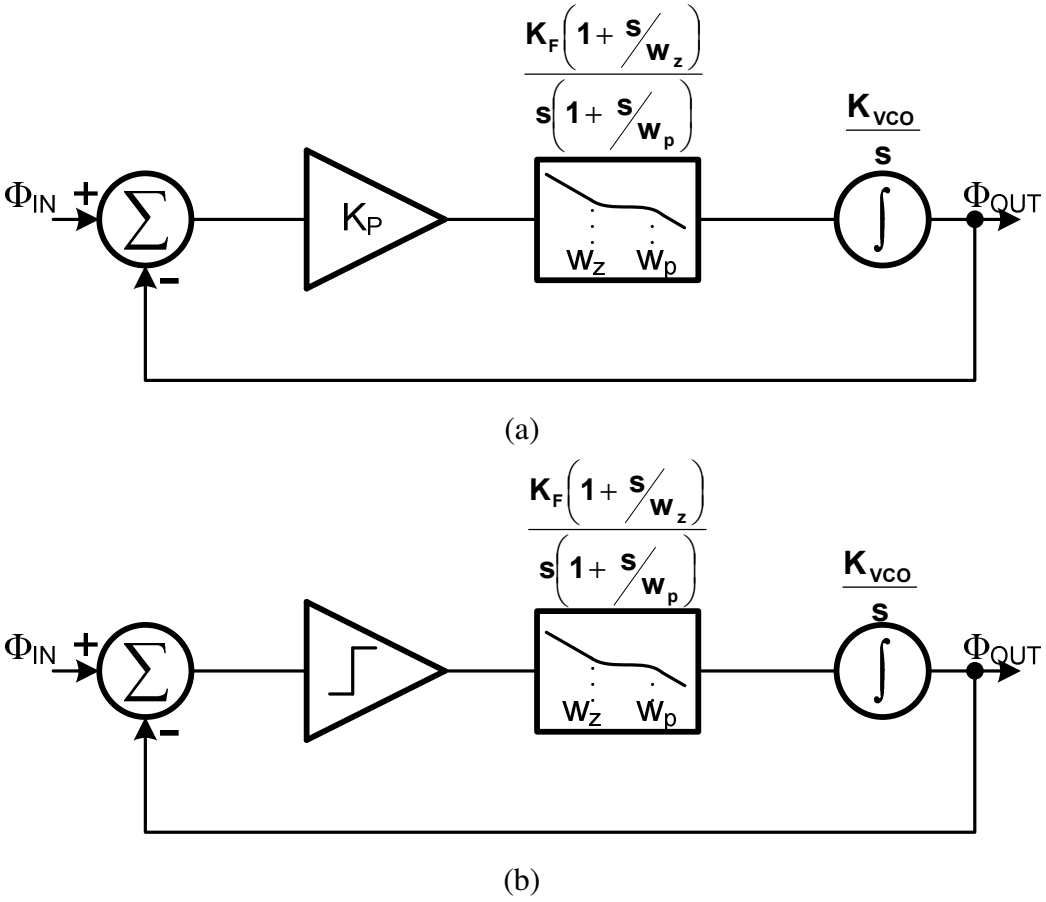
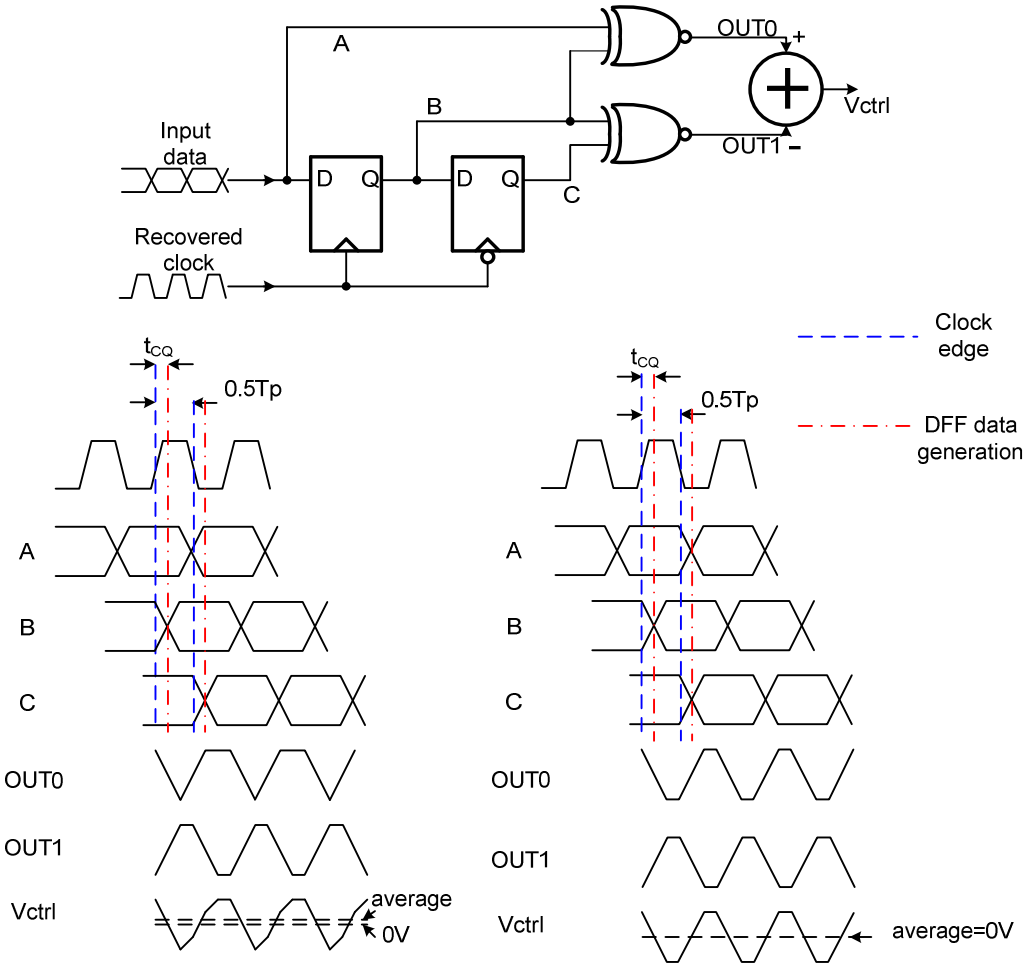
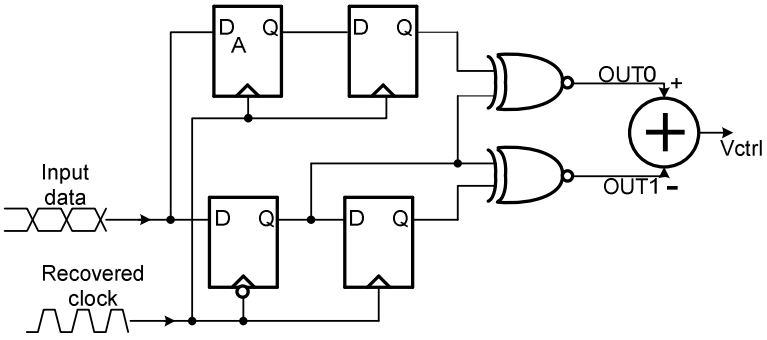


Figure 2. 1 The conceptual model of analog PLL (a) Linear PLL (b) Bang-Bang PLL



(a)



(b)

Figure 2. 2 (a) Phase offset issue of Hogge Detector (b) Alexander PD

Secondly, BBPD is robust to delay issue. Hogge detector, the most commonly used linear PD in CDR application, generates output with XORs and flip-flops as shown in figure 2.2(a). It introduces certain phase offset because there is a finite timing skew between input data and re-sampled data due to clock-to-data delay (t_{CQ}) of flip flop. As shown in the left timing diagram in figure 2.2(a), the output of control voltage will not be locked even if the clock ideally samples data at exact middle point of a bit period. When the clock samples data with phase offset, which is equal to (t_{CQ}), the control voltage presents zero averaged output, and then CDR will be locked at this steady-state. However, BBPD never experiences this problem because all combinational logics are preceded by filp-flop. As an example, Alexander PD, the commonly used topology, is shown in figure 2.2(b). Offset is eliminated since all inputs of XOR are synchronized at the same instant.

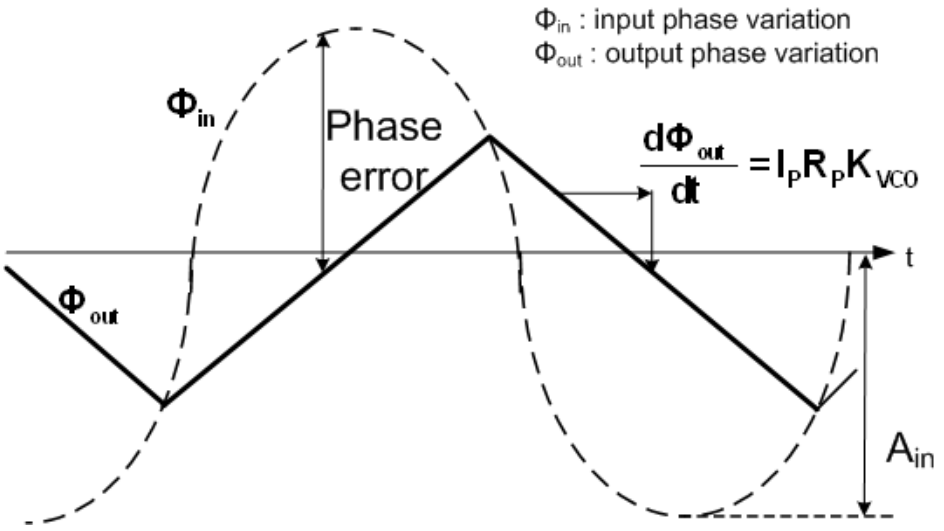


Figure 2. 3 Slope overloaded output in BBPLL

Modeling BBPD as a one-bit quantizer, the overall BBPLL can be represented as a delta-modulator, a well-known modulation scheme in the communications field. The difference is that the second or higher order loop filter adds more complexity to the first order delta-modulator. Based on the delta-modulator model, it can be shown that the loop bandwidth of the BBPLL is nondeterministic. While the loop bandwidth[1] of linear PLL is determined by internal design parameters, the loop bandwidth of BBPLL is dependent on the attribute of input phase perturbation. The characteristic originates from the slope-overloaded behavior of delta-modulator. If the instantaneous slope of input signal exceeds the step size of the delta-modulator, distortion will be generated between input signal and the output of the modulator in experiencing tracking incapability. In equivalent phase model the PLL enters slope-overloaded regime if instantaneous input phase variation or instantaneous input frequency exceeds the phase step of BBPLL as shown in figure 2.3. *Phase-slewing* is the slope-overloaded phenomenon of BBPLL. In order not to experience phase-slewing, loop parameters should satisfy the following condition [16].

$$I_P R_P K_{VCO} \geq max(\varphi(t)/dt) \tag{2.1}$$

where I_P, R_P and K_{VCO} represent the pumping current of CP, resistor in the loop filter and the gain of VCO, respectively. $\varphi(t)$ denotes input phase variation. In case the $\varphi(t)$ is a

[1] Here, loop bandwidth is defined as unity gain frequency of the open loop system

sinusoidal signal, equation (2.1) can be represented by the following equation with input phase amplitude, A_{in} and its frequency, ω_{in}.

$$\begin{aligned} I_P R_P K_{VCO} &> max\left(dA_{in}\ sin\left(\omega_{in} t\right)/dt\right) \\ &= max\left(A_{in}\omega_{in}\ cos(t)\right) \\ &= A_{in}\omega_{in} \end{aligned} \tag{2.2}$$

Equation (2.2) implies large amplitude may cause phase-slewing as well as high frequency, and then attenuation ratio output versus input at certain frequency depends on input amplitude. This property leads to the consequence that the -3dB bandwidth of BBPLL is the function of A_{in}. The detailed expression of -3dB bandwidth of BBPLL is derived as equation (2.3) in [17].

$$\omega_{-3dB} = \frac{\pi I_P R_P K_{VCO}}{2A_{in}} \tag{2.3}$$

Since loop bandwidth is approximately equivalent to the -3dB bandwidth of closed loop, it is concluded from equation (2.2) and (2.3) firstly, wide loop bandwidth is required to avoid phase-slewing and secondly, loop bandwidth is inversely proportional to the amplitude of input phase variation.

Input phase perturbation also affects the transfer curve of PD. The perturbation discussed so far is mainly deterministic with phase amplitude and frequency. Random

jitter (RJ), one of unpredictable perturbations, affects loop characteristics by changing the transfer curve of PD. RJ originates from thermal noise in electrical circuits and the composition of any uncorrelated noise sources [18]. The internal random noise of PD and CP can be also referred to the input as the form of additional RJ. Because of its unpredicted manner, RJ can be analyzed only using statistic methods. Since it is difficult to apply the probability model to deterministic analysis directly, we can re-define the transfer curve of PD associated with RJ by using its probability density function (PDF). The re-defined transfer curve of PD is represented as the convolution of ideal transfer curve of BBPD and PDF of RJ as shown in equation (2.4) [17].

$$\overline{V_{new}}(\Delta T) = \int_{-\infty}^{+\infty} \overline{V_{ideal}}(\Delta T - x)\, p(x)\, dx \tag{2.4}$$

where $\overline{V_{new}}$ and $\overline{V_{ideal}}$ are the transfer function of PD with and without RJ, respectively. ΔT is timing error applied at the input of PD, and $p(x)$ is the PDF of random jitter.

The transfer curve of PD is determined by the meta-stability of a flip-flop as well. So far, we have assumed that transfer curve displays extremely steep slope of transition around zero phase error point unless random noise is presented at the input. The assumption, in practice, does not hold because the flip-flop is not able to reach full swing level with very small phase error. A flip-flop is generally composed of two cascaded D-latches. The D-latch samples data by pre-amplification and regenerates it with a positive

feedback. The speed limitation of circuit may fail the D-latch to pre-amplify or to regenerate output voltage to valid level if allowed time or applied input voltage level is not enough. Therefore, smooth transition will be shown around zero phase error in the transfer curve.

Due to the RJ and meta-stability, PD presents linear-shaped transfer curve around the zero phase error region. Thus, it is possible to analyze BBPLL as a piece-wise linear model if the PLL is locked that phase error is close to zero. Figure 2.4 shows how PD transfer curve changes due to RJ, meta-stability and the combined. The linear region, where is between V_{thn} and V_{thp}, is widened as the PD experiences more meta-stability and random jitter. Since the linear gain is inversely proportional to the width of the region, it is concluded that the loop gain of piecewise-linear modeled BBPLL is dependent on random jitter and process variation.

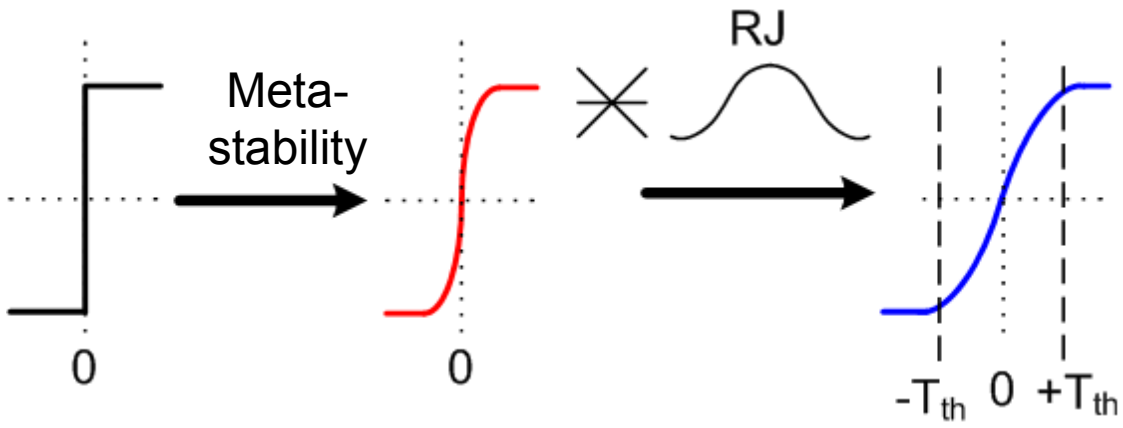


Figure 2. 4 Transfer curve variation of BBPD

The binary characteristic of BBPD also affects the steady-state behavior of PLL. A digital feedback system is not able to converge to a single state due to the discontinuity of quantization process even if the difference of input and output is close to zero. In steady-state, digital feedback system exhibits bounded periodic oscillations at the output in the manner of dithering the quantized output to be close to desired finite value [19]. The periodic oscillation, which is called *limit cycle*, is presented in the BBPLL due to its digital property with BBPD. The quantization error with the limit cycle effect causes timing misalignment. The inherent timing jitter of BBPLL is called *hunting jitter* or *dithering jitter*. The peak-to-peak hunting jitter, $\Delta t_{p\text{-}p}$, is computed as the equation (2.5) and (2.6) according to [20]. Here, $\tau = (T_{delay} / T_b)$.

$$\begin{aligned} \Delta t_{p\_p} &= I_P R_P K_{VCO} \cdot N \cdot \left(2(1+D) + (1+D)\tau + (1+D)^3 \tau^2 + O\left(\tau^3\right)\right) T_b^{\,2} \\ &= \left(I_P R_P K_{VCO} \cdot N \cdot T_{delay}\right) T_b \end{aligned} \tag{2.5}$$

or

$$\frac{\Delta t_{p-p}}{T_o} = I_P R_P K_{VCO} \cdot N \cdot T_{delay} \tag{2.6}$$

where D, T_b and T_{delay} are the normalized loop delay, bit period and effective loop delay, respectively. N denotes the division ratio of the frequency divider or the decimation ratio of digital loop filter. It is typically unity for the analog PLL based CDR. As can be seen in equation (2.6), the normalized hunting jitter is proportional to N and T_{delay}. This correlation implies the limitation of digital or semi-digital topologies as previously

discussed in chapter I. The equation (2.5) and (2.6) are derived based on the assumption that input RJ is much smaller than hunting jitter. With the presence of input RJ, [21] reported the empirical output jitter with respect to loop parameters as following[2].

$$\begin{aligned}\sigma_{OUT} &= 0.7\sqrt{\theta_{bb}\sigma_{IN}} \\ &= 0.7\sqrt{I_P R_P K_{VCO} T_{update}\sigma_{IN}}\end{aligned} \tag{2.7}$$

where σ_{OUT} and σ_{IN} represent standard deviation of output jitter and input jitter, respectively. T_{update} denotes the loop updating time. From the equation (2.3), (2.6) and (2.7), it is observed that wide loop bandwidth increases steady-state output jitter.

The pattern of input data stream is another important element affecting loop characteristics, especially on CDR applications. Unlike a normal PLL, CDR receives non-periodic random data. Since PLL detects and tracks phase error in the vicinity of data transition, the PLL can track faster the phase error as data transition occurs more frequently. Thus, loop bandwidth is also proportional to the rate of data transition, *data density*, which is defined as:

$$D = \#(data\ transition)/\#(bits\ of\ data\ stream) \tag{2.8}$$

Loop bandwidth of CDR is subsequently represented by:

[2] Note that (2.7) is valid only with moderate power of input jitter and large the stability factor (>100).

$$\omega_{loop\_CDR} = D \times \omega_{loop\_BBPLL} = \frac{\pi D I_P R_P K_{VCO}}{2A_{in}} \tag{2.9}$$

2. The Jitter Specifications in Bang-Bang Clock and Data Recovery

In high-speed wire-line communication standard, the system is required to pass different types of jitter specification. Jitter transfer (JTRAN), jitter generation (JGEN) and jitter tolerance (JTOL) are essential jitter specifications widely referred in the industry.

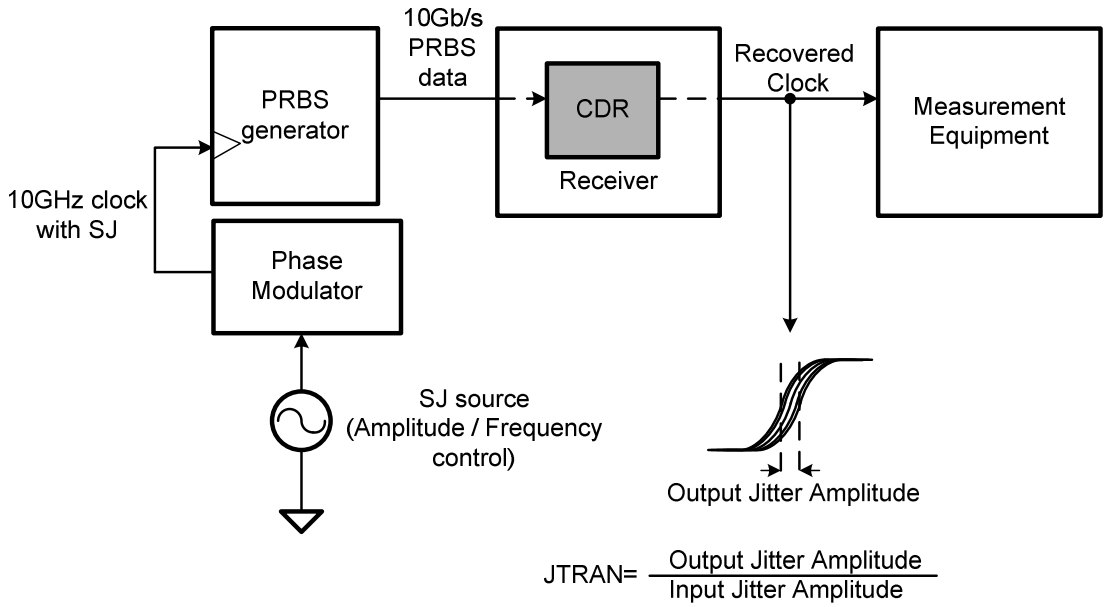


Figure 2. 5 Measurement of jitter transfer

JTRAN is defined as the output jitter suppression of the system to the input jitter. Wire-line communication network generally requires repeater in the middle of media for

the long distance communication. If the jitter is not filtered out by each repeater, the jitter is accumulated and the receiver at the final destination experiences excessive jitter which leads to the degradation of overall bit-error-rate (BER). To avoid the phenomenon, JTRAN suggests the jitter suppression standard. JTRAN is generally the specification relevant to the transmitter because the transmitter generates final output of repeater to the following system. Nevertheless, JTRAN is still the specification related to CDR applications because the jitter of recovered clock and data affects the performance of following components between digital core and receiver front-end.

As illustrated in figure 2.5, JTRAN is represented by the relative output jitter corresponding to the input SJ amplitude at certain frequency. JTRAN, therefore, is generally equivalent to the system transfer function. To satisfy the JTRAN specification, BBCDR must follow low pass characteristic as corresponding to the characteristics of the general PLL.

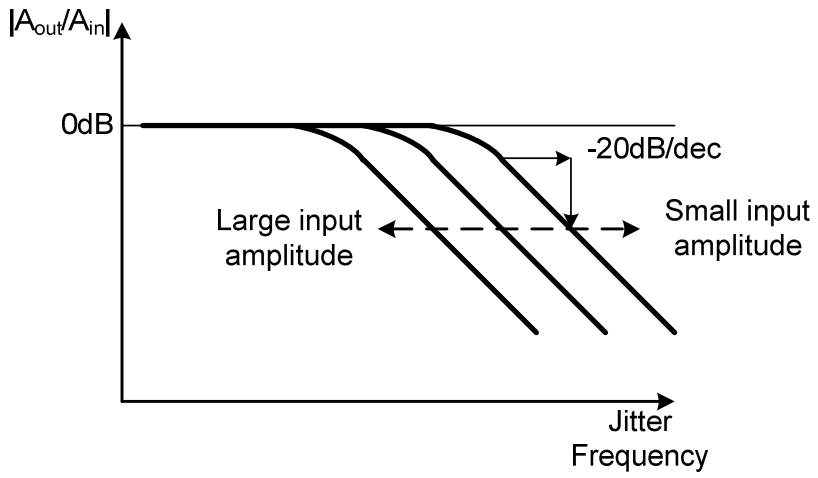


Figure 2. 6 Jitter transfer curve of BBPLL

The important factors of JTRAN are maximum gain peaking and corner frequency. Maximum gain peaking denotes the upper limit of allowable jitter amplification. Corner frequency specifies the upper limit of allowable frequency of transferred output jitter. Concerning the factors, BBCDR presents noticeable properties. First, as illustrated in figure 2.6, corner frequency is the function of input SJ amplitude since it is equivalent to -3dB frequency in equation (2.3). Second, BBCDR exhibits small gain peaking [17]. It is because high gain of PD in linear regime increases the distance between zero frequency and unity gain frequency.

JGEN is the self-generated jitter of the system with the absence of input jitter. JGEN is also the specification relevant to transmitter. Nevertheless, JGEN is still important specification for CDR as an indicator of internal jitter contribution. Figure 2.7 shows the example of JGEN measurement setup. RMS jitter and peak-to-peak jitter should be reported to represent the specification. Generally, the VCO phase noise and hunting jitter are considered as the main contributors of JGEN. Due to its high pass property VCO phase noise is suppressed by wide loop bandwidth. On the other hand, hunting jitter increases for wide loop bandwidth according to the equation (2.6). The loop bandwidth of BBCDR should be selected carefully to minimize jitters from both effects. The optimal loop bandwidth setup can be different according to the VCO topology. For example, with ring VCO, wide loop bandwidth is required to mitigate the significant VCO phase noise. On the other hand, narrow loop bandwidth can be allowed for the implementation with LC VCO because of its superior noise performance over ring VCO

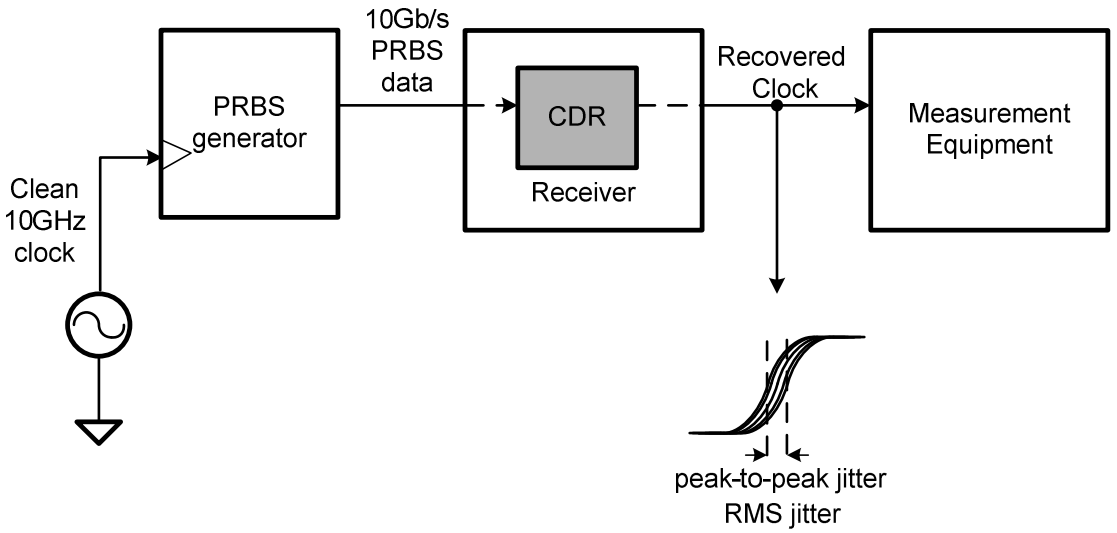


Figure 2. 7 Measurement of jitter generation

JTOL is defined as the maximum amplitude of input phase variation at the specified frequency where receiver maintains BER below the certain value. To satisfy the specification, CDR should regenerate the clock with maximal timing with the presence of jitter. Since many different jitter sources are involved in reality, it is necessary to define the various types of jitter and their characteristics in detail in order to analyze JTOL of BBCDR.

Jitter is generally categorized into two different types, random jitter (RJ) and deterministic jitter (DJ). RJ exhibits unbounded limit range while DJ varies within the certain boundary. DJ is also divided into particular subgroups. Inter-symbol interference (ISI), duty-cycle distortion (DCD) and periodic jitter (PJ) are the typical DJs as main interests in serial link. Due to its natural randomness and unbounded limit, it is hard to predict the behavior of RJ. On the other hand, there exists distinctive behavior of each

DJ. ISI results from the bandwidth limitation of the channel and digital circuitry. When high rate random data are applied at the bandwidth-limited channel and circuitry, output signal may or may not reach full swing depending on the data pattern. The effect draws different delay time for each transition, and accordingly contributes additional timing jitter. Its peak value is deterministic and bounded as shown in figure 2.8.

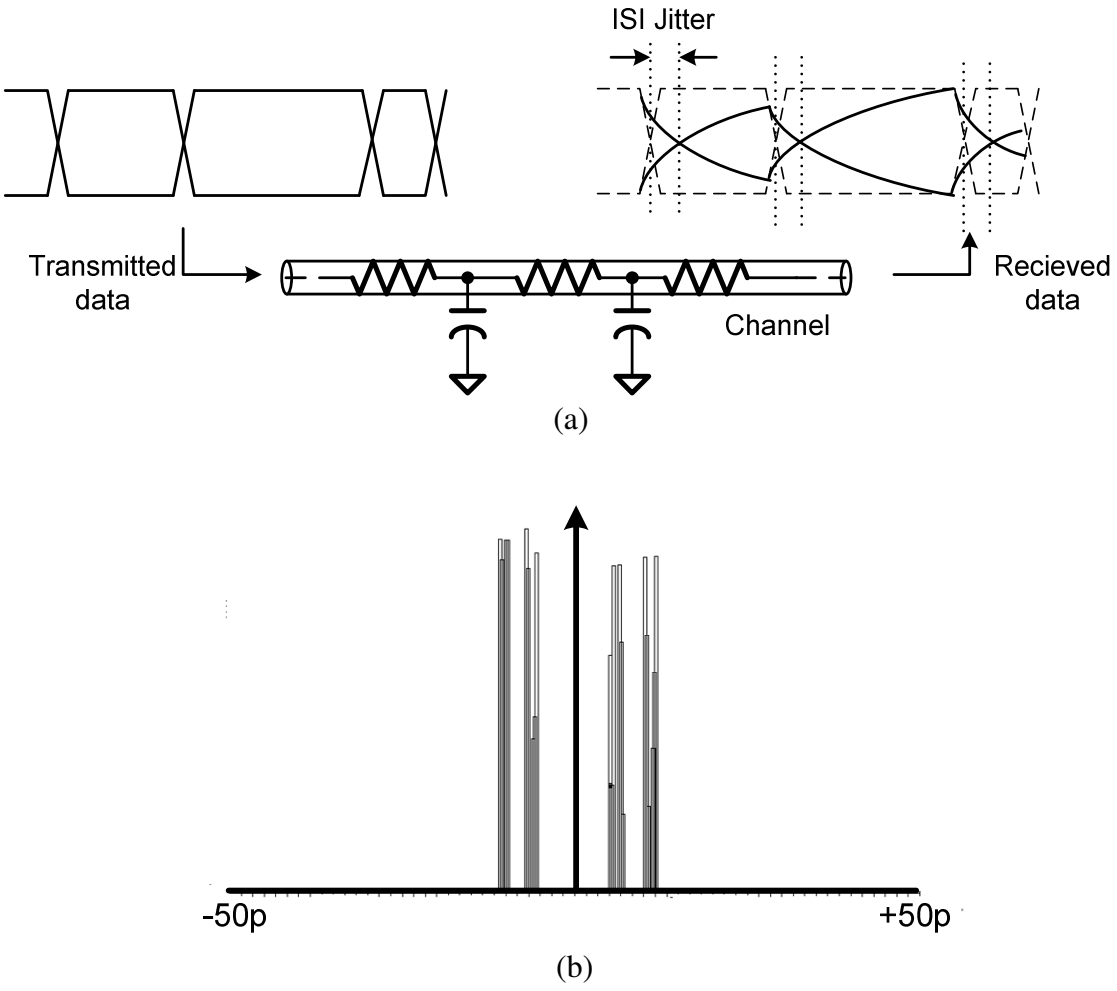


Figure 2. 8 (a) Generation of ISI and (b) its PDF

ISI is basically wide bandwidth jitter because it changes from peak to peak even in 1-bit transition. DCD is generated by the unbalanced rising and falling time of input data. Due to the offsets and mismatches of transmitter side, input data may present asymmetrical transition. It may also result from the different decision thresholds between transmitter and receiver. DCD, however, is not serious issue because it can be easily alleviated with fully differential signaling. PJ is the jitter generated by any periodic disturbances. Switching power supply noise, EMI and RF coupling are the well-known sources of PJ. While ISI and DCD are dependent on the data pattern, PJ is generally uncorrelated with input data pattern. The sinusoidal jitter (SJ) in figure 2.5 is special type of PJ. Due to its sinusoidal behavior, the peak value of SJ is bounded and its PDF exhibits high probability at the both extremes as shown in figure 2.9.

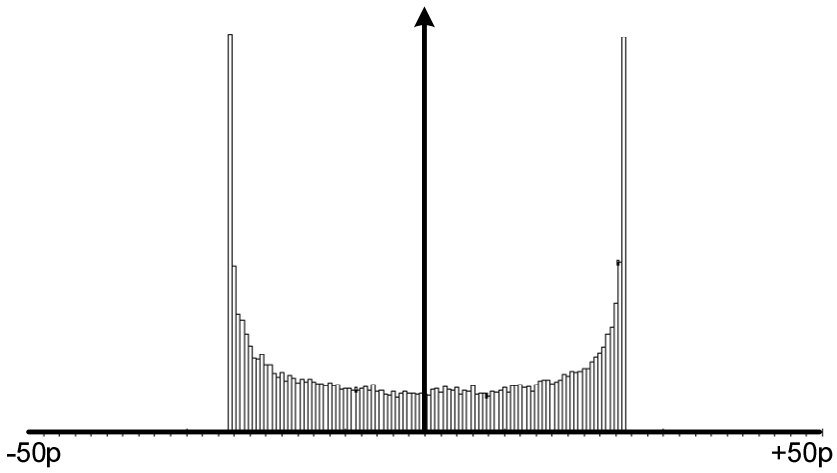


Figure 2. 9 PDF of sinusoidal jitter

To measure JTOL, input SJ is applied to the input of the system. Sweeping the SJ amplitude at the specified frequency, the maximum amplitude can be measured where the BER is beyond the certain level (typically $<10^{-12}$). After collecting these points at different frequencies, JTOL will be plotted on the frequency-amplitude plane. This curve is required to be higher than the suggested mask by industrial standard. For example, the JTOL mask of SONET-OC192 is shown in figure 2.10. Due to the low pass characteristics of CDR, JTOL mask suggests smaller amplitude as frequency increases. If the frequency is beyond the certain frequency, the tolerable amplitude becomes flat because CDR cannot track the high frequency phase variation.

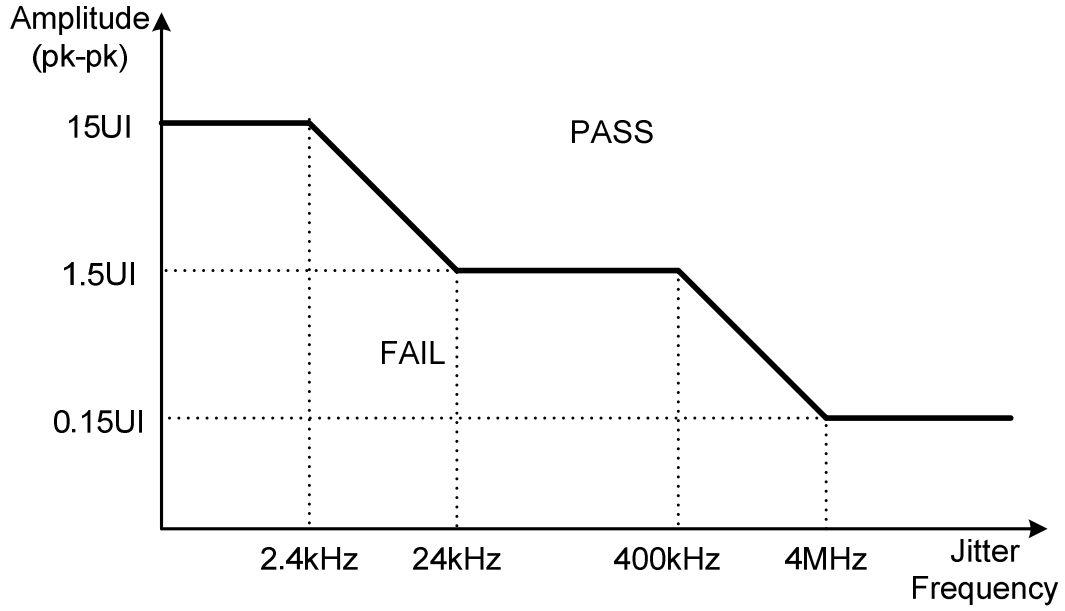


Figure 2. 10 SONET OC-192 jitter tolerance mask

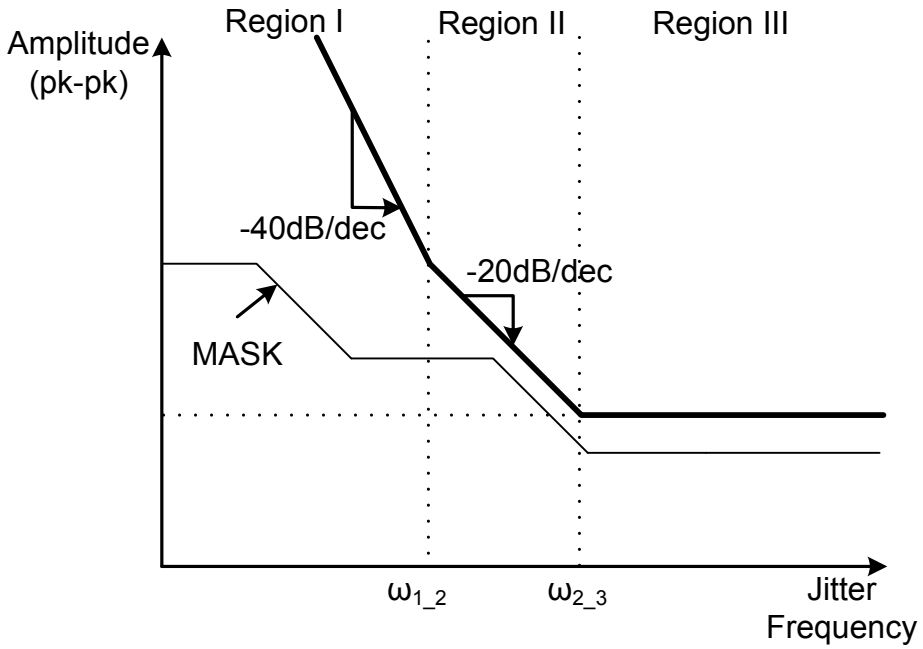


Figure 2. 11 Jitter Tolerance of BBCDR

The JTOL of BBCDR has been studied by [17]. Based on the noise-free 2nd-order BBPLL, JTOL exhibits three distinctive regions, -40dB/dec slope (region I), -20dB/dec slope (region II) and flat range (region III) as illustrated in figure. 2.11. The corner frequency between each region is expressed as:

$$\omega_{1\_2} = 0.63\frac{\pi}{R_P C_P} \tag{2.10}$$

$$\omega_{2\_3} = \frac{I_P R_P K_{VCO}}{2} \tag{2.11}$$

where ω_{1_2} is the corner frequency between region I and II, and ω_{2_3} is between –region II and III, respectively. Equation (2.10) implies that the integral gain with mainly

contributes phase tracking of PLL in region I. Equation (2.11) shows that phase tracking controlled by the proportional gain in region II. At the frequency beyond ω_{2_3}, the loop cannot track phase variation that the JTOL will be flat. The tolerable amplitude of the flat range is ideally 0.5UIpp in noise free system. In practice, however, the system should pass JTOL with the presence of unpredictable wide bandwidth jitter such as RJ and ISI as depicted in figure 2.12. The practical JTOL in the region III is computed as:

$$JTOL = JTOL_{ideal} - RJ_{pp} - ISI_{pp} - CDR_{pp} \tag{2.12}$$

where $JTOL_{ideal}$ is JTOL in noise free case. RJ_{pp} and ISI_{pp} are peak-to-peak value of input RJ and input ISI, respectively. CDR_{pp} represents transferred or self-generated output jitter. For the 10^{-12} of BER, the peak-to-peak RJ, RJ_{pp}, is represented by equation (2.13) [22].

$$RJ_{pp} = 7\sigma_{RJ} \tag{2.13}$$

where σ_{RJ} is the RMS value of RJ. As shown in equation (2.13), the JTOL is degraded by transferred or self-generated output jitter. Therefore, it is the critical design issue to pass the high frequency JTOL mask.

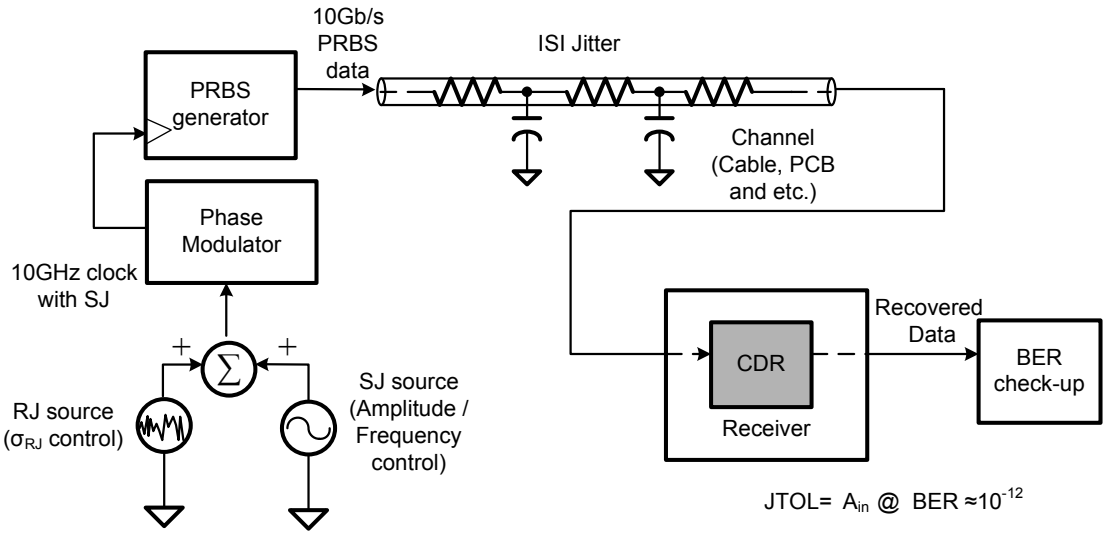


Figure 2. 12 Measurement of jitter tolerance

3 Jitter Tolerance Improvement of Bang-Bang Clock and Data Recovery

As a clock reconstructing module of the receiver, the improvement of JTOL is the primary goal of the CDR design. To guarantee more timing margin for JTOL, optimization of loop bandwidth is important issue among many considerations of CDR design. As discussed so far, wide loop bandwidth is generally advantageous to track the input SJ. In addition, VCO phase noise is highly suppressed by wide loop bandwidth feedback. The wide loop bandwidth setup, however, is not optimal with considerable RJ and ISI. As can be seen in equation (2.6) and (2.7), wide loop bandwidth magnifies wide bandwidth steady-state output jitter associated with RJ, ISI and hunting jitter. Thus, the BBCDR demonstrates degraded JTOL. On the other hand, narrow loop bandwidth of BBCDR suppresses steady-state jitter from RJ and ISI. Nevertheless, system experiences

severe phase-slewing and VCO phase noise that JTOL will be degraded. The opposing characteristics of BBCDR with the different loop bandwidth are illustrated in figure 2.13.

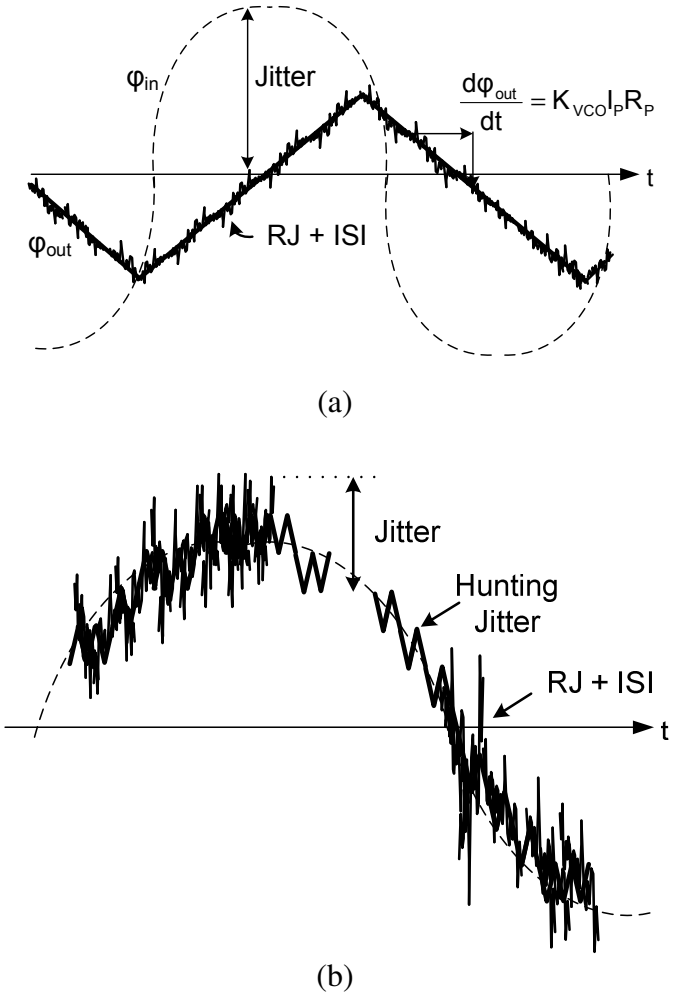


Figure 2. 13 The characteristics of (a) narrow loop bandwidth and (b) wide loop bandwidth

As a result, JTOL will be displayed according to the loop bandwidth setup as:

1) Wide loop bandwidth CDR extends region II due to its high tracking capability. However, JTOL will be degraded in region III because CDR transfers more of wide

bandwidth steady-state jitter. 2) Narrow loop bandwidth CDR suppress wide bandwidth jitter effectively so that it maintain relatively high JTOL in region III. Nevertheless, the corner frequency, ω_{2_3}, is much decreased due to inability of phase tracking.

From the observations so far, it can be found that there exists optimal loop bandwidth to maximize timing margin for JTOL improvement. The optimal loop bandwidth should be wide enough to track input phase variation without phase-slewing. The optimal loop bandwidth is also forced to produce only moderate wide bandwidth steady-state jitter. Unfortunately, the optimal bandwidth is not a deterministic value because the input jitter profile is not predictable. The narrow loop bandwidth is optimal to the case with low frequency / small amplitude input SJ in experiencing harsh RJ and ISI. In contrast, wide loop bandwidth is superior for the high frequency / large amplitude input SJ with gentle RJ and ISI.

To improve JTOL to unknown jitter profile, automatic loop bandwidth optimization schemes have been suggested by previously proposed solutions.

[23] proposes the all digital CDR with automatic loop bandwidth control. After phase error is detected by multi-phase clock, CDR selects loop bandwidth setup to track the phase error without excessive hunting jitter. Basically, [23] achieved an improved corner frequency ω_{2_3} between region II and III. The all-digital structure provides the high integration, low power and robustness to PVT variation. Nevertheless, in high frequency region III, it exhibits more degraded JTOL than the conventional topology. This mainly results from that the CDR adjusts the loop bandwidth according to the *instantaneous* phase error. This topology not only tracks input SJ but also transfers RJ

and ISI. As a result, transferred jitter degrades JTOL according to equation (2.12). The poor phase noise of multi-phase ring VCO also worsens jitter performance. Ring VCO typically demonstrates inferior phase noise performance than LC VCO. Thus, when the narrow loop bandwidth is selected, the CDR will experience serious jitter injection by VCO phase noise.

Semi-digital PLL/DLL based CDR is also proposed with the adaptive loop bandwidth approach by [24]. With digital piece-wise integration, the logic integrates the phase detector output during some cycles. If the absolute value of integrated sum is over the threshold, the loop bandwidth is increased. Conversely, the loop bandwidth is decreased in case the integrated sum is below the threshold. This approach provides the advantage of detecting relative power between wide bandwidth jitter (RJ, ISI) and phase-slewing. It improves JTOL in region III while maintaining tracking capability in region I and II. Additionally, the semi-digital structure presents good integration and moderate power consumption. However, some limitations still exist for the >10Gb/s application. First, the digital loop filter implementation is limited for the high speed application as afore-mentioned. Second, the loop bandwidth updating rate is quite slow. Due to slow updating rate of loop filter, the loop bandwidth updating process takes place every 320bits. The adaptation is not effective if the input SJ frequency is comparable to or faster than the updating rate because the adjusted loop bandwidth is outdated for the current phase variation.

In chapter III, the novel loop adaptation strategy will be discussed to optimize loop bandwidth for improved JTOL while alleviating the problems of previous solutions.

4. Summary

Bang-Bang PLL based CDR shows unique features of its input-dependent transfer function and steady-state limit cycle. The unique features results in the trade-off of loop bandwidth setup for jitter optimization and Jitter Tolerance improvement. Wide loop bandwidth setup introduces excessive wide bandwidth jitter while it demonstrates good tracking capability to eliminate phase-slewing. Narrow loop bandwidth experiences serious phase error due to inability of phase tracking although steady-state wide bandwidth jitter is highly suppressed. For loop bandwidth optimization, previously reported solutions suggest loop automatic loop bandwidth adjustment with digital or semi-digital implementation. Nevertheless, they present the limitations for high frequency jitter tolerance and high input data rate implementation.

CHAPTER III

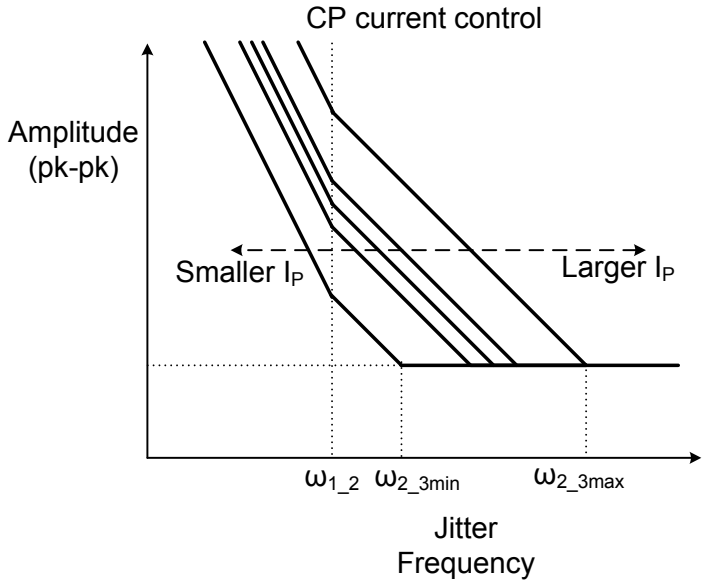
ADAPTIVE LOOP BANDWIDTH CLOCK AND DATA RECOVERY

1. Loop Bandwidth Adaptation

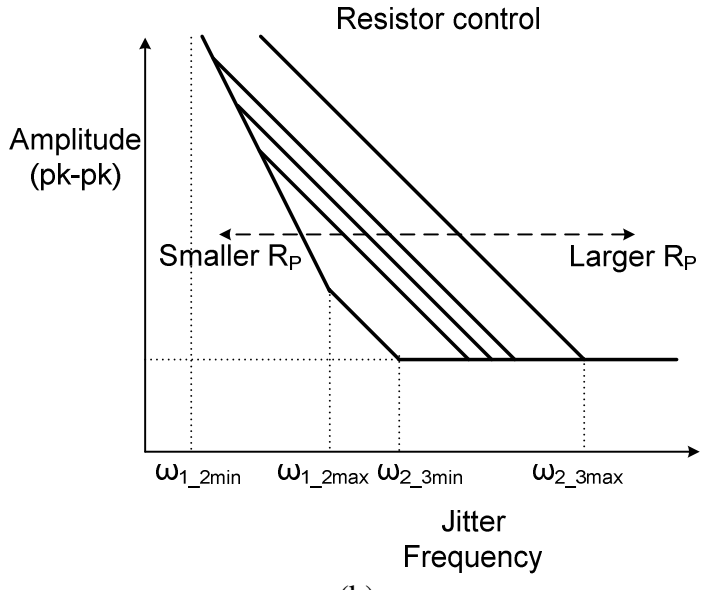
1.1. Loop Bandwidth Adjustment with Charge Pump Current Control

To control loop bandwidth, there exist three adjustable design parameters, CP current, loop filter resistor and VCO gain (KVCO) according to equation (2.3). The KVCO, however, is not an effective option in analog type PLL applications because of its inaccurate control. While CP current and loop filter resistor are likely to be constant, it is hard to maintain constant KVCO due to its non-linear characteristic and the PVT variation.

To compare the effect between CP current control and loop filter resistor control, the JTOL variations are illustrated in figure 3.1(a) and (b). Here, ω_{1_2} is the corner frequency between region I (-40dB/dec region) and region II (-20dB/dec regions) and ω_{2_3} is the corner frequency between region II and region III (flat regions). From equation (2.10) and (2.11), it can be seen that ω_{1_2} is inversely proportional to the resistance in contrast to linear correlation of the ω_{2_3} with resistance. On the other hand, the CP current control changes only ω_{2_3} proportionally while it maintains ω_{1_2} constant. Thus, as depicted in figure 3.1(a), the criteria of region I and II is never affected as region II can be extended or narrowed down by CP current control. Although both approaches control loop bandwidth accurately, in this thesis, CP current control strategy is suggested because of its superiority of the stability and circuit implementation.



(a)



(b)

Figure 3. 1 Jitter tolerance variation with (a) CP current control and (b) resistor control

Stability factor of 2nd order BBPLL is suggested by [21]. It is represented as the ratio of proportional phase gain and integral phase gain. Therefore:

$$\xi = \frac{P_{prop}}{P_{int}} = \frac{I_P R_P K_{VCO} T_{update}}{I_P K_{VCO} T^2{}_{update} / (2C_P)} = \frac{2R_P C_P}{T_{update}} \tag{3.10}$$

According to the equation, the stability factor is determined by the time constant of loop filter and loop updating time, T_{update}. Assuming constant loop delay and capacitance, the stability factor is only affected by loop filter resistance. Thus, resistor control results in time-variant stability factor. If loop bandwidth changes by eight times, the stability factor variation is also eight times. Unexpectedly decreased stability factor introduces additional timing error since it boosts peaking in the transfer function. To guarantee the stability in any loop bandwidth setup, loop filter capacitor will be much lager than conventional fixed loop bandwidth CDR. In contrast, CP current control realizes independent correlation between the stability factor and loop bandwidth variation. Since the CP current is not a relevant term of the stability factor in equation (3.10), the CP current control maintains constant stability factor regardless of loop bandwidth control range.

The analogy of conventional analysis on linear PLL helps shed light on the advantage of CP control. In linear PLL analysis, phase margin is the quantitative indicator of stability. In the 2nd order PLL, the phase margin is determined by the distance between zero (ω_z) and unit gain frequency[3] (ω_c). ω_z and ω_c are represented by:

[3] Note that unit gain frequency is equivalent to loop bandwidth as defined in chapter II.

$$\omega_z = \frac{1}{R_P C_P} \tag{3.11}$$

$$\omega_c = \frac{I_P R_P K_{VCO}}{2\pi} \tag{3.12}$$

Accordingly, the phase margin of 2nd order linear PLL will be shown as:

$$PM = \arctan\left(\frac{\omega_c}{\omega_z}\right) = \arctan\left(\frac{I_P R_P{}^2 C_P K_{VCO}}{2\pi}\right) \tag{3.13}$$

As can be seen in the equation (3.13), the distance between ω_z and ω_c varies linearly to the CP current variation while quadratically to the resistance variation. As a result, phase margin variation is well-controlled by CP current than resistor. It can be deduced, therefore, that CP current control provides superior stability control. Note that this analysis provides only indirect insight to understand the stability of BBCDR by using analogy of linear system. It may be inadequate to apply directly the linear system theory to the BBCDR.

The CP current control also provides advantage of circuit implementation. Generally, CP current control can be accomplished by adjusting tail current of CP. The abrupt glitches in changing loop bandwidth can be absorbed by parasitics on the path from the tail current to the loop filter. On the other hand, the resistor control brings potential problem in its implementation. One example of resistor control method is shown in figure 3.2 To control the resistance of the loop filter, switches need to be

turned on and off in connecting and disconnecting the parallel resistors. Since the source of current or charge glitches are directly connected to the loop filter without filtering, the control voltage of VCO will be very noise. In addition, large size of switches can cause additional phase error. The switch size should be large to minimize its resistance in order to control loop bandwidth accurately. However, induced by large sized switches, charge injection introduces the frequency offset then causes serious the phase error.

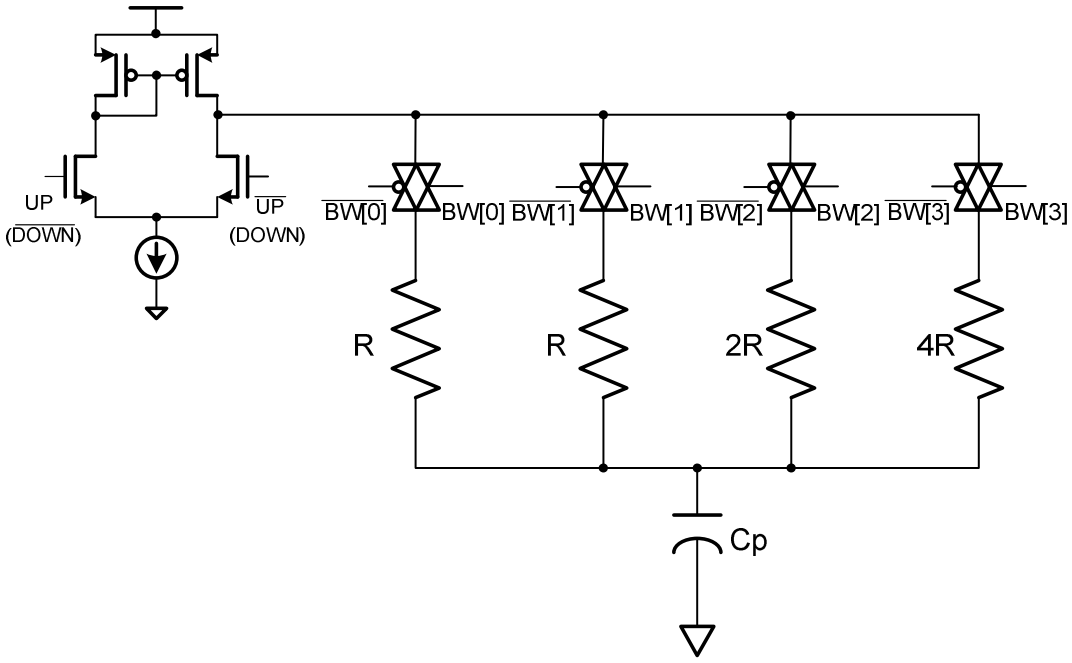


Figure 3. 2 The example of resistor controlled scheme

1.2. Prediction with Mixed Mode Piece-wise Integration

To optimize the loop bandwidth for >10Gb/s applications, a novel adaptive loop bandwidth BBCDR is proposed in this thesis. This technique employs a mixed mode piece-wise integration method.

The overall system is conceptually based on the adaptive delta modulator. As shown in figure 3.3, the loop bandwidth is adjusted according to the binary output information of BBPD as a one-bit quantizer. The predictor interprets the binary information and controls loop bandwidth to minimize timing error under the presence of input SJ, hunting jitter, RJ and ISI.

The predictor detects current jitter profile by integrating the PD output. The effect of the integration on CDR performance is based on two assumptions. First, the hunting jitter, RJ and ISI are wider bandwidth jitter than SJ. Second, the mean value of them is zero. To distinguish the power of wide bandwidth jitter from the phase-slewing, integration will be the solution because it filters most power of zero-mean value jitters. However, direct integration of phase error obtains only the power of phase-slewing jitter because the information of zero mean wide bandwidth jitter, $w(t)$, is vanished after integration time, t_0 as shown in equation (3.1).

$$\int_0^{t_0}[p(t)+w(t)]dt = \int_0^{t_0} p(t)dt + \int_0^{t_0} w(t)dt \cong \int_0^{t_0} p(t)dt \qquad (t_0 >> \tau_w) \tag{3.1}$$

where $p(t)$ is the timing jitter from phase-slewing. The parameter, τ_w, is the inverse of the bandwidth of $w(t)$. To optimize the loop bandwidth, however, the relative power between $p(t)$ and $w(t)$ is more useful information.

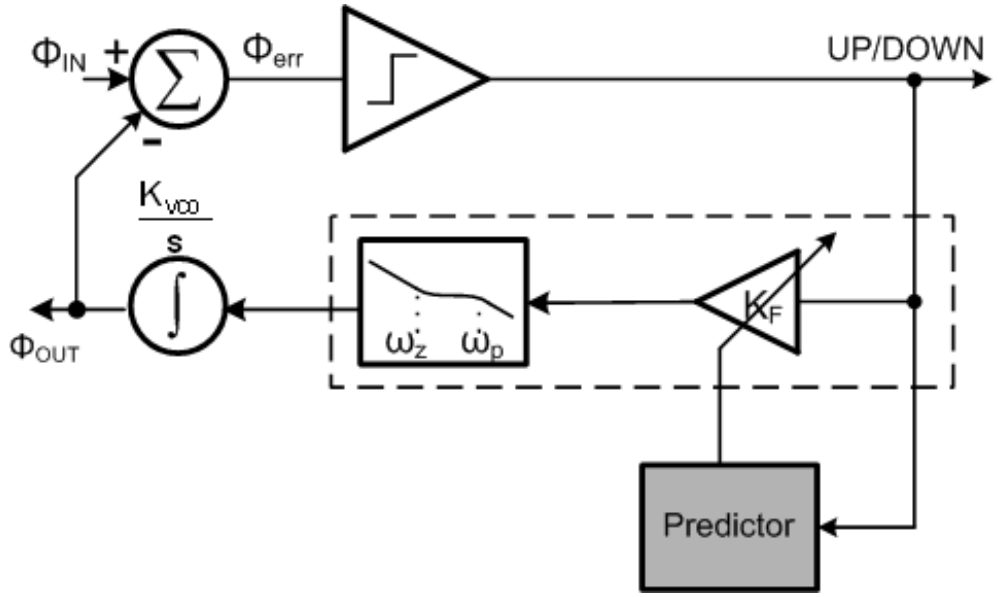


Figure 3. 3 The conceptual diagram of adaptive delta-sigma modulator

If BBPD precedes the integrator, the integrator output will reflect the relative power between phase-slewing jitter and wide bandwidth jitters. As the wide bandwidth jitter becomes more dominant than phase slewing, the averaged value of integrator will decrease. The averaged output will increase for dominant phase slewing as shown in figure 3.4. The equation (3.2) describes it as:

$$\int_0^{t_0} q[p(t)+w(t)]dt \cong \begin{Bmatrix} \int_0^{t_0} q(p(t))dt \cong t_0 \text{ or } -t_0, & (\sigma_p >> \sigma_w) \\ \int_0^{t_0} q(w(t))dt \cong 0, & (\sigma_p << \sigma_w) \end{Bmatrix} \quad (\tau_p >> t_0 >> \tau_w) \qquad (3.2)$$

Here, σ_p and σ_w are power of phase-slewing and wide bandwidth jitter, respectively. The parameter, τ_w and τ_p are the inverse of the bandwidth of $w(t)$ and $p(t)$, respectively.

$q(x)$ is the quantization function as represented in following equation (3.3).

$$q(x)=\begin{Bmatrix}+1, & (x>0)\\ 0, & (x=0)\\ -1 & (x<0)\end{Bmatrix} \tag{3.3}$$

Basically, the information of BBPD output is already integrated in the capacitor of the loop filter. However, it is hard to detect the instantaneous input phase and frequency variation from the voltage of that capacitor. The reason is because the voltage variation is very small in a short period due to the large capacitance value. Also, the voltage across the capacitor is not instantaneous but long term frequency information.

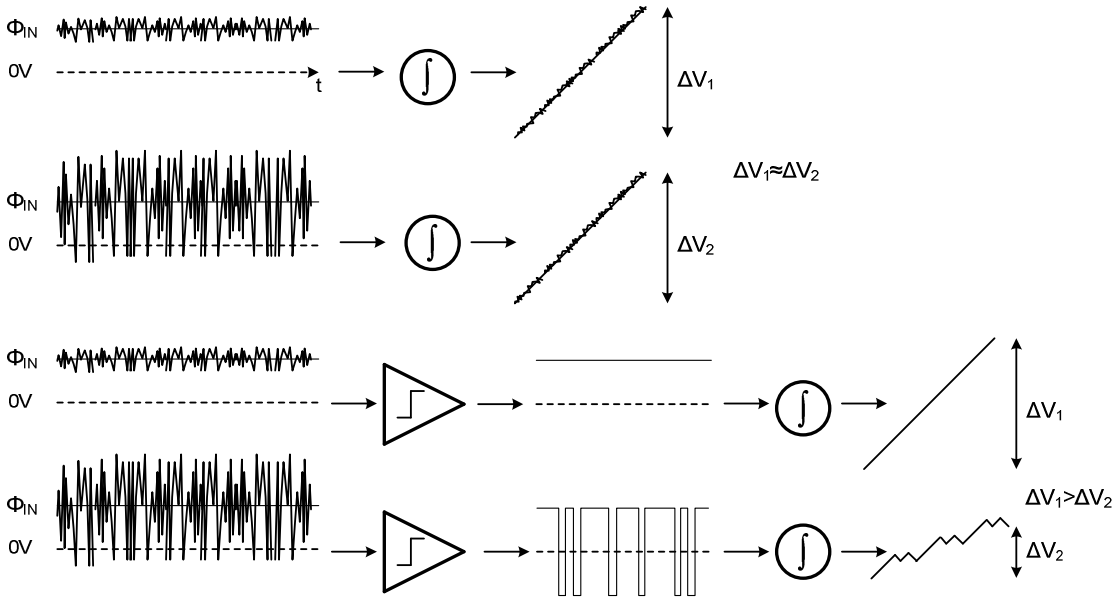


Figure 3. 4 The effect of BBPD on the integration

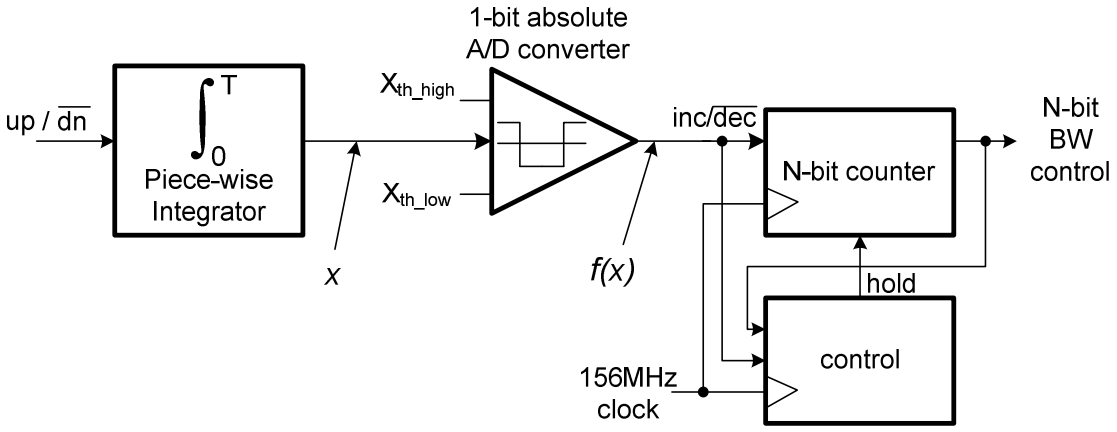


Figure 3. 5 The conceptual diagram of the predictor

Thus, short period piece-wise integration will be the appropriate solution to detect the instantaneous input frequency variation.

A novel predictor shown in figure 3.5 with mixed mode piece-wise integration is proposed. The analog front-end integrates binary output of BBPD, followed by one-bit absolute analog-to-digital (A/D) conversion. The output of absolute A/D conversion determines the increment or decrement of the loop bandwidth. The A/D conversion refers the absolute value of integrator output. For example, if either ‘up’ or ‘down’ is dominant than the other during the integration, the loop bandwidth will increase. Loop bandwidth will decrease if the numbers of ‘up’ and ‘down’ are comparable. Therefore, loop bandwidth should be increase (decrease) when the absolute value of average PD output is larger (smaller) than the threshold point. The absolute A/D conversion can be described as equation (3.4).

$$f(x)=\begin{cases}1, & \left(x \geq X_{th\_high} \;\; or \;\; x < X_{th\_low}\right) \\ 0 & \left(X_{th\_high} > x > X_{th\_low}\right)\end{cases} \tag{3.4}$$

Here, X_{th_high} and X_{th_low} are the upper and lower threshold points. From (3.2) to (3.4), it can be described how to decide the increment / decrement of loop bandwidth from the PD output as shown in equation (3.5).

$$\begin{aligned} & f\left[\alpha\int_0^{t_0} q[p(t)+w(t)]dt+\beta\right] \\ & \cong \begin{cases} f\left[\alpha\int_0^{t_0} q(p(t))dt+\beta\right] \cong f(\alpha t_0+\beta) \;\; or \;\; f(-\alpha t_0+\beta)=1 & \left(\sigma_p >> \sigma_w\right) \\ f\left[\alpha\int_0^{t_0} q(w(t))dt+\beta\right] \cong f(\beta)=0 & \left(\sigma_p << \sigma_w\right) \end{cases} \end{aligned} \tag{3.5}$$

where α and β are fitting factors for practical implementation. β must be selected between X_{th_high} and X_{th_low}. After absolute A/D conversion, a fully digital controller generates the loop bandwidth control signals according to the current and previous increment / decrement output of absolute A/D converter.

The proposed predictor brings apparent advantages compared to the previous solutions. First of all, current mode analog integrator relieves speed limitation. For 10Gb/s input data rate, the digital integrator should operate around 1GHz clock to maintain de-serialized ratio of 1:10. This requires high f_t technology or power hungry CML implementation. On the other hand, current mode analog integrator does not require high f_t. It leads significantly low power consumption for the integration. Second,

this approach maintains high speed loop bandwidth updating rate. The loop bandwidth updating rate is significant for the high frequency input SJ. As shown in figure 3.6, if the rate is quite slower, the updated loop is not valid because it is based on the past information. As afore-mentioned, previous solution [24] takes 320bits for the integration due to the speed limitation of loop filter. On the other hand, the proposed mixed-mode integration takes only 32 bits to update the loop bandwidth since analog loop filter does not involve decimation. Third, the proposed solution still takes advantage of the versatility of digital control. The information is processed in digital after the absolute A/D conversion. Since the required clock frequency of controller is moderate (from 166MHz to 333MHz for 30 to 60 cycle integration), it is possible to implement the required digital logic in 0.18um CMOS technology. Therefore, it can provide the design flexibility to realize various digital control schemes.

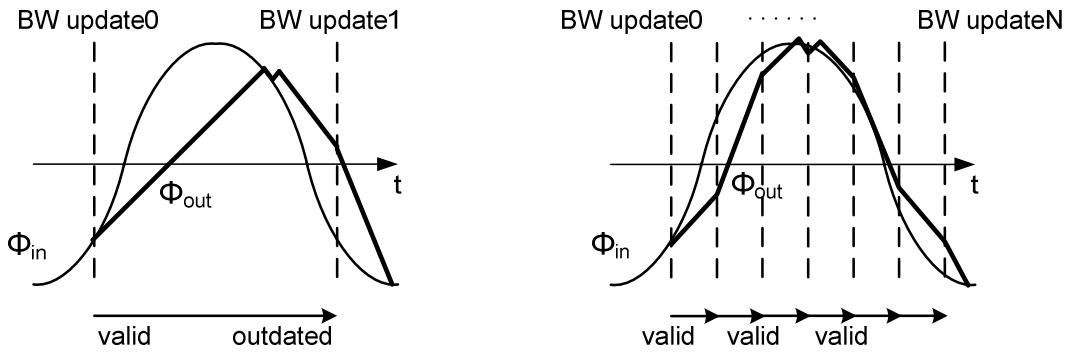


Figure 3. 6 The effect of loop bandwidth updating rate

2. System Overview

The overview of system diagram is shown in figure 3.7. The architecture is based on 3rd order BBPLL. Since the parallel capacitor (C_{P2}) is relatively smaller than series capacitor (C_{P1}), analysis of 2nd order BBPLL model is still valid. Combined with predictor, the BBPLL performs adaptive delta modulation.

As discussed so far, the predictor is connected in parallel to the signal path from BBPD to CP. From the PD output, it detects jitter profile and updates the loop bandwidth by controlling CP current. The digital controller inside predictor is operating at 156MHz. This clock can be easily provided by sharing the frequency divider output in DeSerializer[4].

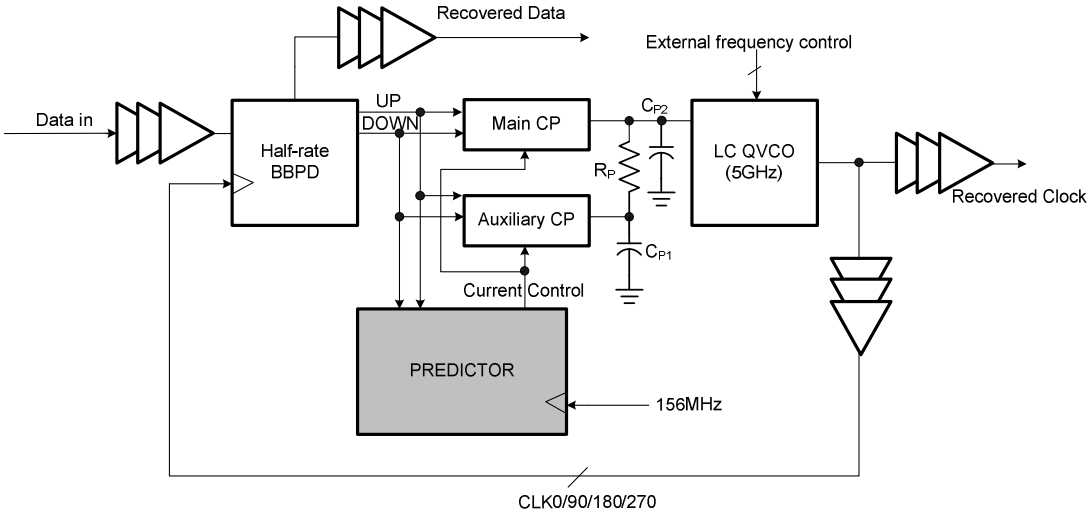


Figure 3. 7 The architecture of proposed adaptive loop bandwidth BBCDR

[4] It is out of the scope in this thesis

The proposed architecture adopts half-rate BBPD for the power and speed issue. For the 10Gb/s application, the full rate PD requires D flip flops updating the input data to the output within 100ps that requires significant power consumption. Moreover, with low f_t technology it may not be possible to realize full-rate operation even with high power consumption. Therefore, the half-rate structure relieves the speed and power requirement even with limited f_t technologies.

Dual variable CP is employed to realize the loop bandwidth control as well as a capacitor multiplication technique for on-chip integration. The current of CP is adjusted by three-bit digital control signal from the predictor. Dual CP structure provides the capacitor multiplication. The capacitor multiplication factor determines the current ratio of main and auxiliary CP. With the capacitor multiplication, required capacitor is reduced from one nF to 250pF in 200x200um^2, which is on-chip implementable value.

Although out of the scope of this thesis, the effect of VCO needs to be considered thoroughly. The phase noise of VCO is especially critical issue in proposed solution. The proposed solution changes the loop bandwidth in real-time. If the loop bandwidth is set to the minimum, the phase noise of VCO may be magnified by the loop and accordingly the output jitter will be increased. Therefore, quadrature LC type VCO is regarded as the possible structure since its phase noise performance is superior than ring VCO. The behavioral model is built based on [25-27] and, for the verification, simulation has been performed with reasonable phase noise specification of typical LC VCO.

3. Predictor Design

As shown in figure 3.8, the predictor consists of a charge pump, a switched capacitor network, absolute A/D converter and digital logic circuitry. Note that charge pump in the predictor is different components from the one connected to loop filter. This integrating charge pump (ICP) performs the mixed mode piece-wise integration with switched capacitor. The ICP generates the current corresponding to the BBPD output. The generated current will be integrated by the capacitor. In order to perform *piece-wise* integration, the charge on the capacitor should be reset periodically, otherwise, the past information will affect the future loop bandwidth decision because charge remains in the capacitor.

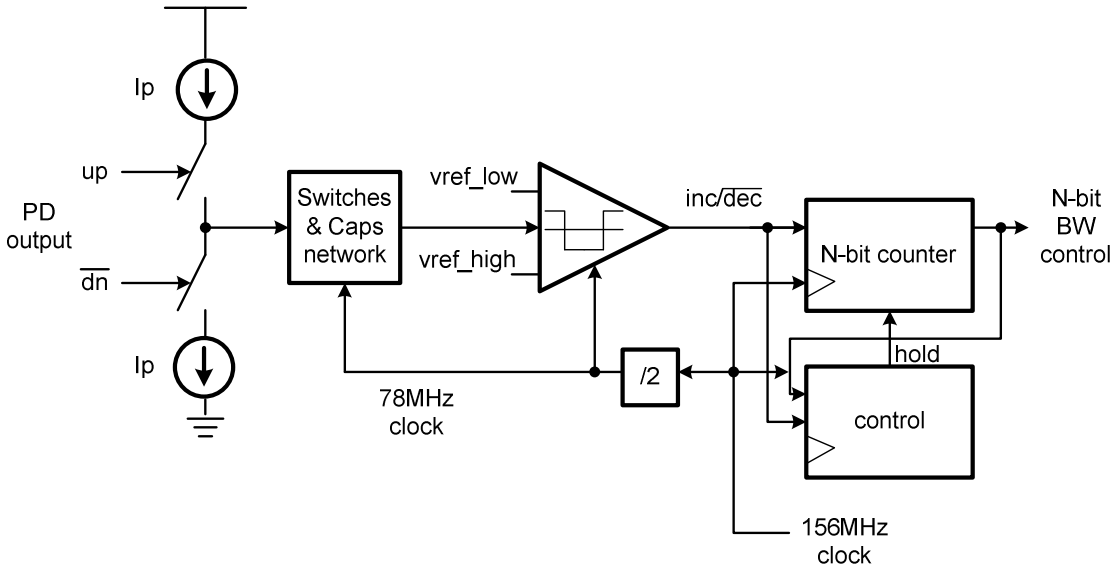


Figure 3. 8 The architecture of the predictor

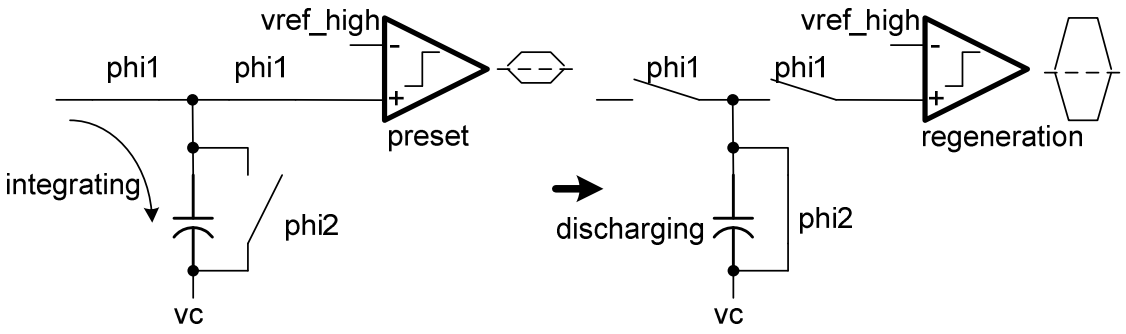


Figure 3. 9 Piece-wise integration with switched capacitor network

The operation is illustrated in figure 3.9 in detail. While the phi1 is on, the ICP current is integrated into the capacitor. When there is a transition of clock (from phi1 to phi2), integrated information is dumped to the A/D conversion stage. Now, while the phi2 is on, the capacitor starts being discharged by turning on the switch across the capacitor while the information of PD output is decoupled with the capacitor. This implies that loop bandwidth is evaluated during phi1 only. To make the system more efficient, dual path integration is required. One ICP and two switched capacitor network operates with complementary clock cycle. One path integrates PD output into the first capacitor while another path discharges the second capacitor. The dual path structure provides better jitter performance because it enables continuous adaptation.

The schematic of analog front end is illustrated in figure 3.10. A differential pair is employed to implement ICP. The switched capacitor network is composed of three CMOS transmission gate and one capacitor. In order to perform effective integration, the output pole of ICP is required to be far below than loop updating frequency because the most current of ICP needs to be injected to the capacitor without loss of charge by

parallel resistance. Therefore, the output resistance of ICP should be much higher than the impedance of capacitor at the loop bandwidth updating frequency rate as:.

$$r_{dsp} \,//\, r_{dsn} >> \frac{1}{2\pi f_{loop\_update} C_C} \tag{3.6}$$

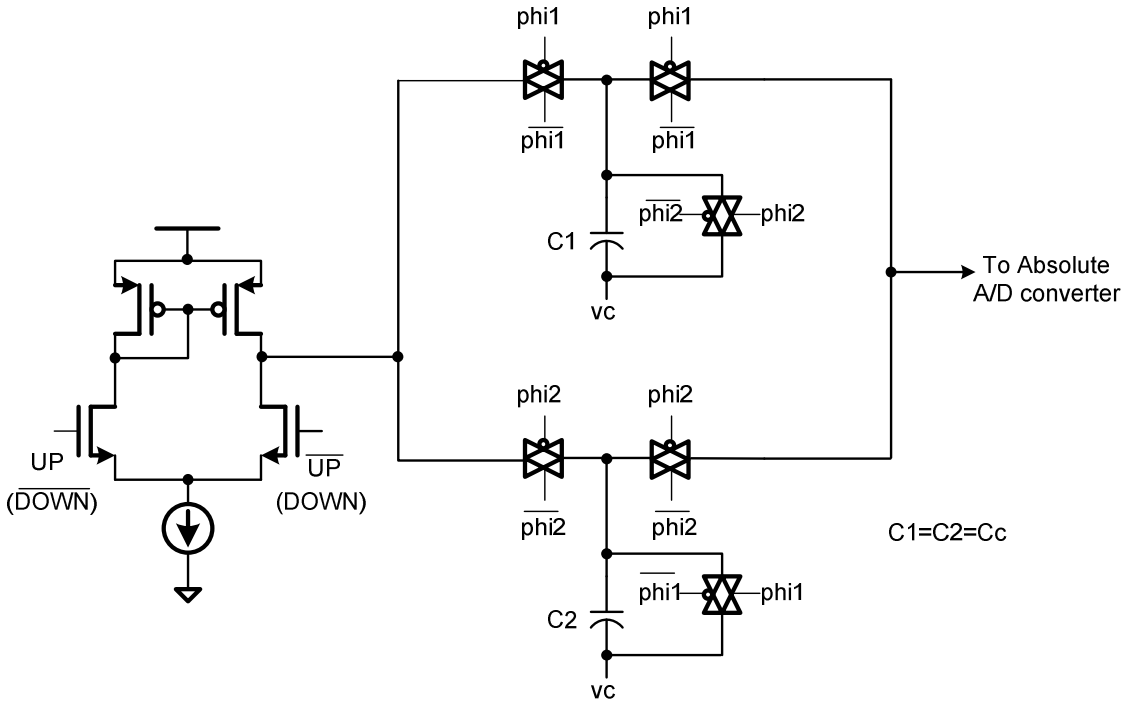


Figure 3. 10 The schematic of analog front end of piece-wise integrator

where r_{dsp} and r_{dsn} denote small signal resistance of PMOS and NMOS, respectively. C_C is the capacitance of piece-wise integrator. f_{loop_update} is the updating frequency of loop bandwidth control. The effect of switch resistance is neglected in equation (3.6).

For a complete analysis, the effect of switch resistance needs to be considered because the size of switch may affect the performance of integrator. To hold the equation (3.6) valid, the parallel resistance of switch should be smaller than the impedance of capacitor. Thus, the following relations will hold as:

$$r_{on} << \frac{1}{2\pi f_{loop\_update} C_C} \tag{3.7}$$

$$\alpha_n \frac{W_n}{L}(V_{DD} - V_O - V_{tn}) + \alpha_p \frac{W_p}{L}(V_O - V_{tp}) >> 2\pi f_{update} C_C \tag{3.8}$$

where $\alpha_n = \mu_n C_{ox}$ and $\alpha_p = \mu_p C_{ox}$, respectively. V_O is the output voltage of the integrator, and V_{tn} and V_{tp} are the threshold voltage of NMOS and PMOS, respectively. According to (3.8), the large transistor width is desirable to reduce the switch resistance. In practice, however, the switch size is limited by non-ideal effects such as charge injection and clock feed-through. The size of transistor is required to be optimized to minimize the effects while the equation (3.8) still holds. Although both conditions can be satisfied with the large Cc, it requires extra silicon area. Moreover, the voltage difference on large Cc will be too small to be detected after the integration.

The analog front end is followed by the one-bit absolute A/D converter. Composed of comparators and combinational digital logic, the absolute A/D converter samples the integrator output and regenerates it to digital domain for the versatility of digital controller.

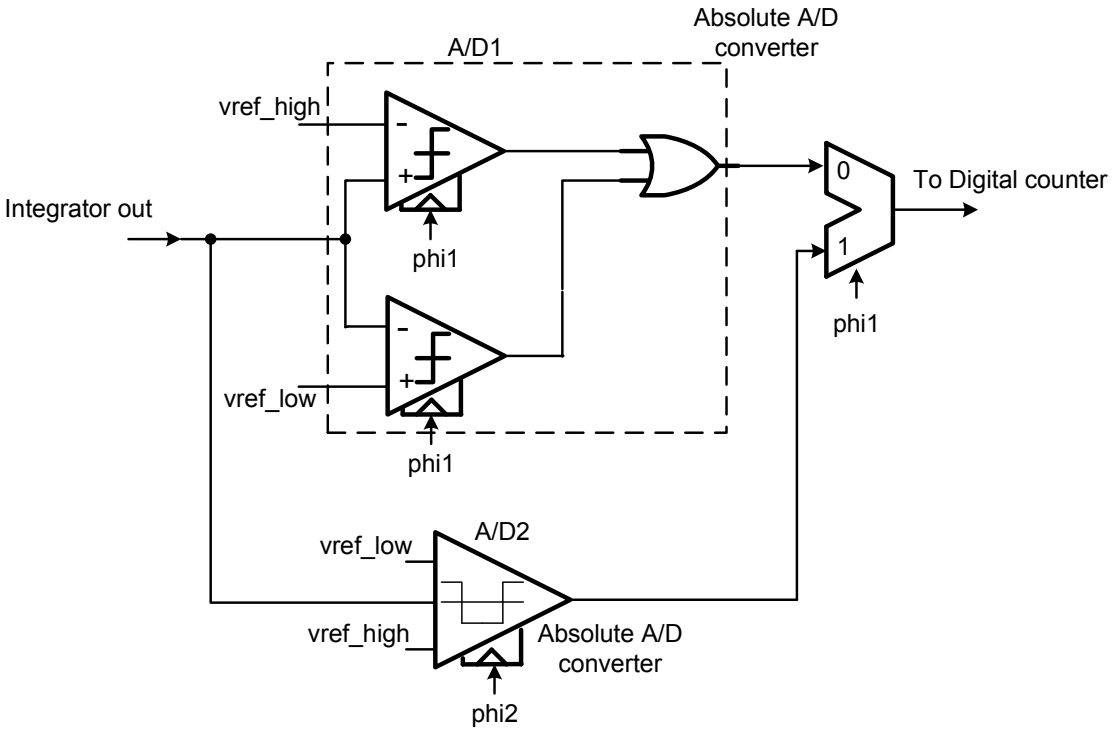


Figure 3. 11 The architecture of absolute A/D converter

The schematic of the converter is shown in figure 3.11 with preceding output of integrator. Two converters are implemented for both paths integrator outputs. Each converter returns its output in complementary phases. By multiplexing the two outputs, the predictor can provide the information to digital controller continuously. The detailed timing dynamics are depicted in figure 3.12.

Each A/D converter consists of two comparators with different threshold point. If the final integrator output either exceeds the high threshold or goes the below low threshold, either of comparators regenerates output to VDD. By or-gating the two comparator outputs, the absolute A/D conversion defined in equation (3.4) is realized.

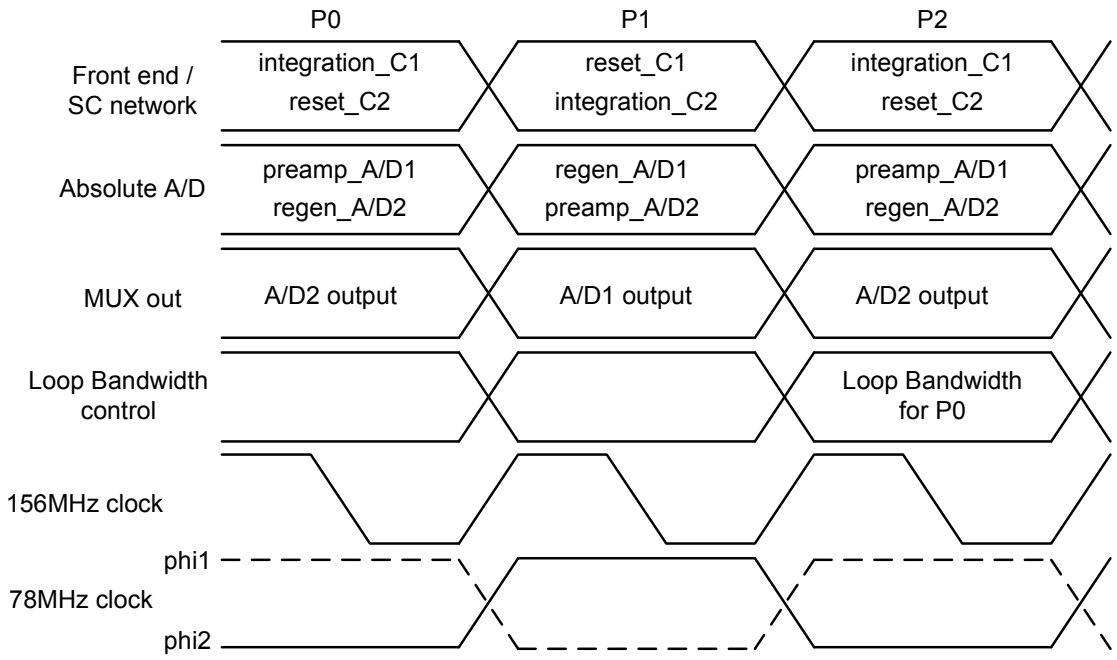


Figure 3. 12 The timing diagram of the predictor operation

As shown in figure 3.13, static type comparator is implemented using a high sensitivity stage and rail-to-rail output. The output of the switched capacitor circuit may exhibit voltage around the threshold points if the wide bandwidth jitter is comparable to jitter by phase-slewing. High input sensitivity reduces the ambiguity of loop adjustment decision for the small input offset. Not limited by bias current, the pseudo differential topology regenerates output fast. The comparator is followed by minimum size inverters to help the output driving capability. Dummy inverters are added to match load condition of differential output.

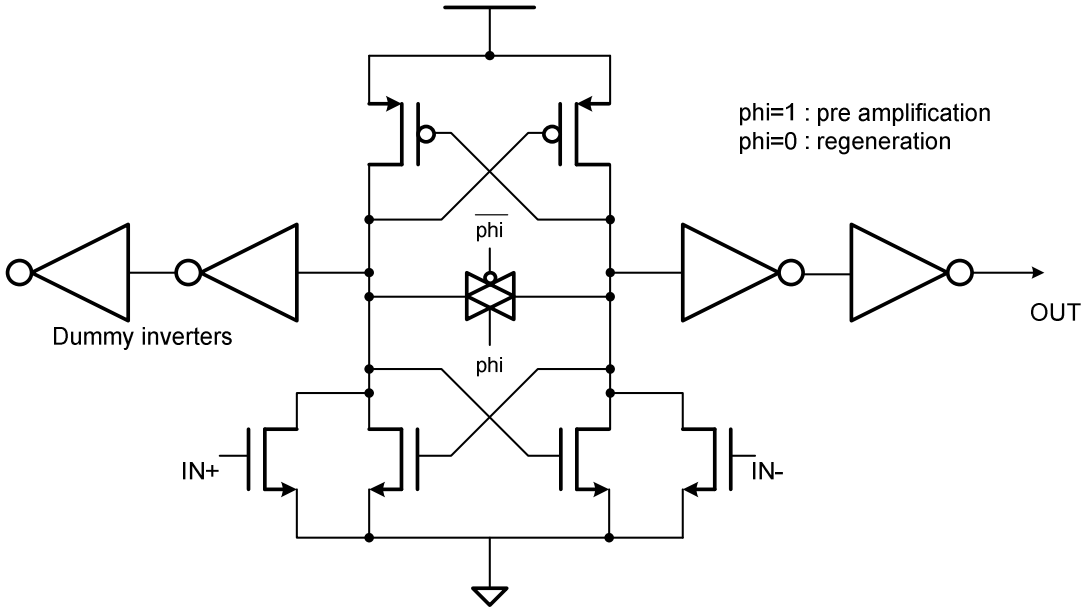


Figure 3. 13 The comparator schematic of A/D converter

The absolute A/D converter returns high for the phase-slewing dominant jitter profile and returns low for the RJ and ISI dominant jitter.

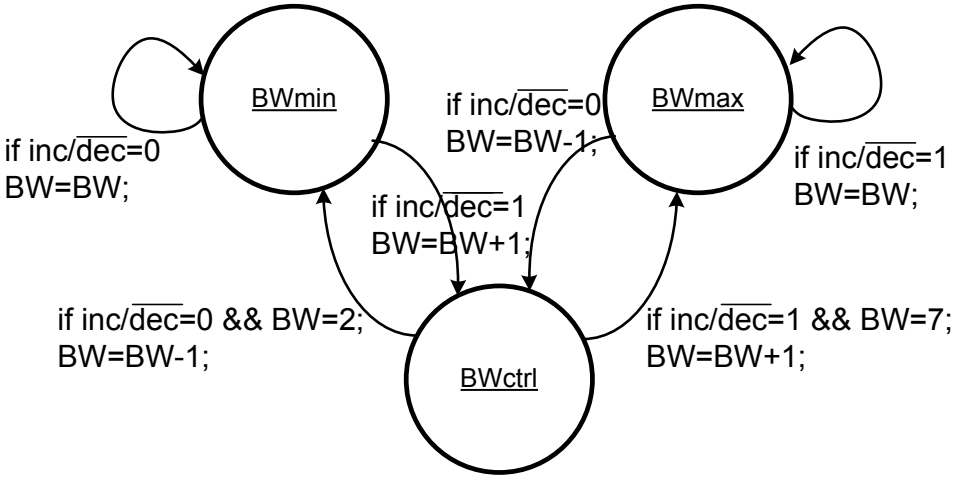


Figure 3. 14 The state diagram of digital counter

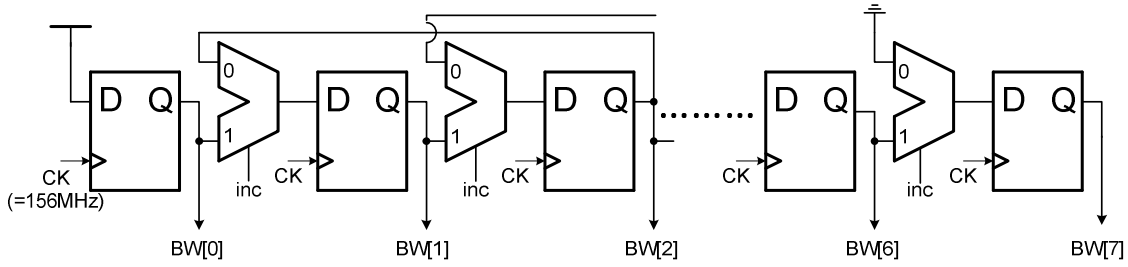


Figure 3. 15 The implementation of bi-directional shift registers for digital counter

According to this, the digital controller adjusts the loop bandwidth. As the bi-directional counter, the digital controller increases one step of loop bandwidth if the converter output is high. It also decreases one step if output is low. Once the loop bandwidth reaches to the maximum (or minimum) setup, the controller maintains the maximum (or minimum) loop bandwidth code until the decrement (or increment) is requested by the A/D converter. The loop bandwidth ranges from one to eight times the basic loop bandwidth. The state diagram of the digital controller is illustrated in figure 3.14. In this work, the digital controller is described with behavioral model for the simulation. One possible implementation is suggested in figure 3.15. Eight bit bi-directional shift register provides control signal to tune the loop bandwidth by a factor of eight. Only eight D flip flop and eight MUXes are required for the implementation.

In order to realize immediate loop bandwidth update, it is still required to minimize the critical delay from the analog front end to the input of digital controller. The updating procedure of predictor may not be accomplished within one clock period due to the excessive delay of comparator and logic. If additional clock cycles are

required to complete the process, consequent latency of updating loop bandwidth results in outdated loop bandwidth setup for the input jitter profile as shown in figure 3.16. It potentially leads degradation on loop bandwidth optimization. The timing requirement, therefore, needs to guarantee the instantaneous loop bandwidth update. To update the loop bandwidth within one clock cycle, the following timing condition must be satisfied.

$$T_{clk} > t_{comp} + 2 \quad t_{inv} + t_{or} + t_{mux\_AD} + t_{mux\_ctrl} + t_{setup} \tag{3.9}$$

where T_{clk} is the predictor clock period (6.4ns for 156MHz). t_{comp}, t_{inv}, t_{or} and t_{mux_AD} are the time delay of comparator, inverter and MUX, respectively. t_{mux_ctrl} is the delay of MUX in digital counter and t_{setup} is the setup time of D flip-flop. Regarding the trade-off between dynamic power and speed, all dimensions of comparators and logic gates need to be carefully determined.

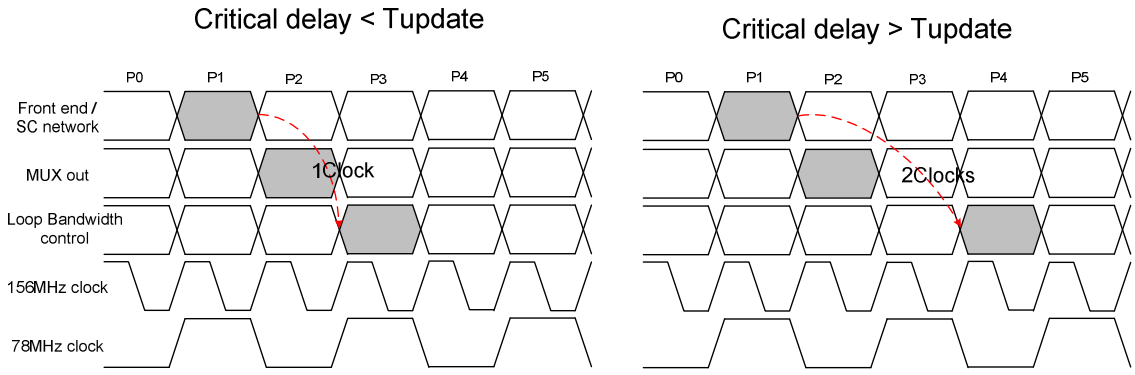


Figure 3. 16 The effect of logic delay on the loop bandwidth updating time

4. Dual Variable Charge Pump Design

Shown in Figure 3.17 is the implementation of the variable CP using multiple differential pairs connected in parallel and sharing their outputs. Each differential pair is turned on and off as the loop bandwidth is increased and decreased. The BBPD output generates a relatively small output swing (typically 400-600mV single-ended) due to its CML implementation. Even if small input swing is generated, the differential pair with small over-driven voltage can steer the current completely in the proper direction.

Two parallel CP examples are illustrated in figure 3.17 for a) binary code control and b) thermo-meter code control. The binary code CP presents the superiority for device mismatch while it brings large instantaneous current variation at the transition of loop bandwidth change. The thermo-meter code CP introduces larger current offset although it accurately controls the loop bandwidth.

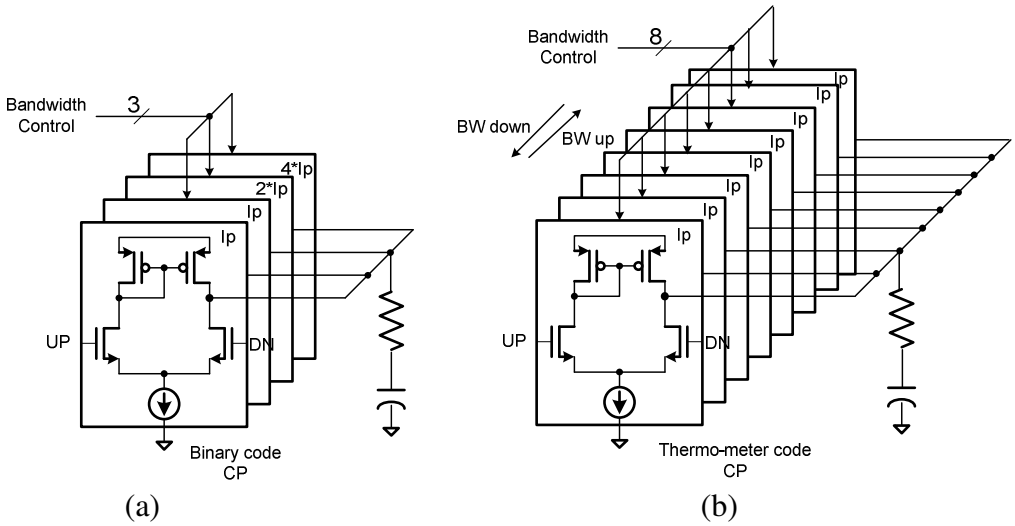


Figure 3. 17 Implementations of variable current charge pump (a) binary control and (b) thermo-meter control

The practical system design should consider some factors. In the presence of the parasitic pole, the current mirror generates asymmetric up and down pumping current. To minimize the asymmetry effect on the loop characteristics, the parasitic pole frequency should be far beyond the 2nd pole of the CDR. Therefore, the following condition should be maintained.

$$\omega_P = \frac{gm}{2C_{gs}} = \frac{\mu_p C_{ox} \frac{W}{L} v_{DSAT}}{2WLC_{ox}} = \frac{\mu_p v_{DSAT}}{2L^2} > 2\pi \cdot 10^9 >> \frac{1}{R_P C_{P2}} \tag{3.14}$$

Thus, where *gm* and C_{gs} are the transconductance and gate-source capacitance of PMOS current mirror, the large over-driven voltage (v_{DSAT}) and short channel length are required to minimize parasitic pole. However, large over-driven voltage reduces the VCO control voltage range, and finite output resistance of short channel length causes large current leakage of loop filter. Therefore, over-driven voltage and channel length of current mirror need to be carefully evaluated to minimize afore-mentioned trade-offs.

The loop filter capacitor is likely to be implemented off-chip due to the requirement of large time constant. Off-chip implementation introduces additional noise by exposing the control voltage to external components. On-chip implementation with capacitance multiplication solves the issue. Capacitor multiplication technique reduces physical value of capacitor while maintaining its large effective capacitance by using active elements. To realize the technique in CDR applications, it should maintain the functionality even at high frequency operation. Moreover, the additional input

capacitance needs to be minimized for the loading effect to PD. To satisfy the afore-mentioned requirements, the technique reported in [28] is adopted.

The conceptual diagram is shown in figure 3.18. The main CP injects (extracts) the current into the resistor while an auxiliary CP extracts (injects) current partially to reduce current injection to the capacitor. If the physical capacitance is C_{P1} and the current ratio of main and auxiliary CP is α, the effective capacitance, C_{Peff}, can be calculated as:

$$P_{int} = \frac{I_P K_{VCO}}{2C_{Peff}} T^2{}_{update} = \frac{(I_P - \alpha I_P) K_{VCO}}{2C_{P1}} T^2{}_{update}$$

$$C_{Peff} = \frac{C_{P1}}{1 - \alpha} = mC_P \qquad (3.15)$$

$$C_{P1} = (1 - \alpha) C_{Peff}$$

The required physical capacitor, C_{P1}, therefore, can be significantly reduced by $(1- \alpha)^{-1}$ times of the effective capacitance. Additional input loading is not serious since the size of the auxiliary CP is smaller than or comparable to the main CP. The technique, however, is limited to acquire very high multiplication factor because of device mismatch issues. The maximum multiplication factor variation is computed in equation (3.16) with the current mismatch of main and auxiliary CP, denoted as ΔI_P and $\alpha \Delta I_P$, respectively.

$$P_{\text{int}} = \frac{(I_P \pm \Delta I_P)K_{VCO}}{2C_{Peff}} t^2{}_{update} = \frac{\{(I_P \pm \Delta I_P) - \alpha(I_P \mp \Delta I_P)\}K_{VCO}}{2C_P} t^2{}_{update}$$

$$C_{Peff} = \frac{C_P(I_P \pm \Delta I_P)}{(1-\alpha)I_P \pm (1+\alpha)\Delta I_P} = \left[\frac{1}{1-\alpha} - \frac{\pm 2\alpha\Delta I_P}{(1-\alpha)\{(I_P \pm \Delta I_P)(1-\alpha) \pm 2\alpha\Delta I_P\}}\right] C_P \qquad (3.16)$$
$$= (m + \Delta m)C_P$$

$$C_P = \frac{1}{m + \Delta m} C_{Peff}$$

As can be seen in (3.16), the error in the multiplication factor, Δm, is an incremental function in terms of α (0<α<1). For higher multiplication factor (a ≈1), it will risk significant variation of loop characteristics due to the deviation of multiplication factor.

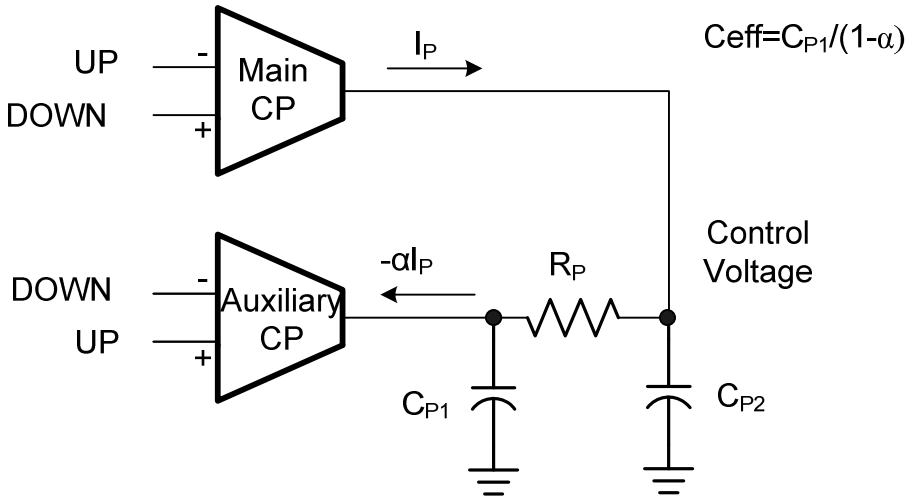


Figure 3. 18 Capacitor multiplication in high speed application [28]

In this work, a capacitance multiplication factor of four is realized with $\alpha = 0.75$. In the presence of 3% current mismatch, the effective capacitance exhibits +23% / -15% deviations from the nominal value. This variation is still tolerable if the stability factor is initially set to have a little margin to minimize noise peaking.

5. Half-rate Phase Detector Design

For the >10Gb/s applications, it is stringent to satisfy the speed requirement of D flip-flop as sample-and-regenerate functions must be accomplished in 100ps. Due to the speed requirement, 10GHz operation D flip flop is hardly reported in >0.18um technology.

To increase the f_t in a given technology, each transistor should hold large over-driven voltage to increase gm/C_{gs} as implied in equation (3.14). The low supply voltage, however, limits the over-driven voltage of each transistor that f_t may not reach the required frequency. [29] reports class AB type D-flip flop without tail current in order to increase driving capability. However, the abrupt dynamic current induces large supply noise associated with the bond-wire inductance. For high speed phase detection with limited f_t, the half-rate PD has been suggested in previous works [30-32]. Among the many proposed structures, topology of [33] is employed in this thesis. This topology can be implemented with less number of logic gates than others. It also provides balanced load condition to I/Q clock sources that I/Q mismatch can be minimized.

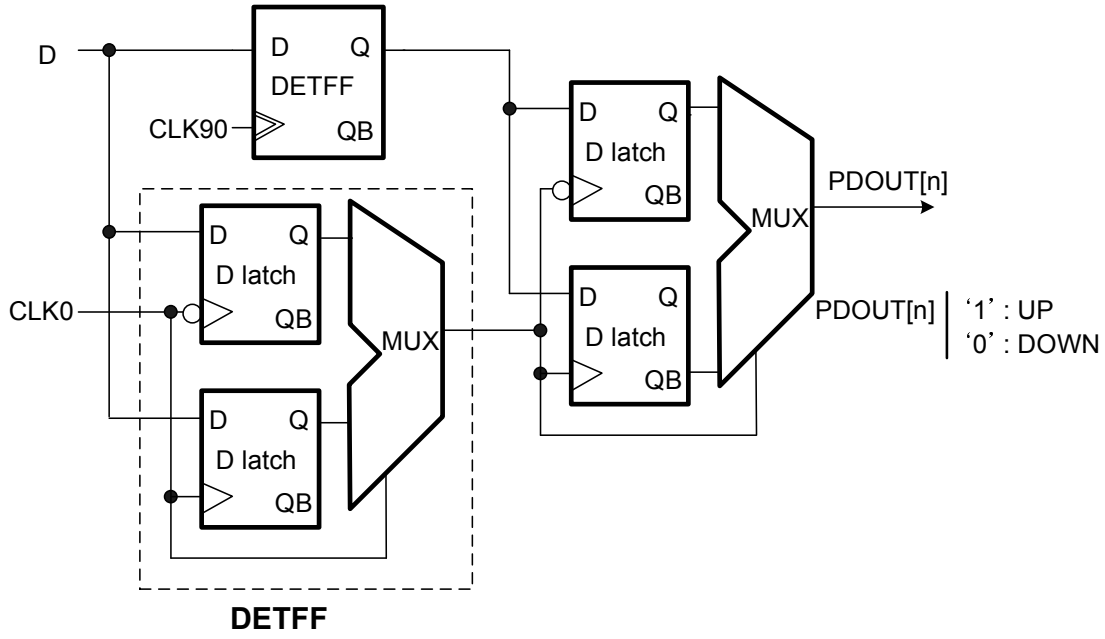


Figure 3. 19 A half-rate Bang-Bang phase detector in [33]

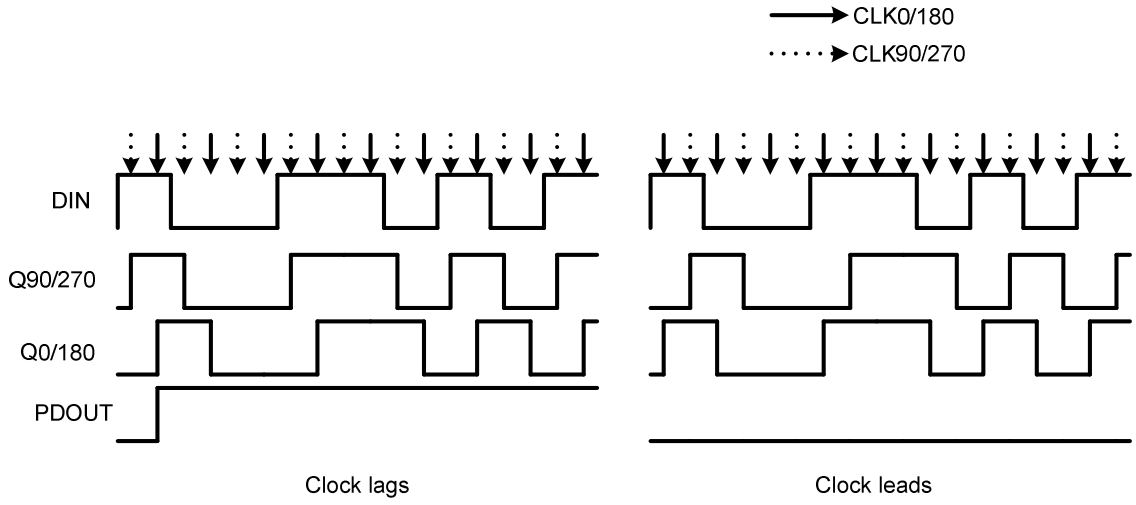


Figure 3. 20 The timing diagram of the half-rate BBPD

The architecture is shown in figure 3.19. The PD is composed of three dual-edge-triggered D flip flops (DETFF), and each DETFF consists of two D latches and one multiplexer. The timing diagram is shown in figure 3.20 to detail the dynamics of the PD.

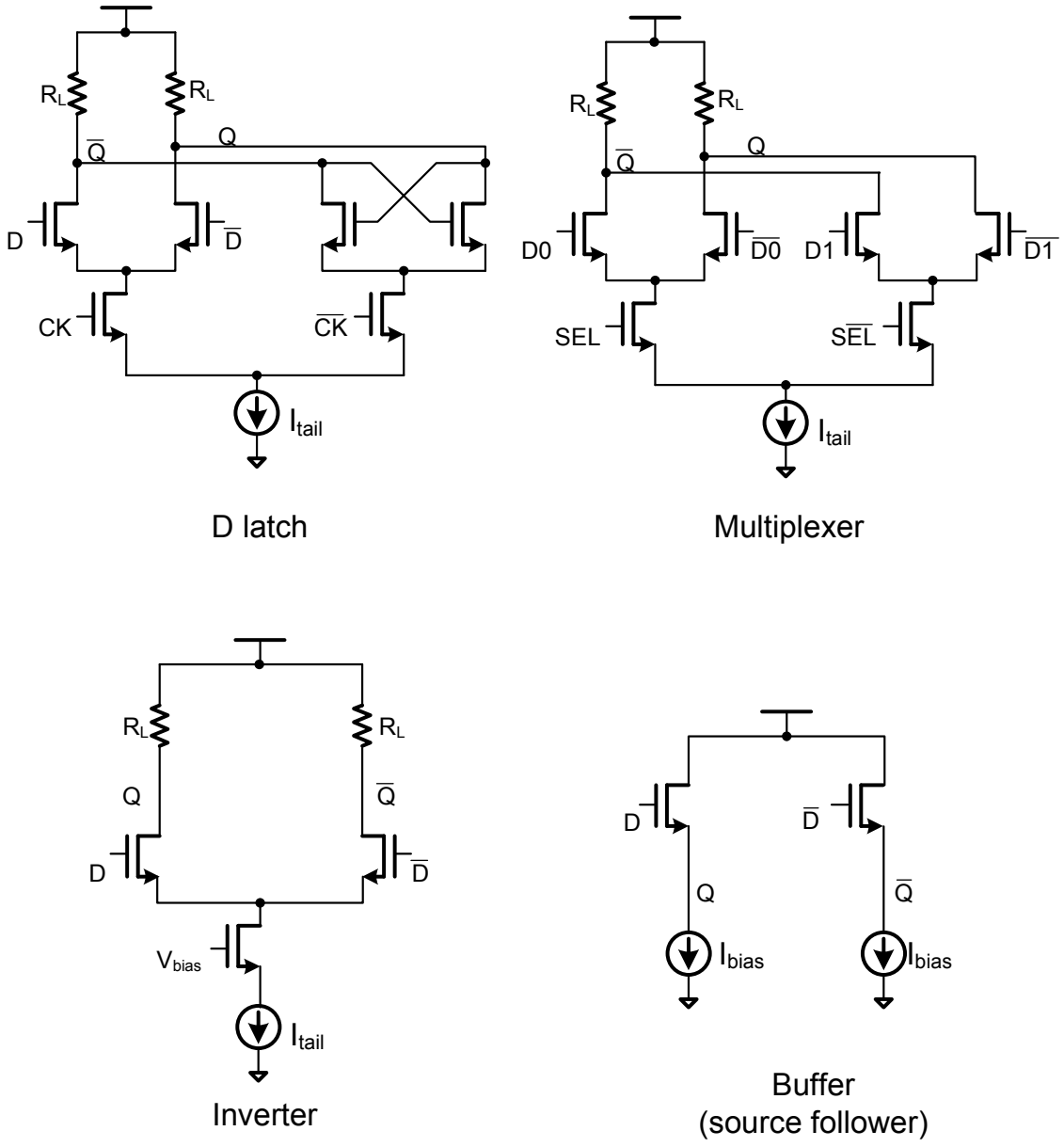


Figure 3. 21 Current mode logic family for the BBPD

The logic circuits of the BBPD are implemented using CML logic. Figure 3.21 shows the schematics of the logic family used for the BBPD. The circuit parameters of CML logic are determined by the following procedure. First, the ratio of input swing and over-driven voltage should be selected. Unlike the typical amplifier, the CML should steer the tail current through one branch completely. Thus, the input swing is forced to be more than several times over-driven voltage, V_{dsat}, as shown in equation (3.17).

$$V_{swing\_single} \geq \alpha V_{dsat} \tag{3.17}$$

The parameter α can be decided from the simple simulation. Excessively large value consumes power inefficiently while too small number fails to steer the tail current completely. Second, over-driven voltage, device type and size are determined by the speed requirement. Before a detailed analysis, note that signal swing, tail current (I_{tail}), and load resistor (R_L) follows the equation (3.18) if the circuit reaches steady state.

$$\begin{aligned} V_{swing\_single} &= I_{tail} R_L \\ V_{swing\_diff} &= 2 \cdot I_{tail} R_L \end{aligned} \tag{3.18}$$

where V_{swing_single} and V_{swing_diff} are single-ended and differential swing, respectively. Also note that the logic circuits should drive larger load capacitance than its input capacitance within the bit period, which suggests that the fan-out should be larger than one.

Otherwise, signal cannot be driven to larger load by the buffers or inverters. In particular, the latch will fail to function because it inherently has one fan-out due to cross-coupled structure as shown in figure 3.21. To drive the fan-out *N*, the RC time constant should be smaller than the inverse of maximum input frequency as (3.19).

$$\begin{aligned} R_L C_L &= N R_L C_{gs} = N R_L (W L C_{ox}) \\ &= \frac{2 N R_L I_{tail} L^2}{\mu_n \cdot V^2{}_{dsat}} < \frac{1}{2\pi f_{in}} \end{aligned} \tag{3.19}$$

Here, f_{in} is the maximum frequency of input data, which is generally twice of input data rate. From (3.17) ,(3.18) and (3.19), this equation can arranged as:

$$\begin{aligned} R_L C_L &= \frac{2N(R_L I_{tail})L^2}{\mu_n \cdot V^2{}_{dsat}} = \frac{2N V_{swing} L^2}{\mu_n \cdot V^2{}_{dsat}} = \frac{2N(\alpha V_{dsat})L^2}{\mu_n \cdot V^2{}_{dsat}} \\ &= \frac{2N\alpha L^2}{\mu_n \cdot V_{dsat}} < \frac{1}{2\pi f_{in}} \end{aligned} \tag{3.20}$$

From (3.20), it is concluded that NMOS with minimum length is preferred due to its higher mobility and small parasitic capacitor. The ratio of swing and over-driven voltage should be minimized as long as the complete current steering is achieved. Especially, larger over-driven voltage is required for high speed application. However, the over-driven voltage is limited by the supply voltage requirement. 2V is the maximum allowable supply from previously reported CML design in 0.18um technology [29].

According to the over-driven voltage, the transistor size can be decided to consume minimum power. Note that the transistor should be sized to hold its gate capacitance dominant over wire capacitance, C_{wire}, as shown in equation (3.21). Otherwise, the driving capability between transistors will be limited by wire capacitance. C_{wire} can be estimated by the extraction from prototype layout.

$$C_L = \frac{2NI_{tail}L^2}{\mu_n \cdot V^2{}_{dsat}} >> C_{wire} \tag{3.21}$$

6. Analysis of the Adaptive Bang-Bang CDR

6.1. Stability Characteristics

The proposed solution employs variable loop bandwidth selection to help the system to adapt the unknown input jitter profile. The proposed solution breaks down the conventional trade-off between wide and narrow loop bandwidth by using variable loop bandwidth. As depicted in figure 3.22, the -20dB/dec region (region II) can be extended according to the maximum loop bandwidth setup while the high frequency JTOL amplitude will be improved by the minimum loop bandwidth. Since the optimal loop bandwidth transition takes place around the corner frequency, ω_{2_3}, between region II and III (flat region), the loop bandwidth range will be set to cover targeting ω_{2_3} to maximize its adaptability. Therefore, the design parameter must satisfy following condition:

$$\frac{I_{P\,min} R_P K_{VCO}}{2} < \omega_{2\_3} < \frac{I_{P\,max} R_P K_{VCO}}{2} \tag{3.22}$$

To accomplish high adaptability it is necessary to increase the range of loop bandwidth setup. However, despite of the obvious advantage for the JTOL improvement, the variable loop bandwidth potentially presents the concern of the stability issue because of its time variant frequency response. Modeling the BBPD as a quantizer, the system stability is approximately defined by the stability factor.

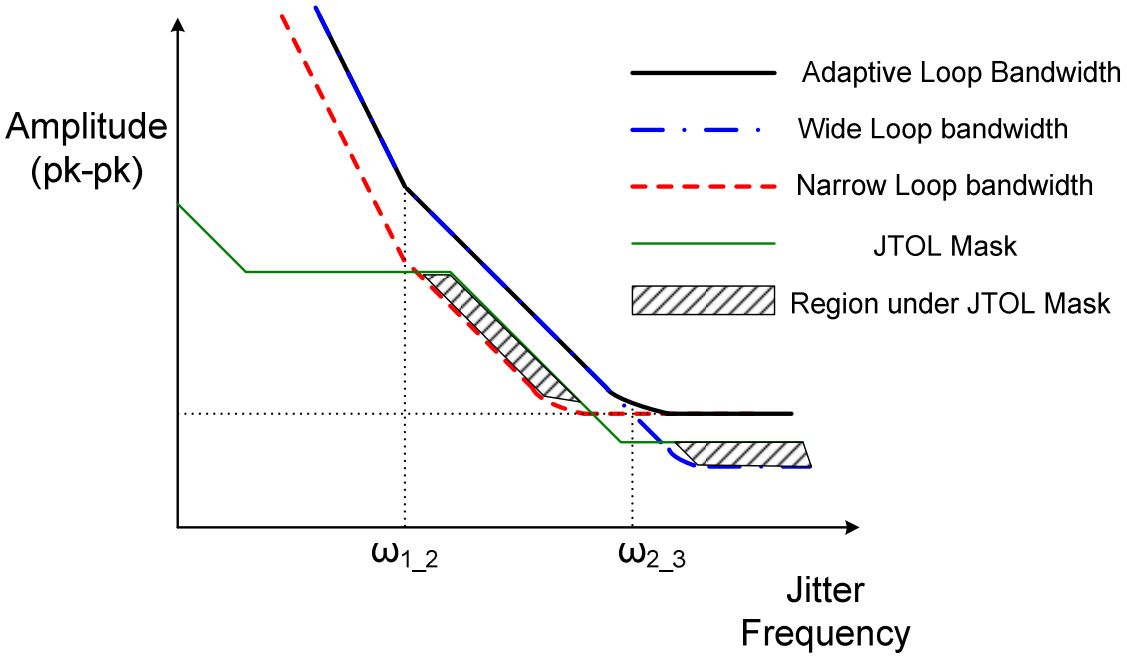


Figure 3. 22 Jitter tolerance improvement with adaptive loop bandwidth

Although it is widely used parameter in systematic analysis of BBPLL, the stability factor is not sufficient to ensure the steady-state behavior because characteristic of BBPD is complicated. The non-linear transfer curve of BBPD can be roughly separated into two regions, linear and binary region. As discussed in chapter II, the regions are determined by the input random jitter and meta-stability of the D flip-flop. If the input phase difference is over the boundary points between the two regions, the BBPD functions as a quantizer. On the other hand, if the phase error is within the boundary points, the BBPD average output shows linear behavior, hence it can be considered as a linear PD. For this case, a piece-wise linear analysis can be applied. Although the stability of the linear region basically does not determine the overall stability of the system behavior due to its non-linear characteristic, the linear region stability must be analyzed thoroughly because JTOL performance will be aggravated if the system is potentially unstable in linear region. In this case, system feedback will fail to suppress the jitter if the power of jitter is within the linear boundaries. Since the boundary point can easily change due to PVT variations, the unstable state may exacerbate the robustness of the system.

To regulate the stability in the linear region, both maximum and minimum PD gain must be carefully studied. Loop parameters, PVT variation and random jitter are also important considerations. In the 3rd order PLL, the phase margin is limited by the low frequency zero ω_z and high frequency pole, ω_p. The phase margin can be re-expressed as:

$$\begin{aligned} PM &= \arctan\left(\frac{\omega_c}{\omega_z}\right) - \arctan\left(\frac{\omega_c}{\omega_p}\right) \\ &= \arctan\left(\frac{\alpha I_P {R_P}^2 C_{P1} K_{VCO}}{2\pi}\right) - \arctan\left(\frac{\alpha I_P {R_P}^2 C_{P2} K_{VCO}}{2\pi}\right) \end{aligned} \tag{3.23}$$

where ω_c is the loop unity gain frequency. α is the slope factor of the BBPD linear gain. If α=1, the BBPD shows linear behavior such as the Hogge detector. If α=∞, the BBPD operates as a quantizer. This is defined as follows (3.24).

$$\alpha = \frac{1}{\pi} \cdot \frac{T_{th}}{T_b} \tag{3.24}$$

where T_{th} is the boundary point between linear and binary region. Thus, α is strongly affected by the PVT variations and input random jitter. With fixed values of R_P, C_{P1}, C_{P2} and K_{VCO}, according to equation (3.23), maximum and minimum limit of loop bandwidth can exist for enough phase margin. From (3.23), the following condition is required to guarantee the stable behavior in the piece-wise linear model:

$$\begin{aligned} &\omega_z << \omega_{c\_min} < \omega_{c\_max} << \omega_p \\ &\frac{1}{R_P C_{P1}} << \frac{\alpha_{min} I_{P\_\min} R_P K_{VCO}}{2\pi} < \frac{\alpha_{max} I_{P\_max} R_P K_{VCO}}{2\pi} << \frac{1}{R_P C_{P2}} \end{aligned} \tag{3.25}$$

where ω_{c_min} and ω_{c_max} are the minimum and maximum loop bandwidth in linear region, respectively. α_{min} and α_{max} are the minimum and maximum slope factor according to the process variation. I_{P_min} and I_{P_max} are the minimum and maximum charge pump current to adjust loop bandwidth. As can be seen in (3.23) and (3.25), the capacitance ratio of C_{P1} to C_{P2} needs to be very high in order to hold the far distance between the zero and pole frequencies. In case the capacitance ratio is limited by some reason, the loop bandwidth range should be regulated not to cause any unstable behavior in the loop.

Table 3. 1 The Loop parameters of the proposed CDR

R_P	500 Ω
C_{P1}	250pF
C_{P2}	0.6pF
I_P	100uA< I_P <800uA

To confirm accurately, the loop stability is analyzed in this section. For the SONET OC-192 JTOL specification, we obtain loop parameters from (2.10), (2.11) and (3.22) as shown table 3.1. For the low frequency range, the stability should be confirmed for minimum unit gain frequency (ω_{c_min}). Assuming α = 1 in equation (3.24), the loop parameters computation yields:

$$\omega_z = 1/(R_p C_1) = 2Mrad/s = 318kHz \tag{3.26}$$

$$\omega_{c\_min} = K_{PD} I_P K_{VCO} R = \frac{1}{\pi} \times 100uA \times 2\pi \times 100MHz \times 500\Omega = 1.59MHz \tag{3.27}$$

The Bode plot is displayed in figure 3.23, the BBCDR with minimum loop bandwidth yields 61degree of phase margin.

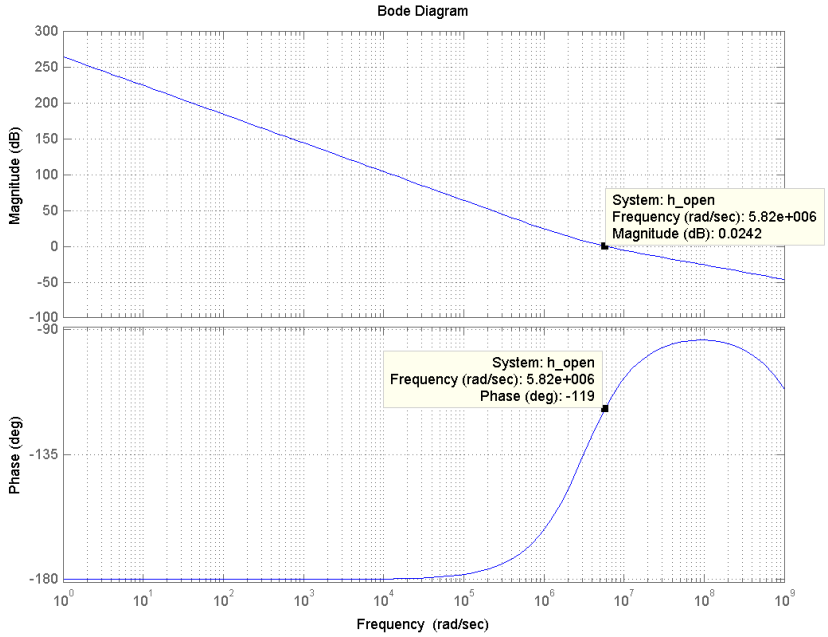


Figure 3. 23 Bode plot of the minimum bandwidth setup

For high frequency stability a simple simulation should be performed in advance to obtain an approximation to the linear gain of BBPD. As shown in figure 3.24, the maximum unit gain frequeny can be calculated associated with maximum current of CP.

$$\omega_{c\_max} = K_{PD} I_P K_{VCO} R = \frac{7}{\pi} \times 800uA \times 2\pi \times 100MHz \times 500\Omega = 89MHz \qquad (3.28)$$

With obtained unit gain frequency and high frequency pole at 500MHz, Bode plot is shown in figure 3.25. In this case, the phase margin is 76 degrees.

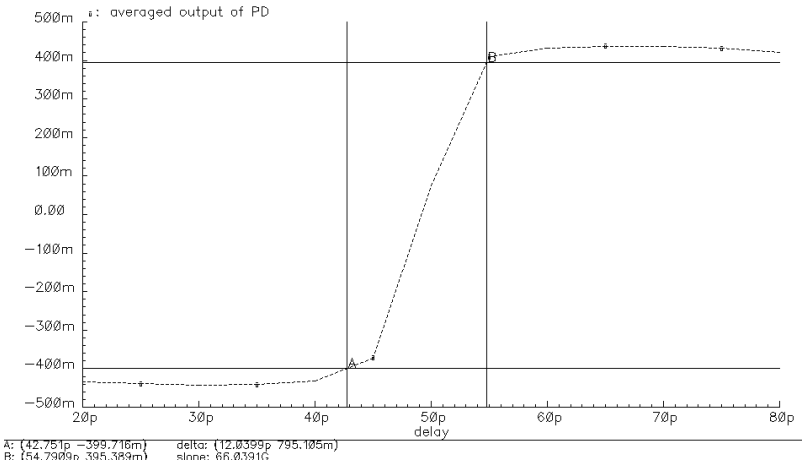


Figure 3. 24 Transfer function of BBPD

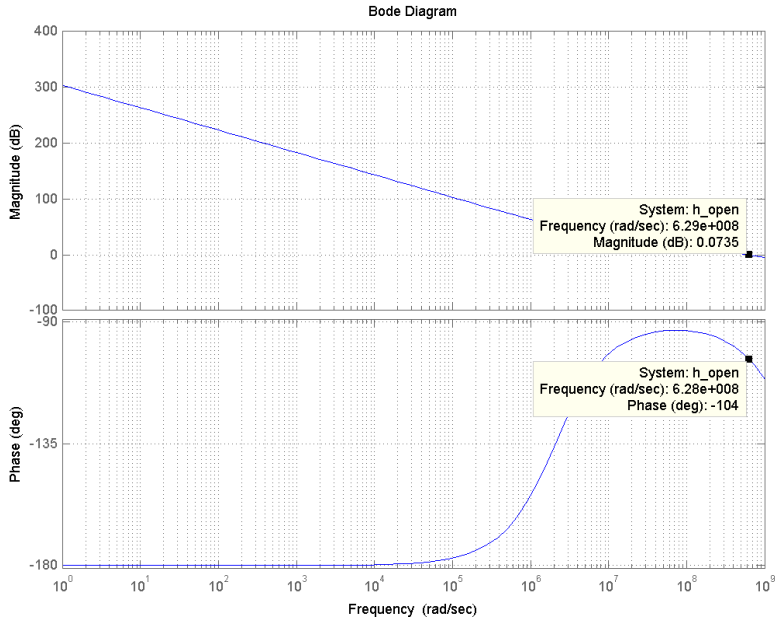


Figure 3. 25 Bode plot of the maximum bandwidth setup

From the frequency analysis of piece-wise linear model of proposed CDR, it is confirmed that the stability of the system is guaranteed not to generate excessive jitter in the linear region with the given parameters.

6.2. Decision of the Predictor Parameters

The predictor dynamics is function of the jitter profile but also of two other important parameters : 1) the loop bandwidth updating rate and 2) threshold points of the A/D converter. To decide those parameters, it should be thoroughly confirmed that predictor controls the CDR loop bandwidth even under extreme cases such as long run length and no input jitter.

For the long run length input data, BBPD returns a long consecutive ‘up’ or ‘down’ in the absence of data transition [33]. The predictor misinterprets the long ‘up’s or ‘down’s as phase-slewing, and accordingly the system may operate with excessively large loop bandwidth. The problem can be alleviated by increasing the updating period. If the run length is shorter than half of the loop bandwidth updating period, the effect of run length will be attenuated by averaging more of following ‘up’ and ‘down’. Therefore, it is desirable to maintain:

$$T_{loop\_update} > 2NT_b \tag{3.29}$$

N denotes the run length, and T_{loop_update} and T_b represent loop bandwidth updating period and bit period, respectively.

The limit cycle is another consideration for the updating rate decision. If input jitter is ignored, BBPLL type CDR exhibits only hunting jitter due to limit cycle as discussed in chapter II. Similarly to the case of long run length, loop bandwidth may be increased if the period of limit cycle is longer than the updating period. Thus, integrating the hunting jitter longer than period of limit cycle, the predictor will average out the effect of the limit cycle. Thus, another lower limit of updating rate is:

$$T_{loop\_update} > T_{limit} \tag{3.30}$$

where T_{limit} is the period of limit cycle. The expression of limit cycle for 3rd order BBPLL was obtained in [34] as:

$$T_{limit} \approx \sqrt{48 R_P C_{P2} \left(0.5T_b + T_{delay}\right)} \tag{3.31}$$

where T_{delay} represents the total loop delay of the CDR. From (3.31), C_{P2} should be small to minimize the limit cycle period. The reduced capacitor, however, may not be able to filter high frequency noise such as supply noise and kick-back noise from VCO.

The upper limit of updating rate will be determined for the adaptation performance. For the accurate adaptation, immediate loop bandwidth update is required. If the CDR controls the loop bandwidth to track the input SJ effectively, the updating period should be more than several times SJ period. To tolerate SJ at higher frequency than JTOL corner frequency requirement (f_{2_3}), the equation (3.32) is required to hold.

$$T_{update} < T_{SJ} < \frac{1}{f_{2\_3}} \tag{3.32}$$

The threshold point of A/D conversion is determined following a similar procedure as the loop bandwidth updating period decision.

Assuming that the maximum N-bit run-length time is around half of updating period, from equation (3.29) the integrator output voltage corresponds to the integration of N times 'up' or 'down'. The high (low) threshold point should be higher (lower) than the deviation in order to regulate loop bandwidth from long run-length. Thus, high/low threshold points will be represented by:

$$\begin{aligned} V_{th\_high} > V_{out\_max} &= V_C + \frac{I_{P2} N T_b}{C_C} \\ V_{th\_low} < V_{outn\_min} &= V_C - \frac{I_{P2} N T_b}{C_C} \end{aligned} \tag{3.33}$$

where I_{P2} is the current of ICP in predictor and V_C is the initial voltage of integrator output.

Limit cycle provides another condition for the threshold points. Integrator returns ideally zero voltage deviation when loop bandwidth updating period is exactly matched to the period of limit cycle. However, it is not possible to match them, and thus, the integrator output will be skewed. If threshold points are too close to the initial voltage,

V_C, the loop bandwidth is increased monotonically that loop bandwidth optimization is failed. The threshold voltage, therefore, should limit the loop bandwidth even with the deviation of limit cycle period. As shown in figure 3.26(a), if the limit cycle period is shorter than updating period, the corresponding maximum deviation is limited to the $(I_{P2}T_{loop\_update})/3C_C$. If the high (low) threshold point is higher (lower) than the deviation from the V_C, the loop bandwidth will not be increased. Therefore:

$$V_{th\_high} > V_{out\_max} = V_C + \frac{I_{P2}T_{loop\_update}}{3C_C}$$
$$V_{th\_low} < V_{outn\_min} = V_C - \frac{I_{P2}T_{loop\_update}}{3C_C} \quad (3.34)$$

The threshold point shown in equation (3.34) cannot regulate loop bandwidth if the limit cycle period is much longer than the updating rate. In this case, corresponding maximum deviation is $(I_{P2}T_{loop\_update})/C_C$ which is equal to the inherent maximum deviation of the integrator. The predictor will fail to increase loop bandwidth if this value is set to the threshold points. Thus, the maximum limit cycle period must be well-controlled to follow the condition.

$$T_{limit} < \frac{4T_{loop\_update}}{3} \quad (3.32)$$

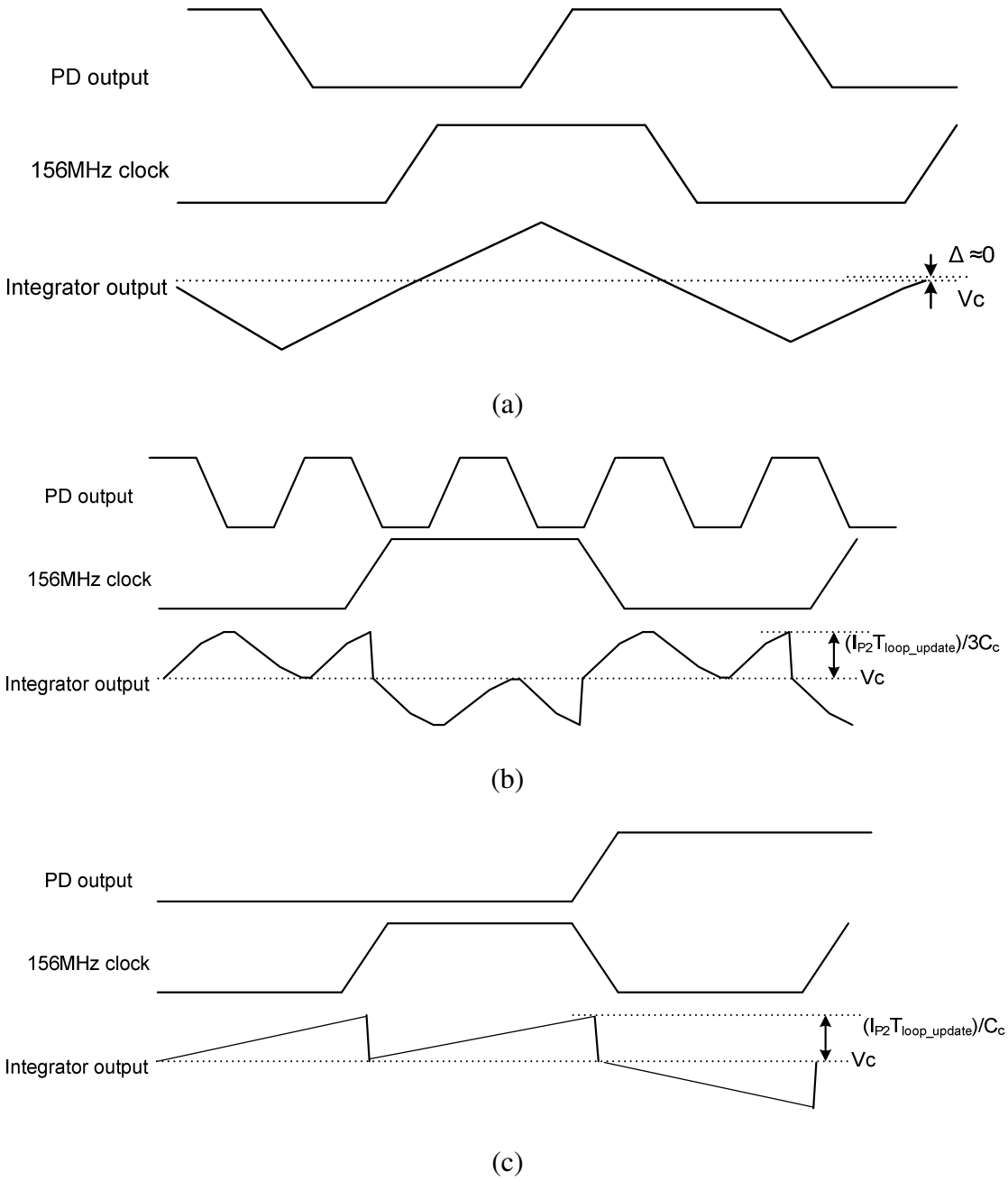


Figure 3. 26 Maximum integrator output if (a) limit cycle period = updating period (b) limit cycle period < updating period and (c) limit cycle period > updating period

As presented by the equation from (3.26) to (3.32), the parameters in predictor must be selected carefully not to degrade the loop bandwidth adaptation. The analysis of the optimal parameter, however, is still a discussion to be clarified.

The effects of the loop bandwidth updating rate and A/D conversion threshold points are illustrated in figure 3.27 and 3.28, respectively.

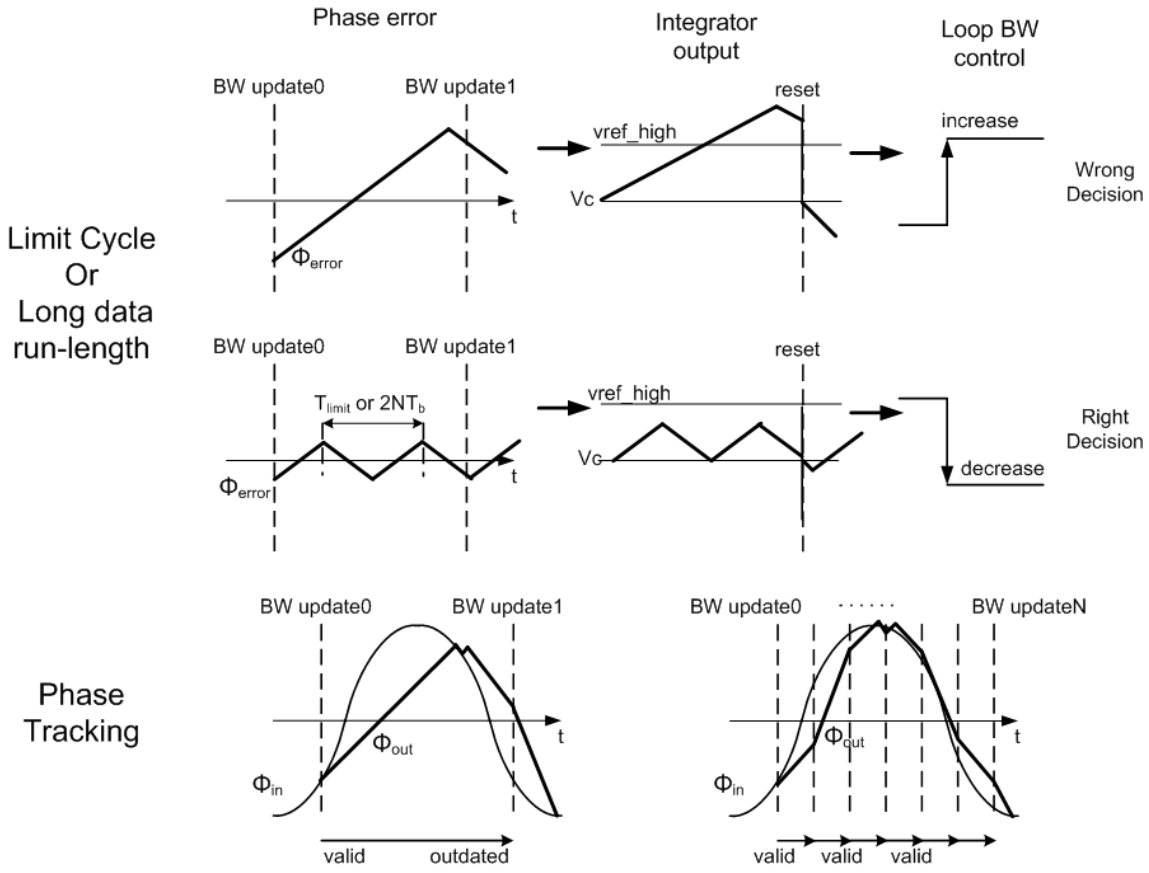


Figure 3. 27 The effect of the updating rate on loop bandwidth control

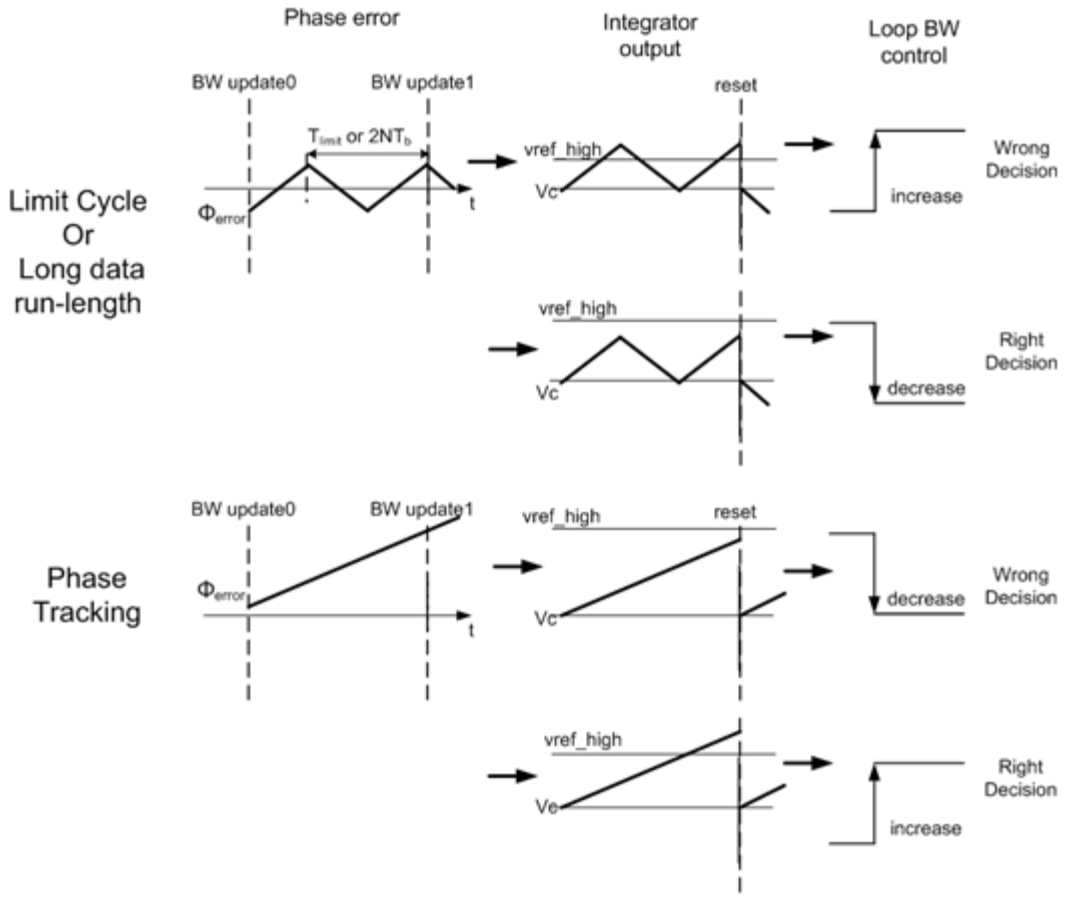


Figure 3. 28 The effect of the threshold points of A/D conversion on the loop bandwidth control

7. Summary

Charge pump current control accommodates the loop adaptation independent of the stability factor variation. With mixed-mode piece-wise integration, the predictor provides jitter profile detection and loop adaptation with low power consumption and high flexibility. The physical capacitance of loop filter can be reduced by the capacitor multiplication with dual charge pump architecture. To alleviate power and speed requirement of phase detector, half-rate structure is implemented. To verify the

functionality of the adaptive loop bandwidth, the stability should be analyzed for all loop bandwidth setup. The parameter setup for predictor is carefully selected for the appropriate loop bandwidth adaptation.

CHAPTER IV

SIMULATION RESULT

1. Loop Bandwidth Control Dynamics

As shown in figure 3.7, the proposed CDR adjusts the loop bandwidth with CP current control. Thus, the dynamics of loop bandwidth control can be monitored with the variation of CP current.

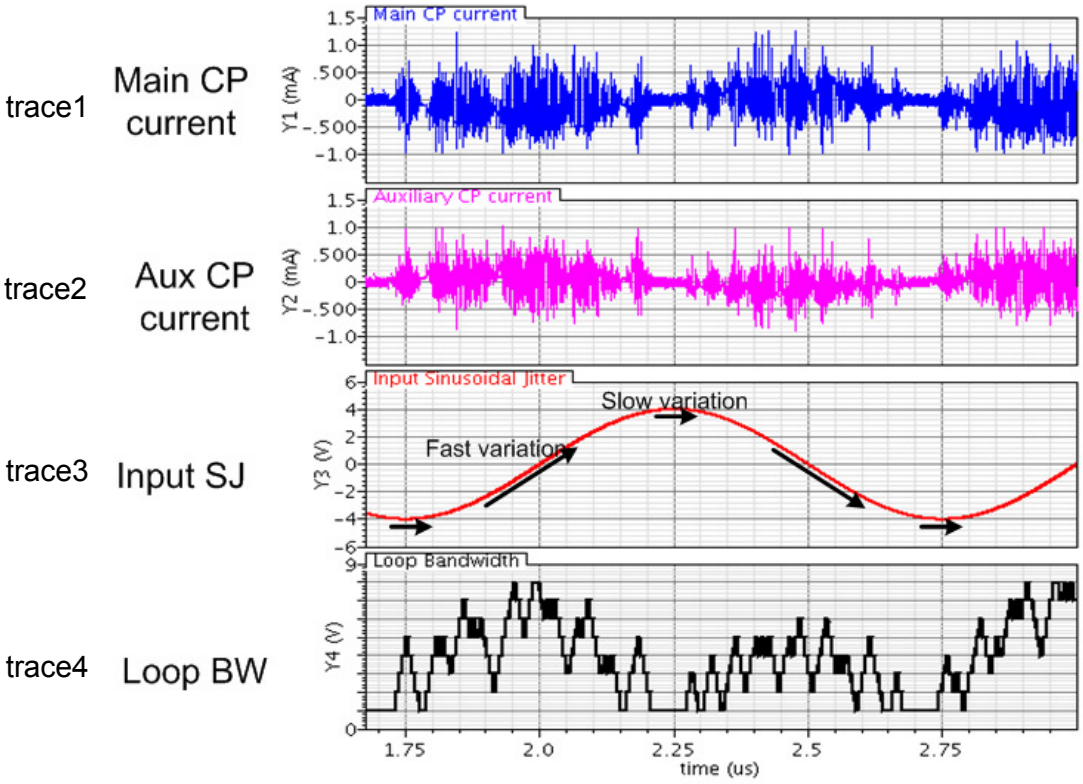


Figure 4. 1 Current and loop bandwidth control of proposed solution. 1)Main CP current, 2)Auxiliary CP current, 3)input phase variation and 4)loop bandwidth setup (From top to bottom)

Figure 4.1 illustrates the main CP current variation, auxiliary CP current variation, input SJ variation and the loop bandwidth code of predictor, respectively (from top to bottom). The predictor adjusts the loop bandwidth setup as the slope of input SJ changes. From 1.75us to 2.00us third trace in the third trace, the SJ slope increases monotonically. As shown in the fourth trace, the loop bandwidth code is roughly increasing according to input SJ slope. Corresponding to this dynamics, CP current is adjusted successfully.

The effect of proposed solution on the jitter performance is shown in figure 4.2. The proposed CDR and the maximum loop bandwidth conventional CDR tracks the high amplitude (8UIpp) SJ at 1MHz without phase-slewing. The standard deviation of RJ is 0.025UIrms and ISI jitter is 0.15UIpp. Note that the maximum loop bandwidth conventional CDR generates more granular jitter than proposed CDR. Although the output jitter of proposed CDR exhibits comparable peak-to-peak value to maximum loop bandwidth CDR, the proposed CDR minimizes the wide bandwidth jitter when the slope of input SJ is relatively relaxed. Minimum loop bandwidth CDR, on the other hand, experiences serious phase-slewing issues; the CDR loses the lock state about once in a cycle of input SJ. From the figures, it is shown that the proposed CDR effectively controls loop bandwidth to minimize jitter.

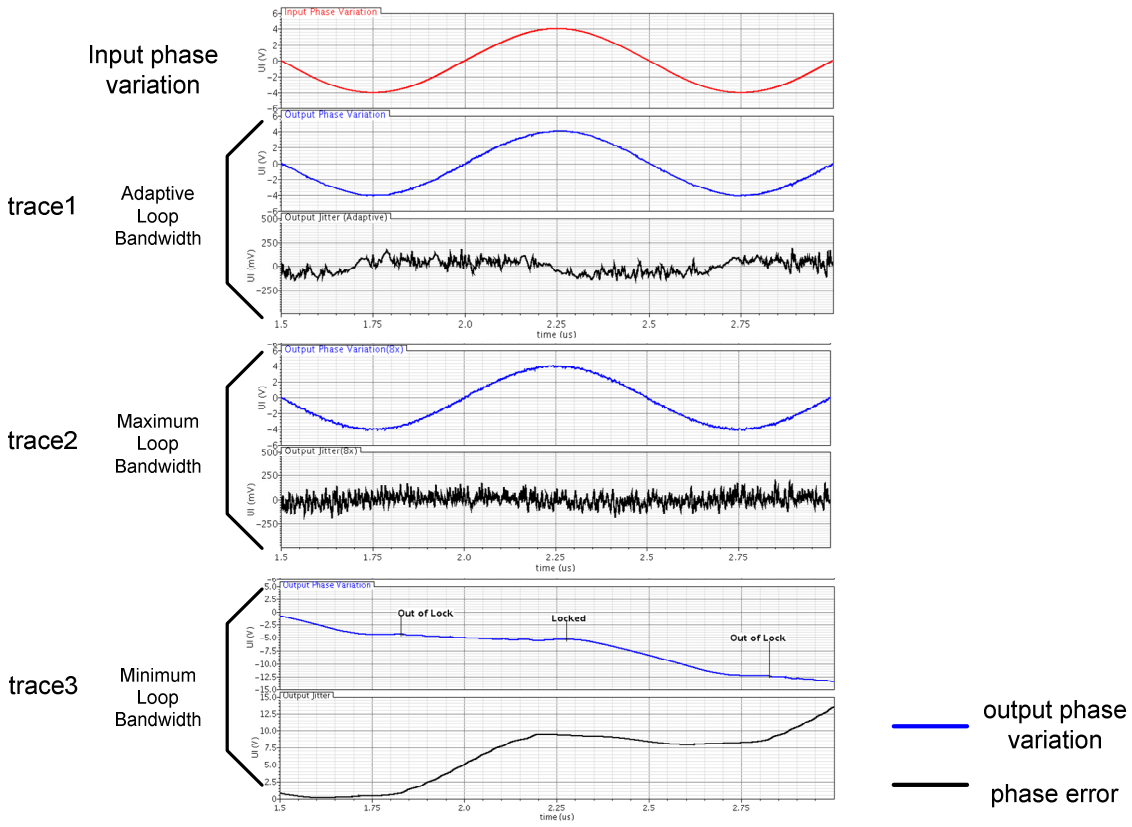


Figure 4. 2 The comparison of jitter performance. 1)proposed CDR 2)the maximum loop bandwidth CDR 3)the minimum Loop bandwidth CDR (from top to bottom)

2. Jitter Histogram

The observation of the jitter histogram provides another point of view on how the loop bandwidth adaptation is achieved. If the predictor detects and makes a correct decision on loop bandwidth selection, the jitter histogram of the proposed CDR exhibits optimal shape such that BER, RMS jitter and peak-to-peak jitter are minimized. The jitter histogram of the proposed solution can be evaluated by the comparison with the maximum and minimum loop bandwidth of the conventional BBCDR. From figure 4.3 to figure 4.6, the jitter histogram of proposed CDR is compared with conventional CDRs

with the maximum and minimum. All simulations are performed with the jitter condition tabulated in table 4.1. The predictor is implemented in schematic level and the fundamental CDR components are described with behavioral models.

Table 4. 1 The condition of input jitter for simulation of the jitter histogram

Condition No.	RJ	ISI	SJ (Amplitude/Frequency)
JHISTO-1	0.05 UIrms	0.3 UIpp	0UIpp / 0MHz
JHISTO-2	0.05 UIrms	0.3 UIpp	0.1UIpp/40MHz
JHISTO-3	0.05 UIrms	0.3 UIpp	1.0UIpp/1MHz
JHISTO-4	0.025UIrms	0.15UIpp	0.6UIpp/40MHz

When BBCDR experiences no SJ, the loop bandwidth should be minimized in order to suppress RJ, ISI and hunting jitter. In figure 4.3, the proposed CDR exhibits very similar shape of histogram to minimum loop bandwidth conventional CDR. For the SJ with high frequency (40MHz) and low amplitude (0.1UIpp), the narrow loop bandwidth will be advantageous to reduce the BER although CDR may experience the phase-slewing. Since the amplitude of SJ is much less than the wide bandwidth jitter power, adaptive loop bandwidth should suppress the wide bandwidth jitter by reducing loop bandwidth rather than tracking high frequency SJ. Thus, the jitter histogram of the proposed CDR is expected to be similar to the minimum loop bandwidth conventional CDR as shown in figure 4.4.

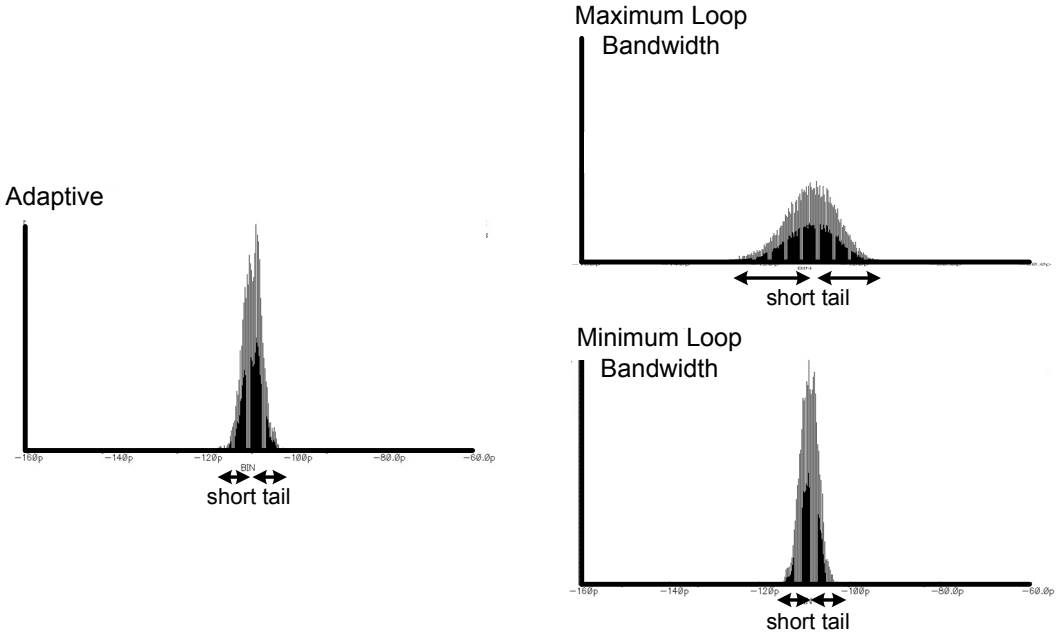


Figure 4. 3 Jitter histogram comparison : JHISTO-1
(Jitter profile : RJ = 0.05UIrms, ISI = 0.3UIpp and no SJ)

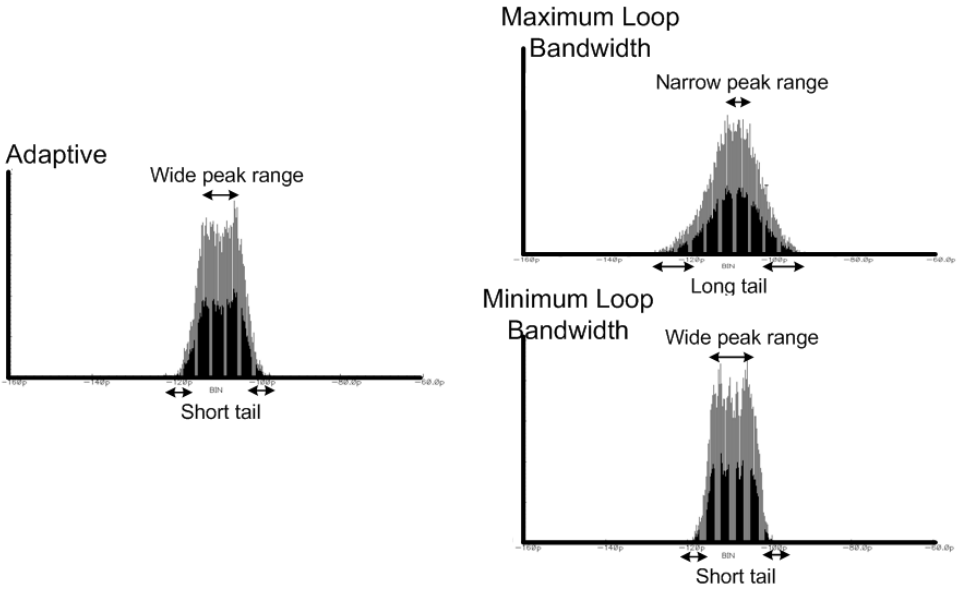


Figure 4. 4 Jitter histogram comparison : JHISTO-2
(Jitter profile : RJ=0.05UIrms, ISI=0.3UIpp and SJ=0.1UIpp@40MHz)

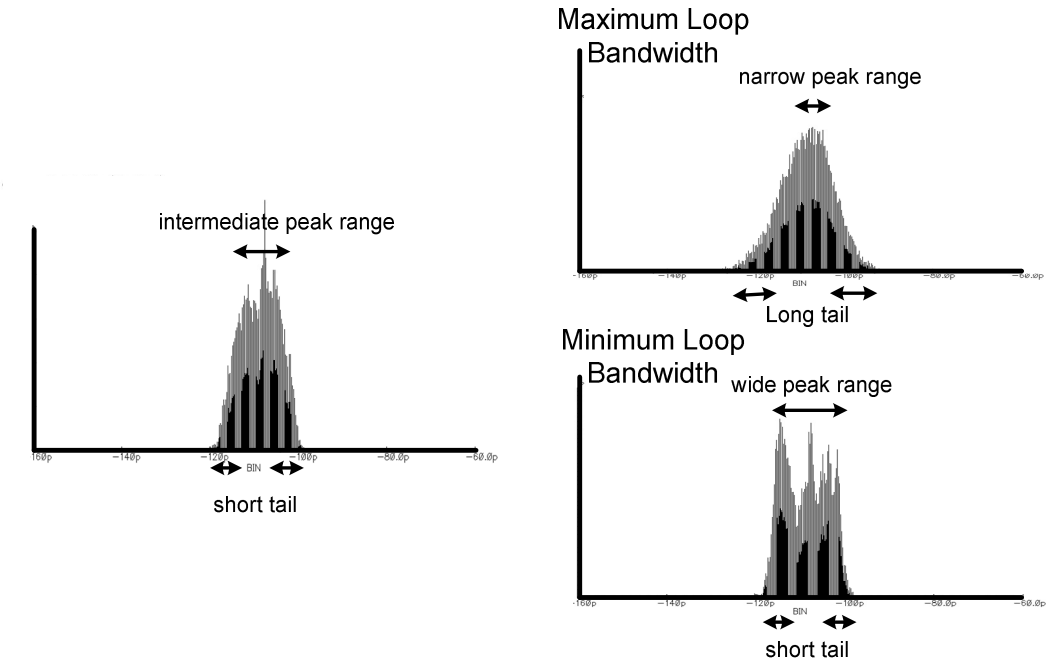


Figure 4. 5 Jitter histogram comparison : JHISTO-3
(Jitter profile : RJ=0.05UIrms, ISI=0.3UIpp and SJ=1.0UIpp@1MHz)

When the SJ frequency is reduced while amplitude is increased, the optimal loop bandwidth will be changed. Due to the large amplitude of SJ, CDR is required not only to suppress the wide bandwidth jitter but also to track the SJ variation. As a result, the jitter histogram of proposed CDR presents intermediate shape of two conventional CDRs as depicted in figure 4.5.

The wide loop bandwidth setup is generally superior in case that wide bandwidth jitter is not dominant over the SJ as the final jitter profile in table 4.1. In this case, the CDR will experience significant phase-slewing while the wide bandwidth jitter is relatively mitigated. Thus, the proposed CDR should track the high speed SJ that jitter histogram is expected to be similar to the maximum loop bandwidth conventional CDR.

The result can be confirmed in the figure 4.6. Note that the figure 4.6 is scaled by twice to show clear result. The minimum loop bandwidth CDR suffers from the phase slewing as the histogram is similar to the PDF of SJ in figure 2.9. This implies that the input SJ is filtered out by narrow loop bandwidth. On the other hand, proposed CDR tracks the SJ effectively that the jitter histogram shows similar shape to the maximum loop bandwidth CDR.

From the observation of the jitter histogram, it can be concluded that the proposed CDR acquires the optimal loop bandwidth without the misleading to excessive jitter generation. The proposed adaptive loop bandwidth BBCDR breaks the trade off of loop bandwidth setup for jitter performance. It is shown that the jitter histogram is not affected significantly by threshold point as shown in figure 4.3 to 4.6.

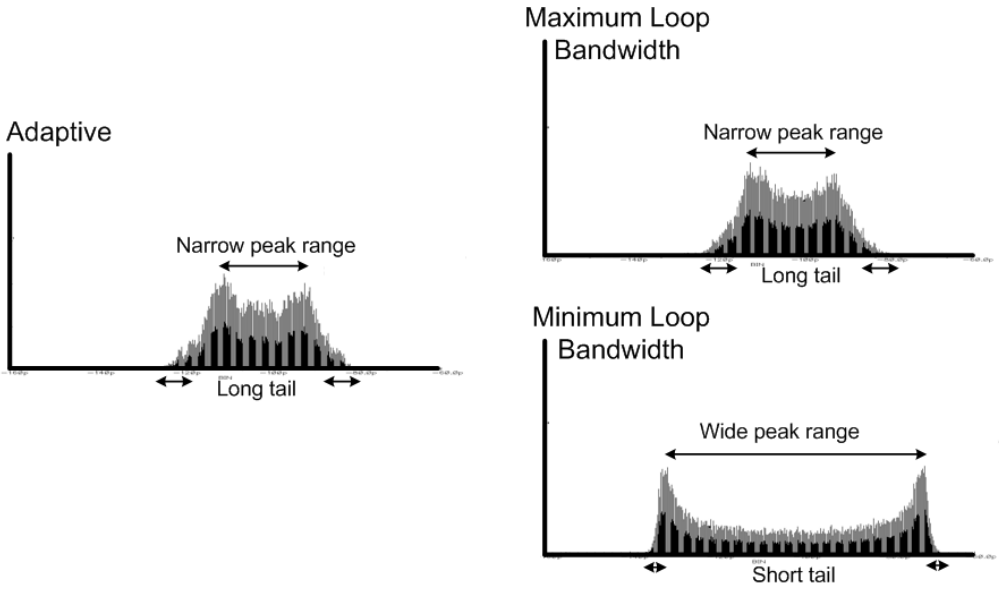


Figure 4. 6 Jitter histogram comparison : JHISTO-4
(Jitter profile : RJ=0.025UIrms, ISI=0.15UIpp and SJ=0.6UIpp@40MHz)

3. Jitter Tolerance

The proposed CDR should be evaluated with JTOL performance to prove the advantage of the proposed adaptive loop bandwidth strategy. JTOL measurement with Cadence simulation, however, is difficult to measure JTOL of 10^{-12} BER because of its excessive computing resources and running time. Therefore, an alternative simulation setup is established to obtain the relevant information of JTOL. For the 10^{-12} BER JTOL with 0.03UIrms of RJ and 0.3UIpp of ISI, the timing margin that CDR must achieve can be obtained by following procedure.

$$1UI = \beta\sigma_{RJ} + ISI_{pp} + P_{margin} \tag{4.1}$$

$$\begin{aligned} P_{margin} &= 1UI - \beta\sigma_{RJ} + ISI_{pp} \\ &= 1UI - 14\times 0.03 + 0.3UI_{pp} \\ &= 0.28UI_{pp} \end{aligned} \tag{4.2}$$

Here, β is the fitting factor for the given BER and increases for the better BER. Since ISI is deterministic jitter generating bounded limit, we can re-calculate the required power of RJ, σ_{RJ_new}, to achieve same timing margin for relaxed BER. In other words, we can project that the CDR can tolerate σ_{RJ} of RJ for 10^{-12} BER if it tolerates an intentionally aggravated RJ, σ_{RJ_new}, for relaxed BER. For the 4us simulation time, we can test if the design achieves BER less than $2.5*10^{-5}$. From (4.1) and (4.2), we figure out the value of alternative, σ_{RJ_new} as:

$$\begin{aligned}\beta\sigma_{RJ\_new} &= 1UI - ISI_{pp} - P_{margin} \\ &= 1UI - 0.3UI_{pp} - 0.28UI_{pp} \\ &= 0.42UI_{pp}\end{aligned} \tag{4.3}$$

Since β is equal to eight to achieve $2.5*10^{-5}$ BER, σ_{RJ_new} is required to be $0.05UI_{rms}$.

To verify the adaptation performance of the proposed system, JTOL is measured in two different conditions as tabulated in table 4.2. In proposed solution the simulations have been performed with two different threshold values. Conventional CDRs with maximum and minimum loop bandwidth setup is used for the jitter histogram result.

Table 4. 2 Jitter profile for the JTOL measurement

Condition No.	RJ (σ_{RJ_new})	ISI	Data Pattern
JTOL-1	0.05 UIrms	0.3 UIpp	2^{31} PRBS
JTOL-2	0.025 UIrms	0.15 UIpp	2^{31} PRBS

The results on the JTOL-1, the testing setup as shown in table 4.2, reflect the JTOL on pessimistic channel condition. Narrow loop bandwidth is more effective than wide loop bandwidth in the setup. As shown in figure 4.7, the minimum loop bandwidth conventional CDR demonstrates generally superior performance than maximum loop bandwidth conventional CDR. The proposed CDR tolerates input phase variation better than or comparable to the minimum loop bandwidth CDR except one example of Adaptive-1 at 40MHz .

JTOL-2 emulates the optimistic channel condition which the phase-slewing error is likely dominant over the RJ, ISI and hunting jitter. Thus, wide loop bandwidth setup will tolerate higher phase amplitude changes. Figure 4.8 illustrates the result of the simulation. Maximum loop bandwidth setup shows better performance than minimum loop bandwidth and proposed adaptive system at 4MHz and 10MHz. The proposed CDR results in comparable jitter performance at 1MHz and 40MHz. In this result, adaptive loop bandwidth CDRs shows degraded performance than expected in section III as shown in figure 4.9. The degraded jitter performance at intermediate frequency is also presented in previously reported adaptive scheme [24]. This can be deduced that the updating rate is still not fast enough for input SJ. Since the wide bandwidth jitter is quite small in JTOL-2, the BER will be occurred mostly due to the phase-slewing. The tentatively reduced loop bandwidth may increase the jitter by instantaneous phase-slewing if the loop bandwidth is not recovered immediately. The effect is disappeared at low frequency (1MHz) because the loop bandwidth updating rate is fast enough to track the slope variation of input SJ.

Even if the degradation is shown at the intermediate frequencies in the setup for optimistic channel, the superiority of the proposed solution over conventional design can be justified by following claims.

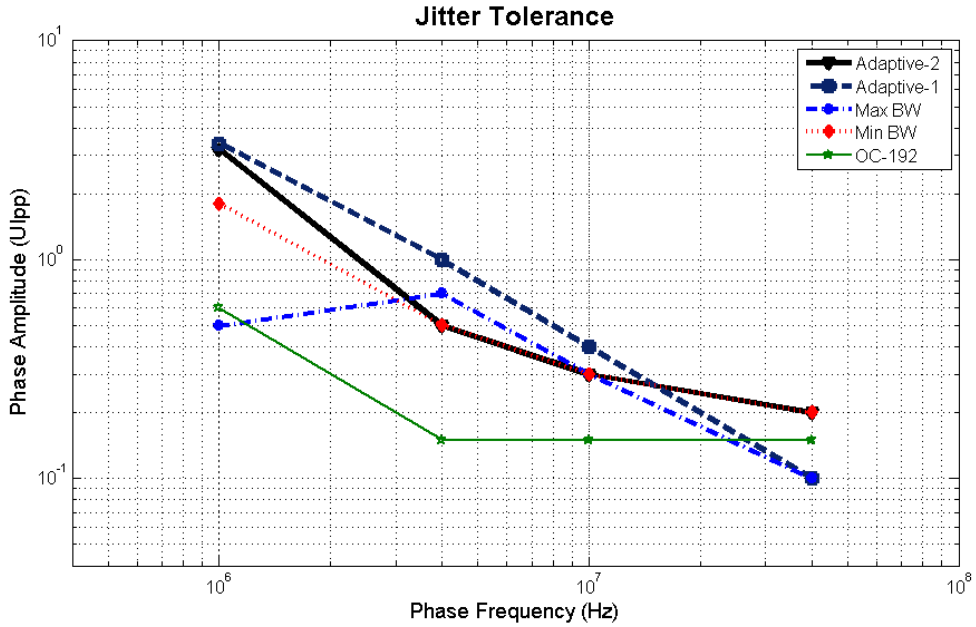


Figure 4. 7 Jitter tolerance of behavioral mode with condition JTOL-1

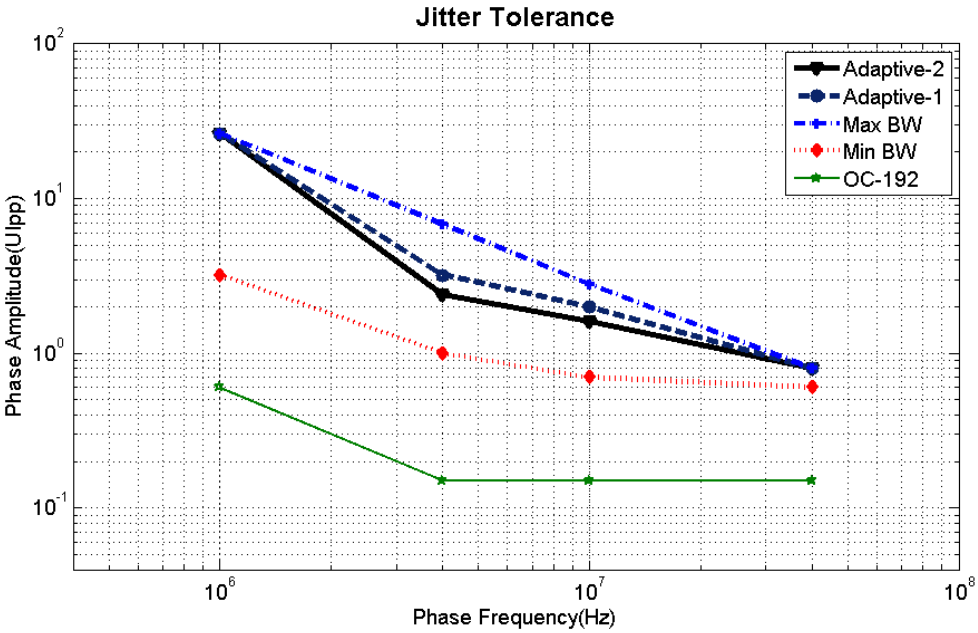


Figure 4. 8 Jitter tolerance of behavioral model with Condition JTOL-2

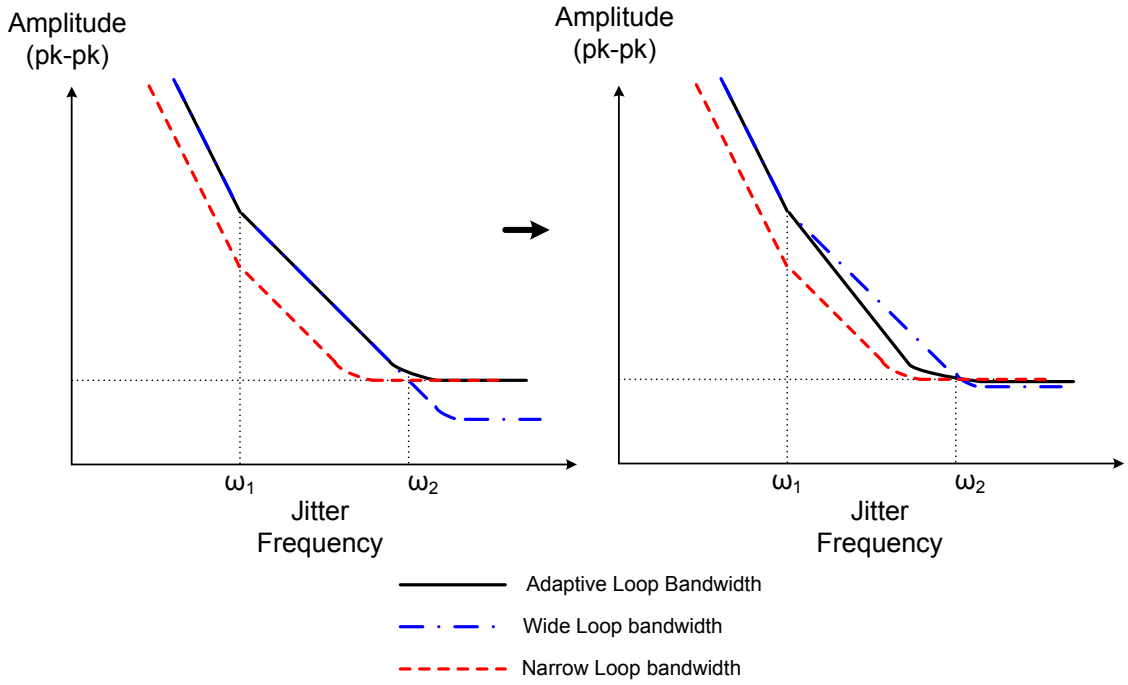


Figure 4. 9 The effect on the low power wide bandwidth jitter profile

First, the proposed CDR demonstrates the comparable performance to the conventional CDR with optimal loop bandwidth regardless of the input jitter profile. The minimum or maximum loop bandwidth presents worst performance if the jitter profile is not matched to their setup. Second, even there exists the degraded points in optimistic channel setup, they are only limited to specific frequencies. Moreover, overall JTOL of proposed CDR exceeds the standard requirement by enough margin.

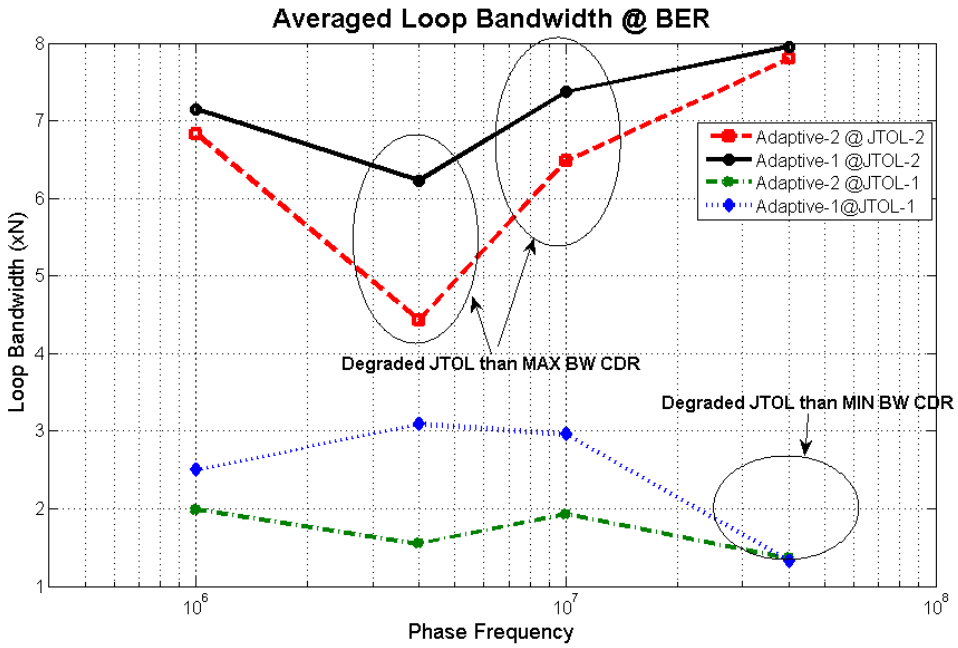


Figure 4. 10 Average loop bandwidth in the presence of bit error

JTOL results also reflect the effect of the threshold point. By observing the average loop bandwidth when the bit-error arises, it can be deduced that how the threshold point should be controlled in the predictor. In figure 4.10, the circled area shows in which case the loop adaptation is less effective. If the average loop bandwidth is far lower than the mid-level loop bandwidth, this implies that the power of wide bandwidth jitter is dominant than phase-slewing. Circled area in right-bottom side shows that small threshold point (closer to the common level) increases the sensitivity of loop bandwidth control to granular wide bandwidth jitter. On the other hand, two circled areas in top side imply that large threshold point (further from the common level) decreases the sensitivity of loop bandwidth control to phase-slewing. In order to increase the

sensitivity to dominant phase-slewing and decrease to wide bandwidth jitter, threshold point control shown in figure 4.11 can be suggested.

To verify the operation of overall system, the JTOL simulations are performed with schematic level with behavioral model of VCO and buffers. Due to the lack of resources and time, the CDRs are tested in one jitter profile, JTOL-2. For the same reason, one threshold point (1.15V / 0.85V) is tested for proposed CDR. PD, CP and VCO are shared by all sets of simulation. As shown in figure 4.12, the proposed CDR demonstrates the best jitter performance. Note that the maximum loop bandwidth conventional CDR shows much degraded performance than others. It can be thought that the internal jitter source, especially internal ISI due to limited bandwidth of D flip-flop, contributes more power of wide bandwidth jitter to the system. Experiencing more serious wide bandwidth jitter, proposed CDR successfully adjust the loop bandwidth to be optimal for input jitter profile.

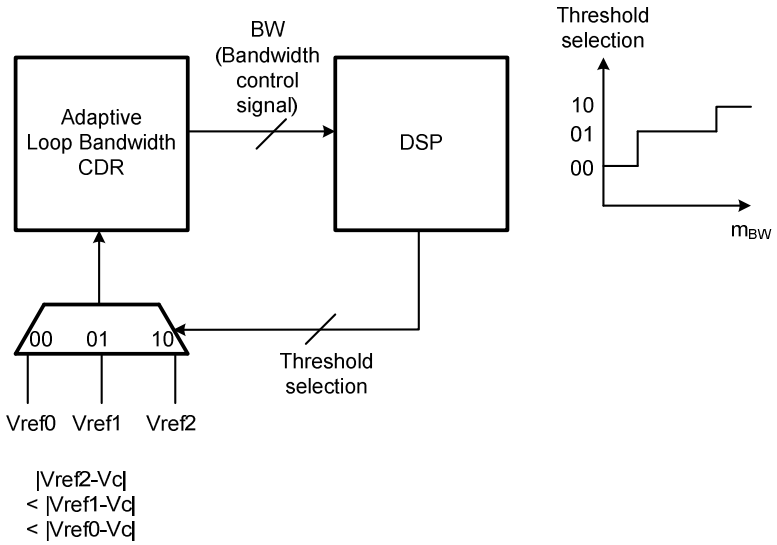


Figure 4. 11 Potential threshold point control scheme

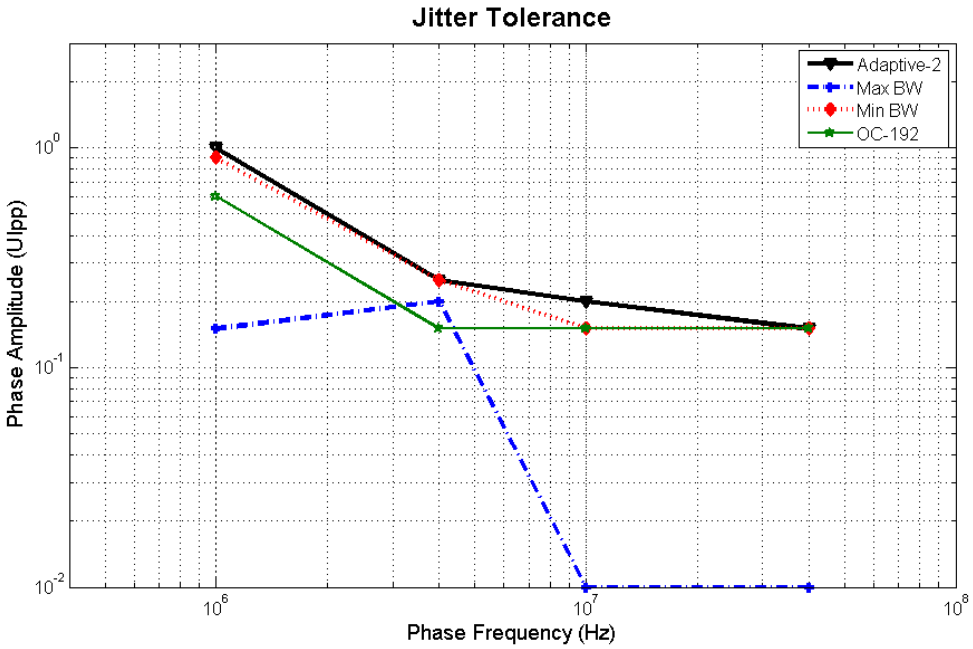


Figure 4. 12 The Jitter tolerance of schematic level with condition JTOL-1

4. Design Summary

Based on the design issues and procedure discussed so far, the proposed adaptive loop bandwidth clock and data recovery is designed and demonstrates following specifications in table 4.3.

Table 4. 3 The design summary of the adaptive loop bandwidth CDR

Bit rate	10Gb/s
Power	Overall : 84.3mW (excluding VCO and buffers) Predictor : 7.9mW
Supply	2V
Estimated Filter area	200X200(um^2)
Technology	0.18um CMOS Technology
JTOL	>0.15UIpp @ 40MHz (RJ = 0.05UIrms / ISI = 0.3UIpp) with 2^{31} PRBS data
JGEN	2.11ps (RMS) / 17ps (p-p) (RJ = 0.05UIrms / ISI = 0.3UIpp) 1.89ps (RMS)/ 12.72ps (p-p) (RJ = 0.05UIrms / ISI = 0.3UIpp)
Loop Bandwidth range	1 to 8 times
VCO phase noise of behavioral mode	-120dBc/Hz@1MHz
Buffer delay	1ns (10 bits)

CHAPTER IV

CONCLUSION

In this thesis, Bang-Bang clock and data recovery with novel adaptive loop bandwidth control strategy is presented for improved jitter performance.

A clock and data recovery system is required to reconstruct a clock from random data stream in the presence of wide bandwidth jitter such as random jitter and inter-symbol interference as well as sinusoidal periodic jitter. Due to its unpredictable and high speed behavior of wide bandwidth jitter, the clock and data recovery system typically confronts the trade-off on the loop bandwidth setup between phase-tracking and jitter filtering. Large time constant requirement is also the issue of the implementation cost.

To optimize loop bandwidth from unknown channel condition and noise sources, the proposed BBCDR detects jitter profile and adjust the loop bandwidth to minimize overall output jitter. Unlike previously proposed digital or semi-digital solutions, this work proposes a predictor with mixed-mode piece-wise integration for the detection of input jitter. An analog front end is employed to perform the piece-wise integration regardless the input data rate. With simple A/D converters and a low logic depth digital counter, the predictor is easily implemented with low power consumption. To maintain stability factor while loop bandwidth keeps being adjusted, a charge pump current control is employed than loop filter resistor control. Capacitance multiplication technique is adopted to reduce the size of loop filter for on-chip implementation.

From simulations in Cadence, the CDR has been tested for loop bandwidth control dynamics, jitter histogram and jitter tolerance. In the case that wide bandwidth jitter is dominant, the proposed CDR successfully improves jitter performance compared to conventional CDRs. Although some degradation arises at intermediate frequencies with small power of wide bandwidth jitter, proposed system performs comparable to the conventional CDR with optimal loop bandwidth. Overall system is verified with schematic level simulations including phase noise and loop delay. From the final result, it is confirmed that the proposed CDR effectively controls loop bandwidth so that it demonstrates superior jitter tolerance.

As semi-conductor industry drives high speed and low cost implementation, the proposed CDR suggests a possible solution to improve jitter performance with reduced power consumption and silicon area in very high speed application. Due to its robustness and high quality jitter performance, the design can be applied to serial link applications where stringent jitter specification is required.

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