DESIGN AND IMPLEMENTATION OF SWITCHING VOLTAGE INTEGRATED CIRCUITS BASED ON SLIDING MODE CONTROL

A Dissertation

by

MIGUEL ANGEL ROJAS GONZÁLEZ

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2009

Major Subject: Electrical Engineering

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ABSTRACT

Design and Implementation of Switching Voltage Integrated Circuits
Based on Sliding Mode Control. (August 2009)
Miguel Angel Rojas González, B.S. (Honors), ITESM Campus Toluca, Mexico
Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

The need for high performance circuits in systems with low-voltage and low-power requirements has exponentially increased during the few last years due to the sophistication and miniaturization of electronic components. Most of these circuits are required to have a very good efficiency behavior in order to extend the battery life of the device.

This dissertation addresses two important topics concerning very high efficiency circuits with very high performance specifications. The first topic is the design and implementation of class D audio power amplifiers, keeping their inherent high efficiency characteristic while improving their linearity performance, reducing their quiescent power consumption, and minimizing the silicon area. The second topic is the design and implementation of switching voltage regulators and their controllers, to provide a low-cost, compact, high efficient and reliable power conversion for integrated circuits.

The first part of this dissertation includes a short, although deep, analysis on class D amplifiers, their history, principles of operation, architectures, performance metrics, practical design considerations, and their present and future market distribution. Moreover, the harmonic distortion of open-loop class D amplifiers based on pulse-width modulation (PWM) is analyzed by applying the duty cycle variation technique for the most popular carrier waveforms giving an easy and practical analytic method to evaluate the class D amplifier distortion and determine its specifications for a given linearity requirement. Additionally, three class D amplifiers, with an architecture based on sliding mode control,

are proposed, designed, fabricated and tested. The amplifiers make use of a hysteretic controller to avoid the need of complex overhead circuitry typically needed in other architectures to compensate non-idealities of practical implementations. The design of the amplifiers based on this technique is compact, small, reliable, and provides a performance comparable to the state-of-the-art class D amplifiers, but consumes only one tenth of quiescent power. This characteristic gives to the proposed amplifiers an advantage for applications with minimal power consumption and very high performance requirements.

The second part of this dissertation presents the design, implementation, and testing of switching voltage regulators. It starts with a description and brief analysis on the power converters architectures. It outlines the advantages and drawbacks of the main topologies, discusses practical design considerations, and compares their current and future market distribution. Then, two different buck converters are proposed to overcome the most critical issue in switching voltage regulators: to provide a stable voltage supply for electronic devices, with good regulation voltage, high efficiency performance, and, most important, a minimum number of components. The first buck converter, which has been designed, fabricated and tested, is an integrated dual-output voltage regulator based on sliding mode control that provides a power efficiency comparable to the conventional solutions, but potentially saves silicon area and input filter components. The design is based on the idea of stacking traditional buck converters to provide multiple output voltages with the minimum number of switches. Finally, a fully integrated buck converter based on sliding mode control is proposed. The architecture integrates the external passive components to deliver a complete monolithic solution with minimal silicon area. The buck converter employs a poly-phase structure to minimize the output current ripple and a hysteretic controller to avoid the generation of an additional high frequency carrier waveform needed in conventional solutions. The simulated results are comparable to the state-of-the-art works even with no additional post-fabrication process to improve the converter performance.

Para Mateo, que dejaste tu estrella para sentir el mar…

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CHAPTER I

INTRODUCTION

High performance circuits with high efficiency and minimum quiescent power consumption are required for present and future electronic devices. The battery life of portable and rechargeable equipment must be extended to offer the maximum operating time. Therefore, switching voltage circuits are highly recommended because their theoretical transfer of power is perfect, delivering the highest efficiency possible. Moreover, even with the drawbacks of practical implementations, switching voltage circuits provide higher efficiency than other architectures.

The research presented in this dissertation approaches two of the most important applications of switching voltage circuits: (1) the design of high performance class D audio power amplifiers, and (2) the design of high efficiency switching voltage regulators.

This dissertation is divided as follows, the first part of it addresses the principles of audio power amplifiers, and the design, implementation, and testing of three different class D audio power amplifiers with a topology based on sliding mode control.

The second part of this dissertation presents the fundamentals of switching voltage regulators, as well as the design, building, and testing of two buck voltage regulators, based on sliding mode control theory, for low-voltage and low-power applications.

A. Class D Audio Power Amplifiers

The use of class D audio power amplifiers has been increasing considerably during last years due to their high efficiency behavior when compared to traditional class A, class B, and class AB audio power amplifiers, however, their poor linearity performance has limited

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a complete market acceptation.

While class A amplifier ideally exhibits a maximum efficiency of 25%, and class B/AB amplifiers yield a top efficiency around 78.5%, class D audio amplifiers present a theoretical efficiency of 100% that makes them the best choice for low-voltage and low-power applications, especially in battery powered devices.

Class D audio power amplifiers are mainly used in hearing aids, headphone amplifiers, wireless phones, audio/video portable players, notebook and netbook computers, radios, and portable video games, where the high efficiency performance is essential to maximize the battery life. Thus, the main challenge designing class D audio amplifiers is to keep their high efficiency inherent characteristic while improving their linearity performance.

The fundamentals on audio power amplifiers and class D audio amplifiers are discussed in Chapter II. It covers the basic principles of sound and audio amplifiers, presenting a brief history on audio amplification and a description of the main audio amplifier classes. This chapter introduces the essential concepts of class D audio power amplifiers and their main architectures. Moreover, it outlines some of the design constraints, and practical design and testing considerations. Lastly, it gives a broad overview of the economic importance of class D audio power amplifiers in the global market distribution.

Chapter III describes the design, implementation, and measurement of a high performance class D audio amplifier using a hysteretic based controller. The proposed class D audio power amplifier operates with a nonlinear controller with sliding mode. Its architecture provides stability, robustness and good performance with simple and small circuitry. One of the main contributions of the proposed topology is the lack of additional building blocks needed in traditional implementations, which produce overhead in power consumption and silicon area. Experimental results of a fabricated integrated-circuit (IC) prototype are shown at the end of the chapter.

Chapter IV presents an improved, lower power consumption and higher performance, version of the first proposed class D audio power amplifier, as well as a second structure with multilevel modulation, to reduce even more the quiescent power consumption. The characteristics of these two class D audio power amplifiers are comparable to the state-of-the-art class D amplifiers but consuming less than one tenth of static power. The two proposed amplifiers were fabricated and tested, and the experimental results are discussed in this chapter.

B. Switching Voltage Regulators

Popularity of switching voltage regulators has multiplied because they offer the advantage of higher power conversion, high efficiency, and superior design flexibility (multiple output voltages of different polarities can be generated from a single input voltage).

Moreover, the efficiency performance of switching voltage regulators, also called switching inductor regulators, is higher than other architectures, like low-dropout regulators (LDOs) or charge-pump regulators. Furthermore, switching voltage regulators present the highest current capability.

A brief introduction to power converters, specially focusing on switching voltage regulators, is presented in Chapter V. It outlines the main power converters architectures, their advantages and drawbacks, the the most common topologies. This chapter also discusses the performance metrics of switching voltage regulators, and some of their practical design constrains. Additionally, a global panorama of the present and future power converters market distribution is presented at the end of the chapter.

Chapter VI describes the design, implementation, and testing of a dual-output buck voltage regulator to show that its monolithic integration is possible, feasible, cheap, and reliable. The proposed dual-output converter delivers a maximum power

efficiency compared to conventional solutions, but minimizing the number of switches, and potentially saving area and number of external components in the input filter. Measured results from a fabricated integrated-circuit prototype are also shown in this chapter.

Chapter VII presents the design and simulation of a fully-integrated buck voltage regulator to show that by integrating the passive components on-chip, the silicon area, cost, and external elements can be reduced and still keeping the efficiency and high-current capability of the voltage switching regulator. Moreover, the design has been done using conventional CMOS technology without any expensive post-fabrication process which reduces even more its potential fabrication cost. However, practical implementation challenges have been found and possible solutions to overcome this drawbacks are discussed.

Finally, Chapter VIII summarizes the contributions of this dissertation and discusses future work.

CHAPTER II

FUNDAMENTALS OF AUDIO POWER AMPLIFIERS

A. Introduction

The audio power amplifiers provide the power to the loudspeaker in a sound system. Audio amplifiers have a history extending back to the 1920s, and with hundreds of thousands amplifiers being built nowadays, they are of considerable economic importance [1]. They can be found in many systems [2] such as televisions, radios, phones, cellular phones, hearing aids, portable audio/video players, desktop, notebook and netbook computers, car audio systems, home theater systems, home audio systems, etc. Therefore, there is a present and future need for high performance, efficient, and reliable audio power amplifiers in a vast number of applications.

This chapter discusses the basic fundamentals of audio amplifiers, their history, classes and principles of operation. Section B introduces the principles of sound, human speech, and frequency bands. Section C explains the fundamentals of audio power amplifiers, presenting a brief history of audio amplifiers, and outlining their different classes. Finally, a formal introduction to class D audio power amplifiers is given in Section D, including their main topologies, performance metrics, practical design considerations, and their global market distribution.

B. Principles of Sound

Unlike electromagnetic waves which propagate through free space, sound waves require a solid, liquid or gas medium to propagate. Sound can be defined as an acoustical or mechanical wave motion in an elastic medium. Air is the most familiar medium but a solid can be better medium for propagation of sound [3]. The sources of sound can be

categorized in six groups [3]: (1) vibrating body (a vibrating vocal cord, a loudspeaker), (2) throttled air stream (a whistle), (3) thermal (a fine wire connected to an alternating current), (4) explosion (a firecracker), (5) arc (thunder) and (6) aeolian or vortex (aeolian harp).

Frequency of a sound wave can be defined only if the wave is periodic in time. The frequency of the wave in Hz (cycles / s) is the reciprocal of the period, i.e. f = 1 / T. The radian frequency is given by $\omega = 2\pi f$ in rad / s. The standard audible band is considered to be from 20 Hz to 20 kHz although a more realistic range can be defined from 30 Hz to 15 kHz. Most people cannot hear frequencies as high as 20 kHz, for example, frequency modulated (FM) broadcasting is limited to 15 kHz bandwidth. On the other end, sounds with a frequency below 30 Hz are felt more than heard.

The infrasonic band is the band below the lowest frequency that can be heard. These sounds are felt and not heard. Some of the organs of the human body can exhibit resonance frequencies in the infrasonic band. On the other hand, the ultrasonic band is the band above the highest frequency that can be heard [3]. Ultrasonic sounds are used in ultrasonic cleaners, traffic detection, ultrasonic imaging in medical applications, burglar alarm systems, remote controls, etc.

Most of the power in human speech is in the frequency band from 200 Hz to 4 kHz. The frequency band of a telephone is normally bounded from 300 Hz to 3 kHz. Only the labial sounds and the fricative sounds have frequencies as high as 8 kHz to 10 kHz, however, there is relatively little power at these frequencies [3].

C. Principles of Audio Power Amplifiers

The audio power amplifier in a sound system must be able to supply the high peak currents required to drive the loudspeaker, which is usually a low impedance load in the 4 Ω - 8 Ω

range. An ideal audio power amplifier must have zero output impedance. In practice, all the audio amplifiers have a non-zero output impedance. Therefore, the impedance must be small when compared to the loudspeaker impedance [3].

The power rating is the most basic amplifier specification, and the test load resistance must be specified as part of the rating. Lower impedances will provide higher output rating. The standard test signal used for power rating measurement is a sine wave with a frequency in the 20 Hz - 20 kHz range. The power rating is obtained by increasing the input level until the output clips. Therefore, if the output voltage of an audio amplifier is defined as

$$v_{OUT}(t) \;=\; V_P \sin\left(\frac{2\pi t}{T}\right) \tag{2.1}$$

where T is the period, then, the average power delivered to the load [3] is given by

$$\begin{aligned} P_{L(ave)} &= \frac{1}{T}\int_0^T \frac{v_{OUT}^2(t)}{R_L}\,dt \\ &= \frac{1}{T}\frac{V_P^2}{R_L}\int_0^T \sin^2\left(\frac{2\pi t}{T}\right)\,dt \\ &= \frac{V_P^2}{2R_L} \;=\; \frac{V_{OUT(RMS)}^2}{R_L} \end{aligned} \tag{2.2}$$

where the units are Watts (W) and $V^2_{OUT(RMS)} = V_P / \sqrt{2}$.

A traditional method to supply more power to the load without using higher power supply is to use a bridged configuration: two identical paths with audio waves inverted drive the same signal. Hence, the effective load impedance seen by each audio path is R_L / 2. Then the voltage across the load is doubled and the load power is quadrupled [3].

1. A Brief History of Audio Power Amplifiers

Audio power amplifiers arose with the need of dealing with impulses which had to remain in a very definite time pattern to be useful. One of the earliest amplifying devices was the pipe organ. However, in a more generally accepted sense, amplifiers were invented

when the nineteenth century technology became concerned with the transmission and reproduction of vibratory power: first sound, and then radio waves [4].

In 1876, Edison patented a device which he called an *aerophone*. It was a pneumatic amplifier in which the speaker's voice controlled the instantaneous flow of compressed air by means of a sound-actuated valve. The air was released in vibratory bursts similar to those that came from the speaker's mouth but more powerful and louder. Later on, an improved *aerophone* was attached to the phonograph [4].

The device which really opened up the field of amplification was the vacuum tube. An early application of vacuum tube was to transmit and receive radio waves. Other applications followed quickly: recording and reproduction of sound, detection and measurement of light, sound, pressure, etc. Later on, the transistor replaced the vacuum tube due to reliability, cheaper cost, size and no warm up period [4].

Push-pull class A amplifiers were dominant until the early 1960s. Designs using germanium devices appeared first, but suffered from the vulnerability of germanium to moderately high temperatures. At first, all silicon transistors were NPN, and for a time most transistors amplifiers relied on input and output transformers for push-pull operation of the output stage. These transformers were heavy, bulky, expensive and very non-linear. Complementary power devices appeared in the late 1960s, and full complementary output stages provided less distortion than their predecessors [1].

2. Audio Power Amplifier Classes

For a long time, the only amplifier classes relevant to high-quality audio were class A and class AB. Class B amplifiers generated so much distortion. Nowadays, solid-state devices gives much more freedom of design, possibilities and architectures. The most important audio power amplifier classes [1], [2] are

- Class A

  In a class A amplifier current flows continuously in all the output devices, which avoids turning on and off their non-linearities. It is the most linear amplifier, however the ideal power efficiency of class A audio amplifiers is only 25%.

- Class B

  In class B amplifier the current flows half of the period in each output device. Linearity of the amplifier is compromised by crossover but theoretical efficiency can reach 78.5%.

- Class AB

  Class AB audio amplifiers are a combination of class A and class B audio power amplifiers. If an amplifier is biased into class B mode, and then the bias is increased, it will become class AB amplifier. For outputs below a certain level, both output devices conduct, and operation is class A mode. At higher levels one device will be turned completely off as the other provides the current. Class AB amplifier eliminates the crossover distortion of class B amplifier. Its efficiency is similar to class B amplifier.

- Class C

  Class C amplifier implies device conduction for less than 50% of the time and is normally used in radio applications.

- Class D

  This amplifier continuously switch the output from one rail to the other at ultrasonic frequency creating a binary signal pulse-width modulated (PWM). Distortion is not inherently low and a sharp low-pass filter (LPF) is usually needed between the amplifier and the speaker, to reduce the high frequency components. Theoretical

efficiency of class D amplifier is 100%.

- Class E

  Class E amplifier operates a transistor with very small voltage across or a small current through almost all the time. This allows to keep the power dissipation very low and reach high efficiency. Class E amplifier is used mostly in RF applications.

- Class G

  The class G amplifier was proposed by Hitachi in 1976 to reduce the amplifier power dissipation. Since musical signals have a high peak/mean ratio at low levels, the dissipation is much less if the amplifier operates from low-voltage rails. On the other hand, for large output signals, the class G amplifier switches to higher voltage rails. The basic class G amplifier operates with two rail voltages, although it can be extended to more supply voltages. Typically the limit is three as a compromise between efficiency and complexity. Theoretical efficiency of class G operating with dual voltage supply reaches 85.9%.

- Class H

  Class H amplifier is an extension of a class G amplifier but with the rail voltage dynamically adapting to the input signal voltage to minimize the losses.

D. Introduction to Class D Audio Power Amplifiers

Class D audio power amplifiers have become very popular because they give the highest efficiency of any of the amplifiers classes, although their performance, particulary in terms of linearity, is not so good [1]. Applications for class D amplifiers can be divided into two main areas: (1) low power outputs and (2) high power outputs. The low power field goes from a few milliwatts (mW) to around 5 W, while the high power applications go from

80 W to 1400 W [1].

The first area of applications includes hearing aids, mobile phones, personal stereos, notebook/netbook computers, portable audio/video players, portable video games, polyphonic ringers, handset speakers, etc. All these products are portable and battery driven, thus high efficiency performance is very important to extend the life of the product [1]. On the other hand, the high-power applications include car audio systems, home theater systems, home audio systems, etc. Class D audio amplifiers are preferred in these applications because they keep power dissipation low and therefore the size of heatsink can be minimized, leading to a smaller, neater and more efficient product [1].

The first work on class D audio amplifiers involved vacuum tubes and goes back to a 1930 patent by Burnice D. Bedford. The idea of class D audio amplifiers resurrected in the 1950s, but the combination of high switching frequencies and valve output transformers limited their development [1].

In 1976, state-of-the-art class D audio amplifiers had a total harmonic distortion (THD) about 5%. The biggest problem of the technology at that time was that bipolar transistors of suitable power-handling capacity were too slow for the switching frequencies required, causing serious losses and producing high levels of distortion. With developing of power FETs, with very fast switching times, class D audio amplifiers became a practical proposition [3].

Class D audio amplifiers are non-linear devices because their output devices work as switches operating at ultrasonic frequency. Figure 1 illustrates the simplified circuit of a conventional class D audio power amplifier.

The class D amplifier, as shown in Fig. 1, consists of a comparator driving a MOSFET output stage and low-pass filter. One input of the differential comparator is driven by the incoming audio signal, and the other by a ultrasonic carrier wave (typically a triangle or sawtooth waveform). The comparator generates a high frequency digital signal pulse-width

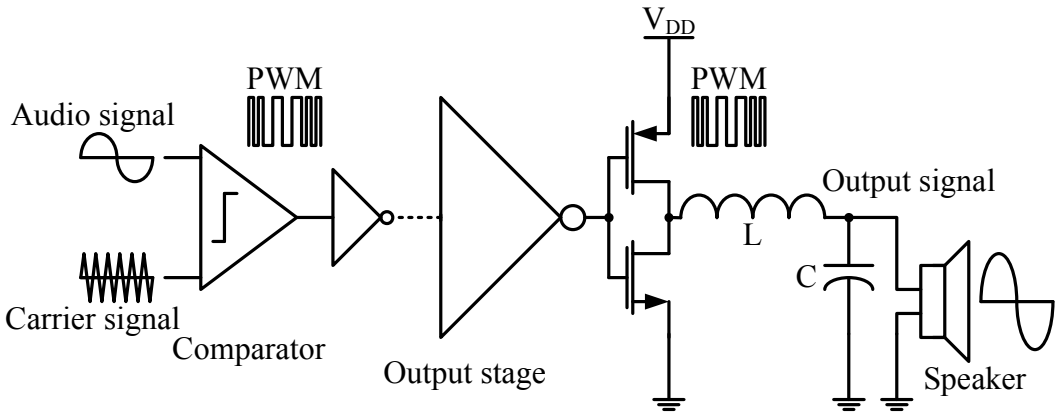


Fig. 1. Conventional class D audio power amplifier architecture

modulated (PWM) whose duty cycle is proportional to the average low-frequency audio signal.

The digital signal is passed through a chain of buffers (inverters) to enhance its driving capability. These inverters are built using switches that toggle between the power supply rails. In theory, these switches have zero resistance when they are turned on (on-resistance), zero voltage across them, and zero power dissipation. On the other hand, the switches have infinite resistance when they are turned off (off-resistance), zero current through them, and none power dissipation. Therefore, in theory, class D audio power amplifiers can achieve perfect transference of power, reaching 100% efficiency. However, in practice, the switches have finite on and off resistances, and optimum sizing of such buffers is crucial to maximize the amplifier's efficiency.

The purpose of the output filter is to remove the high frequency components of the pulse-width modulated signal, and it must be designed to have a flat-frequency response within the audio band (20 Hz - 20 kHz). The typical switching frequency ranges from 50 kHz to 1 MHz. A higher frequency makes the output filter simpler and smaller, but

tends to increase switching losses and consequently, to reduce efficiency.

Class D audio power amplifiers are usually operated in a bridged configuration (H-bridge) to increase the output power without increasing the power supply voltage. It allows, as shown in equation (2.2), to double the voltage swing across the load and increases four times the output power. This method is also called bridge-tied-load (BTL) [1].

1. Overview of Class D Audio Amplifiers Architectures

The architecture of a class D audio amplifier can be classified into four types [5]: (a) pulse-width modulated (PWM), or naturally sampled pulse-width modulated, amplifiers [6]–[9], (b) oversampled $\Delta\Sigma$ amplifiers [10]–[19], (c) bang-bang control amplifiers [20]–[22], and (d) nonlinear control amplifiers [23]–[25].

a. Class D Audio Power Amplifiers Based on Pulse-Width Modulation (PWM)

Class D audio amplifier based on pulse-width modulation, or naturally sampled pulse-width modulation, scheme is the most used architecture [2]. Its circuitry is simple, stable and with low-power consumption. The typical architecture of a class D audio power amplifier based on pulse-width modulation have been shown in Fig. 1.

Pulse-width modulation is based on the simple fact that the mean value of a two-level square wave is proportional to its duty cycle. The modulation is done by comparing the signal to a constant slope carrier. However, the audio signal must be bounded to avoid clipping in the modulation process. Consequently, the amplitude of the audio signal is usually normalized with respect to the carrier wave amplitude and referred to as the modulation index, M where $M \in [0, 1]$.

The Nyquist theorem establishes the minimum sampling frequency, i.e. carrier wave frequency or switching frequency (f_s). However, the Nyquist condition is not sufficient because the slew-rate of the carrier must be higher than the slew-rate of the audio signal

at all times to avoid multiple crossing points within one sample period. For example, for a sinusoidal signal with M = 1, frequency f_a, and a sawtooth carrier, the sampling frequency must be $f_s > \pi f_a$. Also, the nonlinear nature of pulse-width modulation will cause intermodulation of the carrier and the signal frequencies. This increases the practical ratio necessary between the input and modulation frequencies [26].

The switching method of the class D audio power amplifier describes how the output signal is controlled over the load. Usually, the signal is switched between the positive and negative rails to provide a binary signal. However, it is possible to generate a three level modulated signal under certain conditions if the amplifier is used with a bridged configuration.

A class D audio power amplifier with two-level bridge-tied-load (BTL) topology is shown in Fig. 2. As it can be appreciated, the amplifier is the fully-differential version of the conventional class D amplifier in Fig. 1. This modulation is also known as pulse-width modulation AD, or PWM AD [2]. It produces a binary signal with minimum cross-over distortion and zero common-mode components. On absence of signal at the input, the binary signal is a square wave with a 50% duty cycle. Many commercial products [6] are based on this modulation scheme.

Figure 3 illustrates the generation of the two-level pulse-width modulated signal. The audio signal and the carrier wave generate two complementary fully-differential digital signals (PWM+ and PWM-) whose differential voltage is doubled.

Determination of the harmonic frequency components of a pulse-width modulated signal is quite complex and is often done by using a fast Fourier transform (FFT) analysis of a simulated time-varying switched waveform. This approach offers the benefits of a reduced mathematical effort but requires considerable computing capacity and usually leaves uncertainty to simulation errors (specially in systems with higher carrier frequencies) due to time resolution of the simulation and the periodicity of the overall waveform.

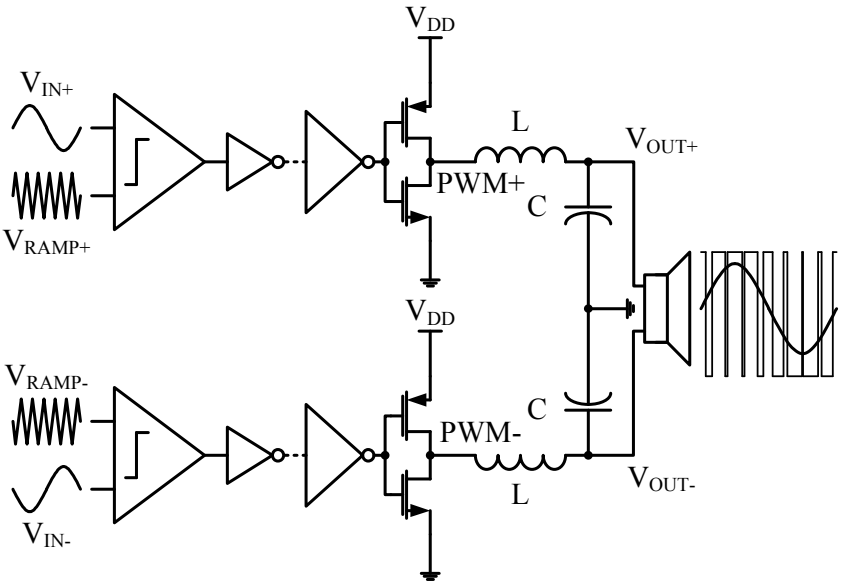


Fig. 2. Two-level bridge-tied-load class D audio power amplifier

In contrast, an analytical solution which exactly identifies the harmonic components of a pulse-width modulated signal ensures that the correct harmonics are being considered. The most well-known analytical method of determining the harmonic components of a pulse-width modulated signal is using the double Fourier integral analysis (DFIA) [5], [26]. This analysis assumes the existence of two time variables, which can be thought of as the high-frequency modulating wave (carrier signal) and the low-frequency modulated wave (baseband audio signal). In general, the value of the function f(t), representing the modulation of a given two time variable waveforms [26], is given by

$$\begin{aligned} f(t) &= \frac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n} \cos\beta + B_{0n} \sin\beta] \\ &+ \sum_{m=1}^{\infty} [A_{m0} \cos\alpha + B_{m0} \sin\alpha] \end{aligned}$$

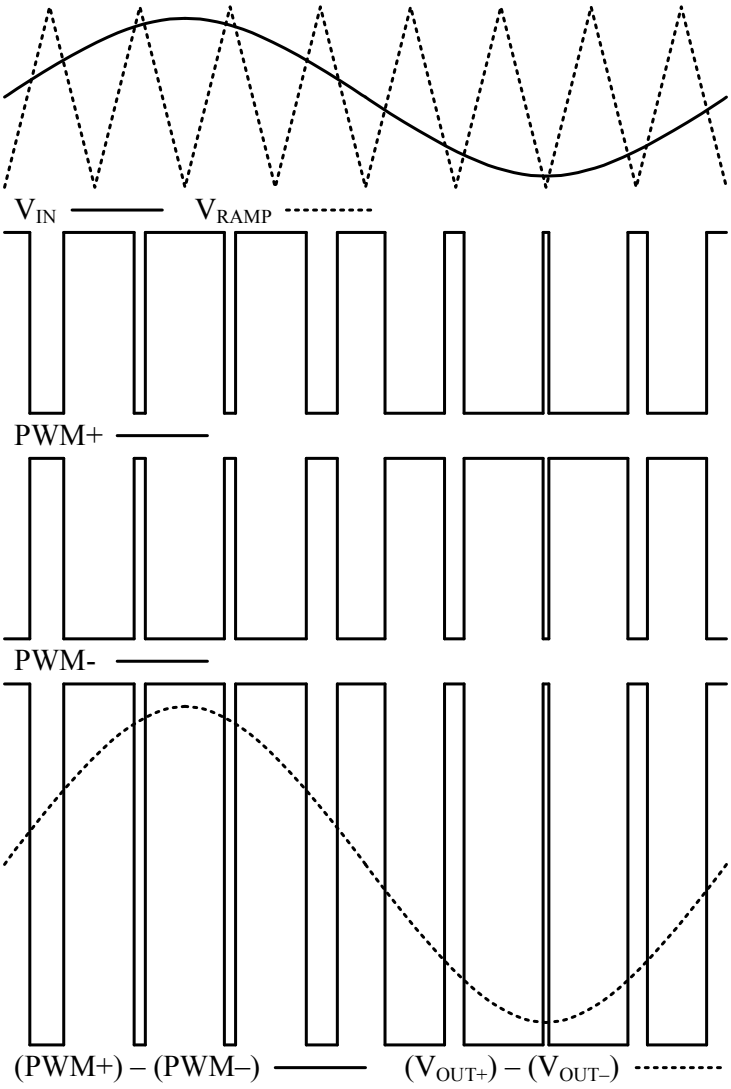


Fig. 3. Generation of two-level pulse-width modulated signal

$$+ \sum_{m=1}^{\infty} \sum_{\substack{n=-\infty \\ (n \neq 0)}}^{\infty} [A_{mn} \cos(\alpha + \beta) + B_{mn} \sin(\alpha + \beta)] \tag{2.3}$$

where

$$\alpha = m(\omega_c t + \theta_c) \tag{2.4}$$

$$\beta = n(\omega_o t + \theta_o) \tag{2.5}$$

and m is the carrier index variable, n is the baseband index variable, ω_c is the carrier angular frequency, θ_c is an arbitrary phase offset angle for the carrier waveform, ω_o is the baseband angular frequency, θ_o is an arbitrary phase offset angle for the baseband waveform, and A_{mn} and B_{mn} are the coefficients of the magnitudes of the harmonic components. In general, the two angular frequencies (ω_c and ω_o) will not be an integer ratio.

The first term of equation (2.3), A_{00} / 2 where m = n = 0, corresponds to the DC offset component of the pulse-width modulated waveform. The first summation term, where m = 0, defines the output fundamental low-frequency (audio signal) and its baseband harmonics (if any). This term includes low-order undesirable harmonics around the fundamental output (harmonic distortion) which should be minimized. The second summation term, where n = 0, corresponds to the carrier wave harmonics, which are relatively high frequency components, since the lowest frequency term is the modulating carrier frequency. The final double summation term, were m, n $\neq$ 0, is the combination of all possible frequencies harmonics formed by taking the sum and difference between the modulating carrier waveform harmonics and the reference waveform and its associated baseband harmonics. These combinations are usually called sideband harmonics [26].

The pulse-width modulated waveform in the class D audio power amplifier can be generated using different carrier waveforms. The most popular are sawtooth waveform, triangle waveform and exponential-shaped waveform.

Figure 4 illustrates an example of naturally sampled modulation using a sawtooth waveform, also called *trailing-edge naturally sampled modulation (TENSM)* [26], where v_{IN}, v_{RAMP}, and v_{PWM} are the input audio signal, the sawtooth carrier waveform and the pulse-width modulated signal. Hence, considering a sinusoidal input audio signal v_{IN} of

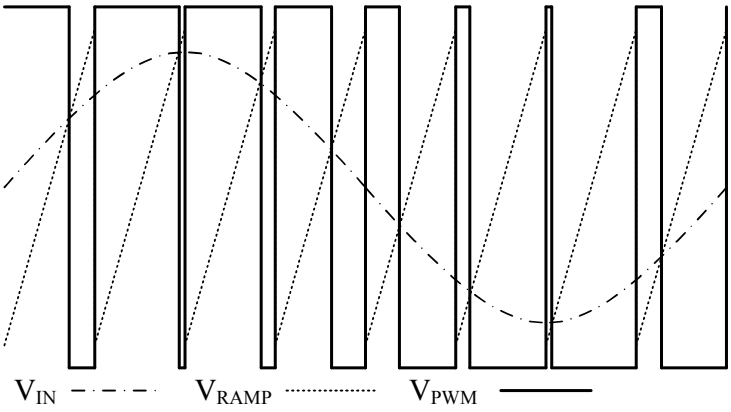


Fig. 4. Sine-sawtooth pulse-width modulation

the form

$$v_{IN}(t) \;=\; M\cos\left(\omega_o t \;+\; \theta_o\right) \tag{2.6}$$

where M is the modulation index, ω_o is the target output frequency, and θ_o is an arbitrary output phase. Then, the resulting pulse-width modulated (v_{PWM}) signal using a sawtooth waveform (v_{RAMP}) can be expressed in terms of its harmonics components, by using the double Fourier integral analysis [26], as

$$\begin{aligned} v_{PWM}(t) \;&=\; V_{DC} \;+\; V_{DC}M\cos\left(\omega_o t \;+\; \theta_o\right) \\ &+\; \frac{2}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\frac{1}{m}[\cos\left(m\pi\right) \;-\; J_0(m\pi M)\sin\alpha] \\ &+\; \frac{2}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\sum_{\substack{n\,=\,-\infty \\ (n\,\neq\,0)}}^{\infty}\frac{1}{m}J_n(m\pi M)\left[\begin{array}{r} \sin\left(n\frac{\pi}{2}\right)\cos\left(\alpha \;+\; \beta\right) \\ -\;\cos\left(n\frac{\pi}{2}\right)\sin\left(\alpha \;+\; \beta\right) \end{array}\right] \end{aligned} \tag{2.7}$$

where V_{DC} is the DC offset component, $J_0(\cdot)$ and $J_n(\cdot)$ are the Bessel functions of the first kind [26], and α and β are the arguments defined in equations (2.4) and (2.5).

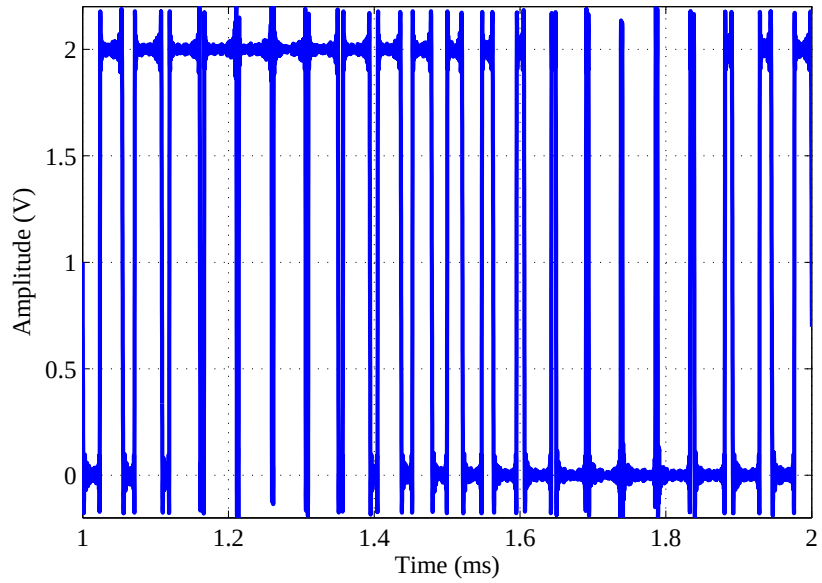


Fig. 5. Two-level pulse-width modulated signal with trailing-edge naturally sampled modulation

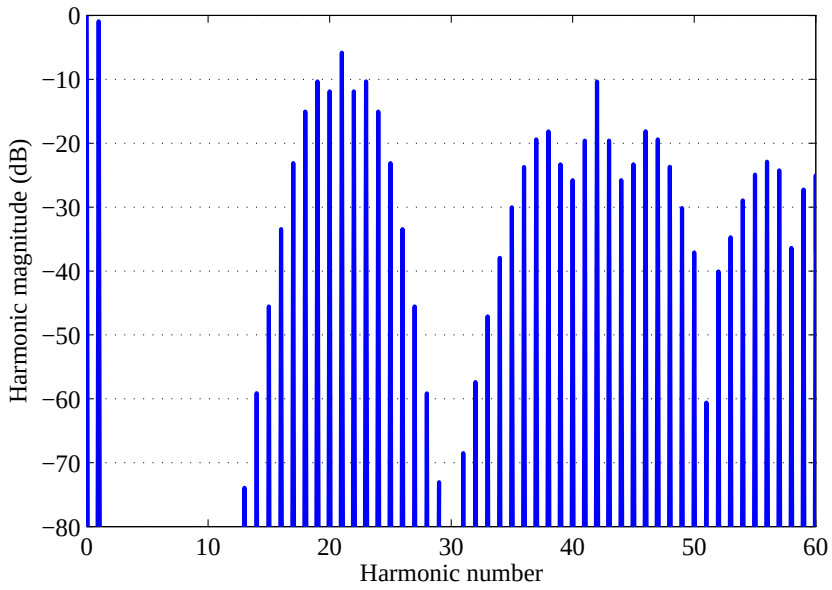


Fig. 6. Harmonic components of two-level pulse-width modulated signal with trailing-edge naturally sampled modulation

The two-level pulse-width modulated signal with trailing-edge naturally sampled modulation in equation (2.7) is plotted in Fig. 5 with coefficients m = n = 50, modulation index M = 0.9, V_{DC} = 1 V and $\omega_c / \omega_o = 21$. Also, in Fig. 6, the spectrum of the pulse-width modulated signal with trailing-edge naturally sampled modulation is presented. Notice that there are no baseband harmonics in the pulse-width modulated signal, since the second term in equation (2.7) contains only the fundamental tone, therefore the harmonic distortion is zero.

The more common form of naturally sampled pulse-width modulation employs a triangular carrier wave instead of a sawtooth carrier as shown in Fig. 7. This type of modulation is also called *double-edge naturally sampled modulation (DENSM)* [26].

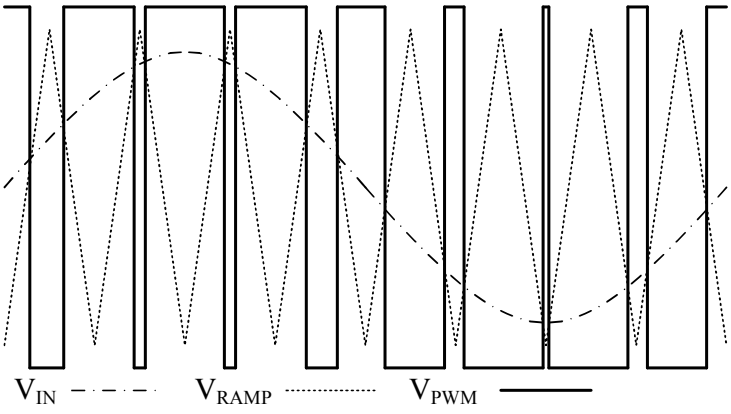


Fig. 7. Sine-triangle pulse-width modulation

The pulse-width modulated signal using a triangular carrier waveform can also be expressed in terms of its harmonic components. Hence, by using the sinusoidal waveform

v_{IN} given in equation (2.6), and applying the double Fourier integral analysis [26], the pulse-width modulated (v_{PWM}) signal with double-edge naturally sampled modulation scheme is given by

$$\begin{aligned} v_{PWM}(t) &= V_{DC} + V_{DC}M\cos(\omega_o t + \theta_o) \\ &+ \frac{4}{\pi}V_{DC}\sum_{m=1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right)\sin\left(m\frac{\pi}{2}\right)\cos\alpha] \\ &+ \frac{4}{\pi}V_{DC}\sum_{m=1}^{\infty}\sum_{\substack{n=-\infty \\ (n\neq 0)}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin\left([m+n]\frac{\pi}{2}\right)\cos\gamma \end{aligned} \quad (2.8)$$

where

$$\gamma = \alpha + \beta \quad (2.9)$$

and V_{DC} is the DC offset component, $J_0(\cdot)$ and $J_n(\cdot)$ are the Bessel functions of the first kind [26], and α and β are the arguments defined in equations (2.4) and (2.5).

Figure 8 shows the two-level pulse-width modulated signal with double-edge naturally sampled modulation in equation (2.8) with coefficients m = n = 50, modulation index M = 0.9, V_{DC} = 1 V and ω_c / ω_o = 21, and Fig. 9 illustrates its harmonic components.

As in the previous modulation scheme (trailing-edge naturally sampled modulation), expressed in equation (2.7), there are no baseband harmonic components in the double-edge naturally sampled modulation signal because the second term in equation (2.8) contains the fundamental tone only, and therefore the harmonic distortion is also zero. Also notice that the power spectrum of the modulated signal with double-edge naturally sampled modulation contains much less carrier harmonic components than the power spectrum of the modulated signal with trailing-edge naturally sampled modulation.

The previous modulation schemes, trailing-edge and double-edge naturally sampled, have shown a perfect modulation with zero baseband harmonic distortion. However, in reality, total harmonic distortion is non-zero due to non-ideal carrier waveforms.

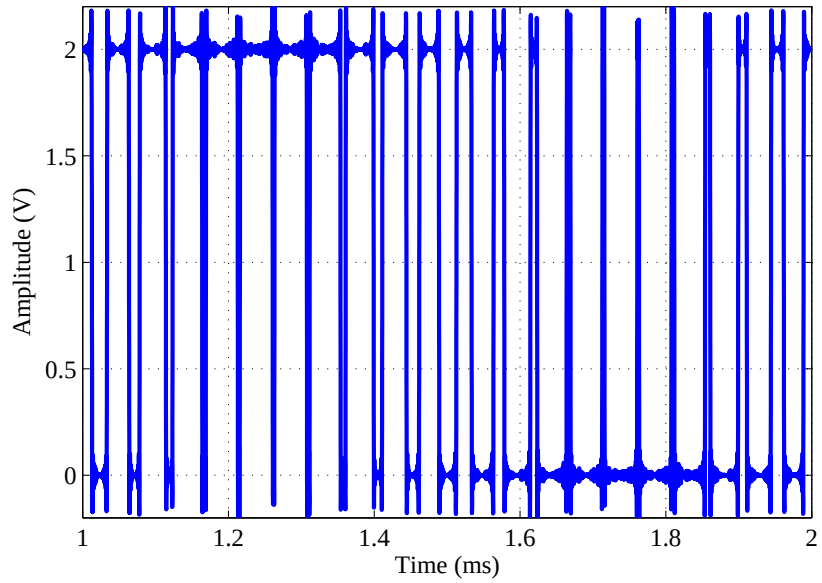


Fig. 8. Two-level pulse-width modulated signal with double-edge naturally sampled modulation

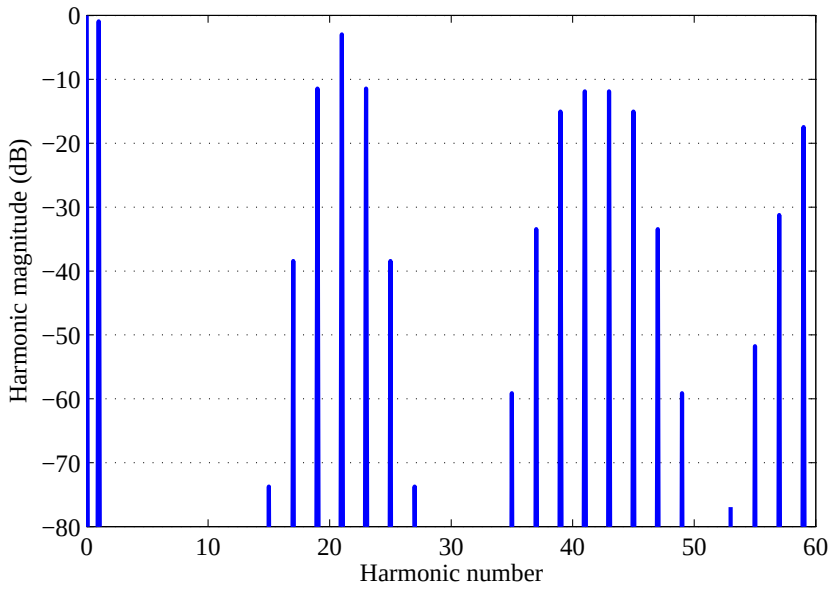


Fig. 9. Harmonic components of two-level pulse-width modulated signal with double-edge naturally sampled modulation

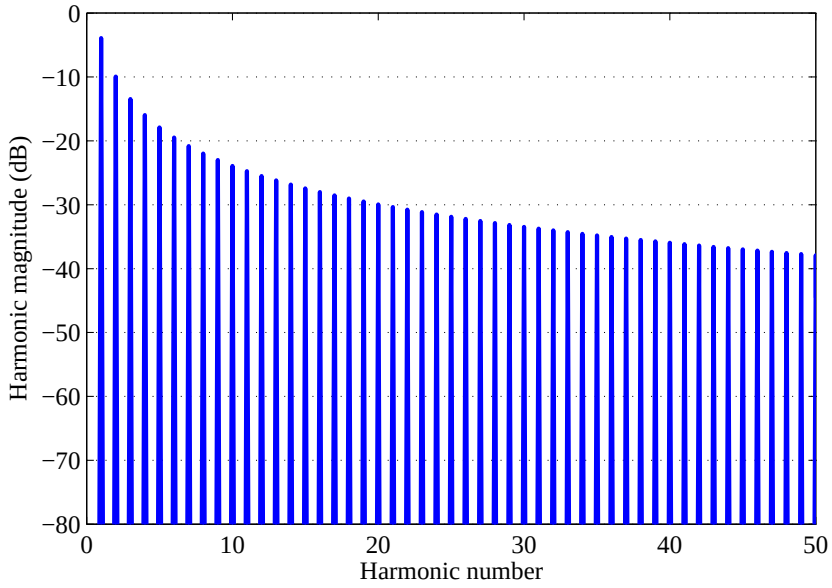


Fig. 10. Harmonic components of sawtooth carrier waveform

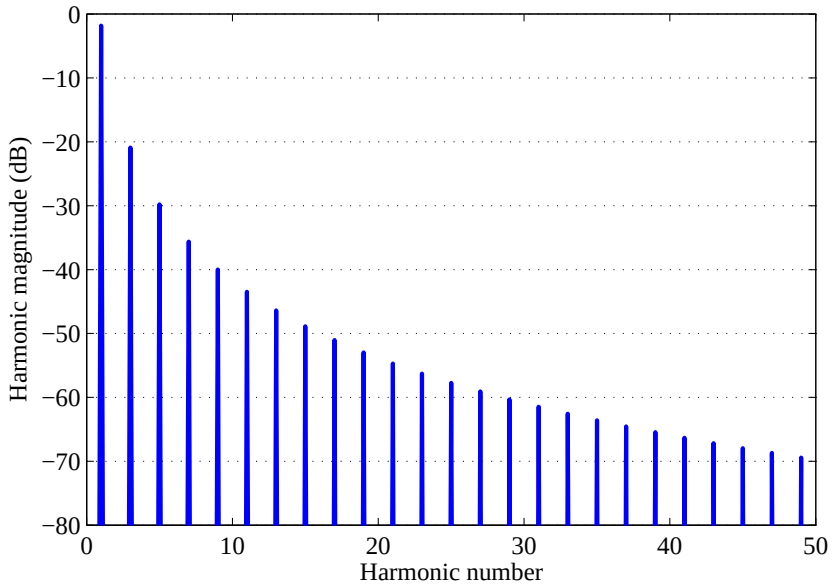


Fig. 11. Harmonic components of triangle carrier waveform

If we define the carrier waveforms in terms of their harmonic components, then an ideal sawtooth carrier waveform f_s can be expressed as

$$f_s(t) = \frac{1}{2} - \frac{1}{\pi}\sum_{i=1}^{\infty}\frac{1}{i}\sin(2i\pi t f_c) \tag{2.10}$$

and an ideal triangle carrier waveform f_t would be

$$f_t(t) = \frac{8}{\pi^2}\sum_{i=1,3,5,\ldots}^{\infty}\frac{(-1)^{(i-1)/2}}{i^2}\sin(2i\pi t f_c) \tag{2.11}$$

Figure 10 and Fig. 11 show the sawtooth carrier waveform and the triangle carrier waveform, respectively, in terms of their harmonic components, and Fig. 12 shows the carrier waveforms with only fifty harmonic considered (i = 50). Therefore, it would be necessary to implement and infinite bandwidth system to generate a perfect carrier signal to obtain zero harmonic distortion in the class D audio power amplifier. Unfortunately,

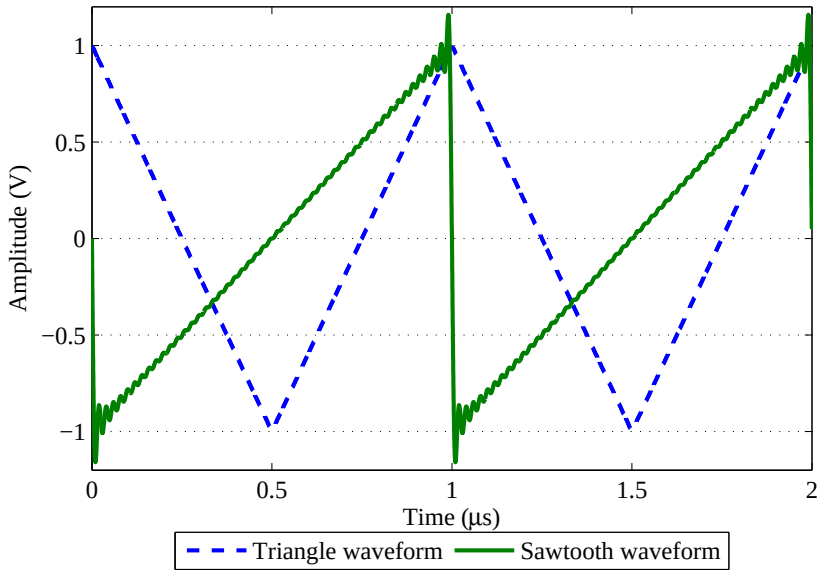


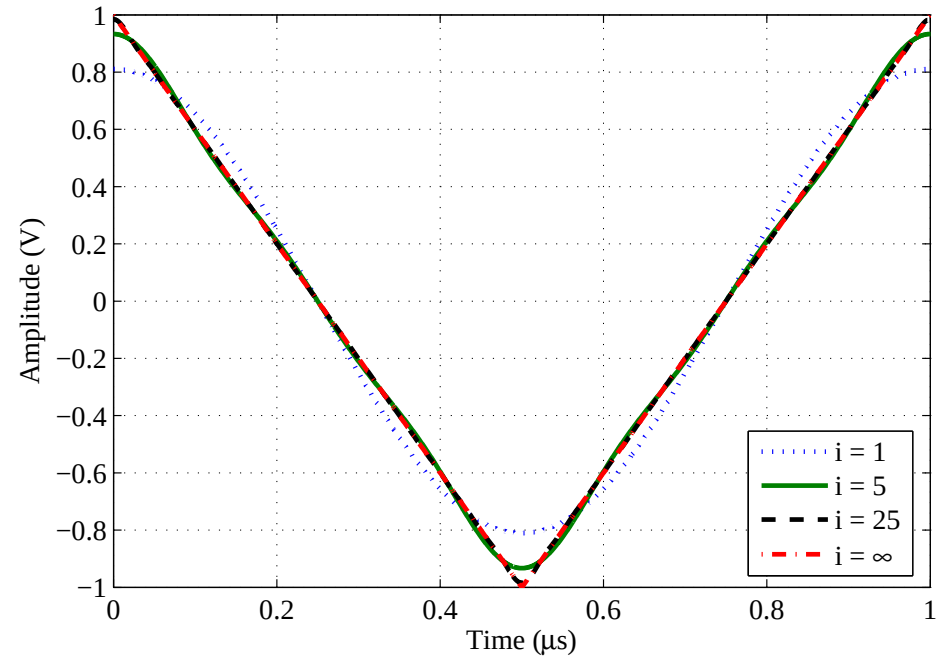
Fig. 12. Triangle and sawtooth waveforms with only fifty harmonic components

band-limited systems degrade the performance of the overall class D audio amplifier by generating undesired baseband harmonic components.

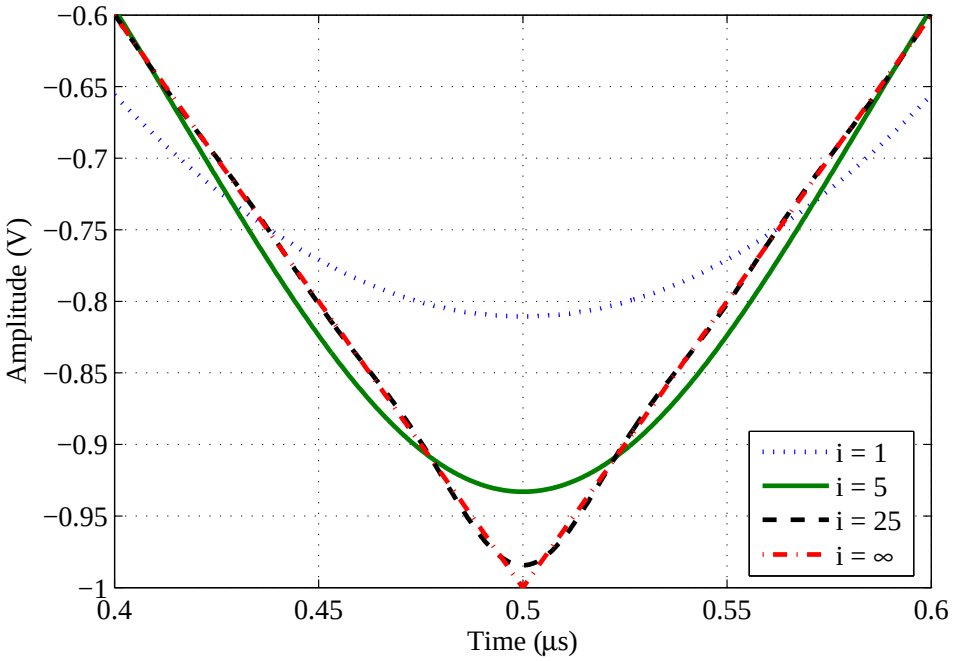
Consequently, we propose to examine the linearity performance of the class D audio power amplifiers by analyzing the harmonic components of their carrier waveforms. A similar analysis has been proposed in [5] in order to model the carrier waveform employing the double Fourier integral analysis. This mathematical derivation is accurate but its complexity and procedure are extensive and tedious, and it has been only applied to a specific carrier waveform. Instead, we evaluate the carrier waveform with the pulse-width modulation (PWM) analysis by duty-cycle variation (ADCV) along with the Jacobi-Anger expansions [26].

The pulse-width modulation analysis by duty-cycle variation assumes that the input audio signal is constant within each carrier cycle, i.e. $\omega_c \gg \omega_o$, which is usually the case. The theory and derivations of the analysis by duty-cycle variation are detailed in Appendix A, and only the main results are shown in this chapter.

Recall that a sawtooth/triangular wave carrier signal is constructed by an infinite sum of sinusoidal functions as expressed previously in equations (2.10) and (2.11), and since there are no unlimited bandwidth systems, the number of harmonics (i) in the carrier signals must be finite. Analyzing the latter case, a triangular wave carrier signal is plotted in Fig. 13(a) for different number of harmonic components. Observe that as the number of harmonic components increases, the triangular waveform approaches more to the ideal one. This phenomenon can be appreciated better in the magnified plot in Fig. 13(b). As a result of the finite number of harmonic components in the carrier waveform, the baseband harmonics of the pulse-width modulated signal, i.e. harmonic distortion, become non-zero and degrade the linearity performance of the class D audio amplifier.



(a)



(b)

Fig. 13. (a) Triangular wave carrier signal for different number of harmonic components and (b) Magnified view

Continuing with the analysis of the triangular waveform, there are two trivial cases regarding the number of harmonics contained in the carrier signal, and the harmonic distortion they produce: (1) when the number of harmonics is infinite the triangle wave is ideal and the baseband harmonic components are zero, and (2) when the number of harmonics is one the triangle wave is a pure sinusoidal signal and the baseband harmonic components become dependents of the modulation index. Applying the analysis by duty cycle variation, as shown in Appendix A, to the second case, i.e. when the number of harmonics is one, the original pulse-width modulated signal expressed before in equation (2.8) becomes

$$\begin{aligned} v_{PWM}(t) &= 2V_{DC}\arccos\left(\arcsin\left[2\sum_{n=1}^{\infty}\sin\left(n\frac{\pi}{2}\right)J_n\left(-\frac{1}{8}\pi^2 M\right)\cos\beta\right]\right) \\ &+ \frac{4}{\pi}V_{DC}\sum_{m=1}^{\infty}\sin\left(m\arccos\left[-\frac{1}{8}\pi^2 M\cos\left(\omega_o t + \theta_o\right)\right]\right)\cos\alpha \end{aligned} \quad (2.12)$$

where V_{DC} is the DC offset component, $J_n(\cdot)$ is the Bessel function of the first kind [26], and α and β are the arguments defined in equations (2.4) and (2.5).

Opposite to the pulse-width modulated signal with a pure triangle waveform derived previously in equation (2.8), the pulse-width modulated signal with a triangle waveform with only one harmonic component in equation (2.12) contains the fundamental tone with baseband harmonic components, whose magnitudes are proportional to the modulation index, which produce unwanted harmonic distortion.

Figure 14 illustrates graphically the baseband harmonic distortion, expressed as total harmonic distortion (THD), as a function of the modulation index M when the triangular carrier waveform contains only one harmonic component. This figure also shows the results of a simulated class D amplifier with a single tone carrier signal in order to compare the results. Notice that the harmonic distortion increases as the modulation index increases as expected from equation (2.12).

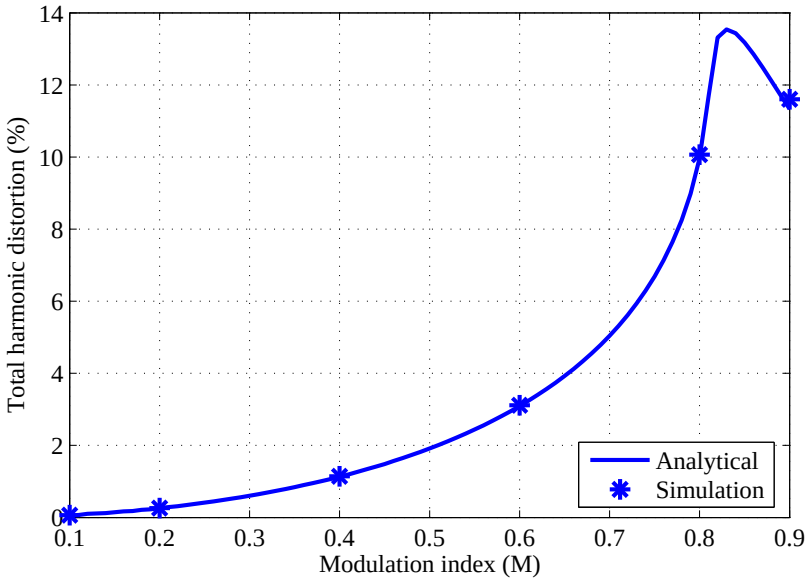


Fig. 14. Total harmonic distortion of class D amplifier when triangle carrier waveform contains one harmonic component

The analysis by duty-cycle variation can be extended to any triangular carrier waveform with specific number of harmonic components (bandwidth), however, the only closed-form solutions exist when the number of harmonic components are i = 1 and i = ∞. The solution of the pulse-width modulated signal when the number of harmonic components in the triangular waveform carrier signal is $1 < i < \infty$ must be calculated numerically.

The numerical and simulated results of total harmonic distortion for triangular waveforms with different number of harmonic components are displayed in Fig. 15, where the analytical results are plotted with solid lines and the simulated results with markers. Observe that the distortion decreases as the number of harmonic components increases. Also, notice that the mathematical analysis predicts with very high accuracy the simulation results.

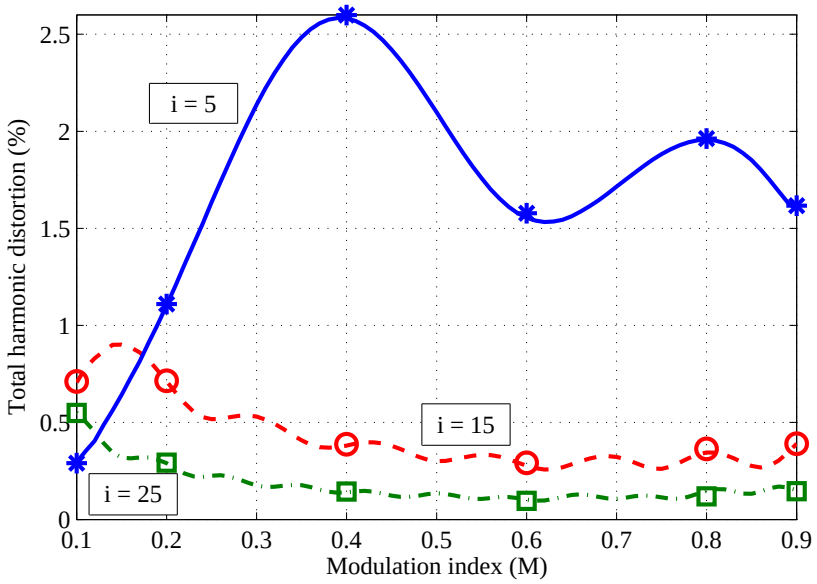


Fig. 15. Total harmonic distortion of class D amplifier when triangle carrier waveform contains different number of harmonic components

Therefore, the analysis of the pulse-width modulated signal by duty-cycle variation can be employed to limit the bandwidth of the class D audio amplifier according to the desired harmonic distortion. In other words, the maximum total harmonic distortion allowed in a given class D audio amplifier design will define the number of harmonic components of the triangular waveform, and consequently, the bandwidth of the system.

Harmonic distortion of class D audio power amplifiers based on sawtooth modulation can also be analyzed using the duty-cycle variation method.

In practice, a common carrier signal used to generate a naturally sampled pulse-width modulation is an exponential-shaped waveform due to its relatively simple implementation. The exponential-shaped waveform is usually generated by charging and discharging a simple RC integrator circuit with square pulses [3], [5], [8], [27], [28]. Figure 16 illustrates the pulse-width modulated signal based on an exponential-shaped carrier waveform.

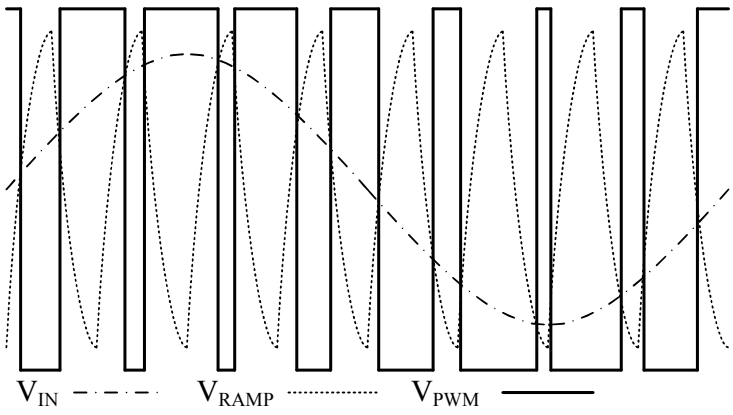


Fig. 16. Sine-exponential-shaped pulse-width modulation

The exponential-shaped waveform f_e can be defined as

$$f_e(t) = \begin{cases} V_{DC}\left(2\dfrac{\exp\left(-\dfrac{t+\frac{T_c}{2}}{t_0}\right)-N_e}{(1-N_e)}-1\right) & \text{when} \quad -\dfrac{T_c}{2} < t < 0 \\ V_{DC}\left(2\dfrac{1-\exp\left(-\dfrac{t}{t_0}\right)}{(1-N_e)}-1\right) & \text{when} \quad 0 < t < \dfrac{T_c}{2} \end{cases} \tag{2.13}$$

where

$$t_0 = -\frac{T_c}{2\ln N_e} \tag{2.14}$$

and V_{DC} is the DC offset component, T_c is the period of the carrier waveform, and N_e is the normalized voltage error between the maximum possible value of the square pulse into the RC network and the actual voltage at which the RC network is discharged (RC constant).

The carrier waveform defined by equation (2.13) resembles an exponential-shaped waveform when N_e is small because the voltage error is minimum and the charging time

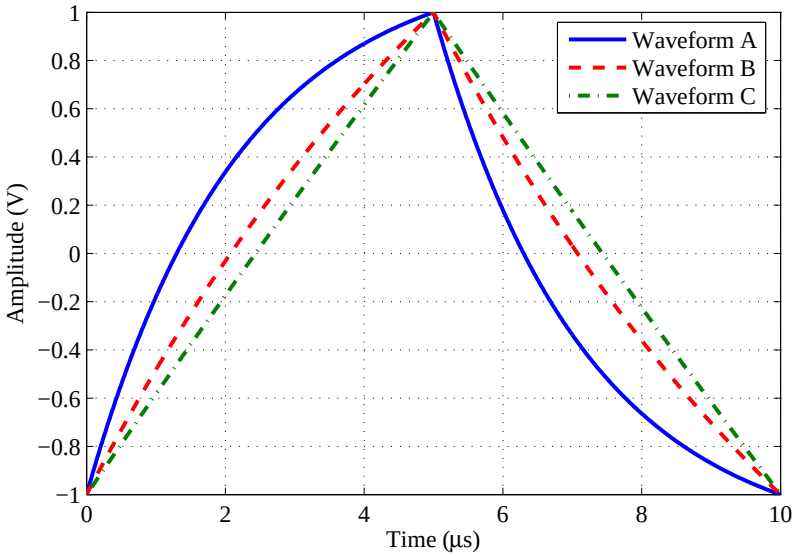


Fig. 17. Family of exponential-shaped waveforms for different values of N_e

is maximum. On the other hand, when N_e is large, the carrier waveform approaches a triangular-shaped waveform because the voltage error is maximum and the linear region is dominant. For example, a family of exponential-shaped waveforms is shown in Fig. 17, where the values of N_e are 0.1, 0.3, and 0.9 for the waveforms A, B, and C, respectively. Observe the exponential shape of waveform A when N_e = 0.1, and the triangular shape of waveform C when N_e = 0.9.

The pulse-width modulation analysis by duty-cycle variation can also be applied to the exponential-shaped carrier waveform, as detailed in Appendix A. In general, a pulse-width modulated signal with exponential-shaped carrier waveform can be expressed as the summation of its Fourier coefficients (a_m and b_m) as

$$v_{PWM}(t) = \frac{a_0}{2} + \sum_{m=1}^{\infty} (a_m \cos\alpha + b_m \sin\alpha) \tag{2.15}$$

where

$$a_0 = \frac{2}{\pi}V_{DC}\left[-t_0\ln\left(1 - \frac{1}{2}[1 - N_e]\left[\frac{M}{V_{DC}}\cos\phi + 1\right]\right) + \pi + t_0\ln\left(\frac{M}{2V_{DC}}\cos\phi[1 - N_e] + \left[\frac{(1 + N_e)}{2}\right]\right)\right] \quad (2.16)$$

$$a_m = \frac{2}{m\pi}V_{DC}\left[\sin\left[-mt_0\ln\left(1 - \frac{1}{2}[1 - N_e]\left[\frac{M}{V_{DC}}\cos\phi + 1\right]\right)\right] - \sin\left[-m\pi - mt_0\ln\left(\frac{M}{2V_{DC}}\cos\phi[1 - N_e] + \left[\frac{(1 + N_e)}{2}\right]\right)\right]\right] \quad (2.17)$$

$$b_m = \frac{2}{m\pi}V_{DC}\left[\cos\left[-mt_0\ln\left(1 - \frac{1}{2}[1 - N_e]\left[\frac{M}{V_{DC}}\cos\phi + 1\right]\right)\right] - \cos\left[-m\pi - mt_0\ln\left(\frac{M}{2V_{DC}}\cos\phi[1 - N_e] + \left[\frac{(1 + N_e)}{2}\right]\right)\right]\right] \quad (2.18)$$

$$\phi = \omega_o t + \theta_o \quad (2.19)$$

and V_{DC} is the DC offset component, ω_o is the audio signal angular frequency, θ_o is an arbitrary phase shift, and α is the argument defined in equation (2.4).

The harmonic distortion (baseband harmonic components) of the pulse-width modulated signal in equation (2.15) can be calculated for any given exponential-shaped carrier waveform. Figure 18 shows the total harmonic distortion of a class D amplifier for the carrier waveforms shown in Fig. 17. Analytical results are plotted with solid lines and the simulation results, using the same carrier waveforms, are plotted with markers. Notice that the analytical results match the simulation results. Also, as expected, the distortion of the amplifier decreases as the carrier waveform approaches a triangular-shaped waveform.

A class D audio power amplifier with three-level bridge-tied-load (BTL) topology is shown in Fig. 19. Notice that the three-level modulation is only possible in a differential architecture. Some commercial class D audio power amplifiers [7] employ this modulation scheme. This modulation is also known as pulse-width modulation BD, or PWM BD [2].

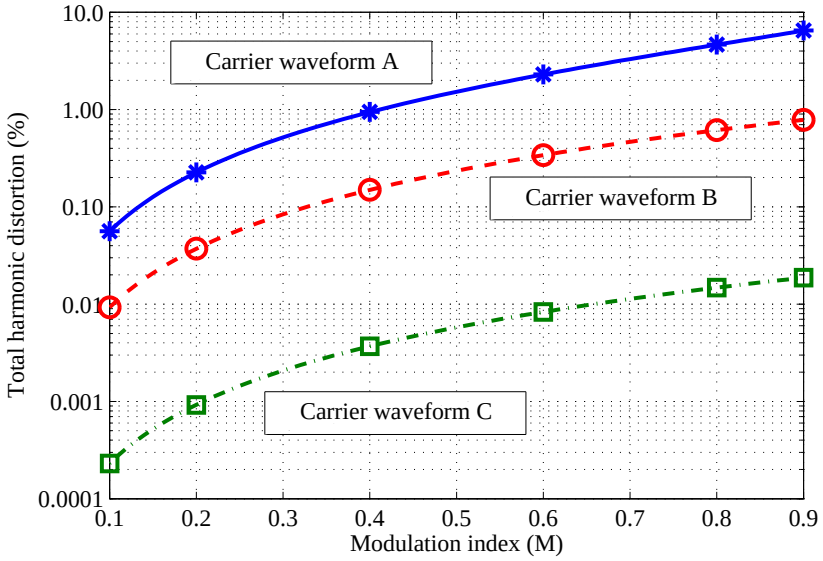


Fig. 18. Total harmonic distortion of class D amplifier for different exponential-shaped carrier waveforms

It generates a ternary signal which produces no output pulses on absence of an audio signal at the input. On the other hand, when the input audio signal is positive the pulse-width modulated signal is constructed with positive pulses, and during negative cycles of the input audio signal the modulation generates negative pulses. Also, the effective switching frequency, as it will be shown later, is twice of the reference carrier waveform. The higher the frequency, the better the filter attenuates unwanted frequencies and the residual ripple is minimized.

However, the three-level modulation scheme suffers of significant electro-magnetic interference (EMI) from the common mode output signal because this signal swings rail-to-rail at the amplifier switching frequency. Then, the class D amplifier requires to be mounted as close as possible to the loudspeaker. Another potential problem of the three-level modulated class D amplifier is the crossover distortion. This problem can be eliminated by

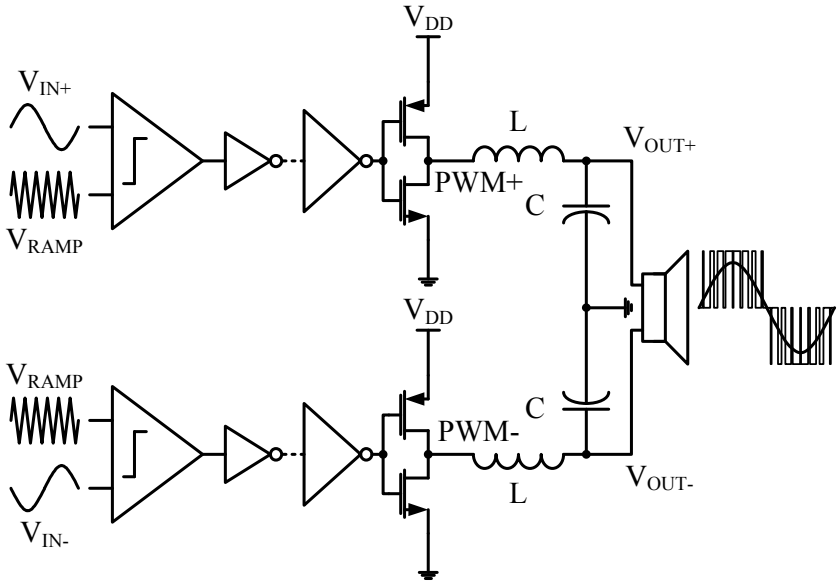


Fig. 19. Three-level bridge-tied-load class D audio power amplifier

designed the power stage logic so that the class D amplifier puts out very narrow alternating positive and negative pulses in the absence of an input signal [2], [3], [29].

Figure 20 details the generation of the three-level pulse-width modulated signal. The audio signal and the carrier wave generate two complementary out-of-phase digital signals (PWM+ and PWM-) whose differential voltage creates a third modulation level.

The three-level modulated signal is created because a fully-differential audio input signal is compared with the same triangular waveform carrier. In other words, one of the pulse-width modulated outputs is inverted in time within one sampled period.

Three-level pulse-width modulated signals can also be generated using the other carrier waveforms (sawtooth waveform, exponential-shaped waveform). Moreover, the harmonic components of all the modulation schemes can be analyzed by using the double Fourier integral analysis and/or the analysis by duty-cycle variation along with the Jacobi-

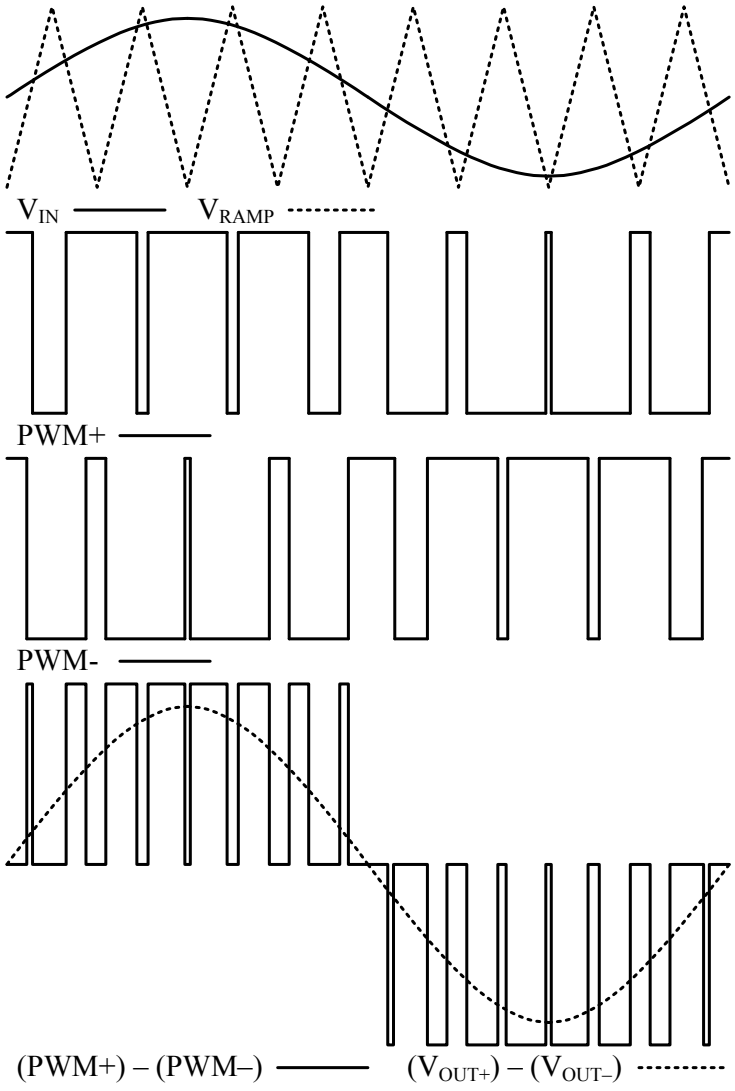


Fig. 20. Generation of three-level pulse-width modulated signal

Anger expansions [26]. For example, the ternary pulse-width modulated signal with a sawtooth waveform carrier (trailing-edge naturally sampled modulation) is given by

$$v_{PWM}(t) \quad = \quad 2V_{DC}M\cos\phi$$

$$+ \quad \frac{4}{\pi} V_{DC} \sum_{m\,=\,1}^{\infty} \sum_{\substack{n\,=\,-\infty \\ (n\,\neq\,0)}}^{\infty} \frac{1}{m} J_n(m\pi M) \sin\left(n\frac{\pi}{2}\right) \cos\left(\alpha\,+\,\beta\right) \qquad (2.20)$$

and the the ternary pulse-width modulated signal with a triangular waveform carrier (double-edge naturally sampled modulation) is given by

$$\begin{aligned} v_{PWM}(t) &= 2V_{DC} M \cos\phi \\ &+ \frac{8}{\pi} V_{DC} \sum_{m\,=\,1}^{\infty} \sum_{n\,=\,-\infty}^{\infty} \frac{1}{2m} J_{2n\,-\,1}(m\pi M) \\ &\times \cos\left([m\,+\,n\,-\,1]\pi\right) \cos\left(2\alpha\,+\,[2n\,-\,1]\phi\right) \end{aligned} \qquad (2.21)$$

where V_{DC} is the DC offset component, M is the modulation index, $J_{(\cdot)}(\cdot)$ is the Bessel function of the first kind [26], and α, β, and ϕ are the arguments defined in equations (2.4), (2.5), and (2.19). Figure 21 shows the time domain representation of the three-level pulse-width modulated signal in equation (2.20) with coefficients m = n = 50, modulation index M = 0.9, V_{DC} = 1 V and ω_c / ω_o = 21, and Fig. 22 illustrates its harmonic components. Observe that all harmonics where coefficient n is even are canceled and the harmonic composition is significantly less than the two-level pulse-width modulated signal plotted in Fig. 6.

The three-level pulse-width modulated signal in equation (2.21) with coefficients m = n = 50, modulation index M = 0.9, V_{DC} = 1 V and ω_c / ω_o = 21 is shown in Fig. 23, and Fig. 24 plots its harmonic spectra. Note that the indices m and n produce only even carrier multiples (2m) with odd sideband harmonics (2n - 1), and the effective switching frequency of the carrier waveform is doubled. As in the previous case, the number of harmonic components have significantly decreased when compared to the two-level pulse-width modulated signal shown in Fig. 9.

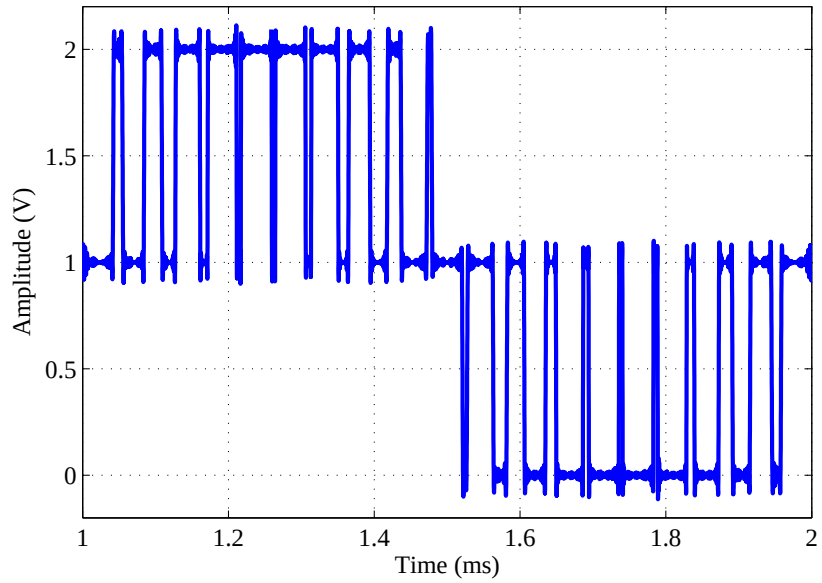


Fig. 21. Three-level pulse-width modulated signal with trailing-edge naturally sampled modulation

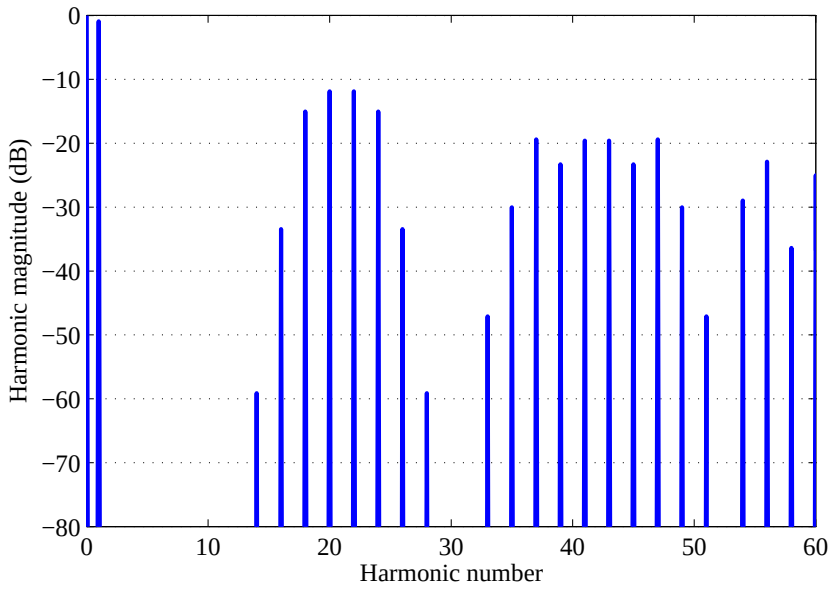


Fig. 22. Harmonic components of three-level pulse-width modulated signal with trailing-edge naturally sampled modulation

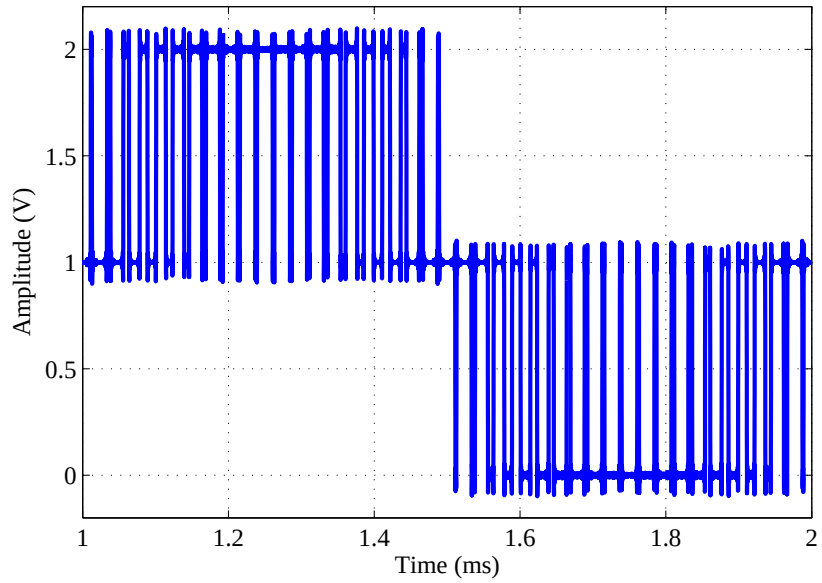


Fig. 23. Three-level pulse-width modulated signal with double-edge naturally sampled modulation

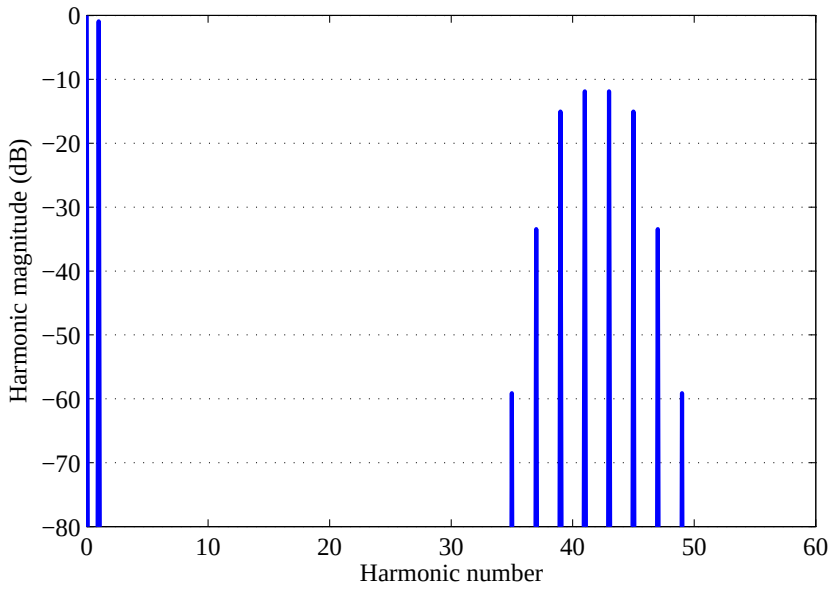


Fig. 24. Harmonic components of three-level pulse-width modulated signal signal with double-edge naturally sampled modulation

The analysis of two-level pulse-width modulation harmonic distortion can also be extended to three-level pulse-width modulation signals, and even multi-level pulse-width modulation schemes, to determine the necessary characteristics, i.e. bandwidth, number of harmonic components, etc., of the carrier waveform for a given linearity specification.

Class D audio power amplifiers are inherently open-loop systems, and, as it has been seen before, their linearity performance relies heavily on the quality of the carrier waveform. Moreover, they provide very poor power-supply rejection ratio (PSRR) and do not have gain control [2]. On the other hand, the open-loop architecture is simple, more efficient, and occupy smaller area [5]. In practice, they are used for low quality applications [2].

Negative feedback is often used around the conventional class D amplifier to improve

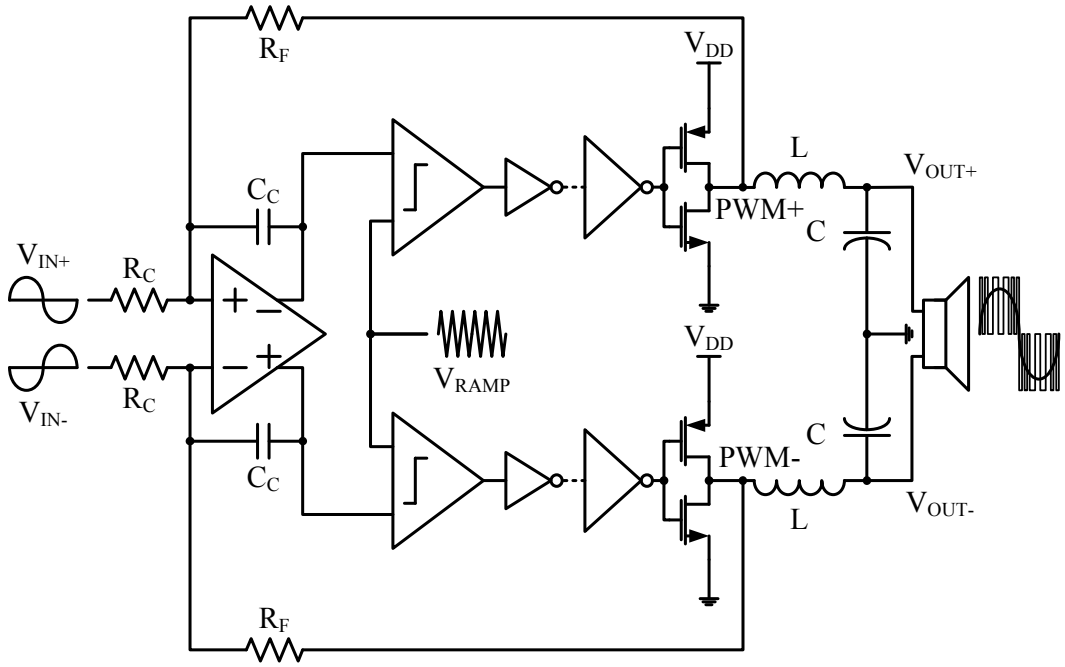


Fig. 25. Conventional class D audio power amplifier with negative feedback

its performance [3]. The closed-loop architecture [2], [3], [8], [9] in Fig. 25 provides an improved topology with more robustness to non-ideal effects. The negative feedback increases linearity and improves the power-supply rejection ratio [2], [3], [30]–[32].

The input of the operational amplifier (OPAMP) in Fig. 25 acts as an integrator to set the system bandwidth. For a sinusoidal input audio signal with frequency much lower than the switching frequency, the effective transfer function for the class D audio amplifier in closed-loop and its pole frequency (f_0) [3] are given by

$$\frac{PWM(s)}{V_{IN}(s)} = -\frac{R_F}{R_C}\left(\frac{1}{1+\frac{s}{\omega_0}}\right) \tag{2.22}$$

and

$$w_0 = 2\pi f_0 = \frac{k}{R_F C_C} \tag{2.23}$$

where k is the class D audio amplifier effective gain which is given by the ratio of the amplitude of the pulse-width modulated signal (V_{DD}) and the amplitude of the carrier waveform (V_{RAMP}).

The pole frequency f_0 must be greater than the highest frequency to be amplified but lower than the switching frequency. A typical value of f_0 is 60 kHz [3].

b. Class D Audio Power Amplifiers Based on Oversampled $\Delta\Sigma$

A class D audio power amplifier based on oversampled $\Delta\Sigma$ modulation is essentially designed as an analog-to-digital converter (ADC). The topology of the class D audio amplifier based on oversampled $\Delta\Sigma$ modulator consists of a closed-loop system, as shown in Fig. 26, whose principle is to make rough evaluations of the output signal PWM, measure the error with respect to the input signal V_{IN}, integrate it and then compensate for that error. The number of integrators, and consequently, the numbers of feedback loops, indicates the order of a $\Delta\Sigma$ modulator [5], [10]–[19].

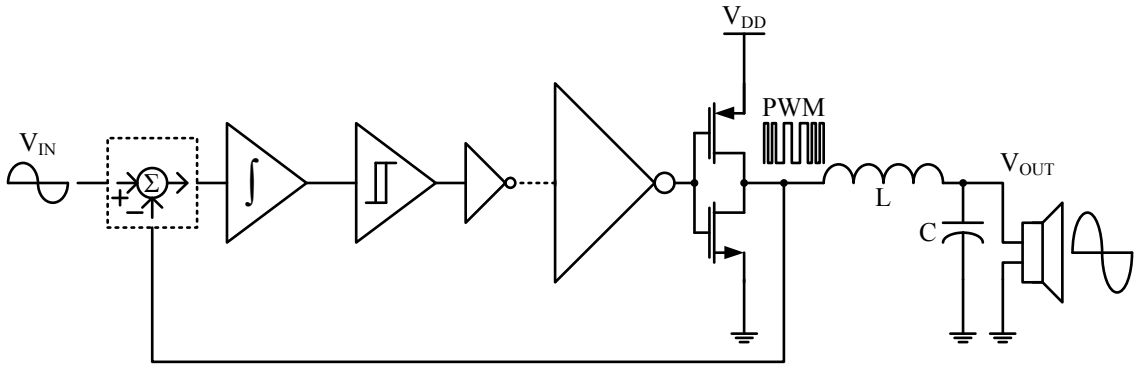


Fig. 26. Class D audio power amplifier based on oversampled $\Delta\Sigma$

Although the $\Delta\Sigma$ modulator was first introduced in the early 1960s, it did not gain importance until recent developments in silicon technology [10]–[18]. Even though the application of analog-to-digital converters based on $\Delta\Sigma$ modulation has become popular in industry, there are still very few commercial class D audio power amplifiers [19] based on this modulation technique.

Class D audio amplifiers based on $\Delta\Sigma$ modulation have the additional benefit of shaping the quantization noise away from signals of interest [10]–[18]. In other words, if the transfer function of the circuit is analyzed from the input signal V_{IN} to the output node V_{OUT}, the result is a low-pass filter shaped function that reproduces the low-frequency input signal. On the other hand, if the transfer function of the amplifier is analyzed from the power supply V_{DD} (source of quantization/switching noise) to the output node V_{OUT}, the resulting transfer function is a high-pass filter that minimizes the noise at low frequencies. Also, when the switching frequency increases (higher oversampling ratio), the signal-to-noise ratio (SNR) also increases, but the overall efficiency of the class D amplifier decreases.

Class D audio amplifiers based on $\Delta\Sigma$ modulation provide very high linearity but their

implementation in real audio applications is complicated [10]–[12]. Other drawback is that the amplifiers based on $\Delta\Sigma$ modulation consume much more power and silicon area when compared to the class D audio amplifier based on pulse-width modulation. This increased power dissipation and hardware overhead are consequences of the circuit complexity and higher switching frequency [5].

Moreover, the $\Delta\Sigma$ modulator are only stable to modulation indexes around M = 0.5, and special techniques must be implemented in order to increase the maximum amount of input signal contained in the switching output signal [10], [13], [14].

In general, the class D audio power amplifiers based on $\Delta\Sigma$ modulation are typically used in medium and high power applications where the power consumed by the modulator does not represent a high percentage of the audio amplifier power rating in order to preserve a relatively high efficiency [13]–[19].

c. Class D Audio Power Amplifiers Based on Bang-Bang Control

Class D audio power amplifiers based on bang-bang control are the simplest topologies with the smallest silicon area. The amplifier is a closed-loop architecture, illustrated in Fig. 27, based on a hysteresis band modulator that calculates the error between the input audio signal V_{IN} and the measured output V_{OUT}. When the error exceeds a certain bound (hysteresis band), the controller changes its state to pull the error back within that bound [5], [20]–[22].

Class D amplifiers based on bang-bang control are simple because they do not need high accuracy circuitry to generate a highly-linear carrier waveform like pulse-width modulation based amplifier, nor to run a very complex audio modulator as $\Delta\Sigma$ class D amplifiers. Instead, their topology is a simple feedback loop which goes into one of the differential inputs of the hysteresis comparator. Also, as consequence, the area occupied by these amplifiers is very small, and their efficiency higher [22].

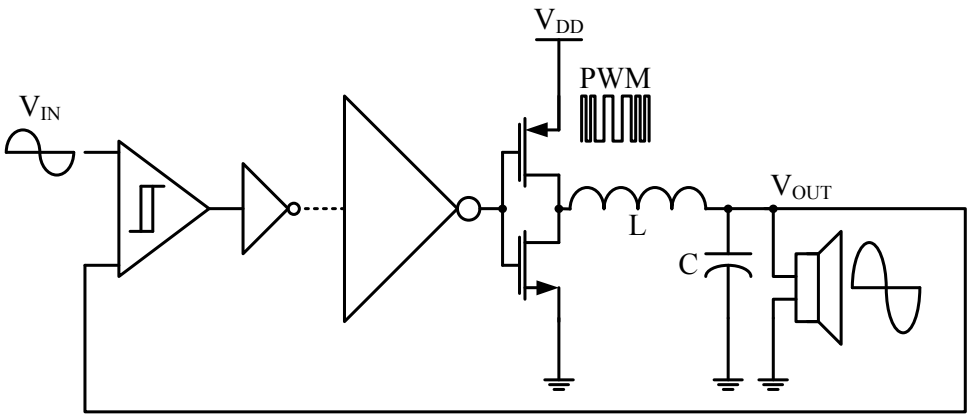


Fig. 27. Class D audio power amplifier based on bang-bang control

However, class D audio power amplifiers based on bang-bang control suffer from two major drawbacks. The first one is the variable switching frequency of the amplifier due to the lack of a robust audio modulator. The variable switching frequency can affect (as switching noise, substrate noise, and/or electro-magnetic interference) sensitive circuits within the integrated circuit (IC) [20]. The second drawback is the limited linearity achieved by the class D amplifier with bang-bang control because the absence of a proper audio modulator. This limitation reduces the potential application of class D audio amplifiers based on bang-bang control to low-quality audio applications. However their limitations are compensated with their simple design and high efficiency [22].

d. Class D Audio Power Amplifiers Based on Nonlinear Control

Class D audio power amplifiers based on nonlinear control techniques were first proposed in the late 1990s [23] but their first monolithic implementations appeared only few years ago [24], [25], and the design, implementation and measurement of such architectures are presented as part of this dissertation.

Given that class D amplifiers are nonlinear systems by nature, or variable structure systems (VSS) in nonlinear control theory [33]–[35], their controllers can be directly designed using nonlinear variable structure control (VSC) with sliding mode control (SMC) [33]–[36]. Development of sliding mode control started in the 1950s in the Soviet Union and has been applied to nonlinear problems with practical applications in power converters, robotics, etc. Sliding mode control provides stability and robustness to external perturbations [35].

The general architecture of a class D audio power amplifier based on nonlinear control with sliding mode is shown in Fig. 28. It is a closed-loop system whose feedback minimizes the error between the input signal V_{IN} and the output signal V_{OUT}. It is a tracking system that replicates the audio signal at the output of the amplifier. The audio modulator, or sliding mode controller, provides the necessary conditions to manipulate the error signal and generate a digital modulated signal.

The class D audio amplifier based on nonlinear control may be considered a hybrid architecture because it combines the simplicity of a hysteretic controller with the robustness

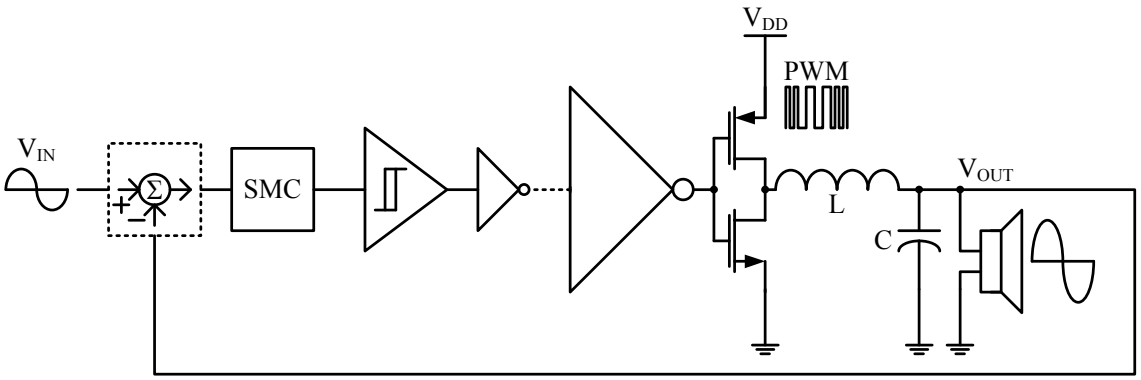


Fig. 28. Class D audio power amplifier based on nonlinear control

of a sliding mode controller. Integrated circuit implementations of this architecture [24], [25] have shown that this topology is suitable for very high-performance applications with very-high linearity requirements and very-low power consumption.

Moreover, its very-low quiescent power consumption makes it a very attractive solution for mobile low-voltage low-power applications with critical battery life. It has been shown that it can perform as high as state-of-the-art amplifiers but consuming less than one tenth of static power [25]. A detailed description of the class D audio amplifiers based on nonlinear control [24], [25] is given in following chapters.

2. Performance Metrics of Class D Audio Power Amplifiers

As it has been pointed out in previous sections, the two main characteristics in an audio power amplifier are the efficiency and linearity performance. However, besides the efficiency and harmonic distortion, there are other key performance metrics that provide very important information about an audio amplifier. The most relevant performance metrics of class D audio power amplifiers [3], [8], [37]–[43] are detailed next.

The class D audio amplifier measurements can be divided into two main groups: (1) the frequency measurements, and (2) the power measurements. The former includes total harmonic distortion (THD), total harmonic distortion plus noise (THD+N), intermodulation distortion (IMD), signal-to-noise ratio (SNR), and power-supply rejection ratio (PSRR). The latter encloses the power rating and power efficiency (η). Therefore, it is necessary to build two different measurement boards [3], [37], [38] in order to perform a complete set of measurements in a class D audio power amplifier.

The basic measurement equipment for class D audio power amplifiers must include: an audio analyzer or spectrum analyzer, oscilloscope, a highly-linear signal generator, evaluation board (printed circuit board), multimeter, power resistors, and the low-pass filter components [37].

A general set-up for frequency measurements is shown in Fig. 29. It includes a System One Dual Domain Audio Precision (AP) [38]–[41] highly linear signal generator V_{IN}, a bias network and a power network for the IC prototype, the low-pass external LC filter network, and the load Z_L (speaker). The Audio Precision equipment also provides a built-in spectrum analyzer.

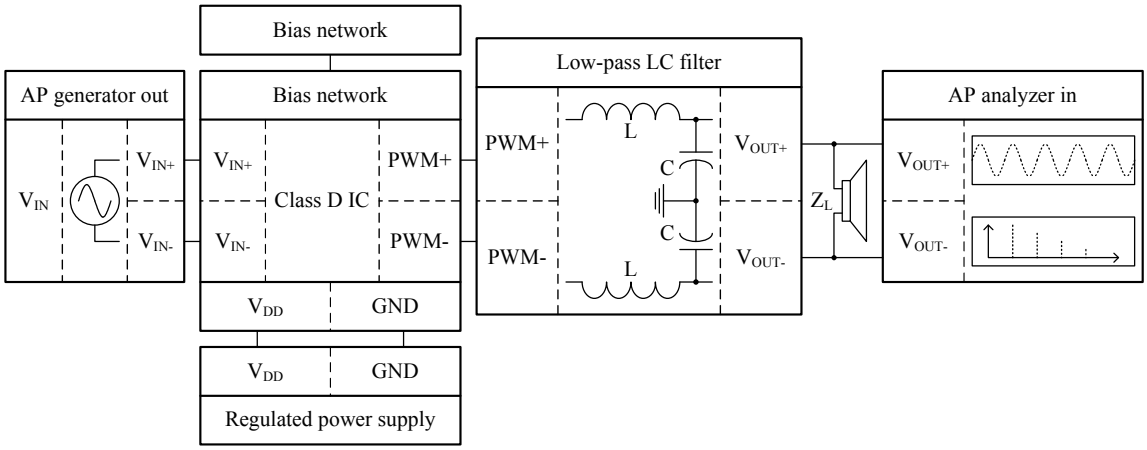


Fig. 29. General set-up for frequency measurements in class D audio power amplifiers

a. Total Harmonic Distortion (THD)

Harmonic distortion is probably the oldest and most universally accepted method of measuring linearity. This technique excites the device under test (DUT) with a single high linear sinusoidal wave and measures the spectrum at the output. The output of the device is not a pure sinusoidal because of the non-linear characteristics of the system. Ideally, only the fundamental frequency of the sine wave input is present at the output of the audio

power amplifier, but, by using Fourier series, it can be shown that the output waveform consists of the original input sine wave plus sine waves at integer multiples (harmonics) of the input frequency. The harmonic amplitudes are proportional to the amount of distortion in the device under test.

The percentage (%) of total harmonic distortion in a class D audio power amplifier [40], [41] is given by

$$THD\,(\%) \;=\; 100 \times \left(\frac{\sqrt{H_2^2 \;+\; H_3^2 \;+ H_4^2 \;+\; \ldots \;+\; H_k^2}}{H_1} \right) \tag{2.24}$$

and the total harmonic distortion in decibels (dB) is simply

$$THD\,(dB) \;=\; 20 \log_{10} \left(\frac{\sqrt{H_2^2 \;+\; H_3^2 \;+ H_4^2 \;+\; \ldots \;+\; H_k^2}}{H_1} \right) \tag{2.25}$$

where H_1 is power level of the fundamental frequency, H_k is the power level of the k^{th} harmonic, and k is the maximum harmonic below the upper limit of the audio frequency band (i.e. 20 kHz). An amplifier with lower harmonic distortion provides better audio quality.

b. Total Harmonic Distortion Plus Noise (THD+N)

The total harmonic distortion plus noise (THD+N) measurement is similar to the total harmonic distortion, except that instead of measuring individual harmonics, this test combines the effects of noise, distortion and other undesired signals (within the audio band) into one measurement, and relates it to the fundamental frequency [37].

Calculation of total harmonic distortion plus noise can be expressed mathematically as

$$THD\,(\%) \;=\; 100 \times \left(\frac{\sqrt{H_2^2 \;+\; H_3^2 \;+ H_4^2 \;+\; \ldots \;+\; H_k^2 \;+\; n^2}}{H_1} \right) \tag{2.26}$$

and

$$THD\,(dB) \;=\; 20\log_{10}\left(\frac{\sqrt{H_2^2 \;+\; H_3^2 \;+ H_4^2 \;+\; \ldots \;+\; H_k^2 \;+\; n^2}}{H_1}\right) \tag{2.27}$$

where n is the noise voltage level.

Both, THD and THD+N are usually measured versus output power, and versus frequency. The measurement of THD and THD+N versus output power is commonly done with a 1 kHz test signal. The bench set up to measure THD and THD+N in a class D audio amplifier is the same illustrated in Fig. 29.

c. Intermodulation Distortion (IMD)

Intermodulation distortion (IMD) is a measurement of non-linearity in response to two or more input signals. There are an infinite number of intermodulation distortion tests one can perform by varying the test tone frequencies, number of test tones, amplitude ratios, and even the waveforms [42].

Intermodulation distortion is the ratio of magnitude of the sum and difference signals to the original input signal [43]. The intermodulation distortion is defined as

$$IMD\,(\%) \;=\; 100 \;\times\; \left(\frac{\sqrt{IM_A^2 \;+\; IM_B^2 \;+\; IM_C^2 \;+\; \ldots}}{V_{f_2}}\right) \tag{2.28}$$

where

$$IM_A \;=\; V_{(f_2 \,-\, f_1)} \;+\; V_{(f_2 \,+\, f_1)} \tag{2.29}$$

$$IM_B \;=\; V_{(f_2 \,-\, 2f_1)} \;+\; V_{(f_2 \,+\, 2f_1)} \tag{2.30}$$

$$IM_C \;=\; V_{(2f_2 \,-\, f_1)} \;+\; V_{(2f_2 \,+\, f_1)} \tag{2.31}$$

and V_{f_2} is the voltage at the input frequency f_2, $V_{(f_2 + f_1)}$ is the voltage at the sum of input frequencies f_1 and f_2, $V_{(f_2 - f_1)}$ is the voltage at the difference of input frequencies f_1 and f_2, etc.

Some authors believe that IMD measurement correlate better with audible quality than THD and/or THD+N figures because gives a measure of distortion products not harmonically related to the pure signal [38]. The lower the IMD, the more linear the class D audio amplifier under test.

The most popular IMD test was adopted in 1939 by the Society of Motion Picture Engineers (SMPE). It originated in the testing and quality control of optical sound tracks on cinema film. Later on, it became the Society of Motion Picture and Television Engineers (SMPTE). The basic concept of SMPTE testing is to look for the presence of amplitude modulation of a high-frequency tone in the presence of a stronger low-frequency tone [42]. The most commonly used test signals are a combination of 60 Hz and 7 kHz mixed in a 4:1 amplitude ratio. In Europe, though, it is common to use 250 Hz and 8 kHz. SMPTE results are expressed in terms of the amplitude modulation percentage of the high-frequency tone.

Another popular intermodulation test is the twin-tone IMD measurement. This test became a standard in 1937 when the International Telephonic Consultative Committee (CCIF) recommended it. This test is usually characterized by using a couple of sine waves with equal amplitude spaced relatively close together in frequency. The big advantage of this form of distortion testing is that high-frequency non-linearity can be explored better than THD and/or THD+n techniques. Audio Precision Inc. recommends testing with a combination of 18 kHz and 20 kHz [38].

The basic set up measurement in Fig 29 must be modified [38],[39] to include multiple input tones to perform an intermodulation test.

d. Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio is the measure of the maximum output voltage compared to the integrated noise floor over the audio bandwidth, expressed in decibels (dB). The integrated noise floor noise is measured by shorting the input terminals to ground. The signal to noise

ratio is calculated using the following equation

$$SNR\,(dB) \;=\; 20\log_{10}\left(\frac{V_{RMS,OUT}}{V_{RMS,N}}\right) \tag{2.32}$$

where $V_{RMS,OUT}$ and $V_{RMS,N}$ are the maximum RMS output voltage and the integrated RMS noise floor, respectively [3], [37], [38]. Signal-to-noise ratio is sometimes computed with respect to 1 W into 8 Ω load [8].

e. Power-Supply Rejection Ratio (PSRR)

A power-supply rejection measurment can be viewed as a special type of crosstalk measurement. Conceptually, a test signal is imposed in series with the target DC supply while the amplifier output is examined for presence of the signal [37],[38]. Supply rejection is usually expressed as a decibel (dB) ratio (PSRR) versus the test signal frequency as

$$PSRR\,(dB) \;=\; 20\log_{10}\left(\frac{V_{OUT}}{V_{DD}}\right) \tag{2.33}$$

where V_{OUT} is the output voltage and V_{DD} is the AC magnitude of the power supply. A typical test for measuring PSRR is to add a sinusoidal waveform with 100 mV amplitude to the DC level of the power supply [8].

The testing configuration in Fig. 29 is modified to couple the sinusoidal waveform into the power supply while the input pins of the device under test are grounded.

The power measurements are taken with the general test bench shown in Fig. 30. The addition of resistors R_1 and R_2 allows to measure the current flowing from the power supply V_{DD}, and the current through the loudspeaker Z_L, with the aid of multimeters V_1 and V_2. The power measurements include the power rating and the power efficiency (η).

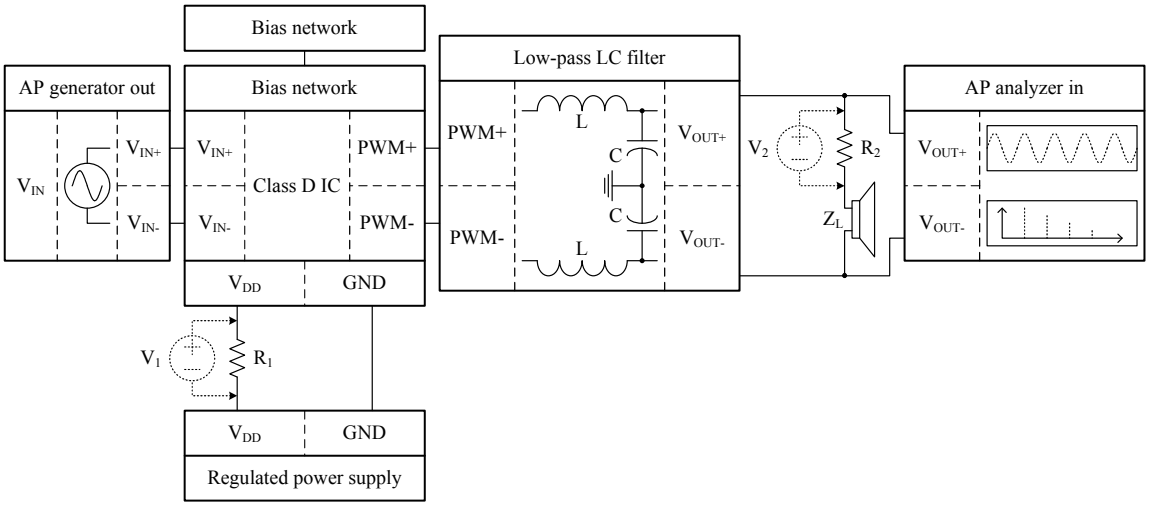


Fig. 30. General set-up for power measurements in class D audio power amplifiers

f. Power Rating

The power rating is measured when the amplifier is driven by a function generator. The most commonly used value for the loudspeaker is 8 Ω, although other values also used are 16 Ω, 4 Ω, and 3 Ω. A sine wave is applied to the input at a typical frequency of 1 kHz and the output is monitored on an oscilloscope. The amplitude of the input signal is increased until the output waveform clips. The output power is giving by equation (2.2) and the power rating of the audio power amplifier [3] is defined as

$$P_{L(max)} = \frac{V_{OUT,peak}^2}{2Z_L} = \frac{V_{OUT(RMS),peak}^2}{Z_L} \tag{2.34}$$

Care must be taken in making power measurements on high power amplifiers. The loudspeaker should have a power rating greater than or equal to the maximum output power of the audio amplifier. Heat sinks may be required during testing [3]. The power rating measurement excludes the resistors R_1 and R_2 in Fig. 30.

g. Power Efficiency (η)

Power efficiency (η) is defined as the ratio of the delivered output power to the input power drawn from the power supply. Efficiency is usually measured by sweeping the amplitude of a 1 kHz test sinusoidal wave signal.

The power efficiency of a class D audio power amplifier is measured by using the configuration shown in Fig. 30. A typical value for resistor R_1 is 0.1 Ω, and value of resistor R_2 is smaller (typically one tenth) than Z_L. The power efficiency of the class D audio amplifier [37], [38] is calculated as

$$\eta\,(\%) \;=\; \frac{P_{OUT}}{P_{VDD}} \;=\; \frac{V_{OUT,RMS} \times I_{OUT,RMS}}{V_{DD,AVE} \times I_{DD,AVE}} \;=\; \frac{V_{OUT,RMS}\left(\dfrac{V_{R2,RMS}}{R_2}\right)}{V_{DD,AVE}\left(\dfrac{V_{R1,RMS}}{R_1}\right)} \tag{2.35}$$

where $I_{DD,AVE}$ and $I_{OUT,RMS}$ are calculated by measuring the voltage drop across resistors R_1 and R_2.

3. Practical Design Considerations for Class D Audio Power Amplifiers

In general, all class D audio power amplifier implementations combine three main building blocks: (1) the audio modulator, (2) the output power stage, and (3) the output low-pass filter. The optimum design of these building blocks reduces sources of possible errors and maximizes the probabilities of high quality performance. On top of that, good layout techniques and careful design of printed circuit board (PCB) are highly important for IC fabrication and testing purposes. Some of the key design consideration for class D audio power amplifiers in practical implementations are presented in this subsection.

a. Audio Modulator

The audio modulator of a class D audio power amplifier is the pulse-width modulated signal generator and is constituted by the audio controller and the comparator. The design and optimization of the controller depends heavily on the class D audio power amplifier architecture.

The design of the class D audio power amplifiers based on pulse-width modulation [6]–[9] include the additional circuitry of a triangle wave carrier generator. Class D audio amplifiers based on $\Delta\Sigma$ modulation [10]–[19] require complex circuits and clock generators. On the other hand, class D amplifiers based on bang-bang control [20],[21] lack of any controller circuitry, and class D audio amplifiers based on nonlinear control [24],[25] require relatively simple controllers. Therefore, the designer must review carefully the specifications of power, noise, bandwidth, linearity, etc., to determine the circuitry needed for building the audio modulator.

Design requirements of the comparator are more general because it is a building employed by all class D audio amplifier topologies. The comparator must be designed with high gain and fast transient response. The propagation delay, as well as rise and fall time, should be minimized and symmetric. Performance of the comparator must not vary across input common mode range. Also, special attention should be focused to offset voltage, noise and hysteresis mismatches [2].

b. Output Power Stage

The output power stage is the source of most of the power losses in the class D audio power amplifier and its optimum design is crucial to maximize the efficiency performance of the system.

The three power dissipation mechanisms of the output power stage in class D audio

power amplifiers [44] are due to parasitic capacitance (P_c), short-circuit current (P_s), and switch on-resistance (P_r), and can be expressed mathematically as

$$P_c = \frac{1}{2} f_s C_p V_{DD}^2 \tag{2.36}$$

$$P_s = I_{mean} V_{DD} \tag{2.37}$$

$$P_r = \frac{1}{T_a} \int_0^{T_a} i_{OUT}^2 r_{on}\, dt \tag{2.38}$$

where f_s, C_p, V_{DD}, I_{mean}, T_a, i_{OUT}, and r_{ON} are the switching frequency, the total parasitic capacitance, the supply voltage, the mean value of the short-circuit current, the period of the audio signal, the load current, and the total on-resistance of the output stage, respectively.

These power mechanisms are directly related to the sizing of the output power stage. The total parasitic capacitance, the short circuit current, and the total on-resistance depend on the size and number of inverters in the power stage chain.

The size of the transistors in the power stage and the number of inverters (tapering factor T) can be optimized to minimize the short-circuit current according to a specific load and switching frequency conditions. This design approach provides much smaller area and reduced power consumption without compromising the propagation delay in comparison to the traditional method of using a tapering factor equal to the number *e* [45].

Once the size and tapering factor have been determined, the class D power efficiency (η) can be rearranged as a function of the PMOS transistor width in the last inverter of the chain W_p and the modulation index M as

$$\eta(W_p, M) = \frac{P_{out}(M)}{P_{out}(M) + P_c(W_p, M) + P_s(W_p, M) + P_r(W_p) + P_q} \tag{2.39}$$

where P_q is the quiescent power consumption and P_{out} is the class D amplifier output power defined in equation (2.2). The quiescent power consumption depends only on the audio modulator design.

The optimum size of the transistors in the inverter chain can be calculated if equation (2.39) satisfies the condition for maximum power efficiency when the modulation index is constant (single modulation index) as

$$\frac{\partial}{\partial W_p}\eta(W_p) \;=\; 0 \tag{2.40}$$

In general, it is desired to optimize the size of the transistors in the power stage to a range of modulation indexes. Then, the average power efficiency from modulation index M_1 to modulation index M_2 can be defined as

$$\eta_{ave}(W_p) \;=\; \frac{1}{M_2 \;-\; M_1}\int_{M_1}^{M_2}\eta(W_p, M)\,dM \tag{2.41}$$

and the size of the transistors for maximum average power efficiency can be calculated when

$$\frac{\partial}{\partial W_p}\eta_{ave}(W_p) \;=\; 0 \tag{2.42}$$

The value of W_p in equations (2.40) and (2.42) may be obtained by using numerical methods. Finally, once the value of the PMOS transistor W_p in the last output inverter is obtained, the size of the NMOS transistor W_n can be calculated using the ratio between PMOS and NMOS transistors for a given technology, and the remaining transistors widths of the preceding stages are designed according to the tapering factor and the number of inverters calculated previously [44], [45].

c. Output Low-Pass Filter (LPF)

The class D output filter provides many advantages by limiting supply current, minimizing electro-magnetic interference, protecting the speaker from switching waveforms, and providing a flat frequency response [1]–[3], [6], [7], [43], [46]. The most typical output low-pass filter (LPF) arrangements in class D amplifiers are shown in Fig. 31.

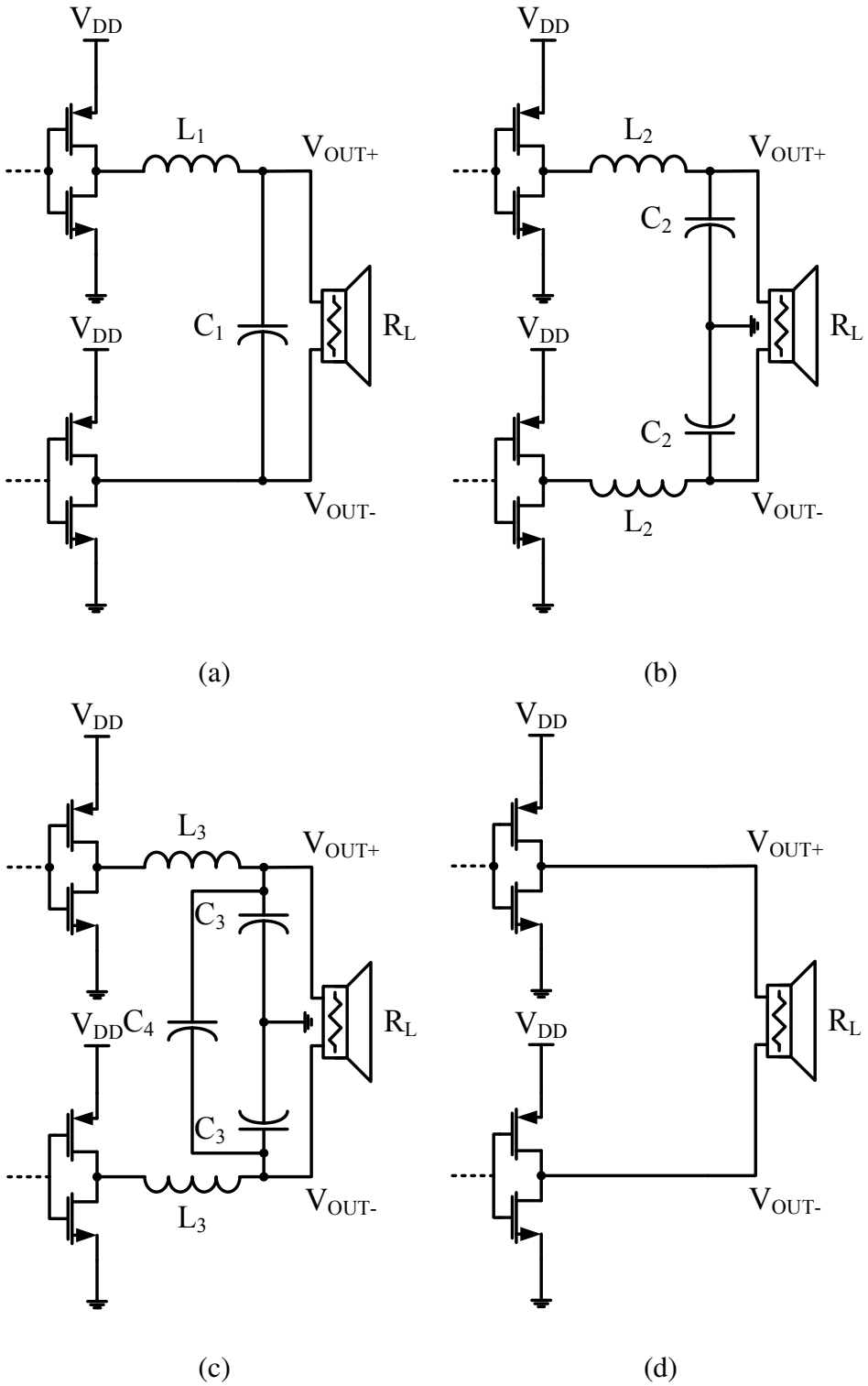


Fig. 31. Typical output filter arrangements in class D audio power amplifiers (a) Half filter (b) Balanced full filter (c) Alternate balanced full filter and (d) No filter

An output filter is required to attenuate the pulse-width modulated switching frequency. Without the filter, the ripple in the load can substantially degrade efficiency and may cause interference problems with other electronic equipment. A *Butterworth low-pass filter* is chosen for its flat passband and nice phase response, though other filter implementations may also be used. These filter designs assume that the loudspeaker is purely resistive and the load impedance is constant over frequency, but calculation of filter component values should include the DC resistance of the inductors and take into account the worst-case load scenario.

The half filter shown in Fig. 31(a) uses the minimum number of external components, but the loudspeaker sees the largest common-mode switching voltage, which can increase power dissipation and interference problems. The values of the inductor L_1 and the capacitor C_1 are given by

$$L_1 = \sqrt{2}\left(\frac{R_L}{\omega_o}\right) \tag{2.43}$$

$$C_1 = \frac{1}{\sqrt{2}}\left(\frac{1}{R_L\omega_o}\right) \tag{2.44}$$

where $\omega_o = 2\pi f_o$, and f_o is the filter cutoff frequency.

The balanced full filters in Fig. 31(b) and Fig. 31(c) are usually preferred because they do not have the common mode swing problems of the single-ended filter. Moreover, the inductors keep the output current constant while the voltage is switching. The values of the inductors L_2 and capacitors C_2 in Fig. 31(b) are calculated as

$$L_2 = \frac{\sqrt{2}}{2}\left(\frac{R_L}{\omega_o}\right) \tag{2.45}$$

$$C_2 = \frac{2}{\sqrt{2}}\left(\frac{1}{R_L\omega_o}\right) \tag{2.46}$$

because the load seen from each branch is half the value of the loudspeaker R_L. A single capacitor C_4 connected across R_L can be used in place of capacitors C_2. If this scheme is

used, additional capacitors C_3, as shown in Fig. 31(c), can be added to provide a high-frequency short to ground. Capacitor C_4 is equal to C_1 and capacitors C_3 are approximately $0.2 \times C_4$. The small value of capacitors C_3 have negligible impact on the filter cutoff frequency [6], [46].

Finally, the class D output stage in Fig. 31(d) shows that the output filter can be completely eliminated if the speaker is inductive at the switching frequency. For example, it can be eliminated if the class D audio power amplifier is driving a mid-range speaker with highly inductive voice coil, but cannot be eliminated if it is driving a tweeter or piezo-electric speaker. Also, the human ear acts as a band-pass filter such that only the frequencies between 20 Hz and 20 kHz are passed [43].

The main drawback to eliminating the filter is that the power from the switching waveform is dissipated in the speaker, which leads to a higher current. A more inductive speaker like a multilayer voice coil is ideal in this applications, however, the voice coil could be damaged if it is not designed to handle the additional power. Eliminating the filter also causes the amplifier to radiate electro-magnetic interference from the wires connecting the amplifier, therefore, the filter-less application is not recommended for sensitive applications [43].

The principle of eliminating the LC filter relies on the fact that the speaker can be modeled as a resistive load plus a reactive load. The models go from a simple resistor and inductor in series with typical values of R = 7.7 Ω and L = 370 μF [2], or RLC networks with R = 8 Ω, L = 330 μF, and C = 100 pF [8], to sophisticated models including an RL network representing the resistance and inductance of the voice coil together with an RLC model to simulate the electromechanical resonance of the cone mass with the suspension compliance and air-spring of the enclosure [1].

The filter-less class D audio amplifier has been subject of many studies [2], [8], [9] because it offers the cheapest and simplest implementation, and even industry has released

commercial versions of filter-less class D audio power amplifiers [7], [19].

d. Layout and Printed Circuit Board (PCB)

The layout phase of class D audio power amplifier is crucial in order to get a good performance during the testing stage. Analog section should be laid off using standard layout techniques such as common-centroid arrangements and use of dummy components for best matching [47], [48].

In addition, special effort must be taken when the output power stage is being designed because the coupling of substrate noise can destroy the analog circuitry performance, and narrow tracks can attenuate the efficiency of the amplifier. Additional layout techniques as guard-rings and metal/via resistance minimization should be employed to reduce the effect of substrate noise in the amplifier.

A suggested list of guidelines for laying out class D audio power amplifiers is shown below.

- Locate analog section as far as possible from digital section, use differential analog circuits to mitigate the effect of common-mode noise, and use dummy elements for analog section (transistors, resistors and capacitors).

- Layout of metals should be transversal between layers. Bottom metals should be used to connect local cells and top metals should be used to implement the power grids.

- Use as many substrate contacts as possible in local cells to provide a homogenous bulk voltage for transistors. Use P+ guard ring and N+ guard ring for NMOS and PMOS transistors, respectively. If the cell is very sensitive, use of dual rings can help to provide better isolation from substrate noise.

- Even that substrate could be the same, separate digital ground from analog ground and routed them as far as possible from each other.
- Use as many contacts as possible in power grids and use wide tracks for power connections to minimize sheet and via resistances.
- Put guard rings as close as possible to circuits, it will reduce the resistance between a noisy circuitry and a ground path.
- Use as many as possible number of pads for digital section, in such way, the bonding inductance will be minimized, and use different frame with ESD circuit protection for analog and digital section to separate noisy common connections.
- If possible, use dedicated guard rings around analog and digital sections, each one of them connected with a dedicated path to the power supply. Such guard rings must be as wide as possible.

Once the integrated circuit has been fabricated, the printed circuit board (PCB) should follow a good design to minimize the risk of degrading the performance of class D audio power amplifiers. There are three main areas concerning the PCB design: (1) the ground plane, (2) the power plane, and (3) the inputs and the outputs [46], [49].

A solid ground plane works as well as other types of grounding schemes because the system operates at relatively low frequency. A solid ground plane also helps to assist in the dissipation of heat, keeping the class D audio amplifier relatively cool and negating the need for an external heat sink. Additionally, the ground plane acts as a shield to isolate the power pins from the output and to provide a low-impedance ground return path. It is important that any components connecting an IC pin to the ground plane be connected to the nearest ground for that particular pin [46], [49].

The power plane contains two main different sections, the analog power pins and the output stage power pins. In general, the power traces must be kept short and the decoupling capacitors should be placed as close to the power pins as possible. The analog plane supplies power for sensitive circuitry and is the most sensitive pin of the device. Therefore, it must be kept as noise free as possible [46]. The output stage power plane is not as sensitive to noise as the analog power plane but its design must be done carefully to minimize ground loops and to provide very short ground return paths. For example, Fig. 32 illustrates two different routing cases of power loops.

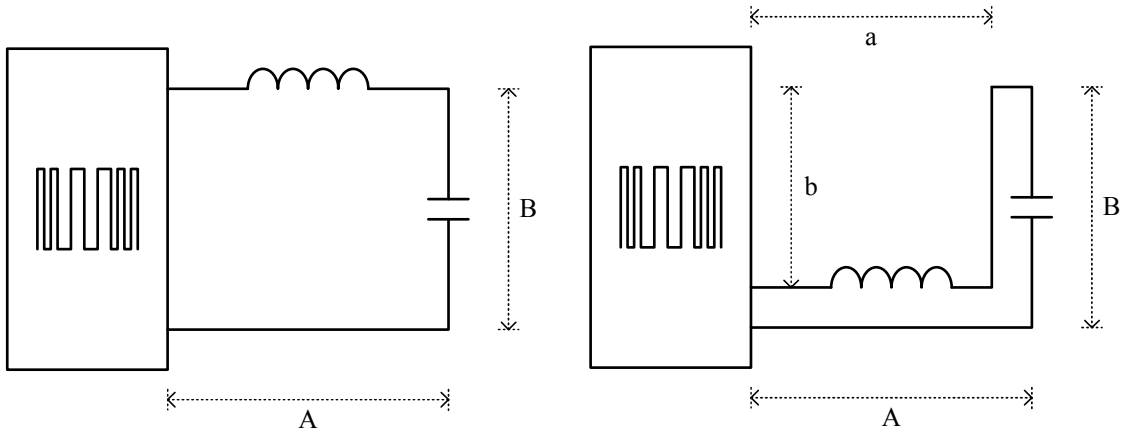


Fig. 32. Design of current loops in class D audio power amplifiers PCBs (a) Large loop area and (b) Optimized loop area

Figure 32(a) shows a bad design for the power plane in the output power path of a class D audio power amplifier because the loop area, Area = A $\times$ B, is large. On the other hand, Fig. 32(b) shows a very good design of the output power loop which minimizes the

loop area to Area = (A × B) - (a × b).

Finally, the input and output power planes must be separated. The loudspeaker traces should be kept as short as possible to reduce noise pickup. The bias network have almost no current flowing through them and then there are no special consideration for the layout of those traces. Standard layout practices will apply. The trace lengths between the output pins and the LC filter components must be minimized. The traces to the inductors should be kept short and separated from the input circuitry as much as possible. All high-current output traces should be wide enough to allow the maximum current to flow freely. Failure to do so creates excessive voltage drops, decreases the efficiency, and increments the distortion [46].

4. Audio Power Amplifiers Global Market Distribution

The audio power amplifier market represented a portion of the $3.5 billion consumer analog market. This sector was approximately 6% of the $58 billion annual consumer semiconductor market in 2008, and with an annual growth rate of 11% it is expected to represent $5.7 billion of the $98 billion consumer semiconductor market by 2013 [50].

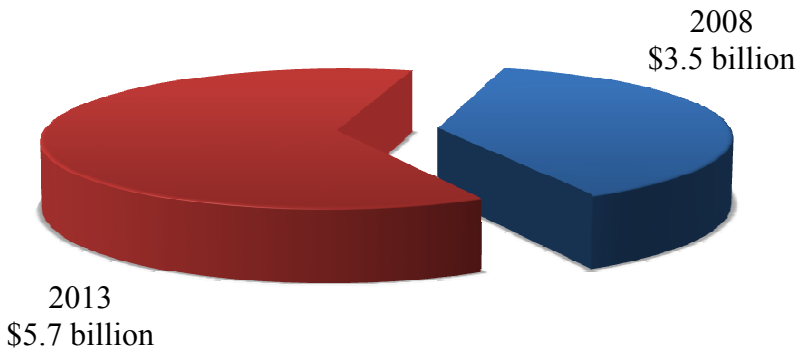


Fig. 33. Current and predicted global market of consumer analog products

The current and predicted market size of consumer analog applications is shown in Fig. 33.

The audio power amplifier market has been dominated by the linear amplifiers (class A amplifier, class B amplifier and class AB amplifier), and represent roughly three fourths of the total audio power amplifiers produced. However, class D audio amplifiers are been increasingly used in applications and are projected to increase in consumption dramatically due to their improvements in speed, efficiency, linearity and power capacity. Currently, class D amplifiers have an annual growth rate of 16%, and as shown in Fig. 34, they are expected to reach a market size close to $800 million by 2013 [50]–[52].

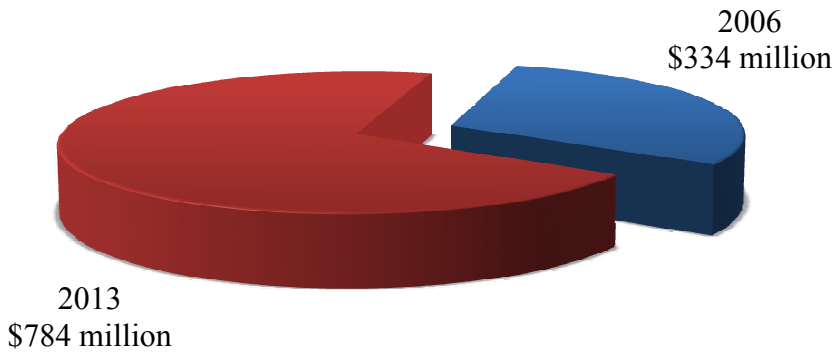


Fig. 34. Present and future global market of class D audio power amplifiers

Class D audio power amplifiers have found many new applications thanks to their high efficiency performance. Use of class D amplifiers in home theater systems and stereo receivers have been predicted to rise from $21 million in 2006 to $95 million in 2011. Nowadays, class D audio power amplifiers are used in 50% of the flat panel televisions with screen size above 40 in. Also, around 15% of multimedia sound boxes apply class D

audio amplifiers [51].

Currently, there are more than one hundred varieties of class D audio power amplifiers and around twenty IC class D audio amplifiers manufacturers [50]–[52], where the most representative companies are Yamaha, Texas Instruments, National Semiconductor, Maxim, Cirrus, Wolfson, On Semiconductor, Zetex, STMicroelectronics, Analog Devices, Microsemi, Sigmatel, Tripath, etc.

CHAPTER III

DESIGN OF A CLASS D AUDIO POWER AMPLIFIER USING SLIDING MODE CONTROL*

In recent years, class D audio amplifiers are becoming the most feasible solution for low-voltage low-power applications due to their high efficiency property; however, to obtain good linearity for high fidelity systems is still a challenge. The audio amplifier presented in this chapter, does not require the triangular carrier signal used in conventional class D audio amplifiers. It is shown that by making use of the sliding mode (SM) control technique along with an extra local feedback loop, the design parameters of a class D audio amplifier can be selected according to the linearity requirements. These techniques are applied in the design of a class D audio power amplifier to yield a single-chip low-distortion audio power amplifier with efficiency above 90% and total harmonic distortion (THD) as low as 0.08%. Experimental IC results, using a commercial 0.5 μm CMOS technology verified the theoretical results.

A. Introduction

The use of class D audio power amplifiers has been increasing considerably due to their high efficiency behavior compared with class A, class B and class AB audio amplifiers [53]. While class A amplifier ideally exhibits a maximum efficiency of 25% and class B/AB amplifiers yield an efficiency of 78.5% [53], [54], class D amplifier presents ideally an efficiency of 100% that makes it the best option for low-voltage low-power applications. Class D audio power amplifiers are mainly used in hearing aids, headphone amplifiers,

*Reprinted with permission from "Design of a class D audio amplifier IC using sliding mode control and negative feedback" by M. A. Rojas-González and E. Sánchez-Sinencio, 2007. *IEEE Transactions on Consumer Electronics*, vol. 53, no. 2, pp. 609-617, © 2007 by IEEE.

wireless phones, portable audio players, and notebook computers [53] where the high efficiency performance is essential to extend the battery life.

Class D audio amplifiers are typically based on pulse-width modulation (PWM) to generate the output waveform. An analog audio signal (20 Hz - 20 kHz) is compared with a high frequency carrier (typically $>$ 200 kHz) to generate a switching wave (PWM). This wave is further increased by a power stage in order to drive the output load. Once the signal is modulated, it is passed through a low-pass filter to recover the analog wave and eliminate the high frequency components [53].

The traditional class D audio power amplifier architecture is depicted in Fig. 35. It is an open-loop based system whose main block is represented by the comparator (pulse-width modulation generator). This topology requires having a well controlled triangular wave shape (carrier signal) which adds cost and potential degradation for a non-ideal

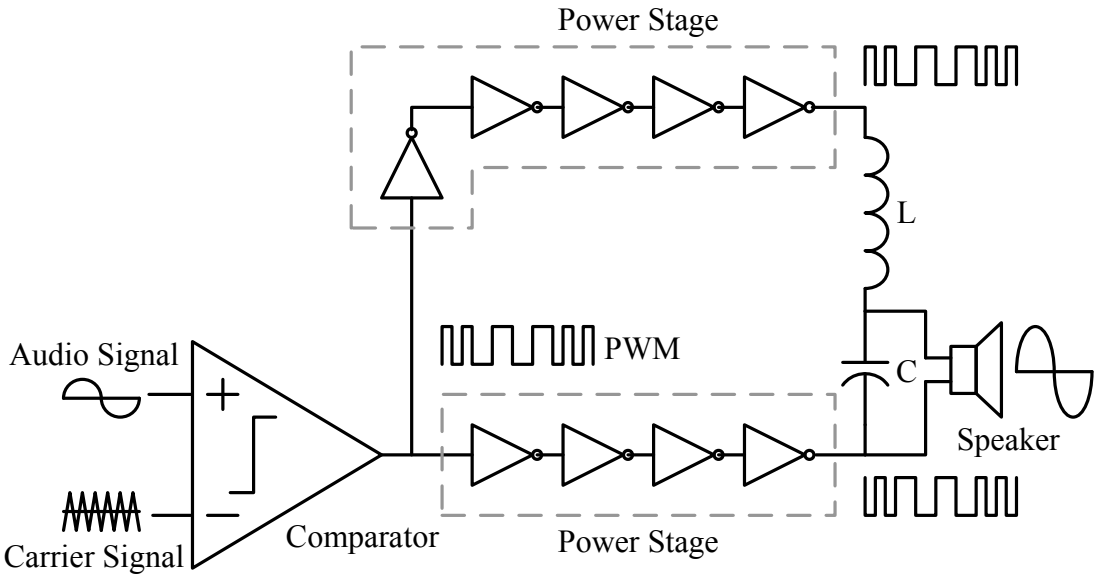


Fig. 35. Typical class D audio power amplifier architecture

triangular waveform. The power stage block allows the system to minimize the output resistance of the amplifier in such way that most of the output power is delivered to the load, typically an 8 Ω speaker, through the low-pass filter, whose frequency response is designed to be as flat as possible within the audible frequency band.

The main disadvantage of the class D audio amplifier versus the class A/B/AB audio amplifiers is that due to the nonlinear nature of its architecture, linearity is degraded and several approaches have been described to alleviate this problem [6]–[9], [15]–[17], [20], [21], [55]. In this chapter, the sliding mode (SM) control technique is applied to the class D audio power amplifier, which is implemented in a single-chip using 0.5 μm CMOS technology. Linearity of the system is enhanced by using negative feedback. Furthermore, this approach avoids the triangular wave signal used in conventional class D audio amplifiers. It is shown that stability of the proposed amplifier is not affected by process and temperature variations (PTV) or by any initial conditions.

Sliding mode theory starts its development in the 1950s as an alternative solution for control problems in systems with discontinuous differential equations. It is mostly applied to variable structure systems (VSS) where each one of their subsystems is continuous although not necessarily stable. Sliding mode control has been applied to robot systems, aircraft control, power converters, pulse-width modulation control, and remote vehicle control. One of the best features of sliding mode control is its robustness to external perturbations [23], [33]–[36].

This chapter is organized as follows. Section B introduces the proposed class D audio amplifier architecture, its fundamentals, potential drawbacks, and proposed alternatives to overcome such issues. Section C outlines the design of the class D audio power amplifiers and its building blocks. Experimental results of the fabricated prototype are shown in Section D. Finally, Section E summarizes the key points of the proposed class D audio power amplifier topology.

B. Proposed Class D Audio Power Amplifier

The proposed class D audio power amplifier conceptual diagram is shown in Fig. 36, where v_A, v_{OUT}, u, and v_{IN} are the input (reference) audio signal, the output signal, the pulse-width modulated waveform, and the digital input signal for the output filter (enhanced pulse-width modulated signal), respectively. It consists of four basic subsystems: the controller, a hysteresis comparator, the output power stage, and the output filter.

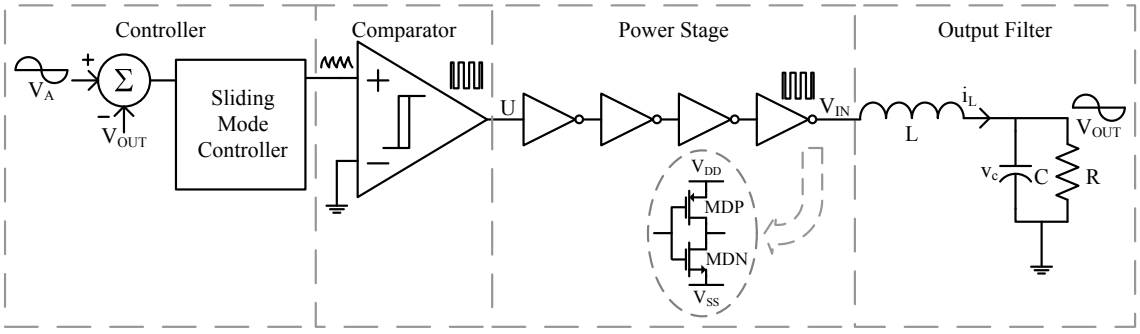


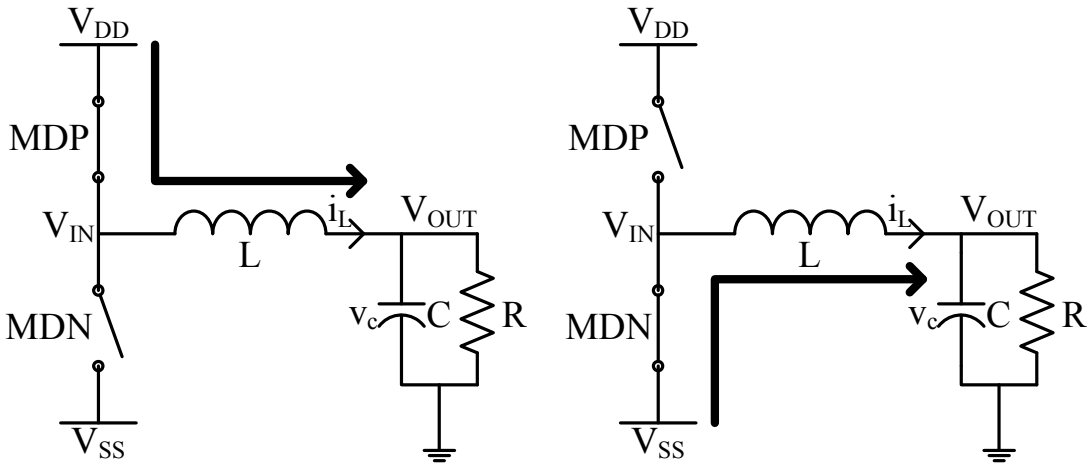
Fig. 36. Conceptual diagram of proposed class D audio amplifier with sliding mode control

The controller and the comparator, which generate the pulse-width modulated signal by using sliding mode control, are both integrated in a single-chip along with the power stage. The output filter is designed to be off-chip due to its large size components. A Butterworth filter approximation is chosen due to its flat frequency response. The cutoff frequency is set to 20 kHz and the load (R) is an 8 Ω speaker with final component values of L = 90 μH and C = 700 nF.

1. Sliding Mode Controller Design

The sliding mode controller design is based on the state variables of the system to be controlled. For this particular case the system consists of the low-pass RLC filter placed at the end of the class D audio amplifier.

Considering just the last inverter of the power stage, the circuit shown in Fig. 37 is obtained. In this figure, the two different substructures during the class D audio amplifier operation can be observed. In the first part of the cycle, depicted as Fig. 37(a), transistor MDP is ON and transistor MDN is OFF, that is, the input v_{IN} equals to v_{DD}. For the second subinterval, Fig. 37(b), transistor MDP is OFF and transistor MDN is ON, i.e. the input v_{IN} is equal to v_{SS}. Then, the dynamical state equation of the low-pass filter at the output



(a) (b)

Fig. 37. Subintervals of operation in class D audio power amplifier under sliding mode control (a) Subinterval I and (b) Subinterval II

of the class D audio amplifier is given by

$$\begin{pmatrix} \frac{d}{dt} i_L \\ \frac{d}{dt} v_C \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix} v_{IN} \tag{3.1}$$

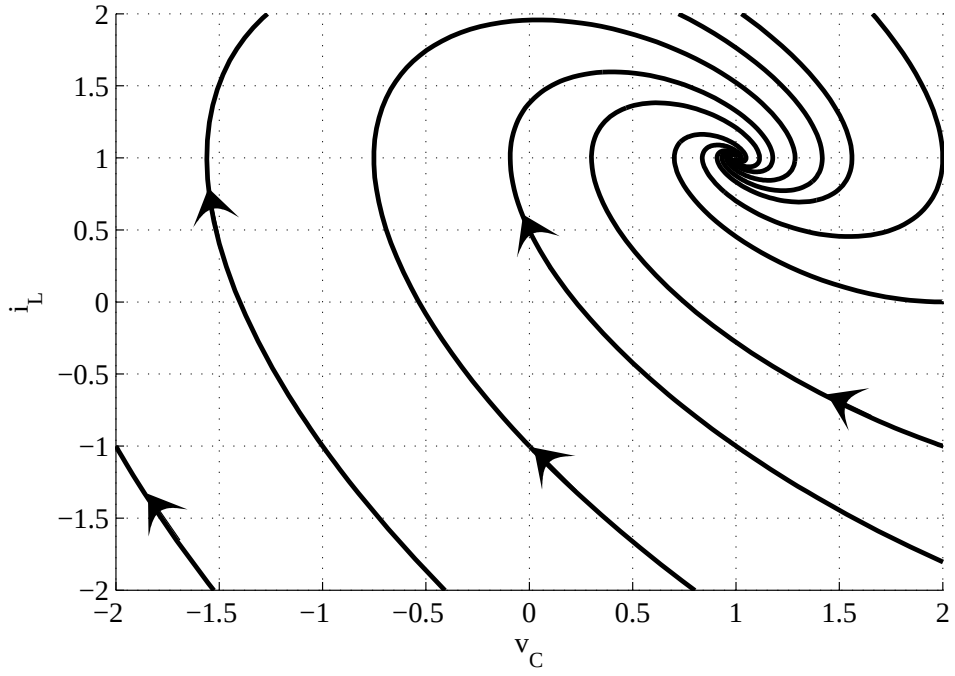
where the state variables i_L and v_C denote the inductor current and the capacitor voltage, and v_{IN} is the input signal that can be either v_{DD} or v_{SS}.

The low-pass filter is a second-order stable system with negative and imaginary eigenvalues that yields a stable focus natural equilibrium point [56] for each case (v_{DD} or v_{SS}), and whose transfer function is

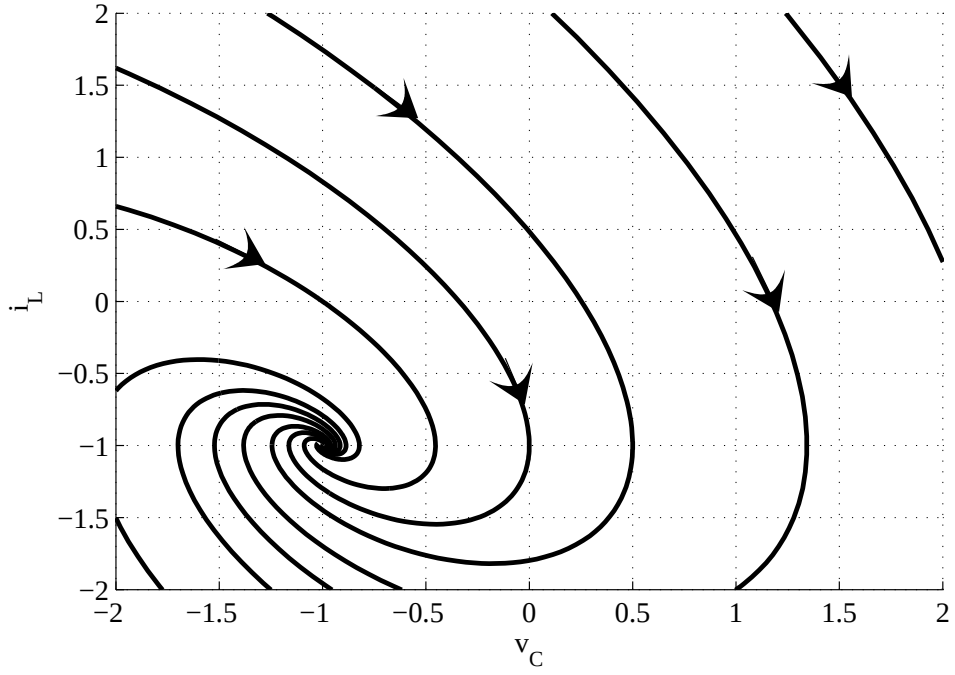
$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{\frac{1}{LC}}{s^2 + \frac{1}{CR}s + \frac{1}{LC}} = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 s + \omega_0^2} \tag{3.2}$$

where ω_0 and ζ are the cutoff frequency of the low-pass filter and the damping ratio, respectively.

Depending on which part of the cycle is operating the class D audio amplifier, the response of the low-pass filter would be that of the value of v_{IN}. Then, we would have two different phase portraits, i.e. a plot of typical trajectories of the state variables v_C and i_L in the state space system defined in equation (3.1) for different initial conditions, each one corresponding to the values of the input signal v_{IN}, as shown in Fig. 38. Figure 38(a) shows the step response of the low-pass filter in the configuration shown in the subinterval I in Fig. 37(a). Notice that the the value of the output voltage (capacitor voltage v_C) goes to the positive supply voltage after a short transient. On the other hand, Fig. 38(b) illustrate the case when a step is applied to the low-pass filter configured as shown in Fig. 37(b). In this case, the value of the capacitor voltage v_C goes to the negative voltage supply. Observe that, at steady state, the value of the current across the inductor i_L is proportional to the value of the normalized resistor R.



(a)



(b)

Fig. 38. Normalized phase portraits of subintervals I and II (a) $v_{IN} = v_{DD}$ and (b) $v_{IN} = v_{SS}$

Even though the nature of the low-pass filter is asymptotically stable, i.e. it reaches a steady state after a step response, our goal is to obtain an output signal equal to the (reference) audio voltage v_A, i.e. the audio input signal in Fig. 36, by combining the different substructures available in the system. Thus, our objective is to design a tracking controller to ensure that the output voltage ($v_{OUT} = v_C$) follows the reference voltage v_A (audio signal). Such controller will allow the output voltage system to follow the audio reference voltage by minimizing the error between those signals creating a sliding surface that will be given by a switching function directly derived from the dynamical state equation (3.1) of the low-pass filter at the output of the class D audio power amplifier.

In order to minimize the error $e_1(t)$ between v_A and v_{OUT}, it is necessary to design a state feedback control law, as shown in Appendix B, to achieve asymptotic tracking. In general, the error function in equation (3.3) is expressed in the controllable canonical form and the control function in equation (3.4) is derived as the linear combination of the canonical state variables [33]–[36].

$$\frac{d}{dt}\, e_i(t) = \dot{e}_i(t) = e_{(i\,+\,1)}(t), \text{ for } i = 1, 2, \ldots, \rho - 1 \tag{3.3}$$

$$e_\rho = -\sum_{i\,=\,1}^{\rho\,-\,1} k_i e_i(t), \text{ for } i = 1, 2, \ldots, \rho \tag{3.4}$$

where ρ is the order of the system. The coefficients of the control function are chosen in such way that the polynomial in equation (3.5) meets the Hurwitz criterion. The switching function in equation (3.6) represents the (ρ - 1) dimensional surface where the points of discontinuity merge.

$$P(s) = s^{(\rho\,-\,1)} + k_{(\rho\,-\,1)} s^{(\rho\,-\,2)} + \cdots + k_1 \tag{3.5}$$

$$s(e_1, t) = e_\rho - \sum_{i\,=\,1}^{\rho\,-\,1} k_i e_i(t) = 0 \tag{3.6}$$

For the case of the class D audio amplifier, the error function expressed in equation

(3.7) is defined as the difference between the reference audio waveform (v_A) and the output signal (v_{OUT}), and the linear control $e_2(t)$, from equation (3.3), is just expressed as the first derivative of the error function $e_1(t)$.

$$e_1(t) = v_A - v_{OUT} \tag{3.7}$$

$$e_2(t) = \dot{e}_1(t) = \frac{d}{dt}e_1(t) = \frac{d}{dt}v_A - \frac{d}{dt}v_{OUT} \tag{3.8}$$

Thus, the switching function, in the time domain, for the class D audio power amplifier operating under sliding mode control is

$$s(e_1, e_2, t) = k_1 e_1(t) + k_2 e_2(t) = k_1 e_1(t) + k_2 \dot{e}_1(t) \tag{3.9}$$

and its equivalent, expressed as a frequency domain function is

$$S(E_1, E_2, s) = (k_1 + k_2 s) E_1(s) \tag{3.10}$$

The sliding mode controller, given by equation (3.10), is a first order polynomial whose coefficients (k_1, k_2) must be selected to meet the Hurwitz criterion [36]. Such condition is met when the coefficients are greater than zero, but their optimization is done using the Bessel approximation to get the smallest possible response time with a delay characteristic as flat as possible. The final values for constants k_1 and k_2 are 1 and $\alpha \approx 5.625 \times 10^{-6}$, respectively. Figure 39 shows the step response of the class D audio amplifier for different constant k_1 and k_2 values. Notice that the amplifier presents a faster response when k_1 increases and k_2 decreases. However, the maximum flat delay response occurs with $k_1 = 1$, and $k_2 = \alpha$ [57].

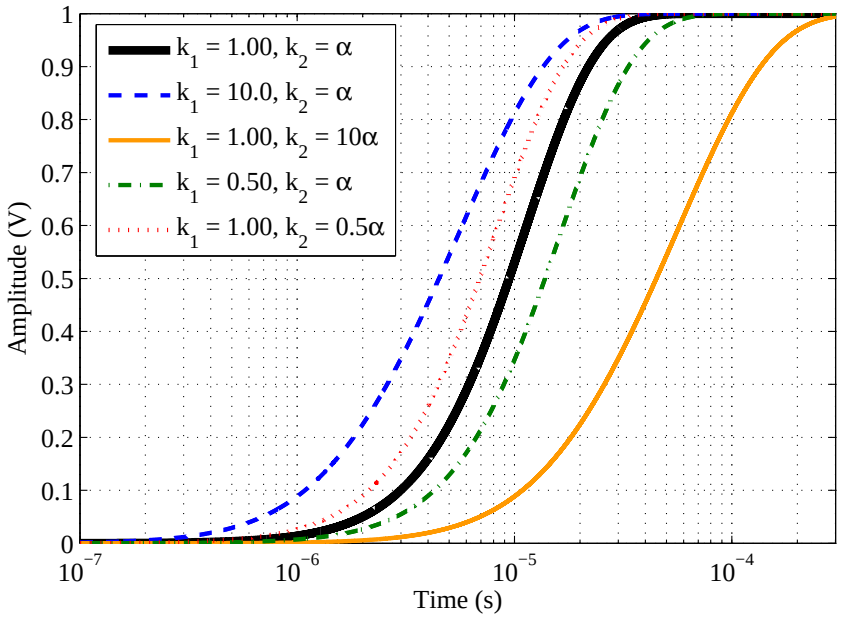


Fig. 39. Step response of the class D audio power amplifier with sliding mode control for different values of constants k_1 and k_2

2. Stability Analysis

The class D audio amplifier operating under sliding mode control consists of two different parts. The first part corresponds to the so called reaching mode, i.e. from any initial condition; the system will reach the sliding surface. Once there, the second part is the motion from the sliding surface to the equilibrium point of the system, i.e. the sliding mode.

The Lyapunov function approach [35], [36], as described in Appendix B, establishes the condition for the initial condition to move toward the sliding surface (reaching condition). The Lyapunov function $v(e_1, e_2, t)$ in equation (3.11) must satisfy the condition

for asymptotical stability given by equation (3.12).

$$v(e_1, e_2, t) \;=\; \frac{s^2(e_1, e_2, t)}{2} \tag{3.11}$$

$$\dot{v}(e_1, e_2, t) \;=\; s(e_1, e_2, t)\dot{s}(e_1, e_2, t) \;<\; 0 \tag{3.12}$$

when $s(e_1, e_2, t) \neq 0$. The sliding mode controller will make the system to switch between v_{DD} and v_{SS} according to the sign of the switching function in equation (3.9).

$$v_{IN} \;=\; \begin{cases} v_{DD} & \text{when} \quad s_(e_1, e_2, t) \;>\; 0 \\ v_{SS} & \text{when} \quad s_(e_1, e_2, t) \;<\; 0 \end{cases} \tag{3.13}$$

The analysis of the discontinuity in v_{IN}, discussed in Appendix B, is overcome by applying the equivalent control approach [35], where the discontinuous function v_{IN} can be viewed as the sum of a high-frequency nonlinear switching component (v_{nl}) and a low-frequency continuous component (v_{eq}), where v_{eq} (called the equivalent control input) can be considered as the mean value of the discontinuous function v_{IN} and must satisfy $v_{eq} < |v_{IN}|$ to fulfill the asymptotical stability condition.

The controller makes the system to satisfy the reaching condition and, on the other hand, the fact that the sliding equilibrium point [56] of the class D audio amplifier is a stable node with eigenvalues real and negative, as derived in Appendix B, guarantees the sliding mode of the system toward its sliding equilibrium point. The sliding mode controller makes the class D amplifier a stable system with a stable node equilibrium point where any initial point in the phase portrait reaches the sliding surface and then moves to the sliding equilibrium point of the system, as shown in Fig. 40.

3. Linearity Improvement

Ideal sliding mode control reproduces exactly the same waveform at the output stage of the class D amplifier using pulse-width modulation; however, due to hardware implementation,

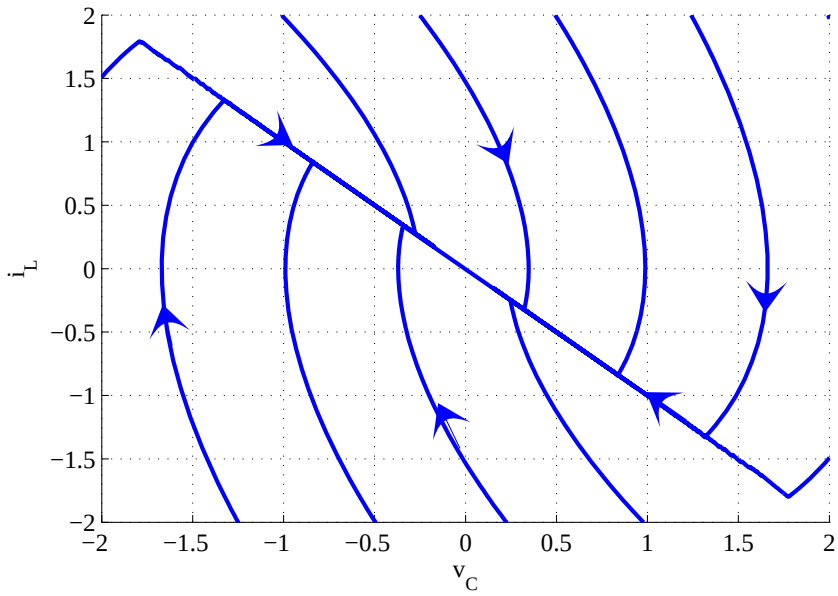


Fig. 40. Normalized sliding mode operation in class D audio power amplifier

sliding mode control faces two main obstacles, the quasi-differentiation operation and the non-infinite switching frequency.

Figure 41 shows the performance of the class D amplifier considering these two limitations. In curve (a), the behavior of the ideal differentiation in the switching function expressed in equation (3.9) can be appreciated, here, even that the switching frequency is finite; the true-derivative of the error helps the system to provide a very good linearity even for low-frequency switching. Curves (b) and (c) in Fig. 41 represent the linearity of the class D amplifier when the lossy-differentiation function

$$E_2(s) = \frac{k_2 s}{1 + \frac{s}{\omega_p}} \tag{3.14}$$

with $\omega_p = 2\pi f_p$, is implemented with poles at f_p = 3 MHz and f_p = 150 kHz, respectively. The pole in the lossy differentiator limits the derivative function at high frequencies and

replaces it with a constant gain of value $k_2\omega_p$ instead of $|k_2\omega|$ in the ideal case. Thus, equation (3.10) becomes

$$S(E_1, E_2, s) = \left[k_1 + \left(\frac{k_2 s}{\frac{s}{\omega_p} + 1}\right)\right] E_1(s) \tag{3.15}$$

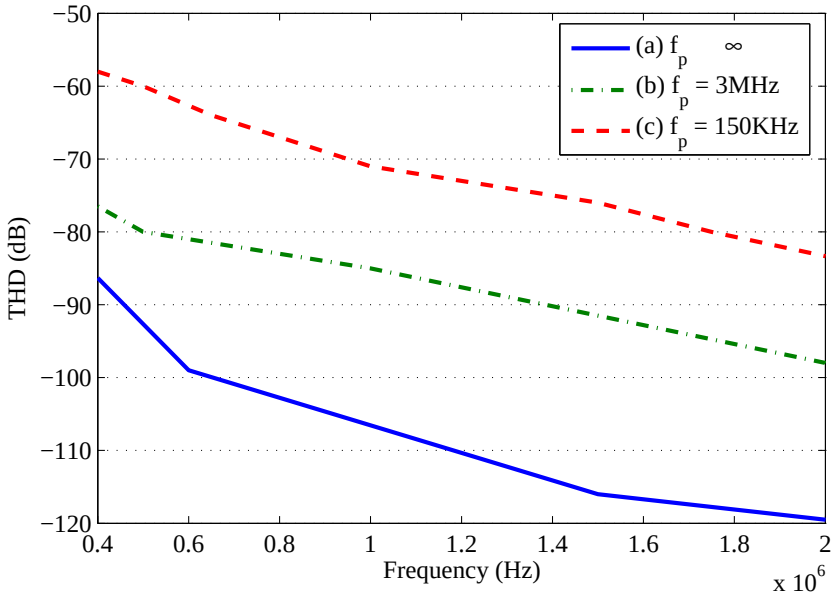


Fig. 41. Linearity performance of class D audio amplifier with lossy differentiator

Even that the sliding mode control makes the class D audio power amplifier a stable system; it does not guarantee high linearity for high fidelity applications. To overcome this problem, a negative loop structure can be applied [58].

The resulting system is the sliding mode class D audio amplifier depicted in Fig. 42 where G represents the power series expansion polynomial of the comparator, the power stage, and the output filter in the class D audio amplifier. If the output of the closed loop

system v_{OUT} is expressed as the sum of the fundamental and the harmonics

$$v_{OUT} \approx g_1 x + g_2 x^2 + g_3 x^3 + \ldots \tag{3.16}$$

where x = s(e_1, e_2, t) - βv_{OUT}, then, the total harmonic distortion (THD) of Fig. 42 yields

$$THD \approx \sqrt{\left(\frac{HD2_{OL}}{(1 + g_1\beta)^2}\right)^2 + \left(\frac{HD3_{OL}}{(1 + g_1\beta)^3}\right)^2 + \cdots} \tag{3.17}$$

where HDn_{OL} is the n^{th} harmonic distortion component of the system in open loop (with $\beta = 0$) and g_1 is the linear gain of the amplifier. With the implementation of the extra local feedback loop, the linearity of the system increases considerably, however, the drawback is the decrement in the amplitude of the output signal inversely proportional to the feedback factor β [26], [58].

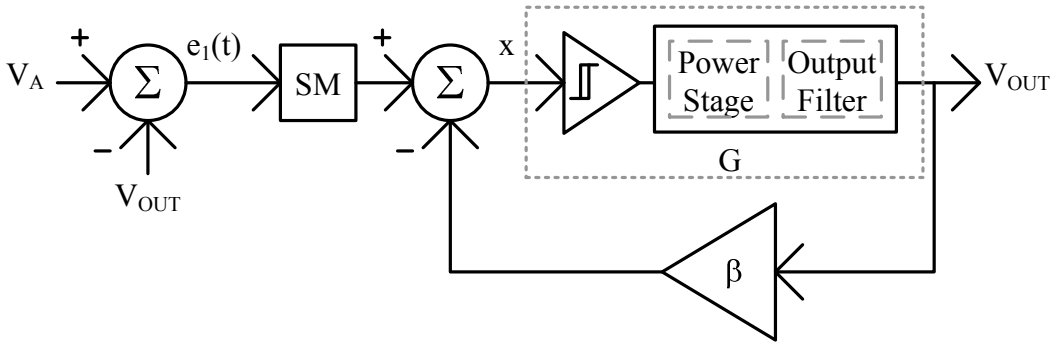


Fig. 42. Macromodel of class D audio amplifier with sliding mode and negative feedback loop

Figure 43 depicts the performance of the class D audio amplifier with sliding mode control and negative feedback loop switching at different frequencies (f_s). The pole in the

lossy differentiator function is placed at f_p = 150 kHz with a high frequency gain of 14 dB. The improvement of the linearity as the feedback factor β increases is appreciated, but on the other hand, the amplitude of the fundamental tone at the output of the system is reduced from 1 when β = 0 down to 0.5 when β = 1.

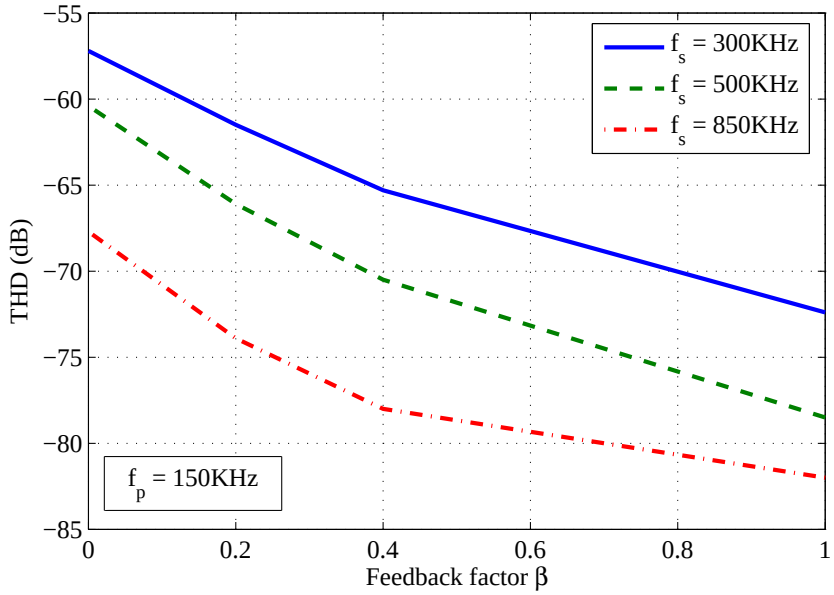


Fig. 43. Linearity improvement with negative feedback for f_p = 150 kHz

A trade-off exists to obtain a low distortion without severely compromising the output power of the amplifier and relaxing the specifications of the analog components. The class D audio amplifier with sliding mode control was selected to be implemented using the lossy differentiator function in equation (3.15) with the pole frequency located at f_p = 150 kHz and a feedback gain β of 0.4 which gives us an increment of approximately 10 dB in the THD and a decrement in the amplitude of the output signal in the order of 25%.

C. Design of Building Blocks

The proposed building block diagram of the class D audio power amplifier is shown in Fig. 44. Besides the feedback loop β, note that the number of building blocks corresponds to that of the proposed architecture in Fig. 36 where the switching function in equation (3.9) implements the sliding mode controller block as the sum of the error function in equation (3.7), $e_1(t) = v_1$, and its derivative, $\alpha e_2(t) = v_2$.

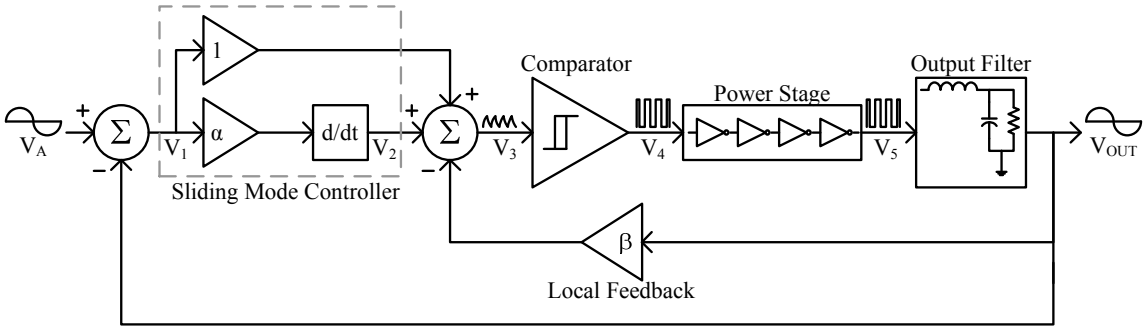


Fig. 44. Class D audio amplifier with sliding mode control and extra local feedback

1. Sliding Mode Controller and Feedback Loop

The circuit diagram of the class D audio amplifier is depicted in Fig. 45. The output stage is designed as a pseudo-differential block to double the output swing of the amplifier.

The error function $e_1(t)$ is implemented as a summer with the operational amplifier (OPAMP) A at node v_1, as expressed in equation (3.18), where $R_1 = 2R_2 = 4R_3$. Also, note that the node v_2 represents the first derivative of the error, $e_2(t)$, as it is expressed in

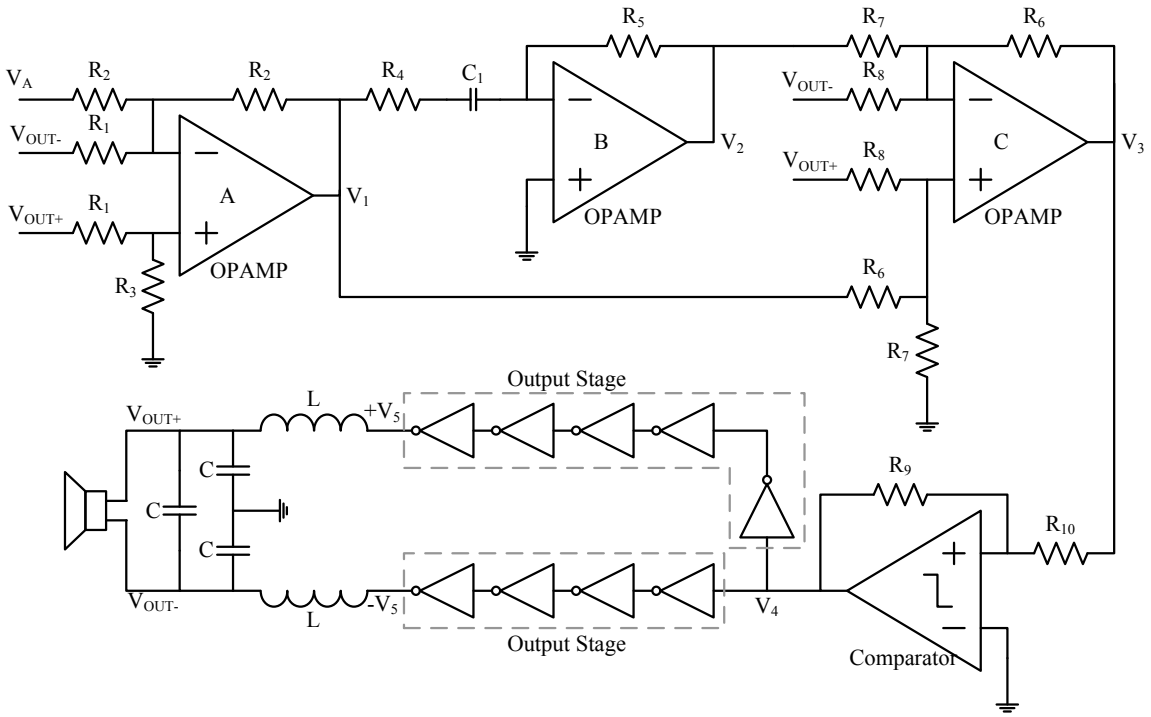


Fig. 45. Schematic implementation of proposed class D audio power amplifier

equation (3.8).

$$v_1 \;=\; e_1(t) \;=\; v_A \;-\; \frac{1}{2}(v_{OUT+} \;-\; v_{OUT-}) \tag{3.18}$$

The lossy-differentiation function is realized around the operational amplifier B. A true differentiator is hard to implement due to the high-pass filter nature of its structure and for this reason, a lossy-differentiator including R_4, R_5, and C_1 is designed. The technology limitations does not allow to integrate a huge capacitor nor a big resistance and then, the gain factor α of this section is split between operational amplifier B and operational amplifier C, with partial gains of 0.25 and 4 respectively, resulting in the constant α divided by four, i.e. $\alpha = 4C_1R_5$. The condition $|sC_1R_4| \ll 1$ must be satisfied in order to get minimum degradation of the derivative function during the operation of the lossy-

differentiator.

Around the operational amplifier C, the second summer of Fig. 44 is implemented. It combines the signal coming from the sliding mode controller and the local feedback loop. The feedback gain β , in equation (3.19), is implemented as $2R_6$ / R_8 and the gain of four between R_7 and R_6 is the complement gain for the previous stage where the gain for the constant α was split, i.e. $R_8 = 5R_6 = 20R_7$.

$$\beta \; = \; 0.4 \; \times \; \frac{1}{2}(v_{OUT+} \; - \; v_{OUT-}) \tag{3.19}$$

The node v_3 in Fig. 44 and Fig. 45 represents the input to the hysteresis comparator. Such comparator is done with a positive feedback loop formed with resistors R_9 and R_{10} to obtain a hysteresis window v_{hys}, defined in equation (3.20), with value of approximately 0.5% of the power supply voltage (2.7 V) which allows the system to switch at an estimate frequency of 500 kHz.

$$v_{hys} \; = \; \frac{R_{10}}{R_9} \; \mid v_{DD} \mid \tag{3.20}$$

The single-ended output filter is modified to a differential version with the same characteristics and same cutoff frequency.

2. Output Power Stage

The transistor level design starts with the output power stage of the class D audio amplifier, which is depicted in Fig. 45. This block consists of a chain of digital inverters with an ideal condition of zero output on-resistance that provides 100% of efficiency to the class D audio power amplifier. For this reason, an optimum design must be done in order to minimize the on-resistance by optimizing the transistors width.

There are several approaches proposed to design an efficient buffer with an optimum tapering factor T, i.e. the ratio of the transistors size in two consecutive stages, in the

inverters chain. However, in [44], [45], it has been shown that the model to obtain the smallest propagation and area must be designed taking in consideration all the transistor parameters as well as load and parasitic capacitances and the switching frequency, hence, such model is taken to design the power output stage to optimize its performance to a range of modulation indexes (M $\in$ [0.2, 0.9]) by optimizing the power efficiency, shown in equation (3.21), as a function of the transistor MDP width (W) and the modulation index M [44].

$$\eta(W, M) \; = \; \frac{P_{out}}{P_{out} \; + \; P_s(W) \; + \; P_c(W) \; + \; P_r(W, M)} \tag{3.21}$$

where P_{out}, P_s, P_c and P_r are the output power at the load, the power dissipation due to short-circuit current during switching, the power due to the parasitic capacitances of transistors, and the power due to the transistor on-resistance (which also depends on the width of the output transistors), respectively [44].

The power efficiency equation described by equation (3.21) takes in consideration all the parasitic capacitances (gate to source, gate to drain, and gate to substrate) and resistances (contact resistances and vias resistances) in the class D audio amplifier output stage. It was solved numerically with the aid of MATLAB to get an optimum transistor size (W_{MDP} = 420.9 μm with multiplicity 120), a tapering factor of T = 12, a number of stages of 4, and an on-resistance of 0.23 Ω, approximately.

3. Comparator and Operational Amplifiers

The comparator must be designed in order to obtain the fastest possible response. A two-stage operational amplifier architecture with high slew rate was chosen [47]. The single-ended comparator schematic is shown in Fig. 46, and its transistor sizes are listed in Table I.

The design of the operational amplifiers for the linear operation of the sliding mode controller was done by using an N-P complementary rail-to-rail input stage [59] in order to

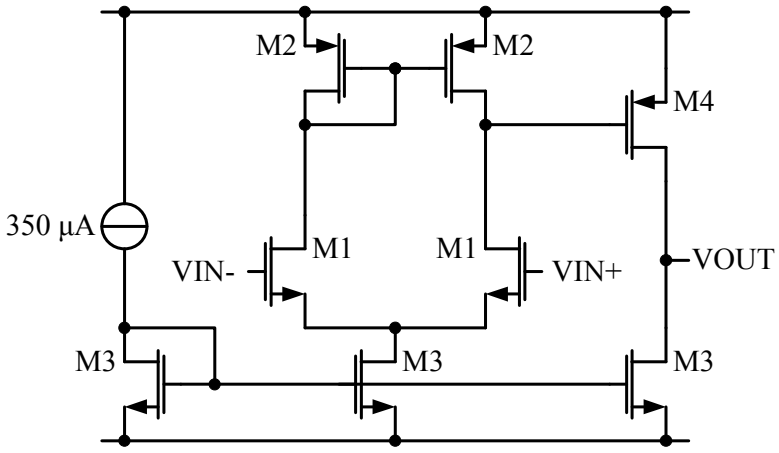


Fig. 46. Schematic of single-ended comparator

Table I. Transistor sizes used in single-ended comparator

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	9	0.6	4
M2	32.25	0.6	10
M3	10.05	0.6	10
M4	38.4	0.6	20

yield good noise performance and small area. Macromodel simulations showed that THD decreases as the hysteresis window in the comparator decreases, and DC gain and gain-bandwidth product (GBW) increase. Those simulations were done by modifying each one of the main parameters in the operational amplifier to see how the system behaved with

these variations.

The work done in the macromodeling of the class D audio amplifier imposed an operational amplifier with a minimum DC gain of 60 dB and gain-bandwidth product (GBW) around 25 MHz because operational amplifiers with higher specifications do not improve the linearity substantially, and on the other hand, increase the power consumption. The operational amplifier has a rail-to-rail constant-g_m input stage architecture, and its second stage was realized with a Miller compensation scheme [47]. Figure 47 illustrates the schematic implementation of the single-ended operational amplifier and Table II shows its transistors sizes.

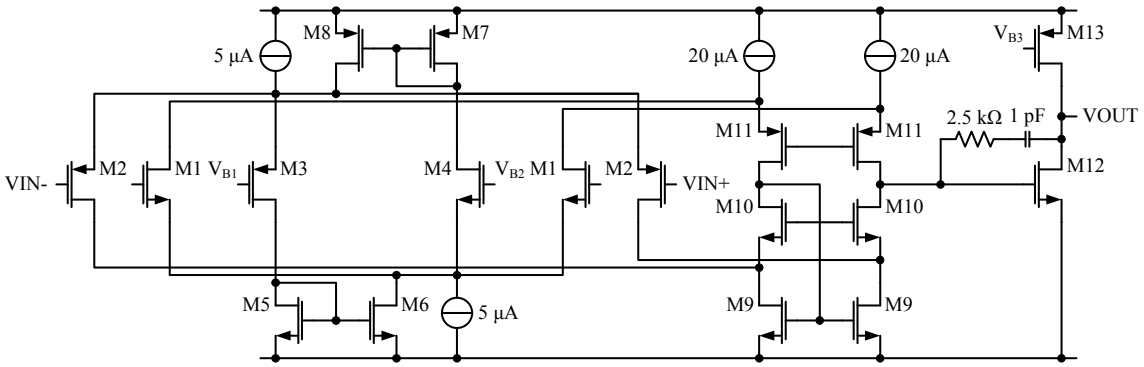


Fig. 47. Schematic of single-ended operational amplifier

Finally, Table III shows the comparator and operational amplifier final design specifications.

Table II. Transistor sizes used in single-ended operational amplifier

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	4.5	0.6	1
M2	5.55	0.6	1
M3	1.5	0.6	1
M4	1.5	0.6	1
M5	7.95	0.6	4
M6	7.95	0.6	12
M7	7.95	0.6	4
M8	7.95	0.6	12
M9	7.95	0.6	1
M10	7.95	0.6	2
M11	7.95	0.6	4
M12	13.05	0.6	8
M13	28.05	0.6	32

D. Experimental Results

The class D audio power amplifier was fabricated through and thanks to MOSIS using AMI 0.5 μm technology, it was tested with a voltage supply of 2.7 V, and the experimental results are shown in this section.

Table III. Comparator and operational amplifier specifications

Parameter	Comparator	OPAMP
DC Gain (dB)	60	66
GWB (MHz)	320	25
CMRR (dB)	63	58
PSRR+ (dB)	64	58
PSRR- (dB)	68	63

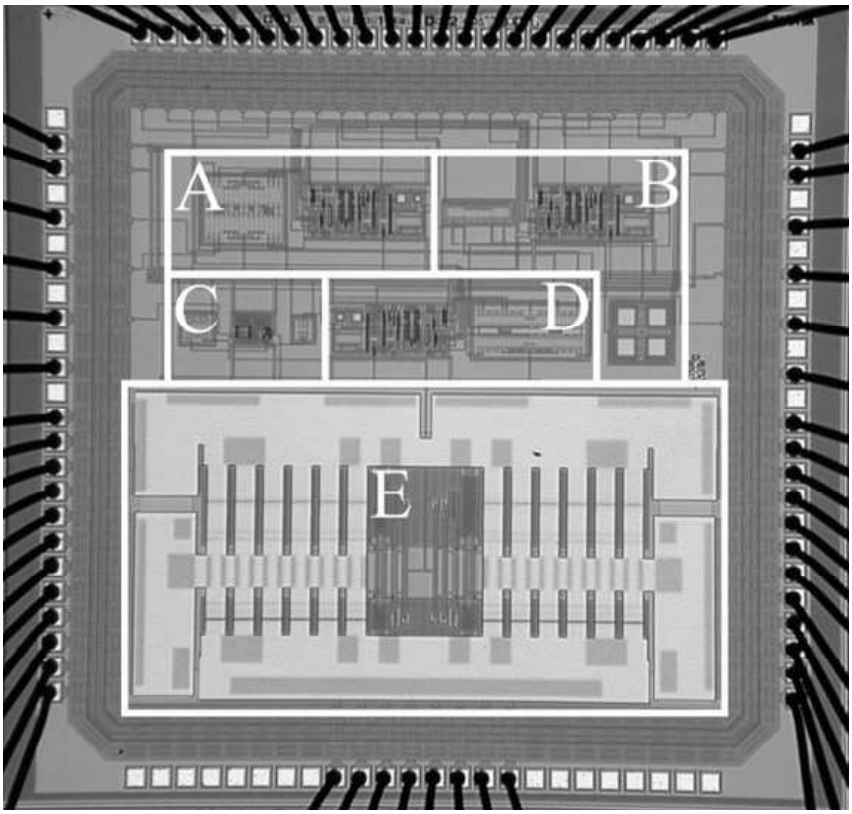


Fig. 48. Micrograph of the proposed class D audio power amplifier

Figure 48 depicts the class D audio amplifier integrated circuit (IC) micrograph where block A represents the operational amplifier A from Fig. 45, block B and D represent operational amplifiers B and C, respectively. The comparator is highlighted in block C, and the output power stage of the class D audio amplifier is shown as block E.

Figure 49 shows efficiency of the fabricated prototype. The class D amplifier presents high efficiency (higher than 90%) for high input voltages and it also has an acceptable efficiency (above 70%) for medium input voltages. The efficiency drops for lower voltages because the mechanisms of power dissipation, P_s and P_c, described in equation (3.21), become comparable to the output power. The value of these power dissipation mechanisms is directly related to the size of the transistors in the output stage, and to the switching frequency of the class D audio amplifier. Therefore, one possible way to boost the efficiency for low input voltages would be to have a reconfigurable output stage with a

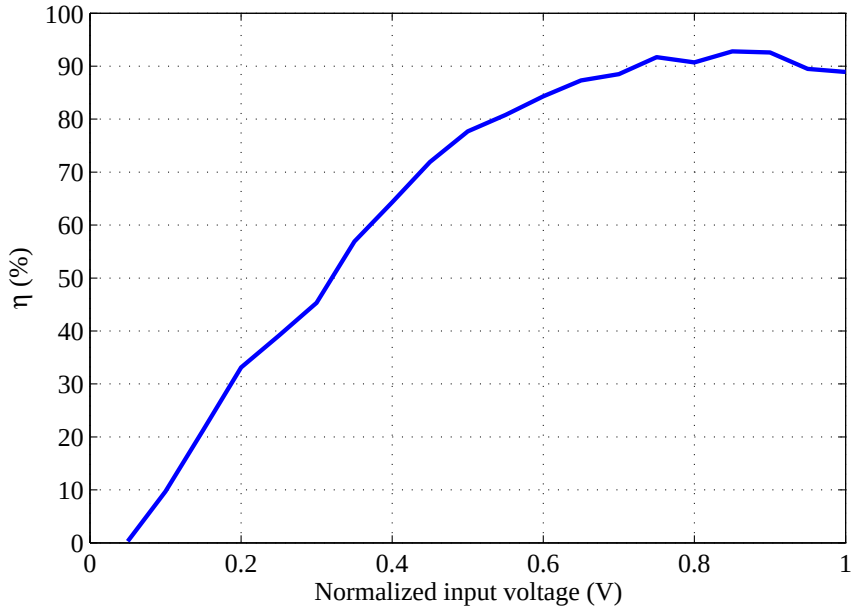


Fig. 49. Class D audio amplifier efficiency versus normalized input voltage

variable switching frequency.

Figure 50 shows the output waveforms of the system for 1 V, 1 kHz sinusoidal input signal. The pseudo-differential outputs are v_{OUT+} and v_{OUT-} and the differential signal, displayed in a different scale, is v_{OUT}.

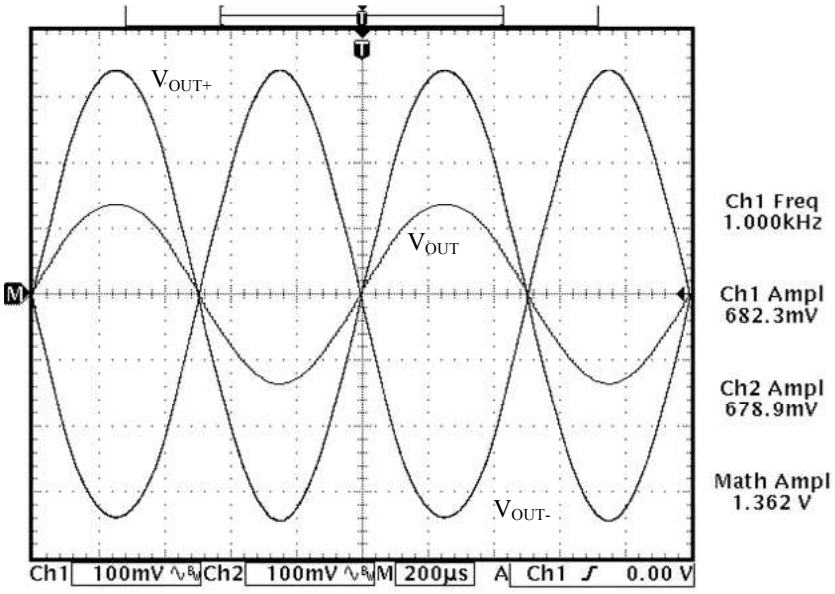


Fig. 50. Class D audio amplifier output waveforms for 1 V, 1 kHz sinusoidal input signal

Figure 51 shows the class D audio amplifier output spectrum for v_A = 300 mV, where the second harmonic, at 2 kHz, is the first unwanted signal to appear. This problem can be avoided in a true fully-differential architecture.

Testing measurements showed a better linearity of the class D audio amplifier at low modulation indexes and a degradation of the THD as the amplitude of the reference signal v_A increases. This fact is important because, in real audio applications, most of the power

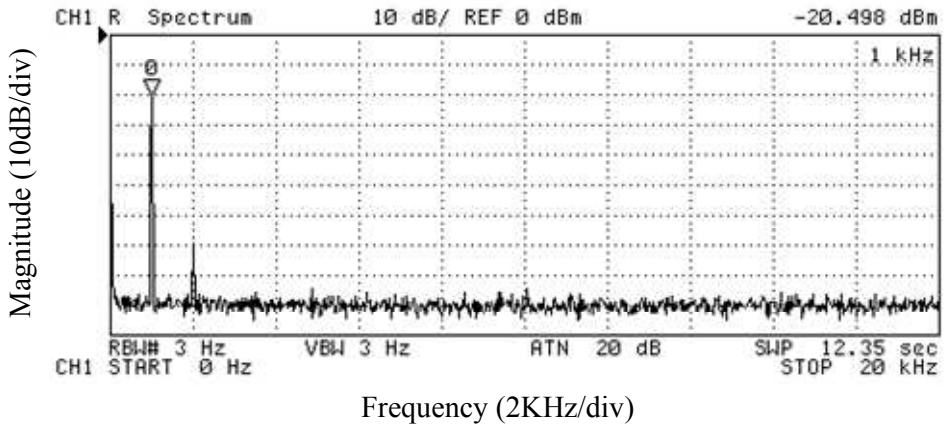
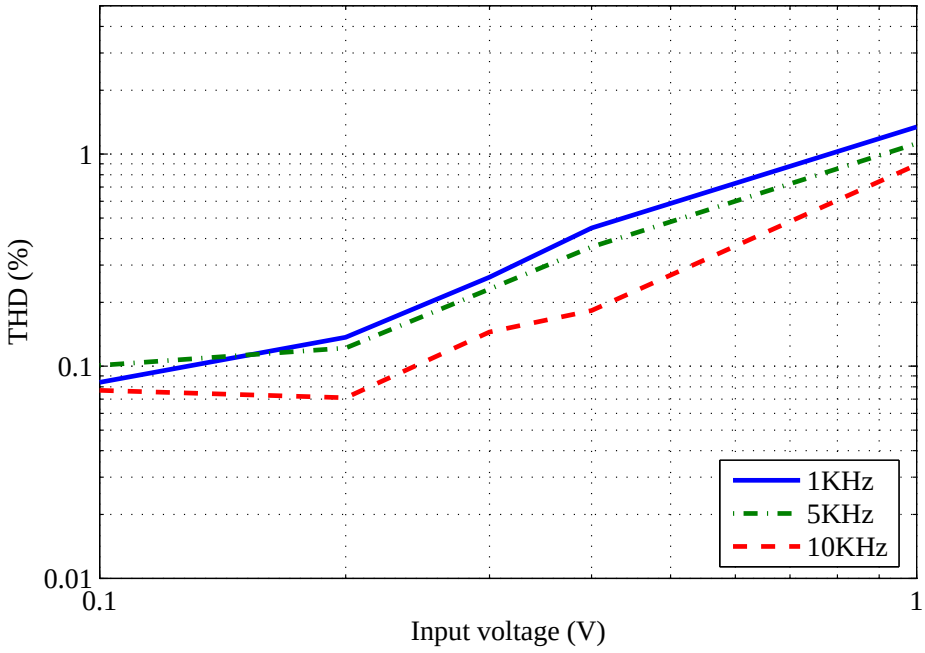


Fig. 51. Class D audio power amplifier output spectrum for v_A = 300 mV

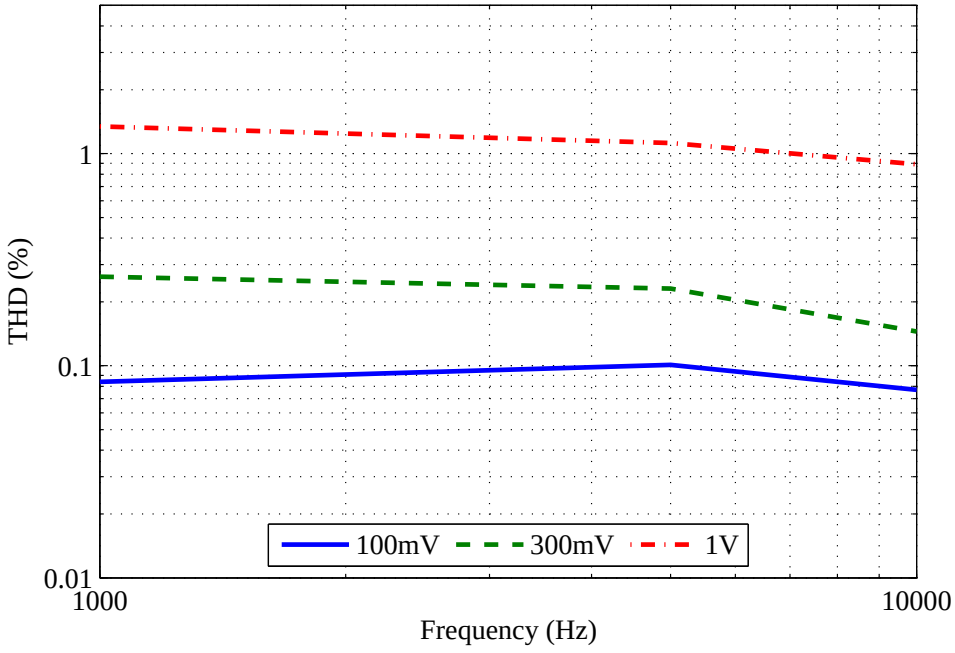
of the audio signal concentrates at low modulation indexes.

At high modulation indexes the THD is approximately 1.50%, but for low modulation indexes, the THD decreases down to 0.08%, as shown in Fig. 52(a), which meets the requirements for high fidelity audio applications. On the other hand, the THD performance of the class D amplifier versus the audio frequency is plotted in Fig. 52(b). Observe that the linearity is constant within the audio band for all the different input signals.

Fig. 53(a) depicts the signal-to-noise ratio (SNR) with respect to v_A = 1 V. The power-supply rejection ratio (PSRR) of the class D audio amplifier, shown in Fig. 53(b), is computed with a ripple on the power supply of 100 mV. Observe that the closed-loop created by the sliding mode controller provides a strong isolation for external perturbations.

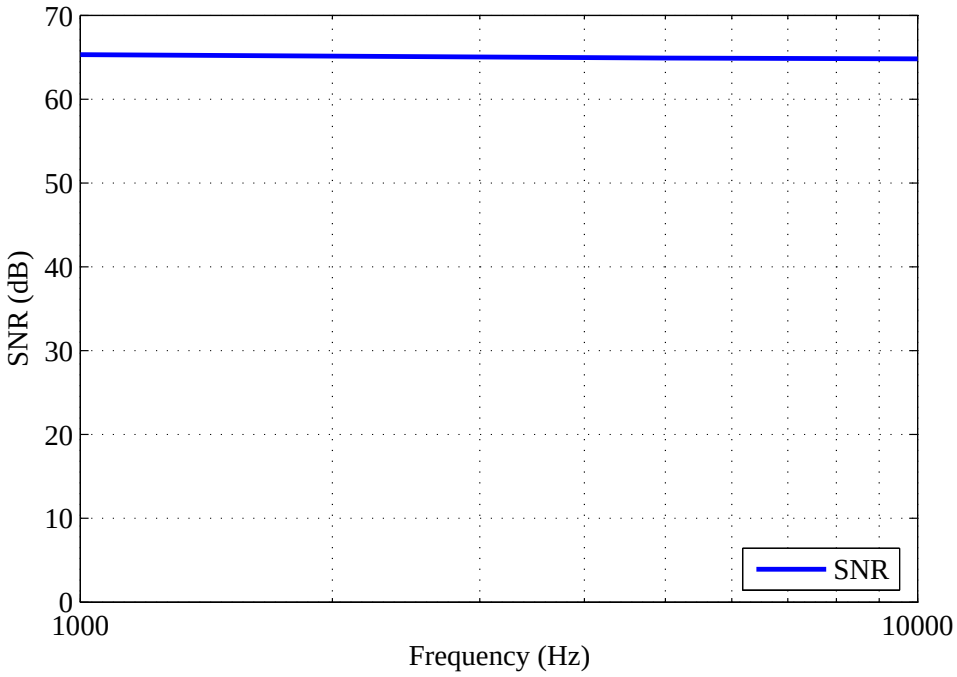


(a)

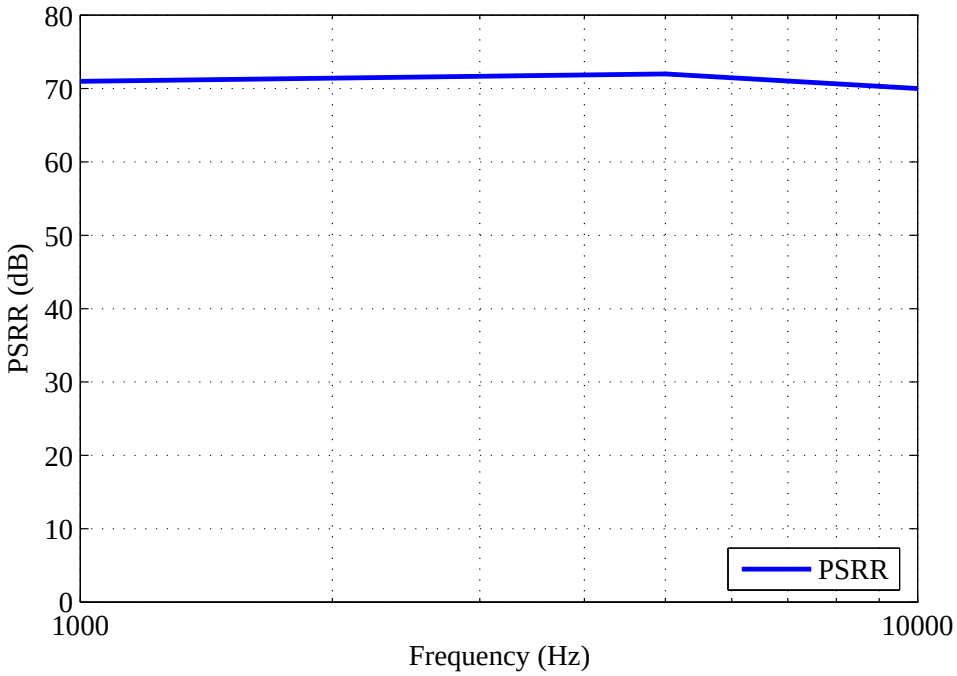


(b)

Fig. 52. Experimental results of harmonic distortion (a) THD versus input voltage v_A and (b) THD versus audio frequency input



(a)



(b)

Fig. 53. Frequency measurements for class D audio amplifier (a) SNR with respect to 1 W into 8 Ω load and (b) PSRR with 100 mV signal coupled to DC voltage supply

The proposed class D audio amplifier was exposed to postlayout simulations with different corner conditions and temperature variations. Simulations results with corner parameters show a worst case variation of 0.1% and 4.3% for THD and efficiency, respectively. Temperature was swept from -40° C to 40° C and the simulations resulted with a variation of ± 3% and ± 0.015% for the efficiency and total harmonic distortion, in that order. The performance of the system was worse at high temperatures and it improved at low temperatures. The results of postlayout simulation, at multiple temperature conditions and different process corners variations, demonstrate the robustness of the proposed class D audio amplifier.

Stability of the class D audio amplifier was tested by applying a square waveform input and obtaining the step response of the system, as shown in Fig. 54. Due to the real and negative eigenvalues of the system, as derived in Appendix B, the step response presents

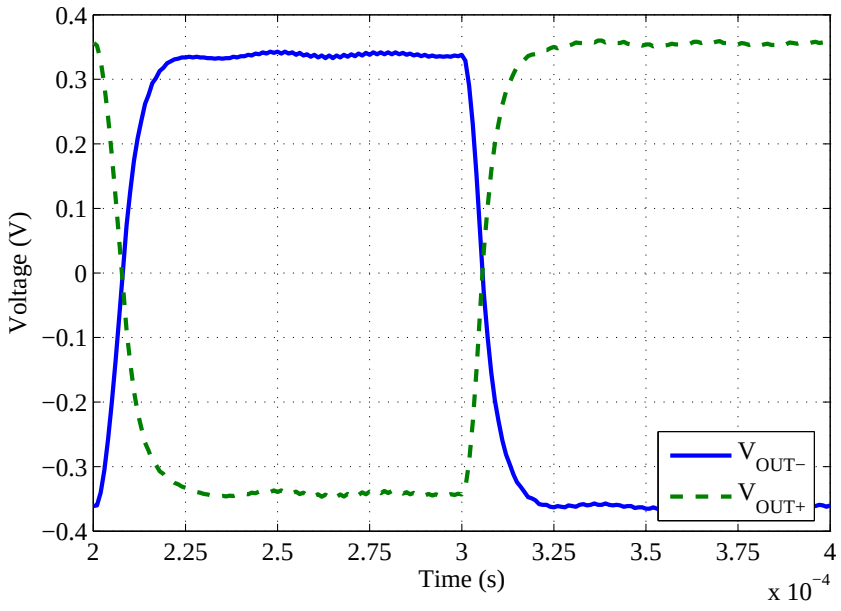


Fig. 54. Step response of proposed class D audio power amplifier

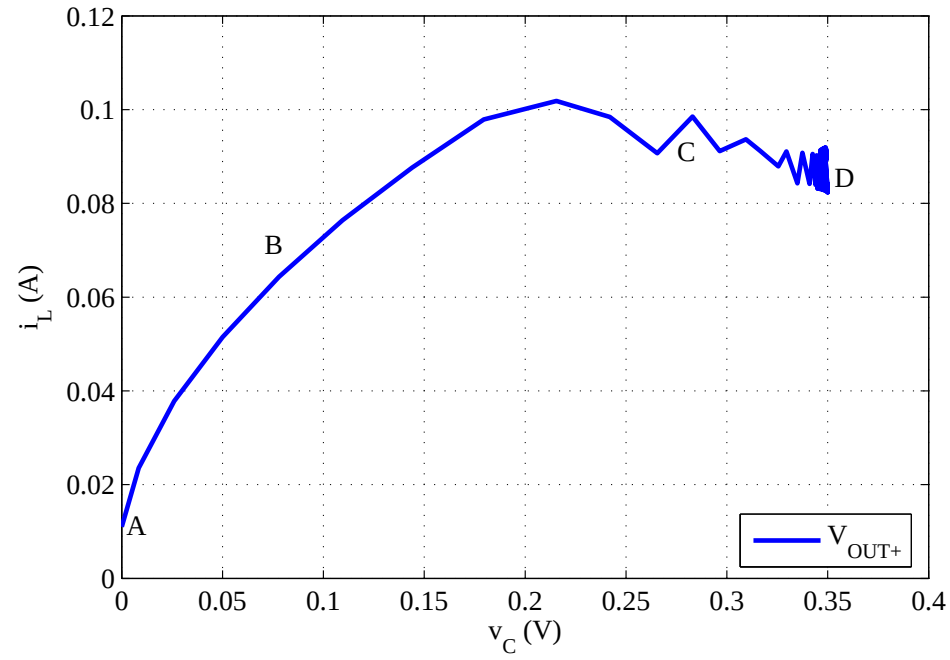
no overshoot and fast time response of 25 μs, approximately.

The movement of the states variables (v_C, i_L), from their initial conditions to the sliding equilibrium point, is plotted in Fig. 55. In this plot, all the different phases of the class D amplifier operation under sliding mode control, in response to an input step, can be appreciated. The system starts at its initial condition (A) and then it moves, i.e. the reaching mode (B), from the starting point to the sliding surface (C), once there it goes into the sliding mode toward the sliding equilibrium point (D). It is interesting to note that the chattering is an effect of the non-ideal sliding mode and it decreases as the switching frequency increases. Also, when the sliding equilibrium point is reached, the system starts switching at a fixed frequency to minimize the error function.

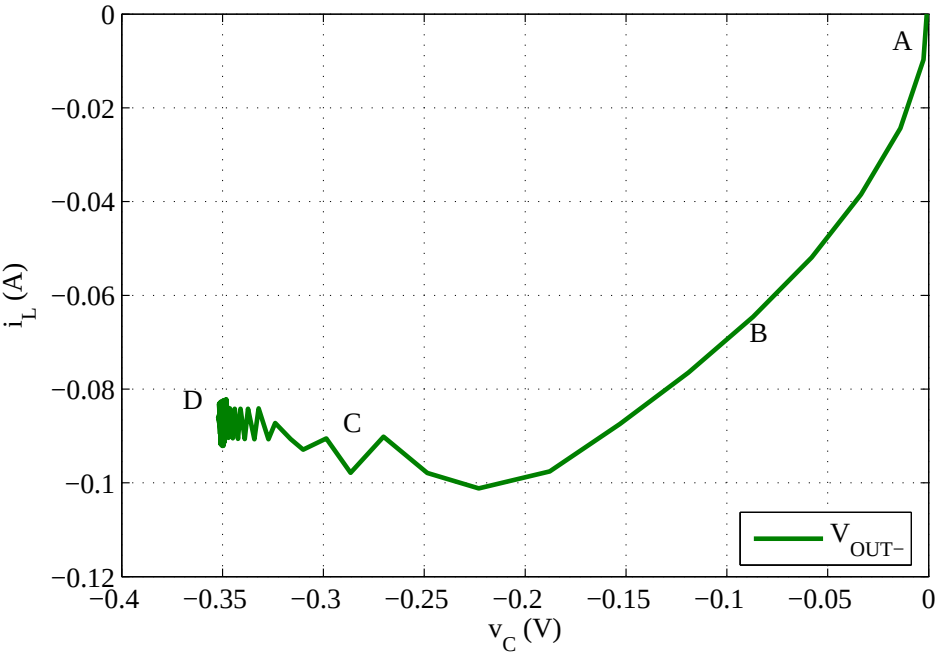
A comparative table with other class D amplifiers is presented in Table IV where a figure-of-merit (FOM), with a normalization factor of 10^5, is proposed to compare the performance of the different amplifiers taking in consideration their main characteristics, i.e. total harmonic distortion (THD), efficiency (η), and current consumption (I_Q).

$$FOM = \frac{\eta}{I_Q \times THD \times 10^5} \tag{3.22}$$

Notice that the proposed class D audio power amplifier provides the best linearity when compared to the other single-ended architectures. A fully-differential version would provide more robustness to common mode noise and ideally it would cancel the even harmonics. Still, observe that the proposed single-ended audio amplifier with sliding mode is still competitive to the rest of the previous reported works and yet, consumes lower quiescent power. Notice that even though the amplifier proposed in [20] provides the best figure of merit, its linearity is very poor when compare to the rest of the class D audio power amplifiers.



(a)



(b)

Fig. 55. Sliding mode operation of class D audio power amplifier for zero initial conditions (a) $v_{(OUT+)}$ and (b) $v_{(OUT-)}$

Table IV. Performance summary of class D audio power amplifiers

Design	THD (%)	η (%)	Supply (V)	Load (Ω)	I_Q (mA)	P_Q (mA)	FOM
[6]‡§	0.40	87	2.7	4	2.8	7.56	0.8
[7]‡§	0.08	85	5.0	4	8.0	40.00	1.3
[8]‡	0.03	76	4.2	8	4.7	19.74	5.4
[9]‡	0.04	79	3.6	8	2.5	9.00	7.9
[15]†	0.11	70	5.0	8	-	-	-
[16]‡	0.20	-	3.0	8	-	-	-
[17]†	0.20	90	5.0	4	-	-	-
[20]‡	0.28	92	2.5	8	0.1	0.25	33
[21]†	0.10	92	12.0	8	-	-	-
SMC†	0.08	91	2.7	8	2.0	5.40	5.7

† Single-ended architecture

‡ Fully-differential architecture

§ Commercial products

E. Conclusion

In this chapter, sliding mode control and negative feedback have been applied to the design of class D audio power amplifiers. Advantages and limitations are discussed as well as a design procedure to select design parameters to yield a class D audio amplifier for a given linearity requirement. A low-voltage low-power IC class D audio amplifier has been

designed and fabricated in 0.5 μm CMOS technology using these techniques. It presents efficiency above 90% and a THD as low as 0.08%.

Sliding mode control theory and an extra local feedback loop are employed to yield high efficiency, robust stability and enhanced linearity. One of the main advantages of this amplifier compared with conventional architectures is the lack of a high frequency carrier modulator which always increases complexity and produces non-linearity due to the non-ideal triangle wave signal.

It has been shown that class D audio amplifiers can achieve high linearity keeping their inherent high efficiency nature and make them a very attractive solution for applications with critical battery life.

CHAPTER IV

TWO LOW-POWER HIGH-EFFICIENCY CLASS D AUDIO POWER AMPLIFIERS*

The architecture, design and implementation of two clock-free analog class D audio power amplifiers using 0.5 μm CMOS standard technology are introduced in this chapter. Both designs operate with a 2.7 V single voltage supply and deliver a maximum output power of 250 mW into an 8 Ω speaker. The two class D audio power amplifiers are based on a hysteretic sliding mode controller, which avoids the complex task of generating the highly linear triangle carrier signal used in conventional architectures. The first design generates a two-level modulated signal and is called binary modulated amplifier (BMA); the second topology produces a three-level modulated signal, hence is named ternary modulated amplifier (TMA).

The architectures and implementations are simple and compact, providing very low quiescent power consumption. Experimental results of the BMA/TMA yield an efficiency of 89/90% and a total harmonic distortion plus noise (THD+N) of 0.02/0.03%, respectively. The efficiency and linearity are comparable to state-of-the-art amplifiers but the static power consumption is less than one tenth of previous proposed architectures. Both class D audio power amplifiers achieve a power supply rejection ratio greater than 75 dB at 217 Hz, and a signal-to-noise ratio (SNR) higher than 90 dB within the whole audio band. Each amplifier occupies less than 1.5 mm^2.

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*Reprinted with permission from "Two class-D audio amplifiers with 89 / 90% efficiency and 0.02 / 0.03% THD+N consuming less than 1 mW of quiescent power" by M. A. Rojas-González and E. Sánchez-Sinencio, 2009. *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 450-451, © 2009 by IEEE.

A. Introduction

Due to their ideally perfect efficiency and linearity, class D amplifiers (CDAs) have become a very attractive solution to implement audio drivers in applications with crucial power consumption and low-voltage requirements. However, component non-idealities degrade the audio quality when compared to the ideal amplifier. Hence, in order to achieve low distortion, the audio modulator often becomes complex and power hungry.

Even with practical drawbacks of a real implementation, class D audio power amplifiers exceed the efficiency of traditional class A, class B and class AB audio amplifiers, as illustrated in Fig. 56. Observe that class A and class B curves are ideal, and the class D curve is an actual measured efficiency. In contrast, the linearity achieved by class D audio amplifiers is worse when compared to the performance of their counterparts. Therefore, the main challenge in designing class D audio amplifiers is to maintain their high efficiency inherent characteristic while improving the linearity and minimizing the quiescent power consumption.

Conventional class D amplifiers based on pulse-width modulation (PWM) architectures [8],[9] require generation of a highly accurate carrier signal, because any nonlinearity present in that signal impacts the distortion of the amplifier. Since the carrier wave is ideally periodic with infinitely many harmonics, the ramp generator requires high accurate circuitry and large bandwidth, increasing complexity and power consumption to the overall system. On the other hand, high-performance topologies based on conventional $\Delta\Sigma$ modulators must be modified to avoid instability and to improve efficiency [13], [14], resulting in amplifiers unsuitable for battery-powered applications due to their intricate, power hungry audio modulator. Other topologies based on alternate modulation techniques have been proposed [24], but their linearity performance is limited, and their quiescent power consumption is still high.

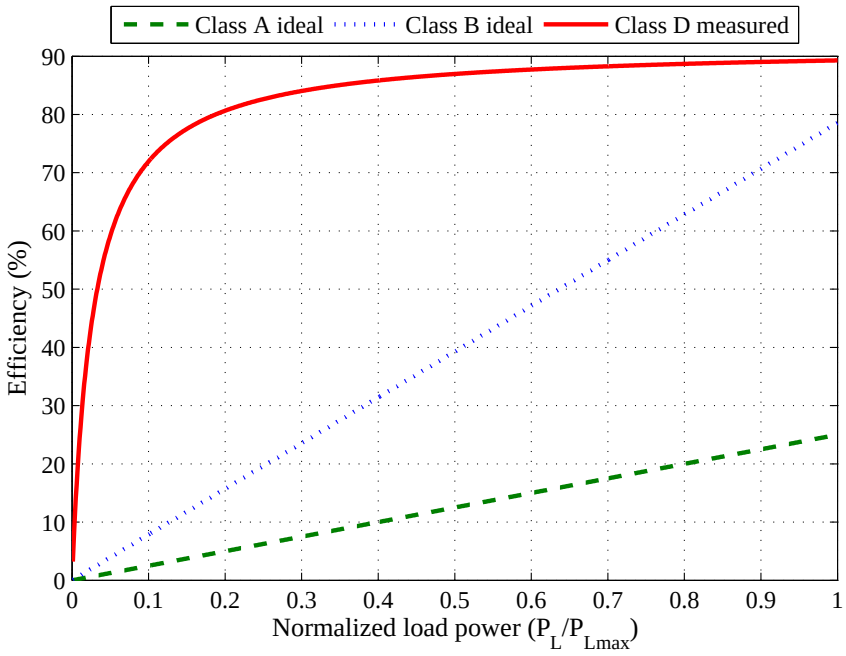


Fig. 56. Normalized power efficiency of ideal class A and class B audio power amplifiers, and real class D audio power amplifier

This chapter presents two different architectures and design methodologies to implement high-performance class-D audio amplifiers with minimal power consumption [25]. Both topologies: a binary modulation amplifier (BMA) and a ternary modulation amplifier (TMA), are based on the same principle: a hysteretic controller based on sliding mode [33]. The chapter is organized as follows. Section B explains the controller design and linearity enhancement, Section C details the BMA/TMA operation, Section D outlines the circuit level design, and Section E presents measurement results. Conclusions are given in Section F.

B. Controller Design and Linearity Enhancement

The proposed class D audio amplifiers are based on the block diagram shown in Fig. 57(a). The architecture implements a sliding mode controller (SMC) defined by the control law, or switching function (SF) [24], [33]

$$s(e_1, t) \;=\; e_1(t) \;+\; \alpha \dot{e}_1(t) \;=\; e_1(t) \;+\; \alpha e_2(t) \tag{4.1}$$

where the sliding parameter α is calculated to meet the Hurwitz stability criterion and to guarantee a fast and smooth transient response with flat delay characteristic, and $e_1(t)$ is the voltage error function given by

$$e_1(t) \;=\; v_{IN}(t) \;-\; v_{OUT}(t) \tag{4.2}$$

and

$$\frac{d}{dt} e_1(t) \;=\; e_2(t) \;\triangleq\; \frac{d}{dt} e_1(t) \tag{4.3}$$

The system can be proven to be asymptotically stable, as shown in Appendix B, since its sliding equilibrium point (SEP) [33], [56] is a stable node whose eigenvalues are real and negative. On the other hand, non-ideal elements in the system compromise the linearity of the class D amplifier. An extra local loop with negative feedback β is added to improve the linearity without jeopardizing the stability. This factor β requires an extra adder node as shown in Fig. 57(a). Figure 57(b) illustrates an equivalent but topologically simpler block diagram that eliminates one adder.

The remaining blocks of the system in Fig. 57 are the hysteresis comparator and the output power stage. The comparator converts the analog control signal in equation (4.1) to a pulse-width modulated (PWM) signal, according to the sign of the switching function. The power stage generates the driving capability to supply the output current to the load, and simultaneously minimizes the output resistance. An off-chip second-order

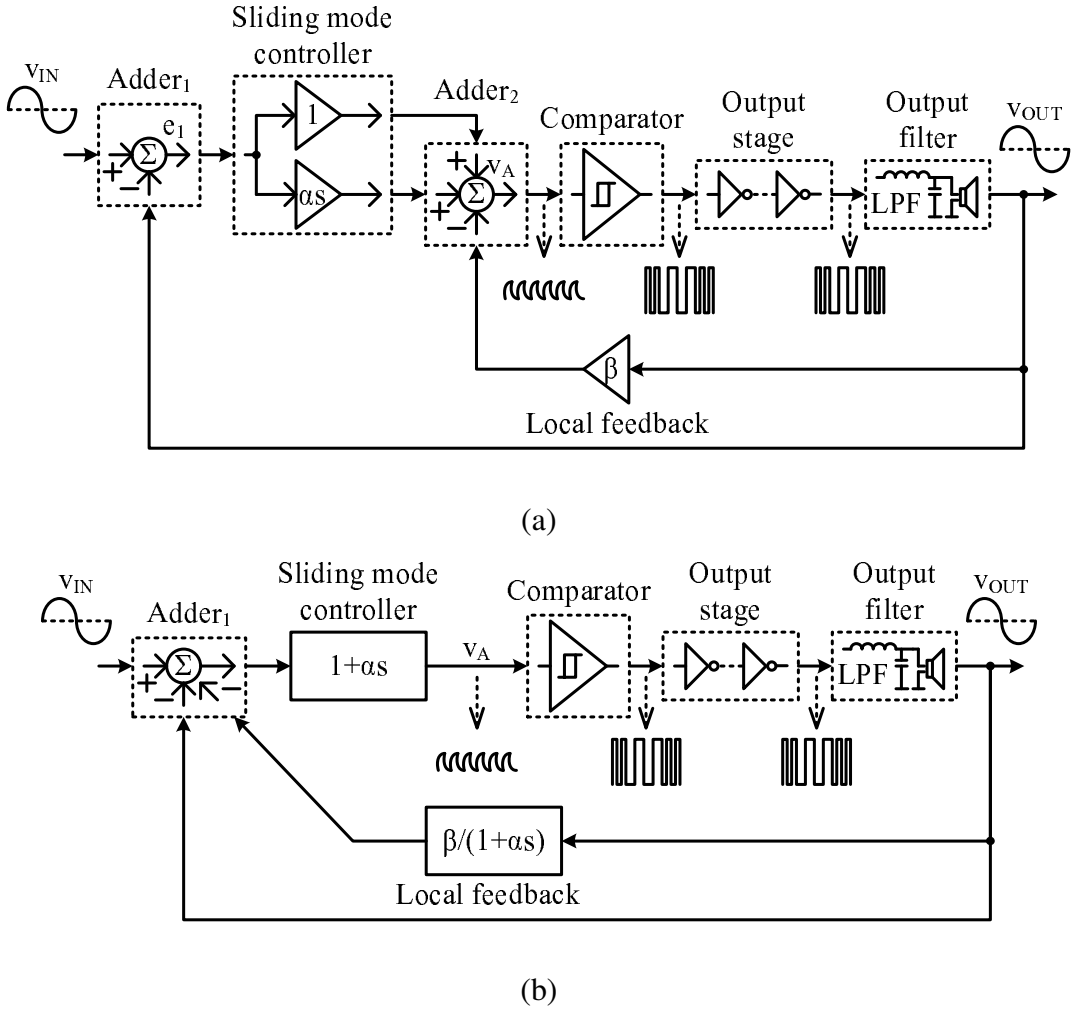


Fig. 57. Proposed class D audio power amplifiers architectures (a) Two-adder implementation and (b) One-adder implementation

flat-response low-pass filter (LPF), with typical component values L = 45 μH, C = 1.4 μF, and an 8 Ω speaker, recovers the analog audio signal. If needed, the class D amplifier can be converted to a filter-less architecture [9] by using the parasitic components of the speaker as an embedded filter and adjusting the coefficient α in the controller to fit the speaker model parameters.

A noise constraint to ideally implement the sliding mode controller is the lossless differentiator function in equation (4.1), due to its infinite bandwidth. A practical solution is to implement a lossy-differentiator (LD) function, with a finite bandwidth ω_{p}, in the control law as

$$S(E_1, s) = \left[1 + \left(\frac{\alpha s}{\frac{s}{\omega_p} + 1}\right)\right] E_1(s) \tag{4.4}$$

where $\omega_{\mathrm{p}} = 2\pi \mathrm{f_p}$. This lossy-differentiator, together with a finite bandwidth operational amplifier (OPAMP) bounds the class D audio amplifier bandwidth required in the system and limits the high-frequency bandwidth noise that could affect the signal-to-noise ratio (SNR) of the audio power amplifier.

Figure 58 illustrates two cases where it can be appreciated that the lossy differentiator with pole $\omega_{\mathrm{p2}} = 20 / \alpha$ gives better linearity than that with $\omega_{\mathrm{p1}} = 10 / \alpha$, since the higher-frequency pole allows for a switching function closer to the ideal control law expressed in equation (4.1). On the other hand, a lossy-differentiator with a higher-frequency pole translates into larger overall controller bandwidth and hence more quiescent power consumption. We thus have a design trade-off between linearity and power consumption of the class D amplifier. The value $\omega_{\mathrm{p}} = 10 / \alpha$ was chosen for the particular design described in this chapter.

The linearity of the class D audio amplifiers increases because the distorting harmonics are reduced by the feedback factor β, as shown in equation (4.5). However, from the expression in equation (4.6), the fundamental tone is also attenuated.

$$THD = \sqrt{\left(\frac{HD_2}{(1+\beta)^2}\right)^2 + \left(\frac{HD_3}{(1+\beta)^3}\right)^2 + \cdots + \left(\frac{HD_N}{(1+\beta)^N}\right)^2} \tag{4.5}$$

$$v_{OUT} = \left(\frac{1}{1+\beta}\right) v_{IN} \tag{4.6}$$

Figure 59 illustrates the effect of the hysteresis-window width in the linearity of the class D audio amplifiers and Fig. 60 shows the effect of the hysteresis voltage window in

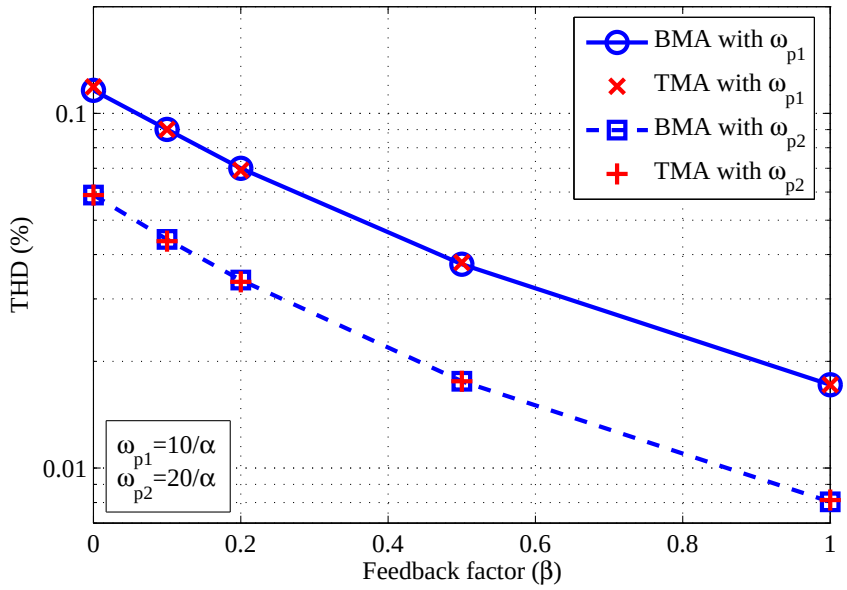


Fig. 58. Effect of feedback factor β in the linearity performance of the class D audio amplifiers

the switching frequency of the amplifiers.

The switching frequency, as it will be shown later, increases inversely proportional to the hysteresis voltage window width [60]. In an ideal system operating with sliding mode control, the hysteresis window is zero and the switching frequency is infinite. Also notice that both amplifiers BMA/TMA provide the same linearity, provided that they switch around the same frequency. This fact is of particular importance because the odd carrier harmonics of the TMA cancel due to the additional modulation level, and its effective switching frequency doubles [26].

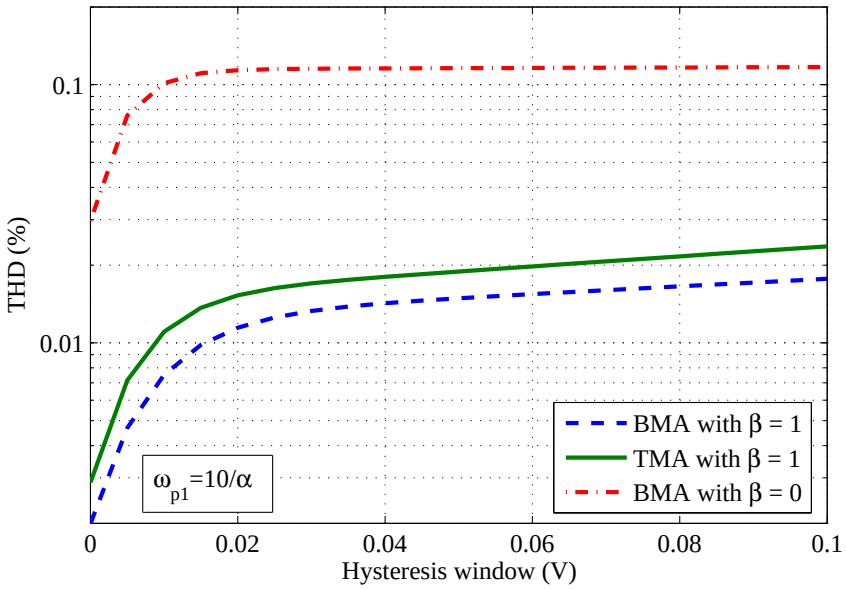


Fig. 59. Effect of the hysteresis-window width in the linearity performance of the class D audio amplifiers

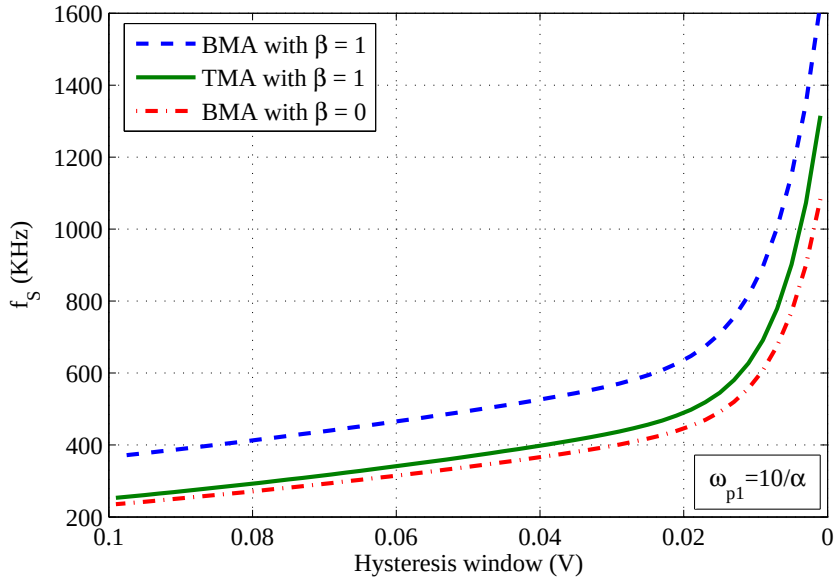


Fig. 60. Effect of the hysteresis-window width in the class D audio power amplifiers switching frequency

Since the BMA requires a smaller hysteresis level than the TMA to achieve a given linearity and to switch at approximately the same effective frequency, the comparator in the latter configuration can be designed with more relaxed specifications and lower power consumption. However, there exists a practical trade-off between the amplifier's frequency of operation and its efficiency because the dynamic power losses of the audio amplifier are proportional to the operating frequency [44]. Fig. 61 shows the theoretical class D amplifier efficiency when the switching frequency is increased from 200 kHz to 2 MHz. Even though the efficiency at full power is still high, the class D audio amplifier with higher switching frequency presents significant efficiency reduction at the most common load configurations.

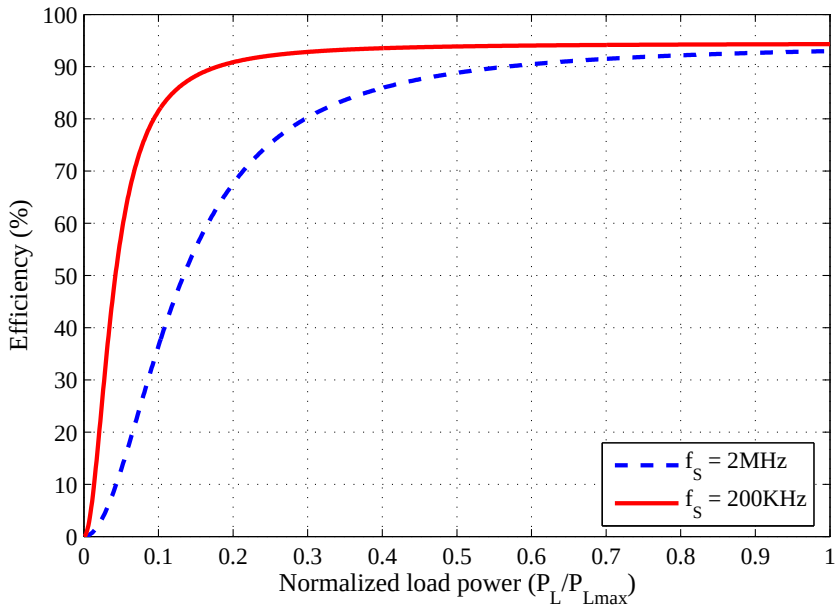


Fig. 61. Effect of the increment of switching frequency in the class D audio amplifiers efficiency performance

Finally, Fig. 62 shows the effect of increasing the feedback factor β in the switching frequency and in the linearity of the class D amplifiers, when the hysteresis window is kept fixed. It can be appreciated that the switching frequency variation is small in both amplifiers.

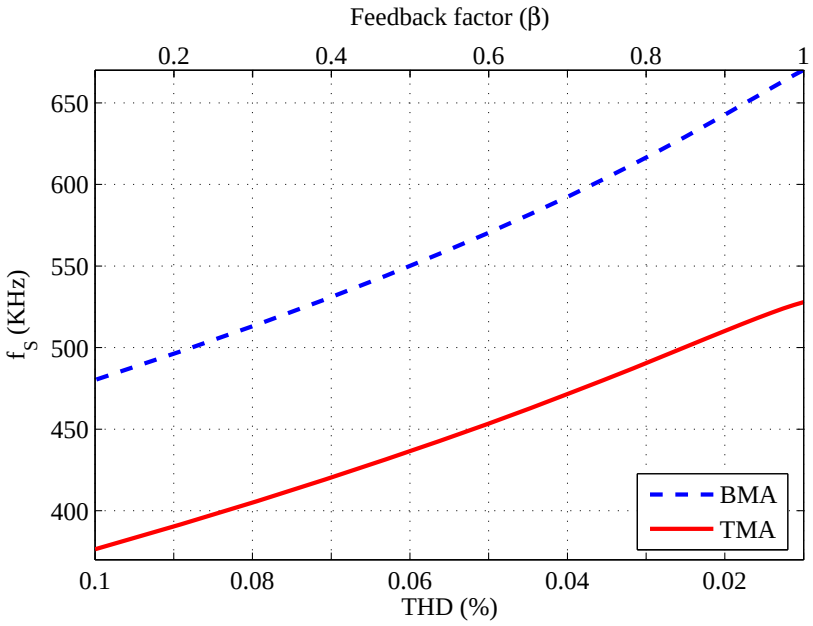


Fig. 62. Effect of β on class D amplifiers switching frequency. Lower (upper) horizontal axis represents THD (β)

C. Proposed Class D Audio Power Amplifiers

The implementation of the switching function described in equation (4.4), by using finite bandwidth circuits (the operational amplifier is characterized by one single dominant pole

at ω_{3dB}), modifies the control law and adds an extra pole to the system, but it does not compromise the class D audio amplifiers stability. As mentioned before, this extra pole limits the high frequency noise and bounds the class D amplifiers bandwidth. The new switching function including the additional pole is

$$S(E_1, s) = \left[\frac{1}{\left(1 + \frac{s}{\omega_1}\right)} + \frac{\alpha s}{\left(1 + \frac{s}{\omega_2}\right)\left(1 + \frac{s}{\omega_3}\right)} \right] E_1(s) \tag{4.7}$$

where ω_1 is the extra pole introduced by the OPAMP closed loop finite bandwidth, and ω_2 and ω_3 are the poles affected by the finite OPAMP closed loop pole (ω_{3dB}) and the lossy-differentiator pole (ω_p). Note that

$$\omega_1 > \omega_2, \omega_3 \tag{4.8}$$

The control law is built using the minimum number of components in both amplifiers in order to reduce silicon area, and more importantly, to reduce the static power consumption of the class D audio power amplifiers. The following sections provide the details of the BMA/TMA switching-function implementations.

1. Binary Modulation Class D Audio Amplifier (BMA)

Recalling the class D amplifier architecture shown in Fig. 57(a), its straightforward active-RC implementation consists of three different building blocks: two adders and one lossy-differentiator [24]. Instead, if the class D amplifier architecture is modified as shown in Fig. 57(b), the whole controller can be implemented using one single block if a fully-differential topology is used and since β is moved to the first adder node, the second adder can be eliminated. Therefore, the area and power consumption of the controller reduce considerably. Figure 63 shows the binary modulation amplifier (BMA) architecture.

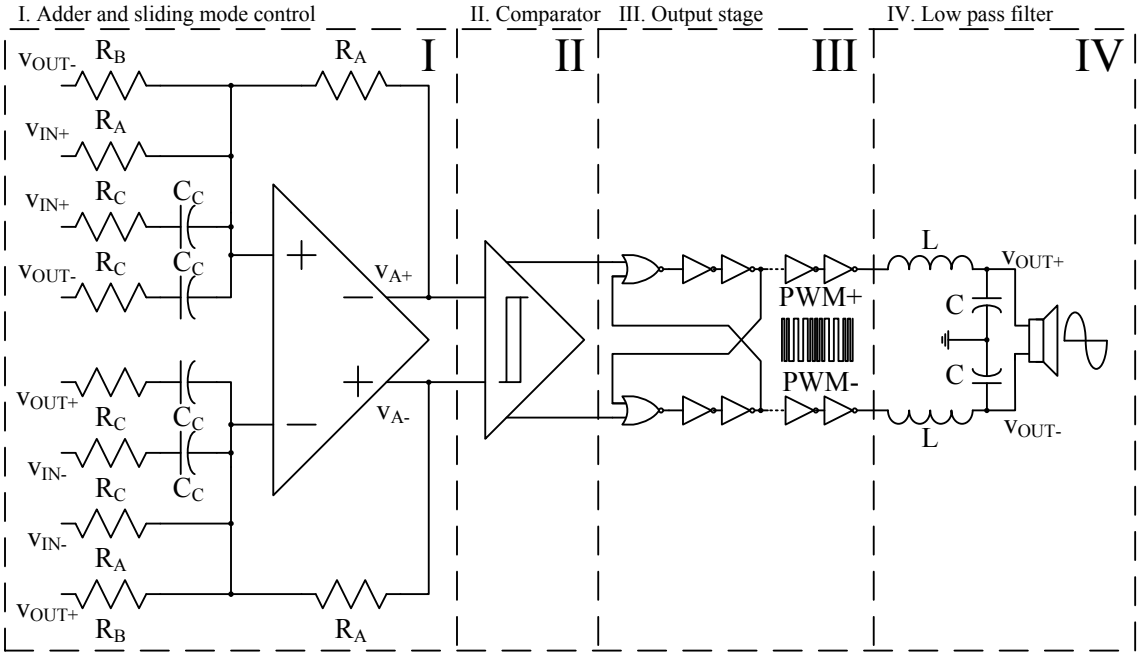


Fig. 63. Binary modulation amplifier (BMA) architecture

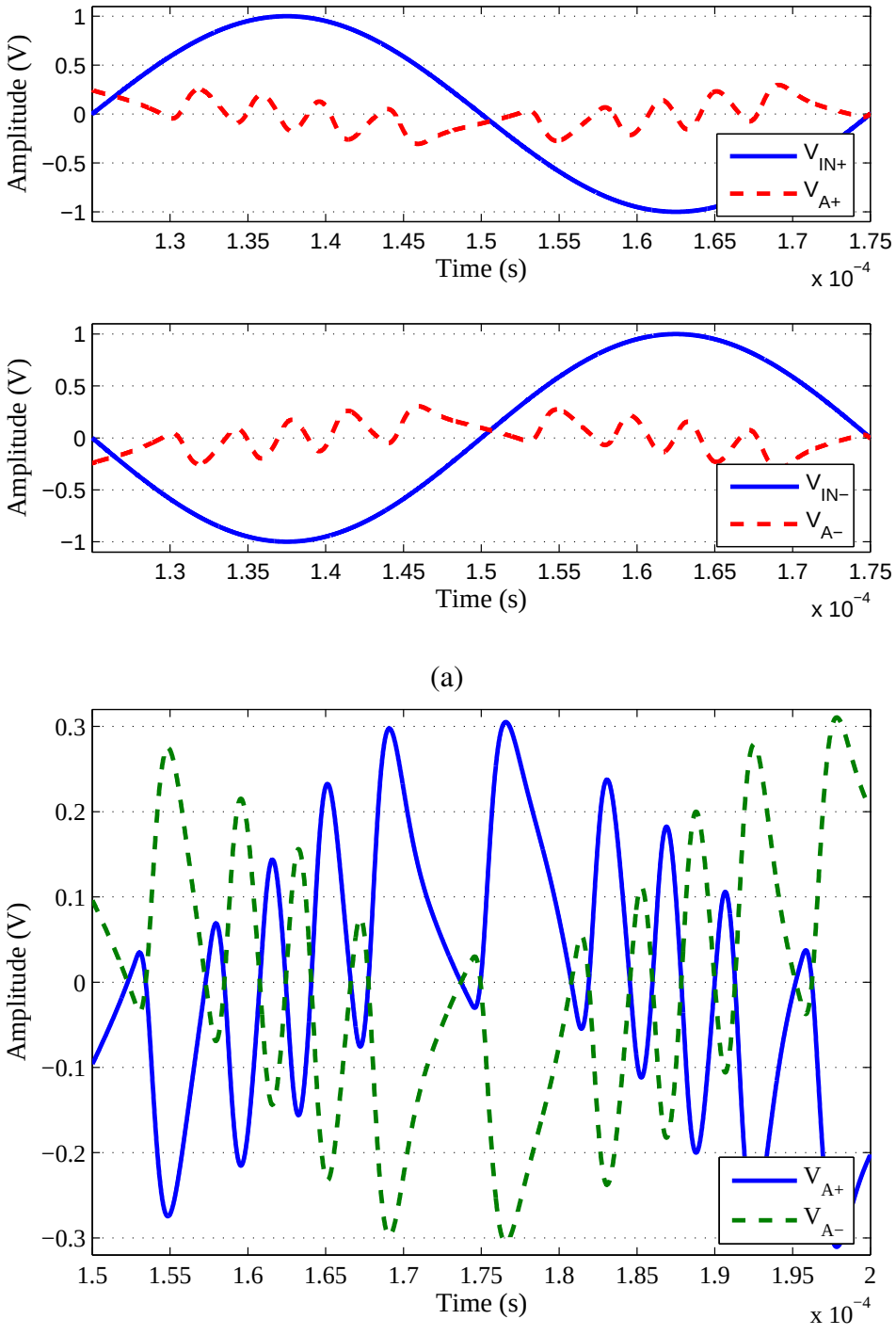
Examining node v_A at Fig. 57(b) yields

$$v_A(t) \;=\; \left[v_{IN}(t) \;+\; \alpha\frac{d}{dt}v_{IN}(t)\right] \;-\; \left[(1 \;+\; \beta)v_{OUT}(t) \;+\; \alpha\frac{d}{dt}v_{OUT}(t)\right] \qquad (4.9)$$

Note that for β = 0, equation (4.9) becomes the ideal switching function expressed before in equation (4.1). In the actual active-RC implementation, neglecting the operational amplifier non-idealities, and after the ideal differentiator (αs) is replaced by a lossy one [αs / (1 + s / ω_p)] , V_A(s) becomes

$$V_{A\pm}(s) \;=\; \left(1 \;+\; \frac{\alpha s}{1 \;+\; \frac{s}{\omega_p}}\right) V_{IN\pm}(s) \;\pm\; \left(1 \;+\; \beta \;+\; \frac{\alpha s}{1 \;+\; \frac{s}{\omega_p}}\right) V_{OUT\mp}(s) \qquad (4.10)$$

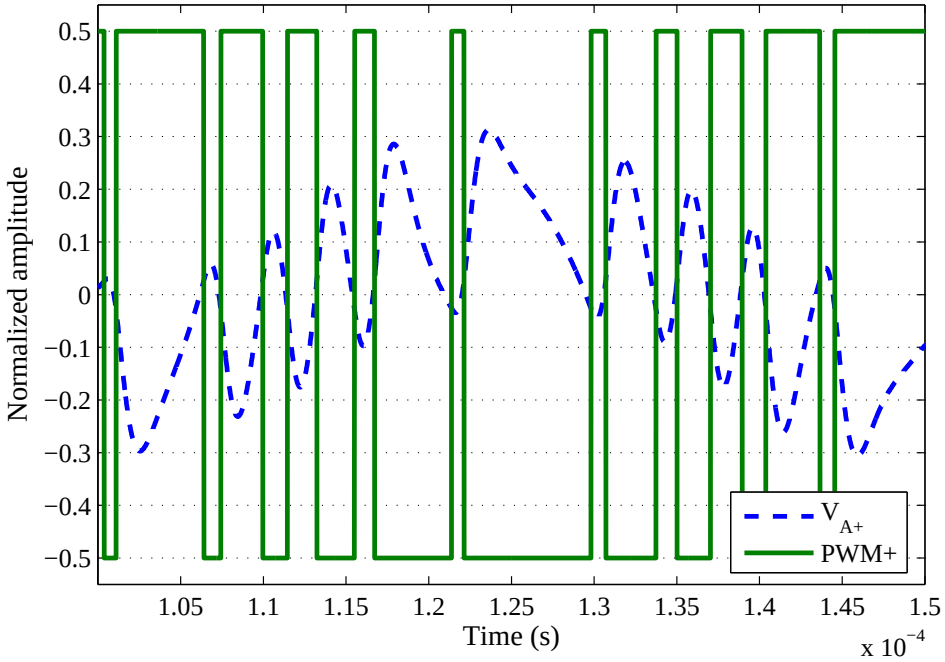
where $\alpha = R_A C_C$, $\omega_p = 1 / R_C C_C$ and $(1 + \beta) = R_A / R_B$.



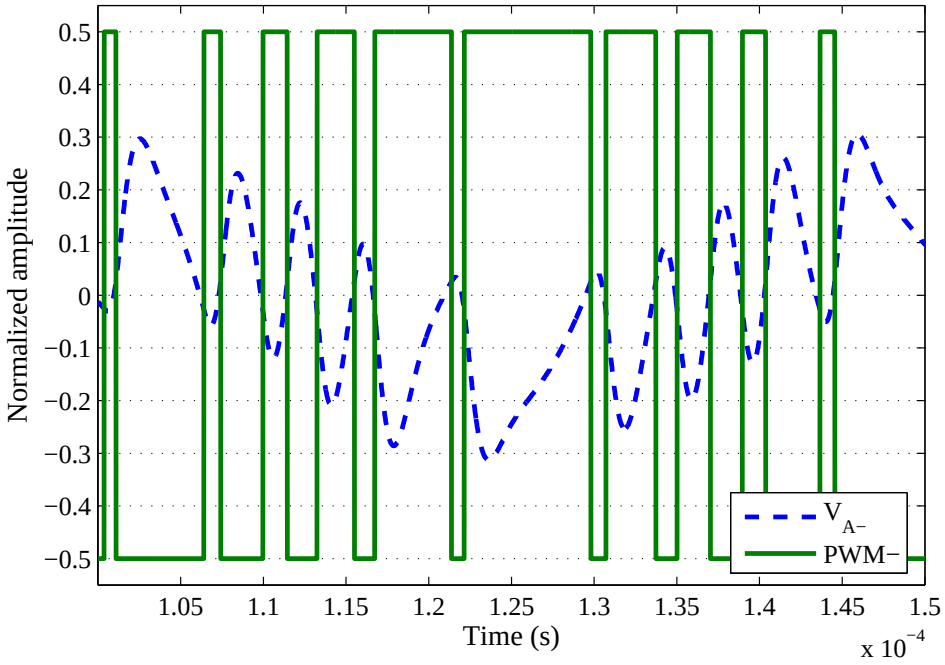
(a)

(b)

Fig. 64. Typical waveforms in the BMA (a) Input v_{IN} and output controller v_A and (b) Zoom in on differential signal v_A

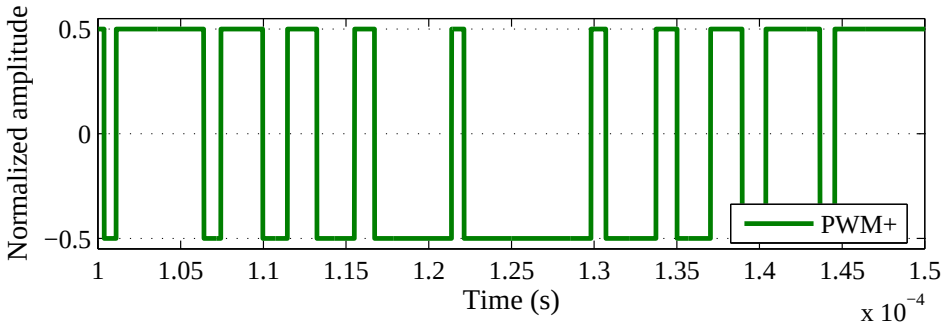


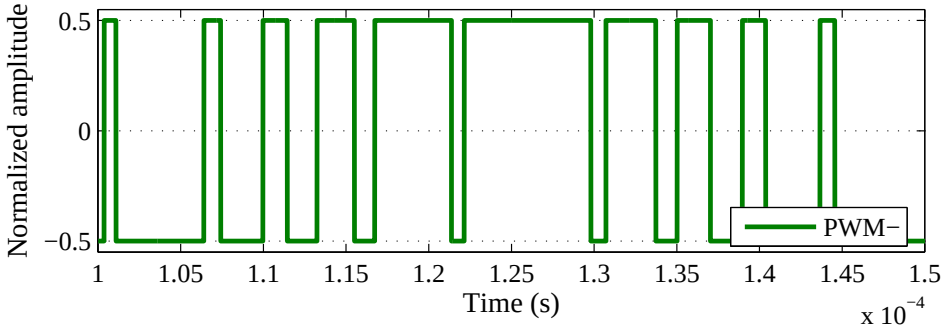
(a)



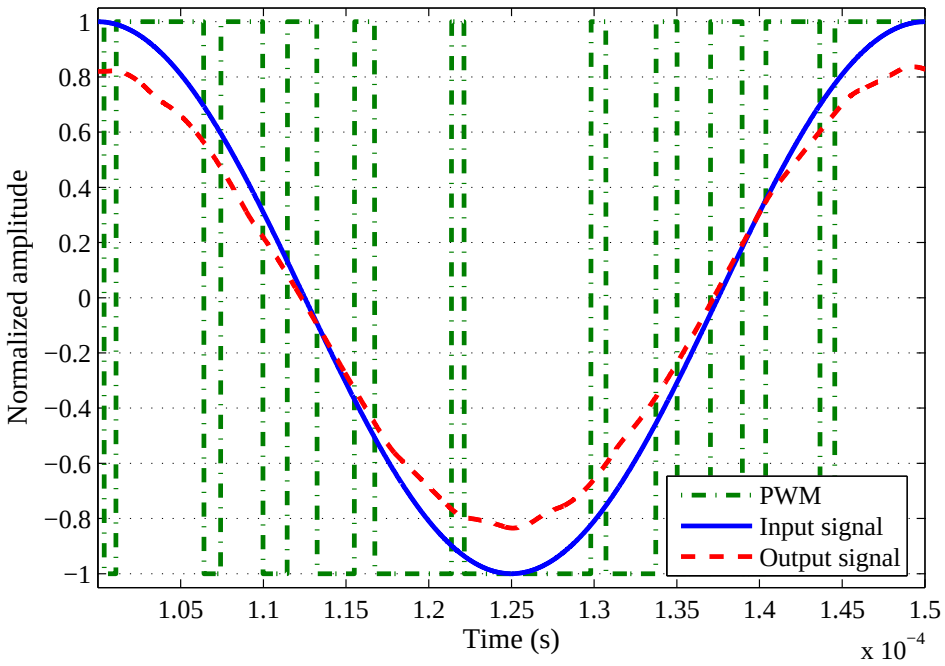
(b)

Fig. 65. Generation of the pulse-width modulation in the BMA when v_A exceeds hysteresis bound (a) Positive PWM+ and (b) Negative PWM-





(a)



(b)

Fig. 66. Input and output signals in the BMA (a) Differential PWM signals and (b) v_{IN}, v_{OUT} and (PWM+) - (PWM-)

Hence, a single fully-differential operational amplifier implements the error function, the lossy-differentiator, and the local feedback β. Figure 64 illustrates typical waveforms in the BMA. The signal v_A represents the output signal of the sliding mode controller and the feedback factor β. Observe that the wave is fully-differential. Figure 65 shows an example of the input and output signals of the comparator. The signal v_A, generated by the previous stage, is transformed into a binary signal, pulse-width modulated, which is fed to the load through the output stage. Figure 66 illustrates a simulated differential pulse-width modulated signal as well as the input and output voltages. Note that the output voltage is attenuated with respect to the input signal due to feedback factor β.

2. Ternary Modulation Class D Audio Amplifier (TMA)

The ternary modulation amplifier (TMA), shown in Fig. 67, uses two single-ended operational amplifiers, and the core implementation of the switching function with the lossy-differentiator as described in equation (4.4), however its topology is based on the architecture used in conventional pulse-width modulation schemes to generate ternary modulation based on a single carrier [8], [9]. More specifically, as shown in Fig. 68, in traditional architectures a single ramp wave is compared to a differential analog signal, generating two binary signals that, when subtracted, generate a third modulation level.

Since the proposed TMA topology, as well as the BMA, lacks of any reference carrier signal, the SMC and β factor are implemented as given by

$$V_{A\pm}(s) = \left(1 + \frac{\alpha s}{1 + \frac{s}{\omega_p}}\right) V_{IN\pm}(s) \mp \left(1 + \beta + \frac{\alpha s}{1 + \frac{s}{\omega_p}}\right) V_{OUT\pm}(s) \quad (4.11)$$

However, notice that the input $V_{IN}(s)$ and output $V_{OUT}(s)$ voltage signals create two independent single-ended loops driving a differential load, generating two different but complementary switching functions to be applied to the comparators. The difference of these two out-of-phase binary signals thus creates three voltage levels.

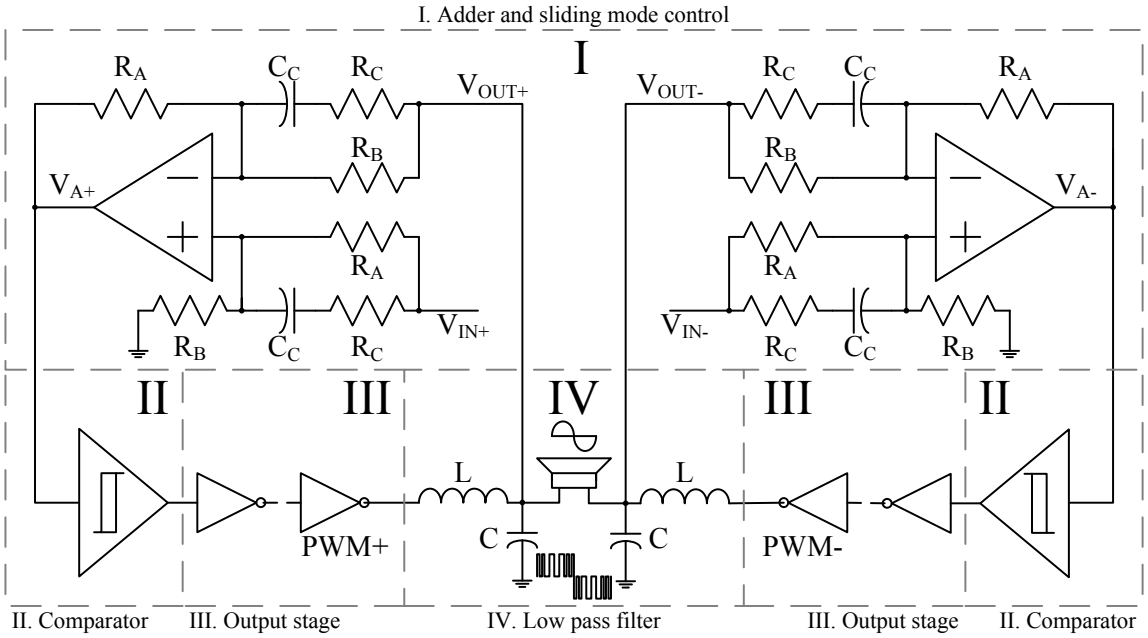


Fig. 67. Ternary modulation amplifier (TMA) architecture

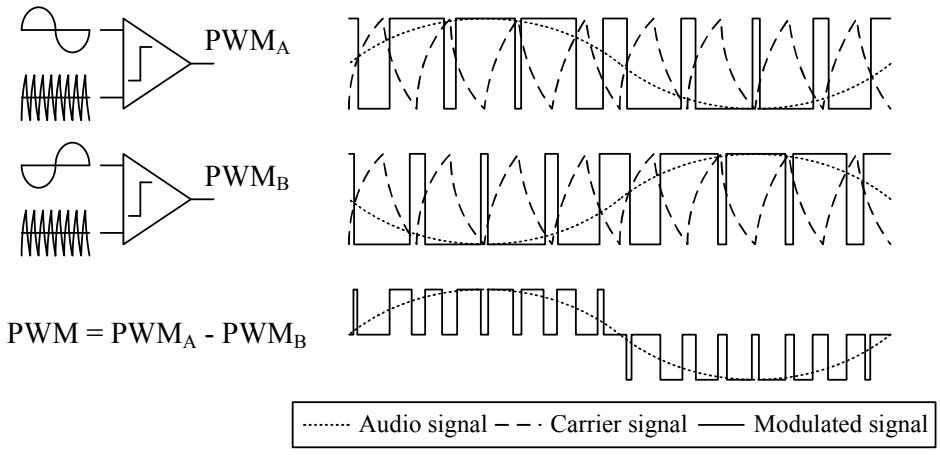


Fig. 68. Conventional ternary modulation scheme where the two top signals are single-ended waveforms whose difference is the bottom signal

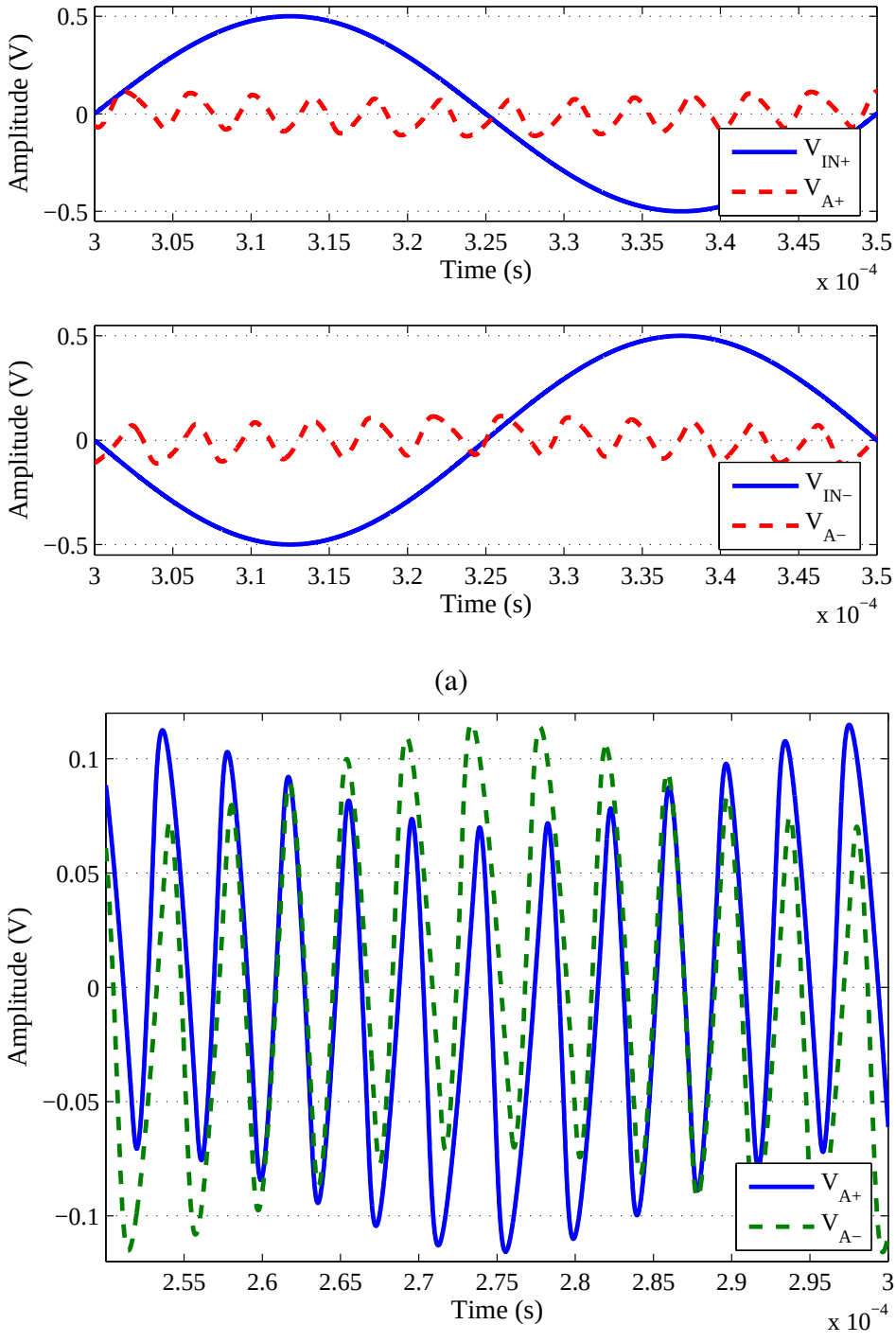
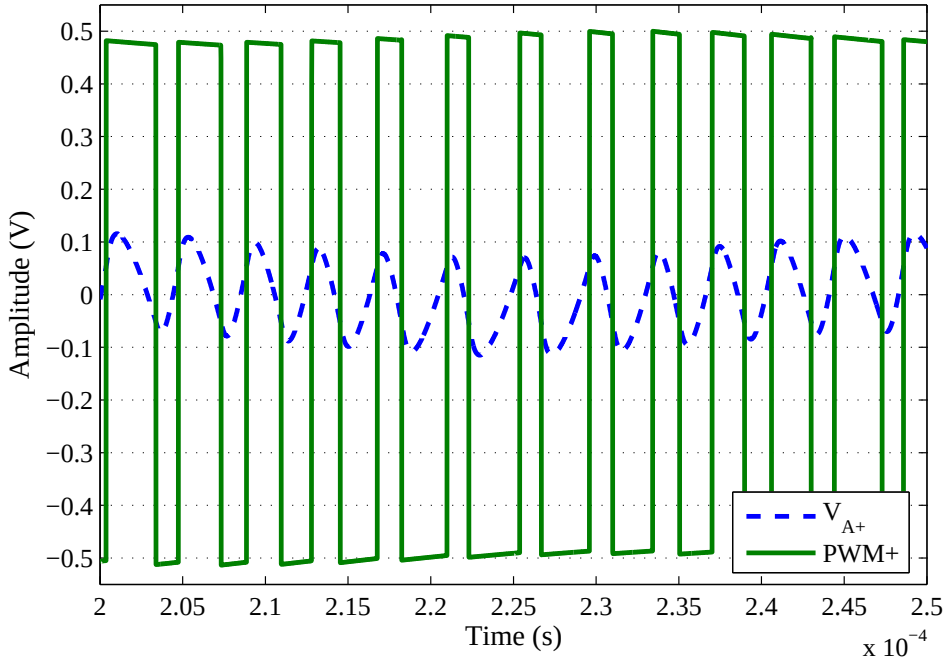
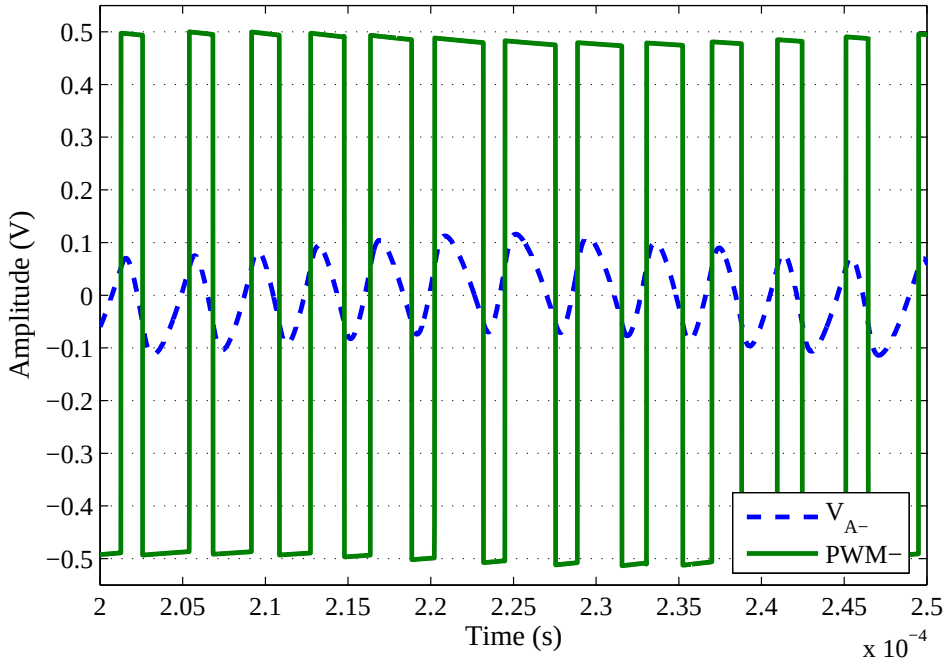


Fig. 69. Typical waveforms in the TMA (a) Input v_{IN} and output controller v_A and (b) Zoom in on complementary signal v_A

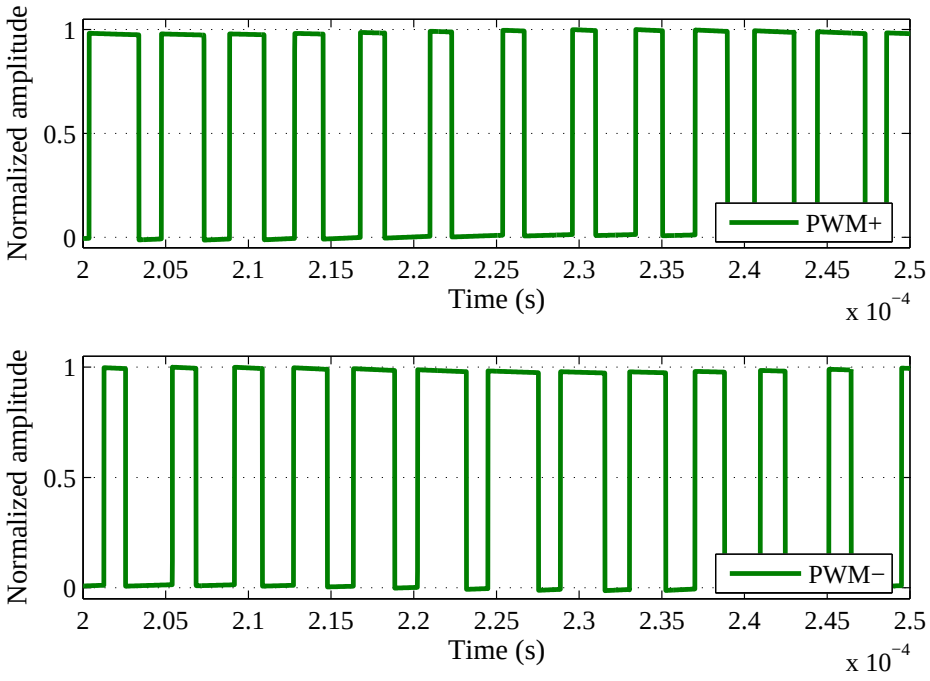


(a)

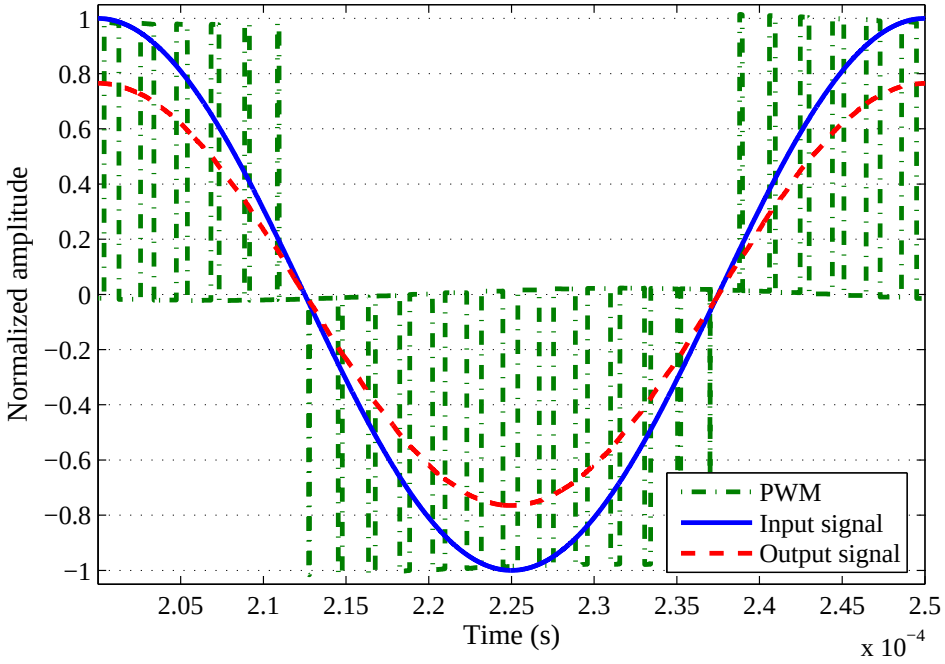


(b)

Fig. 70. Generation of the pulse-width modulation in the TMA when v_A exceeds hysteresis bound (a) Positive PWM+ and (b) Negative PWM-

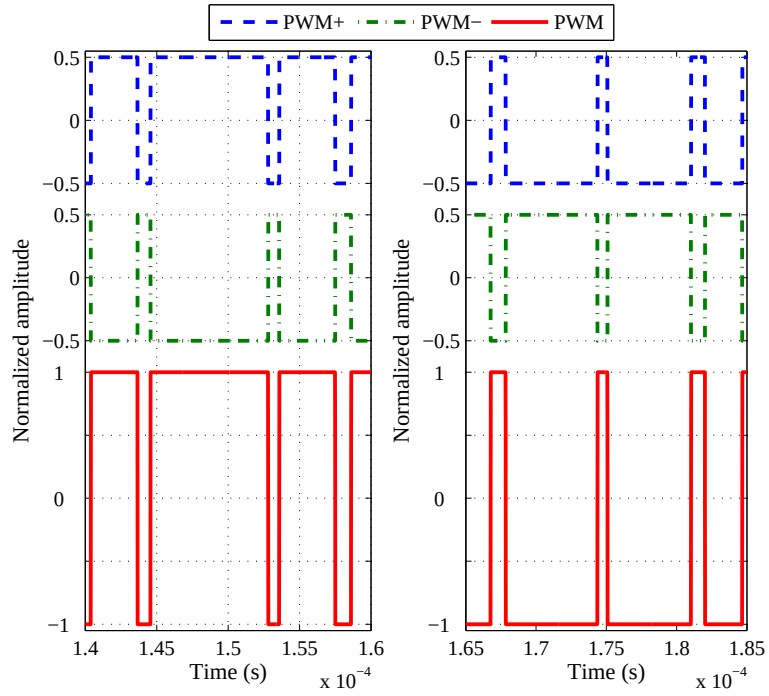


(a)

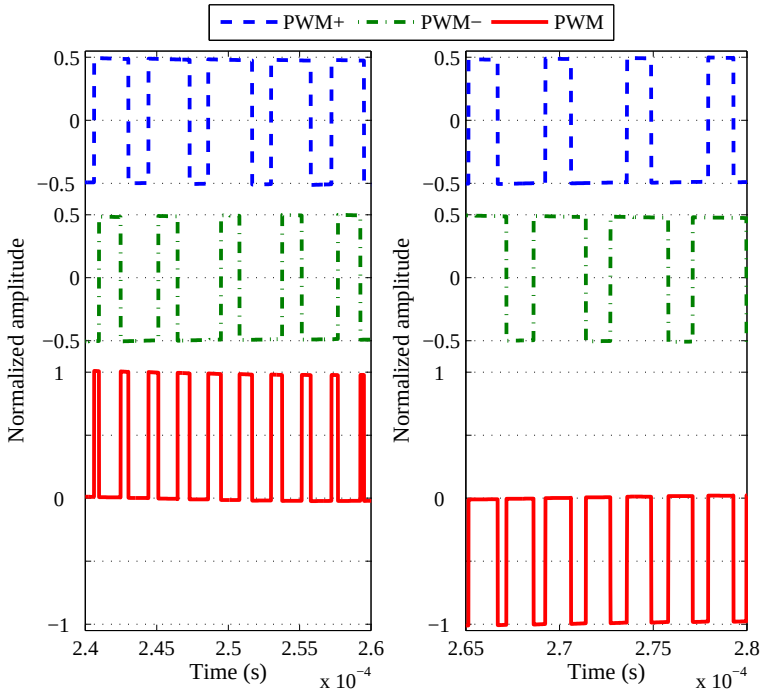


(b)

Fig. 71. Input and output signals in the TMA (a) Complementary pulse-width modulated signals and (b) Generation of third modulation level when PWM = (PWM+) - (PWM-)



(a)



(b)

Fig. 72. Comparison of pulse-width modulated signals in class D amplifiers (a) PWM generation for BMA and (b) PWM generation for TMA

Figure 69 shows a typical waveform v_A in the TMA. In contrast to the BMA, the wave v_A is out-of-phase but is not fully-differential. Figure 70 shows an example of the input/output signals of the comparator in the TMA where analog signal v_A is transformed into a binary signal, pulse-width modulated (PWM). Figure 71 illustrates typical TMA input/output signals. Note that the difference of the pulse-width modulated signals generates a wave with three levels, without any external reference carrier signal. Just as in the BMA case, the output signal is attenuated due to feedback factor β.

Figure 72 shows in detail the BMA/TMA pulse-width modulated signals. Since the BMA is a fully-differential system, then the differential pulse-width modulated signal in Fig. 72(a) is a binary signal. On the other hand, when the pulse-width modulated signals in the TMA are subtracted, as shown in Fig. 72(b), they generate a ternary signal. Observe that the ternary signal goes from 0 to 1 when the input signal is positive, and it goes from 0 to -1 when the input signal is negative.

The switching frequency of the class D audio power amplifiers BMA and TMA is directly related to the hysteresis band in the comparator because the system will toggle between states every time it reaches the hysteresis voltage. Figure 73 shows a magnified view of the ideal switching function $s(e_1, t)$ when it is operating under sliding mode.

The sliding mode operation can be divided into two different subintervals of operation Δt_1 and Δt_2. During the first subinterval of operation, the voltage v_A, defined in equation (4.9), increases until it reaches the hysteresis voltage κ and the pulse-width modulated signal (PWM) goes positive. In the second subinterval, the voltage v_A decreases until its value equals the negative hysteresis voltage $-\kappa$ and then, the pulse-width modulated signal (PWM) goes negative. This cycle repeats in a steady operation during sliding mode. The switching frequency ($f_{s,ideal}$) of the class D audio amplifier with an ideal sliding mode

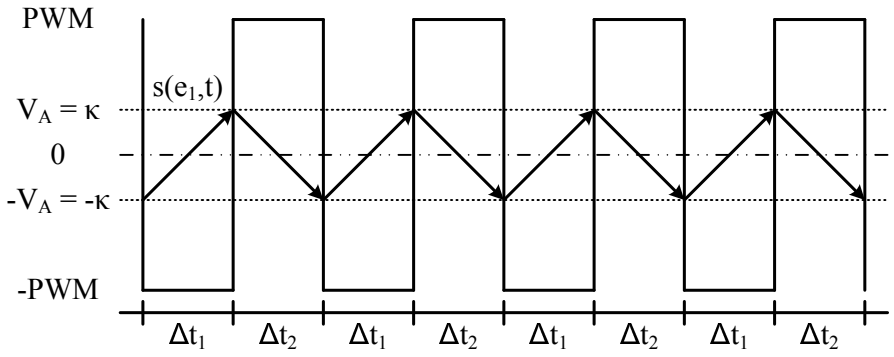


Fig. 73. Magnified view of ideal sliding mode operation for class D amplifiers

controller, as derived in Appendix C, is given by

$$f_{s,ideal} = \frac{1}{2\kappa}\frac{R}{L}v_C\left(1 - \frac{v_C}{v_{DD}}\right) \tag{4.12}$$

where R, L, κ, v_C, and v_{DD} are the speaker load, the output filter inductor, the hysteresis window, the filter capacitor voltage (output voltage), and the supply voltage, respectively.

However, the inclusion of the lossy-differentiator modifies the previous expression in equation (4.12) by reducing the switching frequency in an amount inversely proportional to the lossy-differentiator bandwidth, bounded by ω_p, as defined in equation (4.4). The effect of the lossy-differentiator on the sliding mode operation of the class D amplifiers BMA and TMA is illustrated in Fig. 74. As it can be appreciated, the pulse-width modulated signal (PWM) still toggles when the switching function $s(e_1, t)$ reaches the hysteresis voltage κ, but it exceeds the hysteresis boundary until it equates the voltage v_A. This effect is due to the lossy-differentiator pole which creates an exponential-shaped waveform instead of the triangular shape of the ideal switching function as shown in Fig. 73.

The value of the voltage v_A increases when the pole ω_p decreases, i.e. the switching function is very lossy, and it tends to the hysteresis voltage κ when the switching function

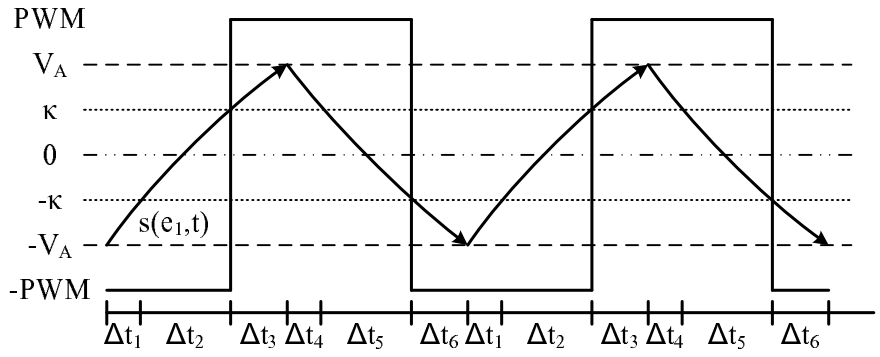


Fig. 74. Magnified view of real sliding mode operation for class D amplifiers

approaches to the ideal case. As a consequence of this, the time that takes to the switching function to recover and change direction is longer and consequently the switching frequency is lower when a lossy-differentiator is employed.

A complete cycle of the lossy sliding mode operation, as shown in Fig. 74, can now be divided into six different subintervals of operation. Subintervals Δt_1, Δt_3, Δt_4, and Δt_6 occur when the absolute value of $s(e_1, t)$ is higher than the hysteresis voltage κ. These subintervals are dominated by an exponential behavior. On the other hand, subintervals Δt_2 and Δt_5 take place when $|s(e_1, t)|$ is smaller than the hysteresis voltage κ. They resemble the two subintervals of operation in Fig. 73 because the slope of $s(e_1, t)$ within those subintervals can be considered constant. Therefore, the switching period, i.e. the inverse of the switching frequency, of the proposed class D audio power amplifiers, derived in Appendix C, can be expressed as

$$T_{s,real} \approx \frac{2\kappa V_{DD}\frac{R}{L}\left(1+\frac{1}{\gamma}\right)}{\left(\frac{R}{L}v_C+\frac{1}{2\gamma C}i_L\right)\left(V_{DD}\frac{R}{L}\left(1+\frac{1}{\gamma}\right)-\left(\frac{R}{L}v_C+\frac{1}{2\gamma C}i_L\right)\right)}$$

$$- \quad 4\frac{\alpha}{\gamma}\ln\left(\frac{v_H \; - \; \kappa}{\gamma e_1}\right) \tag{4.13}$$

where

$$v_H \; = \; e_1\gamma\exp\left(-k_t\right) \; + \; \kappa[1 \; - \; \exp\left(-k_t\right)] \tag{4.14}$$

$$k_t \; = \; -\frac{\gamma}{4\alpha\ln\left(0.01\right)}\left(\frac{1}{f_{s,ideal}}\right) \tag{4.15}$$

and R, L, κ, v_C, i_L, V_{DD}, v_H, $f_{s,\,ideal}$, and e_1, are the loudspeaker load, the filter inductance, the hysteresis window, the filter capacitor voltage, the filter inductor current, the voltage supply, the voltage difference between the voltage v_A and the hysteresis window κ, the minimum possible switching period of the amplifier under ideal sliding mode operation, i.e. the ideal switching frequency defined in equation (4.12), and the error voltage defined in equation (4.2). The factor α is the derivative coefficient in equation (4.1), and γ is the product of the pole in the lossy-differentiator ω_p and the derivative factor α, i.e. $\gamma = \alpha\omega_p$.

The first term in equation (4.13) represents the rising and falling time for subintervals Δt_2, and Δt_5 in Fig. 74. The second term in equation (4.13) takes into account the time taken by the four subintervals Δt_1, Δt_3, Δt_4, and Δt_6. Notice that when γ tends to infinite, i.e. the ideal switching function, the inverse of equation (4.13) simply becomes equation (4.12). The evaluation of equation (4.13) for different values of γ and hysteresis voltages is plotted in Fig. 75 along with simulated results. Observe that the analytical prediction matches very well the simulation data. Also, notice that the switching frequency increases when γ increases and the hysteresis voltage decreases. A transversal view of the same plot is shown in Fig. 76.

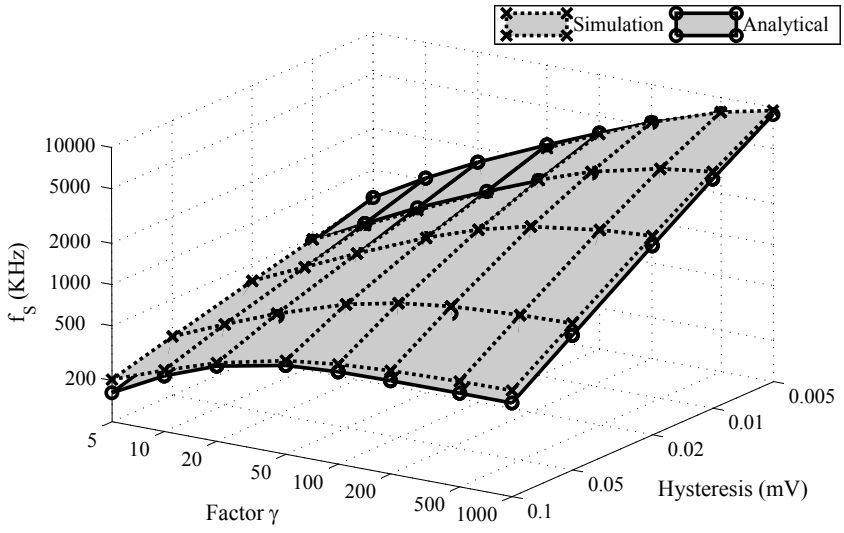


Fig. 75. Class D amplifier switching frequency versus lossy-differentiator factor γ and hysteresis-window width

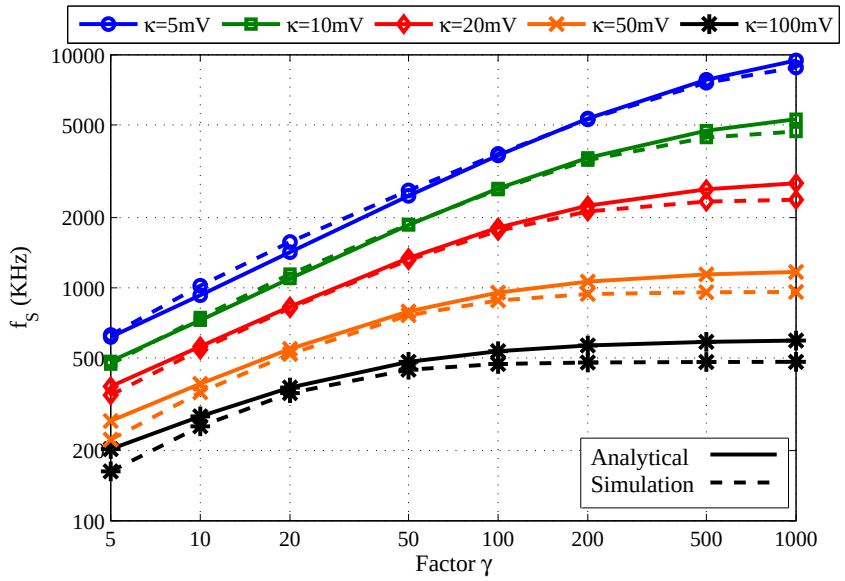


Fig. 76. Transversal view of class D amplifier switching frequency versus lossy-differentiator factor γ and hysteresis-window width

D. Design of Building Blocks

1. Lossy-Differentiator and Feedback Network

The blocks marked as I, II, III and IV in the BMA in Fig. 63, and the TMA in Fig. 67, are the sliding mode controller with feedback factor β, the comparator, the output power stage, and the low-pass filter, respectively. Both amplifiers are implemented with

$$\alpha \;=\; R_A \;\times\; C_C \tag{4.16}$$

where R_A = 300 kΩ, and C_C = 18.75 pF, based on a Bessel approximation [23]–[25], [57]. The lossy-differentiator has $R_C = 0.1 \times R_A$ to effect $\omega_p = 1 / R_C C_C = 10 / \alpha$ in equation (4.4). The factor $(1 + \beta)$ is given by

$$(1 \;+\; \beta) \;=\; \frac{R_A}{R_B} \tag{4.17}$$

We choose β = 0.4 (R_A / R_B = 1.4) for a reasonable compromise between linearity and output power. A simple design flow is listed in Table V.

Table V. Simple design flow given β, ω_p, and α

1. Choose C_C
2. $R_A = \alpha / C_C$
3. $R_B = R_A / (1 + \beta)$
4. $R_C = 1 / \omega_p C_C$

2. Operational Amplifier, Comparator, and Output Stage

The class D audio amplifiers requires the implementation of a fully-differential operational amplifier in the BMA, a single-ended operational amplifier in the TMA, comparators and an output power stage. Both operational amplifiers are based on a two-stage structure with Miller compensation scheme [47].

The fully-differential operational amplifier employed in the BMA is shown in Fig. 77 along with its common-mode feedback (CMFB) circuit. The detailed information of the transistor sizes is listed in Table VI. Additionally, the value of the bias current I_B is 12.5 μA, the compensation capacitor C_C is 1.2 pF, the compensation resistance R_C is 4 kΩ, and the common-mode resistor R_{CM} is 100 kΩ.

The schematic diagram of the single-ended operational amplifier used in the TMA is shown in Fig. 78, and Table VII summarizes the transistor sizes used in the single-ended operational amplifier. The operational amplifier is biased with a current I_B equal to 12.5 μA and it is compensated with a resistor R_C and a capacitor C_C with values 4 kΩ and 1.2 pF,

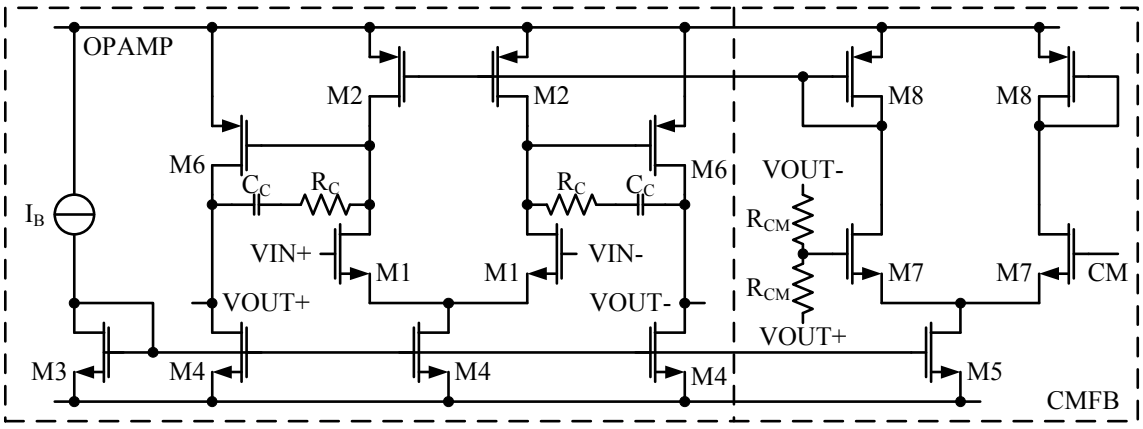


Fig. 77. Fully-differential operational amplifier schematic for BMA architecture

Table VI. Transistor sizes used in fully-differential operational amplifier for BMA

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	4.05	1.2	4
M2	5.55	1.2	8
M3	4.2	1.2	4
M4	4.2	1.2	16
M5	4.2	1.2	8
M6	6.15	1.2	16
M7	4.05	0.9	4
M8	5.55	1.2	4

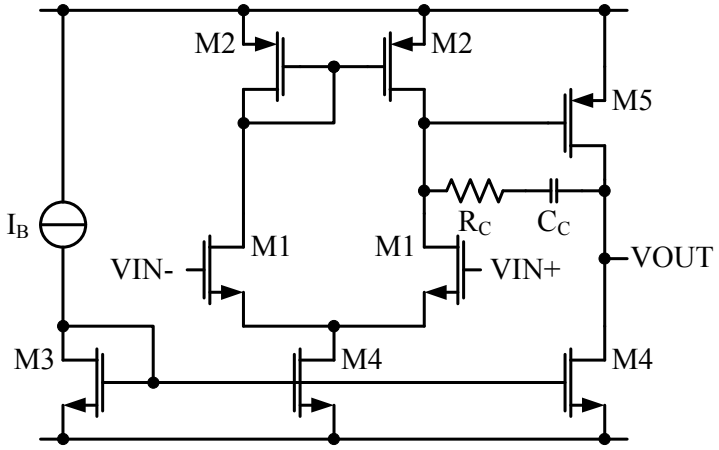


Fig. 78. Single-ended operational amplifier schematic for TMA architecture

Table VII. Transistor sizes used in single-ended operational amplifier for TMA

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	4.05	1.2	4
M2	5.55	1.2	8
M3	4.2	1.2	4
M4	4.2	1.2	16
M5	6.15	1.2	16

respectively.

The frequency response and power consumption characteristics of both, fully-differential and single-ended, operational amplifiers are specified in Table VIII.

Table VIII. Specifications of operational amplifiers in BMA and TMA architectures

Parameter	OPAMP (BMA)	OPAMP (TMA)
DC gain	66.85 dB	73.97 dB
GBW	28.49 MHz	26.19 MHz
Phase margin	74.54°	70.91°
I_Q	171.4 μA	193.6 μA
P_Q	462.7 μW	522.7 μW

The schematic diagram of the fully-differential comparator used for the BMA is shown in Fig. 79. The comparator consists of a preamplifier, a decision circuit with positive feedback, and a latch to hold the output value. It is biased with a current I_B of 12 μA and the values of width and length of its transistors are shown in Table IX.

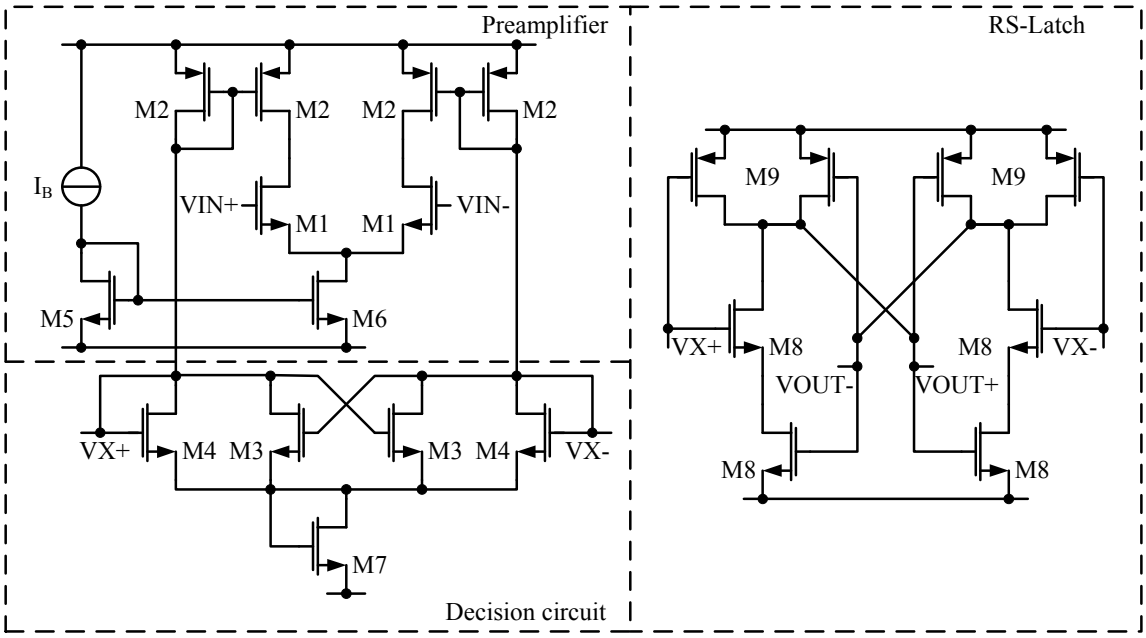


Fig. 79. Comparator schematic for BMA architecture

The schematic of the comparator used in the TMA architecture is illustrated in Fig. 80. It is constituted by a preamplifier differential pair and a decision circuit. The value of its bias current I_B is 3.25 μA. Notice that the power consumed by the comparator in the TMA architecture is less than the power consumed by the comparator in the BMA as discussed previously. Table X lists the transistor sizes used in the single-ended comparator for TMA

Table IX. Transistor sizes used in comparator for BMA architecture

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	10.05	1.95	8
M2	6	1.95	4
M3	2.7	1.95	8
M4	2.7	1.95	8
M5	4.05	1.8	4
M6	4.05	1.8	16
M7	16.05	0.6	24
M8	2.7	0.6	2
M9	8.4	0.6	2

architecture.

Both comparators utilize internal positive feedback [61], [62] and their hysteresis window [60] is set to make the class D amplifiers to switch approximately at 500 kHz. The comparators specifications, voltage hysteresis window, and power consumption, are listed in Table XI.

Additionally, the output power stage is optimized [44], [45] in order to maximize amplifier efficiency. The transistors size, tapering factor (T), and number of stages (N), are calculated considering the short-circuit current during transitions, switch on-resistance, and parasitic capacitances.

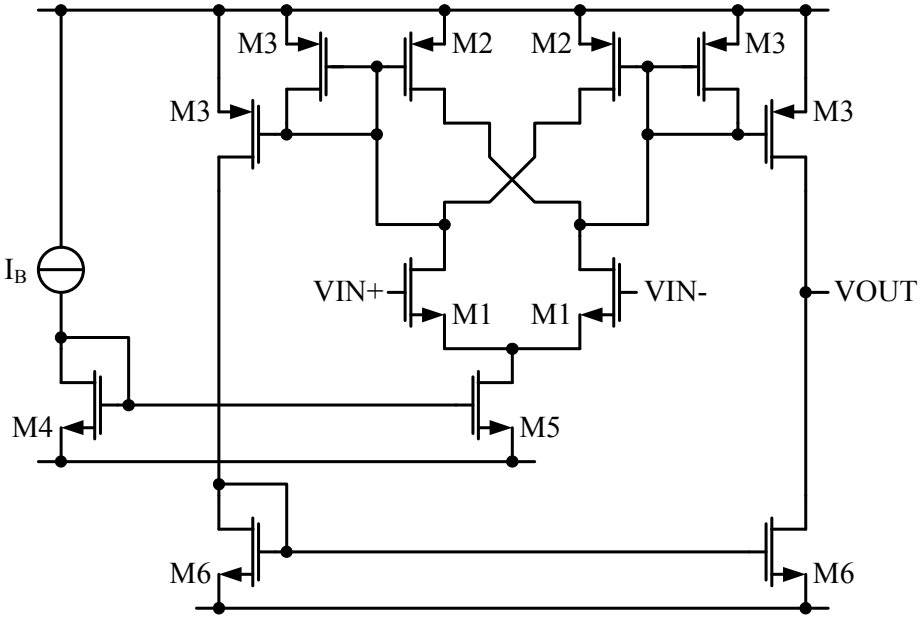


Fig. 80. Comparator schematic for TMA architecture

Table X. Transistor sizes used in comparator for TMA architecture

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	6.75	1.2	2
M2	4.65	1.2	4
M3	5.25	1.2	4
M4	11.55	1.2	4
M5	11.55	1.2	8
M6	2.7	1.2	2

Table XI. Specifications of comparators in BMA and TMA architectures

Parameter	Comparator (BMA)	Comparator (TMA)
Hysteresis voltage	10 mV	18 mV
I_Q	80.16 μA	21.22 μA
P_Q	216.4 μW	57.29 μW

Table XII summarizes the parameters of the output power stage, where W_P and L_P are the width and length of the last PMOS transistor in the buffer, respectively. Since the mobility ratio between PMOS and NMOS transistors is approximately three, it is possible to calculate the size of all the remaining transistors in the power stage from the data in the table.

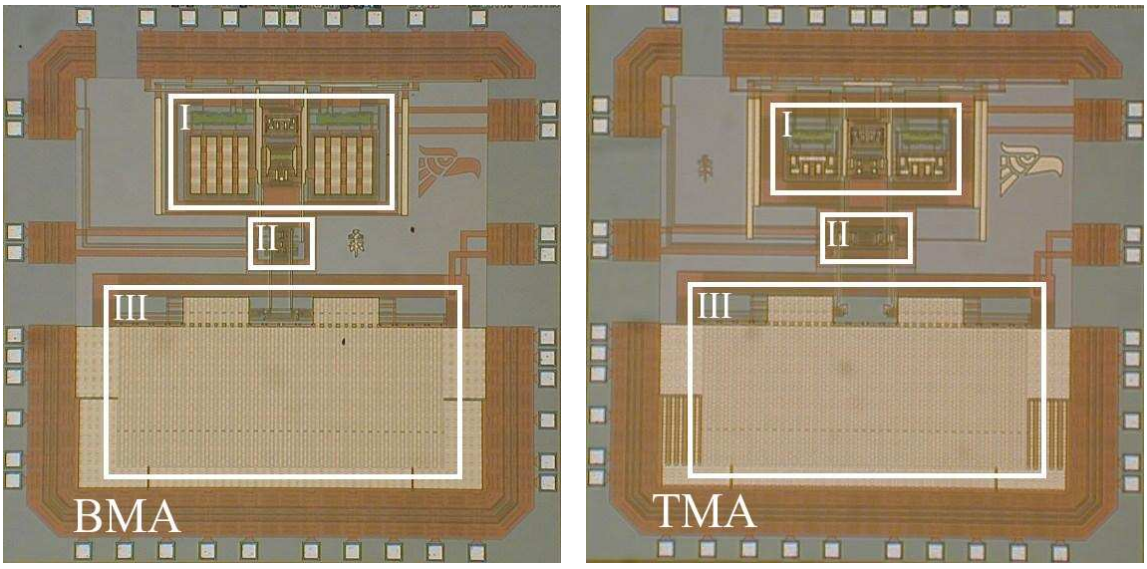
Table XII. Characteristics of the output power stage in BMA and TMA architectures

Parameter	Value
W_P	34560 μm
L_P	0.6 μm
T	14
N	4

The BMA consumes more quiescent power than the TMA because, from Fig. 60 and Fig. 61, the hysteresis-voltage window in the comparator must be smaller to achieve similar effective switching frequency and, consequently, similar linearity. However, because the TMA is not fully differential, it is more vulnerable to process variations and mismatches. The resulting design values are $\alpha \approx 5.625 \times 10^{-6}$, $\omega_p \approx 1.75 \times 10^6$ rad / s, $\omega_{3dB} \approx 125 \times 10^3$ rad / s, and $\beta = 0.4$.

E. Experimental Results

The BMA and the TMA were fabricated in MOSIS 0.5 μm CMOS AMI technology, and the circuits were tested with the System One Dual Domain Audio Precision equipment, using a 2.7 V voltage supply. Figure 81 shows the BMA and the TMA die micrographs



(a) (b)

Fig. 81. Die micrographs (a) Binary modulation amplifier (BMA) and (b) Ternary modulation amplifier (TMA)

where blocks I, II and III represent the sliding mode controller SMC, the comparator, and the power stage, respectively. The total area occupied by the class D audio amplifiers is approximately 1.49 mm^2 for the BMA, and 1.31 mm^2 for the TMA.

The class D amplifiers static power distribution is shown in Fig. 82. The comparator in the BMA consumes more power since it hysteresis window is smaller in order to achieve the same linearity as the TMA. Also, the area distribution of the class D amplifiers is presented in Fig. 83 where I, II and III represent the controller, the comparator and the output power stage of the BMA and the TMA, respectively. Notice that the power stage occupies the most area in both amplifiers while the comparator represents minimal area overhead.

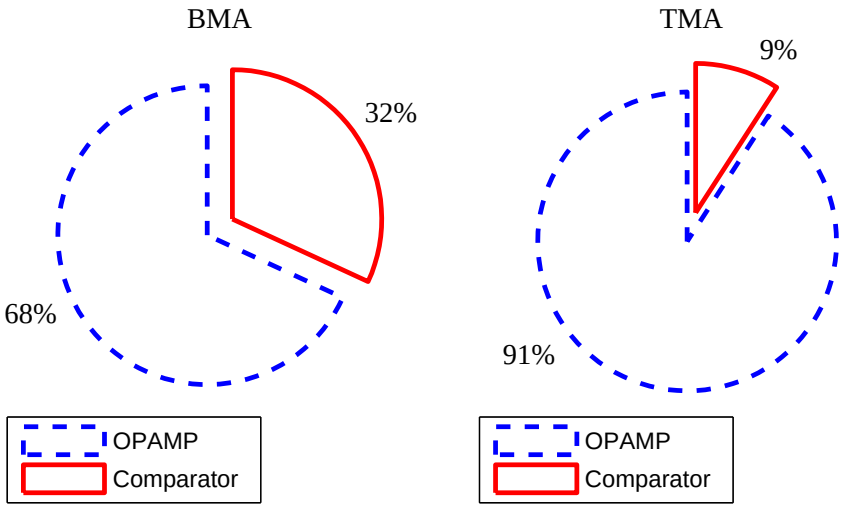


Fig. 82. Class D audio power amplifiers power distribution

The efficiency (η) performance of the class D audio power amplifiers, obtained with a sine wave input signal at 1 kHz, is shown in Fig. 84. The efficiency behavior of both

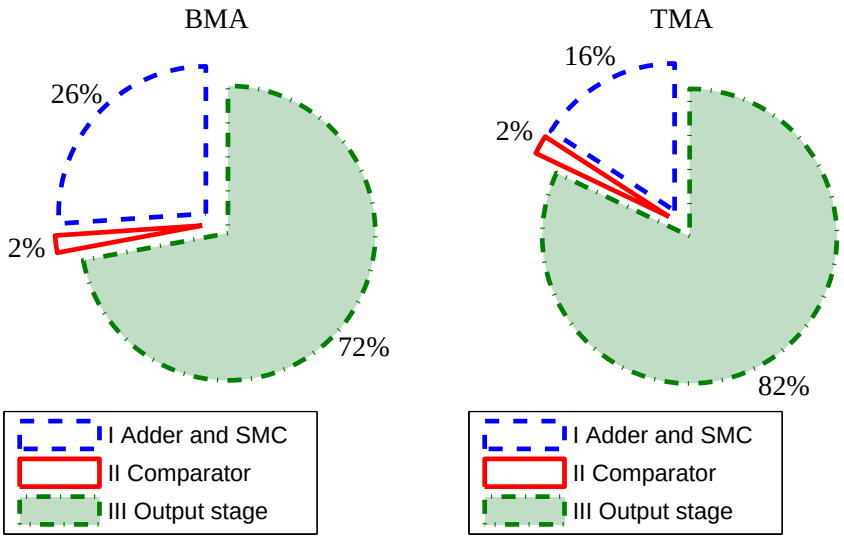


Fig. 83. Class D audio power amplifiers area distribution

amplifiers is comparable since the output stages are similar in both architectures. Figure 84 also illustrates the linearity of the amplifiers with a 1 kHz input signal. Notice that the TMA performance degrades at high output power due to its single-ended architecture.

As shown in Fig. 85, measured power-supply rejection ratio (PSRR) is above 75 dB at 217 Hz with a sine wave ripple of amplitude 100 mV on the power supply. Signal-to-noise ratio (SNR) greater than 90 dB was measured [8] for both class D amplifiers.

Figure 86 shows the typical BMA output waveforms. The output voltages $v_{OUT\pm}$ and the differential voltage v_{OUT}, when the input voltage is 750 mV at 1 kHz, are shown in Fig. 86(a). Similarly, the BMA pulse-width modulated waveforms for the same input signal are shown in Fig. 86(b). The TMA typical output waveforms are presented in Fig. 87. The output voltages, with an input voltage of approximately 2 V at 1 kHz, are shown in Fig. 87(a). Similarly, Fig. 87(b) illustrates the ternary modulation signal generation. The switching frequency of both class D audio power amplifiers is around 450 kHz.

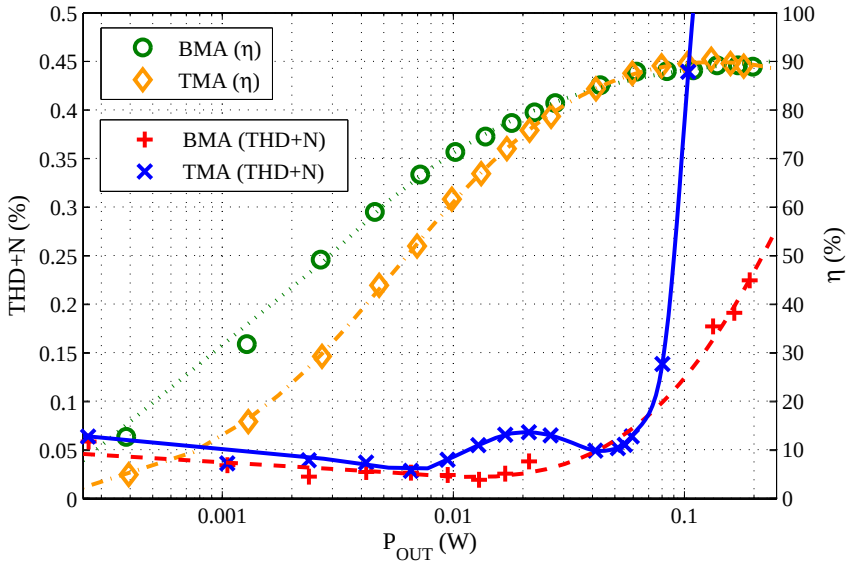


Fig. 84. Class D audio power amplifiers efficiency/THD+N versus output power

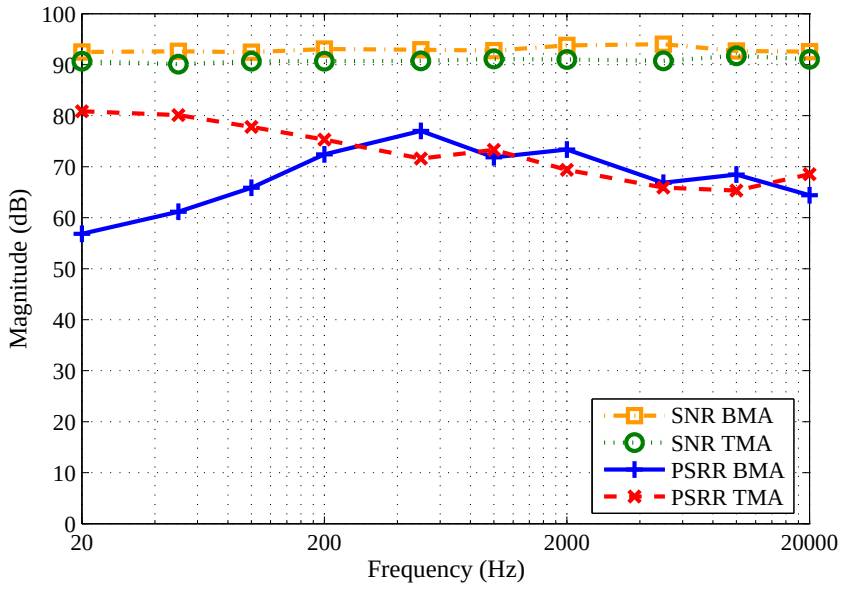
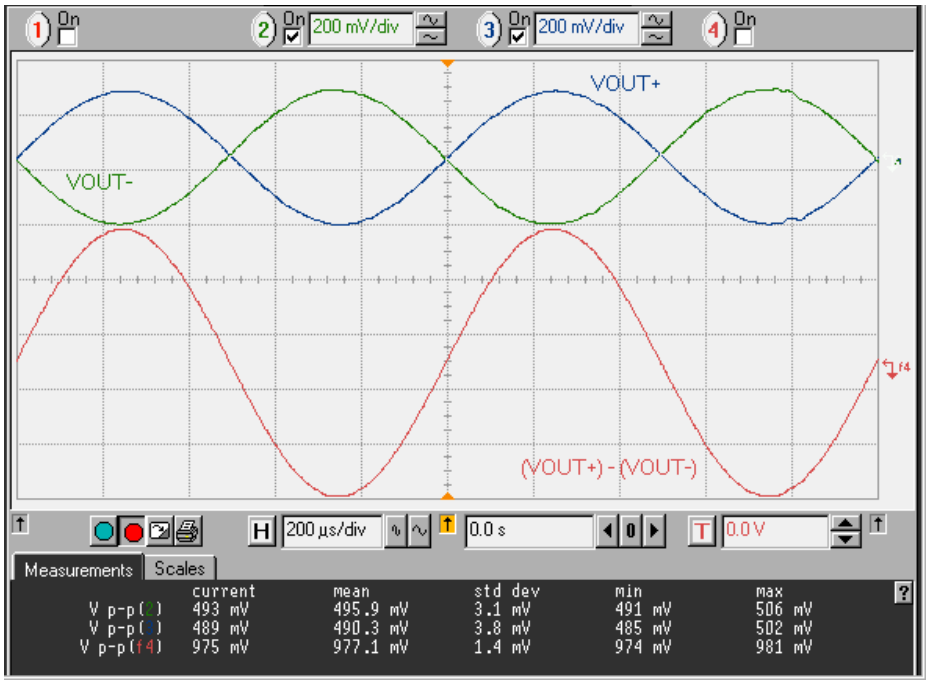
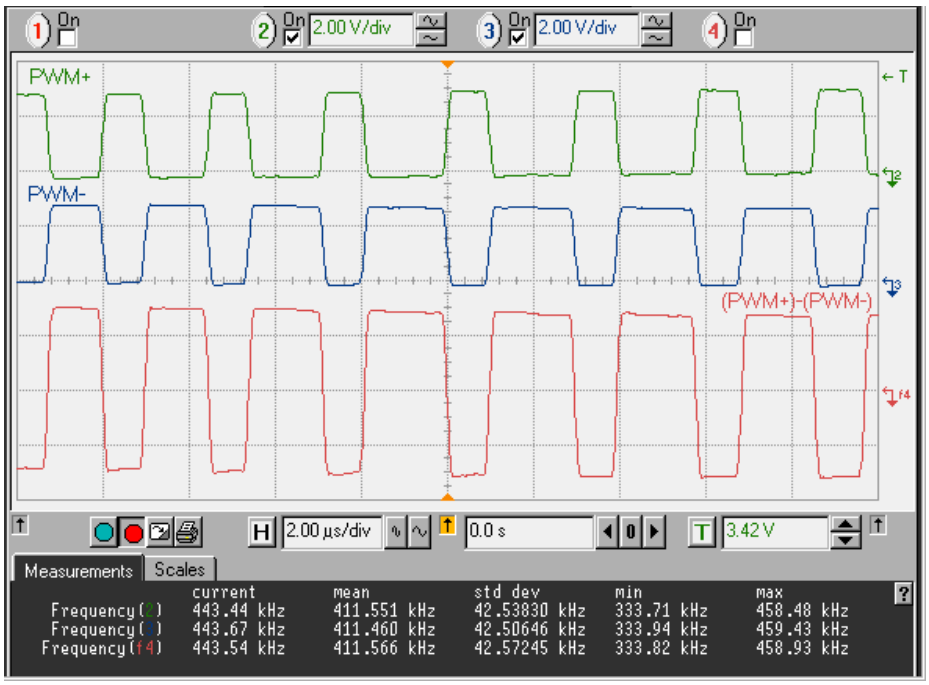


Fig. 85. CDAs SNR/PSRR versus frequency

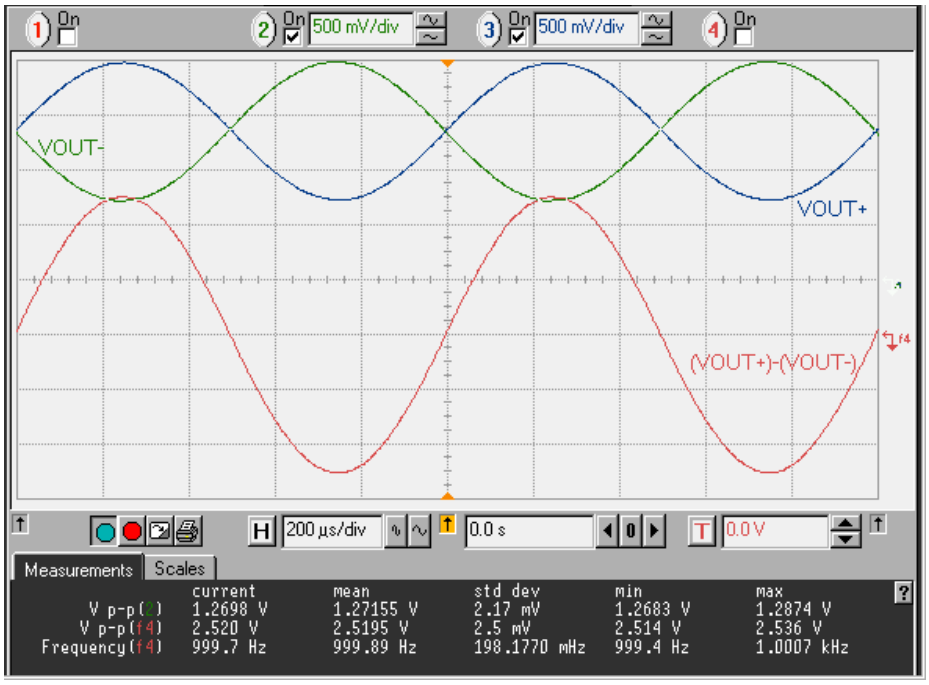


(a)

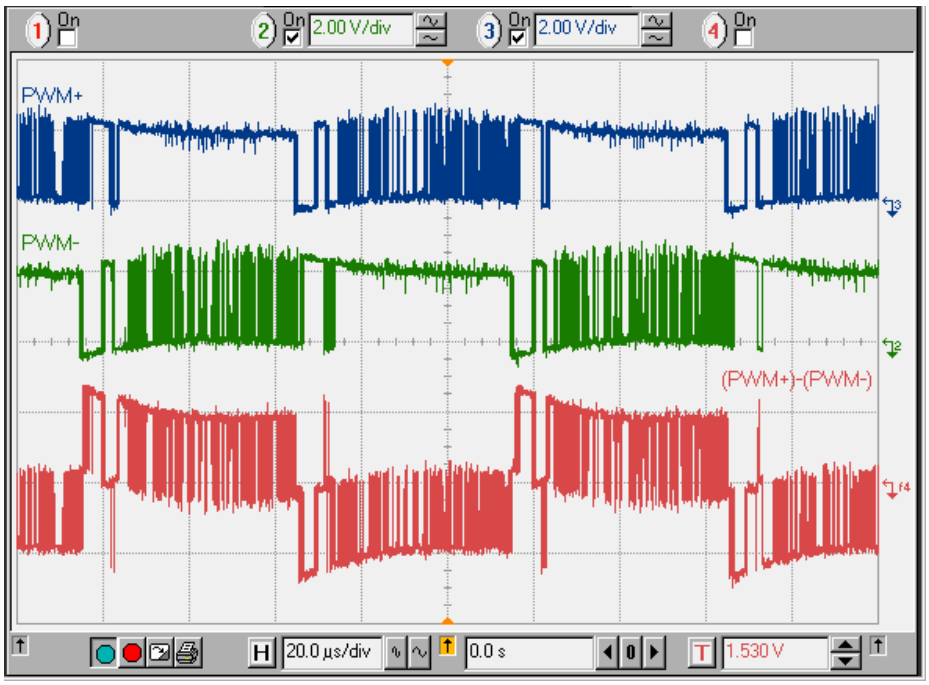


(b)

Fig. 86. BMA output waveforms (a) Audio output signal v_{OUT} and (b) Binary modulated signal

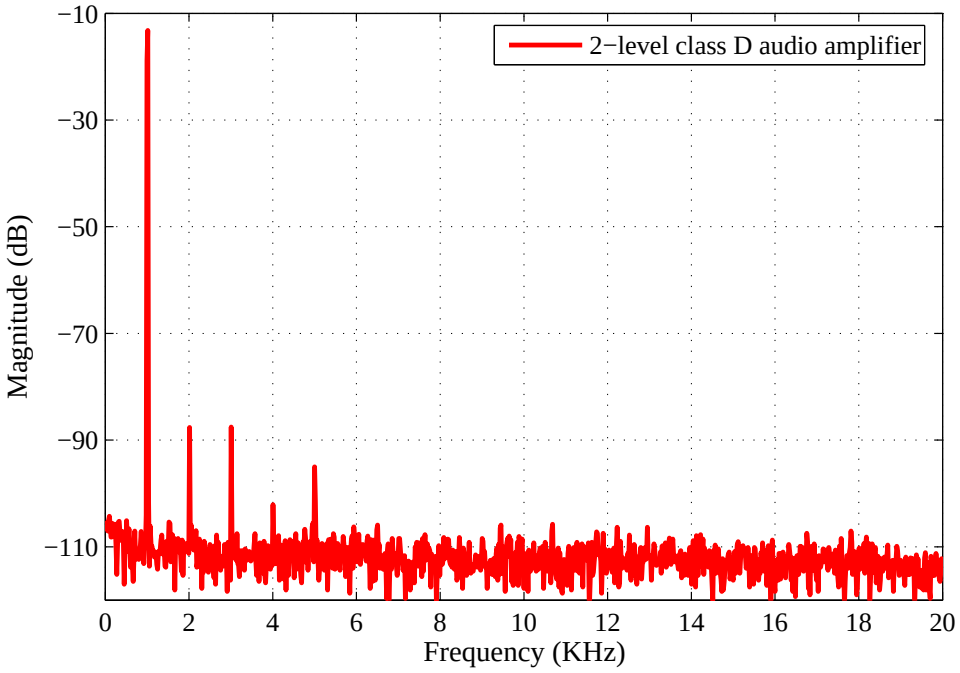


(a)

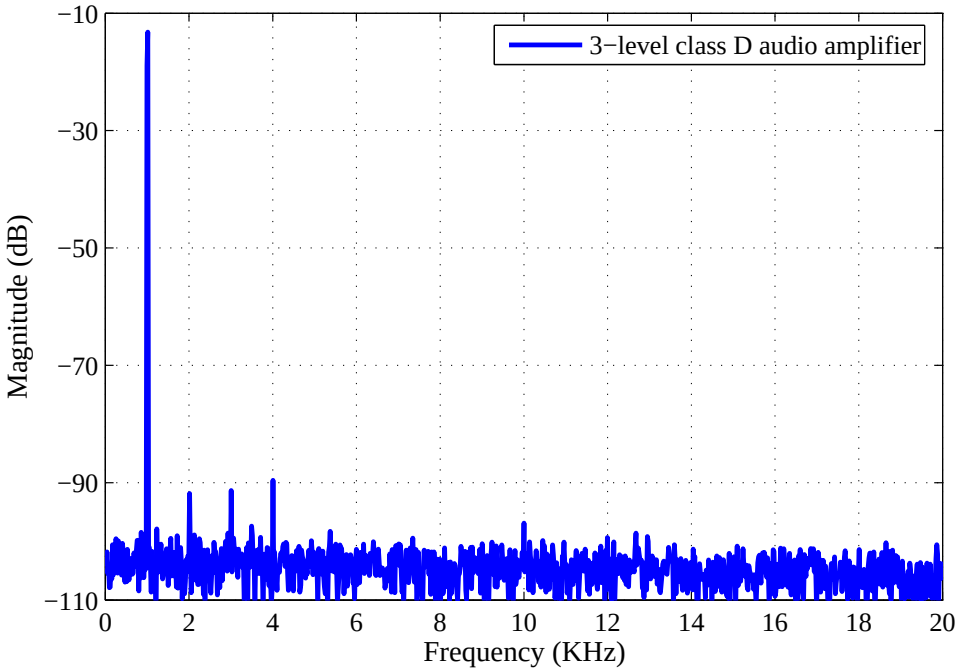


(b)

Fig. 87. TMA output waveforms (a) Audio output signal v_{OUT} and (b) Ternary modulated signal



(a)



(b)

Fig. 88. Class D audio power amplifiers output spectrums when v_{in} = 1 $V_{pk\text{-}pk}$ (a) BMA and (b) TMA

Figure 88 displays the output spectra of both class D audio power amplifiers with a 1 kHz 500 mV input voltage. Note that the harmonic components of the TMA are smaller than the BMA, but the noise floor is lower in the latter case, as expected from Fig. 85, because the signal-to-noise ratio (SNR) performance of the BMA is better than the TMA.

Table XIII compares the performance of the proposed class D audio power amplifiers to that of the state-of-the-art amplifiers where the figures of merit [24], [25] are defined as

$$FOM_1 = \frac{\eta}{I_Q \times THD \times 10^5} \tag{4.18}$$

$$FOM_2 = \frac{\eta \times P_{OUT,n}}{P_Q \times THD \times Area_n} \times 10^4 \tag{4.19}$$

where η, I_Q, P_Q, and THD represent the maximum power efficiency of the class D audio power amplifier, the static current consumption, the quiescent power consumption, and the minimum total harmonic distortion of the amplifier, respectively. Also

$$P_{OUT,n} = \frac{maximum\ output\ power}{maximum\ available\ power} \tag{4.20}$$

$$Area_n = \frac{total\ area}{unity\ size\ technology} \tag{4.21}$$

F. Conclusion

This chapter has presented the architecture, design, implementation, and measurement of two low-power class-D audio amplifiers with a hysteretic non-linear control. The prototypes have linearity, efficiency, signal-to-noise ratio (SNR), and power-supply rejection ratio (PSRR) performance comparable to the state-of-the-art works but consuming an order less of static power.

The amplifiers are fabricated in 0.5 μm CMOS technology, operate with a 2.7 V single voltage supply, and deliver a maximum output power of 250 mW. The area occupied by

Table XIII. Comparison of state-of-the-art class D audio power amplifiers

Design	[7]§	[8]	[9]	[13]†	[19]§	[24]	BMA	TMA
THD (%)	0.05	0.03	0.04	0.001	0.04	0.08	0.02	0.03
η (%)	85	76	79	88	80	91	89	90
Supply (V)	5.0	4.2	3.6	5.0	2.5	2.7	2.7	2.7
Load (Ω)	8	8	8	6	8	8	8	8
I_Q (mA)	4.00	4.70	2.50	10.00	2.90	2.00	0.25	0.21
P_Q (mW)	20.00	14.98	9.00	50.00	7.25	5.40	0.68	0.58
SNR (dB)	87	98	-	-	-	65	94	92
PSRR (dB)	74	70	84	67	75	70	77	81
f_s (KHz)	250	410	250	450	1800	500	450	450
P_{OUT} (mW)	1000	700	500	10000	350	200	250	250
Area (mm^2)	-	0.44	2.25	10.15	-	4.70	1.49	1.31
Levels	2	3	3	2	2	2	2	3
FOM_1	4	5	8	88	7	6	177	141
FOM_2	-	16	867	520	-	49	6020	5457
CMOS	-	90 nm	1.2 μm	0.6 μm	-	0.5 μm	0.5 μm	0.5 μm
Topology	PWM	PWM	PWM	$\Delta\Sigma$	$\Delta\Sigma$	SMC	SMC	SMC

§ Commercial products

† 12 V PVDD, 10 W design, special BCDMOS process

the designs is further reduced by employing a single operational amplifier to implement the hysteretic controller completely avoiding the highly linear triangle wave generator overhead in traditional architectures.

CHAPTER V

PRINCIPLES OF SWITCHING VOLTAGE REGULATORS

A. Introduction

The use of voltage regulators, in a given electronic system, is essential because the integrated circuits in the device require specifications based on a constant and stable voltage supply. Moreover, in most electronic appliances, several circuits with different voltage levels and current rates exist. Therefore, in order to supply these circuits with different voltages, currents, and power ratings, several voltage converters are necessary. Such voltage converters must provide good output regulation, high efficiency performance, and fast transient response [63], [64].

The power delivered by a voltage converter changes dramatically for different applications. For example, in low-power battery-based portable applications, the power demanded by a load is typically in the order of a few watts. Power supplies for computers and office equipment may supply hundreds of watts. However, the power levels found in rectifiers and inverters, that interface DC transmission lines to an AC utility system, can be as high as thousands of megawatts [63].

This chapter presents the basic fundamentals of low-power voltage supplies, their main topologies and principles of operation, and it is organized as follows. Section B describes the different low-voltage power supplies, their characteristics and their global market distribution. Section C outlines the fundamentals of power electronics, as well as their basic circuit architectures. It also describes the main control schemes used in switching voltage regulators. Section D sketches the typical measurement setup for switching voltage regulators. Finally, Section E summarizes some practical design considerations for implementing and testing switching voltage converters.

B. Low-Voltage Power Supplies

Power supplies are used in most electrical equipment. Their field of applications go from consumer appliances to industrial utilities, ranging from milliwatts to megawatts, and from hand-held tools to satellite communications. A power supply is the device that converts the output from a given power line to a steady output voltage, or multiple output voltages. The output voltage is regulated to produce a constant level despite the variations in the input line or the circuit loading [65]. In general, a power converter circuit, as shown in Fig. 89, consists of an input and output power lines, a controller, which generate a control input to drive a pass element (a solid-state device such as transistor), a feedback and/or feedforward loop, and a reference voltage [65], [66].

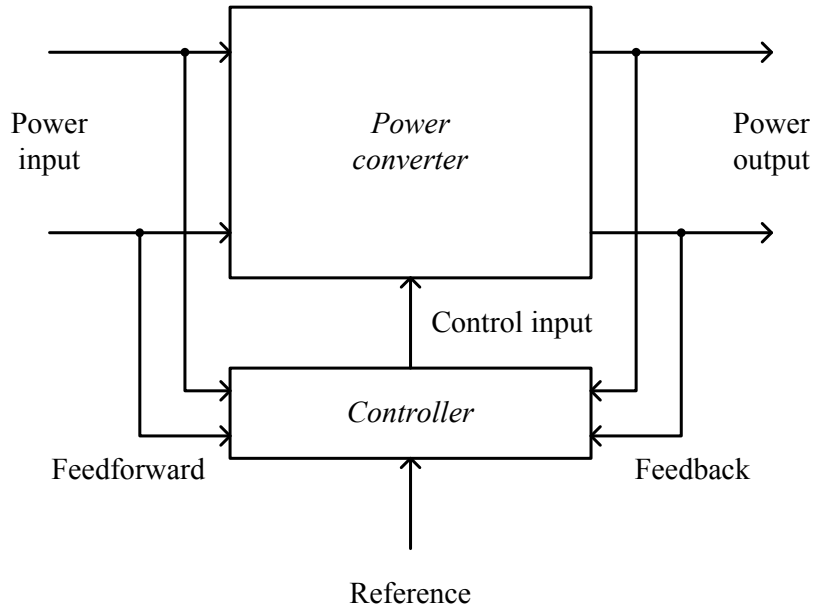


Fig. 89. Typical block architecture in a power converter circuit

The regulation is done by sensing the variations appearing at the output/input of the power converter. This variations are feeding back/forward to the controller circuit. The controller produces a control signal to minimize the error between the reference voltage and the output voltage. As a result, the output voltage of the power converter is maintained essentially constant [65]. If the pass element, i.e. the transistor, is operated at any point in its active region, the regulator is referred to as *linear voltage regulator*. On the other hand, if the pass element operates only at cutoff and saturation, the circuit is referred to as *switching voltage regulator*. Furthermore, the switching voltage regulators can be subdivided into circuits based on capacitors and circuits based on inductors as switching-capacitor voltage regulators and switching-inductor voltage regulators, respectively [63]–[65], [67], [68].

1. Linear Voltage Regulators

Linear voltage regulators, conceptually illustrated in Fig. 90(a), operate on the principle of resistive voltage division. They are popular because their structure is simple and their area is small [63]. They are used to generate an output voltage with a lower magnitude and the same polarity as compared to the input voltage. Voltage linear regulators have intrinsically low efficiency, particularly if the input-to-output voltage conversion ratio is high. A linear regulator can be efficient only in applications that require an output voltage just slightly below the input voltage [63], [64], [67], [68].

Linear voltage regulators should maintain the output voltage within certain limits under variations of the load current and input supply voltage. A general block diagram of a simple linear regulator with feedback circuitry for output regulation is shown in Fig. 90(b). A feedback circuit varies the gate voltage of a series transistor (which behaves as a variable resistor) by comparing the output voltage v_{OUT} to a reference voltage v_{REF} [63], [68].

There are three basic types of linear regulators: standard linear regulator, low-dropout (LDO) linear regulator, and quasi-low-dropout linear regulator [67]. The dropout voltage

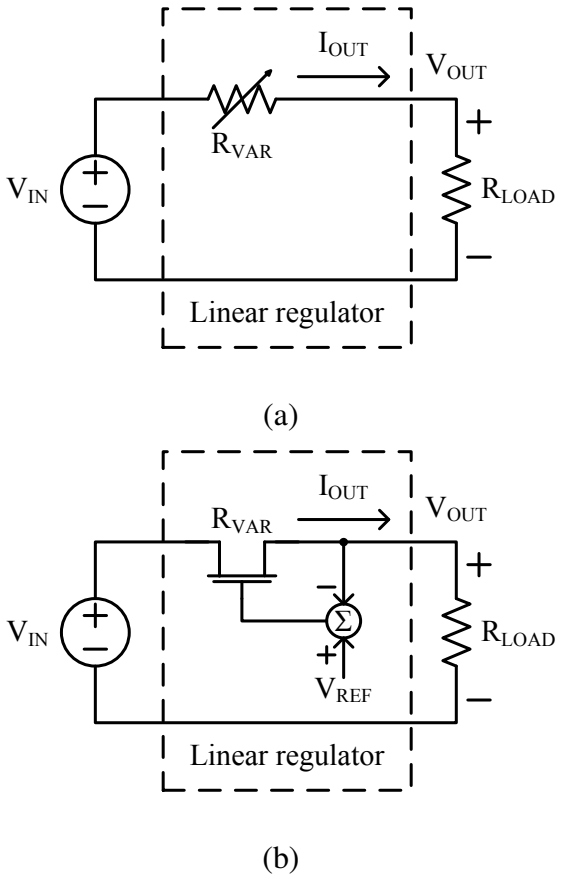


Fig. 90. Linear voltage regulator (a) Conceptual diagram and (b) General block diagram

is defined as the minimum voltage difference between the input voltage and the output voltage to maintain regulation. If the input voltage of a linear regulator drops below a certain threshold, the regulation is lost, and the output voltage will sag below the nominal regulation point. A critical point to be considered is that, the linear regulator that operates with the smallest voltage across it, dissipates the least internal power and has the highest efficiency. The most important difference between these three basic types of linear regulators is their dropout voltage, the low-dropout regulator requires the least voltage across it, while the standard regulator requires the most [64], [67].

Standard linear regulators typically employ Darlington transistors for the pass device. The standard voltage regulator is usually best for AC-powered applications, where the low-cost and high load current make it the ideal choice. The low-dropout linear regulator differs from the standard linear regulator because the pass device of the regulator is made up of only one single transistor. The dropout voltage is directly related to load current, which means that at very low values of load current the dropout voltage is minimum. The lower dropout voltage is the reason low-dropout regulators dominate battery-powered applications, since they maximize the utilization of the available input voltage and can operate with higher efficiency. The explosive growth of battery-powered consumer products in recent years has driven development in the low-dropout regulator product line. Lastly, a variation of the standard linear regulator is the quasi-low-dropout linear regulator, which uses complementary transistors in a Darlington structure as the pass device. The dropout voltage for the quasi-low-dropout regulator is higher than the low-dropout regulator, but lower than the standard regulator [67].

2. Switching-Capacitor Voltage Regulators

Switching-capacitor voltage regulators, also called charge pumps, are used in integrated-circuits (ICs) to modify the amplitude and/or polarity of the input voltage supply of a system. Similar to the linear regulator, the efficiency of a switched-capacitor regulator is typically low and the silicon area occupied is larger when compared to a linear regulator. However, unlike linear regulators, charge pumps can change the polarity and increase the amplitude of an input voltage supply. On-chip switched-capacitor voltage regulators are used to supply power to non-volatile memory circuits, dynamic random access memories (DRAMs), and some analog portions of mixed-signal circuits [63], [64], [68].

A simplified schematic representation of a switched-capacitor voltage regulator is shown in Fig. 91. This circuit provides an output voltage v_{OUT} twice the value of the

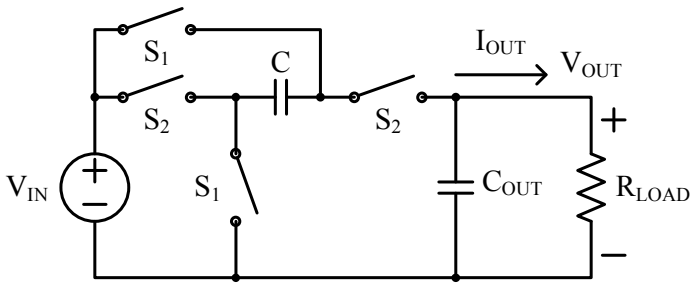


Fig. 91. Simplified representation of a switched-capacitor voltage doubler

input voltage v_{IN} and it operates as follows. Switches S_1 are controlled by the phase one control signal while switches S_2 are controlled by the phase two control signal. Both phases do not overlap. In phase one, the switches S_1 are turned on and switches S_2 are turned off, then capacitor C_1 is charged to v_{IN}. At this phase, the output current is supplied by the output capacitor C_{OUT}. When capacitor C_1 is fully charged, switches S_1 are turned off and switches S_2 are turned on. Therefore, the output capacitor C_{OUT} is charged to twice the value of the input voltage v_{IN}. In practice, though, the value of the output voltage v_{OUT} is less than $2v_{IN}$ due to the voltage drop across the series resistance of the MOSFET switches (on-resistance). Moreover, in an actual implementation, the output voltage degrades when the load current increases [63]. Charge-pumps can produce any rational conversion ratio if more complex configurations are used [64].

The main limitation of switched-capacitor converters is that they can efficiently convert voltages, but they cannot regulate these converted voltages any more efficiently than a linear regulator because the ratios of the elements in the circuit are fixed. Therefore, their most efficient application is limited to situations in which a voltage must be converted to another rationally related voltage but regulation is not necessary. Moreover, the efficiency of a charge-pump converter is limited because their power losses are typically high. This

losses are related to the switch on-resistance and to the parasitic capacitances, in on-chip capacitors implementations [63], [64].

3. Switching-Inductor Voltage Regulators

Switching-inductor voltage regulators are capable of modifying the amplitude and polarity of the input voltages. They can provide high power conversion efficiency and good output voltage regulation, however, their primary drawback is the use of inductive elements (inductors and/or transformers) required for energy storage and filtering. Therefore, filter inductors are, to date, prohibitive in the fabrication of commercial monolithic switching-inductor voltage converters [63].

One of the advantages of switching-inductor voltage regulators is that they can provide the highest power rating with the maximum efficiency, and still provide good voltage regulation. In general, the switching-inductor voltage regulator operates as a closed-loop system in order to compensate the disturbances coming from the input voltage and the load variations. A typical switching-inductor voltage regulator is shown in Fig. 92. It is a step-

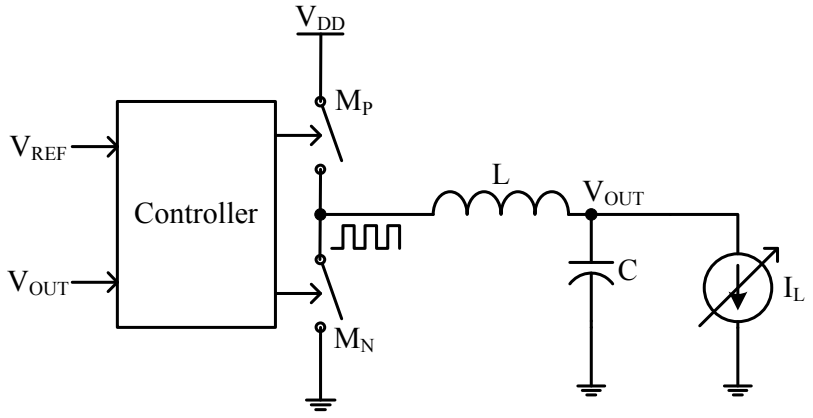


Fig. 92. Simplified diagram of a step-down switched-inductor voltage regulator

down voltage converter, also called buck converter, which generates an output voltage level v_{OUT} smaller than the input voltage v_{DD} [63]–[68].

Notice that the output voltage v_{OUT} in the buck converter is fed back to the controller, where is compared to the reference voltage v_{REF}. Then, the controller generates the logic necessary to operate the switches M_P and M_N, at a given switching frequency f_s. Hence, a digital signal, pulse-width modulated (PWM), is generated by turning on and off these switches. The duty cycle of the pulse width modulated signal represent the targeted output voltage. This digital signal is averaged with the second-order low-pass filter built with the ideally lossless elements, the inductor L and the capacitor C [63]–[68].

Consequently, the choice of a given voltage regulator will depend on the specific application and requirements given to the designer. The three different converters have advantages and disadvantages over the others, hence the appropriate regulator in a particular design is significantly based on the cost and performance of the regulator itself. The main characteristics of the three differen types of low-voltage power supplies are summarized in Table XIV where the best properties of each voltage regulator are highlighted.

4. Low-Voltage Power Supplies Global Market Distribution

Analog power management is now one of the fastest growing markets in the semiconductor industry, due to the greater demand for power management in portable electronics. The analog power IC market includes linear regulators, switching regulators, and other analog ICs like voltage references and battery management circuits. This market is growing at a compound annual growth rate of 10% each year, although some product categories are growing at a much faster rate as demand for DC-DC power converters, low dropout voltage regulators, and battery management continues to climb [69]–[74].

The analog power IC revenue was $5.5 billion in 2004 and it is expected to rise to

Table XIV. Main characteristics of low-voltage power supplies

Parameter	Linear	Switched-capacitor	Switched-inductor
Efficiency	Low	Low	**High**
Current rate	Low	Low	**High**
Area	**Small**	Medium	Large
Output voltage polarity	Same	**Different**	**Different**
Voltage conversion	Down	**Up/down**	**Up/down**
Voltage regulation	**Good**	Poor	**Good**
Noise	**Low**	Medium	High

$12 billion in 2010. The distribution of the analog power IC market in 2004, as shown in Fig. 93, was equally distributed between linear regulators and switching regulators, but the

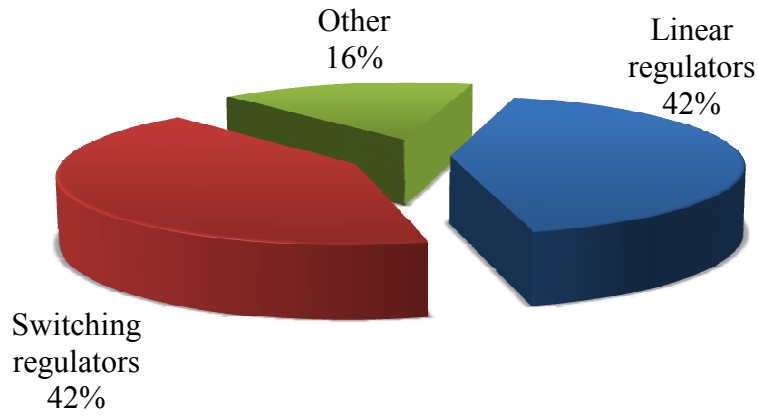


Fig. 93. Analog power IC revenue distribution in 2004

projected analog power IC market distribution for 2010, illustrated in Fig. 94, estimates that more than 50% of the market will be dominated by the switching voltage converters [70].

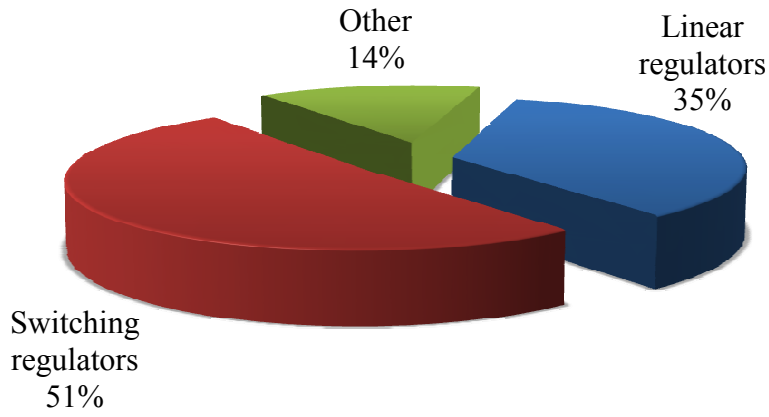


Fig. 94. Analog power IC projected revenue distribution for 2010

The analog power IC market is expected to grow by 22% in 2009, and unit shipments of analog power ICs constitute already over 50% of total standard analog ICs shipments. Unit shipments are expected to grow from about 120 billion units today, to more than 200 billion units by 2013 [69], [73].

Currently, there are more than twenty analog power IC manufacturers [69]–[73], where the most representative companies are STMicroelectronics, Fairchild Semiconductor, Toshiba, Infineon, Texas Instruments, International Rectifier, Linear Technology, ON Semiconductor, Maxim Integrated Products, Microsemi, Intersil, Analog Devices, etc.

C. Fundamentals of Power Electronics

Power electronics involves the study of electronic circuits intended to control the flow of electrical power. These circuits handle power flow at levels much higher than the individual device ratings. The most familiar examples of circuits with this description are AC-DC converters (inverters or rectifiers), DC-DC converters (switching-inductor voltage regulators), and AC-AC converters (cycloconverters). The key element is the switching converter. In general, a switching converter contains power input and control input ports, and a power output port. Power electronics represents an intermediate point where the fields of power and energy systems, electronics and devices, and systems and control converge and combine [65], [66].

A power electronic circuit consists of an energy source, an electrical load, a power electronic circuit, and a controller. The control circuit take information from the source and load, and then determines how the switches operate to achieve the desired conversion. The controller is built using analog circuits and digital electronics. The power electronic circuit contains switches, lossless energy storage elements (inductors and capacitors), and magnetic transformers. Ideally, when a switch is on, it has zero voltage drop and will carry any current imposed on it. When a switch is off, it blocks the flow of current regardless of the voltage across it. Therefore, the switch controls energy flow with no loss. Hence, if the energy storage elements are also lossless, the ideal efficiency of a power electronic circuit is 100% [65], [66].

In the past, bulky linear converters were designed with transformers and rectifiers to provide low-level DC voltages for electronic circuits. In the late 1960s, the use of DC sources in aerospace applications led to the development of power electronic DC-DC conversion circuits for power supplies. Today, in a typical power electronic arrangement an AC source from a wall outlet is rectified, and the resulting high DC voltage is converted,

through a DC-DC converter, to the low-voltage levels required in the electronic device. These switched-mode power supplies are rapidly supplanting linear regulators in all circuit applications because their simplicity and higher efficiency. Nowadays applications of power electronics include automotive and telecommunications industries, as well as markets focused on portable equipment [65].

1. Introduction to DC-DC Voltage Regulators

The DC-DC voltage regulators (switching-inductor voltage regulators) convert a DC input voltage v_{IN} into a DC output voltage v_{OUT} and provide regulation against load and line variations. The power levels found in switching converters range from less than one watt (in battery-operated portable equipment), to tens, hundreds, or thousands of watts (in power supplies for computers and office equipment), to millions of watts (in motor drivers). DC-DC down converters can be found, for example, in DC drive systems, like electric vehicles, electric traction, and machine tools, and in power supplies for electronic circuits (e.g. microprocessors). DC-DC step-up converters are used in radar and ignition systems. Another major area of applications of DC-DC converters is related to the utility AC grid. For example, if the utility grid fails, there must be a backup source of energy, like a battery pack or uninterruptible power supplies (UPSs). Moreover, DC-DC converters are also used in dedicated battery charges [65], [66].

The three basic architectures in DC-DC converters, which are outlined in this section, are the buck converter (step-down converter), the boost converter (step-up converter), and the buck-boost converter (step-up-down converter) [65]–[68].

a. Buck Voltage Regulator

The most commonly used switching converter is the buck convert, which is used to down-convert a DC voltage to a lower DC voltage of the same polarity. This conversion is

essential in systems that use distributed power rails, which must be locally converted to low-voltage supplies with very little power loss [67]. A basic schematic representation of a buck converter is shown in Fig. 95. It consists of a DC input voltage V_{IN}, two controlled switches S_1 and S_2, along with a controller to operate them properly, a filter inductor L, a filter capacitor C, and the load resistance R_{LOAD} [63]–[68].

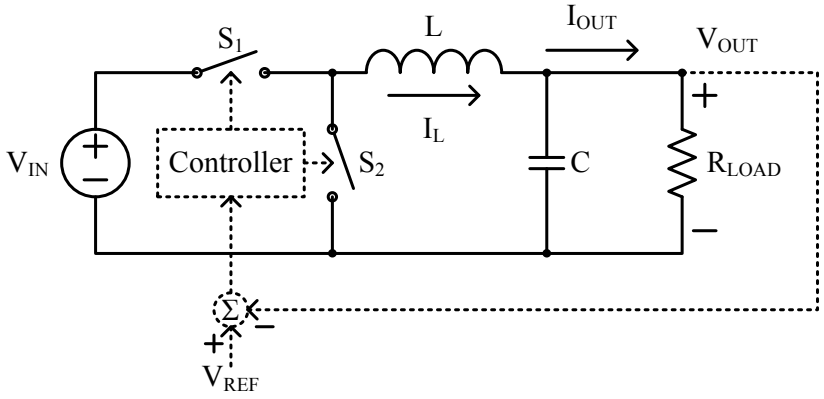


Fig. 95. Simplified schematic diagram of a buck voltage regulator

The relationship between the input voltage V_{IN}, output voltage V_{OUT}, and the duty cycle D of the switches, is given by

$$\frac{V_{OUT}}{V_{IN}} = D \tag{5.1}$$

and the values of the inductor L and capacitor C can be selected according to

$$L = \frac{V_{IN} - V_{OUT}}{2\Delta i_L f_s} D \tag{5.2}$$

$$C = \frac{\Delta i_L}{8 \Delta v_C f_s} \tag{5.3}$$

where Δi_L, Δv_C, and f_s are the inductor current ripple, the capacitor voltage ripple, and the switching frequency, respectively [63]–[66].

b. Boost Voltage Regulator

The boost voltage regulator takes a DC input voltage V_{IN} and produces a DC output voltage V_{OUT} that is higher in value than the input voltage, but of the same polarity. A simplified schematic of a boost voltage regulator is illustrated in Fig. 96. It consists of a DC input voltage V_{IN}, two controlled switches S_1 and S_2, along with a controller to operate them properly, a boost inductor L, a filter capacitor C, and the load resistance R_{LOAD} [63]–[68].

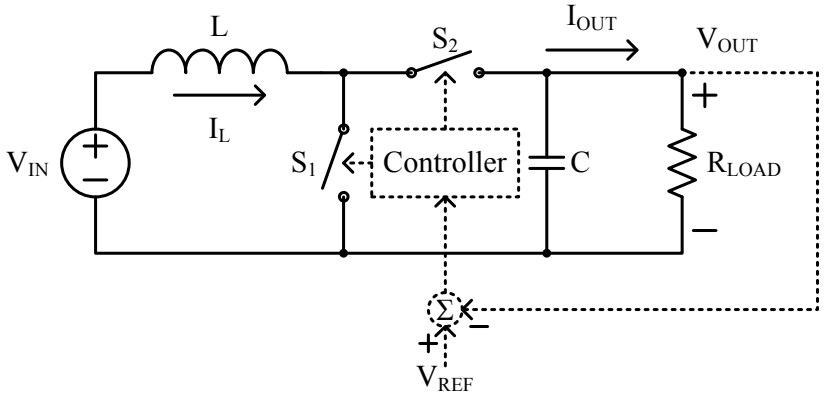


Fig. 96. Simplified schematic diagram of a boost voltage regulator

The relationship between the input voltage V_{IN}, output voltage V_{OUT}, and the duty

cycle D of the switches, is given by

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{1 - D} \tag{5.4}$$

and the values of the inductor L and capacitor C can be selected according to

$$L = \frac{V_{IN}}{2\Delta i_L f_s} D \tag{5.5}$$

$$C = \frac{V_{OUT}}{2\Delta v_C R_{LOAD} f_s} D \tag{5.6}$$

where Δi_L, Δv_C, and f_s are the inductor current ripple, the capacitor voltage ripple, and the switching frequency, respectively [65], [66].

c. Buck-Boost Voltage Regulator

The buck-boost voltage regulator, depicted in Fig. 97, takes a DC input voltage V_{IN} and produces a DC output voltage V_{OUT} that is opposite in polarity to the input voltage. The negative output voltage can be either larger or smaller in magnitude than the input voltage. It also consists of a DC input voltage V_{IN}, two controlled switches S_1 and S_2, with a controller to operate them properly, a filter inductor L, a filter capacitor C, and the load resistance R_{LOAD} [63]–[68].

The relationship between the input voltage V_{IN}, output voltage V_{OUT}, and the duty cycle D of the switches, is given by

$$\frac{V_{OUT}}{V_{IN}} = -\frac{D}{1 - D} \tag{5.7}$$

and the values of the inductor L and capacitor C can be selected according to

$$L = \frac{V_{IN}}{2\Delta i_L f_s} D \tag{5.8}$$

$$C = \frac{V_{OUT}}{2\Delta v_C R_{LOAD} f_s} D \tag{5.9}$$

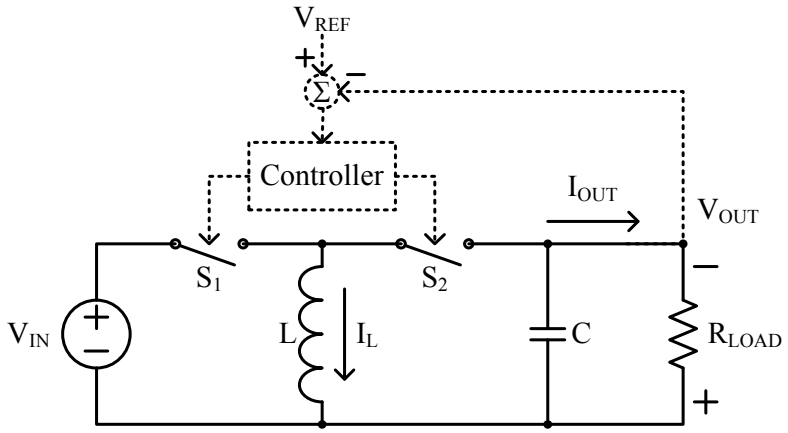


Fig. 97. Simplified schematic diagram of a buck-boost voltage regulator

where Δi_L, Δv_C, and f_s are the inductor current ripple, the capacitor voltage ripple, and the switching frequency, respectively [65], [66].

d. Main Control Schemes for Switching Converters

A DC-DC voltage regulator must provide a regulated DC output voltage under varying load and input voltage conditions. Hence, the control of the output voltage should be done in a closed-loop topology using principles of negative feedback. The two most common closed-loop control methods for DC-DC voltage converters, presented in Fig. 98, are the voltage-mode control and the current-mode control [65], [68], [75]–[77].

In the voltage-mode control scheme, in Fig. 98(a), the converter output voltage $v_{OUT}(t)$ is sensed and subtracted from an external reference voltage $v_{REF}(t)$ in the controller. The controller produces a control voltage that is compared to a carrier, triangular or sawtooth, waveform $v_C(t)$. The comparator produces a pulse-width modulated signal that is fed to drivers, and then filter out at the second-order low-pass filter. The duty cycle of the pulse-width modulated signal depends on the value of the reference voltage [65], [68], [75]–[77].

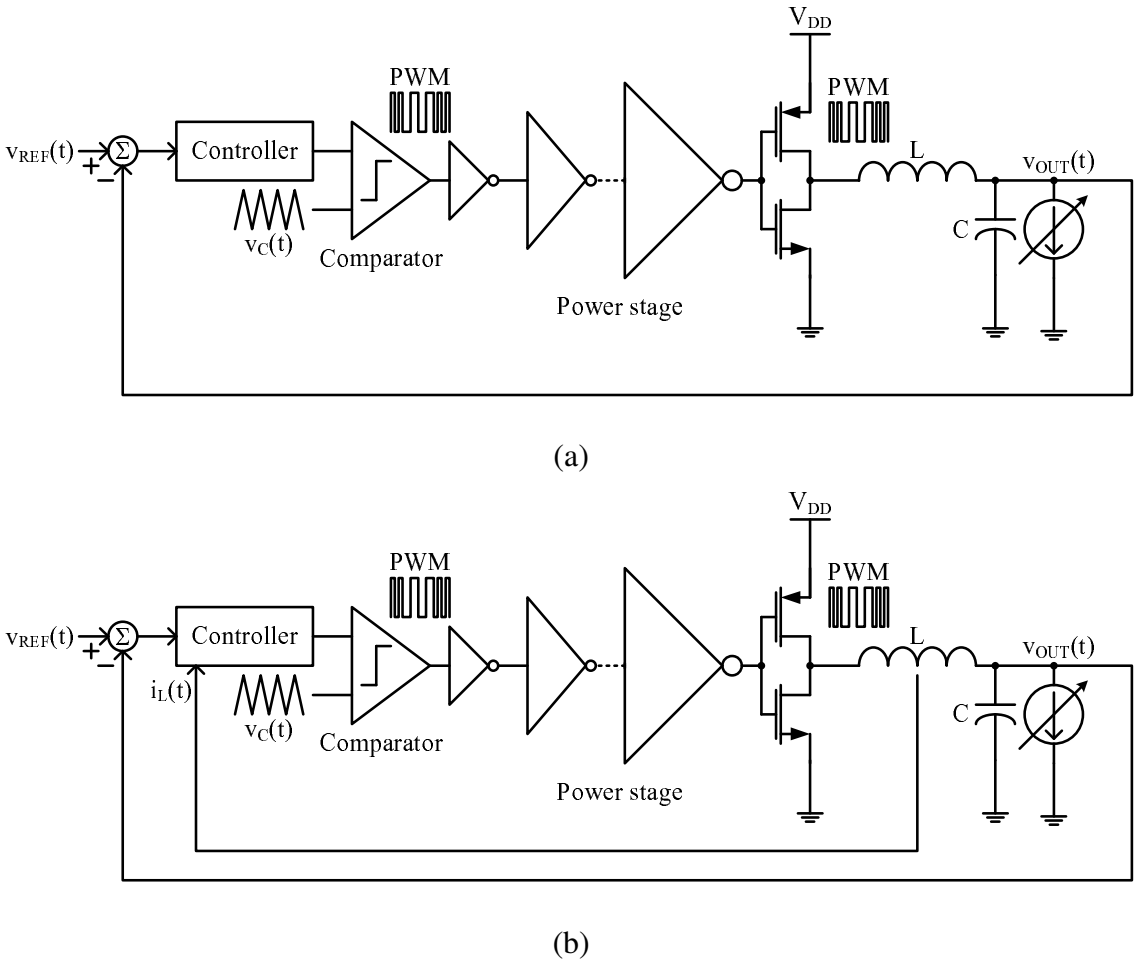


Fig. 98. Main control schemes for DC-DC voltage regulators (a) Voltage-mode control and (b) Current-mode control

The current-mode control, in Fig. 98(b), includes an additional inner loop that feeds back the inductor current signal, and this current signal, converted into voltage, is used to add more degrees of freedom in the variables of the controller. Advantages of the current-mode control are the reduction in the converter dynamic order, the equal current sharing in modular converters, and the limit on the peak switch current. The main disadvantage is its complicated hardware to sense the inductor current [65], [68].

Hysteretic (bang-bang) control is also used as control scheme for DC-DC voltage regulators. This control method is simple and uses minimal number of components. However, the hysteretic control generates variable frequency of operation in the converter. This fact limits its acceptation because it produces electro-magnetic interference [65].

2. Guidelines for Measuring DC-DC Voltage Converters

The DC-DC voltage converter main measurements consist on the steady-state measurements and the transient response measurements. The basic measurement equipment for DC-DC voltage converters must include: a stable voltage reference, an oscilloscope, an evaluation board (printed circuit board), multimeter, power resistors, and the low-pass filter components [78], [79].

A general set-up for measurements is shown in Fig. 99. It includes a voltage reference generator V_{DC}, a bias network and a power network for the IC prototype, the low-pass external LC filter network (if any), the load R_L, and a variable current load I_L.

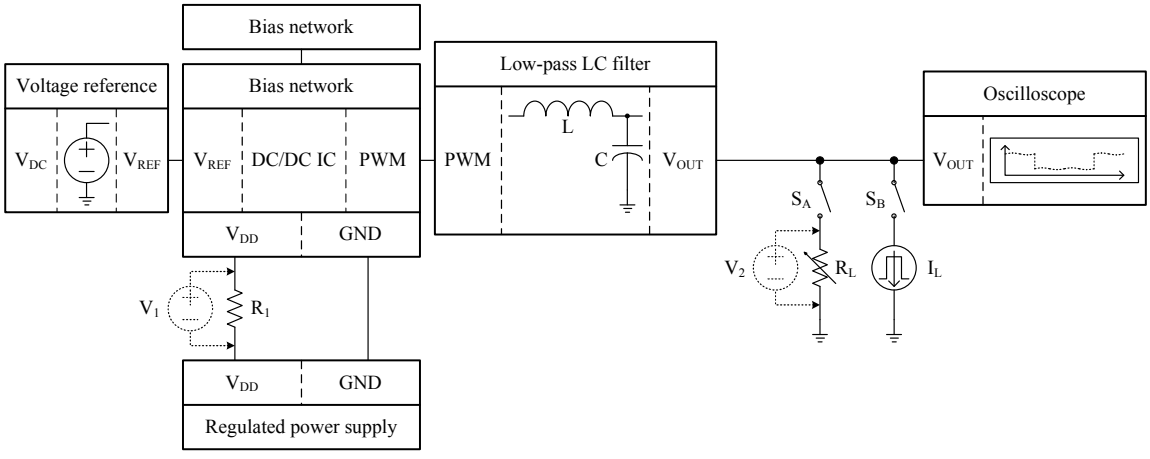


Fig. 99. General set-up for power measurements in DC-DC voltage regulators

a. Steady-State Measurements

The steady-state measurements include the verification of the proper generation of the control signals in the DC-DC voltage converter (voltage ripple, current ripple, pulse-width modulated signal, and switching frequency), and the measurement of the power efficiency of the voltage converter.

These measurements can be performed with the test-bench shown in Fig. 99 when the switch S_A is closed and the switch S_B is open. The control signals can be measured with the oscilloscope, and the power measurements can be performed with the multimeters V_1 and V_2.

The power efficiency (η) of a DC-DC converter is given by the expression

$$\begin{aligned} \eta(\%) &= 100\left(\frac{P_{OUT}}{P_{TOTAL}}\right) \\ &= 100\left(\frac{P_{OUT}}{P_{OUT} + P_{LOSSES}}\right) \\ &= 100\left(\frac{V_{OUT}I_{OUT}}{V_{DD}I_{DD}}\right) \\ &= 100\left(\frac{\frac{V_{OUT}^2}{R_L}}{V_{DD}\frac{V_{R_1}}{R_1}}\right) \end{aligned} \tag{5.10}$$

where P_{OUT} is the average power delivered to the load, P_{TOTAL} is the average total power consumption of the buck converter, and R_1 is a small power resistor (typically 0.1 Ω) placed in series with the voltage supply V_{DD} in order to measure the current consumed by the power supply. Hence, the power efficiency measurement is done by measuring the output and total power, from the minimum output power to the maximum output power by varying the output load R_L [63], [64], [66]–[68].

b. Transient Response Measurements

The objective of the transient response measurements is to verify the operation of the DC-DC voltage regulator when the output current load varies. It is usually done by applying a step current (typically generated with an electronic load) at the output of the converter and measuring the recovery time as well as the overshoot and undershoot voltages. This test provides useful information about the stability of the DC-DC converter and its optimum range of operation.

The test can be performed with the test bench shown in Fig. 99 when the switch S_A is open and the switch S_B is closed. The output waveforms can be observed in the oscilloscope. The size of the step current applied at the output of the converter, and the resulting transient response, depends on the operation conditions specified in the design, but it is usually done with a step from full current load to medium current load, and from full current load to minimum (sometimes zero) current load [67], [68].

3. Practical Design Considerations for Switching Voltage Converters

Due to the similarities between DC-DC converters and class D audio power amplifiers, because both circuits work under the same operating principle, i.e. they are switching structure systems, the practical design considerations, detailed in previous chapters, for the controller, the comparator, the output power stage, and the layout and printed circuit board, in class D amplifiers apply to the design of DC-DC switching voltage converters [64], [67].

However, in DC-DC voltage converter circuits, special care must be taken with input capacitors because the source impedance is extremely important, as even a small amount of inductance can cause significant ringing and spiking on the voltage at the input of the converter. The best practice is to always provide adequate capacitive bypass as near as

possible to the switching converter input. For best results, an electrolytic capacitor is used with a film capacitor (and possibly a ceramic capacitor) in parallel for optimum high frequency bypassing. Another important consideration is that the power switch (which has the highest ground pin current) must be located as close as possible to the input capacitor. This minimizes the trace inductance along its ground path [67], [78], [79].

CHAPTER VI

AN INTEGRATED LOW-POWER DUAL-OUTPUT BUCK CONVERTER BASED ON SLIDING MODE CONTROL*

The design, implementation, and testing of an integrated low-power dual-output buck voltage regulator, using a versatile, simple, and robust controller, based on sliding mode theory, is presented in this chapter. The dual-output buck voltage regulator proposed architecture implements an analog hysteretic controller, together with a digital logic circuitry, to avoid the use of any overhead circuitry to generate a dedicated reference carrier signal to create the pulse-width modulated (PWM) waveform, thus saving area, and reducing static power consumption.

Furthermore, the proposed topology, which implements only three switches instead of four switches used in conventional solutions, can potentially save up to 20% of silicon area, if the switches employed in the dual-output buck regulator are properly designed and sized. The dual-output buck voltage regulator prototype, fabricated in 0.5 μm CMOS standard technology, operates with a single power supply of 1.8 V, generates 1.2 V and 0.9 V output voltage levels, and supplies a total maximum current of 200 mA, reaching up to 88% power efficiency.

A. Introduction

The implementation of multiple supply voltages in a given electronic device has become mandatory due to the use of different circuits fabricated in different technology processes, the trend in technology scaling, and the employment of optimization techniques. A typical

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system requires the interaction of different subsystems, each one of them fabricated in a different technology process and with particular voltage specifications [63], [80], thus requiring multiple voltage levels. Furthermore, there may be building blocks using newer technologies and lower voltage levels, as well as circuits using legacy power supplies and higher voltage levels [81]. In addition, the use of multiple supply voltages in digital circuits has shown significant reduction of dynamic power dissipation, because its value is proportional to the supply voltage [82]. A dual power supply can reduce the dynamic power dissipation in a given system by employing a lower voltage in non-critical blocks and higher levels in critical paths, without compromising the overall circuit performance [63], [83], [84].

Moreover, the voltage conversion must provide good output regulation, robustness and high efficiency performance. Even though linear regulators and switched-capacitor converters can provide good voltage regulation with low circuit complexity, their main drawbacks are their poor efficiency and low current rate [63]. On the other hand, switching-inductor voltage regulators (DC-DC power converters) deliver much higher efficiency and still provide good voltage regulation with higher current capability, hence making them an attractive solution for voltage conversion.

Figure 100 illustrates the basic schematic diagram of a conventional buck voltage converter. The voltage converter is a step-down switching regulator that generates an output voltage (v_{OUT}) lower than the supply voltage (v_{DD}). The output voltage is fed back to the input of the system to obtain the voltage difference between the reference voltage (v_{REF}) and the output voltage. Such error voltage is processed in the controller in order to generate the proper signals to operate switches M_P and M_N. Then, the output of the controller is fed to a comparator, which creates a binary pulse-width modulated (PWM) signal, whose duty cycle (D) is proportional to the voltage conversion ratio. The power stage is needed to enhance the digital modulated signal and to reduce the output resistance. Finally, a second

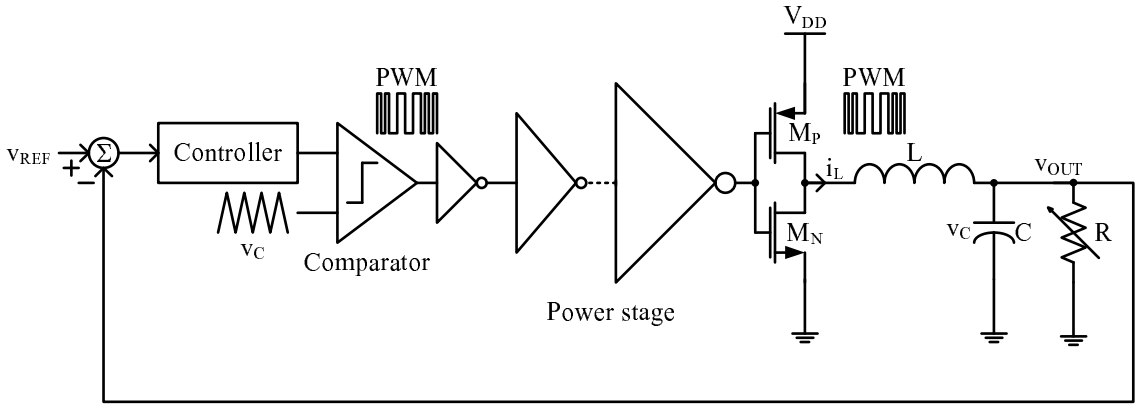


Fig. 100. Basic block diagram of a conventional buck voltage regulator

order LC low-pass filter (LPF) attenuates the high frequency components from the binary modulated signal and delivers its average voltage to the variable load R, along with a small high-frequency voltage ripple.

In order to deliver multiple voltage levels in a given system, the number of switching converters must be multiplied by the same number of voltage supplies required, thus increasing the number of extra components and the amount of area used by the power network [85]. To overcome this problem, several solutions have been proposed, including the combination of switching elements to minimize the number of components in converters with multiple outputs [80], and the reduction of passive components by sharing the output inductor in the low-pass filter [81], [86]. The former method has been already implemented with discrete components, but the lack of a dedicated controller has limited its potentiality. In this chapter, we present the design and implementation of a sliding mode based controller, along with the power switches, to demonstrate that the integration of a dual-output buck voltage regulator [80] can be feasible, reliable, cheap and versatile.

This chapter is organized as follows. Section B introduces the dual-output buck

voltage regulator and its principles of operation, as well as the specifications of the fabricated prototype. Section C discusses the design of the proposed controller. Section D presents the details of the main building blocks used in the proposed architecture. Experimental results of the fabricated prototype are shown in Section E. Finally, Section F summarizes the key points of the proposed dual-output buck voltage regulator.

B. Multiple-Output Buck Voltage Converter

The architecture of a conventional buck converter requires a pair of switches for continuous-conduction mode (CCM) operation [66], hence, in order to generate n number of output voltages it would be necessary to implement $2n$ number of switches. Instead, the proposed dual-output buck converter [80], whose basic schematic diagram is shown in Fig. 101(a), implements $(n + 1)$ number of switches for n number of outputs. The reduction in the number of switches potentially reduces the amount of area, and the number of external components, however, there are also drawbacks due to the higher current rate across the switches [80]. The converter presented in this chapter has been designed for dual-output operation, however it can be easily extended to multiple-output operation by increasing the number of switches, although limiting the converter performance. The proposed dual-output buck voltage converter uses only three switches, instead of four switches used when two output voltages are generated in conventional solutions.

1. Dual-Output Operation

Figure 101 shows the basic schematic diagram of the dual-output buck converter and its operation modes. The steady state operation of the regulator has $(n + 1)$ subintervals for n number of outputs. For this specific case, a complete cycle of operation consists on three different subintervals.

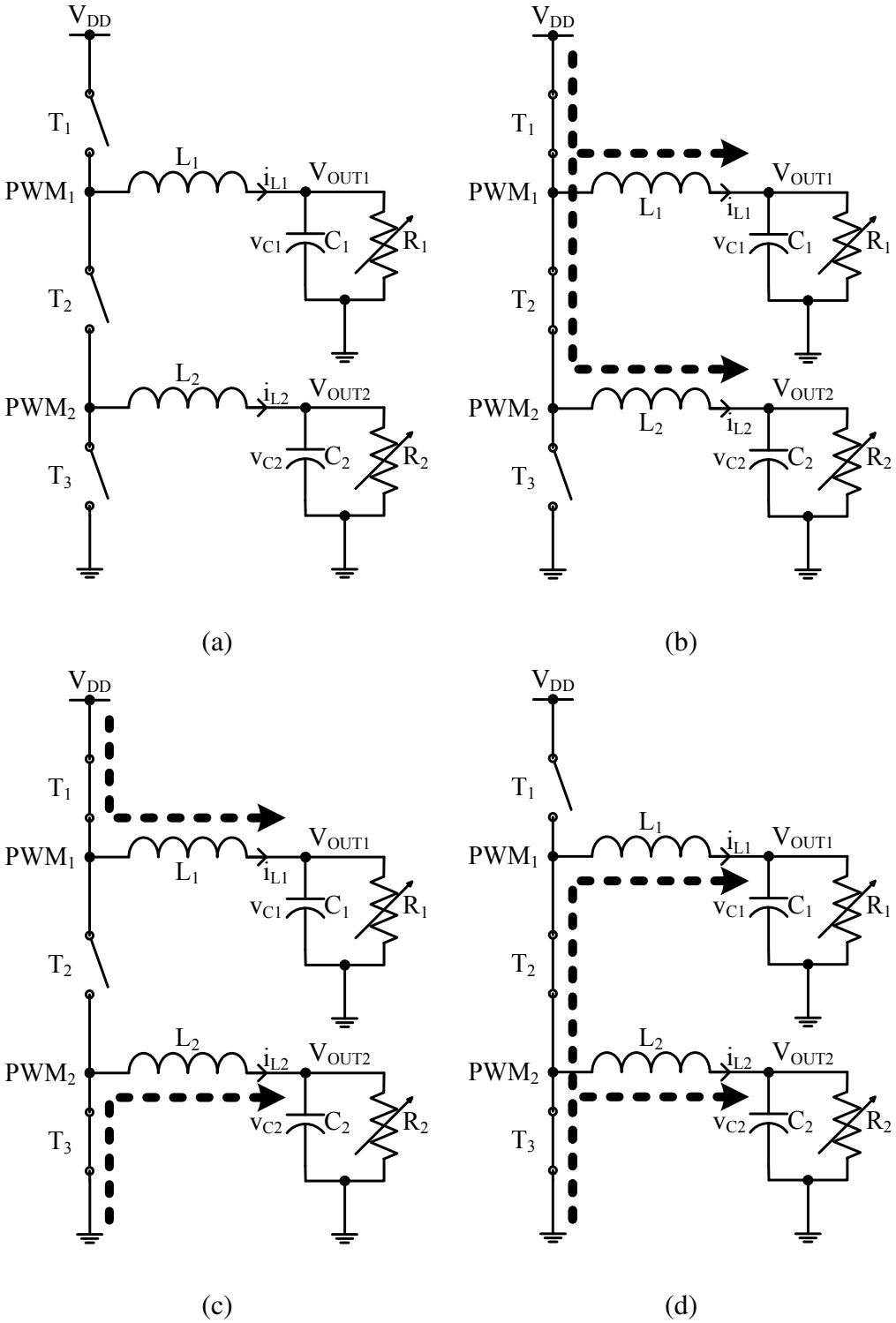


Fig. 101. (a) Basic schematic diagram of the dual-output buck voltage regulator and its operating modes (b) Subinterval I (c) Subinterval II and (d) Subinterval III

During Subinterval I, shown in Fig. 101(b), the switches T_1 and T_2 are closed, and switch T_3 is open. The current flows from the power supply through the inductors toward the output nodes. Since the converter requires $V_{OUT1} \geq V_{OUT2}$ for proper operation, the length of the first subinterval limits the duty cycle of V_{OUT2}. In Subinterval II, illustrated in Fig. 101(c), switch T_1 remains closed, switch T_2 opens, and switch T_3 closes. The duration of Subinterval I plus Subinterval II determines the duty cycle for V_{OUT1} ($D_1 \geq D_2$). Finally, during Subinterval III, depicted in Fig. 101(d), switch T_1 opens, switch T_2 closes again, and switch T_3 remains closed.

Figure 102 sketches the necessary signals to operate the dual-output buck voltage converter. Signals G_1, G_2, and G_3, are applied to switches T_1, T_2, and T_3, in Fig. 101, respectively, and generate each one of the subintervals of operation in the voltage regulator. It is worth to mention that these signals must be generated such that there is a non-

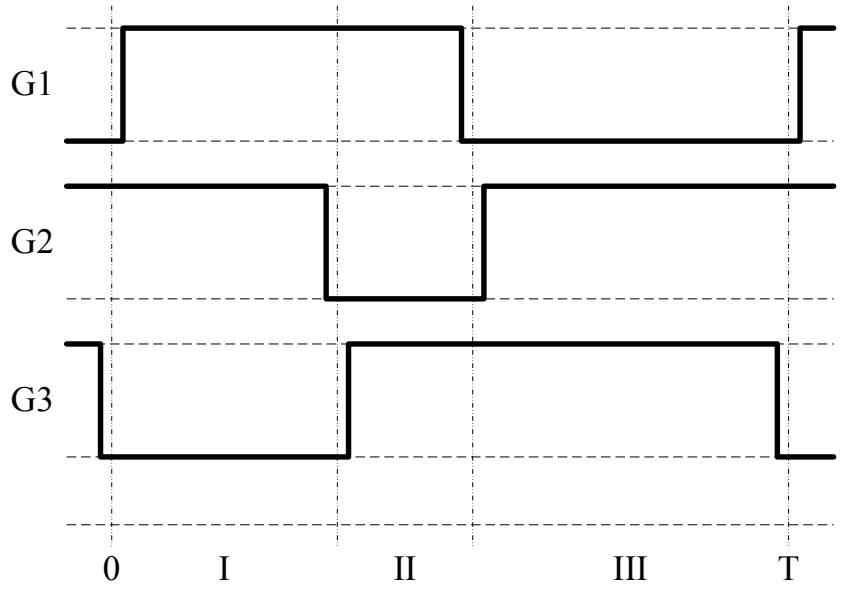


Fig. 102. Sequence of non-overlapping operating signals applied to T_1, T_2, and T_3, in the dual-output buck voltage converter

overlapping sequence in the transition between subintervals to avoid the possible generation of short-circuit current if all switches are closed at the same time.

a. Dual-Output Buck Converter Specifications

The dual-output buck voltage regulator has been implemented using 0.5 μm standard CMOS technology, and its specifications are listed in Table XV. The values of the voltage supply and the output voltages were selected according to the trend in technology scaling. The switching frequency was chosen for compatibility with commercial products. The inductors and capacitors are the only external components of the buck regulator and their values were calculated assuming continuous-conduction mode steady-state operation [66]. The details of the design, implementation, and testing of the dual-output voltage regulator,

Table XV. Dual-output buck voltage converter specifications

Parameter	Output 1 (V_{OUT1})	Output 2 (V_{OUT2})
Supply voltage (V_{DD})	1.8 V	1.8 V
Output voltage (V_{OUT})	1.2 V	0.9 V
Max. output current (I_{MAX})	100 mA	100 mA
Switching frequency (f_s)	500 kHz	500 kHz
Output current ripple (Δi)	0.05 $\times$ I_{MAX}	0.05 $\times$ I_{MAX}
Output voltage ripple (Δv)	0.01 $\times$ V_{OUT1}	0.01 $\times$ V_{OUT1}
Output inductor (L)	82 μH	90 μH
Output capacitor (C)	0.83 μF	1.11 μF
Duty cycle (D)	0.67	0.50

which includes the controller, comparators, and output switches, are explained in the following sections.

C. Design of the Proposed Sliding Mode Controller

1. Preliminaries

Sliding mode control (SMC) is used in systems with discontinuous differential equations and is mostly applied to systems with variable structures. Sliding mode control developed during the 1950s and is intended to solve control problems where the plant changes its structure along time. Robustness to external perturbations is one of the best features of sliding mode control [33]–[36].

In general, the switching converters are examples of systems with variable structures because, during each subinterval of operation, the differential equations describing the system are different. For example, the conventional buck converter in Fig. 100 has two different subintervals of operation, and as a consequence, two different state-space models describe its dynamics. Therefore, the dynamic behavior of the dual-output buck voltage regulator in Fig. 101 can be represented using three state-space models, one for each subinterval of operation. These equations can be condensed as one general state space model as

$$\begin{pmatrix} \frac{d}{dt}i_{L1} \\ \frac{d}{dt}v_{C1} \\ \frac{d}{dt}i_{L2} \\ \frac{d}{dt}v_{C2} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L_1} & 0 & 0 \\ \frac{1}{C_1} & -\frac{1}{C_1R_1} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_2} \\ 0 & 0 & \frac{1}{C_2} & -\frac{1}{C_2R_2} \end{pmatrix} \begin{pmatrix} i_{L1} \\ v_{C1} \\ i_{L2} \\ v_{C2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_1} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \end{pmatrix} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{6.1}$$

where the state variables i_L and v_C represent the inductor currents and the capacitor voltages, and the control inputs u_1 and u_2 are the pulse-width modulated signals at nodes

PWM_1 and PWM_2 in Fig. 101. The values of the input signal vector, u_1 and u_2, generate the three subintervals in the dual-output operation mode. In the first subinterval, nodes PWM_1 and PWM_2 are connected to the voltage supply V_{DD}. During the second subinterval, PWM_1 remains the same but PWM_2 is grounded. Finally, in the last subinterval, both PWM_1 and PWM_2 are grounded.

Even though one cycle of operation in the dual-output buck converter contains three subintervals, each output can be seen as the combination of two different structures because the pulse-width modulated waveform is a binary signal. In other words, the proposed dual-output buck voltage regulator can be seen as two stacked conventional buck converters where each output is defined by the combination of two different states during the three subintervals in one cycle. For example, Fig. 103 illustrates the two different structures of the second output V_{OUT2} during one cycle of operation in the dual-output buck voltage converter. For this case, structure I corresponds to subinterval I, and structure II represents the dual-output buck voltage converter during subinterval II and subinterval III in Fig.

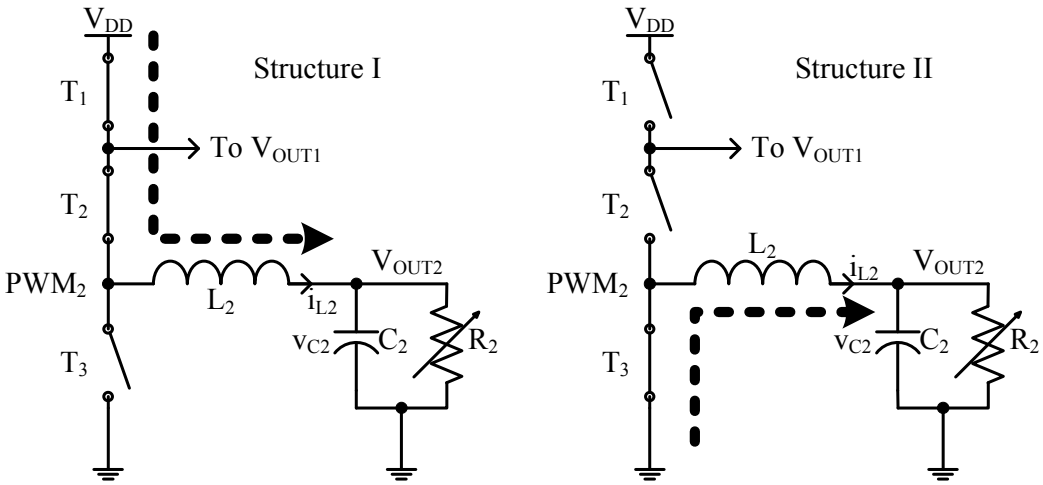


Fig. 103. Structures of the second output V_{OUT2} in the dual-output buck voltage converter

101. Similarly, in the case of the first output V_{OUT1}, its first structure would correspond to subinterval I and subinterval II, and its second structure to subinterval III.

Therefore, every output in the dual-output buck voltage regulator can be analyzed independently, and the representation of the converter can be modeled, for simplicity, as shown in equation (6.2), where the subindexes represent each individual output in the voltage converter. The goal is to design a sliding mode controller for each individual output in the dual-output buck voltage converter. Then, combine the control signals by using digital circuitry to generate the sequence of non-overlapping signals, shown in Fig. 102, to properly operate the proposed converter.

$$\begin{pmatrix} \frac{d}{dt} i_{L1,2} \\ \frac{d}{dt} v_{C1,2} \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L_{1,2}} \\ \frac{1}{C_{1,2}} & -\frac{1}{C_{1,2} R_{1,2}} \end{pmatrix} \begin{pmatrix} i_{L1,2} \\ v_{C1,2} \end{pmatrix} + \begin{pmatrix} \frac{1}{L_{1,2}} \\ 0 \end{pmatrix} u_{1,2} \qquad (6.2)$$

2. Proposed Dual-Output Buck Converter Architecture

The proposed architecture for the integration of the dual-output buck voltage converter is shown in Fig. 104. It is a tracking system that minimizes the voltage errors (e_1 and e_2) between the reference signals (V_{REF1} and V_{REF2}) and the output signals (V_{OUT1} and V_{OUT2}) through the sliding mode controller. Then, a couple of binary control signals (S_a and S_b) are combined using digital logic to generate the signals G_1, G_2, and G_3, which control the operation of the output switches. An output buffer is used to enhance the digital signals and to provide enough driving capability to the output nodes. Also, a sensing circuit at node PWM2 generates a bootstrapped voltage signal to operate the middle switch. As previously stated, the LC low-pass filters are implemented using external components due to their large size.

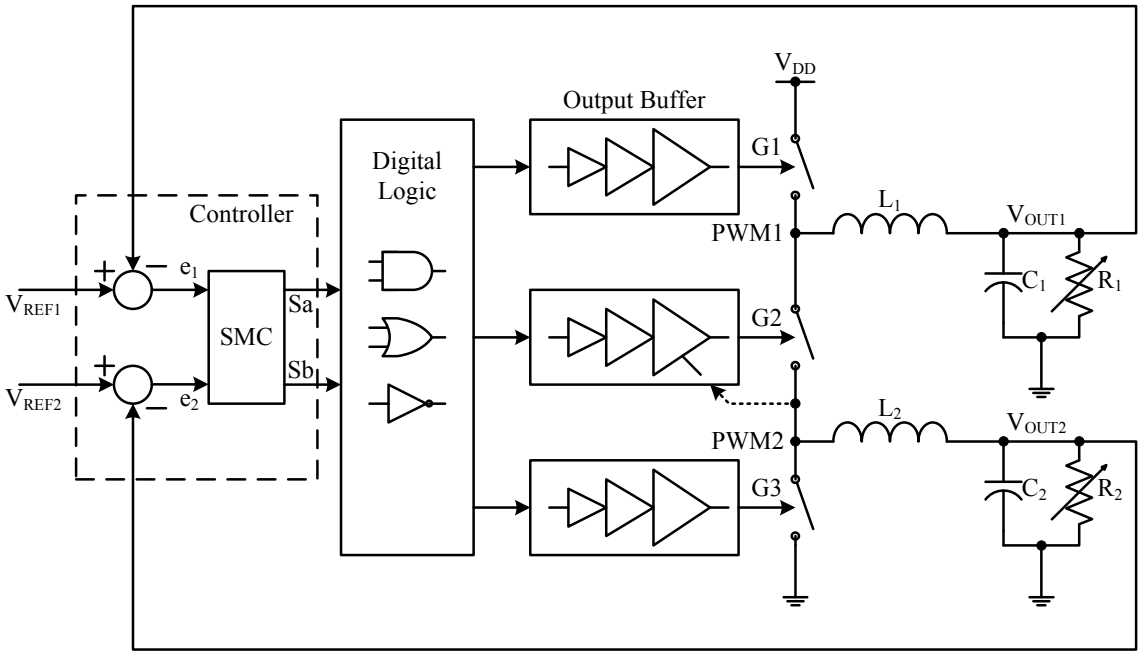


Fig. 104. Dual-output buck voltage converter conceptual diagram

a. Sliding Mode Controller Design

Since the dual-output buck voltage converter is a tracking system, the goal of the sliding mode controller consists in making the output voltages (V_{OUT1} and V_{OUT2}) to follow the reference signals (V_{REF1} and V_{REF2}) by minimizing the error voltages (e_1 and e_2). The sliding mode controller generates a control function, i.e. a control law, also called switching function (SF), to stabilize a given system. The control function makes the system to switch between its different structures until it reaches its sliding equilibrium point (SEP) [56]. The dual-output buck voltage regulator has two different sliding equilibrium points, one for each output voltage. The sliding equilibrium point of the first output voltage node (V_{OUT1}) is

$$SEP_1 = (V_{REF1}, I_{OUT1}) \tag{6.3}$$

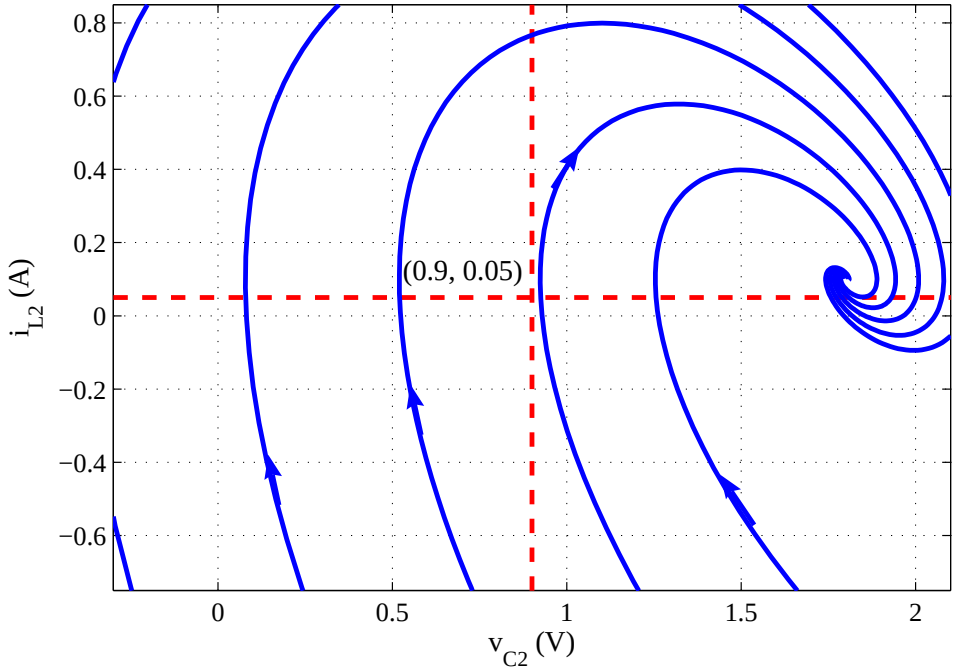
and the sliding equilibrium point of the second output voltage (V_{OUT2}) is

$$SEP_2 = (V_{REF2}, I_{OUT2}) \tag{6.4}$$

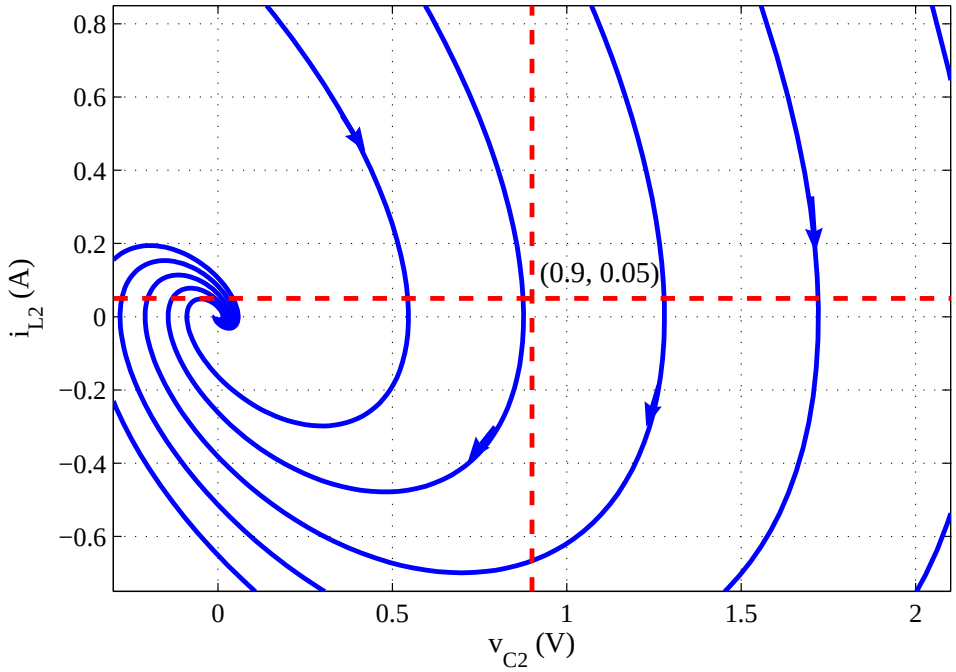
where I_{OUT1} and I_{OUT2} can go from 5 mA (for continuous-conduction operation) up to the maximum current 100 mA.

For example, the phase portraits of the two different structures of the second output voltage (V_{OUT2}) in the dual-output buck converter, in Fig. 103, are shown in Fig. 105, for the particular case of V_{REF2} = 0.9 V and I_{OUT2} = 50 mA. The phase portrait, in Fig. 105(a), corresponds to structure I in Fig. 103. It represents the trajectories of the dynamic system modeled by equation (6.2) when the input signal u_2 equals the supply voltage V_{DD}. Each trajectory represents the motion of the state space variables v_{C2} and i_{L2} in the phase plane. Even though structure I converges to an stable focus [36], it does not reach the sliding equilibrium point (V_{REF2} = 0.9 V, I_{OUT2} = 50 mA). Similarly, the phase portrait in Fig. 105(b) corresponds to structure II, in Fig. 103, when the input signal u_2 is grounded. As in the previous case, structure II does not converge to the sliding equilibrium point.

Figure 106(a) combines the phase portraits of structure I and structure II, shown in Fig. 103, in one single plot for comparison. It can be appreciated that the sliding equilibrium point is never reached. Therefore, the implementation of a controller is necessary. By designing an appropriate sliding mode controller, the switching function will make the system to toggle between both structures, and will create a sliding surface. In other words, regarding of the initial conditions, the dynamics of the system will move toward the sliding surface until they hit it. Once there, the system will slide in direction of the sliding equilibrium point. This phenomenon is illustrated in Fig. 106(b).

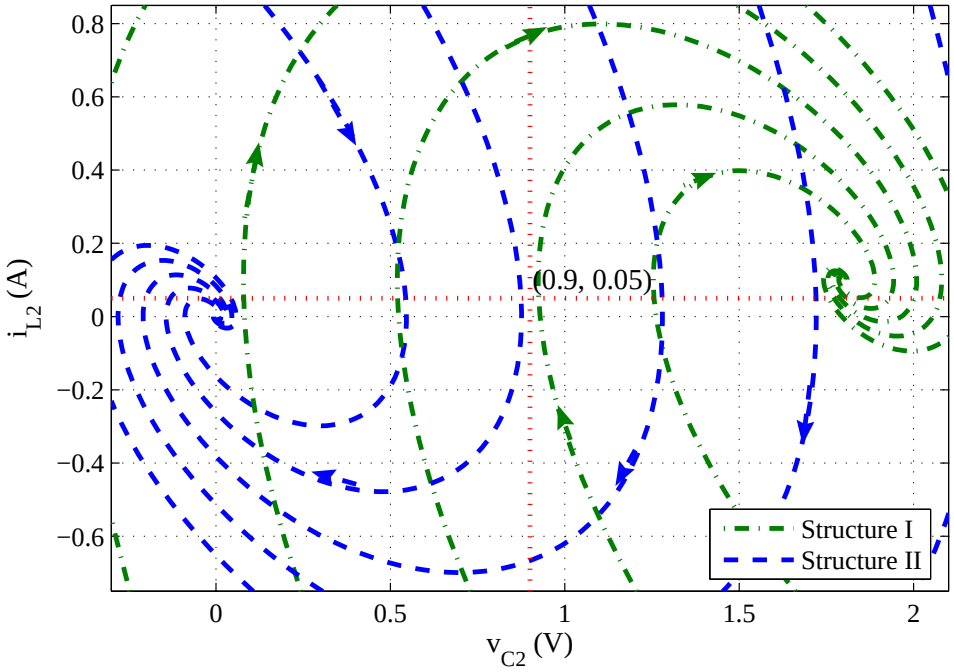


(a)

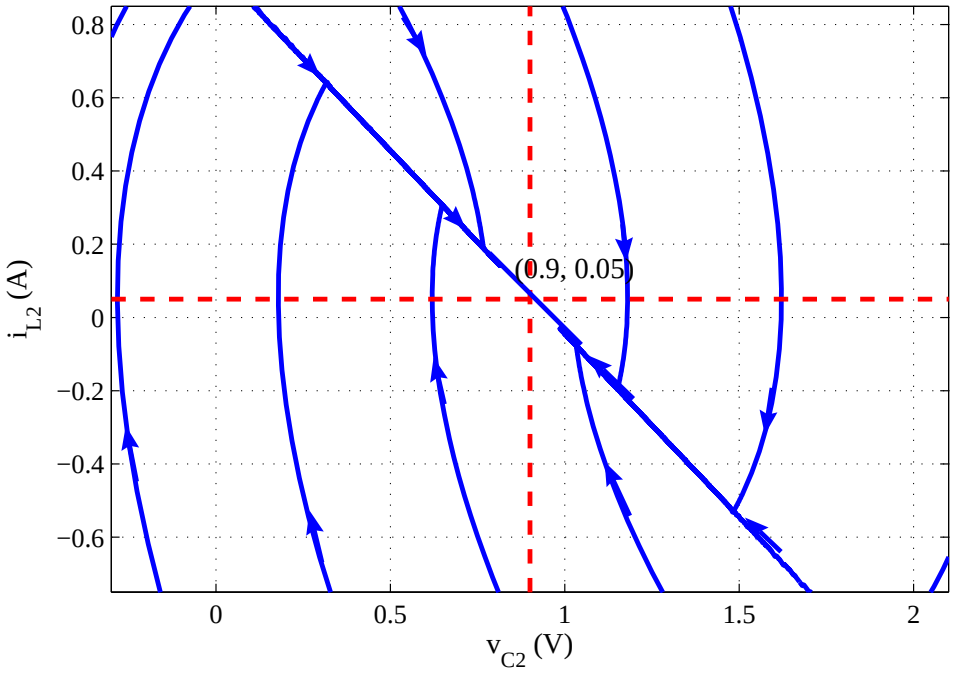


(b)

Fig. 105. Phase portraits of second output voltage (V_{OUT2}) in the dual-output voltage regulator (a) Phase portrait of structure I and (b) Phase portrait of structure II



(a)



(b)

Fig. 106. Phase portraits of second output voltage (V_{OUT2}) in the dual-output buck voltage converter (a) Unregulated system trajectories and (b) Controlled system trajectories

In general, for a system of order *k*, sliding mode theory requires a controller of order *(k - 1)* [33],[35],[36]. Since each output in the dual-output buck converter is modeled by the second-order state-space models in equation (6.2), the controller dynamics are defined by a first order equation. The dual-output voltage regulator switching functions, expressed in the frequency domain, are given by equations (6.5) and (6.6). Their derivation and necessary conditions for stability are discussed in Appendix B.

$$S_1(E_1, s) \;=\; (1 \;+\; \alpha s)E_1(s) \tag{6.5}$$

$$S_2(E_2, s) \;=\; (1 \;+\; \beta s)E_2(s) \tag{6.6}$$

where $\alpha \approx 5.834 \times 10^{-6}$ and $\beta \approx 7.068 \times 10^{-6}$ are calculated using Bessel coefficients to obtain smooth and fast transient response. The switching functions are defined as the sum of the error signals (e_1 and e_2) and their derivatives, multiplied by a constant. The sliding mode control will make each subsystem to switch according to the sign of the switching function as

$$u_{1,2} \;=\; \begin{cases} V_{DD} & \text{when} \quad s_{1,2}(e_{1,2}, t) \;>\; 0 \\ 0 & \text{when} \quad s_{1,2}(e_{1,2}, t) \;<\; 0 \end{cases} \tag{6.7}$$

The practical implementation of the sliding mode controller, including drawbacks and proposed solutions, is detailed in next section.

D. Implementation of Building Blocks

The complete dual-output buck voltage convert diagram is shown in Fig. 107. The single-ended voltages (V_{REF1}, V_{REF2}, V_{OUT1}, and V_{OUT2}) are converted to fully-differential signals through the single-ended to fully-differential (SE2FD) amplifiers in order to minimize the common mode switching substrate noise. Then, the sliding mode controllers (SMC_1 and SMC_2) generate the analog switching functions (S_1 and S_2). Next, the decision circuits

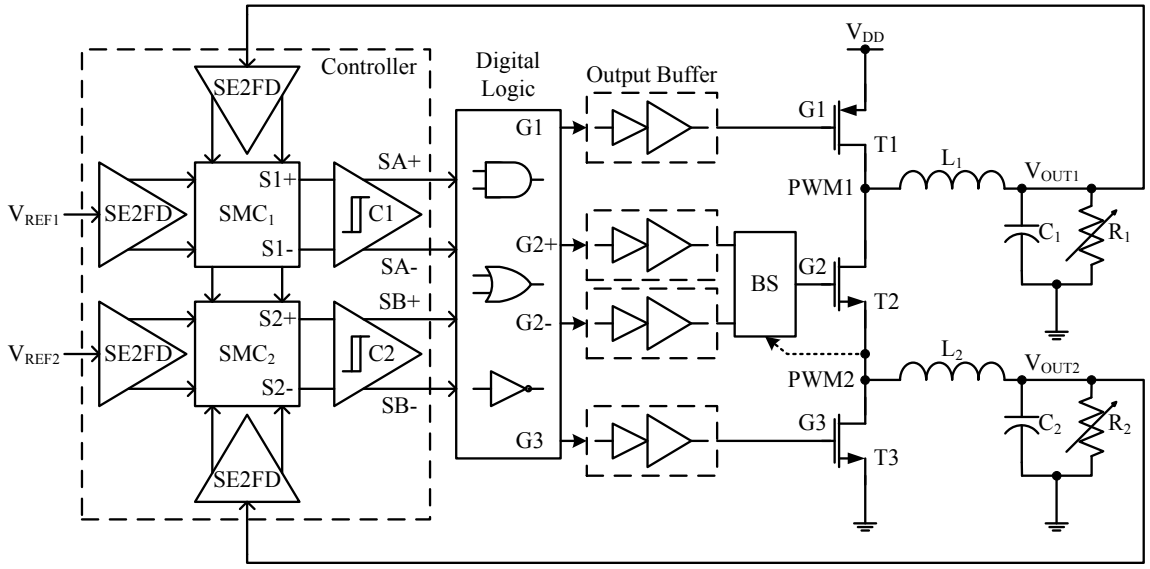


Fig. 107. Complete dual-output buck voltage converter block diagram

(comparators C_1 and C_2) create the binary signals (S_A and S_B) and the digital logic combine them properly to create the operating signals G_1, G_2, and G_3. The bootstrapping (BS) circuit generates the proper voltage level to switch NMOS transistor T_2. Finally, the tow low-pass filters attenuate the high frequency components of the binary signals from nodes PWM1 and PWM2.

1. Implementation of the Sliding Mode Controller

a. Single-Ended to Fully-Differential Converters

The first block of the analog controller is the single-ended to fully-differential converter. Its function is to generate a fully-differential signal which is robust to common mode voltages. Fully-differential routing is also advisable to minimize the effect of common switching noise coming from the substrate. The switching nature of the converter injects high current

spikes into the substrate which can produce false triggering in the pulse-width modulated signals. Fully-differential signals, as well as robust and symmetric layout, use of guard rings, and separation of reference grounds, are also recommended to reduce these problems.

The single-ended signals used in the controller, i.e. the output voltages (V_{OUT1} and V_{OUT2}) and the reference signals (V_{REF1} and V_{REF2}), are converted to fully-differential by using a single-ended to fully-differential converter per signal. The block diagram of this converter is shown in Fig. 108. The operational amplifier (OPAMP) is a two-stage structure with Miller compensation [47]. Its schematic diagram is shown in Fig 109, and the size of the transistors used for its implementation are listed in Table XVI. Additionally,the value of the bias current I_B is 2.5 μA, the compensation capacitor C_C is 1 pF, the compensation resistance R_C is 10 kΩ, and the common-mode resistor R_{CM} is 100 kΩ. A summary of its most important characteristics is shown in Table XVII.

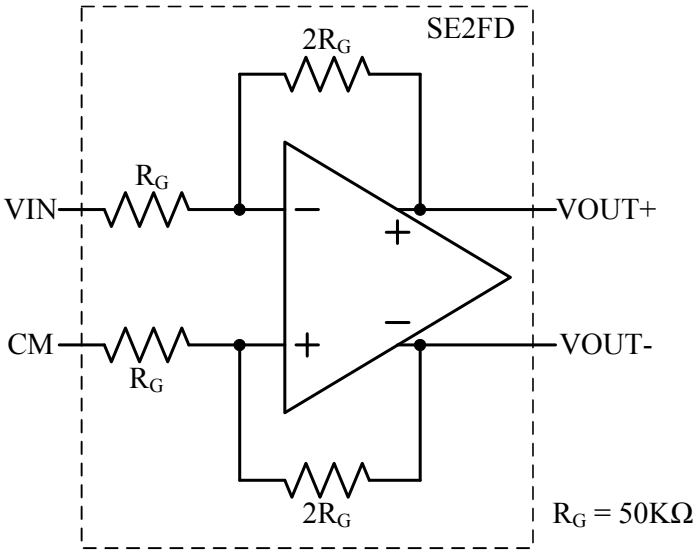


Fig. 108. Single-ended to fully-differential converter top level configuration

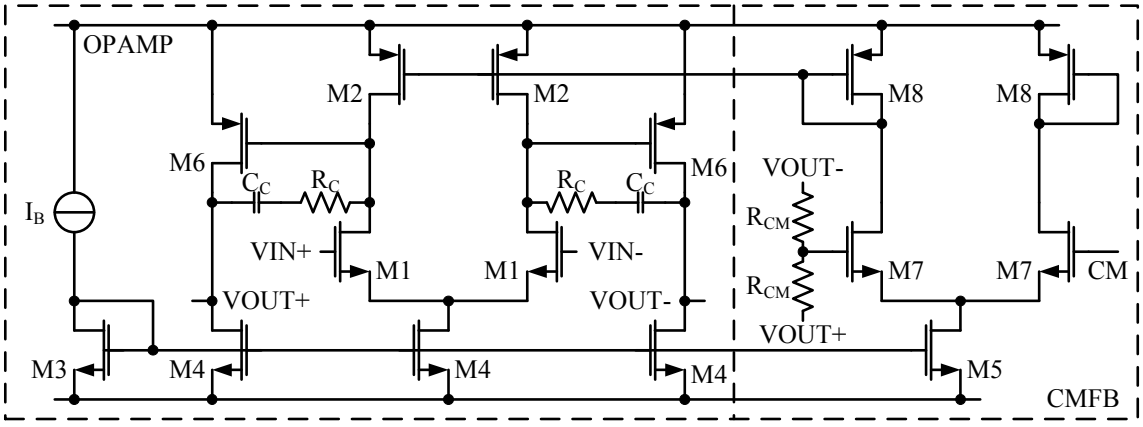


Fig. 109. Schematic diagram of the operational amplifier used to implement the single-ended to fully-differential converters

Table XVI. Transistor sizes used in single-ended to fully-differential amplifier

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	10.05	1.2	12
M2	10.05	1.2	8
M3	4.95	1.2	4
M4	4.95	1.2	16
M5	4.95	1.2	8
M6	10.05	1.2	16
M7	4.95	0.9	8
M8	10.05	1.2	4

Table XVII. Single-ended to fully-differential operational amplifier specifications

Parameter	Value
DC gain	60.52 dB
GBW	11.06 MHz
Phase margin	70.57°
I_Q	31.42 μA
P_Q	56.56 μW

b. Sliding Mode Controllers

The sliding mode controllers implement the switching functions expressed in equations (6.5) and (6.6). The error signals (e_1 and e_2) and the analog switching functions (S_1 and S_2) are generated by using a single operational amplifier in order to minimize the number of components as well as power consumption, and silicon area.

Since the ideal realization of the switching functions require the use of a lossless differentiator element, the high-frequency gain of the switching functions is partially bounded by creating a lossy-differentiator (LD) structure. Then, the modified switching functions are given by

$$S_1(E_1, s) = \left(1 + \frac{\alpha s}{\frac{\alpha}{\gamma} s + 1}\right) E_1(s) \tag{6.8}$$

$$S_2(E_2, s) = \left(1 + \frac{\beta s}{\frac{\beta}{\gamma} s + 1}\right) E_2(s) \tag{6.9}$$

where $\gamma \gg 1$ represents the gain of the lossy-differentiator at high frequencies, and

γ / α = ω_{p} is the frequency of the pole introduced by the lossy-differentiator. In other words as γ increases, the high-frequency gain of the switching frequency increases and the bandwidth requirements of the controller also increases. On the other hand, the use of finite bandwidth operational amplifiers (characterized by one single dominant pole at $\omega_{3\mathrm{dB}}$) in the implementation of the switching functions adds an extra pole to the lossy switching functions, previously expressed in equations (6.8) and (6.9). This natural pole affects the error constant gain as well as the lossy derivative but it does not jeopardize the sliding mode controller stability. The switching functions, including the additional pole, are given by

$$S_1(E_1, s) = \left[\frac{1}{\left(1 + \frac{s}{\omega_{1,1}}\right)} + \frac{\alpha s}{\left(1 + \frac{s}{\omega_{1,2}}\right)\left(1 + \frac{s}{\omega_{1,3}}\right)} \right] E_1(s) \tag{6.10}$$

$$S_2(E_2, s) = \left[\frac{1}{\left(1 + \frac{s}{\omega_{2,1}}\right)} + \frac{\beta s}{\left(1 + \frac{s}{\omega_{2,2}}\right)\left(1 + \frac{s}{\omega_{2,3}}\right)} \right] E_2(s) \tag{6.11}$$

where $\omega_{1,1}$ and $\omega_{2,1}$ are the extra poles introduced by the operational amplifier closed loop finite bandwidth, and $\omega_{1,2}$, $\omega_{2,2}$, $\omega_{1,3}$, and $\omega_{2,3}$ are the poles affected by the finite operational amplifier closed loop pole ($\omega_{3\mathrm{dB}}$) and the lossy-differentiator pole (ω_{p}). Note that

$$\omega_{1,1} > \omega_{1,2}, \omega_{1,3} \tag{6.12}$$

$$\omega_{2,1} > \omega_{2,2}, \omega_{2,3} \tag{6.13}$$

In general, the frequency response of the switching functions, including the effect of the lossy-differentiators as well as the operational amplifiers finite bandwidth, can be represented as the sketch in Fig. 110. The plot represents the frequency response of the first term, $\mathrm{E}_{1,2}$(s), and the second term, (α, β)s$\mathrm{E}_{1,2}$(s), in equations (6.10) and (6.11), as well as sum of them, $\mathrm{S}_{1,2}(\mathrm{E}_{1,2}$, s). Observe that this implementation of the switching functions bounds the high-frequency of the controllers and thus limits the integrated noise.

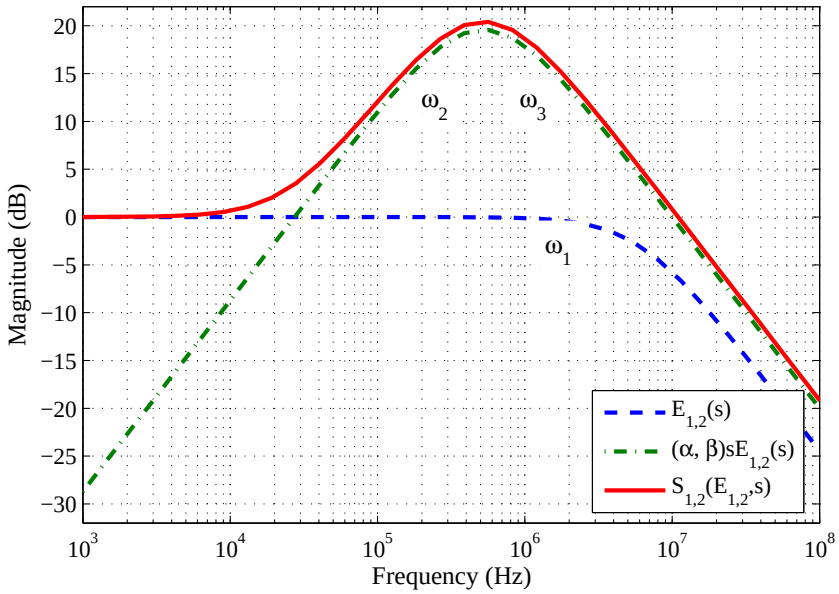


Fig. 110. Sketch of the frequency response of the actual implemented switching functions

The complete dual-buck voltage regulator model was built in MATLAB [87] in order to estimate the requirements of the operational amplifier in the sliding mode controller. The bandwidth of the operational amplifiers was designed specifically to have a transient response error within 10% deviation of the ideal switching functions. Figure 111 shows the transient response of the dual-converter for the different switching function implementations. Case I represents the ideal sliding mode controller, case II corresponds to the switching function with one pole introduced by the lossy-differentiator, and finally, case III depicts the response of the converter when the finite bandwidth of the operational amplifier is taken in consideration. Moreover, Fig. 112 illustrates the error response between the ideal case I and the non-ideal case II and case III. It can be appreciated that the transient response converges to the desired voltage and the initial transient error is less than 9%. The value of γ is set to 10.

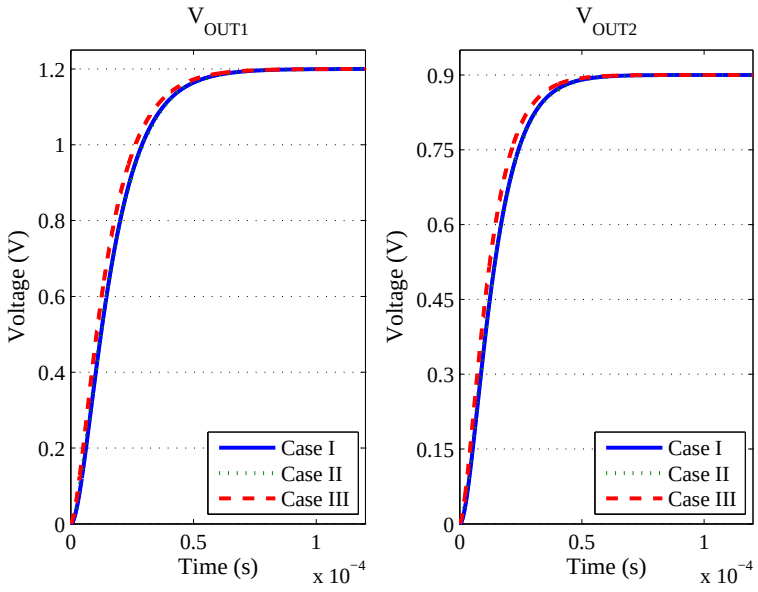


Fig. 111. Transient response of dual-output voltage regulator for non-ideal switching functions

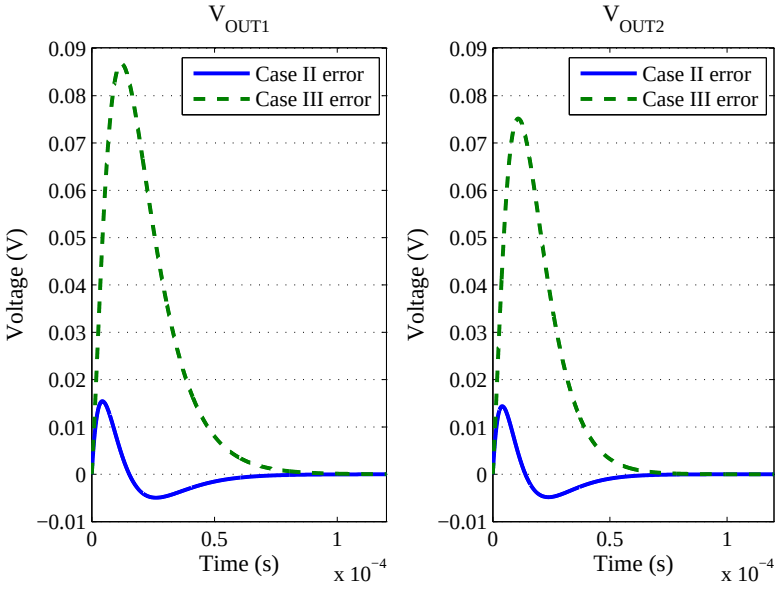


Fig. 112. Voltage errors between ideal and non-ideal switching functions in dual-output voltage regulator

The simulations in the MATLAB model defined an operational amplifier with a minimum DC gain of 60 dB and gain-bandwidth product (GBW) of 12 MHz. The operational amplifier was implemented with a two-stage structure using Miller compensation scheme [47]. The schematic diagram of the operational amplifier is shown in Fig. 113 and its transistor sizes are listed in Table XVIII. The operational amplifier is biased with a current I_B equal to 2.5 μA and it is compensated with a resistor R_C and a capacitor C_C with values of 10 kΩ and 1 pF, respectively. The final operational amplifier characteristics are summarized in Table XIX.

Table XVIII. Transistor sizes used in the operational amplifier employed to implement the switching functions

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	10.05	1.2	12
M2	10.05	1.2	8
M3	4.95	1.2	4
M4	4.95	1.2	16
M5	4.95	1.2	4
M6	10.05	1.2	16
M7	4.95	0.9	4
M8	10.05	1.2	4

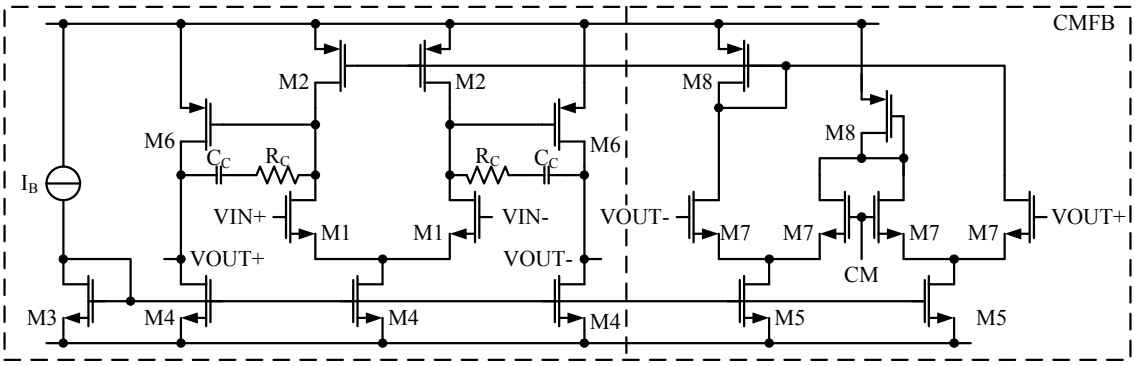


Fig. 113. Schematic diagram of the operational amplifier used to implement the switching functions

c. Decision Circuits

The decision circuits (C_1 and C_2) are two hysteresis comparators based on the schematic of the circuit shown in Fig. 114 [61], [62]. Their objective is to convert the analog switching functions S_1 and S_2 into the binary signals S_A and S_B. The comparators are divided in

Table XIX. Specifications of the operational amplifier used to implement the sliding mode controller

Parameter	Value
DC gain	75.45 dB
GBW	12.06 MHz
Phase margin	66.55°
I_Q	31.42 μA
P_Q	56.56 μW

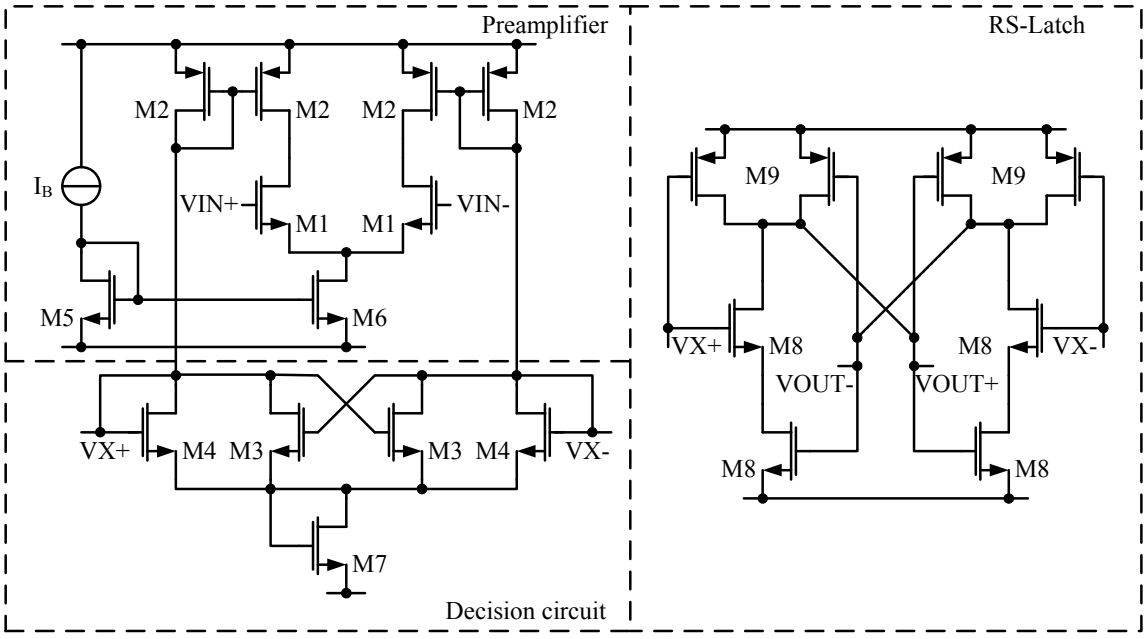


Fig. 114. Schematic diagram of the comparators used to implement the sliding mode controller

three sections; the preamplifier, the decision circuit, and the output latch. The preamplifier amplifies the input signal to improve the comparator sensitivity. The decision circuit is a positive feedback loop able to discriminate the input signals. The ratio of transistors M_3 and M_4 defines the comparator hysteresis window. The latch locks the binary signal produced by the previous stage. The decision circuits specifications, to operate the dual-buck regulator at a switching frequency of 500 kHz, were obtained directly from the MATLAB model simulations. A summary of the size of the transistors employed in the hysteresis comparators is listed in Table XX. A complete list of parameters of comparators C_1 and C_2 is presented in Table XXI.

Table XX. Transistor sizes used in the comparators employed to implement the sliding mode controller

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	4.95	0.6	8
M2	4.95	0.6	4
M3 (C_1)	3.00	0.6	4
M4 (C_1)	3.00	0.6	2
M3 (C_2)	3.00	0.6	6
M4 (C_2)	3.00	0.6	4
M5	10.05	1.2	4
M6	10.05	1.2	16
M7	10.05	0.6	8
M8	3.00	0.6	1
M9	6.00	0.6	4

d. Analog Sliding Mode Controller

The analog sliding mode controller, including operational amplifiers and the decision circuits, is detailed in this section. The first controller (SMC_1 block shown in Fig. 107), implements the switching function in equation (6.10), by combining the output signals coming from the single-ended to fully-differential converters of V_{REF1} and V_{OUT1}. The switching function in equation (6.11) is implemented in the second controller (block SMC_2 in Fig. 107), with the fully-differential signals V_{REF2} and V_{OUT2}.

The schematic of the first controller (SMC_1) is shown in Fig. 115. The ratio of resistors

Table XXI. Specifications of the decision circuits

Parameter	Comparator 1 (C_1)	Comparator 2 (C_2)
Hysteresis voltage	20 mV	15 mV
M_3 / M_4	2.0	1.5
I_B	2.50 μA	5.00 μA
I_Q	15.32 μA	26.61 μA
P_Q	27.58 μW	47.89 μW

R_F and R_C represents the constant gain error in the switching function expressed in equation (6.10), i.e. R_F / R_C = 1. The derivative gain α is determined by the product of R_F and C_C, i.e. $\alpha = R_F C_C$. The pole introduced by the lossy-differentiator is set by the resistor R_F divided by the factor γ, i.e. R_F / γ. As mentioned before, the analog switching function is converted to a binary signal with the comparator (C_1).

The implementation of the second controller (SMC_2) is shown in Fig. 116. As in the previous case, the constant gain error is given by R_F / R_C = 1, the derivative gain β equals to $R_F C_C$, and the lossy-differentiator pole is implemented with R_F / γ. Notice that the value of the capacitor C_C is different than in the first controller because the derivative constant is different, i.e. $\alpha \neq \beta$.

One of the major challenges implementing an analog controller without any reference clock is that both controllers (SMC_1 and SMC_2) may switch at the same frequency, but with out-of-phase signals, causing synchronization problems and potential failure of the system. The proposed solution to overcome this problem is to force both controllers to start switching between states at the same time. Therefore, the first sliding mode controller

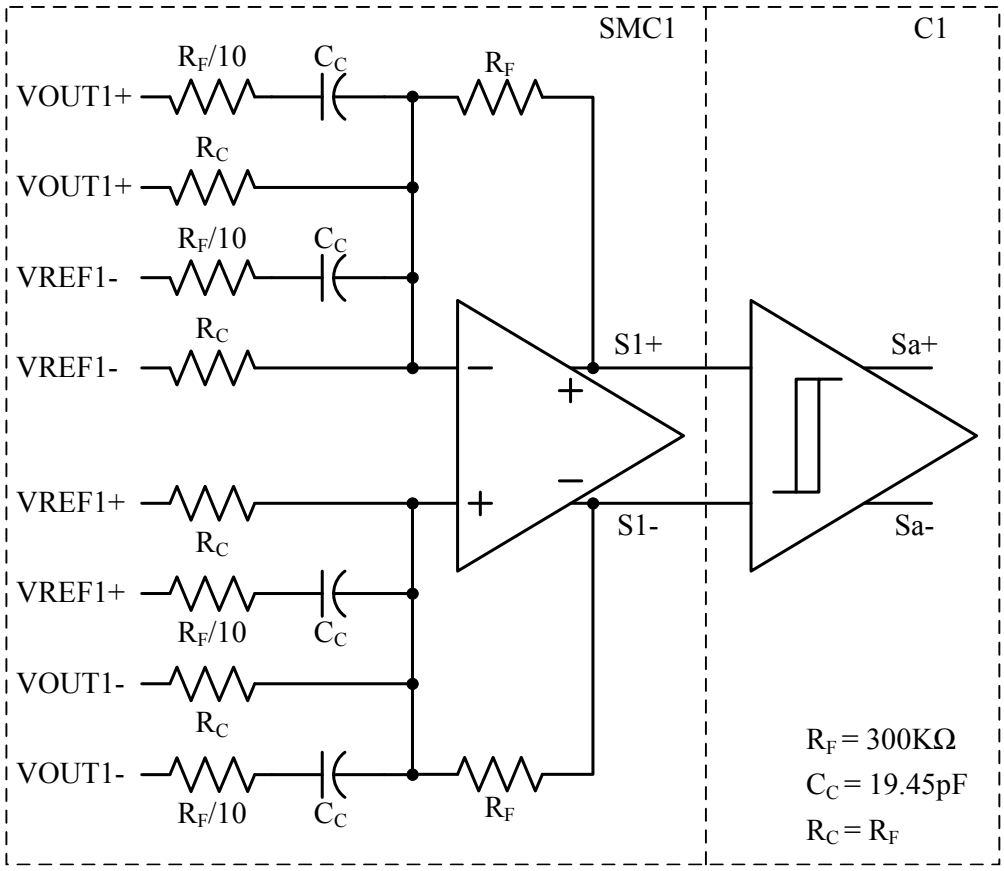


Fig. 115. Sliding mode controller for regulation of V_{OUT1} in proposed voltage converter

(SMC_1) is designated the master subsystem and the second sliding mode controller (SMC_2) its slave counterpart.

The implementation of this synchronization method has been divided in two sections; analog section and digital section. The analog section of the synchronization consists on adding an extra branch to the second controller (SMC_2), using the output signal of the first controller (S_1), as shown in Fig. 116. The objective of that additional branch is to coordinate both controllers, i.e. when the output signal of the first controller (S_1) makes the comparator (C_1) to switch from ground to V_{DD}, the second comparator (C_2) must also

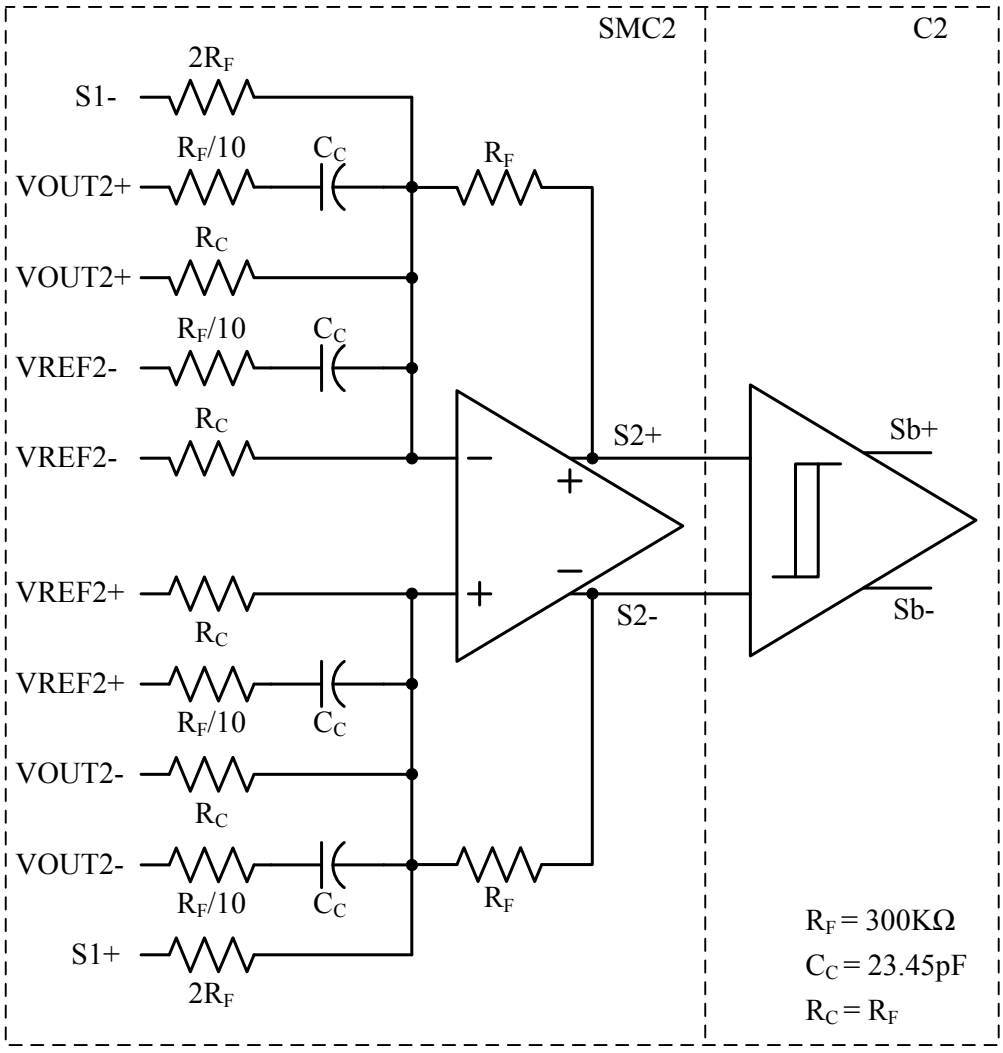


Fig. 116. Sliding mode controller for regulation of V_{OUT2} in proposed voltage converter

change its state at the same time. Since the intention of the output signal of the first controller (S_1) in the second controller (SMC_2) is just for synchronization purposes, and is not part of the controller, a small gain of 0.5 is used to avoid stability issues.

On the other hand, the smaller hysteresis window in the second comparator (C_2), as shown before in Table XXI, helps to the second controller (SMC_2) to detect the change of

state coming in the first controller (SMC_1) and switch states just a few moments before the master subsystem. The digital section of the synchronization circuitry is explained in the next section

2. Digital Logic Circuit

The digital logic has two main objectives; the first one is the synchronization of the binary signals coming from the comparators (C_1 and C_2), and the second goal is the combination of the four digital signals (S_A and S_B) in order to generate the three switching signals in Fig. 102 to properly operate the dual-buck voltage regulator. Figure 117 shows the complete digital logic circuitry.

Figure 118 illustrate the timing diagram of the three gate control signals, their subintervals of operation, and their non-overlapping synchronization. As mentioned before, the second comparator (C_2) switches between states earlier than the first comparator (C_1), therefore, the digital synchronization of the controller consist on the alignment of the rising

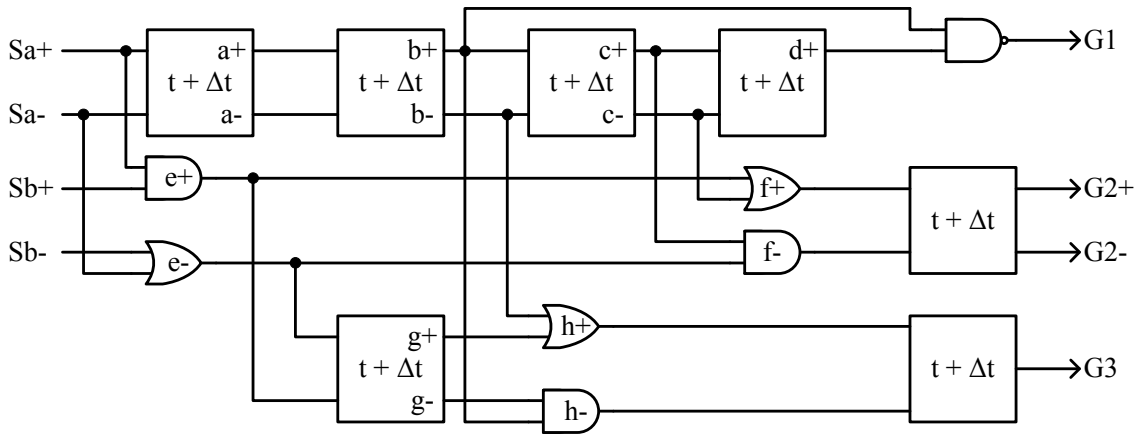


Fig. 117. Digital circuitry used for synchronization of gate signals G_1, G_2, and G_3

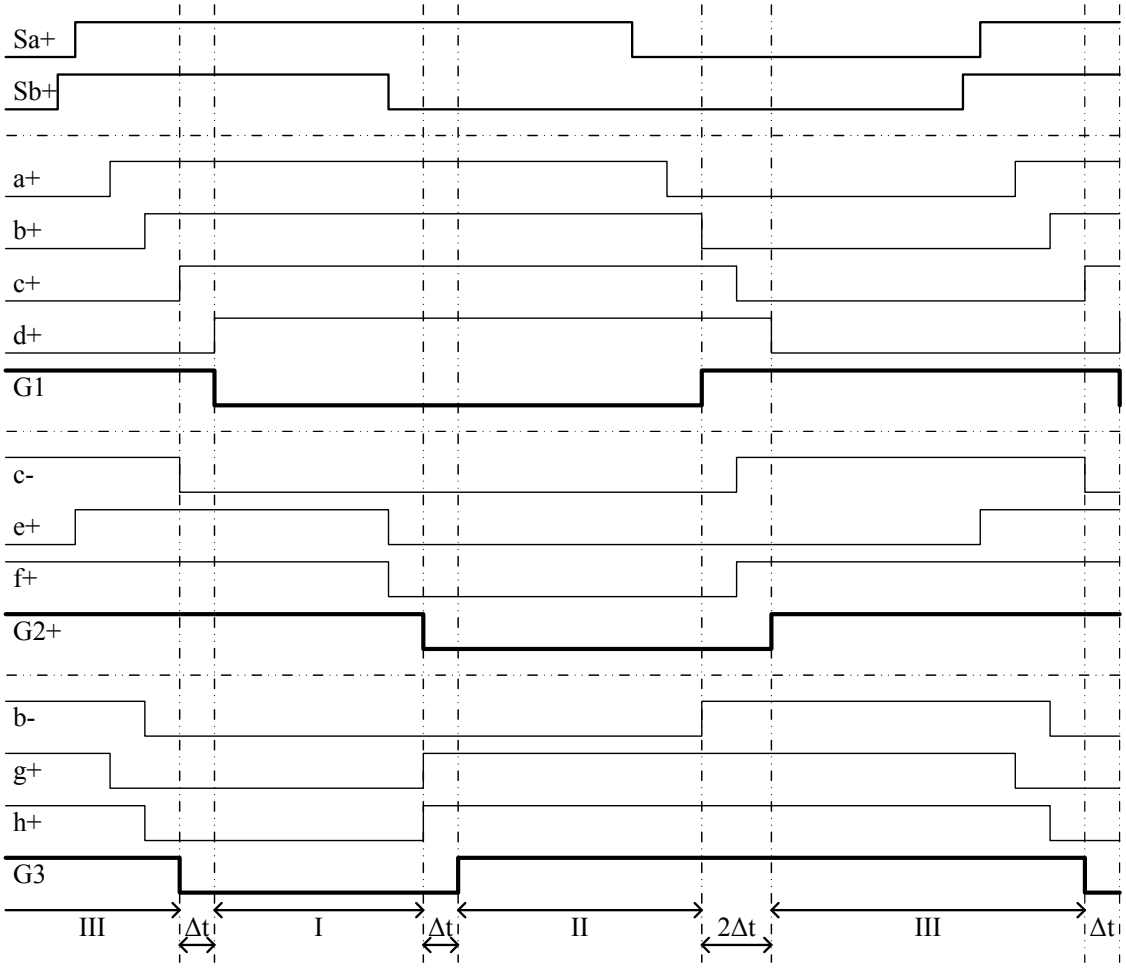


Fig. 118. Timing waveforms of Digital circuitry used for synchronization of gate signals G_1, G_2, and G_3

edge of the slave subsystem with the master controller using the AND/OR logic gates e±. This synchronization scheme forces the slave circuit to track the phases of the master controller as well as its switching frequency.

The binary signals (S_A and S_B) determine the duty cycle of V_{OUT1} and V_{OUT2}, respectively. The duration of control signal G_1 corresponds to the duty cycle of V_{OUT1}, hence, the operation of the signal can be treated as independent of all the other binary

signals, requiring only some timing adjustment for non-overlapping operation. The signals a±, b±, c± and d+ correspond to the delayed versions of the binary signal S_A, where the block labeled as (t + Δt) is a delay circuit implemented by a chain of eight inverters which retards the signal around 15 ns. The last NAND gate, in Fig. 117, inverts the signal G_1 because the top switch T_3, in the dual-output buck converter, is built using a PMOS transistor.

The time diagram in Fig. 118 shows that signal G_1 is valid for subinterval I and subinterval II as established previously in Fig. 102. Control signal G_2 must be high during subinterval I and subinterval III and low in subinterval II. Similarly, control signal G_3 is high during subinterval II and subinterval III and it is low during subinterval I. The generation of the proper functions can be realized by a logic function OR between the complementary binary signal S_A and the differential signal $S_{B\pm}$.

The schematic diagrams of the logic gates used to implement the digital logic circuit are illustrated in Fig. 119, and the size of the transistors in the circuits are listed in Table XXII.

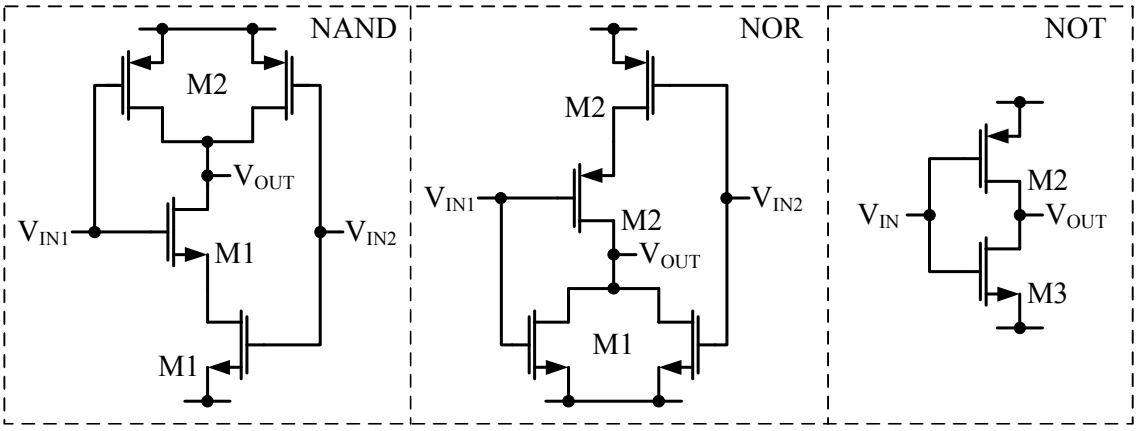


Fig. 119. Schematic diagram of the logic gates used to implement the digital logic circuit

Table XXII. Transistor sizes used to implement the digital logic circuit

Transistor	Width (μm)	Length (μm)	Multiplicity
M1	4.35	0.6	2
M2	13.50	0.6	2
M3	13.50	0.6	2

3. Output Power Stage

The function of the output power stage is to provide enough driving capability to the digital gate control signals G_1, G_2, and G_3, generated by the digital logic circuit. The output power stage, as shown in Fig. 120, is divided into three sections; the output buffers,

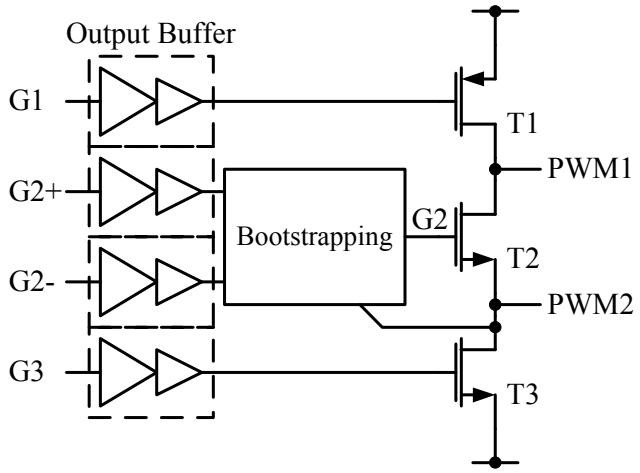


Fig. 120. Block diagram of the output power stage in the dual-output buck voltage regulator

the bootstrapping circuit to generate the voltages necessaries for operation of the middle switch, and the output switches T_1, T_2, and T_3.

a. Output Buffer Stage and Output Switches

The design of the output buffer must minimize the dynamic power dissipation without jeopardizing the propagation delay, as well as reducing the short-circuit current during transitions, and minimizing the CMOS on-resistance (R_{on}). The design of the tapering factor (T) and the number of inverters (N) [45], and the width (W) and length (L) of the transistors [44] is calculated by assuming that the dual-output buck regulator would be working on a medium-load configuration most of the time. Table XXIII summarizes the

Table XXIII. Characteristics of the output buffer stage and output switches

Parameter	Value
W_{T1}	30.6 μm
L_{T1}	0.6 μm
W_{T1} multiplicity	1800
W_{T2}, W_{T3}	30.6 μm
L_{T2}, L_{T3}	0.6 μm
W_{T2}, W_{T3} multiplicity	600
T	24
N	4
R	3
R_{on}	307 mΩ

design parameters of the output buffer stage and the output switches for the dual-output buck voltage regulator. Hence, if the ratio (R) between the electron and hole mobility is approximately three, then it is possible to calculate the values of the output transistors as well as the transistors in the output buffer stage.

b. Bootstrapping Circuit

Power switch T_2 in Fig. 120 requires the use of a bootstrapping circuit in order to turn it on and off completely. Such bootstrapping circuit must obey device reliability considerations of the technology [88]. The schematic diagram of the bootstrapping circuit employed in the dual-output buck voltage converter is shown in Fig. 121. The operation of the bootstrapping

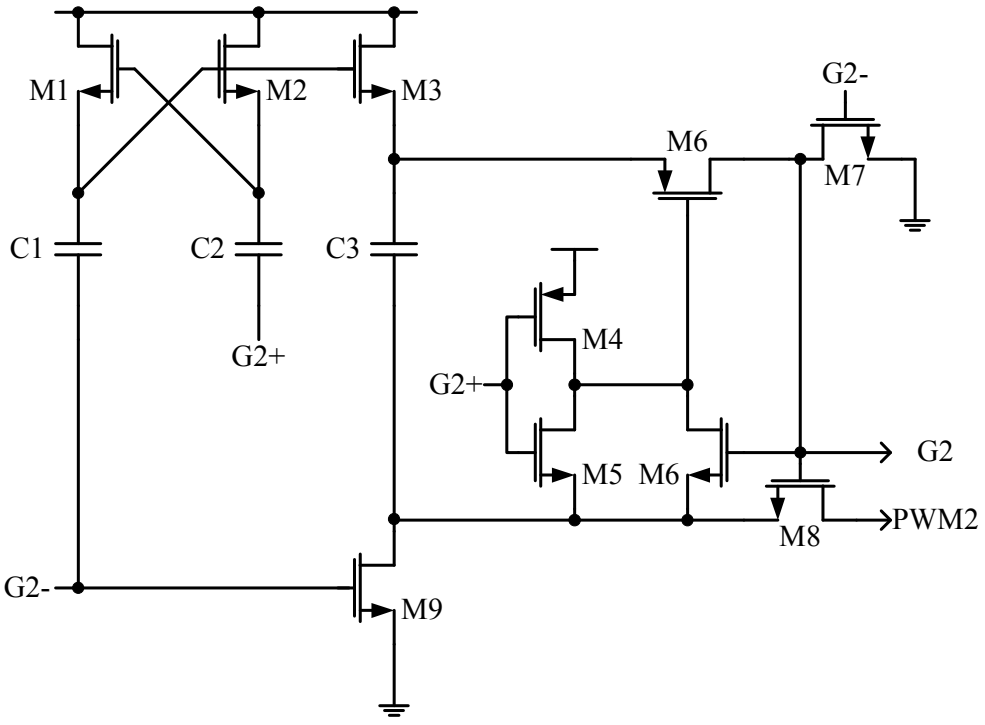


Fig. 121. Schematic diagram of the bootstrapping circuit

circuit is as follows. Basically, transistors M1 and M2, and capacitors C1 and C2, work as a clock multiplier to charge capacitor C3 by enabling transistor M3 [88]. Since capacitor C3 must be large enough to supply the charge to the power switch T_2, it has been implemented as an off-chip element with value of 1 nF. Capacitors C1 and C2 are integrated on-chip with value of 8 pF. The width of all PMOS transistors is 20 μm and width of all NMOS transistors is 60 μm. All transistors use the minimum technology length of 0.6 μm with a multiplicity factor of 16. The digital signals G2$\pm$ generated by the digital circuit logic act as the clocking signals. Outputs G2 and PWM2 are connected to the power switch T_2 gate and source respectively.

E. Experimental Results

The proposed sliding mode controller for the dual-output buck voltage regulator was fabricated using 0.5 μm CMOS standard technology thanks to the MOSIS educational program. The results of the experimental measurements are shown in this section.

The dual-output buck voltage regulator micrograph is shown in Fig. 122, where all the main building blocks are highlighted. It can be appreciated the blocks corresponding to the analog controller, i.e. single-ended to fully-differential (SE2FD) converters, sliding mode controllers (SMC_1 and SMC_2), and decision circuits (C_1 and C_2), the digital logic circuitry, and the output power stage, i.e. the output buffers (OB), the bootstrapping (BS) circuit, and the output switches T_1, T_2, and T_3.

Figure 123 shows the power and area distribution in the dual-output buck voltage regulator. Note that most of the power consumption is burned by the four single-ended to fully-differential converters, even though they are not part of the controller. Also, notice that the second comparator C_2 consumes more power than the first comparator C_1 because its hysteresis window is smaller. In the case of the area distribution, it can be appreciated

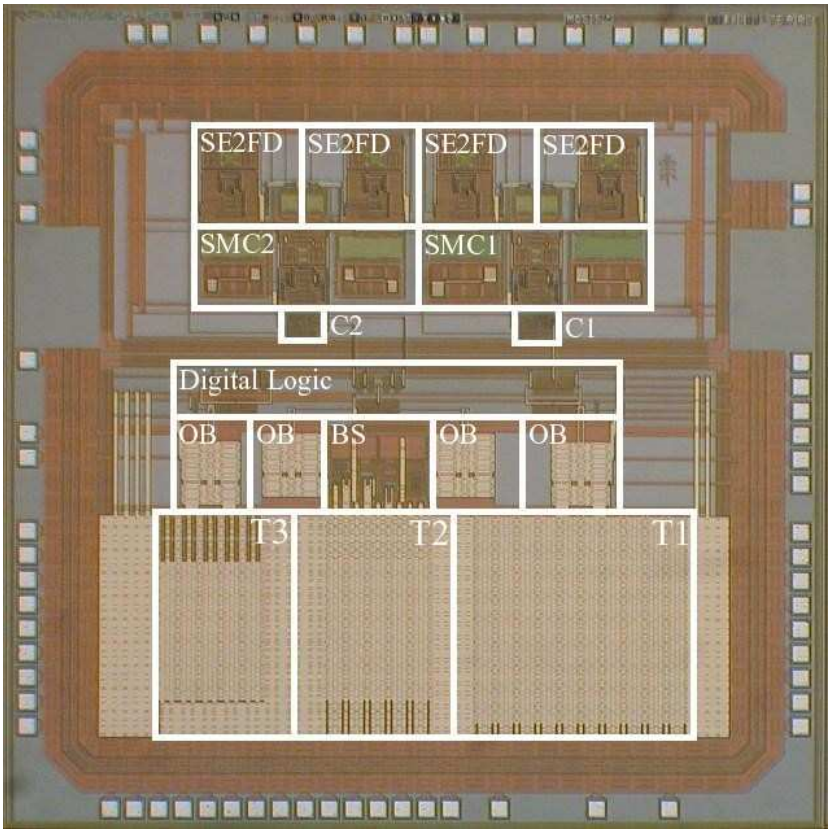


Fig. 122. Dual-output buck voltage regulator micrograph

that most of the area is occupied by the output buffers and output switches. On the other hand, it is worth to mention that the implementation of the bootstrapping circuit does not represent an overhead to the design of the dual-output buck voltage converter.

Figure 124 shows the phase portrait of the implemented switching functions, expressed in equations (6.10) and (6.11), when the dual-buck converter moves from zero initial conditions to the sliding equilibrium points of (1.2 V, 50 mA) and (0.9 V, 25 mA) for V_{OUT1} and V_{OUT2}, respectively. The system starts at its initial condition (A), then it moves, i.e. reaching mode (B), until it hits the sliding surfaces (C). Once in the sliding surfaces, the dual-output buck voltage converter slides to the sliding equilibrium points (D).

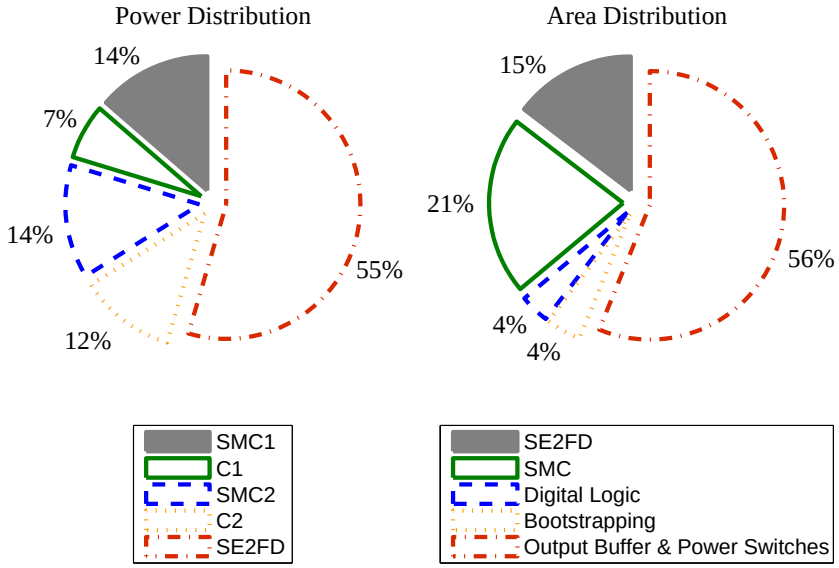


Fig. 123. Power consumption and area distribution in the dual-output buck voltage regulator

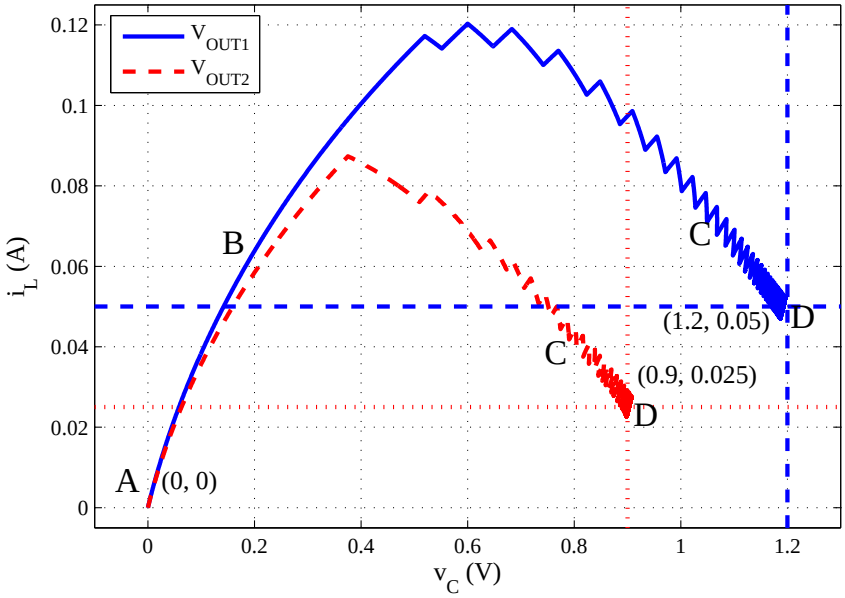


Fig. 124. Phase portrait of sliding mode in the dual-output buck voltage converter

The experimental results of the dual-output buck voltage regulator can be divided into two main sections; the steady-state operation, and the transient operation.

1. Testing of Steady-State Operation

Testing of steady-state operation of the dual-output buck voltage regulator includes the verification of the proper operation of the control signals, and the measurement of the converter efficiency under different load conditions.

a. Control Signals

The measured control signals G_1, G_2, and G_3 to operate the output switches T_1, T_2, and T_3 are shown in Fig. 125. Notice that they follow the same pattern as the operational signals sketched previously in Fig. 102. Moreover, observe that the switching frequency is approximately 506 kHz, which deviates from the theoretical switching frequency, i.e. 500 kHz, by less than 1.5%.

Figure 126 shows the pulse-width modulated signals PWM1 and PWM2. The duty cycle of the converters diverges from the theoretical calculation due to the non-ideal elements in the system, i.e. non-zero on-resistance in the switches, traces and vias resistances, output inductors finite resistances, etc. The measured duty cycle for V_{OUT1} is around 71%, and approximate 55% for V_{OUT2}, which represent a deviation around 10% from the theoretical values listed in Table XV.

Figure 127 depicts the voltage waveforms in the terminals of the bootstrapping capacitor C_3. Waveform CB- is taken in the negative terminal of the capacitor and waveform CB+ in the positive terminal. Waveform CB+ represents the bootstrapped signal that is applied to the gate of power transistor T_2. Notice that the voltage is boosted up to 3.6 V, i.e. $2V_{DD}$.

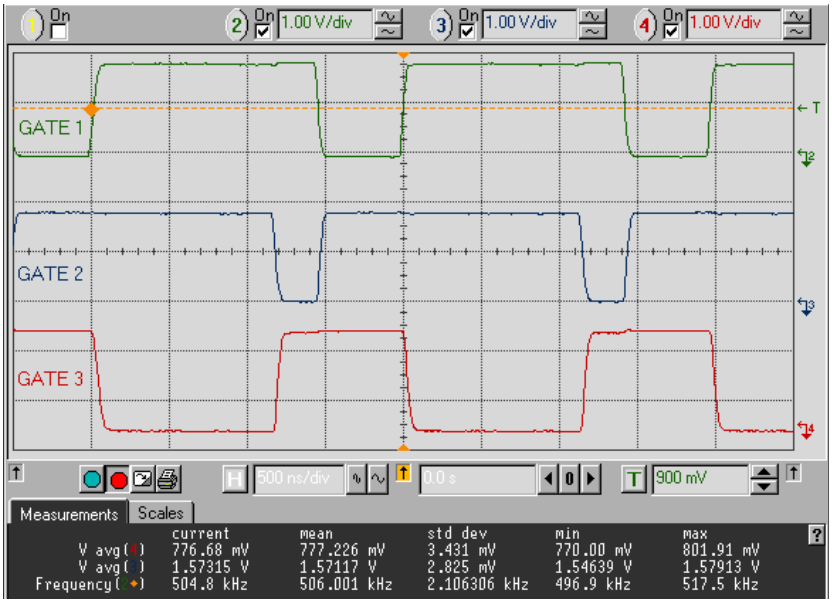


Fig. 125. Measured control signals G_1, G_2, and G_3 to operate the output switches T_1, T_2, and T_3 in the dual-output buck converter

Fig. 126. Measured pulse-width modulated signals in the dual-output buck voltage converter

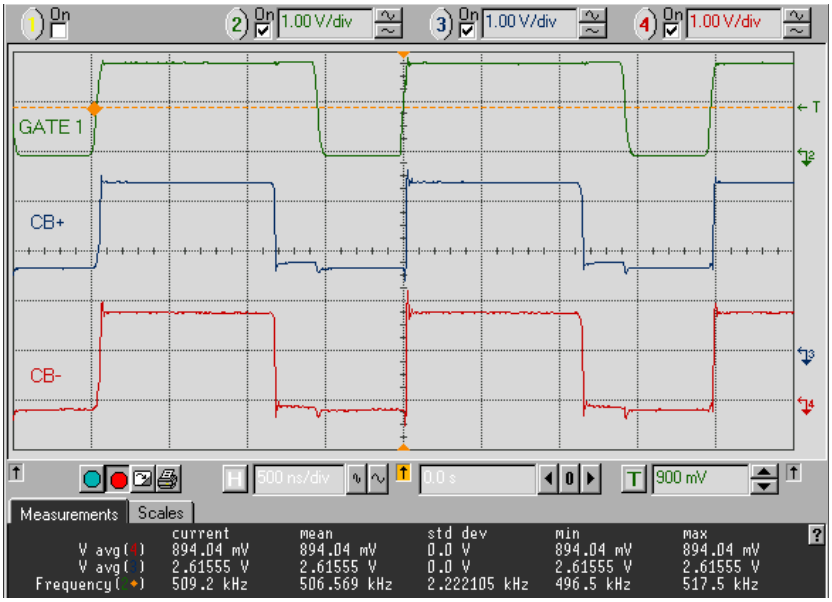


Fig. 127. Measured waveforms across bootstrapped capacitor C_3

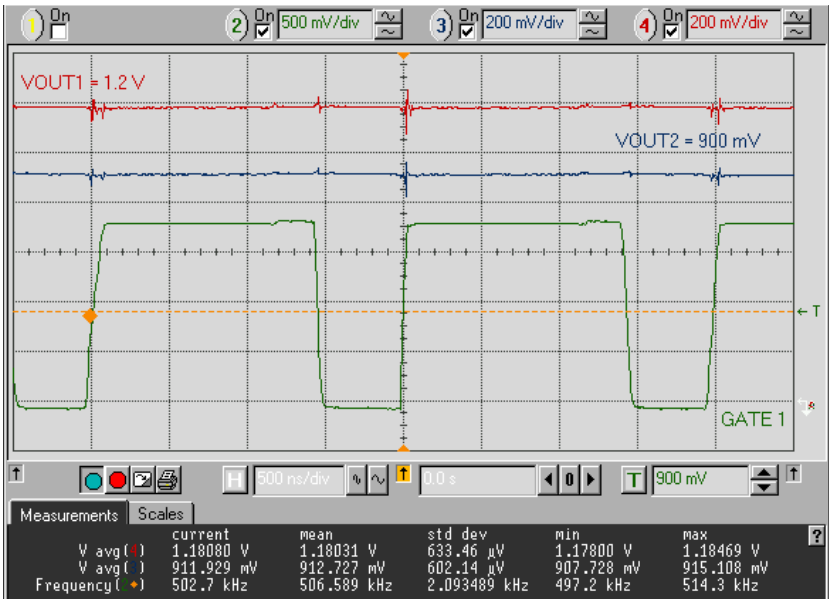


Fig. 128. Measured output voltages in the dual-output buck voltage regulator

Finally, Fig. 128 shows the output voltages in the regulator. Average voltage for V_{OUT1} is 1.18 V and mean voltage for V_{OUT2} is 0.91 V. The variations from the desired output voltages in the first and second outputs are only 20 mV and 10 mV, respectively.

b. Power Efficiency

The efficiency measurements in the proposed regulator are very important due to the switching nature of the converter. The set of three load configurations used for efficiency measurements is shown in Fig. 129, and the values of such loads are detailed in Table XXIV. In case I, the load current is increased gradually from I_{MIN} to I_{MAX} in both outputs. In case II, the value of I_{OUT1} is incremented from I_{MIN} to I_{MAX} while I_{OUT2} is kept fixed at light load (LL), medium load (ML), and hight load (HL). In case III, the load I_{OUT1} is kept constant, at light load (LL), medium load (ML) and hight load (HL), while varying the output current I_{OUT2} from I_{MIN} to I_{MAX}.

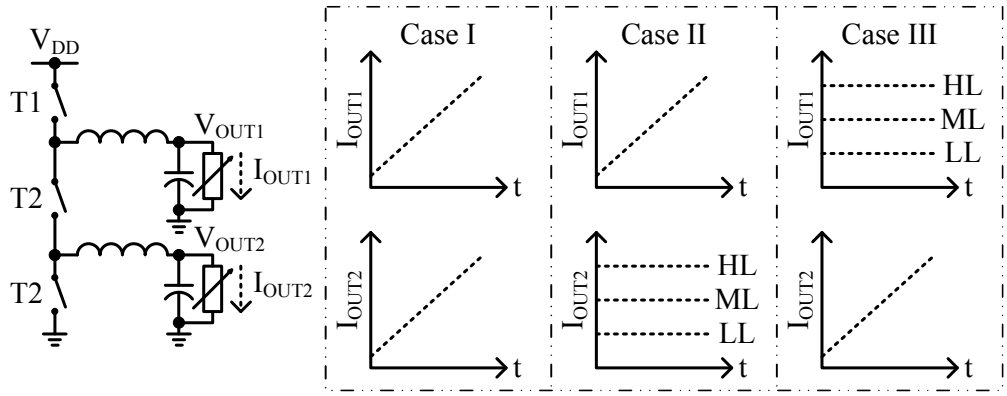


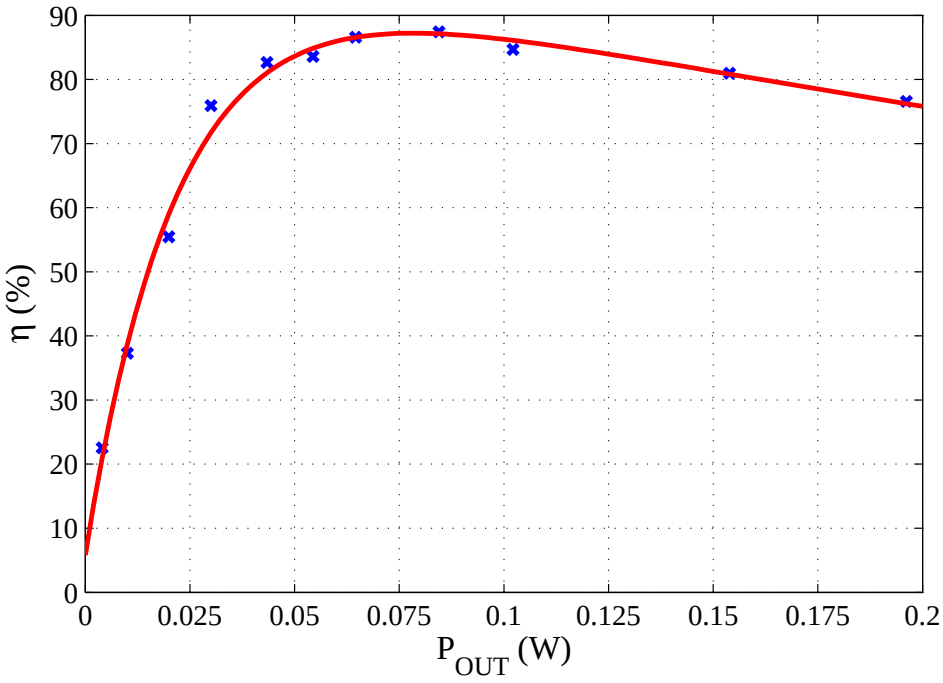
Fig. 129. Load configurations for efficiency measurements in the dual-output buck voltage regulator

Table XXIV. Output load currents for efficiency measurements in the dual-output buck voltage regulator

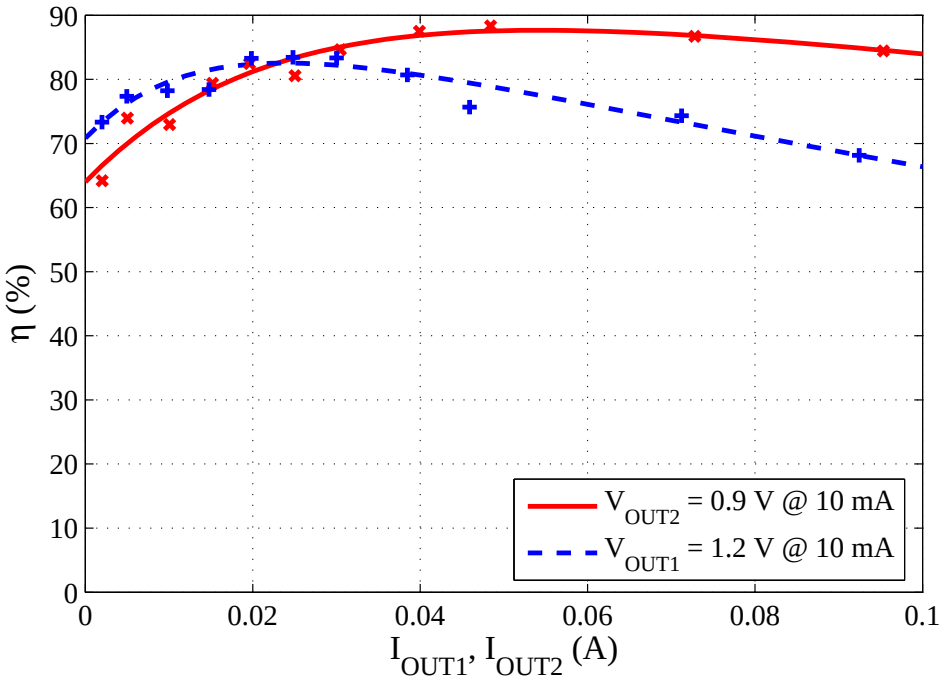
Load		Value
Minimum load	(I_{MIN})	2 mA
Light load	(LL)	10 mA
Medium load	(ML)	30 mA
High load	(HL)	75 mA
Maximum load	(I_{MAX})	100 mA

The efficiency measurements of the dual-output buck voltage regulator are illustrated in Fig. 130, Fig. 131, and Fig. 132. Figure 130(a) shows the efficiency measurement for case I when both output currents are increased simultaneously. Maximum efficiency of the dual-output buck converter for this case is 88%.

Figure 130(b) shows the case when one of the outputs is kept at light load, i.e. 10 mA, while the other output is swept from I_{MIN} to I_{MAX}. Note that the minimum power efficiency of the proposed converter is 65%. Fig. 131(a) illustrates the case where on of the output is fixed at medium load, i.e. 30 mA, while the other is increased from I_{MIN} to I_{MAX}. The minimum power efficiency for this mode of operation is around 75%. On the other hand, Fig. 131(b) depicts the case when one of the outputs is maintained at high load, i.e. 75 mA while the other output is swept from I_{MIN} to I_{MAX}. Observe that the maximum efficiency occurs when the current in the second output is much lower than the high load condition in the first output.

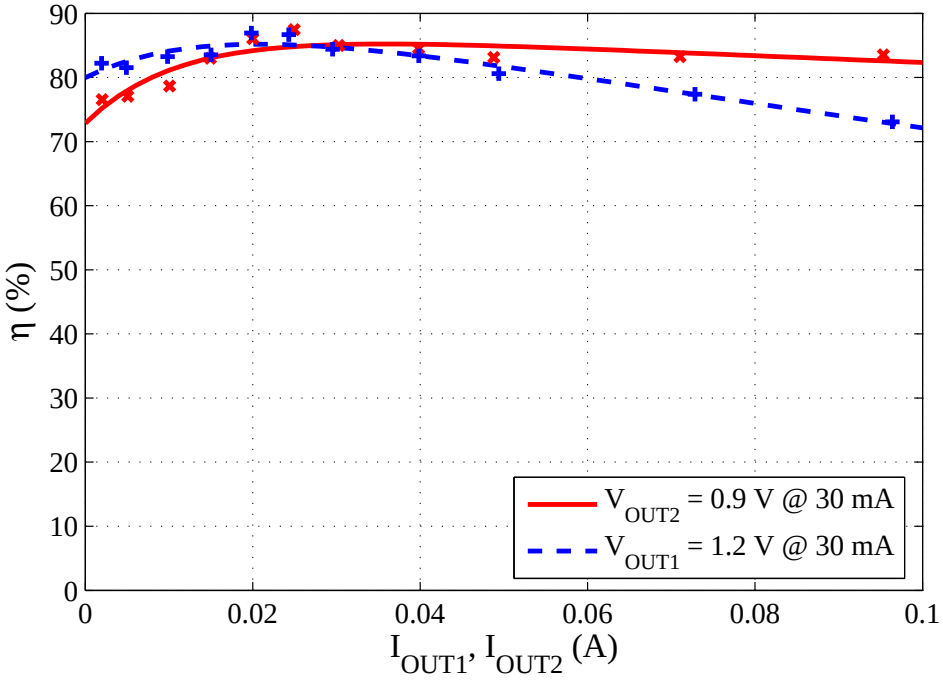


(a)

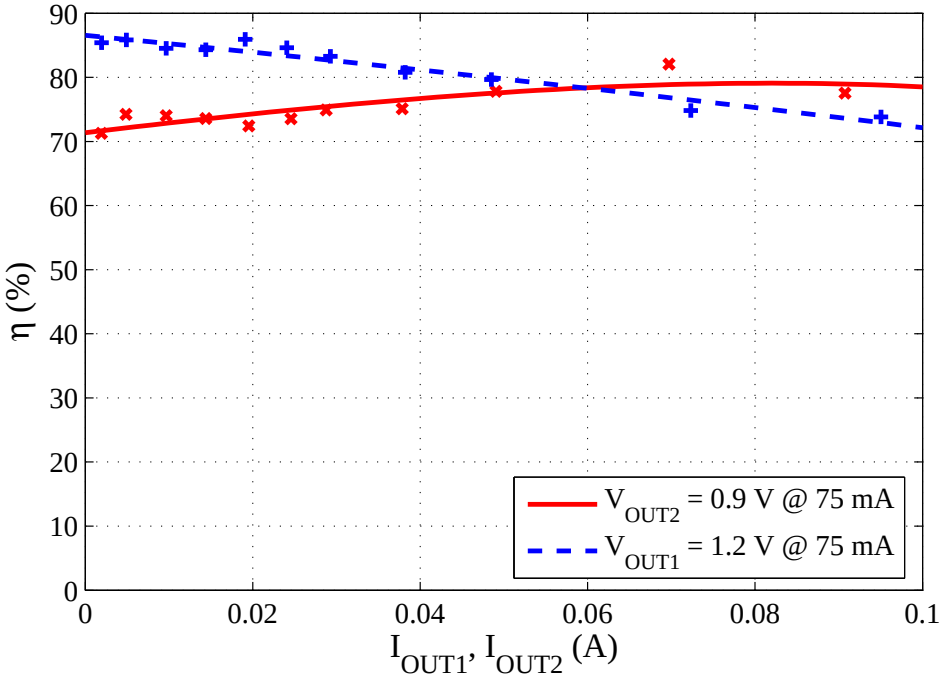


(b)

Fig. 130. Power efficiency measurements of the dual-output buck voltage regulator for (a) Equal increment in output currents and (b) Light load condition

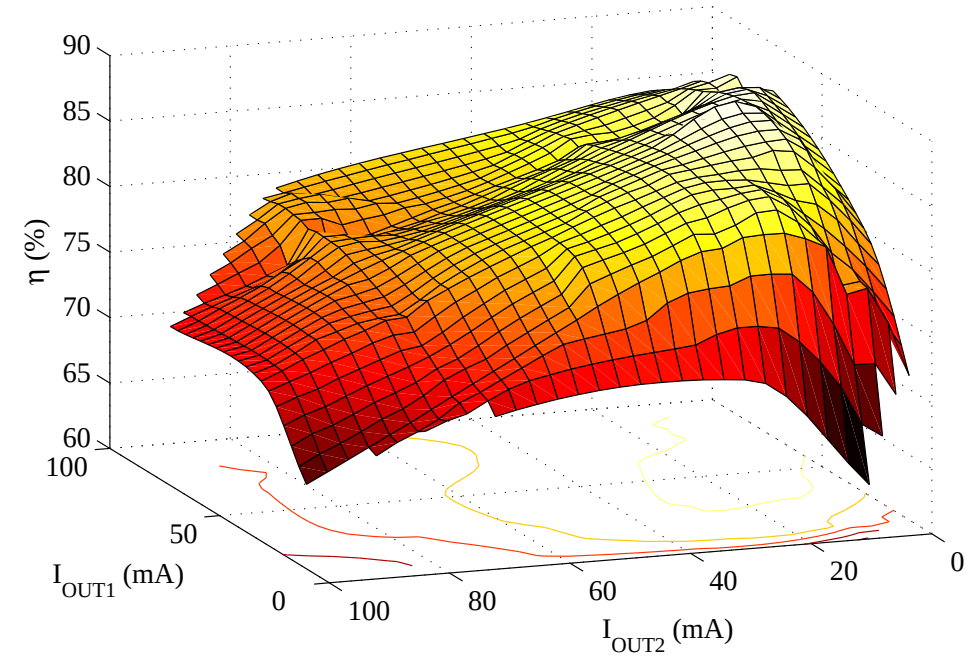


(a)

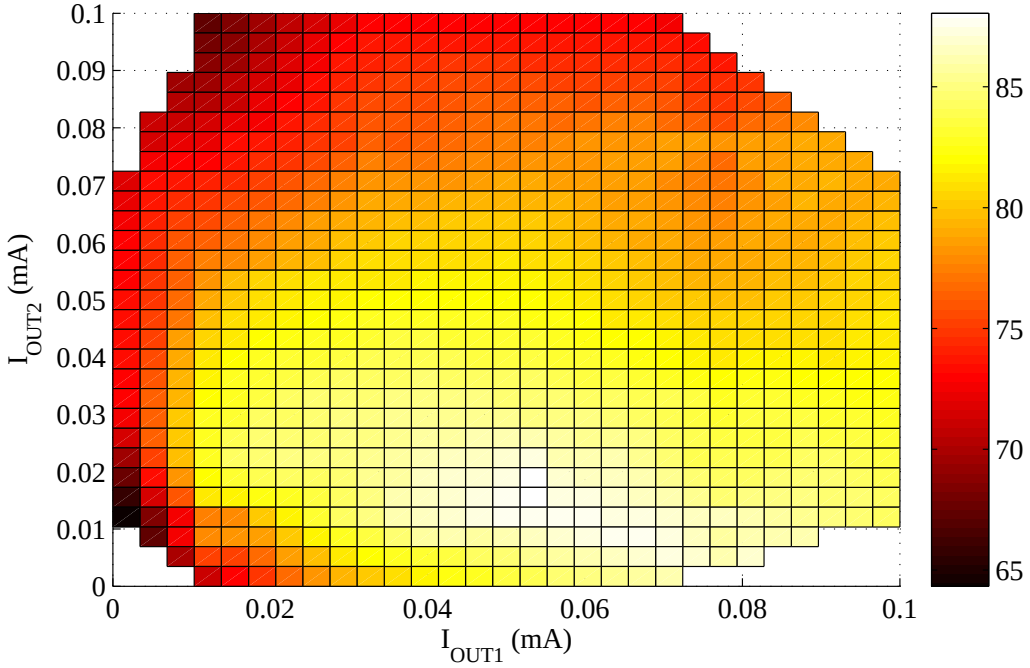


(b)

Fig. 131. Power efficiency measurements of the dual-output buck voltage regulator for (a) Medium load condition and (b) High load condition



(a)



(b)

Fig. 132. (a) Power efficiency measurements of the dual-output buck voltage versus both output currents and (b) Top view

It can be noticed that the efficiency of the dual-output buck voltage converter is always higher when the output V_{OUT1} drains more current than output V_{OUT2}. In other words, the intersection point of efficiency plots occurs around the point where the fixed output current in one of the outputs is equal to the value of the current being swept in the other output.

Finally, Fig. 132 shows the power efficiency versus both output currents (I_{OUT1} and I_{OUT2}). Figure 132(a) is a three-dimensional plot of the power efficiency, and Fig. 132(b) shows a top view of the same plot. Note that the efficiency is maximum when the output voltage V_{OUT1} is set to medium load condition and the output voltage is V_{OUT2} is draining low current.

2. Testing of Transient Operation

The second section of measurements is the verification of the transient response in the dual-output buck voltage regulator. Since the outputs of the converter are related, because they share a common current path, the transient response to different load conditions must be reliable and fast.

The first set of load configurations for the transient test of the dual-output buck voltage regulator is shown in Fig. 133 and the output current details are listed in Table XXV. The objective of the first set of load configurations for transient response is to verify the effect of having a step current in one output while keeping a constant current, either light load (LL), medium load (ML), or high load (HL), in the other output.

Two extreme cases of measured results using the first set of load configurations are presented in Fig. 134. Figure 134(a) shows the case when the first output voltage V_{OUT1} presents a step of 25 mA while the second output voltage V_{OUT2} is at high load configuration, i.e. 60 mA. On the other hand, Fig. 134(b) illustrates the case when the first output voltage V_{OUT1} is kept at high load (60 mA) while a 25 mA step current is applied to the second output voltage V_{OUT2}. It can be noticed that the transient response of the dual-

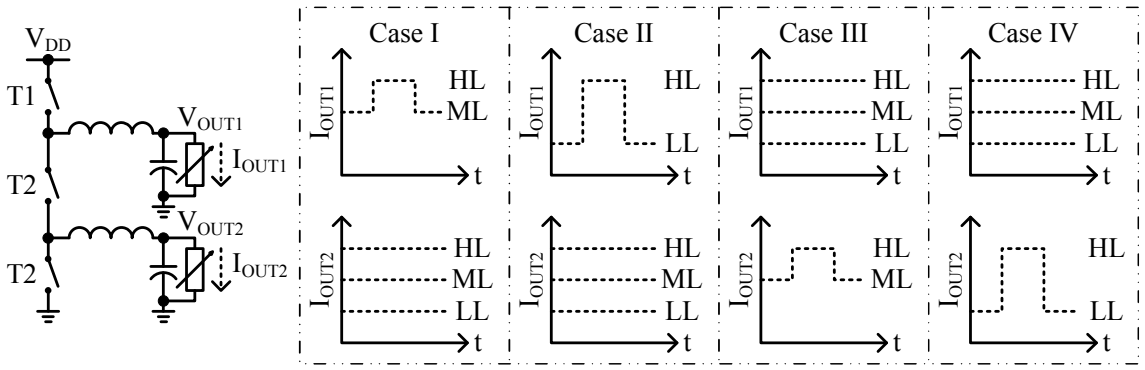


Fig. 133. First set of load configurations for transient measurements

output buck voltage converter is affected more with a current step in the second output voltage V_{OUT2} than a current step in the first output voltage V_{OUT1}. This phenomenon was expected because the path of the output current is shared by both outputs but controlled only by the gate signal G_1.

Table XXV. Output current configurations for transient measurements

Load		Value
Zero load	(ZL)	0 mA
Light load	(LL)	10 mA
Medium load	(ML)	35 mA
High load	(HL)	60 mA

(a)

(b)

Fig. 134. Transient measurements with first set of load configurations (a) 25 mA current step is applied to I_{OUT1} while I_{OUT2} is fixed at 60 mA and (b) I_{OUT1} is fixed at 60 mA while 25 mA current step is applied I_{OUT2}

The second set of load configurations is shown in Fig. 135. In this case, the same current steps of 25 mA and 50 mA, are applied to one of the outputs in the converter but the other output is not loaded at all, i.e. is configured at zero load (ZL) condition.

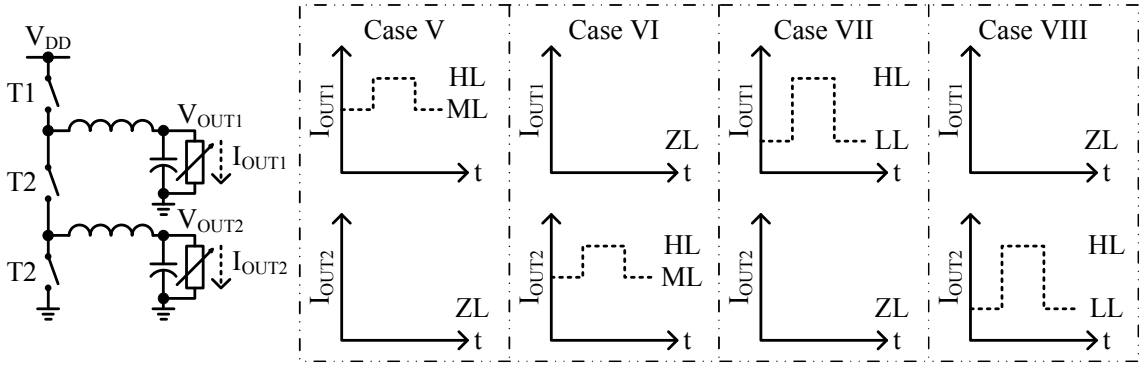
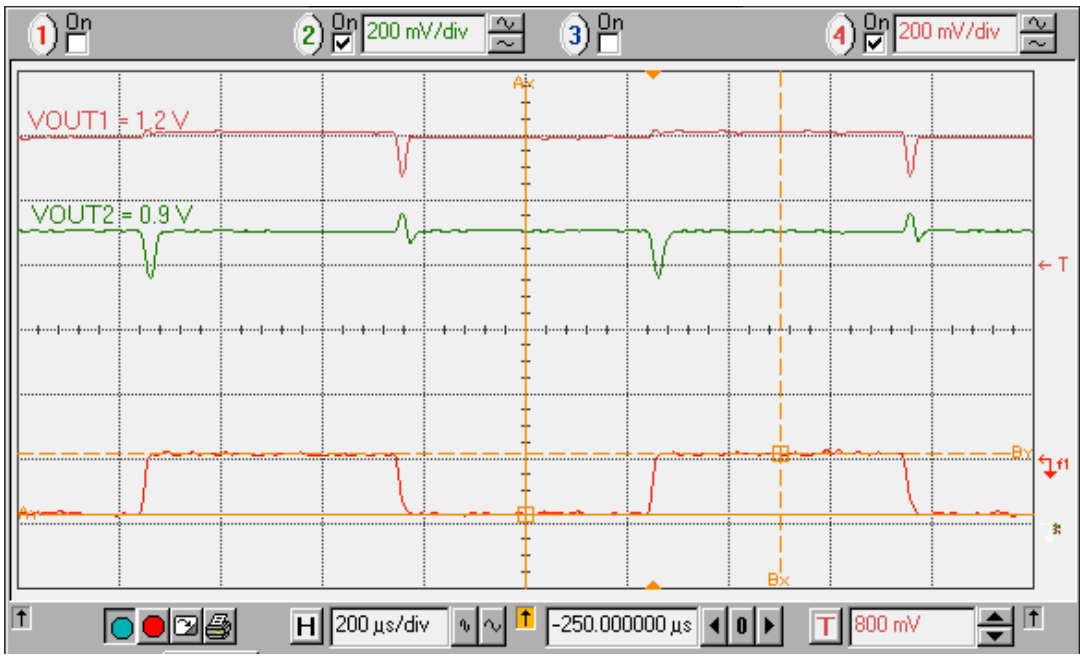
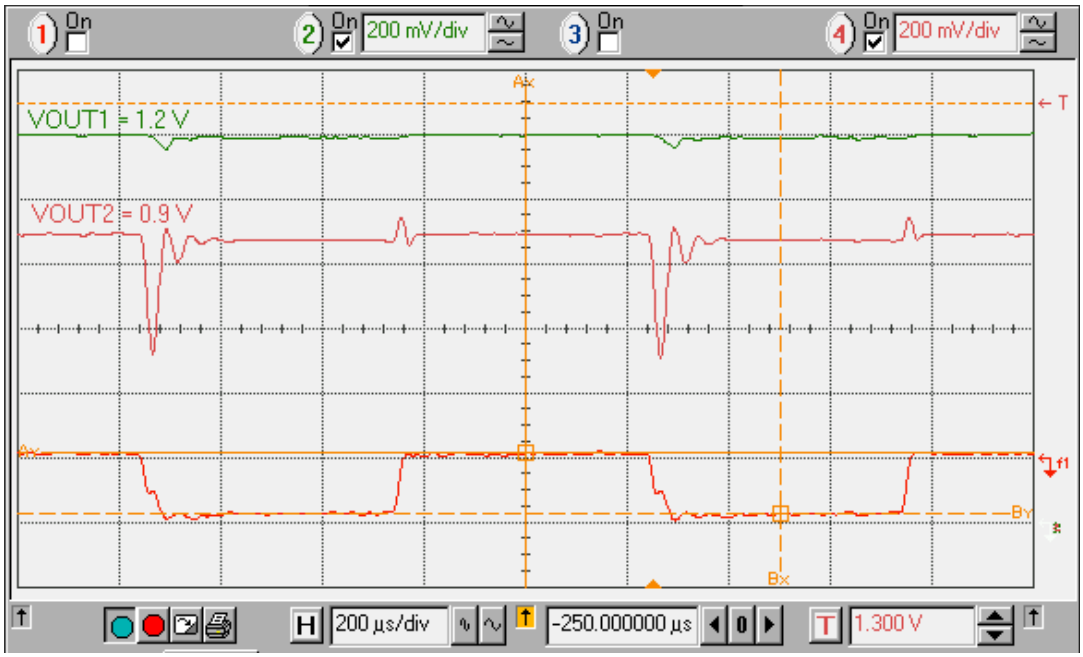


Fig. 135. Second set of load configurations for transient measurements

The experimental results, shown in Fig. 136(a), correspond to 50 mA step current in the first output voltage V_{OUT1} and zero load (ZL) in the second output voltage V_{OUT2}, and Fig. 136(b) is the response of the dual-output buck voltage regulator when a 50 mA current step is applied to the second output voltage V_{OUT2} while the first output voltage V_{OUT1} is kept at zero load (ZL) condition. As in the previous case, the transient response of the converter is worse when the step current is applied to the second output voltage V_{OUT2}. For this particular case, and even though the system recovers fast, the transient response presents an under peak voltage of approximately 300 mV when the step is applied.



(a)



(b)

Fig. 136. Transient measurements with second set of load configurations (a) 50 mA current step is applied to I_{OUT1} while I_{OUT2} is fixed at zero load condition and (b) I_{OUT1} is fixed at zero load condition while 50 mA current step is applied I_{OUT2}

The last set of transients measurements is shown in Fig. 137. The objective of such configurations is to evaluate the response of the dual-output buck voltage converter when steps currents are applied simultaneously to both output voltages. Figure 138 shows the experimental results of the third set of load configurations. It can be appreciated that the system is stable and quickly converges to the reference voltages, as expected. However, as shown in Fig. 138(b), the system presents more ringing when the 50 mA step is applied to the output voltages.

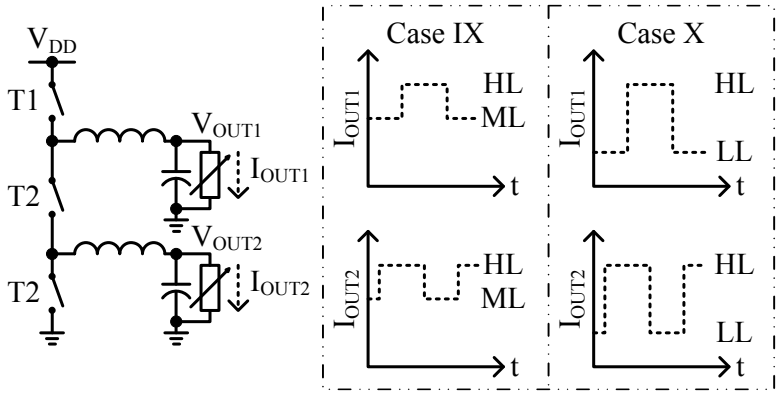
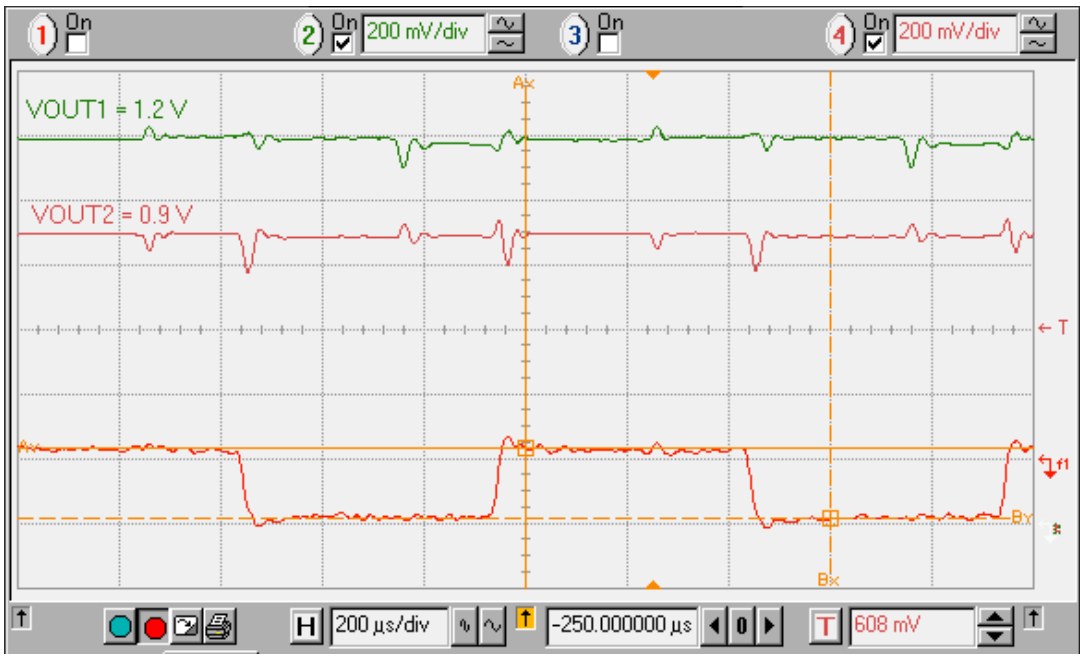


Fig. 137. Third set of load configurations for transient measurements

Through all the experimental results, it has been observed that the dual-output buck voltage converter performs better when $I_{OUT1} \geq I_{OUT2}$. This behavior was expected since the branch connected to the power supply is shared by the two output nodes. Therefore, when the second output voltage V_{OUT2} needs to supply large amount of current instantaneously, the current path may be disconnected because it is controlled by the duty cycle of the first output voltage V_{OUT1}.



(a)

(b)

Fig. 138. Transient measurements with third set of load configurations (a) 25 mA out-of-phase current steps are applied simultaneously to I_{OUT1} and I_{OUT2} and (b) 50 mA out-of-phase current steps are applied simultaneously to I_{OUT1} and I_{OUT2}

The proposed sliding mode controller for the dual-output buck voltage regulator present better efficiency and transient behavior when the output current in the first output voltage V_{OUT1} is higher than the output current in V_{OUT2}.

Table XXVI summarizes the overall characteristics of the proposed converter, and compares them versus other low-voltage dual-output buck voltage regulators. The voltage

Table XXVI. Comparison of low-voltage dual-output buck voltage regulators

Design	[85]	[86]	This work
Voltage supply	3.0 V	3.6 V	1.8 V
V_{OUT1}	2.0 V	3.3 V	1.2 V
V_{OUT2}	1.0 V	1.8 V	0.9 V
I_{MAX}	55 mA	200 mA	200 mA
Efficiency	89%	85%	88%
Inductors	440 μH, 440 μH	22 μH	82 μH, 90 μH
Capacitors	0.22 μF, 0.22 μF	35 μF, 35 μF	0.83 μF, 1.11 μF
Switches	4	4	3
Output voltage ripple	40 mV, 40 mV	31 mV, 24 mV	12 mV, 9 mV
Switching frequency	500 kHz	1 MHz	500 kHz
Static current	200.8 μA	-	104.8 μA
Static power	411.6 μW	-	188.6 μW
Silicon area	4.57 mm^2	2.43 mm^2	2.19 mm^2
Process	-	0.35 μm CMOS	0.5 μm CMOS

regulator presented in this chapter can deliver the same amount of output current than previous works but consuming less static power. Additionally, the reduction of one switch with respect to conventional architectures, saves silicon area if the output stage is optimized for medium load applications. Moreover, the proposed architecture can also bring printed circuit board space benefits because only one input filter is needed, as compared to the conventional solution where two input filters are required.

F. Conclusion

The design, implementation, and testing of a dual-output buck voltage regulator, along with the challenges of the controller realization, and the proposed solution have been presented. An IC prototype of the proposed voltage regulator was fabricated using 0.5 μm CMOS technology. The experimental results show consistency with theoretical calculations.

The maximum measured efficiency of the converter is 88%. Evaluation of the converter efficiency when one of the outputs is fixed while the other output is swept has shown better performance when the first output voltage V_{OUT1} delivers more current than the second output voltage V_{OUT2}. Moreover, transient experiments with step output currents of 25 mA and 50 mA have confirmed that the dual-output buck voltage regulator presents better performance when $I_{OUT1} > I_{OUT2}$. The reason of this particular behavior is due to the fact that both outputs nodes share the same current path from the power supply, therefore, the duty cycle of the second output voltage V_{OUT2} is limited by the load conditions of the first output voltage V_{OUT1}.

The converter performs as high as previous dual-output buck voltage converters, in terms of power efficiency and maximum output current, but saves silicon area and static power. The silicon area is saved because the converter employs less switches in the output stage when compared to conventional solutions. Moreover, the proposed converter can

also reduce the number of external components because only one input filter is needed, in contrast to conventional solutions where two input filters are required.

It has been demonstrated that the implementation of a dual-output buck voltage regulator can be feasible, reliable, cheap, and versatile. Specifically, the voltage condition $V_{OUT1} \geq V_{OUT2}$ must be satisfied to properly operate the dual-output buck voltage converter, but the best efficiency and transient performance is obtained when the current condition $I_{OUT1} \geq I_{OUT2}$ is satisfied.

CHAPTER VII

A FULLY-INTEGRATED BUCK VOLTAGE REGULATOR USING STANDARD CMOS TECHNOLOGY

This chapter presents the design and implementation of a fully-integrated buck voltage regulator using standard CMOS technology. The buck converter employs a dual-phase structure to minimize the output current ripple, and to reduce by half the size of passive components. In addition, the controller topology implements a hysteretic architecture, based on sliding mode theory, to avoid the overhead that represents the generation of a dedicated high-frequency reference carrier signal. Furthermore, the traditional external low-pass filter has been fully-integrated by increasing the switching frequency of the converter up to 50 MHz.

The proposed converter is a monolithic solution, based on standard CMOS technology, for integration of passive components on-chip without the need of expensive and complicated post-fabrication processes, hence, providing a versatile, low-cost, and reliable solution for integrated power supplies. The voltage regulator, simulated in 0.18 μm CMOS standard technology, operates with a single voltage supply of 1.8 V, generates an output voltage of 0.9 V, supplies a maximum current of 400 mA, and delivers 55% maximum power efficiency.

A. Introduction

The function of power converter circuits is to provide a regulated energy source to guarantee the proper operation of electronic equipment. They must supply good voltage regulation, fast transient response, as well as high efficiency performance. There are three different types of voltage regulator circuits: linear voltage regulators, switched-capacitor voltage regulators or charge pumps, and switched-inductor voltage regulators, or simply switching

regulators.

Linear voltage regulators are step-down converters based on resistive voltage division, which produce an output voltage lower than the input voltage. They can easily be integrated since they do not need large passive components, however, their efficiency is poor and their current capability is typically low. On the other hand, switched-capacitor voltage regulators can be used to supply an output voltage with different magnitude and/or polarity than the input voltage, but their power efficiency is low, their output regulation is poor, and their current capability is also low. Finally, switched-inductor voltage regulators deliver the highest efficiency and provide much higher current capability. Switching regulators can provide good output voltage regulation with different magnitude and/or polarity than their input voltage. However, they usually need the implementation of bulky external components which limits their full monolithic integration [63].

Figure 139 illustrates a conventional synchronous buck switching regulator [66]. The buck converter is a step-down switching regulator. It consists of a controller, to track the reference input voltage v_{REF}, a comparator, that generates a pulse-width modulated (PWM)

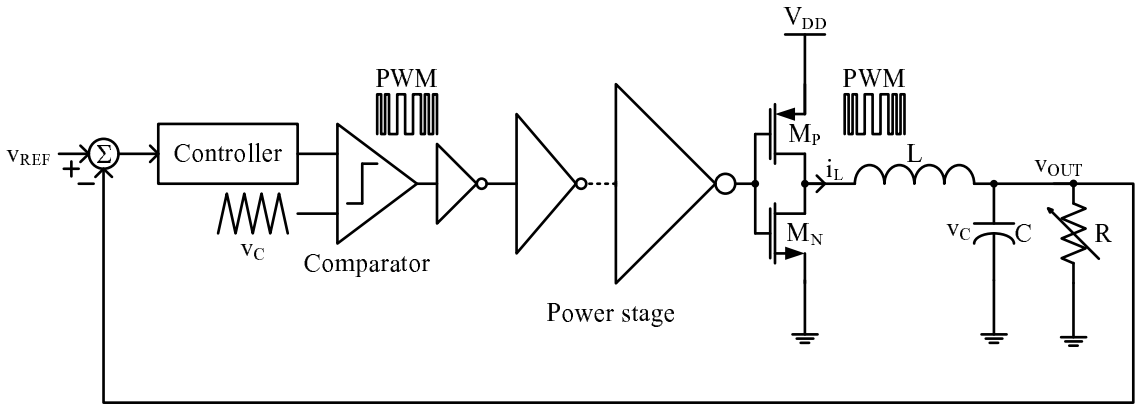


Fig. 139. Simplified diagram of a conventional synchronous buck regulator

signal (whose duty cycle D is proportional to the desired output voltage v_{OUT}), a pair of power switches, M_P and M_N, that provide the driving capability to the load, a passive low-pass filter (LPF) which averages the digital modulated signal, and a load circuitry with variable current consumption.

The traditional implementation of a buck voltage regulator integrates the controller and the power switches, but the low-pass filter is built using external components due to their large size. Typical switching frequencies employed in conventional solutions are in the order of hundreds of kilohertz. At such frequencies, the values of the filter inductor and the filter capacitor, which are inversely proportional to the switching frequency [66], are in the order of μH and μF, respectively. Those values for passive devices restrict the full monolithic integration of the switching regulator.

The fully integration of a switching regulator would provide fewer external components and lower cost, fewer connections and less parasitics, smaller area, and also, it could potentially reduce energy losses. In order to fully-integrate the switching regulator, it is necessary to reduce the filter inductor and capacitor to the order of nH and nF, respectively, by increasing the switching frequency to the order of tens of megahertz [63], [89]–[91].

In this chapter, the design, implementation, and simulation of a fully-integrated buck voltage regulator using standard 0.18μm CMOS technology is presented. The switching regulator operates at 50 MHz switching frequency and delivers 55% maximum power efficiency while supplying a maximum output current of 400 mA and an output voltage of 0.9 V from a 1.8 V single voltage supply.

This chapter is organized as follows. Section B introduces the dual-phase buck voltage regulator architecture, as well as the specifications of the simulated voltage converter. Section C explains the design of the proposed controller. Section D presents the implementation of the main building blocks. Simulation results of the proposed voltage converter are shown in Section E. Finally, Section F discusses future work and provides

suggestions for performance improvement.

B. Buck Voltage Regulator Dual-Phase Architecture

1. Poly-Phase Buck Voltage Converters

The monolithic integration of the passive components in the low-pass filter of the buck voltage regulator requires the increment of the corresponding switching frequency in order to reduce their values to reasonable sizes for integration. In general, the value of the output inductor L and the output capacitor C in Fig. 139, assuming continuous-conduction mode (CCM) operation [66], can be calculated as

$$L = \frac{V_{DD}(1 - D)D}{2\Delta i_L f_s} \tag{7.1}$$

$$C = \frac{\Delta i_L}{8\Delta v_C f_s} \tag{7.2}$$

where D, f_s, Δi_L, and Δv_C represent the ratio between the output voltage and the voltage supply or duty cycle, the switching frequency, the output current ripple and the output voltage ripple, respectively [66].

On the other hand, the increment of the switching frequency, to allow the reduction of the passive components, decreases the power efficiency of the switching regulator because the dynamic losses in the buck converter scale proportionally to the frequency of operation [63], [90], [91]. A possible solution to this drawback is the use of interleaved synchronous converters working in parallel, i.e. a poly-phase structure [92]–[95]. An poly-phase buck converter is the combination of many individual buck converters sharing the same output load. This converters are connected in such way that the current they deliver adds at the output node. Moreover, if the buck converters operate out-of-phase with respect to each other, the total output current ripple Δi_L may be eliminated completely.

The minimization, or even full cancelation, of the output current ripple, and

consequently the output voltage ripple, and at the same time, the reduction of sizes of passive components, without increasing considerably the switching frequency, are the major benefits of using a poly-phase structure. The reduction in the magnitude of the output current ripple for interleaved buck converters [93]–[95] can be expressed as

$$\Delta i_L = \frac{V_{DD}}{2Lf_S} N \left(D - \frac{m}{N} \right) \left(\frac{m+1}{N} - D \right) \tag{7.3}$$

where N and m are the number of phases in the converter, and the maximum integer that does not exceed the product (N×D), respectively.

The output current ripple cancelation for interleaved buck converters can be better appreciated in Fig. 140. Note that the current ripple reduces as the number of phases increases. Also, observe that if the duty cycle is multiple of the the number of phases, the cancelation of the ripple is perfect.

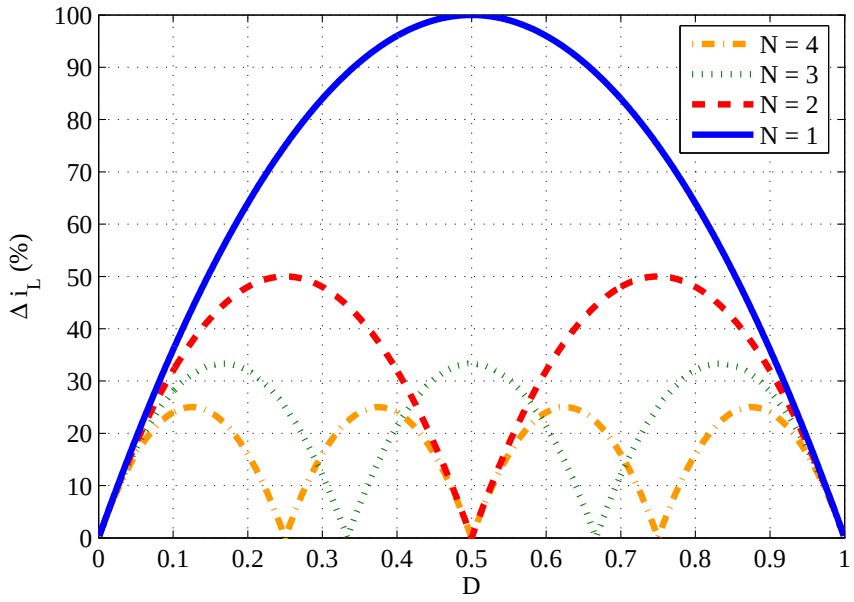


Fig. 140. Output current ripple cancelation for interleaved buck voltage converters

2. Proposed Dual-Phase Buck Converter Architecture

The proposed fully-integrated dual-phase buck voltage regulator architecture is shown in Fig. 141. The converter implements a two-phase architecture which can effectively reduce the output current ripple by half, as shown in Fig. 140. The dual-phase structure was chosen as a trade off between current ripple cancelation and complexity of a system with more phases. The generation of the interleaved pulse-width modulated signals, PWM_1 and PWM_2, is done by employing a hysteretic controller based on sliding mode control theory.

The goal is to minimize the error between the desired voltage V_{REF} and the actual output voltage V_{OUT}. The interleaved output currents are generated by sensing the currents across the respective output inductors and processing them in the controller. Since the architecture employed uses two phases, the effective switching frequency becomes $2f_s$,

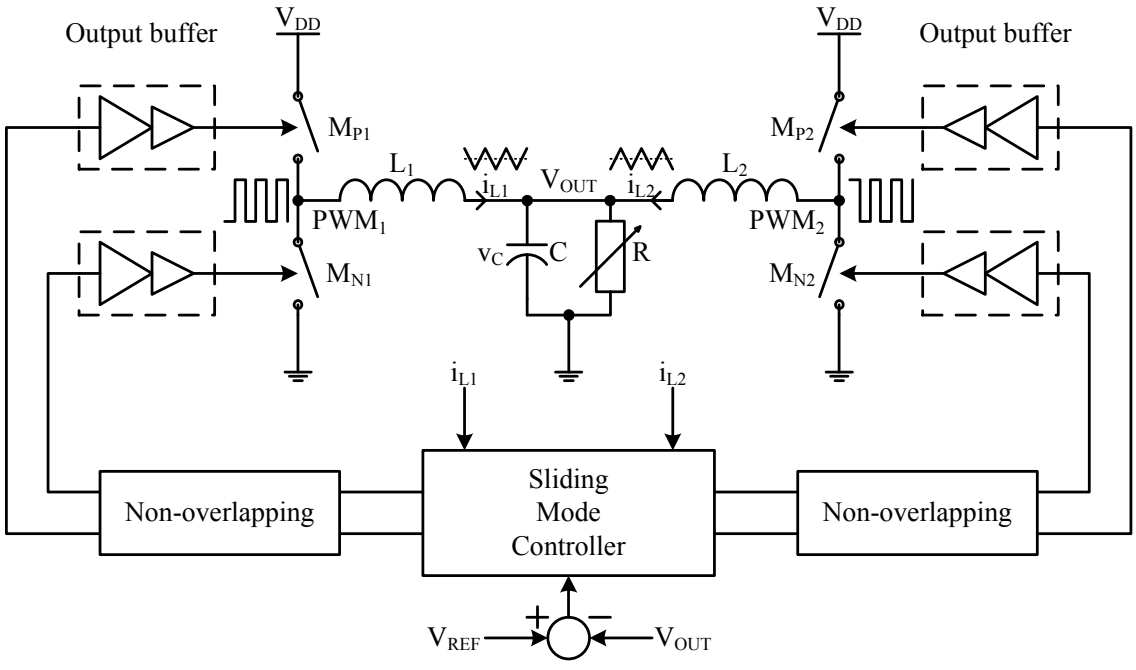


Fig. 141. Proposed fully-integrated dual-phase buck voltage regulator architecture

and the low-pass filter passive elements values, from equations (7.1) and (7.2), can be further reduced by half. Even though the number of passive elements doubles, they can be implemented easier on-chip due to their smaller size.

Besides the controller, the implemented voltage regulator includes the integration of the non-overlapping logic, the output buffers and the power switches, M_P and M_N. All the passive components in the low-pass filter, except for the resistive load, are fully-integrated using CMOS standard technology without any expensive post-fabrication process.

3. Dual-Phase Buck Voltage Regulator Specifications

The dual-phase fully-integrated buck voltage regulator has been designed using 0.18 μm SMIC and TSMC CMOS standard technologies and the specifications are listed in Table

Table XXVII. Dual-phase fully-integrated buck converter specifications

Parameter		Specification
Supply voltage	(V_{DD})	1.8 V
Output voltage	(V_{OUT})	0.9 V
Max. output current	(I_{MAX})	400 mA
Switching frequency	(f_s)	50 MHz
Output current ripple per output	(Δi_L)	100 mA
Output voltage ripple	(Δv_C)	45 mV
Output inductor	(L)	22.5 nH
Output capacitor	(C)	2.75 nF
Duty cycle	(D)	0.5

XXVII. As mentioned before, the reduction in the output current ripple is half, however, since the duty cycle of the converter is multiple of the number of phases implemented, the theoretical cancelation of the output current ripple, from Fig. 140, is total.

C. Proposed Sliding Mode Controller Design

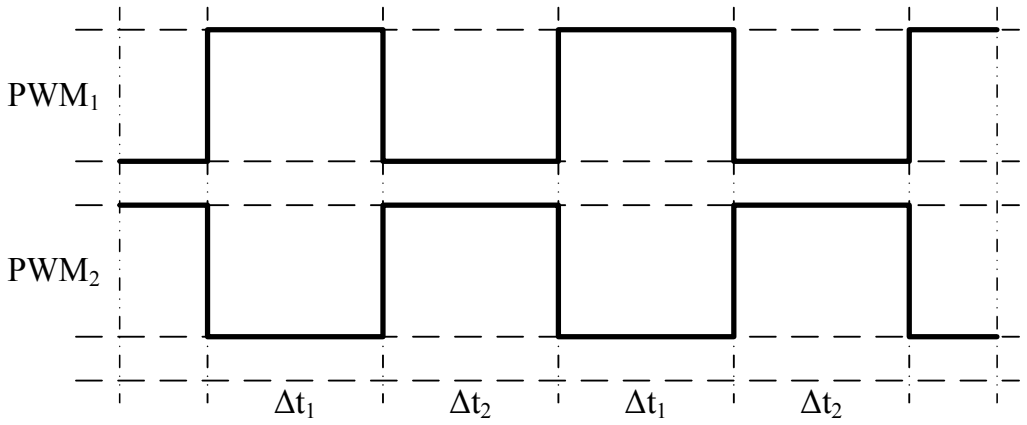
1. Preliminaries

In general, the buck switching regulator in Fig. 139 working in continuous conduction mode has two subintervals of operation [66]. During the first subinterval the top switch M_P is connected to the voltage supply and the bottom switch M_N is opened. This subinterval determines the duty cycle of the buck regulator. In the second subinterval, the top switch M_P opens and the bottom switch M_N closes.

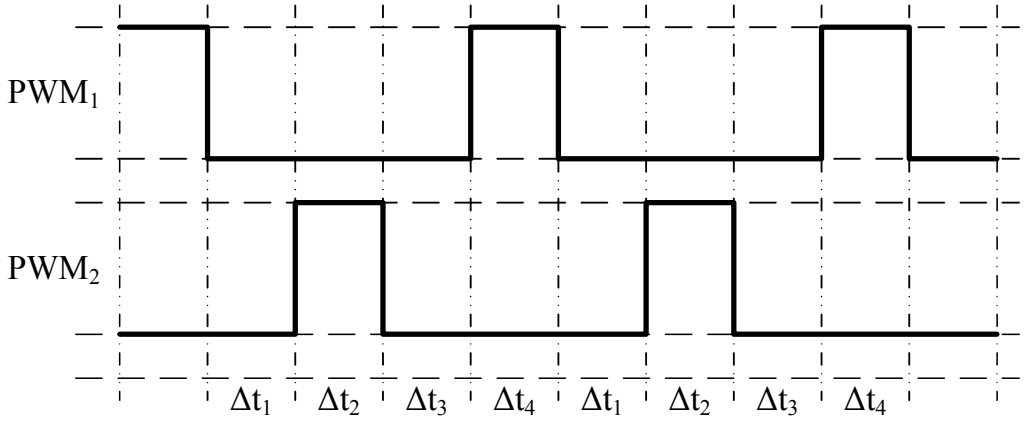
Therefore, the buck switching regulator can be classified as a variable structure system (VSS) because the description of its dynamics change along time, i.e. during each subinterval of operation the system is described with distinct differential equations. Variable structure systems can be regulated by using variable structure control (VSC) with sliding mode. This particular non-linear control technique was first proposed in the Soviet Union during the 1950s and its mean features include insensitivity to parametric uncertainties and robustness to external disturbances [33]–[36].

The dynamics of the proposed dual-phase buck voltage converter in Fig. 141 can be represented as a multiple-input single-output system with the set of differential equations characterized by the following state-space model

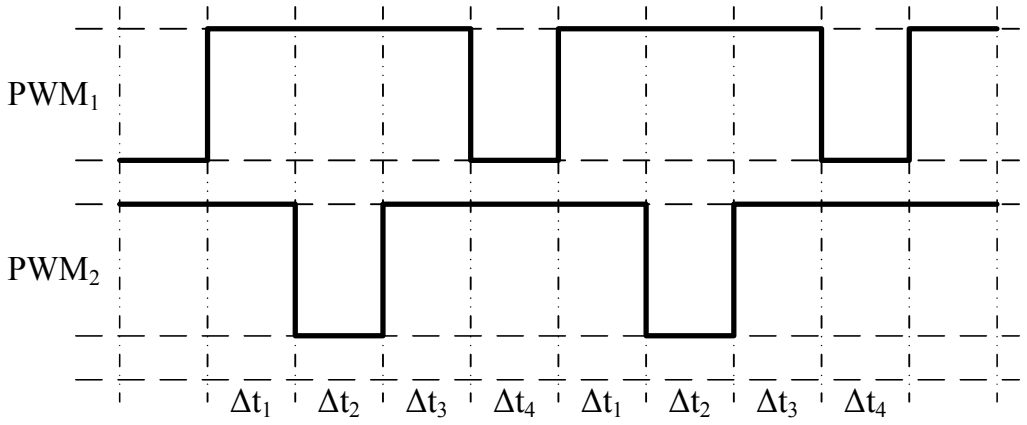
$$\begin{pmatrix} \frac{d}{dt}i_{L1} \\ \frac{d}{dt}i_{L2} \\ \frac{d}{dt}v_C \end{pmatrix} = \begin{pmatrix} 0 & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ v_C \end{pmatrix} + \begin{pmatrix} \frac{1}{L_1} & 0 \\ 0 & \frac{1}{L_2} \\ 0 & 0 \end{pmatrix} \begin{pmatrix} u_1 \\ u_2 \end{pmatrix} \tag{7.4}$$



(a)



(b)



(c)

Fig. 142. Subintervals of operation in a dual-phase buck voltage regulator (a) D = 0.5 (b) D $<$ 0.5 and (c) D $>$ 0.5

The number of subintervals in a dual-phase buck voltage regulator depends on the duty cycle. The minimum number of subintervals can be two if the duty cycle is D = 0.5, as shown in Fig. 142(a). During the first subinterval, PWM_1 is high and PWM_2 is low. During the second subinterval PWM_1 is low and PWM_2 is high.

The number of subintervals is four if the duty cycle is D $\neq$ 0.5, as shown in Fig. 142(b) and Fig. 142(c). In these cases, the two additional subintervals can have both pulse-width modulated signals, (PWM_1 and PWM_2), low if D $<$ 0.5, or high if D $>$ 0.5.

2. Design of the Sliding Mode Controller

The goal of the sliding mode controller (SMC) is to create a tracking system whose objective consists on minimizing the error between the reference voltage (V_{REF}) and the actual output voltage (V_{OUT}). The sliding mode controller generates a control function, also called switching function (SF), which makes the system to switch between its different subintervals until it reaches its sliding equilibrium point (SEP) [56]. The proposed dual-phase fully-integrated buck voltage regulator has one sliding equilibrium point defined as

$$SEP \; = \; (V_{OUT}, I_{OUT}) \; = \; (V_{REF}, I_{OUT}) \tag{7.5}$$

where I_{OUT} represents the output current consumed by the resistive load R in Fig. 141.

Even though the dual-phase buck voltage converter has only one sliding equilibrium point, it is necessary to generate two switching function for the same number of parallel interleaved phases. Therefore, there is a trade off between employing multiple phases and the complexity of implementing the controller. The control laws, for the proper operation of the dual-phase buck voltage converter, are defined in equation (7.6) and equation (7.7) [96]–[103]. Their derivation and necessary conditions for stability are discussed in Appendix D.

$$S_1(s) \; = \; k_1 V_{error}(s) \; + \; k_2 \frac{1}{s} V_{error}(s) \; + \; k_3 \frac{1}{s} I_{e1}(s) \; - \; I_{L1}(s) \tag{7.6}$$

$$S_2(s) \;=\; k_1 V_{error}(s) \;+\; k_2 \frac{1}{s} V_{error}(s) \;+\; k_3 \frac{1}{s} I_{e2}(s) \;-\; I_{L2}(s) \tag{7.7}$$

where

$$V_{error}(s) \;=\; V_{REF}(s) \;-\; V_{OUT}(s) \;=\; V_{REF}(s) \;-\; V_C(s) \tag{7.8}$$

$$I_{e1}(s) \;=\; \frac{1}{2}(I_{L2}(s) \;-\; I_{L1}(s)) \tag{7.9}$$

$$I_{e2}(s) \;=\; \frac{1}{2}(I_{L1}(s) \;-\; I_{L2}(s)) \tag{7.10}$$

and $k_1 = 0.5$, $k_2 = 36.4\times10^6$, and $k_3 = 1.45\times10^9$ are numerically calculated to obtain an smooth and fast transient response [96], [97]. The integral of the error voltage provides a regulated voltage at the output of the voltage converter. Since this term appears in both control laws, then each module can perform this function, resulting in a system with high reliability. On the other hand, the integral of the current differences, provides equal current distribution among the converter modules.

The switching functions force the dual-phase buck voltage regulator to switch between V_{DD} and ground according to the sign of the switching function as

$$u_{1,2} \;=\; \begin{cases} V_{DD} & \text{when} \quad s_{1,2}(t) \;>\; 0 \\ 0 & \text{when} \quad s_{1,2}(t) \;<\; 0 \end{cases} \tag{7.11}$$

The practical implementation of the switching functions, including drawbacks and proposed solutions, are detailed in next section.

D. Implementation of Building Blocks

The diagram of the implemented sliding mode controller is shown, at block level, in Fig. 143. It represents the switching functions, expressed in equations (7.6) and (7.7), and consists of three integrators and two summing nodes (blocks A_1, A_2, and A_3), as well as two hysteretic comparators, to generate the pulse-width modulated signals. The hysteresis

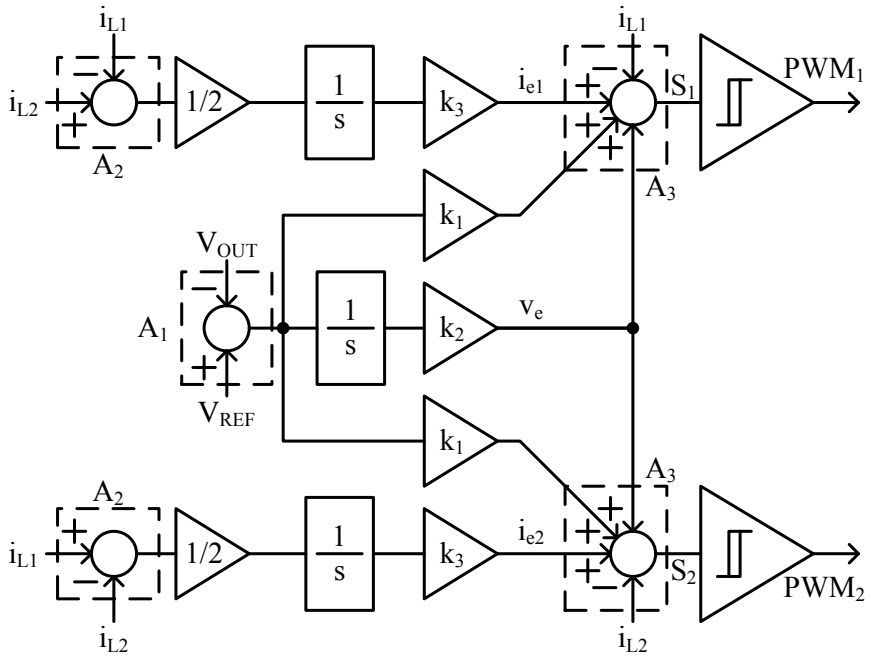
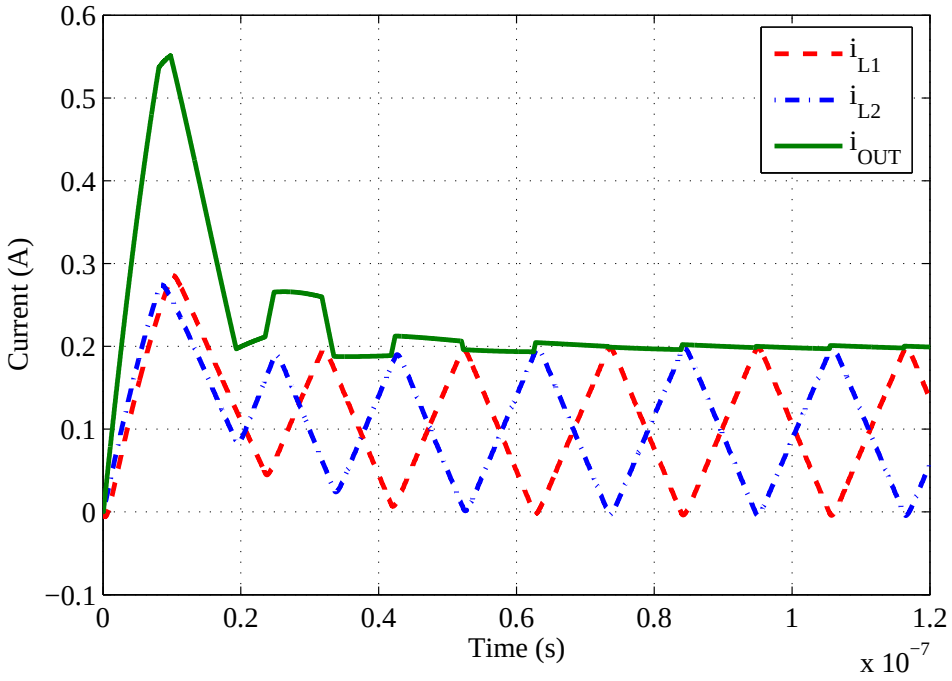


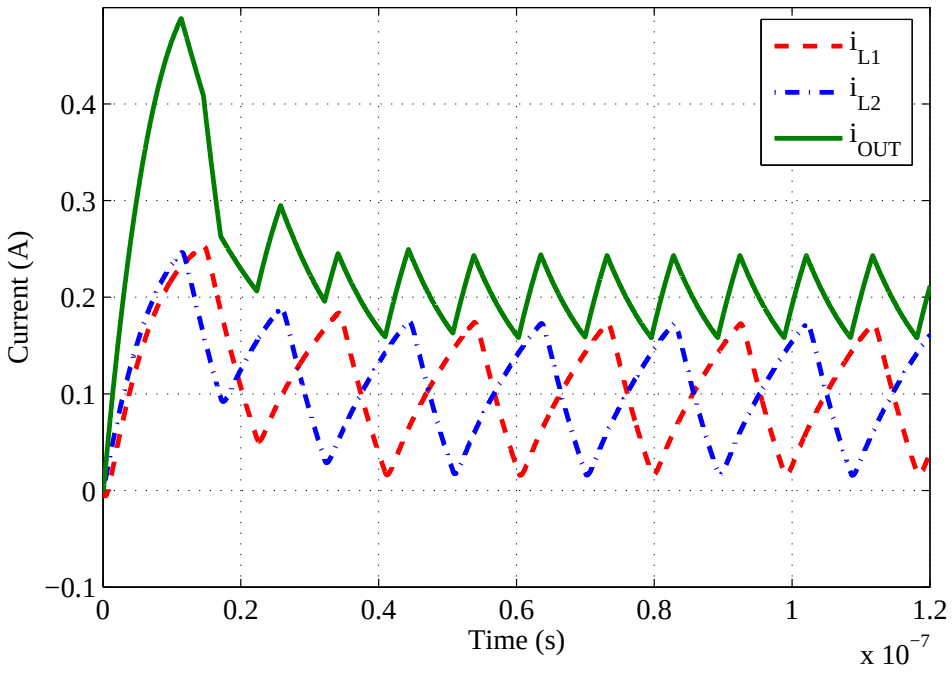
Fig. 143. Block diagram of the dual-phase buck converter sliding mode controller

of the comparators is set in such way that the dual-phase buck voltage regulator switches at approximately 50 MHz [60].

The two-phase buck voltage regulator was modeled in MATLAB [87] including most of the non-ideal effects in order to estimate the requirements of the building blocks in the converter. The model included a band-limited operational amplifier with finite gain, the switches on-resistances, and the inductor series resistance. For example, such non-idealities effects can be appreciated in Fig. 144, where the top plot represents the response of the ideal system, when I_{OUT} = 200 mA, and the perfect current ripple cancelation due to the symmetric duty cycle. On the other hand, the bottom plot shows the simulation of the actual inductor currents which includes the non-ideal effects of parasitic resistances and finite bandwidth of integrators and adders.

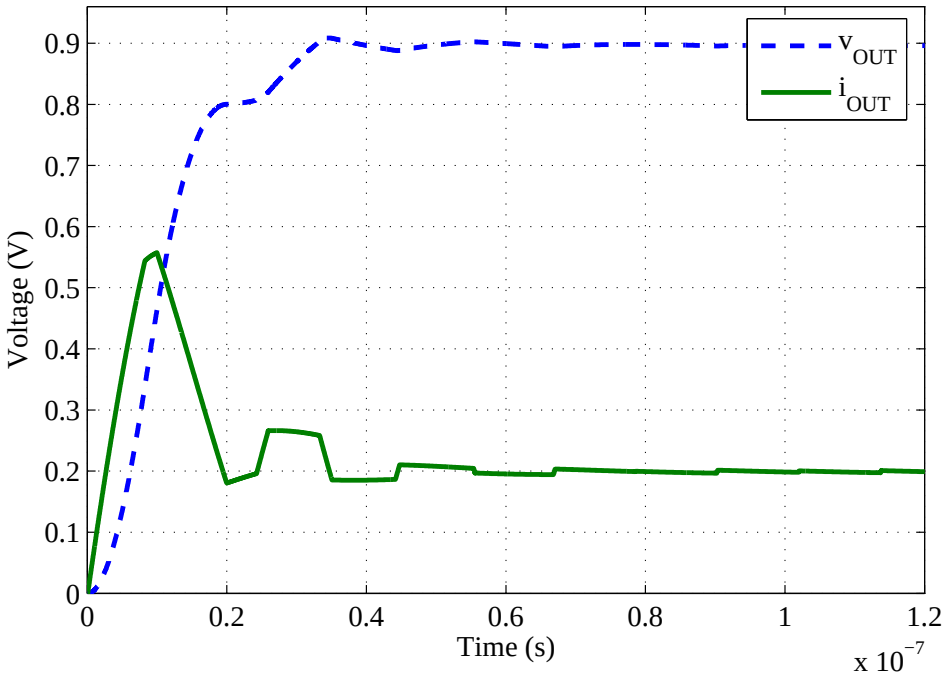


(a)

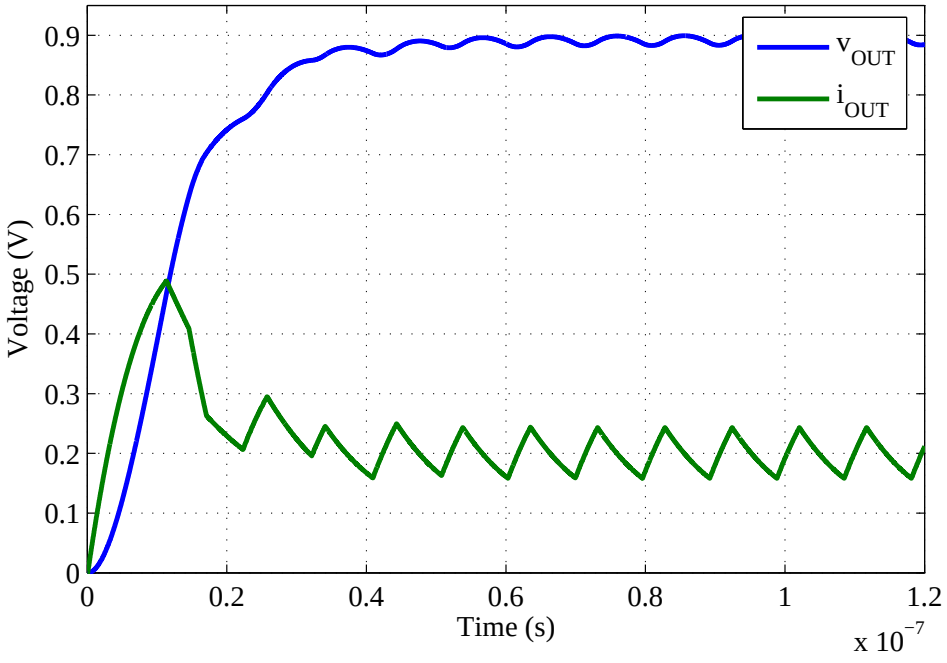


(b)

Fig. 144. Output current ripple cancelation in MATLAB model (a) Ideal case and (b) Non-ideal case



(a)



(b)

Fig. 145. Output waveforms in MATLAB model (a) Ideal case and (b) Non-ideal case

Similarly, Fig. 145 shows the step response of the dual-output buck voltage converter (V_{REF} = 0.9 V and I_{OUT} = 200 mA) for the ideal and non-ideal cases. As in the previous figure, the effect of having non-symmetric duty cycle can be clearly appreciated.

1. Controller Design

The switching functions in equations (7.6) and (7.7) are implemented using an operational amplifier (OPAMP) [47] to integrate the voltage error, and using a differential difference amplifier (DDA) [104]–[107] to integrate the current difference, as well as to implement the summing nodes. The hysteresis comparators represent the decision circuits implementing equation (7.11). The characteristics of the operational amplifier, differential difference amplifier, and comparator were selected through simulation in the MATLAB macromodel.

a. Single-Ended to Fully-Differential Converters

A fully-differential implementation of the buck voltage regulator is desirable to reject common substrate noise that could affect the generation of the appropriate control signals and pulse-width modulated signals. Therefore, a single-ended to fully-differential (SE2FD) converter transforms the single-ended voltages V_{OUT} and V_{REF} to fully-differential signals. The block diagram of the single-ended to fully-differential converter is shown in Fig. 146.

The operational amplifier is a two-stage structure with Miller compensation scheme [47]. Its schematic diagram is shown in Fig. 147 and the sizes of its transistors are listed in Table XXVIII. Its common-mode feedback circuit is illustrated in the schematic of Fig. 148 and its transistor sizes are summarized in Table XXIX. The value of the bias current I_B is 20 μA, the compensation capacitor C_C is 140 fF, and the compensation resistance R_C is 1 kΩ. A summary of its most important characteristics is listed in Table XXX.

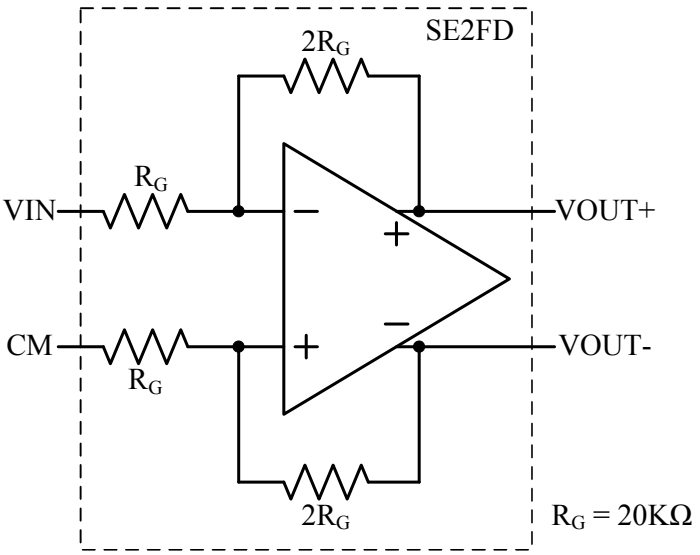


Fig. 146. Single-ended to fully-differential converter top level configuration

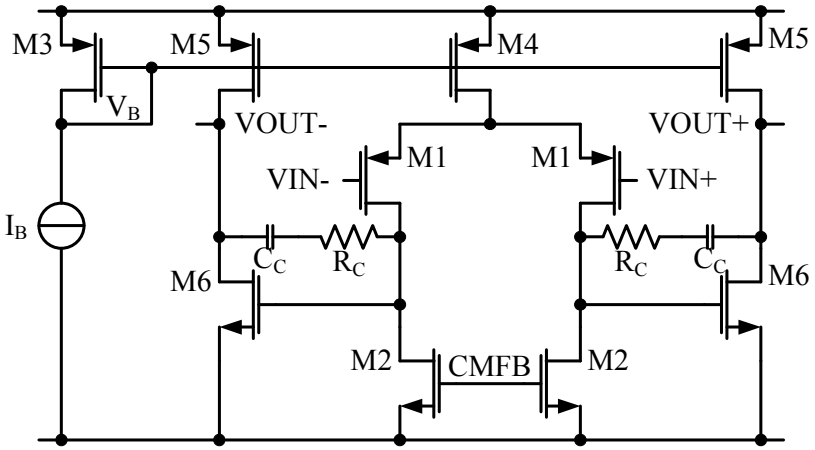


Fig. 147. Schematic diagram of the fully-differential operational amplifier

Table XXVIII. Fully-differential operational amplifier transistor sizes

Transistor	Width (μm)	Length (nm)	Multiplicity
M1	3.75	240	8
M2	2.5	240	4
M3	2.5	180	2
M4	2.5	180	16
M5	2.5	180	32
M6	3	180	8

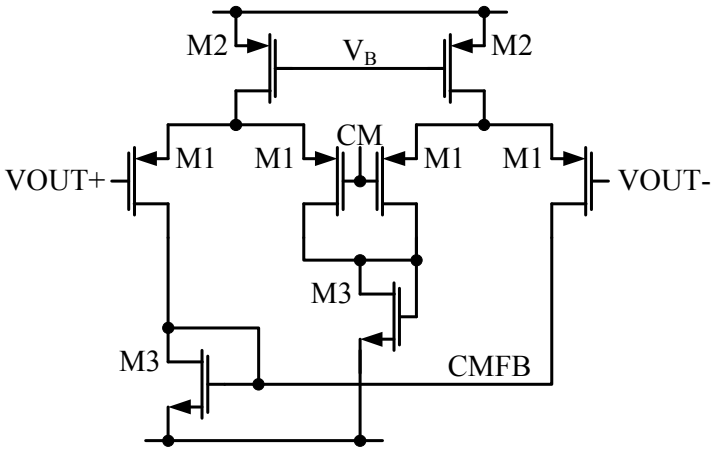


Fig. 148. Schematic diagram of the common-mode feedback circuit

Table XXIX. Common-mode feedback circuit transistor sizes

Transistor	Width (μm)	Length (nm)	Multiplicity
M1	1	240	8
M2	2.5	180	8
M3	2.5	240	4

Table XXX. Operational amplifier specifications

Parameter	Value
DC gain	55.84 dB
GBW	931 MHz
Phase margin	74°
I_Q	1 mA
P_Q	1.8 mW

b. Implementation of Switching Functions

The implementation of the switching functions in equations (7.6) and (7.7) is done using one operational amplifier and three differential difference amplifiers. The operational

amplifier implements the integration of the error voltage (illustrated as adder A_1 in Fig. 143) by using the fully-differential signals generated previously in the single-ended to fully-differential converter. One differential difference amplifier is used to generate the integration of the difference of the currents (shown as adders A_2 in Fig. 143) and other two are employed as the summing nodes (called adders A_3 in Fig. 143) just before the hysteresis comparators.

Figure 149 shows the configuration used to integrate the voltage error (adder A_1 in Fig. 143). It can be noticed the use of a lossy-integrator in order to avoid saturation of the amplifier at low frequencies. Gain k_2 is built using capacitor C_F and resistor R_C as $k_2 = 1 / C_F R_C$. The operational amplifier characteristics are the same as previously specified for the amplifier used to implement the single-ended to fully-differential converter. The differential signals V_{OUT} and V_{REF} are the output voltages generated by the previous

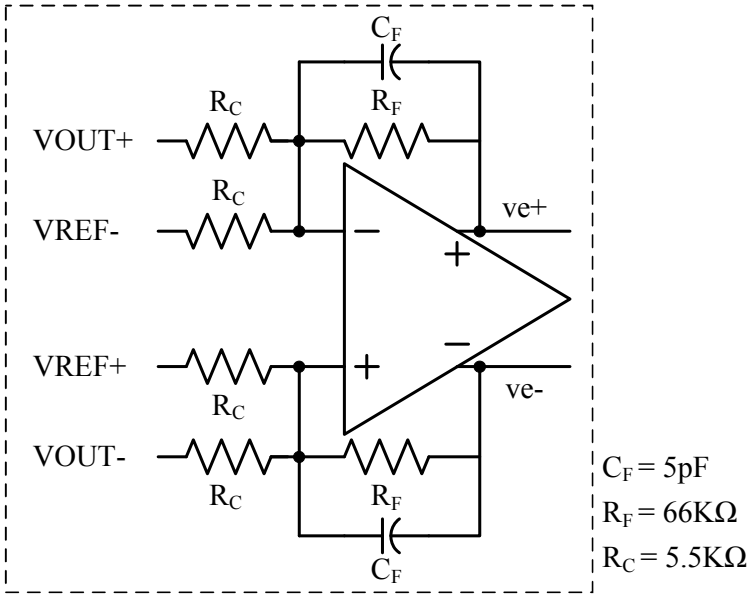


Fig. 149. Block diagram for voltage error integration

amplifier (single-ended to fully-differential converter).

The inductor currents are sensed by implementing a couple of metal sensing resistors R_{S1} and R_{S2} with value of 250 mΩ, as shown in Fig. 150. Therefore, the voltage difference between the node v_{L1} and V_{OUT} is proportional to the value of the current i_{L1} across inductor L_1. Similarly, the difference between node v_{L2} and V_{OUT} represents an scaled value of current i_{L2} across inductor L_2. Such scaling factor is later compensated as a gain in the current error integrator and in the summing amplifiers. The overall dual-phase buck voltage regulator was simulated with a mismatch on the sensing resistors of 20% without compromising the performance of the converter.

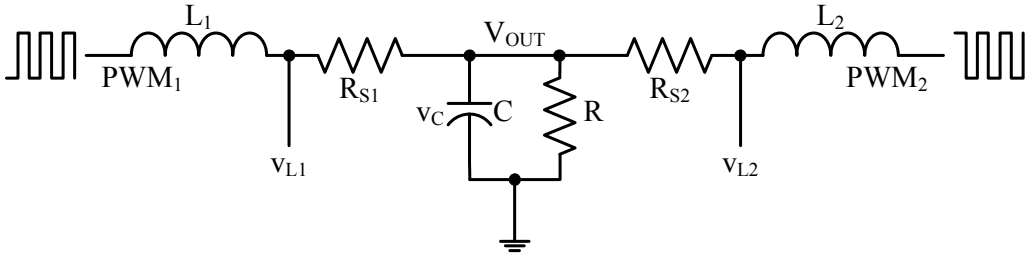


Fig. 150. Implementation of sensing current network

Figure 151 shows the differential difference amplifier configuration which implements the integration of the currents difference. Since node V_{OUT} is common for both current networks, the sensing of that node is mutually canceled. Also, observe that constant k_3 is implemented with resistor R_C and capacitor C_F as $k_3 = 1 / C_F R_C$. The differential difference amplifier integrator is also configured as a lossy-integrator structure to avoid saturation at low frequencies.

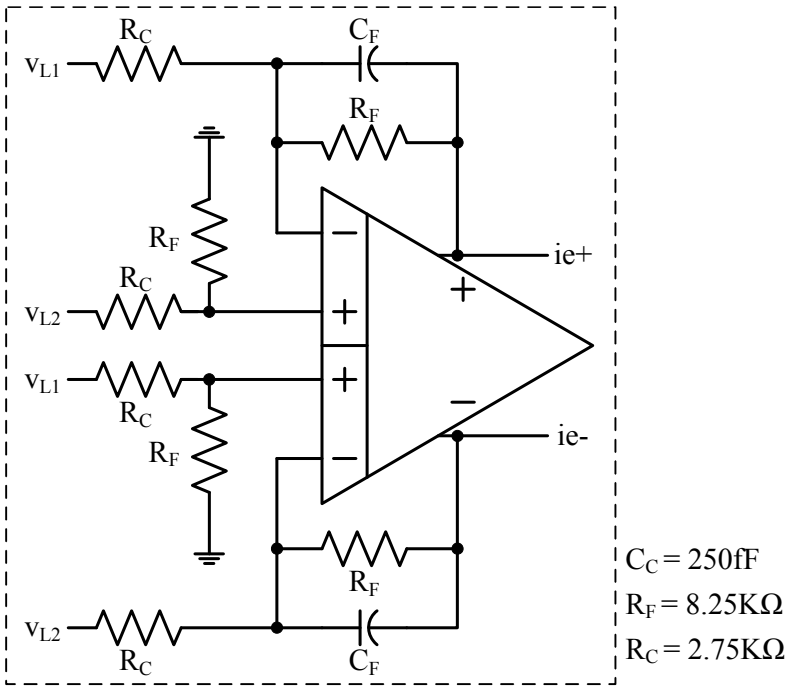


Fig. 151. Block diagram for currents difference integration

The differential difference amplifier is a two-stage structure with Miller compensation scheme [47], [104]–[107], and its schematic diagram is shown in Fig. 152, with the sizes of its transistors listed in Table XXXI.

The common-mode feedback circuit of the differential difference amplifier is the same illustrated before, in the schematic of Fig. 148. Additionally, the differential difference amplifier is biased with a current I_B = 20 μA, and it is compensated with a capacitor C_C = 140 fF, and a resistance R_C = 1 kΩ. A summary of the most relevant characteristics of the differential difference amplifier is listed in Table XXXII.

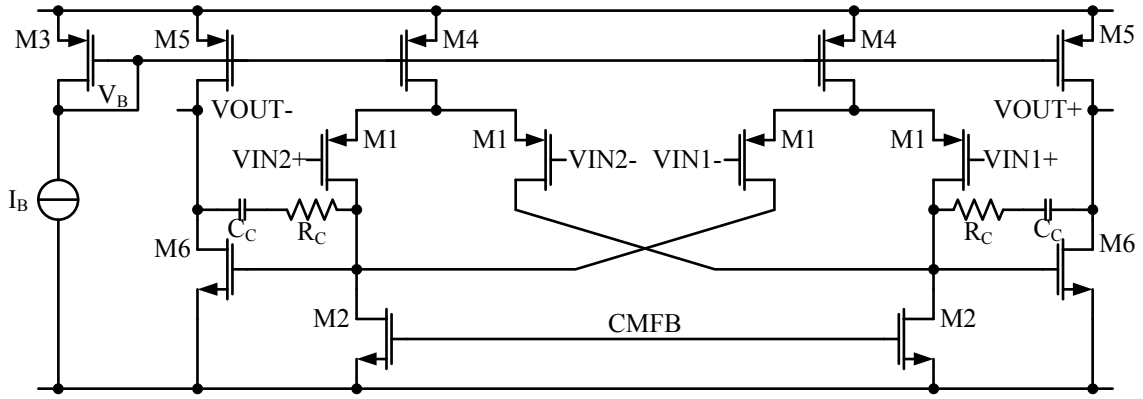


Fig. 152. Schematic diagram of the differential difference amplifier

Table XXXI. Differential difference amplifier transistor sizes

Transistor	Width (μm)	Length (nm)	Multiplicity
M1	3.75	240	4
M2	2.5	240	4
M3	2.5	180	2
M4	2.5	180	8
M5	2.5	180	32
M6	2.5	180	16

Table XXXII. Differential difference amplifier specifications

Parameter	Value
DC gain	55.85 dB
GBW	926 MHz
Phase margin	72°
I_Q	1 mA
P_Q	1.8 mW

Finally, the integrated voltage error signal and the integrated current difference, generated in previous configurations, along with the constant error voltage are merged using a couple of differential difference amplifiers configured as summing amplifiers. These amplifiers implement the adders A_3 in Fig. 143. The first differential difference amplifier builds the switching function S_1, and the second differential difference amplifier the switching function S_2. This configuration can be appreciated in Fig. 153.

Notice that constant gain k_1 and the scale factor in the sensing current circuit are both implemented at this stage. Also, observe that the numbers in parenthesis represent the voltage signals used to build the second switching function S_2. The hysteresis comparator (decision circuit) and the latch are described in the next subsection.

c. Decision Circuits

The decision circuits, which create the binary pulse-width modulated signals, are implemented using a hysteresis comparator [61], [62] as shown in Fig. 153. The schematic details of the decision circuit are shown in Fig. 154.

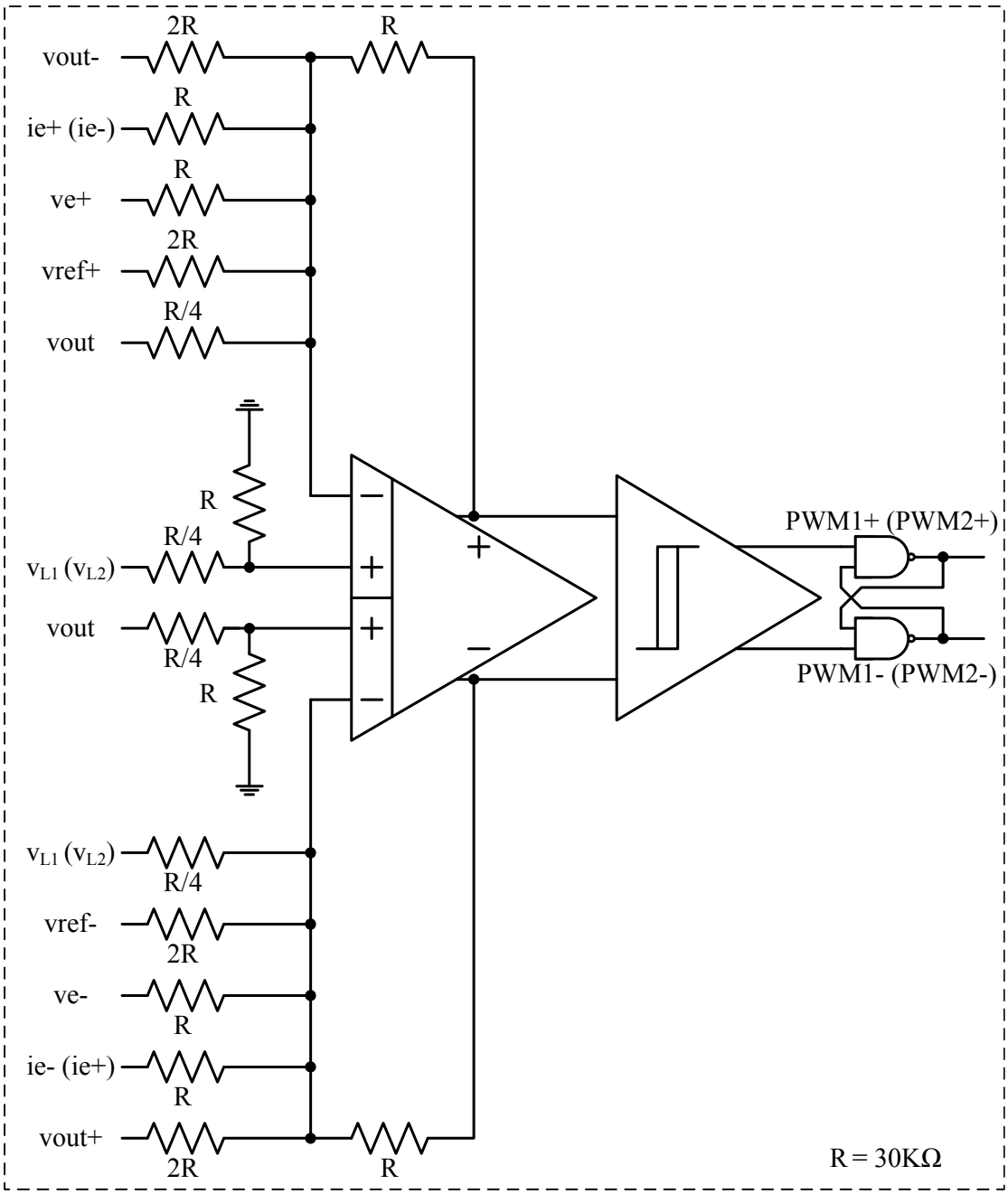


Fig. 153. Block diagram of the summing amplifier

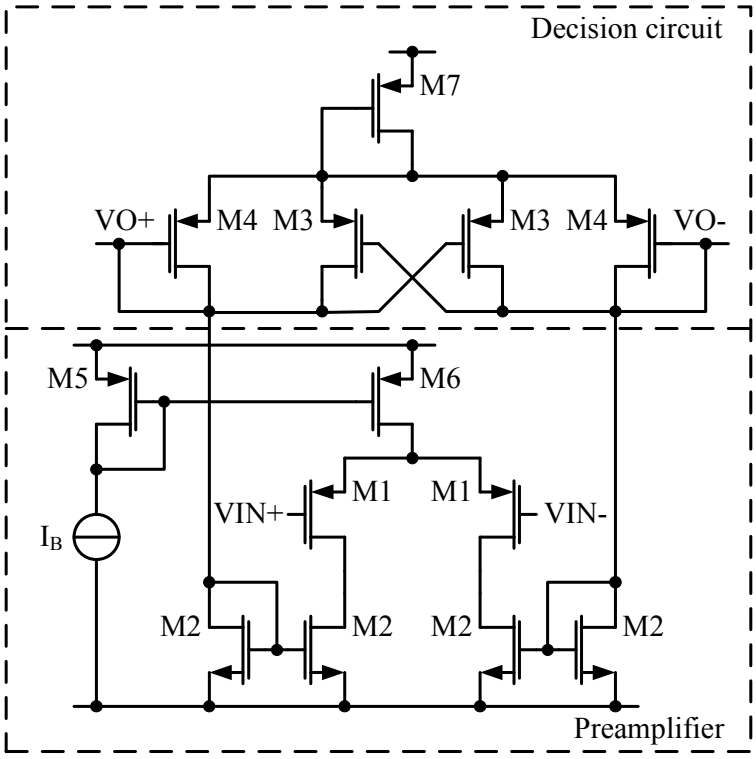


Fig. 154. Schematic diagram of the hysteresis comparators

The hysteresis comparator consists of two blocks, the preamplifier, whose function is to amplify the input signal to improve the sensitivity, and the decision circuit, whose function is to discriminate the input signals. The ratio between size of transistors M_3 and M_4 defines the comparator hysteresis window. The RS-latch in Fig. 153 locks the binary signal produced by the previous stage. The size of the transistors used to implement the hysteresis comparator is shown in Table XXXIII, and the overall details of the comparator are listed in Table XXXIV. The bias current I_B is 25 μA.

Table XXXIII. Size of the transistors used to implement the hysteresis comparator

Transistor	Width (μm)	Length (nm)	Multiplicity
M1	2.5	180	8
M2	1.5	180	2
M3	1	180	8
M4	1	180	4
M5	2	180	4
M6	2	180	16
M7	2	180	16

2. Output Power Stage

The output power stage is shown in Fig. 155. It consists of a non-overlapping circuit, a couple of output buffers and the power transistors M_P and M_N. Its main function is to

Table XXXIV. Summary of hysteresis comparator specifications

Parameter	Specification
Hysteresis voltage	20 mV
M_3 / M_4	2.0
I_Q	250 μA
P_Q	450 μW

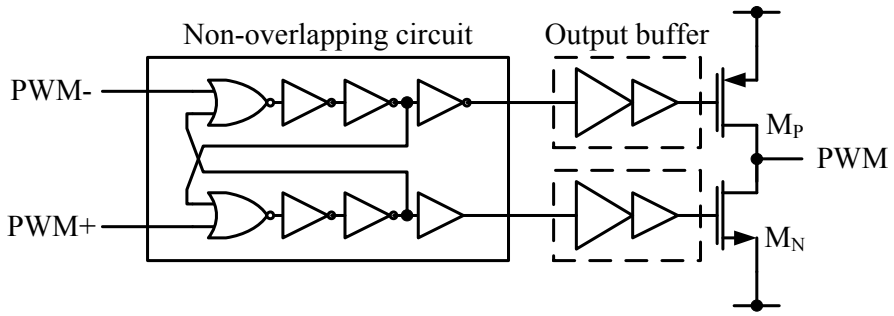


Fig. 155. Block diagram of the output power stage

provide the necessary driving capability to supply the output current to the load. The details of each block are outlined in the next subsections.

a. Non-Overlapping Logic

The non-overlapping logic provides timing synchronization in the pulse-width modulated signals to avoid the possible generation of short-circuit currents during transitions between subintervals of operation. Notice that the path driving the upstairs power switch M_P requires an extra inversion.

b. Output Buffer and Power Switches

The output buffer and power switches are designed in order to minimize the dynamic power dissipation without compromising the the propagation delay, as well as reducing the short-circuit current during transitions, and minimizing the CMOS on-resistance (R_{on}) [44], [45]. The tapering factor (T), and the number of inverters (N), as well as the width (W_P) and the length (L_P) of the power switch M_P are listed in Table XXXV. The size of each transistor in the buffer is calculated by dividing the last power transistors (M_P and M_N) between the

Table XXXV. Output buffer and power switches summary

Parameter	Value
W_{Mp}	14944 μm
L_{Mp}	180 nm
T	5
N	4
R	4
R_{on}	115 mΩ

tapering factor (T) for the total number of stages (N). Size of NMOS transistors is one fourth of size of PMOS transistors due to the mobility ratio (R) between them.

3. Integrated Output Low-Pass Filter

The integrated output low-pass filter, shown in Fig. 141, is a second order structure whose components values are calculated according to equations (7.1) and (7.2). Their monolithic implementation requires a careful design because many practical considerations have to be contemplated.

a. Output Capacitor

The output capacitor is built using MOS capacitors, or MOSCAPs, because they provide the highest capacitance per area when compared to metal-to-metal and poly-to-poly implementations [89], more than twenty times for this particular technology. Furthermore, the size of the unit cell MOSCAP is optimized by analyzing and calculating the minimum

equivalent series resistance (ESR) of the capacitor [108]–[110]. The model for the equivalent series resistance of a MOS capacitor [108], neglecting external resistance and frequency dependence, is given by

$$ESR \;=\; R_{CH} \;+\; R_G \;=\; \frac{1}{\mu C_{ox}(V_{gs} \;-\; V_T)}\frac{L}{W} \;+\; \alpha R_{poly}\frac{W}{L} \tag{7.12}$$

where R_{CH}, R_G, W, and L are the channel resistance, the gate polysilicon resistance and the width and length of the MOSCAP transistor, and μ, C_{ox}, V_{gs}, V_T, and R_{poly} are the mobility factor, the gate capacitance per unit area, the gate-source voltage, the threshold voltage, and the polysilicon sheet resistance, respectively. The factor α equals to 1 / 12 if the gate is connected from two sides and 1 / 3 if it is connected from one side.

The minimum equivalent series resistance for a single MOS capacitor can be calculated by differentiating equation (7.12) with respect the the aspect ratio (W / L) of the transistor as

$$\frac{\partial ESR}{\partial W/L} \;=\; 0 \tag{7.13}$$

Solving equation (7.13) we can get the optimum aspect ratio of the transistor and the minimum minimum equivalent series resistance as

$$\left(\frac{W}{L}\right)_{opt} \;=\; \sqrt{\frac{1}{\alpha\mu C_{ox}(V_{gs} \;-\; V_T)R_{poly}}} \tag{7.14}$$

$$ESR_{min} \;=\; 2\sqrt{\frac{\alpha R_{poly}}{\mu C_{ox}(V_{gs} \;-\; V_T)}} \tag{7.15}$$

Figure 156 shows the results of the minimization procedure. The optimum width and length of a MOSCAP cell is W_{opt} = 22 μm and L_{opt} = 800 nm. The number of unit cells is 16919, the area occupied by the output capacitor is 0.297 mm^2, and the total equivalent series resistance (minimum equivalent resistance divided by the total number of unit cells) is 2.1 mΩ.

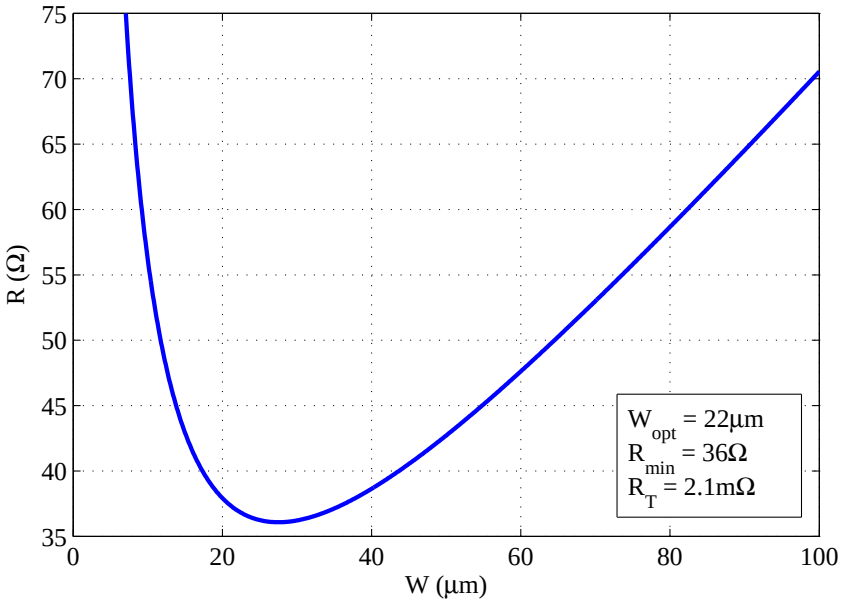


Fig. 156. Equivalent series resistance optimization

b. Output Inductor

The physical dimensions of the output inductor are customized due to the large amount of current that it needs to handle [89], [111]. The characterization of the inductor is optimized

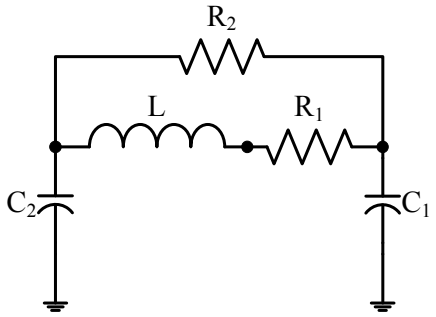


Fig. 157. Extracted schematic inductor model from SONNET

using SONNET, however, the lack of a high-conductivity material in the top metal layer reduces the quality of the inductor.

The schematic model from software simulations is shown in Fig. 157. The main drawback of the designed inductor is its high equivalent series resistance (R_1) due to the poor conductivity, the high sheet resistance, and the relatively thin (2.4 μm) top metal layer. This parasitic resistance reduces the efficiency significatively since its size is comparable to the output resistive load of the dual-phase buck voltage regulator. Table XXXVI summarizes the extracted schematic values of the inductor model from simulations in SONNET, and also, it details the hypothetical sizes of the model if a thicker metal layer were used.

Table XXXVI. Component values of the schematic inductor model

Metal thickness	1X	2X	5X	10X
L	24.5 nH	22.8 nH	22.7 nH	23.7 nH
R_1	2.7 Ω	1.6 Ω	0.9 Ω	0.6 Ω
R_2	62 Ω	147 Ω	329 Ω	385 Ω
C_1	210 fF	201 fF	210 fF	210 fF
C_2	550 fF	560 fF	570 fF	600 fF

The quality factor of the inductor (Q_L) at the frequency of operation is shown in Fig. 158. It can be appreciated that the inductor implementation requires the use of thicker top metal layer to improve its quality factor. Also, it is desirable the use of a metal with better

conductivity and/or magnetic materials to boost the quality of the output inductor.

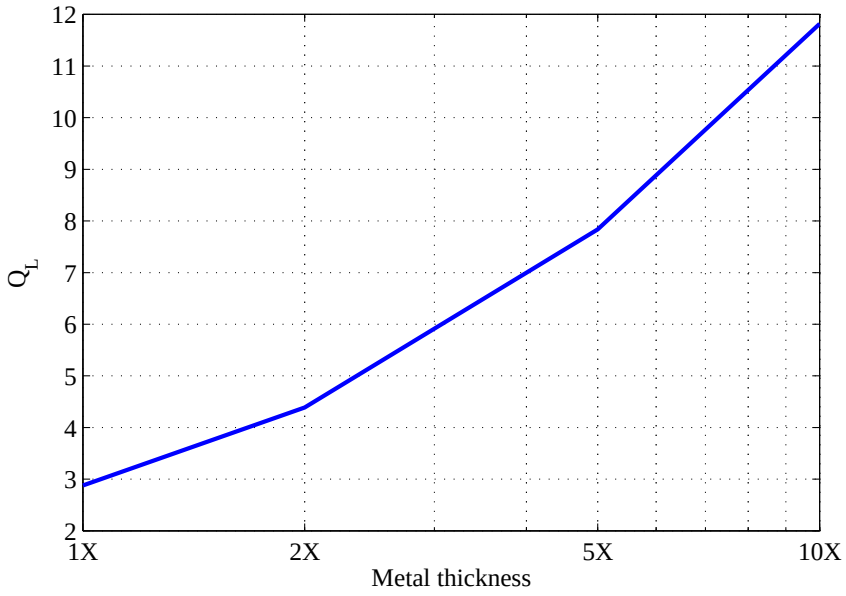


Fig. 158. Quality factor of the output inductor versus metal thickness

E. Simulation Results

The proposed dual-phase fully-integrated buck voltage regulator has been designed and simulated in 0.18 μm SMIC and TSMC CMOS technologies, and it has been sent for fabrication using the latter process. The results of post-layout simulations are shown in this section.

A snapshot of the dual-phase buck voltage converter layout is shown in Fig. 159, where all the main building blocks, presented in previous sections, are highlighted. Figure

160 illustrates the power consumption and area distribution in the proposed converter. It can be appreciated that most of the power is burned by the controller. In addition, notice that the output capacitor and the output inductor occupy more than 90% of the total area.

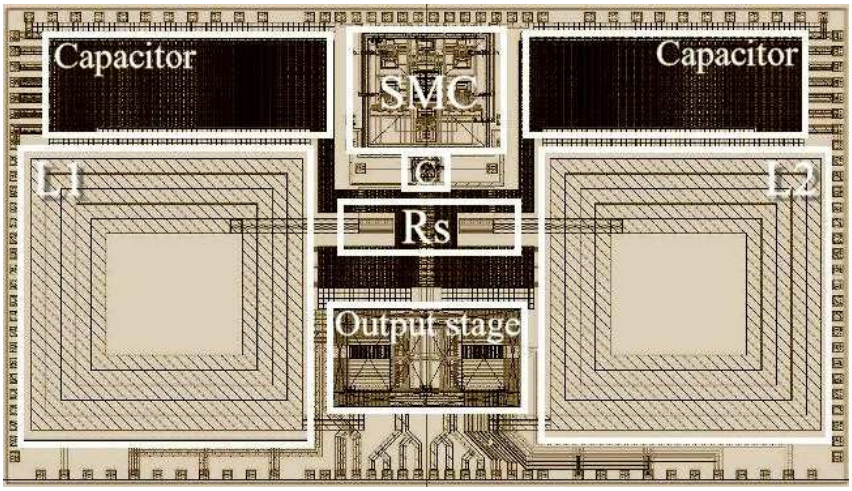


Fig. 159. Snapshot of the dual-phase buck buck voltage converter layout

1. Steady-State Operation

The steady state operation of the buck converter, as well as the efficiency simulations, are presented in this section. Figure 161 shows the pulse-width modulated signals generated by the sliding mode controller. As predicted from the MATLAB model, the theoretical 50% duty cycle incremented up to 70% due to all the non-ideal elements. The switching frequency is approximately 50 MHz. The interleaved inductors currents, driving a total output current of 200 mA, are presented in Fig. 162. Notice that the output current ripple

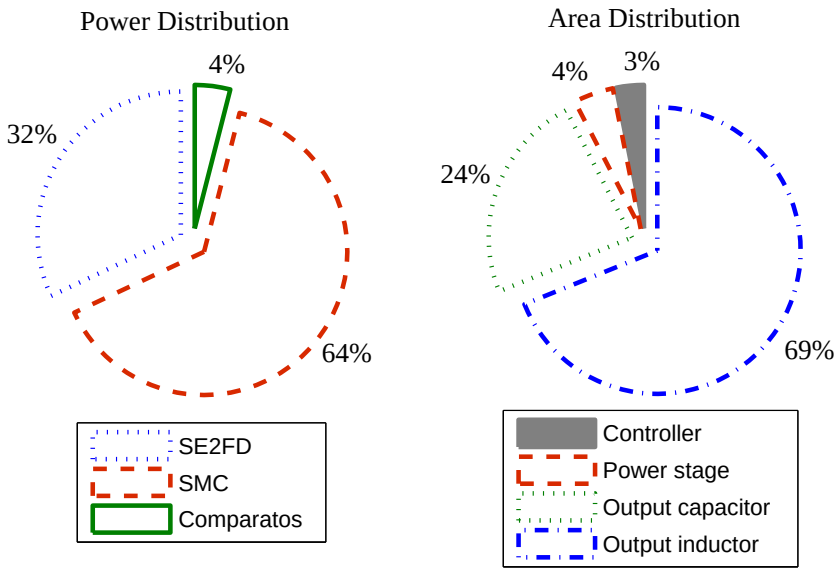


Fig. 160. Power consumption and area distribution of the proposed dual-phase buck voltage regulator

cancelation is not perfect due to the deviation of the duty cycle from its ideal value.

The efficiency of the two-phase buck converter, in SMIC and TSMC technologies, is presented in Fig. 163. As expected, the efficiency of the buck converter is higher in schematic simulations. The fact that TSMC technology has better characteristics in its top metal layer allows the increment of the post-layout efficiency, however, the equivalent series resistance of the output inductor remains as the main contributor for power losses.

Corner process simulations, slow-slow (SS), fast-slow (FS), typical (TT), slow-fast (SF) and fast-fast (FF), were performed to the buck voltage regulator in order to verify the operation of the system and its robustness to process variations. As expected, the system performed poorer at the slow-slow corner and it showed better efficiency when the fast-fast corner was used. The variation on the efficiency for both processes, SMIC and TSMC, is around $\pm 5\%$. Results from these simulations are shown in Fig. 164.

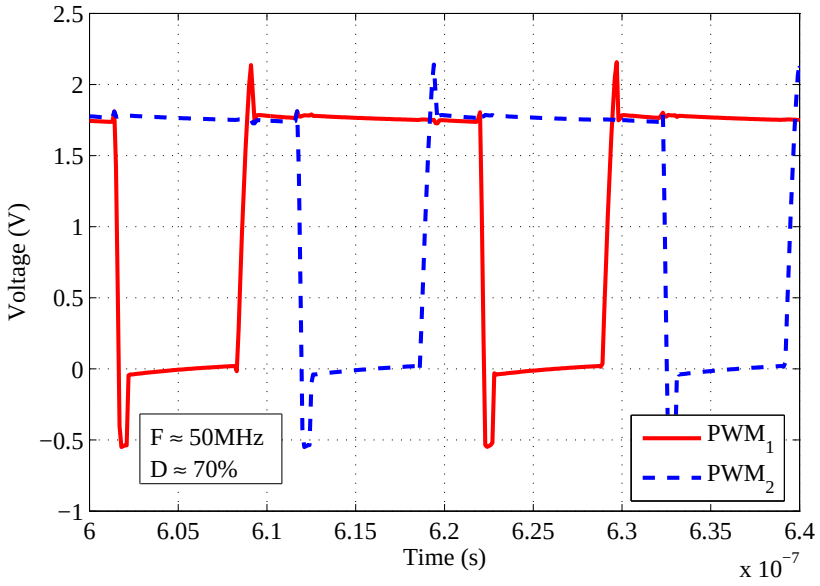


Fig. 161. Pulse-width modulated signals

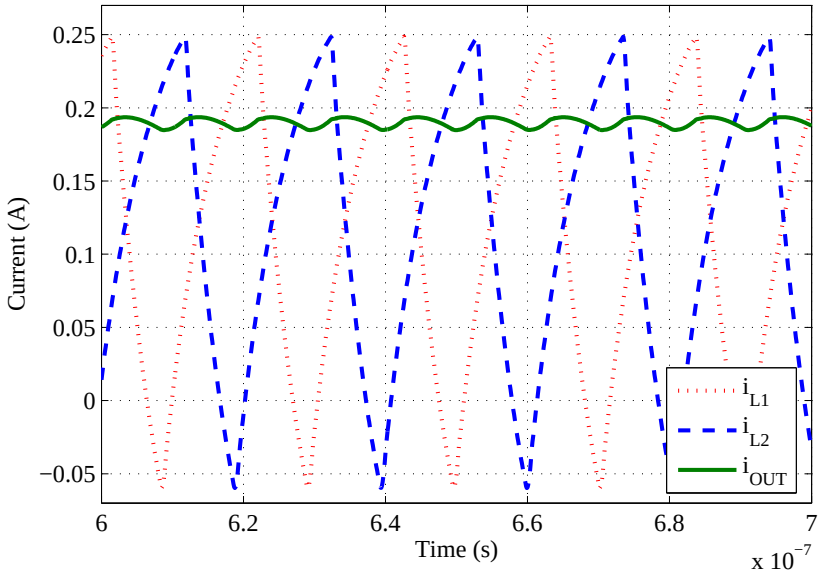


Fig. 162. Interleaved inductors currents

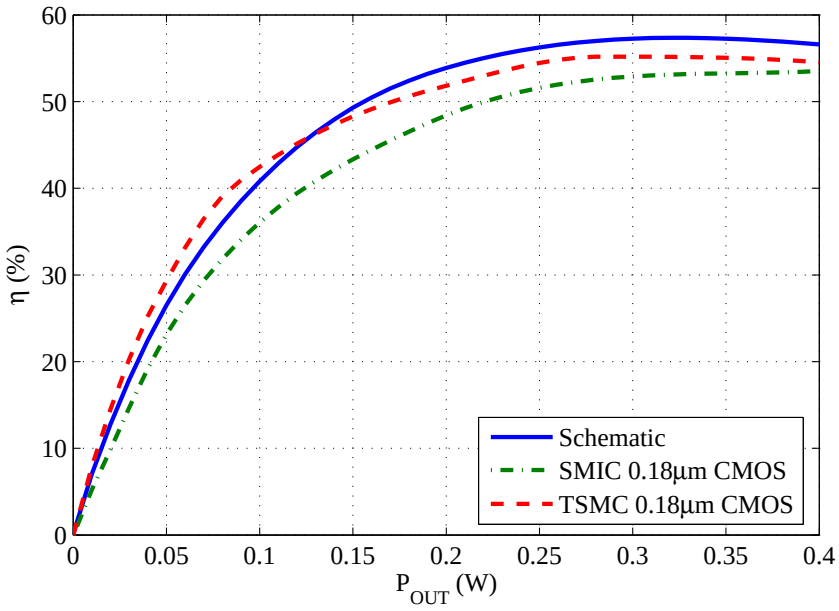


Fig. 163. Fully-integrated buck converter efficiency

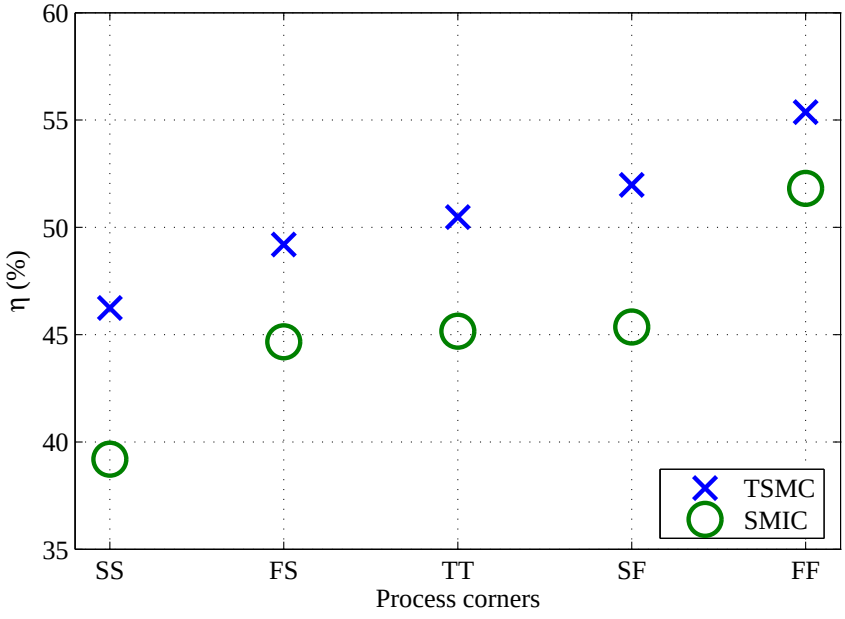


Fig. 164. Efficiency of the buck converter versus corner process variations

In addition, the system was simulated for the case where the output inductor model could actually present lower inductance. This particular case is important because the inductor was custom designed and was not based on any library model from either SMIC or TSMC. The results of these simulations, for an output load current of 200 mA, are shown in Fig. 165. Even though the system converged and operate at the desired voltage and output currents, the efficiency performance of the buck voltage regulator reduced by more than 10% in the worst case.

Finally, the efficiency of the converter was simulated for the hypothetical case of having a thicker top metal layer (better quality factor) and the results are shown in Fig. 166. As the quality factor of the inductor increases and the equivalent series resistance decreases, the efficiency of the buck converter, when the load current is set to 200 mA, increments more than 10% of its original value.

2. Transient Response

The transient response of the buck converter was tested by applying a current step of 100 mA at the output of the regulator. The transient response of the buck converter was simulated for all the corner processes to ensure the convergence of the regulator.

Figure 167 and Fig. 168 show the transient response of the converter. As expected, the best response, with half the voltage ripple, was obtained using the fast-fast corner and the worst with the slow-slow corner. Moreover, the transient response of the voltage converter was tested for the hypothetical case of having a ten times thicker top metal layer in the output inductor (four times better quality factor). As can be appreciated in Fig. 169, the output voltage ripple is reduced when the thicker metal is used due to the reduction in the inductor parasitics.

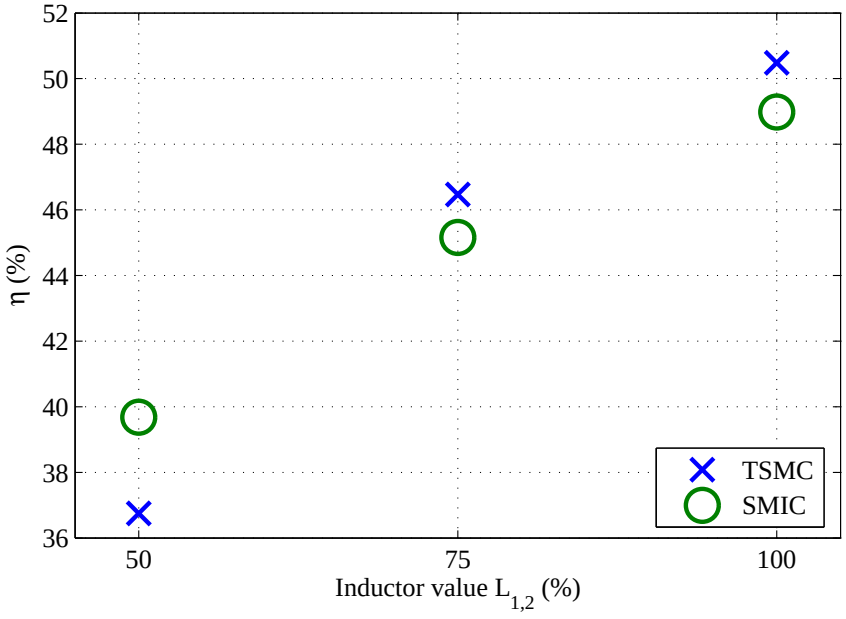


Fig. 165. Efficiency of the buck converter versus normalized inductor value

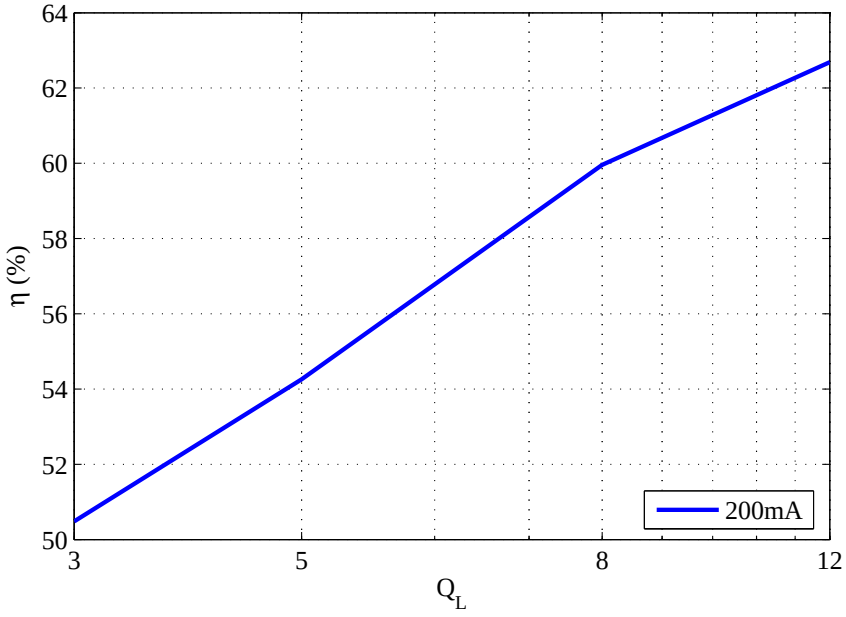


Fig. 166. Efficiency of the dual-phase buck voltage converter versus inductor quality factor

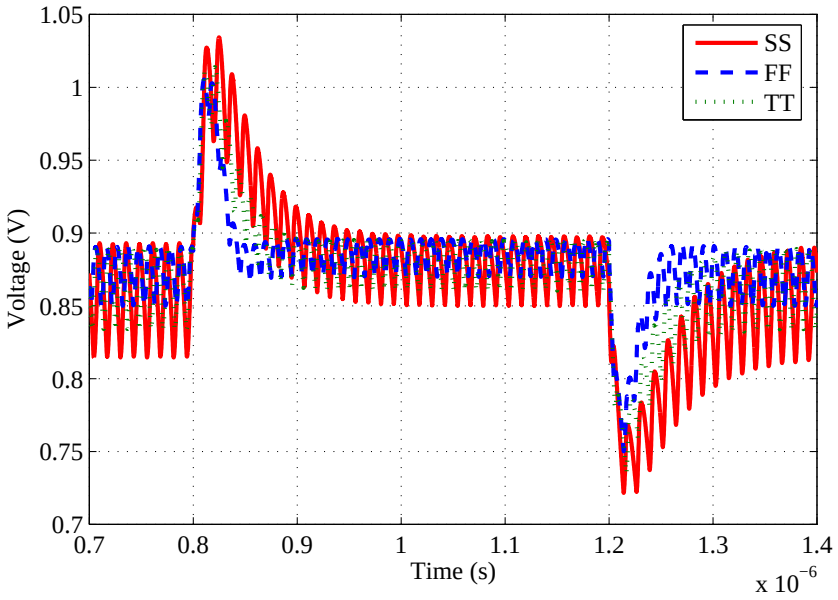


Fig. 167. Transient output voltage when a current step of 100 mA at output node

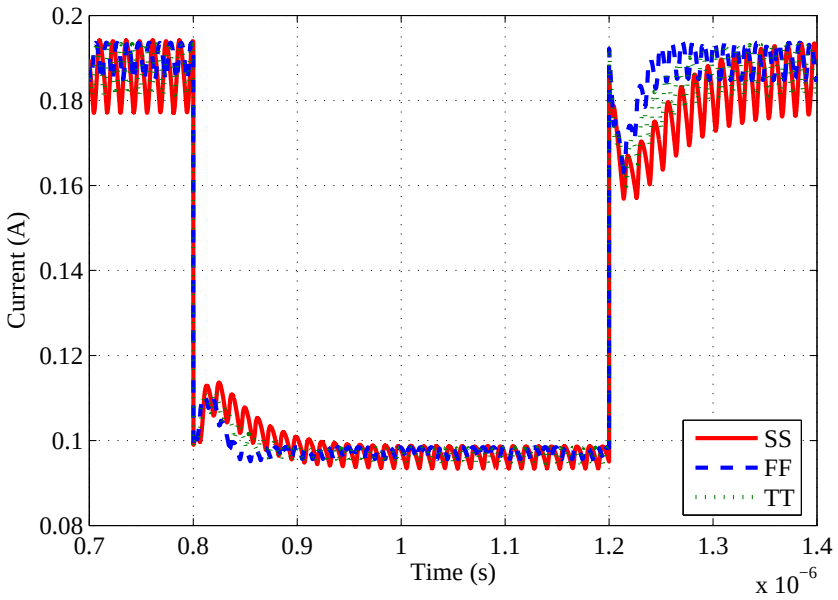


Fig. 168. Transient output current with a current step of 100 mA at output node

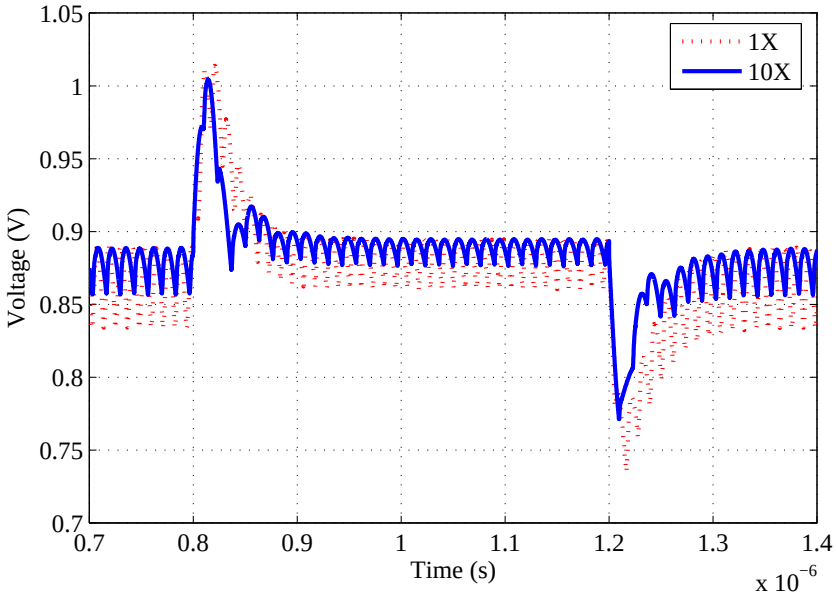


Fig. 169. Transient response for different inductor metal thicknesses

Table XXXVII lists the simulated results along with previously reported works. It can be seen that the specifications of the proposed buck converter are comparable to the state-of-the-art results but its efficiency performance is poorer. This fact is mainly due to the lossy inductor implementation ($Q_L \approx 3$).

The output inductors in the proposed dual-phase buck voltage regulator have been implemented in CMOS standard technology without any special post-fabrication process to boost the inductor quality. On the other hand, all previous reported works have a special fabrication process to improve the converter performance. High-quality air-core inductors with minimum losses are implemented in [94], also, a special top metal layer based on copper have been used in [95]. Furthermore, a CMOS compatible micro-electromechanical (MEM) technique to built air-core plastic deformation magnetic assembly (PDMA) inductors is employed in [111]. Moreover, the inductors in [112] use

magnetic materials to improve the quality factor. The product [113] uses on-package inductors and even an external capacitor. All of the previous works employ expensive post-fabrication techniques or high-cost special fabrication process to generate a good quality inductor. However, the proposed architecture lacks of any kind of expensive post-fabrication process and still has shown to be reliable, stable, robust, and very low-cost.

Table XXXVII. Comparison of state-of-the-art buck voltage regulators

Design	[94]	[95]†	[111]	[112]	[113]	This work
V_{IN} (V)	1.2	2.8	5.0	1.2	5.5	1.8
V_{OUT} (V)	0.9	1.8	2.5	0.9	3.3	0.9
I_{OUT} (mA)	300	200	30	350	1000	400
f_s (MHz)	233	45	10	170	5	50
η (%)	83	64	53	78	93	55
C (nF)	2.5	6.0	3.0	5.2	60000	2.8
L (nH)	6.8	11.0	80.0	2.0	-	22.5
Δv_C (mV)	90	-	50	40	10	45
Technology (CMOS)	90nm	0.18um	1.5um	130nm	-	0.18um
Results	Tested	Tested	Tested	Tested	Product	Simulated

† SiGe special fabrication process

F. Future Work and Suggestions

The design, implementation, and simulation of a dual-phase fully-integrated buck voltage regulator has been presented. The use of a two-phase structure in the converter allows 50% reduction of the output current ripple. The design cycle will be complete once the fabricated integrated circuit is tested. The simulated results are comparable to the state-of-the-art works even though there is not any additional post-fabrication process to improve the converter performance.

The design of the dual-phase fully-integrated buck voltage regulator needs to be improved in two main aspects. The first one is to find a better current sensing method that does not depend on process variations. Also, the sensing current circuit must be lossless and with minimum overhead to the overall system. The second aspect is the improvement on the inductor design. Several inductors must be fully characterized and tested. Also, the need of an extra top layer with thicker and a better conductive metal is desirable; these characteristics could reduce the parasitic resistance of the inductor and increase its quality factor. Furthermore, the use of additional materials with magnetic properties can be explored. Another option is to increase the number of phases in order to reduce even more the size of the inductor and by consequence the current it handles. On the other hand, increasing the number of phases will increase the complexity of the controller.

As shown in this chapter, the main bottleneck on fully integrating a buck voltage regulator consists on having an accurate, small area, and lossless integrated inductor capable of handling very high currents.

CHAPTER VIII

SUMMARY

The design and implementation of switching voltage integrated circuits have been presented. Class D audio power amplifiers based on a hysteretic non-linear topology have been fabricated and tested. The first prototype, discussed in Chapter III, have shown high efficiency performance as well as good linearity, and good power-supply rejection ratio.

Moreover, the binary-modulation amplifier and the ternary modulation amplifier presented in Chapter IV, achieve results comparable to the state-of-the-art works but consuming less than one tenth of quiescent power. Therefore, making them highly suitable for applications where the optimization of battery life is critical.

Further research, which is already been explored, includes the design of audio power amplifiers with even less power consumption and still the same or better performance. After the research done in this dissertation, the interest on digital class D audio amplifiers has emerged, since the analog modulator must be reconfigurable and independent of technology size, and voltage scaling.

Also, alternative topologies like class G and class H audio power amplifiers can be explored. These architectures can exhibit high linearity performance but their efficiency is still poor when compared to class D audio power amplifiers. Need of innovative techniques to increase efficiency are a must.

On the other hand, the design of an integrated dual-output buck voltage regulator has been demonstrated in Chapter VI. The converter has shown high efficiency and good transient response. However, the maximum performance is obtained when the top output voltage in the stacked structure delivers higher output current. This is a special characteristic of the converter, but it is not a limitation because of the many circuits with different power supply requirements in a typical system.

Finally, the first design cycle of the proposed fully-integrated buck converter, in Chapter VII, will be completed once the die is properly packaged and tested. Moreover, the prototype circuit must be optimized in order to improve its efficiency performance. The use of additional post-fabrication processes have to be explored in order to boost the output inductor quality. The implementation of monolithic power supplies with high efficiency and good regulation will be needed for future electronic devices.

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APPENDIX A

ANALYSIS OF HARMONIC DISTORTION IN OPEN-LOOP CLASS D AUDIO POWER AMPLIFIERS BY DUTY CYCLE VARIATION

This appendix details the derivation of the pulse-width modulated signal, and harmonic distortion, in open-loop class D audio power amplifiers, for the particular cases of sawtooth, triangle, sinusoidal, and exponential-shaped carrier waveforms, by means of the analysis by duty cycle variation [26]. It also gives the necessary tools to extend the analysis of distortion in class D audio power amplifiers for any periodic carrier waveform and even multilevel modulation schemes.

The analysis by duty-cycle variation is an alternative method, to the classical double Fourier integral analysis [5], [26], to calculate the harmonic spectrum in open-loop class D audio power amplifiers based on naturally sampled pulse-width modulation. This approach examines the switching process of the amplifier during a few arbitrary cycles of the carrier waveform. The reference audio waveform is assumed to be constant within each carrier cycle, i.e. the frequency of the carrier waveform is much higher than the frequency of the audio waveform ($f_c \gg f_o$), which is usually the case.

Firstly, define the existence of two time variables, x(t) and y(t), who represent the time variation of the carrier and the audio waveforms, respectively. These time variables can be expressed as

$$x(t) \;=\; \omega_c t \;+\; \theta_c \tag{A.1}$$

and

$$y(t) \;=\; \omega_o t \;+\; \theta_o \tag{A.2}$$

where ω_c is the carrier angular frequency, θ_c is an arbitrary phase offset angle for the carrier waveform, ω_o is the baseband angular frequency, and θ_o is an arbitrary phase offset angle

for the baseband waveform. The two angular frequencies (ω_c and ω_o) may not be multiple of each other.

Secondly, recall that any periodic waveform can be represented in terms of its harmonic components. Then, any periodic pulse-width modulated signal can be written as the summation of its Fourier coefficients (a_m and b_m) as

$$v_{PWM}(t) \;=\; \frac{a_0}{2} \;+\; \sum_{m\,=\,1}^{\infty} (a_m \cos mx \;+\; b_m \sin mx) \tag{A.3}$$

where

$$a_m \;=\; \frac{1}{\pi} \int_{-\pi}^{\pi} v_{PWM}(t) \cos mx \, dx \tag{A.4}$$

and

$$b_m \;=\; \frac{1}{\pi} \int_{-\pi}^{\pi} v_{PWM}(t) \sin mx \, dx \tag{A.5}$$

The pulse-width modulation analysis by duty cycle variation consists on the calculation of the coefficients a_0, a_m, and b_m, in equations (A.3), (A.4), and (A.5), by integrating the duty cycle of the resulting digital modulated signal within one cycle of the carrier waveform. The detailed derivations of the pulse-width modulated signals are presented in the next sections.

A.1. Pulse-Width Modulation Based on Sawtooth Carrier Waveform

The generation of the pulse-width modulated signal based on sawtooth carrier waveform is shown in Fig. 170. Observe that one cycle the carrier waveform has been normalized to one period equal to 2π (required for Fourier harmonic analysis), and the audio waveform has been expressed as Mcosy, where M is the modulation index. Notice that $f_c \gg f_o$, and, as mentioned before, the audio waveform can be considered constant within one cycle of the carrier waveform.

For the next step, it is necessary to find the integration limits in the equations (A.4)

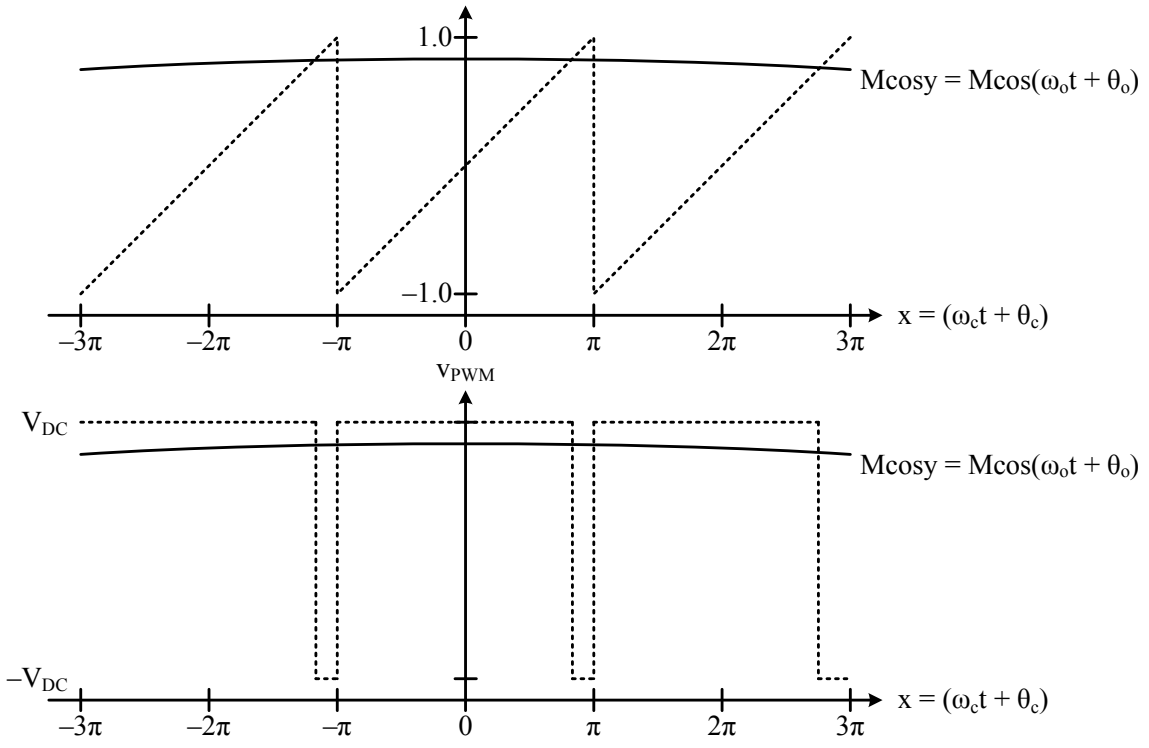


Fig. 170. Generation of pulse-width modulated signal by comparison of sawtooth carrier wave and audio input wave

and (A.5) for the duration of the duty cycle of the pulse-width modulated signal $v_{PWM}(t)$ within one cycle of the carrier waveform, i.e. $-\pi < x < \pi$. In other words, the lower integration limit is calculated when the value of the pulse-width modulated signal $v_{PWM}(t)$ goes high, i.e. when the duty cycle starts, and the higher integration limit is defined when the value of the pulse-width modulated signal $v_{PWM}(t)$ goes low, i.e. when the duty cycle ends. Therefore, the lower integration limit x_L is simply $-\pi$, and the higher integration limit is $x_H = \pi$Mcosy because it is the intersection point of the audio signal Mcosy and the carrier waveform, which can be viewed as a line with slope equal to $1 / \pi$. Then, equations (A.4)

and (A.5) become

$$a_m \;=\; \frac{1}{\pi}\int_{-\pi}^{\pi M\cos y} 2V_{DC}\cos mx\,dx \;=\; \frac{2}{m\pi}V_{DC}[\sin\left(m\pi M\cos y\right) \;+\; \sin m\pi] \quad \text{(A.6)}$$

and

$$b_m \;=\; \frac{1}{\pi}\int_{-\pi}^{\pi M\cos y} 2V_{DC}\sin mx\,dx \;=\; \frac{2}{m\pi}V_{DC}[\cos m\pi \;-\; \cos\left(m\pi M\cos y\right)] \quad \text{(A.7)}$$

when m $\neq$ 0. Notice that when m = 0

$$a_0 \;=\; 2V_{DC}(1 \;+\; M\cos y) \quad \text{(A.8)}$$

and

$$b_0 \;=\; 0 \quad \text{(A.9)}$$

Finally, substituting the equations (A.6), (A.7), and (A.8) into equation (A.3), and combining the resulting terms using the Bessel functions of the first kind $J(\cdot)_{(\cdot)}$ [26], the Fourier series of the pulse-width modulated signal based on sawtooth carrier waveform can be expressed as

$$\begin{aligned} v_{PWM}(t) \;&=\; V_{DC} \;+\; V_{DC}M\cos y \\ &+\; \frac{2}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\frac{1}{m}[\cos\left(m\pi\right) \;-\; J_0(m\pi M)\sin mx] \\ &+\; \frac{2}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\sum_{\substack{n\,=\,-\infty \\ (n\,\neq\,0)}}^{\infty}\frac{1}{m}J_n(m\pi M)\begin{bmatrix} \sin\left(n\frac{\pi}{2}\right)\cos\gamma \\ -\;\cos\left(n\frac{\pi}{2}\right)\sin\gamma \end{bmatrix} \end{aligned} \quad \text{(A.10)}$$

where γ was defined previously in equation (2.9). Observe that equation (A.10) gives the same result as equation (2.7) using the double Fourier integral analysis.

A.2. Pulse-Width Modulation Based on Triangle Carrier Waveform

The same procedure can be applied to generate the harmonic components of a pulse-width modulated signal based on triangular carrier waveform. The generation of the pulse-width modulated signal $v_{PWM}(t)$ based on triangular carrier waveform in illustrated in Fig. 171.

Following the same procedure as described above, it is necessary to find the integration limits of the equations (A.4) and (A.5). The intersection point which determines the lower integration limit x_L is giving by the relation

$$M \cos y \; = \; -\frac{2}{\pi} x_L \; - \; 1 \tag{A.11}$$

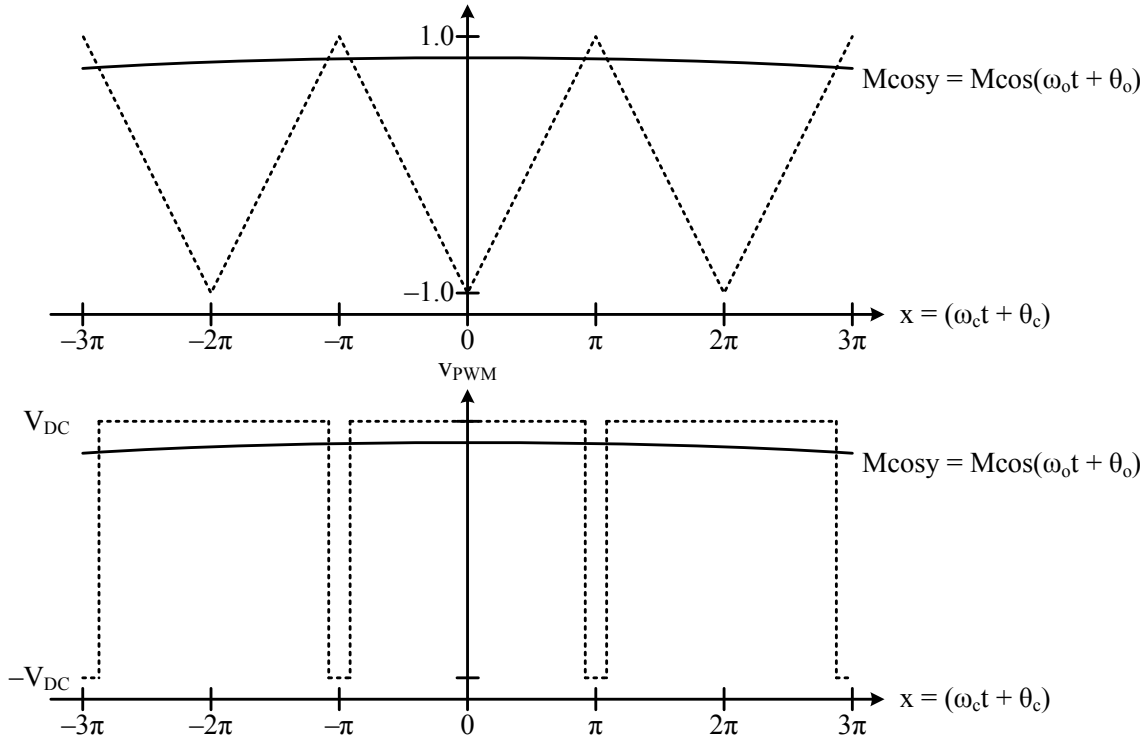


Fig. 171. Generation of pulse-width modulated signal by comparison of triangle carrier wave and audio input wave

because the triangular waveform can be seen as a line with slope -2 / π, shifted down by 1, from -π to 0. On the other hand, the higher integration limit x_H can be calculated by solving

$$M\cos y \;=\; \frac{2}{\pi}x_H \;-\; 1 \tag{A.12}$$

since in this case, the triangular waveform can be seen as a line with slope 2 / π, also shifted down by 1, from 0 to π.

Therefore, the coefficients in equations (A.4) and (A.5) can be calculated as

$$a_m \;=\; \frac{1}{\pi}\int_{-\frac{\pi}{2}(1\,+\,M\cos y)}^{\frac{\pi}{2}(1\,+\,M\cos y)} 2V_{DC}\cos mx\,dx \;=\; \frac{4}{m\pi}V_{DC}\sin\left(m\frac{\pi}{2}(1\;+\;M\cos y)\right) \tag{A.13}$$

when m $\neq$ 0, and

$$b_m \;=\; \frac{1}{\pi}\int_{-\frac{\pi}{2}(1\,+\,M\cos y)}^{\frac{\pi}{2}(1\,+\,M\cos y)} 2V_{DC}\sin mx\,dx \;=\; 0 \tag{A.14}$$

because the triangular carrier waveform is an even function. Also, notice that when m = 0

$$a_0 \;=\; 2V_{DC}(1\;+\;M\cos y) \tag{A.15}$$

Hence, substituting equations (A.13), (A.14), and (A.15) into the general equation (A.3), and after some mathematical manipulation, by employing the Bessel functions of the first kind $J(\cdot)_{(\cdot)}$, the Fourier series of the pulse-width modulated signal based on triangular carrier waveform can be expressed as

$$\begin{aligned} v_{PWM}(t) \;&=\; V_{DC} \;+\; V_{DC}M\cos y \\ &+\; \frac{4}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\frac{1}{m}J_0\left(m\frac{\pi}{2}M\right)\sin\left(m\frac{\pi}{2}\right)\cos mx] \\ &+\; \frac{4}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\sum_{\substack{n\,=\,-\infty \\ (n\,\neq\,0)}}^{\infty}\frac{1}{m}J_n\left(m\frac{\pi}{2}M\right)\sin\left([m\;+\;n]\frac{\pi}{2}\right)\cos\gamma \end{aligned} \tag{A.16}$$

where γ is defined in equation (2.9). Observe that equation (A.16) is identical to equation

(2.8), which was calculated by using the double Fourier integral analysis.

Based on the two previous cases, the simplicity of the pulse-width modulation analysis by duty cycle variation is evident. Therefore, the same analysis can be generalized to quantify the harmonic distortion of an open-loop class D amplifier for any given periodic carrier waveform. Such analysis provides very useful information in order to determine the required specifications of the carrier waveform generator for a targeted linearity.

A.3. Pulse-Width Modulation Based on Bandlimited Carrier Waveforms

The pulse-width modulation based on both, sawtooth and triangle, carrier signals assumes perfect waveforms. In reality, since these carrier waveforms have infinite bandwidth, as shown in equations (2.10) and (2.11), the non-ideal carrier waveforms produces unwanted baseband harmonic distortion at the output of the class D audio power amplifier. The amount of harmonic distortion can be quantified by analyzing the pulse-width modulated signal by duty cycle variation.

In general, the coefficients a_m and b_m in equation (A.3) can be calculated by evaluating the integrals expressed in equations (A.4) and (A.5) from x_L to x_H as

$$a_m = \frac{1}{\pi}\int_{x_L}^{x_H} v_{PWM}(t)\cos mx\,dx \tag{A.17}$$

and

$$b_m = \frac{1}{\pi}\int_{x_L}^{x_H} v_{PWM}(t)\sin mx\,dx \tag{A.18}$$

within one period of the carrier waveform, i.e. $-\pi < x < \pi$, where the integration limits can be found by solving the equations

$$M\cos y = \frac{1}{2} - \frac{1}{\pi}\sum_{k=1}^{\infty}\frac{1}{k}\sin kx_L \tag{A.19}$$

$$M\cos y \;=\; \frac{1}{2} - \frac{1}{\pi}\sum_{k\,=\,1}^{\infty}\frac{1}{k}\sin kx_H \tag{A.20}$$

for a bandlimited sawtooth carrier waveform, and

$$M\cos y \;=\; \frac{8}{\pi^2}\sum_{k\,=\,1,3,5,\ldots}^{\infty}\frac{(-1)^{(k\,-\,1)\,/\,2}}{k^2}\sin kx_L \tag{A.21}$$

$$M\cos y \;=\; \frac{8}{\pi^2}\sum_{k\,=\,1,3,5,\ldots}^{\infty}\frac{(-1)^{(k\,-\,1)\,/\,2}}{k^2}\sin kx_L \tag{A.22}$$

for a bandlimited triangle carrier waveform.

Unfortunately, the evaluation of the integrals expressed in equations (A.17) and (A.18), for $1 < \mathrm{k} < \infty$, must be done numerically because they cannot be expressed in a closed-form expression. However, when there is only one harmonic component in the carrier waveform, k = 1, the production of the pulse-width modulated signal is based on a pure sinusoidal carrier waveform, and its solution can be expressed in closed form. For example, Fig. 172 shows the generation of the pulse-width modulated signal $v_{PWM}(t)$ when the triangular carrier waveform contains only one harmonic component.

For this particular case, the integration limits can be found by solving

$$M\cos y \;=\; -\frac{8}{\pi^2}\cos x_{L,H} \tag{A.23}$$

for k = 1 in equations (A.21) and (A.22), as

$$x_{L,H} \;=\; \mp\arccos\left(-\frac{\pi^2}{8}M\cos y\right) \tag{A.24}$$

and the resulting Fourier series is the pulse-width modulated signal

$$\begin{aligned} v_{PWM}(t) \;&=\; 2V_{DC}\arccos\left(\arcsin\left[2\sum_{n\,=\,1}^{\infty}\sin\left(n\frac{\pi}{2}\right)J_n\left(-\frac{1}{8}\pi^2 M\right)\cos ny\right]\right) \\ &+\; \frac{4}{\pi}V_{DC}\sum_{m\,=\,1}^{\infty}\sin\left(m\arccos\left[-\frac{1}{8}\pi^2 M\cos y\right]\right)\cos mx \end{aligned} \tag{A.25}$$

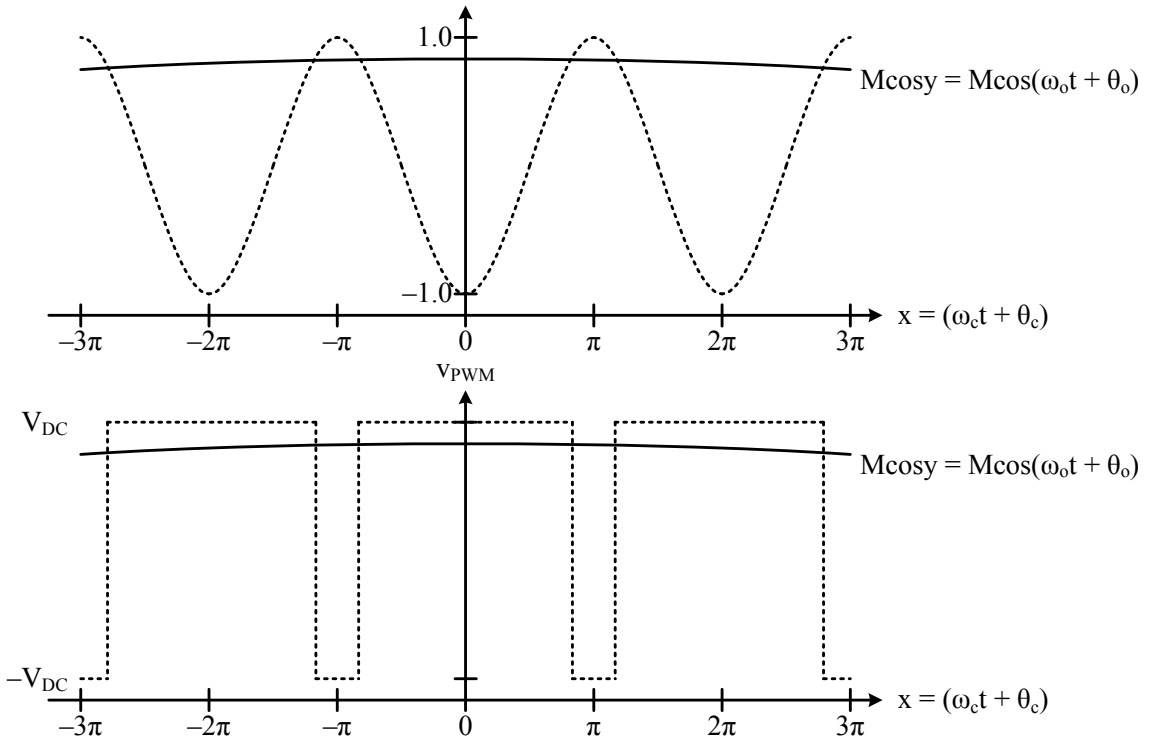


Fig. 172. Generation of pulse-width modulated signal by comparison of cosine carrier wave and audio input wave

which has already been presented in equation (2.12), and is repeated here for completeness.

A.4. Pulse-Width Modulation Based on Exponential-Shaped Carrier Waveforms

The analysis of pulse-width modulated signals can be extended to the set of exponential-shaped carrier waveforms defined by equation (2.13). For example, the generation of the pulse-width modulated signal $v_{PWM}(t)$ with a particular exponential-shaped carrier waveform is shown in Fig. 173.

The calculation of the Fourier coefficients for this particular modulation also requires to find the integration limits in equations (A.17) and (A.18) for the coefficients a_0, a_m,

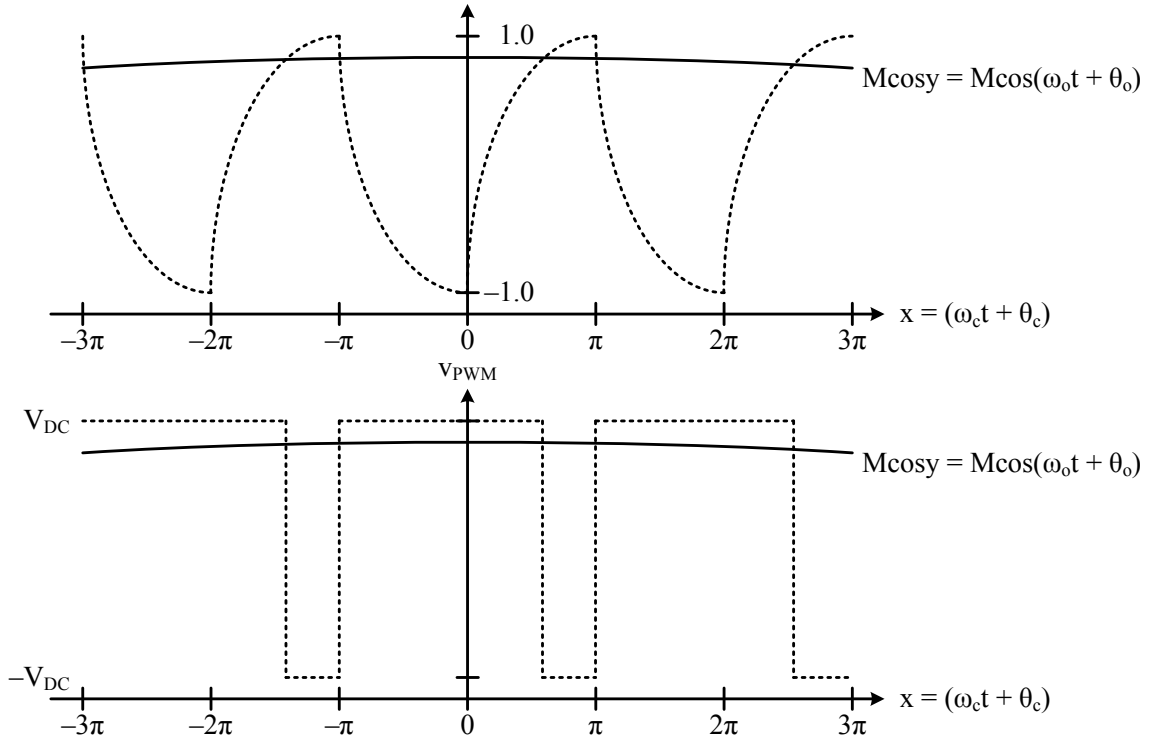


Fig. 173. Generation of pulse-width modulated signal by comparison of exponential-shaped carrier wave and audio input wave

and b_m. Therefore, the intersection points $x_{L,H}$ can be found by equating the sinusoidal audio signal (Mcosy) with the exponential function in equation (2.13) for the subintervals $-\pi < x < 0$ and $0 < x < \pi$. The resulting integration limits are

$$x_L = -\pi - t_0 \ln\left(\frac{M}{2V_{DC}}(1 - N_e)\cos y + \frac{(1 + N_e)}{2}\right) \tag{A.26}$$

$$x_H = -t_0 \ln\left(1 - \frac{1}{2}(1 - N_e)\left[\frac{M}{V_{DC}}\cos y + 1\right]\right) \tag{A.27}$$

and the resulting pulse-width modulated signal $v_{PWM}(t)$ is expressed in equation (2.15) with coefficients a_0, a_m, and b_m specified in equations (2.16), (2.17), and (2.18).

As mentioned before, the analysis of harmonic distortion in class D audio power

amplifiers can be extended to any periodic carrier waveform and even to architectures with multilevel pulse-width modulation.

APPENDIX B

FUNDAMENTALS OF SLIDING MODE CONTROL

This appendix presents the fundamentals of sliding mode control (SMC) theory. It begins with an introductory example to illustrate its principles of operation, and to highlight its main characteristics. Additionally, a formal description of the sliding mode controller, and the switching function, is given. Furthermore, the analysis of stability, based on the Lyapunov function approach and the equivalent control approach, is explained. Finally, the derivation of the switching function and the stability proof, for the particular case of the second-order low-pass filter employed in the design of the systems described in this dissertation, are detailed.

B.1. An Introductory Example

The first developments of sliding mode control (SMC) occurred in the 1950s as a consequence of the analysis of discontinuous variable structure systems (VSS). A variable structure system consists of a set of continuous subsystems together with a switching logic. Therefore, the variable structure control (VSC) with sliding modes consists on selecting the parameters of each one of these substructures to define the switching logic of the system. The most outstanding feature of variable structure control is its ability to result in very robust control systems, insensitive to parametric uncertainty, and external disturbances [33]–[36].

The basic idea of variable structure control with sliding modes, or simply sliding mode control, can be illustrated by analyzing the second order system shown in Fig. 174. The

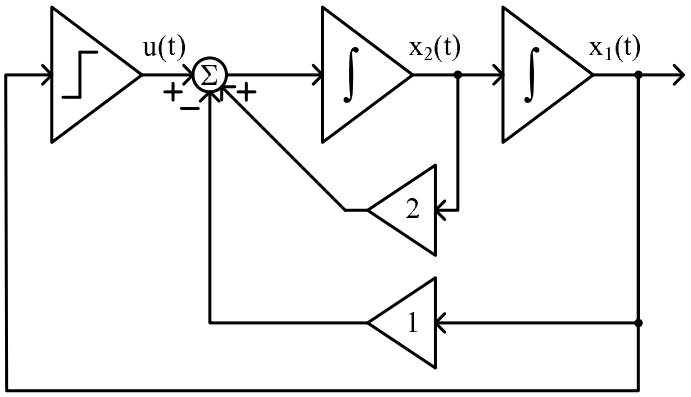


Fig. 174. Model of a simple variable structure system

system can be expressed in terms of its state variables as

$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ -1 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} + \begin{pmatrix} 0 \\ 1 \end{pmatrix} u(t) \tag{B.1}$$

where

$$u(t) = \begin{cases} 4 & \text{when} \quad s(x_1, x_2, t) > 0 \\ -4 & \text{when} \quad s(x_1, x_2, t) < 0 \end{cases} \tag{B.2}$$

and s(x_1, x_2, t), defined as

$$s(x_1, x_2, t) = x_1(t)\left(\frac{1}{2}x_1(t) + x_2(t)\right) \tag{B.3}$$

represents the switching function, which will be defined later in the appendix.

Therefore, the second-order system, in equation (B.1), is analytically defined in two regions of the phase plane, i.e. the x_1-x_2 plane, by two different mathematical models. The

first model, when $s(x_1, x_2, t) < 0$, is

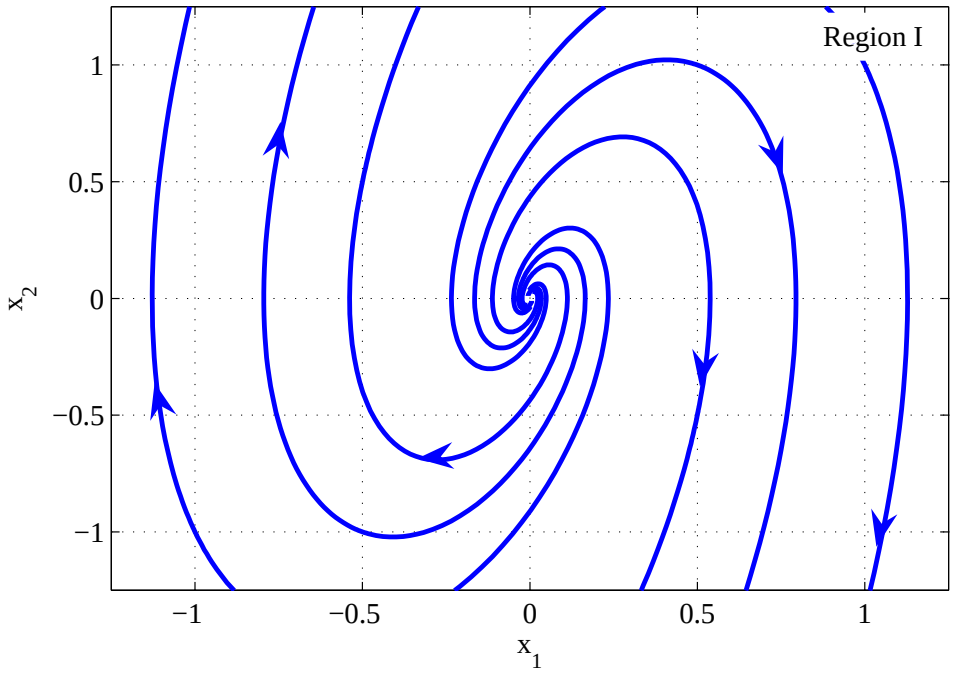
$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ -5 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} \tag{B.4}$$

and the second model, when $s(x_1, x_2, t) > 0$, is

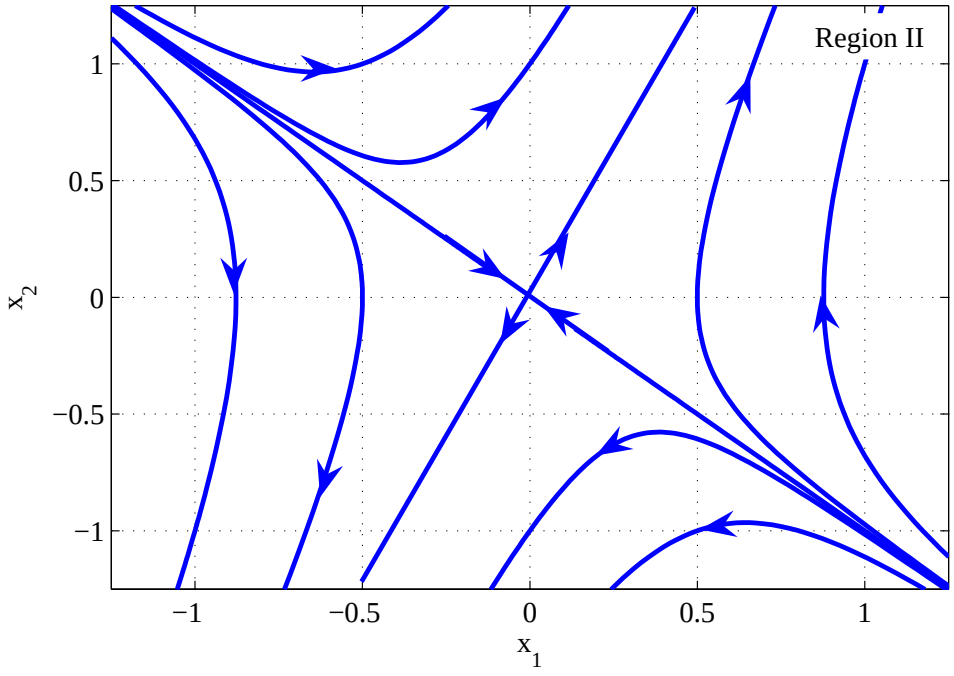
$$\begin{pmatrix} \frac{d}{dt}x_1(t) \\ \frac{d}{dt}x_2(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 \\ 3 & 2 \end{pmatrix} \begin{pmatrix} x_1(t) \\ x_2(t) \end{pmatrix} \tag{B.5}$$

The phase portraits, i.e. the trajectories of the state-space variables in the phase plane for different initial conditions, for the models in equations (B.4) and (B.5) are shown in Fig. 175. Figure 175(a) corresponds to the state-space model in equation (B.4) and represents the first region of operation, i.e. region I. Observe that the equilibrium point is an unstable focus [36], i.e. positive eigenvalues with imaginary part, at the origin. On the other hand, the second region of operation, or region II, is represented by the phase portrait, of the state space model expressed in equation (B.5), in Fig. 175(b). Notice that, in this case, its equilibrium point, at the origin, is a saddle point [36], i.e. one positive and one negative real eigenvalues, and therefore, it is stable for only one trajectory.

The variable $s(x_1, x_2, t)$ in equation (B.3) describes lines dividing the phase plane into the regions of operation where $s(x_1, x_2, t)$ has different sign. Such lines are called switching lines and $s(x_1, x_2, t)$ is called the switching function. The switching lines occur whenever $s(x_1, x_2, t) = 0$ and are known as the switching surfaces. Hence, the feedback control $u(t)$ switches according to the sign of $s(x_1, x_2, t)$. For example, the switching function in equation (B.3) defines the phase portrait, of the second-order system in equation (B.1), as illustrated in Fig. 176. The phase plane is divided into regions of operation, each one of them linked to the state-space systems in equations (B.4) and (B.5). The switching function controls the switching logic to stabilize the system for any given initial condition.



(a)



(b)

Fig. 175. Phase portraits of the second-order system in equation (B.1) for (a) Region I when $s(x_1, x_2, t) < 0$ and (b) Region II when $s(x_1, x_2, t) > 0$

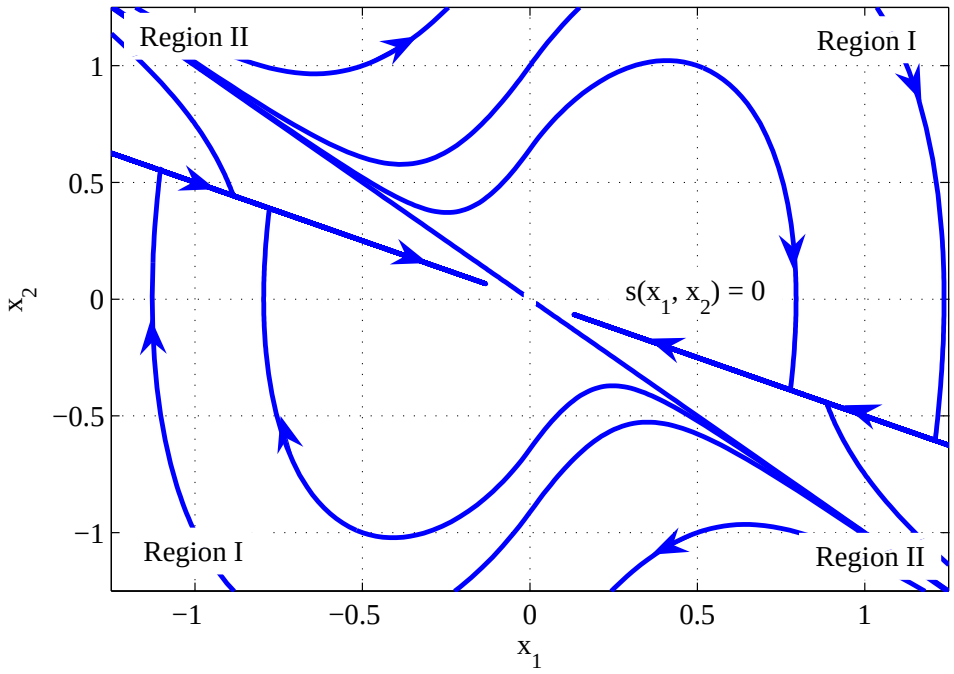


Fig. 176. Phase portrait of the second-order system in equation (B.1) with sliding mode

The phase trajectories, plotted in the phase portrait of Fig. 176, correspond to the two modes of operation of the system. The first part is the reaching mode, also called nonsliding mode, in which a trajectory starting at any initial condition moves toward a switching line and reaches the line in finite time. The second part is the sliding mode, in which the trajectory asymptotically tends to the origin of the phase plane. This displacement is called sliding because in the ideal case, the system switches at infinite frequency, causing a sliding behavior of the particular trajectory. During the control process, the variable structure system, in equation (B.1), varies from one structure to another, thus earning the name variable structure control. The control is also called sliding mode control to emphasize the important role of sliding mode [33]–[36].

B.2. Sliding Mode Controller

The switching function represents the sliding mode controller, i.e. the control law, of a variable structure system. Hence, if the variable structure system is expressed in the controllable canonical form [114]–[116] as

$$\frac{d}{dt}\mathbf{x}(t) \;=\; \mathbf{A}\mathbf{x}(t) \;+\; \mathbf{B}u(t) \tag{B.6}$$

$$y(t) \;=\; \mathbf{C}\mathbf{x}(t) \tag{B.7}$$

where

$$\mathbf{x}(t) \;=\; \begin{pmatrix} x_1(t) \\ x_2(t) \\ \vdots \\ x_{n\,-\,1}(t) \\ x_n(t) \end{pmatrix} \tag{B.8}$$

$$\mathbf{A} \;=\; \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ -a_1 & -a_2 & -a_3 & \cdots & -a_n \end{pmatrix} \tag{B.9}$$

$$\mathbf{B} \;=\; \begin{pmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{pmatrix} \tag{B.10}$$

$$\mathbf{C} \;=\; \begin{pmatrix} c_1 & c_2 & \cdots & c_n \end{pmatrix} \tag{B.11}$$

and $x_n(t)$, u(t), and y(t) are the state variables of the system, the control input, and the output of the system, respectively. Then, the function

$$\mathbf{s}(\mathbf{x}, t) \;=\; k_1 x_1(t) \;+\; k_2 x_2(t) \;+\; \cdots \;+\; k_n x_n(t) \tag{B.12}$$

defines the switching surfaces in the n^{th} space, when **s**(**x**, t) = 0. The coefficients in the switching function define the characteristic equation of the sliding mode if the system model is described in the controllable canonical form [33]–[36].

In the same way, the control law can be designed such that the output of the system y(t) asymptotically tracks a reference signal r(t). Therefore, if the variable structure system is rewritten with

$$\begin{pmatrix} \dot{e}_1(t) \\ \dot{e}_2(t) \\ \vdots \\ \dot{e}_{n-1}(t) \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \end{pmatrix} \begin{pmatrix} e_1(t) \\ e_2(t) \\ \vdots \\ e_n(t) \end{pmatrix} \tag{B.13}$$

where $e_1(t)$ = r(t) - y(t) is the error function, $e_n(t)$ is the control input, and n is the order of the system to be controlled. The control input, defined in equation (B.14), is the linear combination of all canonical state variables [35], [36], and whose coefficients are chosen in such way that the polynomial, in equation (B.15), meets the Hurwitz criterion [114]–[116], i.e. all its roots have negative real part.

$$e_n(t) \;=\; -\left[k_1 e_1(t) \;+\; k_2 e_2(t) \;+\; \cdots \;+\; k_{n-1} e_{n-1}(t)\right] \tag{B.14}$$

$$P(s) \;=\; k_n s^{n-1} \;+\; k_{n-1} s^{n-2} \;+\; \cdots \;+\; k_1 \tag{B.15}$$

Then, the switching function in equation (B.16) represents the (n - 1) dimensional

surface where the points of discontinuity merge [35].

$$\mathbf{s}(\mathbf{e}, t) \;=\; k_1 e_1(t) \;+\; k_2 e_2(t) \;+\; \cdots \;+\; k_{n\,-\,1} e_{n\,-\,1}(t) \;+\; k_n e_n(t) \;=\; 0 \qquad \text{(B.16)}$$

B.3. Stability Analysis

Variable structure systems operating under sliding mode control consist of two parts, the reaching mode and the sliding mode. Therefore, the analysis of stability must demonstrate that (1) the trajectory of a given state moves toward and reaches the sliding surface, and (2) the state asymptotically tends to the equilibrium point of the system.

B.3.1. Reaching Mode Condition

The reaching mode condition can be analyzed by employing the Lyapunov function approach [35]. Hence, by choosing the Lyapunov function candidate

$$\mathbf{v}(\mathbf{x}, t) \;=\; \frac{1}{2}\mathbf{s}^T(\mathbf{x}, t)\mathbf{s}(\mathbf{x}, t) \qquad \text{(B.17)}$$

a global reaching condition is given by

$$\frac{d}{dt}\mathbf{v}(\mathbf{x}, t) \;<\; 0 \qquad \text{(B.18)}$$

when **s**(**x**, t) $\neq$ 0 [35], [36].

B.3.2. Sliding Mode Condition

The convergence of a variable structure system to its equilibrium point, also called sliding equilibrium point or quasiequilibirum point [56], can be found by analyzing the qualitative behavior [36], i.e. calculating the eigenvalues, of the equivalent variable structure system when

$$\frac{d}{dt}\mathbf{x}(t) \;=\; \mathbf{A}\mathbf{x}(t) \;+\; \mathbf{B}u_{eq}(t) \;=\; 0 \qquad \text{(B.19)}$$

$$\mathbf{s}(\mathbf{x}, t) \;=\; 0 \tag{B.20}$$

where $u_{eq}(t)$ is the equivalent control input that describes the dynamics of the sliding mode as the average value of the discontinuous input u(t) [56]. Hence, if the switching function **s**(**x**, t) is expressed in terms of the state variables as

$$\mathbf{s}(\mathbf{x}, t) \;=\; \mathbf{D}(\mathbf{x}, t) \;+\; \mathbf{E}(\mathbf{x}, t)u(t) \tag{B.21}$$

then, the equivalent control control can be found when the state trajectory stays on the switching surface **s**(**x**, t) = 0 [35]. Therefore, differentiating **s**(**x**, t) with respect to time gives

$$\frac{d}{dt}\mathbf{s}(\mathbf{x}, t) \;=\; \frac{\partial}{\partial \mathbf{x}}\frac{d}{dt}\mathbf{D}(\mathbf{x}, t) \;+\; \frac{\partial}{\partial \mathbf{x}}\frac{d}{dt}\mathbf{E}(\mathbf{x}, t)u(t) \tag{B.22}$$

and solving equation (B.22) for u(t) yields the equivalent control input $\mathbf{u_{eq}}$(**x**, t) [35] as

$$\mathbf{u_{eq}}(\mathbf{x}, t) \;=\; -\left(\frac{\partial}{\partial \mathbf{x}}\frac{d}{dt}\mathbf{E}(\mathbf{x}, t)\right)^{-1}\frac{\partial}{\partial \mathbf{x}}\frac{d}{dt}\mathbf{D}(\mathbf{x}, t) \tag{B.23}$$

B.4. Practical Derivation of the Switching Function and Stability Analysis

If the variable structure system, as described in previous chapters, is defined by the second-order state-space system given by

$$\begin{pmatrix} \frac{d}{dt}i_L(t) \\ \frac{d}{dt}v_C(t) \end{pmatrix} \;=\; \begin{pmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix}\begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} \;+\; \begin{pmatrix} \frac{1}{L} \\ 0 \end{pmatrix}u(t) \tag{B.24}$$

with an error function $e_1(t) = v_{REF}(t) - v_C(t)$, then, from equations (B.13) and (B.14), we have

$$\frac{d}{dt}\,e_1(t) = \; e_2(t) \tag{B.25}$$

$$e_2(t) \;=\; -\,k_1 e_1(t) \tag{B.26}$$

and the switching function $s(e_1, e_2, t)$, from equation (B.16), is defined as

$$s(e_1, e_2, t) \;=\; k_1 e_1(t) \;+\; k_2 e_2(t) \tag{B.27}$$

where k_1 and k_2 must be chosen such that the polynomial $P(s) = k_2 s + k_1$, from equation (B.15), is Hurwitz. Therefore, the control input u(t) switches according to

$$u(t) \;=\; \begin{cases} v_{DD} & \text{when} \quad s(e_1, e_2, t) \;>\; 0 \\ v_{SS} & \text{when} \quad s(e_1, e_2, t) \;<\; 0 \end{cases} \tag{B.28}$$

Hence, the switching function in equation (B.27) can be rewritten as a function of the state-space variables as

$$s(e_1, e_2, t) \;=\; e_1(t) \;+\; \alpha e_2(t) \;=\; v_{REF}(t) \;-\; v_C(t) \;-\; \alpha \frac{d}{dt} v_C(t) \tag{B.29}$$

and the derivative of the switching function, from equation (B.22), is

$$\begin{aligned} \dot{s}(e_1, e_2, t) \;&=\; \frac{1}{C}\left(\frac{\alpha}{RC} \;-\; 1\right) i_L(t) \\ &-\; \left[\frac{1}{RC}\left(\frac{\alpha}{RC} \;-\; 1\right) \;-\; \frac{\alpha}{LC}\right] v_C(t) \;-\; \frac{\alpha}{LC} u(t) \end{aligned} \tag{B.30}$$

The analysis of stability based on the Lyapunov function approach assumes the control signal u(t) can be decomposed into two parts

$$u(t) \;=\; u_{eq}(t) + u_{nl}(t) \tag{B.31}$$

where $u_{eq}(t)$ is the equivalent control input, and $u_{nl}(t)$ is the nonlinear switching function, i.e. the high-frequency component. Therefore, the equivalent control input, defined in equation (B.23), for this particular case is

$$u_{eq}(t) \;=\; \begin{pmatrix} \frac{L}{\alpha}\left[\frac{\alpha}{RC} \;-\; 1\right] & 1 \;-\; \frac{L}{\alpha R}\left[\frac{\alpha}{RC} \;-\; 1\right] \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} \tag{B.32}$$

hence, substituting equations (B.28) and (B.32) into equation (B.30) yields

$$\dot{s}(e_1, e_2, t) \;=\; -\frac{\alpha}{CL} u_{nl}(t) \tag{B.33}$$

Therefore, the Lyapunov function candidate, from equation (B.17), becomes

$$v(e_1, e_2, t) \;=\; \frac{1}{2} s^2(e_1, e_2, t) \tag{B.34}$$

and the global reaching condition is

$$\frac{d}{dt} v(e_1, e_2, t) \;=\; s(e_1, e_2, t)\dot{s}(e_1, e_2, t) \;=\; s(e_1, e_2, t)\left(-\frac{\alpha}{CL} u_{nl}(t)\right) \;<\; 0 \tag{B.35}$$

when $s(e_1, e_2, t) \neq 0$. Simplifying and rearranging we get

$$s(e_1, e_2, t) u_{nl}(t) \;>\; 0 \tag{B.36}$$

Hence, based on equations (B.28) and (B.31), when $s(e_1, e_2, t) > 0$, then $u(t) = v_{DD}$ and thus $v_{DD} = u_{eq} + u_{nl}$, therefore, if $v_{DD} - u_{eq} > 0$, it implies that $u_{nl} > 0$ and

$$[s(e_1, e_2, t)][u_{nl}(t)] \;>\; 0 \tag{B.37}$$

for $s(e_1, e_2, t) > 0$. On the other hand, when $s(e_1, e_2, t) < 0$, then $u(t) = v_{SS}$, so $v_{SS} = u_{eq} + u_{nl}$, this implies that if $v_{SS} - u_{eq} < 0$, therefore $u_{nl} < 0$ and

$$[-s(e_1, e_2, t)][-u_{nl}(t)] \;>\; 0 \tag{B.38}$$

for $s(e_1, e_2, t) < 0$. Then, if $v_{SS} < u_{eq} < v_{DD}$ holds, the control law ensures the reaching condition. Since we know that u_{eq} is the low-frequency average signal that tracks the reference input v_{ref}, then the last inequality is true.

On the other hand, the sliding mode condition can be proven if the sliding equilibrium point of the equivalent control system is found, and its eigenvalues have negative real part. Therefore, the equivalent input control input in equation (B.32) is substituted in the state-

space model in equation (B.24) as

$$\begin{pmatrix} \frac{d}{dt}i_L(t) \\ \frac{d}{dt}v_C(t) \end{pmatrix} = \begin{pmatrix} \frac{1}{\alpha}\left(\frac{\alpha}{RC} - 1\right) & -\frac{1}{\alpha R}\left(\frac{\alpha}{RC} - 1\right) \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L(t) \\ v_C(t) \end{pmatrix} \tag{B.39}$$

Then, as shown in equations (B.19) and (B.20), if the resulting equivalent control system, along with the switching function are solved, when they are equal to zero, the sliding equilibrium point yields

$$[v_C(t), i_L(t)] = \left[v_{REF}(t), \frac{v_{REF}(t)}{R}\right] \tag{B.40}$$

The sliding equilibrium point corresponds to the desired voltage $v_{REF}(t)$ at the output second-order low-pass filter. Assuming that $v_C(t) = v_{OUT}(t)$, the sliding mode controller will track the trajectory of the input signal $v_{REF}(t)$. Similarly, the value of the inductor current $i_L(t)$ will be defined by the output voltage divided by the resistive load.

The value of the eigenvalues in the equivalent control model can be calculated to show that the system converges to the sliding equilibrium point. Therefore, solving for $v_C(t)$ in equation (B.29), when $s(e_1, e_2, t) = 0$, and substituting into the equivalent control model expressed in equation (B.39), the eigenvalues (λ) of the equivalent system are

$$\lambda_{1,2} = \left(-\frac{1}{\alpha}, -\frac{1}{RC}\right) \tag{B.41}$$

Thus, the system is asymptotically stable since its sliding equilibrium point is a node whose eigenvalues are real and negative, for $\alpha > 0$.

Furthermore, the final value theorem (FVT) [115] can be used in order to calculate the steady-state of the model to verify that system under sliding mode is in fact a tracking system. In general, the final value of a given system y(t) can be determined as

$$\lim_{t \to \infty} y(t) = \lim_{s \to 0} sY(s) \tag{B.42}$$

The transfer function of the equivalent control model, resulting from the combination of equations (B.29) and (B.39), is

$$\frac{V_{OUT}(s)}{V_{REF}(s)} = \frac{1}{(\alpha s + 1)(RCs + 1)} \tag{B.43}$$

which agrees with the results given in equation (B.41) for the eigenvalues of the equivalent control model.

Applying the final value theorem to equation (B.43) with a step input of value v_{STEP} to the system we have

$$\begin{aligned} \lim_{t \to \infty} v_{OUT}(t) &= \lim_{s \to 0} sV_{OUT}(s) \\ &= \lim_{s \to 0} \left(\frac{s}{(\alpha s + 1)(RCs + 1)} \right) \left(\frac{V_{STEP}}{s} \right) \\ &= v_{STEP} \end{aligned} \tag{B.44}$$

Hence, the equivalent control model tracks the input input step signal v_{STEP}.

APPENDIX C

CALCULATION OF SWITCHING FREQUENCY IN CLASS D AUDIO POWER AMPLIFIER OPERATING UNDER SLIDING MODE

This appendix derives the expressions for the calculation of the switching frequency in class D audio power amplifiers operating under sliding mode. The analysis is done by assuming a steady state operation of the amplifier and a constant load R. The derivations are calculated for two different cases: (1) when an amplifier is operating under ideal sliding mode, and (2) when the amplifier is based on a lossy sliding mode. Also, for this analysis, the output stage and second-order filter are assuming to be described by the second-order state space system defined in Appendix B as equation (B.24).

C.1. Class D Audio Power Amplifier Operating Under Ideal Sliding Mode

A magnified view of the class D audio power amplifier operating under ideal sliding mode has been shown in Fig. 73. The time duration of subintervals Δt_1 and Δt_2 can be calculated [60] as

$$\Delta t_1 \;=\; \frac{2\kappa}{\dfrac{d}{dt}s(e_1,t)} \;=\; \frac{2\kappa}{\dfrac{d}{dt}\left(e_1(t) \;+\; \alpha\dfrac{d}{dt}e_1(t)\right)} \tag{C.1}$$

when $v_{IN} = v_{PWM-} = 0$, and

$$\Delta t_2 \;=\; \frac{-2\kappa}{\dfrac{d}{dt}s(e_1,t)} \;=\; \frac{-2\kappa}{\dfrac{d}{dt}\left(e_1(t) \;+\; \alpha\dfrac{d}{dt}e_1(t)\right)} \tag{C.2}$$

when $v_{IN} = v_{PWM+} = v_{DD}$. Therefore, the time period for one cycle of operation is giving by

$$T_{s,ideal} \;=\; \Delta t_1 \;+\; \Delta t_2 \;=\; \frac{2\kappa}{\varphi} \;-\; \frac{2\kappa}{\varphi \;-\; \dfrac{\alpha}{LC}v_{DD}} \tag{C.3}$$

where

$$\varphi \;=\; \frac{1}{C}\left(\frac{\alpha}{RC} \;-\; 1\right) i_L \;-\; \left(\frac{1}{RC}\left(\frac{\alpha}{RC} \;-\; 1\right) \;-\; \frac{\alpha}{LC}\right) v_C \tag{C.4}$$

and the switching frequency is simply the inverse of equation (C.3)

$$f_{s,ideal} \;=\; \frac{\varphi\left(\varphi \;-\; \dfrac{\alpha}{LC} v_{DD}\right)}{-2\kappa \dfrac{\alpha}{LC} v_{DD}} \tag{C.5}$$

Hence, if we substitute the value of the derivative constant by α = RC $\approx 5.625 \times 10^{-6}$, the equation (C.5) reduces to

$$f_{s,ideal} \;=\; \frac{1}{2\kappa}\frac{R}{L} v_C \left(1 \;-\; \frac{v_C}{v_{DD}}\right) \tag{C.6}$$

as expressed previously in equation (4.12).

C.2. Class D Audio Power Amplifier Operating Under Lossy Sliding Mode

In practice, the sliding mode controller is implemented with a lossy differentiator to bound the bandwidth of the class D audio power amplifier and to limit the high-frequency noise. Hence, the switching frequency of the class D audio power amplifier operating under a lossy switching function becomes inversely proportional to the frequency of the extra pole added.

The derivation of the expression of the switching frequency with a lossy-differentiator follows the same procedure as the ideal case, but, in this case, considering the lossy-switching function s(e_1, t). Firstly, the lossy-switching function, in equation (4.4), can be rewritten, using the partial-fraction expansion method, as

$$\begin{aligned} S(E_1, s) \;&=\; \left[1 \;+\; \left(\frac{\alpha s}{\dfrac{1}{\omega_p} s \;+\; 1}\right)\right] E_1(s) \;=\; \left[1 \;+\; \left(\frac{\alpha s}{\dfrac{\alpha}{\gamma} s \;+\; 1}\right)\right] E_1(s) \\ &=\; \left[(1 \;+\; \gamma) \;-\; \frac{\gamma^2}{\alpha}\left(\frac{\alpha}{s \;+\; \dfrac{\gamma}{\alpha}}\right)\right] E_1(s) \end{aligned} \tag{C.7}$$

Then, the lossy-switching function in equation (C.7) can be expressed in the time domain, applying the inverse Laplace transform, as

$$\begin{aligned} s(e_1,t) &= \mathscr{L}^{-1}[S(E_1,s)] \\ &= (1\ +\ \gamma)e_1(t)\ -\ \frac{\gamma^2}{\alpha}\exp\left(-\frac{\gamma}{\alpha}t\right) * e_1(t) \\ &= (1\ +\ \gamma)e_1(t)\ -\ \frac{\gamma^2}{\alpha}\int_{-\infty}^{\infty}\exp\left(-\frac{\gamma}{\alpha}(t\ -\ \tau)\right)e_1(\tau)\,d\tau \\ &= (1\ +\ \gamma)e_1(t)\ -\ \frac{\gamma^2}{\alpha}\exp\left(-\frac{\gamma}{\alpha}t\right)\int_{0}^{t}\exp\left(\frac{\gamma}{\alpha}\tau\right)e_1(\tau)\,d\tau \\ &= (1\ +\ \gamma)e_1(t)\ -\ \frac{\gamma^2}{\alpha}\exp\left(-\frac{\gamma}{\alpha}t\right)g(t) \end{aligned} \tag{C.8}$$

where

$$\begin{aligned} g(t) &= \exp\left(\frac{\gamma}{\alpha}t\right)\sum_{n\,=\,1}^{\infty}(-1)^{(n\,-\,1)}\left(\frac{\alpha}{\gamma}\right)^{n} e_1^{(n\,-\,1)}(t) \\ &\quad -\ \sum_{n\,=\,1}^{\infty}(-1)^{(n\,-\,1)}\left(\frac{\alpha}{\gamma}\right)^{n} e_1^{(n\,-\,1)}(0) \end{aligned} \tag{C.9}$$

Rearranging terms and simplifying, we have

$$\begin{aligned} s(e_1,t) &= (1\ +\ \gamma)e_1(t) \\ &\quad -\ \sum_{n\,=\,1}^{\infty}(-1)^{(n\,-\,1)}\left(\frac{\alpha^{(n\,-\,1)}}{\gamma^{(n\,-\,2)}}\right) e_1^{(n\,-\,1)}(t) \\ &\quad +\ \exp\left(-\frac{\gamma}{\alpha}t\right)\sum_{n\,=\,1}^{\infty}(-1)^{(n\,-\,1)}\left(\frac{\alpha^{(n\,-\,1)}}{\gamma^{(n\,-\,2)}}\right) e_1^{(n\,-\,1)}(0) \end{aligned} \tag{C.10}$$

The resulting equation (C.10) is an infinite sum of derivative functions, but can be rewritten, for simplicity, by only taking the first three coefficients in the summation terms, as follows

$$\begin{aligned} s(e_1,t) &\approx \left[e_1(t)\ +\ \alpha\frac{d}{dt}e_1(t)\ -\ \frac{\alpha^2}{\gamma}\frac{d^2}{dt^2}e_1(t)\right] \\ &\quad +\ \exp\left(-\frac{\gamma}{\alpha}t\right)\left[\gamma e_1(0)\ -\ \alpha\frac{d}{dt}e_1(0)\ +\ \frac{\alpha^2}{\gamma}\frac{d^2}{dt^2}e_1(0)\right] \end{aligned} \tag{C.11}$$

and whose derivative, assuming α = RC $\approx 5.625 \times 10^{-6}$, is

$$\begin{aligned} \frac{d}{dt}s(e_1,t) \;&\approx\; \frac{R}{L}(v_C \;-\; v_{IN}) + \frac{1}{\gamma}\left[\frac{1}{2C}i_L \;-\; \frac{R}{L}v_{IN}\right] \\ &-\; \exp\left(\frac{\gamma}{\alpha}t\right)\left[\frac{\gamma^2}{\alpha}e_1(0) \;-\; \gamma\frac{d}{dt}e_1(0) \;+\; \alpha\frac{d^2}{dt^2}e_1(0)\right] \end{aligned} \tag{C.12}$$

However, equation (C.12) depends on the initial condition of the error function and its derivatives, which are unknown. Therefore, the derivative of the lossy-switching function is approximated to

$$\frac{d}{dt}s(e_1,t) \;\approx\; \frac{R}{L}(v_C \;-\; v_{IN}) + \frac{1}{\gamma}\left[\frac{1}{2C}i_L \;-\; \frac{R}{L}v_{IN}\right] \tag{C.13}$$

Hence, the original two subintervals of operation of the class D audio power amplifier operating under ideal-sliding control are expanded into a total of six subintervals of operation under the lossy-sliding control, as shown in Fig. 74. Two of the subintervals, Δt_2 and Δt_5, are related to the derivative of lossy-switching function in equation (C.13), and four of the subintervals, Δt_1, Δt_3, Δt_4, and Δt_6, account for the truncated exponential terms of the lossy-switching function in equation (C.12).

Therefore, subintervals Δt_2 and Δt_5 and are defined as

$$\Delta t_2 \;=\; \frac{2\kappa}{\dfrac{d}{dt}s(e_1,t)} \tag{C.14}$$

when $v_{IN} = v_{PWM-} = 0$, and

$$\Delta t_5 \;=\; \frac{-2\kappa}{\dfrac{d}{dt}s(e_1,t)} \tag{C.15}$$

when $v_{IN} = v_{PWM+} = v_{DD}$, and subintervals Δt_1, Δt_3, Δt_4, and Δt_6, are approximated by calculating the time that takes to the exponential wave in equation (C.16) to decay down to 1% of its initial value, at t = 0, for the maximum switching frequency in the ideal sliding

mode as

$$\exp\left(-\frac{\gamma}{\alpha}t\right) \;=\; \exp\left(-\frac{\gamma}{4\alpha f_{s,ideal}k_t}\right) \;=\; 0.01 \tag{C.16}$$

then, subintervals Δt_1, Δt_3, Δt_4, and Δt_6 can be expressed as

$$\Delta t_1 \;+\; \Delta t_3 \;+\; \Delta t_4 \;+\; \Delta t_6 \;=\; 4\Delta t_0 \;=\; \;-\; 4\frac{\alpha}{\gamma}\ln\left(\frac{v_H \;-\; \kappa}{\gamma e_1}\right) \tag{C.17}$$

where

$$v_H \;=\; e_1\gamma\exp\left(-k_t\right) \;+\; \kappa[1 \;-\; \exp\left(-k_t\right)] \tag{C.18}$$

and k_t, from equation (C.16) is

$$k_t \;=\; \;-\; \frac{\gamma}{4\alpha\ln\left(0.01\right)}\left(\frac{1}{f_{s,ideal}}\right) \tag{C.19}$$

as expressed before in equations (4.14), and (4.15).

Finally, the time period for one cycle of operation is giving by

$$\begin{aligned} T_{s,real} \;&\approx\; \Delta t_1 \;+\; \Delta t_2 \;+\; \Delta t_3 \;+\; \Delta t_4 \;+\; \Delta t_5 \;+\; \Delta t_6 \\ &\approx\; \Delta t_2 \;+\; \Delta t_5 \;+\; 4\Delta t_0 \\ &\approx\; \frac{2\kappa V_{DD}\dfrac{R}{L}\left(1 \;+\; \dfrac{1}{\gamma}\right)}{\left(\dfrac{R}{L}v_C \;+\; \dfrac{1}{2\gamma C}i_L\right)\left(V_{DD}\dfrac{R}{L}\left(1 \;+\; \dfrac{1}{\gamma}\right) \;-\; \left(\dfrac{R}{L}v_C \;+\; \dfrac{1}{2\gamma C}i_L\right)\right)} \\ &\quad -\; 4\frac{\alpha}{\gamma}\ln\left(\frac{v_H \;-\; \kappa}{\gamma e_1}\right) \end{aligned} \tag{C.20}$$

as defined previously in equation (4.13).

APPENDIX D

SLIDING MODE CONTROL FOR INTERLEAVED PARALLEL BUCK VOLTAGE REGULATORS

This appendix discusses the derivation of the switching function for interleaved parallel (poly-phase) buck voltage regulators. The general expressions for a buck converter operating with N phases are shown and the particular case of a dual-phase voltage regulator is analyzed. This analysis includes the derivation of the equivalent control model and the stability analysis of the dual-phase buck voltage regulator operating under sliding mode control.

D.1. Derivation of the Switching Function

This section discusses the general form of the switching function (SF) in a sliding mode controller for interleaved parallel buck voltage regulators for asymptotic tracking [96]–[103]. A power system with N parallel buck converters can be expressed by the following general state space model

$$\begin{pmatrix} \frac{d}{dt}i_{L1} \\ \frac{d}{dt}i_{L2} \\ \vdots \\ \frac{d}{dt}i_{LN} \\ \frac{d}{dt}v_C \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & \cdots & -\frac{1}{L_1} \\ 0 & 0 & 0 & \cdots & -\frac{1}{L_2} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & -\frac{1}{L_N} \\ \frac{1}{C} & \frac{1}{C} & \frac{1}{C} & \cdots & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ \vdots \\ i_{LN} \\ v_C \end{pmatrix}$$

$$+ \begin{pmatrix} \frac{1}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{1}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{1}{L_N} \\ 0 & 0 & \cdots & 0 \end{pmatrix} \begin{pmatrix} u_1 \\ u_2 \\ \vdots \\ u_N \end{pmatrix} \tag{D.1}$$

where i_{Lj}, L_j, u_j, C, R and v_C represents the j^{th} inductor current, the j^{th} inductor value, the j^{th} control input signal, the output capacitor, the resistive output load and the voltage across the output capacitor, respectively.

Therefore, there will be necessary N number of control laws for N number of parallel converters. The switching functions defining an equal current distribution across all the individual buck converters are expressed by

$$\begin{aligned} s_1(t) &= k_1\Delta v + k_2\int_0^t \Delta v\, d\tau + k_3\int_0^t \Delta i_{L1}\, d\tau - i_{L1} \\ s_2(t) &= k_1\Delta v + k_2\int_0^t \Delta v\, d\tau + k_3\int_0^t \Delta i_{L2}\, d\tau - i_{L2} \\ \vdots \quad &\quad \vdots \qquad\qquad\qquad\qquad \vdots \\ s_N(t) &= k_1\Delta v + k_2\int_0^t \Delta v\, d\tau + k_3\int_0^t \Delta i_{LN}\, d\tau - i_{LN} \end{aligned} \tag{D.2}$$

where

$$\Delta v = v_{REF}(t) - v_C(t) = v_{REF}(t) - v_C(t) \tag{D.3}$$

and

$$\Delta i_j = \frac{1}{N}\sum_{i=1}^{N} i_{Li}(t) - i_{Lj}(t) \tag{D.4}$$

The term Δv in equation (D.2) regulates the output voltage. The overall system presents high reliability since all the switching functions contain this term. The term Δi_j in equation (D.2) provides equal current distribution through all the parallel converters [96], [97].

The particular case of the dual-phase buck voltage converter is reduced to the state space model defined in equation (7.4) and the switching functions expressed in equations (7.6) and (7.7).

D.2. Stability Analysis of the Proposed Dual-Phase Buck Voltage Regulator

The stability analysis of the fully-integrated dual-phase buck voltage regulator operating under the switching functions, i.e. the control laws, is presented in this section. The method used to demonstrate the convergence of the system to their sliding equilibrium points [56] is based on the equivalent control approach [33]–[35]. Hence, the discontinuous function u in equation (7.11), which is created by the sign of the switching functions, is considered as the sum of a high-frequency (u_{nl}) and a low-frequency (u_{eq}) components, where u_{eq} can be viewed as the average value of the discontinuous function.

$$u \;=\; u_{eq} \;+\; u_{nl} \tag{D.5}$$

Therefore, it is required to find the input u_{eq} such that the states trajectories stay on the switching surface defined by equations (7.6) and (7.7). A necessary condition for the states trajectories to stay on the switching surface is that

$$\frac{d}{dt} s_{1,2}(t) \;=\; 0 \tag{D.6}$$

Then, differentiating equations (7.6) and (7.7) with respect to time and solving for $u_{1,\,2}$ we can obtain the equivalent control inputs as

$$\begin{pmatrix} u_{1,eq} \\ u_{2,eq} \end{pmatrix} \;=$$

$$\begin{pmatrix} L_1\left(-\frac{k_1}{C} - \frac{k_3}{2}\right) & L_1\left(-\frac{k_1}{C} + \frac{k_3}{2}\right) & L_1\left(\frac{k_1}{RC} + \frac{1}{L_1} - k_2\right) \\ L_2\left(-\frac{k_1}{C} + \frac{k_3}{2}\right) & L_2\left(-\frac{k_1}{C} - \frac{k_3}{2}\right) & L_2\left(\frac{k_1}{RC} + \frac{1}{L_2} - k_2\right) \end{pmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ v_C \end{pmatrix} + \begin{pmatrix} L_1 k_2 \\ L_2 k_2 \end{pmatrix} V_{REF} \tag{D.7}$$

Substituting equation (D.7) into the state space model in equation (7.4) we can obtain the general equivalent model given by

$$\begin{pmatrix} \frac{d}{dt} i_{L1} \\ \frac{d}{dt} i_{L2} \\ \frac{d}{dt} v_C \end{pmatrix} = \begin{pmatrix} \left(-\frac{k_1}{C} - \frac{k_3}{2}\right) & \left(-\frac{k_1}{C} + \frac{k_3}{2}\right) & \left(\frac{k_1}{RC} - k_2\right) \\ \left(-\frac{k_1}{C} + \frac{k_3}{2}\right) & \left(-\frac{k_1}{C} - \frac{k_3}{2}\right) & \left(\frac{k_1}{RC} - k_2\right) \\ \frac{1}{C} & \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_{L1} \\ i_{L2} \\ v_C \end{pmatrix} + \begin{pmatrix} k_2 \\ k_2 \\ 0 \end{pmatrix} V_{REF} \tag{D.8}$$

By definition [36], [56], the sliding equilibrium point of the equivalent state-space model in equation (D.8) can be obtained if

$$\begin{pmatrix} \frac{d}{dt} i_{L1} \\ \frac{d}{dt} i_{L2} \\ \frac{d}{dt} v_C \end{pmatrix} = 0 \tag{D.9}$$

when

$$\begin{aligned} s_1(t) &= 0 \\ s_2(t) &= 0 \end{aligned} \tag{D.10}$$

Hence, the sliding equilibrium of the dual-phase buck voltage regulator is given by

$$v_C = V_{REF} \tag{D.11}$$

$$i_{L1} \;=\; i_{L2} \;=\; \frac{1}{2}\left(\frac{V_{REF}}{R}\right) \tag{D.12}$$

The sliding equilibrium point corresponds to the desired voltage in the output of the buck voltage regulator where V_{OUT} tracks the value V_{REF}. Similarly, the value of the output currents will be defined by the output voltage divided by the corresponding load. Notice that since we have equal distribution current in each one of the inductors, the total current is equally split in the two paths. Furthermore, the eigenvalues of the equivalent state model in equation (D.8) correspond to an stable node since their values are real and negative.

In general, the dual-phase buck voltage converter with sliding mode control is stable if the followings conditions of the Routh-Hurwitz criterion [114]–[116] are met for the constants k_1, k_2, and k_3

$$\left(k_3 \;+\; 2\frac{k_1}{C} \;+\; \frac{1}{RC}\right) \;>\; 0 \tag{D.13}$$

$$\left(2\frac{k_2 k_3}{C}\right) \;>\; 0 \tag{D.14}$$

$$\left(k_3 \;+\; 2\frac{k_1}{C} \;+\; \frac{1}{RC}\right)\left(\frac{k_3}{RC} \;+\; 2\frac{k_2}{C} \;+\; 2\frac{k_1 k_3}{C}\right) \;>\; \left(2\frac{k_2 k_3}{C}\right) \tag{D.15}$$

where optimum values for such constants can be obtained following the design procedures described in [96], [97]

D.3. Stability Analysis and the Reduced Equivalent Model

The purpose of this section is to obtain a reduced equivalent model and show its stability analysis. A reduced equivalent model can be easier to analyze in the case of a polyphase parallel buck converter [102].

Hence, assuming an equal distribution of currents, the same control structure for each parallel converter, and the same duty cycle in the pulse-width modulated signals, the

general state space model expressed in equation (D.1) can be reduced to

$$\begin{pmatrix} \frac{d}{dt} i_L \\ \frac{d}{dt} v_C \end{pmatrix} = \begin{pmatrix} 0 & -\frac{1}{L_e} \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} \frac{1}{L_e} \\ 0 \end{pmatrix} u \tag{D.16}$$

where

$$i_L = i_{L1} + i_{L2} + \ldots + i_{LN} \tag{D.17}$$

$$L_e = \frac{1}{N}(L_1 + L_2 + \ldots + L_N) \tag{D.18}$$

Consequently, since the total current is equally distributed among the N inductors, the switching functions in equation (D.2) are reduced to

$$s(t) = k_1 \Delta v + k_2 \int_0^t \Delta v \, d\tau - \frac{1}{N} i_L \tag{D.19}$$

The reduced equivalent control input is found by differentiating equation (D.19) with respect to time, equating the result to zero, and solving for u as

$$u_{eq} = N L_e \left[\left(-\frac{k_1}{C} \right) i_L + \left(\frac{k_1}{RC} + \frac{1}{N L_e} - k_2 \right) v_C + k_2 V_{REF} \right] \tag{D.20}$$

Finally, substituting equation (D.20) into equation (D.16), the reduced equivalent state space model is

$$\begin{pmatrix} \frac{d}{dt} i_L \\ \frac{d}{dt} v_C \end{pmatrix} = \begin{pmatrix} -N\frac{k_1}{C} & N\frac{k_1}{RC} - N k_2 \\ \frac{1}{C} & -\frac{1}{CR} \end{pmatrix} \begin{pmatrix} i_L \\ v_C \end{pmatrix} + \begin{pmatrix} N k_2 \\ 0 \end{pmatrix} V_{REF} \tag{D.21}$$

The sliding equilibrium point, shown in equations (D.22) and (D.23), of the reduced equivalent model is a stable node because its eigenvalues are real and negative, and corresponds to the desired tracking voltage and total load current.

$$v_C = V_{REF} \tag{D.22}$$

$$i_L = \frac{V_{REF}}{R} \tag{D.23}$$

Finally, the conditions for the constants k_1 and k_2 to keep the system stable can be calculated using the Routh-Hurwitz criterion [114]–[116] and the optimization procedure described in [96], [97].

VITA

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