CMOS INTEGRATED CIRCUIT DESIGN FOR ULTRA-WIDEBAND

TRANSMITTERS AND RECEIVERS

A Dissertation

by

RUI XU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2009

Major Subject: Electrical Engineering

CMOS INTEGRATED CIRCUIT DESIGN FOR ULTRA-WIDEBAND

TRANSMITTERS AND RECEIVERS

A Dissertation

by

RUI XU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Approved by:

Chair of Committee,	Cam Nguyen
Committee Members,	Laszlo Kish
	Anthony Cahill
	Andrew K. Chan
Head of Department,	Costas N. Georghiades

August 2009

Major Subject: Electrical Engineering

ABSTRACT

CMOS Integrated Circuit Design for Ultra-Wideband

Transmitters and Receivers. (August 2009)

Rui Xu, B.S. , Southeast University, China;

M.S., Southeast University, China

Chair of Advisory Committee: Dr. Cam Nguyen

Ultra-wideband technology (UWB) has received tremendous attention since the FCC license release in 2002, which expedited the research and development of UWB technologies on consumer products. The applications of UWB range from ground penetrating radar, distance sensor, through wall radar to high speed, short distance communications. The CMOS integrated circuit is an attractive, low cost approach for implementing UWB technology. The improving cut-off frequency of the transistor in CMOS process makes the CMOS circuit capable of handling signal at multi-giga herz. However, some design challenges still remain to be solved. Unlike regular narrow band signal, the UWB signal is discrete pulse instead of continuous wave (CW), which results in the occupancy of wide frequency range. This demands that UWB front-end circuits deliver both time domain and frequency domain signal processing over broad bandwidth. Witnessing these technique challenges, this dissertation aims at designing novel, high performance components for UWB signal generation, down-conversion, as well as accurate timing control using low cost CMOS technology.

We proposed, designed and fabricated a carrier based UWB transmitter to facilitate the discrete feature of the UWB signal. The transmitter employs novel two-stage -switching to generate carrier based UWB signal. The structure not only minimizes the current consumption but also eliminates the use of a UWB power amplifier. The fabricated transmitter is capable of delivering tunable UWB signal over the complete 3.1GHz -10.6GHz UWB band. By applying the similar two-stage switching approach, we were able to implement a novel switched-LNA based UWB sampling receiver front-end. The proposed front-end has significantly lower power consumption compared to previously published design while keep relatively high gain and low noise at the same time. The designed sampling mixer shows unprecedented performance of 9-12dB voltage conversion gain, 16-25dB noise figure, and power consumption of only 21.6mW(with buffer) and 11.7mW(without buffer) across dc to 3.5GHz with 100M-Hz sampling frequency.

The implementation of a precise delay generator is also presented in the dissertation. It relies on an external reference clock to provide accurate timing against process, supply voltage and temperature variation through a negative feedback loop. The delay generator prototype has been verified having digital programmability and tunable delay step resolution. The relative delay shift from desired value is limited to within 0.2%.

DEDICATION

To my parents, my wife and those friends who supported me during this

undertaking.

ACKNOWLEDGEMENTS

Along the journey towards this doctoral degree, it would never be possible to come up with this dissertation and all the work that was put into it, without the generous assistance and support of many people. At first, my most sincere appreciation goes to my academic advisor Professor Cam Nguyen. It has been a great experience to work under his mentoring. His extensive technical knowledge and keen insight have guided me into the field of RF circuit design. He showed me not only handy skills of conducting state-of-the-art research but also good working ethics leading to professional successfulness. All of these will benefit my entire life.

My thanks also goes to my fellow lab mates Xin Guan, Yalin Jin , Mohan Chirala and Meng Miao. Five years of working, studying and having fun with them have been one of my most memorable experiences during my Ph.D. study.

I would also like to express my appreciation to my committee member Dr. Laszlo Kish, Dr. Andrew K. Chan and Dr. Anthony Cahill for serving on my committee and their guidance during my Ph.D. study.

I also wish to thank the National Science Foundation, the Air Force Research Laboratory and the US Army for their support of my research work.

Lastly, I would like to save my deepest gratitude to my parents who always have faith in me during many up-and-downs in my life. I couldn't have done it without your support even it's from the other side of the ocean.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER I

INTRODUCTION

1.1 Background and motivation

According to Shannon's Formula, the maximum amount of information that can be transmitted in a wireless communication system is defined as

$$C = W \log_2 (1 + SNR) \tag{1-1}$$

where W is the bandwidth of the transmitted signal and SNR is the signal to noise ratio in the communication system. The mathematical fact tells that higher transmission speed can be achieved by either increasing signal bandwidth or improving signal to noise ratio (SNR). In the past several decades, the evolution of wireless communication technology has been mainly focusing on improving SNR and modulation efficiency. This is mostly due to the fact that the bandwidth of wireless signal (spectrum) is a strictly limited resource. However the studies and applications of wideband signal have not been neglected. Early applications of ultra wideband signal (UWB) include specialized areas such as military communication, positioning/geolocation and ground penetrating. The wide bandwidth of UWB signal can be translated into ultra short pulse on time domain, which brings some advantages such as multipath immunity, high spatial resolution and low probability of interception. Most of these earlier specialized UWB systems are based on hybrid circuit and there was no imminent need for circuit integration.

_____

This dissertation follows the style of *IEEE Transactions on Microwave Theories and Techniques*.

In 2002 FCC released the revised ruling to allocate the spectrum of 3.1GHz – 10.6GHz for UWB application provided that the power spectrum of which is below certain limit. The FCC ruling expedited the birth of the IEEE 802.15.4A standard which defined the standard of high speed short distance indoor communication employing UWB technology. The IEEE 802.15.4A standard turned out to be the main driving force to bring UWB technologies into consumer electronics because of its potential of connecting various home appliances at ultra fast speed. CMOS technology, which has become the dominant carrier for many wireless communication standards, is considered as first choice for implementing UWB technologies.

In the most of the earlier UWB systems, the front-ends were built on microwave hybrid circuits. These systems usually included components like step recovery diodes (SRD), avalanche transistors or schottky diodes, which are very difficult to be migrated onto CMOS process. Whereas the recent progress and achievement of CMOS wireless transceiver in cell phone, wireless LAN and Bluetooth are mostly narrow band based. To implement UWB technologies on CMOS imposes the development of CMOS front-end building blocks which can perform wideband signal processing such as amplifying, frequency conversion, frequency generation as well as timing control. Designing of these circuit modules while satisfying low power dissipation and high integration is a challenging issue and has yet to be fully studied. Interestingly, a divarication can be observed on the recently effort of integrating UWB technology on CMOS process. The approaches such as OFDM-UWB are based on the ideology of expanding the bandwidth of existing narrow band transceiver structure, which allow reuse of some proven designs

and technologies in narrow band systems. Some other implementations are more based on the impulse radio methodology. These attempts will introduce some new building blocks such as pulse generator, correlator and sliding integrator, which have not been extensively utilized in the mature narrow band transceiver structures. This dissertation tends to focus on the second approach and will present some novel topologies and designs to achieve low power, high performance by making use of the discrete nature of UWB pulse signal.

1.2 Dissertation scopes and organization

This dissertation will investigate and explore the designing of some key monolithic UWB building blocks on CMOS process. Both architecture trade-off and practical design issues will be discussed for each circuit module. Following this introduction chapter II will give an overview on the applications and structures of UWB systems in chronological manner to reveal the evolving of UWB technology and reasoning behind different architectures in UWB system. Chapter III presents a novel UWB carrier based transmitter design. This chapter will thoroughly address the subject of UWB signal generation. A two-stage-switching based configuration is proposed as a solution for low power, high efficiency and low complexity UWB transmitter. Chapter IV covers the designing of a UWB sampling mixer on CMOS process. As the front end in UWB sampling receiver, wideband sampler has not been realized on CMOS process previously. We are able to integrate a LNA with a sampling switch to complete the function of signal amplifying and down-conversion on a single chip while achieving low

power consumption, low noise and high gain at the same time. In Chapter V, the application and design procedure of delay generator in the UWB system will be discussed. The un-calibrated inverter based delay cell has significant process, supply voltage and temperature variations, which cause the timing control in UWB system unpredictable. The proposed delay generator will automatically calibrate the propagation delay in the delay cell through an external clock and a negative feedback loop. The last chapter summarizes the contribution of this dissertation and points out several potential improvements that can be completed in the future.

CHAPTER II

ULTRA-WIDEBAND TECHNOLOGY OVERVIEW

2.1 Brief history of UWB technology

The concept of Ultra-wideband (UWB) can be traced back to the 1960's when Harmuth published a series of papers to discuss non-sinusoid signal based communication systems [1]-[2]. Transmitting non-continuous signals to achieve time multiplexing is one of the motivations behind these discussions. In 1973 Ross filed a patent on so called based-band pulse communication system [3]. It was claimed that because of the wide spread spectrum of the base-band pulses, even the total energy content of the transmitted signal is considerably large it will place little interference on the relatively narrow pass band of other existing radios. The patent diagramed the implementation of transmitter, receiver and antenna which were capable of handling carrier-less pulse signal. The system structure has not changed radically for many UWB
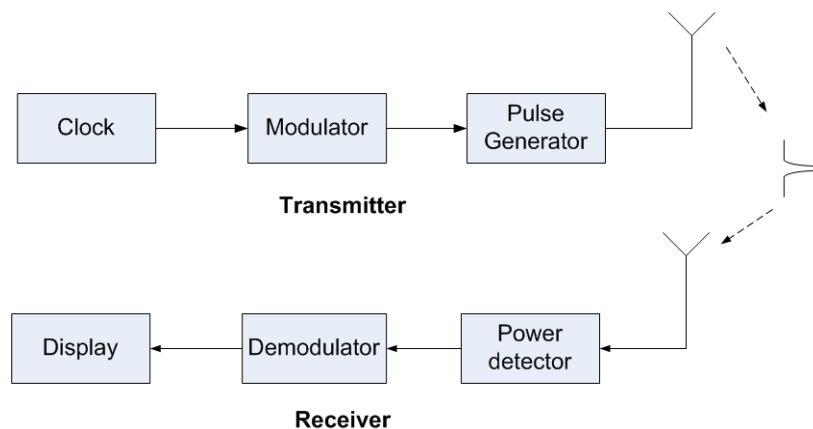
Figure 2.1 System diagram of base-band communication from G.F. Ross [3]
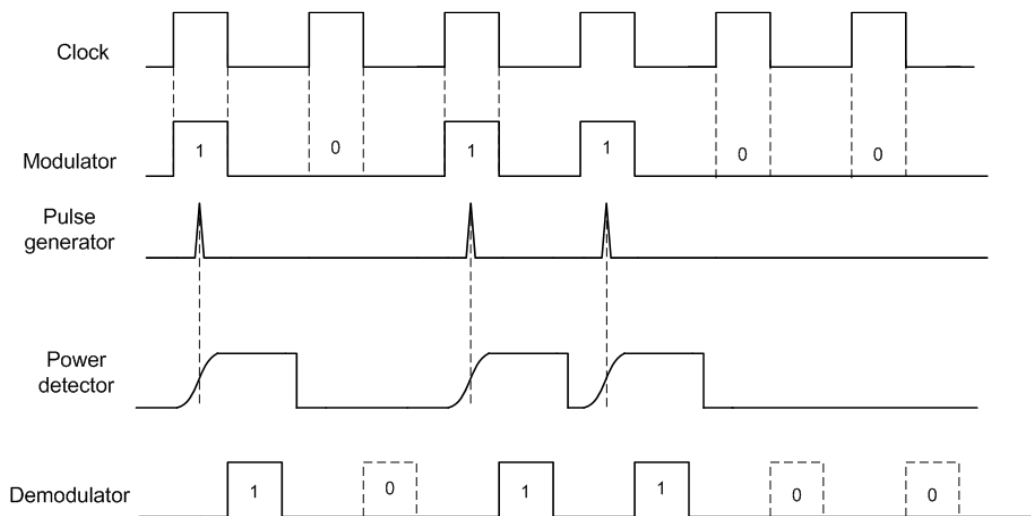
Figure 2.2 Waveforms of different building blocks in based-band pulse radar systems

system emerged later on. Figure 2.1 exhibits the diagram of such pulse system.

Distinct from sinusoid based communication system, the base-band pulse system in

Figure 2.1 doesn't contain any frequency mixing.

Figure 2.2 depicts the time domain waveforms at output of different building

blocks. In the transmitter, the modulation is directly applied to clock signal. We assume

On-Off key modulation is used, e.g. the information bit "1" is represented by the

presence of a pulse and no pulse is sent for bit "0". The modulated clock will be applied

to pulse generator and produces a baseband pulse transmitted through the antenna. The

receiver uses a power detector, in most cases a leading edge detector, to catch the arrival

of pulses. If the pulse amplitude at the input of power detector reaches certain threshold,

the power detector will assume there is a pulse signal instead of noise and generate a

"high" voltage at the output, which signifies a "1". If there is no detected pulse found at

designated time, it will be assumed that a "0" is received. Demodulator will sample this

output voltage, recover these modulated "1" "0" information bits and send to display device. Noticeably, all the signal processing is conducted on time domain. Consequently, such pulse systems sometime are referred as "time domain radio" systems. The time domain radio gets rid of the frequency up-conversion and down-conversion procedure therefore significantly reduces the circuit complexity. However the sensitivity of the power detector is far from satisfying for detecting weak signal. The pulse transmitter needs to have very large output power to assure a strong signal reception. The low receiver sensitivity will also limit the working range of the time domain radio when transmitted power through TX is limited. Wheareas the high power transmitter is the major impediment for making UWB system more compact and power efficient.

In 1977 Van Etten did an empirical testing on the impulse radar system following the topology in Figure 2.1 [4]. He studied the radiation and reception of impulse waveforms as well as the performance of some antenna structures when dealing with impulse signals. In his design, a high voltage was applied to a pressurized spark gap. When the voltage applied reaches the threshold the plasma within the gap will break down and ignite. The generated pulse can achieve 70ps of rising time and 100ps of pulse duration.

Based on similar idea, Morey invented the first ground penetrating pulse radar system which adopted synchronized sampling head in the receiver [5]. The radar system has the advantage of fine range resolution and deep penetration by making use of short pulse signal. It became a commercial success and brought many other followers since.
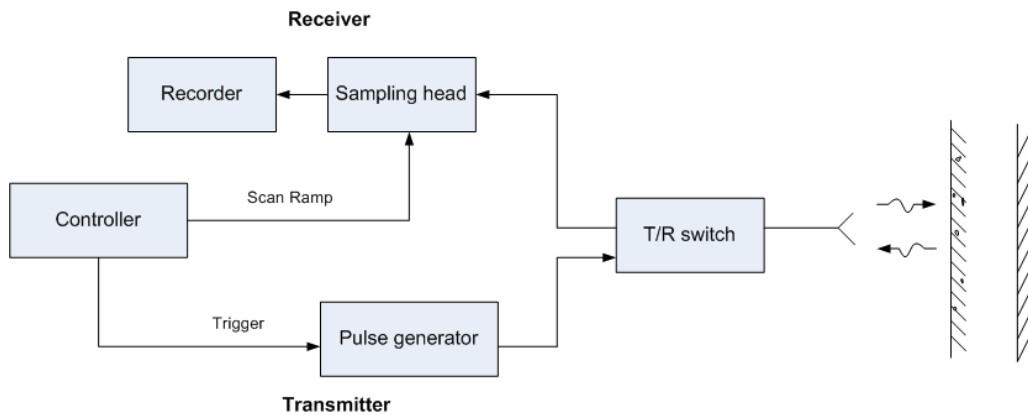
Figure 2.3 The configuration of pulse ground penetrating radar by Morey[5]

The configuration of such radar system is diagrammed in Figure 2.3. Comparing to the diagram in Figure 2.1 the transmitter and receiver of this system are both connected to the same controller. Also the pulse signal is generated periodically. These two features are important because the sampling head which is responsible for recovering the received waveform needs to be synchronized with transmitted signal. By observing the delay from signal transmission to signal reception the distance of reflection path can be accurately calculated. This sampling method is called synchronous sampling. Figure 2.4 illustrates the basic principle of the synchronous sampling method. In Figure 2.4 V_R represents waveform of the input RF signal, V_O is the LO strobe pulse signal to trigger the sampling, and V_D is the down-converted output signal through the (ideal) sample-and-hold operation of the receiver. To achieve down-conversion of the RF input V_R, the frequency of V_R and the pulse repletion rate (PRF) of V_O should have a small difference between them. For impulse radar systems, V_R is actually a pulse signal having a small
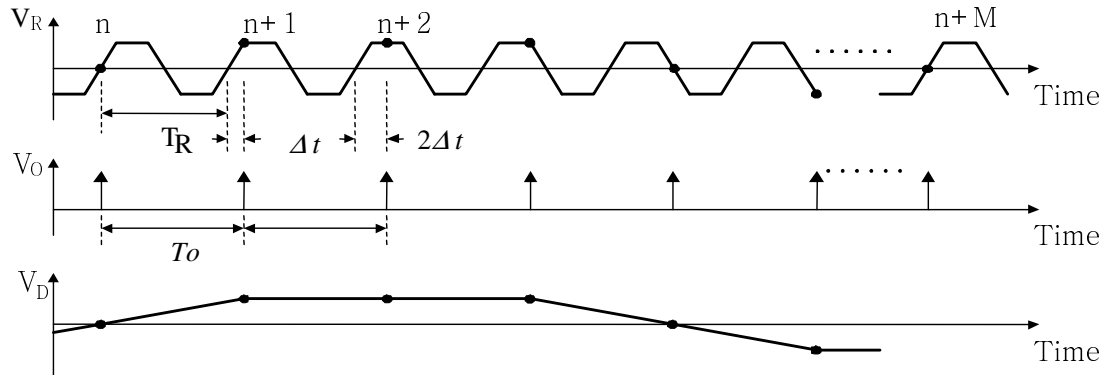
Figure 2.4 Illustration of synchronous sampling

PRF(f_R) and an extremely large duty cycle. For down-converting or stretching of the RF pulse, the PRF of the LO strobe pulse, f_o, should have a small deviation from f_R. The designing details of sampling system will be further explored in Chapter IV. It's worth noticing that in Morey's ground penetrating radar (GPR), avalanche transistor was used for generating pulse with rising time of about 1ns. The employment of semiconductor component had greatly reduced the size of this radar system. By the 1970's the sampling head used in the receiver had undergone extensive studies and became commercially available thanks to the development of sampling oscilloscope. Pulse generation module, an indispensable part of sampling circuit, could also be purchased from companies like Hewlett Packard and Tektronix. The limited output power of pulse generator, however, made it difficult to be integrated into transmitter of pulse based systems.

In 1994 the term "Ultra-Wideband" was applied to all the pulse based systems by US department of defense for the first time. After decades of perfecting and especially rapid development of semiconductor technology, highly integrated pulse radar system finally became possible. In 1994, T.E. McEwan filed a patent on micro-power impulse
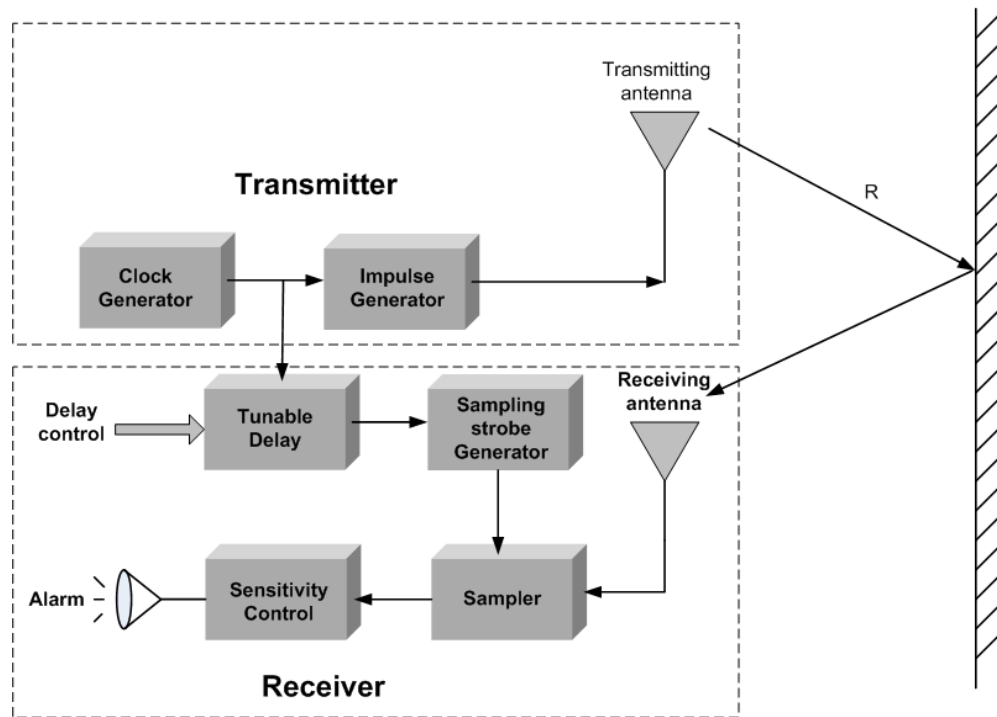
Figure 2.5 Simplified block diagram of MIR
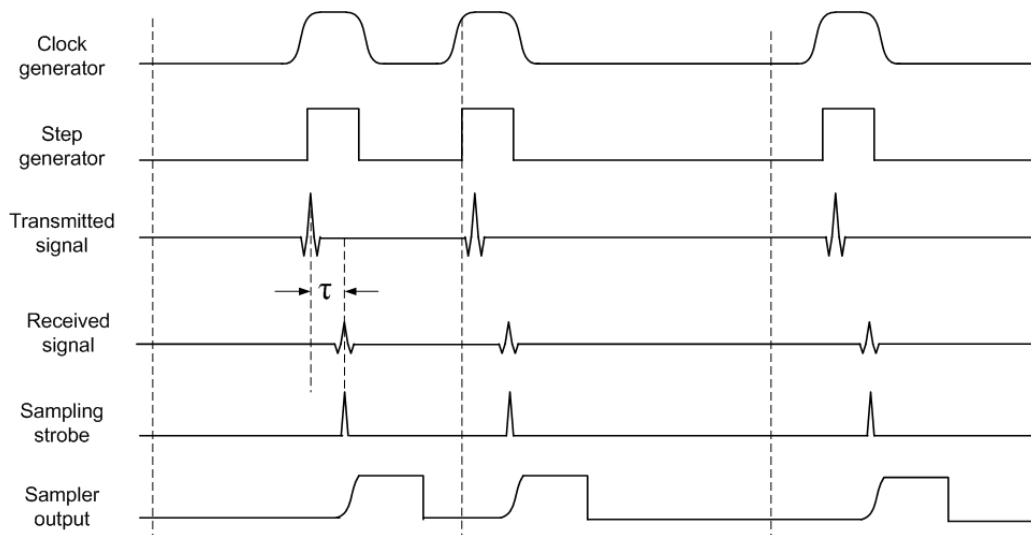
Figure 2.6 Waveform of main components in MIR

radar (MIR), an extremely low power, compact and low cost UWB radar system [6]. This ultra-wideband radar system was initially proposed as a motion sensor. The transmitter emits short duration impulses while receiver is only designed to accept signal echo from a fixed range R. Any motion on the reflector at range radius of R will cause a change on return signal level sensed by the receiver. In this case an alarm will be sent out. The main components of MIR are shown in Figure 2.5. The transmitter contains a clock generator and a step generator. The clock generator produces clocks that have random pulse repetition interval (PRI) rather than generating periodic clock signal. This helps to smooth the spectrum of the transmitted signal so that interference to other electronic systems can be minimized. The step generator utilizes a step recovery diode (SRD) to create a step signal with around 100ps rising time. Passing the signal through the antenna will differentiates the sharp edge and radiates Gaussian shaped impulse. The receiver is composed of a tunable delay generator, a sampling strobe generator, an ultra-wideband sampler and a sensitivity control unit. The tunable delay determines the value of range R by adjusting the time delay between transmitted signal and received signal: $R = c\tau / 2$, where c is light speed and τ is the delay on time domain. The sampling strobes are generated by a delayed transmitted clock and will turn on the receiver when reflected signal is due after traveling distance of 2R. The receiver output can be averaged through integration for repeated sampling by sensitivity control unit. This will essentially improve the signal to noise ratio of the receiver. With clock frequency of 1 MHz, even with 1000 sampling point averaging, the MIR radar can still have 1 *ms* of responding time for motion detection. In Figure 2.6 the time domain waveforms of the

main components are displayed to explain the transmitting and receiving operation of the MIR. Comparing to ultrasonic or passive infrared based motion sensors the pulse radar is not subject to restriction like line-of-sight limitations or degradation caused by fluorescent lighting or in direct sunlight. Although the application of MIR is limited, it signifies that the integration of UWB system has became feasible with advance in semiconductor technologies such as fast-transition SRD and high performance sampling diode. Since the late 1990s the move to commercialize UWB technology began to emerge. Companies such as Time Domain and XtremeSpectrum were founded to bring UWB based system into the field of consumer electronics. Figure 2.7 lists some of the possible applications for commercializing UWB technology. The lack of specified
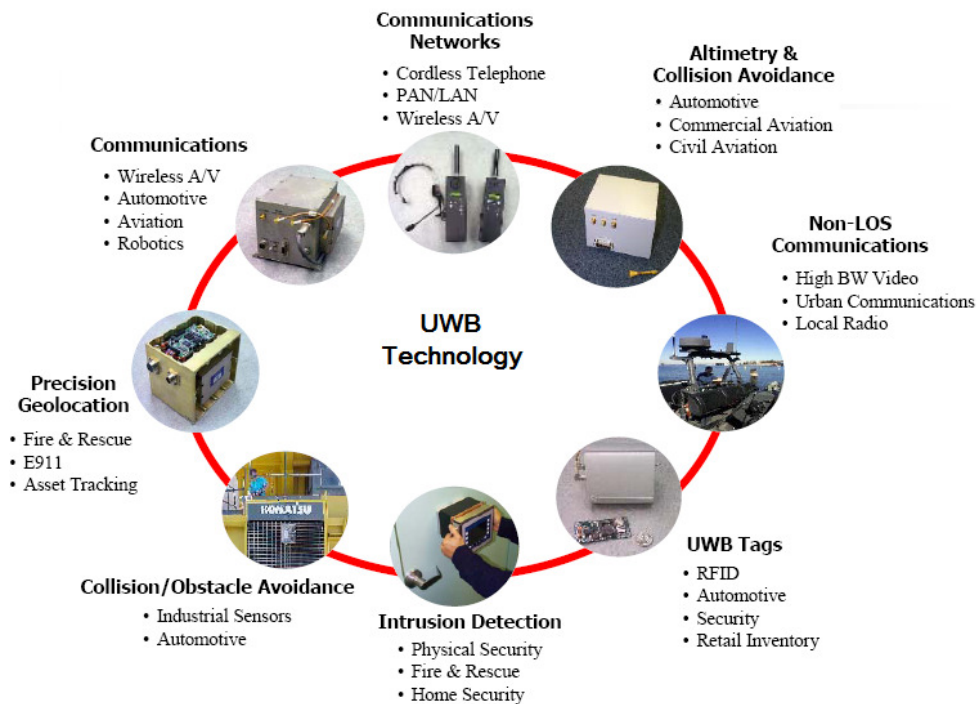
Figure 2.7 Possible commercial applications for UWB technology

physical layer definition of UWB technology had left a very wide space for design innovation. There have been numerous variations and improvements on both concepts of UWB system and instantiation of subsystem blocks. The adoption of pulse shape, modulation scheme and receiver structure can all be implemented differently for each UWB application. We can categorize these UWB systems into two groups: Coherent receiving system and non-coherent receiving system. The coherent receiving based transceiver is illustrated in Figure 2.8. The transmitter comprises a modulator which applies information code to a clock signal generated by baseband DSP block. The clock can be modulated by a pseudo noise code (PN code) to spread the spectrum. For simplification purpose we can assume the clock is periodical and OOK modulation mentioned in

Figure 2.2 is used. On the receiver side the baseband DSP modulate will use a clock that is synchronized with transmitter to drive a pulse generator to produce a train of template signal pulse having the same waveform substantially equivalent to each pulse of the received pulse signal. The modulated template pulse train will be positioned to align with the received pulse train through the adjustable delay generator. Then successive correlation output will be integrated to recover the impulse radio signal out of noise. The demodulator will retrieve the information codes out of the integrator output. Comparing with the receiver structure in Figure 2.1 the coherent receiver knows "when the received signal will arrive" and will only turn on the reception during that small time window, which tremendously reduce the chance of "false alarm" caused by noise or interference in power detection based signal capturing method. Since the template
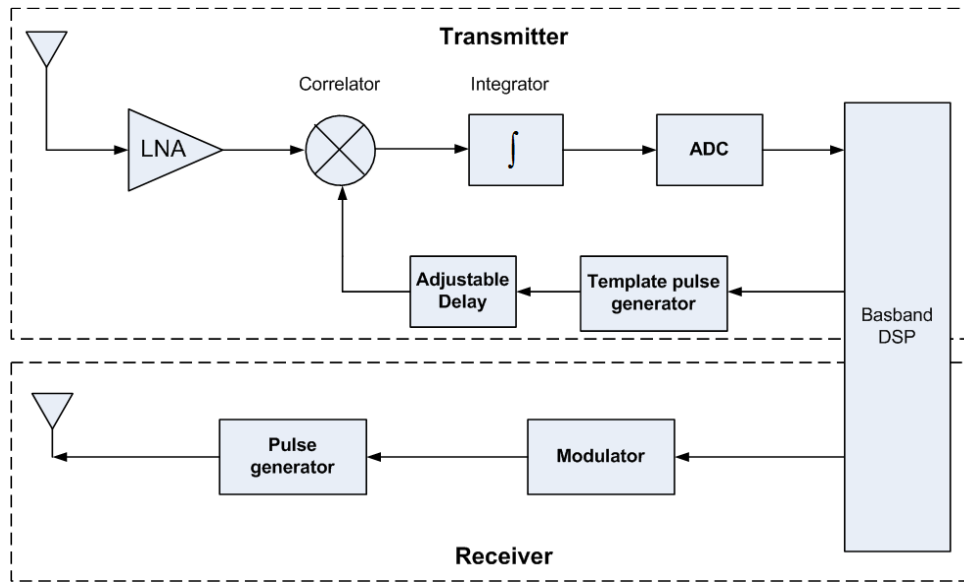
Figure 2.8 Simplified construction of UWB system with coherent receiving
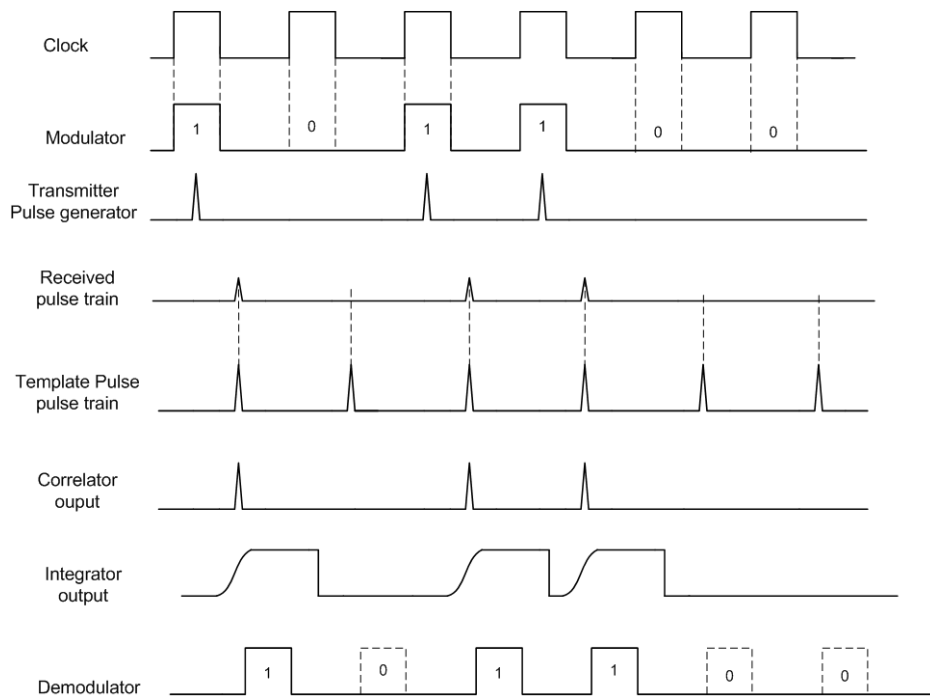
Figure 2.9 Signal timing diagram of coherent receiving based UWB system

signals are generated locally in the receiver, it will have large enough amplitude that helps to increase the conversion gain during the correlation. The timing diagram of signals in different modules of transmitter and receiver is given in Figure 2.9.

Consequently the UWB system proposed by Ross in Figure 2.1 belongs to non-coherent receiving category. However, a more popular structure is often considered when a UWB system adopting a non-coherent receiver as shown in Figure 2.10. Instead of correlating received signal with template pulse train, the non-coherent receiver conducts a square operation for the received signal. The self-correlation is generally superior to peak power detection scheme in Figure 2.1.

Although coherent receiver usually outperforms non-coherent receiver by 3-7dB [7], the synchronization of template signal and received signal requires accurate timing precision and complicated feedback loop, which leads to the increase in power
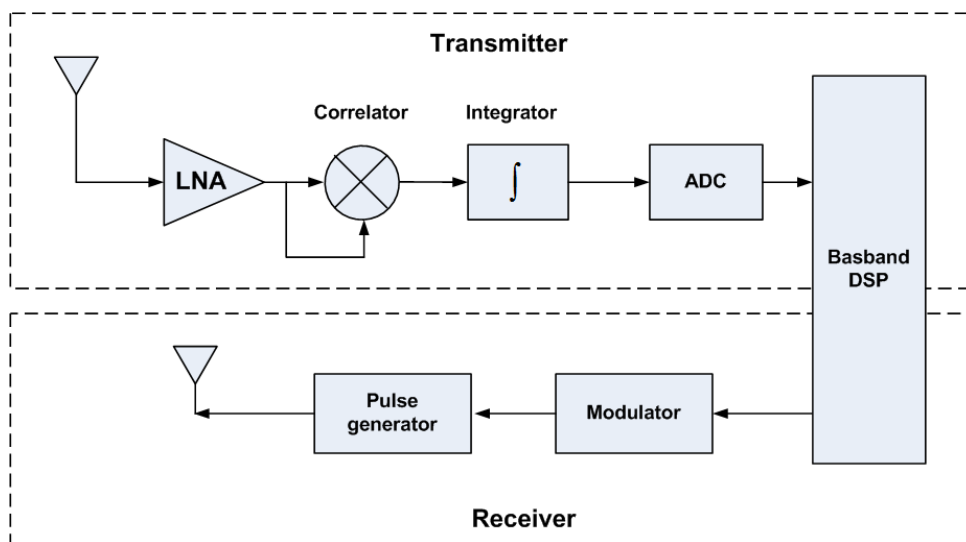
Figure 2.10 Building blocks of non-coherent receiving based UWB system

consumption and circuit complexity. Therefore both coherent and non-coherent received structures are utilized in the recent UWB radar or communication designs based on the trade-off of each instantiation.

A substantial change occurred in February 2002, when FCC issued a ruling that provided official radiation limitations for UWB transmission and permitted the operation of UWB devices on unlicensed basis [8]. According to the regulation, the term 'UWB' is used to define any signal with fractional bandwidth of more than 20% if the central frequency of the spectrum is lower than 2.5GHz or -10dB signal bandwidth of more than 500MHz if central frequency of the signal spectrum is larger than 2.5GHz. UWB radio transmission can legally operate in the frequency range of 3.1GHz to 10.6GHz, with the power spectral density (PSD) satisfying a specific spectral mask assigned by the FCC. Figure 2.11 demonstrates the spectral mask for UWB indoor communications under Part 15 of FCC's ruling. According to this spectral mask the PSD of the UWB signal measured in the 1MHz bandwidth must not exceed -41.3 dBm. For sensitive band such as GPS band (0.96-1.61GHz), the PSD limit is even much lower. This ruling will allow UWB device to overlay with existing narrow band systems while ensuring sufficient attenuation to limit adjacent channel interference. Right after the spectrum resource became officially available, IEEE established the 802.15.3a study group to definite physical layer concept of wireless personal area network (WPAN) by employing UWB technology. WPAN aims to transmit data at rate ranging from 100Mbps to 500Mbps within the distance of 20m. Not surprisingly the impulse based radio transmission model became the immediate candidate for the new standard. At the same time an
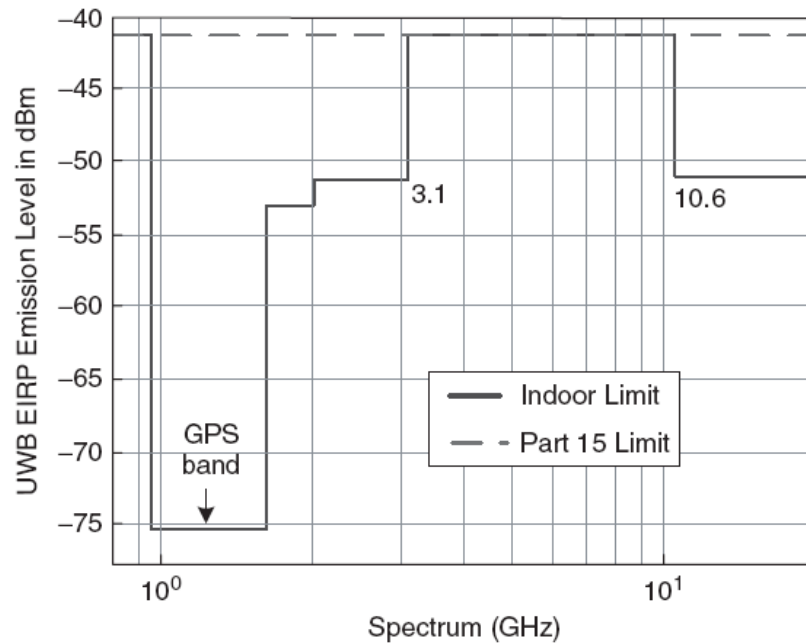
Figure 2.11 UWB spectral mask for indoor communication by FCC

alternative approach that utilizes a combination of multiband approach and orthogonal frequency-division multiplexing (OFDM) techniques was also proposed and began to gain momentum during the competition [9].

The MB-OFDM proposal chops the 7.5GHz UWB band into 13 sub-bands and does frequency hopping within at least three sub-bands as shown in Figure 2.12. In each sub-band, OFDM-QPSK modulation is used. Figure 2.13 shows a time domain representation of multiband UWB signals in which the signals at different center frequencies are transmitted at different discrete time slot. In the figure the center frequencies of the signals relative to the individual bands are shown in the Y axis. OFDM allows each sub-band to be divided into a set of orthogonal narrowband channels. The methodology behind this approach is extending the OFDM concept from
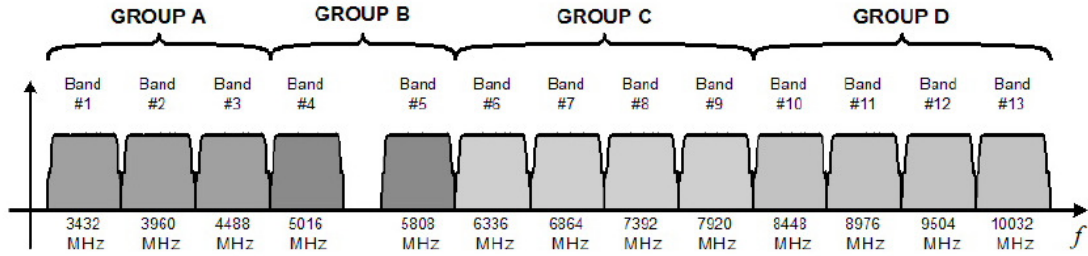
Figure 2.12 Frequency plan for multi-band OFDM based proposal
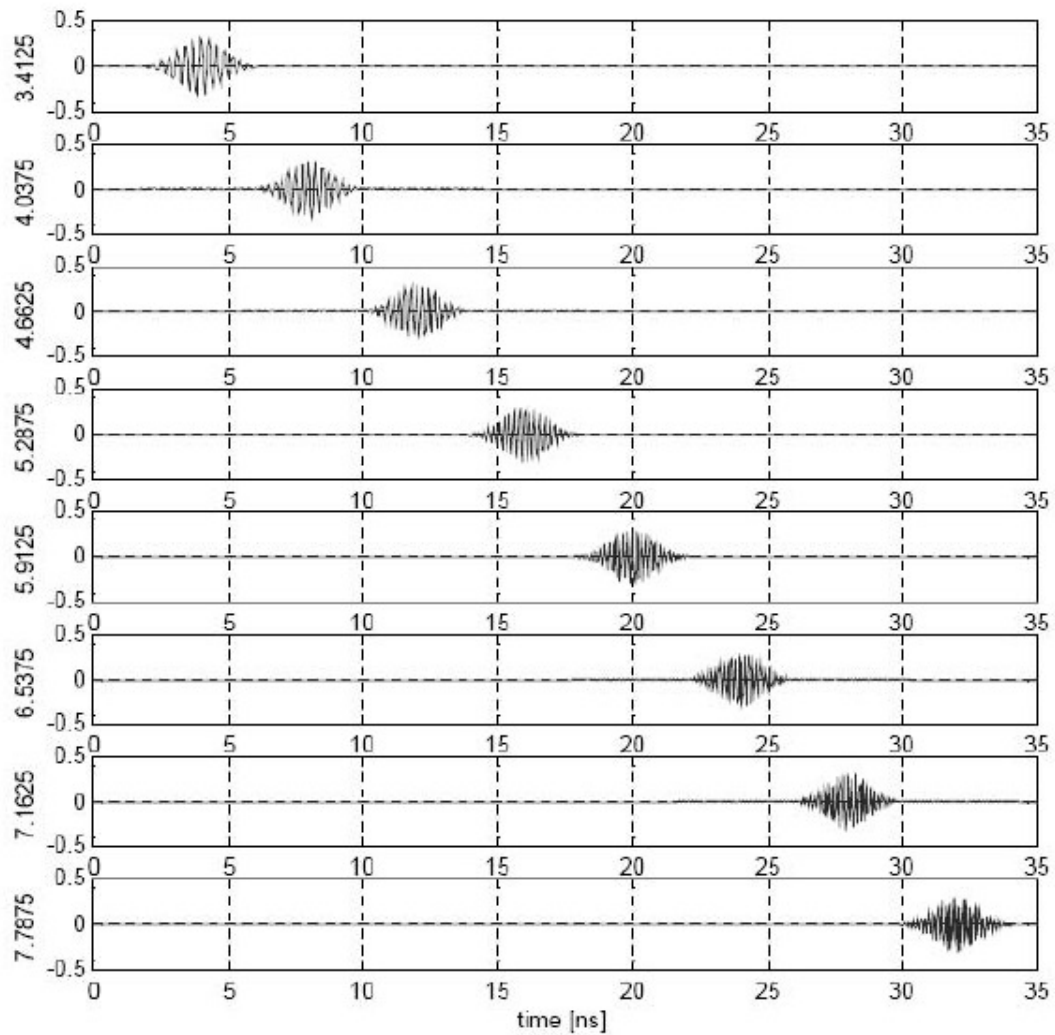
Figure 2.13 Multiband signal transmitted at different time slot

narrow band to ultra-wideband so that the waveform dispersion at the antenna and circuit interface is not critical anymore. Comparing with impulse radio based system, the multi-band approach have more flexibility in regard to foreign spectral regulation which may limit their UWB spectral allocation to smaller range than that authorized by the FCC. Moreover, processing over a smaller bandwidth eases the requirement on A/D converter sampling rate. However the large frequency tuning range and stringent settling time imposed by multi-band approach put a tough challenge on the shoulder of frequency synthesizer designers. The transceiver structure of this proposal is quite similar to that in narrow band system as shown in Figure 2.14.

The argument between impulse based single band approach and MB-OFDM based approach eventually lands on employing different design trade-offs and is beyond the scope of this dissertation. However power consumption, circuit complexity and signal to noise ratio performance are always the most important factors when conducting optimization on both the system level and the component level.
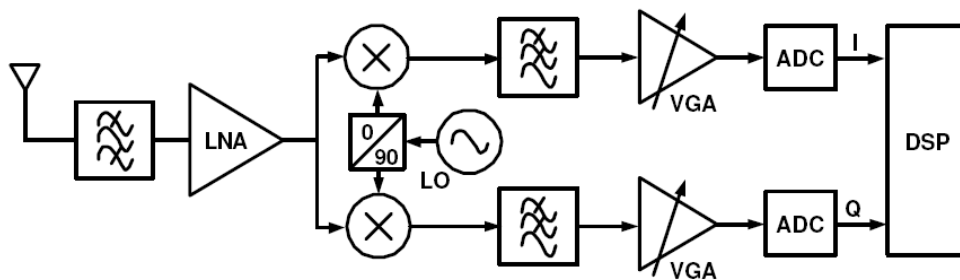
Figure 2.14 Direct conversion based MB-OFD UWB transceiver

2.2 UWB signal characteristics

For any wireless signal, there is a one-to-one mapping between time domain and frequency domain. This mapping is mathematically expressed by the Flourier transform. Intuitively we know that a time limited signal can be transformed to spectrum with infinite frequency range and vice-versa. Impulse waveform becomes the convenient candidates for UWB signal to spreading spectrum. It is also the waveform adapted in the earlier UWB systems. A rectangular pulse with duration of T and amplitude of 1 can be expressed as

$$p(t) = 1 \ , \ -\frac{T}{2} < t < \frac{T}{2} \tag{2-1}$$

The Fourier transform will give its frequency domain representation:

$$P(f) = \frac{T\sin(\pi Tf)}{\pi Tf} \tag{2-2}$$

The waveform and spectrum of *p(t)* is plotted in Figure 2.15. On frequency domain the spectrum's main lobe is between -1/T and 1/T. It also has significant energy lobe outside this main lobe. This could be troublesome since these sidelobes may fall outside
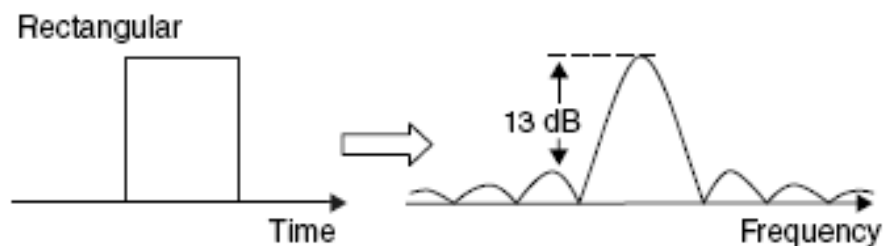
Figure 2.15 Time domain and frequency domain plot of a rectangular pulse
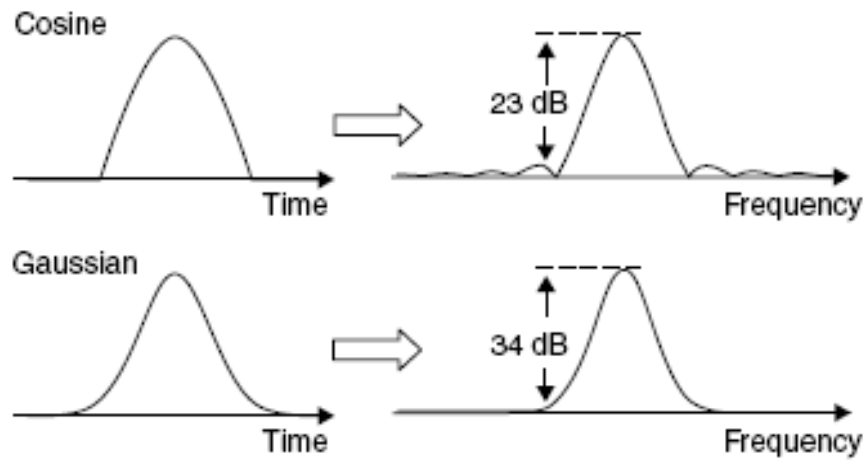
Figure 2.16 Time domain and frequency domain plot of a cosine and Gaussian based pulse

the target UWB band and cause interference to other existing radios. Fortunately, actual impulse obtained by practical circuit doesn't have the ideal abrupt step. The smoother rising/falling edge of the impulse will help to reduce the sidelobe level. For a cosine-shaped pulse $c(t)$ and a Guassian shaped pulse $g(t)$, they can be modeled as:

$$c(t) = \cos(\frac{2\pi f_a t}{2}); \quad -\frac{1}{2f_a} < t < \frac{1}{2f_a} \tag{2-3}$$

$$g(t) = \exp(\frac{-0.5t^2}{u^2}) \tag{2-4}$$

where $1/f_a$ denotes the pulse duration of the c(t). u is the constant that determines the slope of guassian pulse. Their Fourier transform are calculated to be:

$$C(f) = \frac{\cos(\pi \frac{f}{f_a})}{1 - (2\frac{f}{f_a})^2}, \tag{2-5}$$

$$G(f) = \exp[-2(\pi f u)^2] \tag{2-6}$$

The time domain and frequency domain plots for these two pulses are shown in Figure 2.16. The cosine shaped pulse round at the top of the pulse but still have abrupt corners at the zero crossing point. It has smaller sidelobes comparing to rectangular pulse. While Gaussian shaped pulse has smooth transitions everywhere, its sidelobes are completely compressed, which is preferred for the UWB signal transmission. But notice that a large amount of spectrum of these three impulse signals concentrate in DC and low frequency area, which will be difficult to transmit through antenna. Applying an impulse signal directly to an antenna will cause pulse distortion e.g. spectrum variation even the antenna is very wideband. Figure 2.17 shows the measured impulse waveform at input and output of a wideband antenna proposed in [10]. Interestingly we can see that the antenna differentiate the impulse and generate a pulse shape that we called mono-pulse or mono-cycle pulse. If we take a differentiate for Gaussian pulse in (2-4) and do some normalization the mono-pulse can be expressed as

$$m(t) = 6\sqrt{\frac{e\pi}{3}}\frac{t}{T_p}\exp(-6\pi\frac{t^2}{T_p^2}) \qquad (2\text{-}7)$$

where T_p is the pulse duration of the mono-pulse. Its frequency domain expression can be obtained as

$$M(f) = -j\frac{fT_p^2}{3}\sqrt{\frac{e\pi}{2}}\exp(-\frac{\pi}{6}f^2T_p^2) \qquad (2\text{-}8)$$
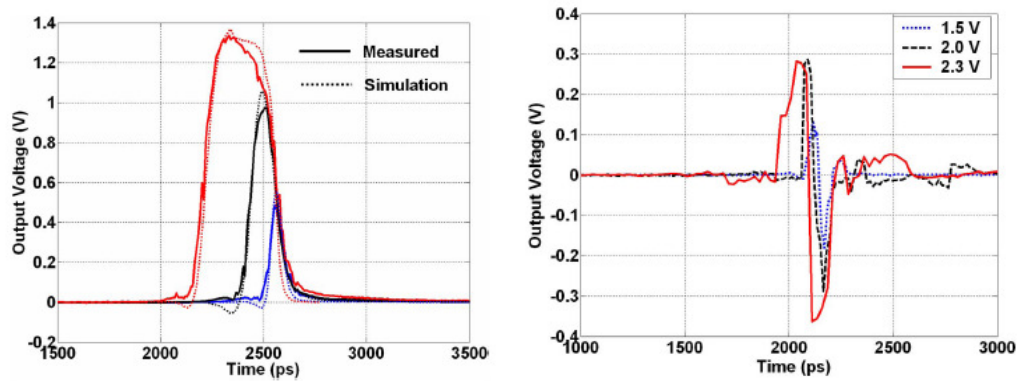
Figure 2.17 Measured time domain waveform of impulse at input and output of a wideband antenna proposed in [10]

The central frequency and the bandwidth of the mono-pulse is determined by T_p. The -3dB bandwidth is roughly 110% of the central frequency $f_0 = 1/T_p$. The time domain waveforms and spectrum of Gaussian mono-pulse with different duration are shown in Figure 2.18 and Figure 2.19 respectively. The ideal Gaussian mono-pulse has one zero crossing. If additional derivatives are taken for the mono-pulse the relative bandwidth decreases and the central frequency of the spectrum increases for a fixed T_p. Mono-cycle pulse UWB signal is a DC-free signal therefore doesn't suffer from significant pulse distortion through antenna. But it can be easily observed that the central frequency and bandwidth of the mono-pulse is correlated through T_p. It's not possible to design a mono-pulse UWB signal located at central frequency with variable bandwidth. This disadvantage will limit the ability of UWB system to efficiently utilize available spectrum.

Aiming at achieving more convenient spectrum management and less distortion through antenna, carrier based UWB signal became the late candidate for radar and
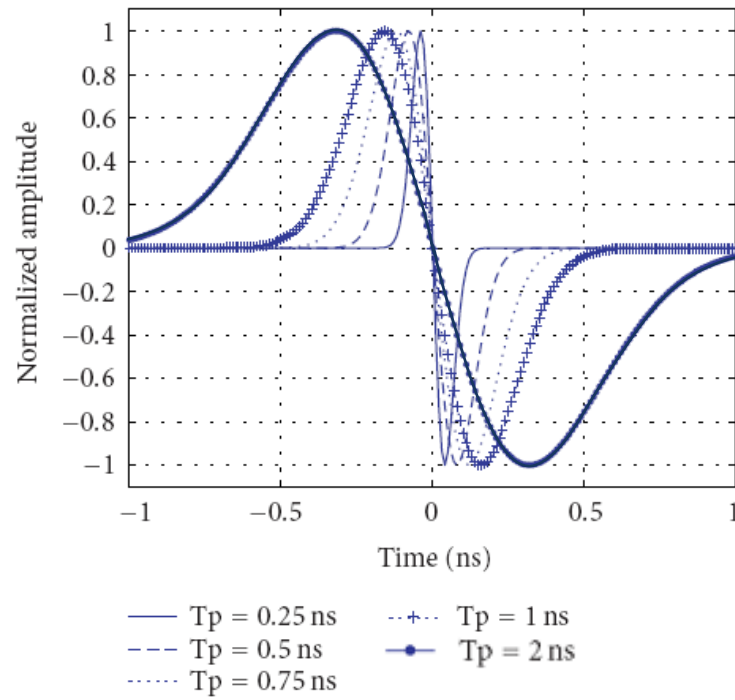
Figure 2.18 Time domain waveform of Gaussian mono-pulse with different T_p
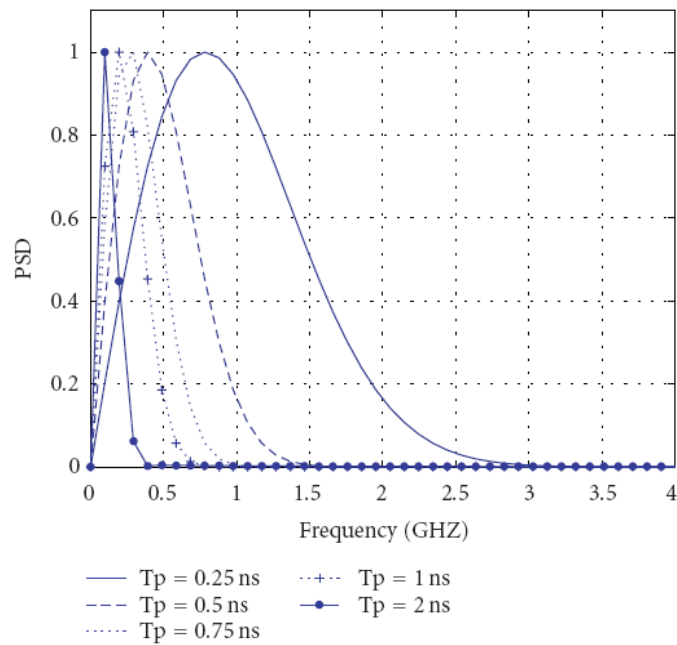
Figure 2.19 Spectrum of Gaussian mono-pulse with different T_p

communication applications [11]. The principle of carrier based UWB signal generation is to conduct a frequency up-conversion for the baseband impulse signal to move its spectrum to desired operating central frequency. The up-converted impulse signal can be mathematically expressed as:

$$c(t) = \exp(-\frac{0.5t^2}{u^2})\cos(2\pi f_c) \tag{2-9}$$

where f_c is the frequency of the carrier. u is a constant that is related to pulse duration. The carrier is AM modulated by the baseband impulse. The bandwidth of the obtained UWB signal will be determined by the duration of baseband impulse. The UWB signal appeared in frequency domain as:

$$C(f) = \exp[-2\pi^2(f \pm f_c)^2 u^2] \tag{2-10}$$

For a carrier based UWB signal with carrier frequency of 4.1GHz and impulse duration of 1ns, the signal mapping from time domain to frequency domain is illustrated in Figure 2.20. The signal spectrum has 10dB bandwidth of 1GHz and 20dB bandwidth of 2GHz. It has been mentioned earlier this chapter that for an impulse different rising edge shape
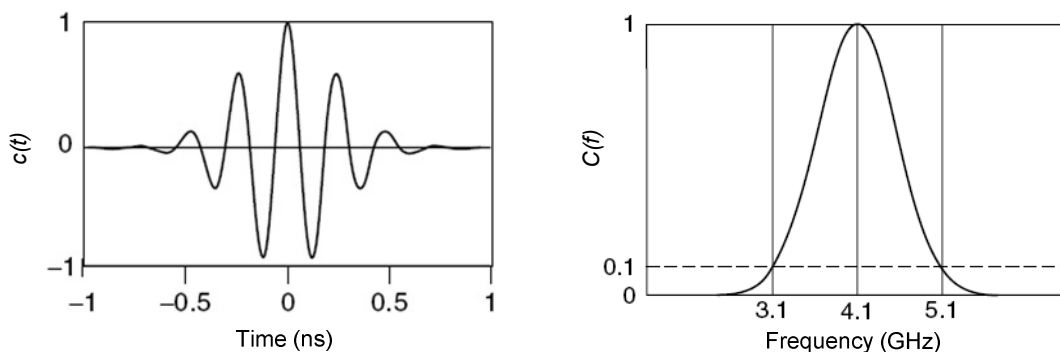
Figure 2.20 Time domain and frequency domain mapping of carrier-based UWB signal

will roughly have the same 10dB bandwidth. Therefore we are able to accurately place the UWB signal at any central frequency and control the bandwidth according to allocated spectrum. The expenses for choosing carrier based UWB signal are increased circuit complexity and possible higher power consumption due to the inclusion of an RF oscillator and an up-conversion mixer. Chapter III will discuss the solution for generating carrier based UWB signal effectively in detail.

2.3 UWB signal modulation

Similar to narrow band system, modulation schemes are also required for UWB communication and sensor systems in order to carry information. Noticeably some narrow band modulation approaches are not available to UWB pulse. For example, frequency modulation (FM) would be difficult to implement on UWB pulse since it needs to be applied to continuous wave (CW) signal. UWB pulse can be sent in discrete (as in GPR system) or near-continuous (as in MB-OFDM) manner. The information code can be applied to pulse position, shape or polarity. The most widely adopted modulation methods include On-Off-Key modulation (OOK), Pulse Position Modulation (PPM), Pulse Amplitude Modulation (PAM), Bi-phase modulation (BPM).

2.3.1 On-Off-Key modulation (OOK)

OOK is the simplest modulation method where presence or absence of a pulse is used to identify "1" or "0". The OOK scheme can be demodulated by power detection based UWB system as mentioned earlier. The modulation can be conducted for clock signal easily prior to the pulse generator. The major disadvantage of OOK is that it is

subject to noise interference and multipath because it will be difficult to determine if the detected signal is echo/noise or the received pulse.

2.3.2 Pulse Position Modulation (PPM)

In PPM, information is distinguished by whether the pulse appeared in a delayed position from regular time or not. PPM is not necessarily a binary system, by specifying different delay values the pulse position can represent multiple possible symbols, e.g PPM can be a M-ary system in which two or more bits can be grouped together to form a symbol. Another advantage of PPM is that the pulse position will appeared to be random on the time domain, which translates into a smoothly spread spectrum on frequency domain. Like OOK modulation, the implementation of PPM can also be applied to digital clock signal provided that fine accurate timing control is required.

2.3.3 Pulse Amplitude Modulation (PAM)

Another way to realize M-ary modulation is using different pulse amplitude to define different symbol. This requires the gain of the pulse generator output driver be programmable. PAM can achieve high data rate since the pulses can be very close to each other. In general it is not the preferred way for UWB communication considering that smaller pulse will be susceptible to noise and interference while larger pulse will require more power for amplification. OOK actually can be considered as a subset of PAM.

2.3.4 Bi-Phase Modulation (BPM)

BPM can be easily understood as to create a binary system based on inversion of certain pulse shape, e.g. the polarity of the pulse. It also benefits from high data rate while not easily affected by noise and interference. The randomly appeared positive and negative pulse will have the benefit of removing spectral peaks. The requirement for accurate timing control is also not as stringent as PPM. Figure 2.21 summarizes and compares different modulation schemes mentioned in this chapter. The information bits to be transmitted are "1 0 0 1". The UWB signal is assumed to be mono-pulse. In a UWB system, the modulation scheme, the pulse shape and the configuration of
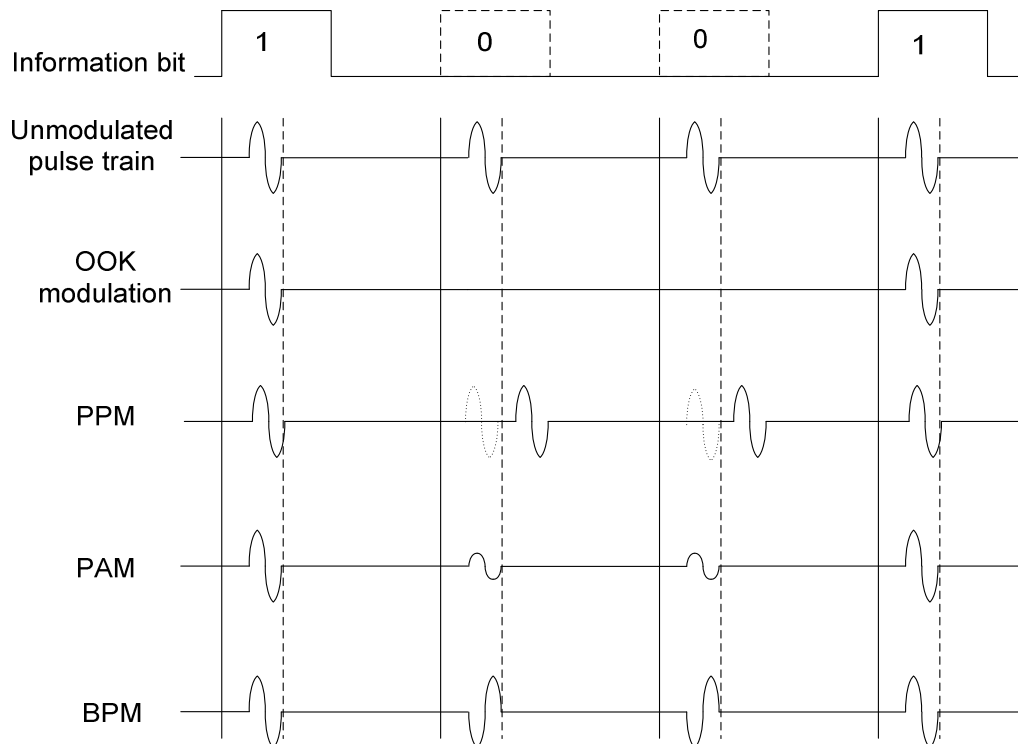
Figure 2.21 Comparison of different pulse modulation schemes for UWB communications

transceiver should be optimized altogether to achieve best trade-off between circuit complexity, power consumption and system performance.

2.4 Multifunctional UWB system

We have demonstrated that the UWB system architectures for radar and communication are quite similar. In coherent receiver structure based UWB communication system, the time of arrival (TOA) come as a byproduct that can be used for range sensing. Through careful design and arrangement, it is possible that a UWB system can accommodate the task of both exchanging data and detecting range. Figure 2.22 diagrams a possible multifunction UWB system that can work for both communication and radar purposes.

When the system works on communication mode, the transmitter sends out a PPM modulated pulse train. The receiver generates a series of pulses with exactly the same shape and intervals(template signal) to correlate with received pulse train in order to detect if the pulse is delayed from its position(stand for "1") or on time (stand for "0"). Because the received signal time delay is unknown, a synchronization process is needed to align the template pulse train and received signal, which will be the function of the synchronization loop.

When the system works on radar mode, the transmitter sends out periodic pulses with lower pulse repetition frequency (PRF). Same transmitted signal will be used as the template signal at receiver side. Basically the receiver performs the same as in communication mode except that the delay value of the delay generator inside the red block will be processed as the roundtrip traveling time of reflected signal. Notes that in
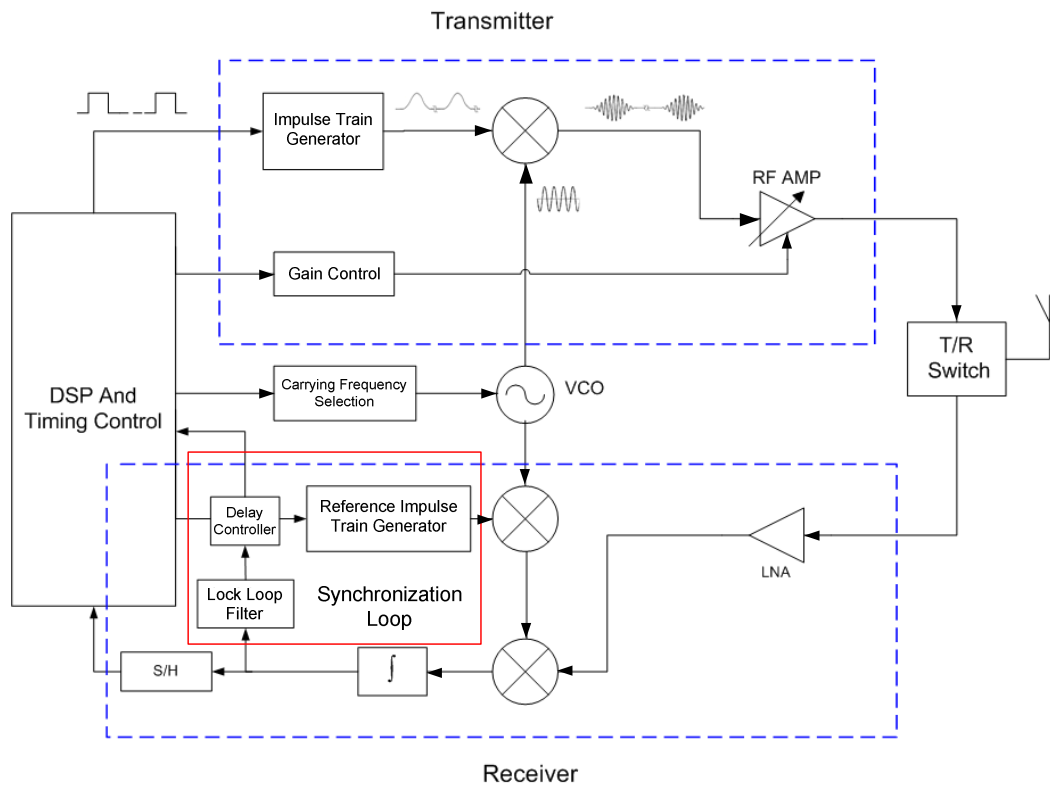
Figure 2.22 Multifunctional UWB system architecture

radar model, both transmitter and receiver use the same clock, which could provide us the transmitting – receiving time delay. The proposed system can use either carrier based UWB signal or carrier free UWB signal. The transmitter needs to have variable gain to serve for different power output level of communication and radar applications. A calibration algorithm is also required when calculating range since the clock prorogation delay in the circuit needs to be taken into account.

CHAPTER III

CARRIER BASED UWB TRANSMITTER DESIGN

3.1 CMOS UWB pulse generator

Although UWB technology is evolving rapidly, the fundamental structure of UWB transmitter has not experienced any radical change. Most design efforts of UWB transmitter are focusing on improving the design of pulse generator. The earlier design conception for pulse generator is to trigger a sharp step by applying a clock signal with large amplitude to an abruptly switching device, such as a step recovery diode (SRD). Then an impulse or mono-pulse can be synthesized from the sharp step signal. Table 3.1summarizes the available devices that can be used for UWB pulse generator before the 1990s. UWB technology mostly targeted for radar and sensing applications during this period. To maximize pulse amplitude, improve power efficiency while obtaining fast rising edge is the main design optimization goal for pulse generator at this stage.

Table 3.1 Summary of available semiconductor devices for UWB pulse generator before the 1990s

Type	Step/Pulse	Best available risetime at amplitude		Notes
Mercury switch	Step	70 ps	300 V	Max PRF = 200 Hz
Avalanche transistor	Pulse	150 ps	12 V	Device selection necessary.
Tunnel diode	Step	25 ps	0.25 V	Fastest transition time.
		100 ps	1.0 V	
Step recovery	Step	60 ps	20 V	Commercially available.
		100ps	50 V	Specially ordered four-
		200 ps	200 V	stack.
Hertzian	Impulse; also	100 ps	1000 V	Limited lifetime, sparkgap.
	pulse modulated.	1 ns	1000 V	
Avalanche diode	Impulse	400 ps	125 V	MHz rep. rate.

As UWB technology extends its reach into low power applications such as short range sensing, geolocation and communications, the integration of UWB pulse generator becomes more and more feasible and attractive. MOSFET has the essential nonlinear I-V characteristics that can be used to shape the fast rising edge required for generating sub-nanosecond UWB pulse. describes this edge sharpening effect of MOSFET. According to Berkeley Short-channel IGFET Model (BSIM) of a typical MOSFET, the drain current and gate source voltage have a nonlinear correlation:

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2] \text{ , when } V_{GS} < V_{th}$$

$$I_D = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}{}^2], \text{ when } V_{th} < V_{GS} < V_{DS} - V_{th} \qquad (3\text{-}1)$$

$$I_D = \frac{1}{2}\mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^2 \text{ , when } V_{GS} > V_{DS} - V_{th}$$

where W and L are the gate width and length of the transistor, respectively. μ is the mobility of the charge carriers. C_{ox} is the gate oxide capacitance per unit area. V_{TH} is the threshold voltage. I_d, V_{GS}, V_{DS} are the drain current, gate-source voltage and drain-source voltage respectively. This I_D - V_{GS} relation is plotted in Figure 3.1. If we apply an input step signal to V_{gs} we can expect to obtain the waveform of output drain current I_{out} through a point-to-point I_D - V_{GS} mapping as shown in Figure 3.1. It can be observed that the attained output current I_{out} is also a step function only with much shorter rising time comparing with input voltage step V_{in}. By cascading several such sharpening stages, a slow-rising step signal can be transformed into step signal with sub-nanosecond rising time. Stemming from this characteristic, most of the recent CMOS UWB pulse generators utilize either analog or digital approaches to synthesize impulse or mono-
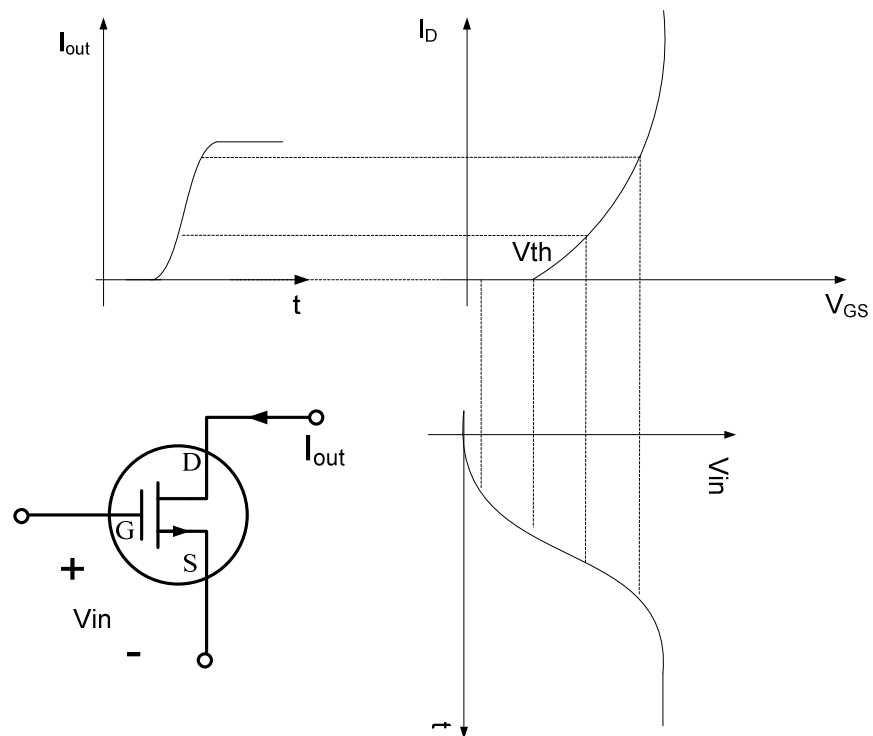
Figure 3.1 Step sharpening effect of MOSFET

pulse [12]-[16]. Usually adding a filter and an inverter-based driver amplifier following

the pulse generator will be able to deliver the required output power to the antenna.

3.2 Carrier based UWB transmitter architecture

Carrier-based UWB transmitter will have to include more building blocks

comparing with simple impulse/mono-pulse transmitter. Essentially, a carrier-based

UWB signal is generated by multiplying an impulse signal with a single-tone carrier

signal. Therefore, the bandwidth and central frequency of the generated signal can be

manipulated by adjusting the pulse width of the impulse signal and the frequency of the
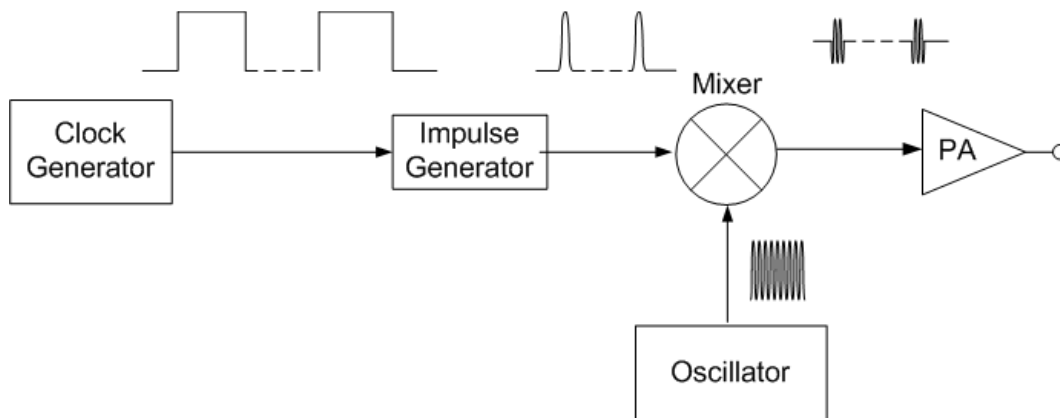
Figure 3.2 Block diagram of a typical carrier-based UWB transmitter

single tone. Figure 3.2 shows a typical carrier-based UWB transmitter. The clock generator is usually composed of timing-control digital circuits and sends out a clock signal that can contain modulation information. The impulse generator produces an impulse signal whose pulse width is inversely proportional to the bandwidth of the required signal. The mixer performs a multiplication between the impulse and a single-tone signal generated by the oscillator. The up-converted signal is then sent to the wideband power amplifier (PA) to achieve required amplitude. In this approach, the oscillator is required to generate multiple tones if the transmitter needs to operate over multiple frequency bands. This carrier-based UWB transmitter suffers from two major disadvantages. First, the PA in the last stage of the UWB transmitter is a challenging design. This PA needs to supply enough gain, have reasonable power efficiency and provide good output matching over a wide frequency range. Second, in UWB radar applications, low pulse repetition frequency (PRF) is often utilized. Since the transmitted signal duration is usually very short, the resultant peak-to-average power ratio is

extremely high. This means no signal needs to be transmitted during most of the time. However, because the PA and other circuits of the transmitter are 'on' all the time, a large amount of power is wasted, rendering the approach power-inefficient. Based on this transmitter configuration various carrier-based UWB transmitters using CMOS and BiCMOS SiGe processes have been developed [17]-[19].

In order to overcome these issues, we proposed a modified UWB transmitter architecture similar to the concept of gated oscillator. Figure 3.3 shows the block diagram of the newly proposed carrier-based UWB transmitter, consisting of a voltage-control oscillator (VCO), a buffer, a SPST switch and two pulse generators. In this approach, power switching is used to perform the signal multiplication, instead of mixing as used in the typical UWB transmitter structure shown in Figure 3.2 and those in [17]-[19]. The transmitter's principle is based upon the concept of generating a carrier-based UWB signal by gating a single-tone signal with a small time window, thereby only producing signal during a small time period. A double-stage switching procedure, using two pulse generators of wide and narrow pulses, and two switches, is adopted in the proposed transmitter to remedy the switching speed limitation of the buffer, inherent in CMOS circuits and to achieve sub-nanosecond gating required in UWB signal generation. The VCO generates carrier signals that define the center frequencies of UWB signal to drive the buffer to achieve sufficient transmitted power and proper output impedance matching. The buffer is gated through its internal switch (first-stage switching) using a wide pulse produced by the pulse generator 1, which should be wide enough to allow the buffer to start and reach stabilization. The second-
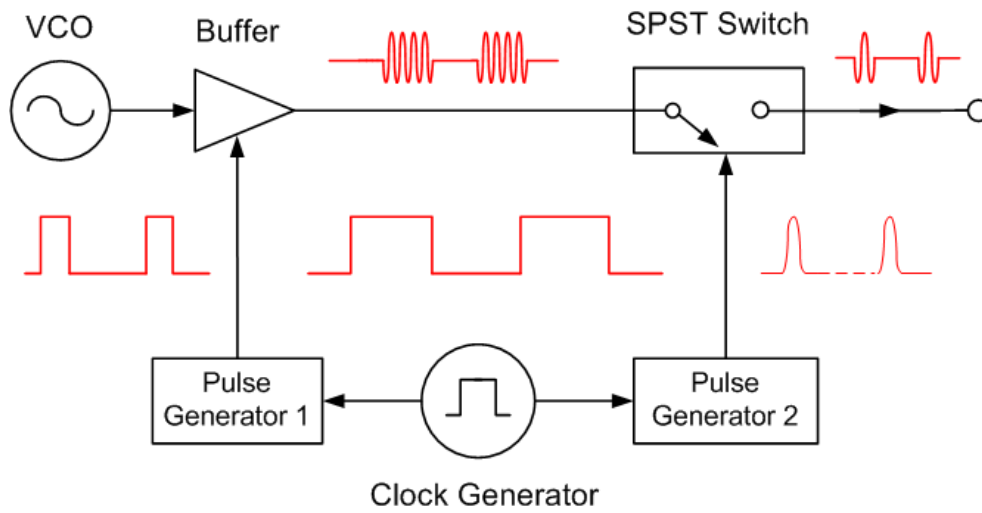
Figure 3.3 The proposed carrier-based UWB transmitter topology
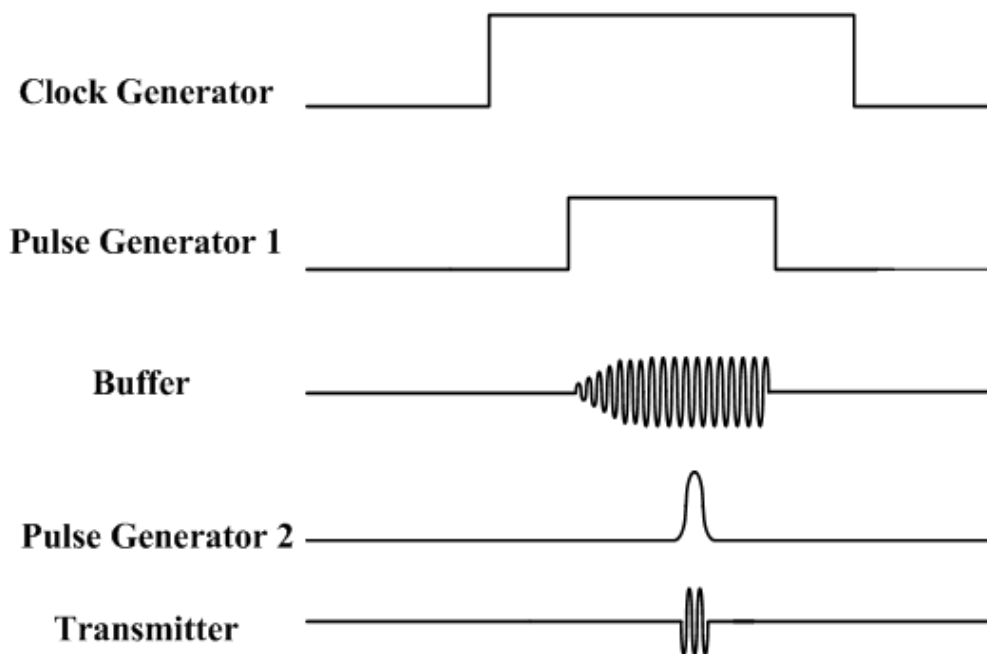
Figure 3.4 Waveforms of the building blocks in the proposed UWB transmitter

stage switching, performed by the SPST switch and the pulse generator 2 generating narrower pulses, is then used to reduce the pulse width of the generated signal, making it an UWB signal having spectrum bandwidth of at least 500 MHz as defined by FCC [8]. Pulse generator 1 and 2 are synchronized using a common clock generator as shown in Figure 3.3.

Figure 3.4 illustrates the time domain waveforms at the output of different blocks of the transmitter. It is noted that the SPST's gating signal from pulse generator 2 needs to fall behind the rising edge of the buffer's gating signal from pulse generator 1 to accommodate the slow switching time of the buffer. Using the first-stage switching to turn on/off the buffer not only saves power, particularly useful for battery-operated UWB devices, but is also needed to relax the isolation requirement for the second-stage switching. In low PRF UWB applications, the level of power leakage needs to be very small, imposing a very strict isolation requirement on the gating components, thus necessitating the use of two switching stages.

Figure 3.5 shows the effects of power leakage and demonstrates the need for two switching stages. In Figure 3.5 (a), only the second-stage switching is used. *Ts* stands for the pulse width of the UWB signal, while *Ti* is the interval between two consecutive pulses. During the time the second-stage switching is off, the LO signal (i.e., the VCO's signal) still manages to arrive at the transmit antenna due to limited SPST switch isolation. Although this LO leakage has much smaller amplitude than the transmitted UWB signal, it can still accumulate sufficiently large power over the duration *Ti* to over-drive the UWB signal on the transmitted spectrum. When such situation happens, a high-
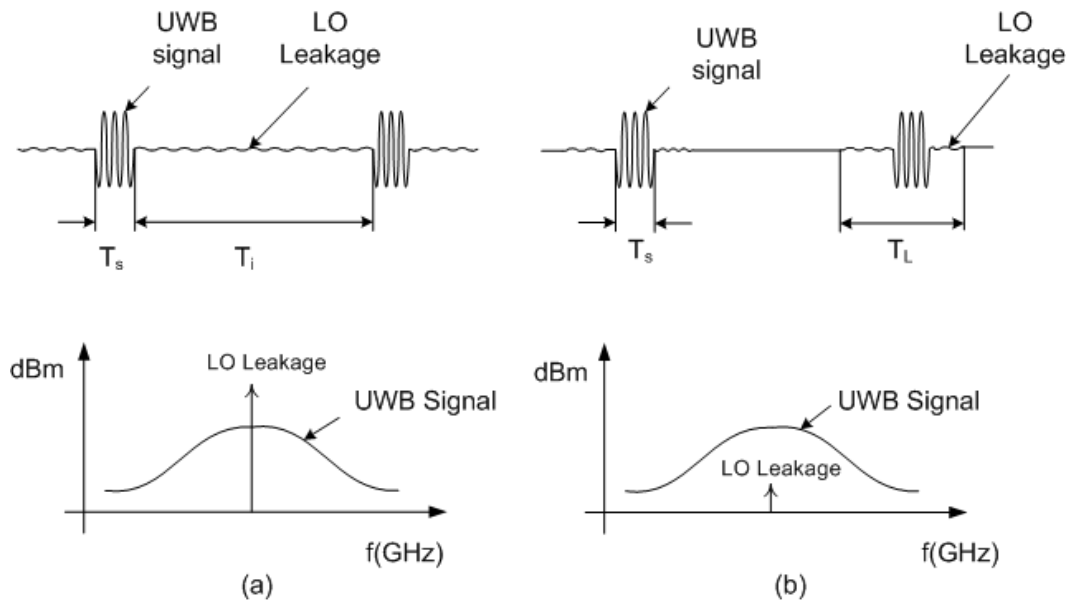
Figure 3.5 Effects of power leakage using (a) single-stage and (b) double-stage switching

power single tone would be observed at the carrier frequency above the UWB signal spectrum. To avoid this problem, the signal-to-leakage ratio should be much higher than *Ti/Ts*. For instance, for a 1-ns UWB signal pulse to be transmitted at 10-KHz PRF with negligible power leakage, the ratio *Ti/Ts* is roughly about 105 and an isolation of much more than 50 dB is thus required to satisfy the leakage requirement if only one switching stage was used (i.e, the second stage). This level of isolation is very difficult to achieve in CMOS switches. In Figure 3.5 (b), both switching stages are applied. The LO leakage only appears during the time the buffer is on; i.e., within the time widow T_L, which is usually no longer than 10 ns. The isolation of the second-stage switching is only required to be larger than T_L/Ts. In this case, 30-dB isolation is sufficient to ensure small LO

leakage regardless of the PRF used. For CMOS switching, 30-dB isolation is a modest requirement and can be achieved by careful design.

3.3 The implementation of UWB transmitter

In order to verify the concept and feasibility of the proposed UWB transmitter topology a new carrier-based UWB transmitter covering the entire UWB band of 3.1-10.6 GHz is realized using a pulse generator-SPST switch CMOS chip, designed and fabricated using the TSMC 0.18-um CMOS process [20], and an external frequency synthesizer. The transmitter is based on the concept proposed in Figure 3.3 but implemented without the pulse generator 1 and the VCO and buffer replaced with an external frequency synthesizer.

3.3.1 CMOS SPST switch design

Figure 3.6 shows the schematic of the CMOS SPST switch. One serial and two shunt MOSFETs are used to provide compromise between insertion loss and isolation. In order to achieve an ultra-wide bandwidth, on-chip inductors between adjacent transistors are combined with the transistors' parasitic capacitances to form a synthetic transmission line between the input and output of the SPST switch. The bulk (or substrate) terminals of the transistors are floated to improve the power handling ability and insertion loss [21]. The SPST's on- and off-state are obtained when the control signals $V_{ctl} / \overline{V}_{ctl}$ are set to Vdd/zero and zero/Vdd, respectively. To ensure wideband performance, the sizes of the serial and shunt transistors need to be carefully determined. The serial transistor
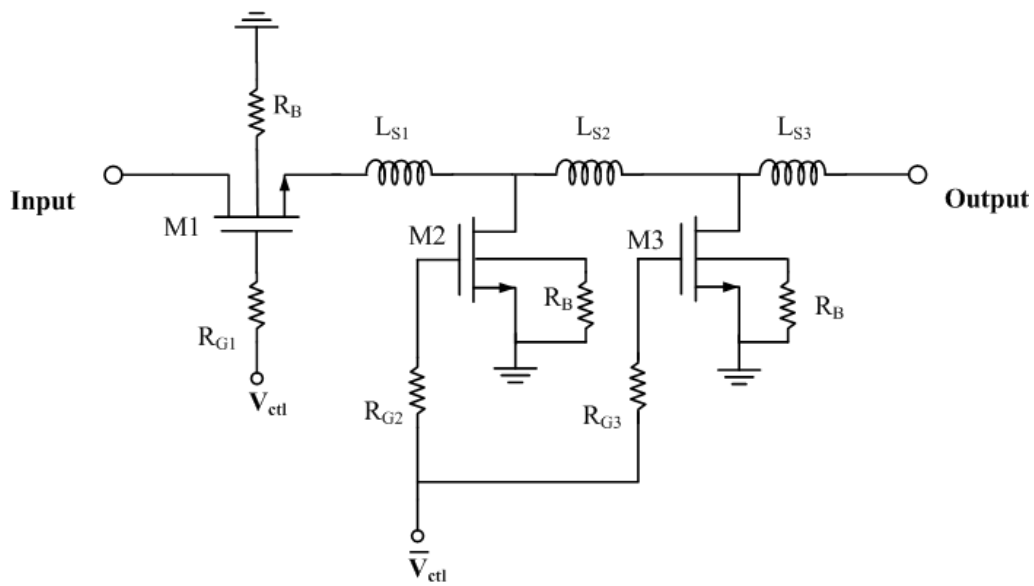
Figure 3.6 Schematic of the CMOS SPST switch

particularly plays an important role in the switch's insertion loss, while the shunt transistors enhance the isolation when the switch is off. Shunt devices, however, inadvertently aggravate the insertion loss due to their parasitics.

For serial-connected transistor the size needs to be carefully chosen, as the gate width is increased, the on-resistance reduces, resulting in low insertion loss in the low-frequency region. The gate-source parasitic capacitance, however, increases, and hence degrading the insertion loss at high frequencies. Figure 3.7 compares the insertion loss of two 0.18-µm MOSFETs, each in series configuration, having two different gate widths (64- µm and 192-µm).   As can be seen, the smaller-size transistor has higher loss at lower frequencies but its insertion loss maintains relatively constant over a wide frequency range. For shunt-connected MOSFETs, a larger size provides higher isolation at lower frequencies.
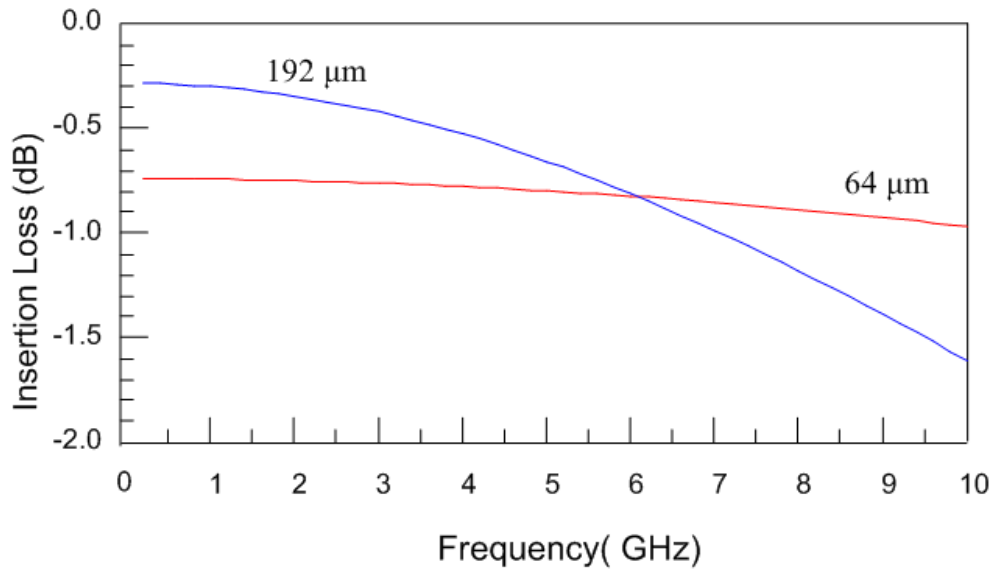
Figure 3.7 Insertion loss comparison of two 0.18-µm MOSFETs having different widths

Typical SPST transistor switch structures are only suitable for slow switching due to the fact that the transistor's gate uses a large biasing resistor to make the gate open at RF so that the switch performance is not affected. This gate biasing resistor, however, leads to a large RC constant, which effectively slows down the control signal applied to the control terminal connecting to the gate via the resistor. Figure 3.8 demonstrates effect of the gate biasing resistor, assuming an ideal step-signal is applied to the control terminal. Due to the gate resistor R_g and gate-to-ground parasitic capacitance C_p, the rising edge of the resultant gate voltage V_g is slowed down. It can be concluded that, a larger gate resistor gives a slower rising edge, leading to slower switching speed. From Figure 3.8, it is apparent that in order to maintain the fidelity of the control sub-nanosecond pulse signals, the gate resistance should be less than a few

Control Step Function
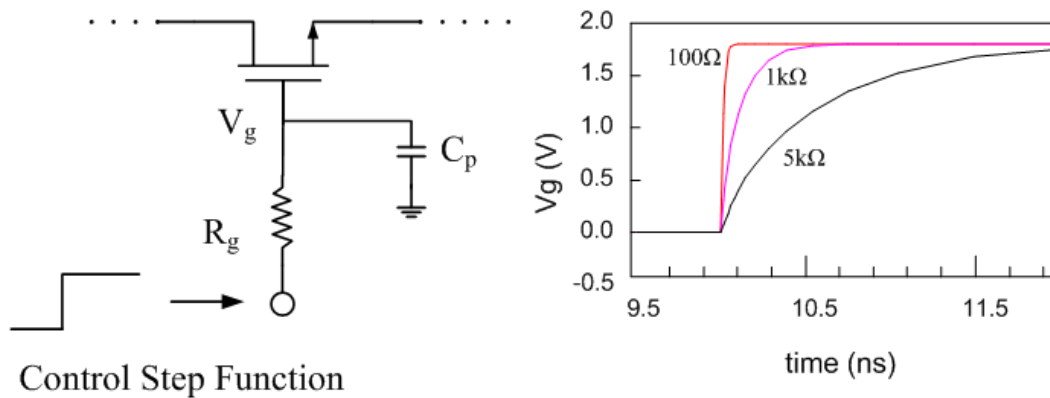
Figure 3.8 (a) MOSFET with a step function applied to the gate and (b) behavior of the gate voltage V_g for different gate bias resistances

hundred ohms. Although this may aggravate the insertion loss and return loss of the switch, the switch is expected to have reasonably good performance by optimizing its other components, while maintaining the rising/falling edge of the control pulse signal.

The gate of each transistor in the SPST switch is in series with an inverter that

(a)   (b)
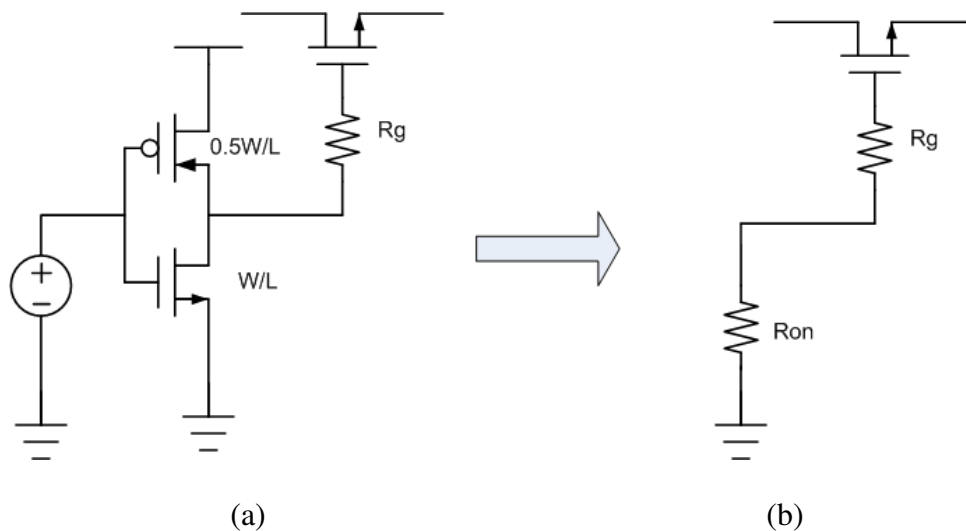
Figure 3.9 The inverter load that connect to the gate of the transistors in SPST switch (a) and its equivalent circuits (b)
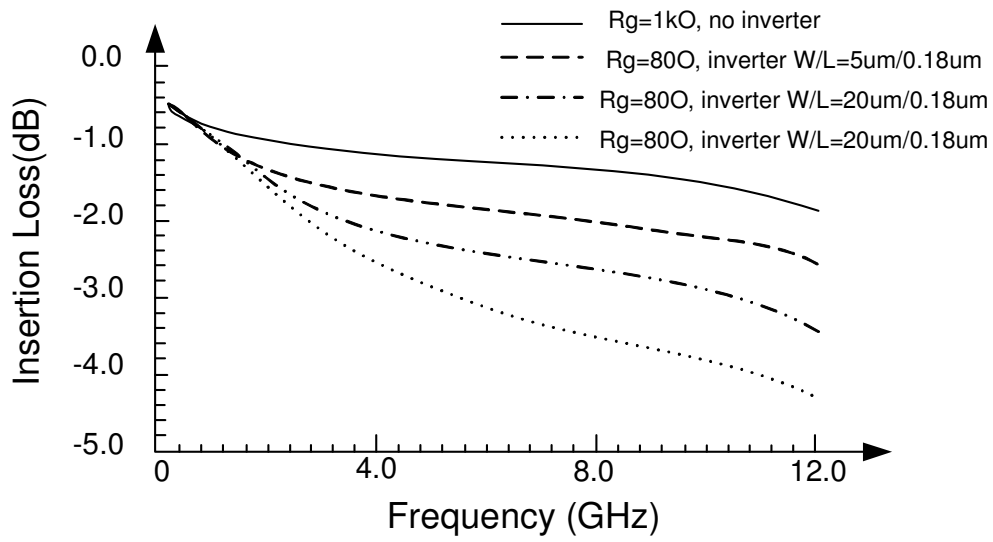
Figure 3.10 The effect of gate resistor and inverter transistor size

has a non-zero output impedance as shown in Figure 3.9. This impedance is equal to the turn-on resistance (R_{on}) of PMOS in the inverter. This resistor (R_{on}), in series with the gate resistor, will actually improve the insertion loss of the SPST switch when gate resistor value is limited. Figure 3.10 compares the insertion loss of a serial transistor with four different loads at its gate. A large gate resistor of 1k ohms is preferred when designing slow switching SPST switch since it gives less loss. Using 80 ohms gate resistor alone to achieve fast switching increases insertion loss by as large as 2dB. While adding a small size inverter in series with 80 ohms gate resistor will only increase the insertion loss by 0.5dB. Table 3.2 summarizes the designed circuit elements in SPST switch.

The SPST switch has been measured on-wafer using a probe station and an automatic network analyzer. Figure 3.11 shows the measured results. The SPST switch

Table 3.2 Summary of the designed SPST's components

Circuit Element	Element Value
M1	512-µm gate width
M2, M3	368-µm gate width
L_{S1}	0.3 nH
L_{S2}	0.6 nH
L_{S3}	0.3 nH
R_{G1}	100 Ω
R_{G2}	100 Ω
R_{G3}	100 Ω
R_B	20 KΩ
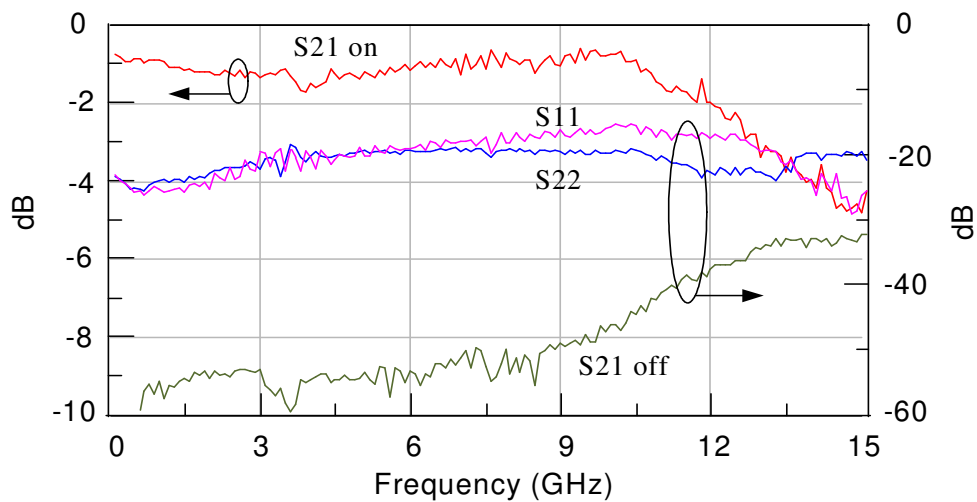
Figure 3.11 Measured insertion loss (S21 on), input return loss (S11), output return loss (S22) and isolation (S21 off) of the 0.18-µm CMOS SPST switch

exhibits measured insertion loss between 0.8 to 1.7 dB, return loss greater than 15 dB, and isolation more than 30 dB from 0.45 MHz to 15 GHz. The performance of SPST switch assures its ability to cover the complete 3.1-10.6GHz UWB band.

3.3.2 CMOS pulse generator design

The pulse generator produces an impulse signal to control the SPST switch. It is preferred that the impulse duration be adjustable so that different bandwidths can be attained for the UWB signal. The pulse generator is implemented based on digital logics NAND gate [22]. Comparing with other pulse generator circuits, this method of pulse generation is especially attractive for our transmitter because it can provide full voltage swing required for the SPST switch operation [23]-[30].

Figure 3.12 shows the designed CMOS pulse generator. An inverter chain is used to sharpen the rising/falling edge of the clock generator's signal needed for subsequent generation of narrow impulse-like signals. The sharpened clock signal is split into two branches. In one of the branch, the clock is delayed and inverted with respect to the other. The NAND gate then combines the rising and falling edges of these clocks to form an impulse. This pulse and its inversion are used to control the shunt and serial transistors in the SPST switch, respectively. The duration of the generated impulse is determined by the delay between the rising and falling edges. The current starved
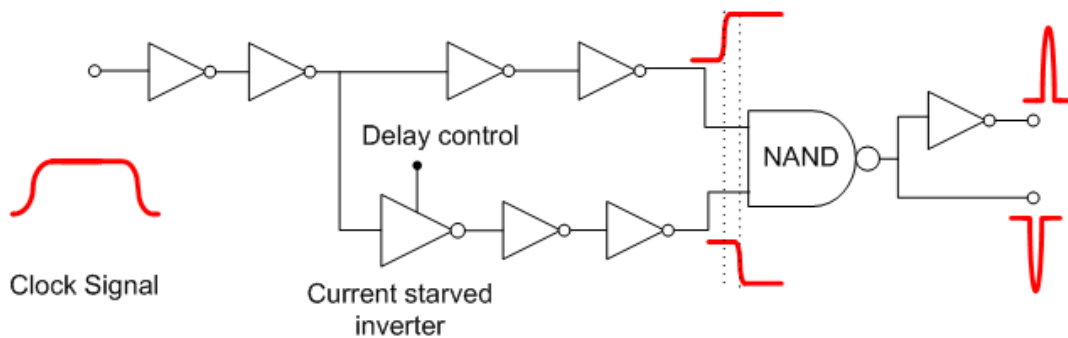
Figure 3.12 Impulse generation using digital NAND gate

inverter, indicated in Figure 3.12 and elaborated in Figure 3.13, is used to flip the clock and generate tunable delay. The delay of an inverter is determined by the time used by the current to charge and discharge the load capacitance. Consequently, varying the inverter charging/discharging current through biasing can change the inverter delay, hence producing tunable impulse which consequently produces variable UWB signal bandwidths.

Figure 3.14 displays different durations of the impulse reaching the gate of the SPST switch at different biasing voltages that control the impulse generator. It is a common assumption that the pulse with of an impulse, used as the gate control signal for a SPST transistor switch, is equal to the duration of the output signal emerging from the

(a)   (b)
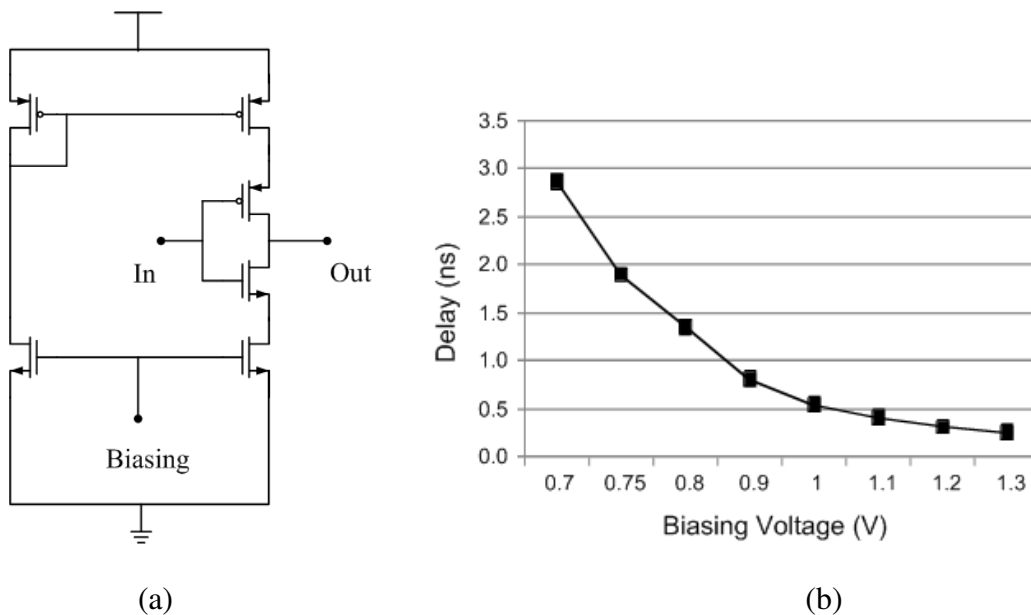
Figure 3.13 Current starving inverter structure (a) and its delay tuning range (b)

switch. However, we find that, in practical circuits, these durations are not the same, mainly due to the fact that the amplitude of the output signal of the switch does not have a linear relationship with the control voltage, which results in different time-dependence between the switch's output signal and the control signal. Figure 3.15 briefly explains this phenomenon. Suppose an impulse with 400-ps rising edge, as shown in Fig. 12(a), is used to control the switch. Figure 3.15(b) displays the calculated normalized output amplitude of the switch versus the control voltage, showing that the switch output begins to appear for control voltage higher than 0.7 V. Figure 3.15(c) shows the switch's output amplitude as a function of time, obtained by mapping the output amplitude into the time domain using the data from Figure 3.15(a) and (b). As can be seen, the rising edge of the output signal is compressed to 200 ps. This sharpened edge is expected to result in an UWB signal having narrower duration than that of the control impulse.
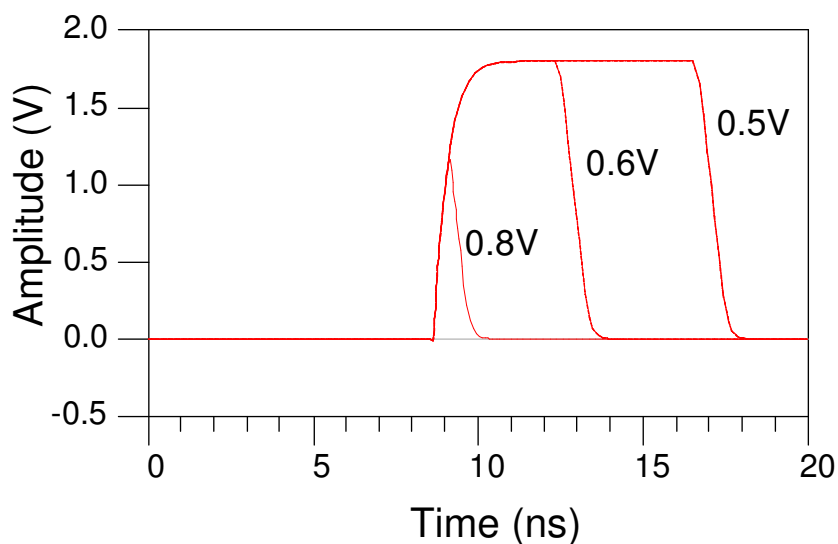
Figure 3.14 Different simulated pulse widths controlled by the bias voltage
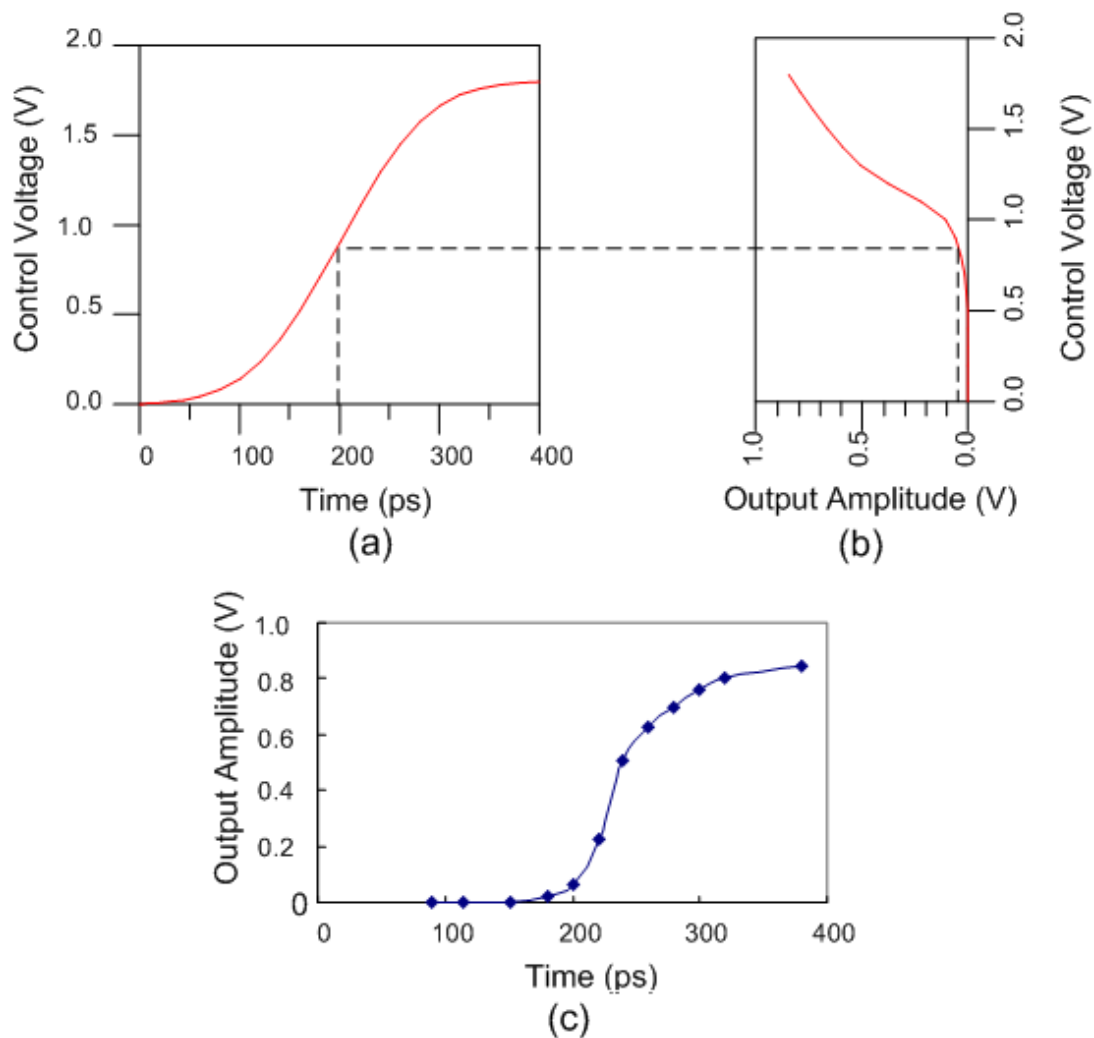
Figure 3.15 Rising edge compression of the SPST switch

It is expected that the gating impulse signal will couple to the transmitter's output port through the transistors' gate-source capacitances. To minimize this undesirable effect, a slower rising/falling edge for the control signal is preferred. By exploiting the edge compression property of the switch, as explained earlier, we can afford to relax the rising/falling edge restriction for the control signal while still meeting the minimum pulse width requirement for the UWB signal. As will be seen in the measurement results

of the new transmitter, the gate coupling is negligible as compared with the generated

UWB signal. The pulse generator circuit is not fabricated and measured separately.

Nevertheless, its workability is demonstrated through the measurement of the entire

CMOS chip integrating the pulse generator and SPST switch.

3.3.3 Measurement results

The 0.18-mm CMOS pulse generator-SPST switch chip has been used in

conjunction with an external frequency synthesizer to demonstrate a new carrier-based

UWB transmitter. The CMOS chip's microphotograph is displayed in Figure 3.16. The
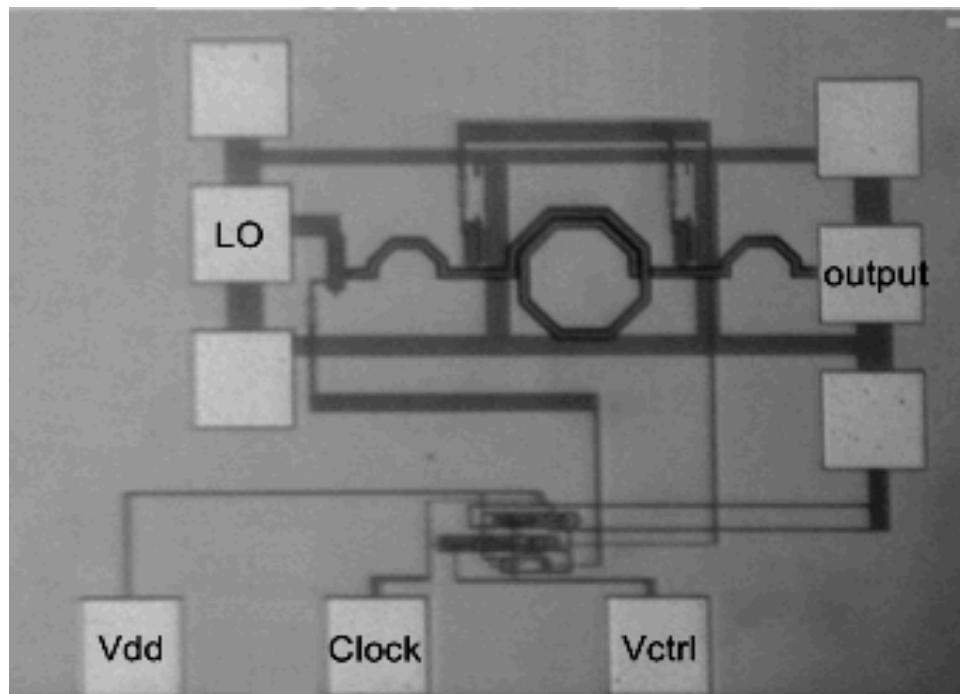
Figure 3.16 Microphotograph of the 0.18-μm CMOS chip integrating the pulse
generator and the SPST switch

die area of the whole circuit is 850 µm by 700 µm including input and output on-wafer pads. The measurement was conducted on-wafer. The frequency synthesizer supplied the LO signal feeding the input port of the pulse generator-SPST switch chip. A 15-MHz clock was used to drive the on-chip pulse generator. The whole circuit consumes less than 1-mA DC current.

Figure 3.17 displays the time domain waveform and the spectrum of a measured UWB signal. The UWB signal has a 3-dB pulse width of 4 ns and a 10-dB bandwidth of 500-MHz at 5-GHz center frequency, which conforms to the FCC's minimum UWB bandwidth requirement. The UWB signal amplitude is 2-V (peak-to-peak) and its amplitude at 5 GHz is -20 dBm. The 2-V peak-to-peak voltage is the maximum voltage level corresponding to the SPST being turned on completely. The side-lobe level is below –15 dBc. By increasing the external biasing voltage for the pulse generator, the pulse width of the UWB signal is reduced. When the pulse width is reduced to a certain value, the amplitude of the UWB signal, however, diminishes due to the fact that the SPST switch cannot be completely turned on any more, which results in partial reflections of the carrier signal. When the amplitude of the UWB signal decreases to half of its maximum value (2 V), the corresponding duration is defined as the minimum pulse width. This minimum pulse width was measured as 0.5 ns. Figure 3.18 displays the UWB signal with this minimum pulse width. The peak-to-peak voltage amplitude is around 1V. The 10-dB bandwidth is around 4 GHz. The LO leakage overshooting can be seen from the spectrum for this signal because only a single-stage switching is used here. This LO leakage confirms experimentally the need of a double-stage switching for

(a)

Frequency (GHz)
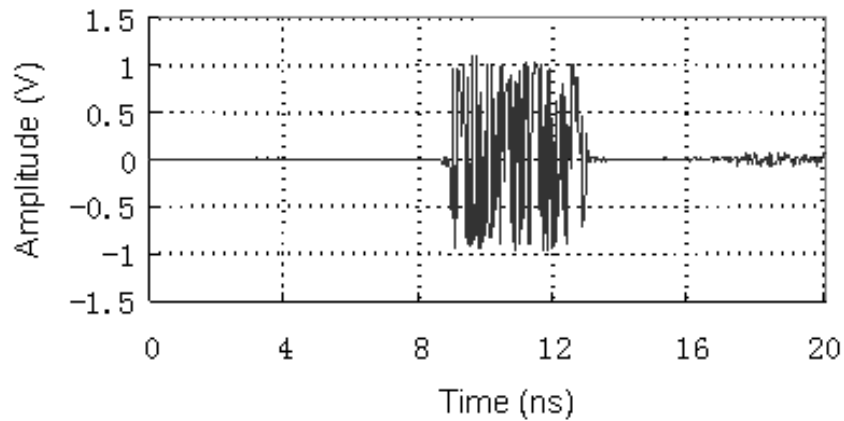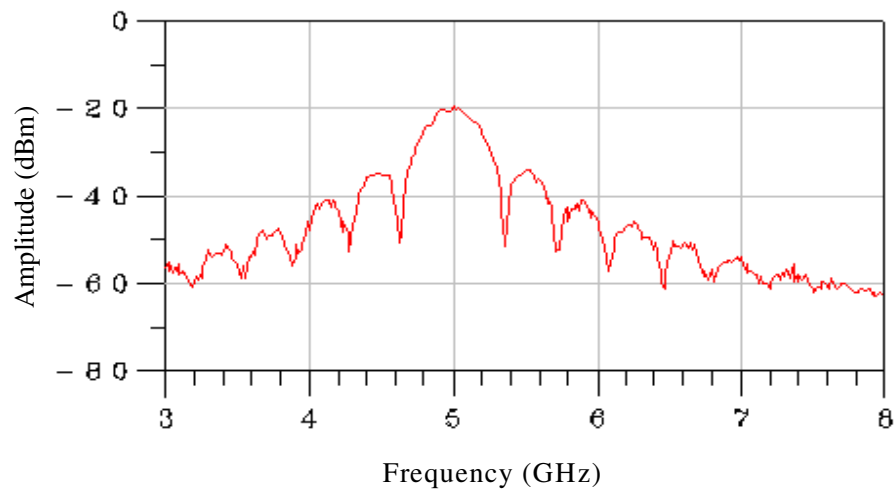
(b)

Figure 3.17 Measured UWB signal having 500-MHz bandwidth: (a) time domain waveform and (b) spectrum

the carrier-based UWB transmitters (Figure 3.3) as explained earlier. With another stage of switching, the LO leakage can be reduced to a negligible level. The pulse width of the obtained UWB signal can be further reduced by increasing the bias voltage of the
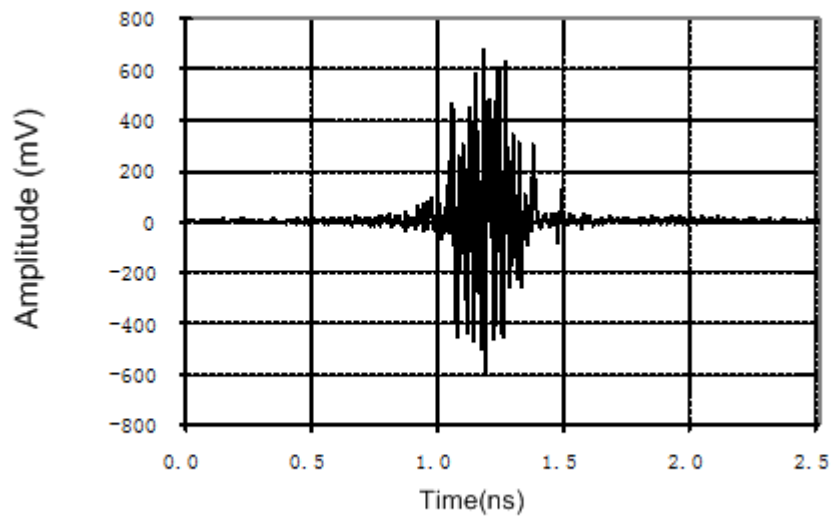
(a)
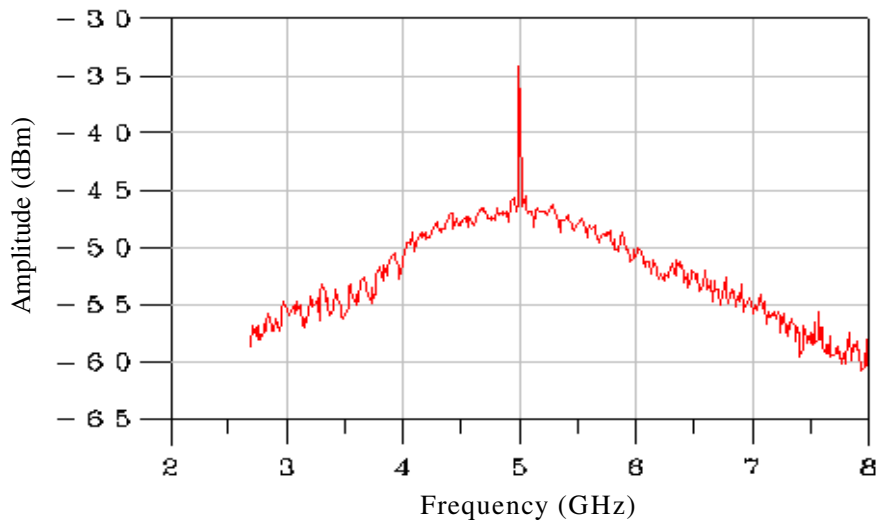
(b)

Figure 3.18 Measured UWB signal having 4-GHz bandwidth: (a) time domain waveform and (b) spectrum

pulse generator, hence achieving wider signal bandwidth than 4 GHz. This, however, is obtained at the expense of its signal amplitude.

Figure 3.19 shows the measured spectrums of different UWB signals obtained by varying the carrier frequency at a certain bias voltage for the pulse generator, demonstrating that the entire UWB band of 3.1-10.6 GHz can be achieved with the developed CMOS chip by using a multi-band signal source.

To evaluate effects of coupling from the impulse signal applied to the SPST's control terminals, we remove the LO input signal and directly observe the coupled signal at the output. The measured coupled signal and its spectrum are displayed in Figure 3.20. The observed positive and negative portions correspond to the rising and falling edges of
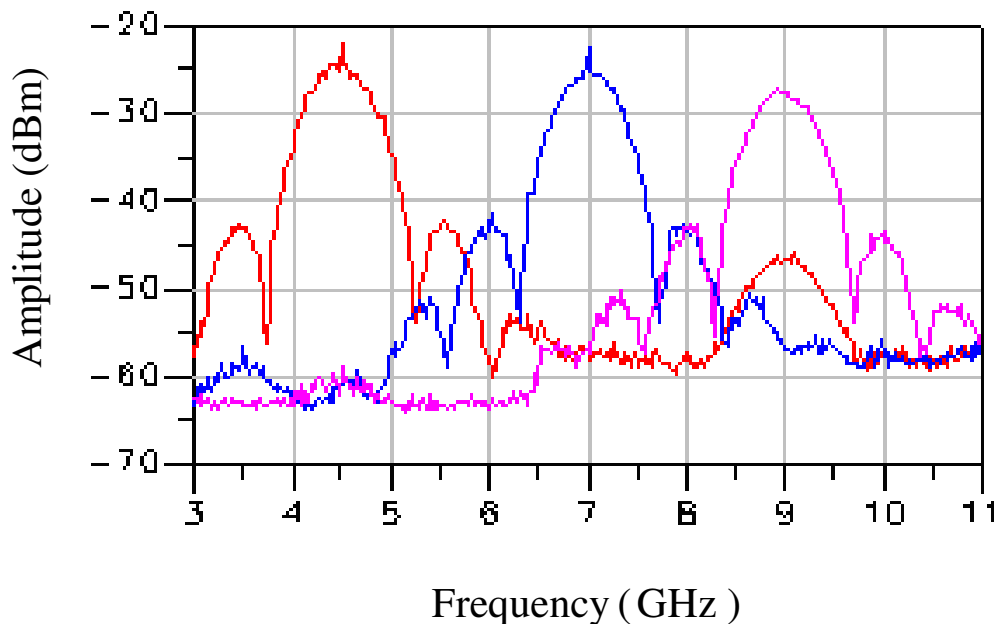
Figure 3.19 Measured spectrums of UWB signals covering the 3.1-10.6GHz UWB band
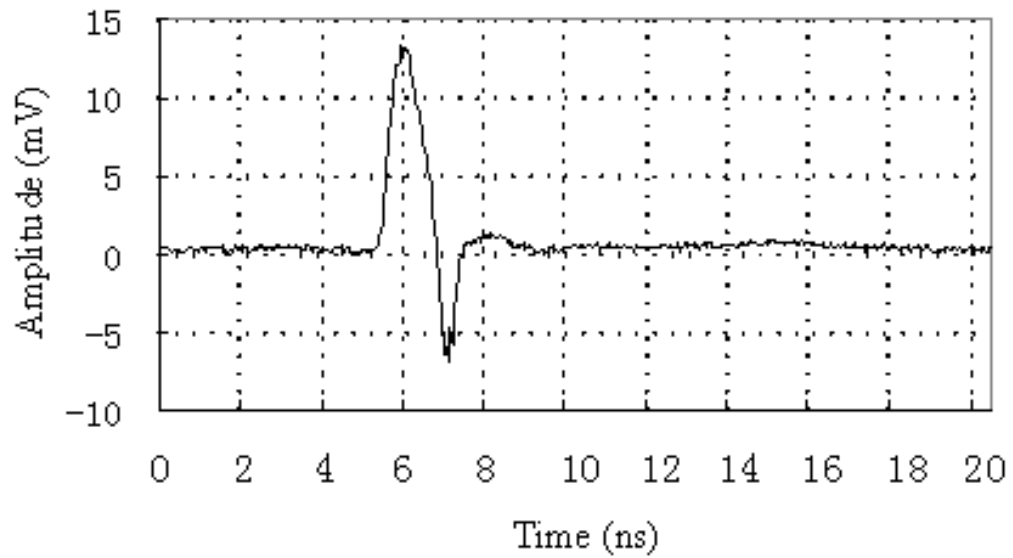
(a)
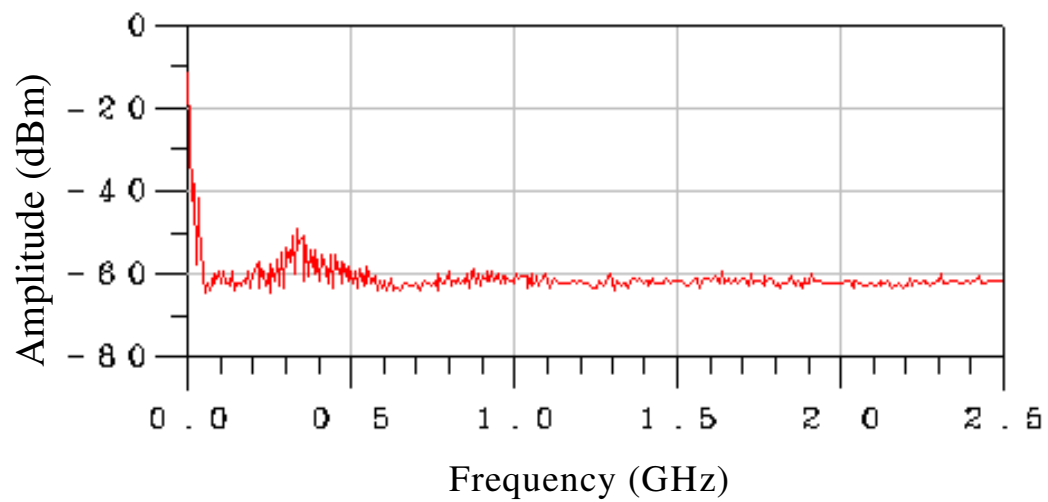
(b)

Figure 3.20 Measured output signal coupled from the impulse control signal (a) and its spectrum (b)

the control impulse, respectively. When the pulse width of the control impulse is increased, the positive and negative parts move away from each other. On the contrary, when the pulse width is reduced, they overlap and cancel each other. The time domain results show that the amplitude of the coupled signal is negligible as compared to the UWB signals shown in Figure 3.17 and Figure 3.18. Furthermore, the energy of this coupled signal is mainly distributed below 1 GHz, as seen in Figure 3.20(b), signifying that the signal is out of the UWB band and can be easily removed using a filter.

CHAPTER IV

UWB SAMPLING RECEIVER FRONT END DESIGN

.
 Sampling techniques have long been used to capture periodic waveforms over wide bandwidths in oscilloscopes. The fundamental principal of sampling is the repeated capturing of subsequent points of a time-varying waveform by sampling gate. The gate is open and closed by a narrow pulse, which is triggered repeatedly. Sampling technology's capability of recovering periodical wideband signal makes it a popular receiver front-end structure in UWB radar and sensing applications as we indicated in Chapter II. Microwave integrated circuit (MIC) and monolithic microwave integrated circuit (MMIC) have been the major technologies used to implement low cost wideband sampling receiver front-end [31]-[33]. CMOS based sampler design has also been published recently, but mainly aiming at narrow band systems [34]-[38]. With the aid of integrated impulse generator, CMOS process is capable of conducting sampling over wide bandwidth, which can compete with or even outperform diode based sampling system.

4.1 The modeling of sample and hold circuit

 The sampling circuit can be modeled as a switch loaded by a capacitor C_H which holds the sampled voltage after sampling. As illustrated in Figure 4.1 an impulse controlled sampling switch can be equivalent to a resistor with time variant conductance $g(t)$, which is in linear relation with control voltage of the switch. A first order linear differential equation can be written for this system:

$$C_H \frac{dV_O(t)}{dt} = [V_{in}(t) - V_O(t)]g(t) \tag{4-1}$$

For simplification purpose, we assume the switching impulse have symmetric linear rising/falling edge. Therefore $g(t)$ can be written as:

$$g(t) = \begin{cases} \dfrac{g_0}{t_r}t\ ,\ 0 < t < t_r \\[2mm] g_0,\ t_r < t < t_w - t_r \\[2mm] \dfrac{g_0}{t_r}(t_w - t)\ ,\ t_w - t_r < t < t_w \end{cases} \tag{4-2}$$

where t_r is the rising/falling time of the impulse, t_w is the duration of the impulse while g_0 is the turn on conductance of the sampling switch. After combining equation (4-1) and (4-2), the input to output transfer function of the sampling system can be analytically solved as [39]:
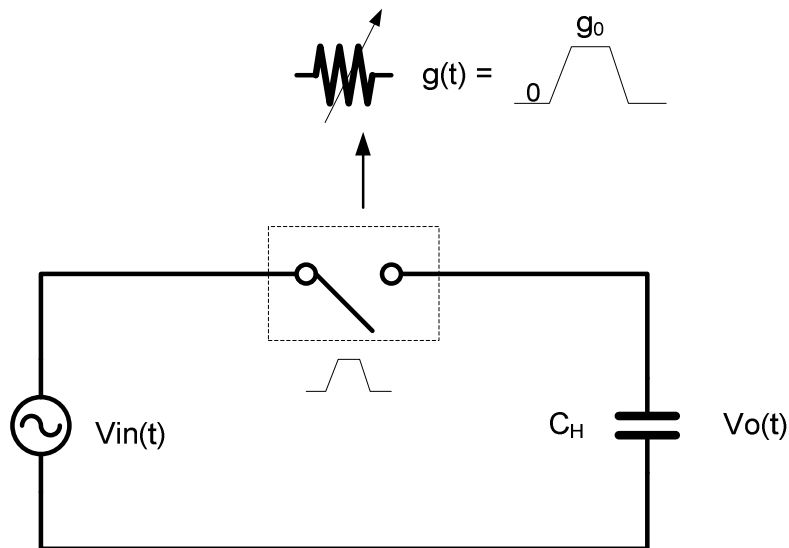
Figure 4.1 Sampling circuit model

$$
h(t) = \begin{cases}
\dfrac{g_0 t}{C_H t_r} e^{\frac{(t^2 + 2t_r^2 - 2t_w t_r) g_0}{2 C_H t_r}} & , \quad 0 < t < t_r \\[4mm]
\dfrac{g_0}{C_H} e^{\frac{(2t + t_r - 2t_w) g_0}{2 C_H}} & , \quad t_r < t < t_w - t_r \\[4mm]
\dfrac{g_0 (t_w - t)}{C_H t_f} e^{\frac{(t - t_w)^2 g_0}{2 C_H t_r}} & , \quad t_w - t_r < t < t_w
\end{cases}
\tag{4-3}
$$

Performing a Fourier transformation for h(t) will be able to get the frequency response of the sampling system. The numerical results indicate that the bandwidth of the sampling is relatively independent of pulse duration t_w while directly affected by rising/falling time t_r. Since the expression in equation (4-3) is too complicated to give an insightful design guideline, we carry out a curve fitting for the calculated bandwidth of a sampling system with $C_H = 1pF$, $g_0 = 1$ s and come up with an empiric equation for estimating the bandwidth of a sampling system:

$$
B \approx \frac{6.3}{\sqrt{t_r}}
\tag{4-4}
$$
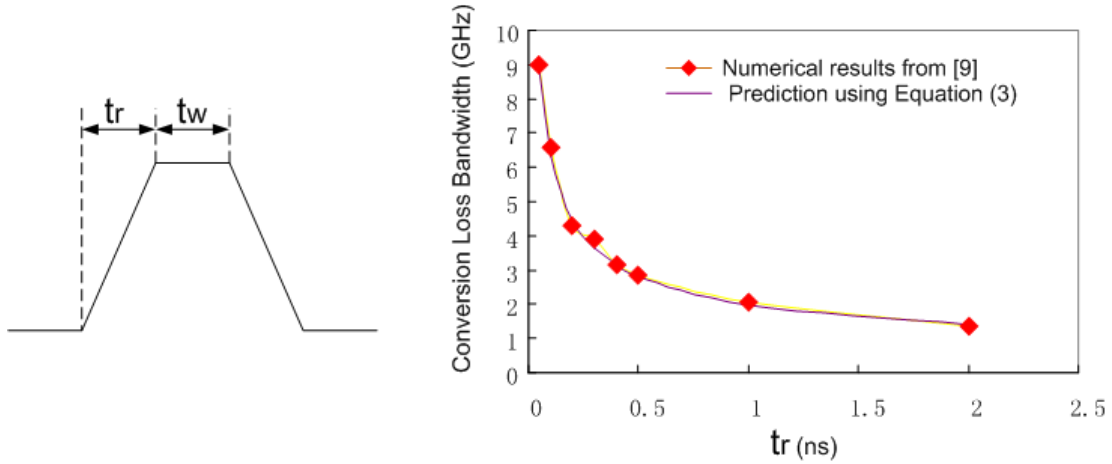
Figure 4.2 Pulse model of a sampling strobe (a) and its effect on sampling bandwidth (b). t_w was set to 0 when calculating the conversion loss using (4-3) and results are similar for other values of t_w

where t_r is in *ns* and bandwidth *B* is in *GHz*. Figure 4.2 compares the sampling

bandwidth using (4-4) and the numerical results based on analytical model (4-3). A good

agreement can be found between the two results, making the simple equation (4-3) good

enough for design purpose. Considering that the bandwidth of sampling system is also

affected by its RC constant as $B = 1/\sqrt{C_H R_{on}}$, (4-3) can be modified to take into

account the switch-on resistance and holding capacitance as

$$B \approx \frac{6.3}{\sqrt{t_r C_H / g_0}} \tag{4-5}$$

In addition to the factors included in (4-5) the jitter of the sampling clock could also cause significant sampling bandwidth reduction [40]. Figure 4.3 depicts how the jitter of sampling clock raises the noise on the sampled voltage. The dithered clock will cause the sampling position vary randomly, which will appeared as sampling error. For a certain rms jitter Δt of the sampling clock , the rms of resultant sampled voltage error can then be derived from the plot in Fig. 4.3 as

$$\tilde{N}_s = \frac{dV(t)}{dt}\bigg|_{rms} \times \Delta t = \sqrt{\frac{1}{T}\int_0^T (\frac{dV(t)}{dt})^2 \, dt} \times \Delta t \tag{4-6}$$

where T is the period of the sampled signal. Assume $V(t)=Asin(2\pi ft)$, then

$$\tilde{N}_s = \sqrt{2}\pi fA\Delta t \tag{4-7}$$

It can be observed that as frequency of the input signal increase, the jitter caused noise rise accordingly. This explains the decrease of sampling bandwidth with the existence of sampling clock jitter.
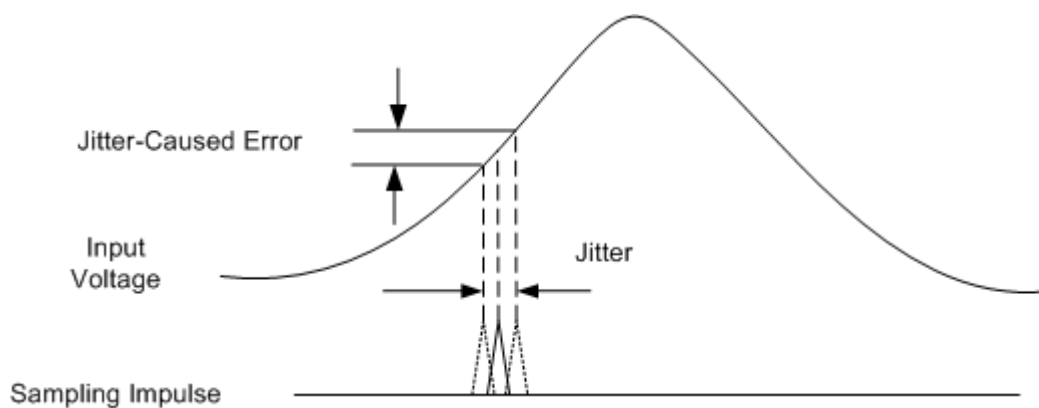
Figure 4.3 Derivation of jitter caused noise
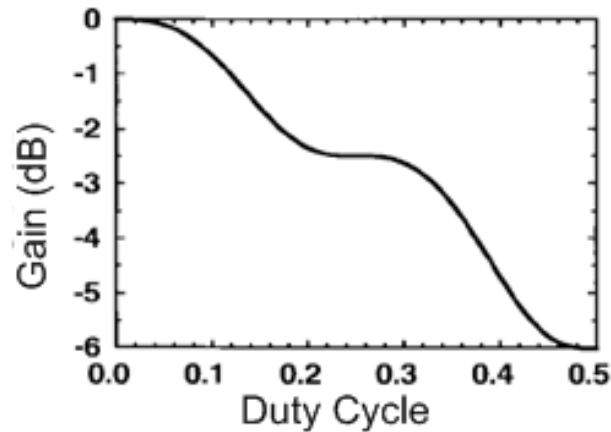
Figure 4.4 The relationship between conversion gain and duty cycle for an ideal sampling circuit

The conversion gain of the sampling system, however, cannot be accurately modeled by equation (4-3) since the model is linear and there is no frequency transformation involved. The nonlinear model shown by Parssinen and Magoon [41] indicates that the smaller duty cycle the sampling pulse has, the less conversion loss the sampling circuit will produce. Figure 4.4 demonstrates the relationship between conversion gain and duty cycle based on the model in [41]. It's easy to understand because wider pulse with larger duty cycle has more "switch-on time", during which the holding capacitor have RF signal passing. Accordingly the output voltage will contain more RF power, less IF power, resulting a lower conversion gain. Figure 4.5 plots the simulated conversion gain with 300ps and 10ns wide sampling pulse respectively. The period of sampling clock is 25ns. The simulated 4dB gain difference between two sampling pulses is quite close to the results given in Figure 4.4.
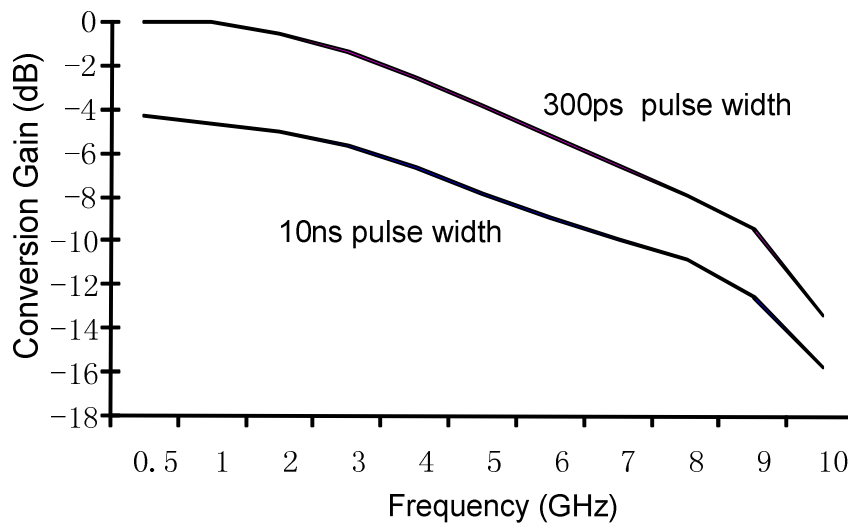
Figure 4.5 Conversion gain comparison using different sampling pulse duration

4.2 Sampling switch design

The sampling switch can be implemented using either a NMOS switch or a NMOS/PMOS transmission gate representing NMOS and PMOS connected in parallel as seen in Fig. 4.6. NMOS switch has simpler structure and only requires one control signal. The NMOS/PMOS transmission gate requires a pair of control signal but is more linear. To investigate their effects on noise figure a frequency domain simulation is conducted for a simple sampler. The sampling clock frequency is set to 40MHz. First sampler uses a single NMOS as sampling switch with 150ps rising/falling time, second sampler uses a NMOS/PMOS pair switch with 150ps rising/falling time, while third sampler use a NMOS/PMOS pair switch with 100ps rising/falling time. The effect of 1/f can be observed at below 100kHz frequency range from Figure 4.6. NMOS/PMOS transmission gate have dramatically less 1/f noise due to the better noise performance of

PMOS. For NMOS switch, increasing transistor size will increase the 1/f noise according to simulation. Shorter rising/falling time can also bring down the 1/f noise floor. At 40MHz, 80MHz , 120MHz, noise peaks appear. This is due to the harmonic of sampling clock at the output of the sampling capacitor. From the comparison we can conclude that a NMOS/PMOS transmission gate is preferred as sampling switch to achieve better noise performance.
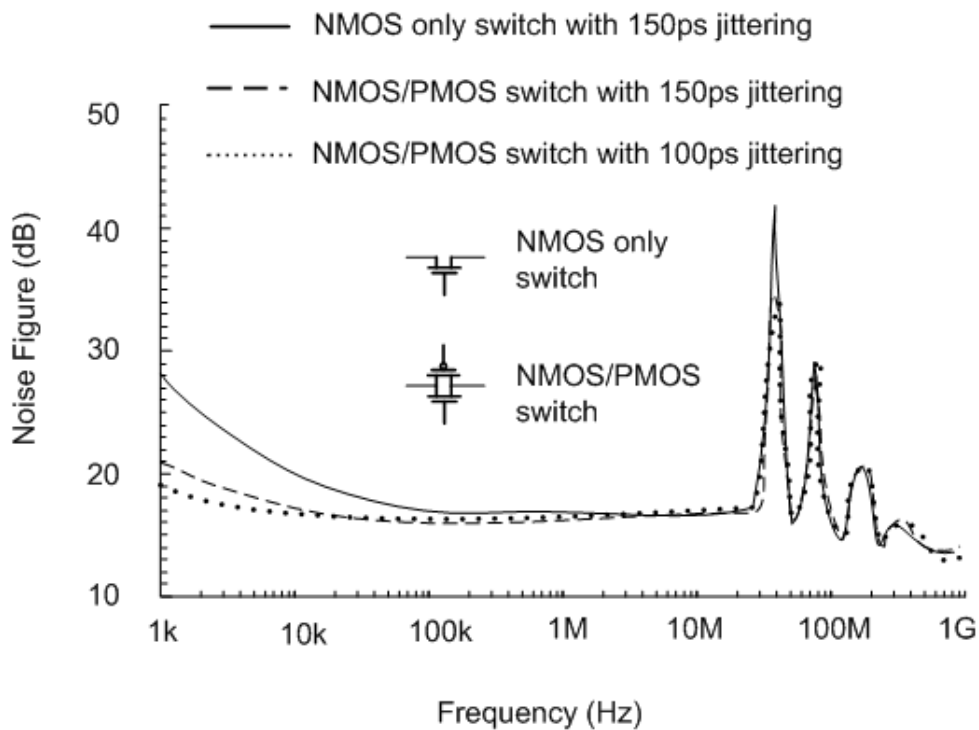
Figure 4.6 Noise figure of simple sampler with different switch structure
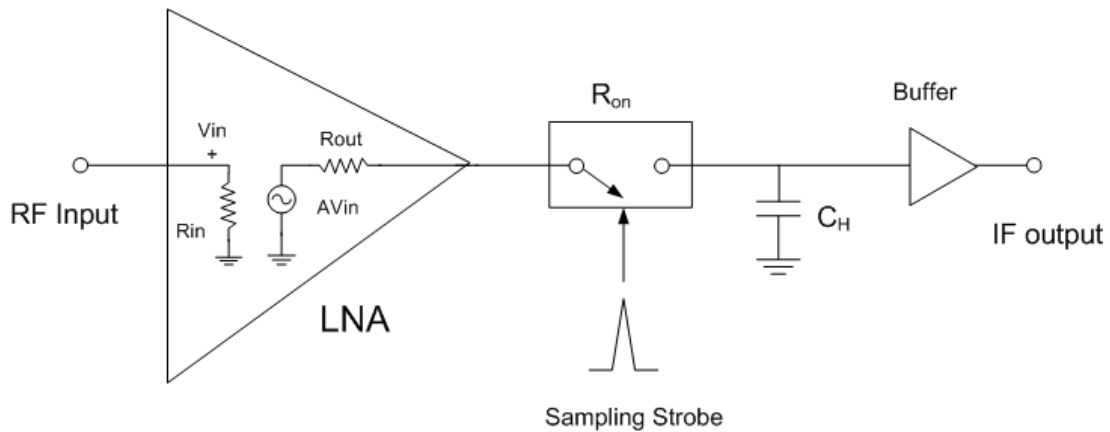
Figure 4.7 Diagram of an integrated LNA-sampling mixer. The schematic inside the LNA represents its simplified small-signal model

4.3 Integrated sampling mixer front-end architecture

Recently emerged CMOS sampling mixers usually incorporate LNA with a sampling switch, which performs the sampling for the purposes of improving noise figure and providing conversion gain [37], [38].

The principle of the integrated LNA-sampling mixer is explained in Figure 4.7. The output of the LNA is connected with a sampling switch in serial with a sample-and-hold capacitor (C_H). When a sampling strobe arrives, the switch will be turned on to allow the sample-and-hold capacitor keep track of the LNA output signal. Besides providing the 50-Ω impedance matching, the LNA also produces a voltage gain that contributes to the conversion gain and reduces the noise figure of the sampling mixer. Based on the model in Figure 4.7, we can derive the equivalent circuit model for noise calculation as shown in Figure 4.8. Two noise sources need to be taking into account
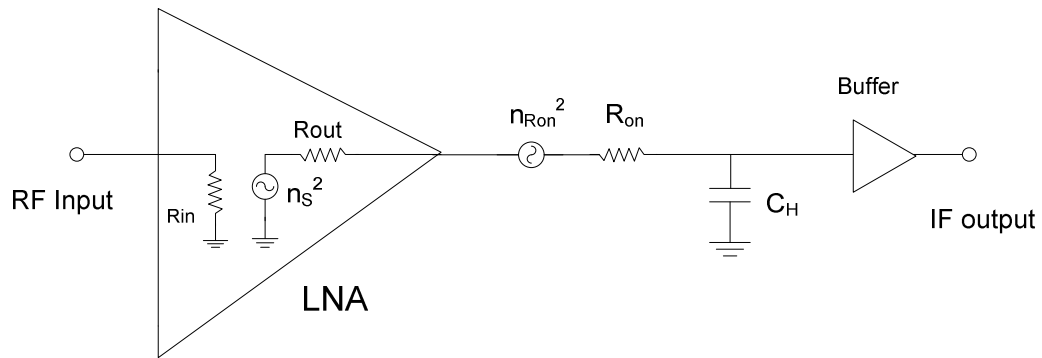
Figure 4.8 Equivalent circuit for calculating sampling mixer output noise

during the calculation, one is n_s which represents the output noise of the LNA, the other is n_{Ron} which is caused by thermal noise of switch-on resistant R_{on}. It can be easily calculated that

$$n_s^{\ 2} = n_i^{\ 2} FG \tag{4-8}$$

where n_i^2 is the input noise density due to input source impedance. F and G are the noise figure and gain of the LNA, respectively.

$$n_{Ron}^{\ 2} = 4KTR_{on} \tag{4-9}$$

where K is the Boltzmann constant, T is the temperature in Kelvin, R_{on} is the switch-on resistance of the sampling switch. In the R-C based equivalent circuit of Fig. 4.8, the equivalent noise bandwidth is

$$\Delta f = \int_0^\infty \left| H(j\omega) \right|^2 df = \int_0^\infty \left| \frac{1/j\omega C_H}{1/j\omega C_H + R_{on} + R_{out}} \right|^2 df = \frac{1}{4(R_{on} + R_{out})C_H} \tag{4-10}$$

If including the sampling clock jitter caused noise in (4-7) , the total out noise can be approximately calculated as

$$\bar{N}_o{}^2 = (n_s{}^2 + n_{Ron}{}^2)\Delta f + 2(\pi f A \Delta t)^2$$

$$= \frac{n_i{}^2 FG + 4KTR_{on}}{4C_H(R_{on} + R_{out})} + 2(\pi f A \Delta t)^2 \tag{4-11}$$

The total noise figure of the integrated LNA-sampling mixer can hence be derived as

$$F_{total} = \frac{n_o{}^2}{Gn_i{}^2} = \frac{\bar{N}_o{}^2}{Gn_i{}^2}\frac{2}{f_s}$$

$$= [\frac{F}{4C_H(R_{on} + R_{out})} + \frac{4KTR_{on}}{4C_H(R_{on} + R_{out})Gn_i{}^2} + \frac{2(\pi f A \Delta t)^2}{Gn_i{}^2}]\frac{2}{f_s} \tag{4-12}$$

where *fs* is the sampling frequency. This formula is very useful for evaluating the noise figure qualitatively. In order to minimize the noise figure of the integrated sampling mixer, the LNA needs to increase the gain and maintains a low noise figure itself, hence rendering difficulty in achieving low power consumption. For UWB systems, where narrow-band pre-filtering typically implemented in narrow-band systems to remove noise, is not feasible, the noise reduction for the sampling mixer will mainly depend on the gain of the LNA. Under this circumstance, the LNA needs to maintain a certain gain over a wide frequency range and, as a result, may draw a large amount of DC current that may jeopardize the power consumption of the whole subsystem. It is noted that in the integrated LNA-sampling mixer in Figure 4.7, while samplings only occur at discrete times, the LNA runs continuously, resulting in not only RF-power inefficiency but also unnecessarily increased power consumption.

It has been concluded in section 4.1 that the narrower the sampling strobe pulse is, the higher the conversion efficiency can be achieved. Additionally, the sampling bandwidth depends on the sampling aperture time which, in turn, depends on the

sampling pulse width. A narrow sampling pulse is thus typically preferred. The duration

of CMOS-based generated impulses is usually hundreds of picoseconds while the period

of a sampling clock is at least several nano-seconds. The resultant low duty cycle of the

sampling strobes means that, during most of the time, the sampling switch is off and the

circuit is in 'hold' status during which no RF signal needs to be transmitted or amplified.

A large portion of RF power will then be wasted if the LNA is turned on all the time.

Aiming at solving this problem, we propose an integrated sampling mixer incorporating

a switching LNA using a power-efficient two-stage switching technique. The block

diagram of the proposed sampling mixer is shown in Figure 4.9. The LNA is gated

through an internal switch by a pulse produced by pulse generator 1, which should be

wide enough to allow the LNA to start and reach stabilization. Pulse generator 2

generates a narrower sub-nanosecond impulse to conduct fast sampling after the LNA is

turned on and stabilized. The output time domain waveforms of different blocks in the
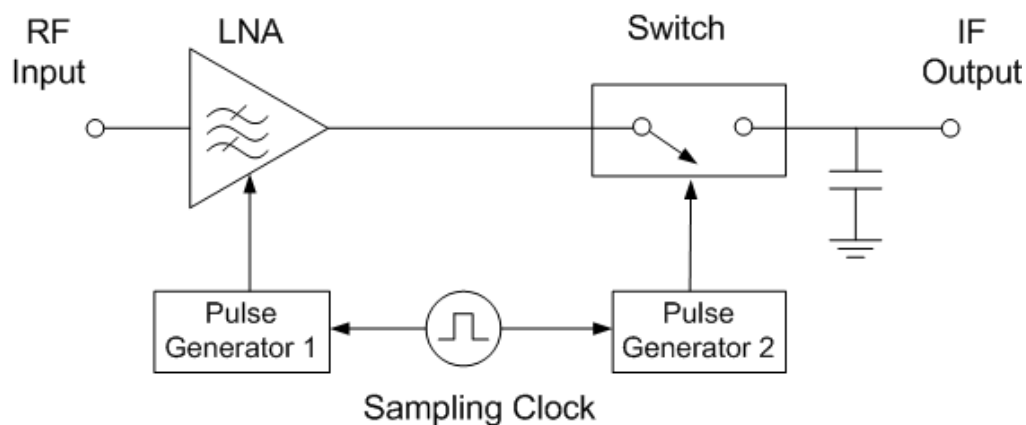
Figure 4.9 Block diagram of the integrated sampling mixer subsystem integrating a double-stage switching sampling mixer with a switching LNA
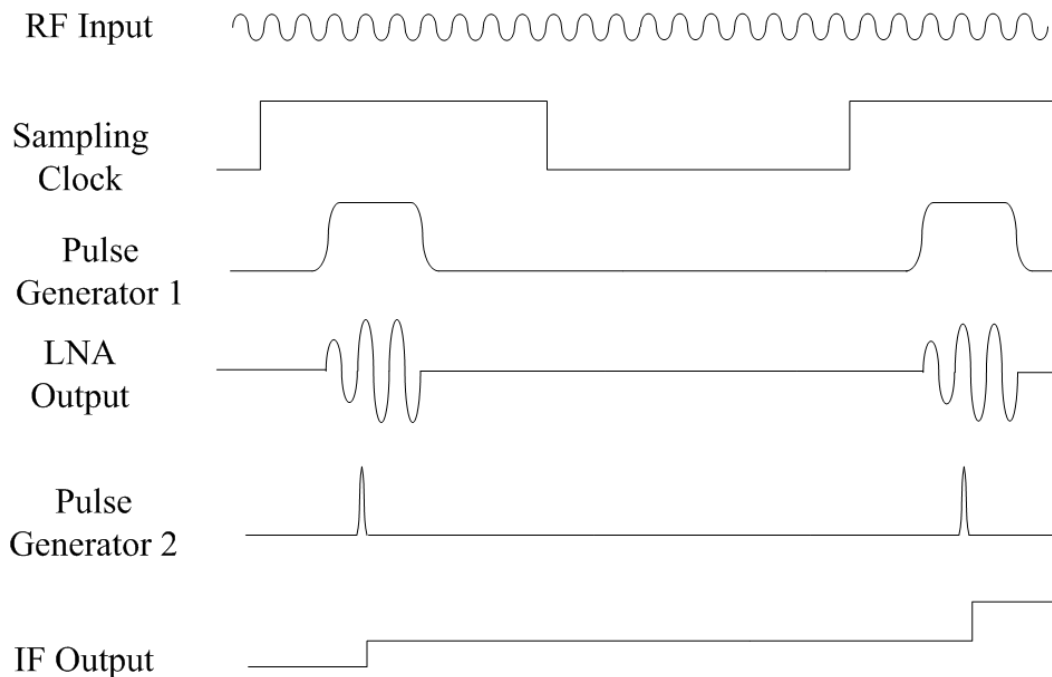
Figure 4.10 Waveforms of the building blocks in the proposed integrated sampling mixer subsystem

integrated sampling mixer are illustrated in Figure 4.10.

It is noted that the sampling impulse from pulse generator 2 needs to fall behind the rising edge of the LNA's switching signal from pulse generator 1 to accommodate possible slow switching time of the LNA. The synchronization of the two pulse generators is realized by using a common sampling clock. Assuming a 100-MHz sampling frequency is used and pulse generator 1 has a pulse duration of 2 ns, then the LNA is only turned on during 20% of the time. In other words, 80% of the power can be saved by switching LNA. If lower sampling frequencies were used then even more power can be saved.

4.4 Switching LNA design

A resistive feedback push-pull structure was chosen for the wideband LNA circuit. Figure 4.11 shows the schematic of the CMOS switching LNA as part of the sampling mixer. Transistor pair M1 and M2 forms a push-pull configuration to provide a large transconductance gm. Serial feedback resistor R_f is utilized to achieve broadband gain. Transistor M3, controlled by the pulse signal generated by pulse generator 1,
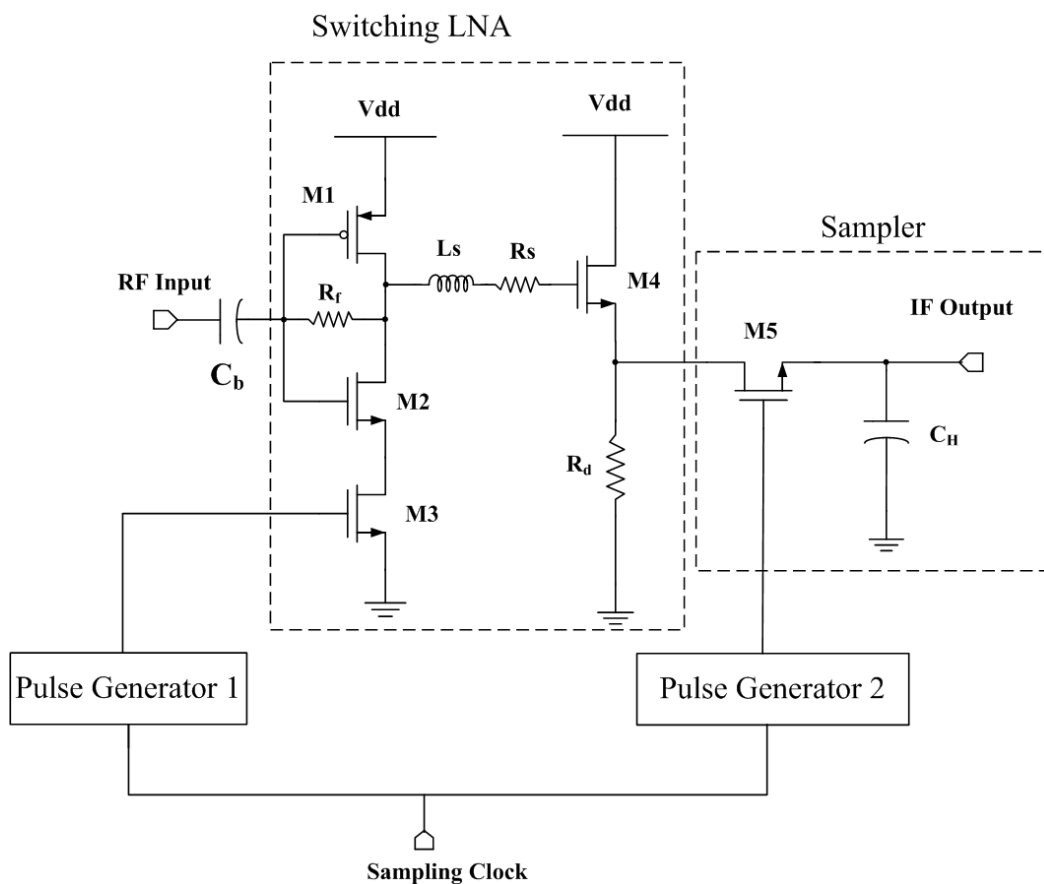
Figure 4.11 Schematic of the integrated sampling mixer subsystem. The pulse generators' schematics are shown in Fig. 9

functions as a switch to turn on and off the DC current of the first LNA stage. The DC-switch M3 is placed as close to the ground as possible to ensure its source terminal is at a low DC biasing point. Therefore, with a fixed turn-on gate voltage, the voltage (Vgs) that determines the switching-on resistance would have enough swing as close as possible to, yet always smaller than, Vdd to turn on the DC path. This also makes the single-ended LNA structure implemented in our approach preferred than a differential LNA for better switching performance. The differential LNA might require the amplitude of the switching signals exceeding Vdd as described in [37]. Transistor M5 is the sampling switch and controlled by the sampling strobe from pulse generator 2. The small-signal equivalent circuits of the switching LNA with M3 turned on are given in Figure 4.12, in which C_{gs12}, C_{gd12}, $,g_{m12}$, r_{o12}, and C_{d12} refer to the combined gate-source capacitance, gate-drain capacitance, transconductance, output resistance, and drain-ground capacitance of M1 and M2, respectively. C_{gs4}, C_{gd4} and g_{m4} stand for the C_{gs}, C_{gd} and g_m parameters of transistor M4. V_1 is the input voltage. V_{gs4} is the gate-drain voltage
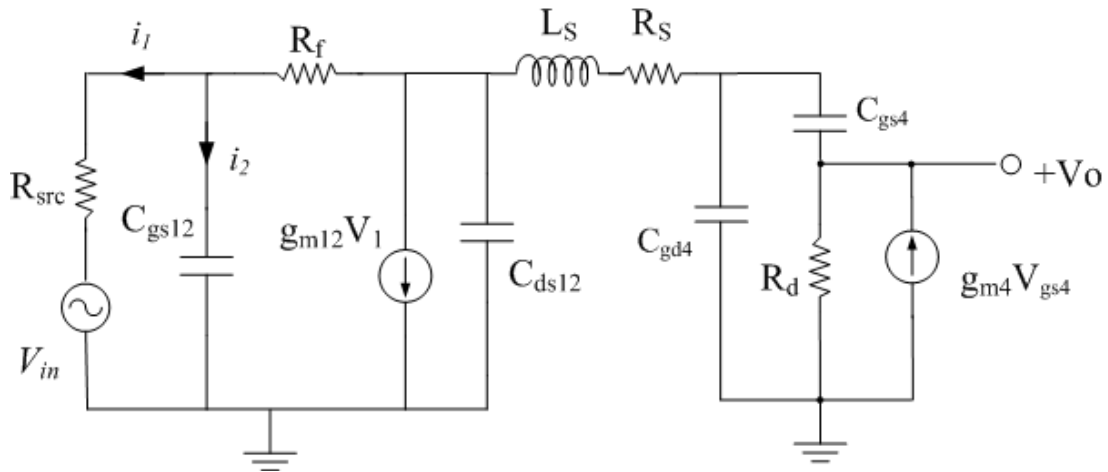
Figure 4.12 Small-signal equivalent circuit of the switching LNA with M3 turned on

across transistor M4. The input impedance of the switching LNA can be estimated as

$$Z_{in} \approx \frac{1}{g_{m12} + j\omega C_{gs12}}$$

(4-13)

where $g_{m12} = g_{m1}+g_{m1}$ and $C_{gs12} = C_{gs1}+C_{gs2}$.

A serial peaking inductor Ls is inserted between the first stage and source

follower of the LNA to extend the bandwidth of the gain [42]. Resistor Rs is connected

in series with Ls to help to achieve a flat gain over frequencies. The use of Rs herein

allows the (internal) parasitic resistance of the inductor to be absorbed into Rs so that the

inductor can be electrically represented by its inductance only instead of with its

parasitic resistance, effectively helping relax the quality-factor requirement for inductor

Ls. Based on the small-signal equivalent circuit in Figure 4.12, the voltage-gain

expression of the LNA can be written as

$$G(j\omega) = G_1(j\omega) \cdot H_{12}(j\omega) \cdot G_2(j\omega)$$

$$\approx G_1(j\omega) \cdot \frac{1}{(j\omega)^2 L_s C_{g4} + (j\omega) R_s C_{g4} + 1} \cdot G_2(j\omega) \tag{4-14}$$

where $G_1(j\omega)$ and $G_2(j\omega)$ are the voltage gains of first and second stages, respectively, $H_{12}(j\omega)$ reflects the frequency response of LC component between first and second stage, $C_{g4}=C_{gd4}+C_{gs4}/(1+R_d g_{m4})$. This equation can be rearranged as

$$G(j\omega) = G_1(j\omega) \cdot \frac{H_0}{(j\omega)^2 + (j\omega)\xi\omega_n + \omega_n^2} \cdot G_2(j\omega) \tag{4-15}$$

in which $H_0 = \dfrac{1}{L_s C_{g4}}$, $\omega_n = \sqrt{\dfrac{1}{L_s C_{g4}}}$, and $\xi = R_s \sqrt{\dfrac{C_{g4}}{L_s}}$

Without the peaking inductor, the gain of the LNA will drop with increasing frequency due to drain-source capacitance C_{ds12} and gate-drain capacitance C_{gd4} of the transistors. Adding a serial inductor Ls between the first and second stages creates a peak to the total gain at the nature frequency ω_n. If Ls is carefully chosen so that the peak can
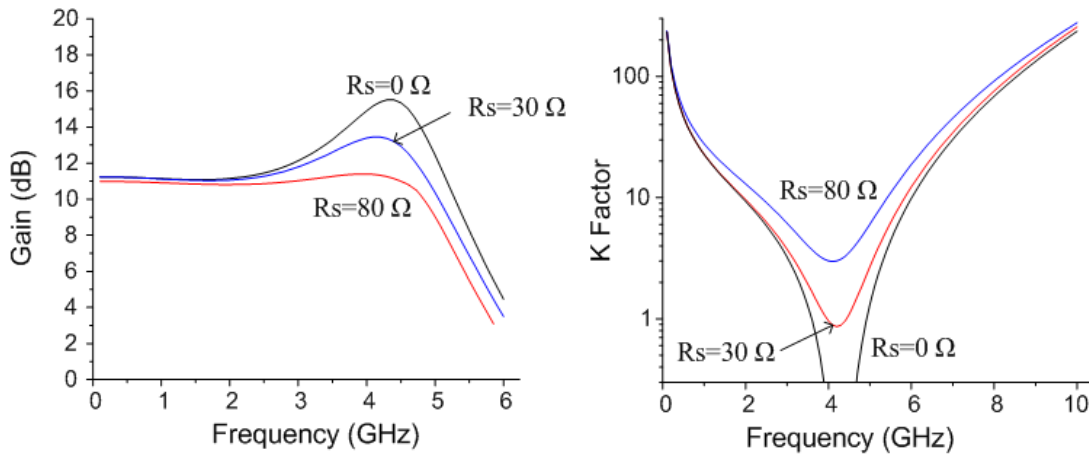
Figure 4.13 Effects of serial resistor Rs on gain (a) and stability factor K (b)
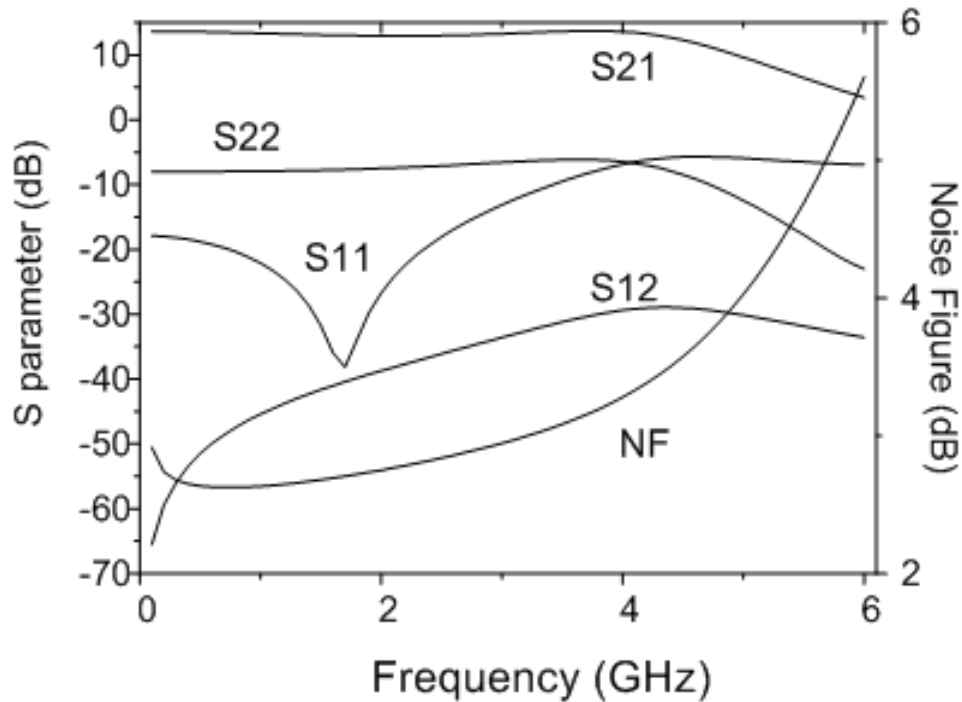
Figure 4.14 Simulated S-parameters and noise figure of the switching LNA

be used to compensate for the gain drop, then the bandwidth of the LNA can be expanded. However, the amplitude of the peak also needs to be controlled so that a flat frequency response can be obtained. Besides, a serial resistor Rs help to kill the potential negative resistance caused by un-stability of the feedback LNA. Figure 4.13 illustrates the effects of the serial resistor Rs upon the gain's frequency response and the stability factor K. It can be seen that at the nature frequency ω_n, a peak and a trough appear for the gain and K factor, respectively. As the Rs value grows, the gain becomes flatter and the K factor becomes larger at the trough. The optimal value for Rs was finally chosen as 80Ω. The simulated noise figure and S-parameters of the LNA are presented in Figure

4.14. From DC to 4 GHz, the calculated gain is 13 ± 1 dB and the input return loss is larger than 10 dB. The noise figure is below 4 dB within this frequency band.

4.5 Time domain performance of the sampling mixer

Switch M3 is turned on within the sampling window represented by a wide pulse produced by Pulse Generator 1. It can be considered as a small resistor. However this resistance of the resistor is affected by the gate source voltage, which may cause trembling gain at first stage of the LNA as explained in Figure 4.15 (a). Therefore it is necessary to investigate the prorogation of ripple from sampling clock to output of LNA first stage. A transient simulation was conducted with zero RF input. The simulated

(a)   (b)
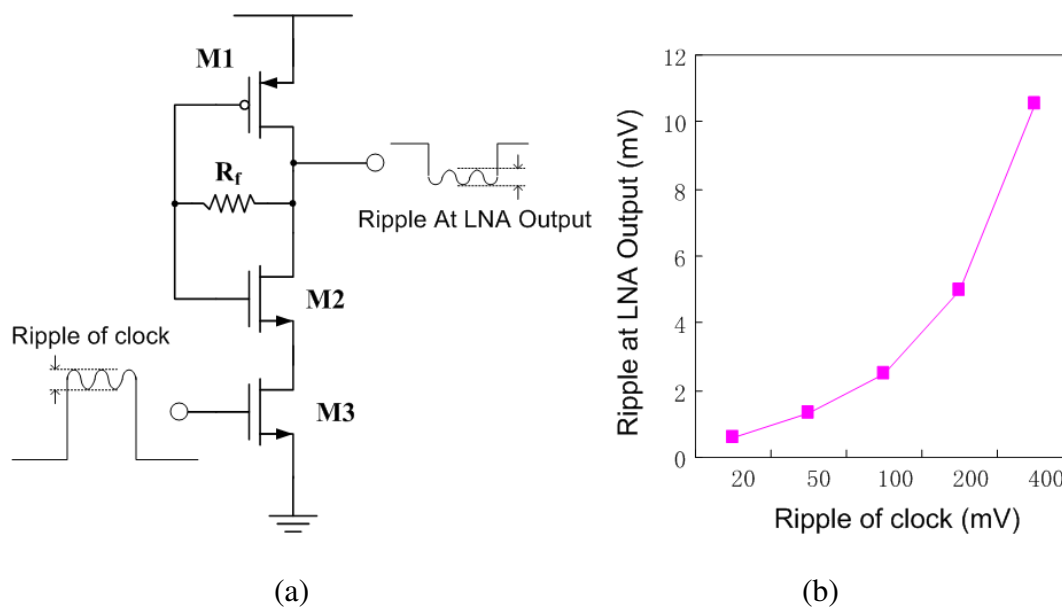
Figure 4.15 (a) The effect of sampling clock ripple and (b) simulated coupling results

output ripple amplitude is given by Figure 4.15 (b). From the simulation, the effect of sampling clock trembling can be omitted as long as its amplitude is kept below 50mV. Further ripple compression can be achieved by increasing the size of the M3, which make the switch more close to short circuit when turned on.

The pulse generators 1 and 2 included in Figure 4.9 and Figure 4.11 use digital NAND gate mentioned in Chapter III to generate pulses [22]. These pulse generators can provide large voltage swings required for turning on and off the switches. They contain inverter chains for delay cells and edge-sharpening purpose, which inadvertently introduce more jitter that can contaminate the input sampling clock [43]. The thermal current noise in the inverter will be causing random position change on the crossing
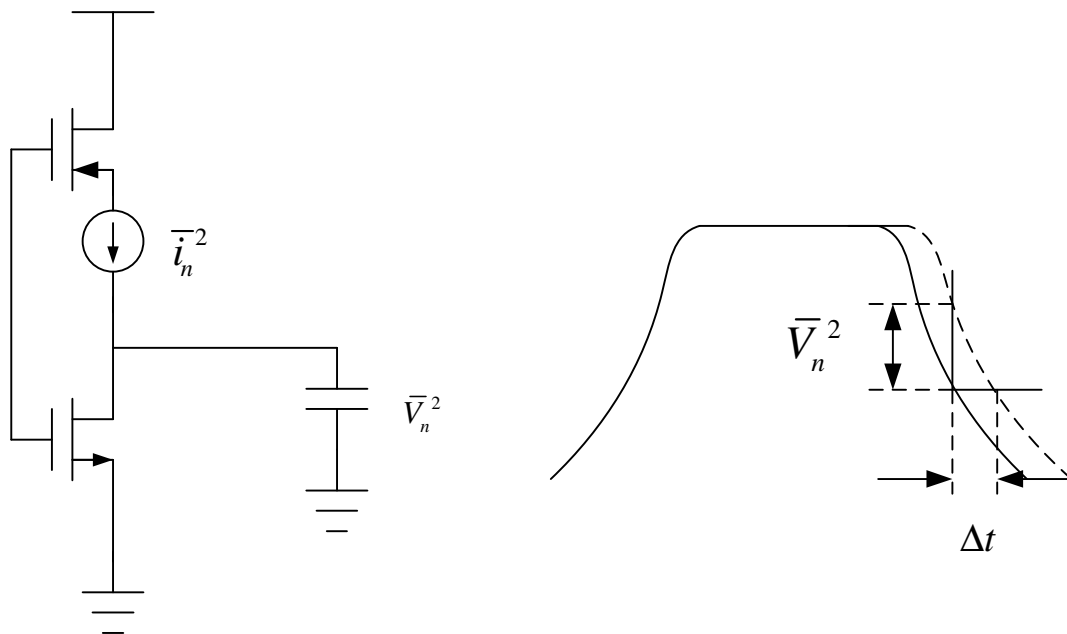
Figure 4.16 The transformation from thermal current noise to jitter

point of half Vdd as illustrated in Figure 4.16. The thermal current noise spectral density

can be modeled as:

$$\overline{i_n} = \sqrt{4kT\gamma g_m} \tag{4-16}$$

where gm is transconductance of the NMOS or PMOS transitor in the inverter.

Coefficient γ is 2/3 for long-channel devices in saturation region and typically 2 to 3

times larger for short-channel transistors. The load of inverter is the parallel

combination of load capacitance and output resistance of the inverter. Therefore

$$\overline{V_n}^2 = \int_0^\infty \overline{i_n}(r_o + 1/j\omega C_L)df = \sqrt{\frac{kT\gamma g_m r_o}{C_L}} \tag{4-17}$$

where r_o is output resistance of the NMOS or PMOS transistor in the inverter, C_L is load

capacitance of the inverter. If the rising and falling edge is linear, e.g. the slope is

constant value, the jitter can be estimated using

$$\Delta t_i = \frac{\overline{V_n}}{SR} = \frac{\overline{V_n}}{I_D / C_L} = \frac{\sqrt{kT\gamma g_m r_o C_L}}{I_D} \tag{4-18}$$

where I_D is drain current of the inverter and SR is the slew rate of the charging procedure.

Assuming the jitter of each inverter stage is independent from each other, the

total jitter for a N-stage inverter chain is $(\Delta t)^2 = N(\Delta t_i)^2$. The calculated jitter of each

inverter stage is below 1 ps. The capacitor-loaded delay chain brings in a jitter of no

more than a few ps. The total introduced jitter of the pulse generator is estimated to be

less than 20 ps based on its circuit topology and component parameters. In order to

investigate the effects of clock jitter on the sampling bandwidth, time domain simulation

was conducted for a basic sampler, consisting of a NMOS switch and a sample-and-hold

capacitor, with a jittered sampling clock. The rising/falling edge of the sampling strobe is set to 100 ps, which is roughly the same as that in the designed pulse generator. Figure 4.17 shows the basic sampler and its simulated conversion gain with different sampling clock jitters. According to Figure 4.17, a 3-dB sampling bandwidth of over 5.5 GHz can be obtained with a clock jitter smaller than 20 ps, which is large enough to cover the entire bandwidth of the designed switching LNA.

Figure 4.18 shows the output transient response of the first stage of the LNA, indicating that the LNA needs roughly 2 ns to reach stabilization after switch M3 is turned on. Therefore, the sampling strobe from pulse generator 2 should appear at least 2 ns after the rising edge of the pulse coming from pulse generator 1. Figure 4.19 plots the

(a)   (b)
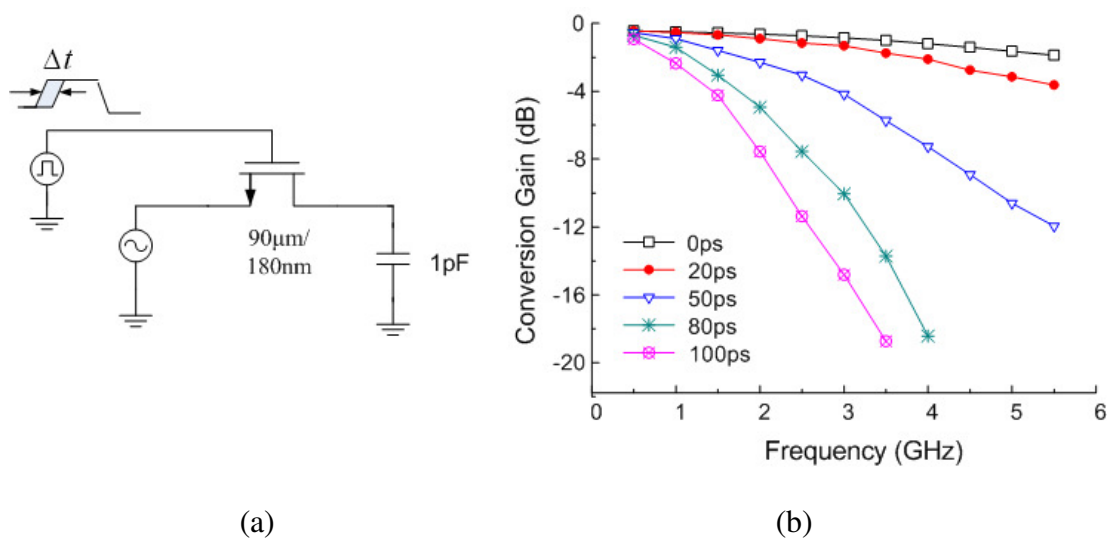
Figure 4.17 A basic sampler with a jittered clock (a) and the clock jitter's effects on the sampler's conversion gain (b). The NMOS has a width of 90 μm and a length of 0.18 μm
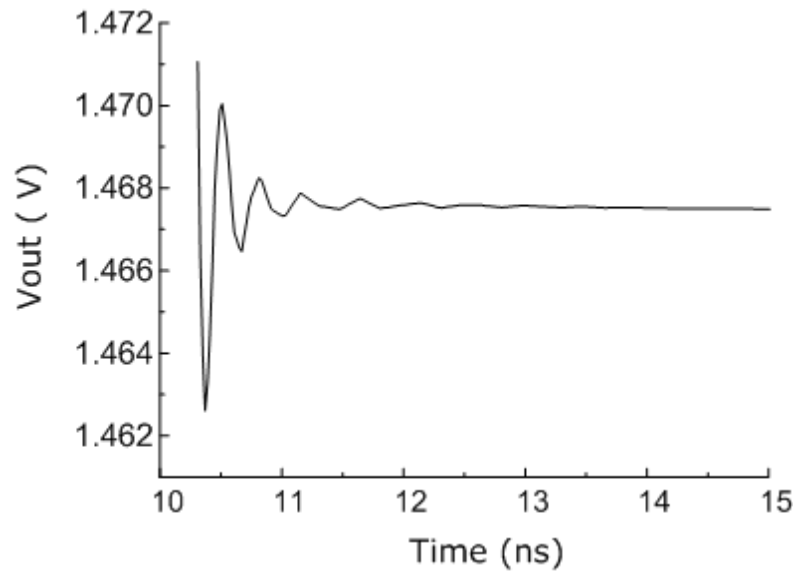
Figure 4.18 Transient response of the output of the switching LNA's first stage

simulated time domain waveforms of different building blocks in the integrated sampling mixer. During hold status, the drain current of switch M3 is kept at 5.6 μA and the LNA doesn't produce any RF output. Before sampling occurs, the gating signal produced by pulse generator 1 will arrive and turn on the LNA. As a result, the drain current of switch M3 jumps to 8.3 mA. After the LNA starts up and stabilizes, the sampling strobe coming from pulse generator 2 will reach M5 and conduct the sampling. This sampling strobe has rising/falling edges of 80 ps and is 2 ns behind the gating signal coming from pulse generator 1. The duration of the pulse produced by pulse generator 1 is 3.5 ns, which limits the sampling frequency to below 200 MHz. For sampling frequency higher than 200 MHz, the duration of this pulse and the delay between it and that from pulse generator 2 will be different from the designed values of 3.5 ns and 2 ns, respectively.
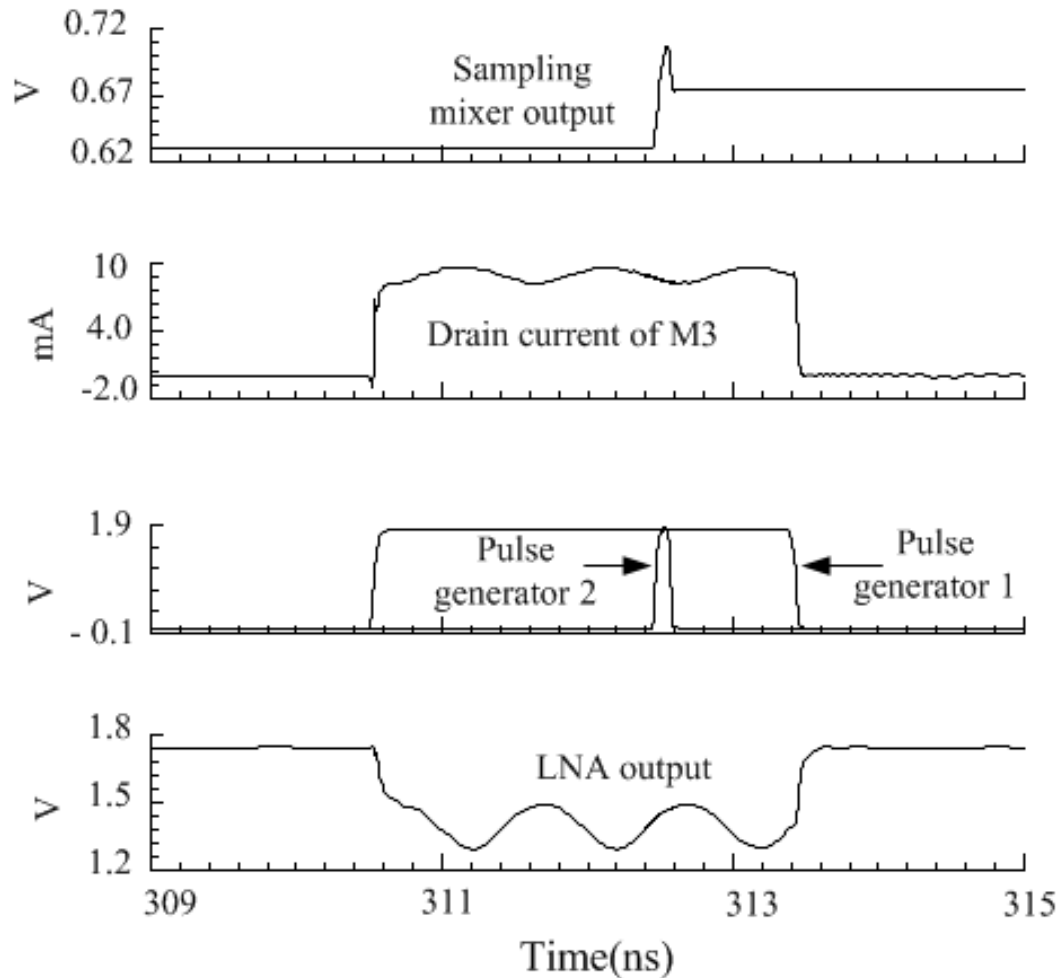
Figure 4.19 Time domain waveforms of different building blocks in the integrated sampling mixer subsystem

Figure 4.20 and Figure 4.21 give the output spectrum and time domain waveform of the integrated sampling mixer subsystem with 505-MHz RF signal and 100-MHz sampling clock. The peak to peak swing of input RF signal is about 20mV. The observed IF swing is more than 100mv from waveform seen in Fig. 4.21. On the spectrum, besides the down-converted signal at 5 MHz, spurs appear at every harmonic of 5 MHz. The

ratio between the down-converted signal to the largest harmonic signal is larger than 20 dBc.
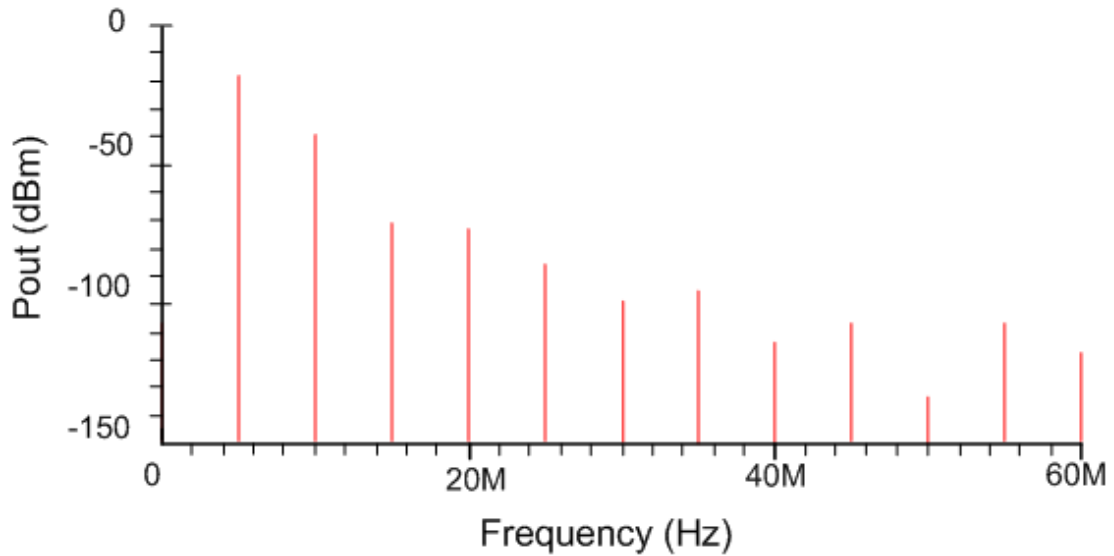
Figure 4.20 Output spectrum of the integrated sampling mixer subsystem
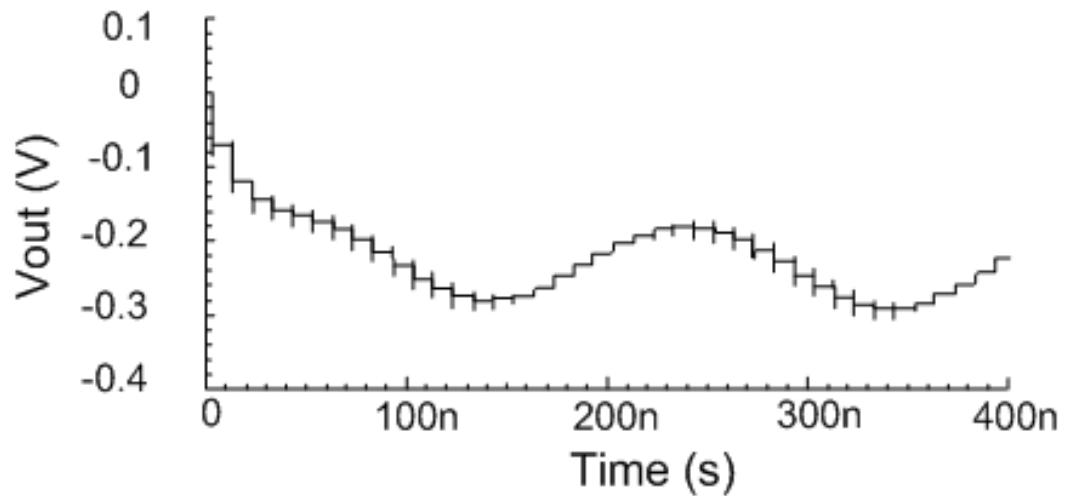
Figure 4.21 Output waveform of the integrated sampling mixer subsystem

4.6 Measurement results

The integrated sampling mixer was implemented on the Jazz 0.18-μm enhanced RF CMOS process [44]. The entire sampling mixer chip, including the switching LNA, pulse generators, sampler, RF pads and output buffer, occupies a die area of 750 μm × 730 μm and is shown in Figure 4.22.

On-wafer measurement was conducted for the fabricated integrated sampling mixer. The input return loss is measured by vector network analyzer through on-wafer probing. The setup for measuring conversion gain is explained in Figure 4.23. Two frequency synthesizers were used during the measurement. One provides large amplitude sampling clock, the other function as a RF signal source with relatively small
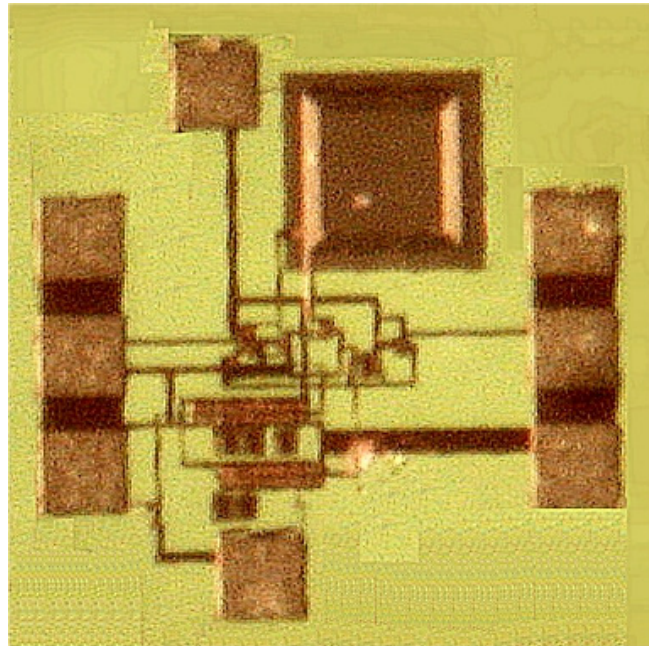
Figure 4.22 Die microphoto of the integrated sampling mixer subsystem
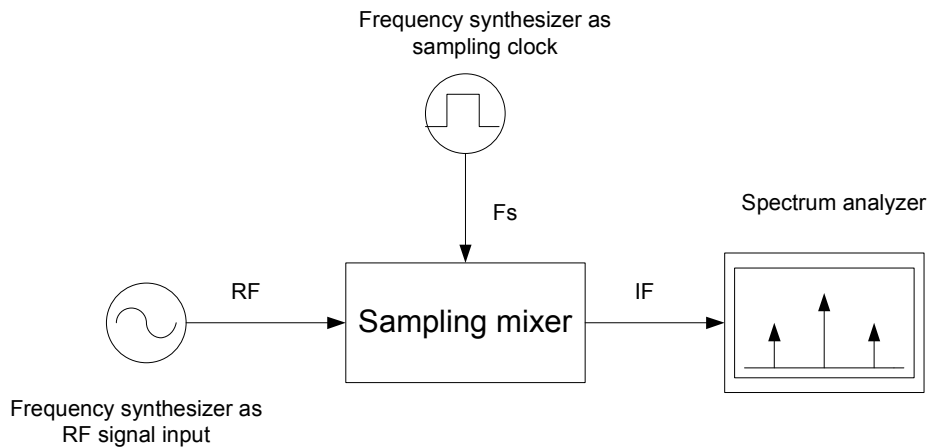
Figure 4.23 The setup for measuring conversion gain of the sampling mixer

output power. Figure 4.24(a) shows its measured input return loss. Figure 4.24(b) gives

the measured conversion gain with 100-MHz and 10MHz sampling frequency

respectively. The measured input return loss is below –10 dB up to 3.8 GHz. The voltage

conversion gain ranges from 9-12 dB across DC-3.5 GHz when using 100MHz sampling

frequency. When the sampling frequency drops to 10MHz, the conversion gain

bandwidth also drops significantly. This is due to larger jitter at 10MHz. It is noted that

the output buffer has a calculated loss of 5 dB. This buffer is used to drive a 50-Ω load

for measurement purposes only and is not needed in complete receiver integration.

Therefore, 5 dB was added to the measured power conversion gain to obtain the actual

voltage conversion gain of the sampling mixer (without buffer) as shown in Figure

4.24(b). It is worth noticing that the measured conversion gain drops faster than the

power gain shown in Figure 4.14 as frequency increases. This is mainly due to the jitter

from the function generator employed as the clock. Figure 4.25 shows that the measured
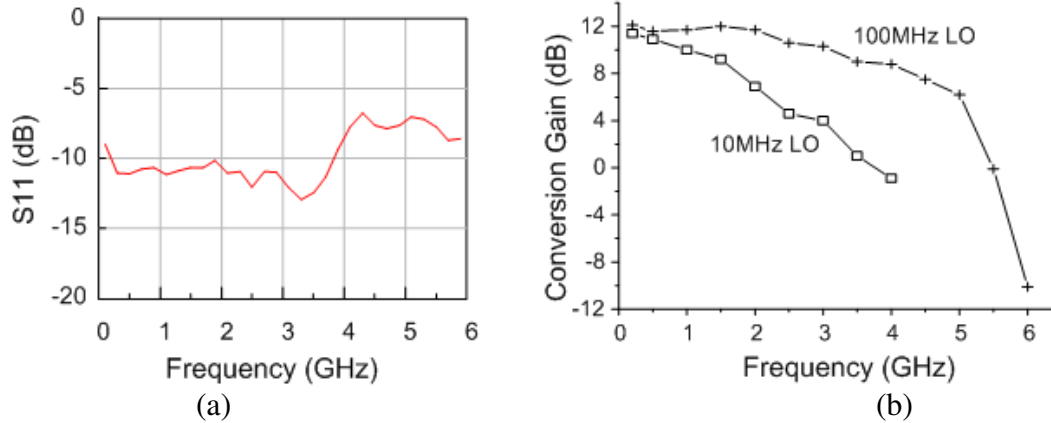
Figure 4.24 Measured input return loss (a) and conversion gain (b) of the integrated sampling mixer subsystem

input 1-dB compression point is around –11 dBm with sampling and RF frequencies of 100 and 500.2 MHz, respectively. As the gain of the switching LNA drops with increasing frequency, the 1-dB compression point will increase.

The noise figure measurement setup is similar to that in Figure 4.23. The procedure is based on the ratio of input SNR and output SNR. Figure 4.26 shows the measured noise figure with 100 MHz and 10 MHz sampling frequency. During the measurement, the output noise floor was recorded with the existence of –20-dBm RF input signal so that the sampling error could be included. As the RF frequency increases, the elevation of the output noise floor can be observed. This agrees with the fact that the sampling error rises with frequency due to clock jitter [40]. Using the 100-MHz clock, the noise figure of the integrated sampling mixer lies between 15 and 25 dB from DC to 3.5 GHz.

The measured power consumption indicates that the integrated sampling mixer including the switching LNA, two pulse generators, sampler, and output buffer
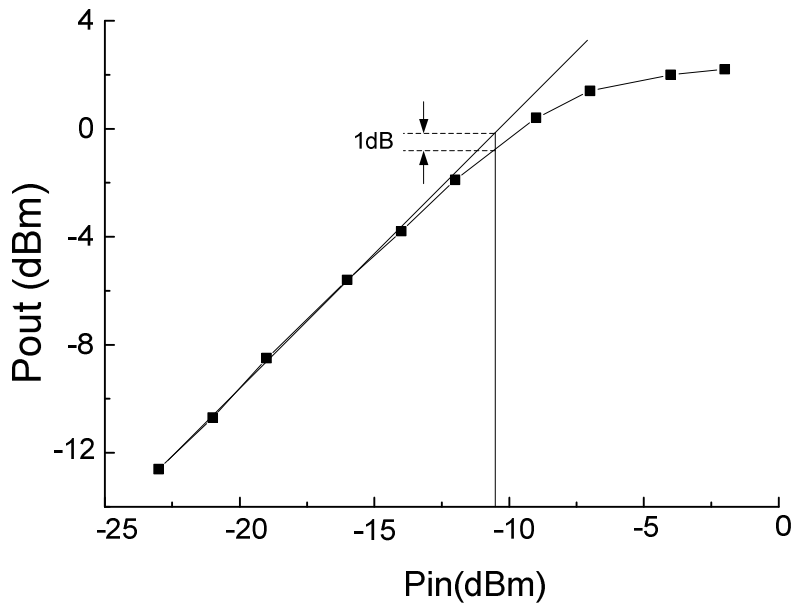
Figure 4.25 Measured 1-dB compression point of the integrated sampling mixer subsystem with 100-MHz sampling clock and 500-MHz RF frequency

consumes 12-mA DC current under a 1.8-V supply voltage and 100MHz LO. The output buffer draws around 5.5-mA DC current. As indicated earlier, this buffer is used solely for measurement purpose. If this sampling mixer was integrated into a receiver, where a buffer is not needed, then the 5.5-mA output buffer current can be saved, thus leading to even lower power consumption. It is noted that if only one switching stage was used (i.e, using only pulse generator 2), the integrated sampling mixer would draw an additional 8-mA DC current due to the LNA being on all the time. The current consumption of the sampling will increase as LO frequency increase due to more and more "turn on" time of LNA. The measured dc current is displayed in Figure 4.27. Table 4.1compares the performance between this integrated sampling mixer and those previously published, which demonstrates unprecedented performance achieved by this mixer. Some of the

listed conversion gains are increased by the amount equal to the associated buffer loss to allow a meaningful comparison.
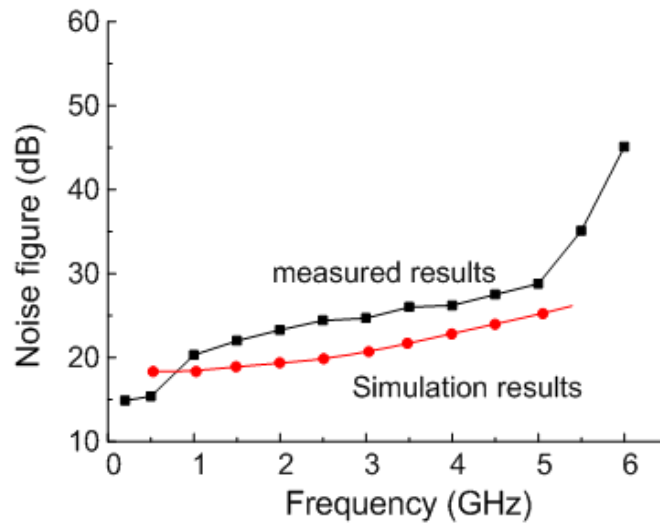
Figure 4.26 Measured and simulated noise figure of the integrated sampling mixer subsystem
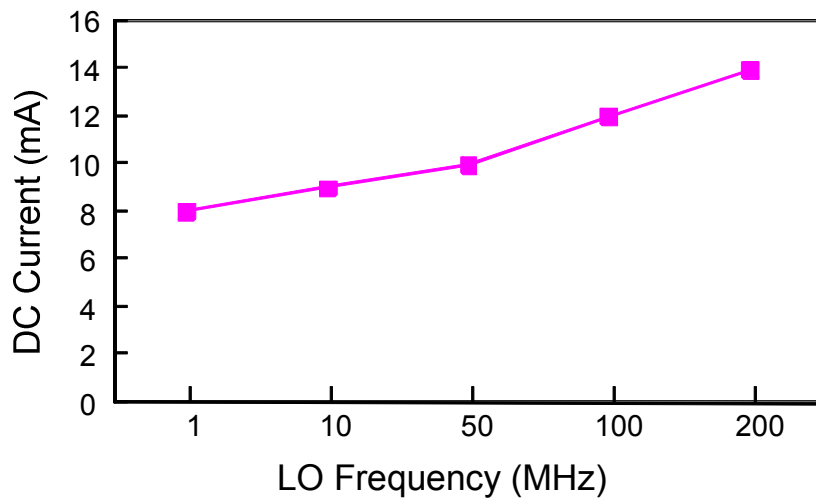
Figure 4.27 Current consumption of sampling mixer as LO frequency change

Table 4.1 Performance comparison of published sampling mixers

Reference	Technology	Frequency	Conversion gain	Noise figure	Sampling frequency	Power
[2]	0.6-µm CMOS	900-MHz/1.8 GHz	-7 dB*/-16 dB*	38 dB/47 dB	50 MHz	N/A
[3]	0.35-µm CMOS	1.6 GHz	-8 dB*	25 dB	1.55 GHz	43 mW
[4]	0.18-µm CMOS	2.4 GHz	7.6 dB**	21.8 dB	100 MHz	95 mW
[10]	0.6-µm GaAs MMIC	DC - 2 GHz DC-1.6 GHz	0-3 dB** -1-2 dB**	23 dB*** 29 dB***	500 MHz 100 MHz	125 mW
This work	0.18-µm CMOS	DC - 3.5 GHz	9 - 12 dB**	15 - 25dB	100 MHz	21.6 mW

* no information on buffer   ** adjusted to compensate for buffer loss   ***   no information on noise figure variation

CHAPTER V

UWB ACCURATE DELAY GENERATOR

.   As we have indicated in the previous sessions, UWB technology is unique on

conducting signal processing in time domain. As the key component which determines

the timing control accuracy, delay generator needs to be carefully designed. Pulse

duration control, accurate placement of pulse position and template signal

synchronization in UWB coherent receiver all rely on high precision delay generator

module. Timing stability is an important issue for time domain based UWB system just

like frequency stability is crucial for narrow band system. Timing error generated by

circuit will degrade system performance and cause interference to other existing radio

systems. Analog based delay unit, such as R-C delay cell can only deal with narrow band

signal. Therefore leading generated UWB pulse through delay cell and keeping a
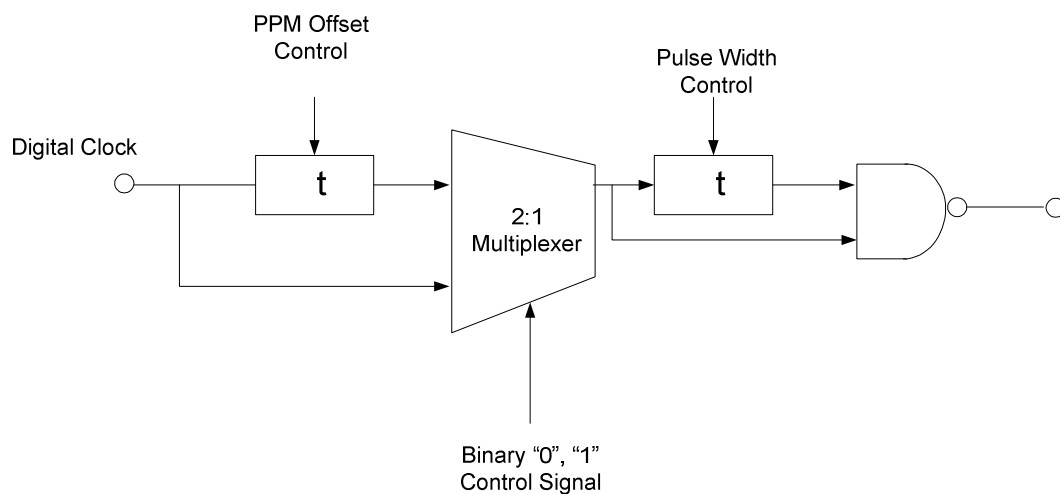
Figure 5.1 The diagram of a PPM based transmitter using delay generator

Input
clock

2τ

Monocycle Pulse
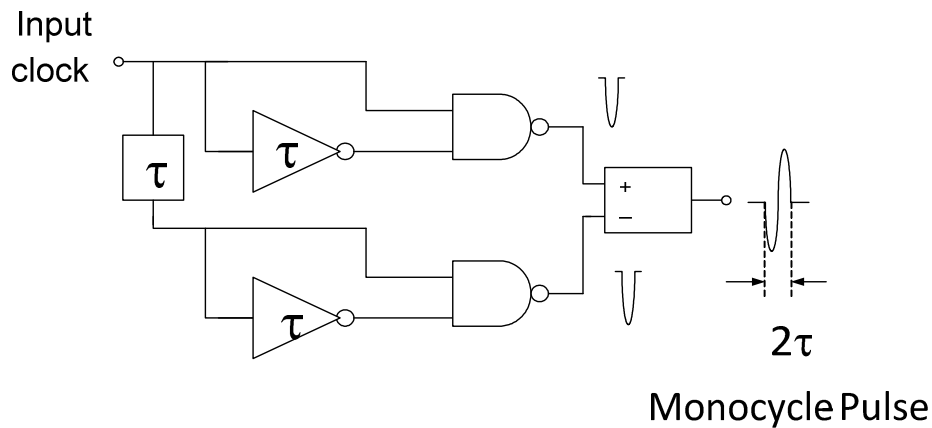
Figure 5.2 Generation of mono-pulse signal using delay generator

constant delay for all the frequency components of the signal is extremely difficult. One

solution is to adjust the delay of the digital clock that drives the pulse generator. Figure

5.1 shows a binary PPM UWB transmitter in which two adjustable delay units control

the PPM offset and pulse duration. The modulation of pulse can be easily implemented

by a 2:1 multiplexer which determines whether the digital clock needs to be shifted from

normal position or not. A mono-pulse can also be generated through delay generator and

logical gate as demonstrated in Figure 5.2. One of the most widely used active delay

circuits for digital clock is inverter chain. However the propagation delay of inverter is

subject to various factors such as process, voltage supply and temperature (PVT)

variations. Delay generator circuits based on high speed digital counter has been

published recently [45]. The simplified system diagram is shown in Figure 5.3. The

VCO controlled by a phase-locked loop (PLL) runs at approximately 2.5 GHz with a 10

MHz reference. Each cycle of the 2.5 GHz VCO advances the 8-bit synchronous counter
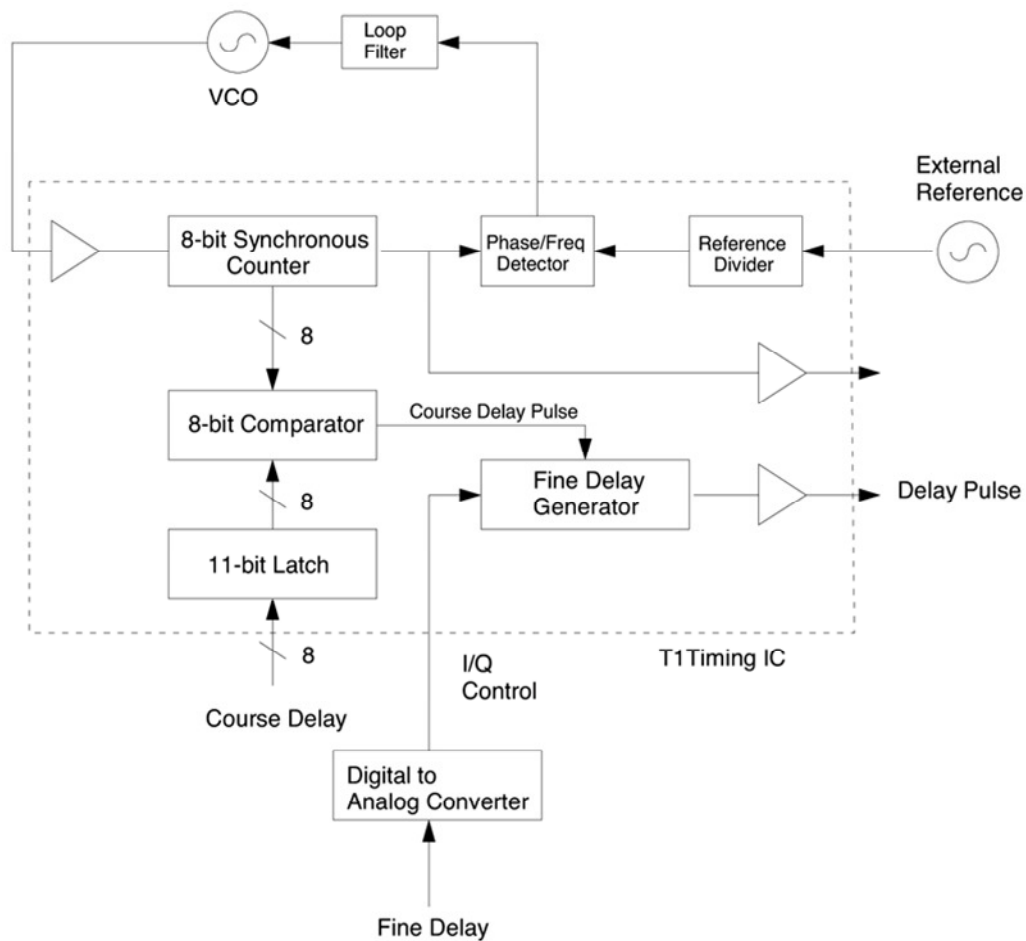
Figure 5.3 Block diagram of digital counter based delay generator in [45]

one count. Each count represents a 400 *ps* time advance. The value loaded into the

comparator determines the number of 400 *ps* steps that can occur before the output of a

course delay pulse. The value loaded into the comparator can be changed dynamically so

that the interval between output pulses can be controlled. The fine delay tuning unit

conducts phase shift to achieve even smaller time step. Although capable of providing

small delay step with decent jitter performance, this delay generator needs to include a

2.5GHz RF oscillator which draw significant amount of DC current and occupy a large

chip area. Also this timing circuit cannot take a digital clock as input and provide a delayed clock at the output. The requirement for a programmable, low power and PVT variation independent delay generator is indispensable in pulse based UWB systems.

5.1 Delay locked loop based delay generator (DLL)

Delay locked loop (DLL) has been widely used in clock generation and frequency generation circuits to provide multi-phase clock signal and accurate frequency regardless of PVT variations [46]. A simplified block diagram of a conventional DLL is outlined in Figure 5.4. A typical DLL includes a voltage controlled delay line (VCDL), a phase detector (PD), a charge pump (CP) and a loop filter (LF). Under locking condition the propagation delay through VCDL equals to the period of reference clock. When PVT condition changes, the resulting VCDL delay will vary as well. Phase detector detects the delay change and lead control voltage of VCDL adjust the delay against PVT
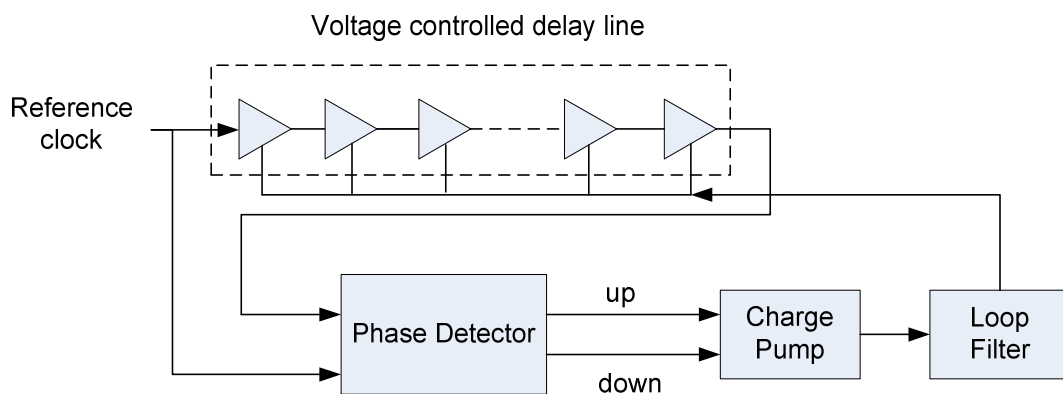
Figure 5.4 Block diagram of a delay locked loop

variation through the loop. This allows each delay cell generate a constant delay value T_{ref}/N, where T_{ref} is the period of reference clock and N is the number of delay cells in VCDL.

Since DLL is a loop structure, reference clock can only be 50% duty cycle periodical signal within a certain frequency range. The generated delay is also fixed corresponding to certain reference frequency. In a UWB transmitters the clock signal is not necessarily periodical due to variable bit rate and modulation scheme. In addition we prefer adjustable delay value to maximize design flexibility. To utilize the constant
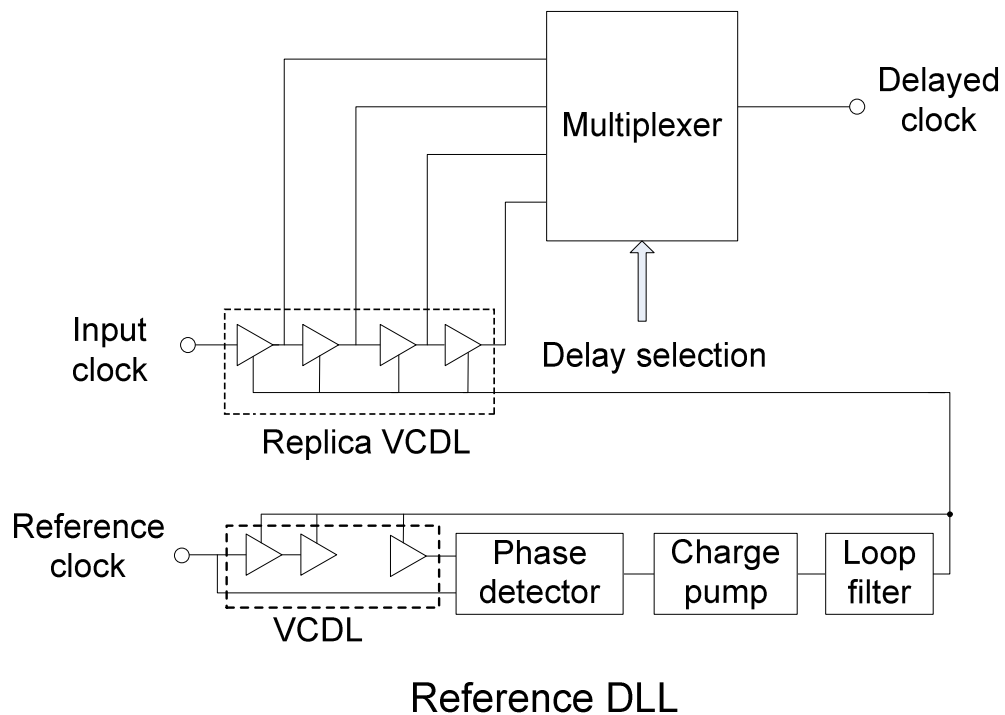
Figure 5.5 Delay generator that composed of a DLL and a replica delay line

delay property of the calibrated VCDL, an identical replica VCDL can be put in parallel in the DLL. Since these two VCDLs share the same control voltage, each delay cell in replica VCDL should also generate the propagation delay of T_{ref}/N. By choosing different branches of replica VCDL through a multiplexer different propagation delay can be manipulated. Since the phase detector only detects the rising edge of the clock the generated propagation delay is independent of duty cycle. This makes the replica delay line suitable for un-periodical clock signal as well. The resolution of the generated delay is limited by minimum delay of the delay cell. While the maximum delay value is only constrained by the number of delay cell that can be put on chip. Figure 5.5 exhibits the topology of proposed delay generator. Through this configuration the reference DLL constantly "calibrates" the duplicate VCDL through the negative feedback loop.

5.1.1 Design of delay cell

As displayed in Figure 5.6 (a) the delay cell in VCDL includes a current starving inverter and a conventional inverter. The two biasing terminals *Vcp* and *Vcn* control the delay by regulating the current flowing through the inverter. This structure is capable of delivering wide delay tuning range, which helps the system endure large PVT variation. The simulated delay tuning range is displayed in Figure 5.6(b). The delay of inverter has been proven [47] be related to input clock signal slope as well as the load capacitance in addition to transistor size. In order to ensure the delay in replica VCDL is absolutely identical to that in the DLL, the input clock slope and the load of delay cells in these two
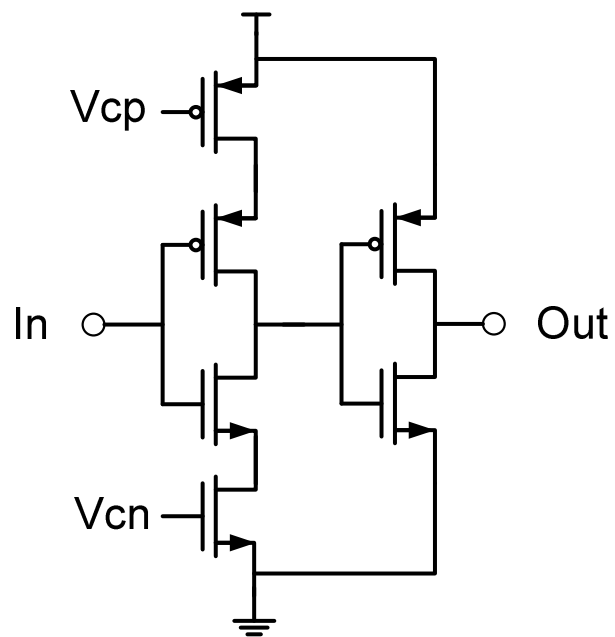
(a)
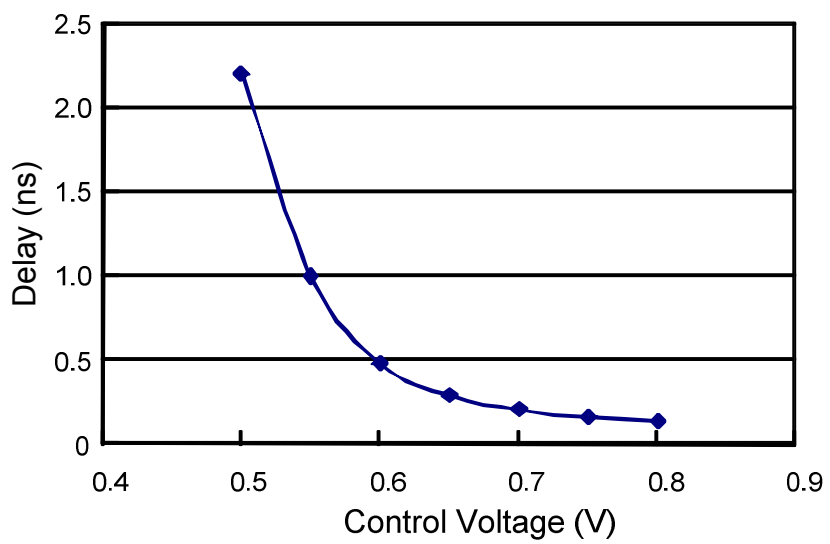
(b)

Figure 5.6 Delay cell structure in VCDL (a) and its tuning range (b)

delay lines are required to strictly resemble each other.

The input clock signal of replica delay line could have different slope of rising edge comparing with reference clock, rendering the delay difference in replica delay line and DLL delay line. Figure 5.7 shows the scenario of two clock signals with different rising times passing through a VCDL delay cell. The clock signal with 0,5*ns* rising time produces 269 *ps* delay. While the one with 1.5 *ns* rising time has 302 *ps* delay. To equalize the rising edge of both input clock and reference clock in our proposed delay generator, a series of delay cell can be used as slope sharpening stage. According to [48] for slow-input transition, the unified output ramping duration, e.g. clock rising time of an inverter can be expressed as

$$\tau_{out} = 2t_{HLS} \cdot \frac{(1-v_{TN})}{(0.5+\dfrac{t_{HL}}{\tau_{in}}-v_{TN})} \tag{5-1}$$

where t_{HLS} is the delay of inverter when input is an ideal step function (high to low). v_{TN} refers to the threshold voltage of NMOS in the inverter. τ_{in} is the rising/falling time of the input clock. While t_{HL} represents the actual delay time of this inverter, which can be estimated:

$$t_{HL} \approx [v_{TN}\frac{\tau_{in}}{2}+(1+2\frac{C_{GDP}}{C_L})t_{HLS}] \tag{5-2}$$

where C_L and C_{GDP} are the load capacitance at output of the inverter and gate drain coupling capacitance of the PMOS respectively. Plug equation (5-2) into (5-1) the relation between output and input ramp duration can be reorganized in the form of
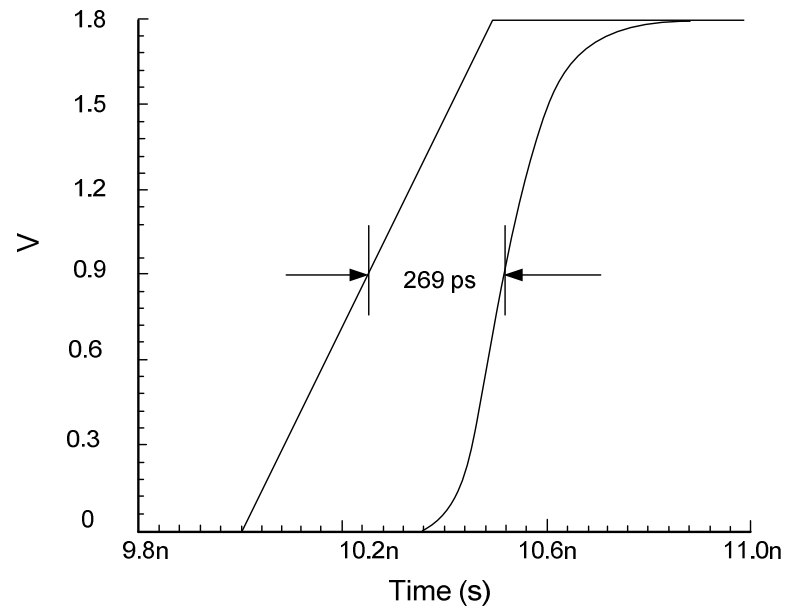
(a)
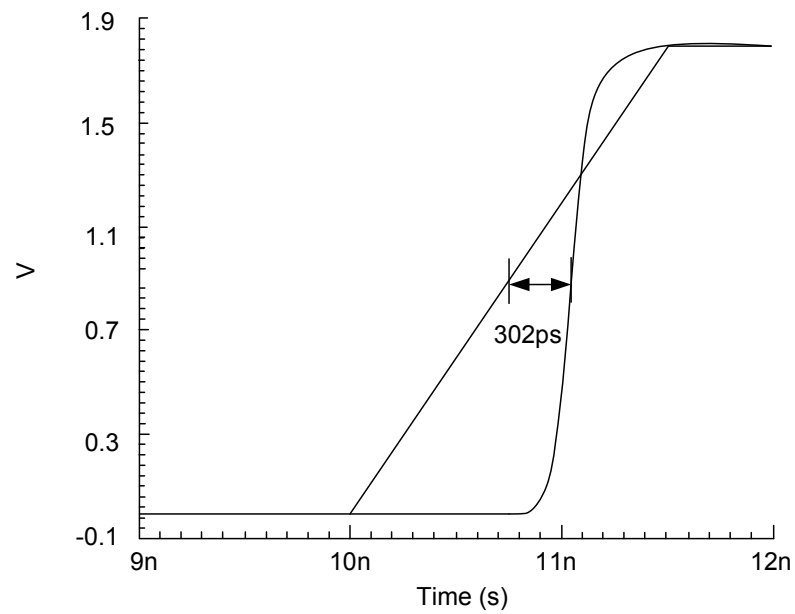
(b)

Figure 5.7 The delay generated by VCDL cell for (a) a clock signal with 0,5ns rising time and (b)a clock signal with 1.5ns rising time

$$(\frac{1}{\tau_{out}} - \frac{1}{t_f}) = k(\frac{1}{\tau_{in}} - \frac{1}{t_f}) \qquad (5\text{-}3)$$

In which k and t_f are variables independent of input clock slope. When N inverters are connected in serial the output ramp duration satisfy the equation

$$(\frac{1}{\tau_{out}} - \frac{1}{t_f}) = k^N(\frac{1}{\tau_{in}} - \frac{1}{t_f}) \qquad (5\text{-}4)$$

For slow input transition it can be proven by simulation that $|k| < 1$. Therefore τ_{out} tends to converge at t_f as the number of cascaded inverters increases. This means the inverter chain can shape the rising/falling edge of any input clock signal to a fixed slope. Although equation (5-4) assume the inverter has symmetric charging/discharging process. The conclusion still applies for practical inverters with non-ideal charging/discharging symmetry. By adding several additional delay cell stages before both DLL and replica VCDL, the slopes of reference clock and input clock can be equalized to similar shape.

Notice that the delay cells in replica delay line has an excess multiplexer input load comparing with that in DLL. This will create a loading mismatching. Besides when a specific branch of replica VCDL is selected by multiplexer the output load will be attached to this branch through transmission gate. This additional load will make delay larger than expected. To overcome this problem a complementary load is employed at multiplexer input. For minimizing loading effect purpose only single stage transmission gate should be used in the multiplexer. As shown in Figure 5.8(a) the two transmission gates conduct alternatively when the branch is selected or blocked. It helps to keep all
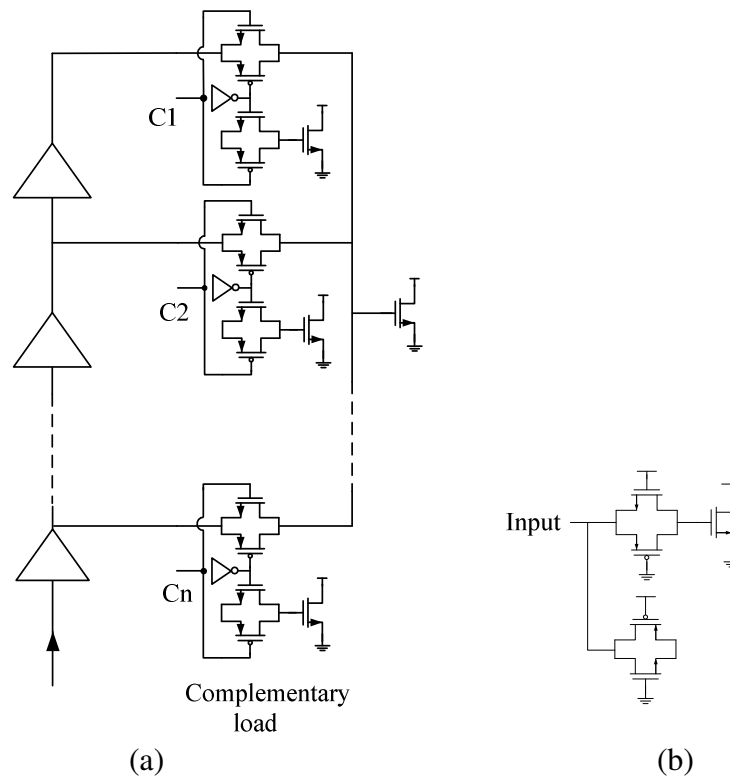
Figure 5.8 Schematic of (a) complementary load at multiplexer input and (b) dummy load for DLL delay cell

the delay cells have the same constant load despites the status of delay selection terminal Cn. The dummy loads were also added to the reference DLL delay cell to keep the loading consistent. The schematic of dummy load is shown in Figure 5.8(b).

5.1.2 The design of reference DLL core

A simplified DLL core was design and implemented as delay reference to verify the proposed delay generator. Instead of using long delay cell chain to provide delay of one clock period, the DLL uses a few delay units to realize one portion of clock period and conduct the loop feedback. Figure 5.9 shows the circuit diagram and operation

waveforms of the reference DLL. The phase detector takes two inputs ICLK and QCLK. ICLK is directly connected to reference clock, and QCLK is delayed from reference clock by a few delay cells. In the charge pump, the pull-up current I_P is tuned to be 1.5 times the pull-down current I_N. (I_P:I_N=1.5:1) When V_x is high, the charge on the filter capacitors will be decreased by $I_N \times T_{high}$, and V_{cr} will go down. On the other hand, when V_x is low, the charge will be increased by $I_p \times T_{low}$. V_{cr} will go up three times faster.

(a)

(b)

Figure 5.9 (a) Structure of reference DLL core and (b) operation waveforms of the reference DLL

When the feedback loop is locked, a stable value of V_{cr} will be obtained with the correlation of $I_p \times T_{low} = I_N \times T_{high}$. Therefore, in the locked state, XNOR output V_x has the low-to-high duration ratio of 1:1.5 ($T_{low}:T_{high}$=1:1.5) , and the rising edge of ICLK leads that of QCLK by one-fifth of clock period. For our design, 200 *ps* resolution is expected, e.g. the delay of each delay ce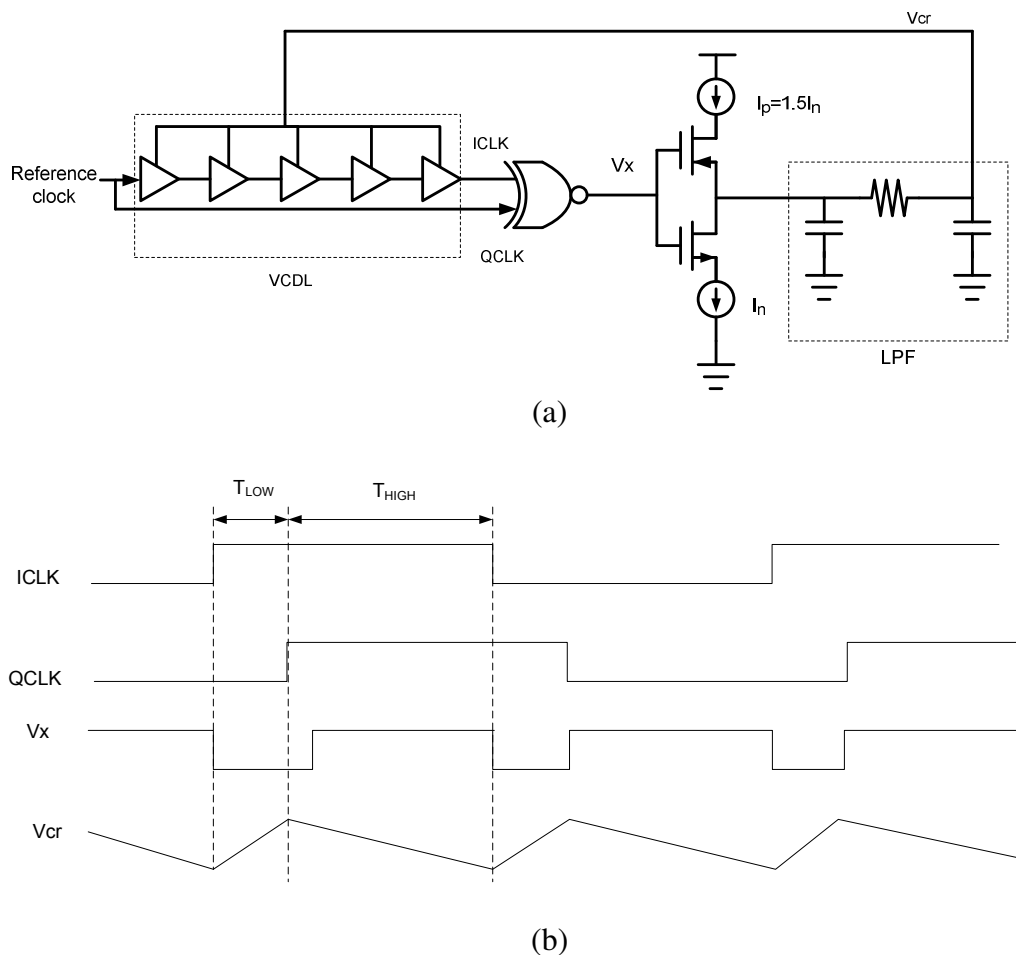ll has to be 200 *ps* at most. We choose a relatively high frequency reference clock 200MHz to reduce delay cell numbers. Five Delay cells were used to generate a 1ns delay e.g. one fifth of 200MHz clock period.

5.1.3 Simulation results

The loop lock build up procedure can be observed from the simulated time domain waveforms in DLL shown in Figure 5.10. It takes about 200ns for the loop to reach stability. The VCDL biasing control voltage have small ripple around 1.1V after the locking is built up. This is due to the alternative charging and discharging in charge pump and non-ideal loop filter as explained in Figure 5.9. In Figure 5.11 the side by side comparison between simulated waveforms of reference clock QCLK and delayed clock ICLK shows delay of 958ps, which is 42ps short of desired 1ns delay. Each delay cell has absolute delay error of 8ps. If delay of one period of clock is implemented instead of 1/5 period the delay error of each cell is expected to shrink to one-fifth as well. Time domain simulations over different process corner shows that the delay remains relatively constant as shown in Figure 5.12. The fluctuation of VCDL biasing control voltage will add around 19ps of jitter to the delayed clock, which is plotted in Figure 5.13. This can be further reduced by improving the LPF in the reference DLL at the cost of extending the loop lock build up time.
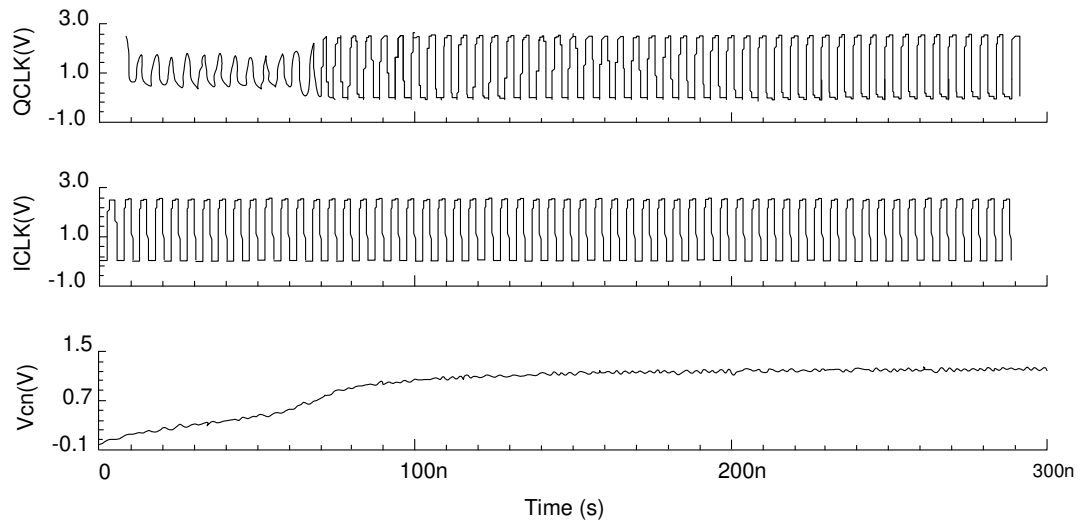
Figure 5.10 Simulated waveform in reference DLL core
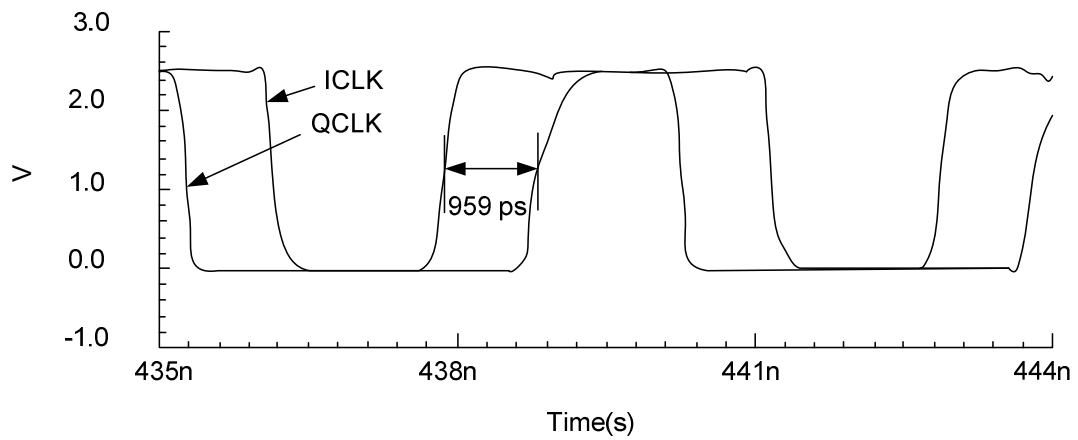
Figure 5.11 Waveform comparison between reference clock and delay clock
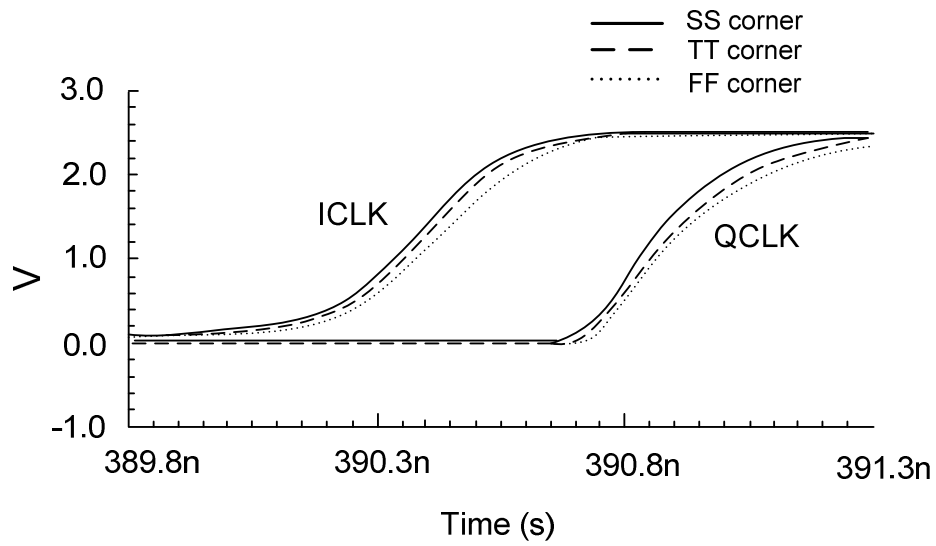
Figure 5.12 Delay over different process corner
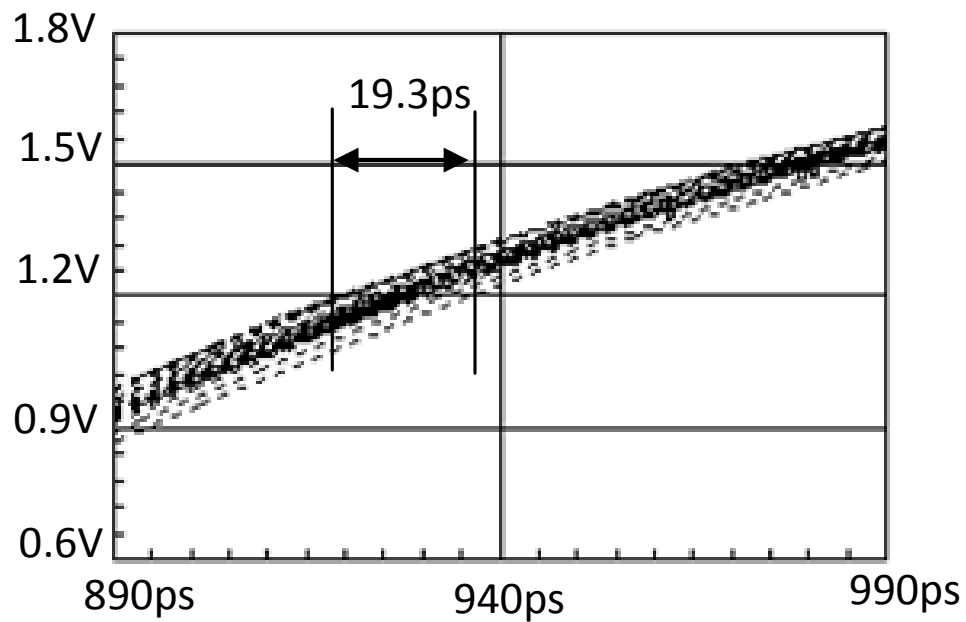
Figure 5.13 The jittering of the clock added by the delay generator

5.2 PLL based delay generator

The DLL based delay generator requires a relatively high frequency reference clock in order to reduce the delay cell numbers in reference DLL. And the delay of each VCDL cell is fixed once the reference clock frequency is setup. Alternatively, the reference DLL in Figure 5.5 can be replaced by a ring oscillator based phase locked loop (PLL). This PLL based delay generator architecture is shown in Figure 5.14. PLL is a loop composed of a voltage controlled ring oscillator, a frequency divider, a phase detector, a charge pump and a loop filter. Under locking condition the propagation delay through VCDL in the ring oscillator is equal to half period of reference clock divided by frequency division ratio M. When PVT condition changes, the VCDL delay as well as
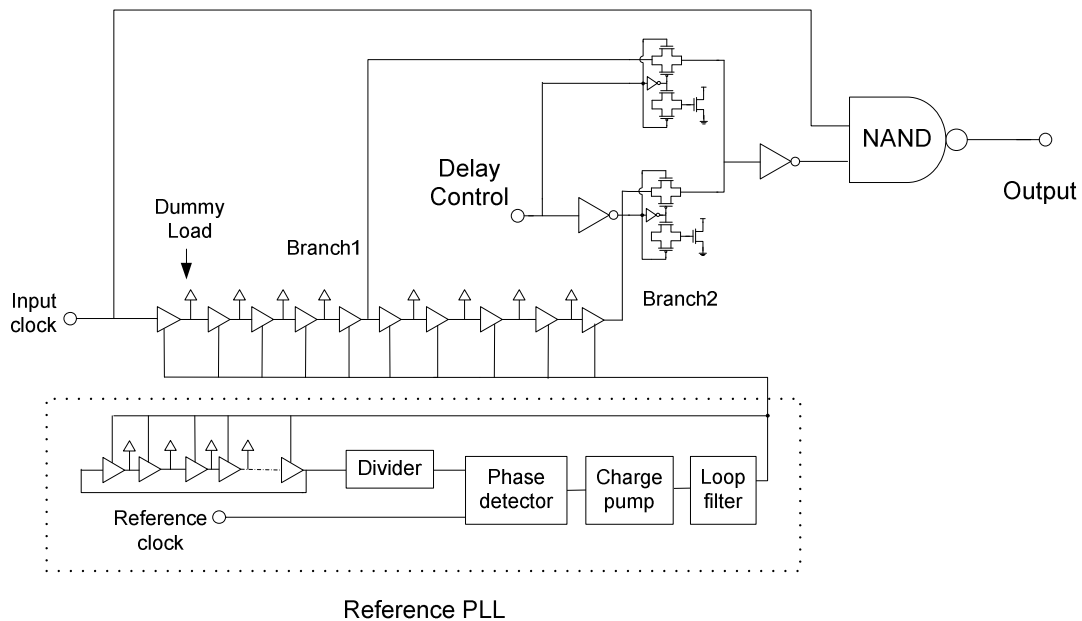
Figure 5.14 System diagram of PLL based delay generator

the ring oscillator frequency will also change. Phase detector detects the frequency shift and conducts the calibration for ring oscillator against PVT variation accordingly through the loop. Each delay cell generates a constant delay value $T_{ref}/2MN$, where T_{ref} is the period of reference clock, N is the number of delay cells in VCDL and M is the divider ratio. The main advantage is that the reference clock can be a low frequency signal source. Additionally the divider ratio M can be made programmable, which means the benefit of programmable delay in VCDL unit.

We implemented a two-branch variable delay generator illustrated in Figure 5.14. Branch 1 in the replica delay line contains 5 delay cells while branch 2 has 10 delay cells. A delay control pin will determine which delay branch is selected. The input clock is combined with the delayed clock to form an impulse for time domain measurement convenience. The ring oscillator in the reference PLL is composed of 20 delay cells. The frequency divider ratio is set to 1 in this design.

5.2.1 Phase detector design

The phase detector topology is exhibited in Figure 5.15. The circuit is composed of two edge-triggered, resettable D flip-flops (DFF) with their D inputs connected to VDD. Terminal *ref* and *clk* act as clock input of two D flip-flops, respectively. If Q output of both D flip-flop is 0, a transition will cause "Up" to go to "high". Subsequent transition on top DFF have no effect on "Up", and when "Down" goes high, the AND gate activates the reset of both flip-flops. Therefore "Up" and "Down" are simultaneously "high" for a duration given by total delay through the AND gate and the

reset path of the flip-flops. Figure 5.16 and Figure 5.17 demonstrate the output of phase detector when two input clock are out of phase and in phase respectively. When one input clock is leading another, one of the outputs will produce a negative pulse to change the stored charge in capacitor of loop filter, therefore changing the biasing voltage of delay cell. The other output will generate a narrow spike which has little effect on the stored charge. When two input clock are in synchronization, both output will be narrow spike. The stored charge remains unchanged.
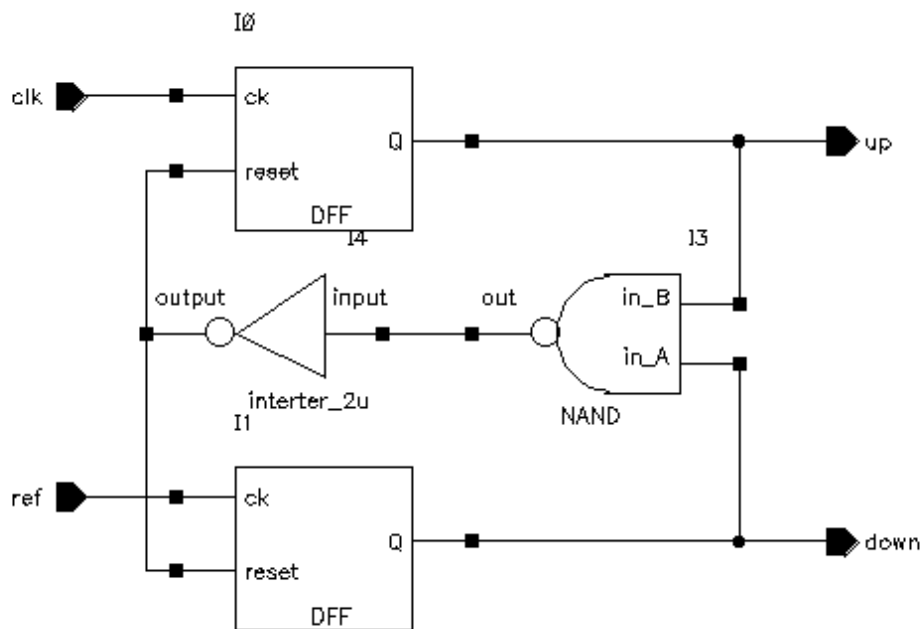
Figure 5.15 Structure of phase detector in PLL
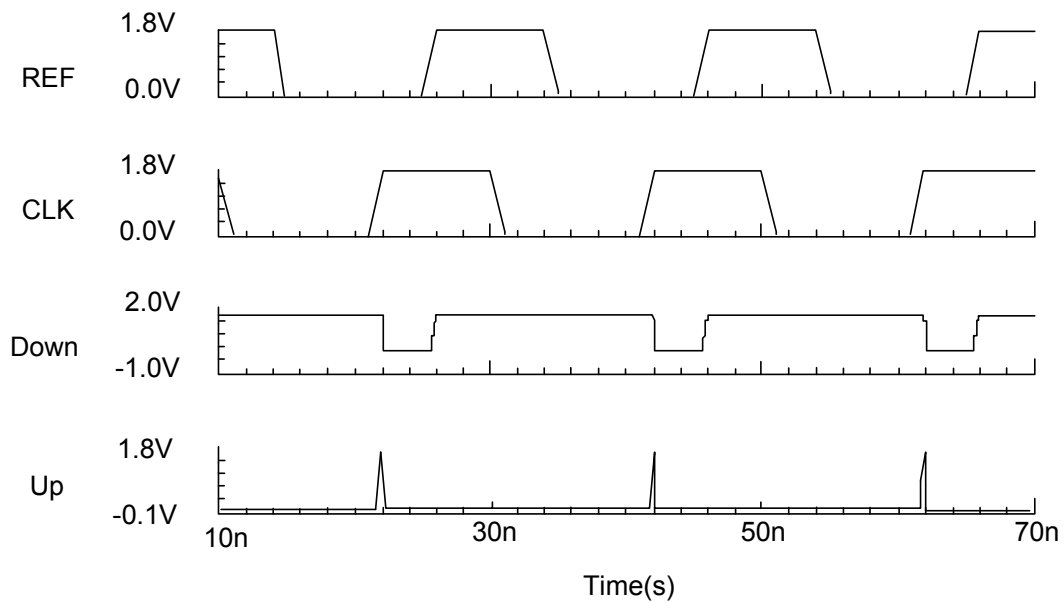
Figure 5.16 Operation waveform of phase detector when CLK is ahead of REF
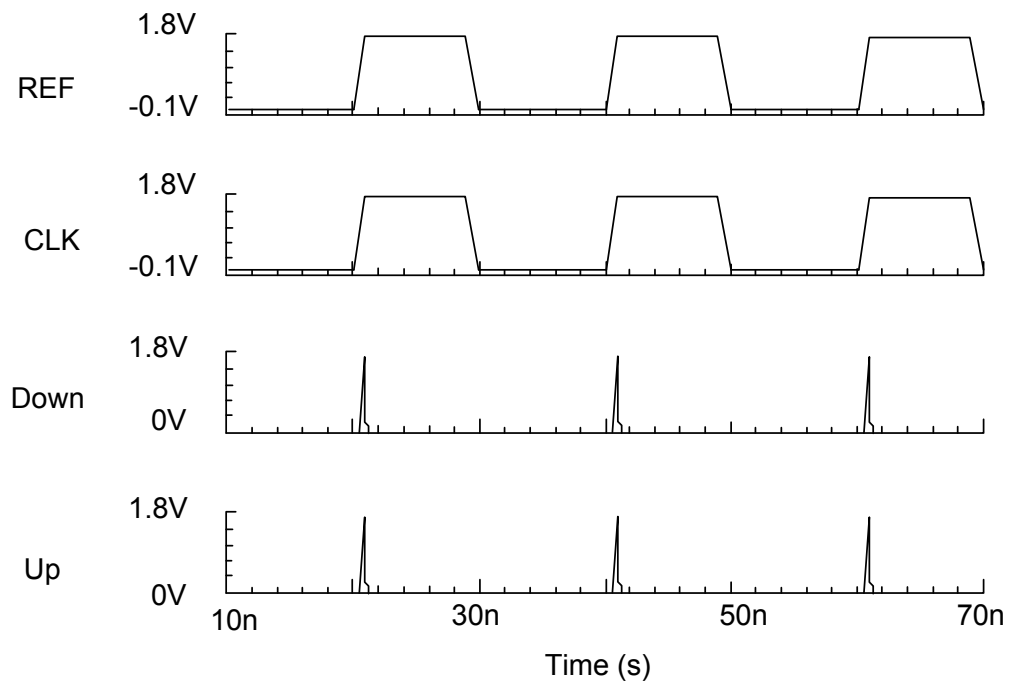
Figure 5.17 Operation waveform of phase detector when CLK and REF are in phase

5.2.2 Charge pump and loop filter design

The schematic of charge pump circuit is given in Figure 5.18. A pull-up and pull-down current are controlled by "Up" and "Down" steering signal from phase detector respectively through switches. Depending on the phase difference between VCO clock and reference clock, the charge pump either charges or discharges the capacitors in loop filter, causing the VCO frequency shift toward one direction or another.
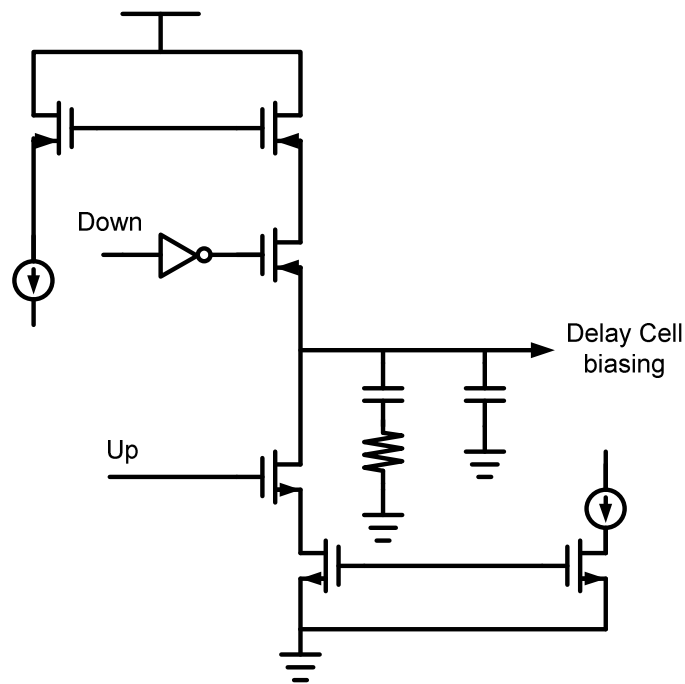
Figure 5.18 Schematic of charge pump and low pass loop filter

5.2.3 Experimental results

The simulated waveform of delay cell biasing voltage in Figure 5.19 can reveal the building up of PLL's stabilization. The toothed shape starting from 0 ns indicates
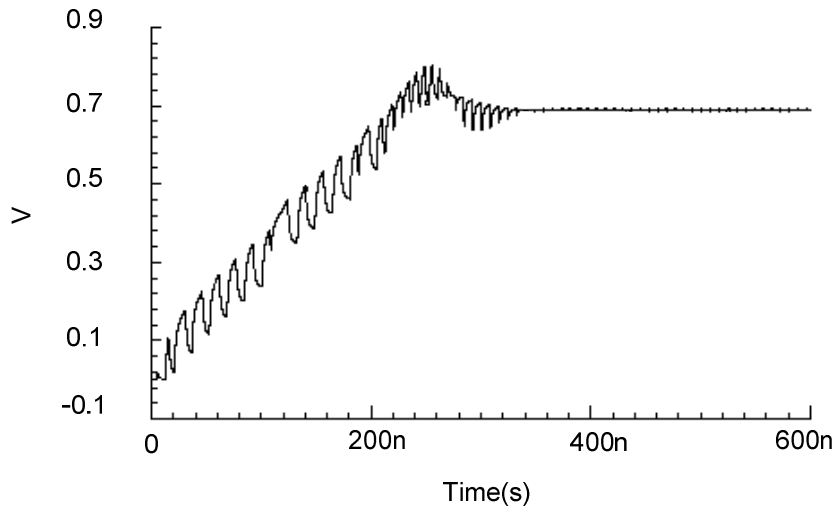
Figure 5.19 Time domain waveform of delay cell biasing voltage

the charge-discharge procedure of the charge pump. After around 350ns, biasing voltage settles at a constant value, which means the stabilization of the PLL is reached. The prototype of PLL based delay generator was fabricated on TSMC CMOS 0.18-μm technology. The layout of the delay generator is shown in Figure 5.20. It occupies the area of 700μm by 560μm including on-wafer probing pads. The measurement is conducted on-wafer using RF probes. Theoretically, the duration of generated impulse is equal to the generated delay. But the actual measured impulse on 50ohm load is always distorted to some extent. However, we can still evaluate the delay of two delay branch by comparing the impulse duration differences. The ring oscillator in the reference PLL is composed of 20 delay cells. Figure 5.21 displays the two impulse waveforms captured on a digital oscilloscope when applying a 100MHz reference clock. The measured delay difference is 1.24 ns, which is very close to the expected value of

1.25ns. Equivalently each delay cell has the delay error of less than 2ps. The designed PLL can track reference clock with frequencies from 60MHz to 180MHz thanks to the large delay tuning range of the delay cell. The total current consumption is 9.5mA under 1.8v power supply.
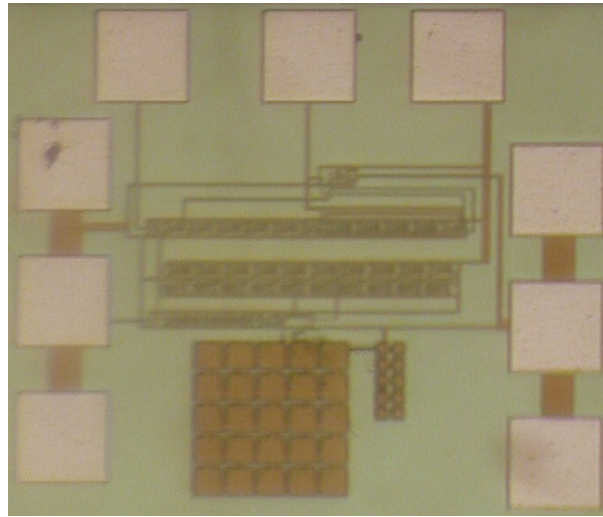
Figure 5.20 Microphoto of fabricated PLL based delay generator
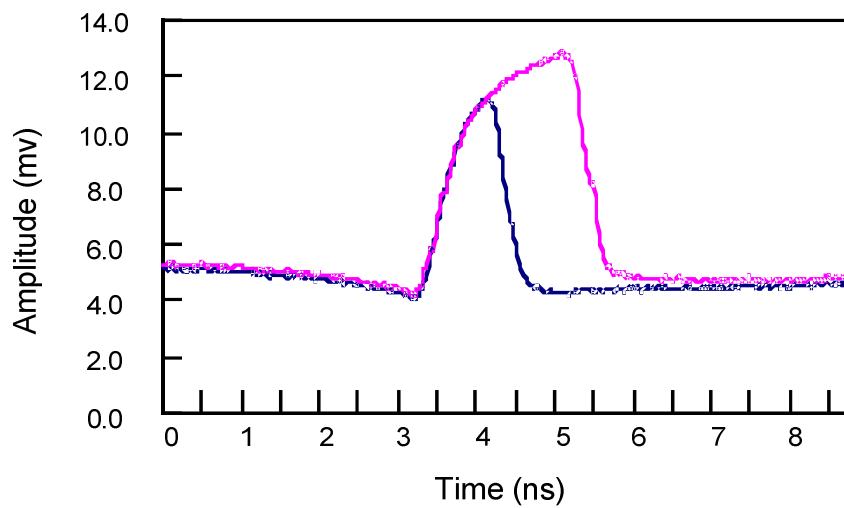
Figure 5.21 Measured impulse for selecting branch 1 and 2

CHAPTER VI

CONCLUSION

6.1 Summary of the research

Ultra-wideband technology distinguishes itself from traditional narrow band system by transmitting discrete short duration pulse and conducting signal processing on time domain. It is capable of transmitting pulse with fine time resolution and high throughput at short distance without affecting other existing radio systems. One of the advantages for traditional UWB system is the simple transceiver structure and low circuit complexity. However the ever increasing requirement for high performance UWB transceiver and engagement of integrated circuit lead modern UWB system seek trade-off between circuit complexity, power consumption and system performance.

This dissertation first described the evolving of UWB system, the basic signal processing and modulation technology on time domain. The main difference between UWB pulse system and narrow band system is that the pulse is transmitted discretely rather than continuously. In another word, the "idle" status occupies a large amount of system time, which leaves an opportunity for circuit designer to achieve low power consumption. Stemming from this concept a two-stage-switching UWB transmitter structure was proposed to generate carrier based UWB signal. The transmitter is power off when no pulse needs to be transmitted, rendering less power consumption. A wideband, power switching SPST switch is used to carry out frequency up-conversion. Because of large power handling ability of the SPST switch the UWB amplifier before the antenna can be removed from transmitter. The transmitter was designed and verified

on TSMC 0.18µm CMOS process. The generated UWB signal has variable duration of from 0.5ns to 2ns. By switching the carrier frequency the UWB signal spectrum can cover the complete 3.1GHz to 10.6GHz UWB band.

By applying a similar two-stage-switching methodology we also designed an Ultra-wideband sampling front-end with inclusion of a wideband LNA and a sampling switch. The DC current of the LNA can be shut off during the idle status to serve for power saving purpose. Due to the fact that the LNA consumes very small amount of current on average we are able to provide enough gain before the sampling stage without consuming too much power, which helps to improve the conversion gain and compress noise figure. Measured results of this sampling front-end show unprecedented performance of 9 to 12 dB voltage conversion gain, 16 to 25 dB noise figure, and power consumption of only 21.6 mW (with buffer) and 11.7 mW (without buffer) across DC to 3.5 GHz with 100-MHz sampling frequency.

The dissertation also discussed timing control circuits, a critical issue in UWB pulse system. Aiming at overcoming PVT variation and obtaining programmable accurate delay, a PLL based delay generator is proposed, analyzed and designed. The delay generator uses an external clock as time reference. The PLL automatically calibrate the active delay line through a negative feedback loop. The creation of replica delay line make the delay generation functional for arbitrary external digital clock signals, regardless their duty cycles, frequencies and coding schemes. The measured delay line has the relative delay error of smaller than 0.2% and less than 10mA of current consumption under 1.8V supply voltage.

6.2 Recommended future work

6.2.1 System integration

The proposed transmitter structure has been verified using external frequency synthesizer, on chip pulse generator and on chip UWB SPST switch. A UWB frequency synthesizer can be implemented on chip alone with the transmitter design presented in the dissertation. The first stage switching approach can be further optimized to allow enough time for frequency synthesizer to power up. PLL based delay generator can be employed in the integrated transmitter to provide accurate pulse duration control.

6.2.2 LNA topology and switching scheme investigation

The two-stage-switching scheme that was invented in sampling front end can also be applied to other Wideband LNA topology. Different wideband LNA architectures can be investigated to further improve the conversion gain and noise figure of the sampling system.

6.2.3 Delay generator programmable divider

In the PLL based delay generator the divider ration determine the delay value of each delay cell. Applying fractional N or sigma delta based divider could potentially achieve better delay step resolution and programmability.

REFERENCES

[1]H. F. Harmuth, "A generalized concept of frequency and some applications", *IEEE. Transactions on Information Theory*, vol. IT-14, May 1968, pp. 375-382.

[2] H.F. Harmuth, "Applications of Walsh functions in communications"*, IEEE Spectrum*, vol. 6, pp. 82-91 November 1969.

[3] G.F. Ross, "Transmission and reception system for generating and receiving base-band duration pulse signals for short base-band pulse communication system", U.S. Patent 3,728,632. 1973.

[4] P. Van Etten, "The present technology of impulse radars,"in *International Radar Conference Proceedings*, October 1977, pp. 535–539.

[5] R.N. Morey, "Geophysical survey system employing electromagnetic impulses". US Patent. 3806795, 1974.

[6] T. E. McEwan, "Ultra-wideband radar motion sensor," U.S. Patent 5361070, 1994.

[7] B. Kull and S. Zeisberg, "UWB receiver performance comparison," in *Proceedings of 2004 International Workshop on Ultra Wideband Systems and Technologies*, May 18-21, 2004, pp. 21-25.

[8] FCC Notice of Proposed Rule Making, "Revision of part 15 of the commission's rules regarding ultra-wideband transmission systems," 2002. [Online]. Available: http://hraunfoss.fcc.gov/edocs public/attachmatch/FCC-02-48A1.pdf, Accessed on Aug.04th, 2008.

[9] G.R. Aiello, "Challenges for ultra-wideband (UWB) CMOS integration" in *Proc. IEEE RFIC Symp.*, Jun. 2003, pp. 497-500.

[10] M. Miao and Cam Nguyen, "On the development of an integrated CMOS based UWB tunable–pulse transmit module," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, pp. 3681-3687, Oct. 2006.

[11] R. J. Fontana, "Recent system applications of short-pulse ultra-wideband (UWB) technology,"   *IEEE Trans. Microwave Theory and Tech.,* vol. 52, no.9, pp. 2087-2104, Sept.2004.

[12] Y. Kim, D. Park, and Y. Joo, "Design of CMOS Scholtz's monocycle pulse generator," *IEEE Conference on Ultra Wideband Systems and Technologies*, pp. 81 – 85, 16-19 Nov 2003.

[13] Y. Zheng, H. Dong, and Y.P. Xu, "A novel CMOS/BiCMOS UWB pulse generator and modulator," *IEEE MTT-S International Microwave Symposium Digest,* vol. 2, pp. 1269 – 1272, 6-11 June 2004.

[14] S. Bagga, W. A. Serdijn, and J. R. Long, "A PPM Gaussian monocycle transmitter for ultra-wideband communications," in *Proc. Joint UWBST/IWUWBS*, May 2004, pp. 130–134.

[15] Y. Jeong, S. Jung, and J. Liu, "A CMOS impulse generator for UWB wireless communication systems," in *IEEE Int. Circuits Syst. Symp.,* May 2004, vol. 4, pp. 129–132.

[16] B. Jung, Y.-H. Tseng, J. Harvey, and R. Harjani, "Pulse generator design for UWB IR communication systems," in *Proc. of 2005 IEEE International Symposium on Circuits and Systems*, vol. 5, May 23-26, 2005, pp. 4381-4384.

[17] R.J. Fontana and J.F. Larrick, "Waveform adaptive ultra-wideband transmitter," *U.S. Patent* 6026 125, Feb.15, 2000.

[18] J. Ryckaert, C. Desset, A. Fort, M. Badaroglu, V. De Heyn, P. Wambacq,G. Van der plas, S.Gonnay, B. Van Poucke, and B.Gyselinckx, "Ultra-wide-band transmitter for low-power wireless body area networks: design and evaluation," *IEEE Trans. Circuits and systems I*, vol.52, no.12, pp.2515-2525, Dec. 2005.

[19] J. Zhao, C. Maxey, A. Narayanan and S. Raman, "A SiGe BiCMOS ultra wide band RFIC transmitter design for wireless sensor networks," in *Proc. Radio and Wireless Conf.,* Sept. 2004, pp.215-218.

[20] TSMC 0.18-μm CMOS Process Design kit, MOSIS Foundry, Marina del Rey, California, USA.

[21] M.-C. Yeh, Z.-M. Tsai, R.-C. Liu, K.-Y. Lin,Y.-T. Chang, and H. Wang, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. Microwave Theory and Tech.,* vol. 51, no.1, pp. 31-39, Jan. 2005.

[22] K. Marsden, H. Lee, D.S. Ha, and H. Lee., "Low power CMOS re-programmable pulse generator for UWB systems" in P*roc. IEEE Conference on Ultra Wideband Systems and Tech.*, Nov. 2003, pp. 443-447.

[23] H. Kim and Y. Joo, "Fifth-derivative Gaussian pulse generator for UWB system," in *Digest of 2005IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, June 12-14, 2005, pp. 671-674.

[24] J. S. Lee and C. Nguyen, "Novel low-cost ultra-wideband, ultra-short-pulse transmitter with MESFET impulse-shaping circuitry for reduced distortion and improved pulse repetition rate," *IEEE Microwave and Wireless Components Letters*, vol. 11, pp. 208-210, May 2001.

[25] Z. N. Low, J. H. Cheong, and C. I. Law, "Novel low cost higher order derivitive Gaussian pulse generator circuit," in *Proc. of 2004 International Conference on Communications Systems*, Sept. 6-8, 2004, pp. 30-34.

[26] J. Han and C. Nguyen, "Ultra-wideband electronically tunable pulse generators," *IEEE Microwave and Wireless Components Letters*, vol. 14, pp. 112-114, Mar. 2004.

[27] P. Rulikowski and J. Barrett, "Truly balanced step recovery diode pulse generator with single power supply," in *Proc. of 2004 IEEE Radio and Wireless Conference*, Sept. 19-22, 2004, pp. 347-350.

[28] J. Taylor, *Introduction to Ultra-wideband radar systems*, 1st ed., CRC Press, Boca Raton, 1995.

[29] Y. W. Yeap, "Ultra wideband signal generation," *Microwave Journal*, vol. 48, no. 9, Sept. 2005, pp. 172-185.

[30] B. Jung, Y.-H. Tseng, J. Harvey, and R. Harjani, "Pulse generator design for UWB IR communication systems," in *Proc. of 2005 IEEE International Symposium on Circuits and Systems*, vol. 5, May 23-26, 2005, pp. 4381-4384.

[31] M. Kahrs, "50 years of RF and microwave sampling," *IEEE Transactions on Microwave Theory and Techniques,* vol. 51, no. 6, June 2003, pp.1787-1805.

[32] J. Han and C. Nguyen, "Coupled-slotline-hybrid sampling mixer integrated with step-recovery-diode pulse generator for UWB applicaitons," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 1875-1882, June 2005.

[33] W.C. Whitely, W.E. Kunz, and W.J. Anklam, "50GHz sampler hybrid utilizing a small shockline and an internal SRD," 1991 *IEEE MTT-S Digest*, pp. 895-89.

[34] D. Jakonis, K. Folkesson, J. Dbrowski, P. Eriksson and C. Sevensson, "A 2.4GHz RF sampling receiver front-end in 0.18µm CMOS," *IEEE J. Solid-State Circuits,* vol. 40, no. 6, pp. 1256–1277, Jun. 2005.

[35] E. Cijvat, P. Eriksson, T. Nianxiong and H. Tenhumen, "A 1.8GHz sub-sampling CMOS downconversion circuit for integrated radio circuits," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 2, May 1998, pp.65-68.

[36] D. Jakonis and C. Svensson, "A 1.6GHz Downconversion sampling mixer in CMOS," in *Proc. IEEE Int. Symp. Circuits and Systems,* vol. 1, May 2003, pp.725-728.

[37] H. Pekau and W. Haslett, "A 2.4 GHz CMOS sub-sampling mixer with integrated filtering," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2159-2166, Nov. 2005.

[38] M. Nakao, S. Takagi and N. Fujii, "Low noise amplifier circuit for bandpass sampling," in *Proc. IEEE Asia Pacific Conf. ASIC,* Aug. 2002, pp.249-252.

[39] Eriksson and H. Tenhunen, "A model for predicting sampler RF bandwidth and conversion loss," in *Proc. IEEE Int. Conf. Circuits and Systems,* vol. 6, May 1999, pp.18-21.

[40] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling system," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp.220-224, Feb. 1990.

[41] A. Parssinen, R. Magoon, S. Long and V. Porra, "A 2-GHz subharmonic sampler for signal down conversion," *IEEE Trans. Microwave Theory and Tech.*, vol 12, pp. 2344-2351, Dec. 1997.

[42] S.S. Mohan, M.D.M. Hershenson, S.P. Boyd, and T.H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no.3, pp. 346-355, Mar. 2000.

[43] M.E. Waltari, and K.A.I. Halonen, *Circuit Techniques for Low-Voltage and High-Speed A/D Converters,* New York, Kluwer Academic Publishers, 2002

[44] CA18HR 0.18-μm Enhance RF CMOS Process, Jazz Semiconductor, Newport Beach, CA, 2007

[45] D. Rowe, B. Pollack, J. Pulver, W. Chon, P. Jett, L. Fullerton, and L. Larson, "A Si/SiGe HBT timing generator IC for high-bandwidth impulse radio applications," *Proc. of the IEEE Custom Integrated Circuits Conference*, May 1999, pp. 221-224.

[46] Y. Moon, J. Choi, K. Lee, D. Jeong, and M. Kim, "An all-analog multiphase delay-locked loop using a replica delay line for wide-range operation and low-jitter performance," *IEEE J. Solid-State Circuits,* vol. 35, pp. 377-384, March 2000.

[47] J. L Rossello and J. Segura, "An analytical charge-based compact delay model for submicrometer CMOS inverters," *IEEE J. Solid-State Circuits,* vol. 51, pp. 1301-1311, July 2004.

[48] D. Auvergne, J.M. Daga, and M. Rezzoug, "Signal transition time effect on CMOS delay," *IEEE Trans. on Circuits and Systems, Part I: Fundamental Theory and Applications,* vol. 47, pp. 1369-1369, Sept. 2000.

VITA

Rui Xu received the B.S. and M.S. in electrical engineering from Southeast University in Nanjing, China, in 1998 and 2001, respectively. In 2002 he joined the Sensing, Imaging and Communication Systems Laboratory at Texas A&M University as a research assistant working toward his doctoral degree. He received his Ph.D. degree in August of 2009. Between September 2007 and August 2008, he was an intern with Qualcomm Inc. in San Diego, California, where he was involved with the development of multi-standard, multi-band complementary metal-oxide-semiconductor (CMOS) radio frequency (RF) front-end receivers. He recently joined Qualcomm Inc. in San Diego, California as a RF integrated circuit senior design engineer. His research interests include RF, microwave and millimeter-wave integrated circuits for wireless communication and sensor systems.

Mr. Xu may be reached at: Qualcomm Inc., 5775 Morehouse Dr., San Diego, CA 92121. His email is: ruix@qualcomm.com.