A HIGHLY LINEAR BROADBAND LNA

A Thesis

by

JOUNG WON PARK

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Sebastian Hoyos
	Kai Chang
	Rainer Fink
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ABSTRACT

A Highly Linear Broadband LNA.

(August 2009)

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Chair of Advisory Committee: Dr. Jose Silva-Martinez

In this work, a highly linear broadband Low Noise Amplifier (LNA) is presented. The linearity issue in broadband Radio Frequency (RF) front-end is introduced, followed by an analysis of the specifications and requirements of a broadband LNA through consideration of broadband, multi-standard front-end design. Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) non-linearity characteristics cause linearity problems in the RF front-end system. To solve this problem, feedback and the Derivative Superposition Method linearized MOSFET. In this work, novel linearization approaches such as the constant current biasing and the Derivative Superposition Method using a triode region transistor improve linearization stability against Process, Supply Voltage, and Temperature (PVT) variations and increase high power input capability. After analyzing and designing a resistive feedback LNA, novel linearization methods were applied. A highly linear broadband LNA is designed and simulated in 65nm CMOS technology. Simulation results including PVT variation and the Monte Carlo simulation are presented. We obtained -10dB S11, 9.77dB S21, and 4.63dB Noise Figure with IIP3 of 19.18dBm for the designed LNA.

To my parents, my sister, and my beloved wife …

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CHAPTER I

INTRODUCTION

1.1 Background of Broadband Multi-Standard RF Front-End

Following the demand of customers, wireless devices have been developed to provide a number of functionalities, such as phone calls, internet access, and GPS. Ten years ago, a cell phone could support either Code Division Multiple Access (CDMA) or Global System for Mobile (GSM). Presently, cell phones are expected to support Universal Mobile Telecommunications System (UMTS) (850, 1900, 2100 MHz) and GSM (850, 900, 1800, 1900 MHz). On top of that, more customers are seeking wireless internet access and wireless device connections encouraging cell phone venders are providing Wi-Fi (2400 MHz) and Bluetooth (2400 MHz) services. Although the performance of the conventional narrowband RF front-end has been tested and proven, a narrowband RF front-end could cover only one of many aforementioned frequency bands. Thus, several narrowband RF front-ends are required for supporting all services.

Although several narrowband RF front-ends are required, designing and fabricating a number of different RF front-ends is not cost effective. It requires several times longer designing time and several times larger die area. Thus, a broadband multi-standard RF front-end system able to cover the multiple frequency bands is attractive for its versatility and low cost.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

1.2 Design Consideration for Broadband LNAs

As we can see in Fig. 1.1, an LNA should process a broadband signal to cover a very wide frequency band. A bandpass filter eliminates unnecessary signals outside a frequency band. However, interferers might exist inside the band pass frequency.

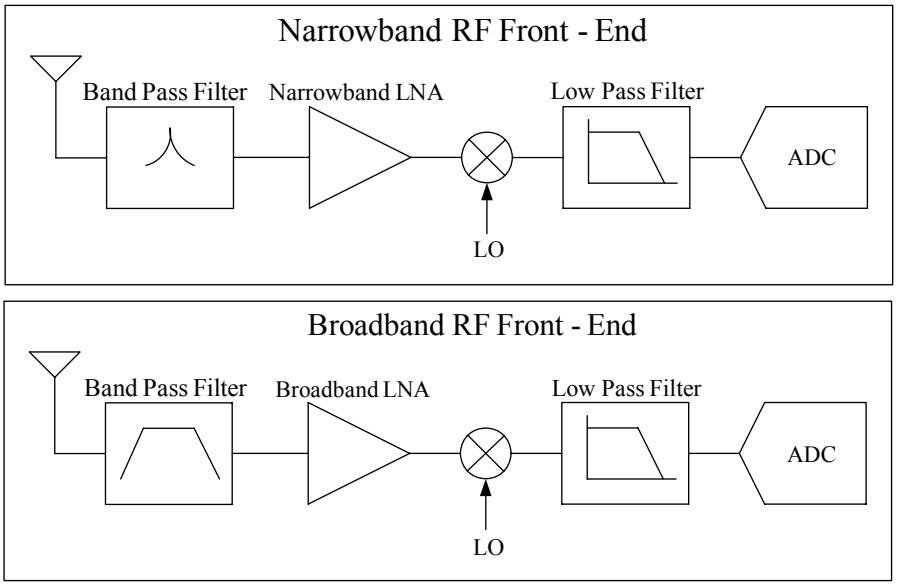


Fig. 1.1 Narrowband RF Front-End and Broadband RF Front-End

The primary concern of a broadband LNA is its linearity. If we have a non-linear amplifier, the third order intermodulation distortion usually falls into the main signal band as shown in Fig. 1.2 [1].

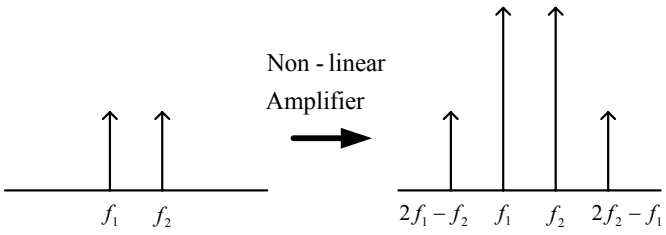


Fig. 1.2 Third Intermodulation Distortion in Non-Linear Amplifier

Fig. 1.3 describes what happens when a narrowband LNA processes the main signal close two high power interferers.

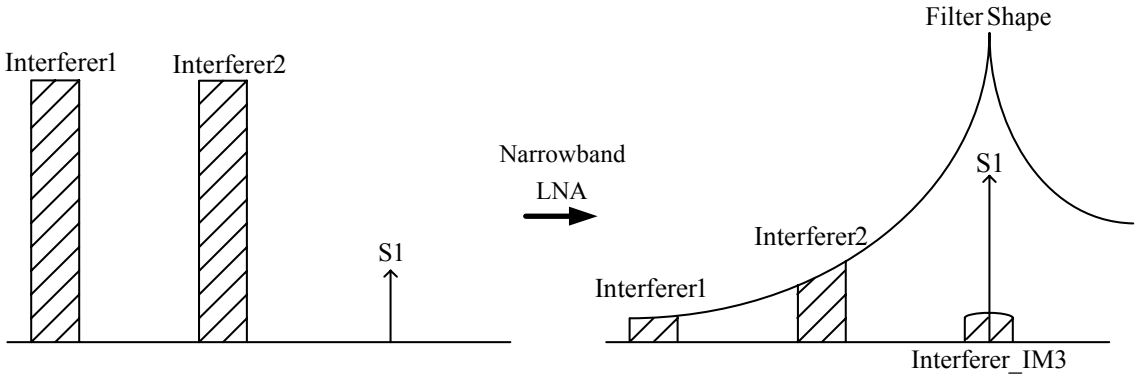


Fig. 1.3 Signal Processing in Narrowband LNA

A bandpass filter suppresses interferers and prevents an LNA from generating a large power image signal, Interferer_IM3, close to the main signal, S1. Thus, the main signal can be recovered in spite of the image signal. However, this scenario drastically changes in the case of a broadband LNA.

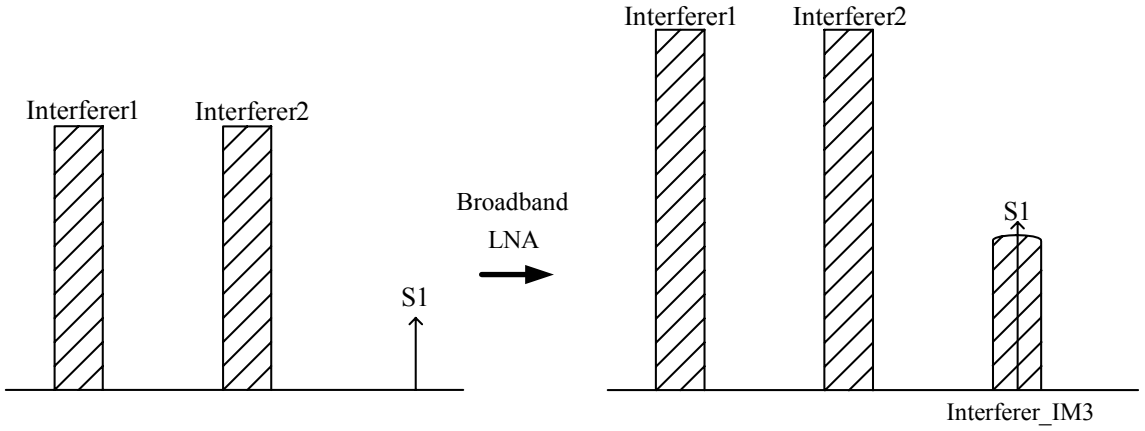


Fig. 1.4 Signal Processing in Broadband LNA

A band pass filter is broadband. Thus, interferers existing near the main signal are not suppressed as shown in Fig. 1.4. Due to cross terms of non-linear devices, these interferers create an image signal, Interferer_IM3, near the main signal, S1. An LNA needs to be highly linear to minimize the power of the image signal. If an LNA is not linear enough, the power of the image signal might be similar to that of the main signal which would make the main signal indistinguishable. In other words, the Minimum Detectable Signal of the system is dominated by the image signal generated due to cross terms present in the non-linear devices. In this situation, lowering Noise Figure does not help improve the Minimum Detectable Signal performance of the system. Although the last stage of an RF front-end is generally considered the most important in the linearity performance, linearity of an LNA and a Mixer in a broadband multi-standard RF front-end are also significant.

1.3 Previous Work

Recently, broadband LNAs were suggested for broadband signal processing [2]–[6]. The resistive feedback LNA in [5] achieved below 3 dB Noise Figure while other performances are similar to narrowband. In [3] and [4], the common-gate LNA was implemented to achieve low Noise Figure using the noise cancellation method. While the noise performance and bandwidth of deep sub-micron CMOS improve with scaling down, the linearity has suffered from the limited supply voltage and high-field mobility effects [7], [8]. The multi-standard RF front-ends require high linearity to suppress the cross-modulation caused by interferers [9].

To improve the linearity of MOSFETs, a number of linearization methods for LNAs have been proposed. A MOSFET can be linearized by applying a proper gate-source voltage (V_{gs}) at which the third order derivative of drain-source current $\frac{d^3 i_{ds}}{dV_{gs}^3}$ is zero [10]-[11]. High third order input intermodulation distortion product (IIP3) is achieved only near the bias point, also called "sweet spot." Furthermore, this method is very sensitive to process and temperature variations. To increase IIP3 stability, the Derivative Superposition (DS) method or the multiple gated transistors method are introduced [12]-[13]. These methods employ multiple gated MOSFETs of different widths and different gate biases to achieve a composite dc transfer characteristic of zero for the total third order derivative of the drain-source current. The main transistor is biased in the saturation region where the third order derivative of the drain-source current is positive and the additional transistor is biased in the sub-threshold region where the third order derivative of the drain-source current is negative. Although these methods are less sensitive than applying a proper gate-source voltage (V_{gs}) method, process and temperature variations are still causing IIP3 instability.

The Modified Derivative Superposition (MDS) method is introduced for the narrowband LNA linearization [14]. The DS method using the additional transistor in the triode region, instead of the sub-threshold region, is also proposed [15]. Other linearization methods are introduced [16]-[20]. However, most of linearization methods are sensitive to process, temperature, and supply voltage variations.

1.4 This Work

In this work, we will exploit high f_t of deep sub-micron transistors and use the proposed novel Derivative Superposition method to design a highly linear broadband LNA. All transistors are biased with constant currents for process and temperature variations tracking. Two additional transistors, one with operating in the triode region and the other in the sub-threshold region, are introduced to compensate the third order derivative of the drain-source current of the saturation region transistor. We obtained -10dB S11, 9.77dB S21, and 4.63dB Noise Figure with IIP3 of 19.18dBm for the designed LNA with the condition of Typical process and 25°C. The designed LNA showed at least 9dB intermodulation distortion power reduction over the conventional LNA for all corners and all temperatures up to -15dBm input power.

1.5 Organization of Thesis

In Chapter II, the MOSFET non-linearity characteristic is analyzed and the limitation of IIP3 performance due to this characteristic is presented. Then, linearization methods, such as feedback and the DS method, are analyzed for LNA linearization. The novel DS methods, such as the constant current biasing and using a triode region transistor, are introduced. These methods provide stable linearization for all processes and temperatures, even with high power input conditions. In Chapter III, a resistive feedback topology is considered as a broadband LNA. A resistive feedback topology is analyzed to find its frequency response, Noise Figure, and linearity characteristics. Then, the novel linearization approach is applied to the resistive feedback topology for a highly

linear broadband LNA. In Chapter IV, LNA performances with and without linearization method are compared. This comparison is done for the three corners simulations. Then, process, temperature, and supply voltage variations simulations are done to check the stability of linearization methods over PVT variations. The Monte Carlo simulation results are also included to find the mismatch impact on the LNA performance. Chapter V of this thesis includes conclusions for these simulations.

CHAPTER II

LINEARIZATION TECHNIQUE

2.1 Non-Linear System Response and IIP3

When two different frequency inputs are applied to a non-linear system, this system generates a number of cross modulated outputs. Resultant frequencies are determined by combinations of two input frequencies. Fig. 2.1 represents a non-linear system model.

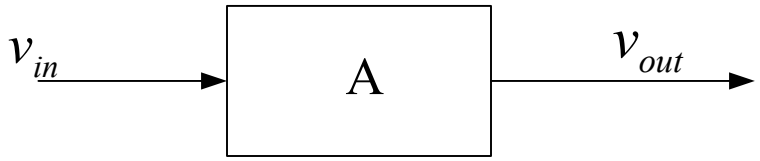


Fig. 2.1 Non-Linear System

Usually, a non-linear system can be modeled as

$$v_{out} = a_1 v_{in} + a_2 v_{in}^2 + a_3 v_{in}^3 \tag{2-1}$$

If the input is consist with signals having frequencies ω_1 and ω_2 , $v_{in} = A\cos(\omega_1 t) + A\cos(\omega_2 t)$, where A is amplitude of the signals. Then,

$$v_{out} = a_2 A^2 + \left(a_1 A + \frac{9a_3 A^3}{4} \right) \cos(\omega_1 t) + \left(a_1 A + \frac{9a_3 A^3}{4} \right) \cos(\omega_2 t) +$$
$$\left(\frac{a_2 A^2}{2} \right) \cos(2\omega_1 t) + \left(\frac{a_2 A^2}{2} \right) \cos(2\omega_2 t) + (a_2 A^2) \cos((\omega_1 + \omega_2)t) +$$
$$(a_2 A^2) \cos((\omega_1 - \omega_2)t) + \left(\frac{3a_3 A^3}{4} \right) \cos((2\omega_1 - \omega_2)t) + \left(\frac{3a_3 A^3}{4} \right) \cos((2\omega_2 - \omega_1)t) + \quad (2\text{-}2)$$
$$\left(\frac{3a_3 A^3}{4} \right) \cos((2\omega_1 + \omega_2)t) + \left(\frac{3a_3 A^3}{4} \right) \cos((2\omega_2 + \omega_1)t) +$$
$$\left(\frac{a_3 A^3}{4} \right) \cos(3\omega_1 t) + \left(\frac{a_3 A^3}{4} \right) \cos(3\omega_2 t)$$

Equation (2-2) shows that a non-linear system generates 12 frequency outputs when two frequency inputs are applied. Intermodulation distortion signals at frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are most problematic since they are very close to ω_1 and ω_2 as shown in Fig. 1.2. If signal powers at the frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are similar to those of the main signals, recovering the main signals would be difficult.

The third order intercept point (IIP3) is defined as the input power where the output power of the main signal at the frequencies of ω_1 and ω_2 are the same as the output power of the intermodulation distortion signals at the frequencies of $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$. Thus, IIP3 is defined as

$$a_1 A_{IIP3} = \frac{3a_3 A_{IIP3}^3}{4} \rightarrow A_{IIP3} = \sqrt{\frac{4|a_1|}{3|a_3|}} \quad (2\text{-}3)$$

Hence linear systems certainly require to minimize the third order non-linear term a_3.

2.2 MOSFET Non-Linear Characteristic

MOSFET transistors can be modeled as a non-linear device. When the gate-source input voltage, V_{gs}, is applied to MOSFET transistors, the non-linear drain-source current, I_{ds}, is generated. Fixing the drain-source voltage, V_{ds} such that the transistor operates in the saturation region, and sweeping V_{gs}, the DC current I_{ds} characteristic can be obtained as displayed in Fig. 2.2.

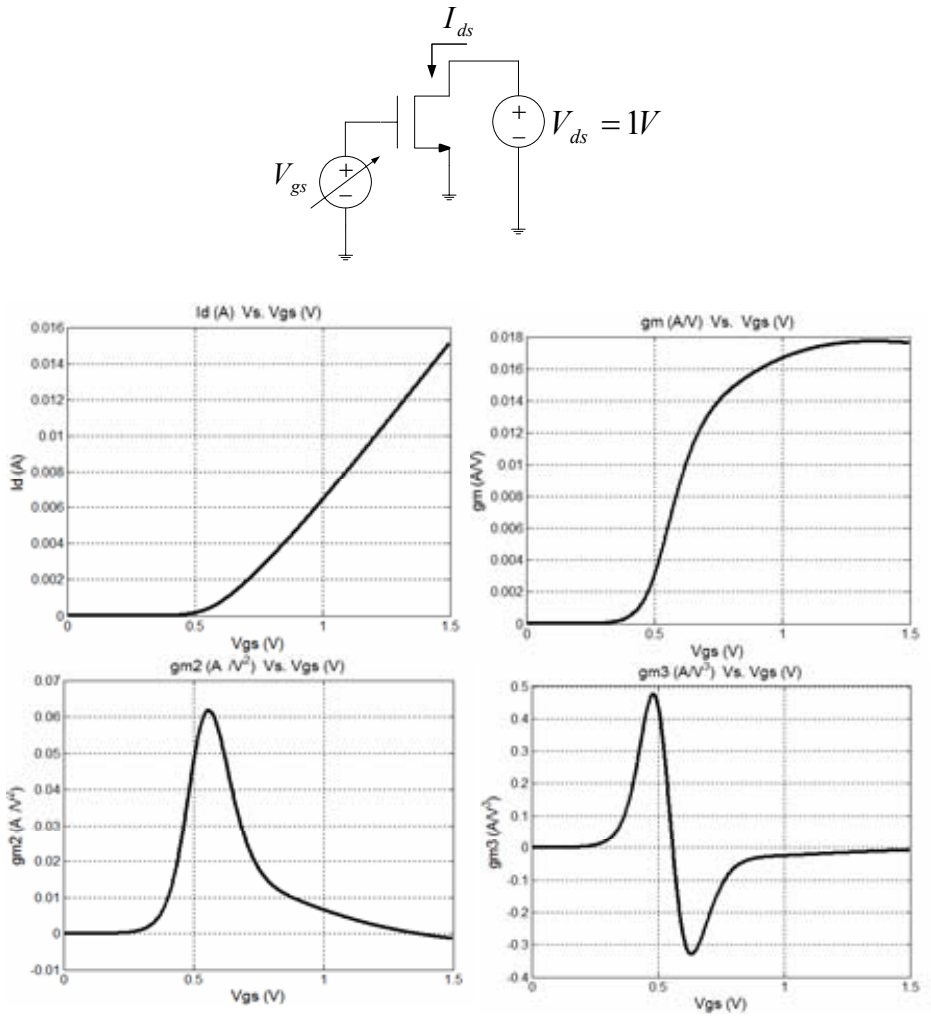


Fig. 2.2 Test Circuit and DC Characteristic of I_{ds}

The first graph of Fig. 2.2 represents the DC characteristic of I_{ds}, the second graph shows transconductance $g_m = \frac{dI_{ds}}{dV_{gs}}$, the third graph shows $g_{m2} = \frac{d^2 I_{ds}}{dV_{gs}^2}$, and the forth graph shows $g_{m3} = \frac{d^3 I_{ds}}{dV_{gs}^3}$. Then, the small signal output current, i_{ds}, can be modeled as

$$i_{ds} = g_m v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 \tag{2-4}$$

where v_{gs} represents the small signal input voltage. When two frequency inputs are applied to a MOSFET, the third intermodulation distortion signals are generated mainly due to the presence of g_{m3}.

While V_{gs} is smaller than the threshold voltage, V_{th}, the MOSFET operates in the sub-threshold region. In this region, the output current is dominantly generated by the Diffusion mechanism and is modeled as

$$I_{ds} \approx I_{d0}\left(1 - e^{\frac{-V_{ds}}{\phi_t}}\right) e^{\frac{(V_{gs} - V_{th})}{n\phi_t}} \tag{2-5}$$

where $I_{d0} = \mu C_{ox} 2n\phi_t^2 \frac{W}{L}$, μ is the mobility of carriers, C_{ox} is oxide capacitance per unit area, W is the width of the transistor, L is the length of the transistor, $\phi_t = kT/q$, and n is fitting parameter which is normally 1~2 in short channel devices. Equation (2-5) can be described using the Taylor Series when V_{ds} and V_{th} are constant and $V_{gs} \approx 0$.

$$I_{ds} \approx I_o e^{\frac{V_{gs}}{n\phi_t}} \approx I_0\left(1+\frac{1}{n\phi_t}V_{gs}+\frac{1}{2(n\phi_t)^2}V_{gs}^2+\frac{1}{6(n\phi_t)^3}V_{gs}^3+\ldots\right) \qquad (2\text{-}6)$$

where $I_o = I_{d0}\left(1-e^{\frac{-V_{ds}}{\phi_t}}\right)e^{\frac{-V_{th}}{n\phi_t}}$.

Since the coefficient of the third order term in the sub-threshold region is positive, g_{m3} is positive as noted in Fig. 2.3.

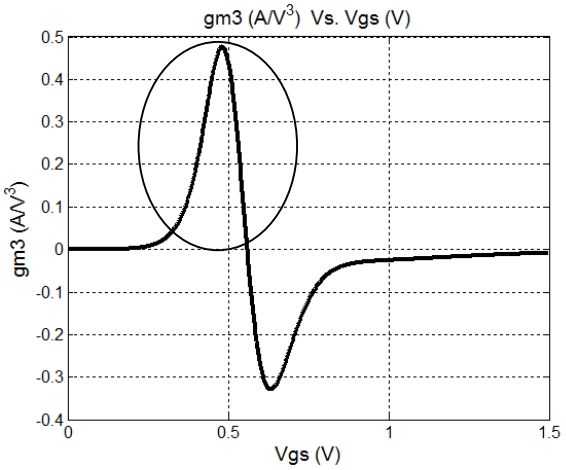


Fig. 2.3 g_{m3} in the Sub-Threshold Region

The mechanism of the output current of a MOSFET drastically changes from Diffusion to Drift when V_{gs} is equal to V_{th}. In this situation, the output current of the MOSFET follows the square-law (2-7).

$$I_{ds} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)\left(V_{gs}-V_{th}\right)^2 \qquad (2\text{-}7)$$

If V_{gs} becomes larger than V_{th}, the output current essentially follows the square-law. On top of the square-law, the short channel effect and the mobility degradation are

applied. Since the mobility is degraded as V_{gs} increases, the output current can be described as

$$I_{ds} \approx \frac{1}{2}\mu_0 C_{ox}\left(\frac{W}{L}\right)\left(V_{gs}-V_{th}\right)^a \tag{2-8}$$

where a is slightly less than 2, especially when large electric fields are present.

In this case, the third order derivative of I_{ds} is negative as noted in Fig. 2.4.

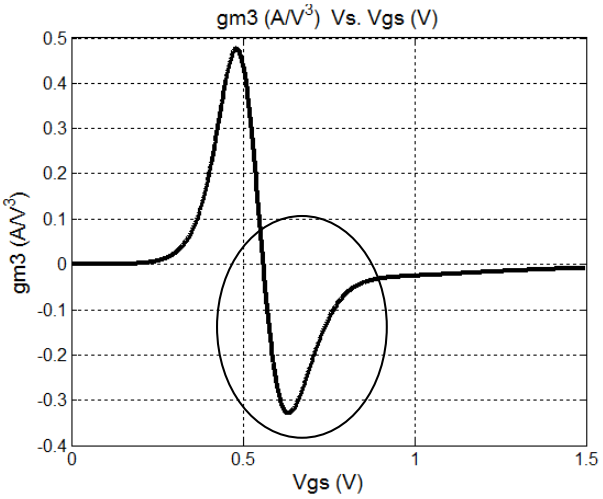


Fig. 2.4 g_{m3} in the Saturation Region

Based on g_m and g_{m3} graphs and from equation (2-3), the IIP3 can be calculated as equation (2-9) when $R_{in} = 50\Omega$.

$$IIP3(dBm) = 10\cdot\log\left(\frac{A_{IIP3}^2}{R_{in}}\right) = 10\cdot\log\left(\frac{3}{4}\cdot\frac{g_m}{g_{m3}}\cdot\frac{1}{50}\right) \tag{2-9}$$

From equation (2-9), and Fig. 2.2, we can obtain the IIP3 graph.

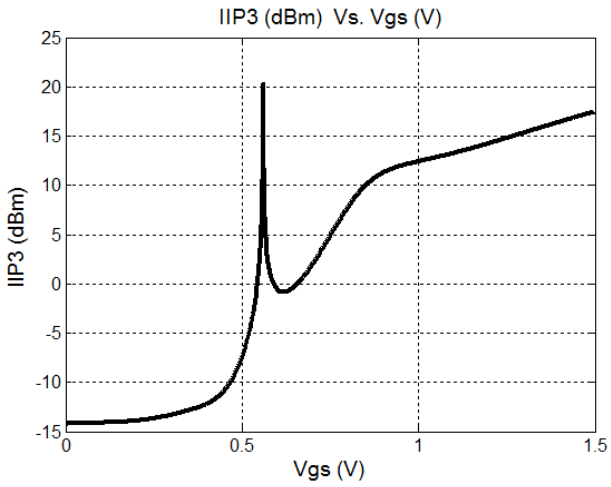


Fig. 2.5 IIP3 vs. V_{gs} for MOSFET Transistor

A so called “sweet spot” exists when the MOSFET operating point changes from sub-threshold to saturation. This point is also proper for the RF circuit since it is a power effective region. In the strong inversion region, g_m does not increase as much as it does in the medium inversion region when the DC current increases. However, a “sweet spot” is a very narrow region meaning that the high IIP3 can be only obtained for the limited input signal power. Moreover, this spot is sensitive to process and temperature variations since the threshold voltage changes as process and temperature change. Thus, exploiting this spot is ineffective in achieving the high IIP3.

According to Fig. 2.5, the high IIP3 can also be achieved by applying large V_{gs}. Unfortunately, this option is not suitable since it requires huge power consumption.

2.3 Feedback

Feedback helps improve the system linearity in two ways. It reduces the amplitude of the main signal so that the power of the third order intermodulation distortion is also decreased. On top of that, the power of the third order intermodulation distortion is reduced by the linear feedback. Although the feedback reduces the power of the main signal, the power of the third order intermodulation distortion is further decreased so that the linearity of the whole system improves. A sample feedback system is displayed in Fig. 2.6.

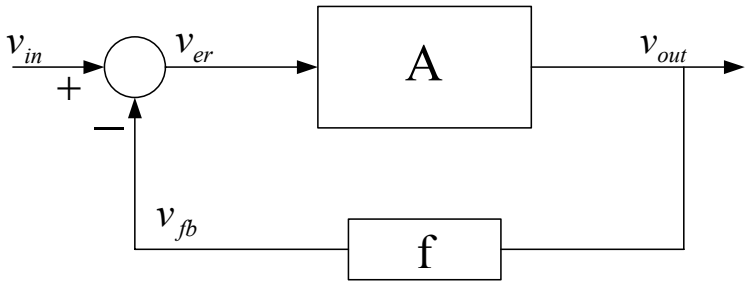


Fig. 2.6 Non-Linear System with Feedback

In this system, the output signal can be modeled as a function of v_{er}.

$$v_{out} = a_1 v_{er} + a_2 v_{er}^2 + a_3 v_{er}^3 \tag{2-10}$$

$$v_{er} = v_{in} - f v_{out} \tag{2-11}$$

where f is assumed to be constant. Then, the output signal can be redefined as

$$v_{out} = b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3 + \ldots \tag{2-12}$$

where b_1, b_2, b_3 represent non-linear coefficients of the feedback system.

From equations (2-10) ~ (2-13), it can be shown that

$$\begin{aligned} b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3 = {} & a_1[v_{in} - f(b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3)] \\ & + a_2[v_{in} - f(b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3)]^2 \\ & + a_3[v_{in} - f(b_1 v_{in} + b_2 v_{in}^2 + b_3 v_{in}^3)]^3 \end{aligned} \tag{2-13}$$

From equation (2-13), the relationship between a_1, a_2, a_3 and b_1, b_2, b_3 can be obtained. The first order coefficient is described in equation (2-14).

$$b_1 = \frac{a_1}{1 + a_1 \cdot f} \tag{2-14}$$

The second order coefficient is described in equation (2-15).

$$b_2 = \frac{a_2}{1 + a_1 \cdot f} \cdot (1 - f \cdot b_1)^2 = \frac{a_2}{1 + a_1 \cdot f} \cdot \left(1 - \frac{a_1 \cdot f}{1 + a_1 \cdot f}\right)^2 = \frac{a_2}{(1 + a_1 \cdot f)^3} \tag{2-15}$$

The third order coefficient is described in equation (2-16).

$$b_3 = -a_1 \cdot b_3 \cdot f - 2 \cdot a_2 \cdot b_2 \cdot f(1 - b_1 \cdot f) + a_3(1 - b_1 \cdot f)^3 \tag{2-16}$$

If we combine equations (2-14), (2-15), and (2-16), equation (2-17) is obtained.

$$b_3 = \frac{1}{(1 + a_1 \cdot f)^5} \cdot \left[a_3 \cdot (1 + a_1 \cdot f) - 2 \cdot a_2^2 \cdot f\right] \tag{2-17}$$

If we assume that $a_3 \cdot (1 + a_1 \cdot f) >> 2 \cdot a_2^2 \cdot f$, equation (2-17) is rewritten as

$$b_3 = \frac{a_3}{(1 + a_1 \cdot f)^4} \tag{2-18}$$

As expected, equation (2-18) shows that the third order non-linear coefficient is proportional to $\frac{1}{(1+a_1 \cdot f)^4}$. Compared to the first order non-linear coefficient, b_1, which is proportional to $\frac{1}{1+a_1 \cdot f}$, the third order non-linear coefficient is drastically reduced by the linear feedback.

$$\frac{b_3}{b_1} = \frac{\frac{a_3}{(1+a_1 \cdot f)^4}}{\frac{a_1}{1+a_1 \cdot f}} = \frac{a_3}{a_1} \cdot \frac{1}{(1+a_1 \cdot f)^3} \tag{2-19}$$

From the equation (2-19), the ratio $\frac{b_3}{b_1}$ is approximately decreased by the factor of cubic of the feedback loop-gain, when $a_1 \cdot f >> 1$. Thus, feedback helps improve the linearity of the system.

Furthermore, equation (2-17) shows that the third order non-linear coefficient of the feedback system is not only affected by the third order non-linear coefficient of the original system but also by the second order non-linear coefficient. In reality, all systems with MOSFET transistors are feedback systems because parasitic capacitance exists between gate-drain, gate-source and drain-source. A DC analysis of non-linear coefficients, thus, is no longer valid at high frequency because the feedback factor increases at a high frequency. A non-linear coefficient analysis at a high frequency is discussed in the next section.

2.4 Derivative Superposition Method

Research has been done to make g_{m3} equal to zero for the high linearity. A potential solution combines two transistors working in different regions [14], combines one transistor working in the sub-threshold region and another transistor in the saturation region to make g_{m3} equal to zero.

2.4.1 Low Frequency Analysis

Fig. 2.7 shows the operation region of two transistors, M_A and M_B. The main goal is to make the sum of g_{m3} of M_A (g_{m3A}) and g_{m3} of M_B (g_{m3B}) equal to zero. Since the absolute value of g_{m3B} is usually smaller than g_{m3A}, the size of the sub-threshold region transistor, M_A, has to be smaller than M_B. However, the exact dimensions that cancel the non-linearities is sensitive to PVT variations. Therefore, A DC characterization of a MOSFET transistor is required before designing the linear LNA.

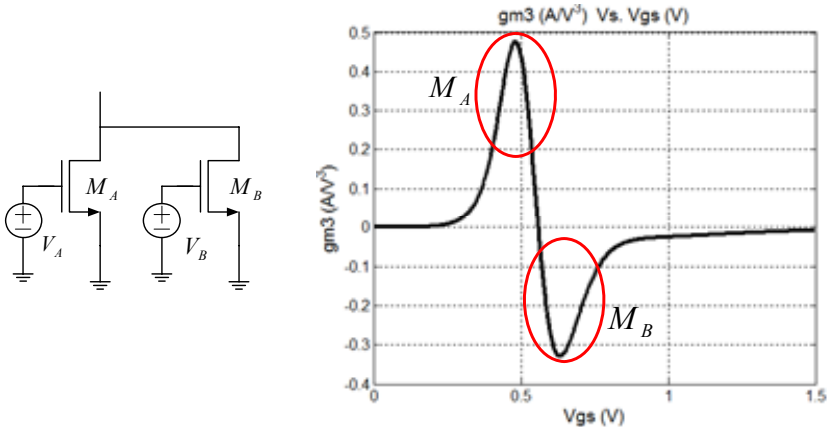


Fig. 2.7 Proper Biasing Points for Derivative Superposition Method

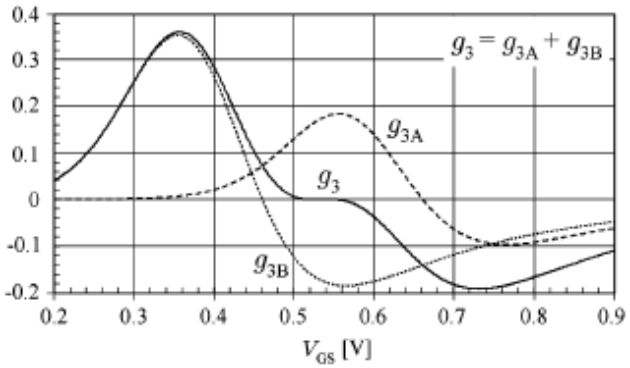


Fig. 2.8 g_{m3} Cancellation [14]

As shown in Fig. 2.8, adding two transistors' currents generates the sum total g_{m3} equal to zero. The size of M_A has to be 70% of M_B [14].

2.4.2 High Frequency Analysis

In a narrow band LNA, the Derivative Superposition method is frequently used for improving the linearity of a system. The compensated LNA is used in the conventional inductive source degeneration topology as shown in Fig. 2.9.

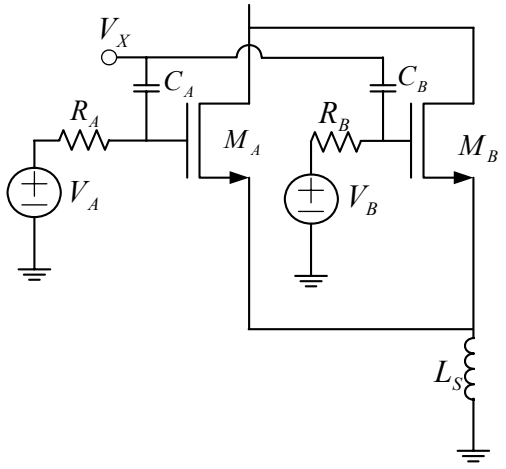


Fig. 2.9 Derivative Superposition Method with Inductive Source Degeneration

The inductive source degeneration topology can be modeled as a feedback system. Thus, we have to consider g_{m3} and g_{m2} for IIP3 characterization. This can be done using volterra series.

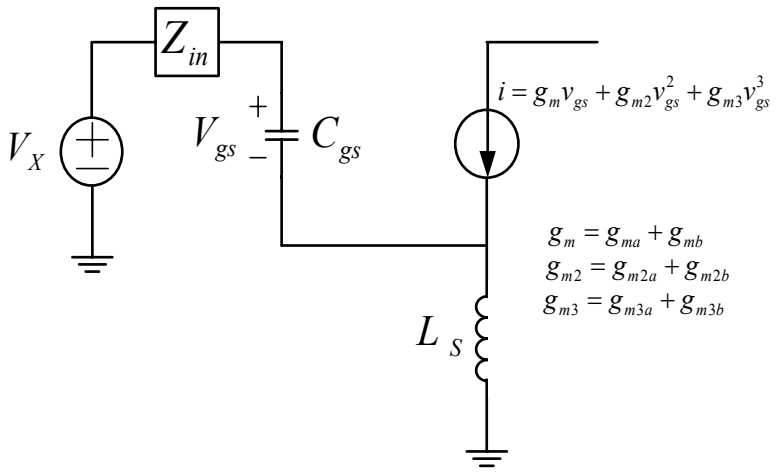


Fig. 2.10 Small Signal Model for Derivative Superposition Method

The LNA small signal model is shown in Fig. 2.10. The gate-drain parasitic capacitance is assumed to be negligible. LNA's total transconductance, total first order derivative of g_m , and total second order derivative of g_m are represented as g_m, g_{m2}, g_{m3} while g_{ma}, g_{m2a}, g_{m3a} and g_{mb}, g_{m2b}, g_{m3b} represent those of M_A and M_B respectively. This circuit can be considered a feedback system with a frequency dependant feedback loop. Therefore, the third order non-linear coefficient is also frequency dependant. From [14], we can obtain IIP3 equation (2-20).

$$IIP3 = \frac{4 g_m^2 \omega^2 L_s C_{gs}}{3|\varepsilon|} \tag{2-20}$$

where

$$\varepsilon = g_{m3} - \frac{\frac{2g_{m2}^2}{3}}{g_m + \frac{1}{j2\omega L_s} + j2\omega C_{gs} + Z_{in}(2\omega)\cdot\frac{C_{gs}}{L_s}}. \quad (2\text{-}21)$$

This result indicates that IIP3 is not only dependant on the total g_m and g_{m3} but also on the total g_{m2} and other variables including the source degeneration inductor, C_{gs}, and the input impedance. Therefore, all variables mentioned above should be taken into account when choosing the size and bias point of the additional transistor operating in the sub-threshold region.

The advantage of this method is the g_{m3} cancellation. Because the additional transistor is working in the sub-threshold region, only a small amount of additional current is required. So, this method can improve IIP3 without significant power overhead. But, it has its own drawbacks. The input parasitic capacitance increases by at least 70% causing frequency response such as, S21 and Noise Figure, to be degraded. The LNA bandwidth also reduces significantly. Since the size of the additional transistor should be similar to that of the main transistor, these drawbacks are inevitable. Furthermore, this method is sensitive to process and temperature variations as shown in Fig. 2.11. SS means a Slow process and 100°C corner, TT means a Typical process and 65°C corner, and FF means a Fast process and -25°C corner.

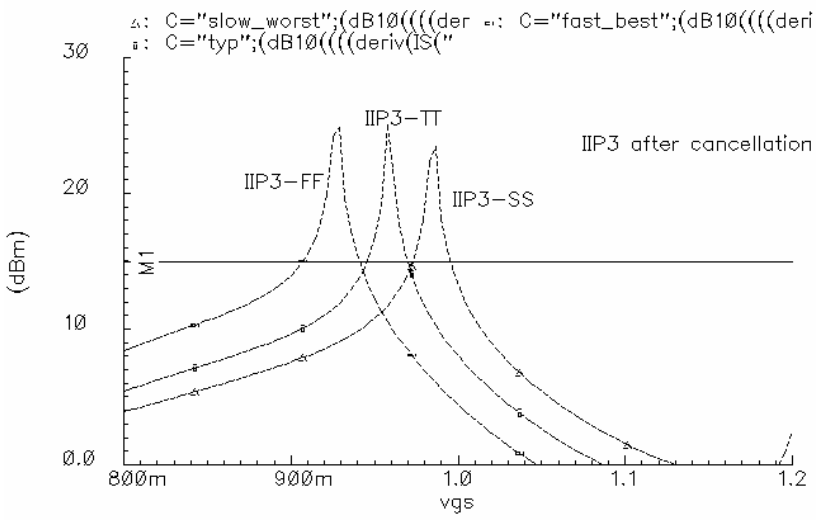


Fig. 2.11 DS Method Sensitivity to Process and Temperature Variations

It is well known that the threshold voltage changes as process and temperature change. Since transistors are biased with constant voltages, operating regions of transistors changes when process and temperature change. This phenomenon makes the g_{m3} cancellation scheme very sensitive to these variations. Also, the g_{m3} cancellation is only valid for small input signals. As shown in Fig. 2.11, the linear voltage region is narrow and determines how much power the Derivative Superposition method can handle. In previous works, the g_{m3} cancellation method may be useful for signals under -25dBm input power.

2.5 Proposed Approach

In this section, the constant current biasing is examined to make the Derivative Superposition method more stable under the conditions with process and temperature variations. Also, the Derivative Superposition method using the triode region and the sub-threshold region transistors is introduced.

2.5.1 Derivative Superposition Method with Constant Current Biasing

The main issue in the previous scheme is that it is sensitive to PVT variations because the transistors are voltage biased. To resolve this, each transistor for the Derivative Superposition method should be biased with a constant current as shown in Fig. 2.12. M_m and M_S are biased such that M_m operates in the saturation region and M_S in the sub-threshold region. The constant current biasing is also applied to the cascode transistor, M_1.

Because the constant current biasing tracks the threshold voltage variation caused by process and temperature variations, the sum of g_{m3} of M_m and g_{m3} of M_S does not vary significantly. Thus, this method improves the stability of the Derivative Superposition method over variations.

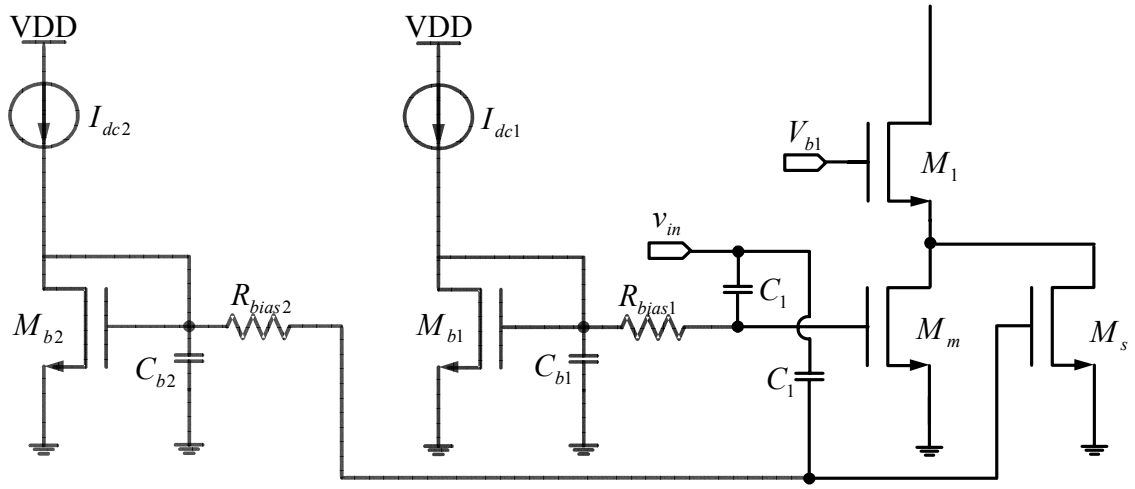


Fig. 2.12 Linearized LNA Core with Constant Current Biasing

The plot at the top of Fig. 2.13 shows g_{m3} for a single transistor as a function of the bias current with different corners and temperatures. Fast-Best (FF) stands for the Fast corner and -25 °C, Typical-Normal (TT) for the Typical corner and 65 °C, and Slow-Worst (SS) for the Slow corner and 100 °C.

As we can see in Fig. 2.13, the g_{m3} cancellation occurs at the certain bias current region for FF, TT, and SS cases. It is found that this "sweet region" covers all process corners and temperatures. Thus, the constant current biasing provides the robust g_{m3} cancellation over PVT variations.

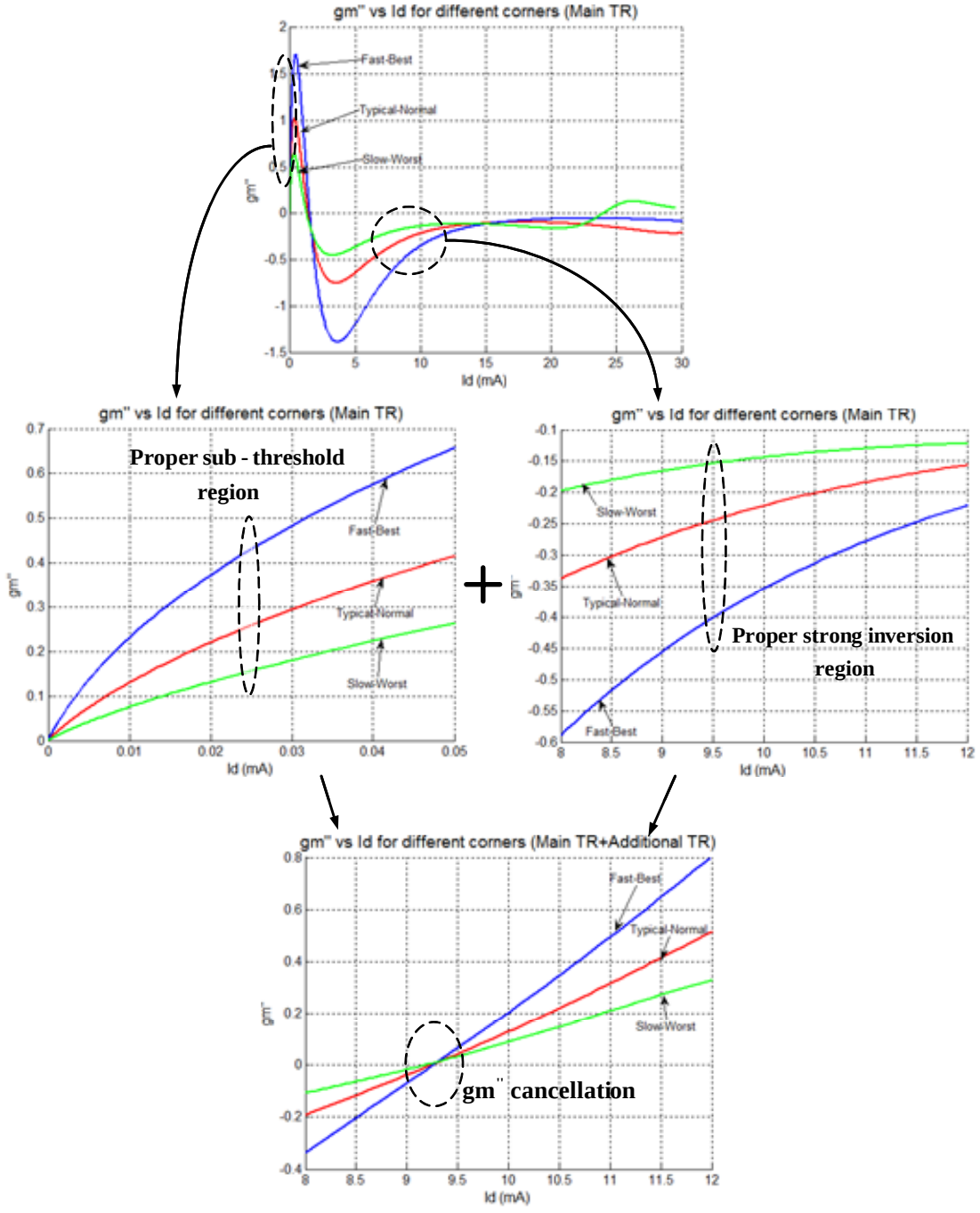


Fig. 2.13 Robust Second Order Derivative of g_m Cancellation for Different Corners

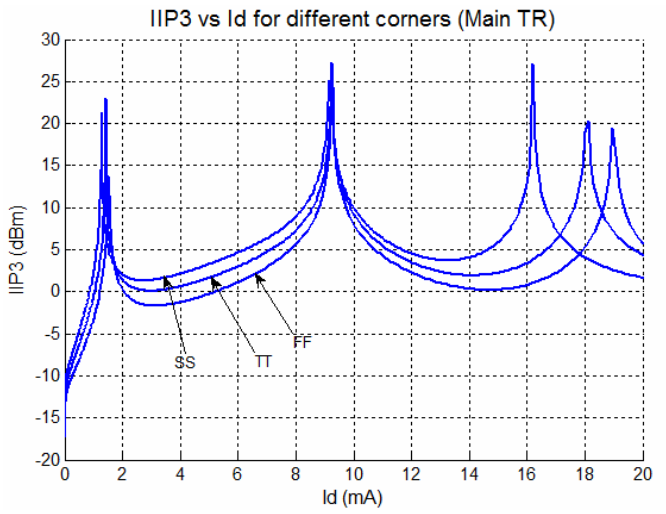


Fig. 2.14 IIP3 (DC Analysis)

Fig. 2.14 shows that the IIP3 performance at low frequencies. This graph is obtained using equation (2-9). Fig. 2.14 indicates that the sweet region for high IIP3 exists for all corners. Therefore, we can guarantee the linearity performance with the specific bias current. The best bias current can be obtained from different corner simulations as depicted in Fig. 2.13.

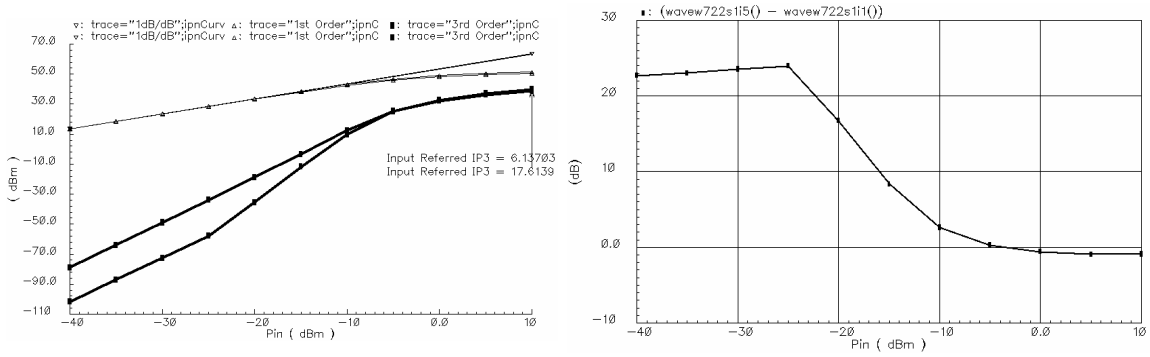


Fig. 2.15 IIP3 and IM3 Power Reduction Simulation Result Comparison between Conventional and Linearized LNA

Fig. 2.15 shows IIP3 and IM3 power simulation results for the LNA with the proposed linearization method shown in Fig. 2.12 and the LNA without the linearization method. When the linearization method is applied, IIP3 increases by 11dB and IM3 power reduction reaches over 20dB until -25dBm power input. IM3 power reduction decreases as input power increases. For over -10dBm input power, the linearization method is no longer valid. This is because the g_m cancellation method only supports limited input power. In other words, if the input voltage is larger than the linear voltage region, IIP3 performance starts to degrade. As the input voltage increases, the IIP3 degradation increases.

2.5.2 Using Triode Region Transistor for Derivative Superposition Method

The conventional Derivative Superposition method has three major drawbacks. Firstly, it is not stable under process and temperature variations. This problem has been solved in the previous section using the constant current biasing. Secondly, the size of auxiliary transistor should be as large as that of the main transistor. Thus, the LNA frequency response suffers from the doubled input capacitance. Lastly, the conventional Derivative Superposition method could provide g_{m3} cancellation only for input power under -20dBm. This method does not work properly over -15dBm input power.

To overcome the remaining problems, a novel Derivative Superposition method is introduced. The fundamental concept is similar to the previous method, but introduction of a triode region transistor prompts a more robust g_{m3} cancellation.

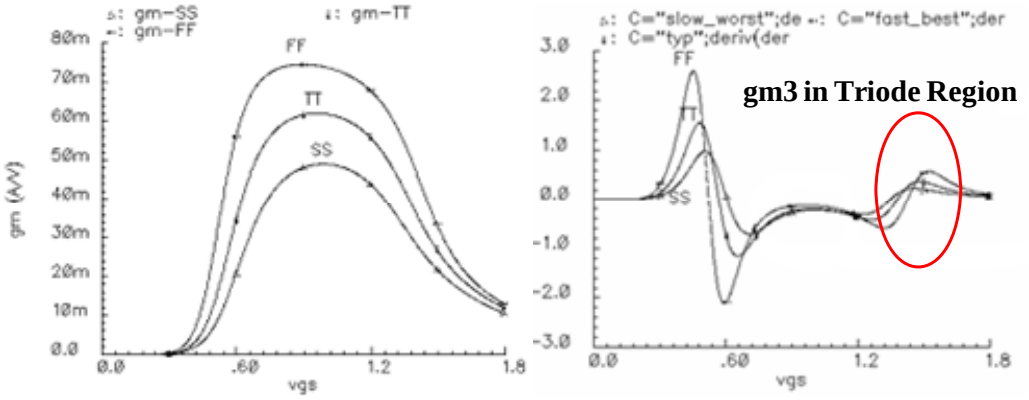


Fig. 2.16 Positive g_{m3} of Triode Region Transistor

Fig. 2.16 shows the g_m and the g_{m3} of a MOSFET transistor. As shown in the first plot of Fig. 2.16, the g_m reduces as a transistor goes into the triode region. If the gate-source voltage is further increased, the g_m reduction rate decreases because the transistor enters the deep triode region. Combining the positive g_{m3} of the triode region transistor and the positive g_{m3} of the sub-threshold region transistor, the negative g_{m3} of the saturation region transistor can be cancelled out.

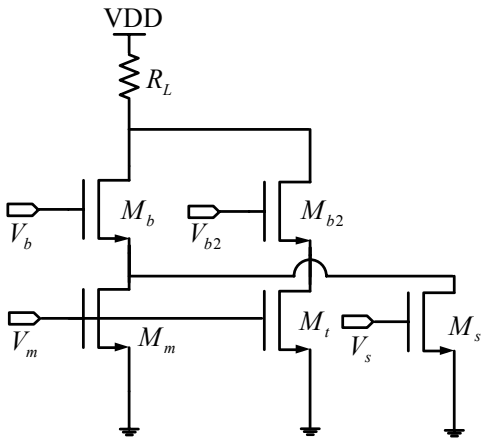


Fig. 2.17 Derivative Superposition Method with Triode Region Transistor

Fig. 2.17 shows the basic circuit implementation of this method. M_m, M_t, and M_s represent the saturation region, the triode region, and the sub-threshold region transistor respectively. Bias voltages for M_m and M_t are the same. M_s is biased in the sub-threshold region. The size and the bias point for M_m are determined by the LNA specification. M_m is usually biased such that its g_{m3} is negative. Although the bias voltage of M_t is the same as that of M_m, the cascode transistor M_{b2} forces M_t to operate in the triode region. Usually, g_{m3} of M_t is positive. This positive g_{m3} value is relatively large permitting the use of a small M_s to make the total g_{m3} equal to zero. On the other hand, M_{b2} also has another function. A triode region transistor has a low output impedance. M_{b2} protects M_t and provides a high impedance at the drain node of M_{b2}.

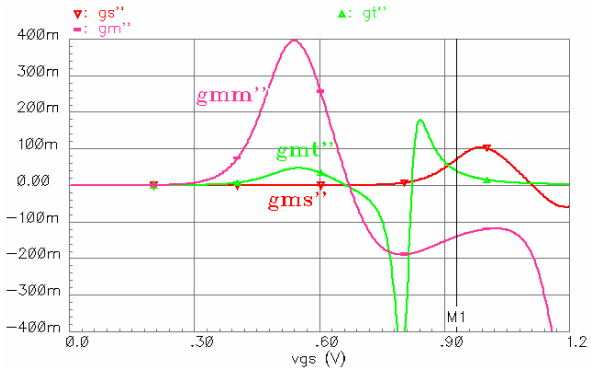


Fig. 2.18 g_{m3} of Transistors ($g''_{mm} - M_m$, $g''_{mt} - M_t$, g''_{ms} - M_s) and Operating Point (vs. Gate-Source Voltage)

Fig. 2.18 shows g_{m3} of each transistor. The negative value of g''_{mm} is canceled by the sum of g''_{mt} and g''_{ms} which are positive values. The size and the operating point of M_t and M_s are adjusted such that the sum of g_{m3} of M_t and M_s cancel out g_{m3} of M_m.

The total g_{m3} is shown in Fig. 2.19. The cancellation method works for an input signal range over 200mV around the operating point. Considering that the previous Derivative Superposition method only works for the very narrow input range, less than 50mV, this method can handle higher input signal power.

Moreover, the conventional Derivative Superposition method requires that the size of M_s be more than 70% of the size of the main transistor. However, in the proposed approach, the sum of the sizes of M_t and M_s is about 40% of the size of the main transistor. Therefore, the additional transistors do not degrade the LNA frequency response. This is another benefit of this method.

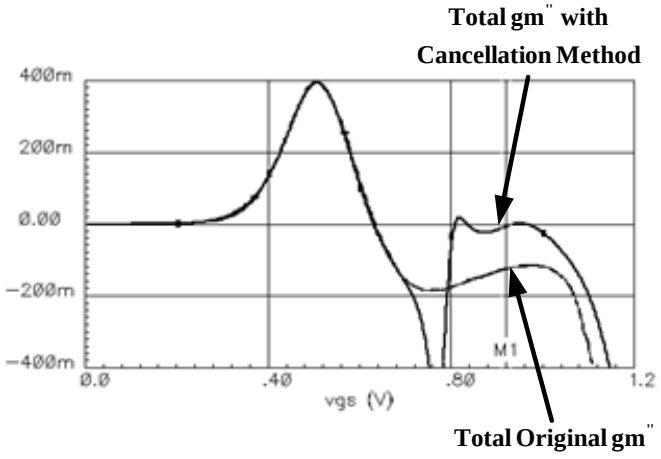


Fig. 2.19 Total Second Order Derivative of g_m (with and w/o Cancellation Technique)

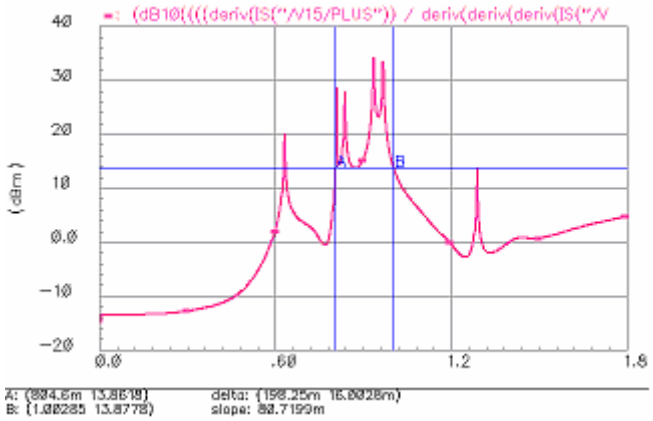


Fig. 2.20 DC Characteristic IIP3

Fig. 2.20 shows the IIP3 performance based on Fig. 2.19. It shows 200mV voltage range around the MOSFET operating point for over 14dBm IIP3. Compared to the previous method which provided 50mV voltage range for the same IIP3, the proposed method improves the input power handling capability of the LNA.

2.5.3 Proposed Derivative Superposition Method with Constant Current Biasing

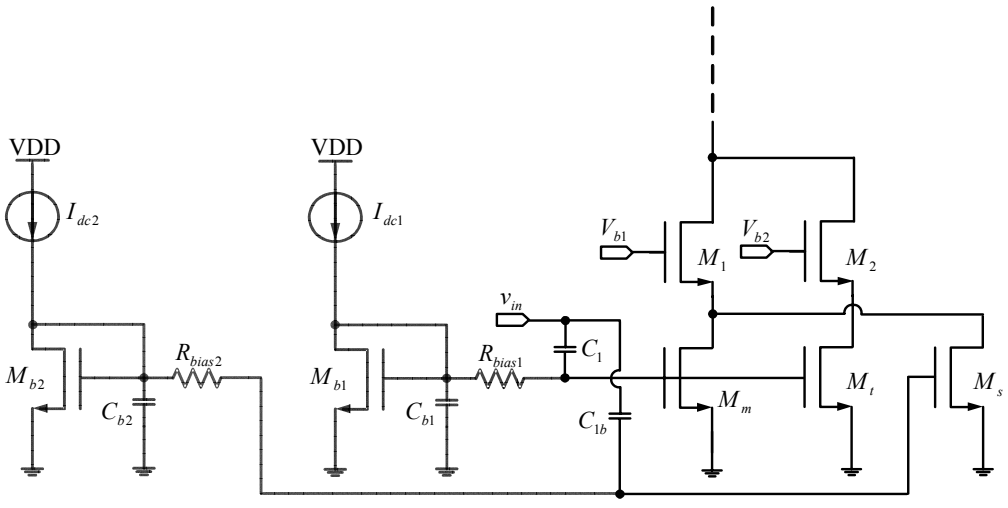


Fig. 2.21 Proposed Derivative Superposition Method with Constant Current Biasing

The proposed solution using constant current biasing circuitry is depicted in Fig. 2.21. Biasing currents are selected to cancel g_{m3} as much as possible and to simultaneously provide a wide linear voltage range to support the large input signal power. M_{b1} and M_{b2} are also biased with constant currents. By using this method, the bias voltages track process and temperature variations and provide robust g_{m3} cancellation.

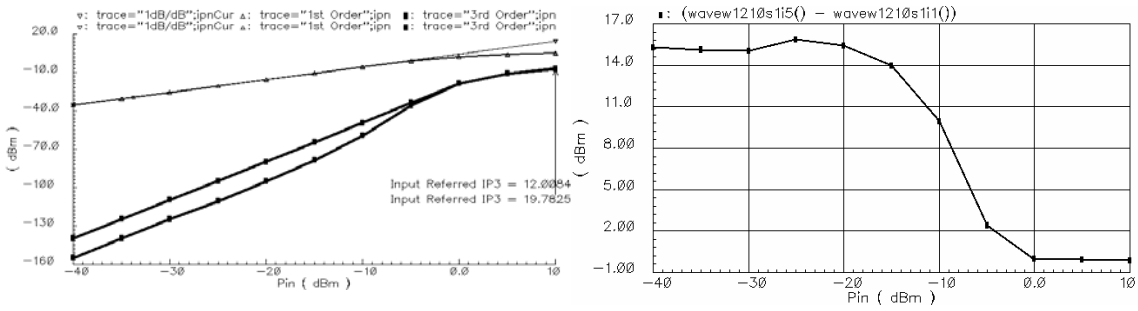


Fig. 2.22 IIP3 and IM3 Power Reduction Simulation Result Comparison between Conventional and Linearized LNA

Fig. 2.22 shows that the proposed linearization method is effective up to -10dBm input power. Compared to the result of Fig. 2.15 which provides linearization up to -20dBm, the proposed approach can handle 10dB higher input power. This is a significant improvement in terms of input power handling capability.

CHAPTER III

A HIGHLY LINEAR BROADBAND LNA

3.1 Design Considerations

Power Gain, Noise Figure and linearity are important for the design of a broadband LNA. The RF front-end system can be described as a cascade of blocks depicted in Fig. 3.1.

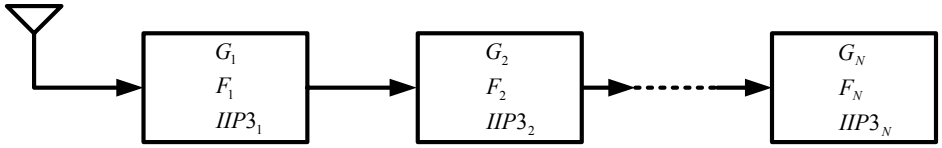


Fig. 3.1 Simplified RF front-end diagram

The total Noise Figure is then expressed by the following equation.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \tag{3-1}$$

where G_i and F_i represent the power gain and the noise factor of the ith block respectively. The total IIP3 can be expressed with the following equation.

$$\frac{1}{A_{IIP3}^2} \approx \frac{1}{A_{IIP3,1}^2} + \frac{G_1^2}{A_{IIP3,2}^2} + \frac{G_1^2 G_2^2}{A_{IIP3,3}^2} + \ldots + \frac{\prod_{n=1}^{N-1} G_n^2}{A_{IIP3,N}^2} \tag{3-2}$$

where $A_{IIP3,i}^2$ is the power level representing the input intercept point. Then, IIP3 can be described as equation (3-3).

$$IIP3_i = 10\log\left(A_{IP3,i}^2 / R_S\right) \tag{3-3}$$

where R_S is the source impedance.

According to equation (3-1), it is obvious that the first block should have a low Noise Figure to minimize total noise. The Noise Figure of the second block is divided by the power gain of the first block. The noise generated by the third block is divided by the product of the power gain of the first block and the second block, and so on. Therefore, a very low noise with a proper power gain is the first block requirement.

Equation (3-2) indicates that the IIP3 of the last block is the most important factor in a highly linear system because the input signal power of the last block is usually amplified by the power gain of previous blocks. Thus, the last block must handle high power signals without distortion. However, the IIP3 of the first block remains important. In a broadband RF front-end system, the IIP3 of the first block is critical to the linearity performance of the whole receiver chain.

For a narrowband LNA, a bandpass filter with a very narrow pass band eliminates interferers close to the main signal. Furthermore, an inductive source degeneration narrowband LNA itself performs like a filter. It is designed to amplify signals for a very small frequency range. Signals with other frequencies are filtered out. The input parasitic capacitance, C_{gs}, and the source degeneration inductor, L_s, have resonant frequency. The LC-tank at the drain node is designed to have the same resonant frequency [21]. L_s C_{gs} network and the LC-tank at the drain node determine the quality factor of the filter. If the filtering is sharp enough to filter out interferers close to the

desired channel, the interferers do not interrupt the main signal recovery process. However, a broadband LNA should be highly linear to prevent image signal generation. If generated, image signals may fall into the main signal frequency range and act as interferers as shown in Fig. 1.4.

Thus, a broadband LNA should have very high IIP3 performance and a reasonable Noise Figure across all frequencies. Meanwhile, S11 should be kept below -10dB for the frequency band of interest. The LNA specifications are listed in Table 3-1.

Table 3-1 Target Specifications for Highly Linear Broadband LNA

Technology	65nm CMOS
Power Supply	2.4 V
Bandwidth	> 5GHz
Input Impedance	50 Ω
IIP3	> 15dBm
Gain	> 10 dB
Noise Figure (NF)	< 4.5 dB
S_{11}	-10 dB

3.2 Design of Highly Linear Broadband LNA

3.2.1 Topology Selection

For broadband applications, a broadband impedance matching is indispensible. To meet a wide frequency range impedance matching, the common-gate topology and the resistive feedback topology are usually preferred. The common-source topology with 50Ω termination at the gate is not considered a solution because the termination resistor itself degrades the Noise Figure by 3dB.

3.2.1.1 Common-Gate Topology

The simplified common-gate topology is depicted in Fig. 3.2 as well as its small signal model.

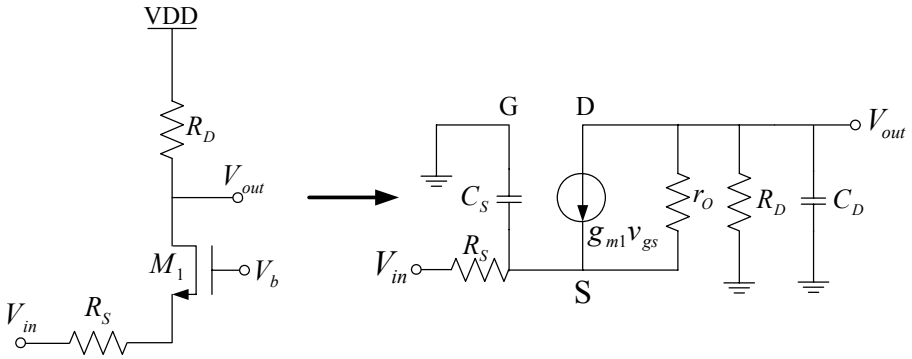


Fig. 3.2 Common-Gate Topology and Small Signal Model

M_1 is a NMOS transistor, R_S is a source impedance, and R_D is a load resistor. g_{m1} is the transconductance of M1 and r_O is the output impedance of M1. C_S and C_D represent the source node parasitic capacitance of M_1 and the drain node parasitic capacitance respectively. Using this model, the input impedance is

$$Z_{in} \cong \frac{1}{sC_S} \left\| \left(\frac{R_D \,\|\, 1/sC_D}{g_{m1} r_O} + \frac{1}{g_{m1}} \right) \right. . \tag{3-4}$$

The DC voltage gain of the common-gate topology is

$$G = \left(g_{m1} + \frac{1}{r_O} \right) \left(R_D \,\|\, r_O \right) . \tag{3-5}$$

Equation (3-6) shows the location of the dominant pole.

$$p_1 \cong \frac{1}{C_D\left[R_D \parallel \left(r_O + R_S + g_m r_O R_S\right)\right]} \tag{3-6}$$

Through consideration of the required voltage gain, the input impedance, and the 3dB bandwidth, g_{m1} and R_D have been obtained. These can be adjusted through simulations for 50Ω input impedance matching. This method provides a decent input impedance matching for the wide frequency range. However, the noise performance is the main drawback of this topology. From [22], the Noise Figure of the common-gate LNA is given in equation (3-7).

$$F \approx 1 + \left(\frac{\gamma}{\alpha}\right)\left(\frac{r_O}{r_O + R_D}\right) \tag{3-7}$$

where $\alpha = g_{m1} / g_{d0}$ is the ratio of the transistor transconductance to the channel conductance at zero V_{ds} and γ is the channel thermal noise coefficient which is in the range of 1 ~ 2. Assuming $r_O >> R_D$, equation (3-7) can be simplified as

$$F \approx 1 + \left(\frac{\gamma}{\alpha}\right). \tag{3-8}$$

For long channel devices, γ / α is small. Typically, the Noise Figure is 3dB or higher. However, short channel devices in deep sub-micron technology, such as 65nm CMOS technology, have higher γ causing the Noise Figure of the simple common-gate topology to be over 4.5dB without noise from bias circuits. If the noise of bias circuits is added, the Noise Figure for this topology can easily reach over 5dB. Because of the

limited Noise Figure performance, the common-gate topology is not selected as an LNA topology for this thesis.

3.2.1.2 Resistive Feedback Topology

The simplified resistive feedback topology and its low frequency small signal model are depicted in Fig. 3.3.

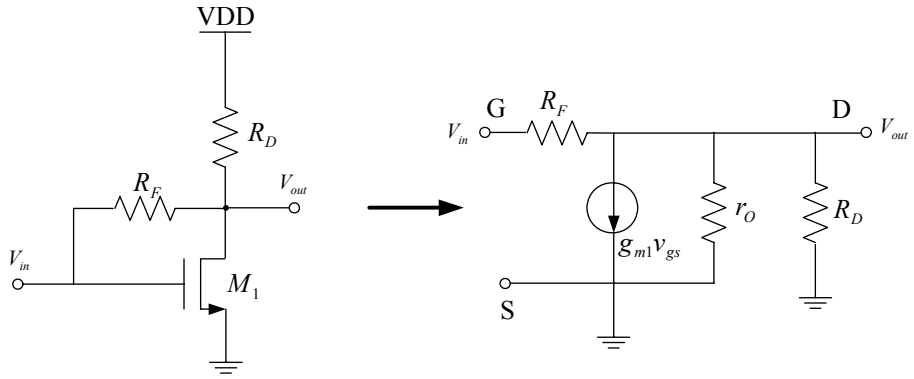


Fig. 3.3 Resistive Feedback Topology and Small Signal Model

M_1 is an NMOS transistor, R_D is the load resistor, R_F is the feedback resistor, g_{m1} is the transconductance of M1, and r_O is the output impedance of M1. The negative feedback resistor provides the real impedance that can be used for input impedance matching. The feedback resistance is divided by the voltage gain of the amplifier to provide the input 50Ω impedance matching. This topology provides a wide bandwidth input impedance matching. Moreover, due to the local feedback provided by R_F, this topology shows better linearity compared to the common-gate topology. The noise

performance mostly depends on the values of g_{m1} and the feedback resistor. Thus, this topology is selected for a highly linear broadband LNA.

3.2.2 Resistive Feedback Topology Analysis

In this section, characteristics of the resistive feedback topology are analyzed including a small signal model analysis, a frequency response, an input impedance matching, the Noise Figure calculation, and the volterra series analysis for linearity.

3.2.2.1 Small Signal Model Analysis of the Resistive Feedback Topology

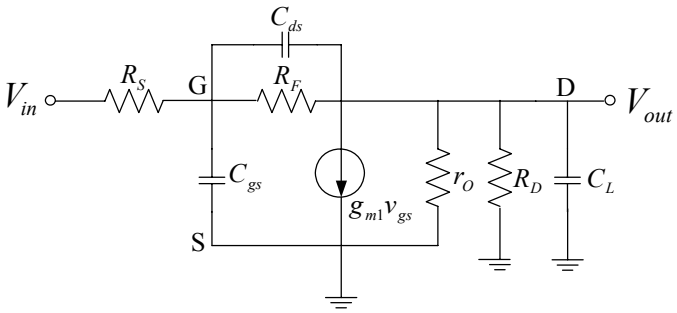


Fig. 3.4 Small Signal Model of Resistive Feedback Topology

A small signal model is depicted in Fig. 3.4 [23]. The source impedance R_S, usually 50Ω, is added. The gate-source parasitic capacitance, C_{gs}, the gate-drain parasitic capacitance, C_{gd}, and the load capacitor, C_L, are also included in the model for more accurate analysis. Assuming $r_O >> R_D$, two equations can be derived using KCL.

$$(V_G - V_{out})(g_F + sC_{gd}) = V_G \cdot g_{m1} + V_{out}(g_D + sC_L) \tag{3-9}$$

$$(V_{in} - V_G)g_S = V_G \cdot sC_{gs} + (V_G - V_{out})(g_F + sC_{gd}) \tag{3-10}$$

where V_G represents the voltage at the gate node. From the previous two equations, the small signal gain can be obtained as equation (3-11).

$$\frac{V_{out}}{V_{in}} = \frac{g_S(g_F - g_{m1} + sC_{gd})}{As^2 + Bs + C} \tag{3-11}$$

where $A = C_{gs}C_{gd} + C_{gs}C_L + C_{gd}C_L$,

$B = C_{gd}(g_S + g_{m1} + g_D) + C_{gs}(g_F + g_D) + C_L(g_S + g_F)$, $C = g_S g_D + g_F(g_{m1} + g_D + g_S)$.

3.2.2.2 Frequency Response

From equation (3-11), the DC gain can be obtained by setting $s = 0$.

$$A_v = \frac{g_S(g_F - g_{m1})}{g_S g_D + g_F(g_{m1} + g_D + g_S)} \tag{3-12}$$

Assuming that $g_{m1}R_F >> 1$, we can rewrite this equation as

$$A_v = \frac{R_D(1 - g_{m1}R_F)}{(R_D + R_F + R_S + g_{m1}R_D R_S)} \approx \frac{-g_{m1}R_F R_D}{(R_D + R_F + R_S + g_{m1}R_D R_S)}. \tag{3-13}$$

From equation (3-11), this system consists of two poles and one zero. We can find the first pole from equation (3-11), which determines the -3dB bandwidth. Although all coefficients in the denominator of equation (3-11) seem significant, the second order coefficient, $C_{gs}C_{gd} + C_{gs}C_L + C_{gd}C_L$, is much smaller than the first order coefficient, $C_{gd}(g_S + g_{m1} + g_D) + C_{gs}(g_F + g_D) + C_L(g_S + g_F)$, and the zero order coefficient

$g_S g_D + g_F(g_{m1} + g_D + g_S)$. This is because the parasitic capacitance and the load capacitor are order of $10^{-15} \sim 10^{-12}$ while transconductance, such as g_S, g_{m1}, g_D, g_F, is order of 10^{-3}. Because the second order term can be ignored, we can assume that the second pole is far enough away from the first pole that its existence is negligible. The first pole is given as

$$\omega_{p1} = \frac{g_S g_D + g_F(g_{m1} + g_D + g_S)}{C_{gd}(g_S + g_{m1} + g_D) + C_{gs}(g_F + g_D) + C_L(g_S + g_F)}. \tag{3-14}$$

3.2.2.3 Input Impedance Matching

The low frequency input impedance can be calculated using the model in Fig. 3.5.

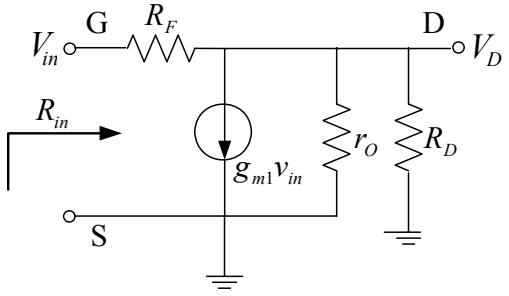


Fig. 3.5 Small Signal Model for Input Impedance

Using KCL, equation (3-15) can be obtained.

$$(V_{in} - V_D)g_F = I_{in} = V_{in}g_{m1} + V_D(g_O + g_D) \tag{3-15}$$

From, equation (3-15), R_{in} can be calculated.

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{1}{\left(1 - \frac{g_F - g_{m1}}{g_O + g_F + g_D}\right)g_F} = \frac{g_O + g_F + g_D}{(g_O + g_{m1} + g_D)g_F} \tag{3-16}$$

Assuming $g_{m1} >> g_D, g_O$,

$$R_{in} = \frac{1}{g_{m1}}\left(\frac{R_F}{R_F \parallel r_O \parallel R_D}\right). \tag{3-17}$$

Equation (3-17) represents the low frequency input impedance. The high frequency input impedance can be obtained considering C_{gs} and C_{ds}.

$$Z_{in} = R_{in} \Big\| \frac{1}{sC_{gs}} \tag{3-18}$$

Therefore, using R_F and R_D and the given g_{m1}, the input impedance can be controlled.

3.2.2.4 Noise Analysis

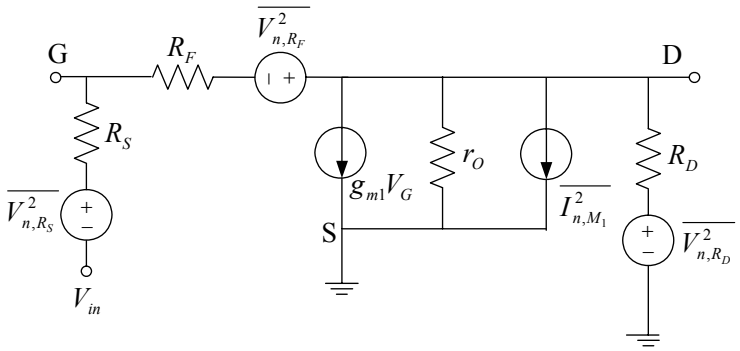


Fig. 3.6 Noise Model

If the gate noise is ignored, the amplifier's noise model can be described as shown in Fig. 3.6. Using the superposition theory, all output noise voltages are added. The total output noise voltage can be referred to the input by dividing it by the voltage gain. In the following analysis, $r_O >> R_D$ is assumed.

From M_1, the noise current $\overline{I_{n,M1}^2} = 4kT\gamma g_{m1}$ generates the output noise voltage.

$$\overline{V_{n,out,M1}^2} = \left(\frac{R_D\left(R_S + R_F\right)}{R_S + R_F + R_D + g_{m1}R_S R_D} \right)^2 4kT\gamma g_m \tag{3-19}$$

From R_D, the noise voltage $\overline{V_{n,R_D}^2} = 4kTR_D$ generates the output noise voltage.

$$\overline{V_{n,out,R_D}^2} = \left(\frac{R_S + R_F}{R_S + R_F + R_D + g_{m1}R_S R_D} \right)^2 4kTR_D \tag{3-20}$$

From R_F, the noise voltage $\overline{V_{n,R_F}^2} = 4kTR_F$ generates the output noise voltage.

$$\overline{V_{n,out,R_F}^2} = \left(\frac{R_D\left(1 + g_{m1}R_S\right)}{R_S + R_F + R_D + g_{m1}R_S R_D} \right)^2 4kTR_F \tag{3-21}$$

Thus, the total output noise voltage becomes

$$\overline{V_{n,out,total}^2} = \overline{V_{n,out,M1}^2} + \overline{V_{n,out,R_D}^2} + \overline{V_{n,out,R_F}^2} \,. \tag{3-22}$$

The output noise voltage can be referred to the input by dividing it by voltage gain which was obtained in equation (3-13). The source resistor noise voltage $\overline{V_{n,R_S}^2} = 4kTR_S$ is also included. Thus, the total input referred noise voltage is described as

$$\overline{V_{n,in,total}^2} = \overline{V_{n,R_S}^2} + \frac{\overline{V_{n,out,M1}^2} + \overline{V_{n,out,R_D}^2} + \overline{V_{n,out,R_F}^2}}{A_v^2} \tag{3-23}$$

$$\begin{aligned} \overline{V_{n,in,total}^2} &= 4kT\left\{ R_S + \left(\frac{R_S + R_F}{g_{m1}R_F} \right)^2 \gamma g_{m1} + \left(\frac{R_S + R_F}{g_{m1}R_D R_F} \right)^2 R_D + \left(\frac{1 + g_{m1}R_S}{g_{m1}R_F} \right)^2 R_F \right\} \\ &\approx 4kT\left\{ R_S + \gamma \frac{1}{g_{m1}} \left(1 + \frac{R_S}{R_F} \right)^2 + \frac{1}{g_{m1}^2 R_D} \left(1 + \frac{R_S}{R_F} \right)^2 + R_S \left(\frac{R_S}{R_F} \right) \right\} \end{aligned} \tag{3-24}$$

where $g_{m1}R_S >> 1$.

From equation (3-24), the Noise Factor can be obtained as

$$F = 1 + \gamma \frac{1}{g_{m1}R_S}\left(1 + \frac{R_S}{R_F}\right)^2 + \frac{1}{g_{m1}^2 R_D R_S}\left(1 + \frac{R_S}{R_F}\right)^2 + \left(\frac{R_S}{R_F}\right)$$
$$\approx 1 + \frac{\gamma}{g_{m1}R_S} + \frac{1}{g_{m1}^2 R_D R_S} + \frac{R_S}{R_F} \qquad (3\text{-}25)$$

where $R_F >> R_S$.

Equation (3-25) indicates that the Noise Factor is a strong function of g_{m1}, R_F, and γ. For the low noise application, both g_{m1} and R_F should be increased. However, the value of g_{m1} is limited by the power consumption specification and the supply voltage. The value of R_F is limited by the input impedance matching condition which is also related to R_D and the supply voltage limitation. Usually, short channel devices have higher γ value than long channel devices. Scaling down to the deep sub-micron technologies would provide a wider bandwidth at the cost of the noise performance degradation.

3.2.2.5 Linearity of Resistive Feedback Topology

The linearity of the resistive feedback topology is analyzed using the volterra series. Fig. 3.7 describes the small signal model for the volterra series analysis

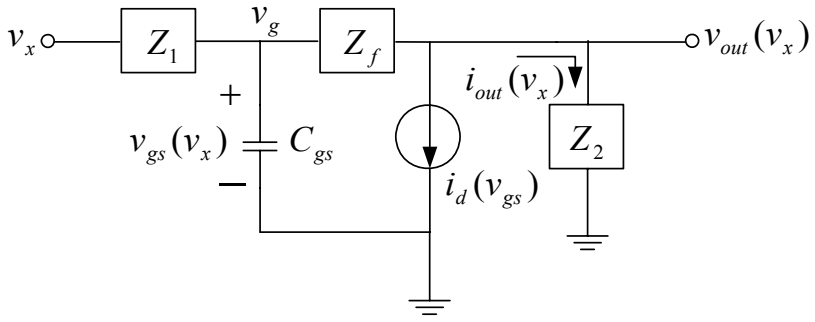


Fig. 3.7 Small Signal Model for Volterra Series Analysis

Through [24] and consideration of the non-linearity of g_m, $i_d(v_{gs})$ can be described as

$$i_d(v_{gs}) = g_1 \cdot v_{gs} + g_2 \cdot v_{gs}^2 + g_3 \cdot v_{gs}^3 \tag{3-26}$$

where g_1, g_2, and g_3 represent g_m, the first order derivative of g_m, and the second order derivative of g_m respectively. Similarly, $v_{gs}(v_x)$, and $i_{out}(v_x)$ can be described in the following equations.

$$v_{gs}(v_x) = A_1(s) \circ v_x + A_2(s_1, s_2) \circ v_x^2 + A_3(s_1, s_2, s_3) \circ v_x^3 \tag{3-27}$$

$$i_{out}(v_x) = C_1(s) \circ v_x + C_2(s_1, s_2) \circ v_x^2 + C_3(s_1, s_2, s_3) \circ v_x^3 \tag{3-28}$$

where operator ∘ represents the volterra operation which has different magnitudes and phases for different frequencies. For example, $A \circ H(s) = A \cdot |H(s)| \cdot \angle H(s)$.

The non-linear currents can be explained by using KCL at the output node.

$$\frac{v_{gs}(v_x) - v_{out}(v_x)}{Z_f(s)} = \frac{v_{gs}(v_x) - i_{out}(v_x) \cdot Z_2(s)}{Z_f(s)} = i_d(v_{gs}) + i_{out}(v_x) \tag{3-29}$$

$$v_{gs}(v_x) - i_d(v_{gs}) \cdot Z_f(s) = i_{out}(v_x)\big(Z_2(s) + Z_f(s)\big) \tag{3-30}$$

$$i_{out}(v_x) = \frac{v_{gs}(v_x) - i_d(v_{gs}) \cdot Z_f(s)}{Z_2(s) + Z_f(s)} \tag{3-31}$$

$$\begin{aligned} & C_1(s) \circ v_x + C_2(s_1, s_2) \circ v_x^2 + C_3(s_1, s_2, s_3) \circ v_x^3 = \\ & \frac{1 - Z_f(s) \cdot g_1}{Z_2(s) + Z_f(s)} \left[A_1(s) \circ v_x + A_2(s_1, s_2) \circ v_x^2 + A_3(s_1, s_2, s_3) \circ v_x^3 \right] \\ & - \frac{Z_f(s) \cdot g_2}{Z_2(s) + Z_f(s)} \left[A_1(s) \circ v_x + A_2(s_1, s_2) \circ v_x^2 + A_3(s_1, s_2, s_3) \circ v_x^3 \right]^2 \\ & - \frac{Z_f(s) \cdot g_3}{Z_2(s) + Z_f(s)} \left[A_1(s) \circ v_x + A_2(s_1, s_2) \circ v_x^2 + A_3(s_1, s_2, s_3) \circ v_x^3 \right]^3 \end{aligned} \tag{3-32}$$

Then, $C_1(s)$ and $C_3(s_1, s_2, s_3)$ can be found by the equations below.

$$C_1(s) = \frac{1 - Z_f(s) \cdot g_1}{Z_2(s) + Z_f(s)} \cdot A_1(s) \tag{3-33}$$

$$\begin{aligned} C_3(s_1, s_2, s_3) = & \frac{1 - Z_f(s_1 + s_2 + s_3)}{Z_2(s_1 + s_2 + s_3) + Z_f(s_1 + s_2 + s_3)} \cdot g_1 A_3(s_1, s_2, s_3) \\ & - \frac{2 \cdot Z_f(s_1 + s_2 + s_3) \cdot g_2 \cdot \overline{A_1(s_1) \cdot A_2(s_2, s_3)}}{Z_2(s_1 + s_2 + s_3) + Z_f(s_1 + s_2 + s_3)} \\ & - \frac{Z_f(s_1 + s_2 + s_3) \cdot g_3 \cdot A_1(s_1) \cdot A_1(s_2) \cdot A_1(s_3)}{Z_2(s_1 + s_2 + s_3) + Z_f(s_1 + s_2 + s_3)} \end{aligned} \tag{3-34}$$

Using KCL at the gate node and at the output node, $A_1(s)$, $A_2(s_1, s_2)$, and $A_3(s_1, s_2, s_3)$ can be obtained.

$$A_1(s) = \frac{1}{1 + sC_{gs} \cdot Z_1(s) + \frac{Z_1(s)}{Z_f(s) + Z_2(s)} + \frac{Z_1(s) \cdot Z_2(s)}{Z_f(s) + Z_2(s)} \cdot g_1} \tag{3-35}$$

$$A_2(s_1, s_2) = -A_1(s_1, s_2) \cdot \frac{Z_1(s_1 + s_2) \cdot Z_2(s_1 + s_2)}{Z_f(s_1 + s_2) + Z_2(s_1 + s_2)} \cdot g_1 \cdot A_1(s_1) \cdot A_1(s_2) \tag{3-36}$$

$$A_3(s_1,s_2,s_3) = -A_1(s_1,s_2,s_3)\cdot\frac{Z_1(s_1,s_2,s_3)\cdot Z_2(s_1,s_2,s_3)}{Z_f(s_1,s_2,s_3)+Z_2(s_1,s_2,s_3)} \cdot\left[2g_2\cdot\overline{A_1(s_1)\cdot A_2(s_2,s_3)}+g_3\cdot A_1(s_1)\cdot A_1(s_2)\cdot A_1(s_3)\right] \tag{3-37}$$

where $\overline{A_1(s_1)\cdot A_2(s_2,s_3)} = \frac{1}{3}\{A_1(s_1)\cdot A_2(s_2,s_3)+A_1(s_2)\cdot A_2(s_1,s_3)+A_1(s_3)\cdot A_2(s_1,s_2)\}$.

Since the input consists of two tones very close to each other for the intermodulation distortion test, $s_a \approx s_b \approx s$, $s_b - s_a = \Delta s \approx 0$ are assumed. Then,

$$A_3(s_b,s_b,-s_a) = -A_1(s)^2\cdot|A_1(s)|^2\cdot\frac{Z_1(s)\cdot Z_2(s)}{Z_f(s)+Z_2(s)}\left[g_3-\frac{2}{3}g_2^2\cdot(2\cdot\kappa(\Delta s)+\kappa(2s))\right] \tag{3-38}$$

where $\kappa(s) = A_1(s)\cdot\frac{Z_f(s)\cdot Z_2(s)}{Z_f(s)+Z_2(s)}$. Now, by inserting equations (3-35), (3-36), and (3-38) into equation (3-34), we can obtain equation (3-39).

$$C_3(s_b,s_b,-s_a) = \frac{Z_f(s)}{Z_f(s)+Z_2(s)}A_1(s)^2\cdot|A_1(s)|^2\cdot\left[1+sC_{gs}Z_1(s)+\frac{Z_1(s)}{Z_f(s)}\right] \cdot\left[\frac{2}{3}g_2^2\cdot\{2\cdot\kappa(\Delta s)+\kappa(2s)\}-g_3\right] \tag{3-39}$$

IIP3 can be described as

$$A_{IIP3}(2\omega_b-\omega_a) = \sqrt{\frac{4}{3}\left|\frac{C_1(s_a)}{C_3(s_b,s_b,-s_a)}\right|}. \tag{3-40}$$

If we change this value to IIP3,

$$IIP3(2\omega_b-\omega_a) = \frac{A_{IIP3}(2\omega_b-\omega_a)^2}{\Re(Z_1(s_a))} = \frac{4}{3\Re(Z_1(s_a))}\left|\frac{C_1(s_a)}{C_3(s_b,s_b,-s_a)}\right| = \frac{4}{3\Re(Z_1(s_a))}\frac{1}{\left|A_1(s)^3\right|\cdot|H(s)|\cdot|\varepsilon(\Delta s,2s)|} \tag{3-41}$$

where $H(s) = \dfrac{Z_1(s) + Z_f(s) + sC_{gs} \cdot Z_1(s) \cdot Z_f(s)}{1 - Z_f(s) \cdot g_1}$, $\Re(Z_1(s_a))$ represents the real part of the source impedance, usually 50Ω, and $\varepsilon(\Delta s, 2s) = \dfrac{2}{3} g_2^2 \cdot \{2 \cdot \kappa(\Delta s) + \kappa(2s)\} - g_3$.

Equation (3-41) indicates that $\varepsilon(\Delta s, 2s)$ should be minimized for high IIP3. To minimize $\varepsilon(\Delta s, 2s)$, not only g_3 but also g_2 and function $\kappa(s)$ should be considered. That is, the second order derivative of transconductance and the first order derivative of transconductance need to be selected properly to minimize $\varepsilon(\Delta s, 2s)$. In the case of a feedback system, the first order derivative of g_m also plays a role in determining IIP3. Each feedback system has its own $\kappa(s)$ which is determined through the feedback circuitry. Since designing $\varepsilon(\Delta s, 2s)$ equal to zero is hard to achieve, it is usually optimized through simulations.

3.2.3 Design Procedure for Linearized Resistive Feedback Broadband LNA

We can design the linearized resistive feedback LNA from the equations of the typical resistive feedback LNA. The required specifications are given in Table 3-2. Three specifications, the Noise Figure, the input impedance matching, and the voltage gain, are used for designing the LNA.

Table 3-2 Specifications for Highly Linear Broadband LNA

Gain	> 10 dB
Noise Figure (NF)	< 4 dB
S_{11}	-10 dB

From the three equations given below, we can calculate proper g_m, R_D, and R_F with the condition that $R_S = 50\Omega$. γ can be assumed to be 3 for the worst case.

$$A_v \approx \frac{-g_{m1}R_F R_D}{\left(R_D + R_F + R_S + g_{m1}R_D R_S\right)} \tag{3-42}$$

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{R_F + R_D}{1 + g_{m1}R_D} \tag{3-43}$$

$$F \approx 1 + \frac{\gamma}{g_{m1}R_S} + \frac{1}{g_{m1}^2 R_D R_S} + \frac{R_S}{R_F} \tag{3-44}$$

Solving the equations, we can obtain

$g_m = 80mA/V$, $R_F = 350\Omega$, $R_D = 100\Omega$

The selection of parameters is also limited by the supply voltage. In this case, the target supply voltage is 2.4V. Given g_m, the current for the main transistor is decided based on the constant current method introduced in section 2.4. Then, two additional transistors, one of which is working in the triode region and the other in the sub-threshold region, are attached to cancel the second order derivative of g_m. Because IIP3 is a function of the second order derivative of g_m and the first derivative of g_m, high IIP3 can be obtained from simulations on top of the initial design providing the best current combination for the main transistor, the triode region transistor, and the sub-threshold region transistor. The bandwidth of the LNA is also a major issue in the design. 100fF load capacitor is attached to emulate the parasitic capacitance of the next stage.

Although a minimum channel length device, 65nm, is available to use, the channel length is chosen as 280nm to sustain high voltages between terminals of transistors. This is because the LNA can be highly linear only with large V_{DS} voltage. The linearization method shown in Chapter II linearizes g_m and the small signal current generated by the main transsitor as shown in Fig. 3.8.

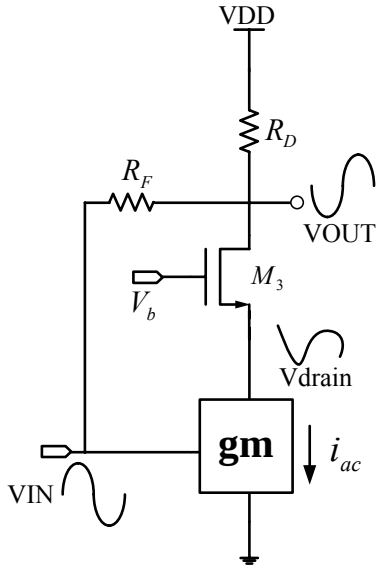


Fig. 3.8 Conceptual Diagram for Linearization

However, what is finally measured is the voltage swing at the VOUT node and the linearity of the voltage swing is determined by both g_m and R_{out} where R_{out} is the output impedance at the VOUT node. This means that not only g_m, but also R_{out} should be linear. Since the cascode device, M_3, provides the large output impedance, the output impedance at the VOUT node is mainly determined by R_D and R_F which are passive

and linear. However, if the drain voltage of the cascode transistor drops, the cascode impedance becomes smaller. Since the cascode impedance is small and non-linear, the total impedance at the VOUT node becomes non-linear. Consequently, the non-linear output impedance generates the non-linear output voltage swing. Thus, keeping the drain voltage of M_3 high enough to provide the large impedance is also important. Without using an inductor, the only way to keep the drain voltage of M_3 high enough is using the high supply voltage.

3.3 The Entire LNA Circuit

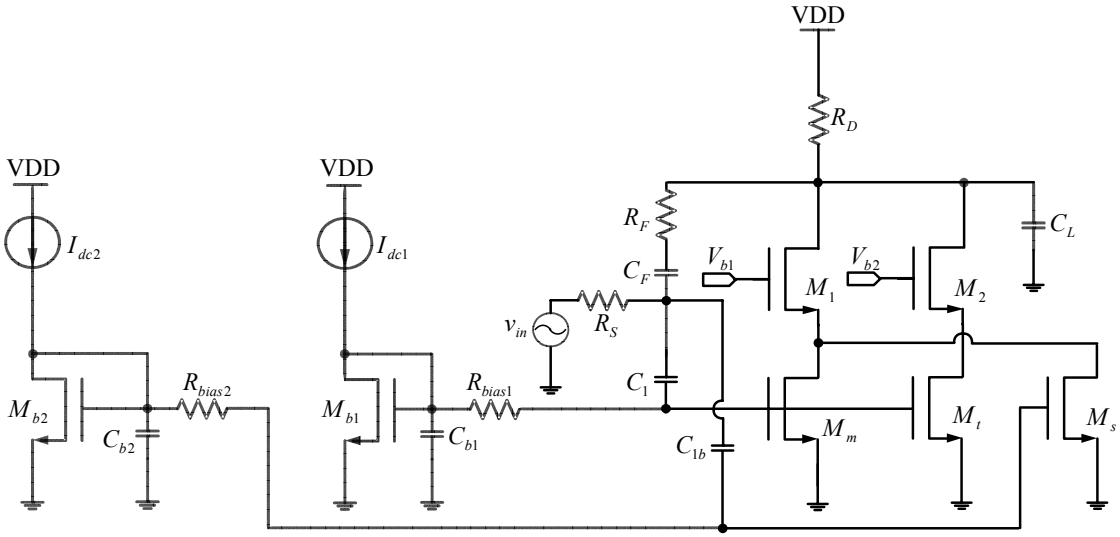


Fig. 3.9 The Entire LNA Circuit

The entire LNA circuit is shown in Fig. 3.9. All transistors are biased with the constant currents. The main transistor, M_m, works in the saturation region while M_t and

M_s work in the triode region and in the sub-threshold region respectively. The high frequency capacitors, such as C_F, C_{1b}, C_{b1}, and C_{b2}, are chosen as 10pF while the value of the load capacitor, C_L, is set to 100fF. Table 3-3 shows other design parameters. M_2 is biased such that M_t works in the triode region. This biasing circuit is not shown in Fig. 3.9. Values of R_F and R_D are adjusted by simulations for better linearity performance.

Table 3-3 Design Parameters

Technology	65nm CMOS Process
Supply Voltage	2.4V
M_m	12(5x3um/0.28um)
M_1	16(5x3um/0.28um)
M_t	2(4x3um/0.28um)
M_2	2(3um/0.28um)
M_s	2(8x3um/0.28um)
R_D	75Ω
R_F	320Ω
C_L	100fF
C_F, C_{1b}, C_{b1}, C_{b2}	10pF
I_{dc1}	10.8mA
$I_{dc\_M_t}$	1mA
I_{dc2}	0.1mA

All simulation results are presented in Chapter IV.

CHAPTER IV

SIMULATION RESULT

In this chapter, the simulation results of the resistive feedback broadband LNA are presented. The LNA was designed in 65nm CMOS technology. This chapter includes the LNA performance in normal case, the Typical process and 65°C. Then, the comparison between the conventional and linearized LNA is shown for the three corners: the Typical process and 65°C, Slow process and 100°C, and Fast process and -25°C. The simulation results for process, supply voltage, and temperature variations are also shown in this chapter. Lastly, the Monte Carlo simulation results are presented.

4.1 LNA Simulation Results

S-parameters are used for the simulations to find the power gain (S21), the input impedance matching (S11), and the Noise Figure (NF). The source impedance is assumed to be 50Ω. Through the two tone test simulation, IIP3 performance is measured. The center frequency is set to 1GHz and two tones at 1GHz and 1.005GHz .

Fig. 4.1 shows the S11 simulation result for the designed resistive feedback broadband LNA. S11 of -10dB is obtained for a wide frequency range. Above 2GHz, S11 is degraded mainly because the power gain of the designed amplifier decreases after 2GHz.

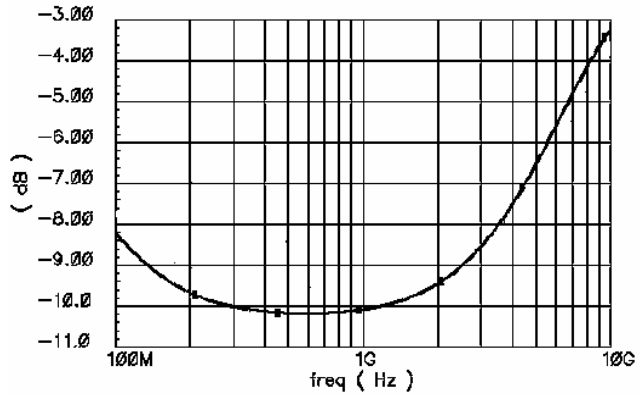


Fig. 4.1 S11 Simulation Result

Fig. 4.2 shows the S21 simulation result. The power gain of the designed amplifier is around 10dB at low frequencies. The power gain decreases after 2GHz.

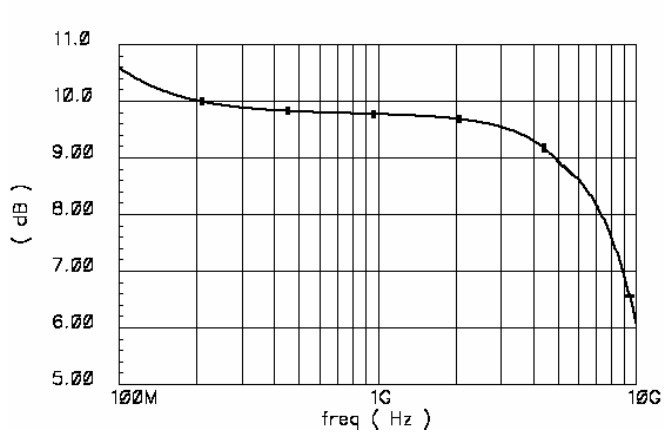


Fig. 4.2 S21 Simulation Result

Fig. 4.3 shows the Noise Figure simulation result. The Noise Figure of 4.6dB is obtained up to 1GHz. Again, degradation starts to occur after 2GHz where the power gain starts to decrease.

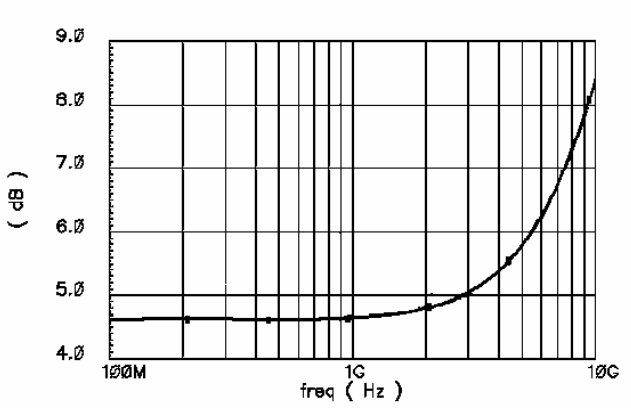


Fig. 4.3 Noise Figure Simulation Result

Fig. 4.4 shows the IIP3 simulation result of the designed amplifier. With the help of the linearization method, the IIP3 performance showed 19.2dBm.

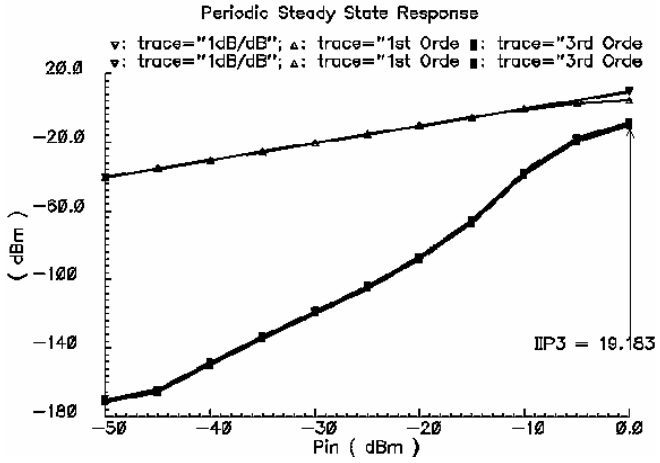


Fig. 4.4 IIP3 Simulation Result

Table 4-1 shows the summary of LNA performance. The simulation results of S11, S21, and NF are similar to the specifications provided in Table 3-1. IIP3 is around 19.2 dBm which is 4 dB higher than the original specification.

Table 4-1 LNA Performance@1GHz

Parameter	Performance
S11	-10.2 dB
S21	9.77 dB
NF	4.63 dB
IIP3	19.183 dBm

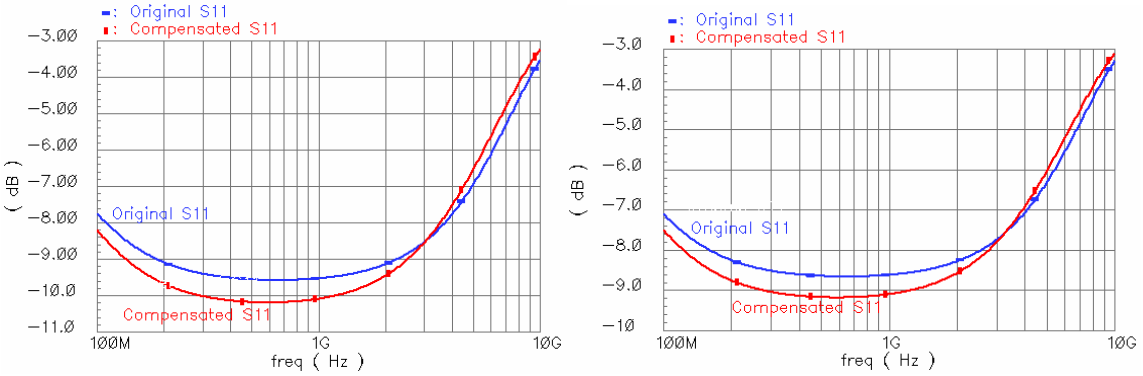
4.2 Simulation Results Comparison between Conventional and Linearized LNA

In this section, the simulation results of the conventional LNA and the linearized LNA are compared for three corners: the Typical process and 65°C, Slow process and 100°C, and Fast process and -25°C.

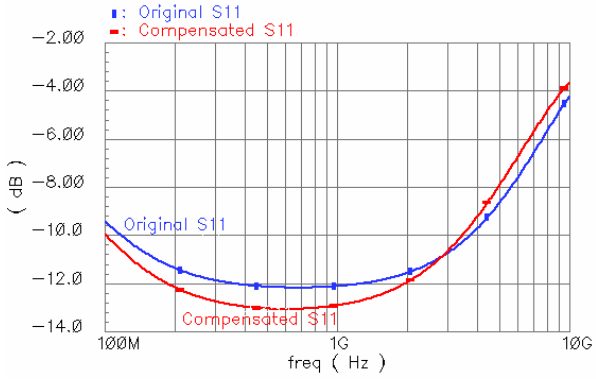
Fig. 4.5 presents the S11 simulation result comparison between the convnetional and the linearized LNA for three corners. Fig. 4.5 (a), (b), and (c) represent the S11 simulation results for the Typical process and 65°C, Slow process and 100°C , and Fast process and -25°C respectively. The “Original S11” and “Compensated S11” in all graphs represent the S11 simulation result for the conventional and the linearized LNA respectively.

Although the “Compensated S11” seems to indicate better input impedance matching at low frequencies for three corners, the linearization method does not improve it. Rather, input impedance matching is a matter of optimization. If optimized, the “Original S11” and “Compensated S11” should show similar results at low frequencies. At high frequencies, “Compensated S11” degrades more quickly since the linearized LNA’s dominant pole is closer than the conventional LNA. As we can see, the absolute

values of S11 can be different from one corner to the other since the transconductance of the transistor can change.



(a) Typical process and 65°C (b) Slow process and 100°C

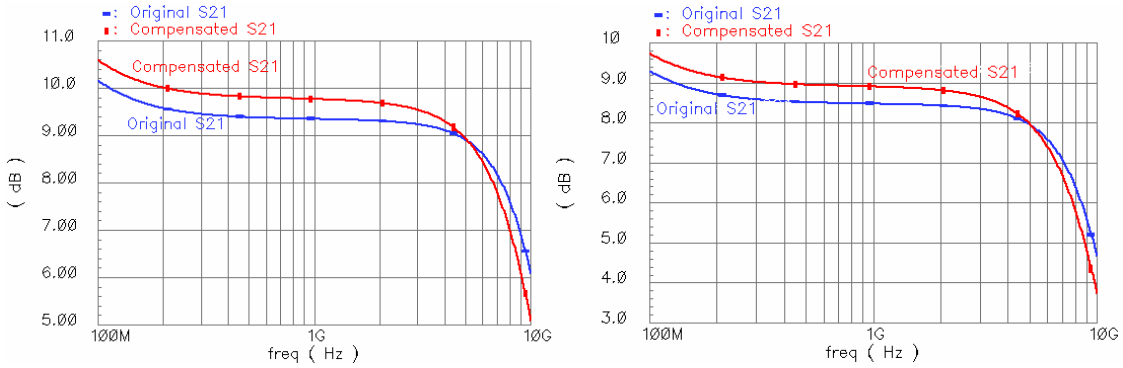


(c) Fast process and -25°C

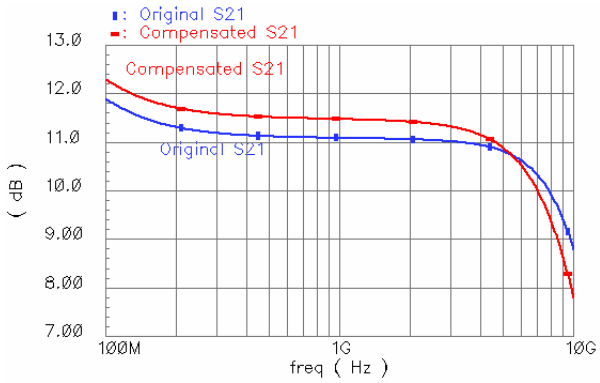
Fig. 4.5 S11 Comparison between Conventional Linearized LNA

Fig. 4.6 shows the S21 simulation result comparison between the conventional and the linearized LNA for three corners. Fig. 4.6 (a), (b), and (c) represent the S21 simulation result for the Typical process and 65°C, Slow process and 100°C , and Fast

process and -25°C respectively. The “Original S21” and “Compensated S21” represent the S21 simulation result for the conventional and the linearized LNA respectively.



(a) Typical process and 65°C (b) Slow process and 100°C



(c) Fast process and -25°C

Fig. 4.6 S21 Comparison between Conventional and Linearized LNA

At low frequencies, the “Compensated S21” shows larger S21. The power gain of the linearized LNA is larger than the power gain of the conventional LNA because the total g_m of the linearized LNA is larger than that of the conventional LNA. The total g_m of the linearized LNA is larger because the additional transistors’ g_ms are added to

the main transistor's g_m. Although the additional transistors cancel the second order derivative of g_m of the main transistor, their g_ms are added to the main transistor's g_m. Since the dominant pole of the linearized LNA is closer to the origin due to the increased input parasitic capacitance, the "Compensated S21" decreases earlier.

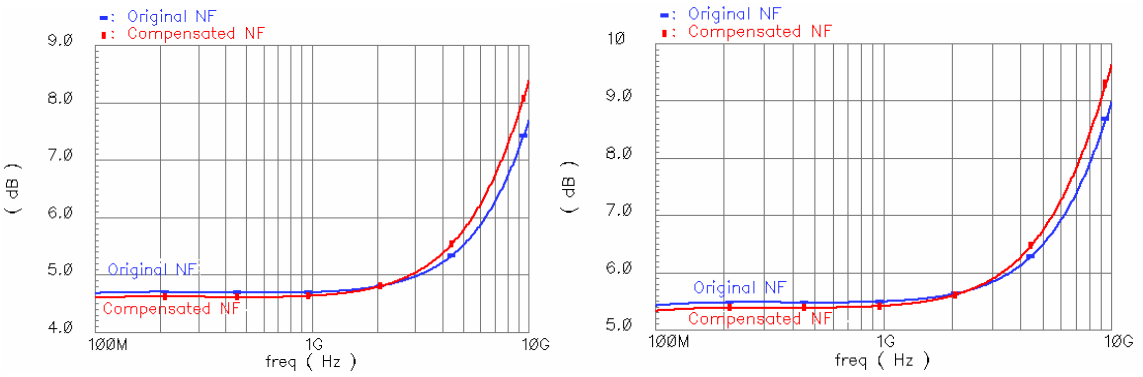
The overall trend of S21 for the Slow process and 100°C corner is similar to the Typical process and 65°C corner. Since the transistor's transconductance decreases for the Slow process and 100°C corner, the power gains of the conventional and the linearized LNA degrade. On the contrary, since the transistor's transconductance increases for the Fast process and -25°C corner, the power gains of the conventional and the linearized LNA increase.

Fig. 4.7 shows the NF simulation result comparison between the conventional and the linearized LNA for three corners. Fig. 4.7 (a), (b), and (c) represent the NF simulation result for the Typical process and 65°C, Slow process and 100°C , and Fast process and -25°C respectively. The "Original NF" and "Compensated NF" represent the NF simulation results for the conventional and the linearized LNA respectively.

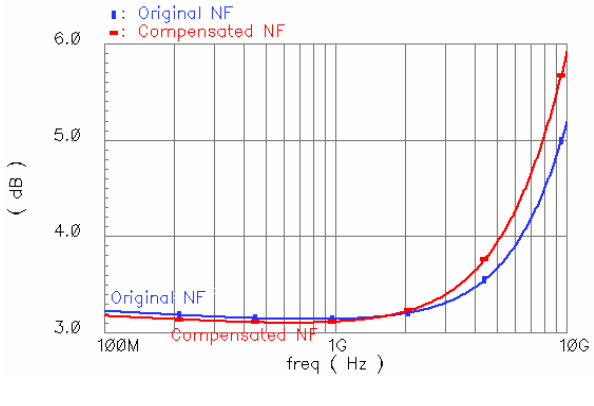
The "Compensated NF" shows better performance at low frequencies due to the increased g_m. However, the "Compensated NF" degrades earlier than the "Original NF" and shows worse performance at high frequencies due to the increased input parasitic capacitance.

The absolute values of the "Original NF" and "Compensated NF" for the Slow process and 100°C are higher than the Typical process and 65°C corner case because the total g_m decreases for the Slow process and high temperatures. On the contrary, since

the total g_m increases for the Fast process and -25°C corner, the "Original NF" and "Compensated NF" show low Noise Figure performance under this condition.



(a) Typical process and 65°C (b) Slow process and 100°C

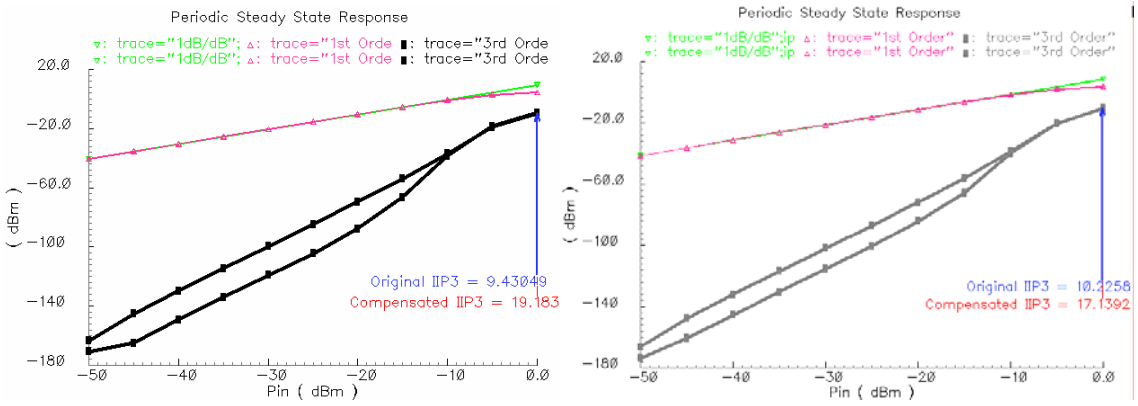


(c) Fast process and -25°C

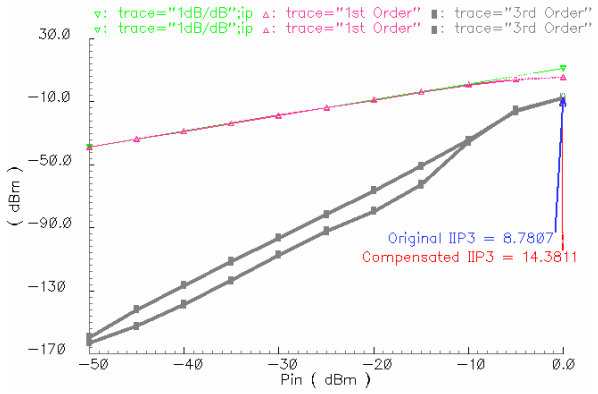
Fig. 4.7 NF Comparison between Conventional and Linearized LNA

Fig. 4.8 shows the IIP3 simulation result comparison between the conventional and the linearized LNA for three corners. Fig. 4.8 (a), (b), and (c) represent the IIP3 simulation result for the Typical process and 65°C, Slow process and 100°C , and Fast

process and -25°C respectively. The “Original IIP3” and “Compensated IIP3” represent the IIP3 simulation results for the conventional and the linearized LNA respectively.



(a) Typical process and 65°C (b) Slow process and 100°C

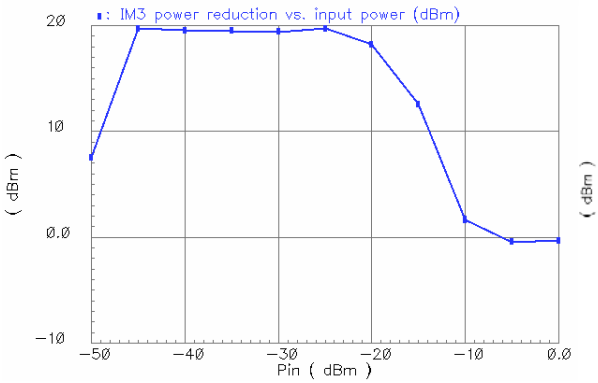


(c) Fast process and -25°C

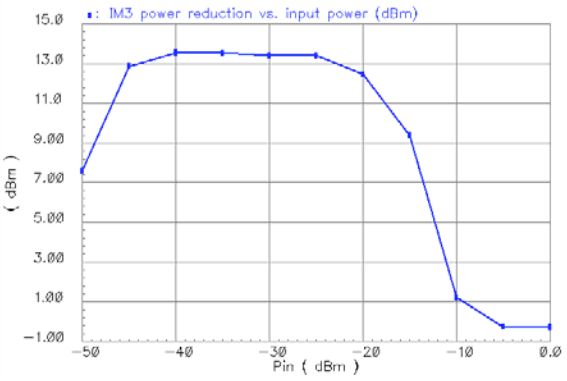
Fig. 4.8 IIP3 Comparison between Conventional and Linearized LNA

The “Compensated IIP3” shows around 10dB higher IIP3 than the “Original IIP3” for the Typical process and 65°C corner. For the Slow process and 100°C corner

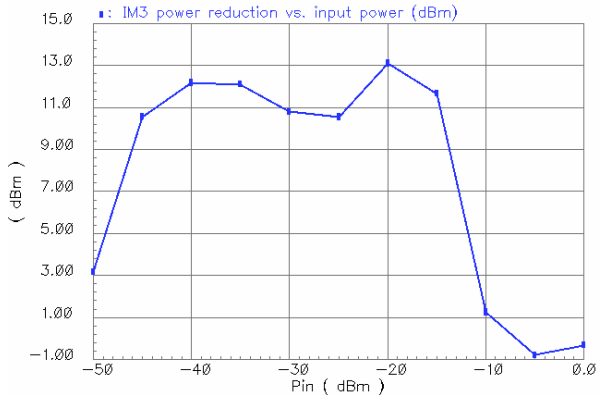
and Fast process and -25°C corner, 7dB and 6dB IIP3 improvement are obtained due to the proposed linearization method.



(a) Typical process and 65°C



(b) Slow process and 100°C



(c) Fast process and -25°C

Fig. 4.9 IM3 Power Reduction Due to the Linearization Method

Fig. 4.9 shows the IM3 power reduction for three corners. Fig. 4.8 (a), (b), and (c) represent the IM3 power reduction for the Typical process and 65°C, Slow process and 100°C , and Fast process and -25°C respectively. Fig. 4.9 (a) shows that the IM3

power is reduced to approximately 20dB, up to -20dBm power input, as a result of the proposed linearization method. Over 12dB of IM3 power reductions are obtained for the Slow process and 100°C corner and Fast process and -25°C corner with -20dBm power input.

IM3 power is reduced by at least 10dB even with -15dBm power input for all three corners. Comparatively the proposed Derivative Superposition method can handle 10dB higher input power than the conventional Derivative Superposition method, which can only operate up to -25dBm input power.

Table 4-2 Simulation Result Comparison for Three Corners

Typical process and 65°C	Original LNA	Linearized LNA
S11@1GHz (dB)	-9.6	-10.2
S21 (dB)	9.34	9.77
NF (dB)	4.7	4.63
IIP3 (dBm)	9.43	19.18
1 dB Compression point (dBm)	-7.588	-7.185
Slow process and 100°C		
S11@1GHz (dB)	-8.6	-9.1
S21 (dB)	8.47	8.9
NF (dB)	5.5	5.4
IIP3 (dBm)	10.2258	17.1392
1 dB Compression point (dBm)	-7.244	-6.8677
Fast process and -25°C		
S11@1GHz (dB)	-12.1	-12.9
S21 (dB)	11.08	11.47
NF (dB)	3.14	3.11
IIP3 (dBm)	8.7807	14.3811
1 dB Compression point (dBm)	-8.07882	-7.75433

Table 4-2 summarizes the simulation results for three corners: the Typical process and 65°C, Slow process and 100°C, and Fast process and -25°C. Interestingly, the 1dB compression point does not change whether the LNA is linearzied or not. This is because the proposed linearization method is effective for the input power level up to -15dBm. As we can see in Fig. 4.8, for over -15dBm input power, the third intermodulation distortion power of the linearized LNA increases rapidly not following the ideal curve of the third intermodulation distortion power. Thus, the 1dB compression point does not change drastically.

4.3 PVT Variation Simulation Result

In this section, the robustness of the proposed linearization method is tested for different processes, temperatures, and supply voltages.

4.3.1 Temperature Variation with Different Processes

Fig. 4.10 presents the S11 simulation results for different corners and temperatures. In this simulation, temperature is changed from -25 to 100°C for all three processes to find the S11 trend. The “Slow S11”, “Typical S11”, and “Fast S11” represent the S11 simulation result for each process with the temperature change.

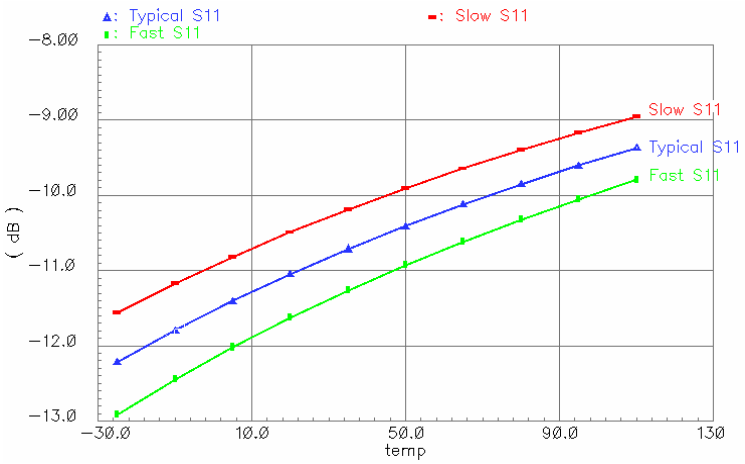


Fig. 4.10 S11 Simulation Results for Three Corners with Temperature Change

Fig. 4.10 shows that S11 degrades at high temperature. As temperature increases, the transistor's g_m decreases. Consequently, the input impedance can change. Since the input impedance of the designed LNA is set to 50Ω, S11 can degrade with an increase in temperature.

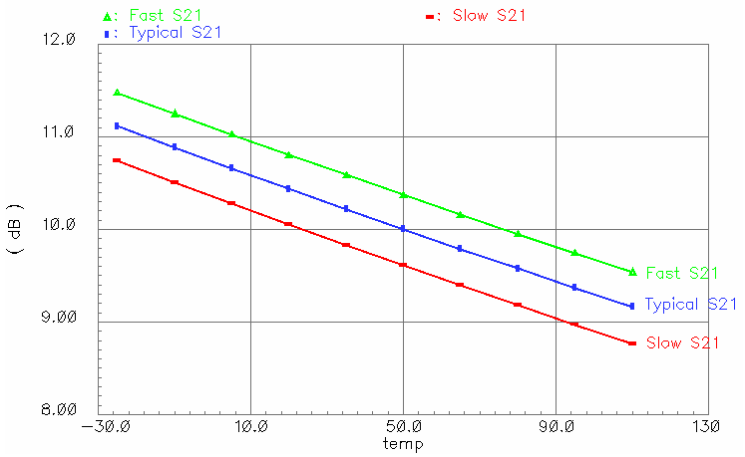


Fig. 4.11 S21 Simulation Results for Three Corners with Temperature Change

Fig. 4.11 presents the S21 simulation results for different corners and temperatures. In this simulation, temperature is changed from -25 to 100°C for all three processes to find the S21 trend. The “Slow S21”, “Typical S21”, and “Fast S21” represent the S21 simulation result for each process with the temperature change. From the figure, a large S21 can be obtained under the Fast process and low temperatures condition since the transistor’s g_m increases under this condition.

Fig. 4.12 presents the NF simulation results for different corners and temperatures. In this simulation, temperature is changed from -25 to 100°C for all three processes to find the NF trend. The “Slow NF”, “Typical NF”, and “Fast NF” represent the NF simulation result for each process with the temperature change. A low NF can be obtained under the Fast process and low temperatures condition since the transistor’s g_m increases under this condition.

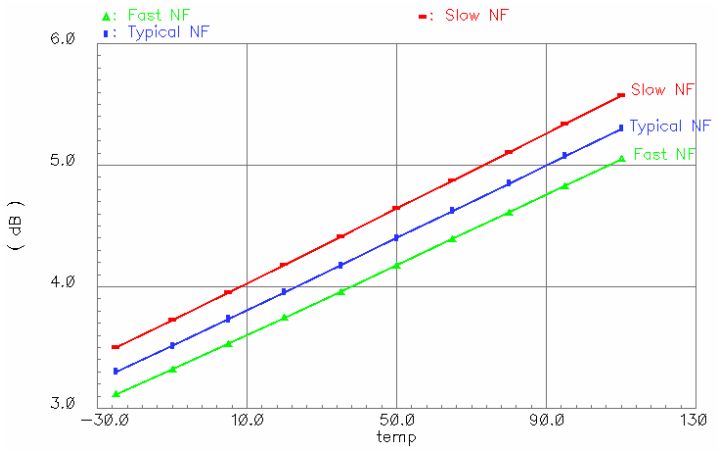


Fig. 4.12 NF Simulation Results for Three Corners with Temperature Change

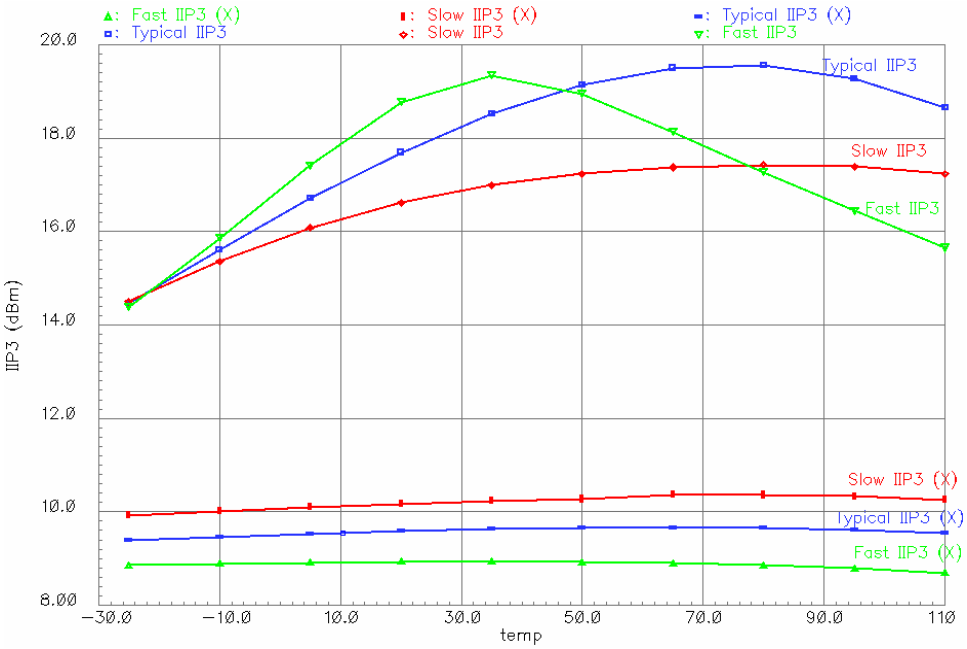


Fig. 4.13 IIP3 Simulation Results of Conventional and Linearized LNA for Three Corners with Temperature Change

Fig. 4.13 shows the IIP3 simulation results of the conventional and the linearized LNA for all processes and temperatures. In the above figure, “Slow IIP3”, “Typical IIP3”, and “Fast IIP3” represent IIP3 simulation result of the linearized LNA for each corner with the temperature change. “Slow IIP3 (X)”, “Typical IIP3 (X)”, and “Fast IIP3 (X)” represent IIP3 simulation results of the conventional LNA for each corner with the temperature change. This graph clearly shows that IIP3 is improved with the proposed linearization method for all processes and temperatures.

4.3.2 Supply Voltage Variation with Different Processes

Fig. 4.14 shows the S11 simulation result for the Typical and 65°C corner with the supply voltage change from 2.2V to 2.6V. S11 does not change drastically. S11 is dependent on the transconductance of the transistor and it rarely changes with the supply voltage change. The S11 simulations for other corners show similar results.

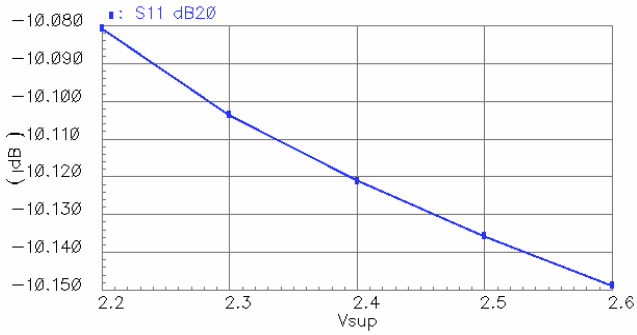


Fig. 4.14 S11 Simulation Result with Supply Voltage Change

Fig. 4.15 shows the S21 simulation result for the Typical and 65°C corner with the supply voltage change from 2.2V to 2.6V. S21 does not change drastically since the transconductance of the transistor does not change for different supply voltages. The S21 simulations for other corners show similar results.

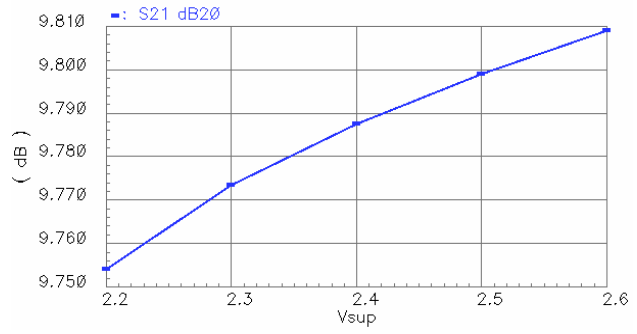


Fig. 4.15 S21 Simulation Result with Supply Voltage Change

Fig. 4.16 shows the NF simulation result for the Typical and 65°C corner with the supply voltage change from 2.2V to 2.6V. Because the transconductance does not change, the NF simulation result remains the same. The NF simulations for other corners show similar results.

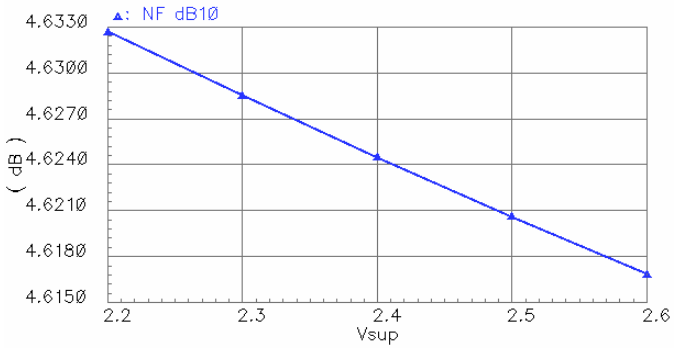


Fig. 4.16 NF Simulation Result with Supply Voltage Change

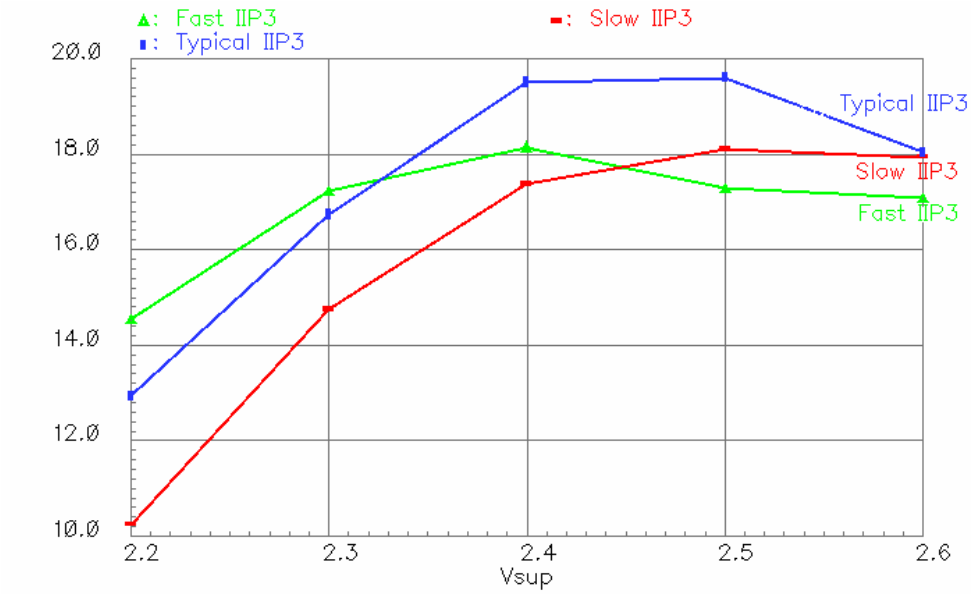


Fig. 4.17 IIP3 Simulation Result for Three Processes with Supply Voltage Change

Fig. 4.17 presents the IIP3 simulation results for the Slow, Typical, and Fast processes with the supply voltage change from 2.2V to 2.6V. The graph shows that IIP3 degrades at the low supply voltage. If the supply voltage drops, the drain node voltage of the cascode transistor also drops. This directly reduces the impedance generated by the cascode transistor and the main transistor. Then, the overall impedance at the output node is no longer dominated by the linear load impedance. As a result, the overall output impedance is determined by both the linear load impedance and the highly non-linear transistor output impedance. Although the overall transconductance is linear, the output voltage can be non-linear if the output impedance is non-linear. IIP3 becomes worse with the reduced supply voltage, below 2.3V.

4.4 Monte Carlo Simulation Result

The Monte Carlo simulations are performed to check the stability against the process variation and the mismatch of MOSFETs. The threshold voltage and the mobility of MOSFETs are assumed to be varied up to 15% from the mean value. All S-parameters are measured at 1GHz. This simulation is performed for the Typical process and 65°C corner. All results are obtained with two hundred simulations.

Fig. 4.18 shows the Monte Carlo simulation for S11. The mean value of -10.6dB and the standard deviation of around 0.117 are obtained. All simulation results are under -10dB. S11 does not vary drastically with the mismatch because it is more dependent on the absolute value of the transconductance.

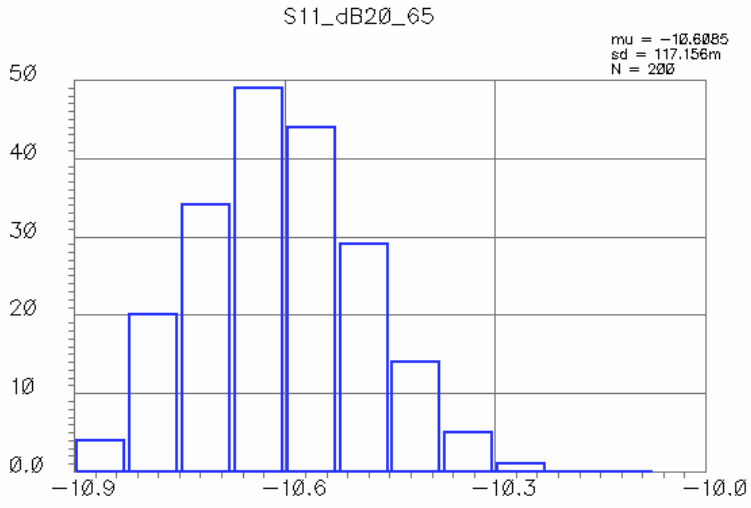


Fig. 4.18 S11 Monte Carlo Simulation Result

Fig. 4.19 shows the Monte Carlo simulation for S21. The mean value of 10.15dB and the standard deviation of around 0.08 are obtained. Similar to the S11 simulation result, S21 does not vary drastically with the mismatch.

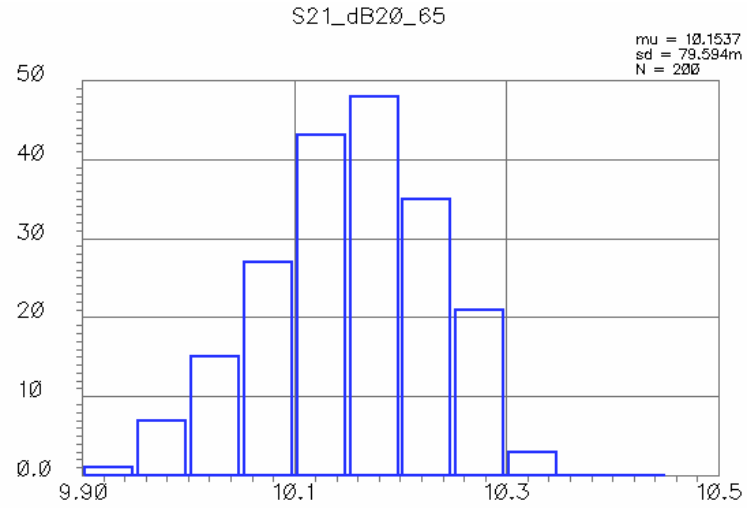


Fig. 4.19 S21 Monte Carlo Simulation Result

Fig. 4.20 shows the Monte Carlo simulation for NF. The mean value of 4.4dB and the standard deviation of around 0.04 are obtained. NF ranges from 4.3dB to 4.6dB. NF also does not vary drastically with the mismatch.

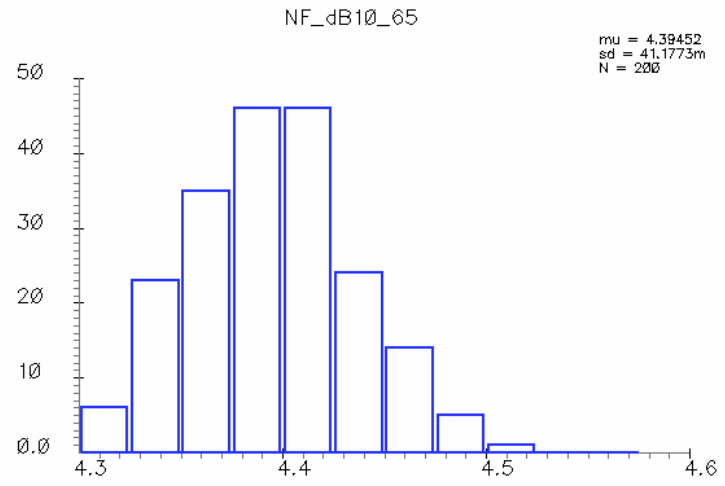


Fig. 4.20 NF Monte Carlo Simulation Result

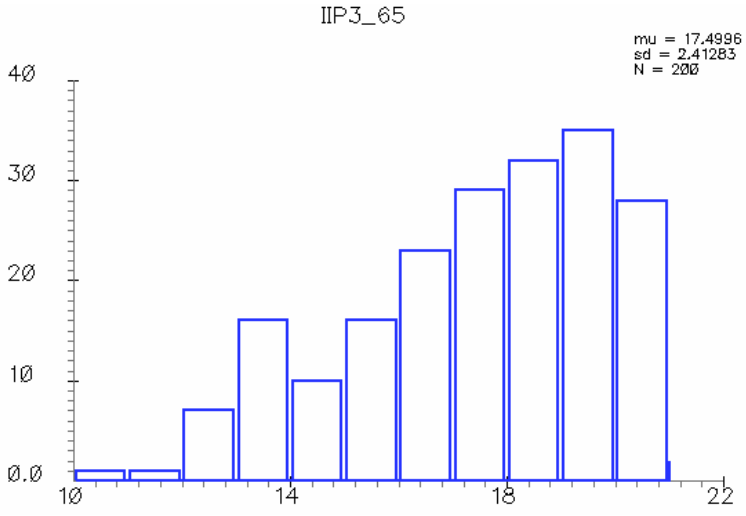


Fig. 4.21 IIP3 Monte Carlo Simulation Result

The IIP3 simulation result is presented in Fig. 4.21. Different from other simulation results, the IIP3 simulation does not show the center-oriented graph. Rather, it can decrease to 10dBm which is 7.5dB below the mean value. Considering that the initial IIP3 simulation value is 19dBm for the Typical process and 65°C corner, IIP3 tends to be worse with mismatches. In other words, the IIP3 performance is more sensitive to mismatches. Nevertheless, around 90% of simulation results are over 14dBm, which is still 4dB higher than the best case IIP3 without the linearization method.

CHAPTER V

CONCLUSIONS

In this thesis, a non-linear system is analyzed and the non-linear characteristic of a MOSFET is discussed, followed by the linearization methods, such as feedback and the Derivative Superposition method. A novel linearization methods, such as the constant current biasing and the Derivative Superposition method using the triode region transistor, are also introduced.

A highly linear broadband LNA is designed and implemented using the proposed linearization method in 65nm CMOS technology. A resistive feedback topology is chosen for the LNA implementation. Its characteristics are analyzed including the frequency response, the input impedance matching and the Noise Figure. The volterra series analysis is included for IIP3 analysis at high frequencies with the feedback system. The input stage of the LNA is linearized using the proposed Derivative Superposition method and the constant current biasing. We obtained S21 of 9.77 dB with the 3dB bandwidth of 8 GHz. The Noise Figure shows 4.63 dB and IIP3 shows 19.18 dBm. IM3 powers are also described for an accurate comparison of the different power inputs. The IM3 power is reduced at least 9dB for up to -15dBm power input. This improvement is obtained with the cost of an additional 2% power consumption and 10% bandwidth degradation.

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