A 3.125 GB/S 5-TAP CMOS TRANSVERSAL EQUALIZER

A Thesis

by

MARCOS LUIS LOPEZ-RIVERA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	José Silva-Martínez
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	Kai Chang
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ABSTRACT

A 3.125 Gb/s 5-TAP CMOS Transversal Equalizer.

(December 2009)

Marcos Luis López-Rivera, B.S.E.E, Universtiy of Puerto Rico

Chair of Advisory Committee: Dr. José Silva-Martínez

Recently, there is growing interest in high speed circuits for broadband communication, especially in wired networks. As the data rate increases beyond 1 Gb/s, conventional materials used as communication channels, such as PCB traces, coaxial cables, and unshielded twisted pair (UTP) cables, etc. attenuate and distort the transmitted signal causing bit errors in the receiver end. Bit errors make the communication less reliable and in many cases even impossible.

The goal of this work was to analyze and design a channel equalizer capable of restoring the received signal to the original transmitted signal. The equalizer was designed in a standard CMOS 0.18 µm process and it is capable of compensating up to 20 dB's of attenuation at 1.5625 GHz for 15 and 20 meters of RG-58 A/U coaxial cables. The equalizer is able to remove 0.5 UI (160 ps) of peak-to-peak jitter and output a signal with 0.1 UI (32 ps) for 15 meters of cable at 3.125 Gb/s. The equalizer draws 18 mA from a 1.8 V power supply which is comparable to recent publications in CMOS transversal equalizers.

DEDICATION

To Camila and Ian Marco

ACKNOWLEDGMENTS

The pursuit of knowledge is an extensive and intricate journey that requires passion, patience and dedication. It is a journey some would endeavor for the satisfaction and lifelong rewards it brings. In this journey there will be ups and downs and that it is why it becomes essential to surround ourselves with people that will provide support and help us reach our aspirations. Without the help and support from many people, I would not have completed my graduate work.

I thank my graduate advisor, Dr. José Silva-Martínez, for his constant guidance and support throughout my graduate studies. It is through your help and patience that I was able to explore great research. Also, I thank Dr. Sebastian Hoyos for the time you took to help with my research in FIR filters.

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CHAPTER I

INTRODUCTION

In recent years with the advent of the internet and the ever increasing speed of digital circuits the need for fast and reliable data transmission have become the main bottleneck in data communication systems, which has brought a fair amount of interest in optical and electronic communication devices and systems. As transmitted data travels through the communication channel (i.e. PCB trace, coaxial cable, UTP cable, etc.) at frequencies beyond the cutoff frequency of the channel, it experiences attenuation and delay due to the frequency dependent characteristics of the materials used. The signal can undergo so much distortion to the point where is unrecoverable by the receiver circuit. To address this problem equalization is used to compensate for the non idealities of the channel. Equalization is done in wireline receivers to provide gain and filtering required for proper detection of the transmitted data.

A. Wireline Transceivers

Figure 1 shows a typical wireline transceiver sytem. It consists of a multiplexer that serializes the data. A retimer is used to synchronize the input data coming from *N* channels and outputs a data with *N* times higher symbol rate. The serialized and synchronized data is sent trough the channel trough a Line Driver that provides the required voltage swing [1] and provides adequate impedance matching with the transmission channel to avoid reflections [2].

This thesis follows the style and format of *IEEE Journal of Solid-State Circuits.*

As the data travels through the band limited channel, the high frequency content of the data is attenuated and distorted in time which introduces a phenomenon called Inter-symbol Interference (ISI).

To remove ISI and compensate for the channel non-idealities an Equalizer is used to filter the input data of the reciver [3]. Once the data is recovered with a decision element, sometimes referred as “slicer”, it is retimed using a Clock and Data (CDR) circuit. To finish the recovery process the data is then deserialized using a demultiplexer (DMUX) and the original *N* channels are again transmitted at original bit rate.

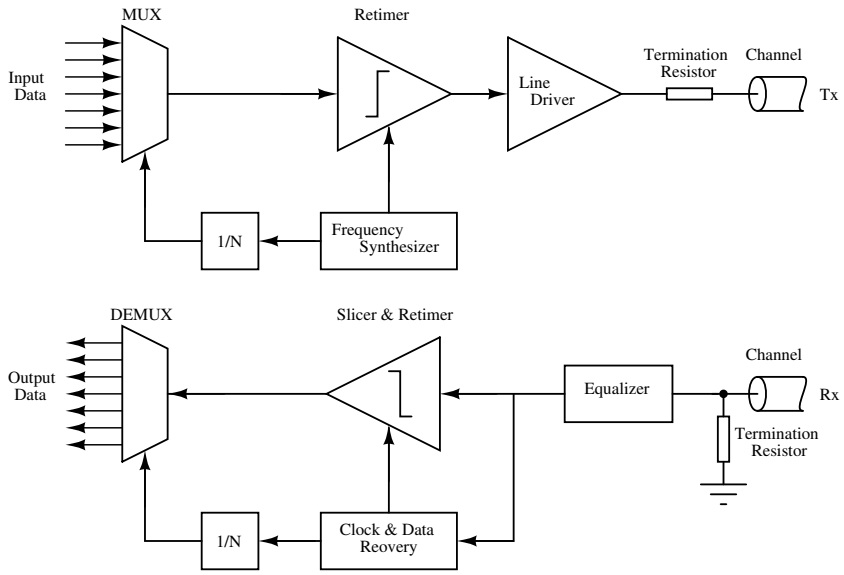

Figure 1. Wireline Transceiver Architecture.

B. Trends in Equalizer Design and Applications

On the demand for higher bit rates in data communications either optical or electrical, high speed analog front-end circuits become a key element in the receiver.

The analog front-end often requires the use of an equalizer to compensate the channel attenuation as discussed in the previous sub-section. Conventionally these equalizers are built using SiGe, GaAs, or bipolar technologies, however in order to integrate digital signal processing circuits into a single chip solution, CMOS analog equalizers with small area and power consumption are preferred. CMOS high speed analog equalizers have gained popularity in applications with data rates ranging from 1 Gb/s up to 10 Gb/s. Among these applications:

1. 1 Gb/s Ethernet
2. OC-48 (2.4 Gb/s)
3. 10GBASE-CX4 (3.125 Gb/s)
4. Chip-to-chip I/O backplane (4 – 7 Gb/s)
5. OC-192 and the new 10 Gb/s Ethernet

This work deals with the design of a 3.125 Gb/s analog adaptive coaxial cable equalizer for 10 GBASE-CX4 applications.

C. Thesis Organization

Before delving in channel equalization and limitations it is imperative to understand the source of non idealities in the communication channel. The second chapter of this work provides an insight on channel modeling and channel distortion and equalization respectively. Chapter III provides an overview on system level implementation and limitations of an equalizer. Chapter III serves as basis for chapter IV where a detailed description of the analysis and design of a 3.125 GB/s CMOS equalizer is given. Final remarks, future work and conclusions are given in Chapter V.

CHAPTER II

COMMUNICATION CHANNEL MODELING AND LIMITATIONS

A. Channel Background

The voltage propagating along a transmission line at a particular x can be expressed as [2]

$$V(z) = V_O^{+} e^{-\gamma x} + V_O^{-} e^{\gamma x} \tag{2.1}$$

where V_O^{+} is the transmitted wave (signal propagating in the +x direction) and V_O^{-} is the reflected wave (signal propagating in the –x direction); γ is the propagation constant and can be rewritten in terms of an attenuation factor α and a phase factor β as follows,

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.2}$$

For a coaxial cable modeled as a transmission line, the attenuation α and phase β parameters can be expressed as,

$$\alpha(\omega) = \mathrm{Re}\left[\sqrt{(R + j\omega L)(G + j\omega C)}\right] \tag{2.3}$$

$$\beta(\omega) = \mathrm{Im}\left[\sqrt{(R + j\omega L)(G + j\omega C)}\right] \tag{2.4}$$

where ω is the angular frequency in rad/sec of the propagating signal, L is the inductance per unit length, C is the capacitance per unit length, R is the conductor loss and G is the loss associated with the dielectric used in the coaxial line. Depicted below in figure 2 is the electrical representation of the equivalent circuit of a coaxial line.

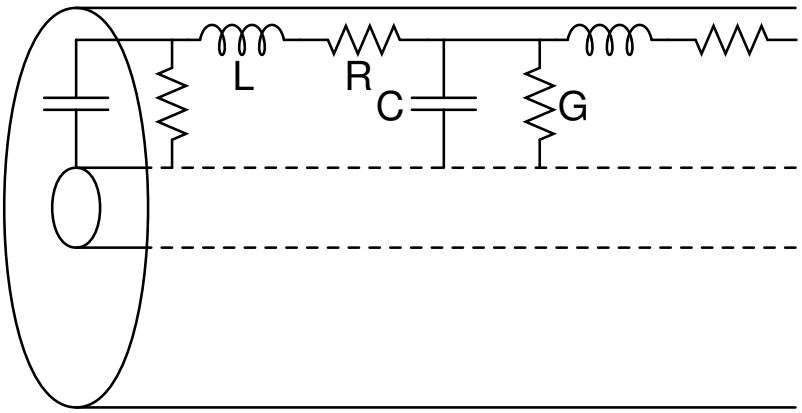

Figure 2. L, C, R and G in a coaxial line.

Similarly the current can be defined as [2],

$$I(z) = I_o^+ e^{-\gamma x} + I_o^- e^{\gamma x} \tag{2. 5}$$

where,

$$I_o^{\ +} = \frac{\gamma}{R + j\omega L} V_o^{\ +}, \qquad I_o^{\ -} = \frac{\gamma}{R + j\omega L} V_o^{\ -} \tag{2. 6}$$

The characteristic impedance of the transmission line is defined as,

$$Z_o = \frac{V_o^{\ +}}{I_o^{\ +}} = \frac{V_o^{\ -}}{I_o^{\ -}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.7}$$

In the case of a lossless line i.e. R = G = 0, the characteristic impedance can be written as,

$$Z_o = \sqrt{\frac{L}{C}} \tag{2.8}$$

also,

$$\gamma = j\omega\sqrt{LC} \tag{2.9}$$

B. Channel Modeling

A typical attenuation profile for a Belden 8219 RG-58A/U 20 AWG cable commonly used in radio communication and amateur radio, thin Ethernet (10Base2) and NIM electronics is shown in table I.

Table – I. Attenuation vs. frequency profile of RG-58A/U cable.

Frequency (MHz)	Attenuation (dB/100 ft.)
1	0.4
10	1.3
50	3.1
100	4.5
200	6.6
400	10.0
700	14.2
900	16.6
1000	18.1

Depicted in Figure 3 is the idealized magnitude response of a coaxial cable. In practice the cable's response will not decay monotonically due to signal reflection at

higher frequencies. Ideally the cable has to be characterized to extract the S_{21} information, but in absence of a physical channel a model can be employed.

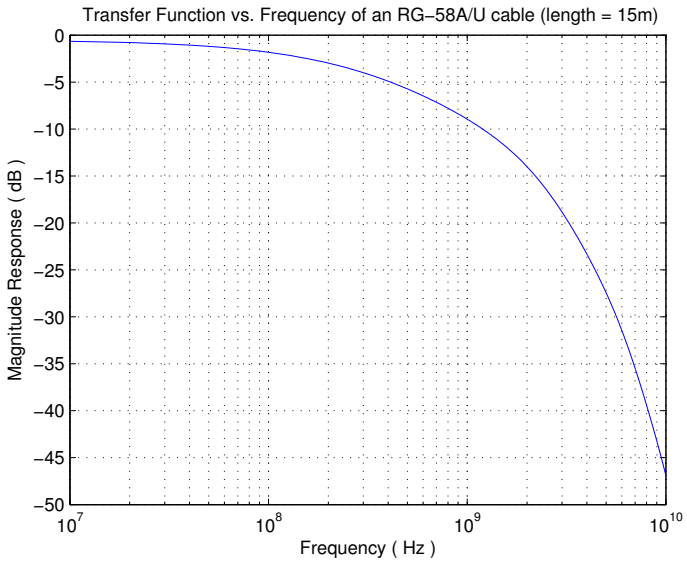

Figure 3. Magnitude response of a 15 meters RG-58A/U cable.

1. ABCD Matrix Channel Representation.

There are various ways to model a coaxial cable or any channel in general (i.e. PCB traces, optic fiber, etc.). One useful method to represent the channel as a cascade of two port networks is the transmission line matrix also known as ABCD matrix [4]. This method relates the input and output voltage and current phasors as follows:

$$\begin{bmatrix} V_O \\ I_O \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_I \\ I_I \end{bmatrix} \tag{2.10}$$

For a transmission line with length *d* the ABCD matrix can be expressed as [4]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma d) & Z_O \sinh(\gamma d) \\ \frac{1}{Z_O}\sinh(\gamma d) & \cosh(\gamma d) \end{bmatrix} \tag{2.11}$$

ABCD matrices can be multiplied by the source and load impedance matrices to obtain the matrix of a terminated line. It is important to mention that an ABCD matrix represents the network at a single frequency, to cover a range of frequencies the Matrix must be evaluated for each frequency in the range of interest.

2. Digital Filter Channel Representation.

Another common method to model the response of a communication channel is to emulate the channel transfer's function with an FIR or IIR digital filter. The only drawback of this method is that the frequency response of the channel has to be known a priori. The S_{21} information of the channel can be fed into an algorithm to calculate the desired filter coefficients. The frequency response information was obtained from the vendor's data sheet and a polynomial fit was performed in Matlab to increase the

number of frequency points for the desired cable. Once enough points were evaluated using a 10^{th} order polynomial, the desired transfer function was emulated using an FIR filter in Matlab. Depicted in figures 4 and 5, is the magnitude and phase response respectively for such FIR model. In a coaxial cable or any electrical link the major degradation is observed in the magnitude response. The phase response is almost linear in the bandwidth of interest resulting in a constant group delay which is a consequence of delay in the cable in contrast to optic systems where distortion is observed in the phase instead of the magnitude.

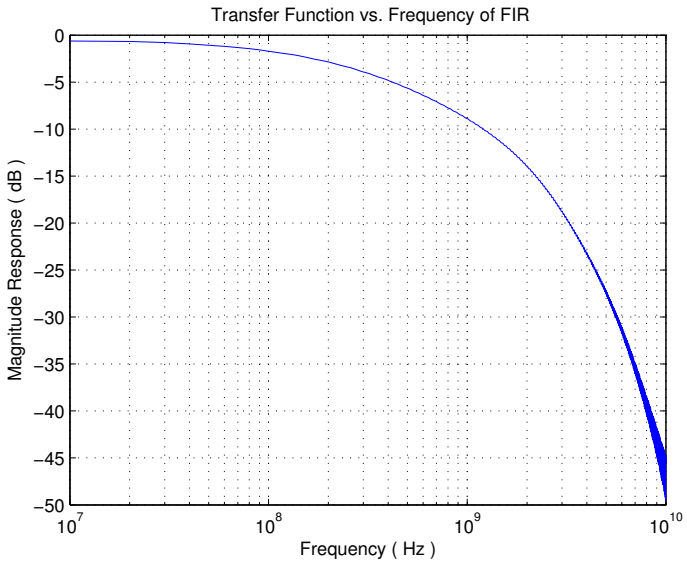

Figure 4. Magnitude response of the FIR channel model (length = 15 m).

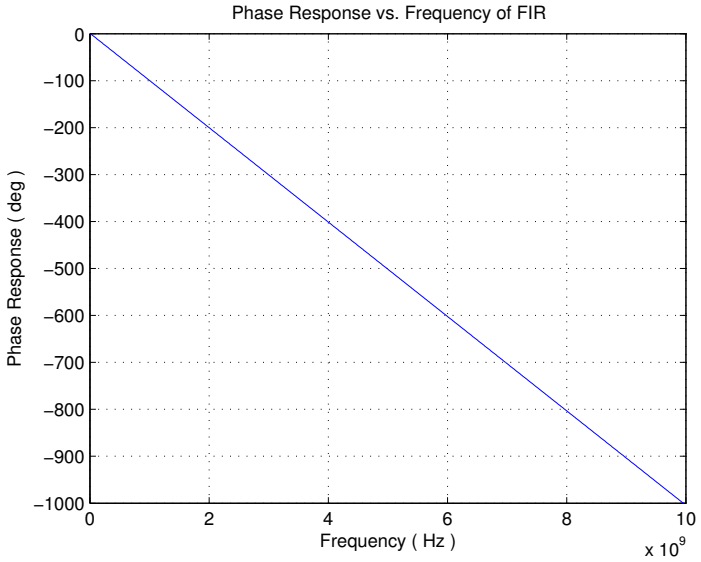

Figure 5. Phase response of the FIR channel model (length = 15 m).

3. Transmission Line Channel Representation.

Another practical method to model wire channels as transmission lines was reported in [5]. This method describes the channel transfer function as follows,

$$C(f) = e^{-d\gamma} \tag{2.12}$$

$$\gamma = \alpha'(1+j)\sqrt{f} - j\beta' f \tag{2.13}$$

where d is the length of the wire in meters and α' & β' are used as fitting parameters to equal the channel frequency response. After all three methods where evaluated, only the digital filter approach and the method reported in [5] were implemented and the former outperformed the latter in terms of reduced complexity. After α' and β' where found to be 2e-6 Hz^2/m and 4.35e-8 Hz/m respectively, a Pseudo Random Binary Sequence (PRBS) was generated in Matlab, then a Fast Fourier Transform (FFT) was performed

on the random data and then multiplied by the channel's transfer function. Once the data was multiplied by the complex frequency response of the channel an Inverse Fast Fourier Transform was performed to obtain the time domain information that could be fed into cadence using a Piece Wise Linear File (vpwlf) voltage source. The frequency and phase response obtained using equation 2.12 are shown in figures 6 and 7 respectively. In the following section an introduction to channel distortion and non idealities due to the channel finite bandwidth and the effects all these have on the transmitted data will be provided.

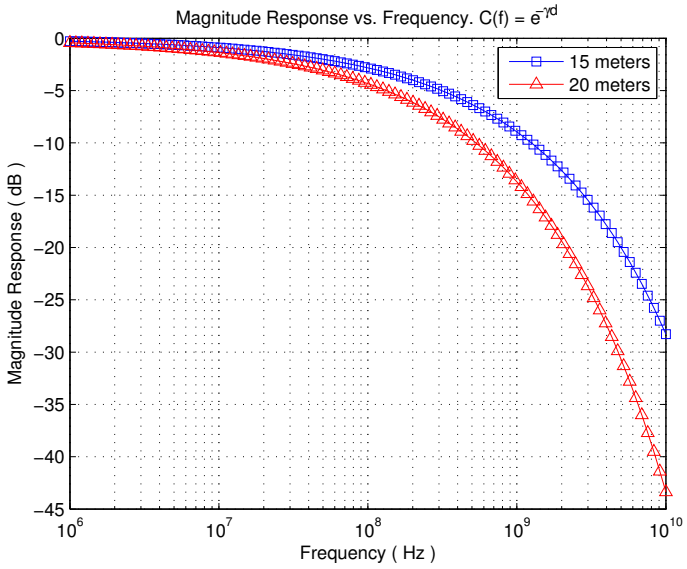

Figure 6. Magnitude response of equation 2.12.

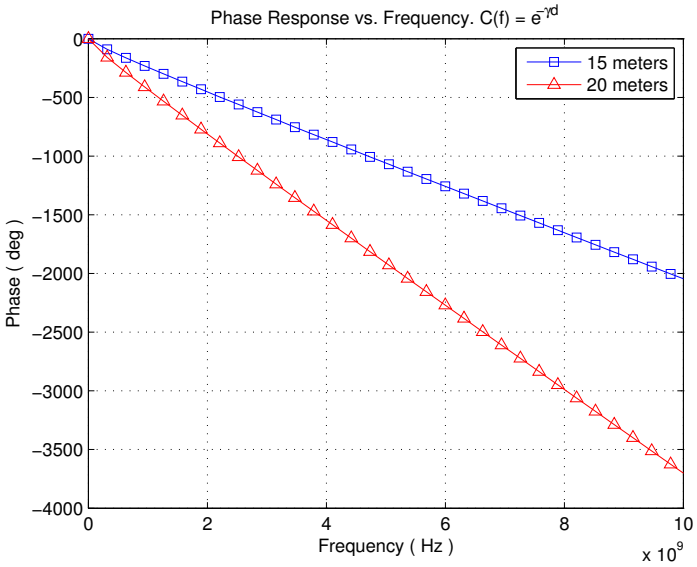

Figure 7. Phase response equation 2.12.

C. Channel Limitations

In a digital communication system the output data coming from the transmitter is a square wave with well defined amplitude. As data travels through the channel it pickups noise and gets delayed, and attenuated reducing the amplitude. The effect that attenuation, delay, and noise have on the data being transmitted will be discussed in detail in this section.

1. Inter-Symbol Iinterference (ISI)

Inter-symbol interference (ISI) is as a form of distortion introduced to a symbol by the previously (precursor ISI) and posterior (postcursor ISI) transmitted symbols in a digital sequence. A mathematical representation of this can be given if we assume that the received signal $y(t)$ is sampled every T seconds, therefore

$$y(kT) = \sum_{n=0}^{\infty} I_n h(kT - nT) \tag{2.14}$$

Similarly,

$$y_k = \sum_{n=0}^{\infty} I_n h_{k-n} = \underbrace{h_0 I_k}_{desired} + \underbrace{\sum_{n=0}^{n<k} I_n h_{k-n}}_{precursorISI} + \underbrace{\sum_{n>k}^{\infty} I_n h_{k-n}}_{postcursorISI} \tag{2.15}$$

where I_n is a chain of transmitted symbols, $h(t)$ is the impulse response of the filter and k is a positive integer. ISI arises from the finite bandwidth or bandwidth limitations of the communication channel. To illustrate this consider the first order channel model depicted below in figure 8.

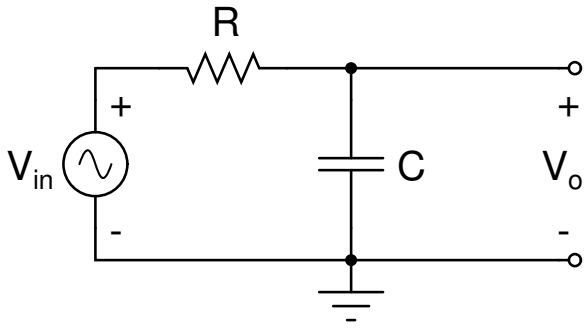

Figure 8. First order channel model.

If a random non return to zero (NRZ) binary sequence with frequency components beyond the 3-dB frequency of the channel is transmitted, the output will suffer considerable ISI and attenuation. A worst case scenario would be when a logic "one" is transmitted with a preceding and trailing chain of logic "zeroes" or vice versa. As an example, assume that the cutoff or 3-dB frequency of the low pass filter is set at

250 MHz, if a random binary sequence containing frequency components up to 500 MHz is sent trough the channel the input data stream will undergo an adequate amount of filtering which can be observed in the output signal (figure 9). Filtering not only decreases the amplitude of the input signal it also spreads the signal in time causing each symbol to be wider than a symbol period T_B and smear or spillover some of its energy into the next symbol causing ISI as shown in figure 10.

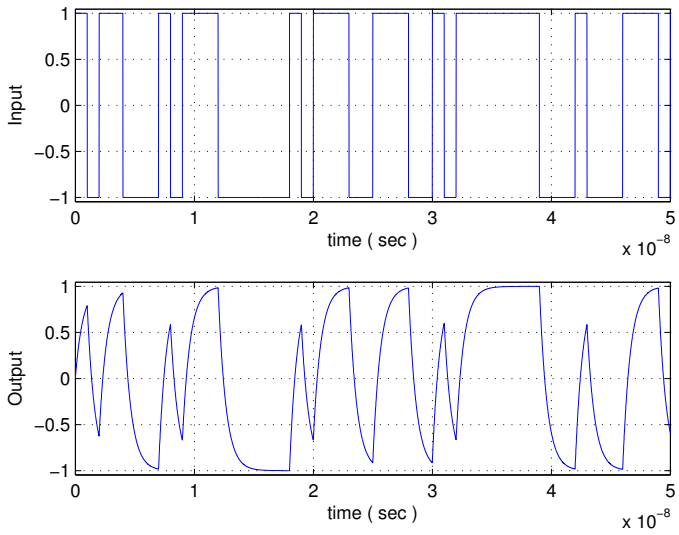

Figure 9. Input (top) and output (bottom) of the first order channel model.

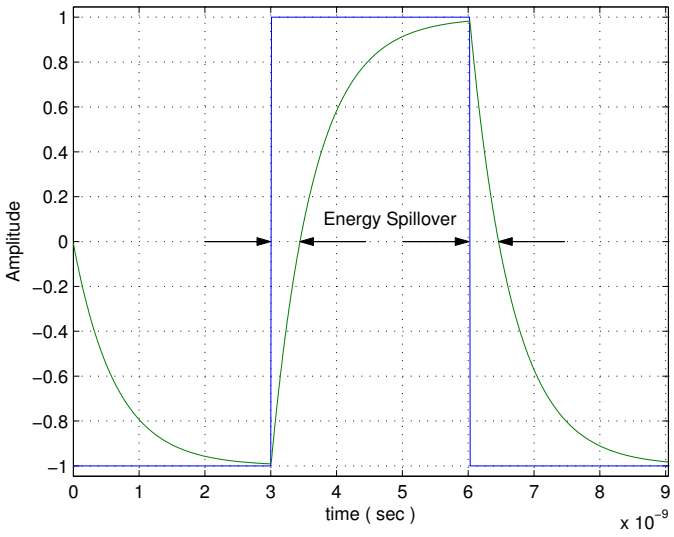

Figure 10. Energy spillover.

Figures 9 and 10 give a qualitative insight on the distortion being introduced by the channel, however they fail to provide quantitative information this is why in telecommunication systems, an eye pattern is used. An eye pattern, also know as an eye diagram is an oscilloscope display in which a digital data signal from a receiver is repetitively sampled and applied to the vertical input, while the data rate is used to trigger the horizontal sweep as shown in figure 11. It is so called because, for several types of coding, the pattern looks like a series of eyes between a pair of rails.

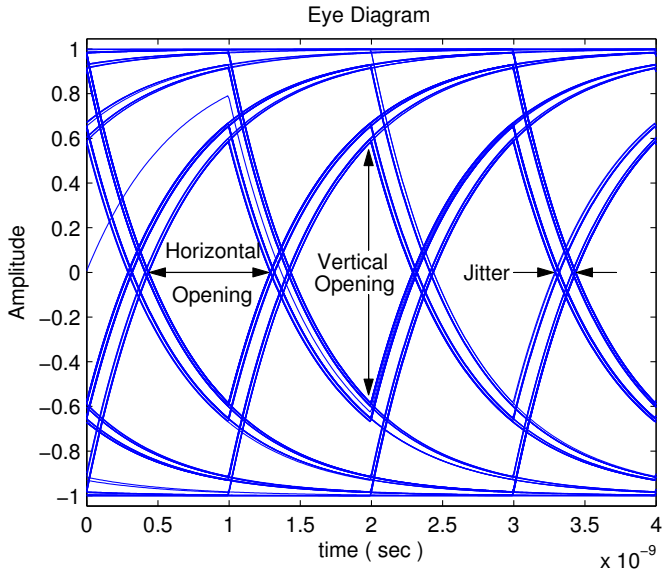

Figure 11. Eye pattern diagram.

Several system performance measures can be derived by analyzing the display. If the signals are too long, too short, poorly synchronized with the system clock, too high, too low, too noisy, and too slow to change, or have too much undershoot or overshoot, this can be observed from the eye diagram. An open eye pattern corresponds to minimal signal distortion. Distortion of the signal waveform due to ISI and noise appears as closure of the eye pattern. Eye closure or inversely eye opening can be either vertical or horizontal and are illustrated in figure 11. On the other hand jitter which is the deviation of the zero crossing points of the signal from the desired one. Jitter can be quantified as follows [6].

1. Cycle-To-Cycle Jitter: Time difference between successive periods of a signal.

2. Period Jitter: An RMS calculation of the difference of each period from a waveform average.
3. Time Interval Jitter: The difference in the time between the actual threshold crossing and the expected transition point.

Depending on the source of the jitter it can be classified into two types:

1. Deterministic Jitter.
2. Random Jitter.

Deterministic jitter arises from the channel limitations it is bounded and can be described by a non-Gaussian probability density function (PDF). It is usually described by its peak to peak values and can be system dependent (crosstalk, power supply switching noise) or data dependent (ISI, duty cycle distortion).

Random jitter is not bounded and can be also described by a Gaussian PDF. It is usually given as an rms value which represents its standard deviation and it is caused by random noise sources such as thermal noise, shot noise and 1/f noise. In other words it is caused by the finite signal to noise ratio (SNR) of the system.

Jitter and channel bandwidth limitation can introduce ISI which degrades the performance of the system and makes the communication less reliable. ISI can degrade the performance of the system because it reduces the eye-opening of the transmitted signal to a great extent where communication between the transmitter and the receiver might be impossible. To remove ISI and improve the eye-opening and equalizer is typically used in wire-line receivers.

D. Equalization

Several physical channels, such as electrical links, not only introduce ISI due to their bandwidth limitations, they also distort the input signal in their pass band. In order is to compensate for the channel bandwidth limitation and remove ISI, equalization is used in the receiver or transmitter as shown in figures 12 and 13 respectively.

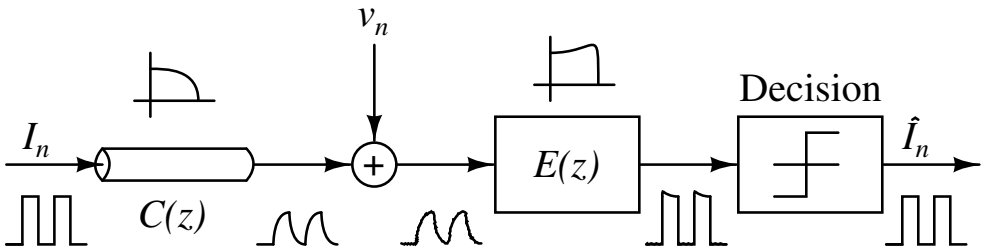

Figure 12. Equalization in the receiver end.

In figure 11 I_n represents a chain of transmitted symbols that will go trough the discretized channel transfer function $C(z)$, v_n represents an additive white Gaussian noise (AWGN) sequence and $E(z)$ represents the equalizer's discrete time transfer function. To overcome all the limitations mentioned above the equalizer must theoretically have a transfer function given by,

$$E(z) = \frac{1}{C(z)} \tag{2.16}$$

The last element in the chain is the Slicer or decision circuit which will transform the equalized data into a chain of detected symbols $\hat{I}_n$.

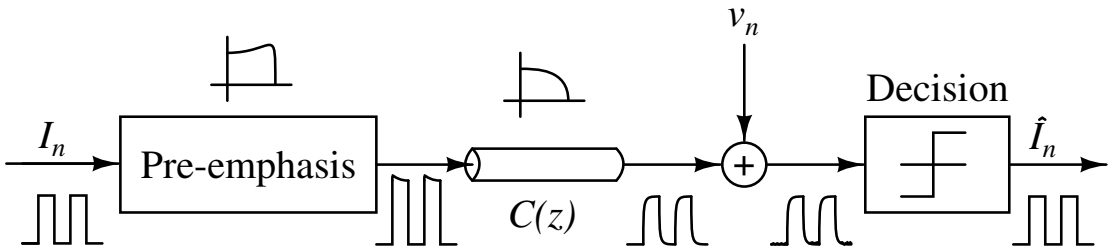

Figure 13. Equalization in the transmitter.

Shown above in figure 13 is a communication system where pre-equalization is done in the transmitter. The chain of symbols to be transmitted I_n will undergo a pre-emphasis, such as a pulse shaping filter, that will distort the signal that is about to go trough the channel's discrete time transfer function *C(z)*. Some of the disadvantages of doing pre-emphasis at the transmitter are the following:

1. Increased transmitter power which taxes the transmitter in the sense of increased dynamic range and electromagnetic interference. Moreover due to the reduced IC supply voltages the maximum output amplitude is constrained leading to a reduced eye at the receiver.
2. Channel transfer function must be known a priori and must be time invariant to fully exploit the benefits of this method, therefore it is harder to have and adaptive system unless feedback from the receiver is implemented which is not always feasible.

Following is an AWGN sequence and last is the decision element that converts the data into the correct logic levels and outputs a chain of detected symbols $\hat{I}_n$.

1. Equalizer Structures

Equalization can be realized in either the discrete or continuous domain. Discrete time equalizers can offer powerful equalization at the cost of reduced speed since they are typically implemented in a DSP and thus are limited to the speed of the former; increasing the frequency of operation of the DSP in order to cover higher frequency ranges means that a high speed quantizer and large digital cells are required. Consequently, the power consumption of the circuit becomes impractical to implement. On the other hand, analog equalizers offer an attractive alternative solution to this problem. They can achieve high speeds with smaller and less power-consuming blocks. Their main drawback is the fact that they require analog building blocks and, thus, they become sensitive to process, voltage and temperature (PVT) variations than their digital counterpart.

a. Feed-Forward Equalization

Over the years one of the simplest and most used equalization techniques has been linear feed forward equalization (FFE). This technique usually involves the use of a linear transversal finite impulse response filter (FIR) as shown in figure 14. The term finite relates to the fact that its response to an impulse ultimately settles to zero. The FIR consists of adjustable tap coefficients $c_0 - c_4$ and a discrete or continuous unit delay z^{-1} between each tap. The amount of delay τ that each z^{-1} represents can be as large as the symbol period T_B, which is often referred as a symbol spaced equalizer. If $\tau < T_B$ the equalizer is called a fractionally spaced equalizer (FSE). According to the Nyquist criterion, in order to avoid aliasing the sampling frequency $f_S = 1/\tau$, has to be greater

than two times the maximum channel bandwidth BW (i.e. $f_S > 2BW$) in other words the value of τ needs to be smaller than half the bit period T_B (i.e. $\tau < T_B/2$).

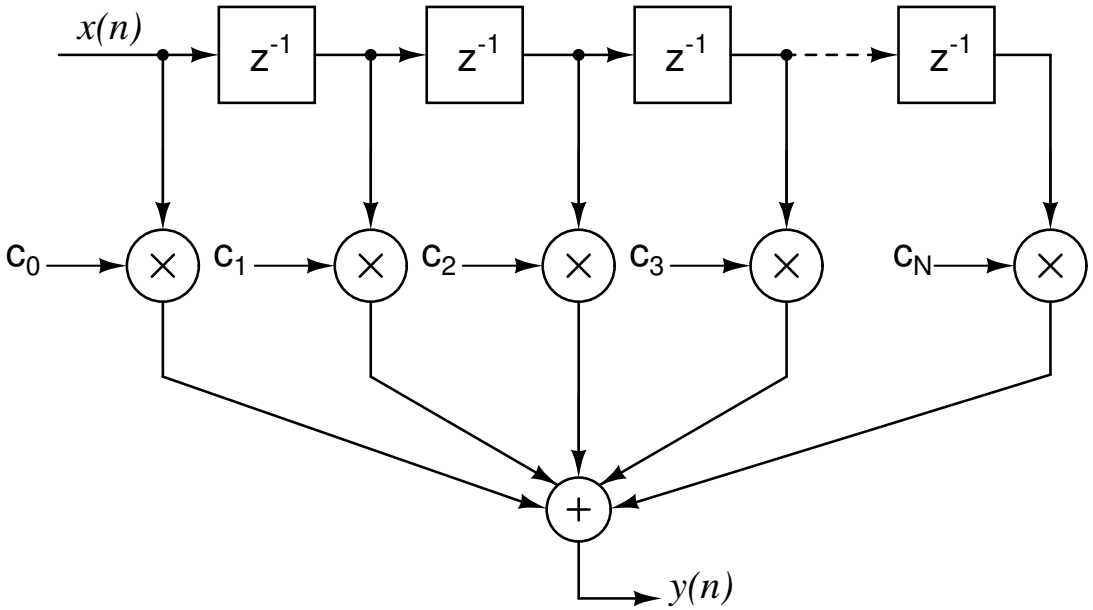

Figure 14. Finite Impulse Response Filter.

The impulse response of the filter $h[n]$ can be found by letting the input $x[n] = \delta[n]$, thus

$$h[n] = \sum_{i=0}^{N} c_i \delta[n-i] = \begin{cases} c_n \,, n = 0,1,2,...,N \\ 0 \,, otherwise \end{cases} \tag{2.17}$$

Taking the Z transform of $h[n]$ yields,

$$H(z) = \sum_{n=0}^{N} c_n z^{-n} \tag{2.18}$$

From equation 2.17 it is clear that the output of the FIR is the summation of a weighted version of the input signal with weighted and delayed versions of itself. With proper

selection of the tap gains this type of equalizer can be used to cancel precursor ISI, postcursor ISI or both. The simplest method to obtain the tap coefficients is to satisfy equation 2.17 (chapter I, section C), this can be achieved using the Zero-Forcing algorithm (ZF) and is often referred to as zero forcing equalization [7, 8]. To illustrate ZF equalization, assume that a two tap filter is required to equalize a channel with impulse response,

$$h(t) = \begin{cases} e^{-\omega t} & t \geq 0 \\ 0 & else, \end{cases} \tag{2.19}$$

Assuming a sampling period *T*, the discrete domain impulse response can be expressed as,

$$h(n) = 1 + e^{-\omega T}\delta[n-1] + e^{-2\omega T}\delta[n-2] + \ldots \tag{2.20}$$

Thus,

$$\begin{aligned} H(z) &= 1 + e^{-\omega T}z^{-1} + e^{-2\omega T}z^{-2} + \ldots \\ &= \sum_{n=0}^{\infty}\left(e^{-\omega T}z^{-1}\right)^n \end{aligned} \tag{2.21}$$

The sum of the power series in equation 2.5 converges to,

$$H(z) = \frac{z}{z - e^{-\omega T}} \tag{2.22}$$

So the equalizer transfer function becomes $E(z) = 1/H(z) = 1 - e^{-\omega T}z^{-1}$. The coefficients of the two tap equalizer are $c_0 = 1$ and $c_1 = -e^{-\omega T}$. Despite the simplicity of the ZF method it increases the gain in the frequency range where the channel response is limited, e.g. zeroes in the transfer function, thus any additive noise will be amplified by

the filter yielding poor SNR. There are various methods reported in literature that try to avoid the ZF condition to obtain the tap gains, among these we can mention, recursive least squares (RLS) [7, 8], least mean squares (LMS) [7, 8], random search algorithm [9], sign-sign LMS [10], etc. In spite of all these methods, the FFE structure still amplifies noise in channels with spectral nulls or zeroes resulting in poor SNR. Therefore, non-linear equalizers such as decision feedback equalizers (DFE) have been used to address this subject.

b. Decision-Feedback Equalization

Decision feedback equalization/equalizer (DFE) was first introduced by M. E. Austin in 1967 [6]. This decision theory approach tries to use knowledge from previous detected symbols to cancel post-cursor ISI on the current symbol. Depicted in figure 15 is the block diagram of the DFE.

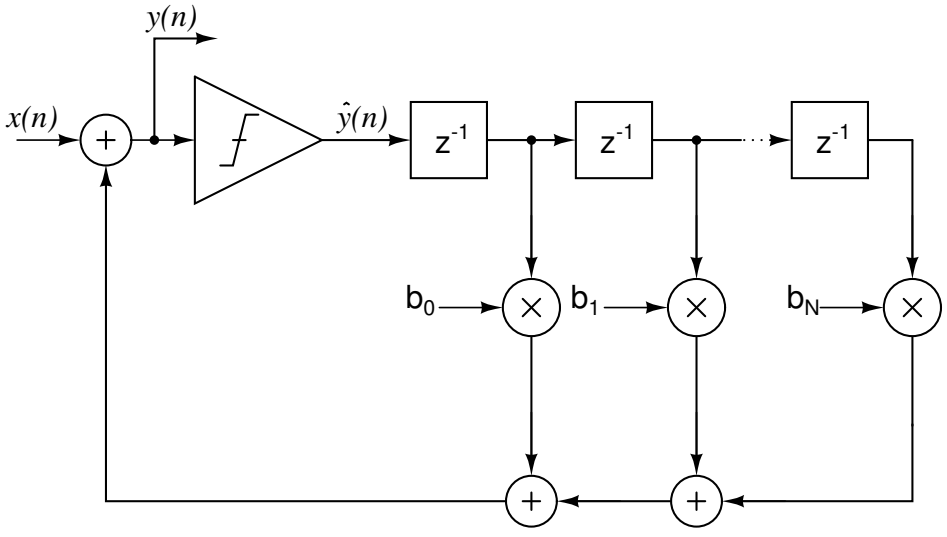

Figure 15. Decision Feedback Equalizer.

The output of the DFE is given by,

$$y(n) = x(n) - \sum_{k=1}^{N} b_k \hat{y}(n-k) \tag{2.23}$$

Since the equalizer works on detected data, assuming a correct decision was taken by the slicer, it uses information from previous symbols to correct the current symbol. The operation of the DFE can be understood by observing figure 16. Assuming that the channel is a linear, and time invariant (LTI) system, the overall impulse response is the superimposed contribution of all the other responses at different sample times, thus the impulse response of the filter can be written as $H[z] = [0.3 \;\; 0.6 \;\; 1 \;\; 0.6 \;\; 0.3]$. In figure 15, h[n] is the current symbol, h[n-1] and h[n-2] are the precursor ISI and h[n+1] and h[n+2] are the post cursor ISI. The DFE operates on the current symbol and subsequent symbols, thus the precursor ISI remains intact after equalization. For example, assume that a two tap DFE is used to equalize the channel in figure 15, the goal is to remove al post-cursor ISI by forcing h[n+1] and h[n+2] to be zero. The first sample to arrive at the equalizer input is the desired information h[n] = 1 thus the output y[0] = 1 and the detected symbol $\hat{y}[0] = 1$ (assume that the slicer toggles between 0 and 1 for simplicity). After a sampling period has passed, h[n+1] arrives at the input and adds to $\hat{y}[0]b_0$ which has already propagated through the equalizer thus,

$$\begin{aligned} y[1] &= h[n+1] + \hat{y}[0] \cdot b_0 = 0 \\ b_0 &= -h[n+1] = -0.6 \end{aligned} \tag{2.24}$$

Following a similar approach b_1 = -h[n+2] =-0.3 thus the equalizer coefficients are [-0.6, -0.3].

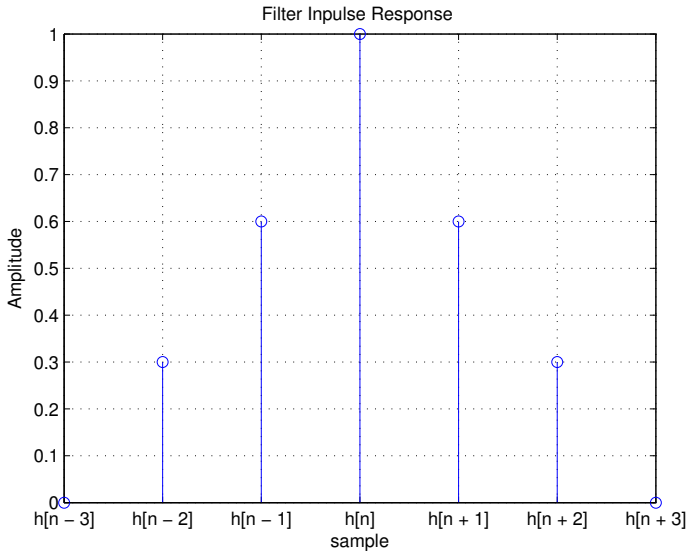

Figure 16. Channel impulse response without equalization.

From equation 2.23 it is evident that all post-cursor ISI can be removed using a DFE however the entire precursor ISI remains present in the detected symbol. This is the major disadvantage of a DFE when compared with an FFE. Since the DFE operates on recovered data the input eye to the DFE has to have some opening or the decision element can make erroneous decisions that propagate along the DFE. To avoid propagating an error in many practical applications a FFE precedes the DFE thus a DFE is generally composed of a feed-forward linear part, a linear feedback part and a non-linear decision element as shown in figure 17.

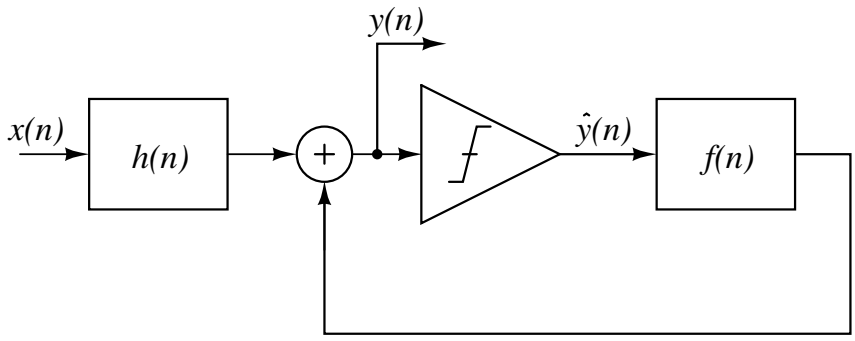

Figure 17. Decision Feedback Equalizer practical implementation .

In the structure depicted in figure 16 the feed-forward filter *h(n)* is usually utilized to remove precursor ISI while the feedback filter *f(n)* is used to cancel post-cursor ISI. By doing this the number of taps required for the FFE is smaller than in the case where the FFE is used to remove pre and post-cursor ISI. The total number of taps combining the DFE and the FFE depend on the channel and can be calculated using system level simulations and defining a desired figure of merit (i.e. eye opening, jitter). The main advantage of working with data that has been detected by the slicer is that the DFE does not amplify noise like in the case of a FFE. Another significant advantage over the FFE is that since the DFE is processing binary valued data, it can be implemented using digital building blocks, for example the delay elements can be current mode logic (CML) cells plus the multipliers do not have to deal with analog valued signals. When the DFE and FFE are used together as shown in figure 16 the feed-forward part is usually a FSE while the DFE is working at the symbol rate. As in the case of an FFE, the delay or sampling period τ of the DFE can be equal to the bit period

$\tau = T_B$ resulting in a symbol spaced DFE or can be made smaller $\tau < T_B$ resulting in a fractionally spaced DFE.

After both architectures where considered, the FFE was chosen over DFE because of reduced complexity. The DFE requires two FFE's and a slicer to completely remove ISI while only one FFE is required to accomplish the same goal. Recall the channel impulse response depicted in figure 16, assume a three tap FFE is required to remove pre and post-cursor ISI, namely h[n-1] and h[n+1]. Using zero forcing conditions the filter weights can be found as follows,

$$\begin{aligned} y[n] &= h[n]\cdot c_0 + h[n-1]\cdot c_1 + h[n-2]\cdot c_2 \\ y[0] &= 1\cdot c_0 + 0.6\cdot c_1 + 0.3\cdot c_2 = 0 \\ y[1] &= 0.6\cdot c_0 + 1\cdot c_1 + 0.6\cdot c_2 = 1 \\ y[2] &= 0.3\cdot c_0 + 0.6\cdot c_1 + 1\cdot c_2 = 0 \end{aligned} \tag{2.25}$$

Hence the filter coefficients are c_0 = -1.03, c_1 = 2.24, c_2 = -1.03. The remaining ISI components can be cancelled by increasing the order of the filter which is equal to the number of taps. In the case of a DFE increasing the taps will only reduce the post-cursor ISI contribution, besides in a DFE more computations are needed to calculate all the coefficients for the two filters.

The basic operation of the FFE, the main limitations, and the mathematical background where given herein this chapter. In the next chapter the analysis and design of an analog FFE will be discussed from a system level perspective. The main limitations such as noise and bandwidth along with practical CMOS implementation will be addressed.

CHAPTER III

IMPLEMENTATION AND LIMITATIONS OF AN ANALOG FFE

In modern CMOS technologies the implementation of high speed transversal equalizer represents a big challenge due to the ever increasing data communication rates. In this chapter the main limitations and building blocks of an FIR (see figure 14) will be discussed. As a final remark the effect of noise on bit error rate will be explored to establish the required SNR of the filter.

A. Delay Lines

As mentioned before the unit delays or delay lines can be discrete or continuous. The goal of both types is to delay the signal an amount of time τ but they differ in the way they accomplish this. In the case of a discrete implementation the delay element is sampled at a rate equal to $1/\tau$ while in the continuous case the signal is delayed by the group delay of the filter.

1. Sampled Delay Lines

The simplest sampled delay line is a unity gain sample and hold as S/H depicted in figure 18.

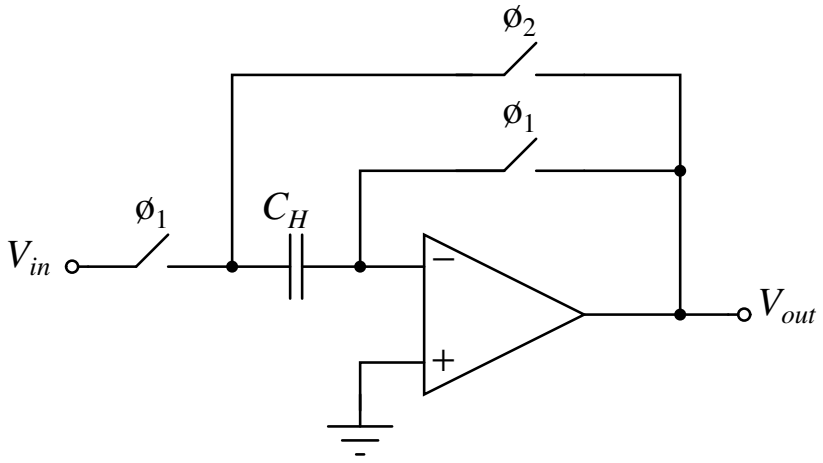

Figure 18. Unity sample and hold.

The cell in figure 18 can be cascaded to implement the unit delays required in an FIR. The main drawback in this topology is the speed at which the amplifier has to react which imposes a huge challenge in the gain bandwidth product (GBW) of the amplifier. There are also several issues regarding the CMOS switches, among these, clock feed-trough, switch on-resistance and resistance nonlinearities. Due to all these short comings the maximum operating speed of this cell is limited to a few hundreds MHz [11].

To circumvent these issues, various topologies have been reported in [12, 13]. The method proposed in [12, 13] is depicted below in figure 19, the main goal is to divide each delay cell into an array of *N* parallel sub-samplers that work at f_{clk}/N. This method reduces the frequency at which the S/H circuits have to work by a factor *N*; nonetheless they increase the circuit area and power by a factor *N* as well. Time interleaved techniques were proposed in [14] but they also suffer from the limitations mentioned above.

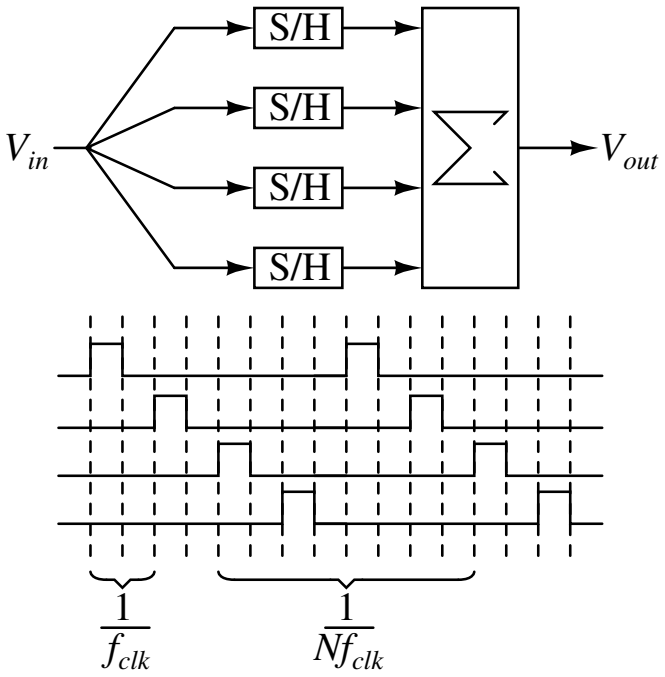

Figure 19. Parallel array of sample and hold elements.

2. Continuous Delay Lines

Continuous delay lines offer an attractive alternative in terms of power consumption, area and circuit complexity. Recently substantial use of continuous delay lines have been reported in equalizers working at speeds higher than 1 Gb/s [6, 9, 11, 15, 16, 17]. An ideal continuous delay line should delay the input signal without adding any attenuation or any form of distortion. Consider the following system,

$$H(j\omega) = |H(j\omega)|e^{j\phi} = |H(j\omega)|e^{-j\omega T_s} \tag{3.1}$$

According to the constraints stated above for an ideal delay line, the magnitude of the system $|H(j\omega)|$ has to be equal to 1 V/V or 0 dB for all the bandwidth of interest which is half the symbol rate (most of the frequency content of the data is confined to half the

symbol rate). The phase response $\phi = -\omega T = 2\pi f T_s$, where T_s is the equivalent sampling period of the equalizer, is linked to the delay of the system τ by the following relationship,

$$\tau = \frac{\phi}{2\pi} T_{Signal} \tag{3.2}$$

where T_{Signal} is the period of the signal going trough the system. To have a constant delay over the bandwidth of interest the phase response has to be linear and inversely proportional to frequency. If the phase response decays linearly with frequency the transit time of each signal going through the system will be the same regardless of its frequency. The transit time of a system is characteristic to the system and it is known as the group delay of the system. The group delay measures the linearity of the phase response of a system and it can be calculated by differentiating the phase response of the system versus the frequency on a linear scale. Hence the group delay can be expressed as,

$$\tau_G = -\frac{d\phi(\omega)}{d\omega} \tag{3.3}$$

where $\phi(\omega)$ is the total phase shift in radians, and ω is the angular frequency in radians per unit time, equal to $2\pi f$, where f is the frequency (hertz if group delay is measured in seconds).

For instance, consider a first order system $H(j\omega)$ with a pole located at ω_p and thus a transfer function given by,

$$H(j\omega) = \frac{1}{1 + \frac{j\omega}{\omega_p}} \tag{3.4}$$

For such system the channel magnitude response can be expressed as,

$$|H(j\omega)| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_p}\right)^2}} \tag{3.5}$$

Similarly the phase response can be expressed as,

$$\phi(\omega) = -\arctan\left(\frac{\omega}{\omega_p}\right) \tag{3.6}$$

Taking the derivative of the phase response to obtain the group delay yields,

$$\tau_G(\omega) = -\frac{d\phi(\omega)}{d\omega} = \frac{1}{\omega_p} \frac{1}{1 + (\omega/\omega_p)^2} \tag{3.7}$$

Depicted below in figure 20 and figure 21 are the magnitude response and group delay of $H(j\omega)$. The frequency axis is normalized to the pole location as ω / ω_P .

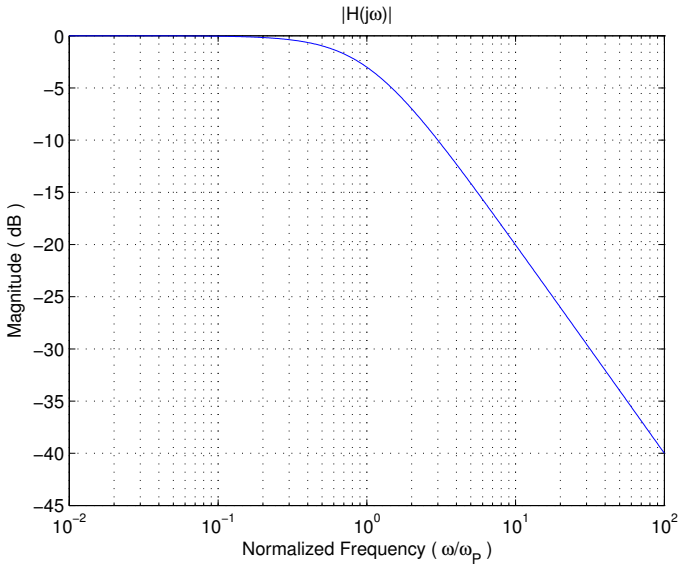

Figure 20. Magnitude response of $H(j\omega)$.

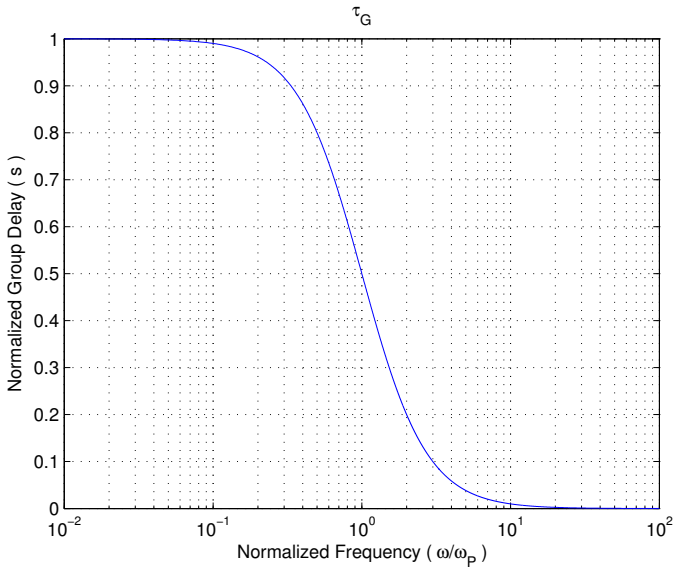

Figure 21. Group delay of $H(j\omega)$.

Figure 21 provides and insight on the group delay of the system and its variation around its -3 dB or cutoff frequency. The system exhibits a variation in group delay of 50% around its cutoff frequency. Group delay variation introduces a phenomenon called

dispersion. Dispersion introduces ISI and will be reflected as a significant decrease in eye opening. Dispersion causes data traveling at frequencies close to the cutoff frequency of the system to have a shorter transit time than data traveling at lower frequencies causing symbols to run into each other thus when the output is sampled some residual energy left from other symbols might be present which results in symbol errors. From this observation it is clear that a first order system cannot meet the stringent bandwidth and group delay flatness requirements essential to broadband delay lines. A cascade of four first order systems was reported in [17]. Each first order module was implemented using simple differential pairs with tunable PMOS loads as shown in figure 22.

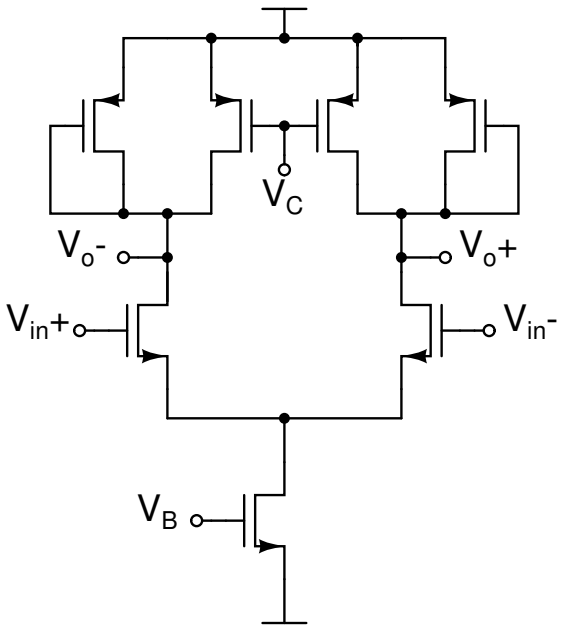

Figure 22. First order module.

The frequency of the pole is determined by the load capacitance and the output resistance which can be adjusted by V_C. The group delay is given by,

$$\tau_G(\omega) = -\frac{d\phi(\omega)}{d\omega} = \frac{4}{\omega_p}\frac{1}{1+(\omega/\omega_p)^2} \tag{3.8}$$

or for N identical stages T/N the required delay can be calculated as follows,

$$\tau_G(0) = \frac{T_B}{N} \tag{3.9}$$

where T_B is the bit period which is the inverse of the bit rate (i.e. $T = 1/R_B$), thus for a $T/4$ equalizer working at 3.125 Gb/s the required group delay is 80 ps. A group delay of 80 ps implies that every unit cell must have their pole located at $\omega_p = 4/\tau_G(0) = 4/80\,\text{ps} = 50\text{Grad/s}$ or 8 GHz. Assuming a load capacitance of 100 fF the maximum resistance allowed is given by,

$$R_L = \frac{1}{2\pi\left(100\times10^{-15}\right)\left(8\times10^{9}\right)} = 200\,\Omega \tag{3.10}$$

Since the gain of the circuit is $A_{DC} = g_m R_L$ the required transconductance for a 0 dB gain is equal to 5 mS. The value of transconductance imposes a challenge in terms of linearity and power consumption due to the large peak currents that the input transistor has to handle without leaving the saturation region. One of the shortcomings of using this topology is the placement of the pole. To allocate the poles at the required -3 dB

frequency of each inverter, a reasonable amount of power has to be spent. Another fundamental limitation arises from the first order nature of each element, even though they might be cascaded, the group delay is inversely proportional to the cutoff frequency of the filter which introduces a tradeoff between bandwidth and group delay, thus making this topology not suitable for high speed operation.

In [16], the authors implemented the delay lines by using emulated transmission lines T.L. Recall from section B chapter II, that a transmission line has very small phase distortion throughout the whole bandwidth of operation. Because large group delays are required in equalizers working at speeds below 10 Gb/s, physical transmission lines will result in impractical lengths for on-chip implementation [16]. To circumvent this limitation, monolithic inductors and capacitors are used to emulate the T.L. as shown in figure 23.

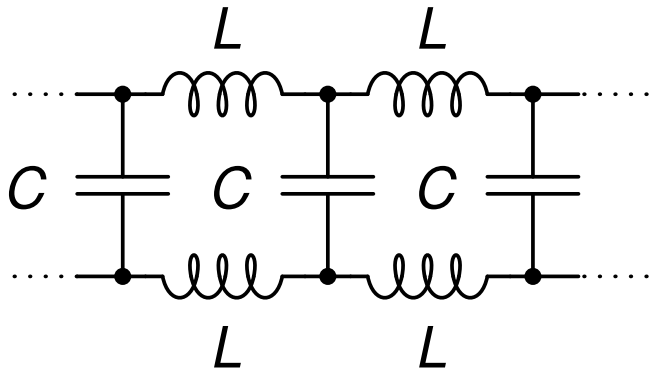

Figure 23. Emulated transmission line.

According to [11] this method exhibits a variation of more than 50% in group delay around the cutoff frequency of the filter. In order to have flatter group delay and

magnitude response the number of LC sections needed to emulate the T.L. tends to infinity [11]. Another disadvantage of emulating the T.L. with passive LC elements is the lack of tuning that the delay has. This imposes a limitation if the delay has to be adjusted due to PVT variations or to adjust the transfer function of the filter.

In [11], the delay lines were implemented using third order linear phase equirriple filter approximation. Each filter was a current mode LC ladder as depicted below in figure 24. Since the target speed was 1 Gb/s, the delay line required an inductor beyond 100 nH. To circumvent this, active inductor emulation based on Gm-C gyrators was employed as shown in figure 25.

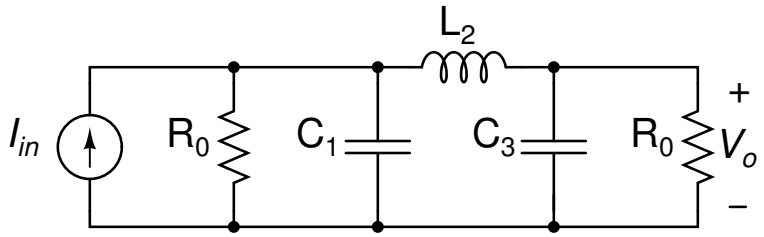

Figure 24. Third order current mode LC ladder prototype.

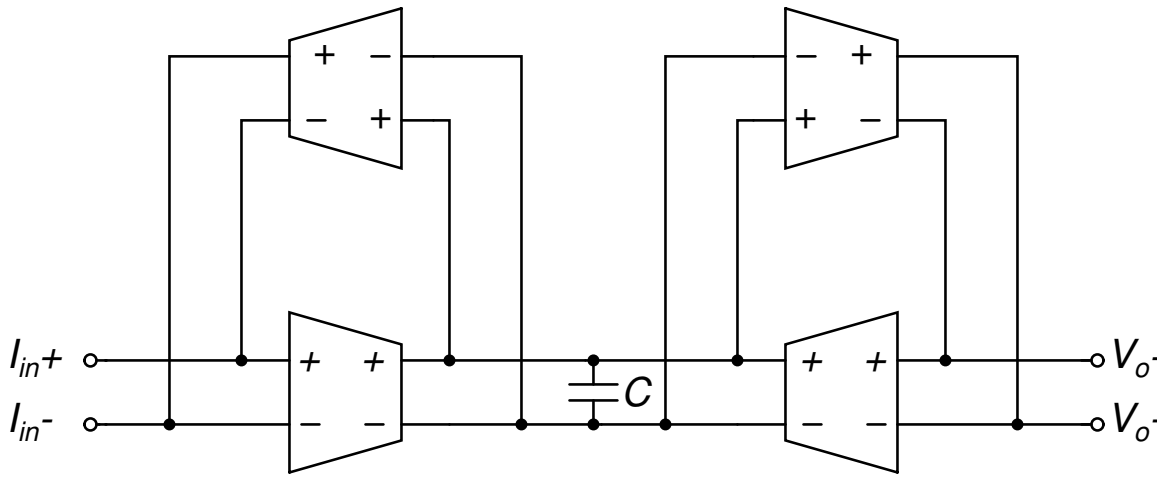

Figure 25. Fully differential floating active inductor.

The magnitude and phase response are shown in figure 26. The 3 dB frequency of the filter is 3.5 GHz which is sufficient for a 3.125 Gb/s data rate. The group delay is also constant throughout the whole band which is desired. These simulations where carried out in Cadence using Ideal components and the values are tabulated below in table II.

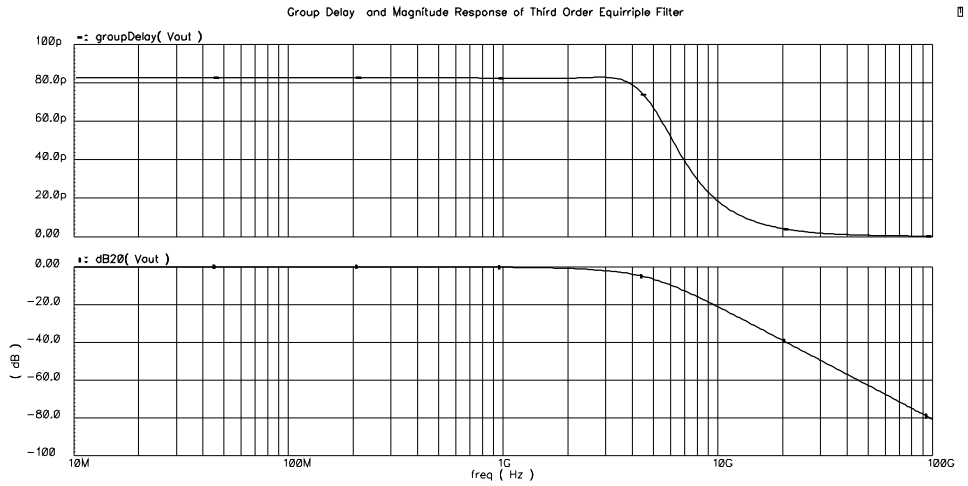

Figure 26. Group delay and magnitude response of 3rd order equirriple filter.

Table – II. Third order equirriple filter component values .

Component	Value
R_o	500 Ω
C_1	38.4 fF
L_2	23.2 nH
C_3	200 fF

The required value for C_1 is too small to ensure its absolute value after fabrication plus it is comparable to transistor parasitic capacitances. Recall that for an LC ladder design the component values can be found using the following [18],

$$C_i = \frac{g_{n,i}}{R_O \omega_C} \tag{3.11}$$

$$L_i = \frac{g_{n,i} R_O}{\omega_C} \tag{3.12}$$

where ω_C is the denormalization frequency, $g_{n,i}$ are the normalized filter component values and R_O is the termination resistance chosen. Therefore to increase the value of C_1 to at least 100 fF the termination resistance has to be decreased by 2.5 times (i.e. R_O = 200 Ω). Decreasing R_O will decrease the inductance to values that can be realized on chip, see figure 27.

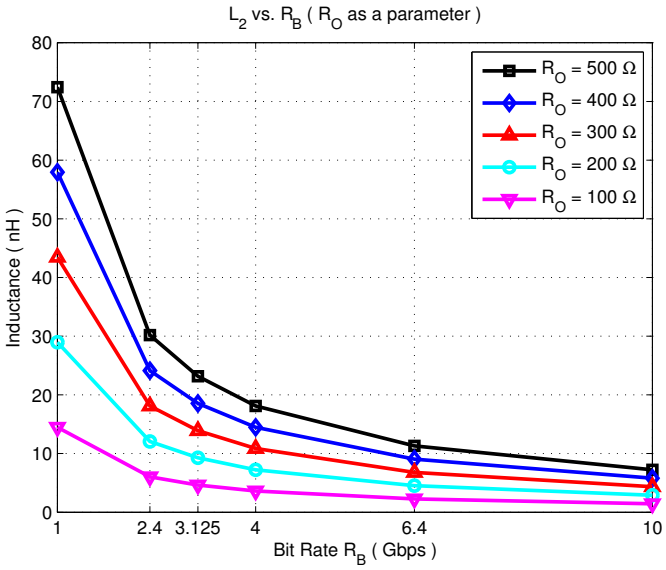

Figure 27. Required inductance of inductor L_2.

The value of R_O cannot be arbitrarily small, bear in mind that the input to the system is voltage thus an input transconductor is needed to convert the transmitted voltage into current that can be used by the current mode filter as shown below in figure 28. Given the nature of the lossy LC Ladder, the transfer function of the delay line at low frequencies will be -6 dB since it is basically the parallel combination of the input and output resistances. Hence, in order to have a gain of 0 dB for an R_O of 200 Ω the input transconductor has to provide a $g_{mi} = 2/R_O = 10\,\text{mS}$.

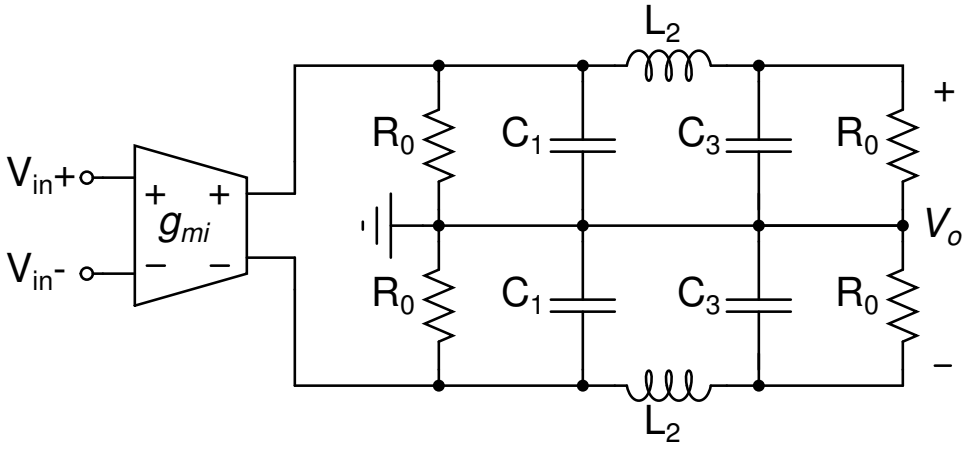

Figure 28. Third order LC ladder filter.

It is worth mentioning that even if the input transconductance is increased to compensate the loss of the ladder, the value of capacitor C_1 will continue to shrink as the frequency of operation increases until it reaches a point where it is again comparable to parasitic capacitances. Also the value of inductor L_2 decreases linearly with frequency to the point where it reaches the sub-nano range which can be easily implemented on chip and outperform its active counterpart in terms of noise and power consumption.

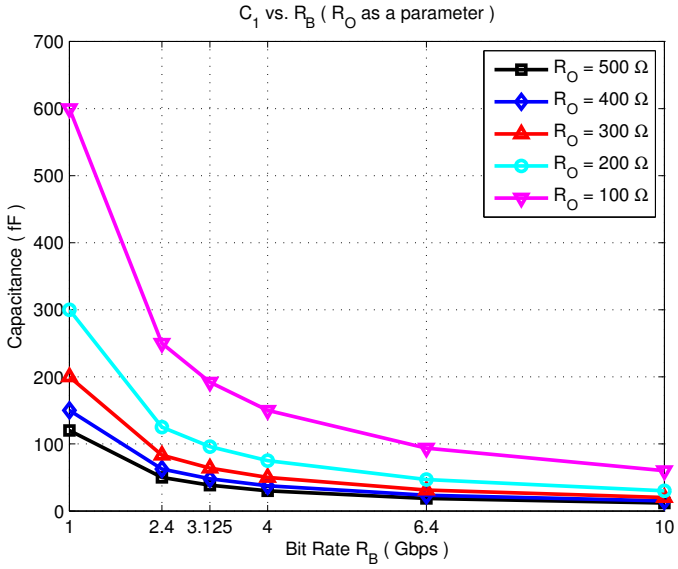

Figure 29. Required capacitance of capacitor C_1.

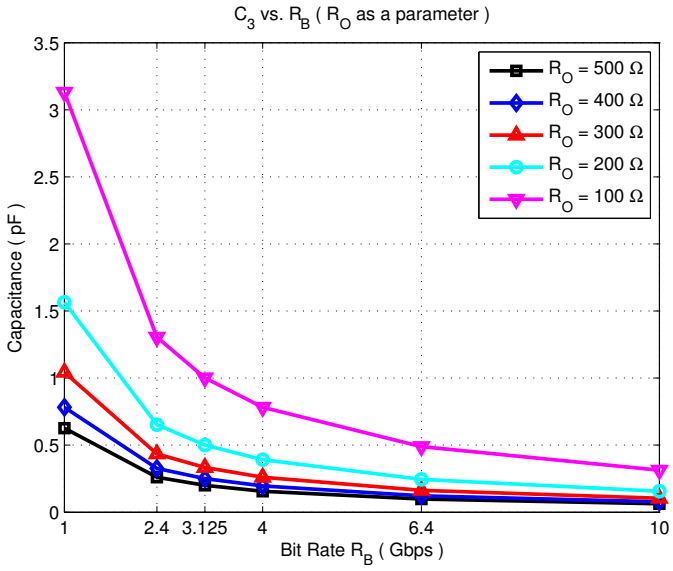

Figure 30. Required capacitance of capacitor C_3.

Figures 29 and 30 depict the required values for C_1 and C_3 across different bit-rates and termination resistance. It becomes clear that this method does not perform well at frequencies beyond 1 to 2 Gb/s at most. The main reason is the required capacitor values in the femto range, as the capacitors shrink the termination resistance has to be increased along with the input transconductance to maintain a gain of 0 dB across the band. The method is best suited for frequencies lower than 1 Gb/s being 1 Gb/s the borderline data rate, beyond 1 Gb/s, the power required to operate the filter makes this topology not viable. It is worth mentioning that as the data rate increases the required values for the inductance reduces to the point where using passive monolithic inductors defeats active inductor emulation.

The main limitations in the implementation of broadband delay elements have been discussed. The delay chosen in this work is an analog delay line based on active feedback and will be discussed in detail in the next chapter. The next blocks required in the equalizer are the multiplier and the adder which will be addressed in the next sub-section.

B. Limitations of Analog Multiplication and Addition

Analog multiplication as it name implies, consists in multiplying two continuous time signals and outputting a continuous time signal that represents the multiplication of the two signals in either voltage or current. In analog multipliers there is usually a control signal and an input signal. The input signal is the signal that is fed into the multiplier and the control signal weights the input signal which results in multiplication, to illustrate this consider the small signal transconductance of an NMOS in saturation region given by,

$$g_m = \sqrt{2\mu_N C_{OX}(W/L)I_D} \tag{3.13}$$

Since the MOS transistor can be considered as a voltage controlled current source where the output current i_o is related to input voltage V_{in} by the transconductace g_m the following expression can be written,

$$i_o = g_m V_{in} \tag{3.14}$$

$$i_o = \sqrt{2\mu_N C_{OX}(W/L)I_D} \cdot V_{in}$$

From equation 3.14 it becomes clear that for a given input voltage V_{in}, the bias current I_D can be used as a control signal to adjust g_m and therefore the output current which is the product of the input voltage times the transconductance. Thus by varying the bias current different multiplication factors can be obtained.

In an analog FIR the multiplication of the signal and its delayed version by the filter weights its usually carried out using four quadrant multipliers, such as the Gilbert Cell [19]. A usual four quadrant multiplier is shown in figure 31.

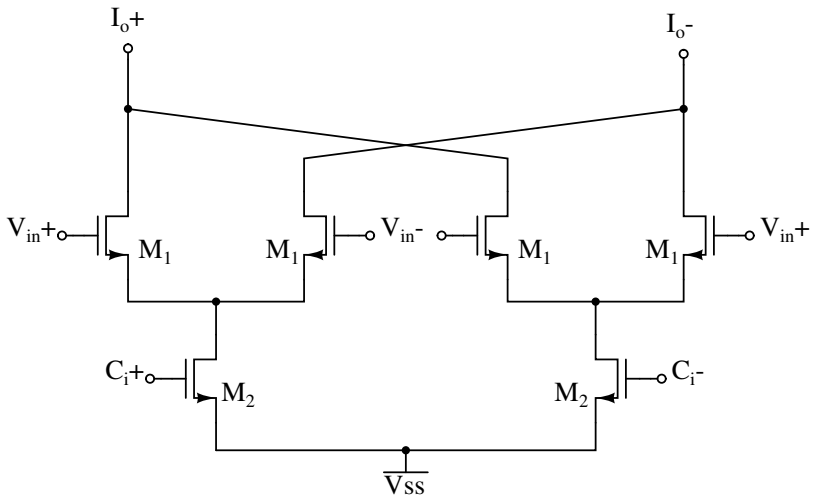

Figure 31. Four quadrant multiplier.

In the analog FIR shown below in figure 32 each multiplier outputs the result of its respective multiplication as a current. The drain coupled nodes (Vo+ and Vo- in figure 32) implement the difference equation of the FIR by adding up the results of all

the multiplications in the current domain. In order to convert this current back into voltage a resistor can be used as shown in figure 32.

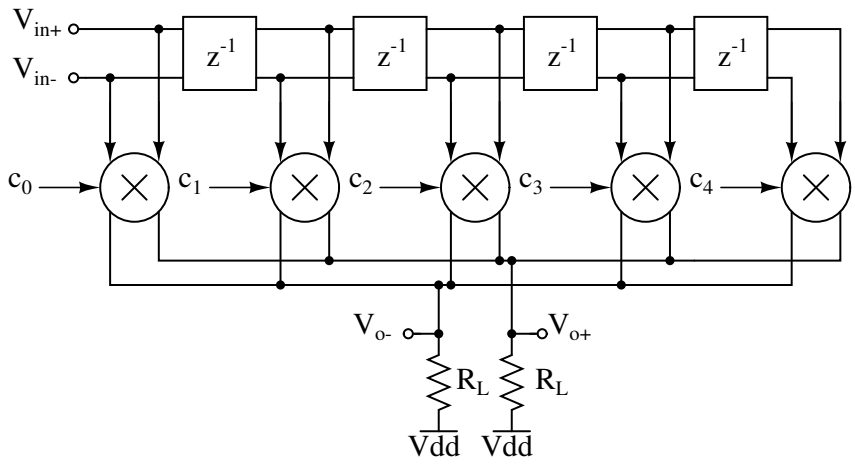

Figure 32. Resistively terminated FIR.

One of the drawbacks of resistively terminating the multipliers is that it introduces a voltage drop that can be substantially high depending on the sum of the bias current on the multipliers. This might be troublesome however the main disadvantage of using a resistor as the current to voltage converter is that due to all the parasitic capacitance C_p, it introduces a pole at [11],

$$\omega_p = \frac{1}{R_L \sum C_p} \tag{3.15}$$

The location of this pole is critical since it defines the bandwidth of the equalizer hence the maximum number of taps allowable. To measure the bandwidth of the equalizer, all the coefficients have to made zero except for the first one (c_0 from figure 30). Now the differential output voltage V_{od}, of the equalizer can be written as,

$$V_o^+ - V_o^- = V_{od} = \left(i_o^+ - i_o^-\right)R_L = i_{od}R_L \tag{3.16}$$

where i_{od} represents the differential output current of the multiplier. Combining 3.14 and 3.16 the differential output current can be expressed as,

$$i_{od} = \left(V_i^+ - V_i^-\right)\left(g_{m1L} - g_{m1R}\right) = V_{id}\left(g_{m1L} - g_{m1R}\right) \tag{3.17}$$

where V_{id} is the differential input voltage applied to the top differential pairs comprised of M_1 in figure 30, g_{m1L} and g_{m1R} represent the transconductace of the left and right differential pairs respectively. Recall that for a MOSFET in saturation the small signal transconductance can be expressed as [19],

$$g_{m1L} = \sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}\frac{I_{TL}}{2}} \quad \& \quad g_{m1R} = \sqrt{2\mu_n C_{ox}\frac{W_1}{L_1}\frac{I_{TR}}{2}} \tag{3.18}$$

where I_{TL} and I_{TR} are the left and right tail currents coming from the bottom transistors M_2 in figure 30. Now assuming that the bottom differential pair M_2 is saturated the tail current I_T can be written as,

$$I_{TL} = \frac{\mu_n C_{ox}}{2}\frac{W_2}{L_2}\left(V_{C0}^+ - V_T\right)^2 \quad \& \quad I_{TR} = \frac{\mu_n C_{ox}}{2}\frac{W_2}{L_2}\left(V_{C0}^- - V_T\right)^2 \tag{3.19}$$

Combining equations 3.17, 3.18, and 3.19, the differential output voltage can be expressed as

$$V_{od} = \underbrace{\frac{\mu_n C_{ox}}{\sqrt{2}}\sqrt{\frac{W_1}{L_1}\frac{W_2}{L_2}}}_{K} V_{id}\left(V_{C0}^{+} - V_{C0}^{-}\right)R_L = K V_{id}\left(V_{C0d}\right)R_L \tag{3.20}$$

where V_{C0d} is the differential control voltage for coefficient c_0. Thus the differential gain of the equalizer can be expressed as,

$$\frac{V_{od}}{V_{id}} = A_{Vd} = K V_{C0d} R_L \tag{3.21}$$

From equation 3.21 it is evident that the gain of the equalizer can be linearly controlled by the tap gains applied as control voltages to the analog multipliers. From equation 3.20 it can also be observed thatt R_L not only introduces a tradeoff between gain and bandwidth it also limits the voltage headroom of the multipliers by $R_L \sum I_{BIAS}$. To circumvent this a transimpedance amplifier (TIA) was proposed as the summing block and it will be further addressed in chapter IV.

C. Signal to Noise Ratio and Bit Error Rate

Inadequate noise levels can disrupt the signal integrity and introduce symbol errors. As mentioned before in chapter II section C, as the data travels trough the channel it picks up unwanted noise $v_n(t)$, to exacerbate this the equalizer is going to introduce some noise to the signal being equalized. To determine the required SNR of the equalizer the impact of its SNR on BER must be studied.

BER is the probability of a bit being misinterpreted due to electrical noise $v_n(t)$. Assuming binary NRZ data (i.e. data toggles between $+V_o$ and $-V_o$) and additive white

Gaussian noise with zero mean, every logic "1" can be defined as $x1(t) = +V_o + v_n(t)$, similarly every logic zero can be defined as $x_0(t) = -V_o + v_n(t)$. Now the total probability which corresponds to the BER can be written as,

$$BER = P(1|0) + P(0|1) \tag{3.22}$$

where $P(1|0)$ is the probability of detecting a logic one when a logic zero was transmitted and is given by [19],

$$P(1|0) = \frac{1}{2}\int_{0}^{+\infty} \frac{1}{\sigma_n\sqrt{2\pi}} \exp\frac{-(x+V_O)^2}{2\sigma_n^2}\,dx \tag{3.23}$$

where σ_n is the standard deviation of the noise. Similarly $P(0|1)$ which is the probability of detecting a logic zero when a logic one was transmitted can be expressed as,

$$P(0|1) = \frac{1}{2}\int_{-\infty}^{0} \frac{1}{\sigma_n\sqrt{2\pi}} \exp\frac{-(x-V_O)^2}{2\sigma_n^2}\,dx \tag{3.24}$$

Assuming that the probability of arrival of logic ones and zeroes is the same, then $P(1|0) = P(0|1)$ and only one needs to be calculated. Performing a change of variables, $u = (x+V_O)/\sigma_n$, simplifies Eq. 3.23 into,

$$\begin{aligned} P(1|0) &= \frac{1}{2}\int_{V_O\sigma_n}^{+\infty} \frac{1}{\sqrt{2\pi}} \exp\frac{-u^2}{2}\,du \\ &= \frac{1}{2}Q\frac{V_O}{\sigma_n} \end{aligned} \tag{3.25}$$

where $Q(x)$ is known as the "Q function" and is defined as,

$$Q(x) = \int_{x}^{\infty} \frac{1}{\sigma_n \sqrt{2\pi}} \exp \frac{-z^2}{2} dz \tag{3.26}$$

Therefore the BER or total probability of error is equal to

$$BER = Q\left(\frac{V_O}{\sigma_n}\right) \tag{3.27}$$

It is worth mentioning that V_O is half the peak to peak voltage of the signal since it was assumed to toggle between $+V_O$ and $-V_O$ and σ_n is the rms value of the noise. Therefore letting $V_{pp} = 2V_O$ Eq. 3.26 can be rewritten as,

$$BER = Q\left(\frac{V_{pp}}{2\sigma_n}\right) \tag{3.28}$$

To evaluate the effect of the SNR on the BER, the SNR at the output of the equalizer (SNR_O for simplicity) can be made equal to $SNR_O = V_{pp}/2\sigma_n$ and the BER can be plotted as a function of the SNR_O as shown below in figure 33. The importance of estimating the BER of the system arises from the limitation imposed by the IEEE standard IEEE802.3 which dictates a minimum BER of 10^{-12} form a 3.125 Gb/s link. BER is also an important metric because it predicts how many errors per day the system will have. Bearing this in mind, a BER of 10-12 or equivalently an SNR equal or greater than 17 dB's was set as the target SNR of the equalizer.

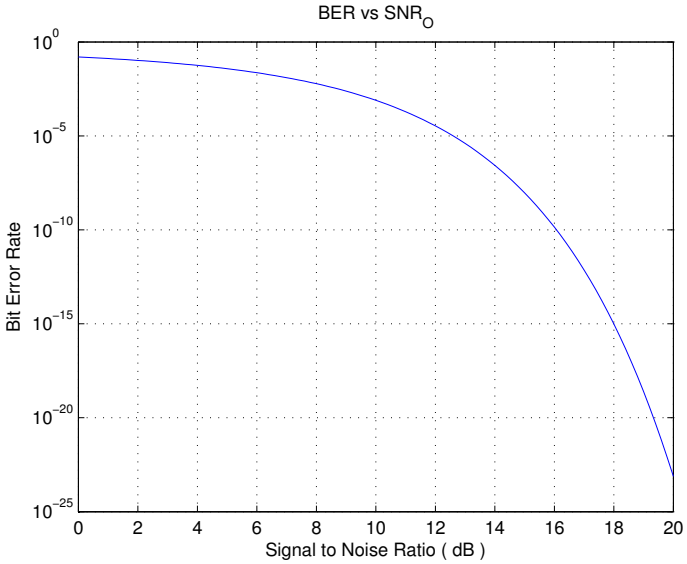

Figure 33. Theoretical BER vs. SNR.

CHAPTER IV

5-TAP 3.125 Gb/s FEEDFORWARD EQUALIZER

This chapter describes the circuit building blocks of the Analog 5 tap FFE, depicted in below in figure 34, schematic level diagrams are given fro all the relevant blocks along with simulation results.

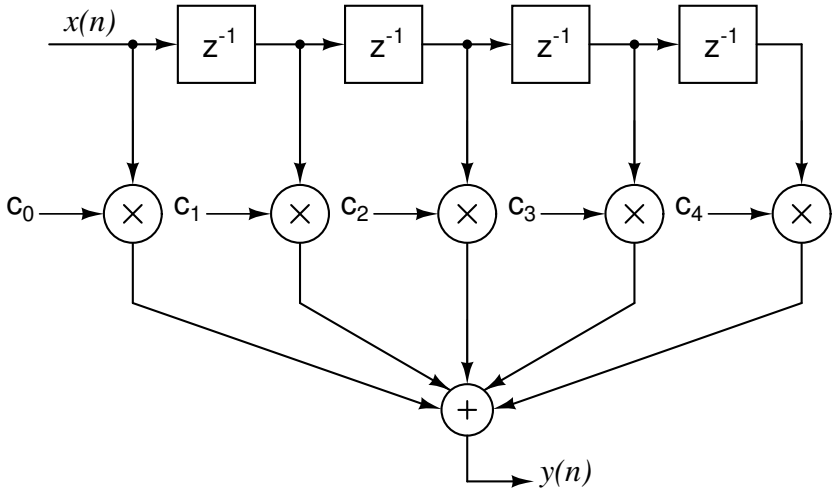

Figure 34. 5 Taps FFE.

The analysis and design of the analog FIR is carried out in this chapter and the simulation results are given for a 3.125 Gb/s equalizer and 4 Gb/s. Even though the equalizer is optimized to work at a bit rate of 3.125 Gb/s, 4 Gb/s was explored for completeness.

As mentioned in chapter III, the main challenge in designing the FFE is the delay cell. It is imperative to ensure a constant magnitude and group delay response

throughout the whole band of operation to avoid introducing ISI. The implementation of the delay cell can be addressed as a linear phase filter design [11]. The order of the filter and the required number of taps play an important role in terms of power consumption. The required number of taps and minimum filter order along with high speed implementation of analog filters will be discussed herein. Another important challenge in the implementation of high speed analog transversal equalizer is the multiplication circuit. The former has to provide linear multiplication and ensure monotonic multiplication across all coefficients to avoid entering into a positive feedback loop and cause divergence of the correction algorithm. The last element in the chain is the summing circuit. As discussed in chapter III, the summing circuits transform the currents coming from the multipliers into a voltage that can be used by subsequent stages (e.g. Slicer circuit). The complexity of the circuit varies from a simple resistor to sophisticated transimpedance amplifiers (TIA). Ideally the TIA should exhibit zero input impedance to drive all the parasitic capacitances connected to the current summation node and zero output impedance to drive the capacitance of any subsequent stage. In practice this is impossible to achieve zero impedance thus the minimum and maximum input and output impedances are selected on a power versus bandwidth perspective. In this chapter a proposed transimpedance summing node will be presented and discussed. Following the analysis of all the building blocks, a summary of results and a comparison between this work and previous work will be provided to evaluate the performance of the designed equalizer.

A. System Building Blocks

1. Delay Lines

In a NRZ communication system, the spectrum of the data will be constrained to frequencies up to half the bit rate since this is the maximum frequency at which the data can toggle between a logic one and a logic zero. Thus an equalizer working at 3.125 Gpbs will have to process data with frequencies up to 1.5625 GHz. To ensure constant group delay and magnitude response a linear phase filter can be used as the delay line as reported in [11]. To minimize circuit complexity and power consumption the order of the filter has to be kept minimal, thus when comparing equirriple, Butterworth and Bessel-Thompson filters the equirriple approximation results in the minimum filter order required. The group delay and magnitude response of linear phase filters with equirriple phase error of 0.05º normalized to 1 radian are depicted below in figures 35 and 36 respectively [18]. A 0.05º phase error was chosen over 0.5º due to its better phase linearity.

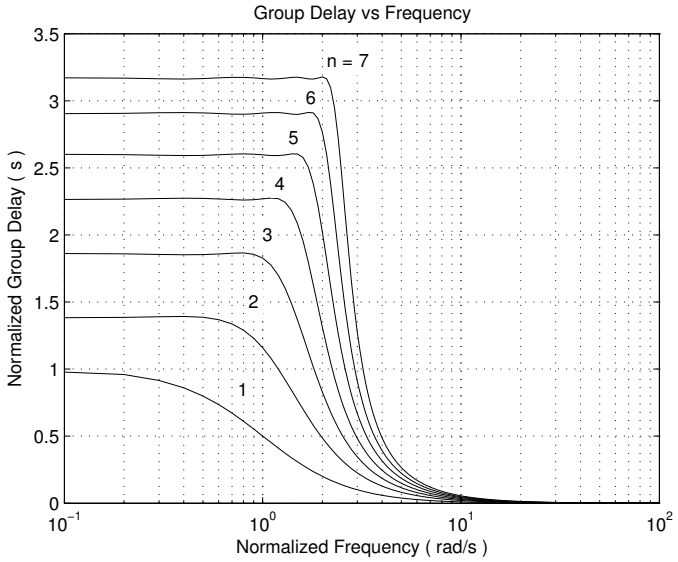

Figure 35. Group delay vs normalized frequency of 0.05º equirriple filters.

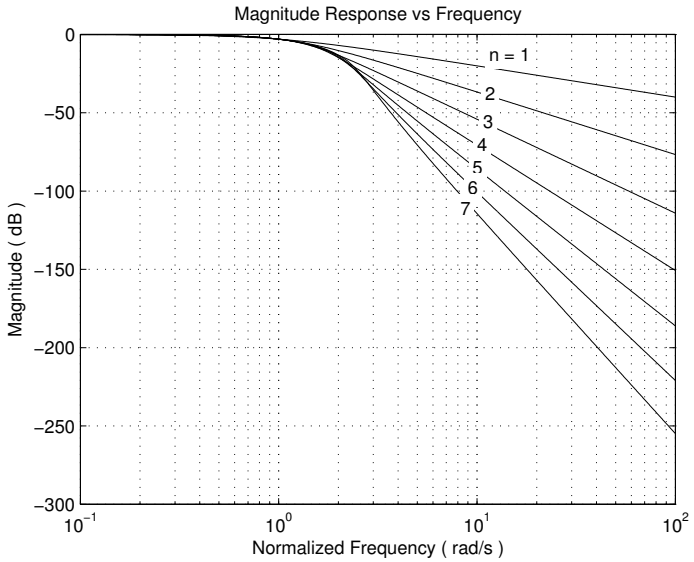

Figure 36. Magnitude vs normalized frequency of 0.05º equirriple filters.

From figure 35 it is clear that in order to have a constant group delay up to the desired normalized bandwidth of 1 radian, the delay line has to be a third order (n = 3) equirriple filter. The normalized pole locations are: $s_{1,2} = 0.8541 \pm j1.0725$, $s_3 = 1.0459$.

The complex poles have a Q of 0.8. For an $T_B/4$ equalizer working at 3.125 Gb/s the equivalent sampling ratio required is 12.5 GHz or a required delay τ of $1/(4R_B) = 1/(4 \cdot 3.125 \times 10^{10}) = 80\,\text{ps}$. Thus from figure 35 the cutoff frequency of the filter can be calculated as follows,

$$\omega_{3dB} = \frac{1.8\,\text{s}}{80\,\text{ps}} \times 1\,\text{rad/s} = 22.5\,\text{G rad/s} \tag{4.1}$$

or equivalently an f_{3dB} = 3.58 GHz.

The complex poles were implemented using a transimpedance active feedback configuration [20] as shown in figure 36.

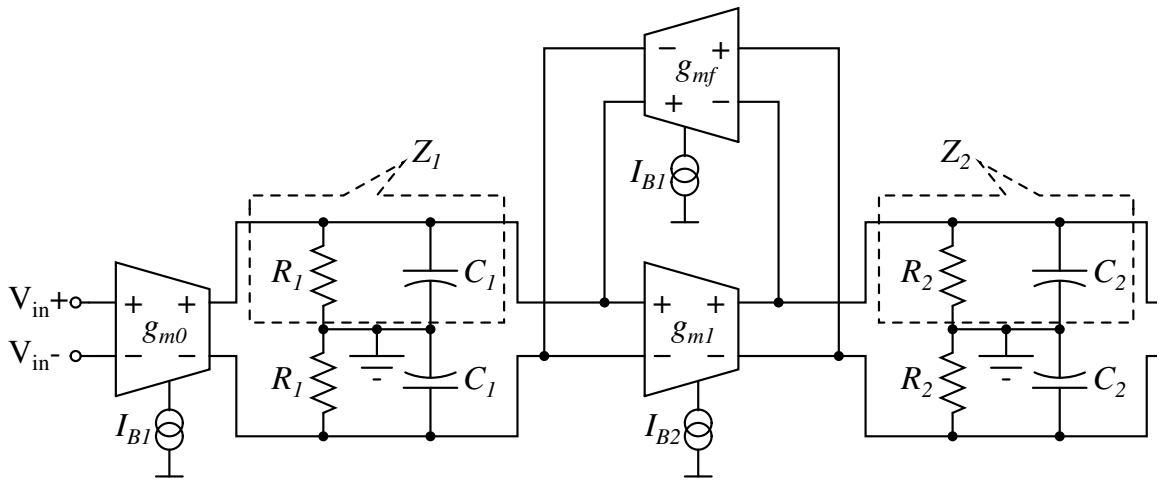

Figure 37. Second order module.

In figure 37 the input transconductor denoted gm_0 converts the input voltage V_{in} into a current that feeds the transipedance filter. To ease the analysis of the second order

module let the impedances Z_1 and Z_2 represent the total resistance and capacitance lumped at the input and output nodes respectively thus,

$$Z_1 = \frac{1}{\frac{1}{R_1} + sC_1} \quad \& \quad Z_2 = \frac{1}{\frac{1}{R_2} + sC_2} \tag{4.2}$$

Transconductor gm_f returns a portion of the output voltage in form of a feedback current that gets subtracted from the current coming from gm_0. An error current resulting from the subtraction of the input current and the feedback current flows into Z_1 creating a voltage that feeds transconductor gm_1 and gets converted into a current that will flow into Z_2 to generate the output voltage V_o. Using Mason's rule the transfer function can be found to be,

$$\frac{V_o}{V_{in}} = \frac{A_{Vo}\omega_n^2}{s^2 + \frac{\omega_n}{Q} + \omega_n^2} \tag{4.3}$$

where,

$$A_{Vo} = \frac{g_{m0} g_{m1} R_1 R_2}{1 + g_{mf} g_{m1} R_1 R_2} \tag{4.4}$$

$$Q = \frac{\sqrt{R_1 R_2 C_1 C_2 \left(1 + g_{mf} g_{m1} R_1 R_2\right)}}{R_1 C_1 + R_2 C_2} \tag{4.5}$$

$$\omega_n = \frac{1 + g_{mf} g_{m1} R_1 R_2}{R_1 R_2 C_1 C_2} \tag{4.6}$$

Since the input current to the transimpedance amplifier composed by transconductors g_{m1} and g_{mf} is equal to $g_{m0}Vi_{in}$, the transimpedance gain Z_{TIA} of the amplifier can be written as,

$$Z_{TIA} = \frac{g_{m1} R_1 R_2}{1 + g_{mf}\, g_{m1} R_1 R_2} \tag{4.7}$$

From equation 4.7 it is clear that for a loop gain $g_{mf}g_{m1}R_1R_2 >> 1$ the transimpedance gain can be approximated by $1/g_{mf}$ which is analogous to the case where resistive feedback is used where the gain is mainly defined by the feedback resistor R_F (See figure 61). One advantage of using a transconductor over a resistor as the feedback element is that the former does not allow any forward transmission (i.e. feed forward) paths that subtracts signal from the output signal reducing the gain. Another advantage is that it the feedback transconductor does not resistively loads the transimpedance stage [20] which provides a degree of freedom when selecting the load resistor R_L in figure 39. Besides all the advantages that using active feedback provides perhaps the most important was demonstrated in [20] where the authors proved that by employing active feedback, the Gain Bandwidth Product (GBW) of the cell depicted in figure 36 increases by factor equal to the ratio of the f_t of the technology and the cell bandwidth, that is,

$$GBW_{NEW} \approx f_t \frac{f_t}{f_{3dB}} \tag{4.8}$$

This result is of utmost importance since it makes this cell suitable for high speed operation and low power consumption.

The transistor level implementation of the second order module is depicted below in figures 38 through 40.

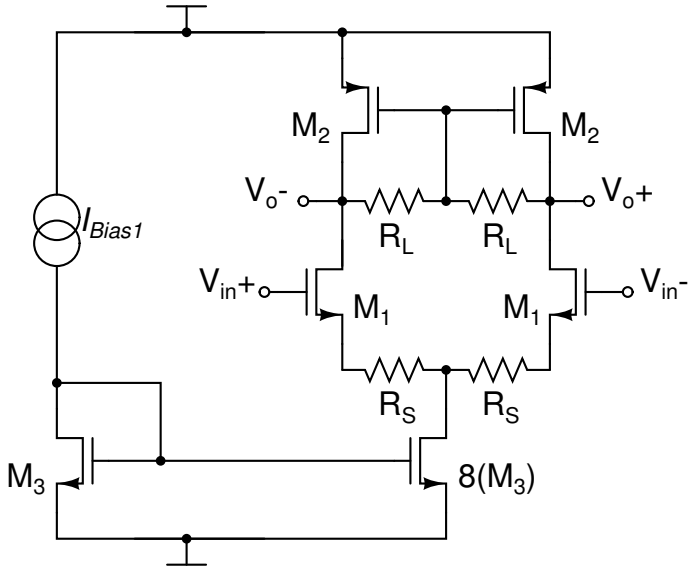

Figure 38. g_{m0}.

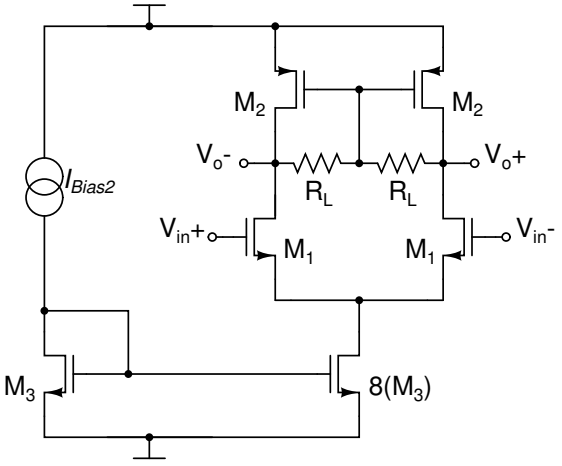

Figure 39. g_{m1}.

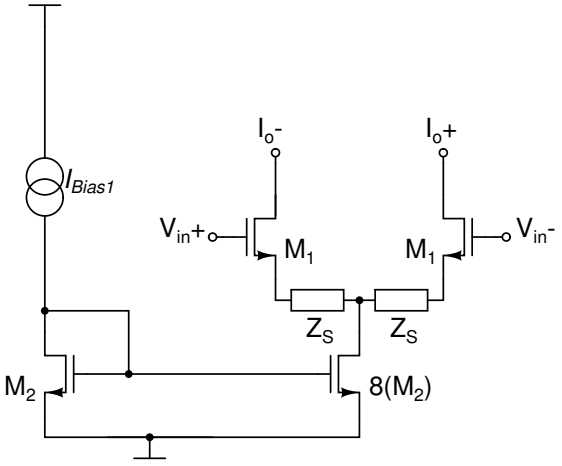

Figure 40. g_{mf}.

The input transconductor (denoted g_{m0} in figure 37) shown in figure 38 is based on a simple differential pair with source degeneration. A simple differential pair was chosen because of its reduced complexity and number of parasitic poles. Source

degeneration was employed to improve linearity given the large input signal of 150 mV_p single ended. Another advantage of source degeneration is that it introduces series-series feedback which increases the bandwidth and reduces the input capacitance by $1 + g_{m0}R_S$ at the expense of reducing the transconductance by the same factor to maintain a constant GBW. Resistor R_L acts as the load resistance and provides local common mode feedback which circumvents the need of a high speed dedicated common mode feedback circuit. A fully differential structure was selected over a pseudo differential one due to the better power supply rejection ratio (PSRR) and better common mode rejection ratio (CMRR). The forward transmission transconductor g_{m1} shown in figure 38 is a scaled version of the input g_{m0}. The gain of this amplifier $g_{m1}R_2$ has to be made as large as possible to avoid any additional loss that a small loop gain might introduce. Before delving on how to increase the gain it is important to analyze the input and output impedances of the transimpedance block. The shunt-shunt feedback loop formed by g_{m1} and g_{mf} in figure 37 introduces impedance gyration thus,

$$Z_{in} = \left[\frac{1}{g_{m1} g_{mf} R_2} + \frac{sC_2}{g_{m1} g_{mf}} \right] \| Z_1 \tag{4.9}$$

$$Z_{out} = \left[\frac{1}{g_{m1} g_{mf} R_1} + \frac{sC_1}{g_{m1} g_{mf}} \right] \| Z_2 \tag{4.10}$$

As can be observed from equations 4.9 and 4.10 the input and output impedances exhibit a resistive part in series with an inductive part. Since the input and output impedance exhibit a similar behavior only the input impedance will be discussed. The

schematic representation of the single ended input impedance is given below in figure 41,

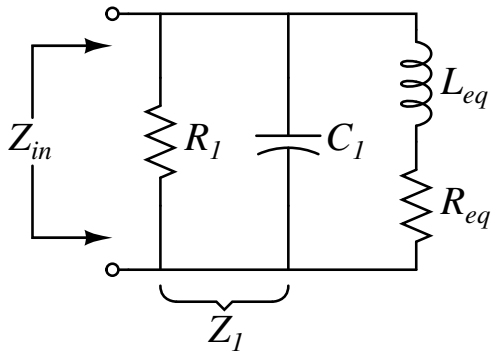

Figure 41. Single ended input impedance.

where, $L_{eq} = sC_2 / g_{m1} g_{mf}$ and $R_{eq} = 1 / g_{m1} g_{mf} R_2$ .The behavior of the impedance can be understood by looking at figure 41. At low frequencies the inductor L_{eq} will act like a short circuit leaving R_{eq} as the total resistance in this branch which is in parallel with an open circuited C_1 and a relatively large resistor R_1, thus at low frequencies the input impedance is approximately R_{eq}. The impedance will continue to increase linearly with frequency until C_1 resonates with L_{eq} at $\omega_o = 1 / \sqrt{L_{eq} C_1}$, at this point the impedance attains its maximum and is purely resistive and is equal to (Appendix A),

$$R = R_1 \parallel R_{eq} \left(1 + \left(\frac{\omega L}{R_{eq}} \right)^2 \right) \tag{4.11}$$

where ω is the frequency in rad/s. After the impedance has attained its maximum it will be dominated by capacitor C_1 and will decay monotonically with frequency, thus from

inspection is evident that the impedance will have a band-pass shape (Appendix A) which is expected. If the input impedance exhibits an excessive peak it means that the Q of the filter is greater than 0.8 and the transfer function of the filter will also exhibit unnecessary peaking. Peaking in the transfer function occur when the complex poles start moving towards the imaginary axis. As the poles get closer to the imaginary axis the Q of the filter increases causing an abrupt change in the phase response which is detrimental to the group delay of the system. To avoid peaking Resistances R_1 and R_2 have to be as large as possible to have enough loop gain and reduce the input & output impedances without adding too much parasitic capacitance. The same applies to the transconductors, the transconductance can be increased by increasing the size of the input devices or by increasing the bias current. Increasing the device size to achieve higher transconductance increases the parasitic capacitance while increasing the bias current increases the power consumption of the cell.

After all these considerations mentioned herein were taken into account a MATLAB script was developed to calculate the required values for the different components. To ease the design of the filter R_1 and R_2 were assumed to be equal as well as C_1 and C_2. The feedback transconductor can be made equal to the input transconductor for a gain of 0 dB and by using equations asdf to asdf the rest of the parameters can be calculated.

The feedback transconductor denoted g_{mf} in figure 37 is an exact replica of the input transconductor g_{m0}. The main difference is that capacitive degeneration was used

to extend the bandwidth of the amplifier. A common source amplifier with capacitive degeneration is shown below in figure 42.

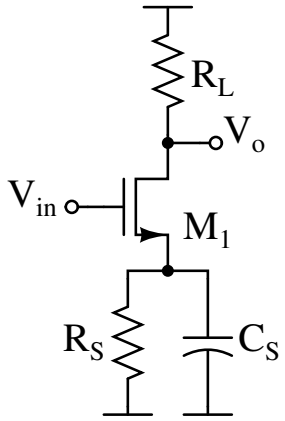

Figure 42. Common source amplifier with capacitive degeneration.

The behavior of this circuit at low frequencies is similar to a conventional source degenerated common source amplifier, however at high frequencies the degeneration capacitor C_S shorts the source of transistor M_1 to ground bypassing the degeneration resistor R_S resulting in a higher transconductance. Carrying out small signal analysis the transcondcutace can be found to be,

$$G_m = \frac{g_m}{1 + g_m\left(R_S \parallel \frac{1}{sC_S}\right)} \tag{4.12}$$

$$= \frac{g_m\left(sR_SC_S + 1\right)}{sR_SC_S + 1 + g_mR_S} \tag{4.13}$$

The transconductance contains a zero at $1/(R_S C_S)$ that can be used to cancel the effect of the pole at $(1+g_m R_S)/(R_S C_S)$ resulting in an extended bandwidth. Simulations were carried out to obtain the required degeneration capacitance; the result is depicted below in figure 43.

To realize the single pole and turn the second order module into a third order system, a 1st order RC low pass filter as shown in figure 44 was used as load. A passive implementation was preferred over an active implementation due to its low power consumption, high linearity, lower noise and ease of implementation.

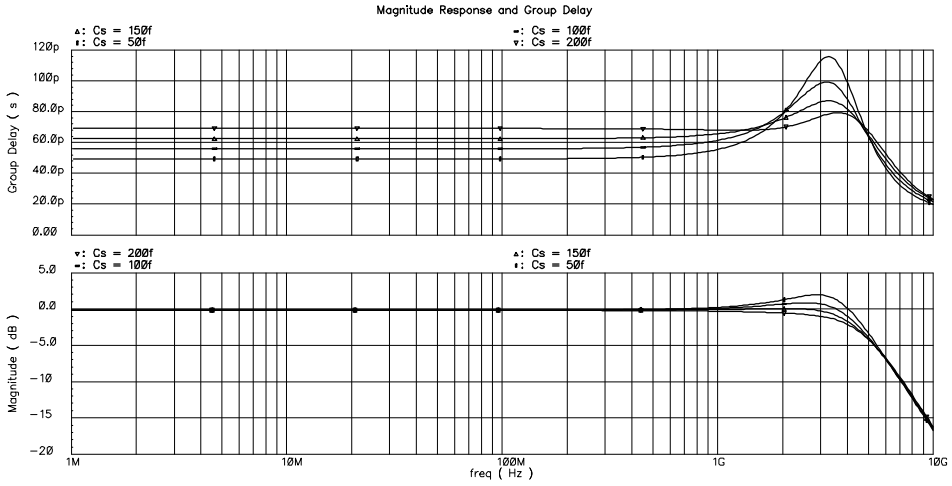

Figure 43. Group delay and magnitude versus degeneration capacitor.

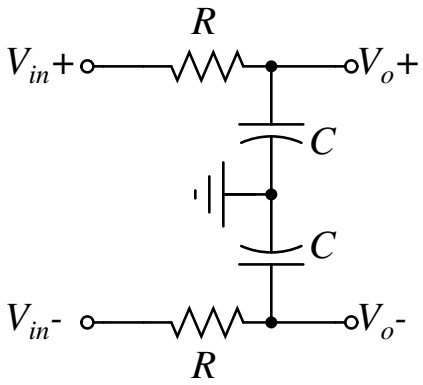

Figure 44. 1st order RC low pass filter.

A single ended representation of the complete delay line is shown below in figure 45.

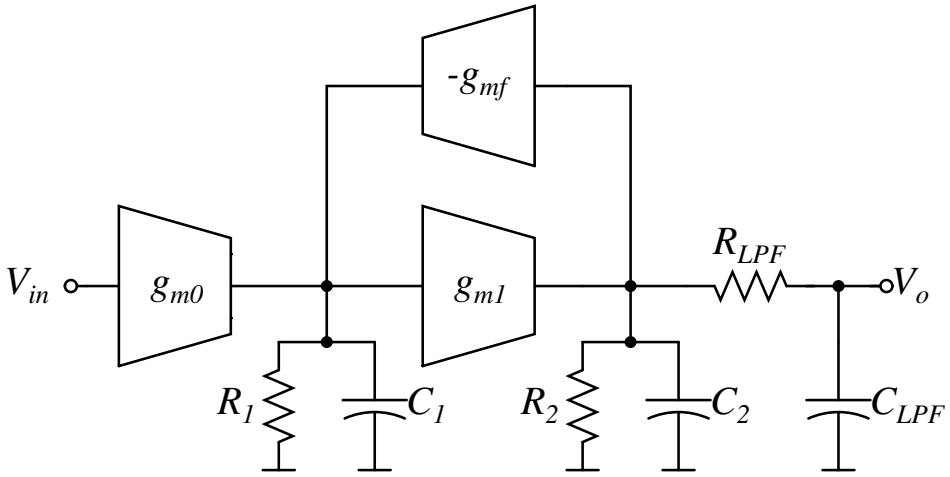

Figure 45. Third order equirriple filter.

Simulations were carried out with an ideal FIR to obtain the optimum delay for required by the channel. After varying the delay from 60 ps to 80 ps the delay where

maximum eye opening was achieved was 70 ps. The simulation results are given below in figure 46 along with the component values tabulated in table III.

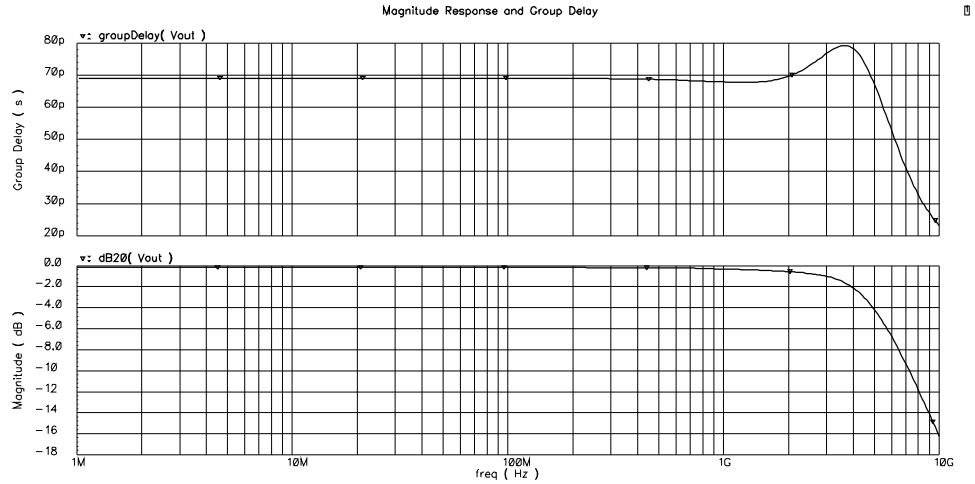

Figure 46. Group delay and magnitude response of third order delay line.

Table – III. Component values for a group delay of 70ps.

Component	Value
g_{mo}	1 mS
g_{m1}	5 mS
g_{mf}	1 mS
C_{LPF}	75 fF
R_{LPF}	220 Ω

The 3 dB bandwidth of the delay line is 4 GHz which is sufficient for a 3.125 Gb/s data rate and the group delay has a variation of less than 10 % up to 2 GHz. To test

the stability of the delay line, a transient simulation was performed and the result is depicted below in figure 47.

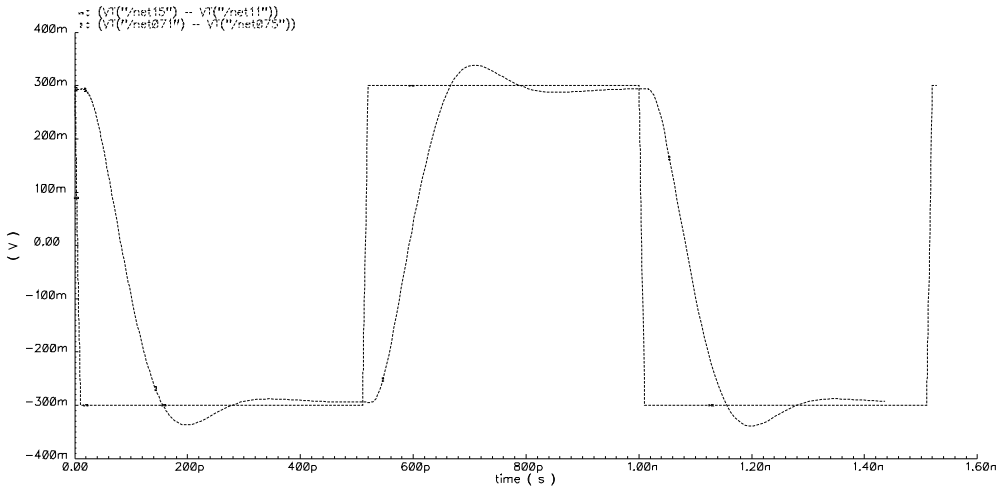

Figure 47. Transient response of the 3rd order delay line.

The transistor dimensions, resistor values and biasing levels of the transconductors used in the delay line are given below in tables IV to VI. The schematic layout for the 3rd order delay line is depicted in figures 48, 49 and 50.

TABLE IV. – g_{m0} design dimensions and biasing levels.

Component	Value
M_1	$(1.5\mu/0.18\mu)\times 4$
M_2	$(4\mu/0.18\mu)\times 4$
M_3	$(4\mu/0.4\mu)\times 4$
R_S	300 Ω
R_L	10 kΩ
I_{Bias1}	75 µA

TABLE V. – g_{mf} dimensions and biasing levels.

Component	Value
M_1	$(1.5\mu/0.18\mu)\times 4$
M_2	$(4\mu/0.4\mu)\times 4$
R_S	300 Ω
C_S	200 fF
I_{Bias1}	75 µA

TABLE VI. – g_{m1} dimensions and biasing levels.

Component	Value
M_1	$(4\mu/0.18\mu)\times 4$
M_2	$(4\mu/0.18\mu)\times 12$
M_3	$(4\mu/0.4\mu)\times 4$
R_L	10 kΩ
I_{Bias1}	150 µA

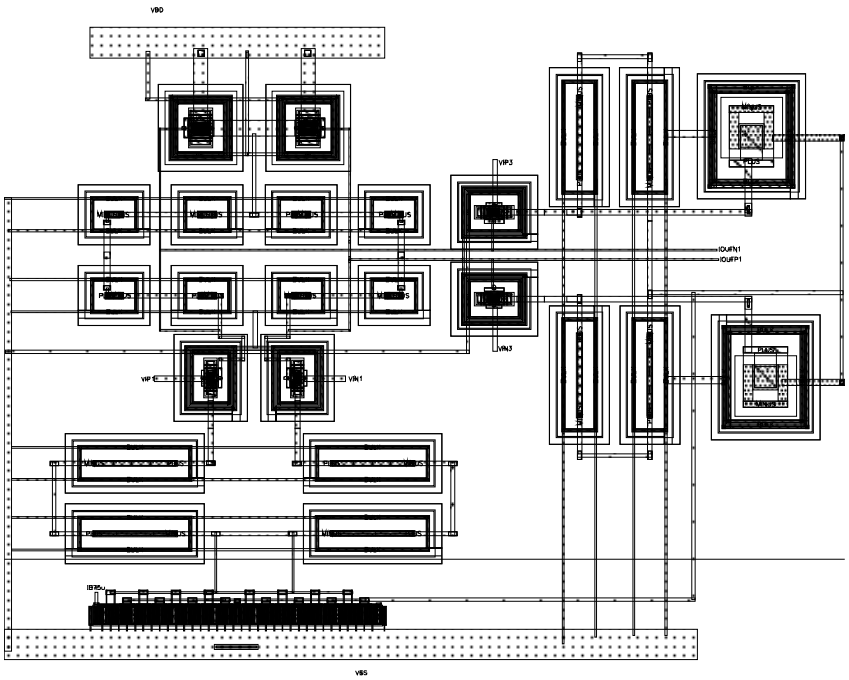

Figure 48. Circuit layout of g_{m0} and g_{mf}.

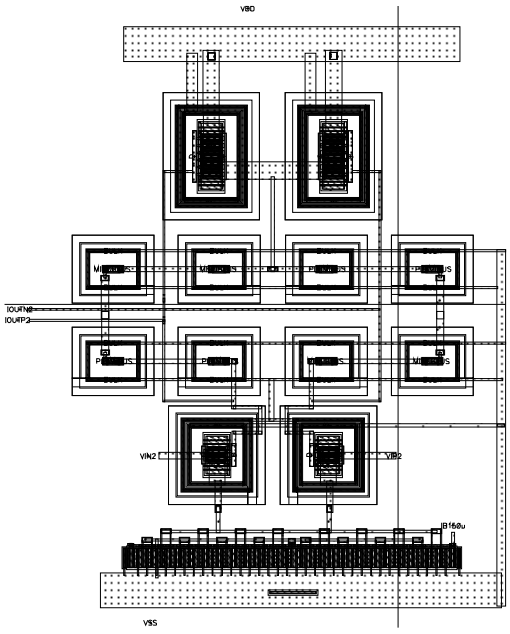

Figure 49. Circuit layout of g_{m1}.

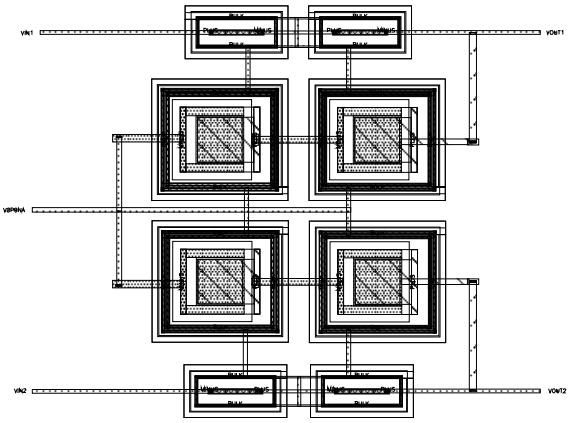

Figure 50. Circuit layout of the LPF.

After the delay line was laid out post layout simulations were carried out to validate the performance of the cell and the simulations are provided below in figure 51.

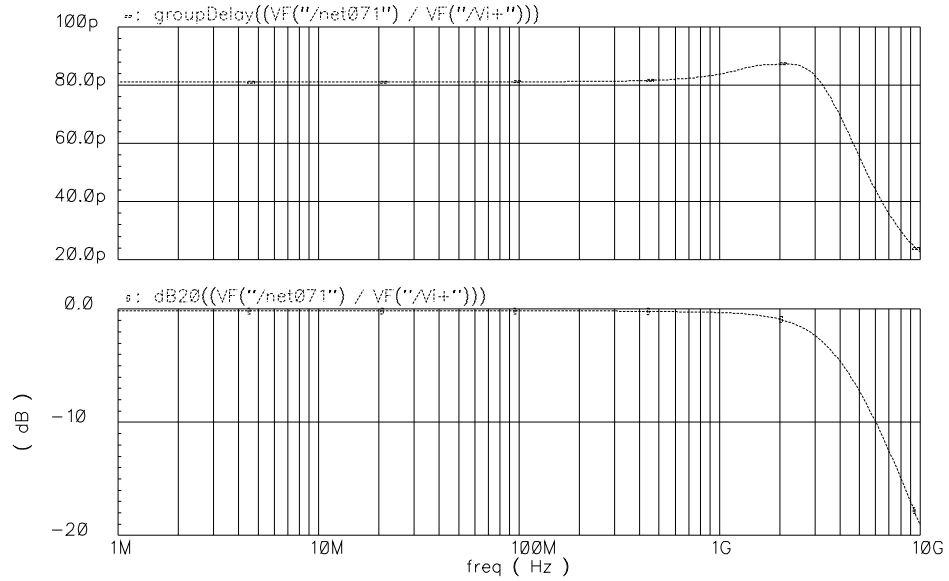

Figure 51. Post-layout group delay and magnitude for the 3rd order delay line.

The bandwidth of the cell was reduced from 4 GHz to 3.2 GHz. This limitation in bandwidth should impose some additional ISI that will contribute to vertical and horizontal opening of the output eye diagram. It is important to mention that since the bandwidth is almost twice of the maximum input frequency of 1.5625 GHz the impact on ISI should be minimal. The post layout group delay was 81 ps which is a 15 % increase in the nominal group delay of 70 ps. The obtained group delay should not have too much impact on the eye because it is the desired delay for a T/4 equalizer at 3.125 Gb/s. An eye diagram with the delay cell layout will be provided in section B of this chapter.

2. Multiplier

References in the literature show that common structures used to perform analog multiplication in transversal equalizers include variable gain amplifiers (VGA), double-balanced multipliers, multiplying digital-to-analog converters (MDAC) or combinations of all these. In either case, the following design considerations must be made when selecting a topology are the following:

- The multipliers must have low input capacitance such that the loading on the delay lines is minimal.
- Their output capacitance must also be as low as possible to minimize the loading at the input of the summing node, which typically sets the bandwidth limitations for the entire equalization system.
- Depending on system requirements, power consumption must be kept to a minimum.
- Multiplication by both positive and negative coefficients must be provided.
- The tuning range of the coefficients must be sufficiently accurate in order to achieve adaptive calibration.
- Noise contribution by the multiplier must be minimal.

The proposed multiplier is depicted below in figure 52.

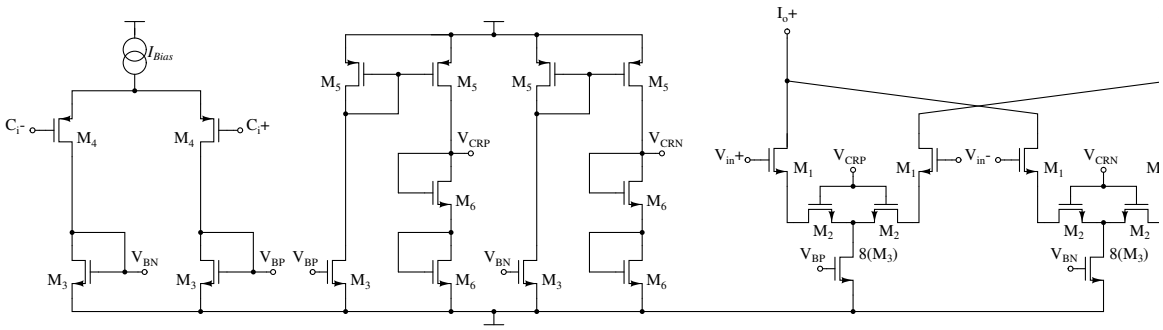

Figure 52. Analog multiplier schematic.

Assuming that a digital control sequence is produced by the adaptive calibration algorithm used in the equalizer (e.g. normalized LMS, sign-sign LMS, etc), control voltage is applied to the PMOS current steering differential pair formed by transistors M_4. This voltage will generate control currents that will flow trough the diode connected loads M_3 and get mirrored to the current mirrors comprised by M_5 and the NMOS differential pairs formed by M_1 respectively. Transistors M_5 will feed current into transistors M_6 to generate a voltage that controls the MOS degeneration transistors M_2. The MOS in linear region exhibits a resistance equal to [21],

$$R_{DS} \approx \frac{1}{\mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TH}\right)} \tag{4.14}$$

Thus by controlling V_{GS}, the transconductace of the source degenerated differential pairs G_m can be controlled as follows,

$$G_m = \frac{g_{m1}}{1 + g_{m1} R_{DS2}} \tag{4.15}$$

s For the maximum value of G_m the resistance attains its smallest value and vice versa yielding linear multiplication especially for low currents. This can be removed leading into a conventional Gilbert multiplier. It is worth mentioning that since the small signal transconductance of transistors M_1, namely g_{m1}, which is given by,

$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{Bias}} \tag{4.16}$$

varies in an opposite direction as the degeneration resistors, the latter do not have to cover a wide range of resistance. Simulations where carried out and the result are given in figures 53 and 54. Table VII shows transistor dimensions and biasing levels used in the multiplier.

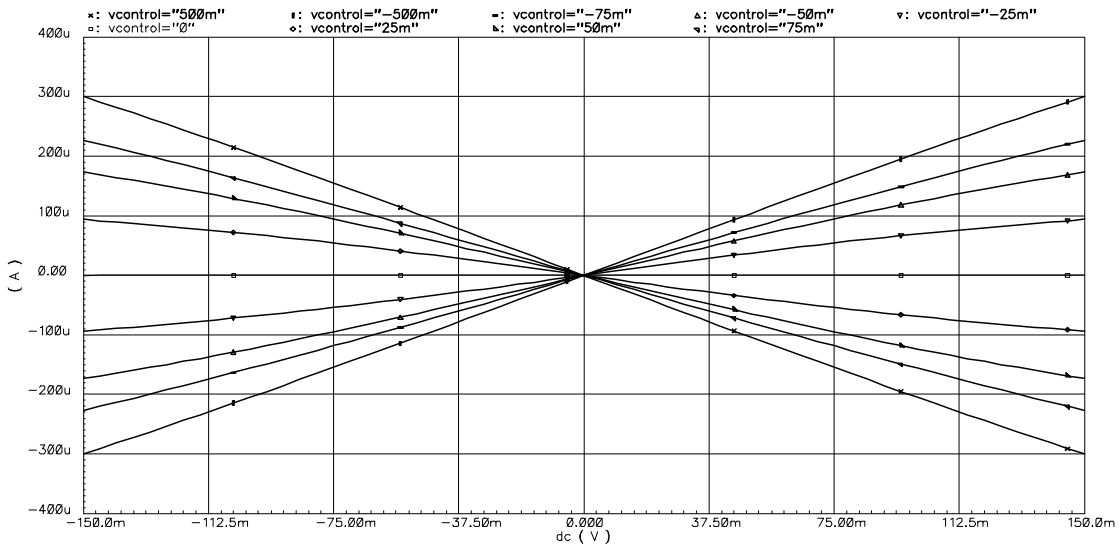

Figure 53. Multiplier output current versus input voltage for various control voltages.

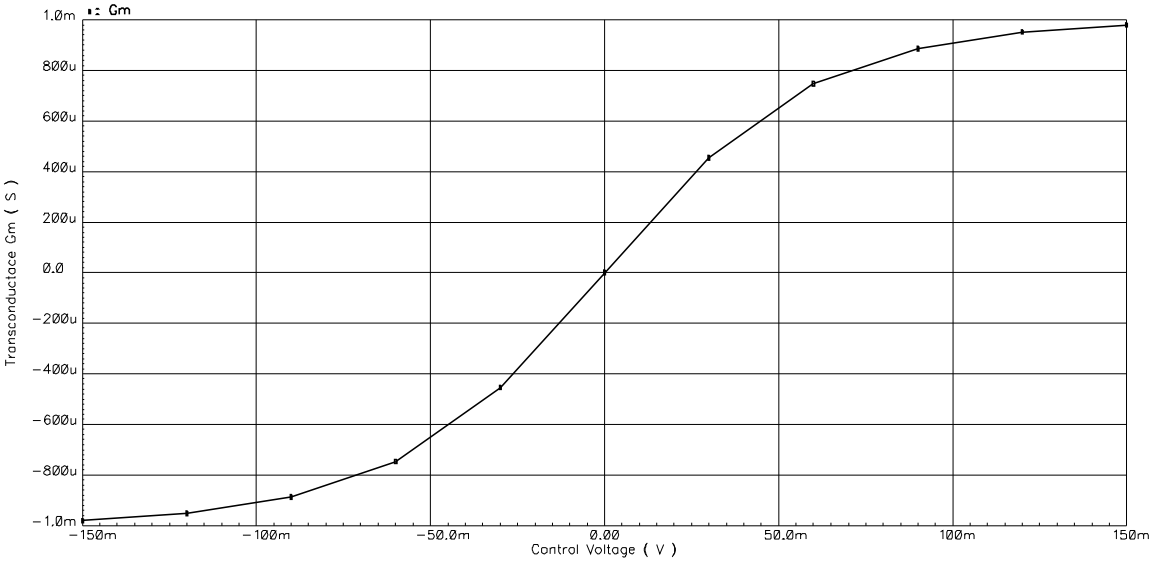

Figure 54. Transconductance versus control voltage.

TABLE VII. – Multiplier design dimensions and biasing levels.

Component	Value
M_1	$(1.5\mu/0.18u)\times 4$
M_2	$(1.6\mu/0.18u)\times 4$
M_3	$(4\mu/0.4u)\times 4$
M_4	$(4\mu/0.4u)\times 4$
M_5	$(4\mu/0.4u)\times 6$
M_6	$(2\mu/0.18u)\times 4$
I_{Bias}	75 μA

3. Summing Currents

To add the output current of the multipliers and convert the sum into a voltage, a trans-impedance amplifier was used. It needs to have low input impedance in order to both, set the DC at the output of the multipliers and to shift the output pole of the multipliers to higher frequencies. The low impedance of the input also guaranties that the output current of the multipliers will flow to that node.

The transimpedance amplifier should be designed such that it pushes the pole at the input to frequencies higher than 3.2 GHz to provide the data rate of 3.125 Gb/s for the system. The output load from multiplier stages are assumed to be 50fF for each branch which makes the total load capacitance 250fF per branch. For the output a 100fF capacitance was assumed to emulate the capacitive load of the buffer. According to system level budget, this block should provide 1KΩ of trans-impedance to ensure proper operation of the system.

The proposed adder is depicted below in figure 55. The design of the adder was based on the same principle of active feedback used in the delay lines. The forward transconductor was implemented using a single stage differential pair formed by transistors M_2 with R_L as loads and common mode feedback and transistors M3 serving as a termination for the DC current. The feedback transconductor is also a single stage operational transconductance amplifier (OTA) with capacitive degeneration. Transistors M_4 adds up all the DC currents coming from the multiplier and R_{CMFB} acts as a common mode feedback for the DC input level of the TIA.

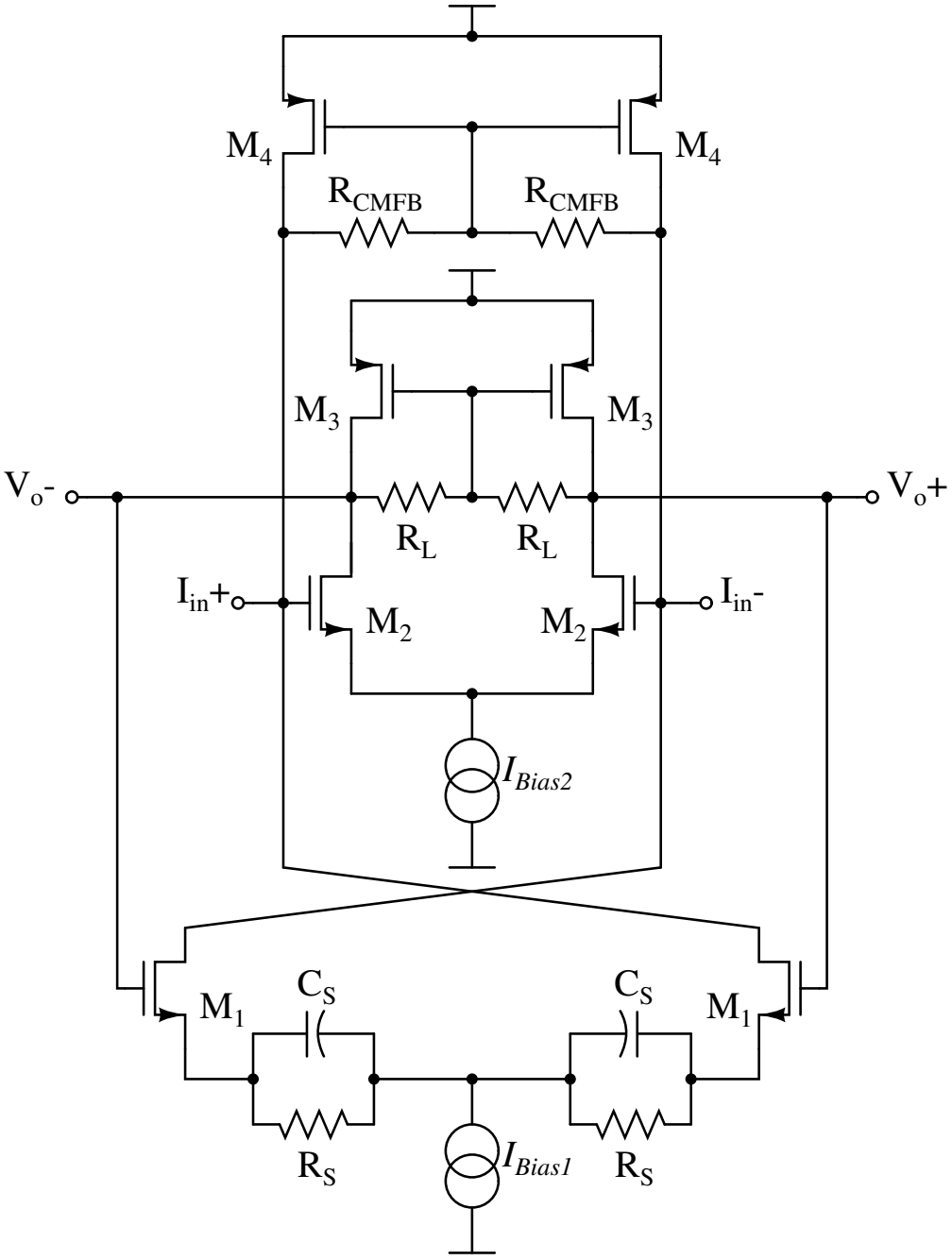

Figure 55. Transimpedance amplifier schematic.

The input resistance of this topology also benefits from the effect of impedance gyration which allows this topology to achieve reasonably small resistance values. Performing small signal analysis to find the input resistance yields,

$$R_{in} = \frac{1}{g_{m1} g_{m2} R_L} \parallel R_{CMFB} \parallel r_{o4} \parallel g_{m1} r_{o1} R_S \tag{4.17}$$

$$R_{in} \approx \frac{1}{g_{m1} g_{m2} R_L} \tag{4.18}$$

In equation 56 the imaginary part of the impedance was not considered for simplicity. However as explained before in section 1, any capacitive loading at the output of the TIA will result in an inductive behavior of the impedance leading to peaking in the transfer function. Peaking can be beneficial since it provides certain bandwidth extension nonetheless it has to be kept minimal since it introduces abrupt changes in the group delay of the TIA leading to ISI.

To approximate the frequency of the pole located at the input of the TIA, the total capacitance lumped at that now must be calculated. Assuming that C_{Mult} is the contribution of all the multipliers connected to the input of the TIA, the total input capacitance can be expressed as,

$$C_{in} = C_{Mult} + C_{gs2} + C_{Miller2} + C_{db4} + C_R \tag{4.19}$$

where C_{gs2} and $C_{Miller2}$ are the gate to source and Miller capacitance of M_2, C_{db4} is the drain to bulk capacitance of M_4 and C_R is the parasitic capacitance of R_{CMFB}.

Thus the frequency of the pole at the input can be expressed as,

$$f_{Pin} = \frac{1}{2\pi C_{in} R_{in}} \tag{4.20}$$

Assuming C_L as the load capacitance connected at the output and following a similar approach the output resistance and pole location can be expressed as,

$$R_o = \frac{1}{g_{m1} g_{m2} R_{CMFB}} \parallel R_L \parallel r_{o3} \tag{4.21}$$

$$R_o \approx \frac{1}{g_{m1} g_{m2} R_{CMFB}} \tag{4.22}$$

$$f_{Po} = \frac{1}{2\pi C_L R_o} \tag{4.23}$$

From section 1 the transfer function can be expressed as,

$$\frac{V_o}{i_{in}} \equiv Z_{TIA} = \frac{g_{m1} R_L R_{CMFB}}{1 + g_{m1} g_{m2} R_L R_{CMFB}} \tag{4.24}$$

$$Z_{TIA} \approx \frac{1}{g_{m1}} \tag{4.25}$$

The simulation results and tabulated component values and biasing levels are given below in figures 56, 57, 58. The dimensions and biasing levels are given in table VIII.

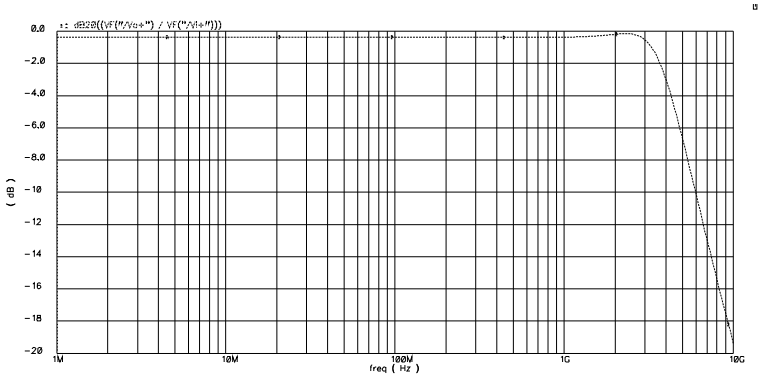

Figure 56. Transimpedance amplifier transfer function.

Figure 56 shows the frequency response of the equalizer without boosting (i.e. only the first coefficient c_0 was set to one and all other to zero). Due to the 40 Ω input impedance of the TIA, the equalizer achieves a bandwidth of 4.1 GHz which is sufficient for a 3.125 Gb/s data rate. The total transimpedance gain obtained from the summing node was 960 Ω, that is the reason why in figure 43 the equalizer gain at low frequencies deviates from 0 dB's by less than 0.5 dB which is not enough to reduce the signal amplitude drastically.

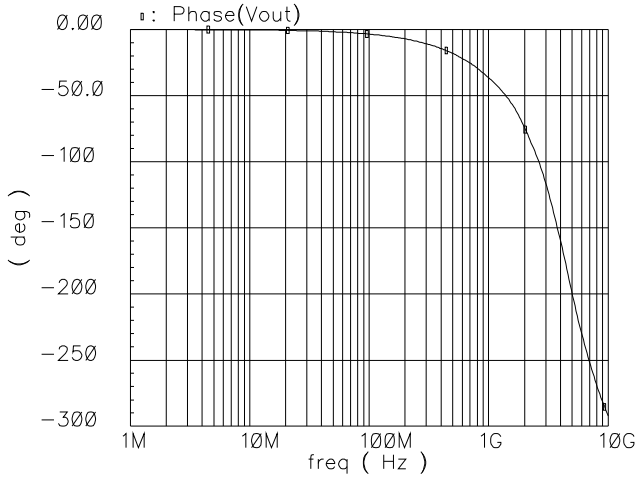

Figure 57. Transimpedance amplifier phase..

Figure 57 show the phase response for the equalizer. As expected it show a logarithmic smooth decay which ensures a linear behavior and thus a constant group delay over the band of interest. To measure the distortion introduced by the transimpedance and the multiplier blocks a two tone simulation was performed with frequencies 1.5125 GHz and 1.6125 GHz and the simulation result is provided below in figure 58.

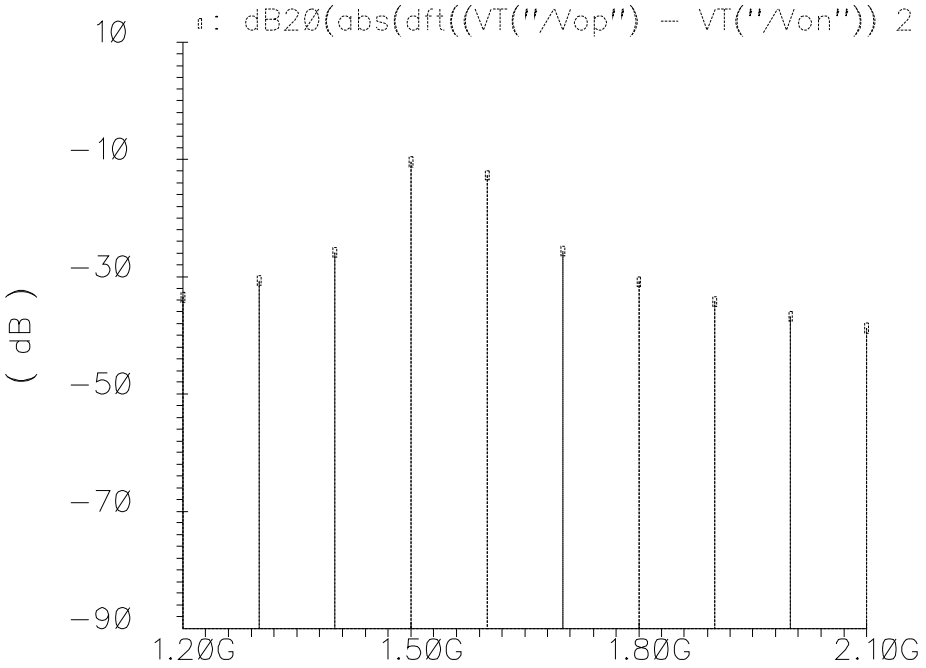

Figure 58. Transimpedance amplifier IM3 simulation .

From figure 58 the IM3 component was found to be 16 dB below the input tones which yields a HD3 = IM3 – 20log(3) = 26 dB for a 600 mV_{pp} differential input signal.

After designing all the equalizer building blocks, system level simulations were carried out in Matlab to calculate iteratively the equalizer coefficients for different test channels. After the coefficients were found, a test bench was setup in Cadence and simulations were carried out. The system level modeling and results are given next in the following subsection.

TABLE VIII. – TIA design dimensions and biasing levels.

Component	Value
M_1	$(1.5\mu/0.18\mu)\times4$
M_2	$(4\mu/0.18\mu)\times10$
M_3	$4\mu/0.18\mu\times12$
M_4	$4\mu/0.18\mu\times10$
R_L	10 kΩ
R_{CMFB}	10 kΩ
R_S	345 Ω
C_S	150 fF
I_{Bias1}	0.45 mA
I_{Bias2}	2.4 mA

B. System Simulation Results

1. Matlab Macromodeling

MATLAB simulations were carried out to find the optimal coefficients for the equalizer. Characteristics of the macromodel created include:

- Channel emulation with a first order LPF and cable model.
- Pseudo-random binary sequence data generation as input.
- White Gaussian noise added to the system.
- Least Mean Square (LMS) calibration performed to derive equalization coefficients.

To test the validity of the model developed in Matlab, the channel was first assumed to be a 1^{st} order low pass filter. Using sign-sign LMS algorithm the coefficients for equalization were found. After the coefficients were found simulations were carried out in Cadence using the same 1^{st} order low pass and the coefficients found from Matlab. For further information on how the signal was generated in Matlab and exported to Cadence refer to appendix C. Figures 59 and 60 show the eye-diagram of the input and output data to the equalizer after LMS calibration in MATLAB and Cadence respectively.

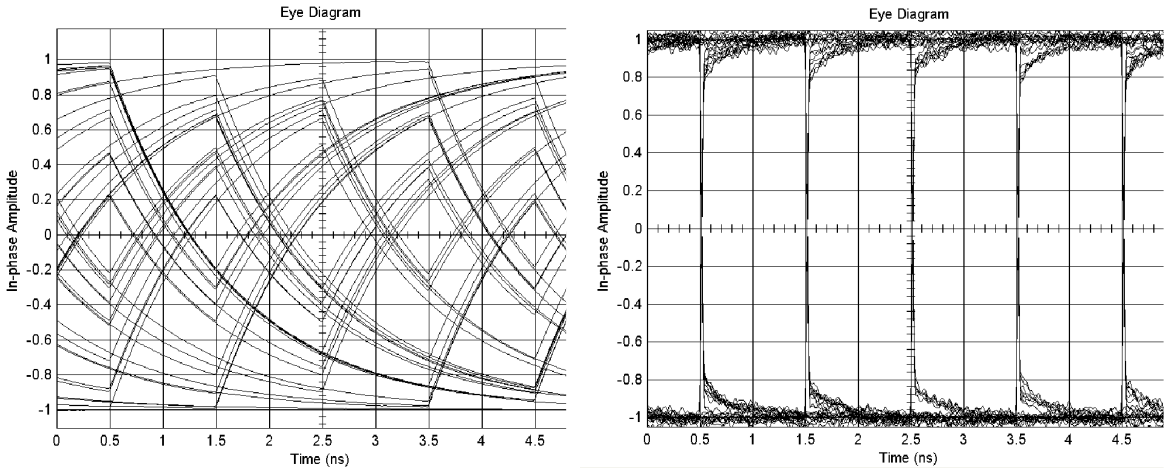

Figure 59. Equalizer input data (left) and equalizer output (right). Matlab.

Figure fixme show the equalization of a 1st order low pass filter with 20 dB of attenuation at 1.5625 GHz the input eye shows peak to peak jitter greater than 0.5 UI and the equalizer is able to remove all this jitter and output data with less completely restored and with peak to peak jitter less that 0.1 UI.

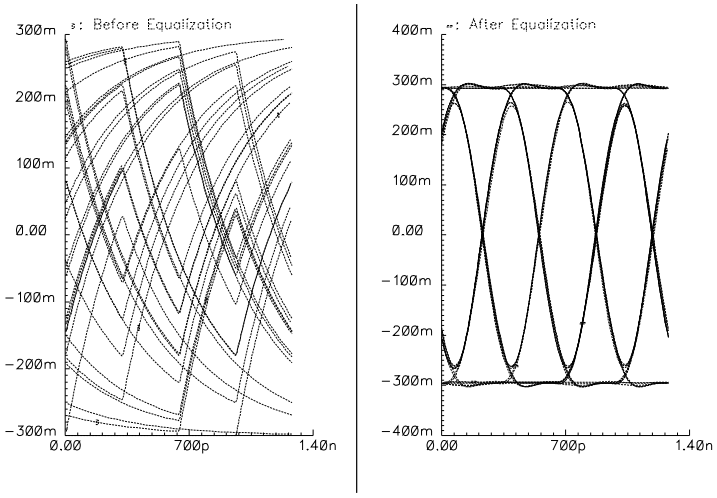

Figure 60. Equalizer input data (left) and equalizer output (right). Cadence.

The same setup was used in Cadence to validate the model developed in Matlab. Again the 1st order low pass filter provides 20 dB of attenuation at 1.5625 GHz and introduces peak jitter greater than 0.5 UI (160 ps)and the equalizer is able to remove all this jitter and output data with less completely restored and with peak to peak jitter less that 0.1 UI (32 ps).

2. Preamp and Output Buffer

To extend the useful range of the equalizer and cover a wider range of cable loss a preamp was designed to provide an extra 2.5 V/V gain to the nominal gain of 0 dB. Providing 2.5 V/V or 8 dBs and a bandwidth beyond 3.2 GHz requires the use of a wideband amplifier, the topology selected for the preamp is a conventional Cherry-Hooper amplifier [19] because it offers a relatively high gain and reduced circuit complexity. The transistor level schematic of the preamp is depicted below in figure 61. The preamp not only provides the additional gain but it also isolates the load on the summing amplifier which will have to drive the output buffer otherwise. Isolation is advantageous since the input capacitance of the buffer might be large enough to produce reasonable peaking in the summing amplifier's transfer function due to impedance gyration. As expected, all this benefits come at the expense of increased power consumption, circuit complexity and elevated noise. It is worth mentioning that now the multipliers have to cover a smaller range since additional boosting is not required from them thus relaxing the design of the former while increasing the linearity of the equalizer. The transistor dimensions and biasing levels are provided in table IX.

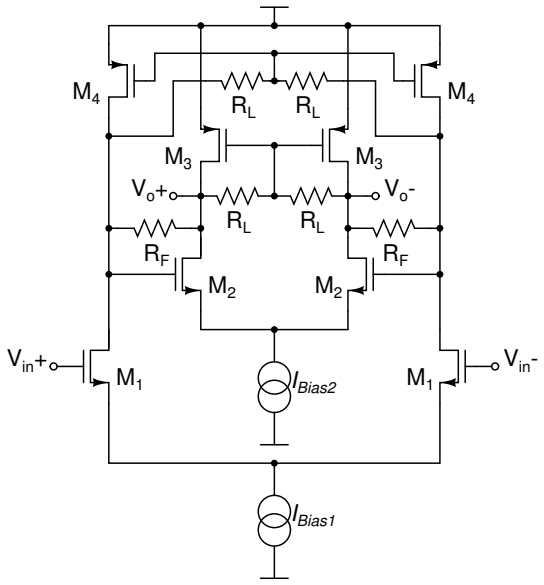

Figure 61. Preamp schematic.

TABLE IX. – Preamp design dimensions and biasing levels.

Component	Value
M_1	$(1.5\mu/0.18\mu)\times 4$
M_2	$(4\mu/0.18\mu)\times 10$
M_3	$4\mu/0.18\mu\times 12$
M_4	$4\mu/0.18\mu\times 10$
R_L	10 kΩ
R_F	1 kΩ
I_{Bias1}	1.2 mA
I_{Bias2}	0.6 mA

After the preamp was designed, an output buffer was required to increase the driving capability of the equalizer. The buffer might be removed if the equalizer is driving an on-chip voltage input load or if the equalizer is probed in a probe station. Since the equalizer was assumed to be able to communicate with test equipment that is outside the chip, a digital buffer was used.

The output buffer designed to drive the 50 Ohms of the measuring equipment and PCB traces is a simple cascade of 3 differential pairs. An internal matching network might be used to account for bonding wire inductance and package parasitics if the 50 ohms are placed on chip. In this case and open drain configuration was employed to better control the termination resistance driven by the latter stage of the buffer which acts like a Current Mode Logic (CML) inverter. The termination resistance at the input of the network analyzer should be 50 Ohms thus the last stage should provide a output swing of 300 mVpp single ended to an equivalent 25 Ohms thus, $I_{Bias} = V_{outpp}/R_L$ = 300 mV/50 Ohms = 12 mA.

The output buffer also requires a pre-driver to ensure proper operation of the CML buffer which adds an additional 4.6 mA, summing up to 16.6 mA of current required. Note that this value even though it might seem high it is actually smaller than the output swing required by the CML standard.

An Low Voltage Differential Signaling (LVDS) buffer was also explored but it was found out that equal power consumption is required to attain the same output swing. In both cases the pre-driver is required to ensure hard switching of the last differential pair in the chain, thus there is little that can be done to circumvent this issue. However it

is important to mention that if an LVDS standard is adopted then reasonable savings in power can be obtained given the smaller output swing required by the LVDS standard. Also the smaller swing at the input should benefit from better linearity. For the scope of this project only ECL logic compatibility was addressed thus an I/O voltage swing of 600 mVpp differential was tackled.

After all the blocks were connected simulations were carried out for different cable lengths and bit rates, the simulation results are given below in figures 62 to 65.

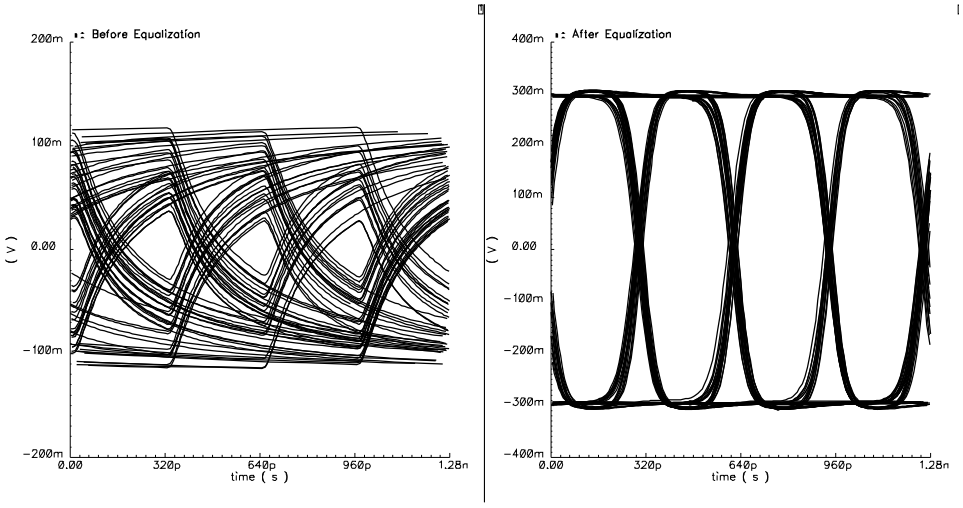

Figure 62. 15 Meters of Belden 8219 RG-58A/U cable data rate 3.125 Gb/s.

Figure 62 shows the equalization of 15 Meters of Belden 8219 RG-58A/U cable at a data rate of 3.125 Gb/s. The eye diagram before equalization (left plot) shows a vertical eye opening of 30 mV which for a maximum amplitude of 120 mV corresponds to 25% of the peak amplitude. After the equalizer, including the buffer, (right plot) the signal was fully recovered showing a vertical eye opening of 290 mV which corresponds

to 97% of the peak amplitude. The simulated input referred noise including the equalizer, the preamp and the buffer was 2.8 mVrms which corresponds to an SNR of 20log(290/5.6) = 34 dB. The theoretical BER < 1×10^{-25} (see chapter III, section C).

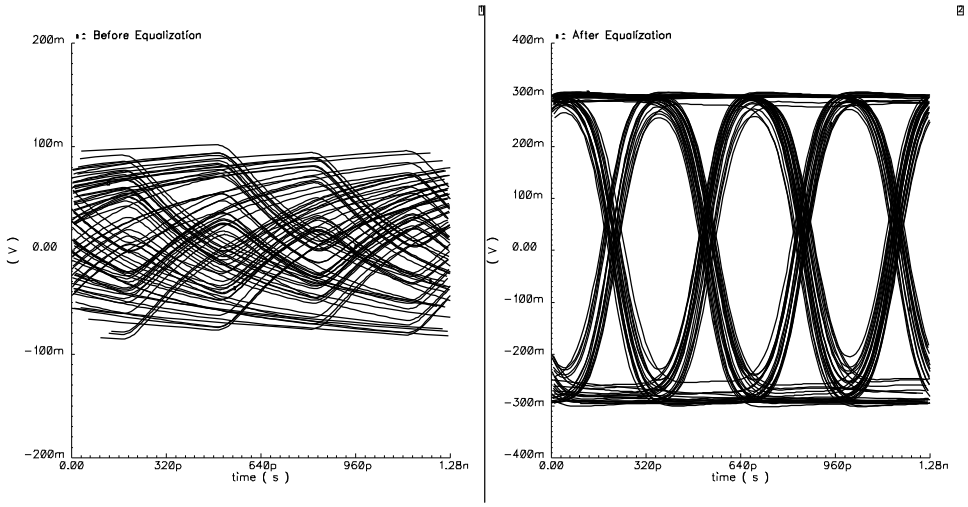

Figure 63. 20 Meters of Belden 8219 RG-58A/U cable data rate 3.125 Gb/s.

Figure 63 shows the equalization of 20 meters of RG-58 A/U cable. The eye-diagram before equalization shows a vertical eye opening of 0 V which corresponds to 0% of the peak amplitude. After the equalizer the signal was recovered showing a vertical eye opening of 230 mV which corresponds to 76% of the peak amplitude. The rms jitter for 15 and 20 meters is below 0.2 UI.

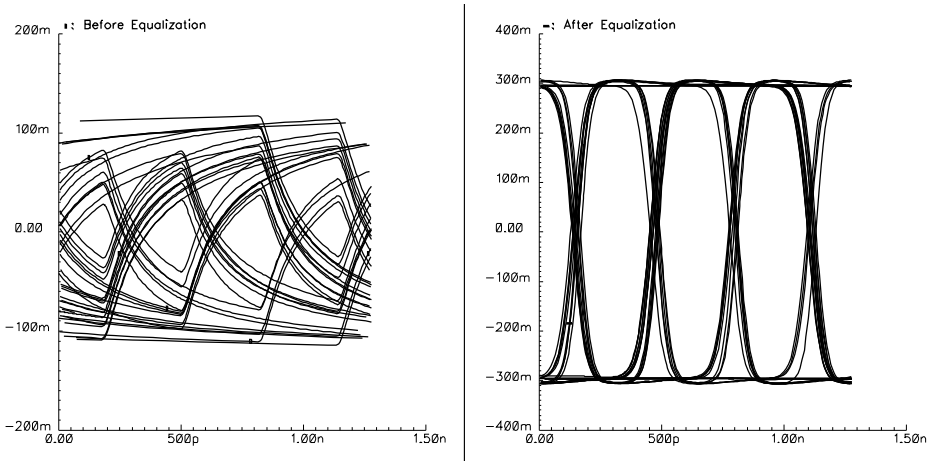

Figure 64. 15 Meters of Belden 8219 RG-58A/U cable data rate 3.125 Gb/s post layout.

Figure 64 shows the post layout equalization of 15 meters of RG-58 A/U cable. The eye-diagram before equalization shows a vertical eye opening of 30 mV which corresponds to 25% of the peak amplitude. After the equalizer the signal was recovered showing a vertical eye opening of 150 mV which corresponds to 50% of the peak amplitude. The rms jitter is below 0.2 UI.

For completeness, equalization was performed on 15 meters of cable at 4 Gb/s and the result is depicted below in figure 65.

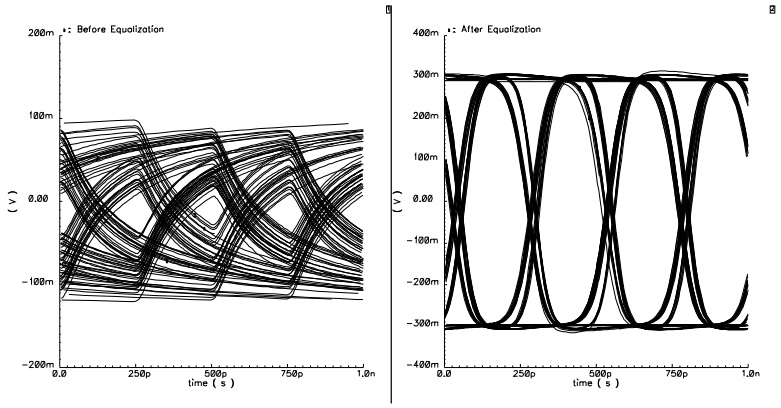

Figure 65. 15 Meters of Belden 8219 RG-58A/U cable data rate 4 Gb/s.

Figure 65 shows the equalization of 15 m of coaxial cable. For this case since the tap spacing or delay was not tuned to the optimal value there is an increase in the jitter and can be seen in the equalized data. Nonetheless as mentioned before, 4 Gb/s is beyond the scope of this work and was only provided herein for completeness.

After all the simulations were carried out, the equalizer was compared to recent work to evaluate the performance of the proposed 3.125 Gb/s equalizer and the results are given in table X. The figure of merit used to compare the speed given the bandwidth limitation imposed by the technology was defined as [11],

$$FOM = \frac{Data\ Rate\ (Mb/s)}{Transit\ Frequency\ f_t\ (GHz)} \tag{4.26}$$

where f_t is the unity current gain frequency of a single minimum size transistor for any given technology. The equalizer is able to perform well and is competitive when compared to other structures in terms of rate/bandwidth. It is worth mentioning that it works at a fraction of the power consumption of some of the previous work.

TABLE X. – Comparison of the proposed equalizer and previous work.

Reference	Technology	Power (mW)	Transit Frequency f_t (GHz)	Data Rate (Gb/s)	FOM Data Rate/f_T (Mbps/GHz)
[11]	0.35 µm CMOS	96	15	1	67
[15]	0.25 µm CMOS	45	30	1	33
[16]	0.18 µm SiGe	30	120	10	83
This Work	0.18 µm CMOS	34	60	3.125	52
This Work	0.18 µm CMOS	34	60	4	67

*The equalizer rated speed is 3.125 Gb/s but was able to perform at 4 Gb/s.

As mentioned in table X the equalizer consumes 34 mW which can be broken down as follows:

- Delay line current consumption = 2.4 mA x 4 = 9.6 mA.
- Multiplier current consumption = 750 µA x 5 = 4.5 mA.
- Summing amplifier current consumption = 3 mA x 1 = 3 mA.
- Preamp current consumption = 1.8 mA x 1 = 1.8 mA.

Thus the total current consumption is: 9.6 + 4.5 + 3 + 1.8 = 18.9 mA or equivalently 34 mW from a ± 0.9 V power supply.

A summary of results is provided in table XI.

TABLE XI. – Equalizer summary of results.

PARAMETER	**RESULT**
Data Rate	3.125 Gb/s
Number of Taps	5
Equivalent sampling rate	1/80 ps = 12.5 GHz
Unity Gain Bandwidth (no boosting)	4.1 GHz
SNR of equalizer without boosting	34 dB
BER	$> 10^{-25}$
Maximum Boosting at 1.5625 GHz	> 20 dB
V_{IN}	±300 mV
Current Consumption	18 mA
Power Supply	± 0.9 V
Technology	TSMC 0.18 µm CMOS

From the results tabulated above it is evident that the proposed equalizer performs well in terms data rate and power consumption. The main limitations that hindered the equalizer from optimal performance was the excessive parasitic capacitance introduced by the PMOS loads used which increased the required power, and the output buffer used to it bandwidth limitations introduced jitter and can be observed in the eye diagrams in figures 62 and 63.

CHAPTER V

CONCLUSION

With the growing trend of research in electrical and optical links, there has been significant interest in designing analog equalizers for wireline receivers. In continuing this trend, the purpose of this project was to research and design a coaxial cable equalizer for 3.125 Gb/s. The project has succeeded in developing various high speed circuits used as building blocks for an analog transversal feed forward equalizer. Among these, a high speed broadband delay line based on active feedback capable of providing flat gain and constant group delay for data rates in the Gb/s range and a wideband transimpedance amplifier based on active feedback capable of operating in the GHz range. The projects also studied the modeling of a communications channel and identify a simple and reliable method to emulate the channel loss and phase distortion. The equalizer performance is comparable to previous work and is capable of restoring the transmitted data after 15 and 20 meters of coaxial cable.

A. Future Work

After designing the first prototype, it was evident that the circuit cannot perform at frequencies beyond 4 Gb/s, however after some minor modifications the equalizer was able to attain frequencies up to 10 GHz which is enough for 10 Gb/s communications (i.e. OC-92 and 10 Gb/s Ethernet). These modifications were basically removing all the PMOS current loads used in the equalizer's building blocks and replacing all the current sources with resistors. This reduced the parasitic capacitance associated with all the

nodes where the PMOS currents sources used to be thus extending the bandwidth of each cell greatly.

The schematic diagrams of all the 10 Gb/s equalizers along with a brief discussion, simulation results and a comparison with previous works is given in the following subsection.

1. 10 Gb/s CMOS Equalizer

The circuit topology is similar to the circuit described in chapter IV, thus it follows the same discussion given in chapters III and IV. The circuit was also designed in TSMC 0.18 μm CMOS process.

The basic structure of a 5-TAP FIR filter is given below in figure 66.

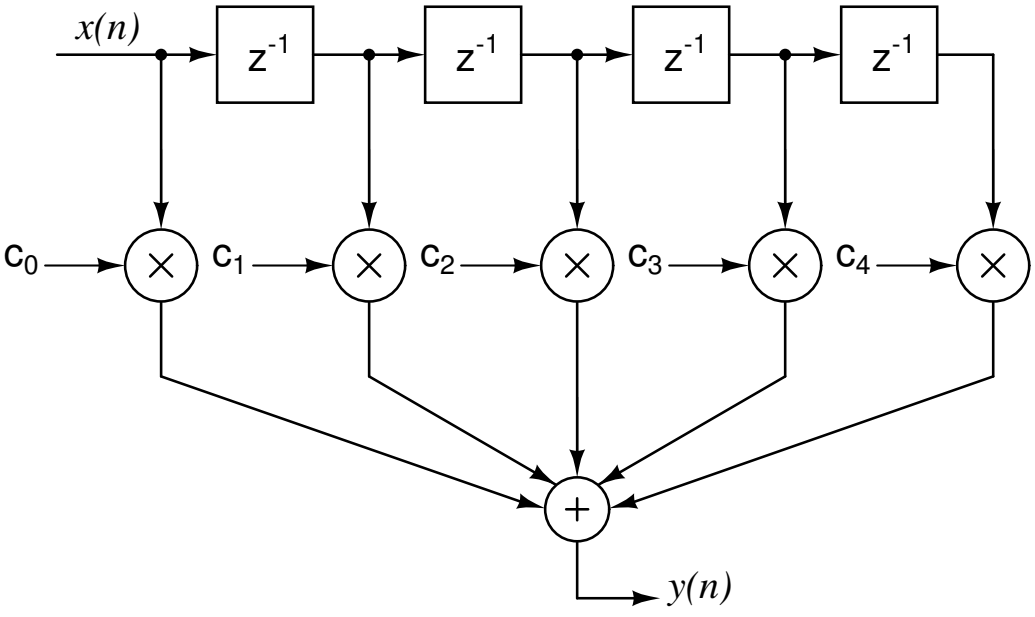

Figure 66. 5 Taps FFE.

The delay lines are based on the same active feedback principle described in chapter IV (see figure 37 chapter IV section A). However the filter order was reduced from a 3rd order filter to a 2nd order filter. The reason for reducing the filter order is to reduce the circuit complexity therefore reducing the number of parasitic capacitances associated with a bigger structure. Also, since the sample time chosen was T/4 a 2nd order filter should have enough bandwidth to cover 5 GHz maximum frequency this becomes evident from figure 60 where a T/2 structure is compared to a T/4 structure. The T/4 structure half the group delay and twice the bandwidth when compared to a T/2 which might be troublesome when designing the delay lines, however thanks to the active feedback used in this design the delay lines where able to attain a -3 dB bandwidth close to 10 GHz and a group delay of 25ps which is required for 10 Gb/s communications.

Figure 67 shows the effect that increasing the sampling frequency, i.e. reducing the sampling period, has on the transfer function of the equalize. For this case the same filter coefficients were used and the sampling period was changed from T/2 = 50 ps to T/4 = 25 ps, thus by using T/4 a second order module can be used.

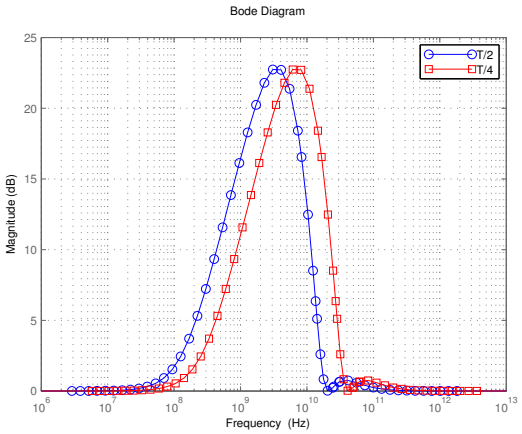

Figure 67. Ideal equalizer with T/2 and T/4 sampling periods.

The forward transconductors of the delay line are depicted below in figures 68 and 69. The transistor dimensions and biasing levels are provided in tables XII and XIII respectively.

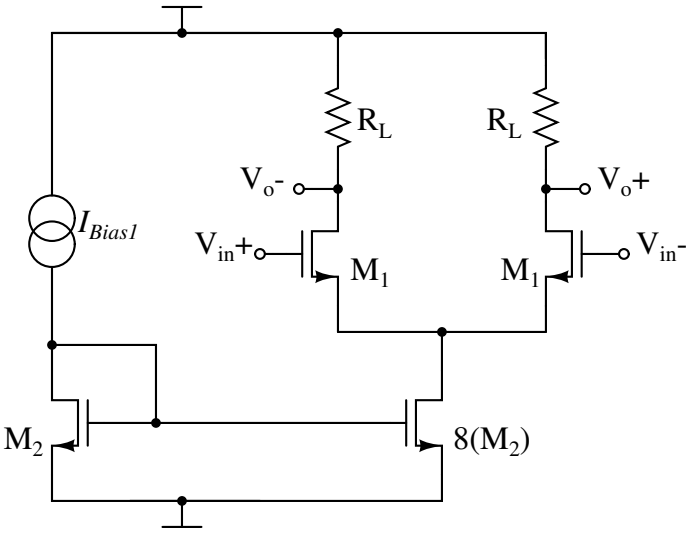

Figure 68. g_{m0}.

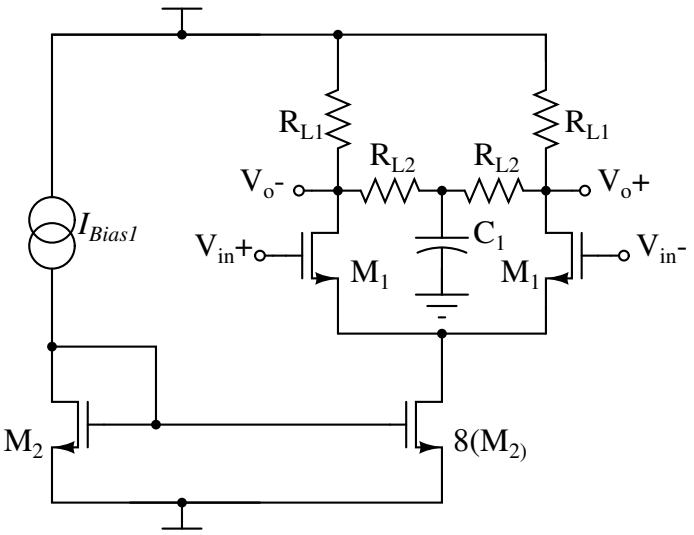

Figure 69. g_{m1}.

TABLE XII. – g_{m0} design parameters.

Component	Value
M_1	$(5\mu/0.18\,\mu)\times 4$
M_2	$(4\mu/0.4\,\mu)\times 4$
R_L	800 Ω
I_{Bias1}	150 µA

TABLE XIII. – g_{m1} design parameters.

Component	Value
M_1	$(6\mu/0.18\,\mu)\times 4$
M_2	$(6\mu/0.4\,\mu)\times 4$
R_{L1}	1.4 kΩ
R_{L2}	150 Ω
C_1	1 pF
I_{Bias1}	150 μA

Depicted in figure 70 is the schematic of the feedback transconductor. The dimensions and biasing levels of the former are given in table XIV.

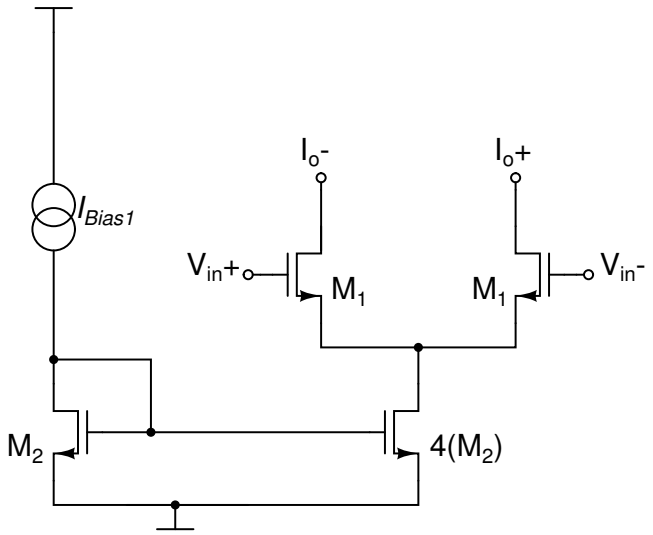

Figure 70. g_{mf} .

TABLE XIV. – g_{mf} design parameters.

Component	Value
M_1	$(5\mu/0.18\,\mu)\times 4$
M_2	$(4\mu/0.4\,\mu)\times 4$
I_{Bias1}	150 µA

The magnitude response and group delay is depicted below in figure 71.

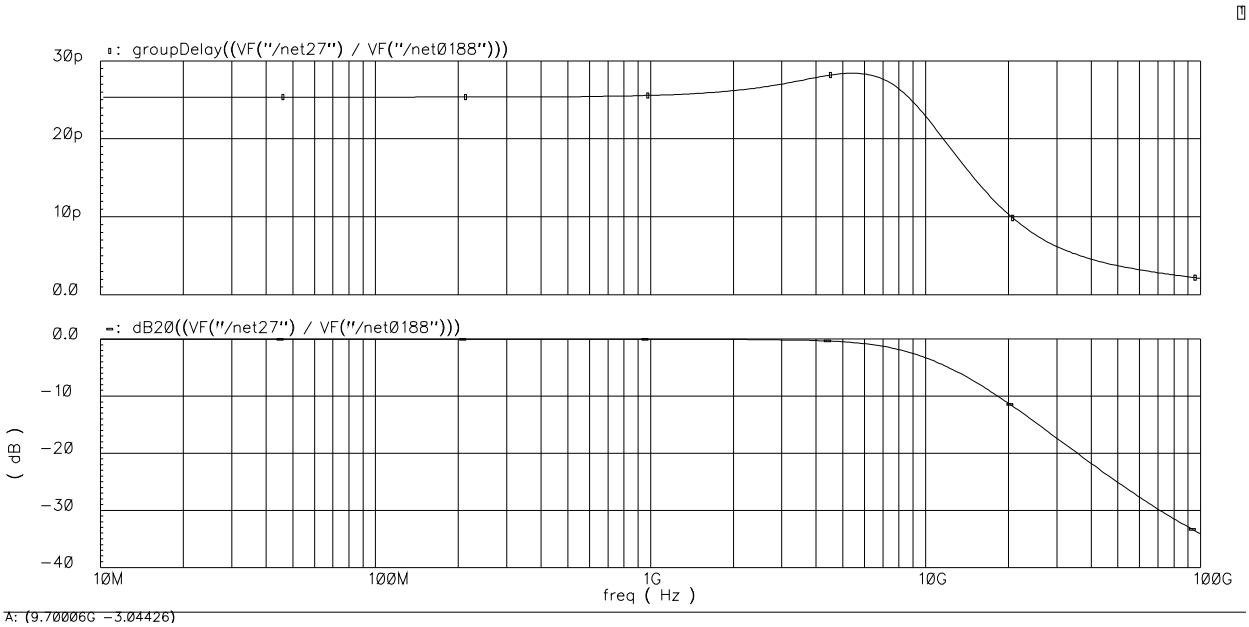

Figure 71. Group delay and magnitude response of the proposed delay line.

The proposed delay line attains a -3 dB bandwidth of 9.7 GHz and a group delay of 25 ps which is enough for a 10 Gb/s data stream.

The multiplier and transimpedance amplifier are depicted in figures 72 and 73 respectively. The design parameters are given in tables XV and XVI.

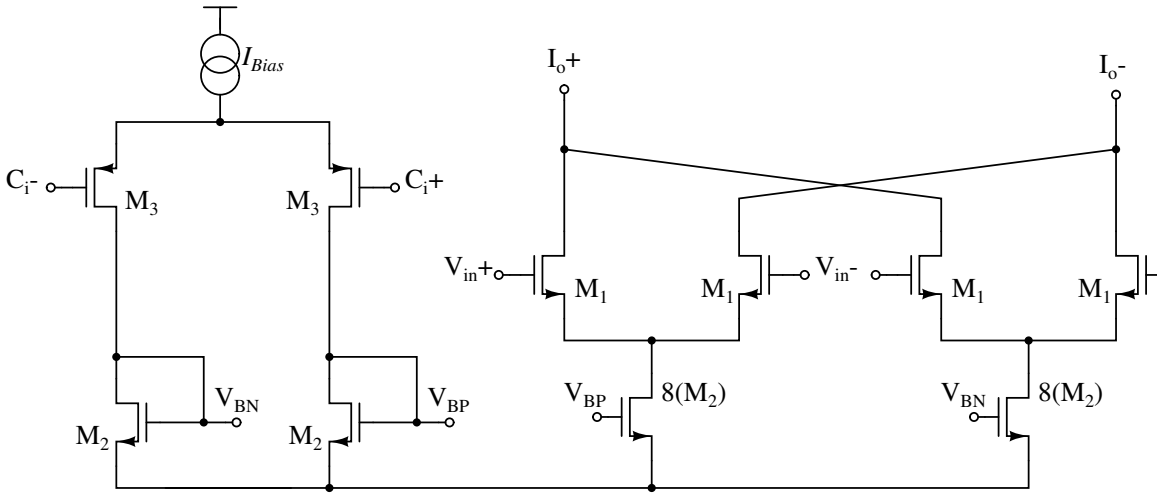

Figure 72. Four quadrant multiplier.

TABLE XV. – Four quadrant multiplier design parameters.

Component	Value
M_1	$(4\mu/0.18\mu)\times 4$
M_2	$(8\mu/0.4\mu)\times 4$
M_3	$(4\mu/0.4\mu)\times 4$
I_{Bias1}	150 µA

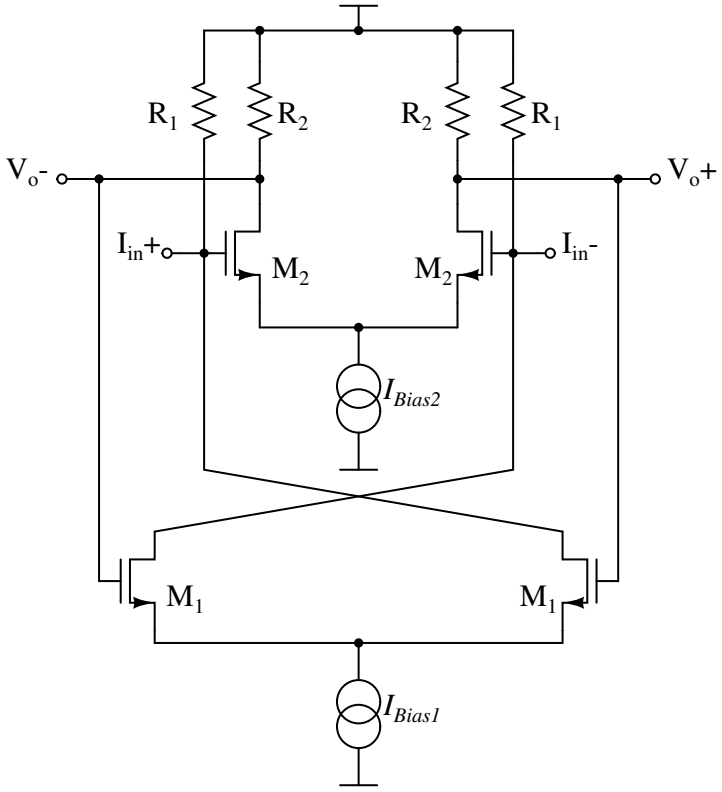

Figure 73. Transimpedance amplifier.

TABLE XVI. – Transimpedance amplifier design parameters.

Component	Value
M_1	$(4\mu/0.18\mu)\times 4$
M_2	$(8\mu/0.18\mu)\times 4$
R_1	200 Ω
R_2	500 Ω
I_{Bias1}	450 µA
I_{Bias2}	2.4 mA

After all the blocks were connected, simulations were carried out to and the results are given below in figures 74 and 75.

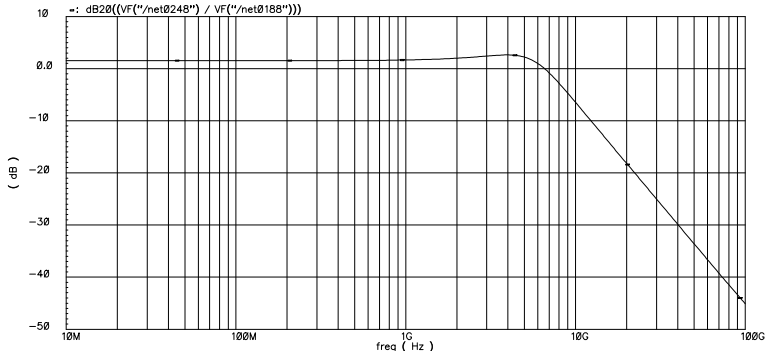

Figure 74. Equalizer transfer function with no boosting.

Depicted in figure 74 is the simulated frequency response of the 10 Gb/s equalizer. The -3 dB bandwidth obtained was 7.5 GHz which could be increased to 10 GHz to improve the eye opening and reduce ISI.

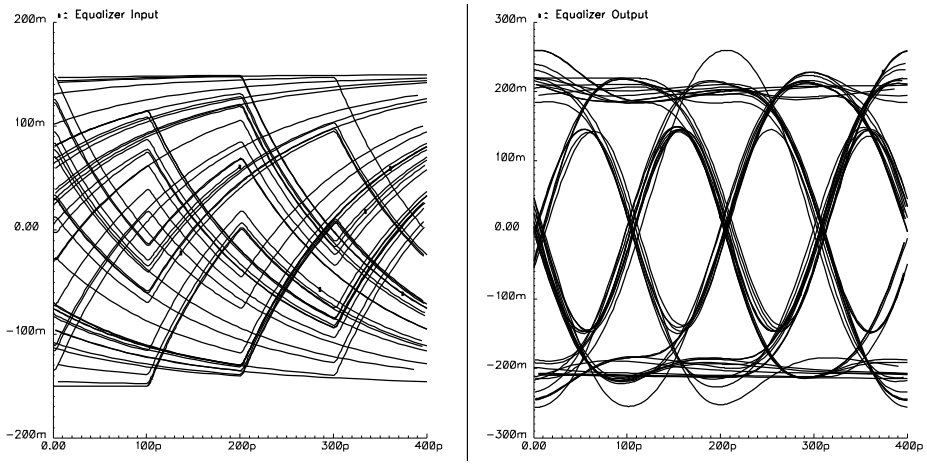

Figure 75. Equalizer input (left), equalizer output (right).

Figure 75 shows the equalization of a 1st order low pass filter channel. The eye-diagram before equalization shows a vertical eye opening of 0 V which corresponds to 0% of the peak amplitude. After the equalizer the signal shows a vertical eye opening of 150 mV which corresponds to 75% of the peak amplitude of 200 mV. The output jitter is 12 ps or 0.12 UI.

From figures 74 and 75 it is clear that the equalizer can operate at a 10 Gb/s data rate. However there are some adjustments that could be done to the increase the bandwidth of the transimpedance summer and therefore improve the performance of the equalizer. All the results obtained were at the simulation level. To fully characterize the

equalizer, all the blocks must be laid out and a limiting amplifier or digital buffer must be designed to drive any external loads. The equalizer consumes 21 mA from a ± 0.9 V supply, or equivalently 37.8 mW which can be divided as follows:

- Delay line current consumption = 3 mA x 4 = 12 mA.
- Multiplier current consumption =1.2 mA x 5 = 6 mA.
- Summing amplifier current consumption = 3 mA x 1 = 3 mA.

To evaluate the performance of the proposed equalizer it was compared to previous works and the results are given in table XVII.

TABLE XVII. – Comparison of the proposed 10 Gb/s equalizer and previous work.

Reference	Technology	Power (mW)	Transit Frequency ft (GHz)	Data Rate (Gb/s)	FOM Data Rate/fT (Mbps/GHz)
[11]	0.35 µm CMOS	96	15	1	67
[15]	0.25 µm CMOS	45	30	1	33
[16]	0.18 µm SiGe BiCMOS	30	120	10	83
This Work	0.18 µm CMOS	38	60	10	167

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APPENDIX A

INDUCTOR RESISTANCE SERIES TO PARALLEL CONVERSION

When analyzing an LC bandpass circuit such as the one depicted in picture 76a, it becomes convenient to transform by mathematical manipulation the series resistance associated with the inductance wire (R_S) into a parallel equivalent resistance (R_P)as shown if figure 76b.

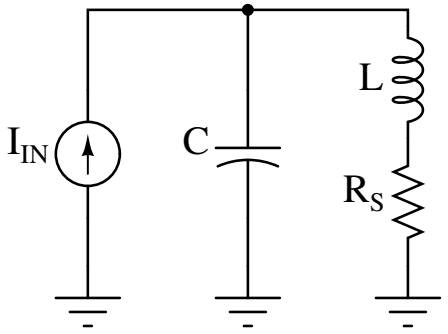

Figure 76a. LC filter with series resistance.)

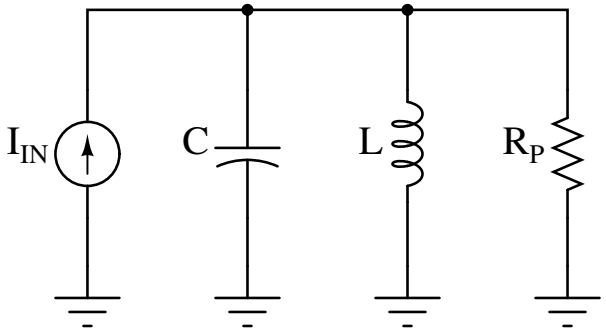

Figure 76b. LC filter with parallel resistance.)

By inspection the admittance seen by the source in figure 67a can be expressed as,

$$Y_a = \frac{1}{R_S + sL}$$

$$= \frac{1}{R_S + sL}\frac{R_S - sL}{R_S - sL} \qquad \text{(A.1)}$$

$$= \frac{R_S}{R_S^2 - s^2L^2} - \frac{sL}{R_S^2 - s^2L^2}$$

Similarly the admittance in figure 67b can be expressed as,

$$Y_b = \frac{1}{R_P} + \frac{1}{sL} \tag{A.2}$$

Equating the real part of A.1 and the real part of A.2 yields,

$$\frac{R_S}{R_S^2 + \omega^2 L^2} = \frac{1}{R_P} \tag{A.3}$$

Solving for R_P yields,

$$R_P = \frac{R_S^2 + \omega^2 L^2}{R_S} \tag{A.4}$$

Rearranging,

$$R_P = R_S\left(1 + \frac{\omega^2 L^2}{R_S^2}\right) \tag{A.5}$$

Since the quality factor Q of an inductor with series resistance R_S is equal to [13],

$$Q = \frac{\omega L}{R_S} \tag{A.5}$$

equation A.5 can be written as,

$$R_P = R_S\left(1 + Q^2\right) \tag{A.6}$$

APPENDIX B

MISCELLANEOUS MATLAB CODE

```
%
////////////////////////////////////////////////////////////////////////
//
% //
//
% //        File:  PRBS
//
% //     Purpose:  Generate a Pseudo Random Binary Sequence
//
% //
//
% //      Inputs:  Rb --> Bit Rate in bits per second
//
% //                      For a NRZ signal Rb = 2*fmax
//
% //               Fs --> Sampling Frequency in Hz.
//
% //            Tstop --> Desired duration time in seconds
//
% //
//
% //     Outputs:  t  --> True time of the nth sample
//
% //        PRBS_gen  --> Pseudo random binary sequence
//
% //
//
% //      Author:  Marcos L. Lopez-Rivera (m.lopez27@gmail.com)
//
% //
//
% //        Date:  February 8, 2009
//
% //
//
%
////////////////////////////////////////////////////////////////////////
//

% // E.g.
% // 10 cycles of an 1 Gbps stream with 10 samples per symbol are
required
% // Rb = 1e9 (Maximum frequency = 500 MHz)
% // Fs = 10*Rb  = 10e9 (10 samples per symbol)
% // Tstop = 10*(1/Rb) = 10e-9 (10 cycles of 1 Gbps stream)
% // [x, t] = PRBS(1e9, 10e9, 10e-9)
```

```
function [PRBS_gen , t] = PRBS(Rb, Fs, Tstop, varargin)

Amax = 1;
Amin = 0;

if nargin > 5
    disp('??? Error using ==> length')
    disp('Too many input arguments.')
    return
end

if nargin == 5
    Amax = round(varargin{1});
    Amin = round(varargin{2});
end

if nargin == 4
    Amax = round(varargin{:});
end

if Amin > Amax
    Amax = Amin;
end

un = floor(Fs/Rb);  % Number of samples per symbol

n = 0:1:Tstop*Fs - 1;    % Number of samples
t = n/Fs;           % True time of the nth sample

r = round(rand(length(n)/un,1));
j = 1;
for i = 1:un:length(n)
    PRBS_gen(i:un*j) = r(j);
    j = j + 1;
end

if nargin > 3
    for i = 1:1:length(PRBS_gen)
        if PRBS_gen(i) == 1
            PRBS_gen(i) = Amax;
        else
            PRBS_gen(i) = Amin;
        end
    end
end

return
```

```
%
////////////////////////////////////////////////////////////////////////
//
% //
//
% //        File:  Equirriple Filters
//
% //     Purpose:  Plot the frequency and group delay of equirriple
//
% //               filter from 1st to 10th order
//
% //
//
% //
//
% //      Author:  Marcos L. Lopez-Rivera (m.lopez27@gmail.com)
//
% //
//
% //        Date:
//
% //
//
%
////////////////////////////////////////////////////////////////////////
//

close all
clear all
clc

% Equiriple delay filters dphase = 0.05

w = logspace(-1,2,1000);
s = j*w;

num = 1;
den = s + 1;
H1 = num./den;

num = 1.4638;
den = s.^2 + 2.0175.*s + 1.4638;
H2 = num./den;

num = 1.9660;
den = s.^3 + 2.7542*s.^2 + 3.6664*s + 1.9660;
H3 = num./den;

num = 2.9098;
den = s.^4 + 3.4188*s.^3 + 6.5467*s.^2 + 6.5781*s + 2.9098;
H4 = num./den;
```

```
num = 4.9527;
den = s.^5 + 4.0722*s.^4 + 10.2813*s.^3 + 15.0219*s.^2 + 12.8995*s ...
      + 4.9527;
H5 = num./den;

num = 8.9446;
den = s.^6 + 4.6578*s.^5 + 14.5748*s.^4 + 27.6303*s.^3 + 34.8174*s.^2
...
      + 25.9327*s + 8.9446;
H6 = num./den;

num = 17.9801;
den = s.^7 + 5.2339*s.^6 + 19.7*s.^5 + 45.9244*s.^4 + 76.5219*s.^3 ...
      + 84.0877*s.^2 + 57.1076*s + 17.9801;
H7 = num./den;

semilogx(w,20*log10(abs(H1)),'k')
hold on
semilogx(w,20*log10(abs(H2)),'k')
semilogx(w,20*log10(abs(H3)),'k')
semilogx(w,20*log10(abs(H4)),'k')
semilogx(w,20*log10(abs(H5)),'k')
semilogx(w,20*log10(abs(H6)),'k')
semilogx(w,20*log10(abs(H7)),'k')
xlabel('Normalized Frequency (rad/s)')
ylabel('Magnitude (dB)');
title('Magnitude Response vs Frequency');
grid on
hold off
h = text(11.5,-13,'n = ','FontSize',10);
set(h,'BackgroundColor',[1 1 1]);
XX = [15 9.5 9.25 8.5 8 7.5 6.75]+1.5;
YY = [-10 -35 -52.5 -67.5 -82 -95 -108]-3;
textArray = ['1';'2';'3';'4';'5';'6';'7'];
h = text(XX,YY,textArray,'FontSize',10);
set(h,'BackgroundColor','w')

w = linspace(w(1),w(end),length(w))/(2*pi);
s = j*w*2*pi;

num = 1;
den = s + 1;
H1 = num./den;
GroupDelay = -gradient(unwrap(angle(H1))*(180/pi),w)/360;
figure(2)
semilogx(w*2*pi,GroupDelay,'k')
hold on

num = 1.4638;
den = s.^2 + 2.0175.*s + 1.4638;
H2 = num./den;
GroupDelay = -gradient(unwrap(angle(H2))*(180/pi),w)/360;
```

```
semilogx(w*2*pi,GroupDelay,'k')

num = 1.9660;
den = s.^3 + 2.7542*s.^2 + 3.6664*s + 1.9660;
H3 = num./den;
GroupDelay = -gradient(unwrap(angle(H3))*(180/pi),w)/360;
semilogx(w*2*pi,GroupDelay,'k')

num = 2.9098;
den = s.^4 + 3.4188*s.^3 + 6.5467*s.^2 + 6.5781*s + 2.9098;
H4 = num./den;
GroupDelay = -gradient(unwrap(angle(H4))*(180/pi),w)/360;
semilogx(w*2*pi,GroupDelay,'k')

num = 4.9527;
den = s.^5 + 4.0722*s.^4 + 10.2813*s.^3 + 15.0219*s.^2 + 12.8995*s ...
      + 4.9527;
H5 = num./den;
GroupDelay = -gradient(unwrap(angle(H5))*(180/pi),w)/360;
semilogx(w*2*pi,GroupDelay,'k')

num = 8.9446;
den = s.^6 + 4.6578*s.^5 + 14.5748*s.^4 + 27.6303*s.^3 + 34.8174*s.^2
...
      + 25.9327*s + 8.9446;
H6 = num./den;
GroupDelay = -gradient(unwrap(angle(H6))*(180/pi),w)/360;
semilogx(w*2*pi,GroupDelay,'k')

num = 17.9801;
den = s.^7 + 5.2339*s.^6 + 19.7*s.^5 + 45.9244*s.^4 + 76.5219*s.^3 ...
      + 84.0877*s.^2 + 57.1076*s + 17.9801;
H7 = num./den;
GroupDelay = -gradient(unwrap(angle(H7))*(180/pi),w)/360;
semilogx(w*2*pi,GroupDelay,'k')
xlabel('Normalized Frequency (rad/s)')
ylabel('Normalized Group Delay (s)');
title('Group Delay vs Frequency');
grid on

hold off
h = text(2.105,3.3,'n = ','FontSize',10);
set(h,'BackgroundColor',[1 1 1]);
XX = [3.05 1.65 1.35 1.15 1 0.85 0.75];
YY = [3.3 3.025 2.725 2.38 2 1.5 0.85];
textArray = ['7';'6';'5';'4';'3';'2';'1'];
h = text(XX,YY,textArray,'FontSize',10);
set(h,'BackgroundColor','w')
%
////////////////////////////////////////////////////////////////////////
//
```

```
% //
//
% //        File:  BERvsSNR
//
% //     Purpose:  Calculate and plot the theoretical BER vs input SNR
//
% //
//
% //
//
% //      Author:  Marcos L. Lopez-Rivera (m.lopez27@gmail.com)
//
% //
//
% //        Date:
//
% //
//
%
////////////////////////////////////////////////////////////////////////
//

clear all
close all
clc

x_dB=0:0.2:20;

x_linear=10.^(x_dB/10);

BER=0.5*erfc(sqrt(x_linear/2));

figure(1)
semilogy(x_dB,BER);
grid on
title('BER vs SNR_O')
xlabel('Signal to Noise Ratio (dB)')
ylabel('Bit Error Rate')
set(gca,'XTick',0:2:20)
set(gca,'XTickLabel','0|2|4|6|8|10|12|14|16|18|20')
zoom on

%
////////////////////////////////////////////////////////////////////////
//
% //
//
% //        File:  writeFile
//
% //     Purpose:  Writes data matrix into text file
//
% //
//
```

```
% //      Inputs:  data  --> Nx2 matrix containing the
//
% //                       the N time samples in the first
//
% //                       column and the N voltage readings
//
% //                       in the second column
//
% //
//
% //     Outputs:  fname --> Selected file name
//
% //               pname --> Selected directory
//
% //
//
% //      Author:  Marcos L. Lopez-Rivera (m.lopez27@gmail.com)
//
% //
//
% //
//
%
////////////////////////////////////////////////////////////////////////
//

function [fname, pname] = writeFile(data)

[fname, pname] = uiputfile('*.txt','Save File As...');
fid = fopen(fname,'w');
if fid == -1
    disp('Error opening output file!')
end
 curdir = cd;
 cd(pname)
dlmwrite(fname,data,'delimiter','\t','precision',6)

st = fclose(fid);
if st == -1
    disp('Error closing output file!')
end

cd(curdir)

return
```

APPENDIX C

GENERATING, FILTERING, AND EXPORTING A MATLAB SIGNAL

In this appendix the process required to generate, filter and finally export a signal from Matlab to cadence is explained by means of an example Matlab script. This example generates a PRBS signal at 1 Gb/s, assumes a 1st order low-pass channel with a – 3dB frequency of 250 MHz and additive white Gaussian noise (AWGN). After the data has been filtered the script prompts the user through a Graphical User Interface to save the data into a text file that could be fed into a Piece Wise Linear Voltage source from Cadence's analog library vpwlf. In the file entry of the source the directory and name of the file should be entered. Functions are given in appendix B.

```
%
////////////////////////////////////////////////////////////////////////
//
% //
//
% //         File:  Channel_h.m
//
% //      Purpose:  Wireline Transceiver model
//
% //
//
% //       Author:  Marcos L. Lopez-Rivera (m.lopez27@gmail.com)
//
% //
//
% //
//
%
////////////////////////////////////////////////////////////////////////
//
%
////////////////////////////////////////////////////////////////////////
//
% //              _______________     __________     ___________
//
% //             |              |   |          |   |           |
//
```

```
% //            | Transmitter |-->| Channel |-->| Receiver |
//
% //            |_____________|   |_________|   |__________|
//
% //
//
% //      xt(t)->FFT->Xt(f)-->Xt(f)*Hc(f)-->Yr(f)*He(f)->IFFT-->yr(t)
//
%
////////////////////////////////////////////////////////////////////////
//

clear all;
close all;
clc

%
////////////////////////////////////////////////////////////////////////
//
% //
% // Transmitter parameters
% //

Rb = 1e9;         % Bit Rate
Fs = 100e9;       % Sampling frequency, sets the number of samples per
symbol
Tstop = 1000e-9;  % Desired simulation time
%
////////////////////////////////////////////////////////////////////////
//
% //
% // Random sequence generation
% //

[xt ,t] = PRBS(Rb,Fs,Tstop,1,-1);   % Generates the input signal


%
////////////////////////////////////////////////////////////////////////
//
% //
% // Channel
% //

delf = Fs/length(xt);               % Frequency delta for the FFT
ft = 0:delf:Fs - delf;              % Frequency vector

AWGN = random('norm',0,0.001,1,length(t));  % Additive white Gaussian
noise
xt = xt + AWGN;                             % Adding noise to each
sample

Xt = fft(xt);           % Taking the FFT of the input signal
```

```
w = 2*pi*ft;
s = j*w;

wp = 250e6;              % Setting the pole at 250 MHz

HLPF = 1./(1 + s/wp);    % Low pass filter transfer function

Yr = (Xt.*HLPF);         % Obtaining the frequency domain received
signal
yr = ifft(Yr);           % Taking the inverse FFT to obtain the time
                         domain   % received signal


data(:,1) = t';          % Entering the time information into the matrix
data(:,2) = yr';         % Entering the received signal into the matrix

writeFile(data);         % Calling the saveFile GUI
```

VITA

Marcos Luis López-Rivera was born in Bayamón, Puerto Rico. He received his Bachelor of Science degree in Electrical Engineering from the University of Puerto Rico, Mayagüez Campus. He worked as intern developing PSPICE models for operational amplifiers in the Standard Linear & Logic at Texas Instruments in the spring of 2004. In fall 2005 he rejoined Texas Instruments and worked developing PSPICE models for DC to DC switching converters in the High Performance Analog Group. He was awarded a GEM fellowship sponsored by Texas Instruments and worked at Texas Instruments in the summers of 2006, 2007 and 2008. In the summer of 2006 he worked for the Precision Analog Group developing PSPICE models for SAR ADC's and developing software tools to aid customers. In the summer of 2007 he worked also in Precision Analog developing PSPICE models for bridge sensors, and developing software tools. In the summer of 2008 he worked for the Storage Products Group designing current steering DAC's and Line Drivers. He received his Master of Science degree in Electrical Engineering from Texas A&M University in December 2009. As of August 2009, he is employed in the Audio and Imaging Products Group in Texas Instruments. He can be reached via his email address, m.lopez27@gmail.com, or his permanent address at Urb. Golden Village, Calle Primavera 82, Vega Alta, PR 00692.