# SINGLE INDUCTOR DUAL OUTPUT

# BUCK CONVERTER

A Thesis

by

HARITHA EACHEMPATTI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2009

Major Subject: Electrical Engineering

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Approved by:

| | |
|---|---|
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# ABSTRACT

Single Inductor Dual Output

Buck Converter.

(May 2009)

Haritha Eachempatti, B.E., Anna University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

The portable electronics market is rapidly migrating towards more compact devices with multiple functionalities. Form factor, performance, cost and efficiency of these devices constitute the factors of merit of devices like cell phones, MP3 players and PDA's. With advancement in technology and more intelligent processors being used, there is a need for multiple high integrity voltage supplies for empowering the systems in portable electronic devices.

Switched mode power supplies (SMPS's) are used to regulate the battery voltage. In an SMPS, maximum area is taken by the passive components such as the inductor and the capacitor. This work demonstrates a single inductor used in a buck converter with two output voltages from an input battery with voltage of value 3V. The main focus areas are low cross regulation between the outputs and supply of completely independent load current levels while maintaining desired values (1.2V,1.5V) within well controlled ripple levels.

Dynamic hysteresis control is used for the single inductor dual output buck converter in this work. Results of schematic and post layout simulations performed in CADENCE prove the merits of this control method, such as nil cross regulation and excellent transient response.

## DEDICATION

*To my parents and sister*

# ACKNOWLEDGEMENTS

First, I thank my advisor Dr. Jose Silva-Martinez for guiding me throughout my Masters program. Working with Dr. Silva has definitely been an enriching experience from which I take home many lessons on problem-solving, persistence and professionalism. I also thank my committee members Dr. Aydin Karsilayan, Dr. Hank Walker and Dr. Sunil Khatri for their time, co-operation and for accepting to serve on my committee.

I would like to thank my parents. Words are insufficient to express my gratitude to them for setting excellent examples for me to follow. I thank my sister for offering me advice and consolation during the roughest of times.

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# CHAPTER I

# INTRODUCTION

Voltage regulators (VR's) are required in electronic devices such as cellular phones, DSPs, laptops, etc. because the analog and digital signal processors require regulated DC voltage. A VR is placed at the output of a battery to serve the following purposes: 1) To adjust the voltage provided by the battery to the desired value for supply to the load. 2) To obtain clean, regulated voltage that is independent of the current drawn by the load and battery supply variations. These objectives can be achieved through regulation of the output of the battery. A VR consists of active and passive components that are interconnected in a manner such as to achieve the conversion of voltage levels. There are two types of VR's: 1) Linear voltage regulators (LVR's) 2) Switched mode power supplies (SMPS's). The regulator types have different advantages and disadvantages over one another.

LVR's have lower efficiency due to the presence of resistive elements that provide the regulating voltage drops and the class-A output driver. Also, only step down conversion is attained using an LVR.

SMPS's have higher efficiency but greater switching noises. Also called a DC/DC converter, the DC input voltage is converted to a DC output voltage of greater or lesser magnitude, possibly with opposite polarity or with the isolation of input and ground references. The generic SMPS topology is shown in Fig. 1. The switched mode power supply (SMPS) consists of the switching converter power stage and the controller that has feedback regulation and feed forward disturbance inputs.

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This thesis follows the style of *IEEE Journal of Solid-State Circuits.*

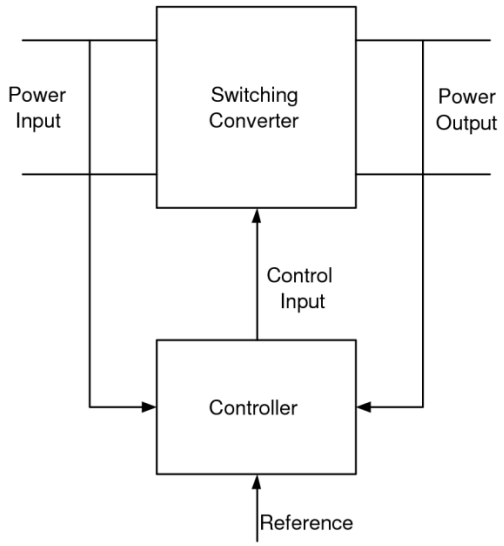


**Fig. 1 Switched mode power supply**

The power input side is called the “line side” and any variation at this point is referred to as “line side disturbance” whereas the power output is called the “load side” and change in the current at the output node is referred to as “load side disturbance”. A robust and well designed SMPS has feedback control that cleans load and line side disturbances so that the output voltage of the switching converter is well controlled. Precise voltage supply is necessary for signal processing circuits. The feedback regulator and the power switches present in the switching converter are normally integrated on the same die as the signal processing circuit in a portable device. The passive components are normally off the chip.

SMPS consists of switches and passive elements such as inductors (L’s) and capacitors (C’s). The presence of L’s and C’s serves a twofold purpose: 1) Filtering the high frequency components that are present in the voltages and currents due to switching 2) Providing stored energy during the switching periods. The output LC filter provides the function of suppressing switching ripple at the output $V_o$ and overall noise shaping such that high frequency random noise present in the loop consisting of the SMPS and controllers is filtered.

An example of a type of switching regulator i.e. the buck converter is shown in Fig. 2. The battery voltage is regulated by adjusting the switching of $S_p$ and $S_n$ while the inductor L and capacitor C filter the high frequency components so that output voltage $V_o$ is maintained at the desired value with low ripple.

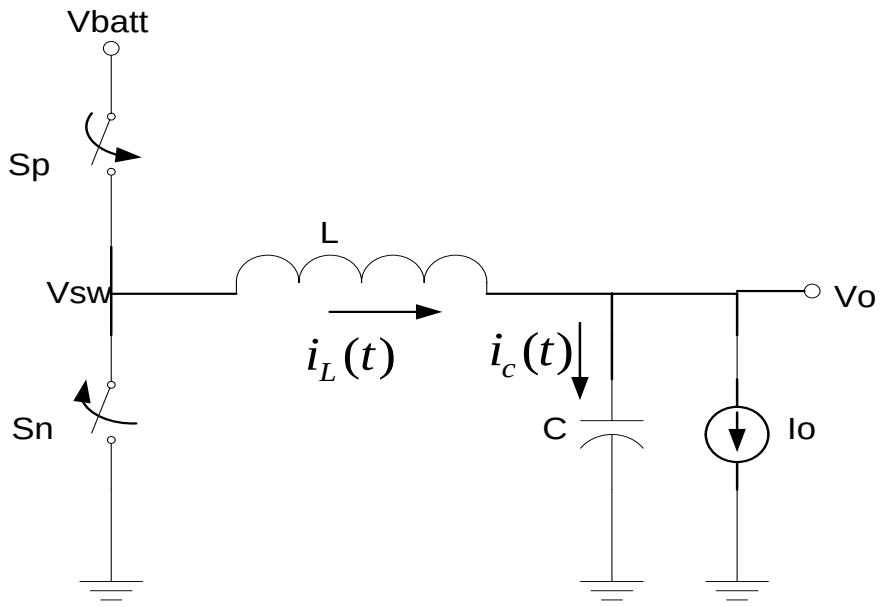


**Fig. 2 Topology of the buck converter**

Apart from switching noise, another major disadvantage of using the switching regulator is the high area and cost associated with the passive filter components. The buck converter is the most frequently used switching converter in portable applications where a voltage $V_o$ lesser than the input battery voltage $V_{batt}$ needs to be supplied to the analog and digital signal processing circuits where technology scaling is accompanied by reduction in maximum permissible supply voltage. Several SMPS's are normally used in a device for obtaining different voltage levels.

An example of the power supply on a portable device such as a cellular phone is shown in Fig. 3. The 60 Hz, 230V RMS AC line input is rectified to DC and is used to charge a battery. The Li ion battery has a nominal output voltage of 4.5V and is bound to discharge to a value as low as 2.5V. Different systems in a portable device need different supply voltage levels. The display needs a higher voltage of around 5V; hence a boost converter is employed to step up the battery voltage. The buck converter has maximum use as most analog and digital circuits require voltage levels lower than the battery. The buck-boost converter is required to supply a fixed voltage of 3.3V to the disk drive.

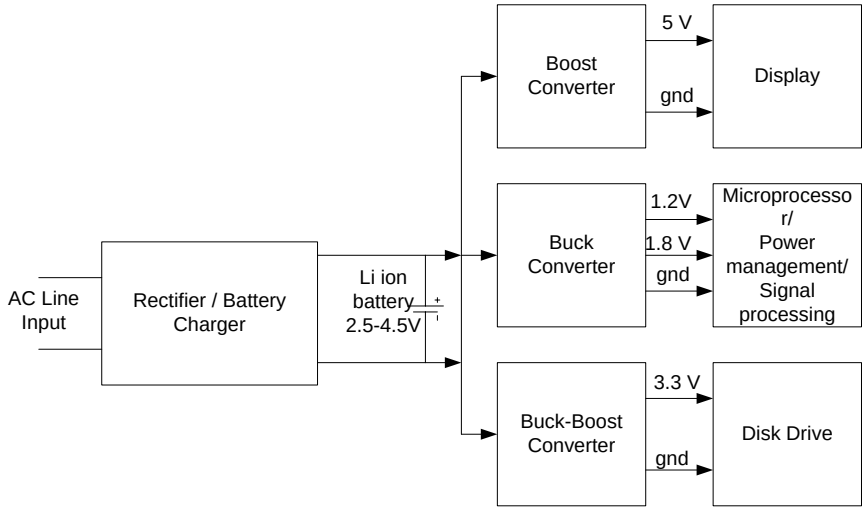


**Fig. 3 Power supply on portable devices**

Hence multiple voltage rails are required on a power management IC. The focus of this work is to demonstrate using a single inductor for two separate outputs in a buck SMPS. The idea can be extended for ‘n’ independent outputs. The purpose of this is lesser system volume, lower board real estate and component cost and greater chip area savings than in the case of two separate switching regulators.

### A. SIDO Buck Converter Topology

In this section the primary objectives that are met with by choosing the SIMO buck converter topology are discussed. The topology of the SIDO buck converter is shown in Fig. 4 where two independent outputs $V_1$ and $V_2$ are obtained from a single inductor L that is shared. Time multiplexing of L is done for the supply of energy to the outputs. $C_1$ and $C_2$ are output capacitors that provide current to the loads $I_1$ and $I_2$ respectively when the inductor is connected to the other output. The topology shown in Fig. 4 can be used for potentially larger number of outputs.

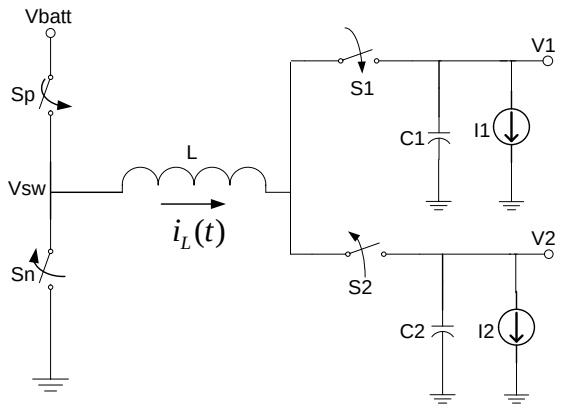


**Fig. 4 SIDO buck converter topology**

The costliest and most area consuming component on the board of a SMPS design is the inductor. For the buck converter shown in Fig. 2 the value of the inductance required for design parameters such as current ripple, input battery voltage, switching frequency and desired output voltage can be expressed as [1]:

$$L = \frac{V_o(1-\frac{V_o}{V_{in}})}{\Delta i_L f_s} \quad (1)$$

where $f_s$ is the switching frequency of $S_p$ and $S_n$ and $\Delta i_L$ is the desired inductor ripple current. The DC value of the inductor current is $I_o$ and the current ripple $\Delta i_L$ is chosen to be around 5-10% of it. Lower the inductor ripple current higher the design value of inductance required. The expression (1) is obtained assuming that the buck converter operates in continuous conduction mode (CCM) i.e. the current flowing through the inductor is positive throughout a switching cycle. CCM is the preferred mode of operation because larger ripple current flows through the inductor during discontinuous mode (DCM) of operation leading to greater current stress of the switches and higher conduction losses [1]. Let us consider that two output voltage rails of 1.2V and 1.5V are required. If two individual buck converters operate at 1 MHz each, the values of the inductances required are 2.5 µH and 2.4 µH for inductor ripple current of around 300mA. The converters enter DCM at 150mA load.

In order to design the inductor for the minimum possible ripple current for the SIMO buck converter with 'n' outputs the value of the inductance is chosen as:

$$\text{L=max}\left(\frac{V_1T_1(1-\frac{V_1}{V_{batt}})}{\Delta i_L}, \frac{V_2T_2(1-\frac{V_2}{V_{batt}})}{\Delta i_L} \ldots \frac{V_nT_n(1-\frac{V_n}{V_{batt}})}{\Delta i_L}\right) \quad (2)$$

where $\Delta i_L$ is the minimum current ripple and $T_1, T_2 \ldots T_n$ are the time windows for which L is connected to the outputs $V_1, V_2 \ldots V_n$ respectively. It is evident that instead of using 'n' inductors of different values, a single inductor of the maximum value ensures minimum ripple current excursion with significant area saving.

The sizing of the inductor is done using expression (2) if the equivalent series resistance (ESR) of the inductor is not considered. The DC current flowing through the inductor is the sum of the load currents of the SIMO converter $I_1 + I_2 + \ldots I_n$. Commercial power inductors have ESRs <1 ohm and switch resistances are in the same order. To avoid the increase in conduction losses, the ESR of the inductor has to be decreased; this can be done by increasing the cross sectional area of the inductor coil. For the same core material the inductance increases in proportion with the area. Hence the value of inductor increases linearly with total loading i.e. with the number of outputs. This implies that a 2.5µH inductor is required for a 1 MHz converter with 300mA load, then 5µH is required for a 500kHz converter with a SIDO buck converter with 300mA load at each output. The rise in cross sectional area of the inductor coil leads to very small increase in the overall volume of the inductor IC. However if the inductor ESR << switch resistance the inductor is sized according to expression (2).

At higher frequencies (3-8MHz) and lower power levels inductors are co-packaged i.e. placed side-by-side to the buck converter die. The style of the inductor used varies with the vendor, some using a copper spiral sandwiched between ferrite cores and others using multilayer ceramic type of inductors. At still higher frequencies (100's of MHz-GHz range), MEMS inductors are grown on the silicon of the buck converter die. These integrated inductor technologies lead to higher efficiency and greater power integrity but are costly. Using a single integrated inductor for obtaining multiple output voltage rails hence leads to significant cost savings. Hence the application of the SIMO buck converter topology becomes very relevant when integrated inductors are used in commercial products with the advantages of higher efficiency, better power integrity, along with higher area and cost savings.

The footprint of the PMIC that has multiple output voltage rails reduces when a SIMO buck converter topology is used. Fig. 5 shows the IC pinout for a PMIC that employs n

independent buck converters for n outputs. It is seen that the IC requires 2n pins for the connection of n inductors between the switching nodes and the feedback points at the outputs. Including the battery input and ground pin, the total number of pins required is 2n+2. The number of power devices required is 2n.

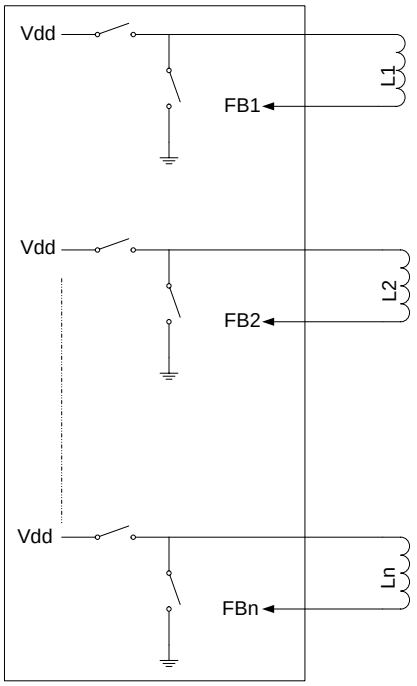


**Fig. 5 Individual buck converters for multiple voltages**

In the case of a SIMO buck converter depicted in Fig. 6, n pins are required for n outputs apart from which only 2 pins are required for connecting the inductor. Hence the total number of pins is n+4 if the battery input and ground pins are accounted for. The number of power switches required is n+2. For n>2 there is a decrease in the pin count of the PMIC leading to area and cost savings.

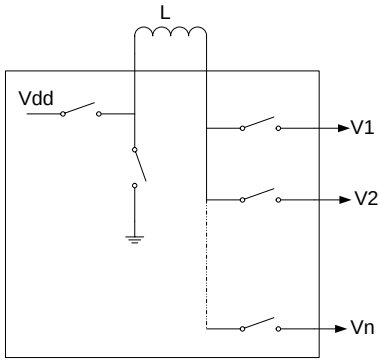


**Fig. 6 SIMO buck converter for multiple voltages**

The objective of this work is to demonstrate the functioning of the SIMO buck converter with two output voltage rails.

## B. Thesis Organization

The focus of this thesis is to demonstrate the control and functioning of a SIDO buck converter that is designed, simulated and laid out using AMI 0.5 µm CMOS process available from the MOSIS service. This particular SIDO Buck converter addresses the problem of cross-regulation, low load efficiency and operation across wide load ranges. Hysteresis control scheme is used in this work.

In the second chapter, the closed loop control principle of the SIDO buck converter is explained. Efficiency analysis is performed as well. In the third chapter, the operation of the SIDO buck converter is explained with the help of an architectural overview and related flow charts and timing diagrams. The implementation of different blocks in the architecture is discussed along with their specifications and performance results from CADENCE. In the fourth chapter, system level schematic and post-layout simulation results that are obtained in

CADENCE are also presented. In the sixth chapter the conclusions and scope for future work in the thesis are discussed.

# CHAPTER II

# SIDO BUCK CONVERTER CONTROL

In this chapter the control principle of the SIDO buck converter is explained. The converter uses feedback control which solves the issues inherent in the topology used. These issues are explained hence formulating the basis for the choice of the type of control.

## A. Proposed Solution

In this section the top level system architecture and operation proposed in the thesis is discussed. Further, the cross-regulation issue associated with the SIDO buck converter topology proposed is discussed along with solutions existing in literature. Also, a comparison of efficiency between the SIDO buck converter and dual independent buck converters is done.

Fig. 7 shows the SIDO buck converter embedded in closed loop control. The feedback controls the switching of $S_1, S_2, S_p$ and $S_n$ such that the inductor L is time multiplexed between the outputs $V_1$ and $V_2$ such that they are maintained at the desired levels Ref1 and Ref2 respectively. Both outputs are lesser in magnitude than the input $V_{batt}$. Switches $S_p$ and $S_n$ are complementary. A single control loop is used for voltages at the outputs of both the branches. The control pulses for the switches $S_1, S_2, S_p$ and $S_n$ are given to pre-drivers. In order to achieve low rise and fall times, pre-drivers are required for the bulky switches. Normally, non overlapping clock pulses are used to drive $S_p$ and $S_n$ in order to avoid "shoot through" currents from supply to ground. $S_p$ is referred to as the high side switch and $S_n$ as the synchronous switch. $S_p$ is implemented using a PMOS or an NMOS driven by a charge pump circuit. $S_n$ is

usually an NMOS switch. The passives L, $C_1$ and $C_2$ are off the chip. The feedback controller, pre-drivers and switches are integrated on chip using 3 Metal, 1 Poly, 5 V Supply 0.5 µm Process.

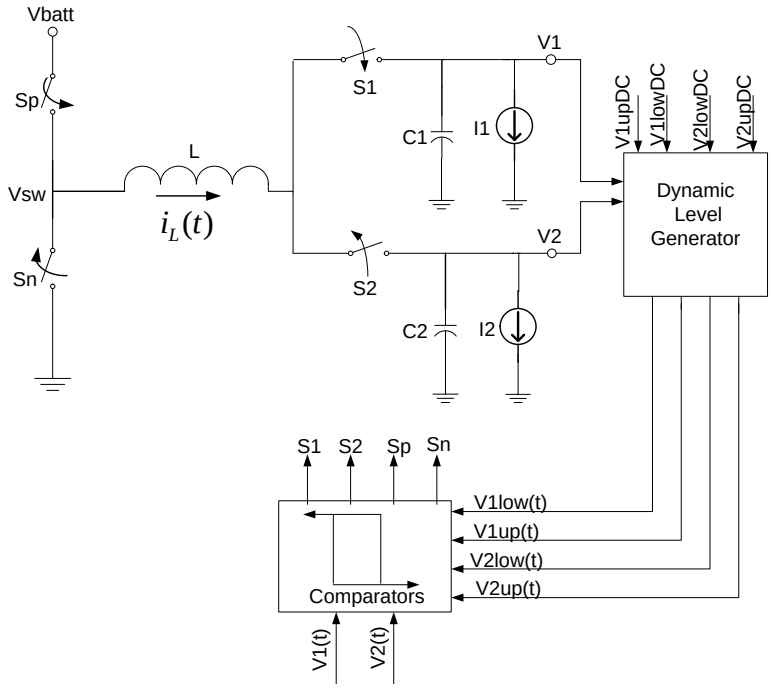


**Fig. 7 SIDO buck converter SMPS**

The timing diagram in Fig. 8 shows the different phases of operation of the SIDO buck converter. It is seen that the switch $S_1$ is ON for a time $T_1$ and switch $S_2$ is ON for a time $T_2$. $T_1$ and $T_2$ represent the time windows during which L is connected to outputs $V_1$ and $V_2$ respectively. The total time period is given by

$$T_s = T_1 + T_2 \tag{3}$$

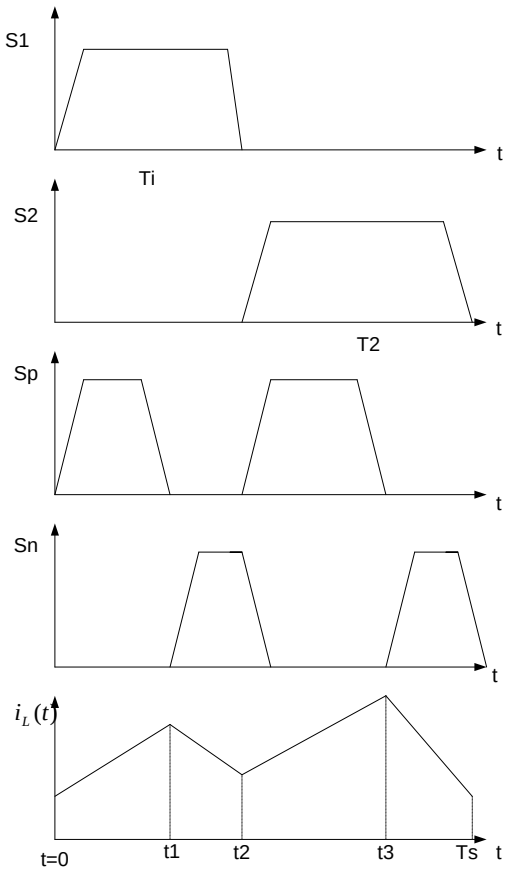


**Fig. 8 Timing diagram of the SIDO buck converter**

At time t=0, $S_p$ and $S_1$ are ON. Hence $i_L$ begins to flow through the output $V_1$ and the rate of current rise is $\frac{V_{batt}-V_1}{L}$. At time t=$t_1$, $S_p$ is turned OFF and $S_n$ is turned ON. Now the current falls with a slope $\frac{-V_1}{L}$. At time t=$t_2$, $S_1$ is turned OFF and $S_2$ is turned ON and $S_p$ is turned ON and $S_n$ is turned OFF. The current now rises with a slope of $\frac{V_{batt}-V_2}{L}$. At time t=$t_3$

$S_p$ is turned OFF and $S_n$ is turned ON and the inductor falls with a slope $\frac{-V_2}{L}$ until the end of the period $T_s$.

The width of each time window depends on the load demanded at each output and is altered interactively by the feedback controller. The time periods $T_1$, $T_2$ and $T_s$ are adjusted by the controller such that the average loads at both outputs are delivered over one time period if the converter is in steady state. The dynamics of the loop is adjusted by the controller such that during steady state the slopes of charge and discharge of the inductor satisfy the expressions:

$$\frac{\int_0^{T_1} i_l(t)dt}{T_s} = I_1 \tag{4}$$

$$\frac{\int_{T_2}^{T_s} i_l(t)dt}{T_s} = I_2 \tag{5}$$

Let us consider the case where $T_s$ is kept constant. A sudden decrease in $I_{1(2)}$ leads to increase in $V_{1(2)}$. This is sensed by the feedback regulator hence $T_{1(2)}$ is decreased as corrective action. As $T_s$ is constant $T_{2(1)}$ automatically increases. Thus the overall dynamics of the loop change until the new steady state condition is reached for the new load conditions. The voltage $V_{2(1)}$ hence increases as the average current flowing through this branch is in excess of the demanded load $I_{2(1)}$. This interactive behavior between the sub converters is known as "cross-regulation" and is undesirable as very different load demands at the outputs make the loop fall out of regulation.

The issue of cross-regulation arises from the sharing of boundary conditions of inductor current between the output branches. This causes coupling between the sub converters. If the inductor were to discharge to a state of zero current at the end of every time window, then independent load supply can be achieved at each output without undesirable rise or fall in voltage. However, the disadvantage of operating the SIDO buck converter in DCM for all load conditions is the rise in peak currents flowing through the inductor, increasing current stress of the switches and conduction losses [1]. This solution has been reported in [2-4]. To decrease the peak inductor currents the inductor may be reset to a constant value $I_{dc}$ instead of zero. This mode of operation is known as "Pseudo Continuous Conduction Mode" (PCCM) and has been reported in [5-6]. A variation of this technique is to reset the inductor to different current values that are dependent on the individual loads. Since $I_{dc}$ varies with the load, this technique is called "dynamic PCCM". The PCCM technique requires an additional reset switch $S_R$ across the inductor as shown in Fig. 9. The reset switch turns ON when the inductor current reaches the value $I_{dc}$. This leads to power loss across the ON state resistance of the switch. Low resistance switch design leads to additional area consumed by the power train. Further, current sensing circuits are required. These circuits are sensitive to high frequency noise.

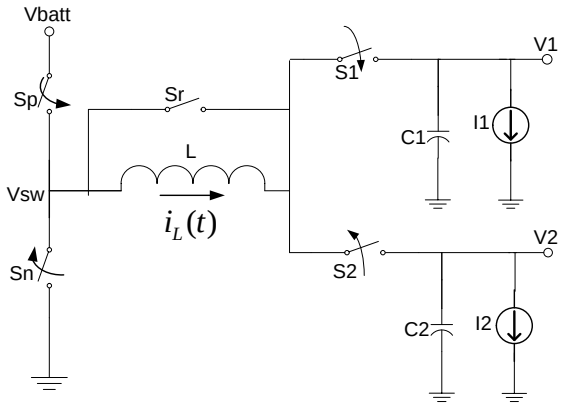


**Fig. 9 SIDO buck converter SMPS with reset switch**

Control methodologies like Adaptive delta modulation [7] and Ordered power distributive control [8] use digital algorithms and analog signal processing circuits to control the voltages by prioritizing the control based on the amount of load present. The solutions proposed have a fixed frequency of operation. This leads to the inability of the SIDO buck converter to get regulated for wide load ranges at both outputs.

In this work, the problem of cross-regulation is overcome by having variable frequency operation. Hence the conditions stated in (4) and (5) can be met irrespective of boundary condition of inductor current i.e. irrespective of load level at the other output. Also very wide load range is possible through variable frequency operation. Often in portable devices some of the functionalities are disabled putting the related systems in sleep mode, demanding very low load, while other functionalities are fully enabled. The SIDO buck converter must be able to supply the output at full load as well as the output at stand-by simultaneously without the undesirable rise or drop in voltage levels at either output. The forthcoming sections of the chapter discuss the control principle in detail.

### B. Hysteresis Control Principle

In this section the variable frequency control method used for the SIDO buck converter is described in detail. The objectives of the SIDO buck converter control are:

i) Obtaining the outputs $V_1(t)$ at $V_{1ref}$ = 1.2V and $V_2(t)$ at $V_{2ref}$ = 1.5V from a battery voltage $V_{batt}$ =3V

ii) Providing widely varying load currents $I_1$ and $I_2$ independent of one another. Maximum load currents are 300 mA at the outputs of the SIDO buck converter

iii) Maintaining the voltage ripples of $V_1(t)$ and $V_2(t)$ within permissible limits i.e. 10% of $V_{1,2ref}$

Both outputs of the SIDO buck converter should be controlled so that when the inductor is connected to an output $V_{1(2)}(t)$ the voltage at the other output $C_{2(1)}$ does not discharge due to high load current $I_{2(1)}$. Dynamic levels that contain information about the first derivatives of the output voltages are used for providing indication of the voltages and load currents at the outputs.

When the inductor L is connected to output $V_1(t)$ current at the second output is provided by the output capacitor yielding:

$$I_2 = C_2 \frac{dV_2(t)}{dt} \tag{6}$$

Hence the capacitor $C_2$ steadily discharges while providing the average load current $I_2$. Thus the first derivative of the voltage indicates the amount of load present at the respective outputs. In this work, two dynamic levels are defined about the reference level. These dynamic levels serve as thresholds with which the outputs are compared so that the voltage ripples are limited to within 10% of Ref1 and Ref2 respectively under various load conditions. Let an output

$V_{1,2}(t)$ have dynamic levels $V_{1,2up}(t)$ and $V_{1,2low}(t)$ whose DC values $V_{1,2updc}$ and $V_{1,2lowdc}$ are 5% about the reference value Ref1,2. The first derivatives of the voltages ride on the respective DC levels in the dynamic threshold limits. They are called dynamic levels because they vary with time.

$$\left.\begin{aligned} V_{1,2up}(t) &= V_{1,2upDC} - K_z * \frac{dV_{1,2}(t)}{dt} \\ V_{1,2ow}(t) &= V_{1,2lowDC} - K_z * \frac{dV_{1,2}(t)}{dt} \end{aligned}\right\} \quad (7)$$

The value of coefficient $K_z$ determines the effect of the first derivative on the dynamic levels. A very large value of $K_z$ causes high swing in the upper and lower dynamic levels and possibly their overlap whereas a small value desensitizes the threshold levels to load current variations increasing the output voltage ripple. Hence an optimum value of $K_z$ is chosen based on the desired swing in the dynamic levels for the value of $\frac{dV_o}{dt}$ at nominal load i.e. if the peak voltage value is attained at the output over a time period $\Delta T$ then the value of $K_z$ for a specified voltage ripple of $\Delta V_o$ and a desired swing of $\Delta V$ in the dynamic level is given by:

$$K_z = \frac{\Delta V \Delta T}{\Delta V_{1,2}} \quad (8)$$

For ripple voltage $\Delta V_{1,2}$ equal to about 10% of Ref1,2 and $\Delta T$ about 1 μs corresponding to a switching frequency of 1 MHz, the value of $K_z$ for a swing lesser than $\frac{\Delta V_{1,2}}{2}$ is < 0.5 μs.

When the output $V_{1,2}(t)$ crosses $V_{1,2up}(t)$ in the positive direction, this indicates that

i) $V_{1,2}(t)$ is higher than the upper static level $V_{1,2upDC}$

ii) $\frac{dV_{1,2}(t)}{dt}$ is positive i.e. $V_{1,2}(t)$ is continuing to increase

Hence the decrease of $V_{1,2}(t)$ is ensured by turning the switch $S_p$ OFF and $S_n$ ON in Fig. 10.

When the output $V_{1,2}(t)$ crosses $V_{1,2low}(t)$ in the negative direction, this indicates that

i) $V_{1,2}(t)$ is lower than the lower static level $V_{1,2upDC}$

ii) $\frac{dV_{1,2}(t)}{dt}$ is negative i.e. $V_{1,2}(t)$ is continuing to decrease

Hence the increase of $V_{1,2}(t)$ is ensured by turning the switch $S_p$ ON and $S_n$ OFF. Thus $V_{1,2}(t)$ is limited to the hysteresis band by comparing it with the dynamic levels to control the switches $S_p$ and $S_n$. By monitoring the output voltage and its first derivative, the transient response is improved leading to quicker convergence of the output voltage to the desired value.

Control of the switches $S_1$ and $S_2$ are also done based on the position of the output voltages with respect to the corresponding dynamic levels. Fig. 10 depicts the output voltage at steady state and the corresponding dynamic levels. Let us consider that the inductor is disconnected from the output $V_{1,2}$; then the capacitor $C_{1,2}$ discharges itself at the rate $\frac{I_{1,2}}{C_{1,2}}$. This causes a step increase in the dynamic level, making it move closer to the output voltage profile.

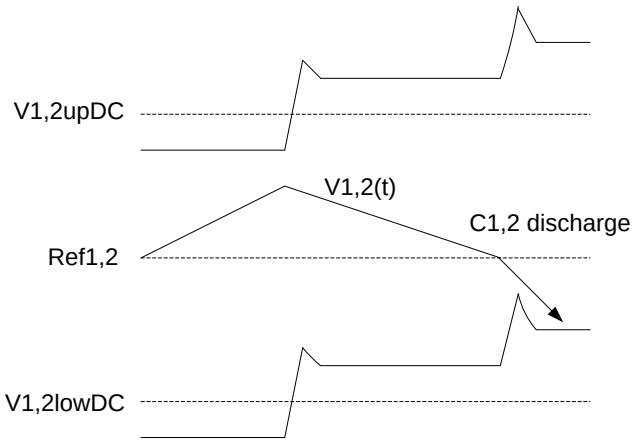


**Fig. 10 Output and dynamic threshold levels**

Hence, from Fig. 10 it is seen that the dynamic levels react to the first derivative of the output voltage in order to ensure that the ripple in $V_{1,2}$ is controlled to stay within the static bounds.

### C. Efficiency

There are two types of losses: switching losses and conduction losses. The switching losses occur due to dynamic energy dissipation through parasitic capacitances of bulky power switches during turn ON and turn OFF. The switches are not ideal and have ON state resistances, leading to voltage drops in the power stage hence conduction losses. The static analysis of a buck converter performed in [1] gives insight on the conduction losses in the system. Similar analysis is done on the SIDO buck converter topology [Appendix A] in order to compare the power efficiency of this topology to the dual buck SMPS options.

Let us consider two separate buck converters for obtaining two output rails of values $V_1 = 1.2V$ and $V_2 = 1.5V$ from a 3V battery. The corresponding values of the duty cycles are $D_1 \approx 0.4$ and $D_1 \approx 0.5$. If the load current at each output is $I_1 = I_2 = 300mA$ then the total

current drawn from the battery is $I_{batt} = I_1 D_1 + I_2 D_2$. The switch resistances are $R_p$ and $R_n$ and are assumed to all be equal to 0.5 Ω. Now the overall efficiency is given by [1]:

$$\frac{P_{out}}{P_{in}} = \frac{(V_1 I_1 + V_2 I_2)}{V_{batt} I_{batt}} \tag{9}$$

(9) can be expressed in terms of the voltage conversion ratios and switch resistances to give [1]:

$$\eta = \frac{\dfrac{D_1}{(1 + \dfrac{D_1 R_p + (1 - D_1) R_n}{R_1})} + \dfrac{D_2}{(1 + \dfrac{D_2 R_p + (1 - D_2) R_n}{R_2})}}{(D_1 + D_2)} \tag{10}$$

In (10) $R_1$ and $R_2$ are the equivalent load resistances at the respective outputs. Using the computed values it can be found the efficiency to be 91%. Hence there is only a 9% loss in efficiency due to conduction losses if two independent buck converters are used for obtaining dual outputs.

In the case of the SIDO buck converter with switch resistances $R_p$ the expression for the overall efficiency is [Appendix A]:

$$\eta = \frac{V_1 I_1 + V_2 I_2}{V_1 I_1 + V_2 I_2 + \sum I_{av} R_p} \tag{11}$$

For equal loads of $I_1 = I_2 = 300mA$ at the outputs and for $V_1 = 1.2V$ ; $V_2 = 1.5V$ the duty cycles are given by $D_1 = 0.4$ and $D_2 = 0.5$ just as in the case of independent buck converters. The efficiency is found to be 81%.

This shows that the efficiency of the SIDO buck converter is slightly less than that of two independent buck converters, if only conduction losses are accounted for. Switching and conduction losses can be reduced through the use of more sophisticated technology. Switching losses occur due to the charge and discharge of the parasitic capacitances $C_p$ is given by

$C_p V^2 F_s$ where V is the voltage across the terminals of the capacitance. Hence the switching losses are directly proportional to the frequency of switching. In this work, the maximum frequency is limited to below 1 MHz to minimize switching losses.

In the hysteretic control method described frequency increases at heavier load and decreases at lighter load. Low frequency leads to higher light load efficiency. Higher frequency at high loads decreases the ripple current decreasing the conduction losses at low loads which is the predominant factor. Hence the control method described in this chapter solves the issues of cross-regulation and improves the efficiency obtainable across a large range of load levels.

# CHAPTER III

# SYSTEM ARCHITECTURE

In this chapter, the control and operation of the SIDO buck converter is examined at the top level. The algorithm governing the control of switches is represented by means of a flowchart and timing diagrams. Next, the functional modeling of the blocks used in the feedback control is performed. Hence the design, implementation and performance of the functional blocks are derived from the modeling.

## A. System Overview

In this section the system architecture is presented with a general overview on the operations controlling the switches of the SIDO buck converter. Analog and digital blocks performing the control operations are discussed as well.

Fig. 11 shows the topology and control architecture of the SIDO buck converter. Four dynamic levels $V_{1,2low}(t)$ and $V_{1,2up}(t)$ are generated and each pair of upper and lower bounds serves the purpose of hysteretic comparison with the corresponding output $V_1(t)$ or $V_2(t)$. The outputs are compared to dynamic levels to give control signals $Up_{1,2}$ for switches $S_p$ and $S_n$.

For control of $S_1$ and $S_2$, the errors are compared to indicate the priority based on the larger error magnitude with the help of a flag 'M'. Also, an indication of the load current is obtained from the signals $Low_{1,2}$. When L is connected $V_{2(1)}$ larger load levels lead to faster discharge of the output capacitor $C_{1(2)}$ thus driving the signal $Low_{1(2)}$ high. The output with higher voltage error and higher load current is connected to the inductor and the corresponding

switch, $S_{1,2}$ is closed. Hence the digital control block uses the signal priority flag M and control signal $Low_{1,2}$ to manipulate $S_{1,2}$ appropriately.

Reverse current is detected through switches $S_1$ and $S_2$ in order to avoid the flow of negative current through the inductor. The digital control block ensures that when the reverse current detector is high the switches $S_n$ and $S_1$ are closed while all the other switches are immediately turned OFF. This switching action grounds the inductor terminals avoiding negative current flow through it.

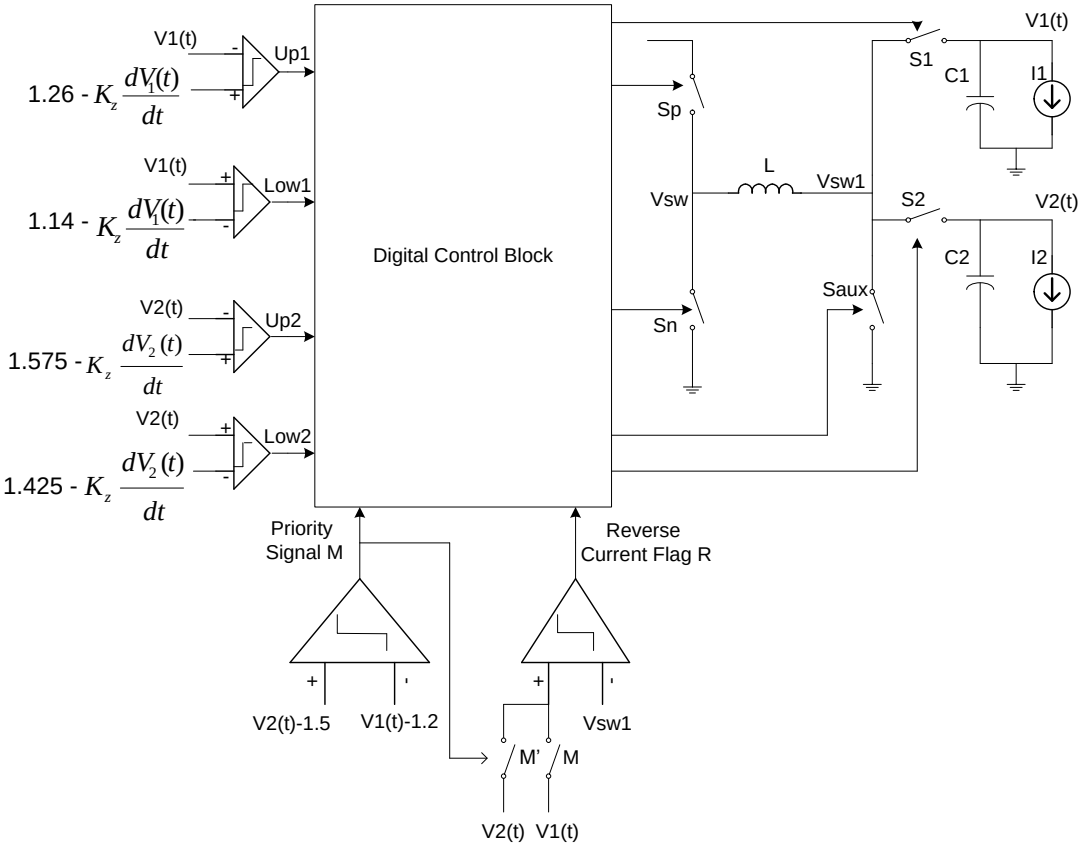


**Fig. 11 System Overview**

The system in Fig. 11 can be broadly divided into three parts:

a. Power stage consisting of the switches $S_1, S_2, S_p, S_n, S_{aux}$ and the inverter drivers

b. Analog control blocks that consist of the differentiators and continuous time comparators. The differentiators generate the dynamic threshold limits for each output. The comparators perform the following functions:

i) Comparison of error voltages $V_1(t) - V_{1ref}$ and $V_2(t) - V_{2ref}$ for priority control of the switches $S_1$ and $S_2$. The output of the priority comparator is represented by the flag 'M'.

ii) Comparison of dynamic threshold levels $V_{1,2low}(t)$ and $V_{1,2up}(t)$ with $V_{1,2}$ to control the switches $S_p$ and $S_n$ using the flags $Low_{1,2}$ and $Up_{1,2}$.

iii) Comparison of $V_{1,2}(t)$ with $V_{sw1}$ in order to detect reverse flow of current during lighter loads when the SIDO buck converter enters discontinuous conduction mode (DCM). The output of the reverse current comparator is represented by the flag 'R'.

c. Digital control consisting of the latches and combinational logic that resolve the signals from the analog comparators and accordingly control the switches.

In Fig. 12 the digital control of the switches $S_{1,2}$ is shown. Let us consider that initially $S_2$ is ON. Priority flag M goes high when the error magnitude of $V_1(t)$ is greater than that of $V_2(t)$. However, $S_2$ is turned OFF and $S_1$ is turned ON only if $Low_1$ is high i.e. if $V_1(t)$ is lower than $V_{1low}(t)$, indicating high load current $I_1$. Hence if $V_1(t)$ has higher error magnitude but is safely higher than the lower static level the inductor remains connected to $V_2(t)$.

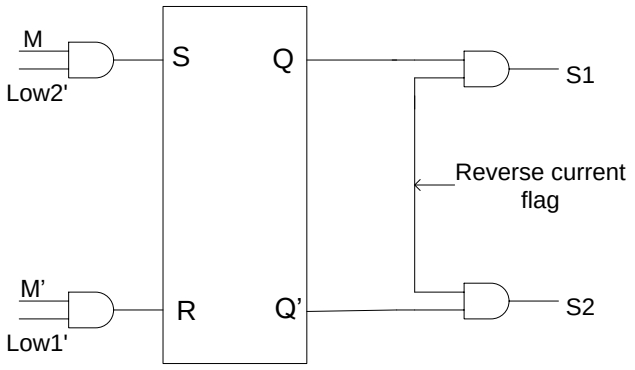


**Fig. 12 Control of switches** $S_{1,2}$

The SR latch in Fig. 12 implements this logic for the control of the switches $S_{1,2}$ are kept the same unless current is demanded by the other output. The outputs of the latch are ANDed with the reverse current flag to make sure that the switches $S_1$ and $S_2$ are OFF when the reverse current flag is high.

In Fig. 13 the digital control of the switches $S_n$ and $S_p$ is shown. When the priority signal M is high then the control signals considered are $Low_1$ and $Up_1$ corresponding to output $V_1(t)$. When the priority signal M is low the control signals considered are $Low_2$ and $Up_2$ corresponding to the output $V_2(t)$. When $Low_{1,2}$ is high, $S_p$ is turned ON and $S_n$ is turned OFF. When $Up_{1,2}$ is high $S_p$ is turned OFF and $S_n$ is turned ON. Thus the hysteretic control action is taken by the latch and gates. The signal $S_{pn}$ is ORed with the reverse current flag to make sure that $S_p$ is OFF when the reverse current flag is high.

The output of the latch $S_{pn}$ is given to buffers that drive the switches $S_{p.n.}$. $S_{p.}$ follows complementary logic as it is a PMOS switch.

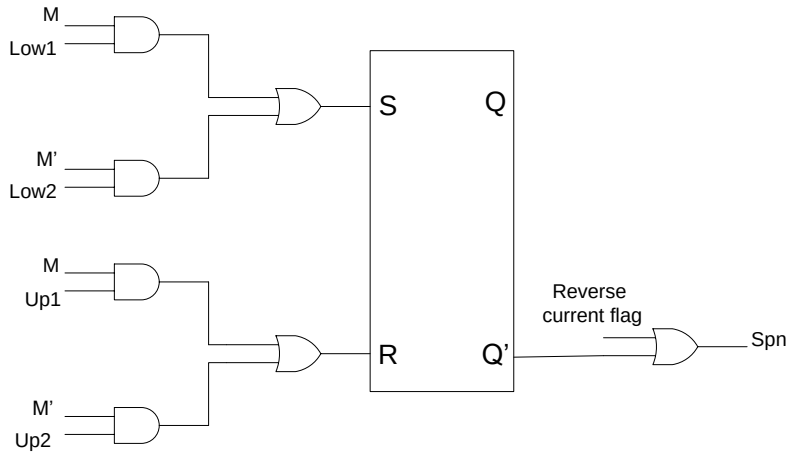


**Fig. 13 Control of switches** $S_{p.n.}$

The SR latch in Fig. 12 and Fig. 13 is implemented by cross coupled NOR gates.

### B. Asynchronous Control Flow

In this section the logical flow of operations performed by the digital circuits discussed in the previous section is presented with the help of a flowchart. Timing diagrams further illustrate the operation of the SIDO buck converter for different load conditions.

The flowchart in Fig. 14 explains the sequence of operations that the digital controller implements. In the flowchart, priority is first decided based on the output voltage error. The inductor is connected to the output with higher voltage error when it goes below the correspondingly lower dynamic level. Thus the prioritization is sensitive to both load and voltage levels at the outputs.

Once the inductor is connected to a particular output, the voltage is compared to corresponding dynamic levels for manipulation of $S_p$ and $S_n$. $S_p$ is switched ON when the

voltage goes below the lower dynamic threshold and $S_n$ is turned ON when the voltage overshoots the upper dynamic threshold.

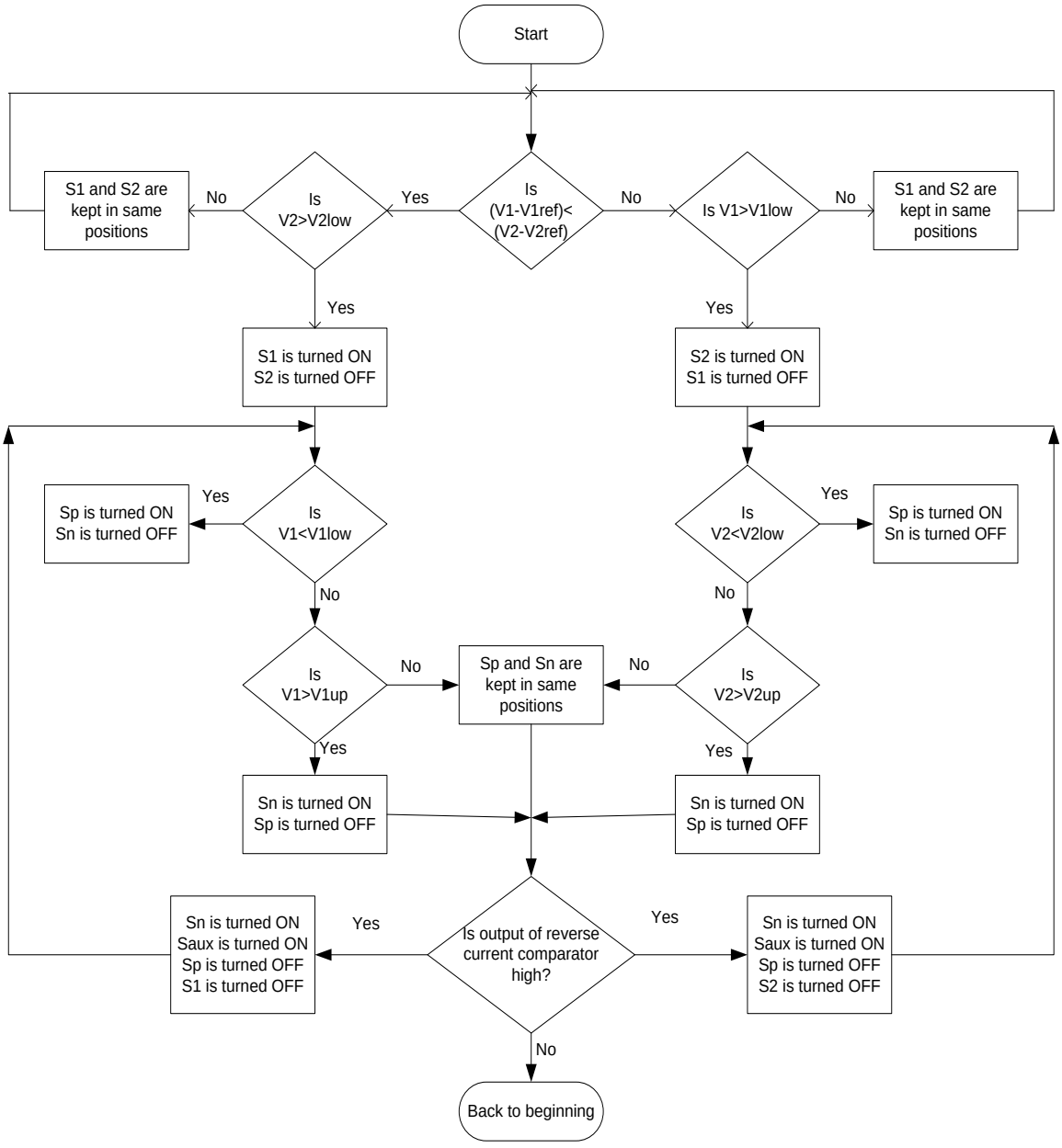


**Fig. 14 Logical flow of operations in the SIDO buck converter**

Thus asynchronous control of the SIDO buck converter is established through variable frequency control pulses that manipulate the power switches. The comparators and digital logic block ensures that the output with higher error and higher load current has priority over the other output. Three possible loading conditions along with the sequence of action is represented in Fig. 15 (a), (b) and (c).

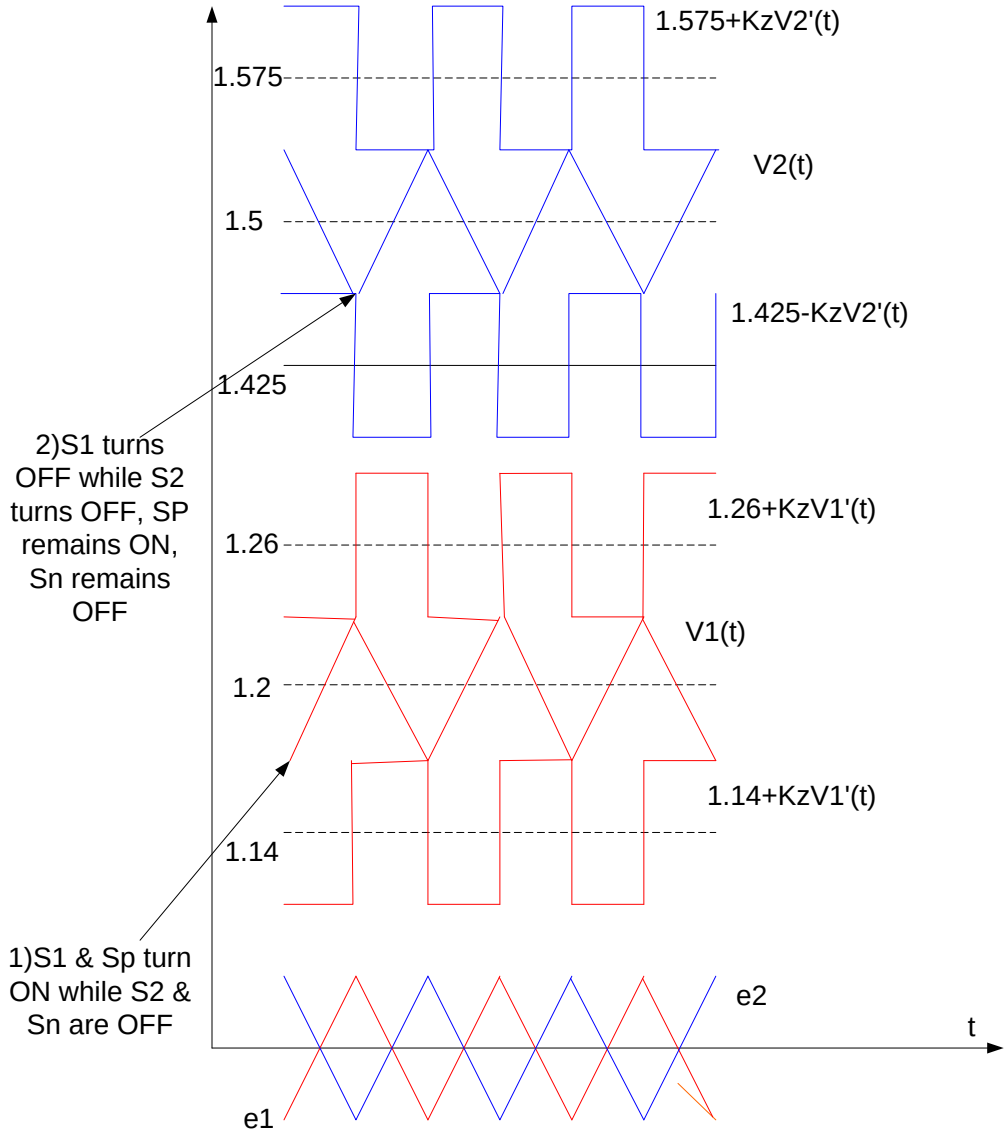


**Fig. 15A. Heavy-Heavy load condition**

In Fig. 15 (a) the dynamic threshold levels of both the outputs are closer together at heavy load condition. The effective frequency of the system is thus increased. The average current drawn from the inductor is high, hence $S_{aux}$ remains OFF throughout the operation.

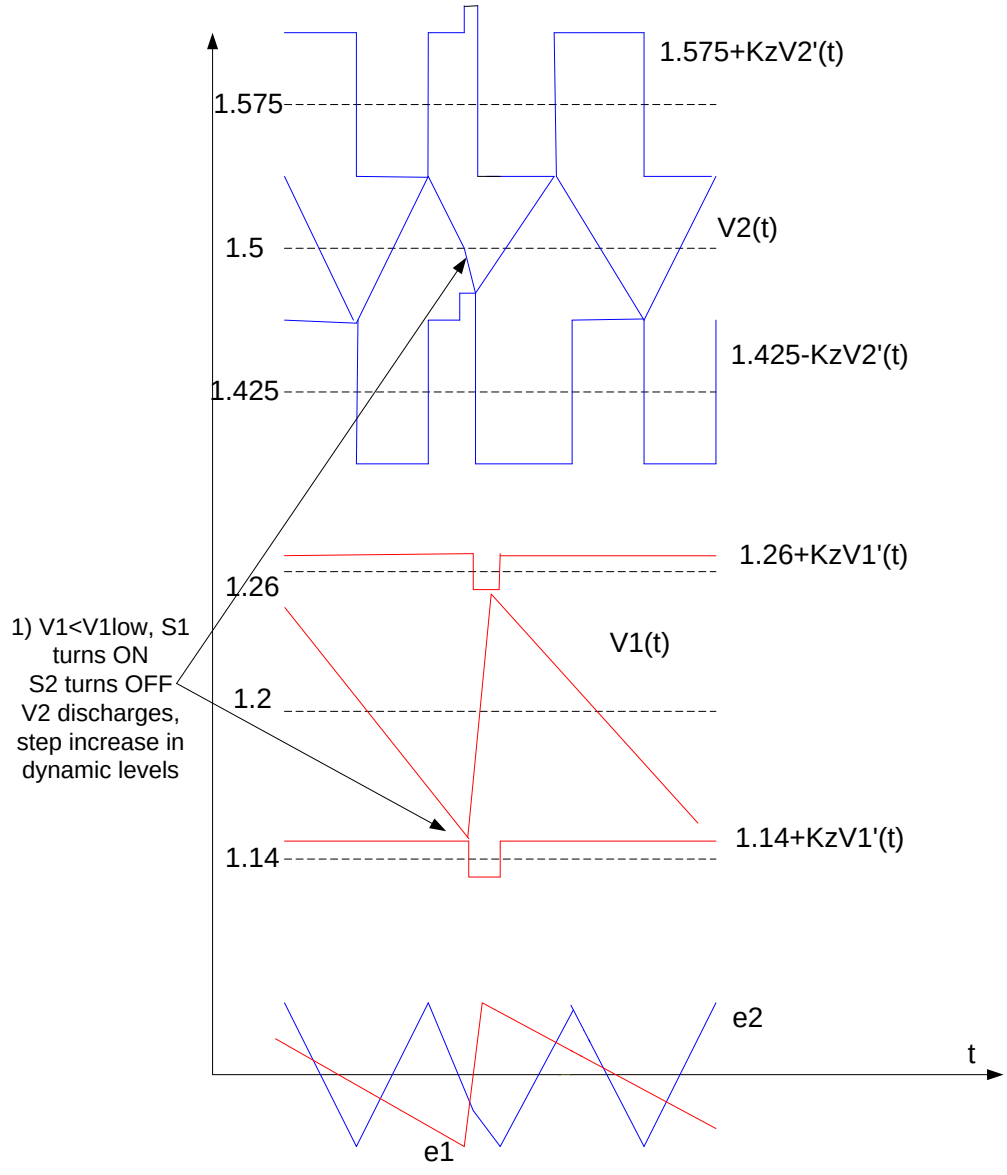


**Fig. 15B. Heavy-Light load condition**

In Fig. 15 (b) the dynamic threshold levels of $V_2(t)$ are closer together because of heavy load condition and those of $V_1(t)$ are farther apart due to light load condition. This leads to the inductor being connected to $V_2(t)$ for majority of the time period. The effective frequency of the system decreases as the overall output power demand drops. The SIDO buck converter may enter DCM turning $S_{aux}$ ON when current through inductor goes negative.

There is a step change in the dynamic levels of $V_2(t)$ due to the discharge of $C_2$ when the inductor switches to $V_1(t)$. The step increase in $V_{2low}(t)$ assures that the inductor rapidly gets connected back to $V_2$. The small duration for which the inductor is connected to $V_1(t)$ is sufficient to charge the output voltage because of the low value of load current $I_1$.

Hence the system is mostly in rest state, drawing quiescent current for the operation of the circuitry, and turning on the power switches occasionally in order to charge the inductor when required. In order to heighten power savings, the circuits can be designed such that they burn very low power at low load, because the frequency of operation drops. The bandwidth required also drops, and lesser quiescent current can be burnt to further optimize the power savings.

In portable systems such as the cellular phone, when in sleep mode very low load is present. In this condition, if the frequency of switching reduces to very low values, this does not cause interference with the audio signal as the transmitter and receiver will not be used in sleep mode.

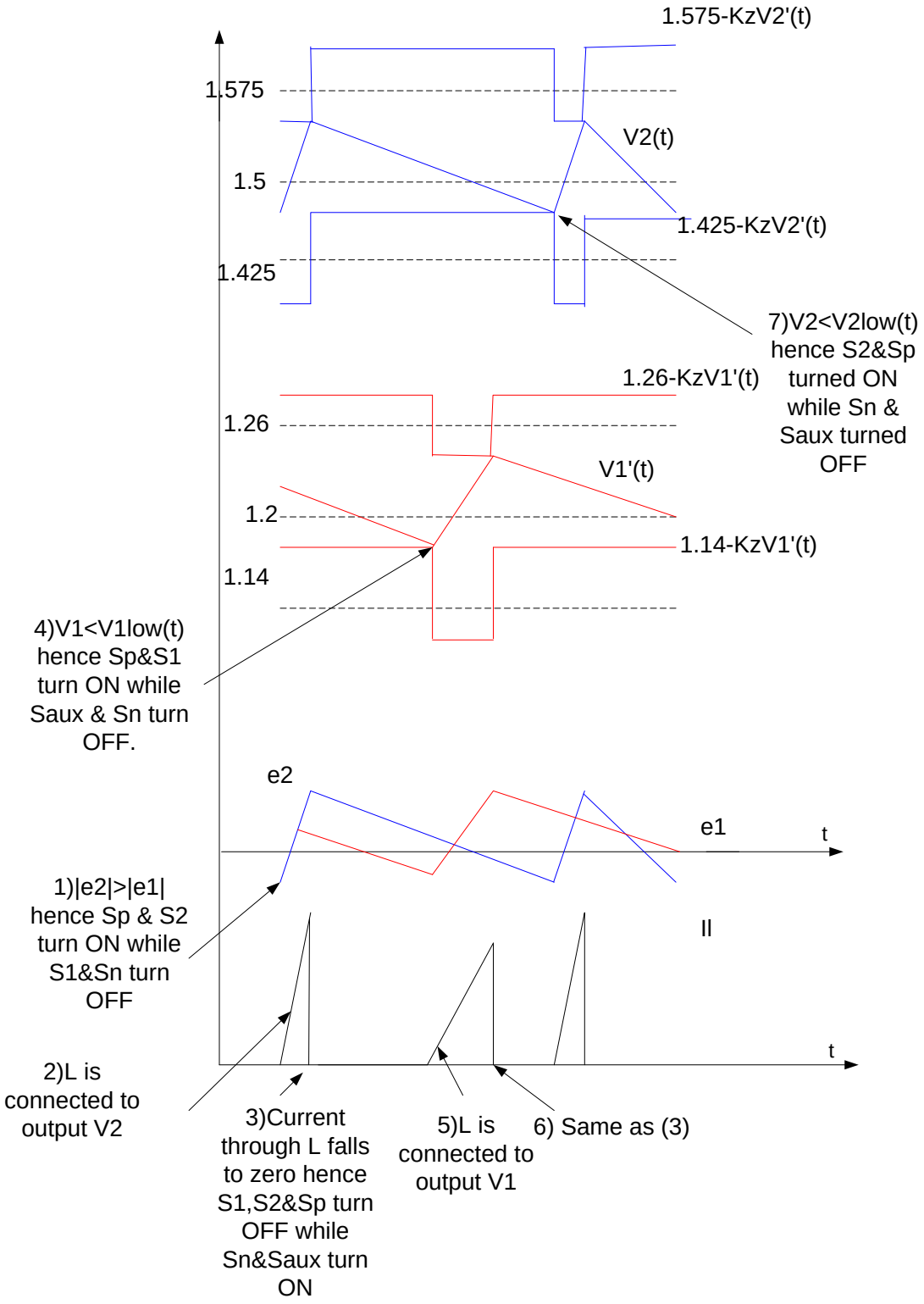


**Fig. 15C. Light-Light load condition**

It is seen in Fig. 15 (c) that the dynamic threshold levels of both outputs are farther apart due to light load condition. The effective frequency of the system hence drops and the SIDO buck converter operates in DCM turning $S_{aux}$ ON during reverse current flow through the inductor. Occasional spikes of current are supplied by the inductor to the output with higher priority in order to maintain outputs within permissible levels. The sequence of actions that are taken is labeled in Fig. 15 (c).

In this section it is evident that the hysteresis control principle leads to the outputs of the SIDO buck converter to have controlled ripple despite a wide range of load currents. The problems of oscillation and instability that are common in PWM controlled SIDO converters are also avoided by using the hysteresis control method.

## C. System Implementation

In this section the circuit level implementation of various blocks is explained. The design concerns from system level performance perspective are discussed.

### 1. Dynamic Threshold Level Generators

Dynamic thresholds serve as hysteresis bounds for comparison. Table I gives a summary of dynamic threshold levels that are generated.

**TABLE I**

**DYNAMIC THRESHOLD LEVELS**

| Significance | Nomenclature | Mathematical Function |
|---|---|---|
| Lower Dynamic Threshold Level of $V_1$ | $V_{1low}(t)$ | $V_{1lowdc} - K_z \frac{dV_1(t)}{dt}$ |
| Upper Dynamic Threshold Level of $V_1$ | $V_{1up}(t)$ | $V_{1updc} - K_z \frac{dV_1(t)}{dt}$ |
| Lower Dynamic Threshold Level of $V_2$ | $V_{2low}(t)$ | $V_{2lowdc} - K_z \frac{dV_2(t)}{dt}$ |
| Upper Dynamic Threshold Level of $V_2$ | $V_{2up}(t)$ | $V_{2updc} - K_z \frac{dV_2(t)}{dt}$ |

In Table II $V_{1lowdc}$ =1.14 V $V_{1updc}$ =1.26 V $V_{2lowdc}$ =1.425 V $V_{2updc}$ =1.575 V and are chosen to be 5% about the reference value $V_{1ref}$ =1.2V and $V_{2ref}$ =1.5V ' $K_z$ ' is chosen as 0.05 μs for obtaining switching frequency of 1 MHz for each converter. For generating the dynamic thresholds an opamp differentiator is used, as shown in Fig. 16. The differentiators are connected to the outputs $V_{1,2}(t)$ of the SIDO converter.

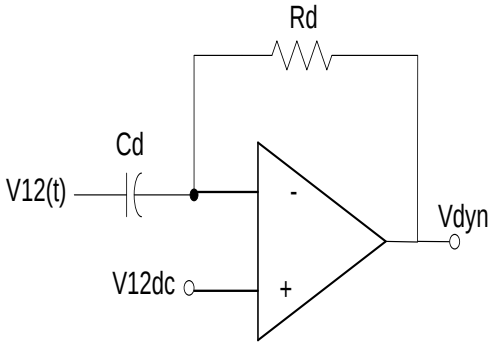


**Fig. 16 Opamp differentiator**

For the differentiator shown in Fig. 16,

$$V_{dyn} = V_{12dc} - R_d C_d \frac{dV_{1,2}(t)}{dt} \tag{12}$$

The feedback resistor $R_d$ is implemented by a NMOS $M_d$ in triode region in all of the four differentiators. The time constant of the differentiator $R_d C_d$ is the coefficient $K_z$ of the desired dynamic thresholds. The expression for resistance of $M_d$ in triode region is

$$R_d = \frac{1}{\mu C_{ox} \frac{W}{L}(V_{gs} - V_T)} \tag{13}$$

In AMI 0.5 µm process for NMOS, $\mu C_{ox}$ =128 X $10^{-6}$ and the threshold voltage when body voltage is accounted for is approximately given as $V_T = 0.9V$. For $V_g = 3V$ the value of $\frac{W}{L}$ is 1 in order to obtain $R_d$ =10 kΩ. The values of $K_z$ corresponding to $C_d$ =4pF and various values of $R_d$ are listed in Appendix-B.

$V_{dc}$ is set at the DC level of the dynamic threshold level. For the output $V_1(t)$ the dynamic thresholds are about 1.14V and 1.26V. A single stage differential pair with PMOS input pair is used so that tail current source transistor $M_b$ does not enter triode region of operation. Fig. 17 shows the circuit for generation of $V_{1low,up}(t)$.

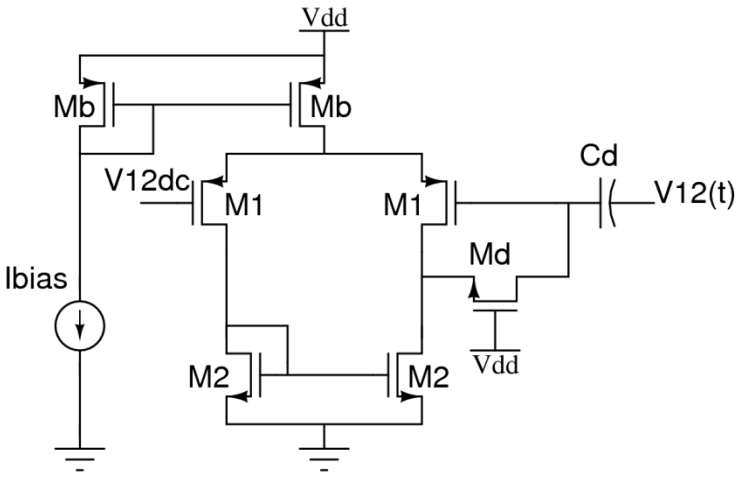


**Fig. 17 Differentiator for** $V_{1low,up}(t)$

For the output $V_2(t)$ the dynamic thresholds are about 1.425V and 1.575V and a differentiator with NMOS input pair is used for generating $V_{2low,up}(t)$, as shown in Fig. 18.

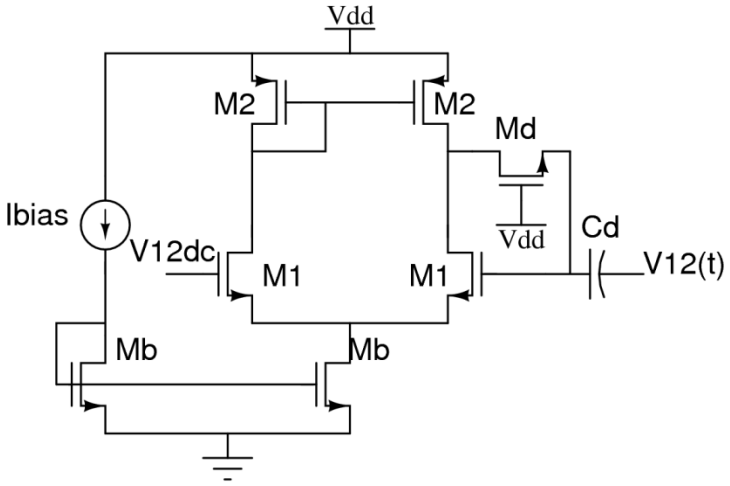


**Fig. 18 Differentiator for** $V_{2low,up}(t)$

There are several specifications for the design of the single stage differential pair opamp. The requirements of the opamp are explained below.

***i) Systematic Offset***

The sizing of the transistors $M_2$ are done such that there is no systematic offset, i.e. when the DC input is $V_{dc}$ it is assured that

$$V_{dd} - V_{sgM2} = V_{12dc} \tag{14}$$

Equation (14) ensures that the quiescent voltage at the source of M2 is equal to $V_{12dc}$ so that inaccuracy due to systematic offset is avoided.

***ii) Output Swing***

The inputs to the differentiators have ripple values of 120 mV or 150 mV depending on whether the differentiator is at the output $V_1(t)$ or $V_2(t)$ respectively. If GBW effects are ignored, $|V_{out}(f)| = 2\pi f R_d C_d$. At f= $f_s$ = 1 MHz the calculated peak values at the outputs are shown in Table II.

**TABLE II**

**OUTPUT VOLTAGE SWINGS OF DIFFERENTIATORS**

| Dynamic Level Generated | Output voltage swing $V_{out}$ (mV) @ 1 MHz |
|---|---|
| $V_{1low}(t)$ | 23 |
| $V_{1up}(t)$ | 30 |
| $V_{2up}(t)$ | 57 |
| $V_{2low}(t)$ | 43 |

### *iii) DC Gain and Accuracy*

If maximum swing at the output is $V_{out}$ then the maximum error in the DC value at the output differentiator is given as $|V_{12ref} - V_{12dc}| - \frac{V_{out}}{2}$. This quantity can be expressed as a percentage of the output DC value $V_{12dc}$ to give the minimum accuracy and gain required of the opamp. Low accuracy may lead to the crossing of upper and lower dynamic levels thus leading to higher ripple at the output voltages. The minimum DC gain is designed to be around 100 for 1% accuracy. Design details and performance of differentiators is in Appendix-B.

## 2. Dynamic Level Comparators

The dynamic levels are compared to corresponding outputs to monitor if the voltage is within permissible levels of ripple. As the outputs are constantly monitored, continuous time comparators must be used. A two stage single ended differential pair in open loop is used as a comparator shown in Fig. 19.

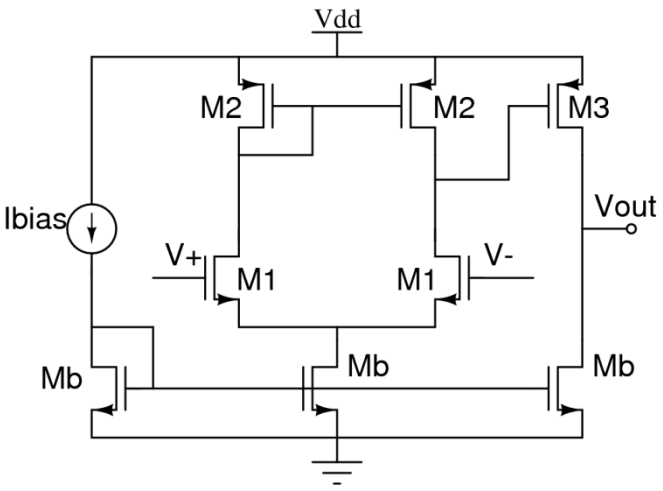


**Fig. 19 Continuous time comparator**

Offset and resolution of the comparator [9] are the most important specifications as the swings of the differentiators are below 50 mV. Input referred offset $V_{os}$ of the priority comparator is minimized for better accuracy of the output voltages $V_{12}(t)$. Random offset can be minimized by designing M1 with large overdrive voltage and by using good layout techniques that improve matching [10]. Resolution of the comparator of gain A is given as $\frac{V_{dd}}{A}$ where $V_{dd}$ is the required output swing of the comparator. Hence for resolution of around 3 mV and $V_{dd}$ of 3V the gain of the comparator has to be at least 1000.

**3. Priority Comparator**

The control of the switches to the load is based on the priority of the error of each output. The magnitudes $V_1(t) - V_{1ref}$ and $V_2(t) - V_{2ref}$ are compared. Equivalently $\frac{V_1(t) + V_{2ref}}{2}$ and $\frac{V_2(t) + V_{1ref}}{2}$ are compared to give the priority bit M, as shown in Fig. 20. Table III shows the values of M for various combinations of error voltages.

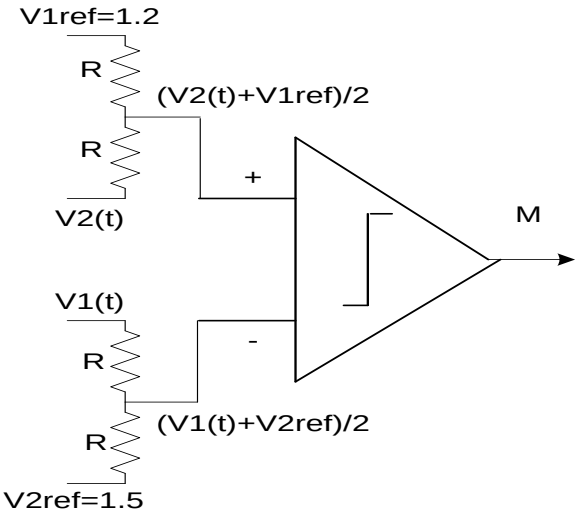


**Fig. 20 Priority comparator**

**TABLE III**

**TRUTH TABLE FOR PRIORITY COMPARATOR**

| Error 1 $e_1 = V_1 - V_{1ref}$ | Error 2 $e_2 = V_2 - V_{2ref}$ | Output of priority comparator M | Significance |
|---|---|---|---|
| $V_1 > V_{1ref}$ | $V_2 > V_{2ref}$ | 1 | $\|e_1\| < \|e_2\|$ |
| | | 0 | $\|e_1\| > \|e_2\|$ |
| $V_1 > V_{1ref}$ | $V_2 < V_{2ref}$ | 0 | |
| $V_1 < V_{1ref}$ | $V_2 > V_{2ref}$ | 1 | |
| $V_1 < V_{1ref}$ | $V_2 < V_{2ref}$ | 1 | $\|e_1\| > \|e_2\|$ |
| | | 0 | $\|e_1\| < \|e_2\|$ |

Gain of 1000 gives a resolution of around 5 mV and is sufficient for the accurate functioning of priority comparator.

**4. Reverse Current Comparator**

Reverse flow of current through the inductor is sensed by a negative voltage across the switches $S_{1,2}$ The drain (D) and source (S) voltages of the switches $S_{1,2}$ are compared depending on which of the switches is ON. The D-S voltages of the switches are $V_{sw1}(t) - V_1(t)$ and $V_{sw1}(t) - V_2(t)$. The reverse current comparator is shown in Fig. 21.

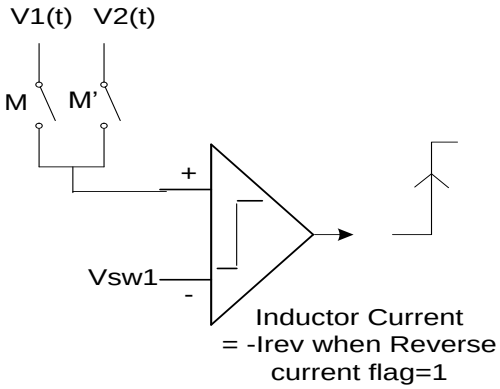


**Fig. 21 Detection of reverse current flow**

The rise time of the comparator is a critical design parameter because the current through the inductor rapidly goes negative causing negative voltage drop across the D-S terminals of the switches $S_{1,2}$. The negative voltage is detected by the comparator to raise the reverse current flag. Ideally the output of the reverse current comparator goes high when the voltage across $S_{1,2}$ crosses zero. Due to the propagation delay $t_r$ of the comparator $i_L(t)$ reaches a negative value $I_{rev}$ in the negative direction before the reverse current comparator is

triggered. For higher light load efficiency $I_{rev}$ drawn in the negative direction needs to be as small as possible, hence a low value of $t_r$ is to be attained.

Fig. 22 illustrates the flow of negative current $i_L(t)$ from the output $V_{1,2}(t)$ to ground through L, $S_{1,2}$ and $S_n$ before the reverse current flag is raised. The capacitor $C_{1,2}$ is assumed to be large enough for the ripple of $V_{1,2}(t)$ to be negligible hence maintaining the outputs at the DC levels $V_{1,2}$ at light load.

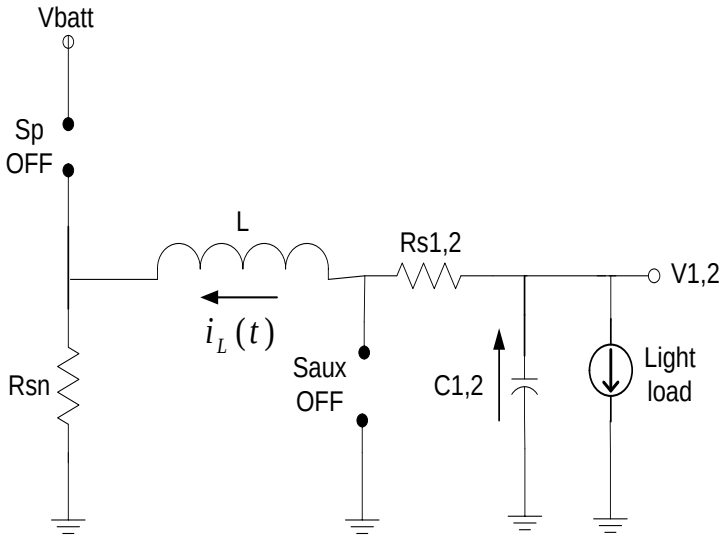


**Fig. 22 Negative current from output $V_{1,2}$**

If $R_{s1,2}$ is the resistance of switch $S_{1,2}$ and $R_{sn}$ is resistance of switch $S_n$ it can be obtained that:

$$V_o = +L\frac{di_L(t)}{dt} + i_L(t)(R_{sn} + R_{s1,2}) \tag{15}$$

Solving the differential equation (15) for $i_L(t)$,

$$i_L(t) = \frac{V_o}{(R_{sn} + R_{s1,2})}(1 - e^{\frac{-Rt}{L}}) \tag{16}$$

The current $I_{rev}$ is reached at the time $t_r$. These boundary conditions are applied to (16) to obtain $t_r$ for a desired $|I_{rev}|$.

$$t_r = \frac{L}{(R_{sn} + R_{s1,2})} \ln\left(\frac{1}{1 - \frac{|I_{rev}|(R_{sn} + R_{s1,2})}{V_{1,2}}}\right) \tag{17}$$

The values of $t_r$ for outputs $V_{1,2}(t)$ are shown in Table IV for L=1 μH, $R_{s1,2} = R_{sn}$=0.5 Ω, $|I_{rev}|$= 40mA. The minimum value is chosen as the specification $t_r$ =27 ns.

**TABLE IV**

**MINIMUM RISE TIMES OF COMPARATOR for $I_{rev}$ =40 mA**

| Output | $t_r$ (ns) |
|---|---|
| $V_1$ =1.2 V | 34 |
| $V_2$ =1.5 V | 27 |

The output of the comparator needs to toggle from zero to $V_{dd}$ during $t_r$, hence the minimum value of positive slew rate is obtained as

$$SR_+ = \frac{V_{dd}}{t_r} = 111V/\mu s \tag{18}$$

Fig. 23 shows the flow of current during the period when $S_{aux}$ is turned ON. The current dies from - $I_{rev}$ to zero exponentially with a time constant of $\frac{L}{R_{sn}+R_{saux}}$.

The design details and performance of the comparators are given in Appendix-C.

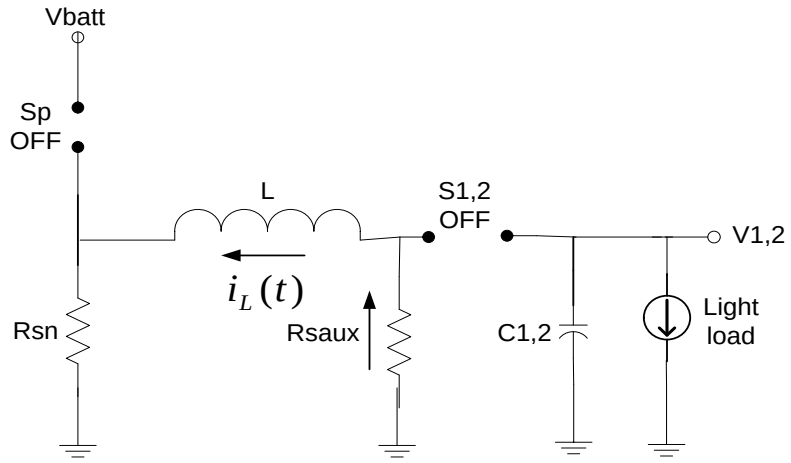


**Fig. 23 Current flow through $S_{aux}$ and $S_n$**

**5. Switches**

The topology of the SIDO buck converter with switch implementations is shown in Fig. 24. $S_p$ is implemented by a PMOS transistor. $S_1, S_2, S_n$ and $S_{aux}$ are implemented by NMOS transistors.

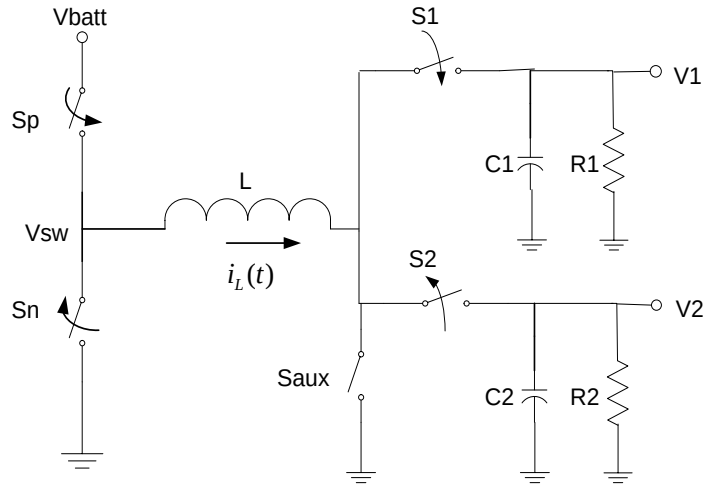


**Fig. 24 SIDO buck topology**

The values of the switch resistances of determine the overall voltage drops in the power train, hence the resistive losses of the system

$$R_{loss} = \frac{1}{\mu C_{ox} * \frac{W}{L} * (V_{gs} - V_{th})} \tag{19}$$

$R_{loss}$=0.5-1Ω is desired value for the switch resistances. For a PMOS $\mu C_{ox} = 50X10^{-6}$ and for a NMOS $\mu C_{ox} = 128X10^{-6}$ in the AMI 0.5 µm technology. In the presence of body effect $V_{th}$ of the NMOS is around 0.9V. For the desired value of $R_{loss}$ the aspect ratios of the power switches are $\left(\frac{W}{L}\right)_p = 30{,}000$, $\left(\frac{W}{L}\right)_n = 10{,}000$, $\left(\frac{W}{L}\right)_1 = 20{,}000$ & $\left(\frac{W}{L}\right)_1 = 20{,}000$.

For switches $S_p$, $S_n$ and $S_{aux}$ there is no body effect present as their sources are tied to the bulks, hence $V_{th}$ are approximately 0.9V and 0.7V for the PMOS and the NMOS respectively. The swing at the gates is equal to $V_{dd}$ (=3 V). The value of $V_{dd}$ =10,000 and $V_{dd}$ =30,000 for attaining $V_{dd}$ <1 For switches $S_1$ and $S_2$ the presence of body effect increases the

values of $V_{th}$'s. Hence the gate swings are made higher than $V_{dd}$ (=4 V) to attain lower switch resistance values. A charge pump is not designed in this work for obtaining a gate swing of 4 V; instead an external supply is used.

Another important consideration that comes with large size switches is the parasitic junction capacitances. The tradeoff in switch design arises from the need to have bulkier switches for lower resistance and higher current stress, but this leads to large capacitances at the junctions. Solutions have been proposed where dynamic switching is used i.e. the size of the switch varies with the load. Lower load values require lesser number of unit transistors in parallel. At higher loads, larger number of transistors is put in parallel. The switch size is manipulated through digital control and registers [11]. Design parameters and switch parasitic are presented in Appendix D.

# CHAPTER IV

# SIMULATION RESULTS

In this chapter the schematic transistor level and post layout simulations of the SIDO Buck Converter are performed in order to verify the operation Thus the performance of the system is assessed through parameters such as voltage ripple, current ripple, frequency vs. load variation, overall power efficiency, cross-regulation and disturbance rejection.

## A. Schematic Simulations

In this section the transient start-up and steady state convergence of the SIDO buck converter are demonstrated via the Spectre simulation engine in CADENCE. Simulations are run at different load combinations at the outputs, thus highlighting the capabilities of the controller to regulate a wide range of loads.

### 1. Heavy-Heavy Load Combination

Maximum load i.e. 300 mA is present at each output hence the total loading on the inductor is 600 mA. The objective is to demonstrate the supply of heavy load current whilst maintaining the outputs within well controlled ripple bounds set by static levels. Dynamic thresholds that are superimposed on the static levels serve the purpose of controlling the output voltage ripple irrespective of the load condition. If static bounds were used, the amount of ripple voltage present at the output would depend on the load current value, which implies that the ripple voltage is not well controlled.

The output voltage $V_1(t)$ and corresponding dynamic levels are seen in Fig. 25(a), where the ripple voltage is within static bounds 1.26V and 1.14V. Any overshoots or undershoots over the static bounds is due to the response time of the loop control. In Fig. 25(b)

the control of $V_1(t)$ using static levels is depicted. The ripple is large and undesirable overshoot is exhibited in the output waveform.

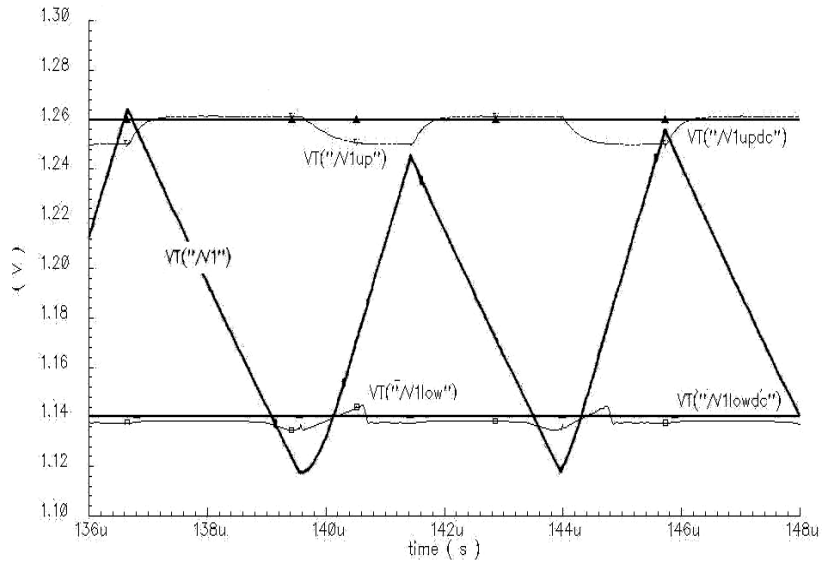


**Fig. 25A. Control of $V_1(t)$ using dynamic thresholds**

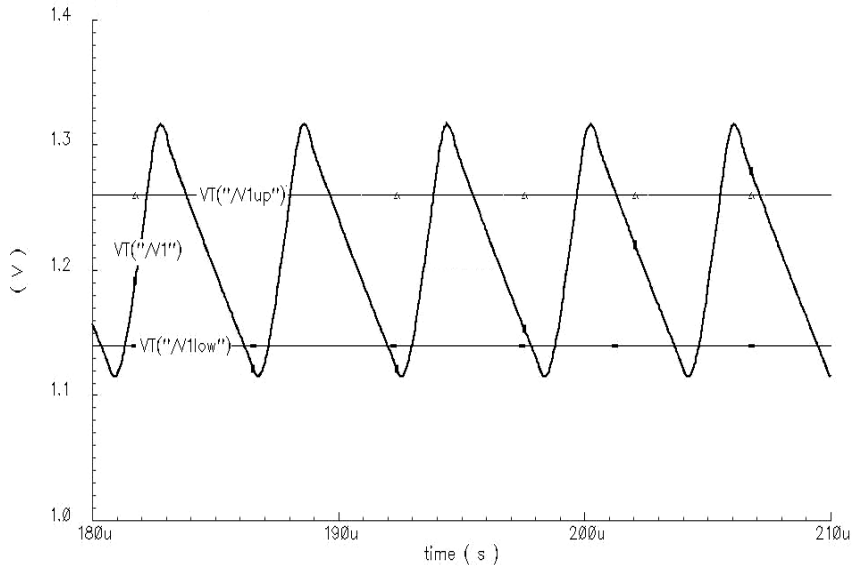


**Fig. 25B. Control of $V_1(t)$ using static thresholds**

Similarly the low ripple waveform $V_1(t)$ when controlled by dynamic levels is depicted in Fig. 26(a). In Fig. 26(b) $V_1(t)$ has higher ripple due to static hysteresis control.

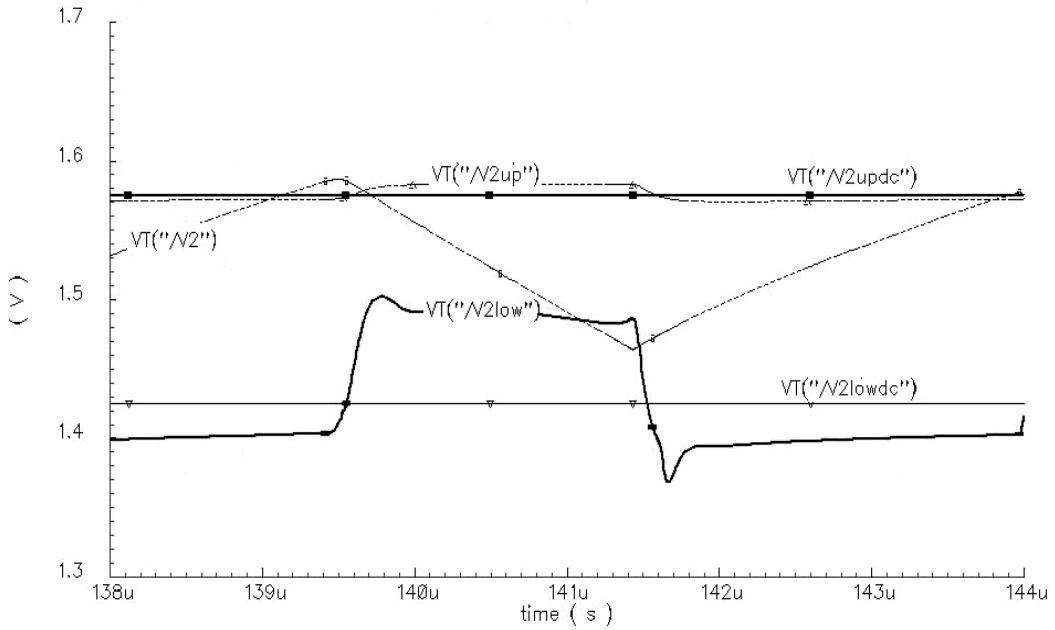


**Fig. 26A. Control of $V_2(t)$ using dynamic thresholds**

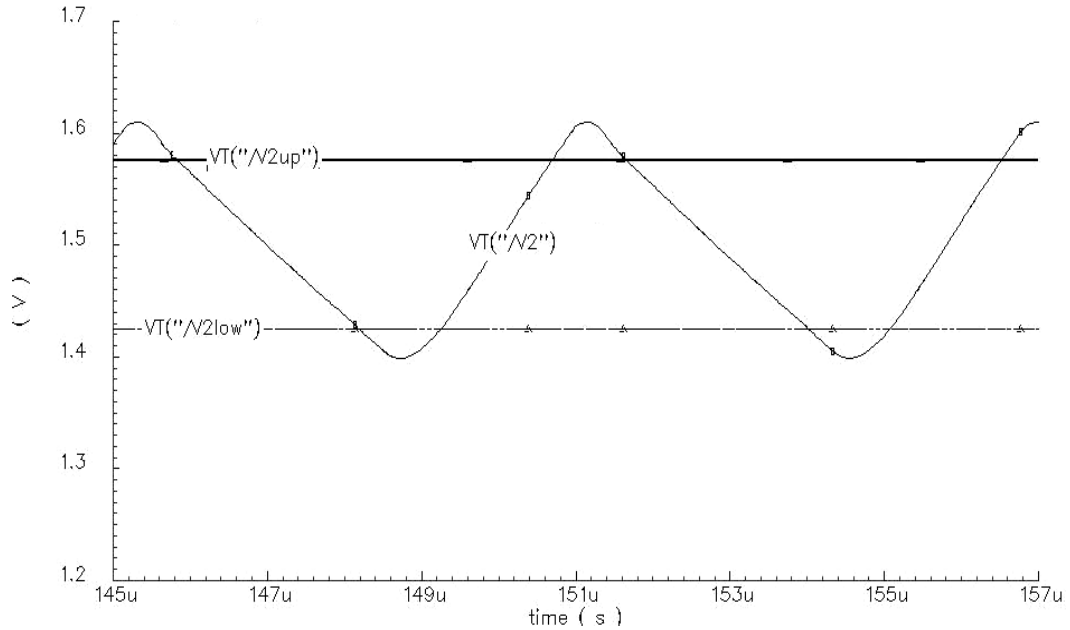


**Fig. 26B. Control of $V_2(t)$ using static thresholds**

The ripple voltages at the outputs are independent of the load value in the when dynamic thresholds are used, since the hysteresis width is controlled adaptively in proportion to the load current. When static levels are used the ripple is not well controlled and is bound to vary with the amount of load. In Fig. 27 it is seen that $V_2(t)$ and $V_2(t)$ have well controlled ripples, with the inductor time multiplexed between the outputs.

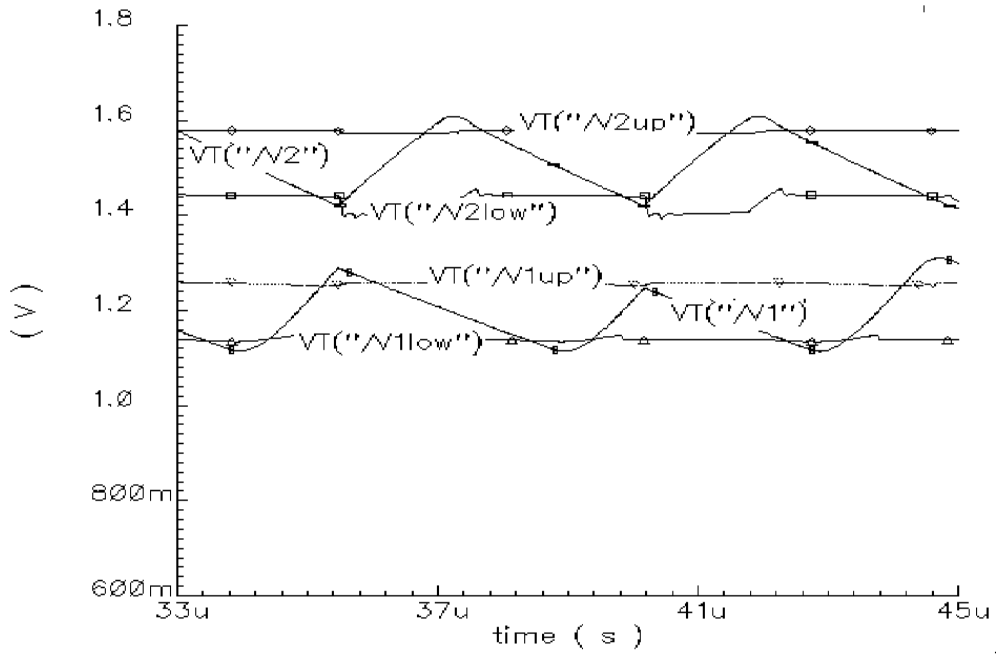


**Fig. 27 Outputs and dynamic thresholds for $I_1 = I_2$ =300 mA**

The switching frequencies of both $S_1$ and $S_2$ increase to almost equal to 250 kHz each. $S_p$ and $S_n$ switch at a frequency of 500 kHz. The pulses given to switches are shown in Fig. 28.

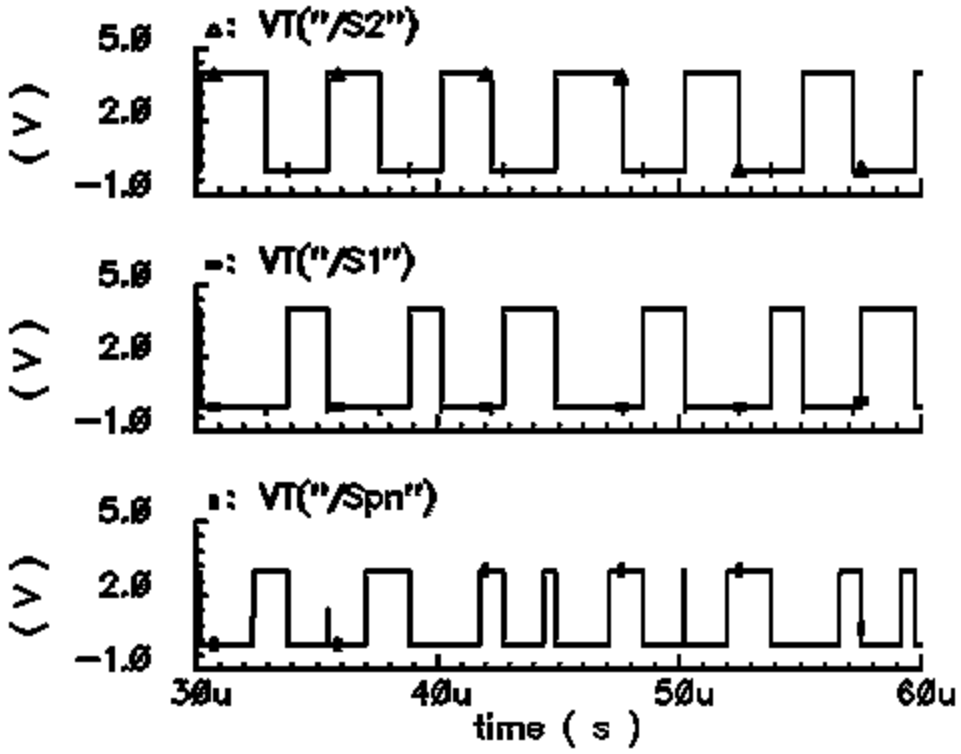


**Fig. 28 Control pulses given to switches $S_p$, $S_n$, $S_1$ and $S_2$**

The efficiency of the SIDO buck converter at rated load is 50%. The reason for the low efficiency is the high values of switch resistances (~ 3Ω total resistance).

**2. Heavy-Light Load Combination**

Simulation results are shown where the current drawn at output $V_1(t)$ is high i.e. 300 mA and the current drawn at output $V_2(t)$ is low i.e. 10 mA. The inductor is hence connected to very different load points; the objective is to maintain the outputs without an unnecessary rise in the voltage at light load or drop in voltage at high load.

When either of the voltages cross the lower dynamic level, the inductor immediately gets connected to the corresponding output. Hence the dynamic thresholds serve to reduce the large dips in the heavy load output while the inductor is connected to the light load output.

In Fig. 29 the inductor is connected to the light load output $V_2(t)$. Hence the voltage $V_1(t)$ drops from 1.17V to 1.12V at which point the inductor hence switches back to $V_1(t)$. Irrespective of the load condition the output voltages are thus maintained within their static levels.

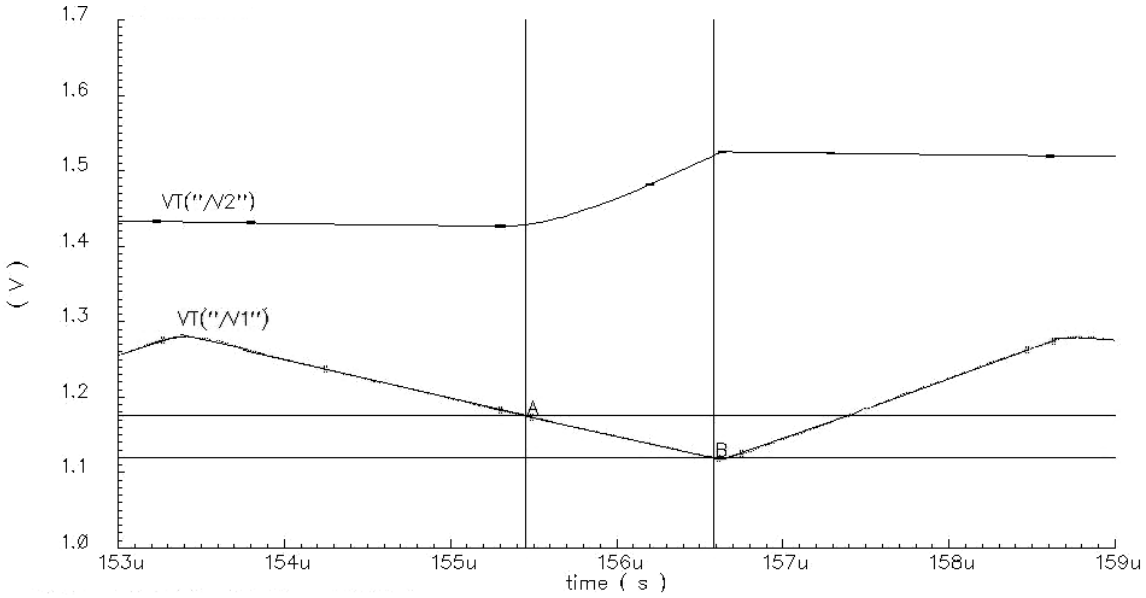


**Fig. 29 Dynamic threshold control**

In Fig. 30 static comparison levels are used. When the inductor is connects to $V_2(t)$ the value of $V_1(t)$ is 1.117V and goes on discharging to 1.107V before L connects to $V_1(t)$ once more. Thus the output discharges to much below the static limit.

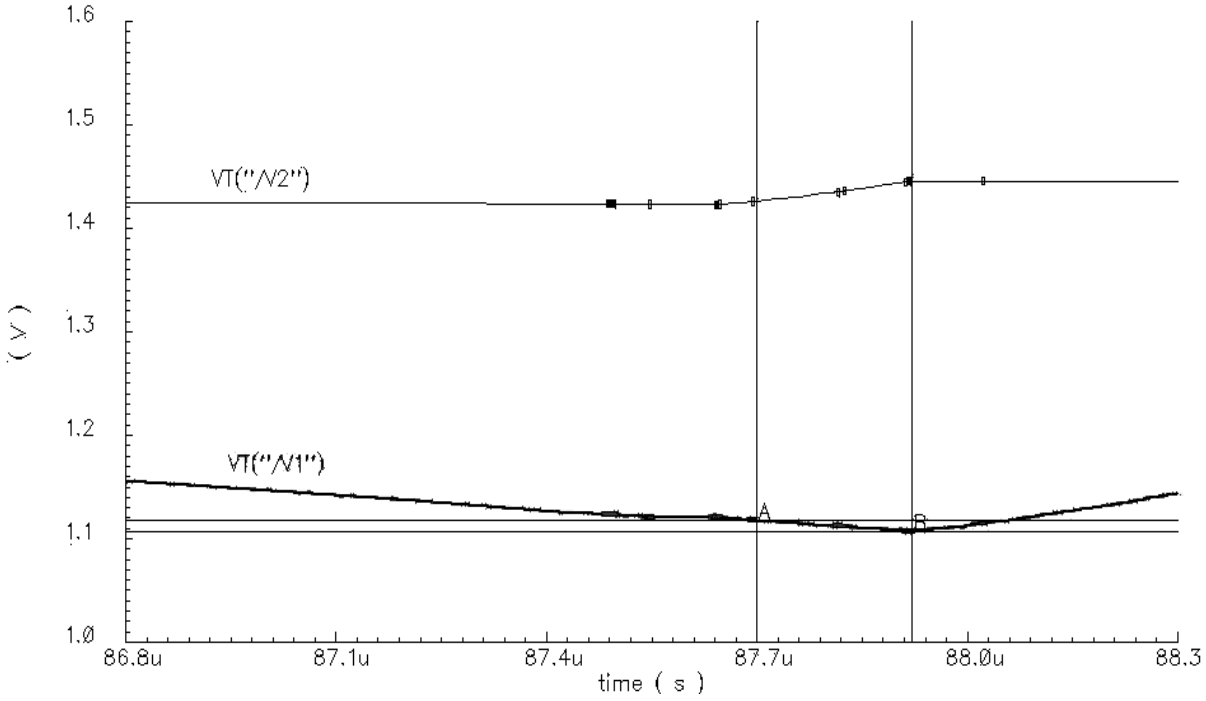


**Fig. 30 Static threshold control**

In the absence of dynamic levels the problem of voltage dips is fixed by either increasing the value of the output capacitance (high form factor) or having narrower static hysteresis bounds which lead to a certain ripple voltage for a certain maximum load value.

On the other hand dynamic bounds have adaptive width variation based on load current, hence the output voltage is controlled to stay above static bounds relatively independent of capacitor value and load current. This is achieved because of the presence of the first derivative term whose swing varies in proportion with the amount of load present. Hence “adaptive control” of the ripple voltage is achieved through the introduction of the dynamic term in hysteresis comparison levels.

In Fig. 31 $V_1(t)$ approaches $V_{1low}(t)$, the inductor is disconnected from $V_2(t)$ before it overshoots $V_{2up}(t)$. Hence the heavy load is duly served. When $V_2(t)$ hits $V_{2low}(t)$ the inductor is

disconnected from the heavier load. This shows that the voltage at the light load output does not drop due to heavy load in the other branch. This indicates very good cross regulatory behavior in the system. The start-up time of the system is 10 µs.

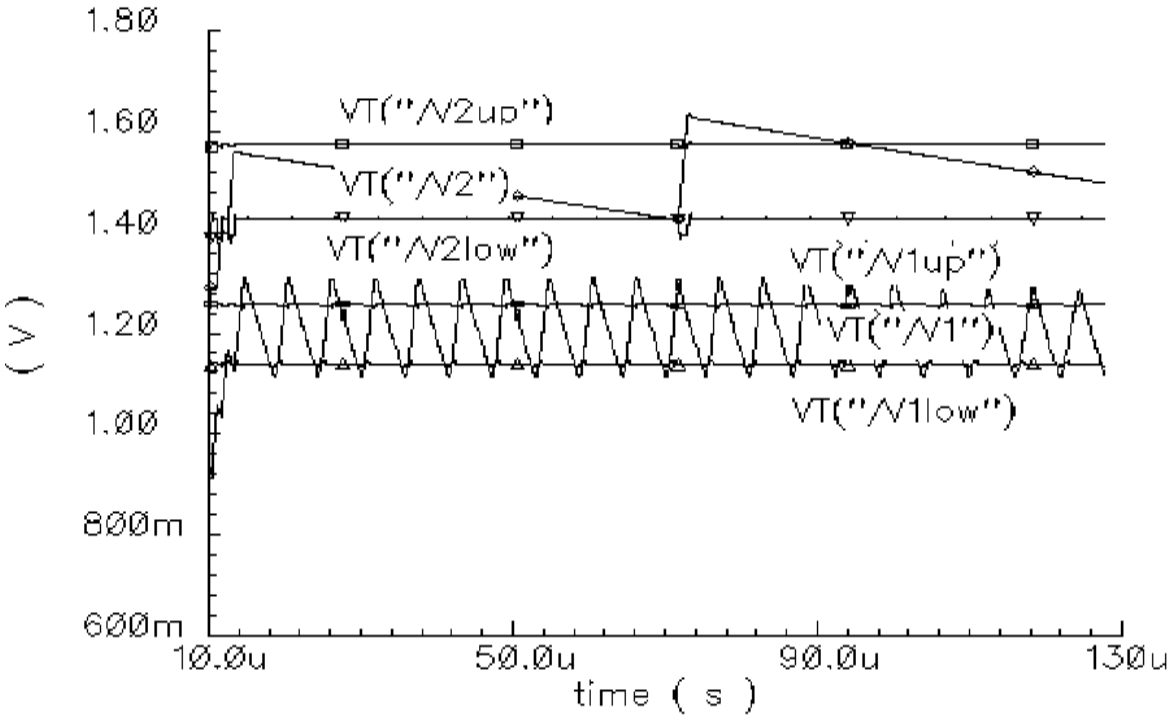


**Fig. 31 Outputs and dynamic thresholds for $I_1$ =300 mA $I_2$ = 10 mA**

In Fig. 32, the switching frequency of $S_1$ is 250 kHz and much greater than that of $S_2$ (10 kHz). The switches $S_p$ and $S_n$ operate at 250 kHz. In the figure, it is seen that when $I_L$ just goes negative the auxiliary switch is activated so that no current is extracted from the output, leading to no power loss. The overall efficiency has been found to be 55%.

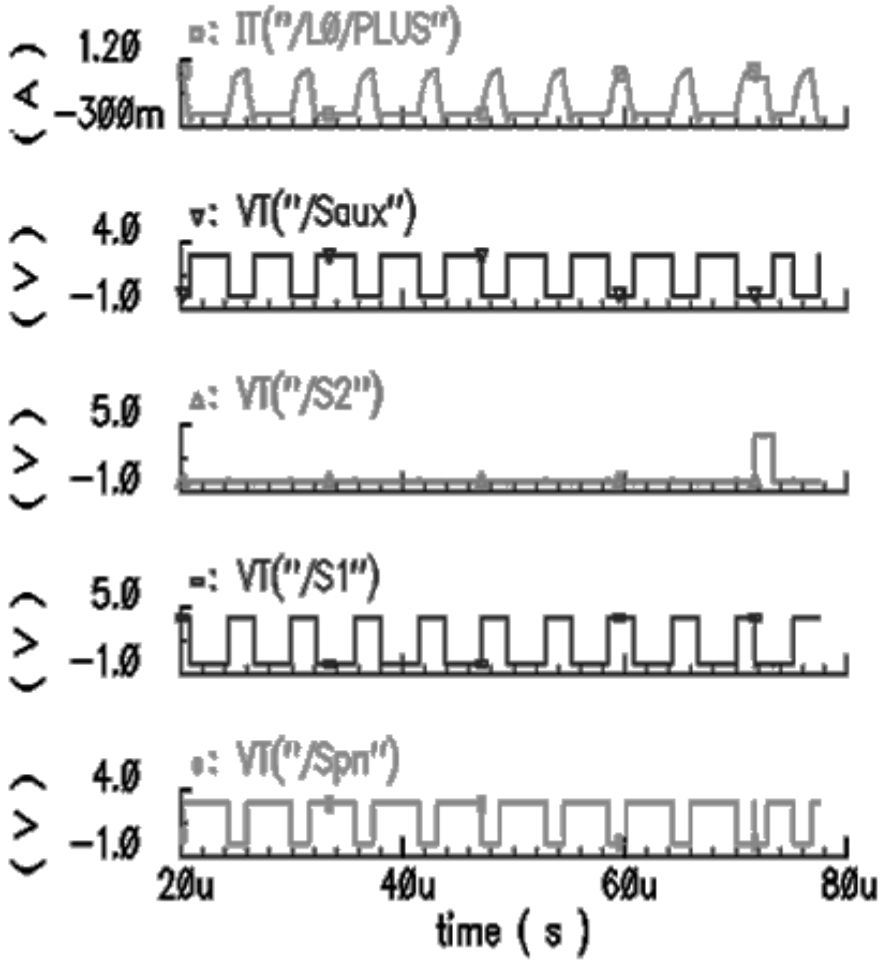


**Fig. 32 Control pulses to switches and inductor current**

### 3. Light-Light Load Combination

In the combination the current drawn at both outputs is very low i.e. around 10 mA. The concern at low loads is the low efficiency due to switching losses and negative current drawn from the output capacitors.

The presence of the shunt switch $S_{aux}$ serves the purpose of ringing suppression and prevents the extraction of negative current from the output capacitor. In Fig. 33 the ringing is exhibited in the output voltages $V_1(t)$ and $V_2(t)$ when the switch $S_{aux}$ is ON.

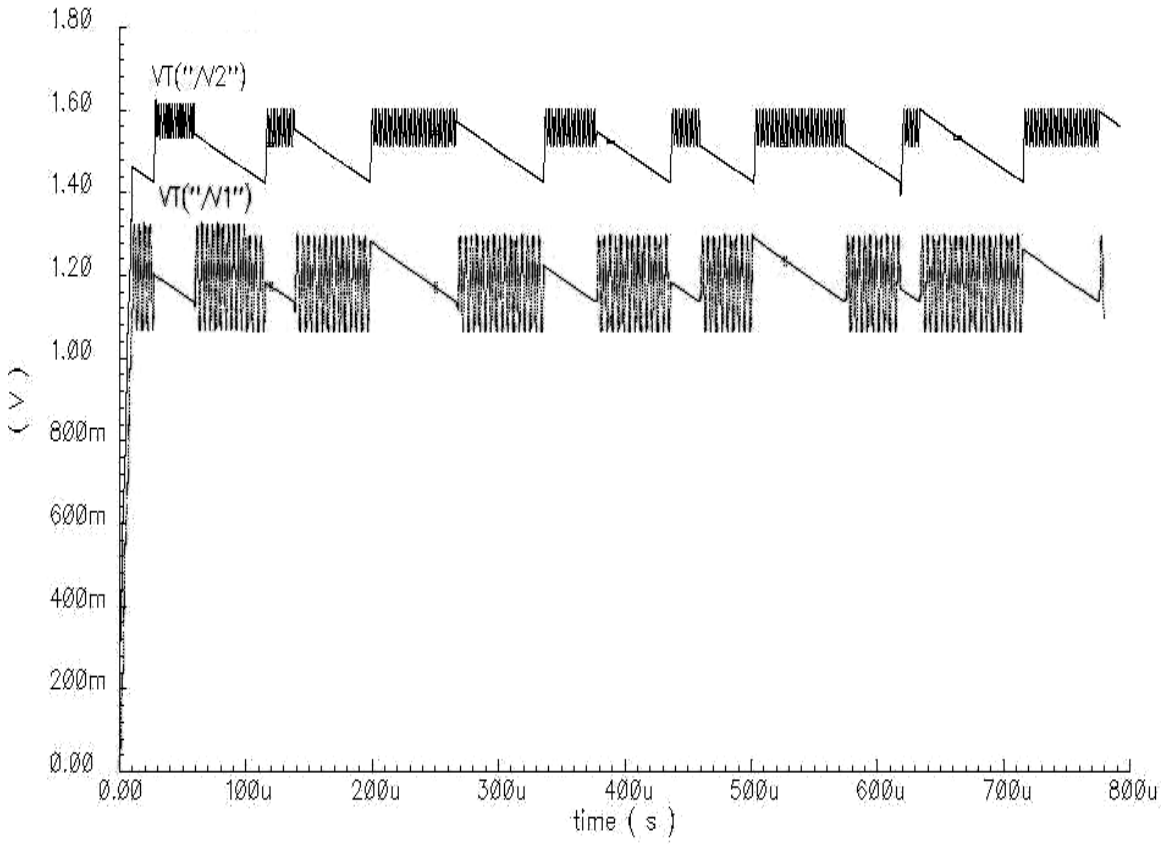


**Fig. 33 Light load outputs without** $S_{aux}$

Negative current $i_L(t)$ is drawn from the output capacitor through the inductor, forming a series tank circuit as shown in Fig. 34.At light load the low damping of the circuit leads to the oscillatory voltage response at the output $V_o$. The overall power efficiency is 20%.

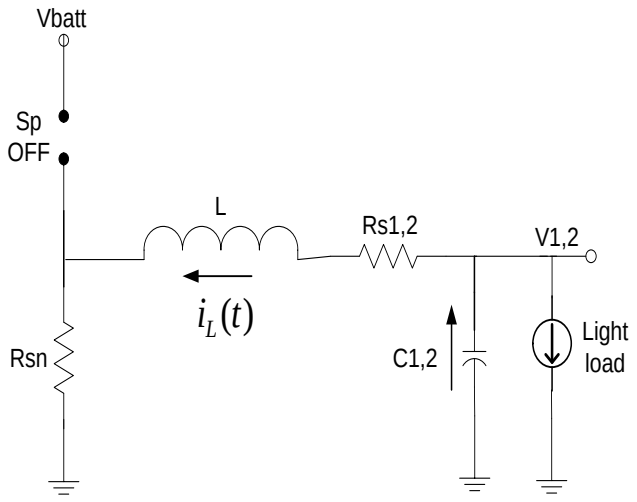


**Fig. 34 Negative current flow without $S_{aux}$**

In obtaining the output voltages depicted in Fig. 35 $S_{aux}$ is activated during the negative excursions of inductor current. Ringing is suppressed and the power efficiency of the system increases to around 55%. Hence there is a 30% increase in efficiency with the employment of the low resistance shunt switch $S_{aux}$. The system start-up time is 10 μs.

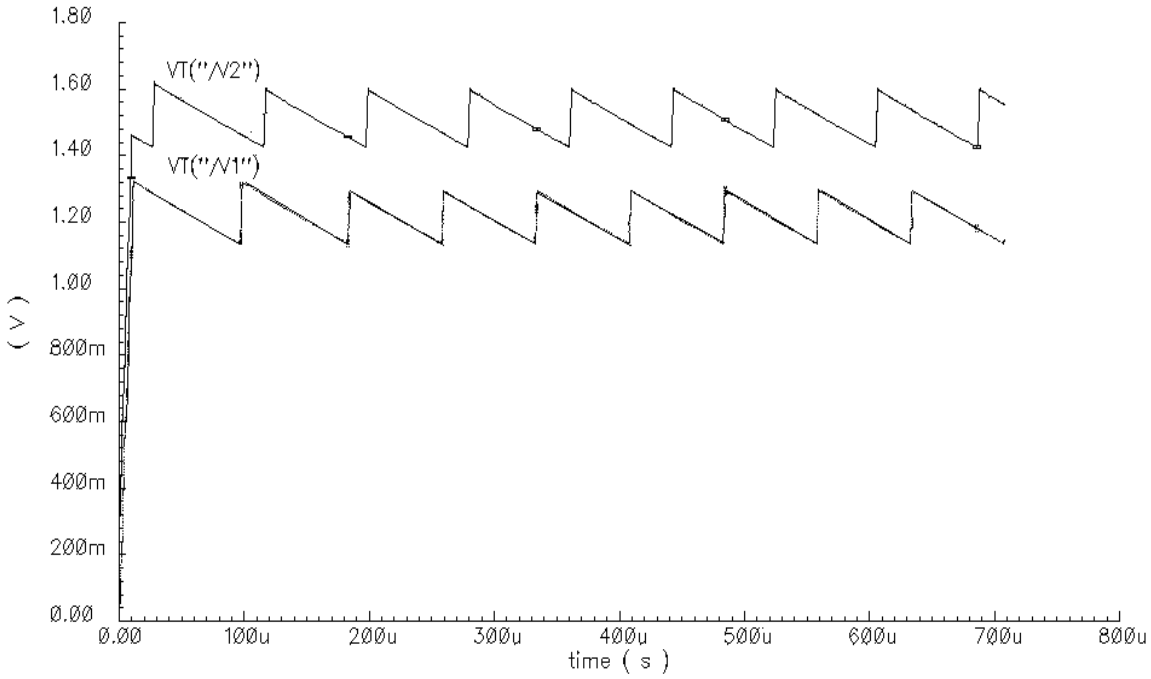


**Fig. 35 Light load outputs with** $S_{aux}$

Fig. 36 shows the inductor is connected to the output that hits its lower limit, and during the rest of the period the converter is in "hold" state. The inductor current reaches zero, hence the turn ON loss of the switches is zero. Also, since the threshold levels at both outputs are far apart at light load, the switching frequency drops, preventing high switching losses that normally occur at low load. Switching frequency of $S_1$ & $S_2$ =20 kHz, $S_p$ & $S_n$ =40 kHz. The power efficiency is 56%

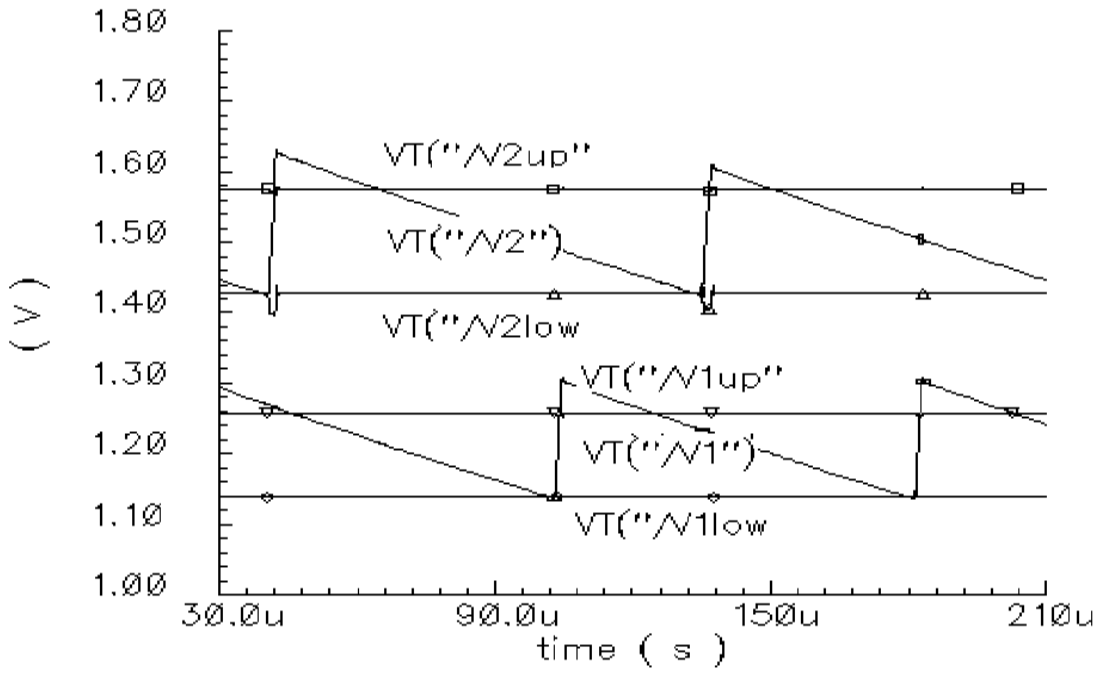


**Fig. 36 Outputs and dynamic thresholds for $I_1 = I_2$ = 10 mA**

Hence from simulations it can be concluded that the SIDO buck converter can be made to have independently varying outputs. Frequency of operation is "adaptive" leading to faster switching during high loads and slower switching during low loads, leading to improved efficiency. Also, the problem of negative inductor current during discontinuous conduction mode is solved, with no ringing transients, due to the presence of the auxiliary switch. Also, the efficiency of the system is almost constant over the individual load ranges. This leads to an almost flat efficiency-load curve as depicted in Fig. 37 that is desirable in many applications in order to optimize the performance of the power supple over a wide range of loads.

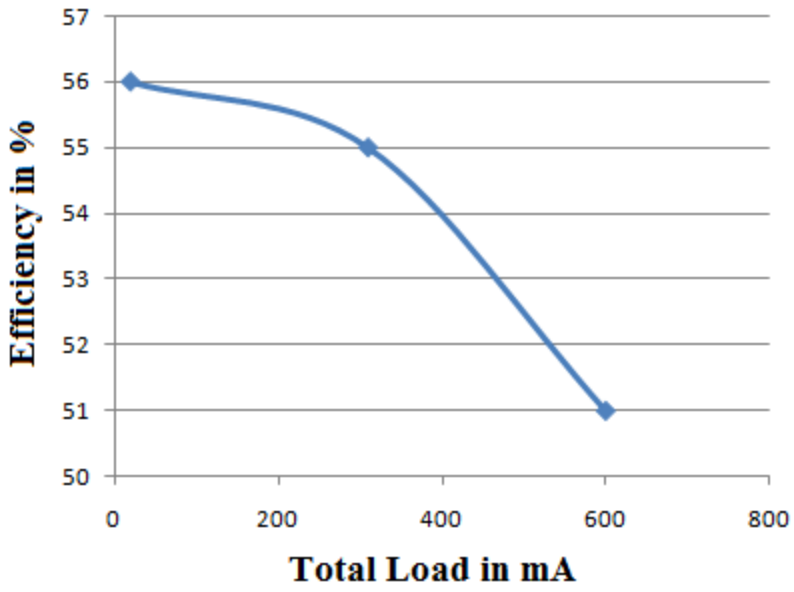


**Fig. 37 Efficiency vs. load curve**

Fig. 38 shows the response of the output voltages $V_1(t)$ and $V_2(t)$ to a step variation of the load current $I_1$. $I_1$ is increased from 10% to 100% of rated current over 1 µs. It is seen that there is no dip in $V_1(t)$ or $V_2(t)$, verifying that this method of control leads to very low cross regulation and excellent load side disturbance rejection.

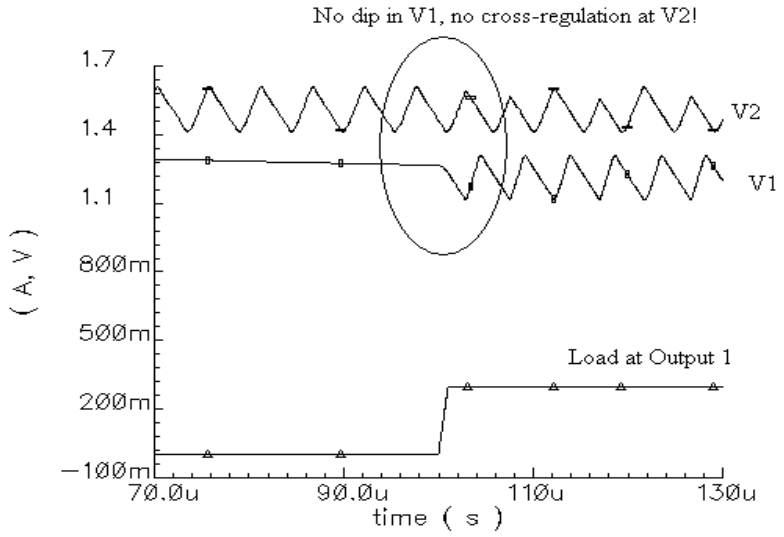


**Fig. 38 Load step response**

Fig. 39 shows the response of output voltages to 500 mV drop in battery voltage over 1 µs time period. The voltages at the outputs do not experience any dips because of the drop in battery voltage. This proves that the control is robust to battery voltage variations.

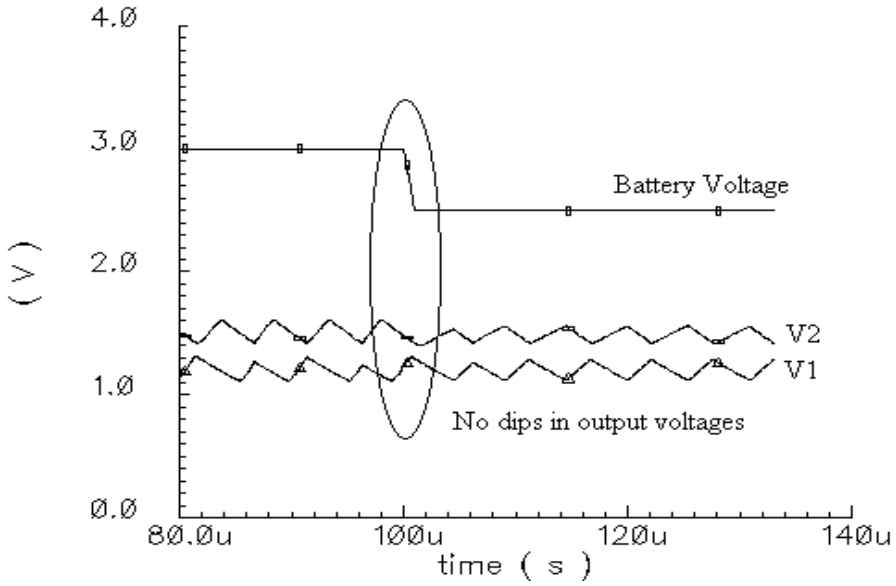


**Fig. 39 Input voltage step response**

### B. Post-layout Transient Simulations

In this section the system level post layout simulation results are presented. In Fig. 40 the layout of the integrated switches, analog blocks (comparators and differentiators), digital circuits and drivers is shown. The area of the layout integrating the controller and power switches is 7.225 $mm^2$. The expected values of the switch resistances of $S_p$ and $S_n$ is 1-2 Ω and for $S_1$ and $S_2$ the values are 0.5-1 Ω. The pads for the outputs and external connections of the inductor are placed close to the switches to minimize impedance associated with long paths. Several pads are used for power and ground due to high currents that flow in these paths.

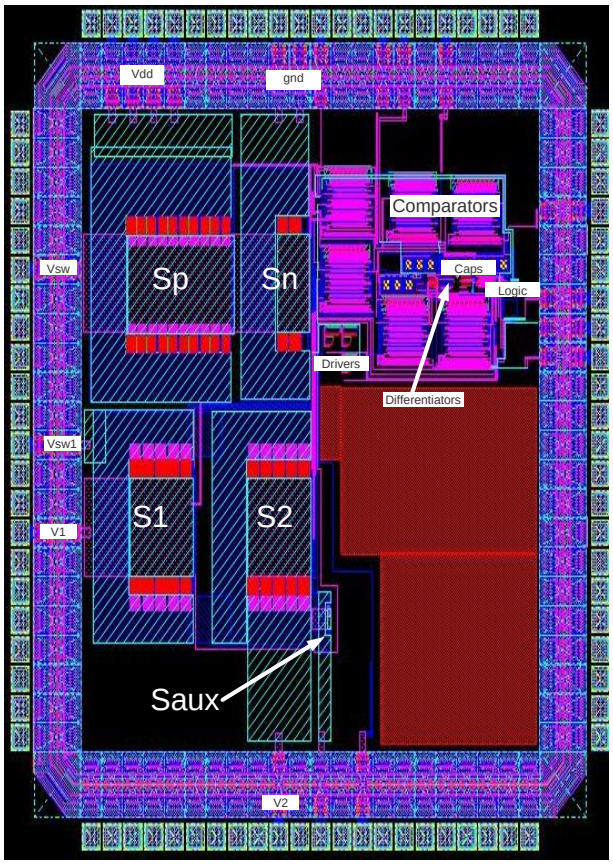


**Fig. 40 Overall chip layout**

Transient post layout simulations are performed with various load combinations.

**1. Heavy-Heavy Load Combination**

The maximum rated current of 300 mA are present in both branches. It is seen in Fig. 41 that convergence of individual outputs to their respective reference values (1.5V and 1.2V) is achieved. The start-up time is 40 µs without overshoot or ringing. Superior transient response is necessary in portable systems where RF type loads have stringent requirements on the accuracy and limits of power supplies. Also the low start-up time is desirable for better system performance in portable electronics. In steady state the ripple is within the 10% specified limit.

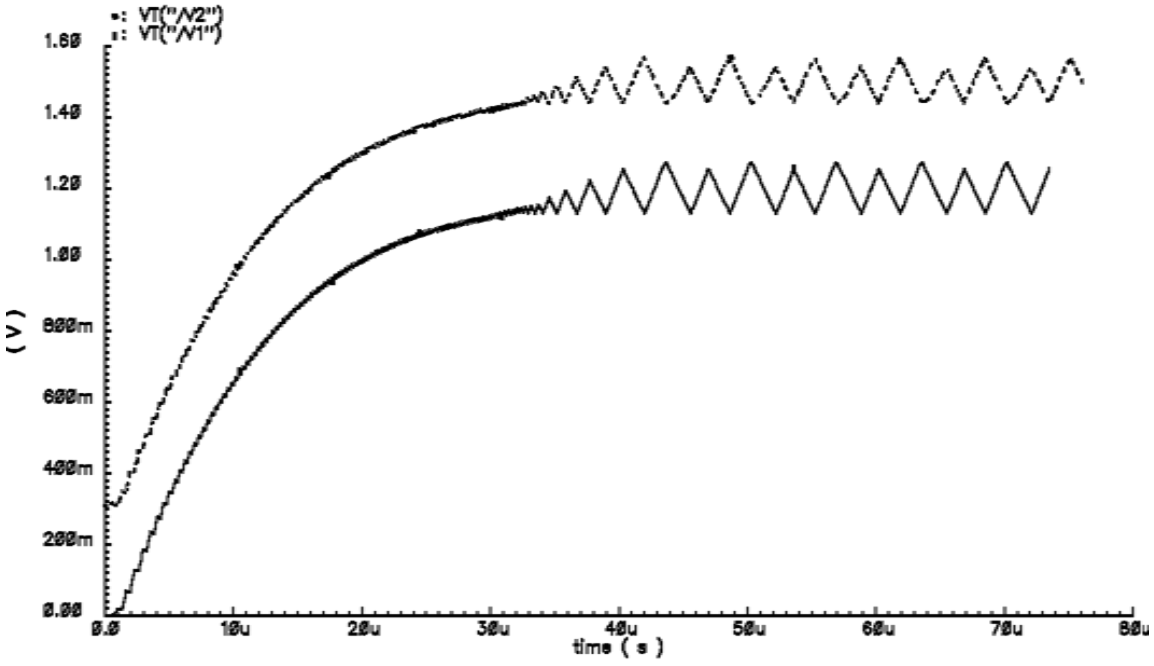


**Fig. 41 Outputs at heavy load**

In Fig. 40 it is evident that during start-up the frequency of switching is very high, leading to rapid transfer of energy to the load. When the voltages get sufficiently charged, the frequency reduces. Hence the variable switching frequency aids in the quick transient response and start-up of the system. The overall switching frequency is around 500 kHz.

**2. Light-Light Load Combination**

A load of 10 mA is drawn from each output. As seen in Fig. 42 the outputs converge at their respective references (1.5V and 1.2V), and stay within the permissible limits of 10%.

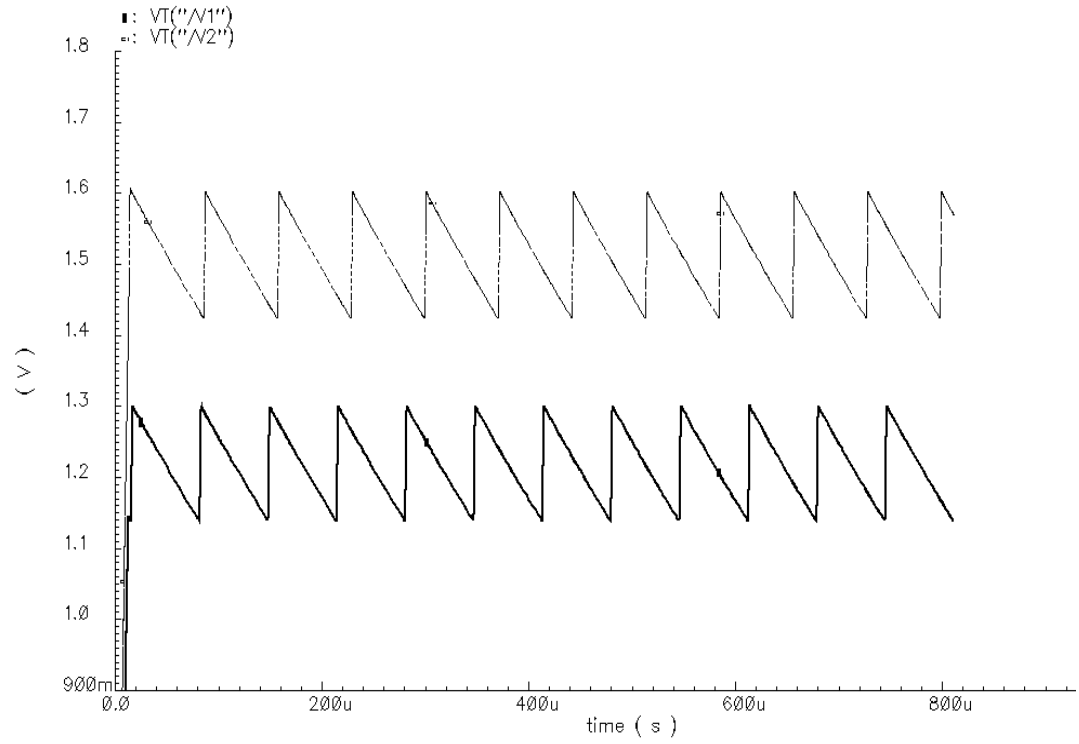


**Fig. 42 Outputs at light load**

It is seen in Fig. 43 that when inductor current $I_L$ goes negative $S_{aux}$ goes high activating the auxiliary switch. During the time delay, the current reaches a peak negative value

of 85 mA, and the time for which negative current lasts is for 600 ns due to the time constant of inductor discharge. The total time period is 40 µs. Hence the average negative current extracted from the load due to comparator and circuit delay << average current supplied to the load, leading to negligible loss in efficiency. Besides switching frequency at light load decreases to about 25 kHz leading to reduced dynamic losses.

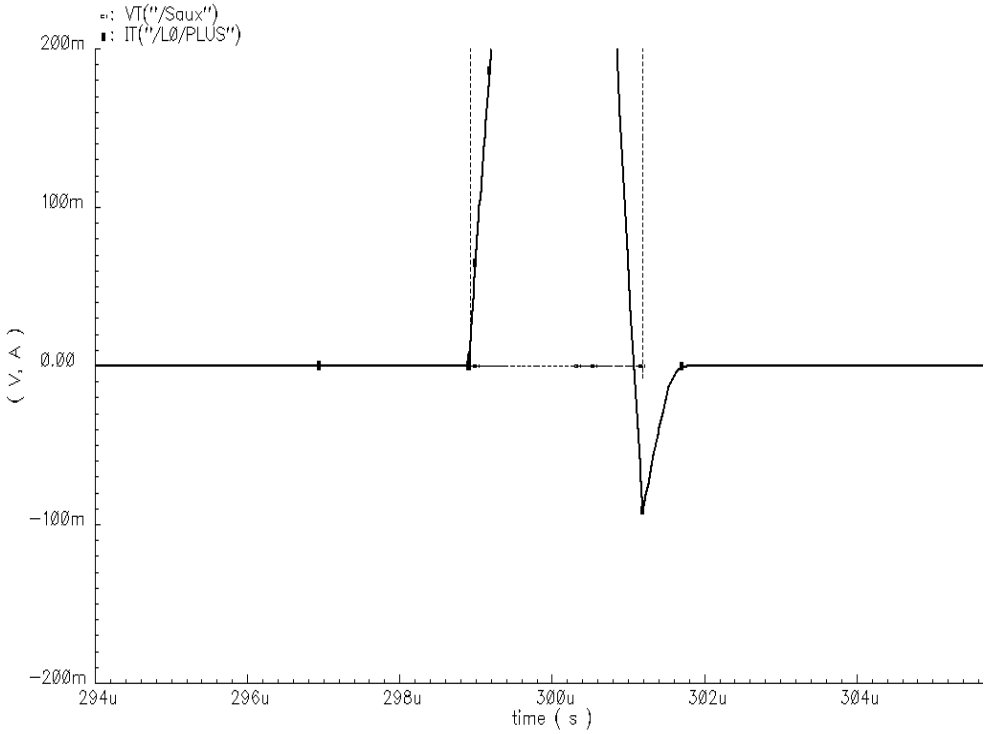


**Fig. 43 Reverse current flow and auxiliary switch control**

The following conclusions may be drawn from the schematic and post-layout transient simulations performed:

i) The outputs $V_1(t)$ and $V_2(t)$ then they can be controlled in a manner that is robust to line and load variations.

ii) The problem of cross-regulation is overcome by this control methodology as the frequency is variable and the time period adjusts in such a way that load demanded at both outputs are supplied over a time period

iii) The voltage ripples of the individual outputs are well controlled relatively independent of the output capacitor and load current values.

iv) The overall efficiency of the system is improved across wide range of loads. In a buck converter, switching losses dominate the system in low load condition, while conduction losses dominate during heavy load condition. In the proposed scheme, the frequency of switching is dependent on the load condition. At heavier load, the inductor current ripple is controlled from peaking by increasing the frequency of operation. Hence at higher load, conduction losses are reduced. At lighter load the frequency of operation is reduced such that the system reaches a standby condition, the only losses of the system being the negligible conduction and switching losses of the power stage and quiescent power consumed by the circuits.

The primary disadvantage of the control method used is that the switching frequency is not fixed. In portable systems, it is desirable to limit the switching frequency to a band that is outside of the audio range (up to 20 kHz), for better audio quality in cellular phones. In this work, the frequency is not controlled hence there is a possibility of switching disturbance occurring in the audio range of frequencies.

# CHAPTER V

# CONCLUSION

The design, schematic and post-layout simulations results of the sliding mode control of a SIDO buck converter have been presented. Two outputs of 1.2V and 1.5 V each are obtained with low cross regulation, good accuracy and 10% ripples limits. A maximum current of totally 600 mA can be supplied by the SIDO buck converter.

Non linear hysteresis control techniques such as sliding mode control applied to the SIDO buck converter leads to superior transient performance and disturbance rejection. Using the dynamic hysteresis control method the flat efficiency-load curve that is an advantage for optimum system performance is achieved. The power efficiency values can be improved using more sophisticated technology and through employment of methods such as dynamic switching where the width and gate swing of power switches vary adaptively with the load demanded from the power supply.

The disadvantage of this method is the variation of frequency with load, and as a solution to this adaptive dynamic levels maybe used i.e. the switching frequency can be controlled to stay within a band of frequencies by tuning the width of the hysteresis loop using an auxiliary feedback loop. Experimental results are expected to demonstrate similar results.

The SIDO buck converter is expected to meet 10% ripple requirements with output capacitors of value 4.7 μF and an inductor of value of 1 μH. Commercially used surface mount type of passive components can be used for low board real-estate and better performance.

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# APPENDIX A

Fig. A-1 shows the SIDO buck converter and the related timing diagram.

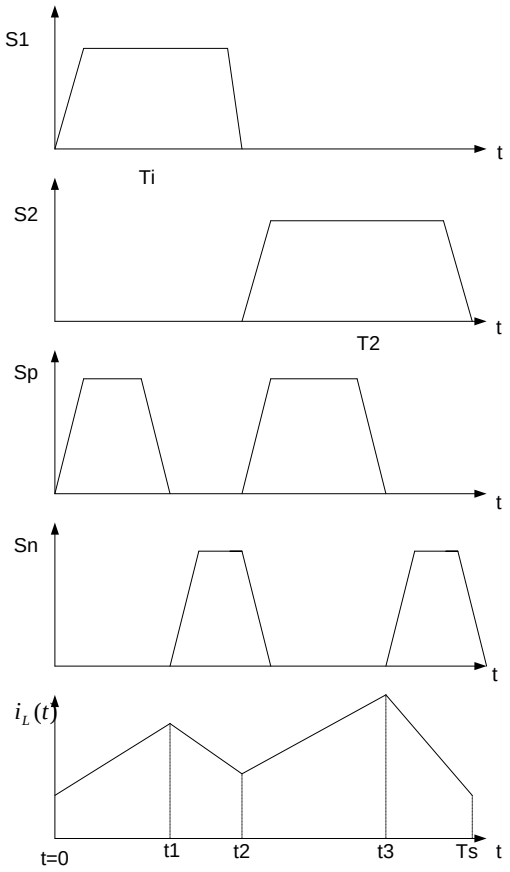


**Fig. A-1 Timing diagram of the SIDO Buck Converter**

$D_1$ is the duty cycle of the sub converter 1 and $D_2$ is the duty cycle of sub converter 2.

$$I_L = I_1 + I_2 \tag{20}$$

The average current carried by the inductor is equal to the sum of the average currents demanded at the output branches.

Also, it is obtained that:

$$\frac{T_1}{T_2} = \frac{I_1}{I_2} \tag{21}$$

The time periods for which the inductor is connected to the outputs are proportional to the average load present from the outputs. The total time period is $T_s$.

The switch resistances are $R_{s1}$, $R_{s2}$, $R_{sp}$ and $R_{sn}$. The average currents flowing through these resistances can be computed over a single time period $T_s$ for finding average conduction losses. The different phases of switching over a single time period are depicted in Fig. A-2 (a), (b),(c),(d).

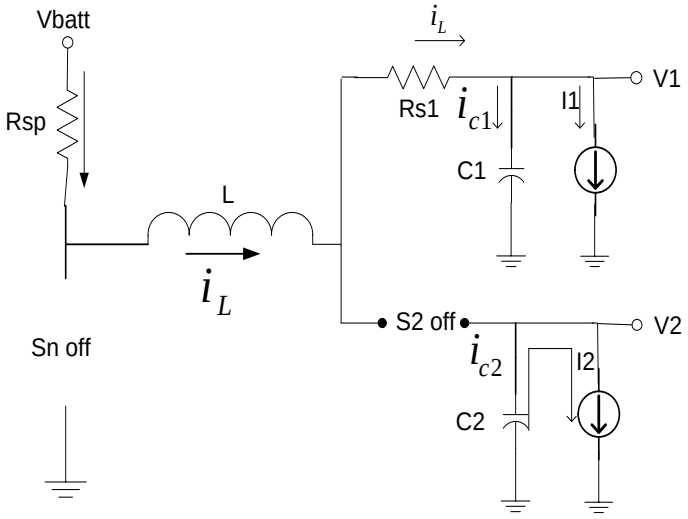


**Fig. A- 2A. Charge Phase** $D_1T_1$

In Fig. A-2(a) $S_1$ and $S_p$ are ON hence L supplies current to $C_1$ and $R_1$. $i_{c2}$ supplies the load $I_2$ and $C_2$ is steadily discharging.

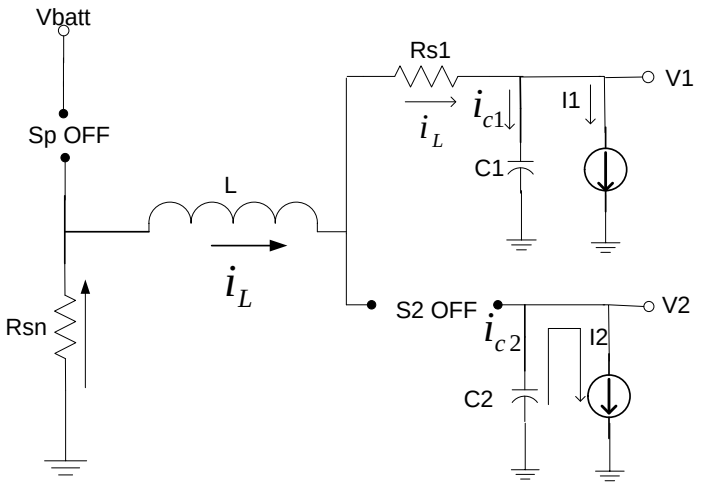


**Fig. A-2B. Discharge phase of** $(1-D_1)T_1$

In Fig. A-2(b) $S_1$ and $S_n$ are ON hence L supplies current to $C_1$ and $R_1$. $i_{c2}$ supplies the load $I_2$ and $C_2$ is steadily discharging.

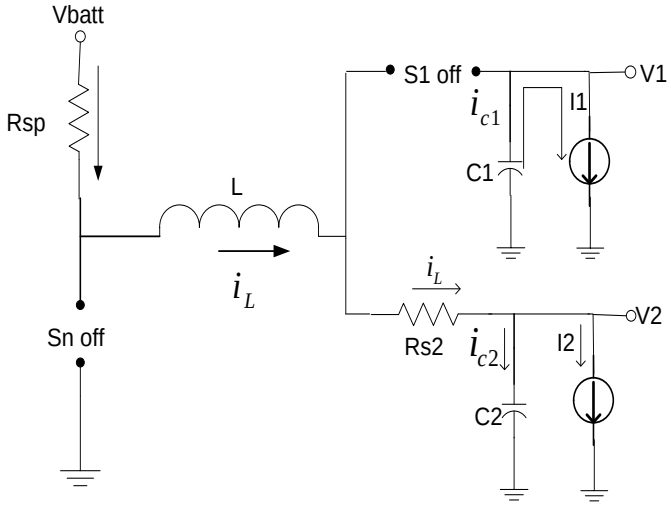


**Fig. A-2C. Charge phase** $D_2T_2$

In Fig. A-2(c) $S_2$ and $S_p$ are ON hence L supplies current to $C_2$ and $R_2$. $i_{c1}$ supplies the load at $I_1$ and $C_1$ is steadily discharging.

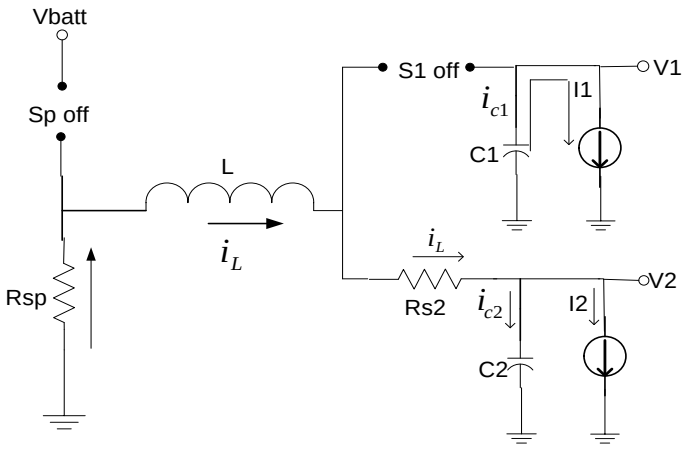


**Fig. A-2D. Discharge phase** $(1-D_2)T_2$

In Fig. A-2(d) $S_2$ and $S_n$ are ON hence L supplies current to $C_2$ and $R_2$. $i_{c1}$ supplies the load $I_1$ and $C_1$ is steadily discharging. This phase lasts for a time period $T_{2on}$.

Average currents over a time period are given by:

Drawn from battery $I_{batt} = \dfrac{I_L(T_{1on}+T_{2on})}{T_s} = \dfrac{(I_1+I_2)(T_{1on}+T_{2on})}{T_s}$

Through $R_{s1} = \dfrac{T_1}{T_s} I_L$

Through $R_{s2} = \dfrac{T_2}{T_s} I_L$

Through $R_{sp} = \dfrac{(D_1T_1 + D_2T_2)}{T_s} I_L$

Through $R_{sn} = \dfrac{(1-D_1)T_1 + (1-D_2)T_2}{T_s} I_L$ (22)

From (22) the total average losses across the switch resistances can be found as $\sum I_{av}^2 R_p$ where $I_{av}$ is the average current flowing through the switch resistance $R_p$. The efficiency can be expressed as:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{V_1 I_1 + V_2 I_2}{(I_1 + I_2)^2 (R_{spn} + R_{s12}) + V_1 I_1 + V_2 I_2} \tag{23}$$

# APPENDIX B

The schematics of the opamps used in the differentiators are shown in Fig. B-1 and Fig. B-2.

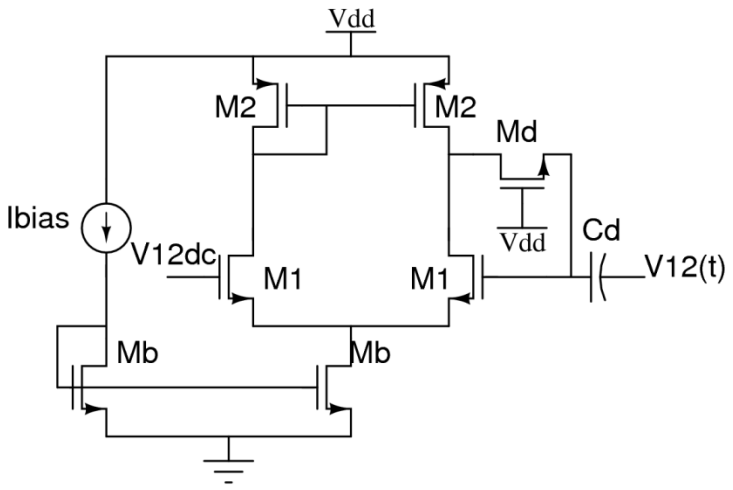


**Fig. B-1 Differentiator for** $V_{2low,up}(t)$

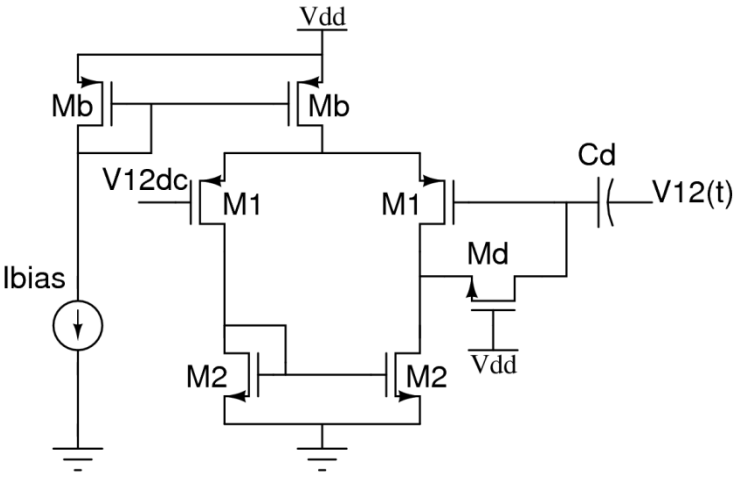


**Fig. B-2 Differentiator for** $V_{1low,up}(t)$

The values of the transistor sizes and bias currents used in the differentiators are shown in Table B-1.

**TABLE B-1**

**DESIGN VALUES OF DIFFERENTIATORS**

| | $V_{1up}(t)$ | $V_{1low}(t)$ | $V_{2up}(t)$ | $V_{2low}(t)$ |
|---|---|---|---|---|
| $I_{bias}$ (µA) | 80 | 40 | 20 | 80 |
| M1 | 4.05u/1.2u | 20u/1.2u | 16.2u/1.2u | 16.2u/1.2u |
| M2 | 40.5u/1.2u | 4.05u/1.2u | 4.05u/1.2u | 8.1u/1.2u |
| Md | 1.5u/1.2u | 16.2u/1.2u | 3u/1.2u | 1.5u/1.2u |

The theoretical (designed) values of $R_d$ and corresponding values of $K_z$ for each of the dynamic threshold levels for $C_d$ = 4 pF are shown in Table B-2. There are slight variations in the resistance values between the four differentiators because the gate source voltage $V_{gs}$ of the triode MOS is different for each of the cases.

**TABLE B-2**

**TIME CONSTANTS OF DIFFERENTIATORS**

| Dynamic Level Generated | $R_d$ (kΩ) | $K_z$ (µs) |
|---|---|---|
| $V_{1low}(t)$ | 8 | 0.03 |
| $V_{1up}(t)$ | 10 | 0.04 |
| $V_{2low}(t)$ | 12 | 0.046 |
| $V_{2up}(t)$ | 15 | 0.06 |

Table B-3 shows the variations of the Gains & GBW's of the differentiators across corners and in typical process parameter values. The simulations were run at temperature 80 deg. C. The DC value at the input $V_{dc}$ is used to indicate which differentiator is being referred to.

**TABLE B-3**

**PERFORMANCE OF DIFFERENTIATORS ACROSS PROCESS CORNERS**

| Corner | GBW (in MHz) | | | | Gain | | | | $R_d$ (in kΩ) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{dc}$ (V) | 1.14 | 1.26 | 1.425 | 1.575 | 1.14 | 1.26 | 1.425 | 1.575 | 1.14 | 1.26 | 1.425 | 1.575 |
| TT | 314 | 538 | 1003 | 572 | 70 | 65 | 82 | 108 | 29 | 41 | 100 | 21 |
| FS | 311 | 454 | 924 | 443 | 70 | 67 | 77 | 103 | 28 | 37 | 82 | 14 |
| SF | 327 | 564 | 938 | 528 | 71 | 66 | 86 | 110 | 32 | 47 | 155 | 45 |
| SS | 320 | 496 | 787 | 567 | 71 | 66 | 82 | 109 | 32 | 46 | 147 | 25 |
| FF | 334 | 516 | 1064 | 428 | 69 | 64.8 | 82 | 107 | 27 | 36 | 75 | 21 |

# APPENDIX C

A high gain open loop amplifier is used as a comparator. The comparator circuit is shown in Fig. C-1.

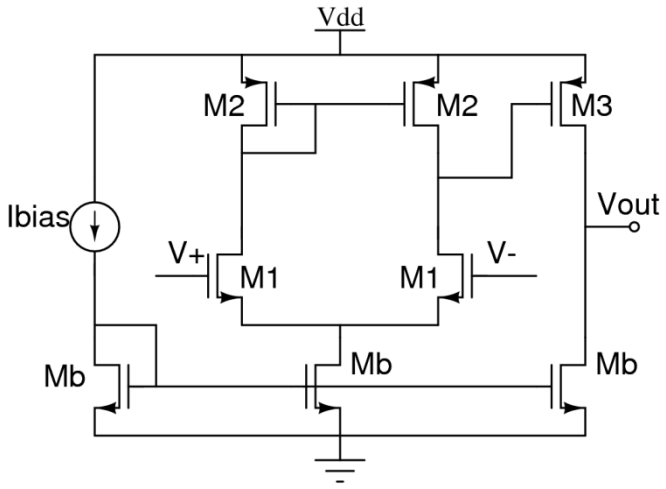


**Fig. C-1 Transistor level continuous time comparator**

Bias current of the comparator is designed accordingly for the desired slew rate. The design values of the comparator are shown in Table C-1.

**TABLE C-1**

**DESIGN VALUES OF COMPARATORS**

| Transistor | Size |
|---|---|
| M1 | 300u/1.2u |
| M2 | 36u/1.2u |
| M3 | 72u/1.2u |
| Mb | 40u/1.2u |
| $I_{bias}$ | 75 µA |

In Table C-2 the positive and negative slew rate and gain values are shown at different corners at 80 deg C.

**TABLE C-2**

**PERFORMANCE OF COMPARATORS ACROSS PROCESS CORNERS**

| Corner | Positive Slew Rate (in V/µs) | Negative Slew Rate (in V/µs) | Gain (in dB) |
|---|---|---|---|
| TT | 105 | 105 | 77 |
| FS | 106 | 104 | 76 |
| SF | 102 | 118 | 77 |
| SS | 103 | 110 | 76 |
| FF | 107 | 103 | 77 |

# APPENDIX D

The sizes and ON state resistances of the power switches of the SIDO buck converter are shown in Table D-1.

**TABLE D-1**

**DESIGN VALUES OF POWER SWITCHES**

| Switch | Size | $R_{ds}$ (Ω) |
|---|---|---|
| $S_p$ | 15m/0.6u | 0.38 |
| $S_n$ | 5m/0.6u | 0.41 |
| $S_1$ | 10m/0.6u | 0.45 |
| $S_2$ | 10m/0.6u | 0.675 |
| $S_{aux}$ | 200u/0.5u | 10 |

Table D-2 gives the values of the sizes and variations of on state resistance $R_{ds}$ and parasitic gate source capacitance $C_{gs}$ with process at 80C.

**TABLE D-2**

**PARASITICS OF POWER SWITCHES ACROSS PROCESS CORNERS**

| Switch | $R_{ds}$ (in ohm) | | | | | $C_{gs}$ (in pF) | | | | | Size |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | TT | FF | FS | SF | SS | TT | FF | FS | SF | SS | |
| $S_p$ | 1.2 | 1.16 | 1.15 | 1.15 | 1.15 | 15.3 | 15.8 | 15.21 | 15.7 | 15.18 | 15m/0.6u |
| $S_n$ | 1.15 | 1.13 | 1.17 | 1.17 | 1.17 | 4.92 | 4.92 | 4.91 | 4.91 | 4.91 | 5m/0.6u |
| $S_1$ | 67 m | 76 m | 68m | 68m | 68m | 9.69 | 9.79 | 9.84 | 9.85 | 9.85 | 10m/0.6u |
| $S_2$ | 78m | 65m | 81m | 81m | 81m | 9.86 | 9.82 | 8.76 | 9.81 | 9.81 | 10m/0.6u |
| $S_{aux}$ | 54 | 53 | 55 | 56 | 55 | 0.12 | 0.12 | 0.12 | 0.14 | 0.12 | 200u/0.5u |

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