BASEBAND ANALOG CIRCUITS IN DEEP-SUBMICRON CMOS TECHNOLOGIES TARGETED FOR MOBILE MULTIMEDIA

A Dissertation

by

VIJAYAKUMAR DHANASEKARAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2008

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Baseband Analog Circuits in Deep-Submicron CMOS Technologies Targeted for Mobile Multimedia. (August 2008)

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Co-Chairs of Advisory Committee: Dr. Edgar Sanchez-Sinencio
Dr. Jose Silva-Martinez

Three main analog circuit building blocks that are important for a mixed-signal system are investigated in this work. New building blocks with emphasis on power efficiency and compatibility with deep-submicron technology are proposed and experimental results from prototype integrated circuits are presented.

Firstly, a 1.1GHz, 5th order, active-LC, Butterworth wideband equalizer that controls inter-symbol interference and provides anti-alias filtering for the subsequent analog to digital converter is presented. The equalizer design is based on a new series LC resonator biquad whose power efficiency is analytically shown to be better than a conventional Gm-C biquad. A prototype equalizer is fabricated in a standard 0.18μm CMOS technology. It is experimentally verified to achieve an equalization gain programmable over a 0-23dB range, 47dB SNR and -48dB IM3 while consuming 72mW of power. This corresponds to more than 7 times improvement in power efficiency over conventional Gm-C equalizers.

Secondly, a load capacitance aware compensation for 3-stage amplifiers is presented. A class-AB 16Ω headphone driver designed using this scheme in 130nm

technology is experimentally shown to handle 1pF to 22nF capacitive load while consuming as low as 1.2mW of quiescent power. It can deliver a maximum RMS power of 20mW to the load with -84.8dB THD and 92dB peak SNR, and it occupies a small area of 0.1mm^2. The power consumption is reduced by about 10 times compared to drivers that can support such a wide range of capacitive loads.

Thirdly, a novel approach to design of ADC in deep-submicron technology is described. The presented technique enables the usage of time-to-digital converter (TDC) in a delta-sigma modulator in a manner that takes advantage of its high timing precision while noise-shaping the error due to its limited time resolution. A prototype ADC designed based on this deep-submicron technology friendly architecture was fabricated in a 65nm digital CMOS technology. The ADC is experimentally shown to achieve 68dB dynamic range in 20MHz signal bandwidth while consuming 10.5mW of power. It is projected to reduce power and improve speed with technology scaling.

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CHAPTER I

INTRODUCTION

1.1 Motivation and Goals

Internet and computer technologies have revolutionized communication and entertainment in recent times. These technologies are expected to be available to a large population when low cost and long battery life are achieved by the ultra-mobile, wireless internet enabled multimedia devices [1]. The microprocessors that serve as the backbone of these ultra-mobile multimedia devices have constantly reduced cost and power consumption and improved performance due to technology scaling and innovative microprocessor architectures. Since these devices are targeted for communication over internet, they should also support low cost, low power data communication and analog interface circuit blocks. Since the device is targeted for a large user base it is preferable to have it flexible. While software can be easily made to adjust according to user preferences, there are several difficulties in making power-efficient circuit blocks that can work across a wide range of usage scenarios. These requirements open up opportunities for research in development of new circuit architectures that achieve high speed with low power while maintaining low cost through integration in digital CMOS technology along with the microprocessor.

This dissertation follows the style of *IEEE Journal of Solid-State Circuits*.

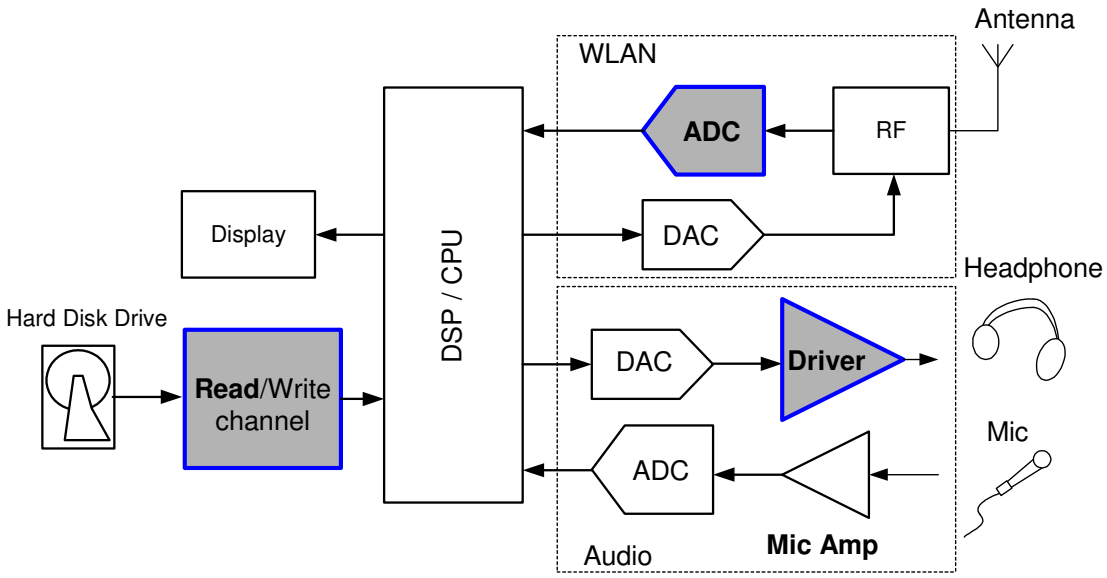


Fig. 1.1 Block diagram of a typical mobile multimedia device.

A block diagram of a typical mobile multimedia system with emphasis on mixed-signal circuit blocks is shown in Fig.1.1. Some of the circuit blocks take up a significant fraction of the overall power consumption of the system and poses serious design challenges in deep submicron technology. The focus of this work is to develop low power architectures for challenging circuit blocks like read-channel filters, analog-to-digital converter (ADC) and versatile audio interface circuits in deep sub-micron digital CMOS technologies. Specifically, new architectures for the following circuit blocks that are compatible with digital CMOS technology were investigated and efficient solutions were proposed.

a) A 1.1GHz equalizing filter based on a new active-LC topology [2].

b) A low-power headphone driver based on a new compensation scheme that can handle a wide range of load conditions [3].

c) A novel ADC architecture suitable for integration in nanometric digital technologies [4].

1.2 Organization

The design and implementation of the novel circuits blocks mentioned in section 1.1 are explained in a detailed manner in the following chapters. A 1.1GHz 5^{th} order active-LC Butterworth type equalizing filter is presented in Chapter II. A series LC resonator based biquad is proposed and its frequency response, noise performance, power efficiency, linearity and area requirements are analyzed in detail. Transistor level implementation of the 5^{th} order equalizer transfer function based on the proposed series resonator biquad is described in detail. Experimental results from the prototype built in 0.18μm CMOS technology are discussed and comparison with benchmark Gm-C equalizers is presented.

Chapter III describes a load capacitance aware compensation for 3-stage amplifiers. The behavior of the existing compensation schemes under large load variation is analyzed. The damping factor variation across load capacitance is found intuitively and a solution to maintain the damping factor roughly independent of the load capacitance is proposed. Implementation of a class-AB driver amplifier based on the proposed 3-stage compensation scheme is presented. Experimental results from the prototype fabricated in 130nm technology are discussed. The chapter concludes with a performance comparison with state-of-the-art headphone driver amplifiers.

A continuous time delta-sigma analog to digital converter (ADC) based on a time domain quantizer and feedback element is described in Chapter IV. The benefit of processing signal in time domain is briefly discussed and a technique that enables the time domain quantizer by means of a pulse width modulation (PWM) generator and a time to digital converter (TDC) is presented. The realization of the proposed ADC architecture using various circuit techniques is described in detail. The quantization noise of the time domain quantizer, the impulse response of the PWM generator and the TDC, the excess loop delay, the effect of clock jitter and the overall noise transfer function are analyzed. Design of a 20MHz signal bandwidth 10-bit ADC based on the proposed architecture is presented. The simulation and experimental results from the prototype built using a 65nm digital CMOS technology are also discussed.

In Chapter V, conclusions are drawn and a possible area for future work related to the presented architectures is identified.

CHAPTER II

A 1.1GHz 5th ORDER ACTIVE-LC BUTTERWORTH TYPE EQUALIZING FILTER

2.1 Introduction

On-chip inductors are routinely used for narrowband RF circuits. However, their use in broadband filtering has been limited. Emerging multi-Gbps data communication systems require wideband filtering and equalization with bandwidth in GHz range. In such systems, high equalization gain is incorporated to control Inter-Symbol-Interference (ISI) and maximize data rate for a given channel bandwidth. Realization of this high gain further imposes stringent noise and power requirements. High power efficiency and smaller size at GHz range make LC resonator based biquads more attractive and are thus considered in this work.

2.1.1 Previous Equalizer Solutions

A survey of previous equalizer solutions is presented in this section. The drawbacks associated with previous architectures when used for boost gain around 24dB and a large bandwidth in the range of several hundreds of MHz is examined.

A single terminated ladder based boost filter is reported in [5] for DVD applications. Its fifth order representation is shown in Fig. 2.1. The normalized transfer function H(s) is

$$H(s) = \frac{K_2(s^2 - 1) + K_1 - 1}{D(s)} = \frac{K_2 s^2 - 1 + K_1 - K_2}{D(s)} \qquad (2.1)$$

where K_1 and K_2 are the first and second feedforward path gains respectively. The intended numerator is of the form: $K_2 s^2 - 1$. The input is directly gained and injected into the third integrating node to create the desired $K_2 s^2$ term in numerator of (2.1). However K_2 path also introduces a low pass feed-through term $-K_2$ which needs to be cancelled through the additional feedforward path consisting of K_1 ($K_1 = K_2$). Creating large gains at frequencies much lower than the filter's cut-off frequency and then canceling this undesired component (using an additional K_1 path) results in loss of power efficiency. The second drawback of this structure is due to realizing entire boost gain in a single gain stage constituting of K_2. This implies that for 24dB boost gain, the transconductance of the boost OTA needs to be 16 times of that of main path OTA that injects current in to the same node.

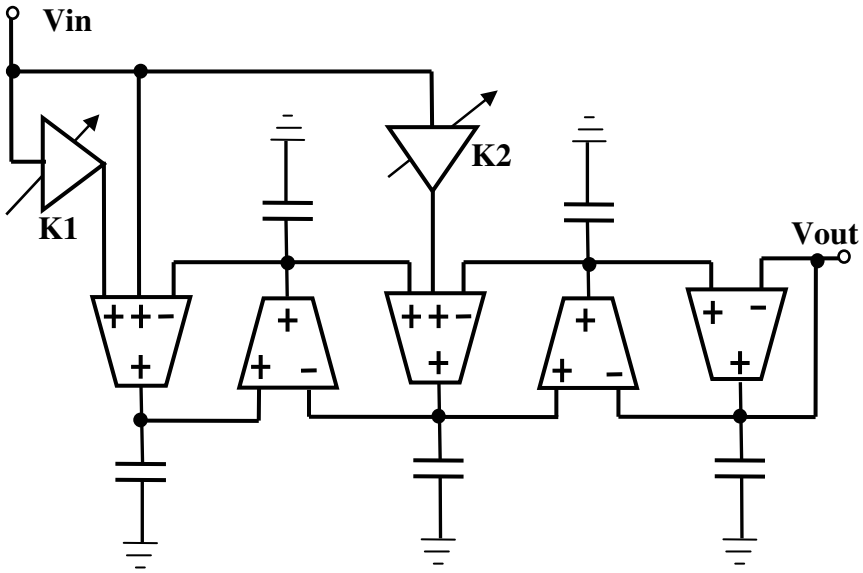


Fig. 2.1 Boost architecture based on single terminated ladder reported in [5].

A differentiator is used in [6] to inject differentiated input signal into the low pass node of the biquad to generate two real zeros. While there is no injection of large low frequency signal currents, keeping the differentiator parasitic poles far away from significantly increases the power consumption [7]. Also, the entire boost gain is realized in a single stage using two zeros created by the differentiator, increasing power requirement. The topology employed in [7] makes use of the differentiator pole as a part of a third order cell and two such cells are used to realize the complete transfer function. However, this scheme introduces one real pole for each zero realized by the differentiator, limiting the types of filter responses that may be realized.

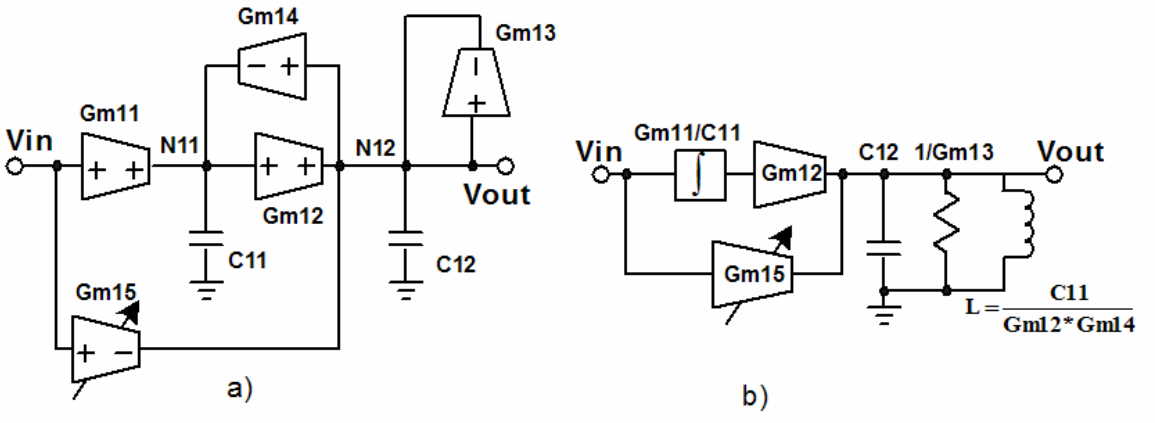


Fig. 2.2 (a) Biquad section of the boost filter reported in [8]. (b) Equivalent circuit.

A cascade structure reported in [8] splits the boost gain between two biquads, realizing a zero each. Fig. 2.2 shows the biquad section of this architecture with a single

zero implemented and its equivalent circuit. Boost OTA (Gm15) injects unfiltered signal current from the input of the biquad into the output node N12. Low frequency component of this injected current is absorbed almost entirely by the emulated inductor (Gm12, Gm14, C11 gyrator). This superfluous low frequency current has an indirect impact on power efficiency. The current equation for node N12 at low frequency or DC, under the simplifying assumption that node N11 is lossless, is

$$Gm15*Vin = Gm12*V_{N11} \quad @ \text{ low frequencies} \tag{2.2}$$

Thus, to maintain voltage swing similar to Vin at node N11, the transconductor Gm12 has to be as large as Gm15. Notice that for 24dB boost, Gm15 is about four times as large as the input OTA and there are two such biquadratic blocks in the entire filter. Further, parasitic capacitance at node N12 become prohibitively large as it is driven by two large OTAs (Gm15 and Gm12). Thus, this scaling up of transconductors adversely affects the power efficiency of this architecture especially when used for wideband filters.

One of the efficient schemes for realizing equalization gain using Gm-C filters has been proposed in [9]. This scheme splits the boost gain between two biquad stages while solving the power disadvantage posed by other cascade architectures. The cascaded representation of the transfer function is given by:

$$H_{boost}(s) = \frac{\omega_o s\sqrt{K} + \omega_o^2}{s^2 + \frac{\omega_o}{Q1}s + \omega_o^2} * \frac{\omega_o s\sqrt{K} - \omega_o^2}{s^2 + \frac{\omega_o}{Q2}s + \omega_o^2} * \frac{\omega_o}{s + \omega_o} \tag{2.3}$$

Here, Q1 and Q2 refer to the quality factor of biquad 1 and 2 and their values are 0.618 and 1.618 respectively. K determines the placement of zeros and its value ranges from 0

to 16 for 0 to 24dB high frequency boost. One way to implement the zeros is to add (subtract) lowpass and bandpass voltage signals. This is done in [8] by injecting amplified current proportional to the unfiltered input voltage into the bandpass impedance node (with parallel resonator of a resistor, capacitor and emulated inductor as in Fig. 3(b)). Alternately, if bandpass current is added (subtracted) from lowpass current, zeros can be directly constructed without creating the superfluous low frequency current. Hence, to achieve good power efficiency, the two real axis zeros are realized by combining bandpass and lowpass signals that are inherently available in Gm-C biquads (conceptual diagram shown in Fig. 2.3). OTA-C realization of such equalizer section is shown in Fig. 2.4.

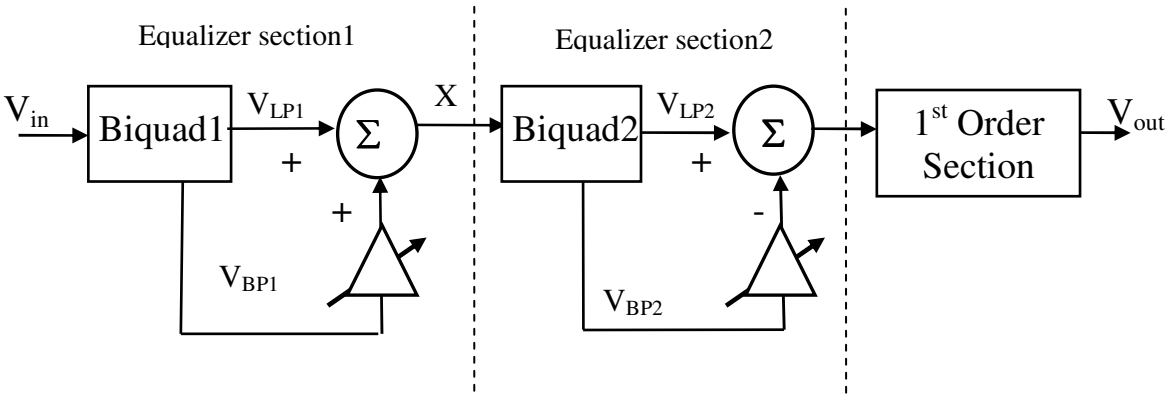


Fig. 2.3 Scheme used in [9] to realize equalization gain ($D_5(S)$ represents 5^{th} order Butterworth poles).

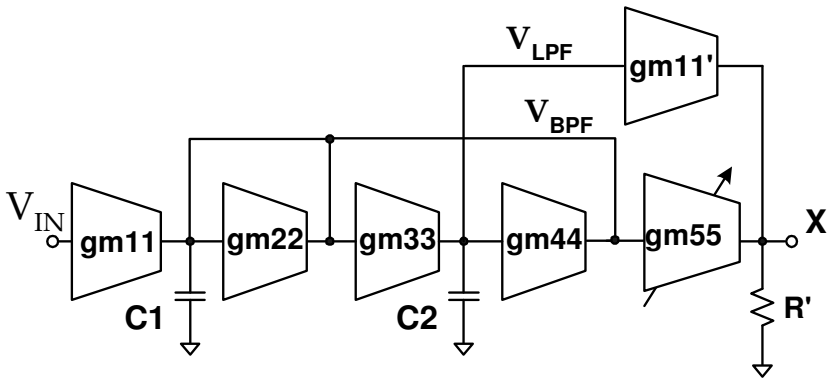


Fig. 2.4 Gm-C biquad used to realize an equalizer section.

2.1.2 Need for LC Equalizer

It can be seen that the active elements used to emulate an inductor (in any Gm-C resonator section) would make these filters noisier than their LC counterpart. An active LC bandpass filter that improves the dynamic range over Gm-C bandpass filter was initially demonstrated in [10], and an alternative approach was adapted in [11]. So far, improved performance of LC filter over the Gm-C ones was demonstrated only for narrowband RF applications and the main focus of these filters was to achieve high-Q bandpass response. Although an 800MHz LC lowpass Butterworth filter has been demonstrated in [12], it is essentially a passive ladder filter unsuitable for realizing equalization gain. Thus, efficient circuit techniques are yet to be developed to exploit the high dynamic range of LC resonators for wideband low-Q filters.

For bandpass filters, it has been shown that filters employing parallel LC resonators are about 2Q+1 times more power efficient compared to their Gm-C counterpart [13]. This advantage, however, is diminished for filters that employ biquads with low Q values. Another expression, discussed in [14], predicts power efficiency as a

function of inductor's quality factor but this applies to Q-enhanced LC filter. In the following sections, the proposed series resonator is described and its superior power efficiency for low-Q filter realization is demonstrated. Circuit implementation of the complete 5^{th} order Butterworth equalizing filter based on the proposed series LC resonator is discussed. Furthermore, a wide-band common mode feedback (CMFB) technique that provides high DC accuracy is discussed. Experimental results from the prototype design are also presented and are compared to state-of-the-art.

2.2 Analysis of Series Resonator Based Equalizer Section

To implement the equalizer sections shown in Fig. 2.3, both 2^{nd} order lowpass and bandpass signals are needed. An important property of series resonator prototype shown in Fig. 2.5(a) is that it generates both 2^{nd} order bandpass current and 2^{nd} order lowpass voltage as opposed to a parallel resonator which generates bandpass voltage alone. This property greatly simplifies the realization of the equalizer section. An active implementation of the series resonator prototype that uses just one transistor is proposed and is shown in Fig. 2.5(b). Transistor M1 generates bandpass current, acts as a buffer for the input and provides termination for the series resonator. Since large bandpass current is required to generate high equalization gain, re-use of M1 as termination element brings down the impedance level of the network. This factor in combination with reduced number of active elements results in superior noise performance and power efficiency.

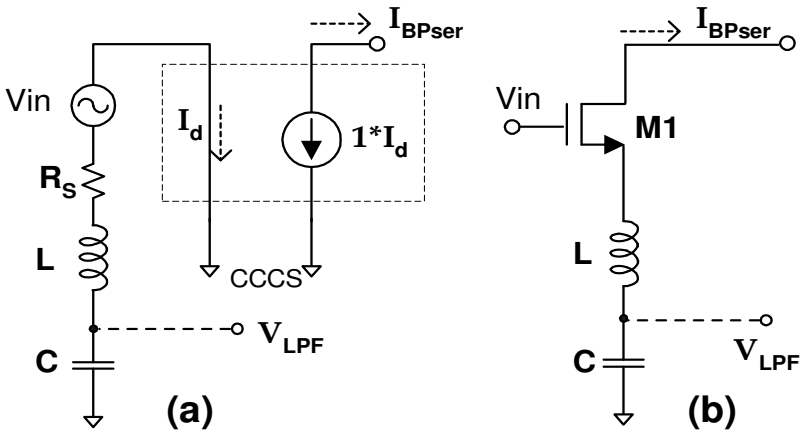


Fig. 2.5 (a) Series resonator prototype. (b) Transistor implementation.

An equalizer section with required poles and zero can be constructed as shown in Fig. 2.6. Properties of this series resonator based equalizer section are examined below.

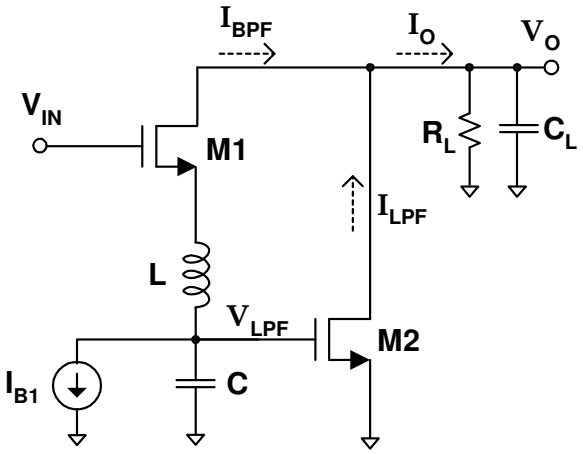


Fig. 2.6 Proposed Series resonator LC based equalizer section.

2.2.1 Frequency Response

Summation of bandpass and lowpass current signals generates an equalizing zero besides a pair of complex poles. Neglecting inductor and transistor (M1's) parasitics and modeling M1 using a T-model, simplified expression for output current I_o is obtained as:

$$I_O(s) = \underbrace{\frac{Vin * sC}{s^2LC + s\frac{C}{gm1} + 1}}_{I_{BPF}} + \underbrace{\frac{Vin * gm2}{s^2LC + s\frac{C}{gm1} + 1}}_{I_{LPF}} = \frac{Vin * (sC + gm2)}{s^2LC + s\frac{C}{gm1} + 1} \tag{2.4}$$

where gm1(2) is the transconductance of M1(2). Since a real zero gives a gain increase at the rate of 6dB/Octave for high frequencies, the equalizing zero (gm2/C) is to be placed two octaves ahead of resonant frequency $1/\sqrt{LC}$ ($\omega_O=2\pi*1.1$Grad/s) to achieve 12dB equalization gain per section. This implies $gm_2/C=\omega_O/4$ or $gm_1=4*Q*gm_2$. The equalization gain can be programmed between 0-12dB by scaling down the bandpass current. R_L acts as an I-V converter that converts $I_O(s)$ to $V_O(s)$. Due to the capacitance C_L, the output voltage (V_O) has a real pole in addition to the complex poles and equalization zero of $I_O(s)$. This real pole is assumed to be located at frequency $2\omega_O$ for rest of this section.

2.2.2. Noise

In order to analyze the noise properties of the equalizer, the basic principle of impedance scaling must be understood. The transfer function of an electrical network remains unaltered if the impedance of all the elements is scaled by the same factor (α). In case an active element like transistor is used, the transconductance must be scaled by

1/ α to retain the transfer function. Consider, for example, the Gm-C integrator in Fig. 2.7.

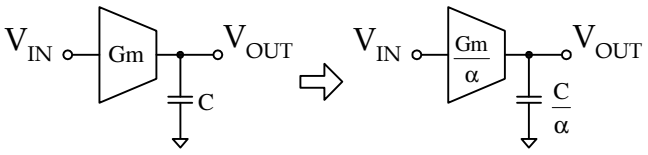


Fig. 2.7 Impedance scaling of a Gm-C integrator.

The transfer function of the integrator (Gm/sC) remains unaltered if both Gm and C are scaled by the factor 1/ α. How does one decide the absolute value of Gm and C since any scaled version will do equally well? This is where the noise performance of the circuit comes in to play. The integrated input referred noise (thermal) of the circuit in the bandwidth 0 to Gm/(2πC) is given by 8/3* kTγ/(2πC) where K is Boltzman constant, T is absolute temperature in Kelvins and γ is the noise factor of the transconductor. The Gm and C is typically scaled such that the total noise given by 8/3KT* γ /C meets the noise specification. This is a very important principle that lets the designers “scale” a circuit according to the noise performance required off the circuit. Thus, the Signal to noise ratio (SNR) of a filter can be scaled up by factor ‘α’ by scaling down all impedances by the same factor, which in turn increases power by the same factor. Impedance scaling can reduce noise only at the expense of power, leaving the product of power and noise unchanged [15]. Hence a quantity called ‘power-noise product’ is

introduced to asses the noise performance of the proposed circuit in the following analysis.

Since the total targeted boost gain is 24dB, a gain of 4 is assumed for the bandpass path (corresponding to a real zero at one-fourth of the resonant frequency ω_o or a boost gain = 12dB per section). R_L = 1/gm2 is assumed to ensure 0dB low frequency gain. Also, for noise calculations, R_L is assumed to be implemented by a transistor. The noise of I_{B1} is also considered since a common bias current for differential arms is not possible. Noise of all active elements is expressed in terms of V_{nGm2}^2 (input referred noise density of gm2). Expressions for output referred noise density due to lowpass path (V_{nLPF}^2) and bandpass path (V_{nBPF}^2) of the series-LC equalizer section are thus derived as:

$$V_{nLPF-LC}^2 = V_{nGm2}^2 \left| \frac{2\omega_o}{s+2\omega_o} \right|^2 \left\{ \frac{1}{4Q} \left| \frac{\omega_o^2}{D(s)} \right|^2 + \frac{1}{4Q} \left| \frac{\omega_o (Qs+\omega_o)}{D(s)} \right|^2 + 1 + 1 \right\} \tag{2.5}$$

$$V_{nBPF-LC}^2 = 4V_{nGm2}^2 \left| \frac{2\omega_o}{s+2\omega_o} \right|^2 \left\{ \frac{1}{Q} \left| \frac{s\omega_o}{D(s)} \right|^2 + Q \left| \frac{\omega_o^2}{D(s)} \right|^2 \right\} \tag{2.6}$$

where, $D(s) = s^2 + \omega_o s/Q + \omega_o^2$, the terms within the curly braces in (2.5) correspond to the noise contribution of M1, I_{B1}, M2 and R_L in that order and the terms within the curly braces in (2.6) correspond to the noise contribution of M1 and I_{B1} in that order. The total power consumed by the LC biquad is given by:

$$P_{LC} = (2+4Q) * P_{Gm2} \tag{2.7}$$

where P_{Gm2} is the power consumption of gm2. Similar analysis is also performed on Gm-C equalizer section shown in Fig. 2.4 for sake of comparison. Expressions for $V_{nLPF-GmC}^2$, $V_{nBPF-GmC}^2$ (noise density due to lowpass and bandpass path of the Gm-C equalizer section) and P_{GmC} (total power consumed by Gm-C equalizer section) are derived as follows.

A gain of 4 is assumed for the bandpass path (same as the LC equalizer case) yielding gm11=gm33=gm44=gm22*Q=gm11'=gm55/4=R' and C1=C2. Noise of gm11' and R' are not included since they are usually a part of next biquad or first order section (inclusion of this would result in double-counting of noise). Expressions for output referred noise density in lowpass path ($V_{nLPF-GmC}^2$) and bandpass path ($V_{nBPF-GmC}^2$) are given by:

$$V_{nLPF-GmC}^{\ 2} = V_{nGm11}^{\ 2}\left|\frac{2\omega_o}{s+2\omega_o}\right|^2 * \left\{\left|\frac{\omega_o^{\ 2}}{D(s)}\right|^2 + \frac{1}{Q}\left|\frac{\omega_o^{\ 2}}{D(s)}\right|^2 + \frac{1}{Q^2}\left|\frac{\omega_o(Qs+\omega_o)}{D(s)}\right|^2 + \left|\frac{\omega_o^{\ 2}}{D(s)}\right|^2\right\} \tag{2.8}$$

$$V_{nBPF-GmC}^{\ 2} = 16 * V_{nGm11}^{\ 2}\left|\frac{2\omega_o}{s+2\omega_o}\right|^2 * \left\{\left|\frac{s\omega_o}{D(s)}\right|^2 + \frac{1}{Q}\left|\frac{s\omega_o}{D(s)}\right|^2 + \left|\frac{\omega_o^{\ 2}}{D(s)}\right|^2 + \left|\frac{s\omega_o}{D(s)}\right|^2 + \frac{1}{4}\right\} \tag{2.9}$$

Total power consumed by the Gm-C equalizer section is given by:

$$P_{Gm-C} = (7+ 1/Q)\ P_{Gm11} \tag{2.10}$$

where P_{Gm11} is the power consumed by OTA Gm11.

A simple plot of the ratio P_{Gm-C}/P_{Gm11} is shown in Fig. 2.8.

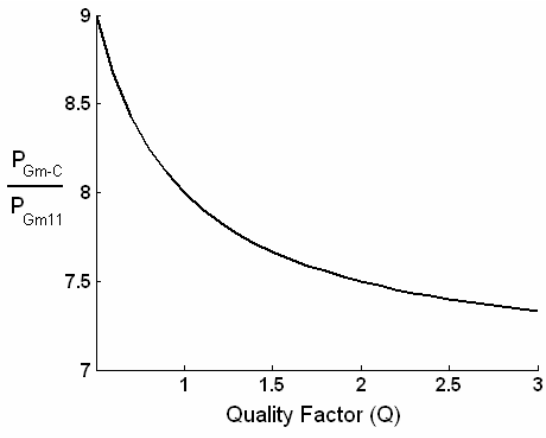


Fig. 2.8 P_{Gm-C}/P_{Gm11} vs quality factor.

The normalized power-noise products are found by taking the product of total power and total noise density and normalizing it by $V_{nGm2}^2 * P_{Gm2}$ ($V_{nGm11}^2 * P_{Gm11}$ in case of Gm-C equalizer).

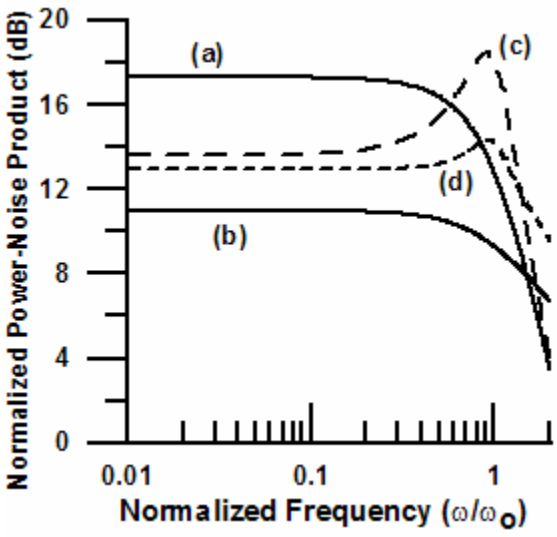


Fig. 2.9 Normalized power-noise product for Lowpass path (traces: (a) Gm-C, Q=0.618 (b) Series LC, Q=0.618 (c) Gm-C, Q=1.618 (d) Series LC, Q=1.618).

The normalized power-noise products for series-LC as well as the Gm-C equalizers are shown for lowpass path in Fig. 2.9 for Q=0.618 and 1.618. As expected the power-noise product of the series-LC equalizer section is significantly better than that of the Gm-C equalizer section. The slight degradation in out-of-band power-noise product in case of series-LC occurs due to the noise from I_{B1} having larger values near the resonant frequency.

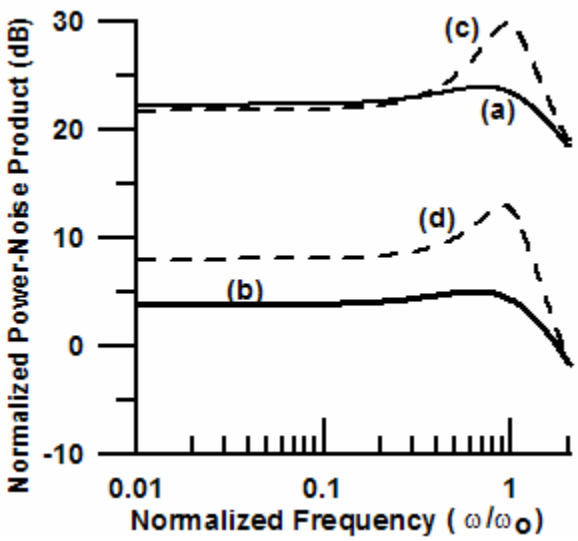


Fig. 2.10 Normalized power-noise product for bandpass path (traces: (a) Gm-C, Q=0.618 (b) Series LC, Q=0.618 (c) Gm-C, Q=1.618 (d) Series LC, Q=1.618).

The normalized power-noise products for bandpass paths are plotted in Fig. 2.10. Trends similar to the lowpass case in improvement of power-noise product in case of series-LC equalizer section are observed. The results of the power-noise product analysis are used to formulate the relative power efficiency of different equalizing structures.

2.2.3. Relative Power Efficiency

Since Gm-C filter is commonly used for wideband equalization (in sub-GHz frequency range), it is chosen as a benchmark for power efficiency. The relative power efficiency of the proposed LC equalizer section (η) is defined as the ratio of integrated power-noise product of Gm-C equalizer section to that of itself

$$\eta = P_{GmC}\int_0^{\omega_0}\left(V_{nLPF-GmC}{}^2 + V_{nBPF-GmC}{}^2\right)d\omega \Big/ P_{LC}\int_0^{\omega_0}\left(V_{nLPF-LC}{}^2 + V_{nBPF-LC}{}^2\right)d\omega \qquad (2.11)$$

Fig. 2.11 (trace a) shows the plot for η for different values of Q. It is evident from the plot that the proposed LC biquads (with Q=0.618 and Q=1.618) are on an average about 7.3 times more power efficient than Gm-C biquads.

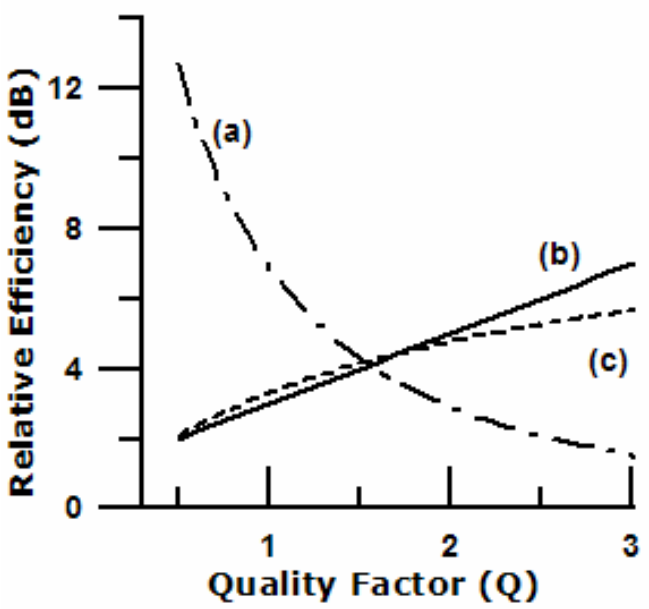


Fig. 2.11 Relative power efficiency versus quality factor (traces: (a) Series LC equalizer section - η (b) Parallel LC BPF - η_2 (c) Parallel LC BPF – η_{par}).

The relative power efficiency for parallel LC bandpass filter (BPF) with respect to Gm-C BPF (η_2) is obtained in [13] as 2Q+1 (shown in Fig. 2.11 trace b for reference). This, however, is valid only at resonant frequency (since it is derived based on noise density at resonant frequency). An appropriate relative efficiency for parallel LC BPF for wideband case (η_{par}) is found by integrating the noise across the pass-band and is plotted in Fig. 2.11 trace c for reference.

$$\eta_{par} = P_{GmC} \int_0^{\omega_0} \left(V_{nBPF-GmC}{}^2 \right) d\omega \Big/ P_{LCpar} \int_0^{\omega_0} \left(V_{nBPF-LCpar}{}^2 \right) d\omega \qquad (2.12)$$

where $V_{nBPF-LCpar}{}^2$ is output referred noise similar to (2.6) obtained for parallel LC BPF. From the plot it can be concluded that for low Q equalizer sections, the proposed LC biquad using series resonator is likely to be more efficient than a parallel LC based structure even if the problem of generating lowpass signal is solved for the latter.

2.2.4. Effect of Quality Factor of the Inductor

For a given value of L and ω_o, the termination resistance R_S (see Fig. 2.5(a)) is fixed by the Q of the biquad. To account for the loss in the coil, gm1 has to be scaled such that gm1'=gm1 $\frac{Q_L}{Q_L - Q}$ (where Q_L is the quality factor of the inductor). This ensures 1/gm1'+R_C=R_S (where R_C is the resistance of the coil). When this factor is accounted, the power consumption P_{LC} in (2.7) changes to $\left(2 + 4\frac{Q_L Q}{Q_L - Q}\right)$*$P_{Gm2}$. Saving for the noise contribution of I_{B1}, $V_{nLPF-LC}{}^2$ and $V_{nBPF-LC}{}^2$ remains almost

unchanged since the effective termination resistance is preserved. For Q_L=7.5 (used in this design), P_{LC} increases by 1.13 times (average between Q = 0.618 and 1.618) compared to (2.7). Just as additional data points, for Q_L=5 and 10, P_{LC} increases by 1.22 and 1.09 times respectively. Note the weak dependence of power-noise product on Q_L, which is in sharp contrast with that of Q-enhanced LC filters ($Q>>Q_L$) where the power-noise product is inversely proportional to Q_L^2 [14]. Essentially, large Q_L is not useful for low-Q series resonator biquads since it does not improve the power efficiency significantly.

2.2.5. Linearity

The differential implementation of the circuit shown in Fig. 2.6 (refer to Fig. 2.16) can be viewed as two differential pairs formed by M1 and M2. The differential pair formed by M1 takes advantage of the finite coil resistance of the inductor (Rc) to introduce source degeneration. The lowest value of source-degeneration factor in this case is gm1*Rc. For differential pair formed by M2, the source degeneration is explicitly added using a poly resistor. The worst case HD3, which corresponds to lowest source degeneration factor, is given by

$$HD3 \approx \frac{Vi^2}{32*(1+gm1*R_C)^2 V_{GST}{}^2} \tag{2.13}$$

where V_{GST} is the gate overdrive voltage of M1. Thus, the distortion performance can be improved by increasing R_C (reducing inductor's quality factor (Q_L)).

2.2.6. Area

Following analysis formulates the relationship between area of the proposed LC filter as a function of cut-off frequency (f) and SNR. Let A_{Co}, A_{gmo} be the total area taken by capacitors and transistors of a LC equalizer section respectively for signal to noise ratio SNRo(47dB) and cut-off frequency fo(1.1GHz). C, L and gm values can be projected as a function of SNR and f by applying impedance scaling and frequency scaling (for constant noise) respectively. Capacitor and transistor area scales by the same factor as C and gm respectively. To find the inductor area as a function of L, inductors with same Q value (=7.5) but different L values were created using the TSMC 0.18um CMOS design kit. The L values and area (including shield) measured from layout are shown in Table 2.1.

Table 2.1 Inductor area as a function of L.

L (nH)	**Area (Kμm^2)**
12	235
6	160
3	109
1.33	73

From this data the relation between L and area of inductor is fitted as $A_L(L)$ = 14.9*L+61.3 where L is expressed in nH and A_L is expressed in Kμm^2. The constant term in $A_L(L)$ is due to fixed shield area. Although this approximation for $A_L(L)$ tends to overestimate the area for large L, it is still used to keep the analysis simple and

insightful. A plot of $A_L(L)$ measured from the layout and its linear approximation is shown in Fig. 2.12.

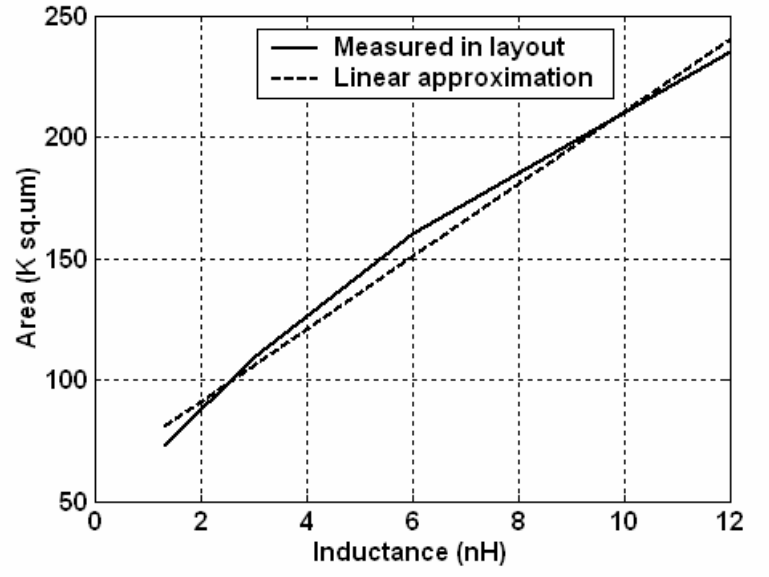


Fig. 2.12. Area of the inductor as a function of its value.

The area estimate for the series-LC equalizer section thus found from the above analysis is expressed as

$$\text{Area}_{LC}(\text{SNR}, f) = A_{Co} * \frac{\text{SNR}}{\text{SNRo}} + A_{gmo} * \frac{\text{SNR} * f}{\text{SNRo} * fo} + A_L \left(Lo * \frac{\text{SNRo}}{\text{SNR}} * \left(\frac{fo}{f} \right)^2 \right) \quad (2.14)$$

If $\eta_{1,2}$ represent the value of η obtained for the two biquads (with Q_1=0.618 and Q_2=1.618), area of a corresponding Gm-C filter (as a function of SNR and f) can be expressed in terms of A_{Co} and A_{gmo} as:

$$\text{Area}_{GmC}(\text{SNR}, f) = \frac{1}{2} \sum_{i=1}^{2} \left[A_{Co} * \frac{\eta_i (2 + 4Q_i)}{2(7 + 1/Q_i)} * \frac{\text{SNR}}{\text{SNRo}} + A_{gmo} * \eta_i * \frac{\text{SNR} * f}{\text{SNRo} * fo} \right] \quad (2.15)$$

In 0.18um technology, $Area_{LC}$(46dB,1.1GHz) = 630Kum^2 (area occupied by present design) which is about twice of $Area_{GmC}$(46dB,1.1GHz). However, from (2.14) and (2.15) it is projected that $Area_{GmC}$ would outrun $Area_{LC}$ beyond certain f for a given SNR and beyond certain SNR for a given f. Fig. 2.13 captures this trend by plotting both the areas in K-μm^2 across SNR and f.

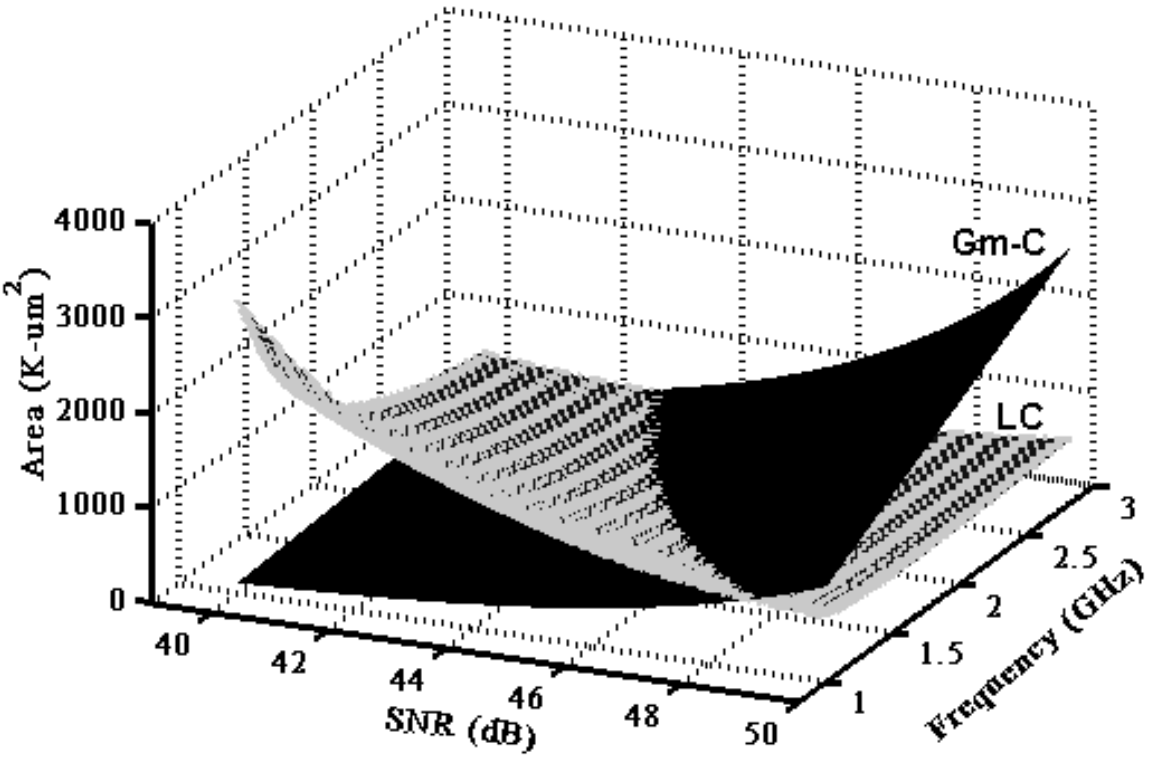


Fig. 2.13 Area comparison for Gm-C and LC equalizer section.

A cross section of the 3-D plot in Fig. 2.13 is provided at 2GHz in Fig. 2.14. $Area_{LC}$ initially reduces with increasing SNR due to the area reduction of the inductor. At SNR of about 47dB, $Area_{LC}$ gradually increases due to the dominance of area of the capacitors

and the transconductors. $Area_{Gm-C}$ equals $Area_{LC}$ for SNR of about 45dB and progressively increases for higher SNR. This trend suggests that the proposed LC biquad can achieve much better power efficiency without area penalty at sufficiently high frequencies or SNR.

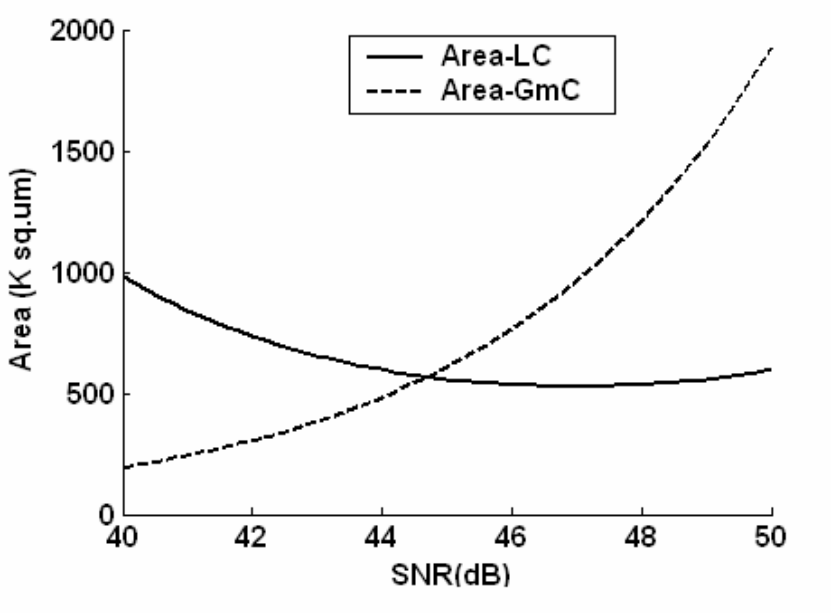


Fig. 2.14 Area of LC and Gm-C equalizer sections as a function of SNR at 2GHz.

Another aspect worth mentioning is that the area of inductor can be reduced at the expense of Q_L [16]. In this design, inductors have a metal width of 15μm for Q_L of 7.5. By decreasing metal width to 6μm (Q_L to 4.9), area can be reduced to 69% of its present value at an expense of 11% additional power. Reduction in inductor sizes can also be achieved by using technology that has Cu interconnects.

2.3 Proposed Architecture and Circuit Implementation

In the proposed architecture, the 5th order Butterworth filter is realized by cascading two series-resonator based LC equalizer sections. Since a real pole is associated with each equalizer section, there are 6 poles in the overall transfer function. The two real poles are placed such that their overall effect in magnitude and phase response in the pass-band is close to that of the single real pole in 5th order Butterworth response. In this design, these real poles are placed at 3GHz and 2GHz so that the magnitude error (1.3dB) and phase error (3.9degrees) are minimal in the pass-band.

A simplified single-ended version of the complete filter that realizes fifth order Butterworth function is shown in Fig. 2.15.

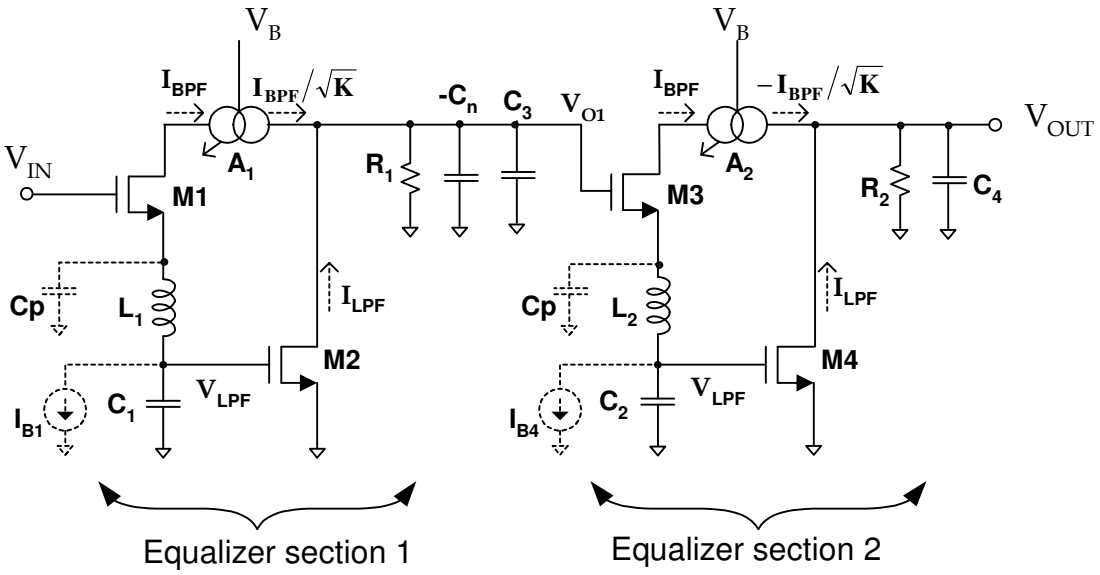


Fig. 2.15 Simplified schematic (single-ended) of the 5th order Butterworth filter.

Currents from transistors M1 and M3 (I_{BPF}) are required to be variable for programmability of equalization gain. This is achieved by variable gain current attenuators A_1 and A_2 controlled through V_B. The real pole at 1st biquad output is pushed to 3GHz by using a negative capacitor $-C_n$ (similar to one proposed in [17]) which is designed to counter the parasitic and common-mode detector capacitance at the output node of the 1st biquad (C_3). Ignoring the parasitic capacitance Cp, using (2.4) along with node equations at V_{O1} and V_{OUT}, the complete transfer function $H(s)=V_{OUT}(s)/V_{IN}(s)$ can be written as:

$$H(s) = \frac{(sC_1 + gm2)}{s^2 L_1 C_1 + s\frac{C_1}{gm1} + 1} * \frac{(sC_2 + gm4)}{s^2 L_2 C_2 + s\frac{C_2}{gm3} + 1} * \frac{1}{1 + s(C_3 - C_n)R_1} * \frac{1}{1 + sC_4 R_2} \quad (2.16)$$

For exact analysis of a very high frequency filter, effect of node parasitic cannot be ignored. Replacing the inductor by its pi model [18] and accounting for the critical parasitic capacitances of M1, M2 and I_{B1}, bandpass current which was earlier shown in (2.4) can now be modified as:

$$I_{BPF1}(s) \approx Vin \frac{sC'\left[s^2 L_1 Cp + sR_c Cp + 1\right]}{s^2 L_1 C' + s(R_c + 1/gm_1)C' + 1} \quad (2.17)$$

where $Cp=Cp'+Csb_{M1,}$ $C'=C_1 + Cp'+Cdb_{IB1}+Cgs_{M2}$, Cp' is the effective capacitance from each inductor terminal to substrate and R_c is the coil resistance. Here, Cdb_{IB1} refers to drain to bulk capacitance of the transistor that would realize I_{B1}. From (2.17), it can be seen that there is a pair of complex parasitic zeros whose frequency is slightly less than the self-resonant frequency of the inductor. Intuitively, this could be interpreted as the effect of the parasitic tank circuit formed by L_1, R_c and Cp (present in any practical LC

design). By choosing to connect current source I_{B1} at the capacitor-end of the inductor (V_{LPF} node) rather than the transistor-end, Cdb_{IB1} is absorbed in C' instead of Cp. This helps to keep the parasitic zeros far out from filter's pass-band. In the present design, parasitic zeros (complex) are located around 3.8GHz and 5.1GHz for biquad 1 and biquad 2, respectively, making their effect insignificant.

2.3.1 Biquad

The fully differential circuit implementation of a single equalizer section (without the loads) is shown in Fig. 2.16. To make the circuit balanced and hence improve the common mode rejection, the differential arms share the same floating capacitor (C) for the resonator. Moderate frequency tuning is provided by PMOS varactors controlled by external voltage V_{TUNE}. The gain in the bandpass path is varied using a Gilbert-cell based attenuator ($A_{1,2}$ in Fig. 2.15). Transistors Mg (Fig. 2.16) form this Gilbert-cell, which is used to control the location of the real axis zero in the transfer function and thereby controlling the boost gain. Current sources (I_{B2}) are controlled through a CMFB loop discussed in section B.

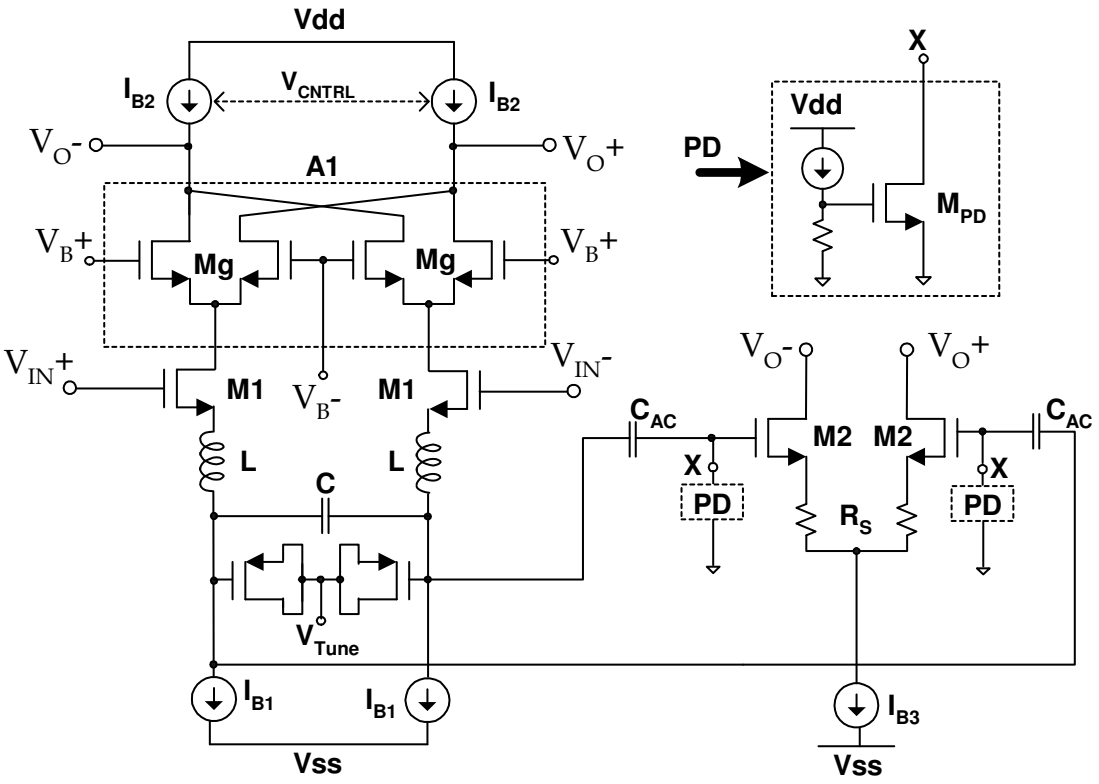


Fig. 2.16 Schematic of the proposed fully differential series LC resonator based equalizer section.

The differential pair formed by M2 implements the transconductor in the lowpass path. The differential pair is ac coupled to the resonator in order to minimize the voltage headroom requirement of the biquad. The ac coupling is achieved by using a blocking capacitor C_{AC} and a pull-down transistor (M_{PD} in PD block) biased in deep-subthreshold. This approach is similar to the quasi-floating gate technique described in [19] but avoids completely cut-off transistors to ensure that the gate of M2 stays at common mode voltage (0V). Note that high threshold voltage of 700mV (source of M_{PD} is connected to

0V instead of VSS) prevents device M_{PD} from 'turning on' even for the peak signal swing.

2.3.2 Negative Capacitance

The negative capacitance emulation circuit (similar to one in [17]) is shown in Fig. 2.17. Assuming that this circuit is operated at a frequency well below the f_T of M5, the single ended admittance of this circuit can be approximated as $\frac{-sCn * gm5}{gm5 + sCn}$. The pole of the admittance lies at frequency ω_{Cn}=gm5/Cn, which makes this circuit appear like a capacitor –Cn at frequencies much less than ω_{Cn}. When connected to node V_{O1}, this effectively pushes the first order pole to higher frequency ($\omega_3=2\pi*3$Grad/sec in this case).

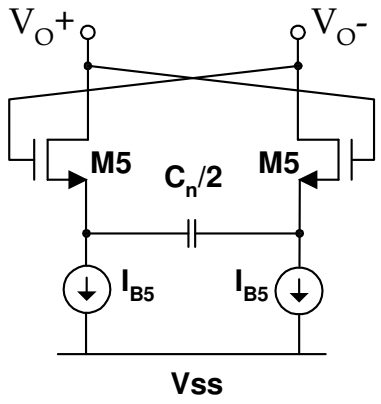


Fig. 2.17 Negative capacitance emulation circuit (similar to one in [17]).

For this design, since gm5 ≅ gm2, the noise density at the output of the equalizer section due to this circuit (including noise from M5 and I_{B5}) can be expressed as

$$V_{nCn}^{\ 2} = V_{nGm2}^{\ 2}\left|\frac{\omega_3}{\omega_3 + s}\right|^2 \tag{2.18}$$

From (2.18) and plots in Fig. 2.9 and Fig. 2.10, it can be concluded that the noise contribution due to this circuit is insignificant. Also, the distortion contribution of the negative capacitance circuit is very small. The capacitor Cn/2 offers a reactive source degeneration factor of gm5/jωCn, which suppresses the distortion by >30dB at 1.1GHz and even more at low frequencies. This is expected since the voltage to current conversion, in the frequency of interest, is mostly performed by the linear element Cn, rather than gm5.

2.3.3 Common-mode Feedback

Although useful signal is present only up to filter's cut-off frequency (1.1GHz), the differential -3dB bandwidth increases to about twice the nominal value under application of large boost gain. In order to avoid boosting of common mode noise, a CMFB bandwidth of about twice the cutoff frequency is desirable. A new method is proposed to achieve such large bandwidth in common mode loop.

One of the main limitations of the CMFB loop bandwidth is the pole at the output of the equalizer section (V_O+, V_O- node in Fig.2.3.2). In the proposed technique, the load resistance (R_2 for second equalizer section) is split between the common-mode load resistance R_2'=2*R_2 and the common-mode detector resistance R_2''=2*R_2 as shown in

Fig.2.3.4. This allows for high frequency pole at output node (Vo+, Vo-) as well as a common mode detector (R_2'' and C_4) that is virtually frequency independent. The pole at output node for common-mode signals, determined by the R_2' and the output parasitic capacitance (Cpo), is about 2π*2.6Grad/s for this design.

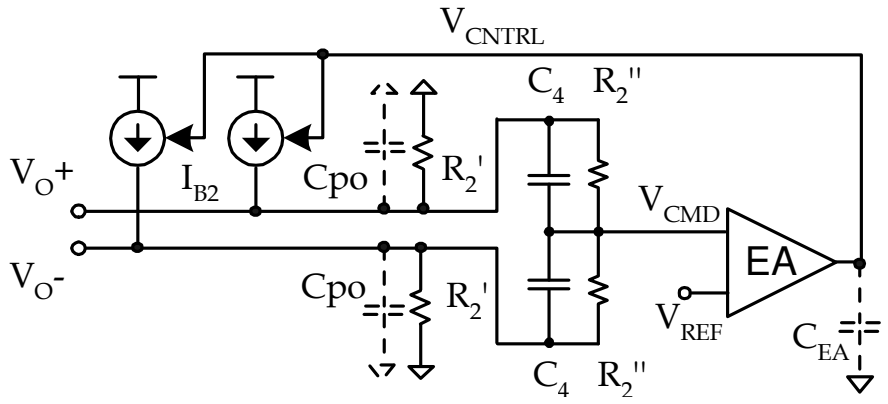


Fig. 2.18 Implemented CMFB loop.

If the error amplifier (EA) is a simple integrator with a single low frequency pole, two limitations occur. Firstly, the maximum unity gain frequency that can be achieved for the CMFB loop shown in Fig. 2.18 is about 1.5GHz for 60^O phase margin (due to non-dominant pole $1/R_2$'Cpo located at 2.6GHz). Secondly, for the same phase margin, the transconductance of the current source I_{B2} (Gm_{IB2}) is upper bounded by

$$Gm_{IB2} \le \frac{1}{1.5}\left(\frac{1}{R_2'Cpo}\right)^2 \frac{C_{EA}}{Gm_{EA}} Cpo \qquad (2.19)$$

where C_{EA} and Gm_{EA} are the load capacitance and the transconductance of the EA. The usual implication of this upper bound is that not all bias current of the biquad can be

flown through the controlled source I_{B2}. Therefore, only a part of the bias current source can be controlled by the CMFB loop. Under extreme offset condition, control of only a fraction of bias current could result in significant variation of I_{B2}'s output conductance (due to large or small overdrive applied to part of the controlled current source). The proposed implementation of current source and EA circumvents the above limitations.

A split frequency current source (Fig. 2.19) used in [20] to avoid latching states in opamp is used in place of I_{B2}, It comprises of transistors M15 and M15' and R_6-C_6 network. DC transconductance is determined by both M15 and M15' while high frequency behavior by M15 alone. Note that, by choosing $1/R_6C_6$ well below unity gain frequency, the effective loading of EA at V_{CNTRL} node (C_{EA}) is limited to gate capacitance of M15 (along with junction capacitance of M13 and M14).

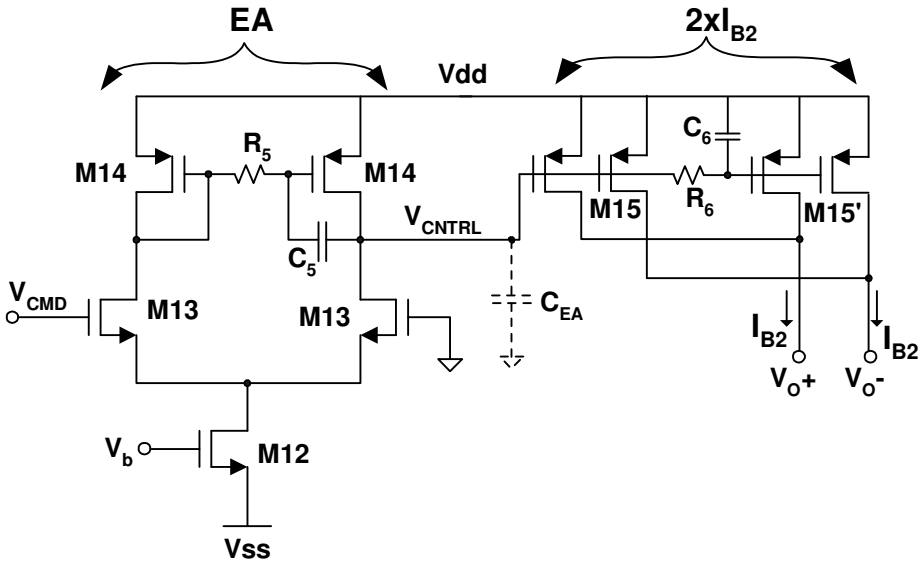


Fig. 2.19 Proposed EA and split frequency current sources.

Combination of the low pass and the direct path driving M15' and M15 respectively results in a pole-zero pair in transconductance of I_{B2}, which is given by

$$Gm_{IB2}(s) = \frac{I_{B2}(s)}{V_{CNTRL}(s)} = \frac{gm_{15}(s+\omega_{z2})}{(s+\omega_{P3})} = \frac{gm_{15}(1+k+sR_6C_{gs15'})}{(1+sR_6C_6)} \tag{2.20}$$

where k (=2) is the ratio of sizes of M15'and M15 and $C_{gs15'}$ is gate capacitance of M15'

It is preferred to have a high gain EA for well controlled operating points and DC accuracy. Also, the pole introduced by the split frequency current source needs to be cancelled in order to extend the bandwidth. To this end, the EA shown in Fig. 2.19 with R_5 and C_5 applied around M14 is used. Transfer function of the EA is given by

$$\begin{aligned} H_{EA}(s) = \frac{V_{CNTRL}(s)}{V_{CMD}(s)} &= \frac{gm_{13}R_o(s/\omega_{z1}+1)}{(s/\omega_{P1}+1)(s/\omega_{P2}+1)} \\ &= \frac{gm_{13}R_o(sR_5C_5/2+1)}{(gm_{14}R_OR_5C_5s+1)(sC_{EA}/gm_{14}+1)} \end{aligned} \tag{2.21}$$

where C_{EA} refers to parasitic capacitance at V_{CNTRL} node and $R_O = 1/(gds_{14}+gds_{13})$.

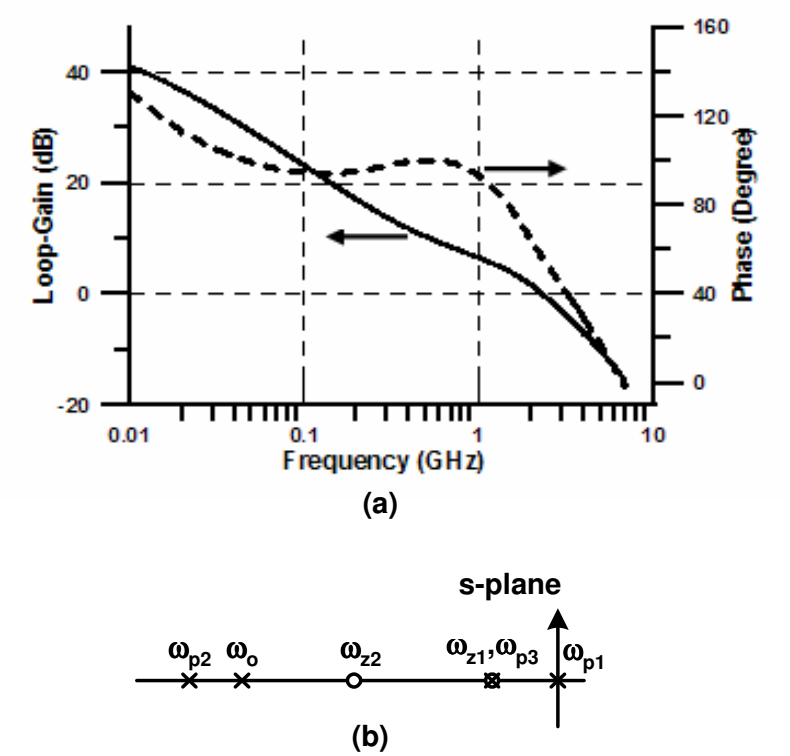


Fig. 2.20 (a) AC response of the CMFB loop. (b) Poles and zeros in s-plane.

AC response (open loop) of the complete CMFB loop is shown in Fig. 2.20(a). Also indicated in Fig. 13(b) are relevant poles and zeros. ω_{p1} is the dominant pole located around 2π*13Mrad/s, ω_{z1} and ω_{p3} are situated around 2π*500Mrad/s. ω_{z2} (introduced by R_6-C_6 network) partially recovers the phase lost due to the dominant pole and extends the bandwidth. The output pole (1/R2'Cpo) is located around 2π*2.6Grad/s while ω_{p2} is at about 2π*5Grad/s. Corner simulations show a minimum unity gain frequency of 2.2GHz and a worst case phase margin of 50^{O}.

2.4 Experimental Results

The prototype for 1GHz equalizing filter was fabricated using TSMC 1P6M 0.18µm standard CMOS technology. Thick Metal-6 layer is used for inductors. The filter layout is folded so as to minimize magnetic coupling between two biquads without sacrificing much area. The microphotograph of the chip is shown in Fig. 2.21.

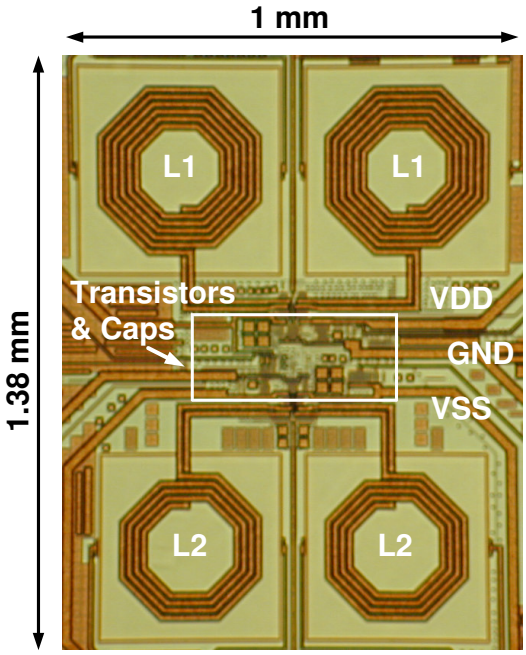


Fig. 2.21 Chip micrograph.

2.4.1 Test Setup

A schematic of the test setup is shown in Fig. 2.22. Differential input is generated by using wideband pulse inverter based balun (picoseconds 5315A). Measurement of the S_{21} of the equalizer, especially at the out-of-band frequencies, posed a particular difficulty due to feedthrough of input through the printed circuit board (PCB). Due to

lack of good quality balun at the output, an offline difference method was used to accurately measure the transfer function. The S_{21} parameter of each of the single ended outputs was measured and saved as a complex vectors after averaging over a sufficient time. The complex vectors were then subtracted using a MATLAB program to generate the correct differential output that is free of a common-mode feedthrough component from the PCB.

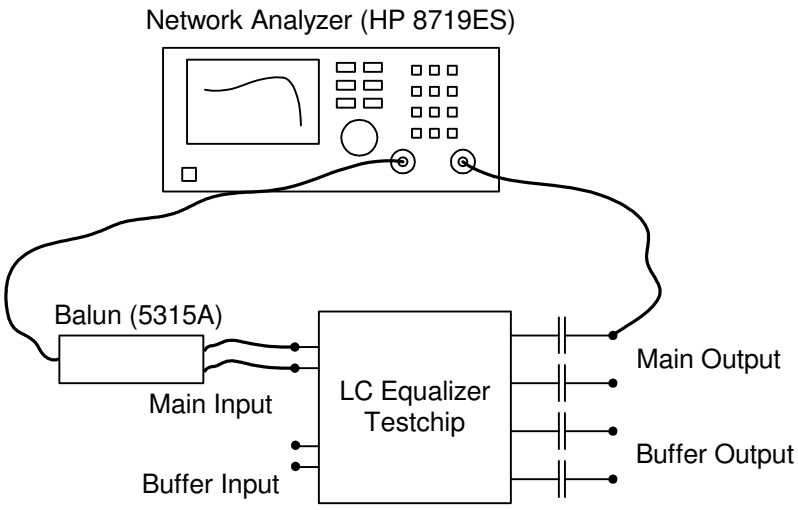


Fig. 2.22 Test setup for measurement of the transfer function of the equalizer.

A photograph of the PCB used to make the measurements is shown in Fig. 2.23. The PCB is made as compact as possible and the ground planes were split between input and the output sides in order minimize the feedthrough of signal from input to output in the out-of-band frequencies.

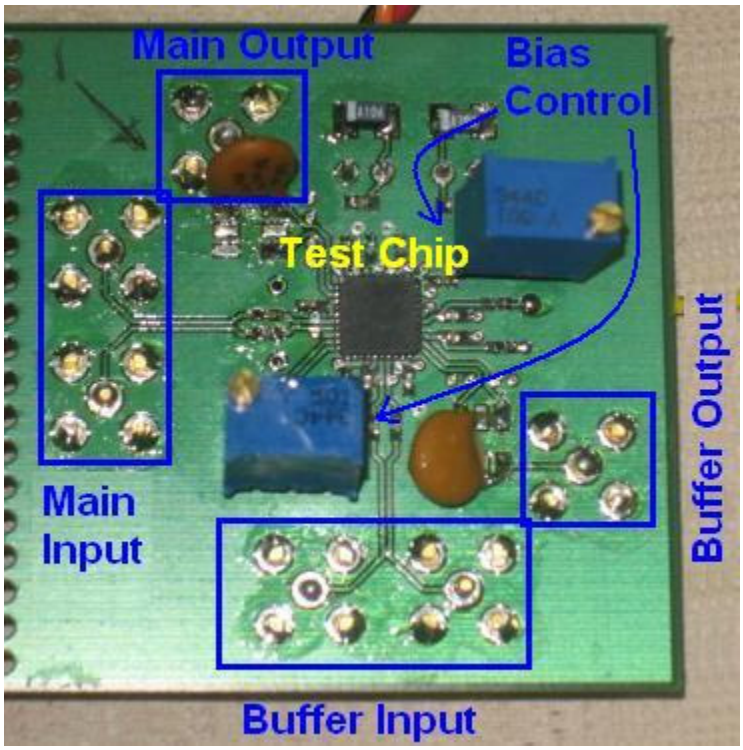


Fig. 2.23 PCB used for testing the equalizer testchip.

2.4.2 Measurements Results and Comparison

The frequency response was measured through a network analyzer using the setup described in section 2.4.1. An on-chip buffer is used at the output of the filter to isolate bondpad, bondwire and external loads. Stand-alone buffer, also included in the chip, is used to de-embed the buffer response. Experimental magnitude plots, thus obtained, are shown in Fig. 2.24.

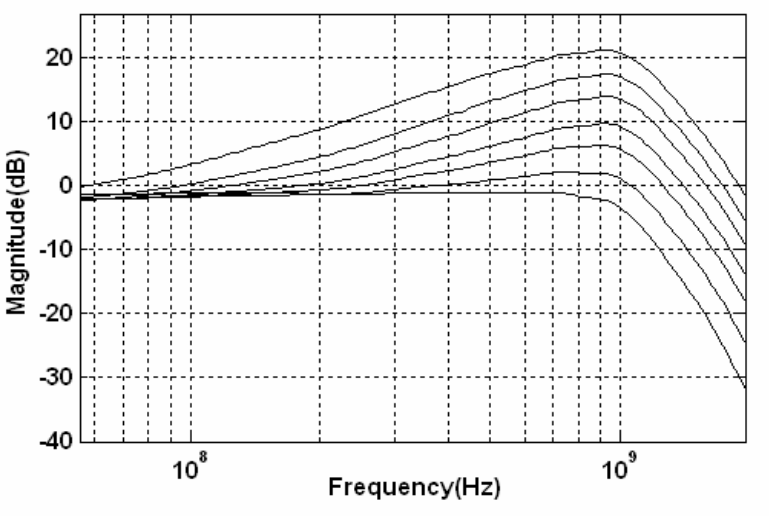


Fig. 2.24 AC magnitude across boost measured using network analyzer.

A maximum boost gain of 23.6dB is achieved. The filter displays -3dB frequency of 1.15GHz, which can be manually tuned by ±7% using varactors' control (V_{TUNE}). Note that for the LC filter, where L variation with process are small [21] and MIM capacitor also show minimal variation (< ±3%, as per the process data from the kit), such range might be sufficient to cover for process variations. The group delay response for 0dB boost gain setting is shown in Fig. 2.25.

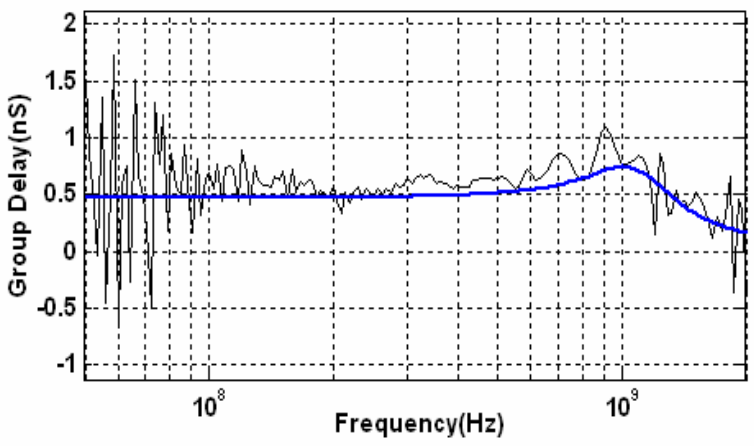


Fig. 2.25 Measured group delay response (bold trace corresponds to ideal group delay of 5^{th} order lowpass Butterworth filter).

To measure linearity performance around highest pass-band frequency, a two-tone test is performed by applying tones at 925MHz and 975MHz with a total peak-peak voltage of 250mV. A setup similar to the one used for measuring frequency response is employed with signal generator at input and spectrum analyzer at output port. Third order intermodulation distortion (IM3) of -48dB is observed at 0dB boost setting (shown in Fig. 2.26) and -58dB is observed at 23dB setting. The improvement at higher boost gain setting is attributed to lower voltage swings in the first biquad (for IM3 test at highest boost, input signal needs to be scaled down to maintain same output swing). Table 2.2 summarizes the experimental results.

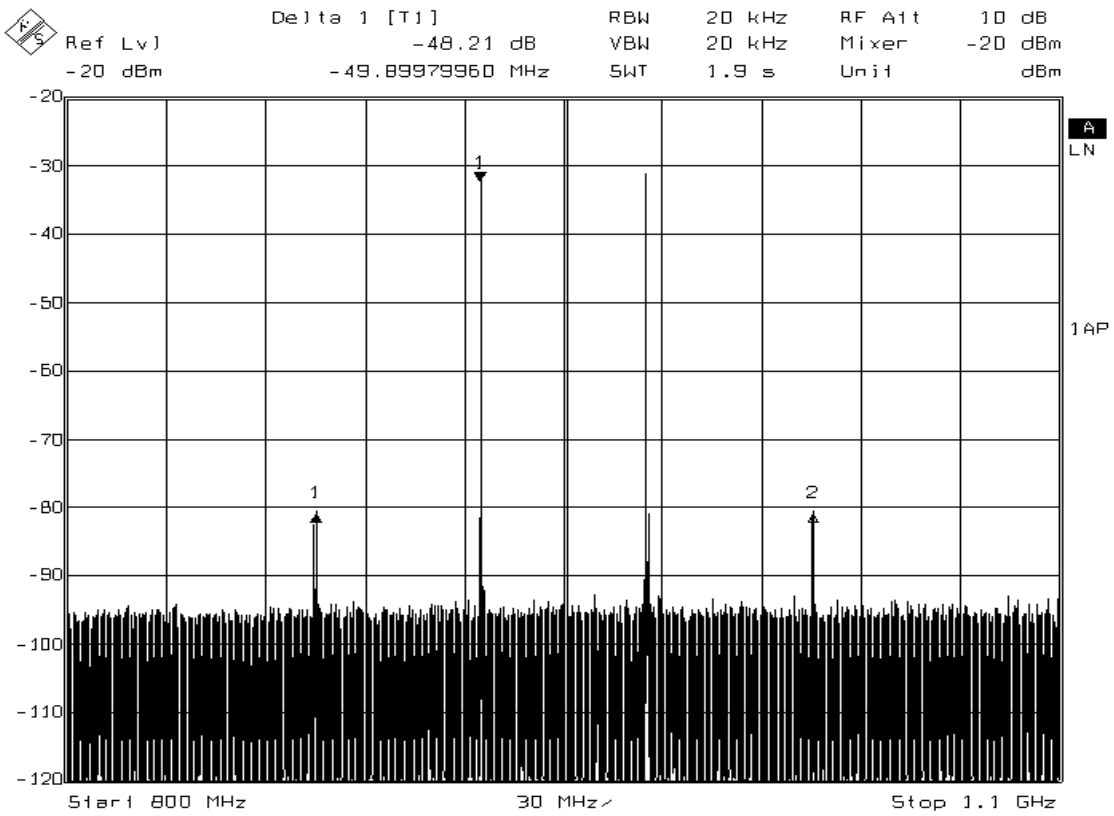


Fig. 2.26 Measured intermodulation distortion.

Table 2.2 Experimental results for the proposed LC equalizing filter.

Parameter	Value
Bandwidth at no boost	**1.074-1.23GHz**
Maximum boost	**23.6dB**
Power	**72.2mW**
IM3 at 0dB boost	**-48.2dB**
Output swing	**250mVp-p**
SNR at 0dB boost	**47dB**
Low frequency gain (at 50MHz)	**-0.5 to -1.8dB**
Frequency tuning range	**±7%**
Total area	**1.38mm^2**

Key aspects of some of the benchmark CMOS Gm-C equalizing filters are shown in Table 2.3. Due to differences in the equalizing gain, transfer function, signal swings, cut-off frequency and distortion performance, comparison of power-noise product among the filters in Table 2.4.2 is very difficult. Since many of these aspects are common between [9] and this work, the relative power efficiency of the proposed LC equalizing filter can be estimated against the Gm-C equalizing filter in [9]. After normalizing for cut-off frequency, IM3 and SNR, the relative power efficiency is calculated to be 7.9, which is close to the theoretical prediction of 7.3.

Table 2.3 Comparison of proposed LC equalizing filter with Gm-C equalizing filters.

Reference	[7]	[5]	[22]	[9]	This Work
BW (MHz)	120	200	300	330	1100
Boost (dB)	14	13	8.5	24	23
Order	8	7	4	5	5
SNR (dB)	45	-	53	49	47
THD (dB)	50	42	40	40 (IM3)	48 (IM3)
Signal swing (Vpp)	0.2	0.8	0.4	0.25	0.25
Technology feature (μm)	0.25	0.25	0.35	0.35	0.18
Power (mW)	120	210	156	43	72

2.5 Summary

To the best of my knowledge, this work has demonstrated the first wideband active LC equalizing filter for GHz range in silicon. Bandwidth of the filter is 1.1GHz with maximum boost gain of 23.6dB around cut-off frequency. Measurement results show IM3 of -48dB around 950MHz and SNR of 47dB. The proposed series resonator based architecture is shown to be well suited for realizing low Q equalizing filters. Specific quantitative analyses are presented for series LC, parallel LC and Gm-C topologies in terms of power-noise and quality factor. It was also shown that for applications working at even higher frequencies, the series LC biquad filter could retain the power efficiency benefit without any area penalty.

2.5.1 Future Work

Some of the equalizer applications need a wide programmability range for the bandwidth of the equalizer. This is required in order to support varying data rates and it is important to recognize that this is different from fine-tuning the bandwidth to account for process variations. A Gm-C equalizer is readily programmed in a wide range by switching transconductors in and out of the circuit [23]. It might appear that the LC equalizer can be programmed to smaller bandwidths by switching in additional capacitors. This, however, this is not feasible due to two reasons. Firstly, the bandwidth is inversely proportional to square-root of the capacitance unlike the Gm-C case (where it is inversely proportional to the capacitance). This would require impractically large capacitors. Secondly, the transconductance of the series transistor has to be increased

along with the capacitor in order to preserve the quality factor of the biquad. This would be detrimental to the power consumption of the LC equalizer.

A possible solution could be to increase the inductance while keeping the capacitor constant (note that this also achieves a constant integrated noise performance across various bandwidth settings). The important upside of this approach is that the series resistance should increase proportional to the reduction of the bandwidth for maintaining a constant quality factor. This would possibly allow low quality factor, small area, large value inductors (even one that includes lower metal levels) to be switched in when the bandwidth has to be reduced (see Fig. 2.27). A good research direction would be to investigate a bandwidth programmable LC equalizer with this approach whose bandwidth can be programmed down to one-half of the nominal value of the bandwidth.

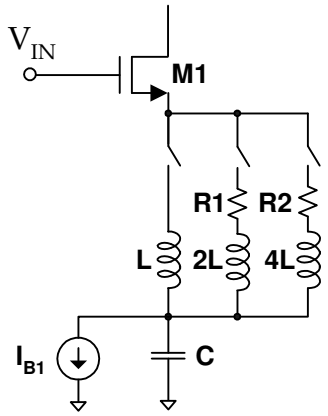


Fig. 2.27 Bandwidth programming of LC equalizer.

CHAPTER III

A 1.2mW 1.6Vpp SWING CLASS-AB 16Ω HEADPHONE DRIVER CAPABLE OF HANDLING LOAD CAPACITANCE UP TO 22nF

3.1 Introduction

Due to rapid growth in mobile entertainment electronics, the demand for high efficiency headphone drivers has generated a great deal of interest in recent times. While there are many publications related to class-D speaker drivers, little attention is paid to the problem of designing a power efficient and robust class-AB driver for headphones. Owing to the modest distortion performance and electro magnetic interference (EMI) issues, class-D drivers are generally not preferred for headphone applications. Hence the class-AB architecture is usually chosen for such applications.

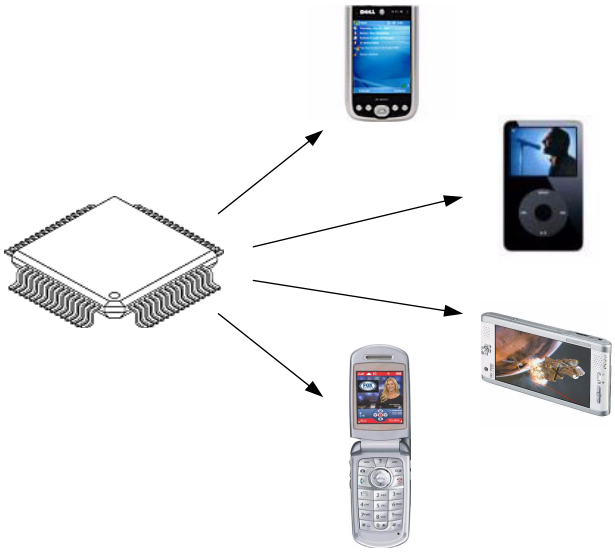


Fig. 3.1 Driver module to be deployed in a wide range of platforms.

In order to reduce design cycle time and time-to-market, a versatile driver that can be deployed to a variety of platforms is preferred (see Fig. 3.1). Also, the end-users typically prefer to use the headphone output as an input for other devices like desktop speakers, FM transmitters, home theater systems, etc. The challenge presented by this kind of usage is that the load impedance at the driver output varies in a wide range.

The load resistance variation is easily handled in most cases. For smaller resistances, the voltage swing at the driver output should be cut down according to the maximum output current capability of the class-AB stage. This is to ensure that the distortion performance is retained. For larger load resistance there is no change required. In fact, the distortion performance improves under this condition due to the improved linearity of the class-AB stage. Some of the platforms also use a FM choke in series with the headphone. The purpose of the FM choke is to block the FM signal from getting in to the driver while the headphone cable doubles as an antenna for the FM radio receiver. As will be apparent later, the presence of this FM choke nullifies the damping provided by the load resistance. Hence, the main challenge in the design of the driver lies in the variation of the capacitive load. Capacitive loads as large as 20nF are used in some platforms for electro static discharge (ESD) protection and EMI suppression. Other platforms may use low capacitance diodes for ESD protection. Also, depending on the usage conditions, the cable capacitance can range from few tens of pF to few 100pF. Hence it is desirable that the driver handle load capacitance ranging from few pF to 20nF.

Another important aspect of the driver used in the portable gadgets is its power efficiency. The power efficiency (P_{EFF}) is defined as the ratio of the average power delivered to the load to the average power dissipated from the supply. The peak-to-average ratio or the crest factor (CF) of the waveform plays a major role in determining the power efficiency of the amplifier. This relates to the fact that the degree of usage of the power supply voltage is inversely proportional to the CF. For instance, in Fig. 3.2, the waveform has a peak to peak swing of $2*V_P$ but on an average, the waveform utilizes only a fraction of the power supply equal to $1/(2CF)$. Here, CF is defined as V_P/V_{RMS} with V_{RMS} denoting the root mean square of the waveform across time.

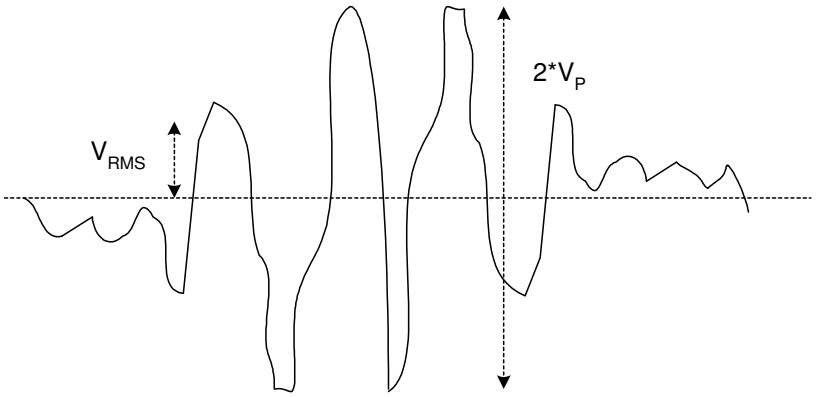


Fig. 3.2 Supply voltage utilization limit due to crest factor.

With the simplifying assumption of rail-to-rail output voltage swing ($VDD=2*V_P$), the average power dissipation (P_{AVG}) of the class-AB stage is given by

$$P_{AVG} = \frac{V_P^{\,2}}{CF*R} + 2V_P I_Q \tag{3.1}$$

where I_Q is the quiescent current and R is the load resistance.

The first term represents the signal dependant power dissipation, which is a product of supply voltage of each half of the class-AB stage (V_P) and the average load current (V_P/(CF*R)). The second term represents the power due to the quiescent current used to bias the class-AB stage.

The power efficiency of the class-AB stage, which is the ratio of the actual power delivered to the load (V_P^2/(CF^2*R)) to P_{AVG}, can be expressed as

$$P_{EFF} = \frac{1}{CF\left(1 + 2CF\frac{I_Q}{I_P}\right)} \tag{3.2}$$

where I_P is the peak current delivered to the load.

Since the CF of the music waveform is large (~20dB), the quiescent current significantly affects the P_{EFF} of the driver. In order to improve power efficiency, $I_P/I_Q >> 2CF$ is desired.

In summary, the main design goal for the headphone driver is to achieve stable operation for capacitive loads ranging from 1pF to 20nF while minimizing the quiescent power dissipation.

3.1.1 Previous Work on Class-AB Audio Drivers

In this section, a summary of some of the headphone driver design with emphasis on their strengths and weakness will be discussed. A low-voltage two-stage class-AB driver is proposed in [24]. This design uses a folded-mesh biasing approach described in [25] to achieve 0.8V operation. The folded-mesh approach eliminates the need for two

series diode connected transistor in the bias circuit. It uses a “minimum selector” circuit that is shown in Fig. 3.3.

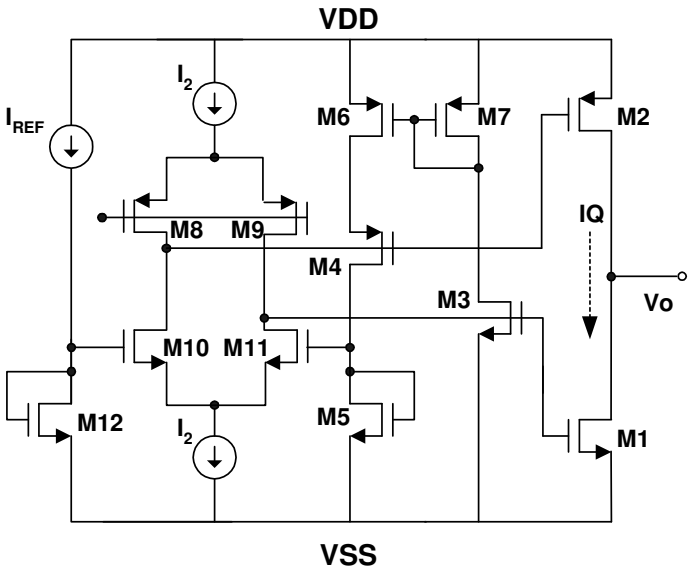


Fig. 3.3 Folded mesh circuit for low voltage class-AB biasing.

In this circuit, transistors M3-M7 realize the minimum selector circuit. Assume that the transistors are sized such that $(W/L)_{M5}$ equals $(W/L)_{M12}$, and $(W/L)_{M6}$ equals $(W/L)_{M7}$. The amplifier consisting of M8-M11 serves to force current through M5 to I_{REF}. In quiescent state, M6 is in triode region and M4 and M6 together acts like a “composite transistor” with twice the length. Under this condition, M5 sees a bias current that is proportional to the average of the bias currents of M1 and M2, which sets the quiescent current. When M1 is strongly conducting, M6 is in deep triode region, acting like a closed switch. M4 serves to mirror the current through M2, thus maintaining a minimum current equal to the quiescent current for M2. Similarly, M2 is

strongly conducting, M4 acts like a cascode device and M3, M6 and M7 serves to mirror the current through M1. This serves to maintain a minimum current equal to the quiescent current for M1.

This design supports a maximum of 0.45Vpp output, which produces only 1.6mW of maximum power at 16Ω headphone load. Thus, the main drawback of this approach is that the power delivered to the headphone is inadequate for many cases. The other drawback is that the linearity is limited to about 65dB (even for a small swing of 0.45Vpp) due to limited gain in the two stage amplifier.

An interesting approach that uses an adaptive bias current to minimize the quiescent current is proposed in [26]. A block diagram representation of the adaptive bias generation circuit is shown in Fig. 3.4.

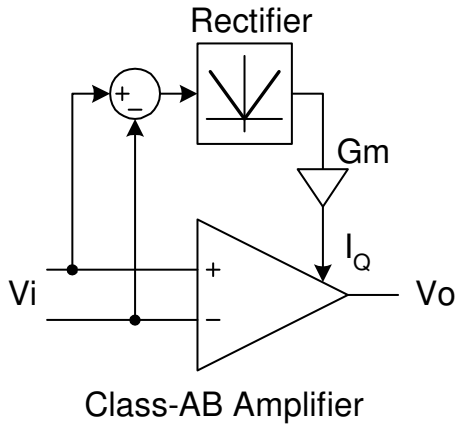


Fig. 3.4 Adaptive quiescent current generation.

The virtual ground of the opamp typically displays very small swing due to high gain of the amplifier. However, when large cross-over distortion occurs, virtual ground

deviates from this state and begins to show a larger variation. This variation is sensed by a summer and is rectified and used an error signal to adjust the biasing of the class-AB output stage. Despite using this technique, the design provides only a modest distortion performance of 50dB. Although this distortion performance maybe sufficient for a speakerphone driver, this is definitely inadequate for a headphone driver. Besides, the non-linear feedforward path created by the adaptive bias generator results in additional stability issues that needs to be solved.

Another design presented in [27] is based on three-stage nested miller compensated (NMC) class-AB amplifier. The basic topology used (standard NMC) is shown in Fig. 3.5. This circuit was designed in 65nm technology using 1.2V devices. In order to prevent breakdown of these devices, cascoding of the output devices are used. Since the three-stage amplifier has sufficiently large gain, a reasonable distortion performance of 68dB is achieved. The design also supports wide range of load capacitors ranging from no load to 12nF. The main drawback of this approach is that the quiescent power consumption of the amplifier is quite large (12.5mW), which is mainly attributed to the NMC scheme.

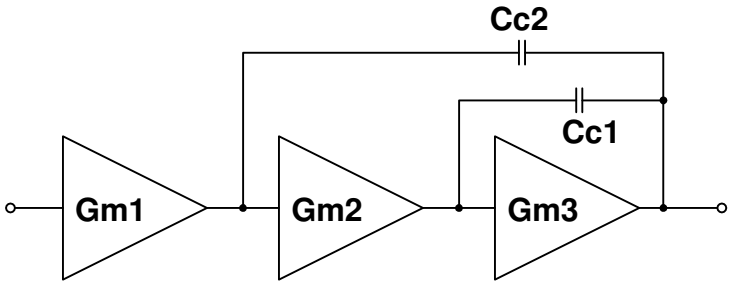


Fig. 3.5 Nested miller compensation topology.

Table 3.1 Merits and demerits of existing headphone amplifier designs.

Reference	Main feature	Merit	Demerits
[24]	Two-stage folded mesh biased class-AB	Low voltage operation (Vdd=0.8V)	1. Limited output power 2. Modest distortion performance
[26]	Two-stage class-AB with adaptive quiescent current control	Low quiescent power	1. Stability issues due to adaptive bias 2. Modest distortion performance
[27]	Three-stage NMC compensated	27mW power output using 1.2V 65nm devices	1. 12.5mW quiescent power consumption 2. Large area of capacitors

A summary of merits and demerits of the approaches discussed is presented in Table 3.1. The main conclusion from these approaches is that the three stages are required in the amplifier in order to achieve the required linearity performance since none of the two-stage amplifier achieves good distortion performance. It is also apparent that the power consumption in case of the NMC amplifier is quite large and an alternate compensation scheme is desired.

3.2 Compensation Schemes and Their Behavior Under Large Load Variation

Due to large swings associated with the input of a class-AB stage, at least 3-stages are required in the amplifier to meet the distortion performance (>80dB). Thus, 3-stage class-AB architecture was chosen for the driver. Two stage amplifiers that support a wide range of loads have been reported [28-29] but so far this capability is not demonstrated in 3-stage amplifiers. Several compensation schemes for 3-stage amplifiers driving large capacitance load with power efficiency more than 10 times that of the conventional nested miller compensation (NMC) scheme have been reported recently [30-34]. The damping factor control frequency compensation (DFCFC) is the core idea behind many of these schemes and is also suitable for low resistance drivers. The main aim of these compensation schemes is to maximize the performance for a single value of capacitive load. However, all of these schemes are vulnerable to large peaking in frequency response and potential instability when the load capacitance is dropped to small values. In order to come up with a compensation scheme for a wide range of capacitive loads, an insightful intuitive analysis of the 3-stage amplifier compensation scheme and the pole locus as a function of capacitive load is required. The following sections present these analyses.

3.2.1 Intuitive Interpretation of 3-stage Amplifier Compensation and Power Efficiency Improvement in DFCFC

A proposed equivalent circuit of a 3-stage amplifier with miller capacitor around second and third stage is shown in Fig. 3.6 Gm1 represents the transconductance of the

first stage of the amplifier. A2 represents the gain of the second stage and A3 represents the third stage gain inclusive of the load capacitance. The following reasonable assumptions are necessary for the equivalent circuit to hold.

a) The capacitance at the output node of Gm1 is much smaller compared to Cc1.

b) The loading of Cc1 at the output is small compared to that of the actual load capacitor at the output.

c) The feed-forward current via Cc1 to the output is insignificant. Due to low resistance load, the transconductance of the last stage tends to be large. This makes the frequency at which the forward current from the capacitor Cc1 dominates the current from to output stage (i.e. the zero frequency) very large. Hence, the effect of the feed-forward path can be safely ignored in this equivalent circuit.

There are two ways to interpret this equivalent circuit. a) Replace Cc1 with equivalent grounded capacitors by applying miller's theorem. This yields a grounded capacitor of value (1+A2A3) Cc1 at the input of amplifier stage A2 and another grounded capacitor at the output of A3 with value (1+1/(A2A3)) Cc1. The capacitor at the output can be ignored since it would be much smaller than the actual load capacitance. b) Think of A2A3 as a high gain amplifier. A2A3 along with Cc1 acts an "active RC" integrator though the current generator is Gm1 instead of R. Now, the full circuit can be modeled as an integrator (Gm1/sCc1) cascaded by A2A3 in unity feedback (-A2A3/(1+A2A3)). Cc1 provides the unity feedback assuming high output impedance for Gm1 and ignoring the parasitic capacitance at the output node of Gm1. Both

approach gives the same result, however, the second approach gives very good insight and helps easy understanding of more complicated cases.

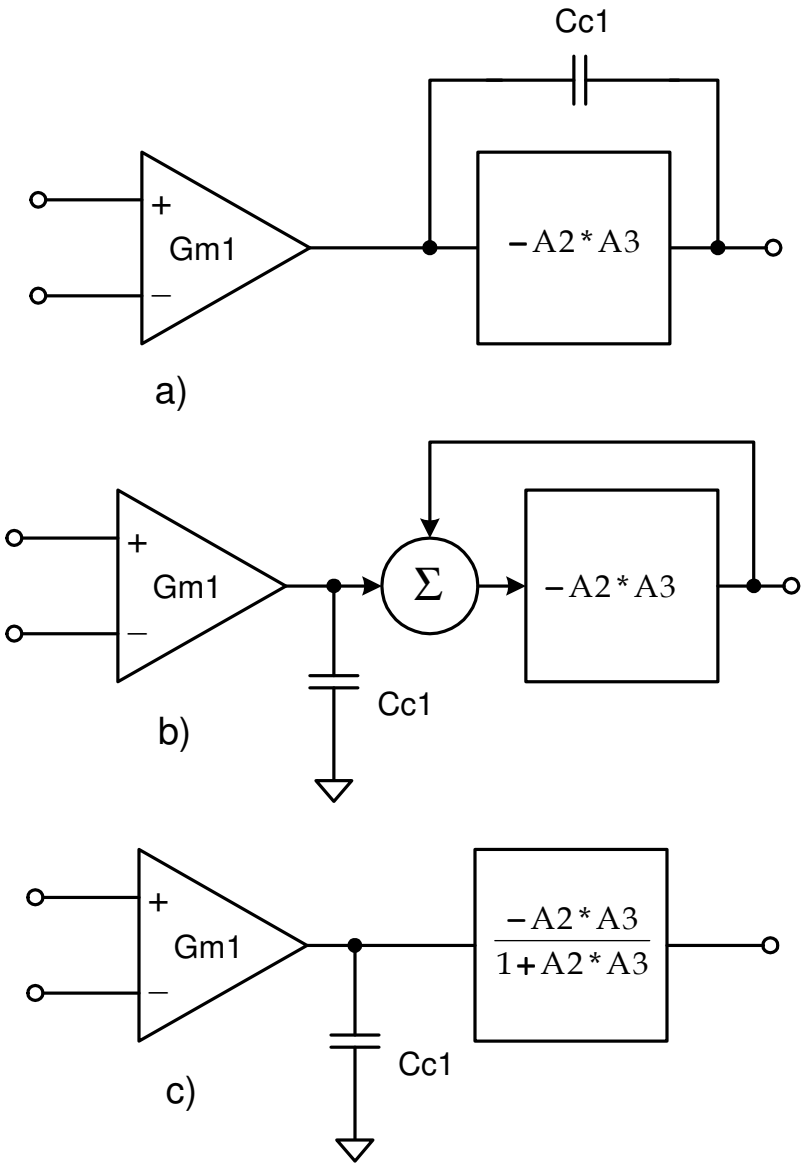


Fig. 3.6 (a) Simplified representation of 3-stage amplifier. (b) Cc1 providing unity feedback around second and third stage. (c) Equivalent circuit.

The equivalent circuit is very useful for the analysis since it breaks up the problem of 3-stage compensation to that of an integrator and a biquadratic section (hitherto referred as biquad) design, which are very well understood. Also, the behavior of the closed loop poles of the 3-stage amplifier can be easily understood by looking at the complex poles of the biquad in this equivalent circuit. Further analysis is performed for a) NMC, the basic multistage compensation scheme and b) DFCFC, one of the power efficient compensation schemes suitable for low resistance drivers.

The biquad formed by the second and third stage in the unity feedback loop for both of the cases are shown in Fig. 3.7. Gm2 and Gm3 represent the transconductance of the second and third stage respectively. Cc2 is the second miller compensation capacitance. Cp3 is the parasitic capacitance at the input node of the third stage. GmD is the conductance of the damping resistance (implemented by a transconductor) and C_D is the blocking capacitance of the damping network.

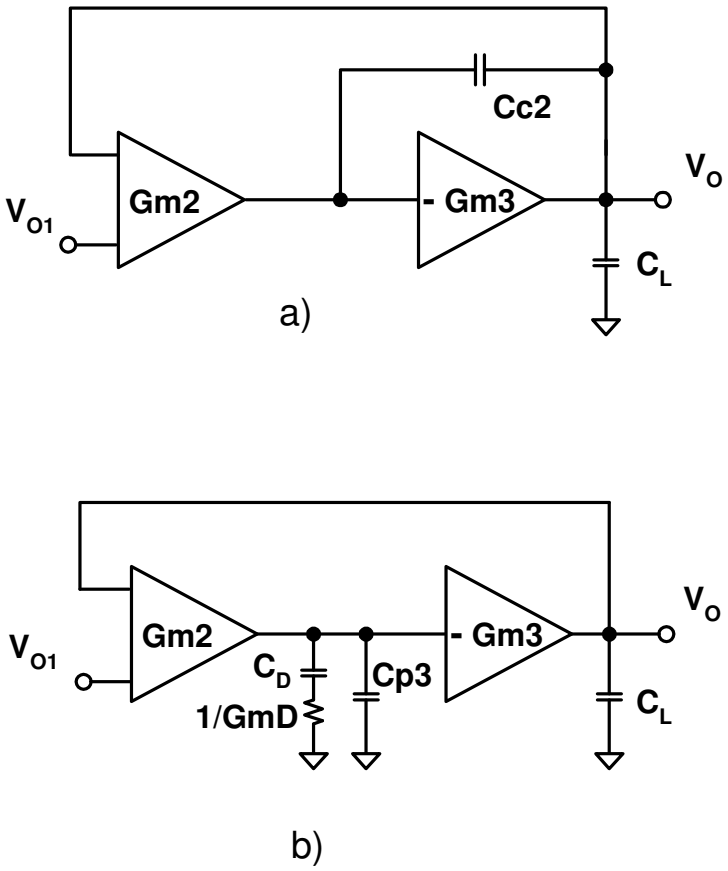


Fig. 3.7 (a) Second and third stage in unity feedback loop – NMC. (b) Second and third stage in unity feedback loop – DFCFC.

In case of NMC, the transfer function of the biquad section is given by

$$\frac{V_O}{V_{O1}} = \frac{\frac{Gm2Gm3}{Cc2C_L}}{s^2 + s\frac{Gm3}{C_L} + \frac{Gm2Gm3}{Cc2C_L}} \tag{3.3}$$

The product and the sum of the poles are given by $Gm3/C_L$*$Gm2/Cc2$ and $Gm3/C_L$ respectively. The square root of the product of the poles is defined as pole magnitude

(ω_{23}) and the sum of the poles is defined as the "loss bandwidth" (ω_{23}/Q_{BQ}) of the biquad, where Q_{BQ} refers to the quality factor of complex poles of the biquad.

The conditions to achieve 3rd order Butterworth pole constellation for the full closed loop 3-stage amplifier (including the integrator and biquad) shown in Fig.3.3, can be derived as follows. The third order lowpass Butterworth transfer function is given by

$$H_{B3}(s) = \frac{\omega_{CL}{}^3}{s^3 + 2s^2\omega_{CL} + 2s\omega_{CL}{}^2 + \omega_{CL}{}^3} \tag{3.4}$$

where ω_{CL} is the closed loop pole magnitude

The transfer function of the open-loop three stage amplifier is given by

$$Ao(s) = \frac{Gm1}{sCc1}\frac{\omega_{23}{}^2}{\left(s^2 + s\frac{\omega_{23}}{Q_{BQ}} + \omega_{23}{}^2\right)} \tag{3.5}$$

where Gm1/Cc1 is the first stage (integrator) bandwidth

Since the amplifier will be used in inverting unity gain configuration, the closed loop gain is given by

$$A_{CL}(s) = \frac{1}{2}\frac{Ao(s)}{1 + Ao(s)/2} = \frac{Gm1/Cc1 * \omega_{23}{}^2/2}{s^3 + s^2\frac{\omega_{23}}{Q_{BQ}} + s\omega_{23}{}^2 + Gm1/Cc1 * \omega_{23}{}^2/2} \tag{3.6}$$

Since we need $A_{CL}(s)=H_{B3}(s)$, we can compare the denominator of right hand side of (3.4) and (3.6). This comparison yields $\omega_{23}=\sqrt{2}\omega_{CL}$, $Q_{BQ}=1/\sqrt{2}$ and $Gm1/Cc1=\omega_{CL}$. This translates to the following conditions on the bandwidth of the gain stages.

$$\frac{1}{2}\frac{Gm3}{C_L} = \frac{Gm2}{Cc2} = \frac{Gm1}{Cc1} = \omega_{CL} \tag{3.7}$$

Note that for a given bandwidth of the amplifier and the load capacitance C_L, the output stage transconductance Gm3 is fixed. This limitation is due to the fact that the loss bandwidth of the biquad is solely determined by $Gm3/C_L$, as indicated by (3.3).

In case of DFCFC biquad, the transfer function contains an additional pole-zero pair due to the damping network. The root locus of the overall amplifier is largely independent of this pole-zero pair and hence its effect can be safely ignored. The transfer function of the DFCFC biquad section is thus approximated by

$$\frac{V_O}{V_{O1}} \approx \frac{\frac{Gm2Gm3}{Cp3C_L}}{s^2 + s\frac{GmD}{Cp3} + \frac{Gm2Gm3}{Cp3C_L}} \tag{3.8}$$

The pole magnitude squared and the loss bandwidth of the biquad is given by $Gm2/Cp3*Gm3/C_L$ and GmD/Cp3 respectively. Following the same procedure used to derive (3.7), the conditions for the Butterworth pole constellation can be easily verified to be

$$\frac{1}{2}\frac{GmD}{Cp3} = \frac{Gm1}{Cc1} = \omega_{CL} \tag{3.9}$$

and

$$\frac{Gm2}{Cp3}\frac{Gm3}{C_L} = 2\omega_{CL}^{\ 2} \tag{3.10}$$

An important change enabled by the damping network is that the loss bandwidth is determined by an independent parameter namely, GmD/Cp3. This change allows the design to trade Gm2/Cp3 for $Gm3/C_L$ for a given product shown in (3.10). Since Cp3 is due to parasitic capacitance of the transistors, it can be a few orders of magnitude

smaller than C_L in case of large C_L. Hence, for a given numerical value of the ratio, Gm2/Cp3 can be realized with substantially lesser power than $Gm3/C_L$. This helps to keep the power dissipation down since the quiescent power can be solely dictated by the distortion performance rather than the frequency compensation.

3.2.2 Effects of Load Capacitance Variation

For the fixed load amplifiers, the closed loop poles of the amplifier are typically designed to fall in the Butterworth constellation [35]. This is done in order to achieve a fast and smooth transient response. However, the Butterworth pole constellation is inevitably disturbed if the load capacitance is varied by a large factor. The following analysis quantifies this variation and its effects.

Assume that the 3-stage amplifier is designed for Butterworth pole constellation for C_L=20nF. As it can be seen from (3.3) and (3.8), the magnitude of the complex poles of the biquad increases as C_L is dropped from 20nF. In case of NMC, the denominator of the biquad's transfer function is of the form $D(s) = 1+K_1s+K_2C_Ls^2$ where K_1 and K_2 are coefficients that depend on the transconductance and compensation capacitances. The quality factor of the complex poles of the biquad is given by

$$Q_{BQ-NMC} = \frac{\sqrt{K_2 C_L}}{K_1} \tag{3.11}$$

Since the quality factor is proportional to $\sqrt{C_L}$, dropping C_L from 20nF to 200pF, for instance, would reduce $Q_{BQ\text{-}NMC}$ from 0.7 to 0.07 (which actually results in real poles). Assuming that the compensation is designed to have Butterworth pole constellation for a

load capacitance of C_L and setting ω_{CL} to 2πMRad/S, the step response of 3-stage NMC is computed for load capacitances of C_L, $C_L/10$ and $C_L/100$. The step responses thusly computed are shown in Fig. 3.8. The plots indicate that in case of NMC, dropping the capacitive load by a big factor does not adversely affect the step response of the amplifier.

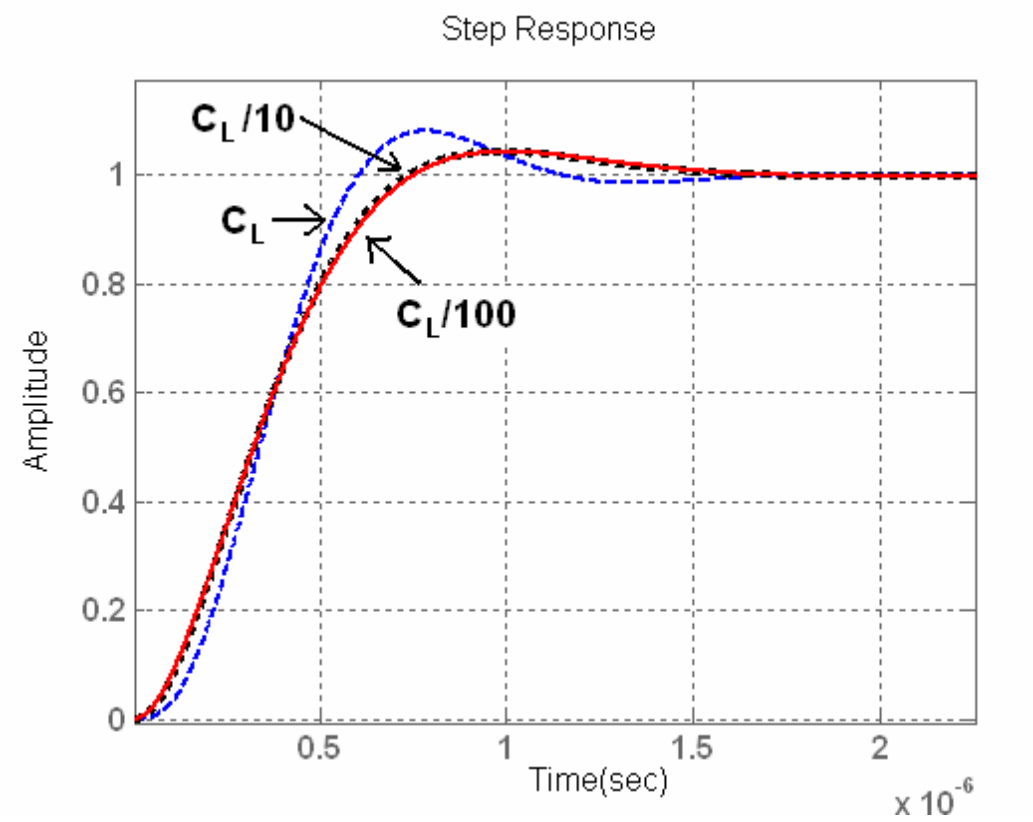


Fig. 3.8 Step response of NMC with Butterworth poles for load capacitance = C_L.

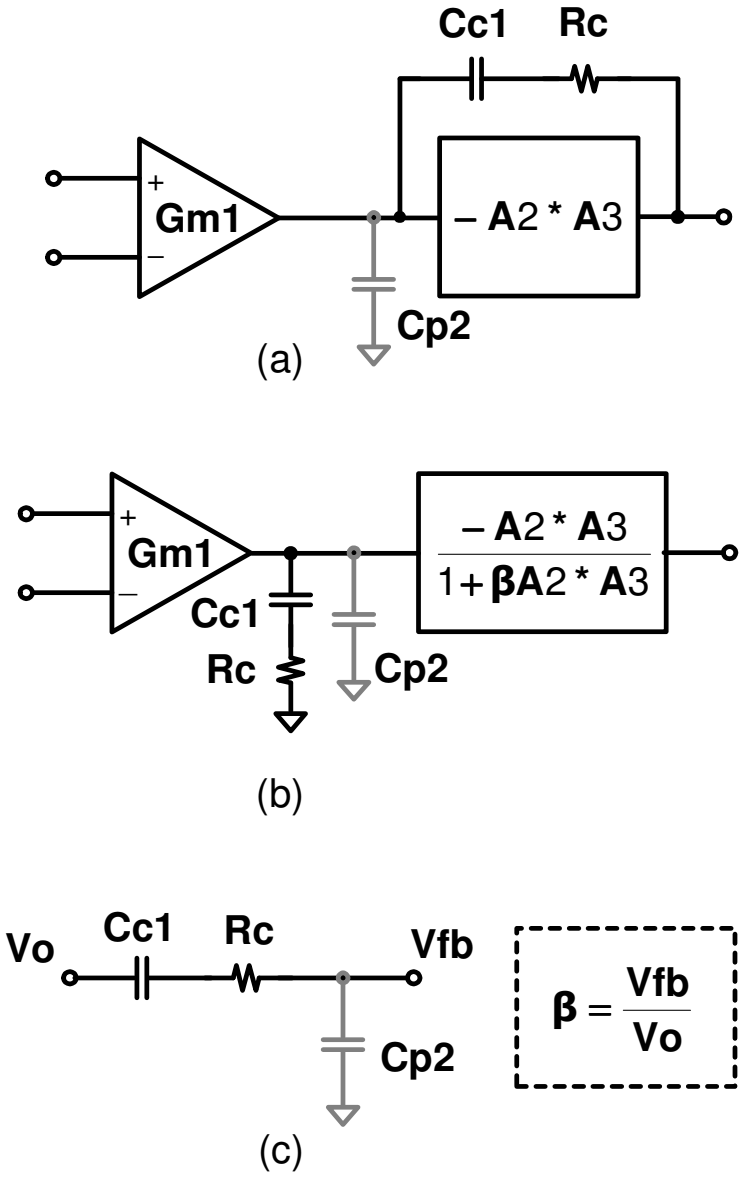


Fig. 3.9 (a) 3-stage amplifier with LHP zero resistor. (b) Equivalent circuit. (c) Feedback factor for A2*A3.

Since the driver input is a band-limited audio signal, rapidly changing inputs are not expected. The Butterworth pole constellation yields a phase margin of about

60degrees for the open loop amplifier. In most cases, the Butterworth pole constellation can be sacrificed to one that has a lower phase margin for the open loop amplifier. This reduction in phase margin translates to power savings in the second and third stage of the amplifier since the product $Gm2/Cc2*Gm3/C_L$ is reduced. Further reduction in power can be achieved by introducing a LHP zero using a resistor (Rc) in series with the compensation capacitor Cc1 (see Fig. 3.9.a)).

With the resistor Rc, the model for the 3-stage amplifier changes to one shown in Fig. 3.9.b). The unity feedback around 2^{nd} and 3^{rd} stage is now modified to a feedback with a factor β equal to $Cc1/(sRcCc1Cp2+Cp2+Cc1)$, where Cp2 represents the parasitic capacitance at the input of the second stage. Essentially, the LHP zero at 1/RcCc1 brings in an additional parasitic real pole placed roughly at 1/RcCp2. An example design with 45degrees phase margin is achieved by dropping the product $Gm2/Cc2*Gm3/C_L$ from $2\omega_{CL}^2$ to $1.18\ \omega_{CL}^2$ and setting the LHP zero at $\omega_{CL}/\sqrt{2}$. The additional parasitic real pole is assumed to be located at $5\ \omega_{CL}$. The step responses of the 3-stage amplifier using this design are shown in Fig. 3.10. As in case of Butterworth constellation, the step responses are acceptable even for $C_L/10$ and $C_L/100$.

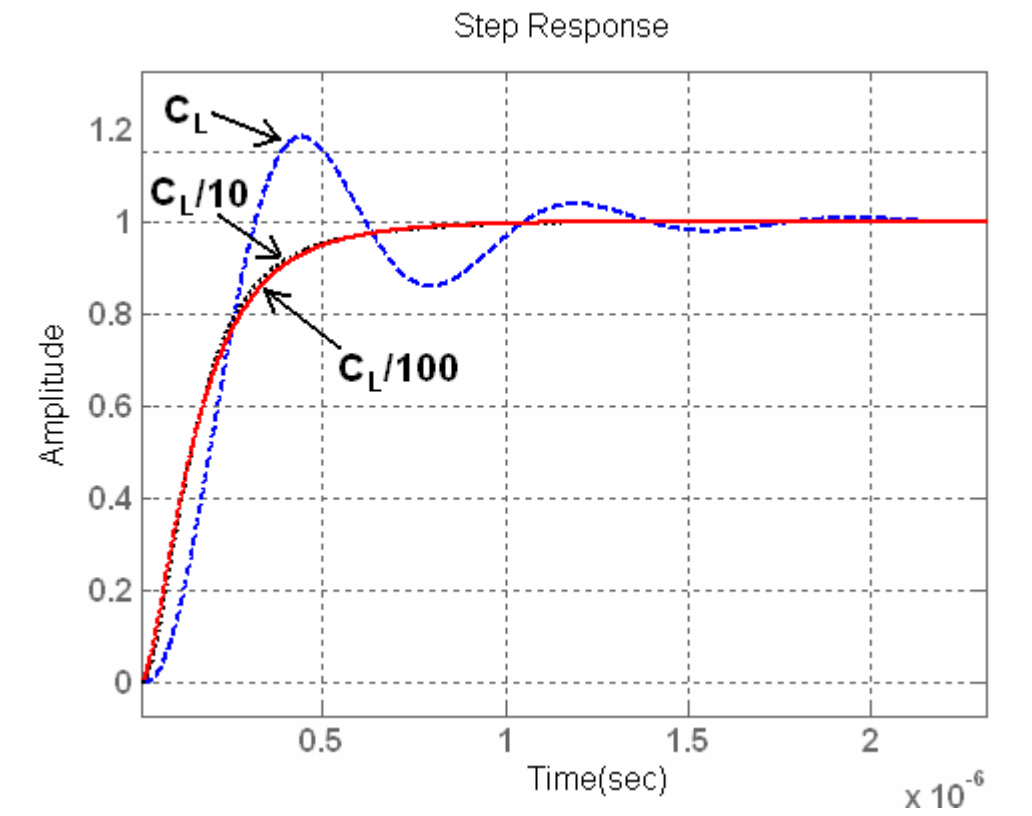


Fig. 3.10 Step response of NMC with 45degrees phase margin for load capacitance = C_L.

In case of DFCFC, the denominator of the biquad's transfer function is of the form $D(s) = 1+K_1C_Ls+K_2C_Ls^2$. The quality factor of the complex poles of the biquad is given by

$$Q_{BQ-DFCFC} = \frac{1}{K_1}\sqrt{\frac{K_2}{C_L}} \tag{3.12}$$

Since the quality factor is proportional to $1/\sqrt{C_L}$, dropping C_L from 20nF to 200pF would increase $Q_{BQ\text{-}DFCFC}$ by 10 times (from 0.7 to 7). Since the Q of the closed loop complex poles of the 3rd order system (3-stage amplifier) closely follows Q_{BQ} (only differ by a scale factor), large Q_{BQ} translates to large Q for the closed loop complex poles. The large

Q_{BQ} resulting from the small load capacitance leads to an under-damped system with large peak in the frequency response. Assuming that the compensation is designed to have Butterworth pole constellation for a load capacitance of C_L, the step response of 3-stage DFCFC amplifier is computed for load capacitances of C_L, $C_L/10$ and $C_L/100$. The plots of these step responses are shown in Fig. 3.11. Note that the step responses for under-damped systems display ringing when the input changes fast. Also, this behavior is different from that of a separate second order system with large Q poles. The difference is expected since the pole magnitude of the biquad increases (as well as the pole Q) with reduced load capacitance while the integrator bandwidth remains the same and provides high frequency attenuation.

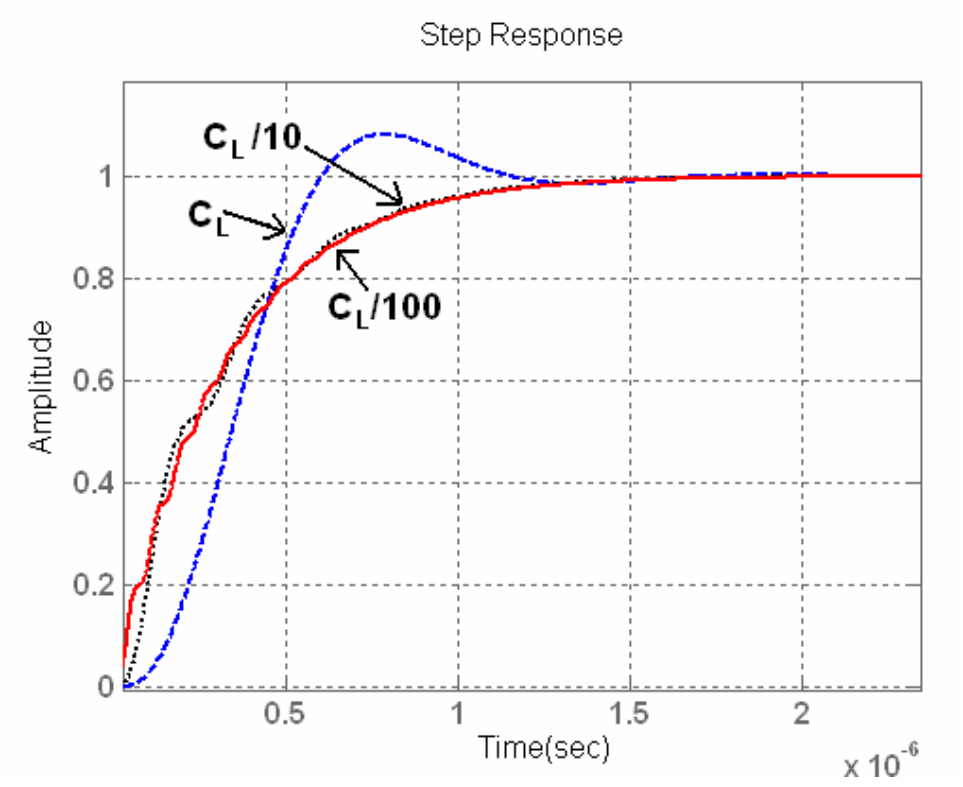


Fig. 3.11 Step response of DFCFC with Butterworth poles for load capacitance = C_L.

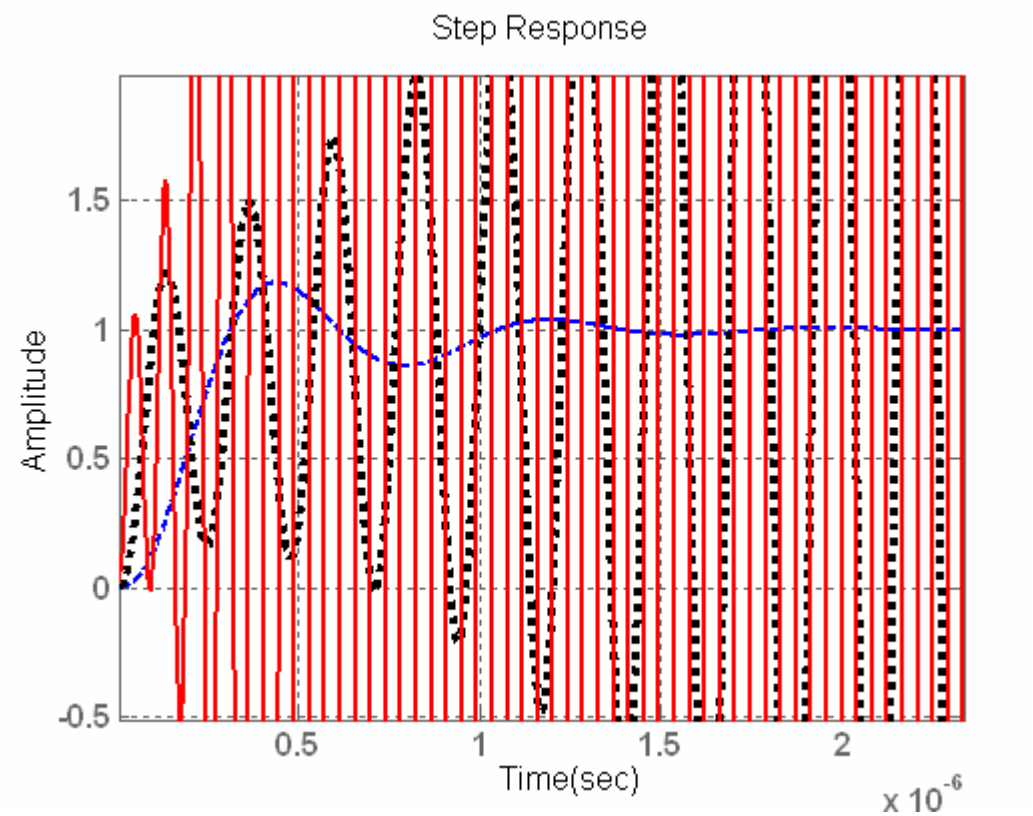


Fig. 3.12 Step response of DFCFC with 45degrees phase margin for load capacitance = C_L.

The problem gets worse when the DFCFC amplifier is designed for 45degrees phase margin using similar set of conditions as NMC (achieved by dropping the product Gm2/Cp3*Gm3/C_L from $2\omega_{CL}^2$ to 1.18 ω_{CL}^2 and setting the LHP zero at $\omega_{CL}/\sqrt{2}$ and the associated real pole at 5 ω_{CL}) . For small load capacitances, the high-Q poles are pushed to the RHP plane, yielding unstable systems. The step responses in Fig. 3.12 shows oscillations when C_L is dropped to $C_L/10$ or $C_L/100$ due to the RHP poles.

The effect of load capacitance variation can also be visualized in terms of pole locus as a function of load capacitance. Assuming that the compensation is designed to have Butterworth pole constellation for a load capacitance of C_L, the pole locus is computed as the capacitance is swept from C_L to $C_L/100$. The resulting pole locus for NMC and DFCFC schemes are shown in Fig. 3.13. In case of NMC, it is observed that for small values of C_L, the real pole tends to infinity and the complex poles tends to $\pi(1\pm j)$MRad/S. This can be viewed as a three stage amplifier asymptotically becoming a two stage amplifier with a 2nd stage loaded with capacitance Cc2 and 3rd stage acting as a high gain buffer in unity feedback. For DFCFC, as predicted in (3.12), the quality factor of the complex poles explodes for small values of C_L as the pole locus turns parallel to $j\omega$ axis.

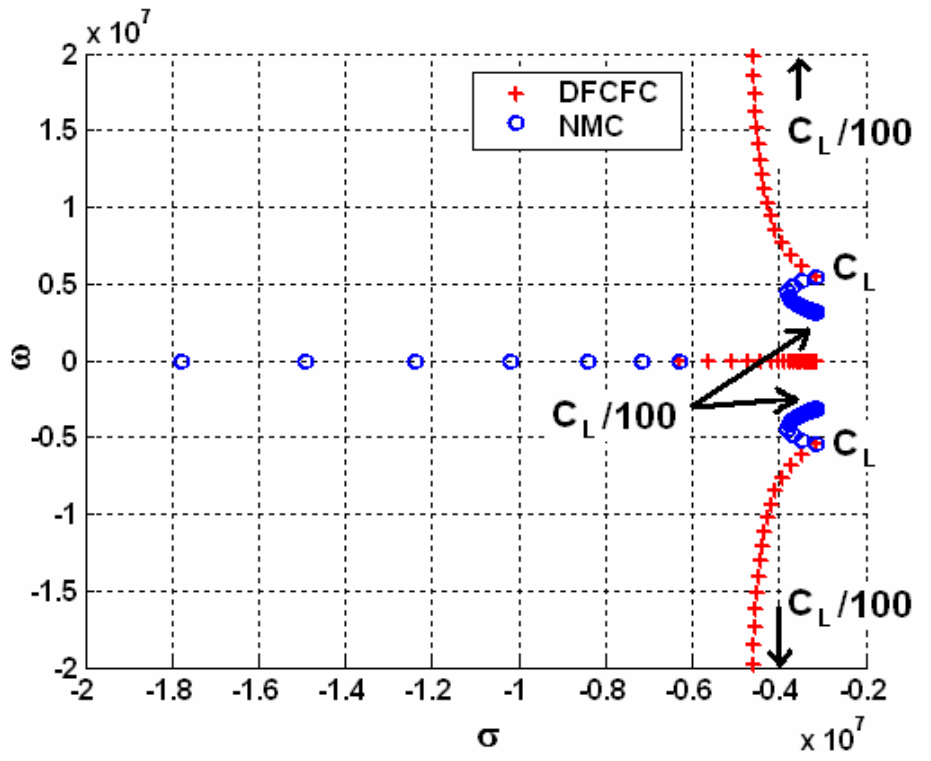


Fig. 3.13 Pole locus as load capacitance is varied from C_L to $C_L/100$ (Butterworth pole constellation for load capacitance = C_L).

Assuming that the compensation is designed for 45degrees phase margin (as explained before) the pole locus is computed as the load capacitance is swept from C_L to $C_L/100$. The resulting pole locus for NMC and DFCFC schemes are shown in Fig. 3.14. Due to the lower value of phase margin and the presence of the additional real zero and real pole, the pole locus follows a different path. In case of NMC, the complex poles turn real for small values of C_L, resulting in a system with three real poles. In case of DFCFC, this condition leads to a grave situation – the high-Q complex poles are pushed to the RHP plane (due to the excess phase in the loop), yielding unstable systems.

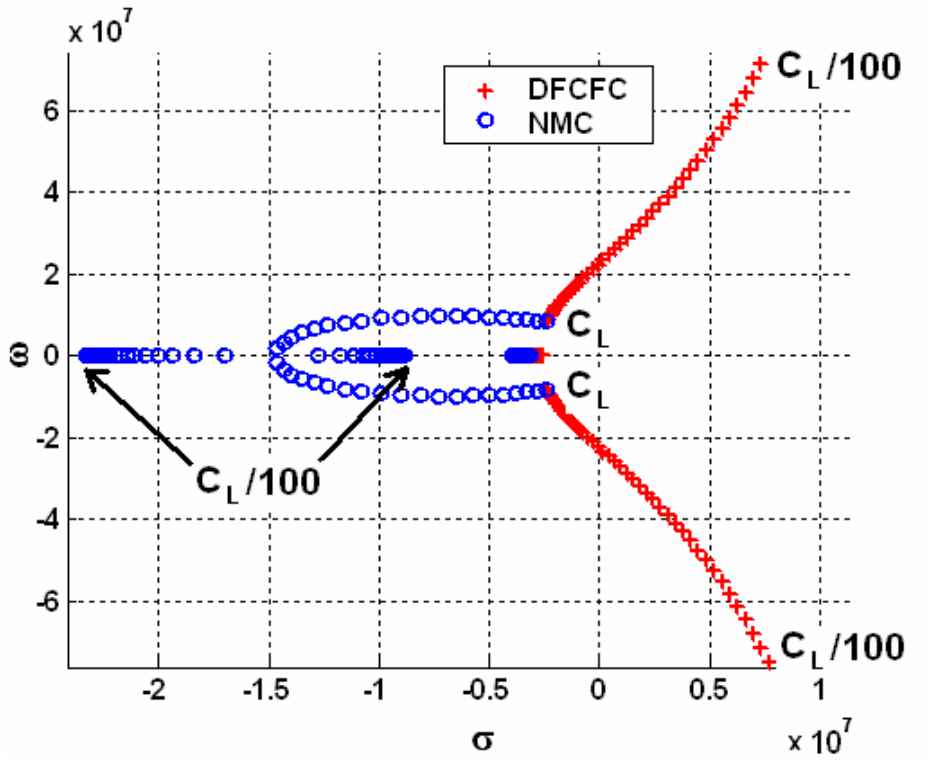


Fig. 3.14 Pole locus as load capacitance is varied from C_L to $C_L/100$ (45degree phase margin design for load capacitance = C_L).

3.3 Proposed Load-Capacitance-Aware Compensation Scheme

In the previous section, it was shown that the DFCFC scheme resulted in unstable systems as the capacitive load is reduced from the original design even by a modest factor of 10. From (3.8) and (3.12), it was predicted that the equivalent biquad formed by 2nd and 3rd stage in closed loop would have large Q_{BQ} when the load capacitance is dropped to small values. Equivalently, the damping factor ζ of the complex poles of the biquad is proportional to $\sqrt{C_L}$, which makes the system under-

damped for small load capacitance. In case of NMC, ζ is inversely proportional to $\sqrt{C_L}$, which makes it inherently immune to this problem. However, NMC suffers poor power efficiency and hence the need for a power efficient compensation scheme. Since the Q of the closed loop complex poles of the 3rd order system (3-stage amplifier) closely follows Q_{BQ}, it is desirable to have a compensation scheme that has a Q_{BQ} independent of C_L. Hence the aim of the new compensation scheme is to achieve constant Q_{BQ} (and hence constant ζ) and yet be more power efficient than NMC.

As explained in section 3.2.1, a separate damping network at the output of the second stage improves the power efficiency over NMC for large C_L. A damping network realizes a series RC network, where the damping resistor R_D provides the necessary loss and C_D is an equivalent capacitance that prevents the R_D from reducing the low frequency gain. The role of R_D is to provide the necessary loss in the biquad so that the Q of the complex poles can be fixed to a desired value. In order to achieve constant Q across C_L, the loss-bandwidth must be made inversely proportional to $\sqrt{C_L}$. In other words, R_D must be made directly proportional to $\sqrt{C_L}$ (see Fig. 3.15).

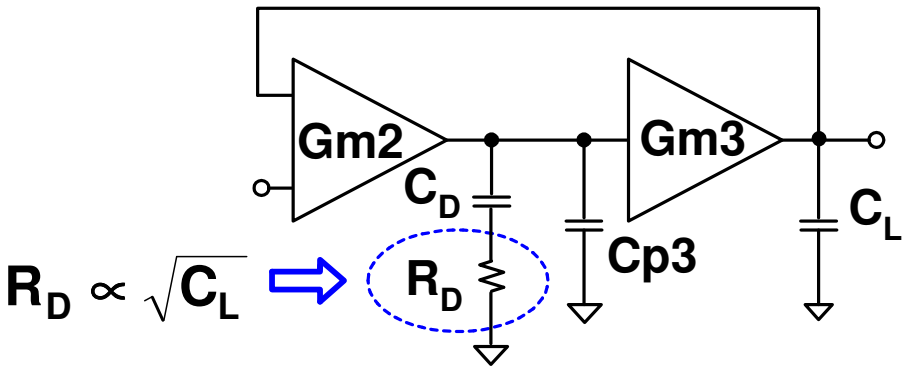


Fig. 3.15 Damping resistance requirement for constant Q complex poles.

Due to the obvious difficulties in realizing the square root dependence using linear circuits, a piece-wise approach is taken in the proposed scheme. Fig. 3.16 shows the architecture of the proposed amplifier. The damping circuit formed by GmD, R_D and C_D emulates a damping resistance of $R1 \approx 1/GmD$ and an equivalent capacitance of $Ceq1 \approx GmD*R_D*C_D$. The damping resistance provided by C_{D2} is $R2 \approx C_L/(Gm3*C_{D2})$, which provides the necessary small damping resistance in case of small C_L. The capacitances Ceq1 and Ceq2 are necessary to block the damping resistors at low frequencies (signal bandwidth) so that the gain of the amplifier stage can be maintained. At high frequencies, the impedance is dominated by the damping resistors, which governs the Q of the complex poles.

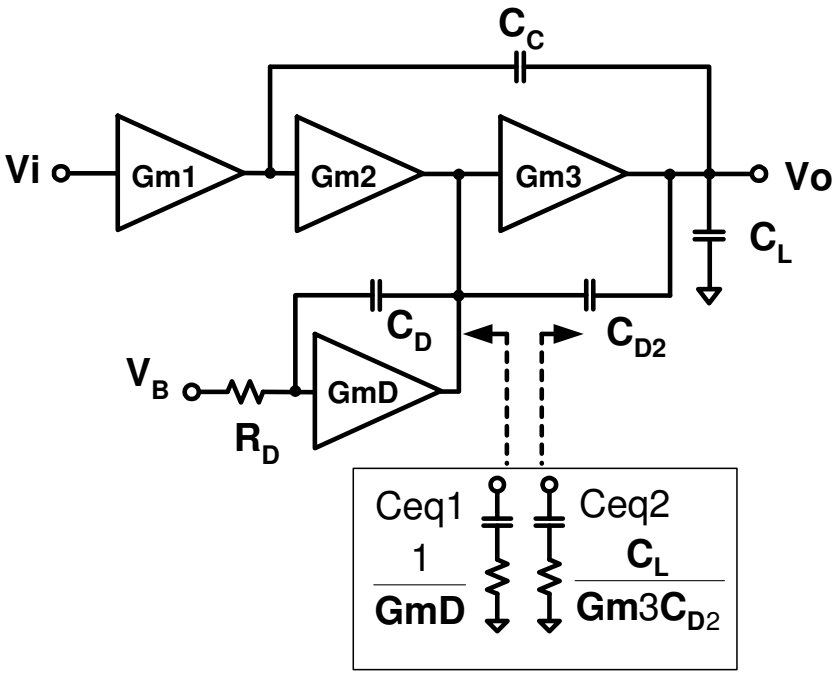


Fig. 3.16 Architecture of the proposed compensation scheme.

R1 and Ceq1 are derived later in section 3.4.3. Ceq2 and R2 can be easily derived by applying miller theorem on the admittance of C_{D2}. If the gain of the third stage can be expressed as $Gm3/(sC_L+go3)$, where go3 is the conductance at the output of the third stage, the grounded impedance looking in from third stage input is approximately give by $(go3+sC_L)/(sC_{D2}Gm3)$. This impedance can be separated in to two series components, namely Ceq2 and R2. The capacitor Ceq2 is equal to $C_{D2}*go3/Gm3$ and the resistor R2 is equal to $C_L/(Gm3C_{D2})$.

The idea can be easily understood from Fig. 3.17. It illustrates that the parallel combination of R1 and R2 provides a reasonable approximation of the desired proportional-to-$\sqrt{C_L}$ resistor. For large value of the C_L, GmD provides the necessary damping and for small values of C_L, the equivalent resistor seen through C_{D2} provides adequate damping. For intermediate values of C_L, both the damping resistance contributes to the loss. To have reasonable damping for a wide range of C_L, deviation from the ideal damping resistance is inevitable. Especially, the small and large C_L region would be somewhat over-damped and the intermediate region is somewhat under-damped.

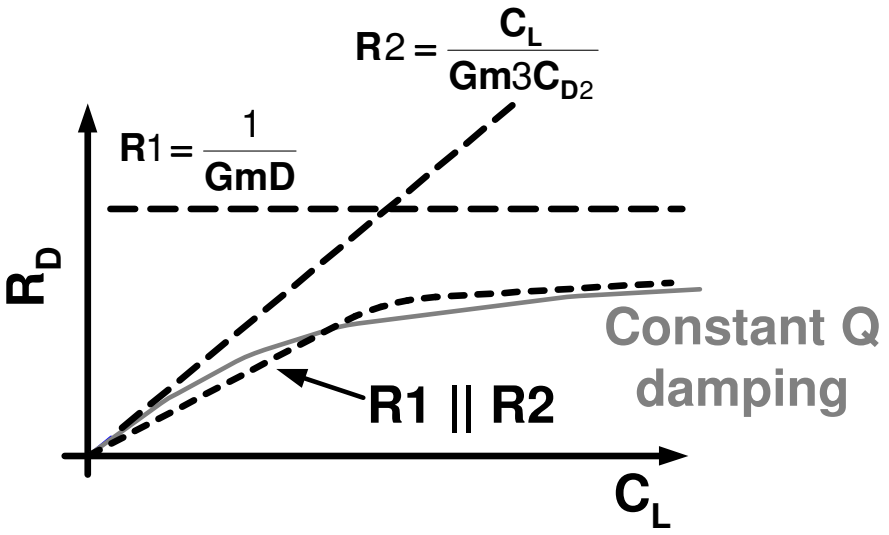


Fig. 3.17 Piecewise approximation for proportional-to-square-root resistor.

It is worth noting that C_{D2} is much smaller than the 2nd miller capacitor used by NMC. This is the case since C_{D2} is meant to provide damping for small C_L conditions in the proposed scheme whereas the 2nd miller capacitance need to provide damping even for the largest C_L. The step responses for various load capacitances are shown for the Butterworth case in Fig. 3.18. As seen in the plots, the proposed scheme provides gracious step response even when the load capacitance is lowered by 100 times.

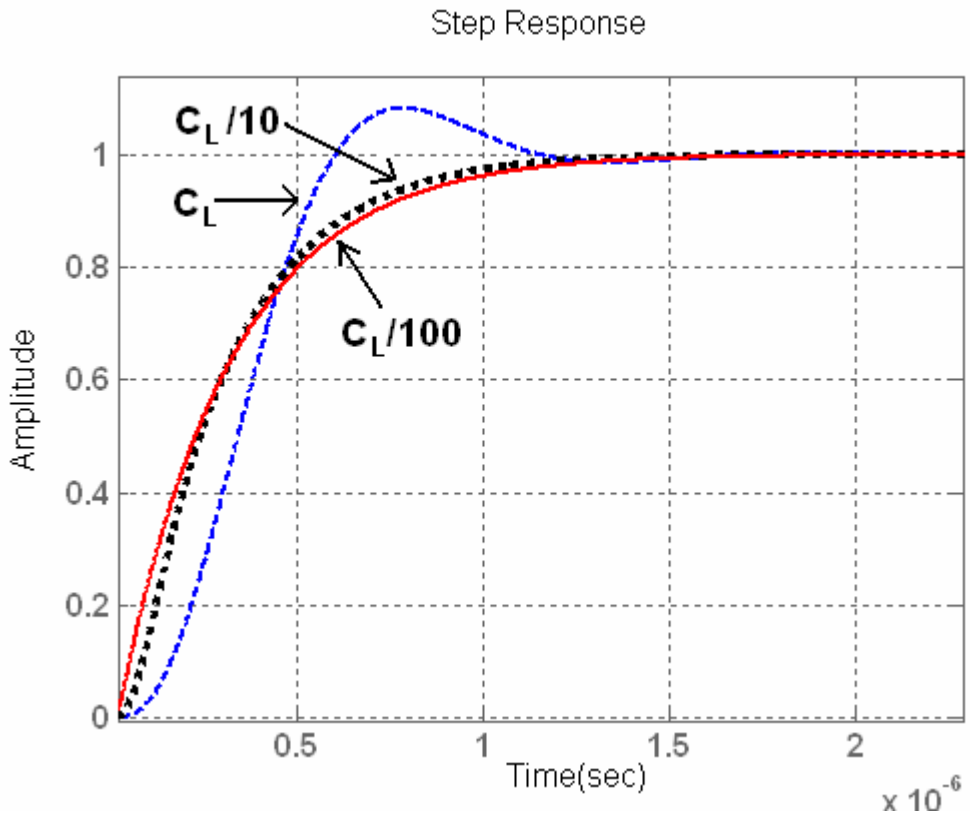


Fig. 3.18 Step response of proposed scheme with Butterworth poles for load capacitance = C_L.

The step responses are also computed for 45degrees phase margin design achieved by using 1.18 ω_{CL}^2 for Gm2/Cp3*Gm3/C_L and setting the LHP zero at $\omega_{CL}/\sqrt{2}$ and the associated real pole at 5 ω_{CL}. As it can be observed from the plots (see Fig. 3.19), the proposed scheme yields stable systems displaying step responses with minimal ringing. Additional ringing is due to lower phase margin (as seen in NMC) and is acceptable as a reasonable trade-off between phase margin and power consumption.

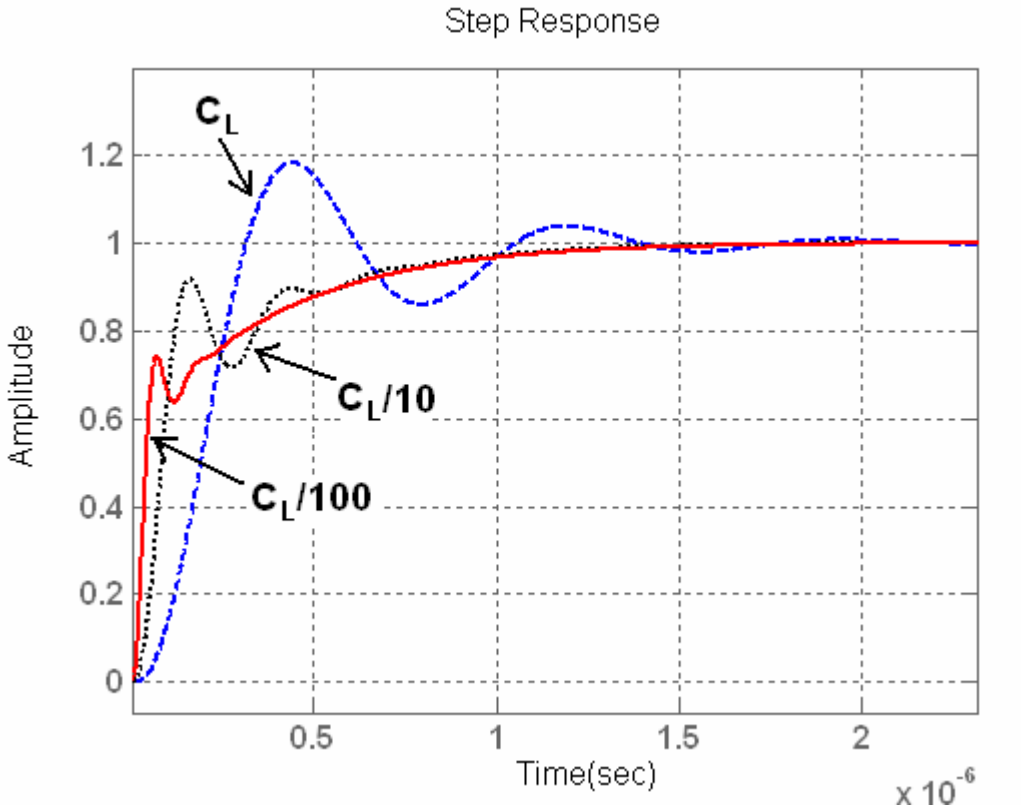


Fig. 3.19 Step response of proposed scheme with 45degrees phase margin for load capacitance = C_L.

The pole locus as a function of load capacitance is shown in Fig. 3.20 for the constant Q_{BQ} case, proposed scheme and DFCFC. The pole locus for the case of 45degree phase margin design is also shown in Fig. 3.21. From the pole locus, it is apparent that the proposed architecture provides necessary damping across a wide range of C_L and retains almost a constant Q factor. Due to the piece-wise approximation of the proportional-to-square-root resistor, the proposed structure shows some deviation from

the constant Q case. This is still acceptable since the step responses do not show ringing or oscillatory behavior.

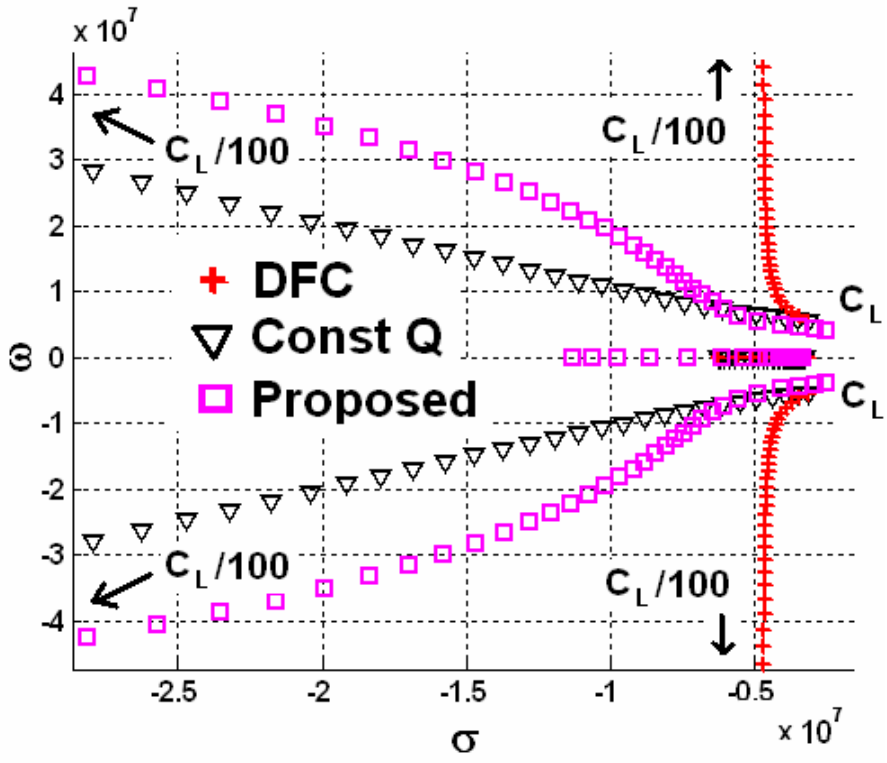


Fig. 3.20 Pole locus of proposed design as load capacitance is varied from C_L to $C_L/100$ (Butterworth pole constellation for load capacitance = C_L).

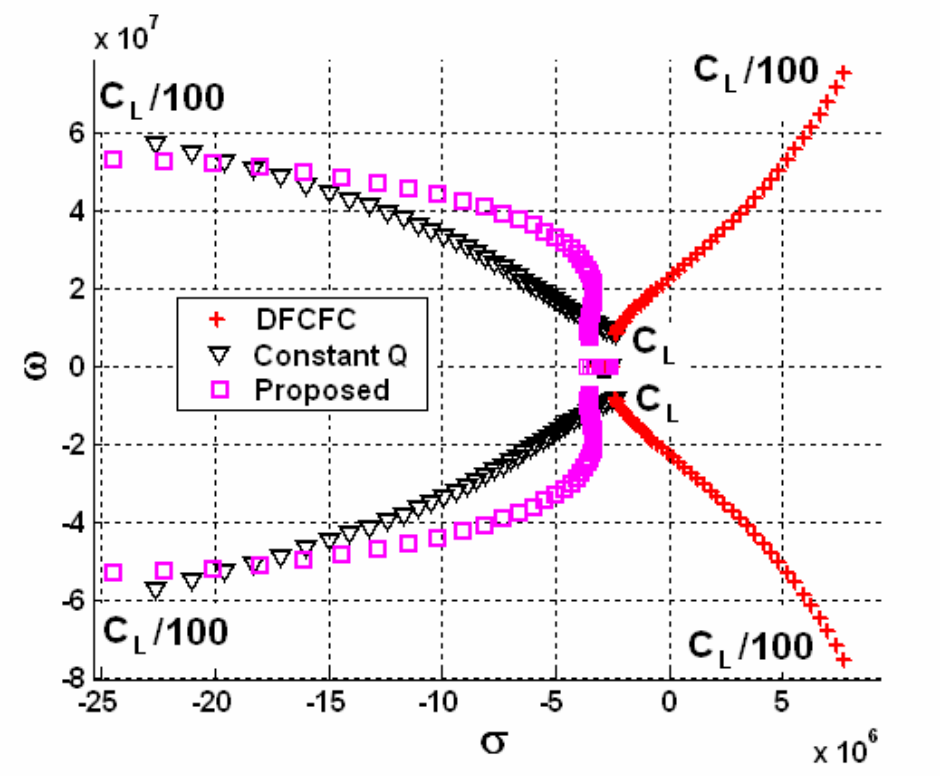


Fig. 3.21 Pole locus of proposed design as load capacitance is varied from C_L to $C_L/100$ (45degree phase margin design for load capacitance = C_L).

The effect of the load capacitance on the DFCFC and the proposed scheme can also be seen in the bode plots of the frequency response. Fig. 3.22 shows a family of bode plots for various values of C_L ranging from C_L to $C_L/100$ (logarithmically spaced) for the DFCFC scheme. Based on the phase response that increases with drop in magnitude response (which corresponds to RHP pole), it can be concluded that DFCFC scheme yields unstable systems for small values of load capacitance.

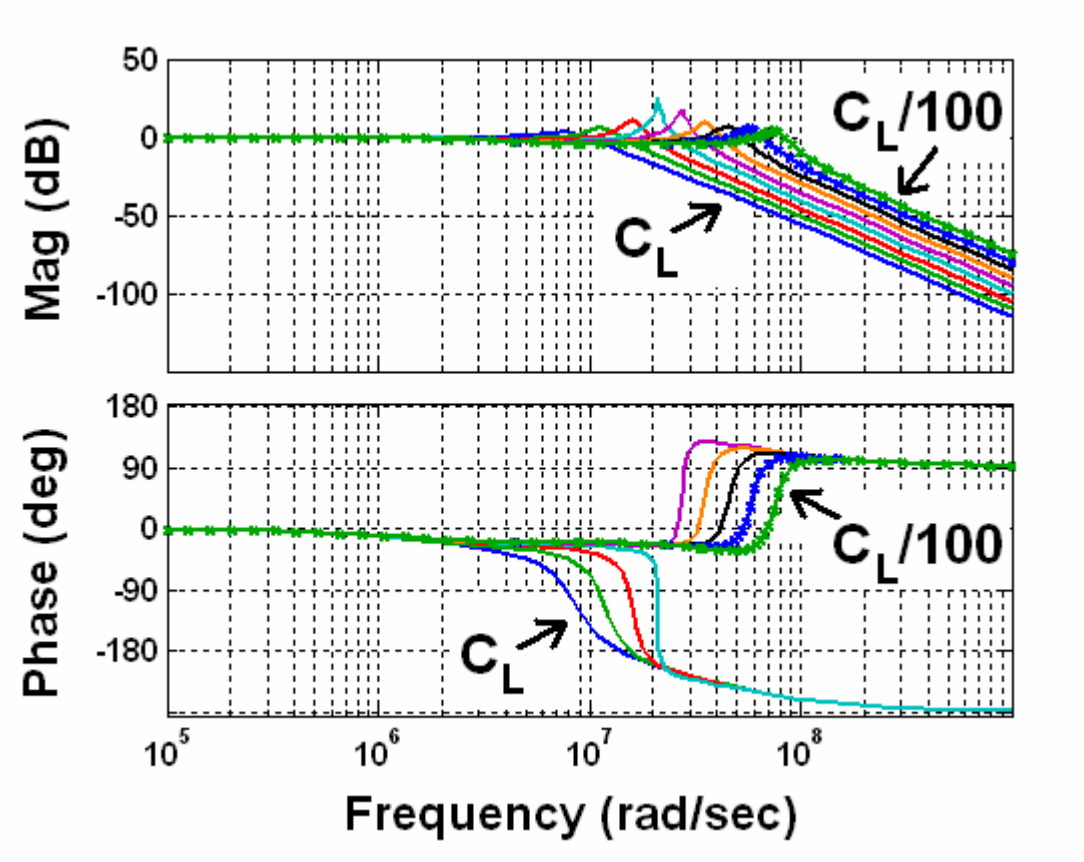


Fig. 3.22 Bode plot of DFCFC scheme as load capacitance is varied from C_L to $C_L/100$ (45degree phase margin design for load capacitance = C_L).

Fig. 3.23 shows a family of bode plots for various values of C_L ranging from C_L to $C_L/100$ (logarithmically spaced) for the proposed scheme. It is observed that the proposed scheme exhibits gracious frequency response for a wide range of load capacitance.

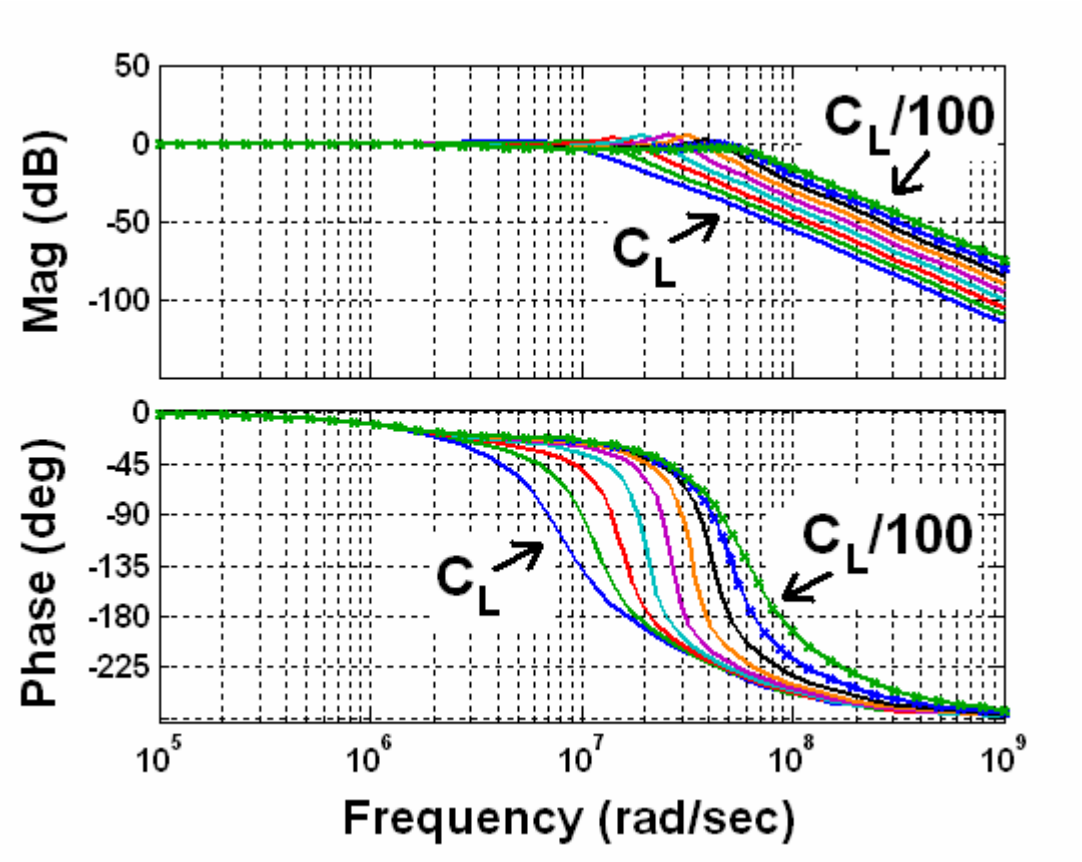


Fig. 3.23 Bode plot of proposed scheme as load capacitance is varied from C_L to $C_L/100$ (45degree phase margin design for load capacitance = C_L).

3.4 Implementation of the Proposed 16 Ohms Driver

The schematic of the 16Ω driver using the proposed architecture is shown in Fig. 3.24. The design considerations of each of the stages are explained in this section.

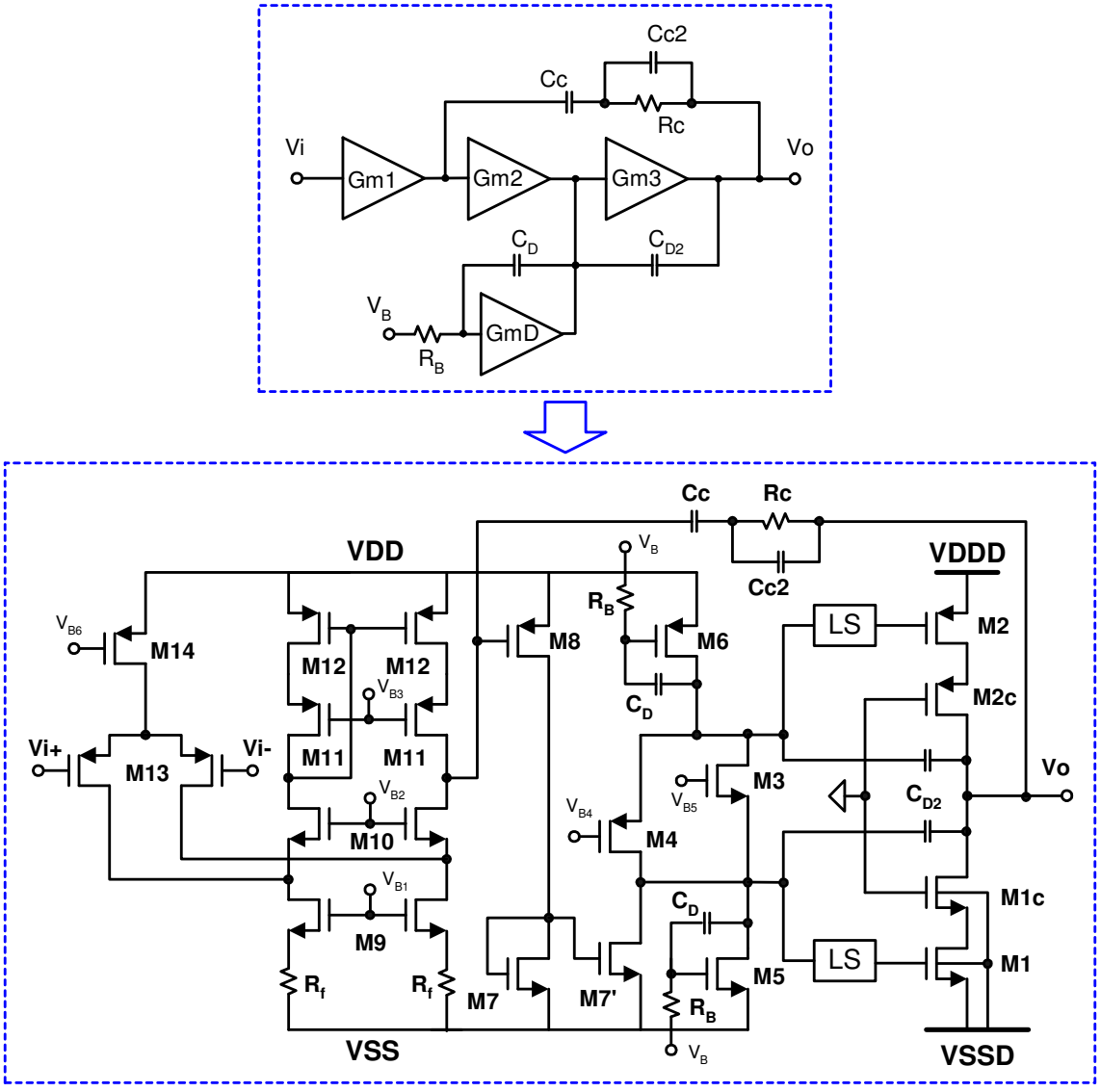


Fig. 3.24 Schematic of the proposed 16Ω driver.

3.4.1 First Stage (Gm1)

Gm1, the input stage, is realized using the folded cascode transconductor formed by M9-M14 (see Fig. 3.25). The input transistors M13 are carefully sized and matched to minimize the offset voltage and 1/f noise. The highest 1/f noise contribution of a PMOS-input folded cascode stage comes from the NMOS current source transistors (M9). A well-known technique of source degeneration (using resistors R_f in this case) is used to minimize the 1/f noise contribution of M9. The bias voltages V_{B1}, V_{B2} and V_{B3} are generated using standard low-voltage-cascode bias generators while V_{B6} is generated by a simple diode connected transistor. The bias currents of M13 and M12 are made equal to ensure equal slew rate for positive and negative transitions.

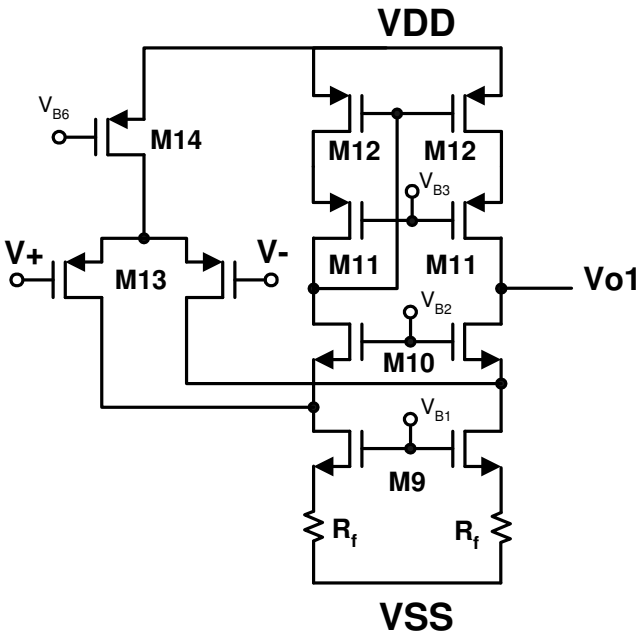


Fig. 3.25 Schematic of first stage of the driver.

3.4.2 Second Stage (Gm2)

Transistors M7, M7' and M8 realize the amplifier's second stage Gm2 (see Fig. 3.26). This is implemented as "positive Gm stage" in order to ensure negative feedback around second and third stage. The transconductance of M8 is augmented by a current mirror gain of 2 in M7, M7'. The output current of the second stage is pumped into the floating current mirror formed by M3 and M4. These floating current mirrors, described in [36], provide the necessary biasing for the class-AB output stage.

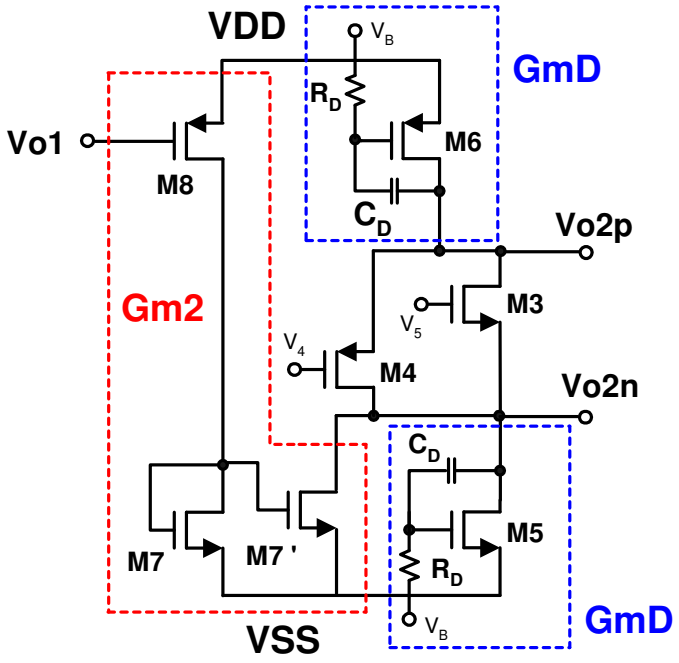


Fig. 3.26 Schematic of second and GmD stage of the driver.

3.4.3 Proposed Damping Stage (GmD)

Due to large swings associated with the class-AB output stage, the damping network is split such that M5 and M6 realize GmD for the NMOS and the PMOS path respectively. M6 also serves as a bias current source for Gm2. The gate of M5/M6 is biased using the resistor R_D and the drain node is connected directly to the Gm2 output. This enables the circuit to work under large swing conditions without pushing GmD into triode region. The damping circuit used in [30] is shown in Fig. 3.27(a). This is meant for an amplifier with predominantly capacitive load and it relies on the assumption that the voltage swings at the input of the transconductor used in the damping factor control block is small enough to not send the outputs to supply rail (this is equivalent to assuming that the last stage has sufficient voltage gain across swings). This assumption is not valid for low resistance drivers with class-AB output where the input swing of the output stage (Gm3) is intentionally kept large for power efficiency reasons. Hence, a damping network that works under large swing conditions is desirable. The proposed circuit, shown in Fig. 3.27(b), serves this purpose.

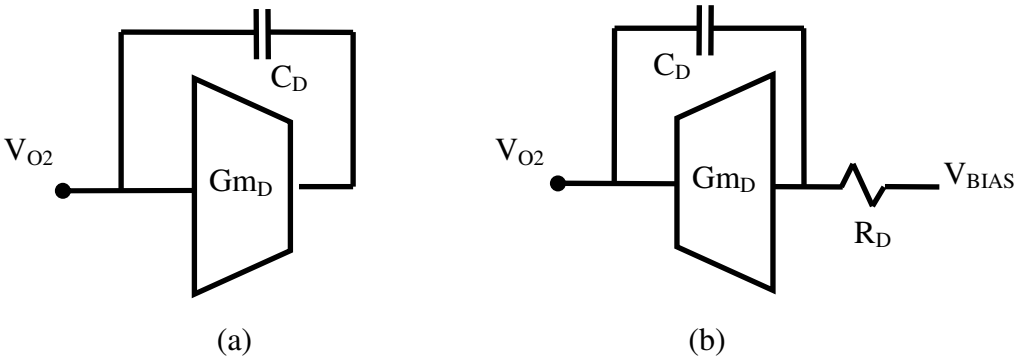


Fig. 3.27 (a) Damping network used in [30]. (b) Proposed damping network.

The input impedance of the network in Fig. 3.27(a) looking in from port V_{O2} is given by

$$\text{Zina} = \frac{sC_D + go_D}{sC_D(Gm_D + go_D)} \tag{3.13}$$

where gm_D is the transconductance of the OTAs, go_D is the output conductance of the OTAs. For the proposed implementation (in Fig. 3.27b), the input impedance is given by

$$\text{Zinb} = \frac{sC_D + G_D}{sC_D(Gm_D + G_D)} \tag{3.14}$$

where G_D is the conductance of the resistor R_D used to bias the OTA. Since go_D of the OTA in Fig. 3.27(b) can be combined with the output conductance of the node where the damping network would be tied, go_D is not considered a part of Zinb. From the expression for Zina, it can be seen that the network behaves like a capacitor of value $C_D(1+gmD/go_D)$ at frequencies well below go_D/C_D and as a resistor of value $1/Gm_D$ at frequencies much higher than that. Similarly, from the expression for Zinb, it can be seen that the network behaves like a capacitor of value $C_D(1+Gm_D/G_D)$ at frequencies well below G_D/C_D and as a resistor of value $1/Gm_D$ at frequencies much higher than that. Thus, the proposed circuit provides a damping network with a resistance of $1/(Gm_D+G_D)$ in series with an equivalent capacitance of $C_D(1+R_DGm_D)$. Note that the second stage of the overall amplifier (Gm2) drives the output of the damping stage rather than the input. This arrangement allows for large swings at the input of the output stage.

3.4.4 Output Stage (Gm3)

Fig. 3.28 shows the schematic of the output stage. In order to avoid a large DC blocking capacitor at the output, dual supply is used. The class-AB output stage and the level shifters (LS) are operated from a +/-1V supply while the rest of the amplifier uses +/-0.6V supply.

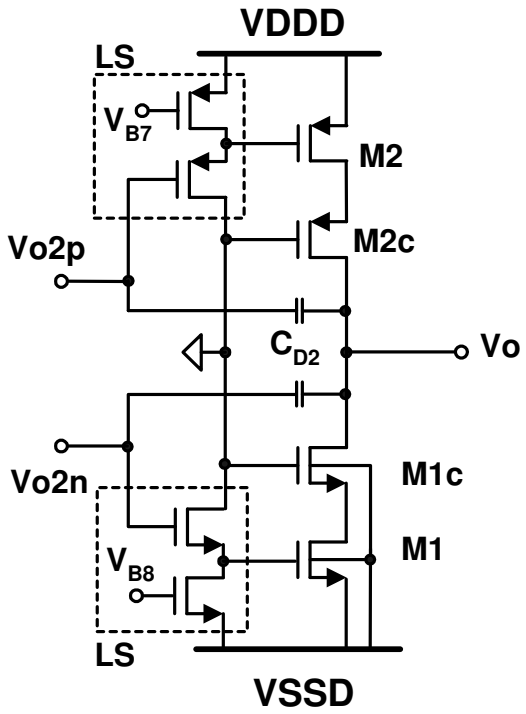


Fig. 3.28 Schematic of the output stage of the driver.

In order to prevent oxide breakdown in the gate-drain overlap region, cascoding technique is employed. When the output swings close to VDDD (VSSD), the output voltage is effectively shared between the VDS of the main transistor M1 (M2) and cascode transistor M1c (M2c). The cascode transistors (M1c, M2c) are biased such that

the VDS of the output transistors are maintained to be <1.2V under all swing conditions (see Fig. 3.29). The NMOS output devices are in triple well, which allows their sources and bodies to be 0.4V below the substrate voltage. The level shifters are implemented using source followers. The NMOS level shifter also makes use of triple well transistors to handle voltage levels below the substrate potential.

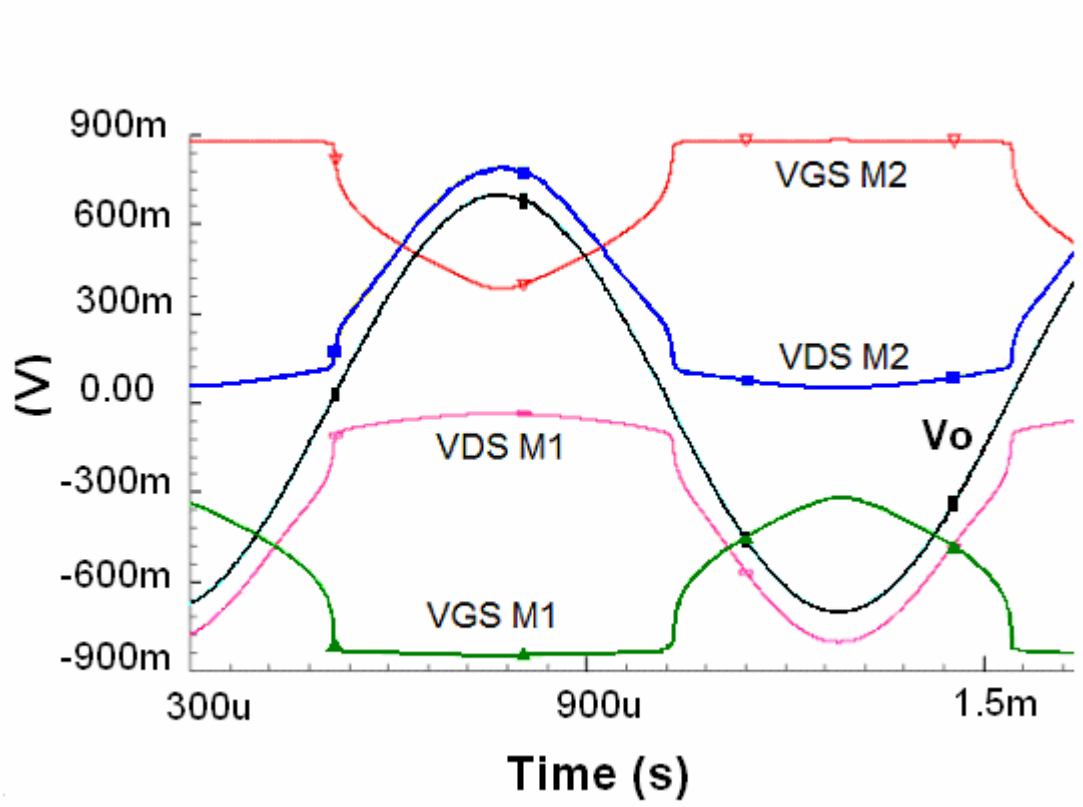


Fig. 3.29 Voltage swings across gate-source and drain-source of driver transistors.

3.4.5 Class-AB Bias Generation Circuit

The NMOS part of the class-AB bias generation circuit is illustrated in Fig. 3.30. The straight forward approach to generate the bias voltages V_{B4} and V_{B5} is to pump current into three diode connected copy-transistors with sizes proportional to transistors

M1, Mls and M3 connected in series (similar to the biasing scheme in [36] but for an additional diode connected transistor to account for the level shifter). This, however, results in extremely large mirroring error. The main source of the error arises from the fact that the drain voltage of main transistors in the driver (M1, Mlsb and M3) and their corresponding copy-transistors in the bias circuit experience a different drain voltage. The drain voltage difference results in mismatch between the threshold voltage of the main and copy transistor due to drain induced barrier lowering (DIBL) effect.

The proposed bias generation circuit takes into account the drain voltage of the output transistors as well as the floating-current-mirror transistors M3 and M4. This is achieved by diode connecting the copy transistor M1b and M3b via level shifters formed by Mlsb, Ib2 and M3b', Ib3 respectively. In case of M3b, the size of M3b' and Ib3 is designed so that the drain voltage of M3b matches that of M3. In case of M1b, the drain voltage is set by the sum of Vgs of M1b and Mlsb, which was close to the drain voltage of M1 in this design. If the drain voltage of M1b is larger than that of M1, a resistor may be inserted in series with the drain of M1b to absorb the excess voltage. Thus, the mirroring error is substantially reduced in case of the proposed circuit.

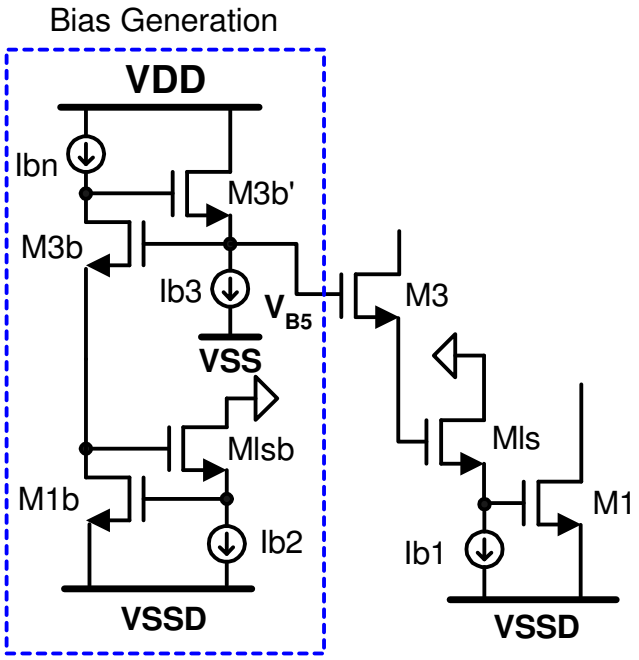


Fig. 3.30 Class-AB bias generation circuit.

3.5 Experimental Results

The driver prototype was fabricated in UMC 130nm CMOS technology and packaged in a SOIC20 package. The die photograph with markings of essential circuit components is shown in Fig. 3.31. The output stage is placed as close to the bond-pad as possible. The power supply and the ground lines of the output stage are double bonded to minimize parasitic resistance. The total layout area occupied by the driver is 0.1mm^2 (350µm x 290µm).

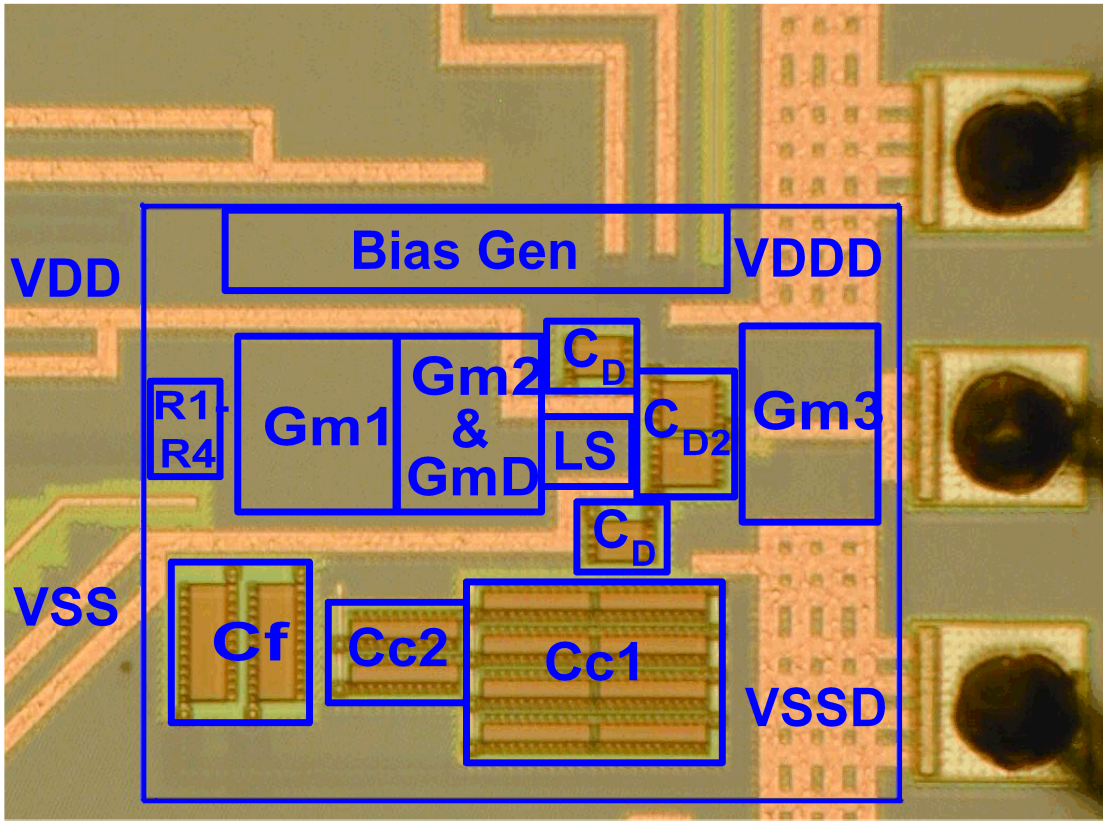


Fig. 3.31 Micrograph of the testchip.

3.5.1 Test Setup

A schematic of the test setup is shown in Fig. 3.32. Low noise, low distortion signal input was generated using the audio-precision system-one instrument. The differential signal generated by the instrument is directly applied to the input of the driver testchip. The single ended output from the PCB is directly connected to the input of the analyzer of the audio-precision system-one. The audio-precision system-one instrument is controlled by a computer via a APIB bus. The software that runs on the computer can not only provide a FFT for single input condition but also automatically sweep frequency and amplitude and make "sweep" type measurements.

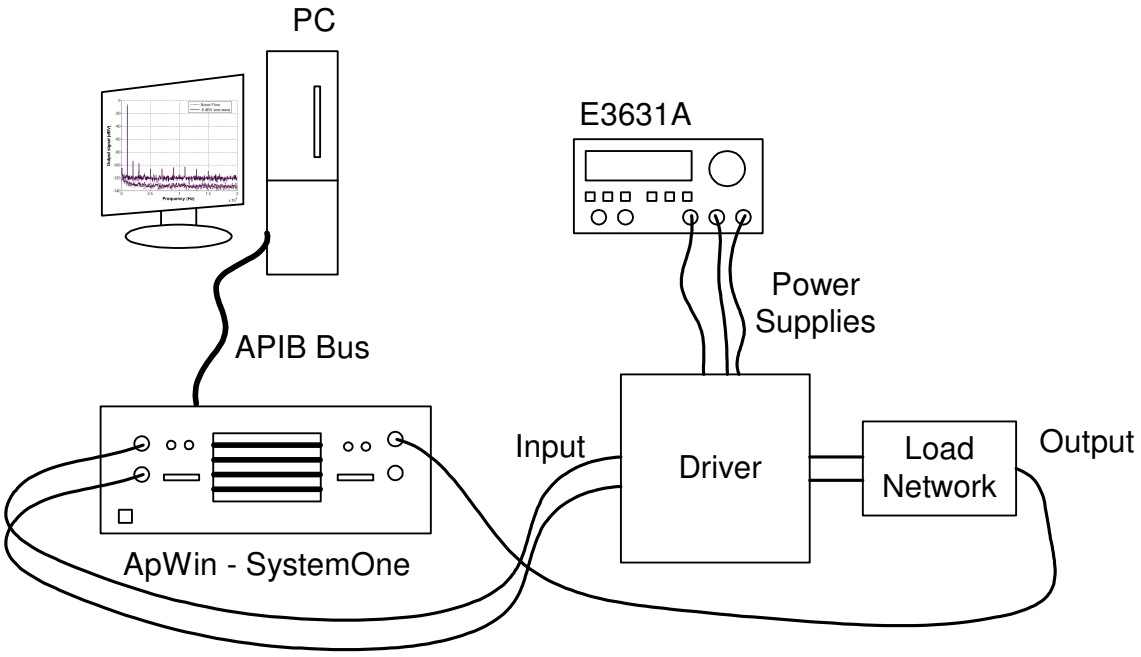


Fig. 3.32 Test setup for 16Ω driver.

The PCB used for the characterization is shown in Fig. 3.33. The output of the driver is loaded with the on-board load network. The load network consists of a series 10μH inductor and 16Ω resistor, and the load capacitor is varied for different test conditions.

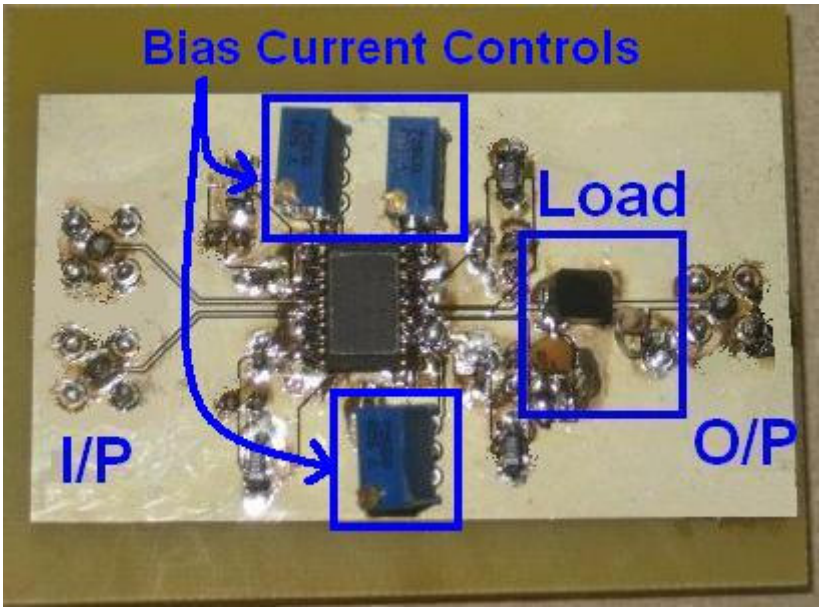


Fig. 3.33 PCB used for characterization of 16Ω driver.

3.5.2 Measurement Results and Comparison

The pulse responses of the driver measured for various load capacitors are shown in Fig. 3.34. Absence of ringing in all cases positively verifies the automatic damping control across a wide range of load capacitors. The minimum capacitance in the test setup is limited to 8pF by the probe capacitance. However, simulations confirm that there is no peaking/ringing behavior even in the case of 1pF load. The slew rate is

limited by the second stage to 0.4V/μS, which is more than what is required by a full-scale 20KHz signal. When fast changing input is applied, the second stage output momentarily charges in the opposite direction before returning to slewing state. This effect produces some cross over distortion for fast changing input and is more prominent for smaller load capacitance. This, however, is not an issue for signals in audio frequency range.

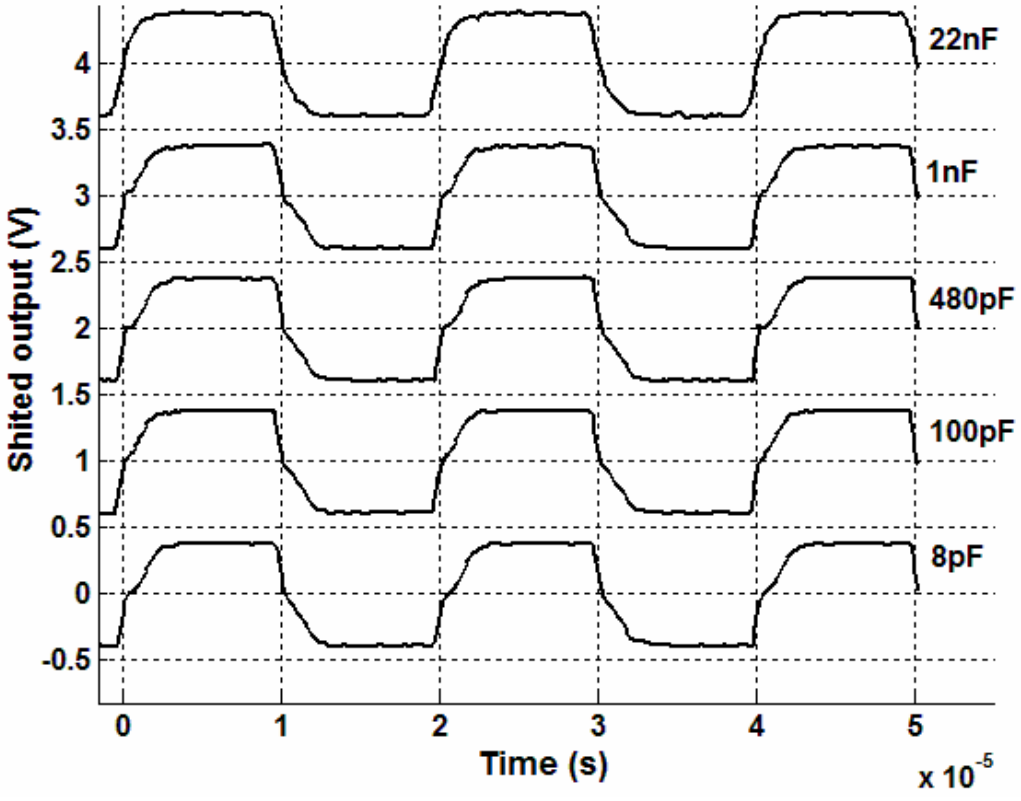


Fig. 3.34 Pulse response as load capacitance is varied from 8pF to 22nF.

Fig. 3.35 shows the measured FFT of 1.4Vpp sine-wave output and the noise floor with zero input condition under 1nF capacitor load in both cases. A maximum

THD of -84.8dB and a maximum un-weighted SNR of 92dB was measured with 1.6Vpp 1KHz tone. The noise and distortion performance was almost independent of load capacitance. Since the headphone outputs are always single-ended, dominant second harmonic distortion is inevitable. Higher harmonics are observed due to small cross-over distortion in the class-AB stage that is unsuppressed by the loop gain.

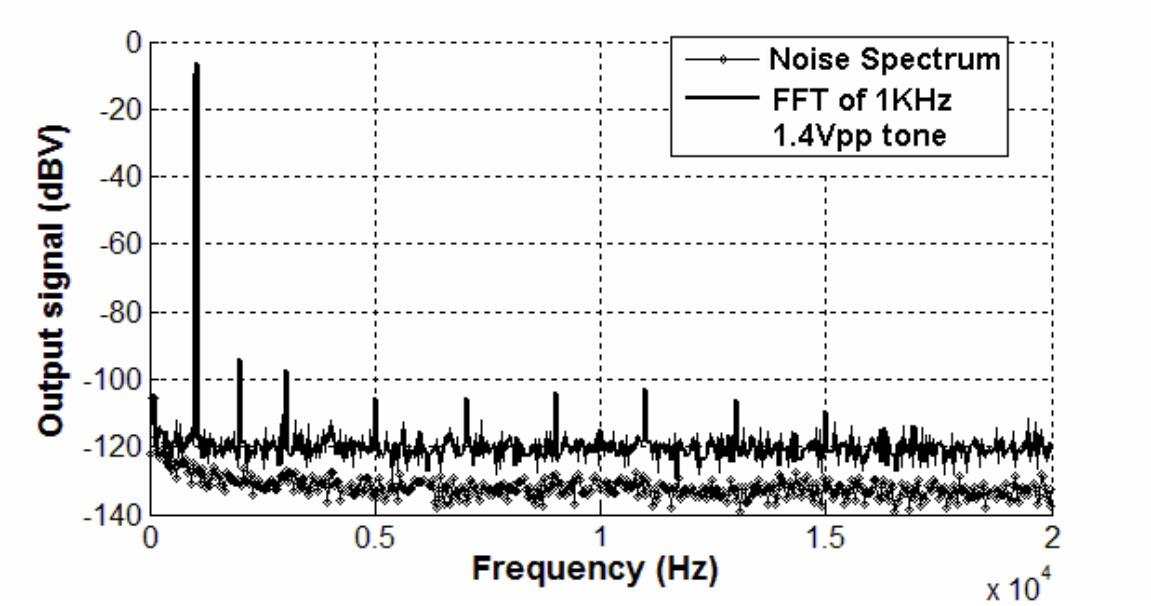


Fig. 3.35 Spectrum of 1KHz tone and noise.

Fig. 3.36 shows the THD+N as a function of output signal amplitude for a 1KHz tone and as a function of frequency for 1.4Vpp amplitude under 1nF capacitor load in both cases.

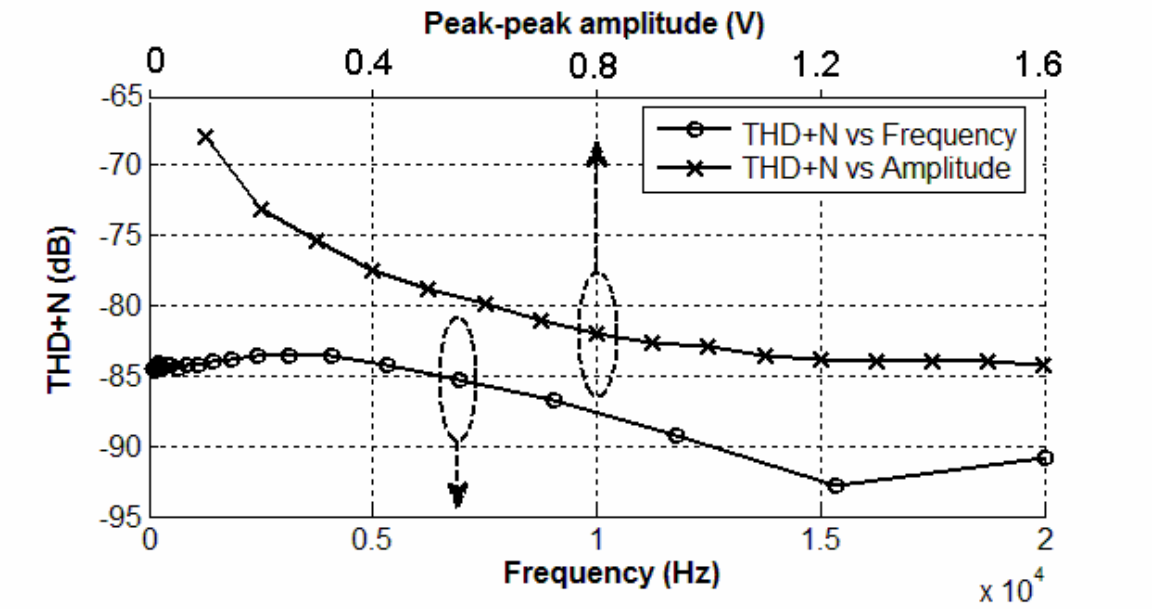


Fig. 3.36 THD+N as a function of frequency and amplitude.

For small output amplitude cases, THD+N are limited by the noise and hence the decreasing trend. As expected, the THD+N measurements did not show any appreciable change with load capacitance variation. The output stage and the bias generation loop consume a quiescent current of 400µA from +/-1V supply while the rest of the amplifier consumes 330µA from +/-0.6V supply.

A recently published NMC based class-AB 16Ω driver [27] and a 16Ω driver catalog product [37] is compared with the presented work in Table 3.2. The quiescent power of the proposed driver is about $1/10^{th}$ of that reported in [27] and [37]. Since the peak-to-average ratio of music is large (20-40dB), the quiescent power significantly affects the playback time. A figure of merit (FOM) defined as a ratio of the peak power

delivered to load to the quiescent power is included in the table. The total compensation capacitors used is less than half of that in [27], which translates to reduced area.

Table 3.2 Comparison of measurement results with state-of-the-art.

Parameter	[37]	[27]	This work
Technology	-	65nm CMOS (1.2V devices)	130nm CMOS (1.2V devices)
Capacitance load	0-300pF	0-12nF	1pF-22nF
Output stage supply	3.0V	2.5V	2.0V
Output voltage	2.50Vpp	1.85Vpp	1.60Vpp
THD+N @ max. output	-90dB	-68dB	-84dB
Total compensation capacitance	-	35pF	14pF
Quiescent power	12.0mW	12.5mW	1.2mW
FOM	8.1	4.3	33.3

3.6 Summary

A Simple and intuitive method to analyze 3-stage amplifiers was described. A load capacitance aware compensation scheme was developed. A 16Ω headphone driver design that can handle 1pF-22nF of load capacitance by using the proposed compensation scheme was discussed. Experimental results from the prototype that consumes 10 times lesser power than state-of-the-art was shown. Since the design uses only the 1.2V core devices, it can be easily ported to smaller feature size technology.

3.6.1 Future Work

The idea of automatically adjusting for several decades of variation in load capacitance by some means of transforming the impedances was presented in this work. As it is true in many cases, there are other areas with similar problems where this idea can be applied. For instance, a linear voltage regulator that allows the user to choose a wide range of de-coupling capacitors. In this case, the specification on "minimum required de-coupling capacitance" can be eliminated. Other possible application is a power efficient general purpose low voltage operational amplifier that can handle a wide range of load capacitance.

CHAPTER IV

A 20MHz SIGNAL BANDWIDTH 68dB DYNAMIC RANGE CONTINUOUS TIME ΔΣ ADC BASED ON TIME DOMAIN QUANTIZER AND FEEDBACK ELEMENT

4.1 Introduction

Recent developments in mobile computing and wireless internet have led to exponential growth in demand for portable computers and smart phones that needs low-cost, low-power WLAN using 802.11g/n standards. The low-cost, low-power digital computing required by these gadgets is facilitated by process scaling that follows Moore's law and is expected to continue to 10nm physical gate length [38]. However, integration of efficient baseband circuits in these process technologies remains a challenge. The focus of this chapter is development of new ADC architecture for nanometric technologies. A prototype 20MHz bandwidth, 10bit ADC designed in 65nm digital CMOS technology using the proposed architecture will be described in detail.

Delta-sigma architecture has attracted a lot of attention as digital-friendly architecture for ADC since a substantial part of the signal processing is performed in the digital domain. This architecture enables a few integrators, a comparator and a digital filter to perform analog-to-digital conversion. Fig. 4.1 shows a block diagram of a 1-bit delta-sigma modulator. In this architecture, the component matching is hardly a concern since both the 1-bit DAC and 1-bit quantizer are inherently linear. Digital filters are not only easily amenable to process scaling but also progressively consume less power for a given dynamic range as the technology feature scales down. Low-cost and low-power

digital signal processing coupled with analog circuits that need minimal or no matching requirements makes delta-sigma an ideal architecture for nanometric technologies.

Application of a 1-bit delta-sigma modulator to WLAN ADC problem faces several obstacles. High over-sampling ratio (OSR), needed to meet the signal to quantization noise ratio (SQNR), increases the bandwidth and the settling speed requirement of the integrators as well as the switching frequency of the decimation filter. This leads to increased power dissipation in integrators as well as the decimation filters. On the other hand, achieving the required SQNR with low OSR and higher order filtering is limited by over loading effects and stability of the modulator [39]. Cascade approach can alleviate the stability issue [40], however, leakage due to mismatch between analog and digital blocks remains a problem. Calibration is required to eliminate this mismatch, especially for the continuous-time modulators, which is undesirable for low-cost systems. Due to these constraints, 1-bit delta-sigma modulator is not an ideal choice for applications with high signal bandwidths like 20MHz.

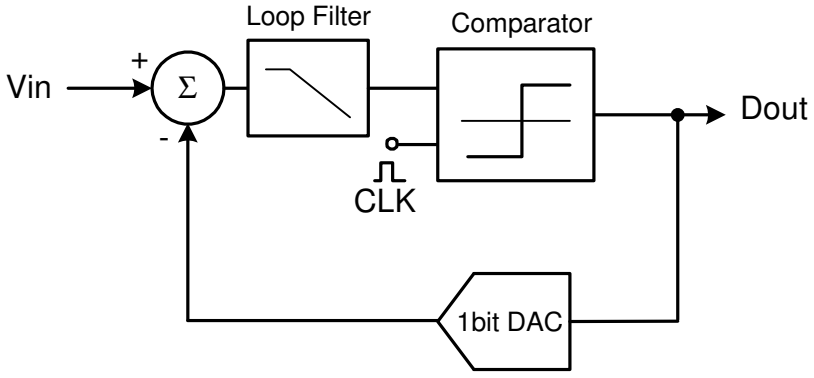


Fig. 4.1 Single-bit delta sigma modulator.

One of the alternatives to improve the SQNR without increasing the switching frequency is to use a multi-bit quantizer and a multi-bit feedback DAC instead of a 1-bit quantizer and a 1-bit feedback DAC. In this approach, the noise-shaping gain required in the loop filter is lesser due to the smaller quantization noise associated with the multi-bit quantizer. Multi-bit architecture has been successfully used in [41] to design a 20MHz bandwidth ADC using 0.13um technology. However, the "digital friendly" advantages of the 1-bit architecture are lost in the multi-bit solution. Specifically, the feedback DAC linearity (element matching) significantly affects the performance of the ADC since it directly adds error to the input summer and is not noise shaped. Hence, the performance of the ADC cannot be better than that of the feedback DAC. A slew of dynamic element matching (DEM) techniques were proposed to tackle this problem [42-43]. However, the first order shaping of mismatch error provided by these techniques proves to be inadequate in case of low OSR designs. A robust solution is preferred for nanometric technologies where matching of devices is more problematic due to gate leakage mismatch [44].

It is important to note that the modulator with continuous time loop filter offers several advantages over discrete time delta-sigma at high signal bandwidth [39]. Firstly, unlike discrete time modulator, sampling occurs after all the integrator stages (at comparator input) rather than at every integrator stage. This reduces the thermal noise contribution of first (and possibly second) integrator stage since the high frequency thermal noise is substantially filtered out before sampling and the consequent aliasing.

This in turn translates to power reduction in integrators. Secondly, due to sampling occurring at the end of the loop filter, the internal waveform transients and hence the settling requirements of the integrators are relaxed. Thirdly, the loop filter also provides anti-alias filtering for the input signal, which is absent in case of discrete-time modulators. Finally, implementation of good switches poses a significant problem in deep-submicron technology, especially in case of low-leakage flavors of the technology that is preferred for the Digital Signal Processor (DSP). The continuous time approach eliminates the switches, thereby completely avoiding this problem. For these reasons, the proposed ADC is designed with continuous time loop filter rather than a discrete time filter.

In order to overcome the shortcomings of the nanometric technologies and at the same time take advantage of the precise timing edges available in these technologies, a time to digital converter (TDC) based approach for multi-bit quantization and feedback is investigated in this work. A brief overview of previous works on TDC is presented next.

4.1.1 Previous Work on Time to Digital Converters

Time to digital converter was originally proposed to measure single-shot pulses in nuclear experiments [45]. The schematic of a basic time to digital converter is shown in Fig. 4.2. The input propagates through a cascade of digital buffers, whose outputs are fed to the D input of an array of flipflops. The stop pulse latches the states of these

flipflops. The output of the flipflops provides a thermometric coded output that represents the time duration between start and stop pulse.

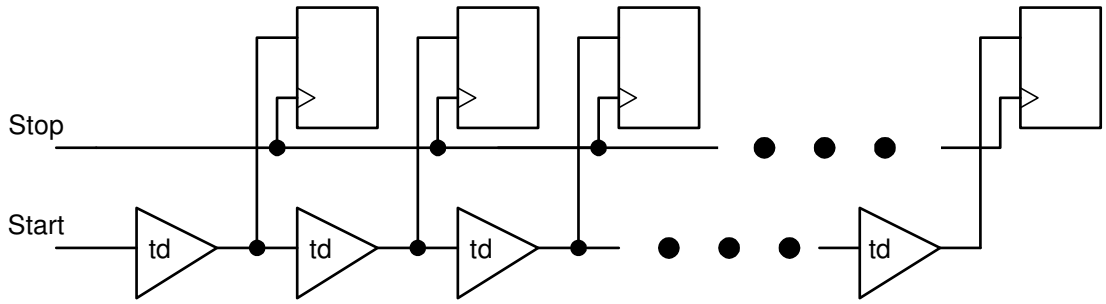


Fig. 4.2 Basic single-shot TDC.

It is readily apparent that the time resolution of this single-shot TDC is limited to the delay of one digital buffer. In order to overcome this limitation, several solutions were proposed. The approach used in [46] makes use of the idea of "vernier" delay element chain to realize finer time resolutions. The schematic of the vernier delay chain based TDC is shown in Fig. 4.3. The time delay of the buffers in the delay chain for start pulse (t1) is designed to be slightly greater than that of the buffers in the delay chain for stop pulse (t2). With this arrangement, the flipflops register logic 'HIGH' until the time the stop pulse "catches up" with the start pulse. Thus, the output thermometric code represents the number of delay difference (t1-t2) rather than the delay itself. Note that the number of delay elements and the flipflops, in this scheme, has increased proportional to the improvement in the time resolution. The TDC reported in [46] that uses this approach is shown to achieve a time resolution of 30pS in 0.7um technology, which is significant lower than the delay of the digital buffer in this technology.

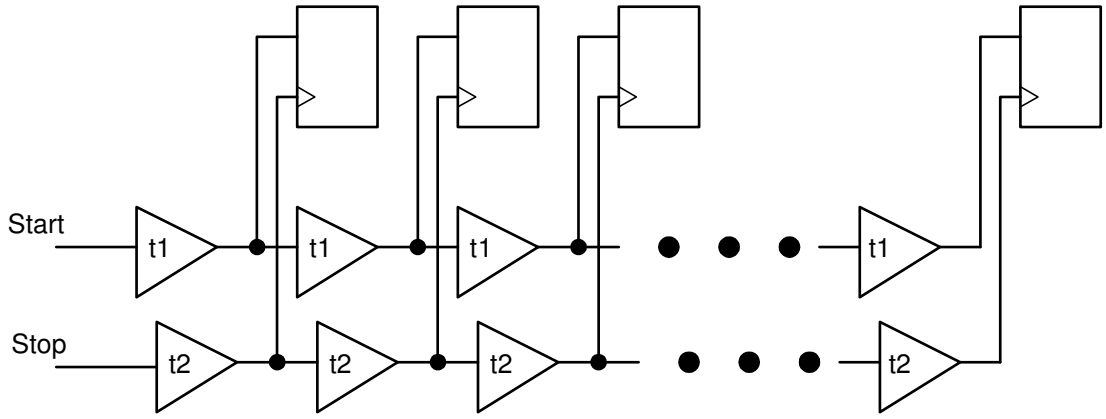


Fig. 4.3 Vernier delay line based TDC proposed in [46].

Another approach uses a technique called “pulse shrinking” [47]. The schematic of the TDC using this approach is shown in Fig. 4.4.

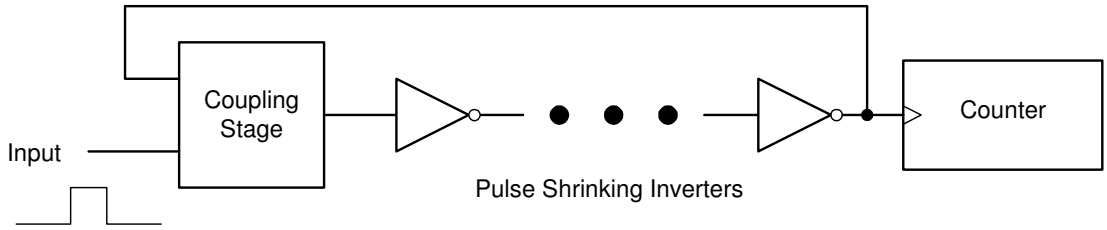


Fig. 4.4 Pulse shrinking inverter based TDC reported in [47].

The input pulse is propagated through “pulse shrinking inverters” that are designed with three digital inverters in cascade with the middle one having skewed NMOS/PMOS strength. The skewed strength results in the width of the pulse to shrink. The approach is to count the number of these pulse shrinking inverters that are required

to completely disappear the pulse. This is done by an arrangement that cycles the pulse through a chain of pulse shrinking inverters while a counter measures the number of cycles required to disappear the pulse. The counter output represents the width of the pulse.

A recently reported approach uses a residue amplification based approach to enhance the time resolution [48].

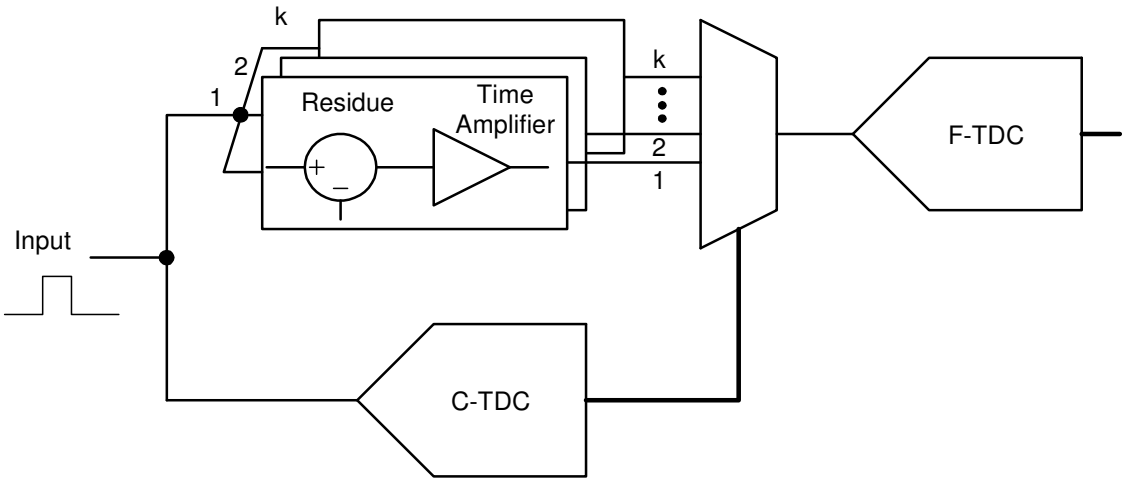


Fig. 4.5 Residue amplification based TDC proposed in [48].

The input pulse is simultaneously fed to a coarse TDC (C-TDC) and an array of residue generators (see Fig. 4.5). Since the time residues cannot be stored, all possible residues are calculated and the relevant residue is multiplexed to a fine TDC (F-TDC) after amplification. The amplification of the residue is performed by using a “time amplifier”. The “time amplifier” essentially makes use of the metastability behavior of a SR latch where the latch exhibits a large clock-to-Q delay when the data and the clock

edges occur very close. Once the residue is amplified, it can be passed on to the FTDC (which has the same resolution of the CTDC) to realize finer time resolution.

All of the approach that improves the time resolution needs some kind of calibration and also has latencies that are more than an order of magnitude larger than the time resolution itself. Although this is acceptable for single-shot TDC, it is undesirable if the TDC needs to process steady stream of pulse inputs occurring at fast rates. Also, as the technology scaling increases the speed of the digital gates, the raw time resolution of the delay chain improves. Recognizing this fact, a TDC based on pseudo differential delay elements was proposed in [49]. The architecture is similar to the basic single-shot TDC but there are two sets of delay elements serving to generate pseudo differential time reference for differential flipflops. The differential circuits are used to avoid any duty-cycle distortion of the input clock. Due to small gate delay in 90nm CMOS technology, this TDC achieves 20pS time resolution without employing the special techniques used by other architectures.

A summary of various techniques discussed in this section is presented in Table 4.1. Note that the time resolution of 20pS is reached in case of [49] without any resolution enhancing techniques. This primarily attributed to speed improvement that is achieved due to technology scaling and it is expected that the performance of the TDC improves along with the technology scaling.

Table 4.1 Summary of various TDC techniques.

Reference	Technique	Technology (μm)	Time resolution (pS)
[46]	Vernier delay lines	0.7	30
[47]	Pulse shrinking	0.8	20
[48]	Residue amplification	0.09	1.25
[49]	Raw performance	0.09	20

4.2 ADC Architecture with Time Domain Quantizer and Feedback Element

One of the main challenges in implementing high-speed and high-precision analog functions in nanometric digital CMOS technology is the low supply voltage [50]. An important consequence of using low supply voltage is the reduced signal voltage swings. This in turn demands smaller noise levels for a given signal to noise ratio (SNR) as compared to a circuit with larger signal swings. As illustrated in Table 4.2, low supply voltage results in increased power consumption and large capacitance area (to check the thermal noise) for analog circuits. One of the ways to tackle this problem is to make use of the time resolution rather than relying on voltage resolution to represent high dynamic range signals. This approach has recently gained a lot of interest [51-52] due to the availability of fine time resolution in scaled CMOS technologies.

Table 4.2 Scaling of various parameters with supply scaling under constant SNR.

Parameter	Supply voltage =VDD	Supply voltage =VDD/K
Voltage Swing	Vpp	Vpp/K
Noise power	Vn^2	Vn^2/K^2
Capacitance	C	$C*K^2$
Frequency of operation	f	f
Transconductance	Gm	$Gm*K^2$
Current	ID	$ID*K^2$
Power	VDD*ID	VDD*ID*K

4.2.1 Signal Representation in Time Domain

There are three common ways of signal representation that is being used in electronic circuits. They are Continuous Time Continuous Amplitude (CTCA), Discrete-Time Discrete Amplitude (DTDA) and Discrete Time Continuous amplitude (DTCA). As explained in [53], using time resolution of digital waveform to represent signals correspond to the fourth way of signal representation, which is, Continuous Time and Discrete Amplitude (CTDA). One of the main benefits of CTDA approach is that the power dissipation follows the CV^2f rule, where the power dissipation of a digital gate driving a load capacitance C and switching between voltages 0 to V at a rate of f is given by CV^2f . Due to the fact that the signal swing is in time domain, the supply voltage is virtually uncoupled from SNR. This makes low supply voltage advantageous in terms of

power unlike the signal that is continuous in amplitude domain. It is important to note that although the dynamic range relies on fine time resolution, the circuit switching frequency is still a function of input signal frequency. This makes the power dissipation signal activity dependent [54], which helps reduce the average power consumption of the circuit. Since the signal representation is in time domain, the only noise of concern is due to timing jitter. The timing jitter and corresponding SNR for a unity gain buffer can be calculated with the aid of Fig. 4.6.

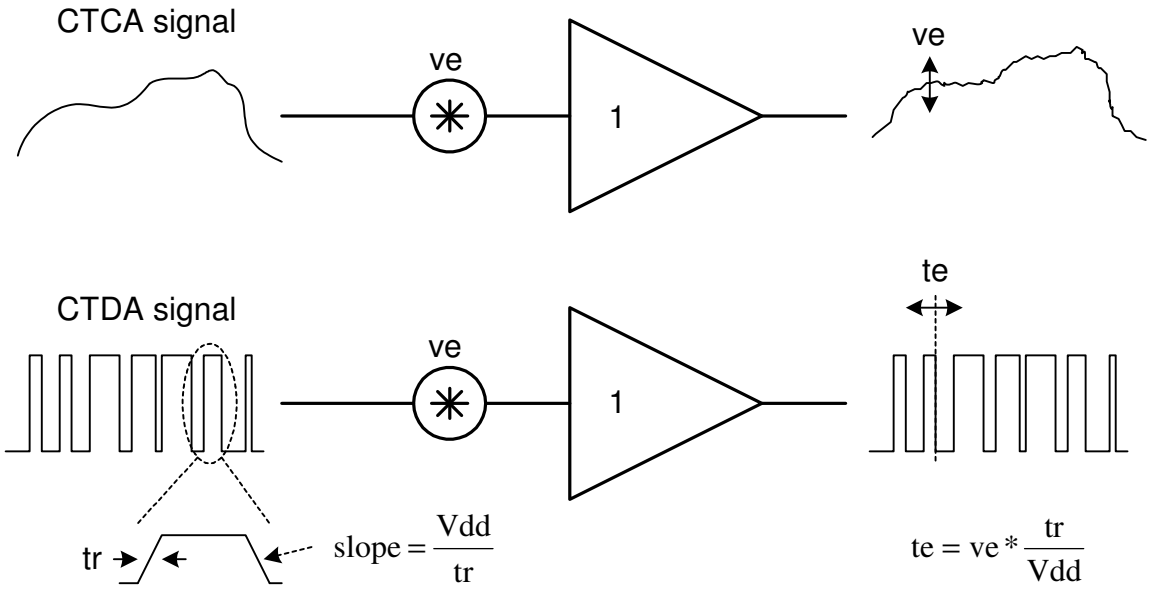


Fig. 4.6 Translation of voltage noise to timing noise.

Assuming that the slope of the rising/falling edge of the digital waveform is given by Vdd/t_r, where Vdd is supply voltage and tr is the rise/fall time and the standard

deviation of the voltage error (ve) is denoted as v_σ and the standard deviation of the timing error (te) is denoted as t_σ can be expressed as

$$t_\sigma = \frac{v_\sigma}{dv/dt} = \frac{v_\sigma * t_r}{Vdd} \tag{4.1}$$

If we use a CTDA waveform that has two transitions in every clock period (Ts), the upper limit for SNR in time domain is given by

$$SNR_T = \frac{T_S^{\,2}}{8 * 2t_\sigma^{\,2}} \tag{4.2}$$

The upper limit for SNR of the corresponding signal in the amplitude domain is given by

$$SNR_V = \frac{Vdd^2}{8v_\sigma^{\,2}} \tag{4.3}$$

Thus, the SNR is improved by a factor

$$\frac{SNR_T}{SNR_V} = \frac{T_S^{\,2}}{2 * t_r^{\,2}} \tag{4.4}$$

As an example, for Ts=4nS and tr=28pS same circuit block provides 40dB better SNR in case of CTDA representation.

4.2.2 Description of the Proposed Architecture

The strategy for new architecture is to A) use digital circuits wherever possible to take advantage of CV^2f rule and B) represent signal in time domain to leverage the fine time resolution available in the scaled technologies and take advantage of the noise benefit associated with it while avoiding the limitations of the voltage domain. Fig. 4.7a shows a simplified block diagram of a standard multi-bit delta-sigma modulator. The N-

bit quantizer and N-bit DAC suffers due to increased voltage offset and mismatch issues in scaled technologies. The proposed architecture, that can alleviate these issues based on the above strategy, is shown in Fig. 4.7b.

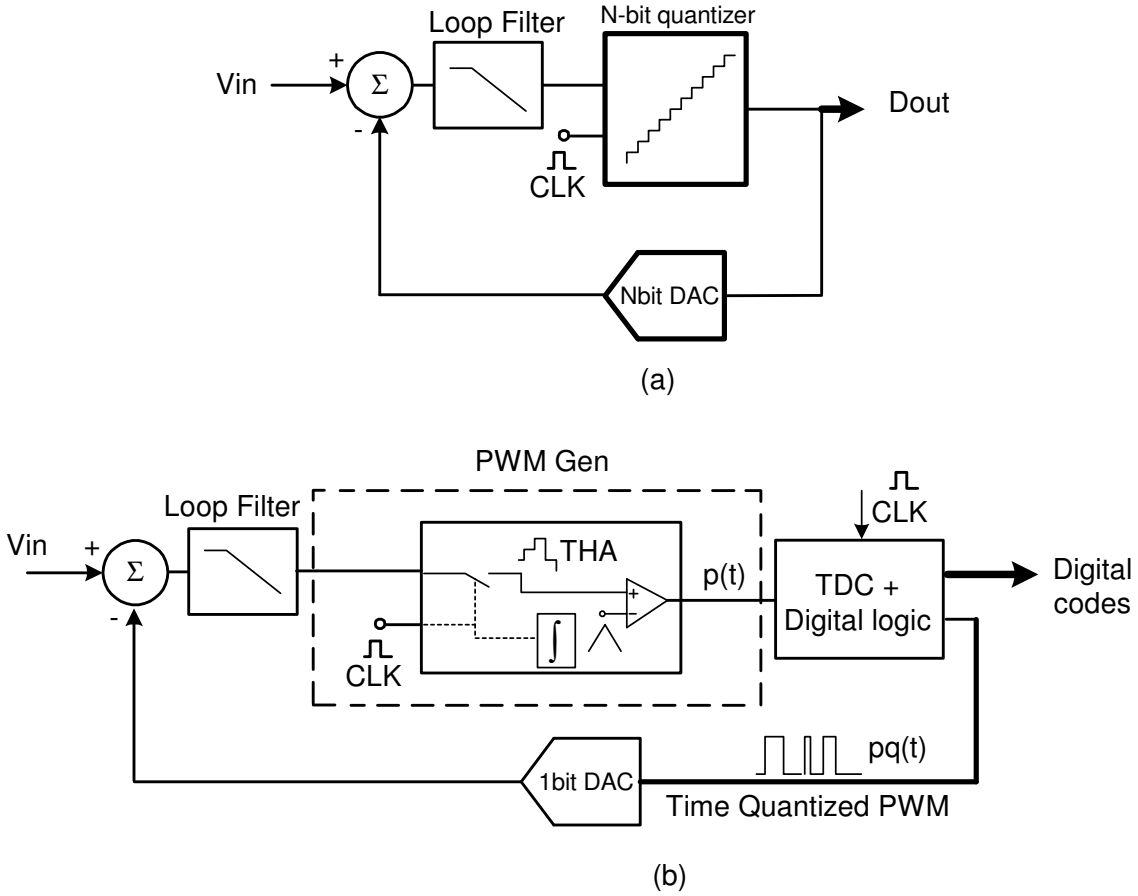


Fig. 4.7 (a) Conventional multi-bit delta sigma modulator. (b) Proposed time-domain quantizer/DAC based delta sigma modulator.

In the proposed architecture, the Pulse Width Modulation Generator (PWM-Gen) and the Time to Digital Converter (TDC) replaces the multi-bit quantizer and the multi-

bit DAC. The PWM- Gen block generates a pulse whose width that is proportional to the amplitude of its input signal for every clock period. Double sampled PWM [55] is used to eliminate the harmonics of the input signal present in case of single sampled PWM. The TDC outputs a pair of digital codes that corresponds to the time edges of its input pulse and it also generates a "time-quantized" feedback pulse. The quantization of the pulse is required to ensure that the feedback signal corresponds to the quantized code output of the TDC (this condition must be met in order to ensure quantization noise shaping). The continuous time loop filter noise shapes the TDC's quantization noise and PWM non-linearity error. A differential pair (1bit DAC) is used for generation of feedback current pulses from the time-quantized digital waveform in order to achieve good power supply rejection and have a reasonably accurate reference. Each of the building blocks is explained in detail below.

4.2.3 TDC, Feedback Pulse Generation and Decimation Filter

The functionality of the TDC is illustrated using a simplified example in Fig. 4.8. In this example, there are N (8 in this case) equally spaced time steps of value T_Q each within a clock period (Ts). For the input pulse shown in this example, the TDC block provides two output codes, Drout (2) and Dfout (6) that corresponds to rising edge and the falling edge of the input pulse respectively. These codes can be used to reconstruct the pulse in clocked digital domain.

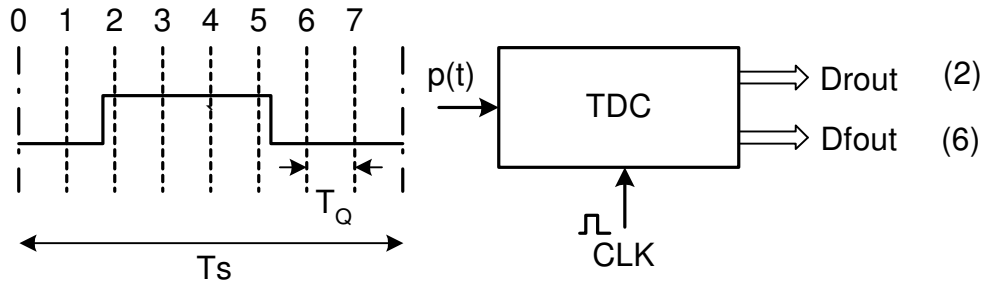


Fig. 4.8 TDC functionality.

In order to generate these codes, the input pulse is latched by an array of D-flipflops that are triggered by N-phases of the clock (see Fig. 4.9).

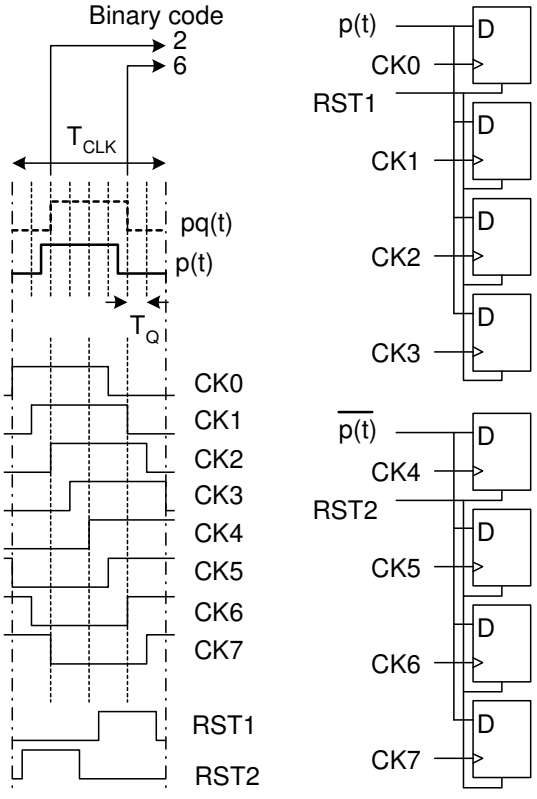


Fig. 4.9 Output code generation circuit.

This arrangement is similar to the one described in [56], however, the order of p(t) and clock input of the D-flipflop is interchanged. In the proposed circuit, p(t) drives the D input so that, as will be explained soon, the feedback pulse can be easily generated. The first N/2 flipflops use the non-inverted input pulse (p(t)) and the second N/2 flipflops use the inverted pulse (complement of p(t)). The outputs of these first and second set of flipflops provide a thermometric code that corresponds to Drout and Dfout-N/2 respectively. N phases of the input clock can be generated using an array of delay elements in cascade. The delay elements can be realized using a chain of simple CMOS inverters. The accuracy of the delay time can be tuned using a scheme described later in section 4.4.4. The time-quantized feedback pulse, denoted as pq(t) in Fig. 4.9, by definition, has to make transitions only at the time instances of clock transitions (rising edge of CK0-7). This can be achieved by triggering the D-flipflops using the N-phase clocks.

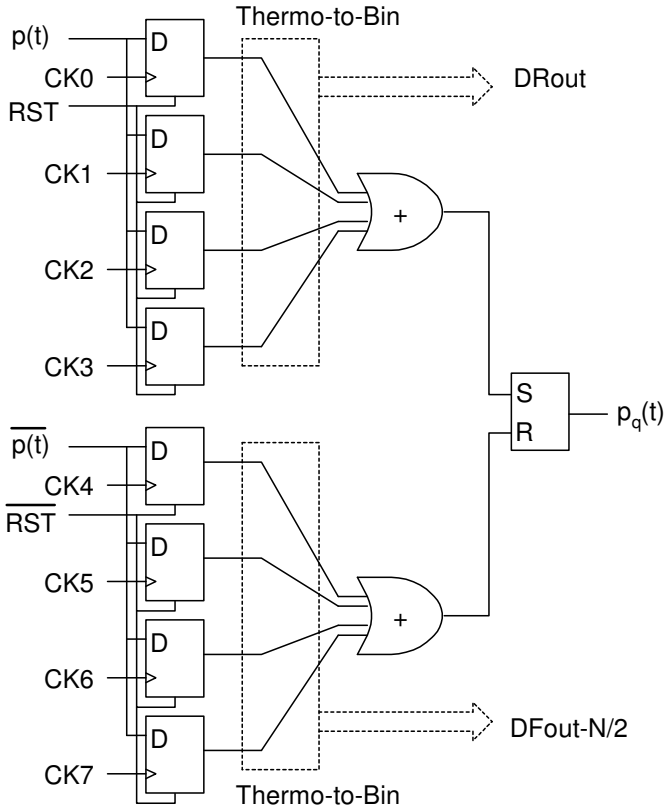


Fig. 4.10 Generation of feedback pulse using logical OR and SR latch.

The time quantized feedback pulse, Pq(t), can be generated using a pair of OR gates and a SR latch as shown in the circuit arrangement in Fig. 4.10. Pq(t) turns 'High' when the earliest of CK0-3 goes 'High' after p(t) is 'High'. Pq(t) turns 'Low' when the earliest of CK4-7 goes 'High' after p(t) turns 'Low'. The outputs of the D-flipflops are passed to thermometric to binary converters to generate the output codes. It is important that all the inputs of the OR gate sees equal systematic delay from input to output (unequal delay would result in non-linearity in the feedback path). This can be achieved by using the "wired-NOR" structure shown in Fig. 4.11.

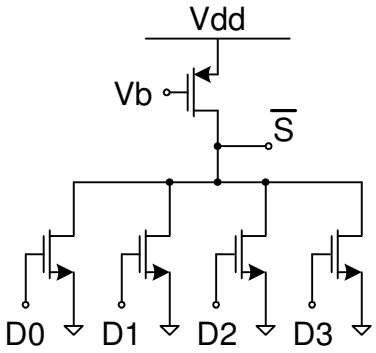


Fig. 4.11 Wired-NOR for equal systematic delay from input to output.

The output codes from the D-flipflops represent the pulse edge timings rather than the usual impulse amplitudes represented by clocked digital codes. Thus, a pulse to impulse amplitude converter is required at the output of the modulator (See Fig. 4.12). In double-sampled PWM signal, the information is contained in pulse width as well as the pulse position. Thus, it would be incorrect to consider the pulse width the same as impulse amplitude. Taking pulse width in each clock period as the digital amplitude samples implies an operation equivalent to integrate-sample-reset. In frequency domain, the PWM waveform's spectrum contains signal frequency, reference frequency and its harmonics and progressively higher order intermodulation products of reference harmonics and signal frequency [55]. The integrate-sample-reset operation, however, corresponds to down-conversion by a factor of N after a mere first-order sinc filtering. Clearly, this down-conversion is being performed with inadequate filtering and would result in aliasing error that would degrade the SNR of the output signal. The obvious solution to this problem is to run the digital decimation filters at a clock rate of $1/T_Q$

(rather than 1/Ts) and process the quantized PWM signal as regular 1-bit data stream. However, this is impractical since the digital filter would either consume huge amount of power or simply cannot be built due to timing constraints depending on the value of T_Q. To circumvent this problem, the digital decimation filter's architecture has to be fundamentally changed.

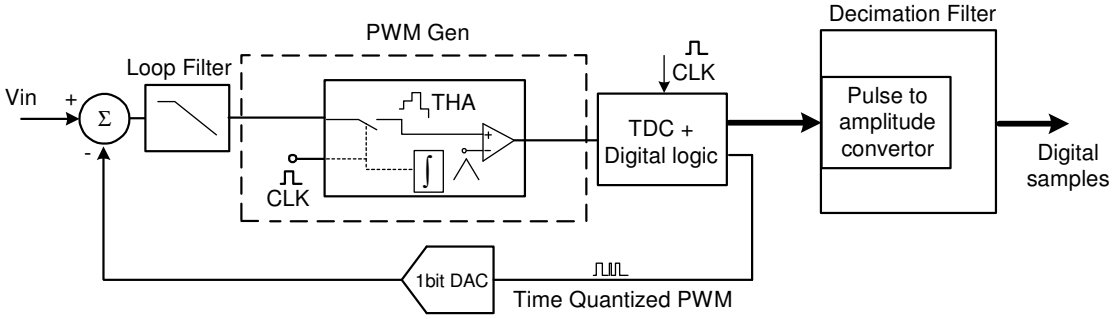


Fig. 4.12 Pulse to amplitude convertor / decimator.

Consider a conventional K-tap FIR filter with decimation factor of K shown in Fig. 4.13. For each output clock period (K*Ts), the output is determined by weighted sum of K input sequence (the weights being the coefficients h[1] to h[K]). If this filter has to be modified in a brute-force way to prevent aliasing, it must be scaled to have N*K coefficients and must operate at a frequency of N/Ts. Since the input pulse has a regular pattern (switches exactly twice during a clock period) the FIR filter can be modified to perform convolution of h[n] with finite-width pulses rather than impulses. The proposed filter would have N*K coefficients. Instead of the actual coefficients h[n], a running sum of the coefficients (Σh[n]) would be stored in the memory. The codes

Dfout and Drout can be used to address the memory holding Σh[n] to fetch the values whose difference would yield the convolution with a particular pulse (see Fig. 4.14 for illustration). Summation of K such differences would give the final output of the filter.

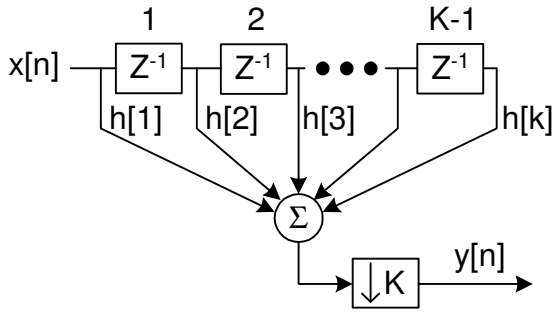


Fig. 4.13 FIR decimation filter – simplified block diagram.

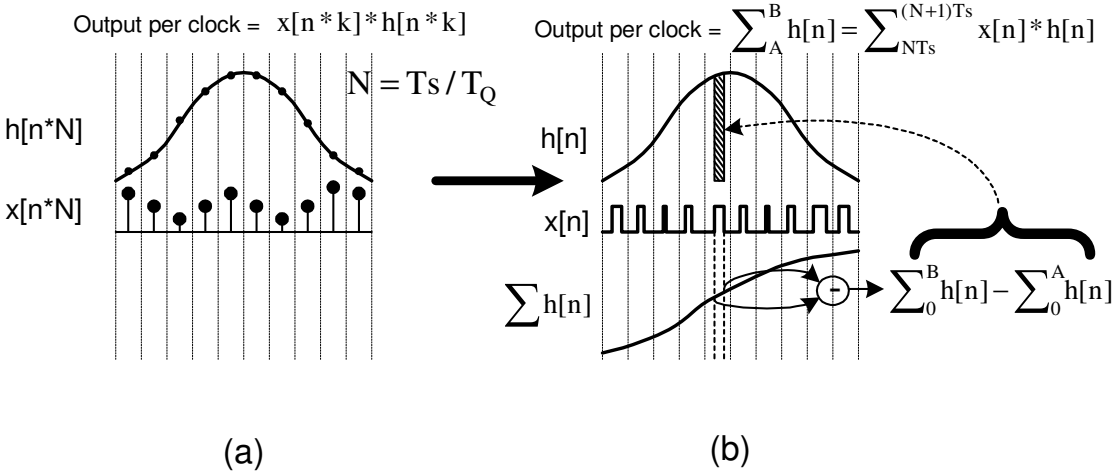


Fig. 4.14 (a) Conventional multiply-accumulate-dump FIR filter.

b) Proposed FIR filter.

Note that the proposed filter operates at frequency 1/Ts while able to filter out-of-band tones until N/(2*Ts) frequency. Each multiply operation is replaced with two mux and one difference operation, which could save significant amount of power.

4.2.4 PWM Generator

The PWM waveform is generated by using the well known technique of comparing the input signal with a triangular waveform. The generator consists of a track and hold (T/H) circuit, a ramp generator and a pair of comparators. A simplified single-ended version of the PWM-generator is shown in Fig. 4.15. The T/H circuit is used before the comparator in order to keep the output pulse rate at clock frequency (1/Ts). T/H is clocked at twice the clock rate to ensure double sampling. Essentially, the rising part of the ramp waveform and falling part of the ramp waveform are compared with two different samples of the input signal that are staggered by Ts/2. The PWM generators noise and linearity performance is relaxed due to noise shaping effect of the loop. Simple circuit implementation is preferred due to high speed and low dynamic range requirement. Inverter based comparator is used to support large voltage swings and hence maximize the reference voltage (peak of the ramp waveform). The ramp generator is realized by a simple integrator with capacitors and switched current sources driven by the input clock. Transistor level implementation of the inverter based comparator and the ramp generator will be discussed in section 4.4.3. Since the error of the PWM generator is also noise shaped, the linearity specifications of the ramp generator is quite relaxed.

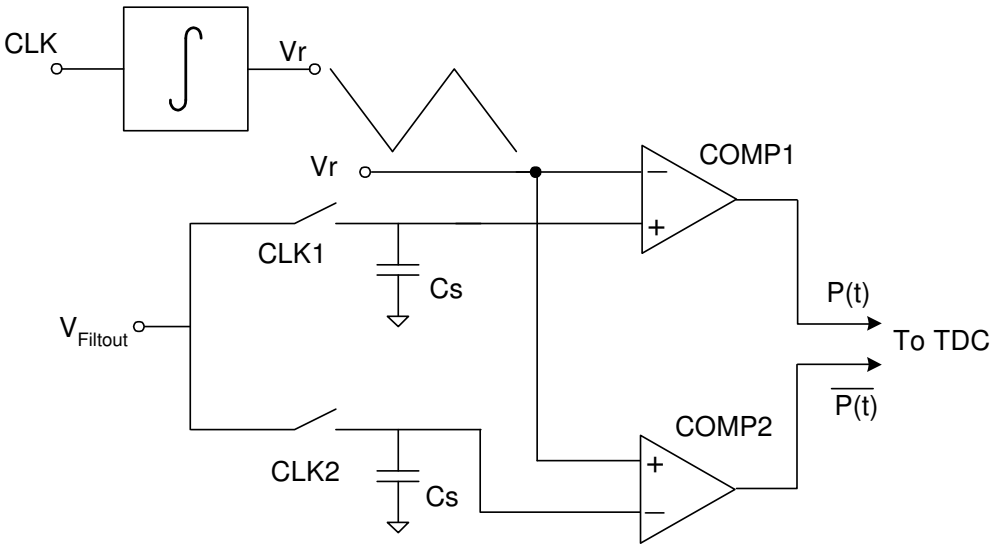


Fig. 4.15 Simplified block diagram of PWM generator.

4.3 Analysis of the Proposed Architecture

In this section, the new architecture will be analyzed to identify the key differences in the design procedure as compared to that of a standard continuous time delta-sigma modulator as outlined in [39]. The analysis will be restricted to the linear model of the delta-sigma modulator. The first step is to identify a linear model for the time-domain quantizer. After this, the impulse response of the PWM generator and the TDC is analyzed. This is followed by a discussion of the sources of excess loop delay and the solution to compensate for the same. The effect of external clock jitter on the proposed delta-sigma modulator will be also examined.

4.3.1 Time-Domain Quantizer

PWM spectrum consists of signal frequency (ω_S) and its odd harmonics, reference tones due to ramp fundamental (ω_R) and its harmonics and intermodulation products of the signal and the reference tones. The exact spectral content of a double-sampled (also called asymmetric regular sampled) PWM is shown in [55] to be

$$\begin{aligned} v_p(t) = {} & \frac{2V_a}{\pi}\sum_{n=1}^{\infty}\frac{1}{\left[n\frac{\omega_S}{\omega_R}\right]}J_n\left(n\frac{\omega_S}{\omega_R}\frac{\pi}{2}M\right)\mathrm{Sin}\left(n\frac{\pi}{2}\right)\mathrm{Cos}(n\omega_S t) \\ & + \frac{2V_a}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}J_o\left(m\frac{\pi}{2}M\right)\mathrm{Sin}\left(m\frac{\pi}{2}\right)\mathrm{Cos}(m\omega_R t) \\ & + \frac{2V_a}{\pi}\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty}\frac{J_n\left(\left[m+n\frac{\omega_S}{\omega_R}\right]\frac{\pi}{2}M\right)}{\left[m+n\frac{\omega_S}{\omega_R}\right]}\mathrm{Sin}\left([m+n]\frac{\pi}{2}\right)\mathrm{Cos}(m\omega_R t + n\omega_S t) \end{aligned} \tag{4.5}$$

Here, V_a represents the PWM signal amplitude, J_n represents Bessel function of order n and M represents the modulation index of the PWM.

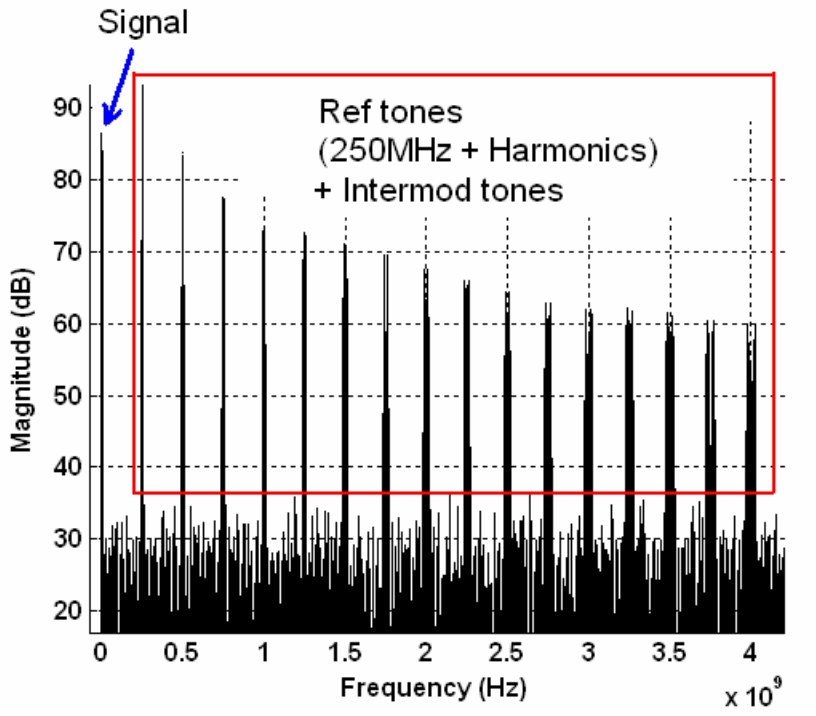
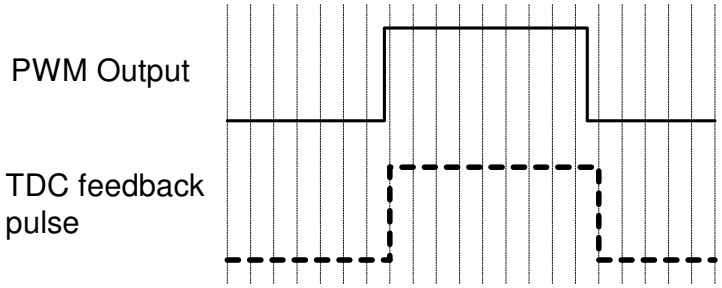


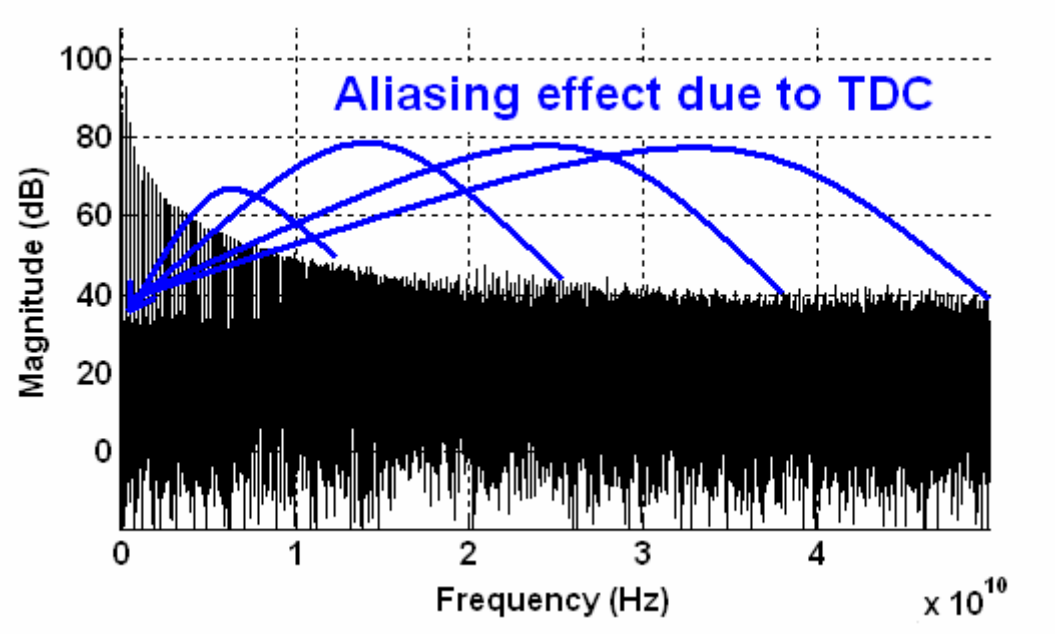
Fig. 4.16 Example spectrum of a PWM waveform.

The spectrum of a PWM waveform with 1MHz signal tone and 250MHz ramp frequency is shown in Fig. 4.16. As it can be observed from the plot, the higher order reference harmonics carry more prominent higher order intermodulation products, eventually leading to a noise floor kind of spectrum at high frequencies. The TDC quantizes the PWM waveform in time-domain. The feedback pulse generated by the TDC is essentially a sampled and held version of the PWM pulse with a sampling period of T_Q. This sampling process inevitably results in aliasing of the high frequency tones

present in the spectrum of the input PWM waveform. Fig. 4.17a shows the TDC sample and hold effect in the time domain. The aliasing of the higher order reference tones and their intermodulation products within nyquist frequency is shown is Fig. 4.17b. In this example, the quantization time step T_Q (sample period) of the TDC is 80pS. This implies sampling at a frequency of 12.5GHz, resulting in folding of the spectral components into a bandwidth of 6.25GHz. Fig. 4.17c shows the spectrum of the quantized waveform at the TDC output. It can be seen that a "quantization noise floor" is formed due to the TDC sampling. This is similar to the quantization noise floor in conventional sampled amplitude quantizer, where the harmonic distortion of the quantized signal folds over to form a quantization noise floor due to sampling [57]. Clearly, the quantization noise floor due to intermodulation aliasing (in case of PWM+TDC time quantizer) is different from that would result from harmonic aliasing (in case of a conventional sampled amplitude quantizer). Hence, for a given number of "quantization steps", the time domain quantizer is expected to have a different SQNR compared to an amplitude quantizer. Due to the complexity of equation (4.5), the quantization noise of the time quantizer for a given number of steps is found through simulations.

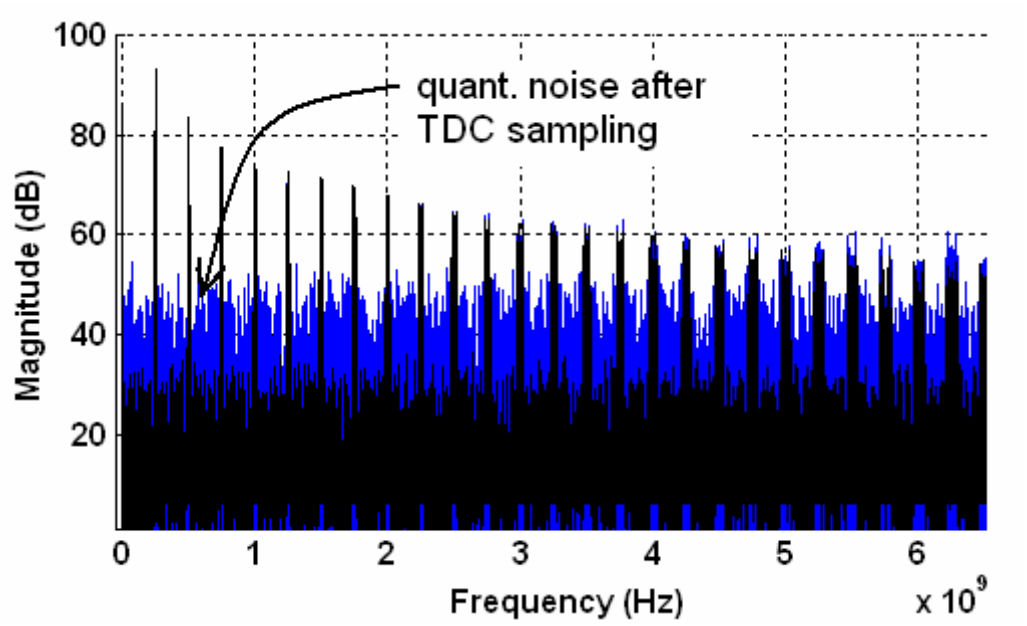


(a)



(b)

Fig. 4.17 (a) "Time quantization" due to TDC. (b) Aliasing effect due to time quantization. (c) Quantization noise floor due to aliasing.



(c)

Fig. 4.17, continued

Fig. 4.18 shows plots of SQNR vs. number of quantization steps (N_Q) in case of amplitude and time quantizer. This is obtained by considering the "integrated noise" over frequency 0 to 1/(2Ts). It can be seen that the time quantizer exhibits higher quantization noise (due to aliasing of PWM intermodulation components rather than just the signal harmonics) for a given N_Q. The difference in the quantization noise reduces with N_Q due to higher TDC's effective sampling frequency ($1/T_Q$) and lower levels of intermodulation tones at high frequency that is aliased back. This reduction slows down for large N_Q (>50) due to flattening of the amplitude of the intermodulation components at very high frequencies (see Fig. 4.17b) and narrows to about 8dB for number of quantization steps between 50 and 200. It is important to note that higher quantization

noise is not necessarily a disadvantage since the time quantizer can easily implement large number of quantization steps as opposed to the amplitude quantizer. For example, in case of 250MHz clock (Ts=4nS), T_Q=80pS or a number of quantization steps (Ts/T_Q) equal to 50 can be easily realized. This corresponds to a SQNR of 25.6dB, which is equivalent to a 4-bit quantizer in amplitude domain.

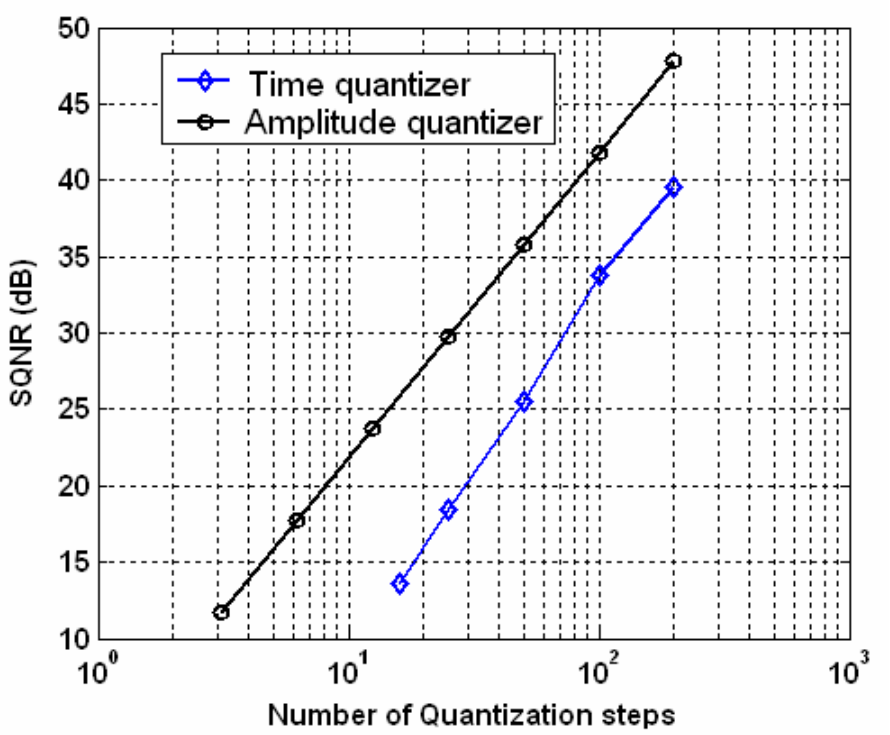


Fig. 4.18 SQNR of time and amplitude quantizer.

4.3.2 Impulse Response of PWM Generator and TDC

Impulse response of all components in the loop has to be determined in order to accurately model the NTF. For a conventional continuous time delta-sigma modulator, as outlined in [39], the impulse response of the continuous time filter (found through

impulse invariant transformation) and the feedback DAC response can be used to determine the NTF. In case of the proposed architecture, the PWM generator's and the TDC's impulse response must be determined. The PWM generator's impulse response can be easily found by examining its operation. Due to its double-sampled nature, the sample and hold circuit in the PWM generator operates at a frequency of 2/Ts. The ramp comparison operation does not have any frequency dependence by itself (it only adds error due to reference tones and intermodulation components). Thus, the impulse response of the PWM generator is attributed entirely to the S/H circuit. Fig. 4.19 shows the impulse response of the PWM generator, which is given by

$$H_{PWM}(s) = \text{sinc}(fTs/2) \tag{4.6}$$

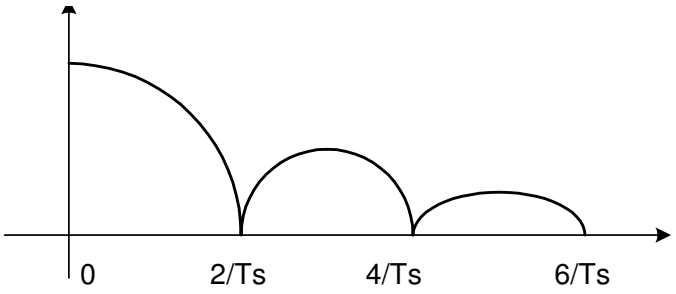


Fig. 4.19 Impulse response of the PWM generator.

TDC performs a sample and hold operation with an effective sampling period of T_Q. The frequency response that corresponds to this operation is given by

$$H_{TDC}(s) = \text{sinc}(fT_Q) \tag{4.7}$$

For large N_Q, T_Q is much less than Ts/2. In that case, TDC's frequency response introduces only a small droop at 2/Ts (see Fig. 4.20) that can be ignored for all practical purposes. Thus, the frequency dependence mainly arises due to continuous time loop filter and the PWM generator. The procedure outlined in [39] for NTF design, needs the continuous time loop filter's transfer function and the "DAC impulse response". This procedure can be easily adapted for the NTF design of the proposed modulator by assuming a NRZ pulse of width equal to Ts/2 for DAC impulse response (which, in this case, actually comes from the PWM generator).

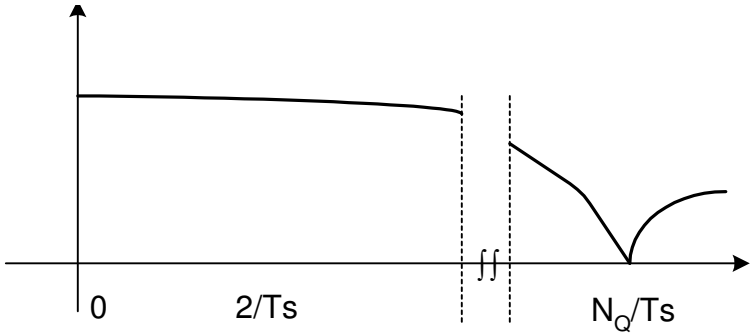


Fig. 4.20 Impulse response of the TDC.

4.3.3 Excess Loop Delay

One of the important parameters that affect the NTF of the modulator is the excess delay in the loop. The main contribution of the excess delay comes from propagation delay in the digital logic of the TDC that is used to generate the feedback pulse, the PWM comparator's delay and the excess phase of the loop filter. It is shown that the excess delay effectively increases the order of the loop due to "spill over" of the

feedback pulse to the next clock period [39]. In order to preserve the NTF, the loop filter must be redesigned to implement the transfer function $H(z)*z^{+D}$ instead of the desired loop filter transfer function H(z). Here, D denotes the fractional excess delay (the ratio of excess delay-time to the sampling period) in the loop. This redesign requires an additional feedback path around the quantizer to ensure controllability of the system [58]. Fig. 4.21 illustrates the standard compensation scheme used to mitigate the effect of loop delay.

In case of the proposed architecture, the direct feedback to the input of PWM generator is faced with some difficulties. Since the last integrator of the active-RC loop filter behaves like a voltage source charging the sampling capacitor of the PWM generator, a straight forward addition is not possible. An interesting method discussed in [41] employs a differentiator in digital domain that enables a pair of feedback DAC to inject current at the virtual ground of the last integrator of the loop filter. The proposed method uses an arrangement with much less complexity.

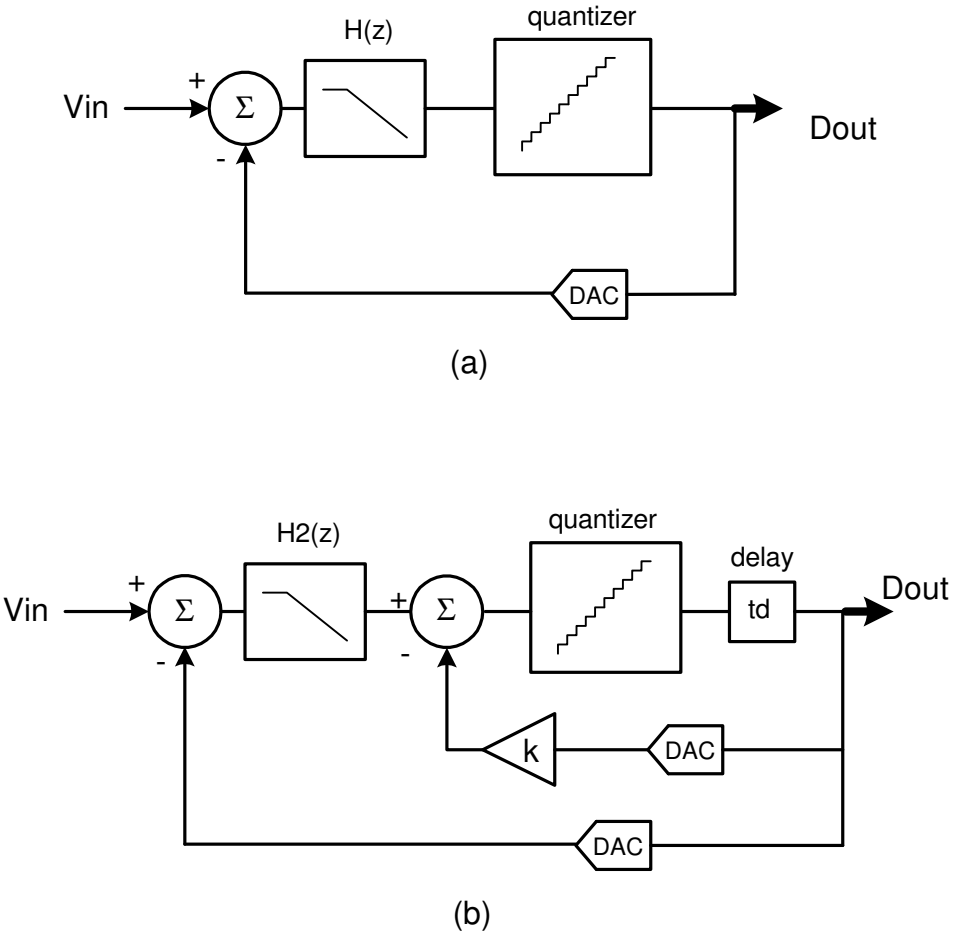


Fig. 4.21 (a) Delta-sigma loop with no excess delay. b) Delta-sigma loop compensated for excess delay.

In the proposed scheme a capacitor is used to generate a differentiated current that is proportional to the output waveform. This is achieved by driving the virtual ground of the last integrator of the loop filter with a CMOS inverter through a MOS capacitor connected in series. Fig. 4.22 shows the circuit arrangement for the proposed compensation method. A bank of binary weighted CMOS inverters and MOS capacitors

is used to facilitate programming of the feedback coefficient in order to accommodate process variations. The feedback coefficient 'k' is determined the supply voltage of the inverters and the ratio of the total feedback capacitor to the integrator's capacitor. The calculation of the coefficient 'k' is described later in section 4.4.2. The overall compensation scheme for loop delay remains essentially the same as in a conventional continuous time modulator.

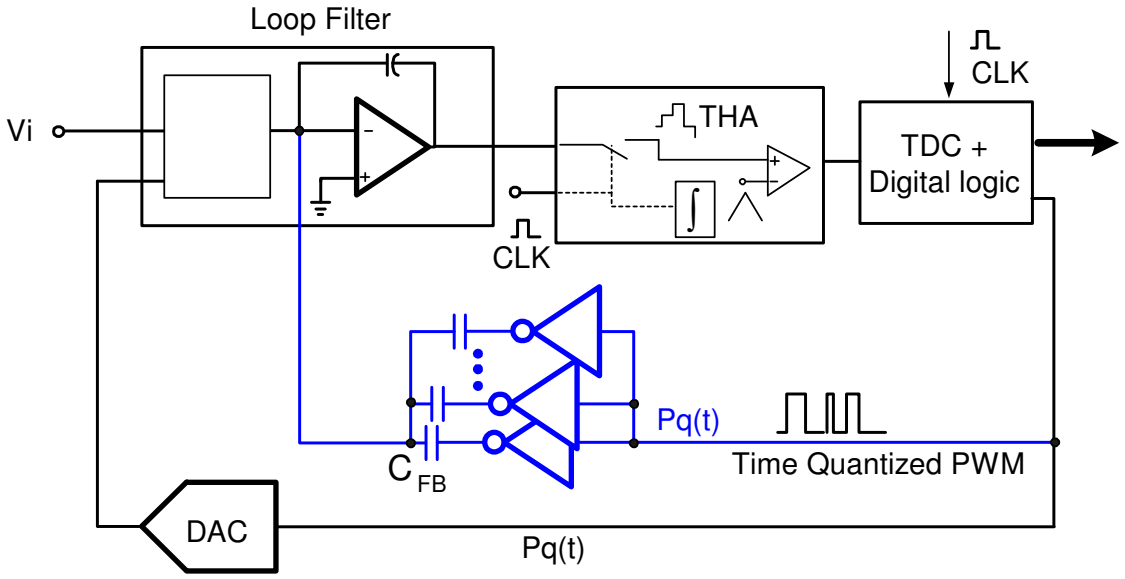


Fig. 4.22 Proposed method for generating feedback around quantizer.

4.3.4 Clock Jitter

Clock jitter remains as one of the limiting parameters of the performance of a continuous-time modulator. The error introduced in the feedback pulse due to the clock jitter is not noise-shaped by the loop filter (since it directly appears at the input). This error can be modeled as a random phase modulation of the feedback pulses [39]. In case

of the proposed architecture, some rejection of jitter is achieved due to the arrangement that generates the feedback pulse. From Fig. 4.23, it can be seen that both the rising and the trailing edge of the feedback pulse within a clock period carries the same time shift due to the clock jitter. This is due to the fact that rising edges of CK0-7 are derived from the same clock edge using delay elements. Hence, the clock jitter affects only the position of the feedback pulse. The pulse width remains unchanged. The effect of random pulse position modulation of a PWM waveform is cumbersome to analyze with equations. The necessary insight can be gained through simulations.

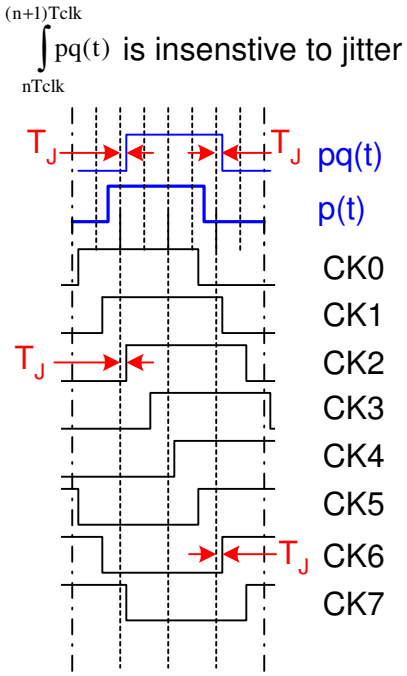


Fig. 4.23 Effect of clock jitter in proposed scheme.

Simulations were performed using the MATLAB model of the proposed ADC with additive Gaussian white phase noise in the clock waveform. The SNR limitation due to the clock jitter for various values of RMS clock jitter is plotted in Fig. 4.24. The SNR limitation for conventional feedback using RZ pulse, calculated using the formula given in [39] is also plotted in the same figure. It is observed that the proposed scheme has about 10dB rejection of noise due to jitter. This is attributed to the invariance of the pulse width in the presence of clock jitter.

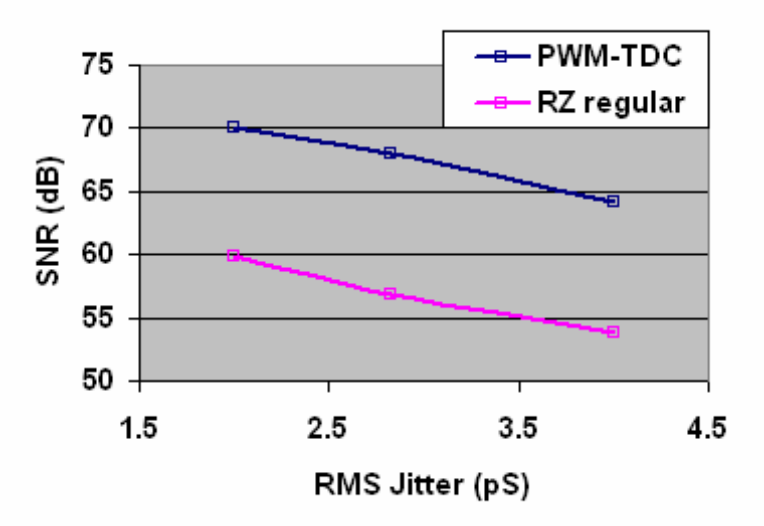


Fig. 4.24 SNR limitation due to clock jitter for RZ and proposed scheme.

4.4 Design of 20MHz BW, 10bit ADC Using the Proposed Architecture

A 20MHz BW, 60dB Dynamic range, ADC designed based on the proposed architecture is discussed in this section. The choice of NTF and the topology of an active-RC filter that realizes the loop filter of the delta-sigma modulator are discussed. The coefficient calculation, taking in to account the excess loop delay in the modulator, is presented. The design of the PWM generator and the TDC are described. Noise contributions from various building blocks will be examined. Non-idealities of various building blocks are examined and dynamic range limitations due to each of these were found using simulation on the SIMULINK model.

Wideband delta-sigma modulators are typically designed with a clock frequency as high as the technology allows. This is done in order to achieve the best SQNR, which is proportional to $OSR^{(2L+1)}$ [59], where L is the order of the modulator. In order to improve the power efficiency, however, it is best to design with as low OSR as possible provided the SQNR requirement is met. In this design, the speed of the technology will be utilized to maximize the number of the steps in the time-domain multi-bit quantizer while the OSR is minimized to save power in the loop filter and the digital decimation filters. Since SQNR improves rapidly with OSR, and hence the power dissipation, it is still desirable to have the overall performance limited by the thermal noise. In order to achieve 10-bit ENOB, a SQNR of 70dB is targeted. A clock frequency of 250MHz is chosen and T_Q=80ps is used in order to achieve an effective 4-bit quantizer. A third order loop filter is used to achieve the necessary SQNR.

4.4.1 NTF Design and Loop Filter Topology

Although the data throughput from the time-domain quantizer is 250MSPS, the sample-and-hold before quantization is clocked at 500MHz (due to double-sampled PWM). This allows to double the OSR for a given throughput rate. The loop filter is designed to achieve a third order quasi-inverse-Chebyshev high pass noise shaping. The infinite Q complex poles, that are required to realize an ideal inverse-chebyshev high-pass, are replaced with ones with Q of 8 to yield an approximate equiripple characteristic. A plot of the desired NTF is shown in Fig. 4.25. The discrete-time loop filter transfer function that yields this NTF is given by

$$H(z) = \frac{1.622z^2 - 2.093z + 0.8024}{z^3 - 2.922z^2 + 2.894z - 0.9721} \tag{4.8}$$

The equivalent continuous time filter is found by using the 'd2cm' function in MATLAB. A sampling period of 2nS (1/500e6) is assumed and the option 'zoh' is used to indicate the zero-order hold, which accounts for the sample and hold in the PWM generator. The transfer function of the resulting continuous time filter is given by

$$H(s) = \frac{5.908e8s^2 + 2.086e17s + 4.223e25}{s(s^2 + 1.414e7s + 1.279e16)} \tag{4.9}$$

This H(s) provides a minimum in-band gain of 37dB that serves to suppress quantization noise and other errors introduced by the subsequent blocks in the forward path.

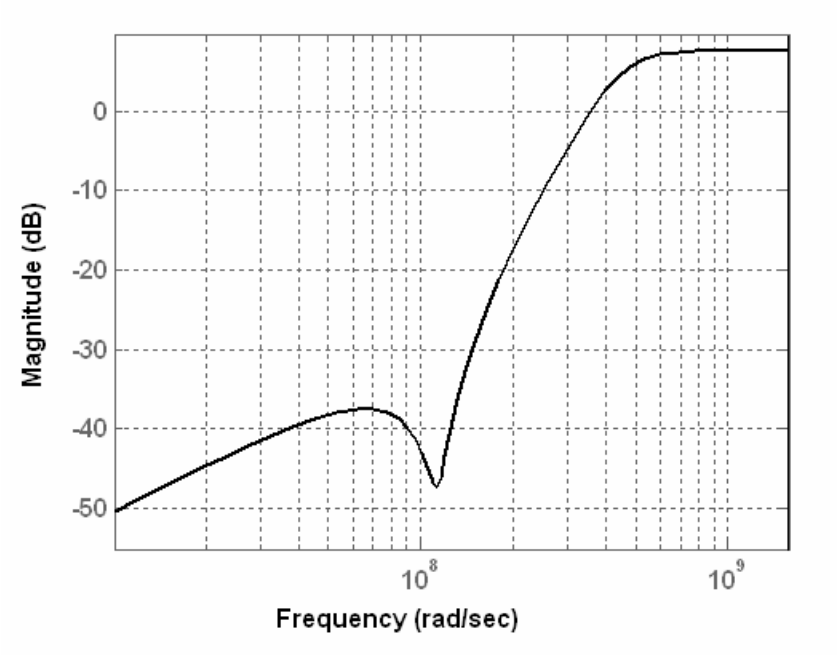


Fig. 4.25 Noise transfer function of the modulator.

A single-ended version of the active-RC filter topology that realizes the transfer function described by (4.9) is shown in Fig. 4.26. The -1 gain block indicates that the differential counterpart is used to ensure that the desired transfer function is produced. Amplifiers A1 and A2 along with the passives form a biquad section. The feedforward capacitances C_B and C_H provide the second-order bandpass and highpass outputs from the biquads respectively. Resistor R3 is used to generate second order lowpass current. The combined lowpass, bandpass and highpass signals at the output of the integrator formed by A3 and C3 provide the desired transfer function.

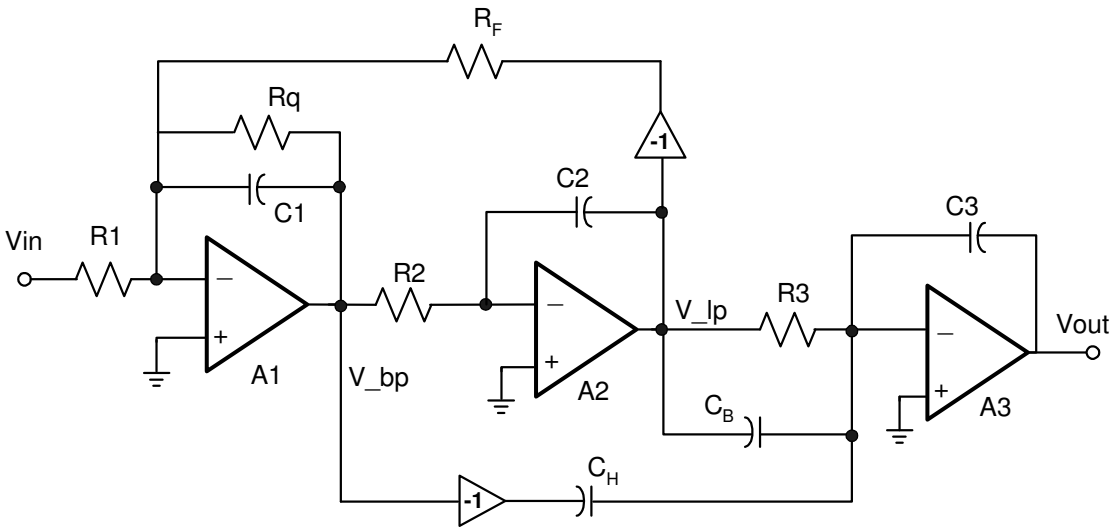


Fig. 4.26 Active-RC loop filter topology.

4.4.2 Loop Delay Compensation and Coefficient Calculations

The continuous time loop filter's transfer function calculated from H(z) assumes that the feedback pulse instantaneously starts when the PWM input is sampled. In practice, however, the loop exhibits a finite "excess delay". In order to retain the NTF, the loop filter coefficients have to be adjusted. A procedure similar to one described in [60] is followed to accomplish this. From the initial design, the additional delay due to the PWM comparator and the digital logic use to generate the feedback pulse was found to be 660pS. This is roughly equal to one-third of the clock period 2nS. If we realize $H2(z^{1/3}) = z^{1/3} * H(z^{1/3})$, the loop delay can be effectively compensated. Here, $H(z^{1/3})$ is a equivalent transfer function of H(z) at thrice the sampling rate, found using the "d2d" function in MATLAB.

$$H(z^{1/3}) = \frac{0.4399z^{2/3} - 0.7751z^{1/3} + 0.3477}{z^{3/3} - 2.985z^{2/3} + 2.9764z^{1/3} - 0.9906} \tag{4.10}$$

A constant term can be removed from H2($z^{1/3}$) to arrive at the following form.

$$H2(z^{1/3}) = 0.4399 + \frac{0.538z^{2/3} - 0.9613z^{1/3} + 0.4358}{z^{3/3} - 2.985z^{2/3} + 2.9764z^{1/3} - 0.9906} \tag{4.11}$$

The constant term represents the coefficient of the feedback path around the quantizer as shown in Fig. 4.21b. The remaining part of the transfer function is converted back to original sampling rate (using the "d2d" function) and is further transformed to the equivalent continuous time transfer function H2(s) using the "d2cm" function .

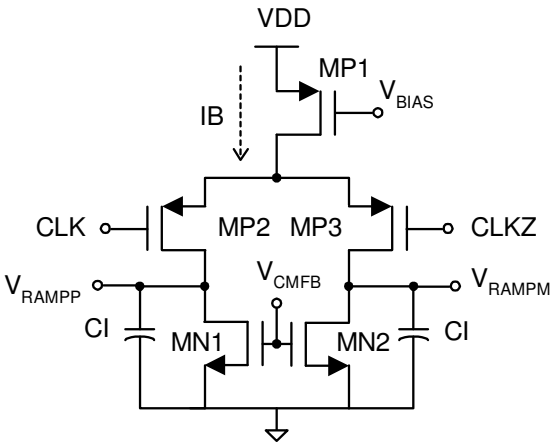
$$H2(s) = \frac{7.312s^2 + 2.312e17s + 4.223e25}{s(s^2 + 1.414e7s + 1.279e16)} \tag{4.12}$$

Note that H2(s) has slightly lower zero frequency compared to H(s) while the pole location remains virtually unaltered. Thus, the feedback around the quantizer and redesign of complex zero location compensates for the excess loop delay.

4.4.3 PWM Generator Design

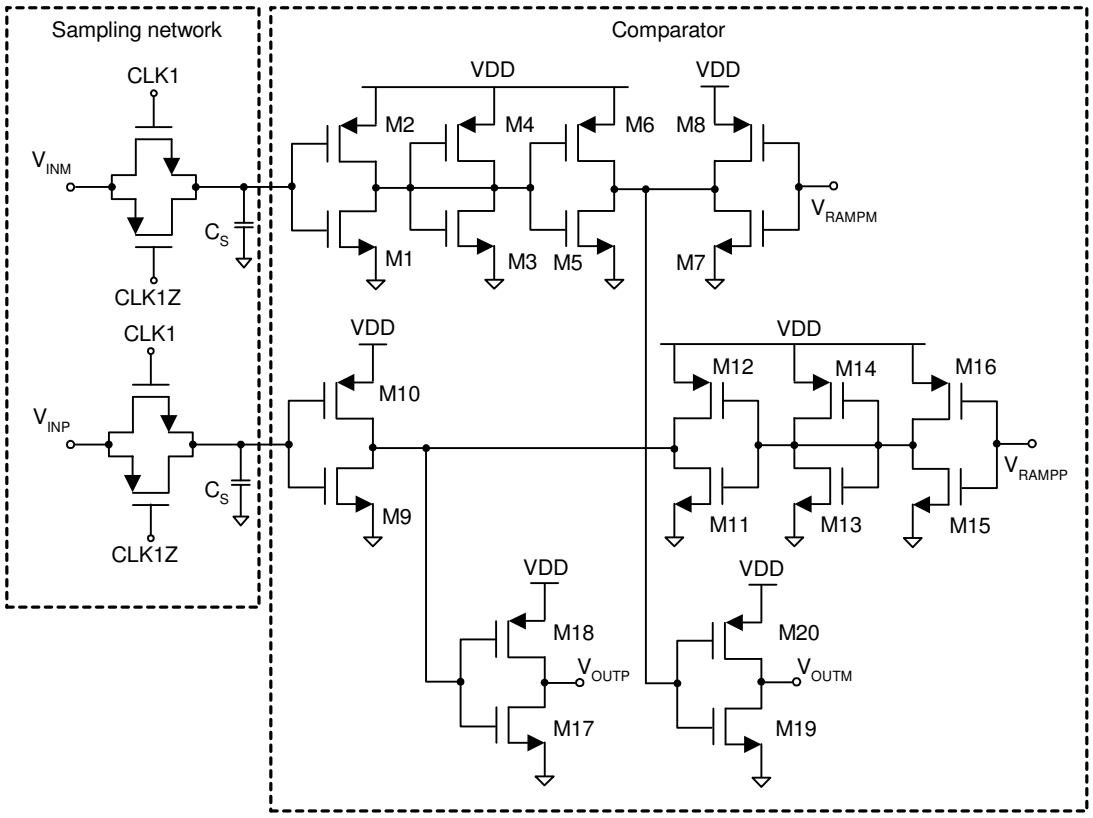
The schematic of the overall PWM generator was already shown in Fig. 4.24. The ramp generator, the sampling network and the high speed comparator schematics are shown in Fig. 4.27. The PWM generator uses a ramp waveform at 250MHz with differential amplitude of 1.2Vpp. The ramp waveform is generated using a switched current integrator (differential pair loaded with capacitors) clocked at 250MHz. The tail current source of the differential pair (MP1) and the load capacitance (CI) determines the amplitude of the ramp waveform. The amplitude can be tuned by adjusting the bias current of the differential pair. The common mode voltage of the output is set using a common mode feedback circuit. The output of the loop filter is sampled at 500MHz.

Since the output of the PWM comparator must be valid for the whole clock period, two separate sampling networks and comparator (each like one shown in Fig. 4.27b) are used for each clock phase (CLK1 and CLK2) such that one of them tracks the input while the other one holds it for the comparator and vice-versa.



(a)

Fig. 4.27 (a) Ramp generator. (b) Sampling network and comparator (two of these are used).



(b)

Fig. 4.27, continued

In order to maximize the voltage swings and retain immunity to common mode noise, an inverter based fully differential comparator is used. Transistors M1-M6 and M11-M16 form the positive Gm first stages of the comparator while the transistors M7-M10 form the negative Gm first stages. The second gain stages are implemented by transistors M17-M20. Note that the cross-coupled latches cannot be used since the output pulse must be valid continuously during the period of operation of each comparator.

The timing of the clock waveforms that drives the two separate sampling networks are shown in Fig. 4.28. Note that the hold instance of the switches exactly coincides with the clock edges of the ramp generator in order to minimize the delay introduced by the PWM generator after the sample is held. A guard time of 200pS is allowed in the tracking phase to avoid conflict between the 'ON' times of the two clock phases CLK1 and CLK2. The non-linearity introduced due to the charge injection of the switches, mismatch between the two paths and the distortion of the ramp waveform is noise shaped by the gain of the loop filter. Hence, the error contribution of the PWM generator is below quantization noise (-70dBFs) even if it meets a modest signal to noise + distortion ratio of 34dB.

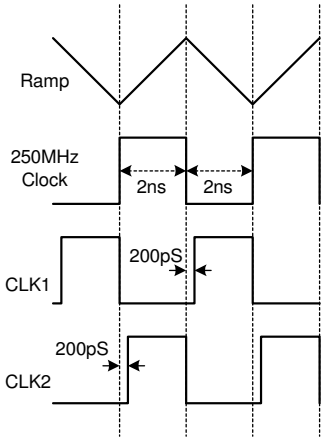


Fig. 4.28 Clock timing for the sampling switches of the PWM generator.

4.4.4 TDC Design

The TDC is designed to generate 50 quantization steps in 4nS period (1/250MHz). The schematic of the TDC is shown in Fig. 4.29. The 50 clock phases are

generated using digital inverter delay elements in cascade. The delay elements are tuned by adjusting their power supply voltage so that the phase of the clock at the output of the 50^{th} delay element matches the phase of the input clock. This can be accomplished by using a delay-locked-loop. However, in the prototype chip, the supply voltage is manually adjusted while monitoring an error signal generated by a phase detector. A simplified schematic of the phase detector that generates the required error signal (Test) is shown in Fig. 4.30. This circuit generates a square-wave output at 62.5MHz if CK50 edges are not within +/- 50pS range from the CLKIN edges and settles to logic 'High' if CK50 edges are within the range.

Each of the clock phases generated using the delay elements are used to drive the clock input of a flipflop as described earlier in section 4.2.3. The first 25 flipflops D inputs are driven by the PWM output pulse whereas the inputs of the last 25 flipflops are driven by the complement of the PWM output pulse. The "wired-NOR" gate shown in Fig. 4.11 has to be designed to accommodate 25 inputs. In order to minimize the gate delay, this gate is split into two stages, each involving 5 sets of 5 input wired-NOR gate followed by a 5 input wired-NAND gate.

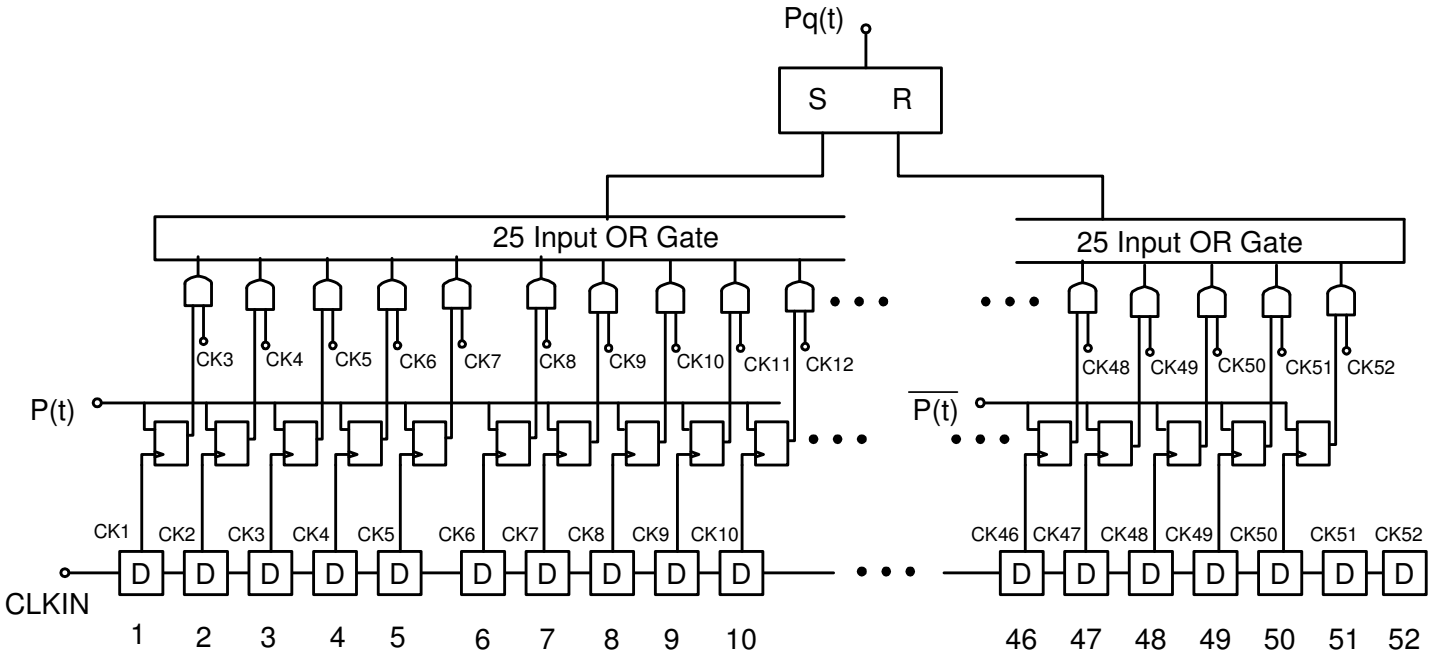


Fig. 4.29 Simplified schematics of the TDC.

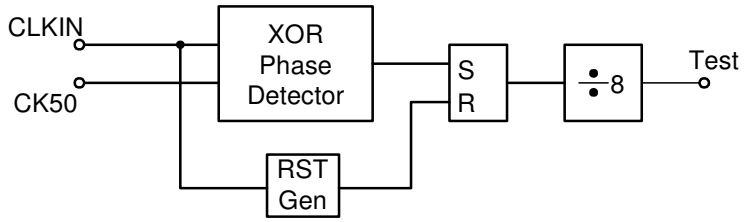


Fig. 4.30 Schematic of phase detection circuit for delay tuning.

The data dependant delay or the "metastability" of the flipflops can lead to error in the feedback pulse that is signal dependant. If not checked, this can result in distortion of the signal. The maximum error that can occur due to this effect happens when the flipflop is registered as different logic levels by the digital logic that generates output code and the one that generates the feedback pulse. Since the maximum error corresponds to one quantization step ($1/50^{th}$ of full scale), the probability of occurrence of this error has to kept at 1.6% or below to meet a distortion performance better than -70dB. From simulations, it was found that if the flipflop outputs are read after 160pS from its clock trigger, this level of probability is easily achieved. This is implemented by introducing an AND gate at the flipflop output that is gated by a clock that is two phases ahead of the flipflops own clock input (see Fig. 4.29). For this reason, two additional delay elements (51 and 52) are used in the end.

4.4.5 Noise Contributors and Budgeting

Various noise contributors in the ADC are shown in Fig. 4.31. The input referred in-band RMS voltage noise of the filter (v_{nLF}) directly appears at the input and thus

contributes directly to the input referred noise. The output referred in-band RMS current noise of the DAC (i_{nDAC}) translates to the input referred noise through a multiplicative factor R1. Here, the DAC injects the feedback current in to the virtual ground of the first integrators opamp and R1 is the input resistor of the first integrator. The output referred in-band RMS timing jitter of the TDC (t_{nTDC}) can be mapped to the input referred noise by appropriately scaling it with Ts, Iref and R1, where Ts in the clock period (4nS) and Iref is the reference current of the DAC. The input referred noise contribution due to the input referred RMS voltage noise of the PWM generator (v_{nPWM}) is simply $v_{nPWM}/|H_{LF}|$, where $|H_{LF}|$ is defined as the average in-band gain of the loop filter over the signal bandwidth of 20MHz. The overall input referred noise can be expressed as

$$v_{nin} = \sqrt{v_{nLF}^{\,2} + i_{nDAC}^{\,2} * R1^2 + \frac{t_{nTDC}^{\,2}}{Ts^2} * Iref^2 * R1^2 + \frac{v_{nPWM}^{\,2}}{|H_{LF}|^2}} \tag{4.13}$$

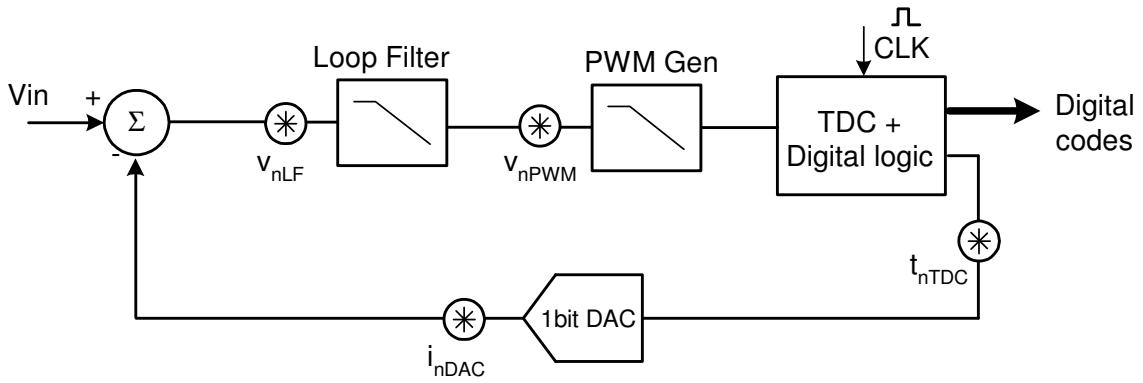


Fig. 4.31 Noise contributors of the ADC.

The reference voltage of the ADC is fixed at 1.08V differential. The input resistance of the loop filter (R1) is chosen as 3KΩ and the DAC reference current is set to 180uA. The loop filter has an integrated input referred RMS noise of 84.5μV (including the input resistor R1). i_{nDAC} is designed to be within 22.4nA and the RMS timing jitter of the TDC is designed to be less than 500fS. From (4.13), it can be verified that the integrated noise of the overall ADC is better than -69dBFs. The breakup of noise power contribution of various blocks is shown in Table 4.3.

Table 4.3 Noise contribution of various blocks.

Block	Input referred voltage noise (μV)	Percentage noise power contribution
Loop filter	85	41.6
DAC	66	25.1
TDC	67	25.8
PWM	36	7.5

In addition to the noise and timing jitter, the mismatch between the quantization steps of the TDC contributes to non-linearity in the feedback. Based on the SIMULINK simulations of the ADC model, it is determined that the RMS mismatch between the time steps of the delay elements of the TDC must be less than 800fS to achieve a distortion performance greater than 65dB with 95% confidence level. The spice

mismatch models were used to size the transistors of the delay elements in order to achieve this level of mismatch performance.

4.5 Simulation and Experimental Results

The SIMULINK model used to design and verify the ADC is shown in Fig. 4.32. The MATLAB simulations were performed in "fixed time step" mode with 0.5pS time step in order to ensure the fidelity of the PWM spectrum. The loop filter is initially modeled with poles and zeros based on the NTF design equations. A more sophisticated model is used later in the design process that includes the parasitic poles and zeros extracted from the transistor level design using SPECTRE's "pz" function. The PWM generator is modeled using a signum function (block "Sign1" in Fig. 4.32) that compares the samples input with the 250MHz ramp waveform. The delay of the comparator is extracted from the transistor level design and used in the block "Transport Delay1". The TDC, along with the feedback pulse generation is simply modeled by a sample and hold block operating at 12.5GHz (1/80pS).

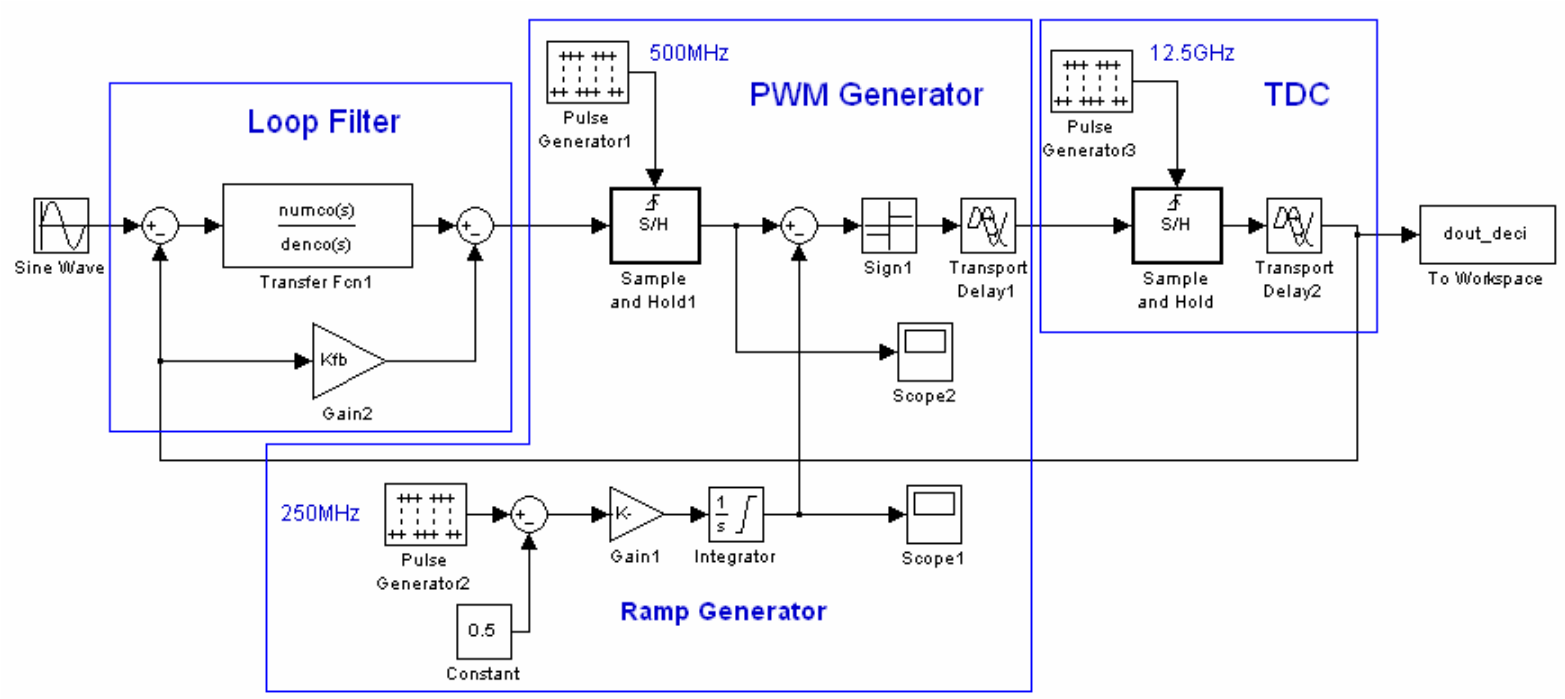


Fig. 4.32 SIMULINK model of the proposed ADC architecture.

The delay of the TDC is extracted from the transistor level design and included in “Transport Delay2” block. The mismatch among the delay elements were modeled by replacing the source block “Pulse Generator3” with “file input” source. The file input provides a clock waveform with randomly distributed period with a mean of 80pS that repeats every 4nS (Ts). In later design stages, the mismatch of the delay elements are extracted using the foundry provided mismatch models and used as a file input source.

Since the parasitic poles and the delay in the loop can affect the NTF, an extracted netlist spice simulation of the full ADC is performed. Fig. 4.33 shows the waveforms at the output of integrator3, integrator1 and TDC feedback pulse from the C-only extracted netlist simulations. The plots in Fig. 4.33 confirm that the 3^{rd} order $\Delta\Sigma$ loop is stable after power up even if the integrators are released from reset (which is required to recover from occasional overload of the modulator) at the peak value of the signal waveform. The spectrum at the output ADC for a 4.7MHz, -5dBFs sine-wave input is shown in Fig. 4.34. A Signal to quantization noise and distortion ratio of 67dB is achieved in 20MHz bandwidth.

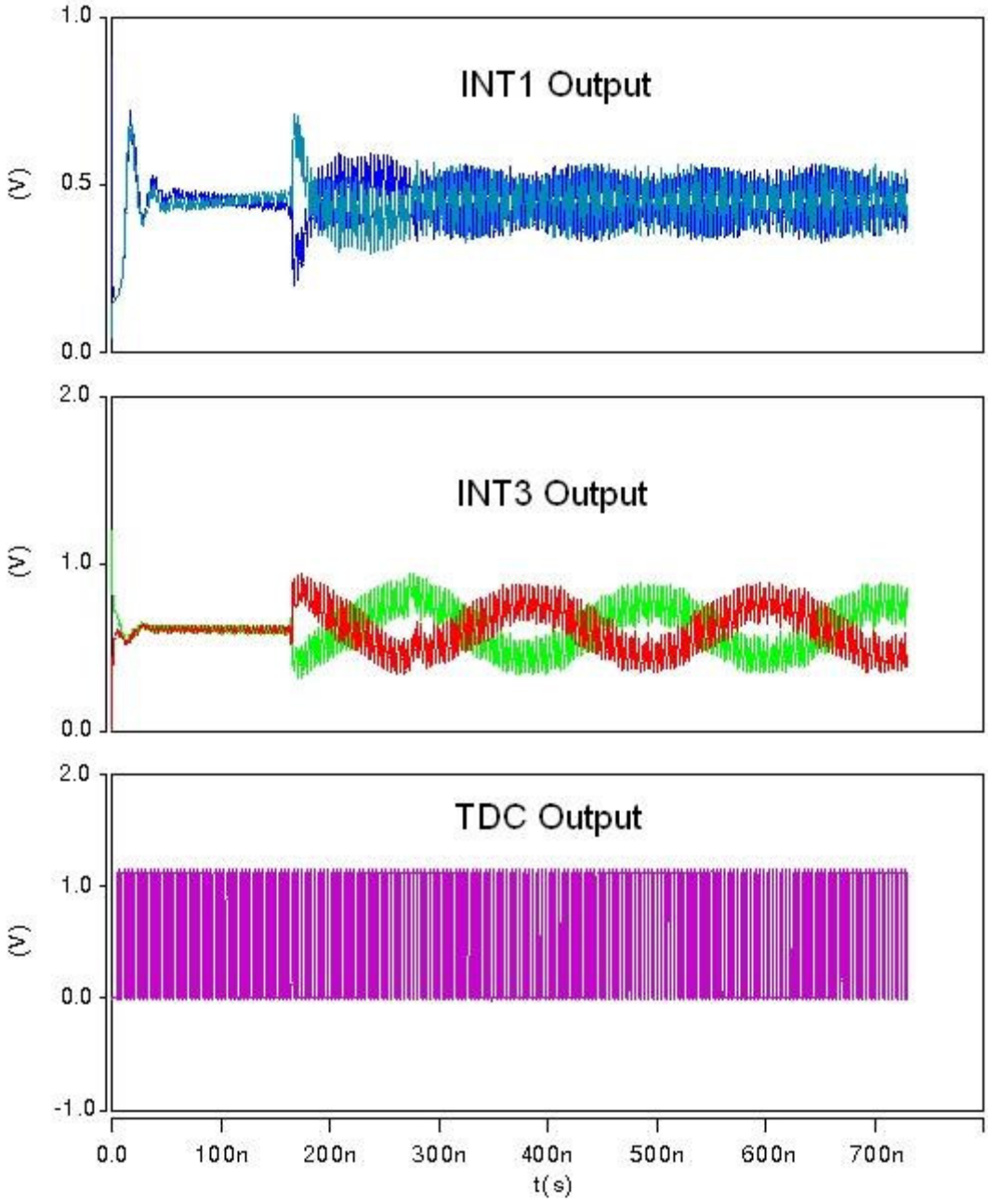


Fig. 4.33 Internal node waveforms from C-only netlist simulation of the full ADC.

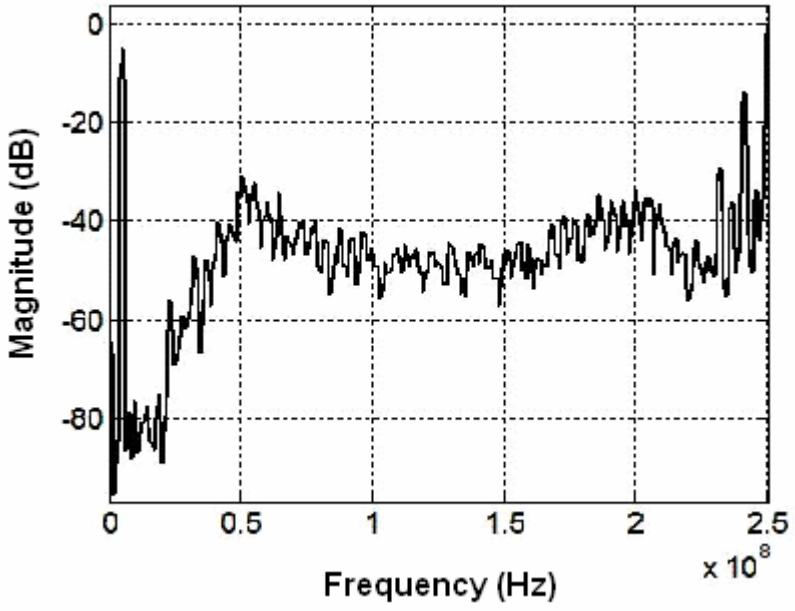


Fig. 4.34 FFT from simulation of full C-only ADC netlist with 4.7MHz -5dB input.

The prototype of the proposed ADC was fabricated in TI 65nm digital CMOS technology. The micrograph of the testchip is shown in Fig. 4.35. The ADC occupies an area of 0.15mm^2. The PCB used for characterization of the testchip is shown in Fig. 4.36. A diagram of the test setup used is shown in Fig. 4.37. A low jitter clock for the ADC is generated using an on-board SAW oscillator. The input signal is generated from a moderate performance signal generator (Agilent E4432B) and a high-Q, passive, LC bandpass filter was used to remove the noise and distortion of the signal source. The signal is converted from single-ended to differential with appropriate common-mode voltage using an on-board low-noise, low-distortion opamp circuit (SE2DE). Power supply lines were filtered using off-the-shelf line filters to remove noise and spurious tones and was further regulated using on-board adjustable regulators. A digital pattern

generator was used for programming various options in the chip. A 5-bit low-voltage differential signal (LVDS) interface running at 500MHz clock speed was used to capture the data with a high speed logic analyzer (Agilent 16950B). The low capacitance differential probe (E5387A) was used to connect the on-board LVDS buffers to the logic analyzer.

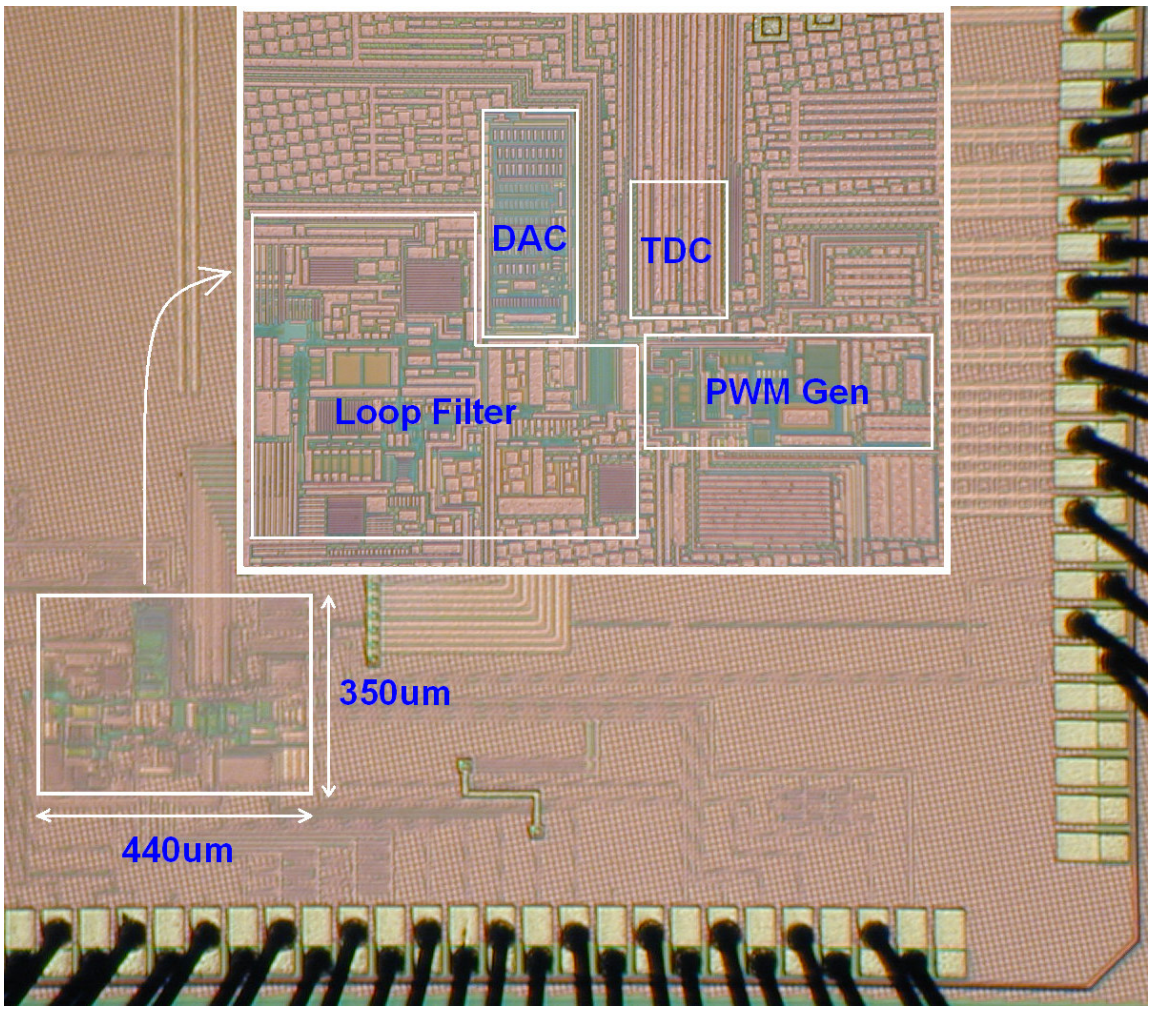


Fig. 4.35 Chip micrograph.

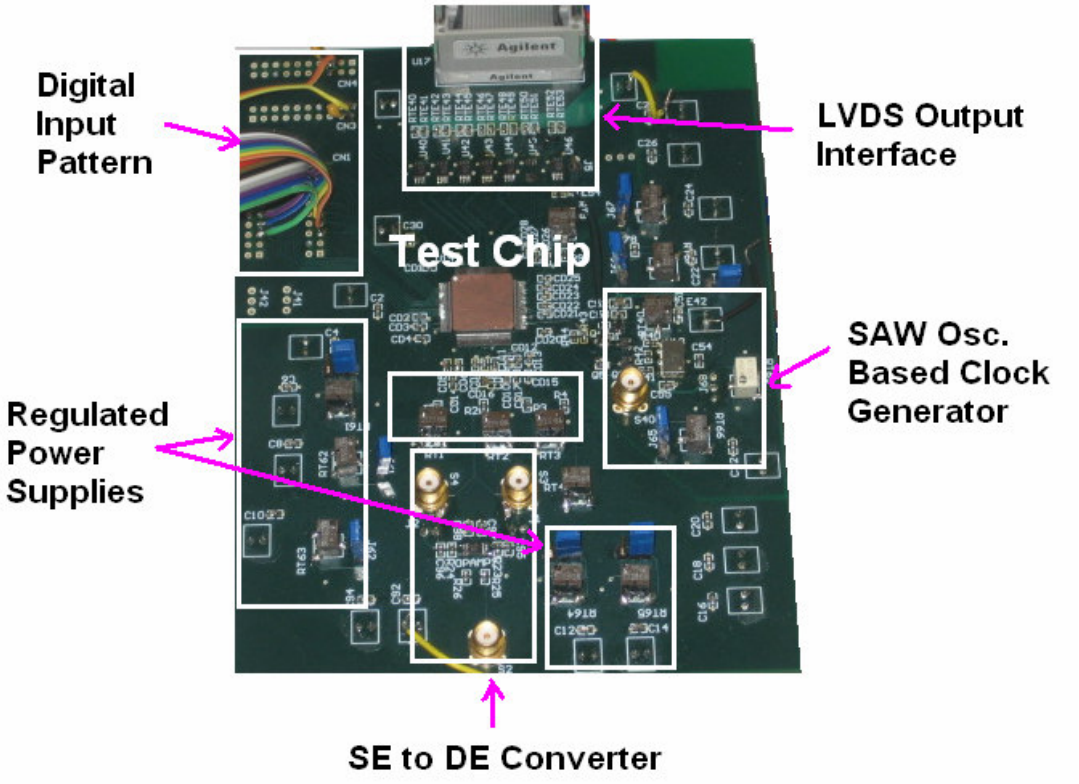


Fig. 4.36 Characterization board.

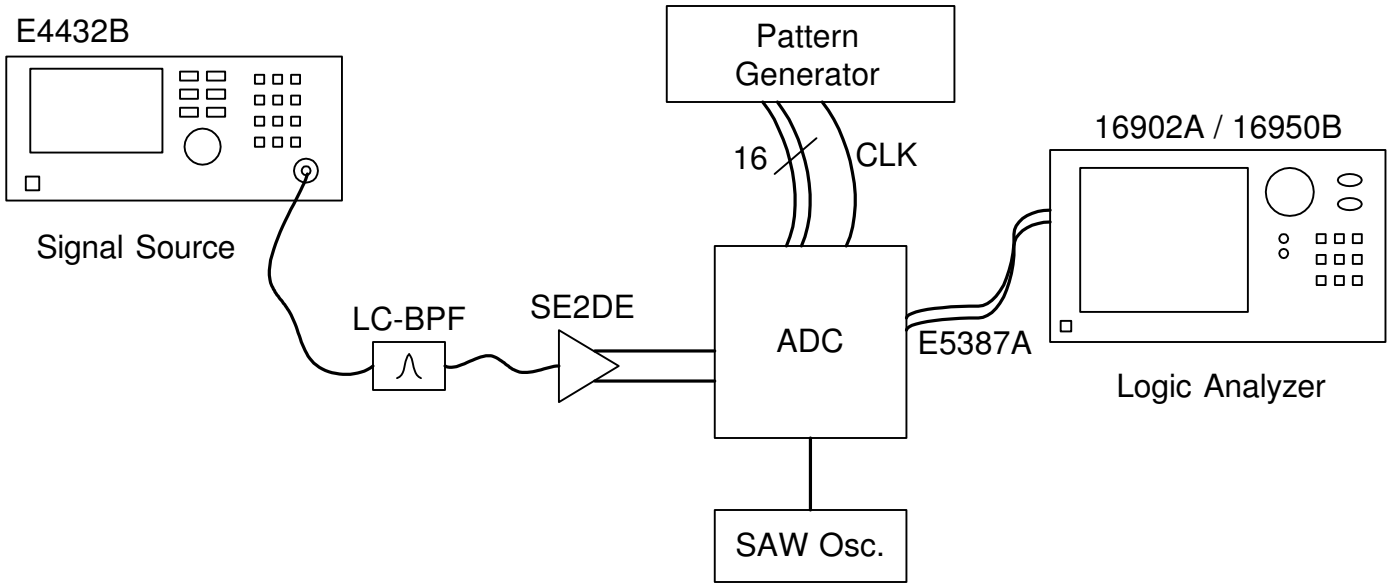
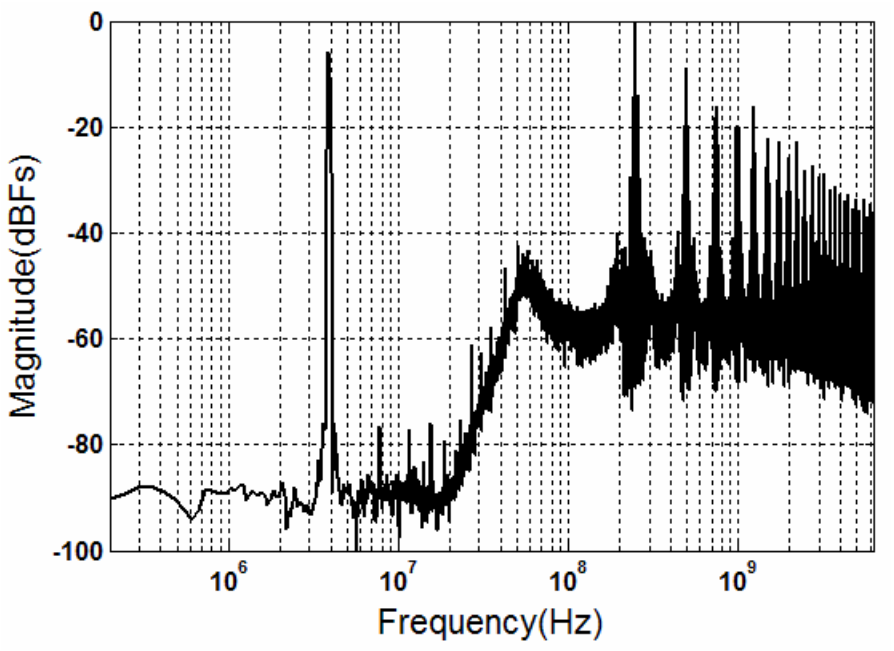
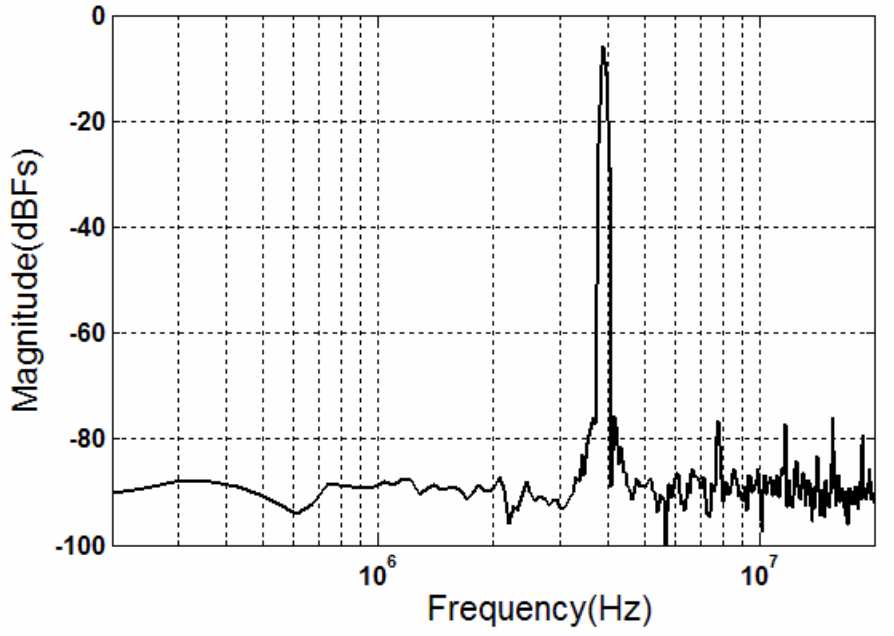


Fig. 4.37 Test setup used for characterization of the ADC.

The data captured from the logic analyzer represents the quantized pulse timing edges and are used to reconstruct the PWM waveform in MATLAB. Fig. 4.38(a) shows the measured spectrum of the reconstructed output data stream captured from the test setup described above. The noise shaping effect of the delta-sigma loop can be clearly seen in the zoomed area of the spectrum shown in Fig. 4.38(b). A plot of signal to noise ratio (SNR) and the signal to noise+distortion ratio (SNDR) for various amplitudes of the input signal is shown in Fig. 4.39. From the measurements shown in Fig. 4.39, the dynamic range (defined as the amplitude range for which the SNR is above 0dB) is found to be 68dB. The peak SNR and signal to noise and distortion ratio (SNDR) are about 62dB and 60dB respectively and are observed at -5dBFs input level. The peak total harmonic distortion (THD) is about 67dB and occurs at -6dBFs input level. These measured results closely match the design and simulation results.



(a)



(b)

Fig. 4.38 (a) Output spectrum. (b) Spectrum in 20MHz frequency band.

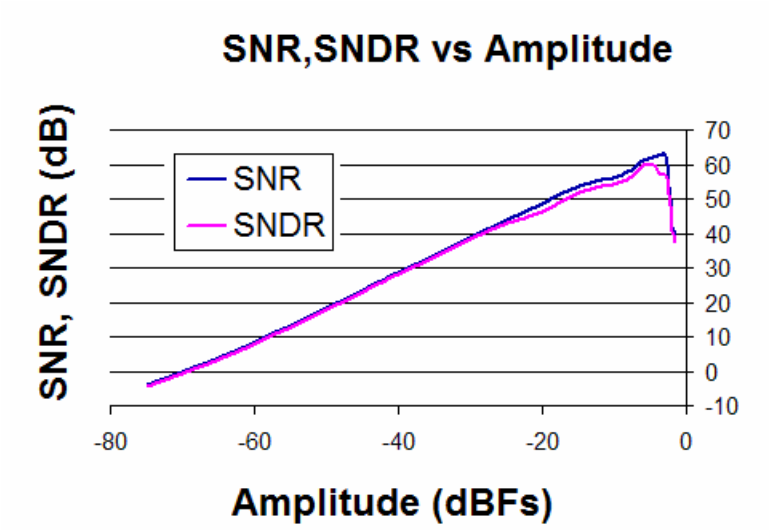


Fig. 4.39 SNR and SNDR across signal amplitudes.

Table 4.4 compares the performance of the proposed ADC with that of the state-of-the-art delta-sigma ADCs with no calibration. The typical figure of merit (FOM), used to assess the power efficiency of ADC in terms of energy used per conversion step, is given by Power/(2.BW.2^{ENOB}). The FOM of the proposed ADC compares favorably with the state-of-the-art. It is important to note that the output data rate of the proposed ADC is much smaller compared to other ADCs in the Table 4.4. This results in slower clock frequency for the digital decimation filters following the modulator, which can reduce the overall power in case of the proposed ADC. As the technology scales down, the reduction in decimation filter power becomes less significant due their reduced share of the overall power consumption. However, the proposed ADC would continue to save power in the TDC block, while the amplitude domain quantizer of the conventional architecture does not. Thus, the overall power efficiency is projected to improve in case of the proposed ADC architecture.

Table 4.4 Comparison of performance of the proposed ADC with state-of-the-art.

	[61]	[52]	[40]	Proposed
SNDR (dB)	69	55	70	60
Power (mW)	56	38	27.9	10.5
FOM (fJ/Step)	298	2058	270	319
Area (mm^2)	0.5	0.19	1.0	0.15
Output Rate (MSPS)	680	950	420	250

4.6 Summary

This work has demonstrated the first time-to-digital converter based ADC in silicon. Sub pico-second time edge matching is experimentally proven. The proposed architecture not just works around scaled technology limitations but leverages its strength. The ADC prototype built for 20MHz bandwidth using the proposed architecture provides 68dB while consuming 10.5mW. Power consumption is projected to reduce further along with technology scaling.

4.6.1 Future Work

It is shown in this work that an ADC built using the proposed method achieves about 70dB SQNR. The SQNR can be improved further by using more number of quantization steps within a clock period. In other words, the time quantization step can be reduced from 80pS to say 40pS. This would result in increased loop delay in the feedback pulse generation path but can be tackled by designing the loop delay compensation appropriately. The limitation, however, eventually arises from the timing mismatch of the delay elements in the TDC. This mismatch limits the distortion performance to about 65dB in the current design. Obviously, the matching can be improved but increasing the size of the delay cells, which increases the area and potentially the power consumption of the TDC. Digital calibration can be used to reduce the error introduced due to timing mismatch. If the processing overhead can be tolerated, this opens up the possibility of improving the dynamic range of the ADC by spending only the additional power required to reduce the thermal noise.

CHAPTER V

CONCLUSIONS

5.1 Summary

New architectures that achieve low power consumption for various mixed signal building blocks were proposed. Specific results from prototypes of a 72mW, 1.1GHz active LC equalizer, a 1.2mW, 16Ω headphone driver and a 10.5mW, 20MHz bandwidth, 68dB dynamic range ADC were presented. The presented active-LC equalizer architecture improves the power efficiency over the conventional Gm-C equalizers by over 6 times. It is shown that the power benefits can be achieved with no area penalty for sufficiently large frequencies and SNR. The proposed 16Ω headphone driver can handle capacitive loads ranging from 1pF to 22nF while being competitive in power with respect to headphone drivers that are restricted to narrow load range. Its power efficiency is an order of magnitude better than existing ones that can support such a wide range of capacitive loads. The ADC prototype based on the proposed architecture achieves power efficiency competitive with state-of-the-art and is expected to improve its power efficiency along with technology scaling.

All of the new architectures that are presented are compatible with deep-submicron CMOS technologies. This aspect enables easy integration on single chip solutions so that cost reduction of the overall system is achieved.

5.2 Possible Area for Future Work

The technology scaling enables faster and power efficient devices and would continue to remain a major driving force in consumer electronics industry. The design of pure analog circuits like operational amplifiers, however, gets increasingly difficult in scaled technologies. The ADC architecture proposed in this thesis solves this problem for quantizer and the feedback element by replacing analog circuits with digital circuits by using time domain signaling technique. However, the loop filter remains purely analog and it continues to be plagued by the side effects of technology scaling. There are fundamentally two different research directions that may be followed. First one is to come up with robust inverter based amplifiers that supports large voltage swings to beat the noise limitation while providing the required linearity performance. This should ensure small area as well as best possible power efficiency achievable for a given supply voltage. The second direction would be to rethink the receiver/transmitter architecture of the communication system such that they recognize the fact that nanometric technologies are not efficient in handling signals in amplitude domain. This would essentially mean that the digital modulation schemes that improve spectral efficiency by using the amplitude dimension (such as M-ary quadrature amplitude modulation) would be extremely inefficient in terms of power. Although these schemes are inevitable in many cases, short range communication system such personal area network, where the spectral efficiency is not an issue, can adapt modulation schemes that requires only two levels of amplitude. There is a possibility of a power efficient digital communication system that uses purely digital circuits for most of the signal processing.

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