Jitter Aware Economic PDN Optimization with a Genetic Algorithm

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***Abstract*—This paper proposes a jitter aware decoupling placement optimization method for capacitors that uses the genetic algorithm (GA). In addition, a novel method for defining the optimization target function in regard to power delivery network (PDN) optimization based on the GA-based tool is proposed. The proposed method can provide an optimum and economic solution for the number of decoupling capacitors to use in a power delivery network (PDN). In addition, by modifying the optimization target function with our proposed method, an optimum solution regarding both the number of decoupling capacitors and the power source induced jitter (PSIJ) can be obtained. The PSIJ analytical expressions are derived in conjunction with a resonant cavity model that includes the coordinates of the decoupling capacitors and the PSIJ transfer function. The GA-based optimization algorithm with the proposed target function is first applied to optimize the number of decoupling capacitors, and then, the PSIJ is taken into account. A comparison between these two cases is made, with the results proving the efficiency of our proposed method. Finally, the measured jitter from HSPICE simulation results is used to verify our optimization method, such that both the simulated results and analytically calculated results support the efficiency of our proposed optimization method.**

***Index Terms*—PDN, Jitter, PSIJ, Decoupling capacitor, Genetic algorithm, Power integrity**

I. Introduction

BECAUSE high-speed applications have spread to all types of electronics, the operating data rate of a typical device can now reach hundreds of Gb/s. Meanwhile, the size of modern electronics has decreased significantly, either consistent with Moore's law or, in some cases, even surpassing it [1]. Some of the challenges that have previously been ignored now must be taken into account. One of the most challenging tasks for electronic designers is maintaining the power and signal integrity in a high-speed system while reducing cost [2], [3]. In addition, due to the incorporation of a large number of transistors inside the typical integrated circuit (IC), the current level of the power traces can reach values as great as 100 A [4]. Such large currents generate significant supply voltage fluctuations if the power delivery network (PDN) is not well designed. The induced supply voltage fluctuations significantly affect both the signal and power integrity (SI and PI). Aside from the large current generated by the on-chip circuit, the sub-systems of a typical high-speed system, such as its voltage regulator modules (VRMs), interconnects, and packages, also remain significant problems for the SI and PI.

The SI and PI normally interact in high-speed systems and correspond, respectively, to the signal quality and power delivery quality. The major SI and PI issues include reflection, insertion loss, crosstalk, ground bounce, simultaneous switching noise (SSN), etc. [5]. The first three issues are current questions for the SI, while the latter two items concern the PI. In high-speed applications, SSN is a significant problem for both SI and PI engineers, because the SSN generates noise in the PDN network that also impacts the SI in terms of timing variations at the data/clock output [6]. In particular, a high SSN affects the supply noise by that can cause signal distortion, jitter, and bit error rate (BER) [7].

Time variation remains a challenging issue in high-speed designs and is also known as the jitter that occurs at the transition edges of the clock and data signals. Time variation can be defined as the timing difference at the transition edges from their ideal positions. The jitter in a high-speed system is categorized as either random jitter (RJ) or deterministic jitter (DJ) [8]. The deterministic jitter can be characterized by different methods. Many investigations have been carried out on power supply-induced jitter (PSIJ) [7], which is one type of DJ. The jitter budget can be achieved by minimizing the PSIJ for some high-speed applications such as USB, DDR, PCIe, etc. For a post-product validation, the jitter can be measured by using a phase analyzer [2], [9], jitter analyzer, or oscilloscope, among others. However, for a pre-layout design, only simulations are possible to evaluate the jitter performance. To study PSIJ, PDNs need to be included. Due to the distribution characteristics of PDNs at high frequency, the layout parasitic capacitance and inductance can not be ignored in the PDN design for high-speed applications. As the behavior of the power/ground plane pair that supports the radial wave propagation grows increasingly complex, lumped models are no longer efficient for the characterization of PDN performance.

The placement of the decoupling capacitors in a device significantly influences its performance [10]–[12]. In previous studies [13]–[15], different effective decoupling regions of decoupling capacitors were investigated, in which the influence of their placement was analyzed based on the resonant cavity model, which is known to support high-frequency PDN perfor-

Manuscript received xxx. This work was supported in part by the National Science Foundation under Grant No. IIP-1916535. *Corresponding author: Zihao Wang, Chulsoon Hwang.*

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mance characterization. The resonant cavity model has been employed to efficiently compute the optimal locations of the decoupling capacitors based on the Newton iteration method [16], [17]. However, this kind of method is only applicable to a single capacitor at a single frequency point. Recently, an investigation of the placement of multiple capacitors over a frequency band was proposed in [18]. However, the method that those authors applied was still fundamentally an iteration method used for frequencies, where the frequency points at the peaks of the PDN impedance curve were selected individually to optimize the decoupling capacitor positions to decrease the PDN impedance curve. This method is not suitable for PSIJ optimization, in part because the proposed methods are based on single frequency point optimization, which means that for each optimization only one frequency is used. However, because the PSIJ is a time-domain phenomenon, an integration process over the entire frequency band with all decoupling capacitors is necessary. Another important issue is that PDN optimization is normally based on the target impedance definition [18]. When the target impedance is satisfied with a certain number of decoupling capacitors, different locations and types of decoupling capacitors also exhibit differences in terms of jitter. The existing studies or tools can only consider the target impedance, such that once the target impedance is met, the optimization process or search is stopped. However, because other schemes with the same number of decoupling capacitors but different locations can meet the target impedance, these overlooked schemes could offer better jitter performance.

Therefore, the placement of the decoupling capacitors must be simultaneously optimized for all of the frequency points to reduce the jitter and achieve a clean power supply. In this paper, a new target problem definition is proposed to achieve the goal of an economic number of decoupling capacitors and its minimum associated PSIJ. Section II presents the analytical derivations of the PSIJ, including PDN cavity models and the PSIJ transfer function. The coordinates of the decoupling capacitors are considered in the PDN resonant cavity model. The derived analytical expressions are integrated into our proposed method in section III. Section IV examines our optimization algorithm by comparing both the PDN impedance and jitter results for two case studies. In section V, the optimized results are verified with an HSPICE simulation. Finally, the achievements and weaknesses of the proposed method are analyzed in Section VI.

II. Jitter Aware Analytical PDN Impedance Derivation

Analytical expressions for the PSIJ that consider the placement of the decoupling capacitors are presented in this section. The PSIJ can be reduced by optimizing the coordinates and number of decoupling capacitors through the derived expressions.

A. Cavity model-based matrix expression of the power/ground plane pair with multiple capacitors

The cavity model's expression has been widely used to compute the impedance matrix of a power/ground pair [11], [13]:

$$Z_{ij} = \frac{j\omega\mu d}{ab}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\frac{c_m^2 c_n^2 F_{PO} F_{CO}}{k_m^2 + k_n^2 - k^2} \tag{1}$$

where a and b are the width and length of the plane pair; d is the dielectric thickness; c_m and c_n are, respectively, the mode types and the wave guide number k; C_m and C_n are the coefficients of the m^{th} and n^{th} modes along the edges of the cavity, respectively, cm and cn are equal to 1 for $m, n = 0$ and $\sqrt{2}$ for $m, n \neq 0$; k is the wave number, $k_m = m\pi/a$; $k_n = n\pi/a$; and F_P and F_C, as calculated below, representing the port size and decoupling capacitor coordinates functions, respectively [13].

$$k = \omega\sqrt{\mu_d \varepsilon_d}\cdot\left(1 - j\left(\frac{\tan\delta + \sqrt{2/\omega\mu_c\sigma_c}/d}{2}\right)\right) \tag{2}$$

$$F_P = \mathrm{sinc}\frac{k_m W_{xi}}{2}\cdot\mathrm{sinc}\frac{k_n W_{yi}}{2}\mathrm{sinc}\frac{k_m W_{xj}}{2}\cdot\mathrm{sinc}\frac{k_n W_{yj}}{2} \tag{3}$$

$$F_c = \cos k_m x_i \cdot \cos k_n y_i \cdot \cos k_m x_j \cdot \cos k_n y_j \tag{4}$$

where (W_{xi}, W_{yi}) and (W_{xj}, W_{yj}) are the dimensions of ports i and j, both of which are very small in comparison to the plane dimension and, therefore, are ignored in this paper. (x_i, y_i) and (x_j, y_j) are the coordinates of ports i and j, respectively.

Based on a matrix expression of the power/ground plane pair with multiple decoupling capacitors as developed in [19]:

$$\mathbf{Z} = (\mathbf{E} + \mathbf{Z_{pg}} * \mathbf{Y_C})^{-1} * \mathbf{Z_{pg}} \tag{5}$$

where $\mathbf{E}$ is a unit matrix, the impedance matrix $\mathbf{Z_{pg}}$ of the bare power/ground plane without any decoupling capacitors is obtained through the equation in (1). $\mathbf{Y}$ is the conductance matrix of all of the added capacitors, VRM impedance, etc. and can be expressed in a diagonal matrix as:

$$\mathbf{Y} = \begin{pmatrix} 0 & 0 & 0 & \cdots & 0 \\ 0 & Y_{VRM} & 0 & \cdots & 0 \\ 0 & 0 & Y_{C1} & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & Y_{CN} \end{pmatrix} \tag{6}$$

N represents the number of capacitors applied in the PDN optimization. Y_{VRM} and Y_C represent the admittance of the VRM and the capacitors. The diagonal element will be zero if an IC port is added, such as the first element. Every component in $\mathbf{Y}$ has its own coordinate, and all of the coordinates (x, y) shown in (7) will be put into equation (1) to obtain the bare power/ground plane impedance $\mathbf{Z_{pg}}$ with the same size as $\mathbf{Y}$.

$$(x, y) = \begin{bmatrix} x_{IC} & x_{VRM} & x_1 & \cdots & x_N \\ y_{IC} & y_{VRM} & y_1 & \cdots & y_N \end{bmatrix} \tag{7}$$

where (x_{IC}, y_{IC}) and (x_{VRM}, y_{VRM}) are the coordinates of the IC port and VRM, respectively. (x_p, y_p) with $p = \{1, ..., N\}$ are the coordinates of the decoupling capacitors.

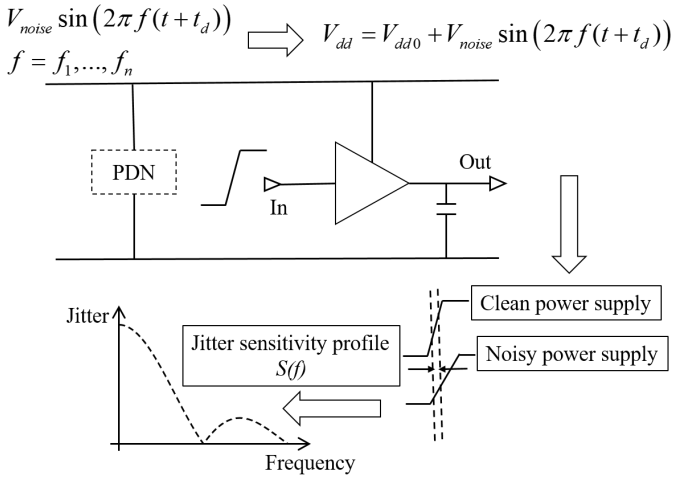

Fig. 1. Circuit system for PSIJ sensitivity transfer function establishment.

Looking from the IC port, the impedance is represented as Z_{pdn}, which is the first element of matrix **Z**. The magnitude of Z_{pdn} is defined by the following expression:

$$Z_{pdn}(x_p, y_p, f) = |Z(1,1)| = \sqrt{Z(1,1)Z(1,1)^*} \quad (8)$$

where $p = \{1, ..., N\}$ with N is the number of different capacitors applied.

B. Frequency domain PSIJ transfer function

The jitter caused by the supply fluctuation is defined as continuous time interval error (CTIE). The peak-to-peak value of the CTIE is used to define the PSIJ. The CTIE, as described in [20], [21], covers all of the possible time interval error values if no fixed phase relationship is added. The frequency domain PSIJ is determined based on two factors. One is the supply fluctuation noise spectrum $V(f)$, and the other is the dependent PSIJ sensitivity transfer function $S(f)$ [22], [23]. The following expression is usually adopted to describe the transfer relationship between the power supply fluctuations to PSIJ [7], [24].

$$J(f) = V(f) \cdot S(f) \quad (9)$$

The supply fluctuation noise can be calculated as shown in (10) when the impedance of PDN and the current spectrum are available.

$$V(f) = Z_{pdn}(x_p, y_p, f) \cdot I_{ICnoise} \quad (10)$$

The PSIJ sensitivity transfer function in a real application can be obtained through the system with PDN responding to an input stimulus, as shown in Fig. 1. By sweeping the frequency of the single-tone sinusoidal wave in a dedicated frequency band, the PSIJ sensitivity transfer function can be established as shown at the bottom of Fig. 1. The x- and y-axes represent the single-tone frequencies and the PSIJ sensitivity amplitude, respectively.

An analytical method based on propagation delay is usually used to extract $S(f)$ for the IC without PDN on the PCB. The $S(f)$ is analytically expressed as a $sinc$ function, as given below [25]:

$$S(f) = \frac{T_{pmaxDC} - T_{pminDC}}{VDDmax - VDDmin} sinc(f \frac{T_{pmaxDC} + T_{pminDC}}{2}) \quad (11)$$

The PSIJ sensitivity transfer function is determined by the maximum and minimum propagation delays (T_{pmaxDC} and T_{pminDC}), as well as the corresponding maximum and minimum DC power supplies (VDD_{max} and VDD_{min}), which can be extracted from either the datasheet or the operating conditions. With the optimized PDN impedance, the time-domain PSIJ can be obtained by using the inverse discrete Fourier transform over the frequency band, as shown in (12) [7], [24].

$$j(t) = \frac{1}{N} \sum_{n=0}^{N-1} J(f) e^{j\frac{2\pi n}{N} f} \quad (12)$$

Then, the peak-to-peak PSIJ can be obtained:

$$j_{pp} = Max(j_{(t)}) - Min(j_{(t)}) \quad (13)$$

To optimize the decoupling capacitor placement in regard to the number and PSIJ, the IC current noise source and PSIJ sensitivity transfer function are assumed to be known. Therefore, the PSIJ optimization becomes a question of optimizing the integration of Z_{pdn} over the desired frequency band. As the derivations of Z_{pdn} are carried out from (1) to (7), the optimization question changes to optimize the coordinates of the decoupling capacitors to meet the target impedance with a minimum number of decoupling capacitors and its minimum associated PSIJ.

III. Optimization with Utility Maximization

Four sets of variables exist in this optimization question:

- The frequency, which is a known discrete vector with a large size that normally includes hundreds to thousands points, depending on the application.
- The number of capacitors.
- The coordinate vector variables of the decoupling capacitors, which include x and y with the same size.
- The indexes of the capacitors, which is also a vector variable with the same size as the coordinates vector.

All of these four groups variables are interacted with each other. The coordinates and indexes of capacitors are optimized over the desired frequency band to obtain a minimum number of decoupling capacitors which can meet the target impedance and have minimum associated PSIJ. The traditional optimization methods cannot handle such a complex problem, as explained in Section I. Therefore, a GA-based method is proposed in this section.

A. Heuristic optimization algorithm

Heuristic optimization methods have been applied for many high-dimensional non-linear constrained optimization problems. The original groups of heuristic optimization algorithms

were mostly inspired by physical or biochemical processes in the natural environment. Recent works on artificial intelligence successfully applied heuristic optimization algorithms for complex system optimization tasks, such as neural network reasoning [26], robot path planning [27], and SARS-CoV-2 drug design [28]. The genetic algorithm (GA) is one of the best-known heuristic frameworks for solving such non-linear optimization tasks, including our targeted problem. The decoupling capacitor placement optimization can be treated as a discrete constrained non-linear optimization task, in which both the number of decoupling capacitors and the magnitude of PDN impedance in a corresponding frequency band are constrained. The optimization variables include the positioning and selection of the capacitors. To employ the GA algorithm to optimize the placements of the decoupling capacitors, we must mathematically define the optimization loss function of the problem.

B. Formal definition of the target problem

First, we construct a loss function by considering the number of capacitors and PDN impedance. The convergence condition is that the PDN impedance must be less than a certain level within a defined frequency band.

Our argument variables include:

1) The variable m encodes the action of selecting a combination of capacitors $C' \subseteq C$ from a set of capacitors $C : \{c_p \in C, p \in \mathcal{N}\}$, where p is the index of the corresponding capacitors.
2) Variables (x_p, y_p) indicate the placement position of the selected capacitor $c_p(x_p, y_p)$.

The selection matrix $\mathbf{M}$ is an encoder matrix that indicates whether or not the corresponding capacitors have been selected. We can define $\mathbf{M}$ as a binary diagonal matrix,

$$\mathbf{M} = \begin{pmatrix} 1 & 0 & 0 & \cdots & 0 \\ 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & m_1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & m_N \end{pmatrix}, \mathbf{m_p} \in \{\mathbf{0}, \mathbf{1}\} \tag{14}$$

where the first two diagonal elements are defined as one because they are related to the port and the VRM, which have the defined coordinates but none of the capacitors are attached. $m_p = 1$ means that the capacitor c_p is selected, or vice versa. Therefore, the updated (x', y') becomes:

$$(x', y') = (x, y) * \mathbf{M} \tag{15}$$

and the updated $\mathbf{Y}'$ becomes:

$$\mathbf{Y}' = \mathbf{Y} * \mathbf{M} \tag{16}$$

Next, we rewrite (5) by introducing the selection matrix (14) as:

$$\mathbf{Z} = (\mathbf{E} + \mathbf{Z_{pg}}(x', y', f) * \mathbf{Y} * \mathbf{M})^{-1} * \mathbf{Z_{pg}}(x', y', f) \tag{17}$$

The magnitude of $Z_{pdn}(x', y', f)$ and $j_{pp}(Z_{pdn})$ can be computed through (8) and (13).

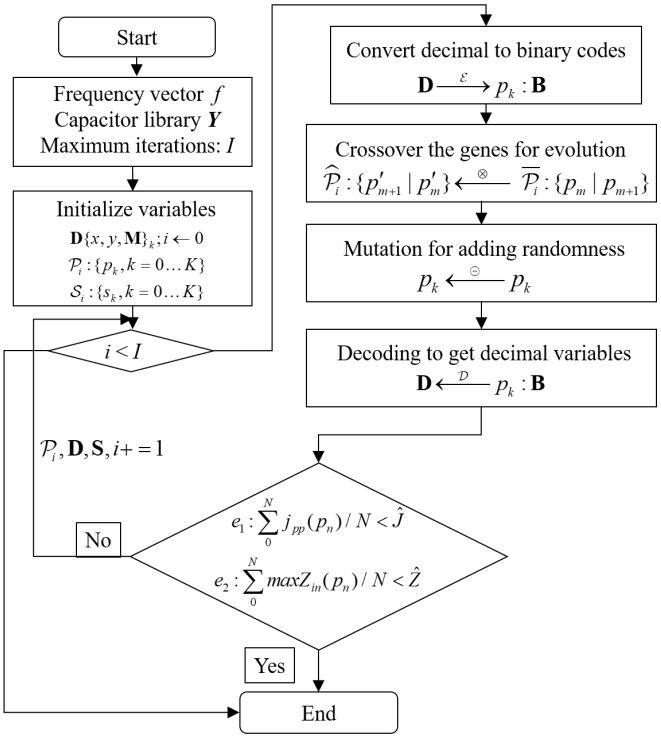

Fig. 2. Diagram for showing the genetic algorithm applied for decoupling capacitor placement.

The direct minimization of (8) would lead to a full selection of the available capacitors, which is not desired. Thus, we must constrain the optimization target by considering the number of capacitors selected, which would be the trace $\mathbf{tr}(\mathbf{M})$ of the selection matrix $\mathbf{M}$. By considering the number of capacitors, we now define the optimization target as:

$$\begin{aligned} \underset{x,y \in \mathbf{R}^N, m_i \in \{0,1\}}{\arg\max} \quad & T(x, y, f, \mathbf{M}) = \\ & Z_{pdn}(x, y, f, \mathbf{M}) \cdot \mathbf{tr}(\mathbf{M}) \\ \mathbf{s.t.} \quad & max(Z_{pdn}(x, y, f, \mathbf{M})) < \hat{\mathbf{z}} \end{aligned} \tag{18}$$

The optimization of equation (18) only considers the target impedance and the number of decoupling capacitors; the PSIJ is not considered. Since the approximations of the PSIJ transfer function is not avoidable, meeting a defined PSIJ criterion will easily induce overestimation or underestimation problems. Therefore, by playing with the optimization target, as shown in (19), when the target impedance is met, the optimization results can output a minimum number of decoupling capacitors with a minimum PSIJ. Compare to meeting a PSIJ criterion, our proposed method is trustful in real applications.

$$\begin{aligned} \underset{x,y \in \mathbf{R}^N, m_i \in \{0,1\}}{\arg\max} \quad & T(x, y, f, \mathbf{M}) = \\ & j_{pp}(x, y, f, \mathbf{M}) \cdot \mathbf{tr}(\mathbf{M}) \\ \mathbf{s.t.} \quad & max(Z_{pdn}(x, y, f, \mathbf{M})) < \hat{\mathbf{z}} \end{aligned} \tag{19}$$

The defined target function leads the optimization problem to an inequality constructed non-linear mixture integer optimization, which can be tackled by the GA algorithm. The output of the optimization gives an economic solution to the

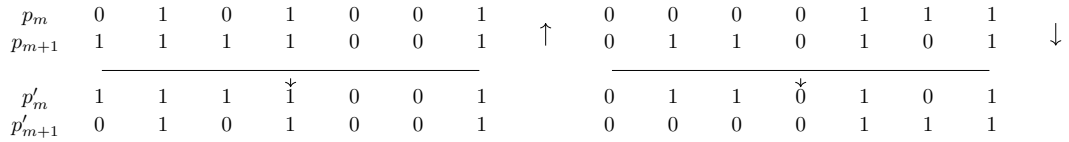

Fig. 3. Diagram demonstrating the genetic chain cross-over process. Two genetic chains p_m and p_{m+1} are exchanging their gene fragments (p_m swap half-segments with p_{m+1}), resulting in two new genetic chains.

number of decoupling capacitors and the minimum associated PSIJ.

C. GA optimization for decoupling capacitor placement

The GA algorithm is based on Charles Darwin's theory of natural selection and the principal of genetic biological inheritance. Because the frequency variable is a known vector, to leverage the GA method for capacitor placement, we must consider the variable set $\{x, y, \mathbf{M}\}$ that feeds the loss function (18) as an encoding genetic chain. The diagram Fig. 2 shows the workflow of the GA optimization process.

1) The decimal variables must be encoded as binary numbers (encoding step) during the initialization process for application to genetic operations. The encoding step converts the decimal variable set $\mathbf{D}\{x, y, \mathbf{M}\}$ to a binary code set $\mathbf{B}\{x, y, \mathbf{M}\}$ to use genetic theories for evolution.
2) The group of different binary encoded chains (species) consists of the population set $\mathcal{P}_i\{p_n\}$ that contains the status of the different capacitors. The chains correspond to various variables that can be used for calculating the corresponding target function score.
3) All of the genetic chains are allocated with a score that can be computed from (18). The score represents the quality of the genetic chain (specie). An evolution probability function $P(i, T(x, y, f, \mathbf{M}))$ is defined by the bias weight placed on the high-scoring species that leads the higher-scoring species to be preferred for the selection for crossover.
4) The species are randomly sampled from the population $\mathcal{P}_i$ intended for crossover, to generate the next generation's species. The crossover step of two genetic chains exchange partial gene segments, as shown in Fig. 3.
5) For the crossover-generated species, a subset of species with the probability of $P_{mutations}$ is selected, and then, one Bit of the genetic chain is randomly inverted and put back into the species set from which the next population $\mathcal{P}_{i+1}$ is obtained.
6) Perform the iterative evolution process until the average score of the population arrives at a certain threshold or satisfies the constraint functions (equation e_1 and e_2), then return the final population and corresponding scores.

A detailed pseudo algorithm describes in detail the full optimization procedures, which can be found in *Algorithm 1*.

Algorithm 1: GA optimization for PDN capacitor placements.

Inputs: Frequency vector f; Capacitor Library $\mathbf{Y_C}$; Maximum iterations: I
Output: Last population $\mathcal{P}_n$ and score $\mathcal{S}_n$;
Condition: $e_1 : \sum_0^N jpp(p_n)/N < \hat{J}$
Condition: $e_2 : \sum_0^N maxZ_{in}(p_n)/N < \hat{Z}$
Condition: $\epsilon : e_1 \wedge e_2 \vee \{i > I\}$
`// Decimal to binary`
Define: Encoder $\mathcal{E} : \mathbf{B} \xleftarrow{\mathcal{E}} \mathbf{R}$;
`// Binary to decimal`
Define: Decoder $\mathcal{D} : \mathbf{B} \xrightarrow{\mathcal{D}} \mathbf{R}$
`// Sorting function: sorting array` $< A|B >$ `based on key array B`
Define: Sort $\Omega : \mathbf{A}|\mathbf{B} \xrightarrow{\Omega} \mathbf{A}'|\mathbf{B}'$
Define: Crossover $\otimes$
Define: Mutation $\ominus$
Initialize variables $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k}$; $i \leftarrow 0$
$\mathcal{P}_i : \{p_k, k = 0 \dots K\}$
$\mathcal{S}_i : \{s_k, k = 0 \dots K\}$
while $NOT\ \epsilon$ **do**
  `// The population size is` K
  for $k = 0; k < K; k++$ **do**
    `// Get genetic chain` $\mathbf{B}_k$
    Encoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xrightarrow{\mathcal{E}} \mathbf{p_k} : \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
    Decoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xleftarrow{\mathcal{D}} \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
    `// Computing species score` $\mathcal{S}_k$
    $s_k \leftarrow T(\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k})$
  end
  `// Sorting pairs on the scores`
  $(\mathcal{P}_i|\mathcal{S}_i) \xrightarrow{\Omega} (\mathcal{P}_i|\mathcal{S}_i)$
  `// Take` $2 \times M$ `species based on score ranking for crossover`
  $\bar{\mathcal{P}}_i \xleftarrow{P(i,\mathcal{P}_i|\mathcal{S}_i)} \mathcal{P}_i$
  for $m = 0; m < 2 \times M; m + 2$ **do**
    Crossover $\hat{\mathcal{P}}_i : \{p'_{m+1}|p'_m\} \xleftarrow{\otimes} \bar{\mathcal{P}}_i : \{p_m|p_{m+1}\}$
  end
  $\mathcal{P}_i \leftarrow \hat{\mathcal{P}}_i \cup \{\mathcal{P}_i \setminus \bar{\mathcal{P}}_i\}$
  for $k = 0; k < K; k++$ **do**
    Mutation $p_k \xleftarrow{\ominus} p_k$
    Decoding $\mathbf{D}\{x, y, \mathbf{M}\}_\mathbf{k} \xleftarrow{\mathcal{D}} \mathbf{p_k} : \mathbf{B}\{\mathbf{x}, \mathbf{y}, \mathbf{M}\}_\mathbf{k}$
  end
  $i \leftarrow i + 1$
end

IV. Jitter Aware Decoupling Capacitor Placement Optimization

In this section, the optimization algorithm has been applied to meet the target impedance first by optimizing the coordi-

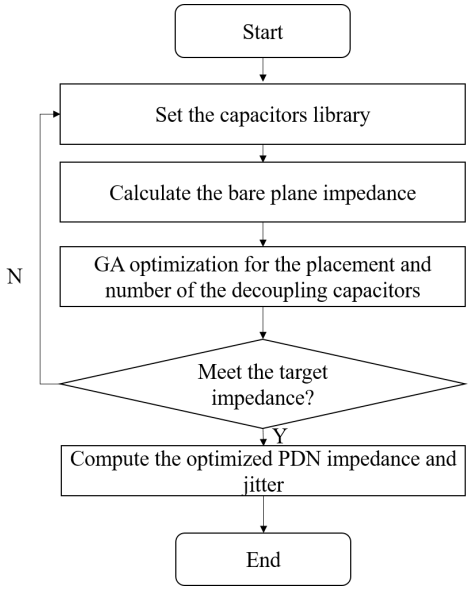

Fig. 4. Jitter aware decoupling capacitor placement optimization methodology.

nates and number of decoupling capacitors. Then the algorithm is applied to optimize both the target impedance and PSIJ.

A. Algorithm process for jitter aware decoupling capacitor placement optimization

Fig. 4 shows the workflow of the PSIJ optimization process. The general algorithm process is described as follows:

1) Compute the bare plane PDN impedance without any capacitor in place.
2) Set the capacitor library.
3) Optimize the location and number of the decoupling capacitors.
4) If the optimized results meet the target impedance, then the process moves on to the next step; else, the process goes back to step 2, and the capacitor library must be increased.
5) Finally, the optimized scheme with its minimum associated PSIJ and number of decoupling capacitors is obtained.

B. Decoupling capacitor placement optimization based on the proposed method

In this case, the target function from (18) is applied to obtain the minimum number of decoupling capacitors needed to meet the target impedance, while the PSIJ is not considered. The proof-of-concept (POC) is designed as shown in Fig. 5. In this case, the power plane pair consists of two 100 mm × 100 mm planes with a 0.1-mm dielectric thickness, 0.035-mm conductor thickness, and dielectric constant 4.4. The input port is located at (15 mm, 40 mm) on the plane, and the VRM is located at (5 mm, 7 mm). The decoupling capacitors are placed near the port in a square region from position (20 mm, 20 mm) to (60 mm, 60 mm). However, the capacitors located at different positions in this square region will have different

TABLE I
DECOUPLING CAPACITOR LIBRARY

Type	C (nF)	ESR (mΩ)	ESL (nH)
1	68	41.5	0.264
2	10	92	0.268
3	2.2	214	0.273
4	1	70	0.25
5	0.33	114	0.272
6	0.22	114	0.2
7	0.1	180	0.272
8	0.019	11.8	0.299
9	0.0082	180	0.3385
10	0.003	222.7	0.352

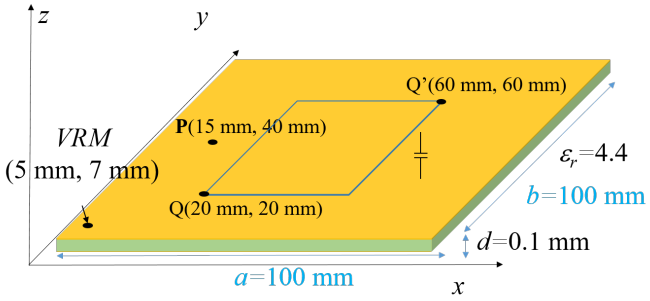

Fig. 5. Plane pair with dedicated optimization area.

performances in regard to both the PDN impedance and the PSIJ performance. The capacitor library is set as in Table I. Specifically, ten types of capacitors are set in the capacitors library. The optimization process produces a minimum number of decoupling capacitors needed to decrease the PDN impedance curve to a value less than the target impedance. In this example, the placements of the decoupling capacitors are optimized by considering only the target impedance. The target impedance is set 0.5 Ohm until 1 GHz in this case.

The impedance results, looking from Port P (15 mm, 40 mm) of the bare-plane pair without any capacitors placed, are shown as the blue solid trace in Fig. 6. After the optimization process shown in Fig. 4, the optimized results, shown as the orange dashed trace, decreased the impedance curve to less than 0.5 Ohm to a frequency of 1 GHz, in which case only 5 capacitors have been applied. Their locations are listed in Table. II. The effectiveness of the cavity model proposed in (1) has been proved by measurements in [11].

TABLE II
EMPLOYED DECOUPLING CAPACITORS AND LOCATIONS FOR THE PDN TARGET IMPEDANCE OPTIMIZATION

Type	C (nF)	ESR (mΩ)	ESL (nH)	**Location (mm)**
2	10	92	0.268	**(40.9, 43.7)**
3	2.2	214	0.273	**(57.6, 60)**
5	0.33	114	0.272	**(38.9, 36.7)**
6	0.22	114	0.2	**(20, 41.3)**
7	0.22	114	0.2	**(20. 37.1)**

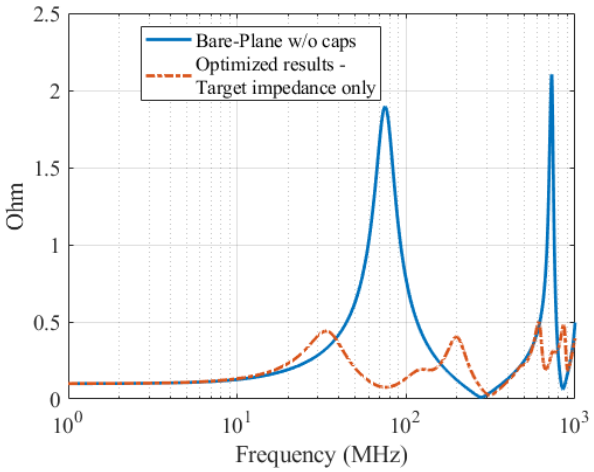

Fig. 6. Impedance comparison between the bare-plane pair and optimized results.

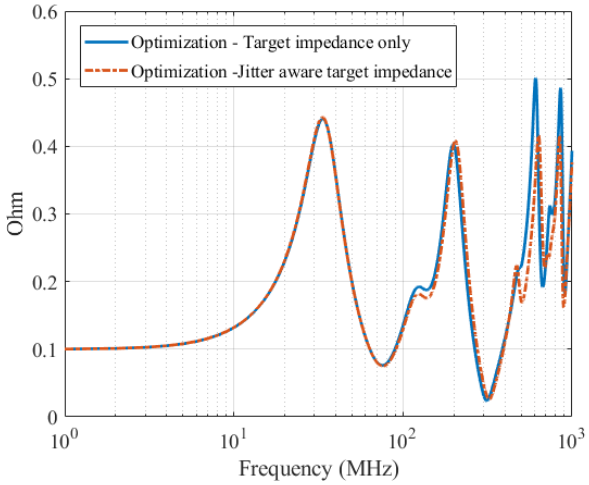

Fig. 7. Impedance comparison between target impedance optimization only and jitter aware target impedance optimization.

TABLE III
EMPLOYED DECOUPLING CAPACITORS AND LOCATIONS FOR THE JITTER AWARE PDN IMPEDANCE OPTIMIZATION

Type	C (nF)	ESR (mΩ)	ESL (nH)	**Location (mm)**
2	10	92	0.268	**(47.1, 48.6)**
3	2.2	214	0.273	**(60, 20)**
5	0.33	114	0.272	**(36.3, 30.6)**
6	0.22	114	0.2	**(20, 49.1)**
7	0.22	114	0.2	**(20. 33.9)**

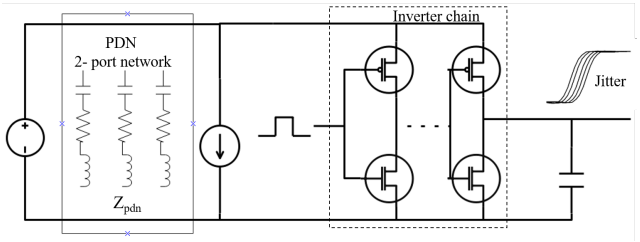

Fig. 8. Jitter simulation schematic for verification.

C. Jitter aware decoupling capacitor placement optimization based on the proposed method

The same POC is applied for the jitter aware decoupling capacitor placement optimization to obtain a comparison with the results presented in the previous section. We expected to see reduced jitter after optimization with the target function based on the PSIJ optimization defined in (19).

However, after running the optimization process with the same number and type of decoupling capacitors as used in the previous section, the positions of these capacitors are different to those of the previous case. The locations of the applied capacitors are shown in Table III.

From the curves presented in Fig. 7, the jitter aware optimization results, shown as the orange dashed trace, yield the lower impedance amplitude in the higher frequency range than the optimization performed only with the target impedance requirement. In addition, the position of the overall curve is less than the target impedance limit, until 1 GHz. The comparison results also indicate that even with the same number of decoupling capacitors, different locations of the decoupling capacitors will have different performances in regard to the PDN impedance when the target impedance is met.

The PSIJ can be calculated for these two cases with the optimized PDN impedance results and other parameters by using Eq. (10) to (13). The characteristics of the IC current source and the PSIJ sensitivity transfer function used in the PSIJ calculation are shown in Table. IV and Fig. 9, respectively. Therefore, the peak-to-peak jitters with the two optimized PDN results are calculated through Eq. (13):

- Target impedance optimization only

$$j_{pp} = 4.98\ ps \tag{20}$$

- Jitter aware target impedance optimization

$$j_{pp} = 4.38\ ps \tag{21}$$

A PSIJ reduction of approximately 0.6 ps is observed in the case of jitter aware optimization. The result shows the effectiveness of the defined target function. With the proposed optimization method, an economic solution with minimum number of decoupling capacitors can be obtained to meet the target impedance and having a minimum associated jitter value.

V. JITTER AWARE DECOUPLING CAPACITOR PLACEMENT OPTIMIZATION RESULTS VALIDATION

The HSPICE simulation is employed to show the effectiveness of our proposed optimization method. The simulation setup and results are presented in this section.

A. Simulation setup and parameter definitions

To verify our proposed optimization method by using a real application, a simple inverter chain (see: Fig. 8) is used in the HSPICE simulation. The maximum and minimum propaga-

TABLE IV
SIMULATION SETUP PARAMETERS

Characteristics	Amplitude	Period	Pulse width	Rise/Fall
Input	1.8 V	4 ns	2 ns	10 ps
Current source	80 mA	6.25 ns	0	250 ps
VDD	Nominal = 1.8 V, Max = 1.9 V, Min = 1.7 V			

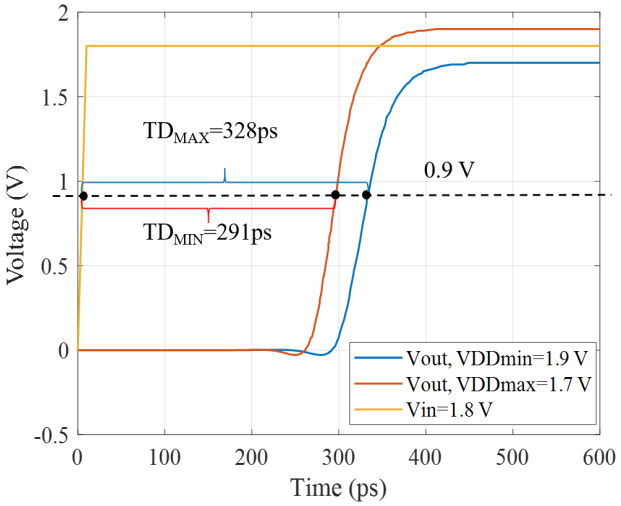

Fig. 9. Maximum and minimum propagation delays.

tion delays due to an unstable power supply can be simulated as shown in Fig. 9. As shown in Fig. 9, the propagation delays are correspond to the supply voltage, which indicates that the voltage ripples will cause the propagation delay and therefore induce the PSIJ. By substituting the obtained TD_{Max} = 328 ps and TD_{Min} =291 ps values to (11), the PSIJ sensitivity transfer function can be obtained as shown in Fig. 10. This data can be combined to previous analytical expressions to get the analytical calculated PSIJ.

The IC noise source is assumed to be a current source in a triangular waveform. The characteristics of the current source

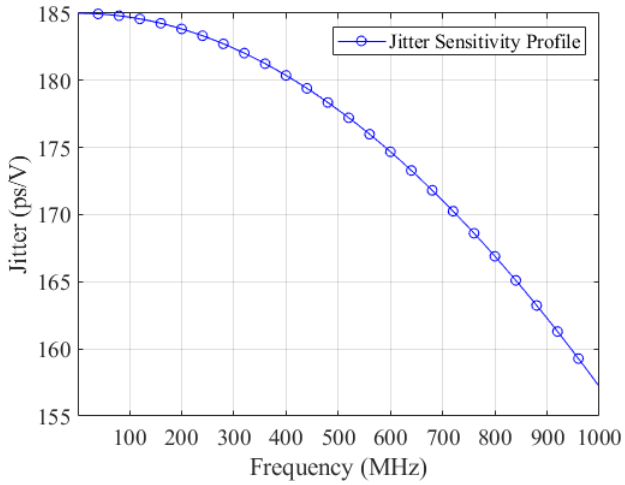

Fig. 10. PSIJ sensitivity transfer function.

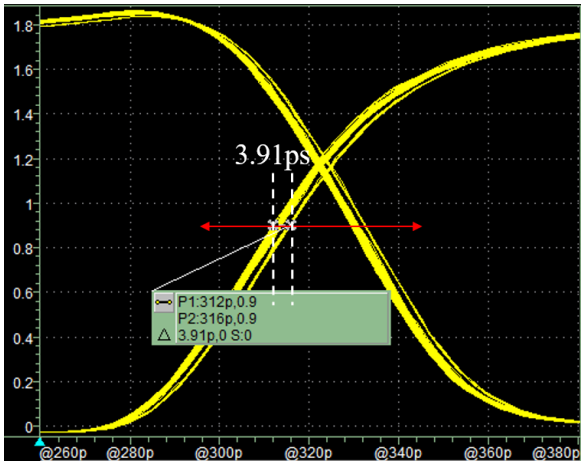

Fig. 11. Target impedance optimization only.

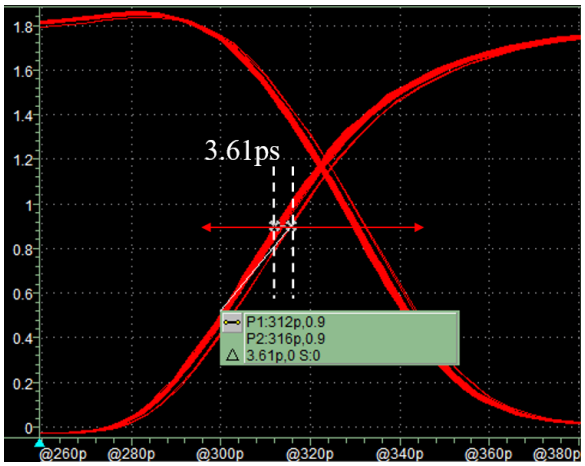

Fig. 12. Jitter aware target impedance optimization.

and all other parameters in the simulation are presented in Table. IV. The Fourier tranform will be performed for this current waveform and then combined to previous analytical expression in (10). However, in this HSPICE simulation, the transient waveform of the current source is applied.

B. Results validation

The optimized PDN impedance parameters are implemented in the transient simulations. Two optimized PDN cases are studied in the HSPICE simulation.

1) The optimized PDN parameters without considering the PSIJ; only the target impedance requirement is considered.
2) The optimized PDN parameters considering both the PSIJ and target impedance.

Fig. 11 shows the jitter simulated by using the optimized PDN impedance from case (1), where the jitter is measured at the amplitude equal to $\frac{VDD}{2}$ for the rising edges. The measured result shows a jitter with 3.91 ps, which is very close to what we calculated in Section IV-B. Since our objective is to optimize the coordinates and indexes of capacitors over the

desired frequency band to obtain a minimum number of decoupling capacitors which can meet the target impedance and have minimum associated PSIJ, this difference is acceptable. Fig. 12 shows the jitter simulated by using the optimized PDN impedance from case (2): 3.61 ps of jitter is measured in this case, which is less than in the first case. The jitter values in both the analytical solution and simulation demonstrate that our proposed optimization method for the PDN network can provide an economic solution with minimum number of decoupling capacitors to meet the target impedance, in the meanwhile, it can give us the minimum jitter among the decoupling schemes with the minimum number of decoupling capacitors.

VI. Conclusion

An analytical expression that combines the PDN impedance, which is related to the decoupling capacitor placement, and PSIJ sensitivity function is developed.

A new concept of target function definition, applied in a genetic algorithm, is proposed to optimize simultaneously the jitter and PDN impedance with a minimum number of decoupling capacitors.

A comparison of the optimization results between the optimization with the condition of target impedance only and the optimization with conditions of both target impedance and PSIJ is carried out. The results demonstrate the efficiency of our jitter aware decoupling placement optimization method. The optimized PDN impedance is simulated in HSPICE. Both the simulated and analytical results prove that the jitter is reduced by using our proposed optimization method. However, because modern electronics are heading toward communication speeds as great as 100 Gb/s, a more accurate analytical model of the PSIJ transfer function is needed in further research.

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