High performance control of a three-phase PWM rectifier using odd harmonic high order repetitive control

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Abstract

The control goal for three-phase pulse width-modulated rectifiers focuses on generating sinusoidal input currents and regulating the DC output voltage. Despite the fact that control strategies such as resonant and repetitive control have been proposed in recent works, with many notable results on the area, they have significant performance decay when the frequency changes in the exogenous signal. In this paper, it is shown that the use of an Odd Harmonic High Order Repetitive Controller can be used to control the three-phase rectifier current loops with a performance that is considerably superior to traditional alternatives developed in this field. This compensator's Odd Harmonic property keeps a computational complexity similar to that of the conventional repetitive controllers but it has the advantage of increasing the robustness when the signal frequency varies. Simulation and experimental results show the high performance that was obtained even in the case of deviation of network frequency from its nominal value.

Keywords: current control; Odd Harmonic High Order Repetitive Controller; Three- Phase PWM rectifier.

Control de alto desempeño de un rectificador PWM trifásico usando control repetitivo de alto orden

Resumen

El objetivo de control en rectificadores de potencia trifásicos se basa en generar corrientes de entrada sinusoidales y regular el voltaje de salida DC. Aunque el Control Repetitivo y Resonante son enfoques de control que han presentado excelentes resultados, su principal desventaja se basa en la pérdida considerable de desempeño cuando la frecuencia de la red se desvía de su valor nominal. En este artículo, se presenta el uso de un Controlador Repetitivo Impar de Alto Orden para controlar los lazos de corrientes de un rectificador trifásico con un desempeño considerablemente superior a otras alternativas tradicionalmente implementadas en este campo. Este controlador permite el rechazo de los armónicos impares introducidos en el sistema, lo que mantiene una complejidad computacional similar a la obtenida con los controladores repetitivos convencionales con la ventaja de incrementar la robustez cuando la frecuencia de la señal varíe. Las simulaciones y los resultados experimentales muestran un alto desempeño aún cuando se presenten desviaciones de la frecuencia de la red respecto a su valor nominal.

Palabras clave: Control de Corriente; Controlador Repetitivo de Alto Orden Impar; Rectificador PWM Trifásico.

1. Introduction

More recently, reactive power and harmonic currents generated by power converters have become a crucial issue in many electric power systems [1]. In this case, diode bridge and phase controlled bridge rectifiers have been considered as one of the most important causes of electrical pollution [2]. Although these solutions have been widely implemented in industrial applications because of their economic advantages, they begin to look unsustainable due to the impositions of stricter harmonic standards.

Pulse width modulation rectifiers (PWM) have arisen as

a solution to overcome these problems, reducing harmonic pollution [3,4] and adapting in accordance to the highest requirements for energy quality [5,6]. Using these devices, it is possible to control the output voltage and to obtain sinusoidal ac currents. In order to assess the performance of a three-phase PWM rectifier, two parameters are taken into account: the Total Harmonic Distortion (THD), which is a measurement of the harmonic content of the current signal; and the Power Factor (PF), which accounts for phase differences between the current and the voltage. With this thread in mind, PWM rectifiers seek a unity PF and a small THD.

Several strategies have been proposed to control three-phase PWM rectifiers. In the reported research, multiple Proportional Integral controllers [7] have been implemented in the current loops, mainly due to the ease of implementing them as well as their satisfactory performance. However, the main limitation of this approach lies in an inherent tracking (amplitude and phase) error [8].

Over the last few years, interesting emerging control techniques such as resonant control [9,10] and repetitive control (RC) [11-13] have been developed to track/reject periodic signals. Good response characteristics are achieved by using these strategies, ensuring near unit power factor and constant output dc voltage under parameter uncertainties, as well as load disturbances. The main disadvantage is related to the lost of performance caused by variations of the network frequency from its nominal value [14].

In this paper, an odd harmonic HORC Controller is proposed for the current loops of a three-phase PWM rectifier. Hence, taking advantage of its inherent properties, only the odd harmonics are removed. By using this strategy, two aims are achieved: 1) Computational complexity is substantially reduced by the odd property of this compensator, which is very similar to that obtained with the conventional repetitive controllers, and 2) Robustness is increased when the signal frequency varies. Experimental results show a high performance at nominal frequency, even when harmonics are present in the voltage source waveforms and have the additional characteristic of preserving low THD and unitary PF, despite network frequency variations.

The paper is organized as follows: section 2 describes the three-phase PWM rectifier model, introduces the control objectives, and presents the controller structure. In Section 3, the structure of an Odd HORC Controller for the current loops is explained in detail; the control implemented for the voltage loop is described in Section 4. Section 5 reports experimental results and demonstrates a comparison to a classical HORC Controller. Finally, in Section 6 we present conclusions and future directions.

2. System description

2.1. Three-phase PWM rectifier

PWM techniques have been widely implemented to control the output of power converters as they allow shaping voltage and/or current waves based on specific applications [15].
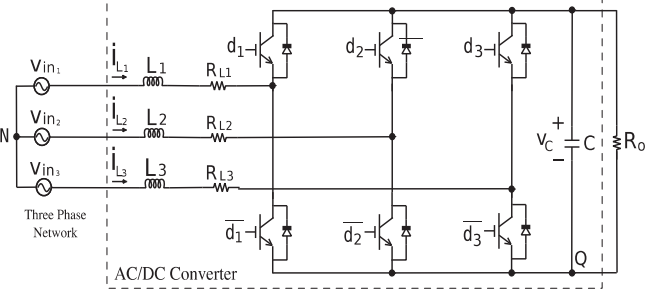

Figure 1. Three-phase pulse width-modulated (PWM) rectifier.
Source: The authors.

The three-phase PWM rectifier circuit, as shown in Fig. 1, has three-legs with IGBT transistors. It is known as a bi-directional boost rectifier (increasing the voltage) and works using fixed DC voltage polarity. Input inductors are an integral part of the rectifier and are selected based on their design [16]. We achieve harmonic compensation through the input inductors, and we ensure smooth voltage waveforms by using capacitors.

The dynamics of the three-phase PWM rectifier (as shown in Fig. 1) can be described as:

$$L_1 \frac{di_{L1}}{dt} = -R_{L1}i_{L1} - (V_c * d_1 + V_{QN}) + V_{in1}, \qquad (1)$$

$$L_2 \frac{di_{L2}}{dt} = -R_{L2}i_{L2} - (V_c * d_2 + V_{QN}) + V_{in2}, \qquad (2)$$

$$L_3 \frac{di_{L3}}{dt} = -R_{L3}i_{L3} - (V_c * d_3 + V_{QN}) + V_{in3}, \qquad (3)$$

$$C \frac{dV_c}{dt} = (i_{L1} * d_1) + (i_{L2} * d_2) + (i_{L3} * d_3) - \frac{V_c}{R_o}, \quad (4)$$

where L_n, C and R_o are the nominal values of inductances, the capacitor and the load resistance, respectively; i_{L1}, i_{L2} and i_{L3} are the phase currents and V_c is the capacitor voltage; V_{in1}, V_{in2} and V_{in3} are the known three-phase sinusoidal voltages; $V_{in1}+V_{in2}+V_{in3}=0$; R_{Ln} is the parasitic inductor resistance for each phase; $V_{QN} = -\frac{V_d}{3}(d_1 + d_2 + d_3)$; and d_n is the control action used to trigger the IGBTs. Their values range within the interval [0,1].

2.2. Control system structure

Control objectives for three-phase PWM rectifier systems are quite similar to the objectives for the single-phase case. They are focused on achieving unit power factor, constant output dc voltage and a suitable low harmonics sinusoidal waveform for the input current. The difference is to be found in the fact that the control aim for the current loop should be achieved for every phase, taking into account the shifts associated with a three-phase current flow.

Fig. 2 depicts the general control system structure. It consists of a double-loop structure: two inner current loops that ensure a sinusoidal waveform in the current input, and an outer dc voltage loop designed to regulate the output voltage and proportionate the active power balance in the system. The voltage loop gives the amplitude, $I_{dn}(t)$, of the

reference currents that is to be used in the two inner current loops. The reason behind only using two current loops is that, under the assumption of a balanced system ($V_{in1}+V_{in2+}V_{in3}=0$), the compensation action applied in two phases will generate the action to be applied for the third phase. Thus, control action d_3 will be generated form d_1 and d_2 using $d_3 = -d_1 - d_2$, as shown in Fig. 2.

A PLL (Phase Locked Loop) system takes the phase voltages and produces sine waves with appropriate phases. These signals, together with the amplitude $I_{dn}(t)$, create the two current references for the current loops.

In this way, the control system should track sinusoidal signals with suitable I_{dn} magnitudes and phases and reject the system disturbances. Among these disturbances, two are recurrent in these kinds of systems: low-frequency signals and harmonics generated by distortions in the network voltage. Due to the fact that symmetrical waveforms only contain odd harmonics, distortions in the voltage waveform are regularly found between the 3th and 9th harmonic [17].

In addition, in order to keep a constant output dc voltage, the system should react to changes in the network voltage and in the rectifier load. Finally, it is worth drawing the reader's attention to the fact that the voltage control loop uses the average of the measured dc voltage to avoid introducing its ripple into the loops.

In this work, an Odd Harmonic High Order Repetitive Controller is adopted for the current loops in order to compensate the odd harmonics that are introduced to the system by the network voltage and increase system robustness to changes in the network frequency. A PI controller is integrated into the voltage loop for the purpose of achieving an active power balance and keeping the average value of the output voltage constant.

3. Current control loops

This section describes the Odd Harmonic High Order Repetitive Controller that is proposed for the current loops. Identical current control loops are designed for two of the system phases and can be seen in Fig. 2.
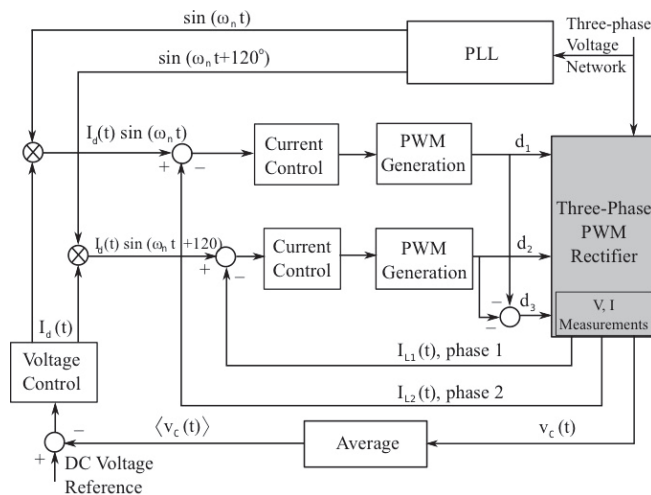

Figure 2. Control System Structure.
Source: The authors.

Primarily, the structure of conventional repetitive control scheme is explained in order to introduce the high-order controller design.

3.1. The odd harmonic high order repetitive controller

Repetitive control (RC) has proven to be a useful control strategy to track/reject periodic signals [18,19]. Using this control strategy, the sinusoidal signal references in the current loops are tracked and the harmonics generated by the network voltage are rejected. In order to accomplish this, the RC scheme incorporates a generator of periodic signals (also known as internal model) in the control structure [20]:

$$I(z) = \frac{\sigma W(z)H(z)}{1 - \sigma W(z)H(z)}, \qquad (5)$$

where $W(z)$ is a time delay function, $H(z)$ is a low-pass filter which provides robustness at high frequencies, and σ takes the values 1 or -1 and determines if the control is applied to all harmonic components; $\sigma = 1$ or $\sigma = -1$ only for odd harmonics. The way in which the internal model (eq. 5) is added to the control structure will be described in the next section.

The standard internal model, used in repetitive control [21], can be determined by using $H(z) = 1$, $\sigma = 1$, or $W(z) = z^{-N}$ with $N=T_p/T_s$, where T_p is the period of the signal being tracked/rejected and T_s is the sampling period of the control system. This model provides infinite gain at fundamental frequency and all its harmonics until the $(N/2-1)$-th. Having high gains at selected frequencies guarantees the tracking/rejecting capability in closed-loops for signals with this frequency content.

However, an internal model which only generates infinite gain at odd-harmonic components [22] can be obtained using $H(z) = 1$, $\sigma = -1$, $W(z) = z^{-N/2}$.

The magnitude frequency responses of the standard and odd internal models are shown in Fig. 3. The sampling period is selected to be $T_s=15$ kHz, which yields N=250, and the fundamental frequency is set to 60 Hz. As can be appreciated from the figure, these models generate infinite gain at fundamental and harmonic frequencies. This establishes a
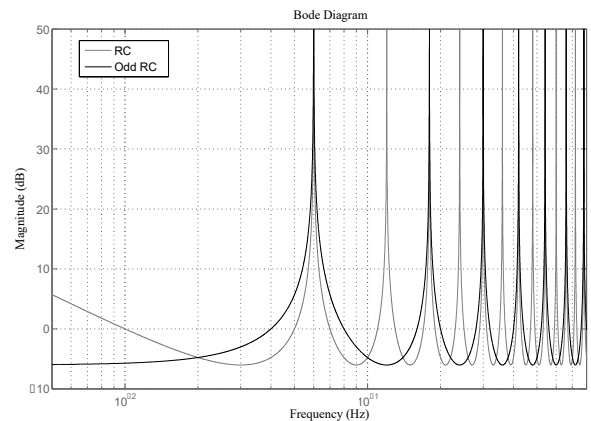

Figure 3. Frequency responses for the standard and odd internal models.
Source: The authors.

very limited frequency band that is centered around each harmonic component. This feature currently represents the main disadvantage of standard and odd internal models. As a result, the standard repetitive control exhibits a considerable loss of performance when the exogenous signal frequency varies from its nominal value, even with very small deviations [14].

In this regard, by modifying the time delay function *W(z)*, an internal model can provide high gain over a broader frequency interval around the fundamental and harmonic modes. This increases the robustness against changes in network frequency. Accordingly, $H(z) = 1, \sigma = -1$, and the time delay function is given by [5]:

$$W(z) = -1 + \left(1 + z^{-\frac{N}{2}}\right)^M, \tag{6}$$

where *M* denotes the Harmonic High Order Repetitive Controller (HORC). By using this definition, the internal model (eq. 5) is given by:

$$I_{odd}(z) = \frac{1 - \left(1 + z^{-\frac{N}{2}}\right)^M}{\left(1 + z^{-\frac{N}{2}}\right)^M} \tag{7}$$

Fig. 4 compares the magnitude response of the internal models used in odd-harmonic RC and odd-harmonic HORC for second (M=2) and third (M=3) order case; these have a nominal frequency of 60 Hz and a sampling period of 15 KHz. Fig. 4 also highlights the gain of the internal models designed for nominal frequency deviations of 59.5 and 60.5 Hz and their corresponding harmonics. It can be seen that the gain is higher for the odd-harmonic HORC (M=2 and M=3) compared with the odd-harmonic RC (M=1) for the same frequency variation. This improves the robustness against frequency changes and the performance under non-ideal operating conditions. However, internal models with high orders can decrease the robustness due to the elevated gains in the highest harmonics. Although this problem can be overcome by using a lower cut-off frequency in the low-pass filter H(z), this could cause performance decay because of the action reduction in the superior harmonics. For this reason, a tradeoff between the internal model order M and the filter bandwidth H(z) is required in order to achieve performance and stability robustness [18,19].

Based on the facts that frequency variations in the Colombian electric system are quite small (59.8-60.2) [23] and that it is desirable to keep the distortion as low as possible in the input current of the rectifier, the Odd Harmonic High Order internal model with M=2 (2ORC) has been experimentally validated as the controller with the best performance.

The odd internal model with the low-pass filter *H(z)* and *M=2* becomes:

Furthermore, it is important to note that the odd internal model (eq. 8) and the standard repetitive controller are mostly of the same order, which results in a similar computational complexity during their implementations. This implies that
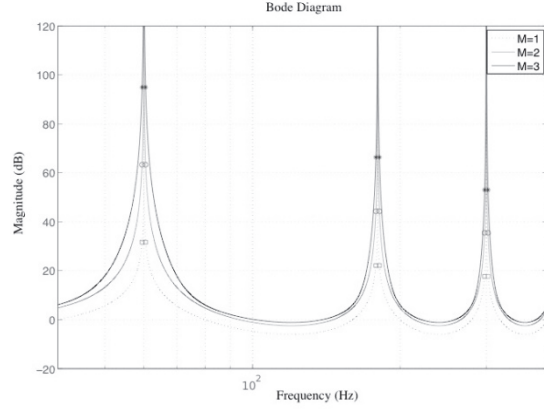

Figure 4. Odd-harmonic RC and odd-harmonic HORC internal models gain diagram
Source: The authors.

standard internal models and second order odd harmonic internal models with same *N* parameter would perform almost the same number of multiplications and additions, and also use the same amount of memory during an experimental implementation.

$$I_{2odd}(z) = \frac{-\left(2z^{-\frac{N}{2}} + z^{-N}\right)H(z)}{1 + \left(2z^{-\frac{N}{2}} + z^{-N}\right)H(z)} \tag{8}$$

3.2. Repetitive controller structure

Each current control block shown in Fig. 2 has a corresponding repetitive controller, which is as the one shown in Fig. 5. In order to include one of the internal models that were defined in the previous section, i.e. *I(z), I_odd(z), or I_2odd(z)* (equations (5), (7) and (8), respectively), repetitive control is usually implemented using the plug-in configuration presented in Fig. 5. As can be seen, the internal model (*I(z), I_odd(z) or I_2odd(z)*) is added, as part of the existing controller *G_c(z)*, and the filter *G_x(z)* is also incorporated. The compensator *G_c(z)* is used to stabilize the plant *G_p(z)* and to provide disturbance attenuation across the rectifier bandwidth. Additionally, compensator *G_c(z)* should offer good robustness margins, and filter *G_x(z)* is designed to ensure system stability in closed loop.

The transfer function of the plant is obtained from (eq. (1)-(3)), which performs the variable change $\alpha_n = d_n v_c$ and causes each phase to result in the following:
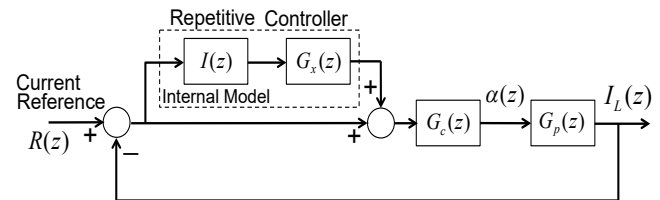

Figure 5. Repetitive control structure.
Source: The authors.

$$G_p(s) = \frac{1}{sL + R_L} = \frac{I_L(s)}{\alpha(s)} \qquad (9)$$

From the discretization of (9) the following can be obtained:

$$G_p(z) = Z \left[\frac{1}{sL + R_L} \frac{1 - e^{-T_s}}{s} \right]_{T_s} \qquad (10)$$

Control action in each phase results in:

$$\alpha(z) = (I(z)G_x(z) + 1)G_c(z)\big(R(z) - I_L(z)\big) \qquad (11)$$

with $R(z)$ being the z-transform of $r(k)$. $r_1(k) = i_d(t)\sin(\omega_n k)$ and $r_2(k) = i_d(t)\sin(\omega_n k + 120°)$, which are the reference signals for phase 1 and phase 2, respectively. Finally, dutty cycle d_n is calculated as $d_n = \alpha_n/v_c$ and sent to eah PWM generator, as seen in Fig. 2.

3.3. Stability

The closed-loop system of Fig. 5 is stable if the following conditions are fulfilled [24]:

The closed-loop system without the repetitive controller is stable, which means the transfer function $T_o(z)$ should be stable:

$$T_o(z) = \frac{G_c(z)G_p(z)}{1 + G_c(z)G_p(z)} \qquad (12)$$

1. $\|W(z)H(z)(1 - T_o(z)G_x(z))\|_\infty < 1$, where H(z) and G$_x$(z) should be chosen adequately.

Whole system dynamics, shown in Fig. 2, are divided into two parts: fast dynamics given by the current loop, and slow dynamics represented by the voltage loop. Therefore, to ensure the convergence of the whole system, two considerations are assumed: 1) the voltage loop provides very slow changes in the current reference, and 2) the current loop responds so fast that its dynamic behavior does not affect the evolution of the voltage loop. In order to obtain this behavior, the bandwidth of each loop should be properly selected in order to achieve a sufficient separation to differentiate between both dynamics. See reference [25] for a more detailed analysis on this topic.

3.4. Design of filter H(z)

Filter H(z) is used to limit the repetitive controller bandwidth, and, as such, it impacts performance, limiting the number of harmonics that will be taken into consideration. In general, the choice of filter bandwidth implies a trade-off between stability robustness and performance. Although numerous optimization techniques to define a conventional filter H(z) have been proposed, H(z) is chosen to be a null phase low-pass FIR filter [26].

3.5. Design of filter G$_x$(z)

In the event of a minimum phase systems, $G_x(z)$ is usually selected as $G_x(z) = k_r(T_o(z))^{-1}$, while for non minimum phase systems, it is possible to use the approach proposed in
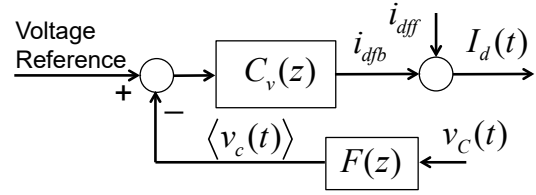

Figure 6. Voltage loop structure.
Source: The authors.

[21]. Finally, the value of the gain k_r requires a trade-off between stability robustness and steady state performance [27].

4. Voltage control loop

Voltage loop control is designed to achieve an active power balance in the rectifier and to provide the magnitude of the current reference for the current loops. Given that voltage at the rectifier output terminal has a waveform that is highly rippled, a low pass filter is usually applied to obtain a smoother signal. The purpose of this is to avoid the ripple propagation to the current reference $i_d(t)$, which would negatively impact the harmonic distortion of the rectifier input current $i_L(t)$. In this work, the low pass filter has been replaced by an averaging filter that has been tuned at 60 Hz:

$$F(z) = \frac{1}{N} \frac{(1 - z^{-N})}{(1 - z^{-1})}. \qquad (13)$$

By using this filter, the average voltage is calculated from the output voltage $V_{dc} = \langle v_c \rangle$.

Voltage loop structure is shown in Fig. 6. This structure is comprised of two basic components: a feedback control action, i_{dfb}, generated by a PI compensator, and a pre-feeding action i_{dff}. The PI controller in the feedback loop will regulate the average value of the output voltage to the desired value with zero error:

$$C_v(z) = k_i \frac{T_s}{2} \frac{(z + 1)}{(z - 1)} + k_p \qquad (14)$$

Moreover, the pre-feeding signal, i_{dff}, is designed in order to avoid sudden changes in voltage levels causing transients with high current peaks. This pre-feeding stage is calculated based on the rectifier power balance in steady state. As such, the balance between the AC active power and the DC power is given by:

$$\frac{1}{2}V_m I_m = V_{dc}I_{dc} + P_{losses} \qquad (15)$$

where $V_m = V_{in}\sqrt{2}$ is the peak value of the network voltage, $I_m = I_d$ is the peak value of the rectifier input current, $V_{dc} = \langle v_c \rangle$ is the average value of the capacitor voltage, $I_{dc} = \langle i_L \rangle$ is the average value of the load current, and P_{losses} are the rectifier losses. On that basis, the pre-feeding value can be computed by:

$$i_{dff} = \frac{1}{2}\frac{V_m I_m}{V_{dc}} + I_{losses} \qquad (16)$$

where I_{losses} is a factor that weighs the rectifier losses. As a result, the reference signal amplitude for the current loop is calculated by:

$$I_d = i_{dfb} + i_{dff} \qquad (17)$$

5. Experimental results

In this section the experimental results are presented and analyzed. Two different setups are defined for nominal and varying frequency conditions. A comparison of HORC and RC is provided in order to show the advantages of implementing the odd harmonic HORC.

5.1. Experimental setup

The utility network frequency is 60 Hz, thus defining a period of Tp=1/60 s. The sampling period is set to Ts=1/15000 s, which corresponds with the PMW switching frequency. As a result, the discrete period is N=Tp/Ts=250.

The transfer function of the plant is obtained from (eq. 10) with $L=300$ mH and $R_L=0.1$ ohms. The internal controller is $G_c(z)=(6,293z-6,283)/(z-0.998)$, which provides enough robustness margins. Filter $H(z)$, which has a good robustness-performance tradeoff, is comprised of $H(z) = -0,003871z^5 + 0,03209z^3 + 0,1167z^2 + 0,2207z + 0,2687 + 0,2207z^{-1} + 0,1167z^{-2} + 0,03209z^{-3} - 0,003871z^{-5}$. Concurrently $G_x(z) = k_r(T_o(z))^{-1}$ with $k_r=0.7$. A PI controller for the voltage loop defined in (9) takes the values $k_p=0,01$ and $k_i=0,7$.

For comparison purposes, a conventional RC with internal model, as in (5), has been designed with $H(z) = 0,175z + 0,65 + 0,175z^{-1}$, $\sigma = -1$, $W(z) = z^{-N/2}$, $N=250$, $G_c(z) = (6,293z - 6,283)/(z - 0.998)$, and $G_x(z) = k_r(T_o(z))^{-1}$ with $k_r=0,3$.

Results at nominal frequency are obtained with the rectifier connected to the grid, and results at different frequencies are acquired using an AC varying frequency voltage source from PowerSun. In both cases, a three phase autotransformer is used to provide $V_{in}=20$ Vrms to the rectifier. The three-phase rectifier is a power converter from Semikron, and control algorithms were implemented in an Intel PC with Matlab XPCTarget real time software. Bus dc voltage is $V_c=80$ V with a resistive load of 25 ohms.

5.2. Nominal frequency performance

Fig. 7 shows the response of the non-controlled rectifier. It can be seen that non-sinusoidal currents with a THD=34.4% are obtained. It is important to note that Fig. 7 also shows the distortion in the voltage network with 5th and 7th harmonics with a THD of 4.3 %. This distortion acts as a disturbance in the current loops.

Fig. 8 presents the results with the proposed odd harmonic HORC. It can be seen that currents now have a sinusoidal shape in the phase with the voltage source. The THD obtained is 2.2 %. Power factor is presented in Fig. 8 in which it can be seen that PF=1 was obtained.

These results show that odd harmonic HORC satisfies the control objectives, achieving a low THD and unitary power factor, even in the case of distortion in the voltage source. Based on its definition, conventional RC should also achieve the same performance. However, since HORC provides smaller robustness margins, the cut-off frequency of filter $H(z)$ is usually smaller than the one selected for RC. This entails a slight performance reduction that appears as a small THD degradation. Fig. 9 shows the THD obtained with RC under the same conditions.
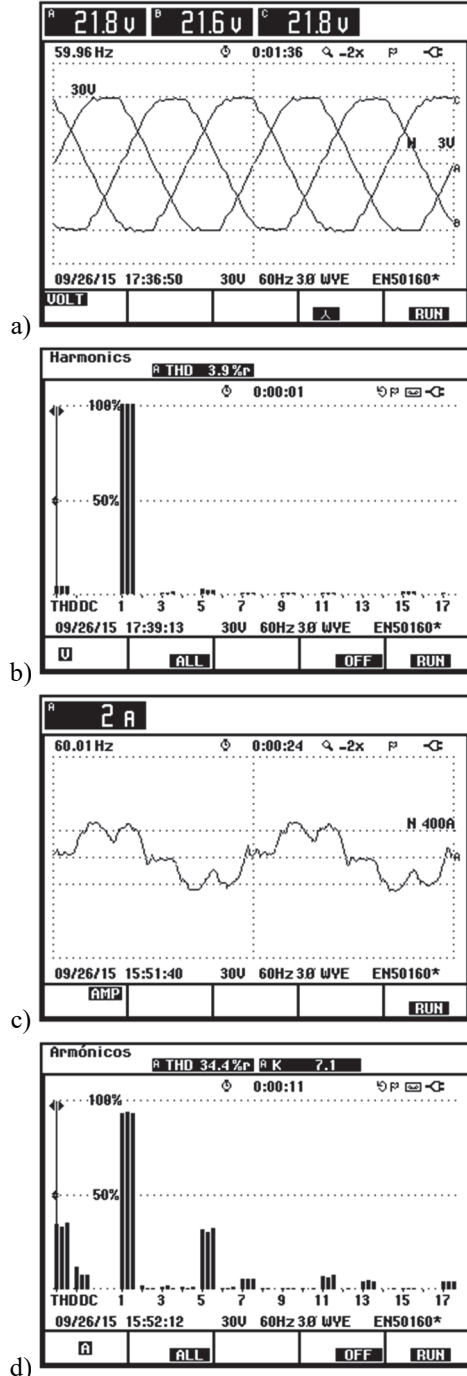

a)

b)

c)

d)

Figure 7. Non-controlled rectifier response. a) Voltage signals. b) Voltage harmonic content. c) Current signals. d) Current harmonic content.
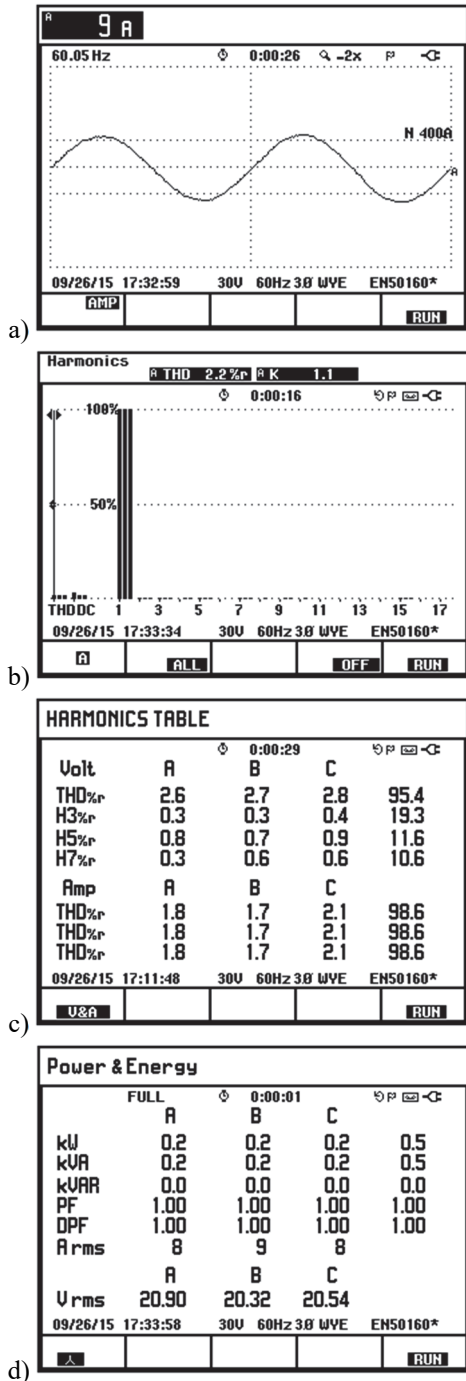Source: The authors.

a)

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Figure 8. Controlled rectifier response (odd harmonic HORC). a) Current signal. b) Current harmonic content. c) Harmonic table. d) Power and energy table.
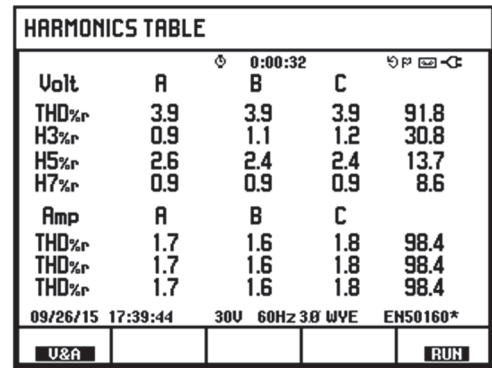Source: The authors

Figure 9. Harmonic content table for conventional RC.
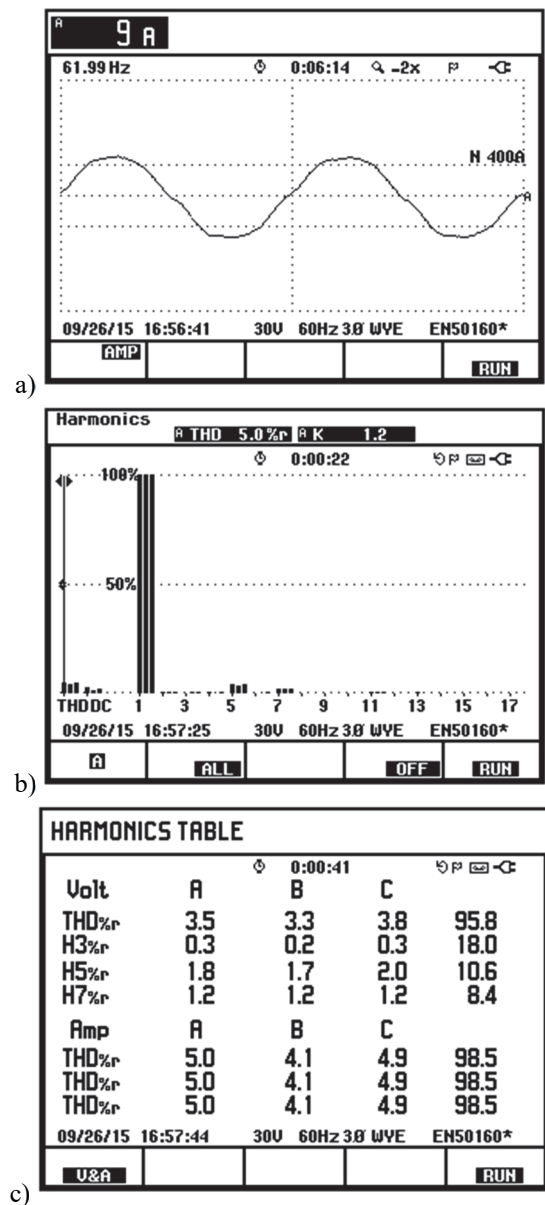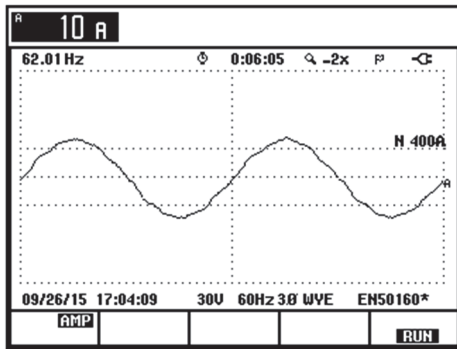Source: The authors

a)

b)

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Figure 10. RC response at 62 Hz. a) Current signals. b) Current harmonic content. c) Harmonic table. d) Power and energy table.
Source: The authors

5.3. Varying frequency performance

These experiments use an AC voltage source that comes from PowerSun and has a configurable frequency. Fig. 10 depicts the current waveforms when the source frequency is 62 Hz and uses conventional RC. The distortion of the obtained currents can be seen with a THD=5 % with 5th and 7th harmonics. Also, the degradation of the power factor is now present with PF=0.98.

d)

Figure 10. RC response at 62 Hz. a) Current signals. b) Current harmonic content. c) Harmonic table. d) Power and energy table.
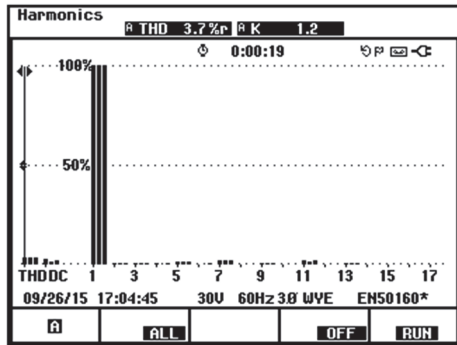Source: The authors

d)

Figure 11. Response of odd harmonic HORC at 62 Hz. a) Current signals b) current harmonic content c) harmonic table d) power and energy table
Source: The authors

Using odd harmonic HORC yields, a significantly better performance can be seen in Fig. 11. The obtained THD and PF are 3.8 % and 1, respectively.
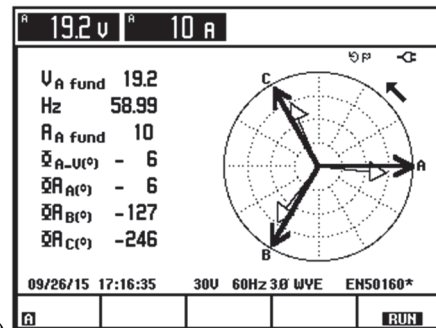

a)

b)

c)

a)

b)

Figure 12. Response of RC at 59 Hz. a) Harmonic table d) Phasor diagram.
Source: The authors

Similar behavior is expected at lower frequencies. Fig. 12 and Fig. 13 present the THD and phasor diagram results for 59 Hz for RC and HORC, respectively. It can be seen that HORC performs better with a lower THD and a smaller current phase deviation.

6. Conclusion

This work has proposed an odd harmonic HORC has for the current control loops in a three phase-PMW power rectifier. Experimental validation has shown that the proposed controller achieves high performance with THD=1.7% and a unitary PF. Compared to conventional RC, the HORC has the advantage of providing higher robustness against network frequency variations. This characteristic allows the rectifier to accomplish the more demanding standards of power quality, even under varying frequency conditions.
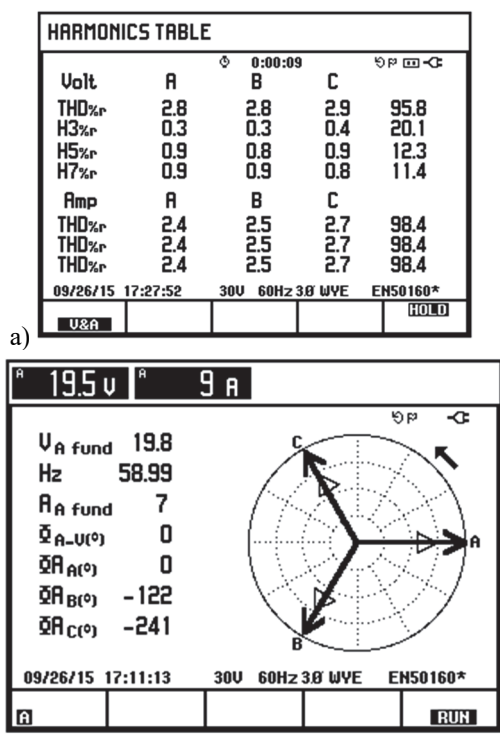
Figure 13. Response of the odd harmonic HORC at 59 Hz. a) Harmonic table. d) Phasor diagram.
Source: The authors

Despite being a high order controller, it was found that odd harmonic HORC has a similar computational burden when it was compared to a full- harmonic RC.

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