FULLY INTEGRATED CMOS PHASE SHIFTER/VCO

FOR MIMO/ISM APPLICATION

A Thesis

by

AHMAD REZA TAVAKOLI HOSSEINABADI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2007

Major Subject: Electrical Engineering

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ABSTRACT

Fully Integrated CMOS Phase Shifter/VCO

for MIMO/ISM Application. (December 2007)

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Chair of Advisory Committee: Dr. Kamran Entesari

A fully integrated CMOS $0 - 90^0$ phase shifter in 0.18um TSMC technology is presented. With the increasing use of wireless systems in GHz range, there is high demand for integrated phase shifters in phased arrays and MIMO on chip systems. Integrated phase shifters have quite a high number of integrated inductors which consume a lot of area and introduce a huge amount of loss which make them impractical for on chip applications. Also tuning the phase shift is another concern which seems difficult with use of passive elements for integrated applications. This work is presents a new method for implementing phase shifters using only active CMOS elements which dramatically reduce the occupied area and make the tuning feasible.

Also a fully integrated millimeter-wave VCO is implemented using the same technology. This VCO can be part of a 24 GHz frequency synthesizer for 24 GHz ISM band transceivers. The 24 GHz ISM band is the unlicensed band and available for commercial communication and automotive radar use, which is becoming attractive for high bandwidth data rate.

To my dear parenets, Bagher and Zahra, and my sisters, Maryam and Fatemeh

ACKNOWLEDGEMENTS

I find myself in great debt to my parents and my sisters, for their love and support. For that I will always be grateful.

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1. INTRODUCTION TO PHASE SHIFTERS

1.1 -Multiple Input Multiple Output (MIMO) Systems

MIMO communication systems are becoming more attractive for high frequency and data-rate wireless systems [1]. MIMO systems take advantage of phased arrays in their structure in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions [2]. This beam-forming provides several advantages over conventional single-input single-output (SISO) wireless systems in terms of reliability, overall SNR and overall dynamic range [3], [4]. A more in-depth mathematical study on MIMO wireless systems has been done in [5].

Portability of the wireless system (e.g. hand-held devices) is another important concern that is becoming more and more important these days. Therefore the wireless systems should take less area while working with tiny power consumption and still work perfectly. These demands are pushing the industry to provide the whole wireless systems on a single chip which means the front-end needs to be compatible with ordinary digital CMOS technology while consuming as less chip area as possible.

In general, several different architectures have been used to implement on-chip phased arrays. Fig.1 shows the traditional architecture for phase arrays. In the traditional architecture, the signals are superposed before the mixer. This will cancel out the interferers from other directions, which relaxes the linearity of the mixer and phase noise

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This thesis follows the style of *IEEE Journal Solid State Circuits.*

of the VCO. As a result the traditional architecture is more robust comparing to the other

methods which provide the phase shift and summation in the IF path.
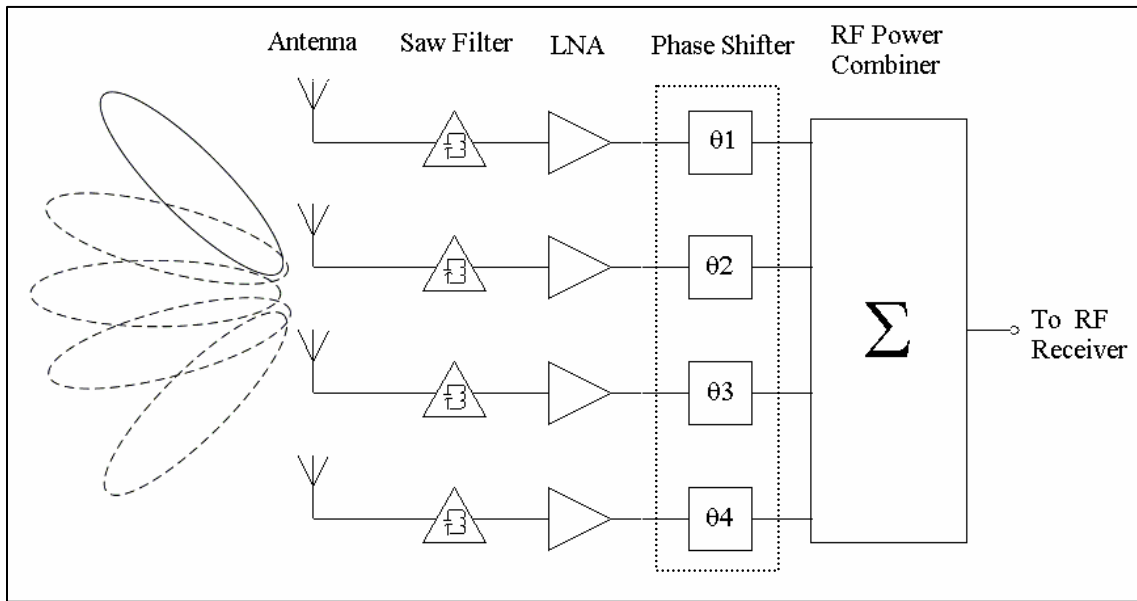
Figure 1: Traditional architecture for implementing phase array

Tunable phase shift elements (phase shifters) are one of the key elements in these

types of phase-arrays. The main role of phase-shifters is to provide the beam-forming

properties of the phased array.

1.2 –Different types of phase-shifters

There are two main categories of phase shifters: (1) True time delay (TTD) phase

shifters and (2) Reflection type phase shifters (RTPS).

1.2.1 –True time delay phase shifter

This type of phase shifter takes advantage of the delay in the signal when it passes through a passive network (e.g. phase shift of a signal when passes through a transmission line). This phase shift is constant for a fixed structure at a certain frequency. Thus the desired phase shift can be achieved by changing the structure such that the phase shift at the signal changes at desired frequency accordingly.

Eq.1 shows the approximate phase shift of a transmission line (T.L.) as a function of T.L. parameters. According to this equation, there are two ways to change the phase: changing the electrical parameters of the T.L. (e.g. C, L) or changing the effective length of the T.L.s (e.g. l)

Equation 1

$$\Delta\theta = \beta \times l = \approx \omega\sqrt{L \times C} \times l$$

In order to change electrical parameters of the T.L., one can periodically load the T.L. with tunable capacitors (Fig.2). The tunable capacitors can be implemented either with MEMS-switched capacitors (Fig.3) [6], or semiconductor based variable capacitors [7] (e.g. MOS-Cap).
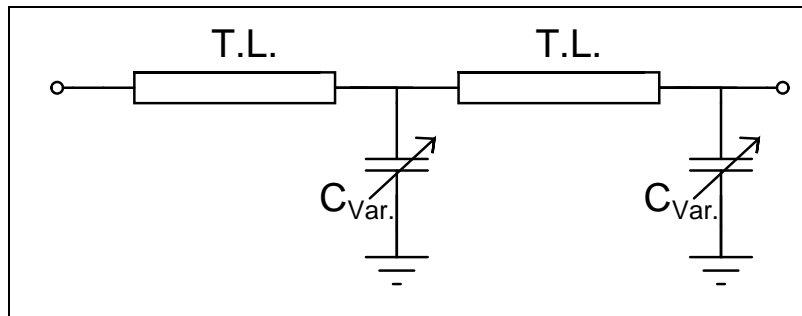
Figure 2: Periodically capacitive loaded T.L.
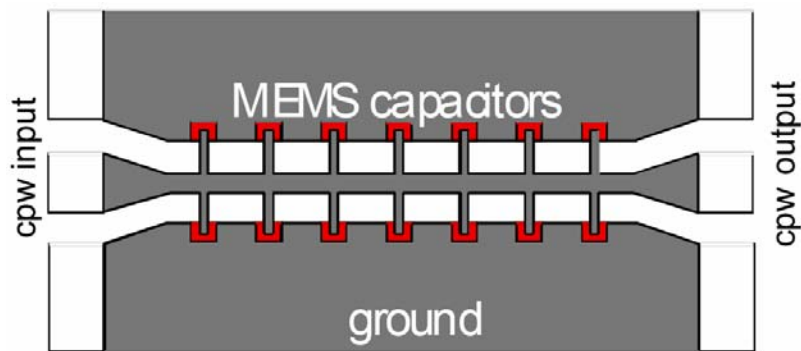
Figure 3: Example of capacitive loaded T.L. with MEMS cap

Besides changing the electrical parameters of the T.L, one can switch the signal path through different T.L.s (Fig.4). The switches can be implemented with a MEMS switch [8], or a semiconductor switch such as a GaAs switch [9] or a PIN diode switch [10].
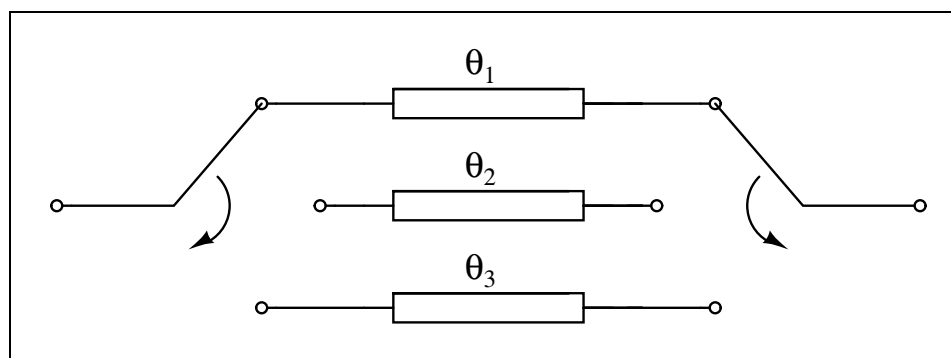
Figure 4: Phase shift by changing the signal path

1.2.2 –Reflection type phase shifter

This type of phase shifter uses a coupler (Fig.5) in its structure. When port 3 and port 4 are both terminated with an equal reactive load, the signal entering port 1 will be reflected to port 2 with the same amplitude but a different phase [11](Fig.6). The resulted phase shift at the output signal can be controlled and tuned by varying the reactive load (more analytical calculation is provided in Section 2). RTPS usually provides the highest phase tunability among the other types (can reach 360° [12])
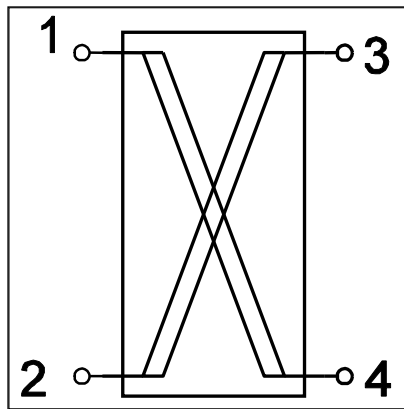
Figure 5: Symbolic view of a coupler
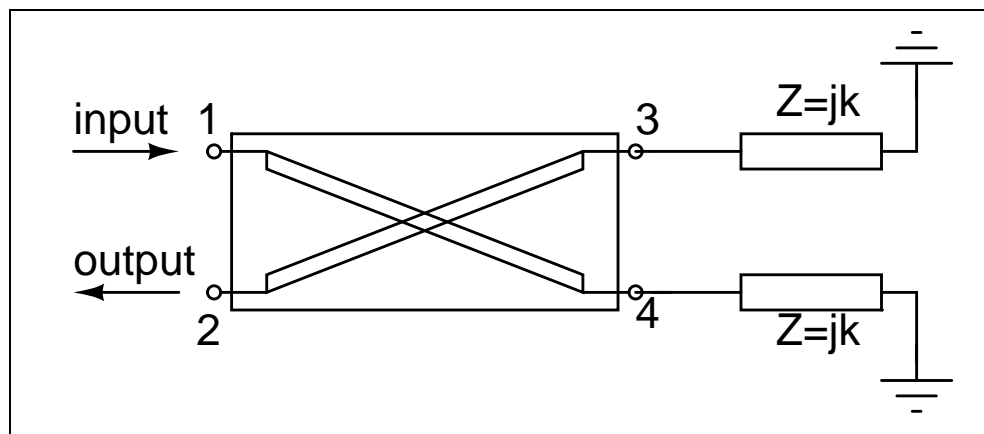
Figure 6: Implementation of reflection type phase shifter with coupler

1.3 –Implementation of phase shifters

Depending on the application and the frequency of operation, one can implement phase shifters with passive or active components.

1.3.1 –Passive implementation

The most common way of implementing phase shifters in microwave and millimeter-wave frequencies is to use passive elements to implement phase shifters. For higher frequency applications (f > 30 GHz) usually transmission lines are used in order to implement phase shifters for on-chip applications. Both TTD and RTPS can be implemented with distributed elements (Fig.7) [7], [13]. Since distributed elements are bulky in lower frequencies (f < 30 GHz) and occupy a huge amount of space especially for integrated circuit applications, the lumped model of the structures are used for lower frequencies (Fig.7 and Fig.8) [15], [16]. These structures usually employ variable capacitors in their construction which can be based on MOS, SiGe, GaAs, etc, and their inductive section is usually fixed.
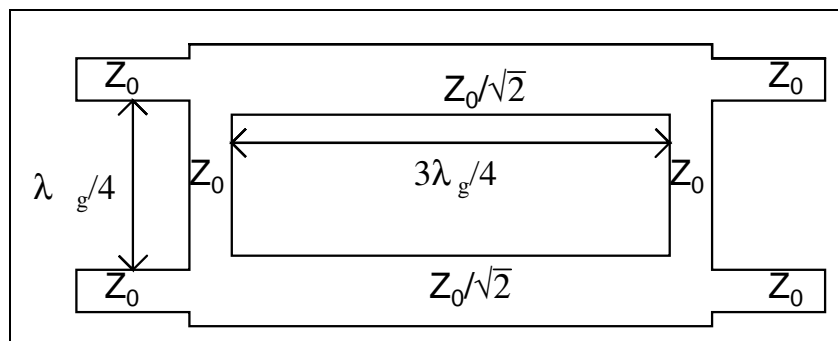
Figure 7: Distributed implementation of a coupler with micro-striplines

The main advantage of passive implementation is:

o No power consumption

o High linearity

o Perfect stability

o High power handling

But they have the following disadvantages:

o High insertion loss

o Large size for frequencies below 10GHz.
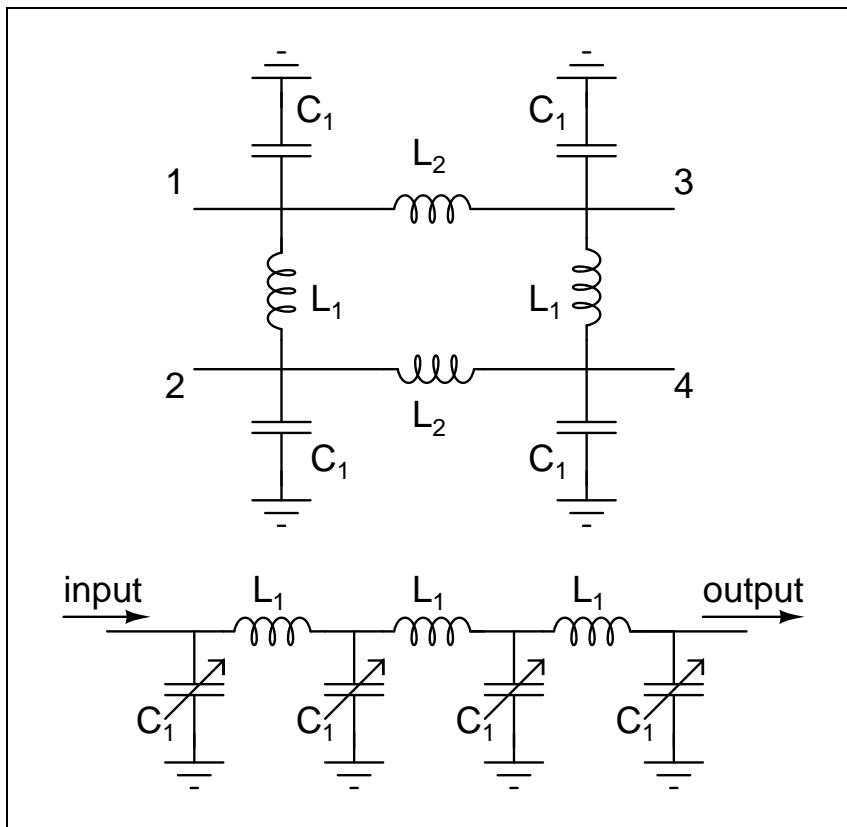
Figure 8: Lumped implementation of a coupler with inductors and capacitors (top), lumped implementation of true time delay phase shifter (bottom).

1.3.2- Active implementation

Passive implementation of phase shifters is promising for high frequencies. But current wireless systems are working at frequencies below 10 GHz. Distributed elements and inductors at these frequencies are too bulky and also too lossy to be used for on-chip phase shifters.

The idea of active phase shifter is to replace the bulky passive components in the original passive design with active circuits which emulate those passive devices (e.g. active inductors [17], [18]). Using this method, Prof. Allstot in [19] has implemented a TTD phase shifter by replacing inductors with active inductors. Our focus it to design an active phase shifter circuit based on RTPS structure.

Speaking of an active phase shifters the main advantages are:

- o Low insertion loss (in some cases a gain can be expected)

- o Compact size (specially for conventional RF frequencies), easy to integrate

But they suffer from:

- o Poor dynamic range comparing to passive devices

- o Stability problems

- o Non-zero Power consumption

1.4 – Thesis overview

In this thesis a fully integrated CMOS, reflective type phase shifter is implemented. The design is performed by employing 0.18um TSMC technology. The center frequency to be considered is 4 GHz which is close to typical working frequencies of current wireless systems. The same design procedure with more advanced CMOS technology such as 0.13 μm, 90 nm and 65 nm can be used to implement the phase shifter for higher frequencies.

Following by this Section, Section 2 studies the theory of the reflective type phase shifters and the properties of the distributed/lumped implementations, Section 3 investigates the design and the characteristic of active inductors, Section 4 provides the final design along with the simulation result of the whole active phase shifter and finally the conclusion is provided.

2. REFLECTION TYPE PHASE SHIFTER

2.1 – 3 dB hybrid coupler

The core of a reflection type phase shifters is a 3 dB hybrid coupler (in this thesis the word coupler refers to 3 dB hybrid coupler). A coupler is a four-port network (Fig.9). When all four ports of a coupler are matched to the reference impedance   (50 Ω), the signal inserted in port 1 will be transferred to port 3 and port 4 while port 2 is isolated from port.1. The signals at the output ports (port 3 and port 4) will have the same amplitude (half the power of input signal) but with 90^0 phase difference. Eq.2 shows the equivalent S-parameter matrix associated with this coupler.
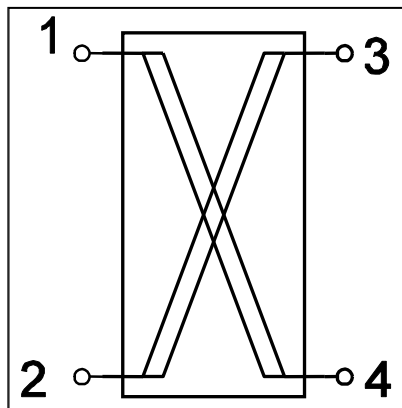
Figure 9: Symbolic view of a coupler

Equation 2: S-parameter of the coupler

$$S = -1\big/\sqrt{2} \begin{bmatrix} 0 & 0 & j & 1 \\ 0 & 0 & 1 & j \\ j & 1 & 0 & 0 \\ 1 & j & 0 & 0 \end{bmatrix}$$

2.2 – Phase shifter with 3dB coupler

If port 3 and port 4 are terminated with a pure reactive element (Fig.10), port 3 and port 4 are no longer matched. The signal in port 1 of the coupler propagates through port 3 and port 4. Since port 3 and port 4 are terminated with pure reactive elements, both signals will be completely reflected back from those ports.

These reflected signals will go back to port 1 and port 2. If both termination impedances have the same value, the reflected signals in port 1 will cancel out but the signal at port 2 will have the same amplitude as the input signal but with different phase. This phase difference between the input and output signal is provided in Eq.3.
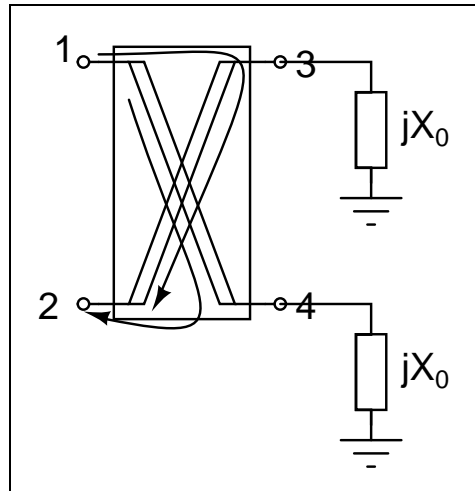
Figure 10: Phase shifter with a coupler

Equation 3

$$\theta = -2\tan^{-1}\left(\frac{X_0}{Z_0}\right)$$

As Eq.3 shows, by varying the value of X, the amount of the phase difference can be changed (analog phase shifter). This phase shift can be formulated in terms of new X impedance (X_1) (Eq.4) [20].

Equation 4

$$\Delta\theta = 2\left[\tan^{-1}\left(\frac{X_0}{Z_0}\right) - \tan^{-1}\left(\frac{X_1}{Z_0}\right)\right]$$

As a conclusion, for implementing this type of phase shifter a coupler terminated with variable reactive elements is required. It should be emphasized that this variable element should be pure reactive (High Q) since any real impedance is directly translated to loss in the phase shifter.

2.3 – Implementation of 3dB coupler

There are several methods available to implement a coupler, depending on the application. In this section, three typical methods of implementing couplers have been investigated. Then a systematic design of the coupler using ideal passive elements has been presented.

2.3.1 – Distributed implementation of a 3 dB coupler

3dB couplers are generally used for power dividing in microwave circuits. These couplers are usually implemented using distributed elements at high frequencies. Fig.11 shows the distributed implementation of 3 dB two-branch coupler.
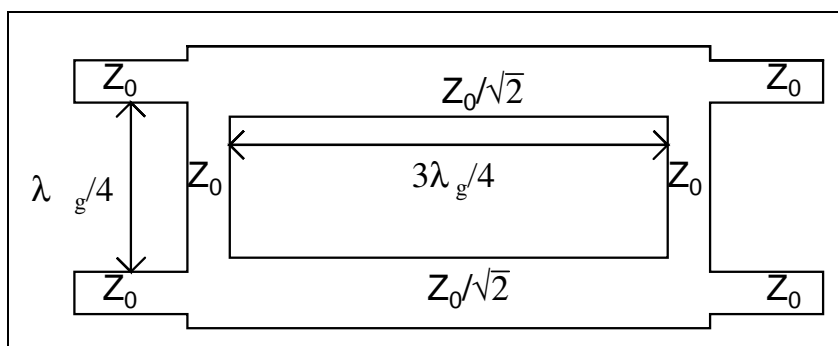
Figure 11: Distributed implementation of two-branch coupler with micro-striplines

The two-branch implementation of the coupler is a narrowband circuit (λ_g is frequency dependent) as a result it is not suitable for wide band applications.

Another distributed implementation of coupler is a three-branch coupler (Fig.12) with higher bandwidth of operation which makes it suitable for wideband applications

such as our case of study. The more in-depth analysis on multi-branch couplers and their properties can be found in [21]
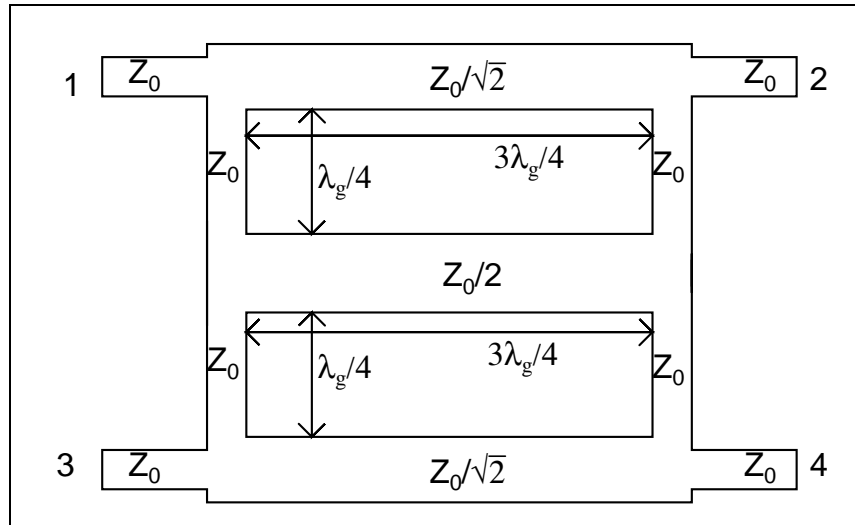
Figure 12: Distributed implementation of a three-branch coupler with micro-striplines

2.3.2 – Lumped implementation of a 3 dB coupler

The distributed implementation of a coupler has been used for many years at millimeter-wave frequencies. But for on-chip implementation in frequencies lower than 30 GHz, the size of the distributed structures becomes extremely large. E.g. $\lambda_g/4$ in 4 GHz is around 1cm when the dielectric is SiO2 (permittivity=3.8). This means the wideband phase shifter will consume an area equal to 2cm×3cm ($\lambda_g/2 \times 3\lambda_g/4$) which is extremely large for on-chip application.

The alternative solution is using lumped elements instead of distributed elements for lower frequencies. In order to find the lumped equivalent of distributed couplers the

common approach is to replace the transmission line with equivalent Π model for quarter

length transmission line (Fig.13, Eq.5 and Eq.6).
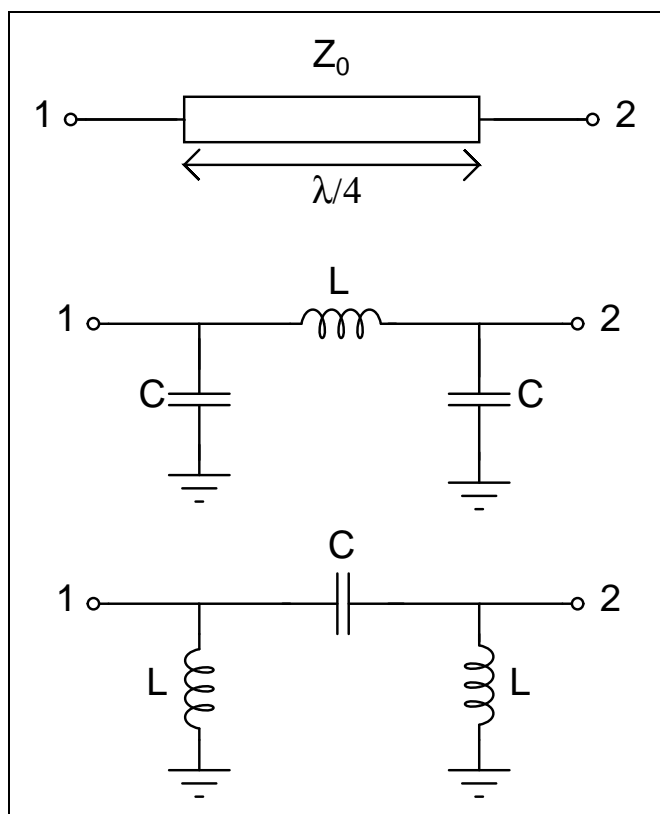
Figure 13: Equivalent Π models of a quarter length transmission line

Equation 5

$$L = \frac{Z_0}{2\pi f}$$

Equation 6

$$C = \frac{1}{2\pi f \times Z_0}$$

Based on Π model for transmission lines, Vogel [22] and Ohta [23] have proposed how to model the two branch distributed coupler with lumped elements. Depending on application and implementation constrains, one of these lumped models (Fig.14) can be selected to implement a lumped two branch coupler.
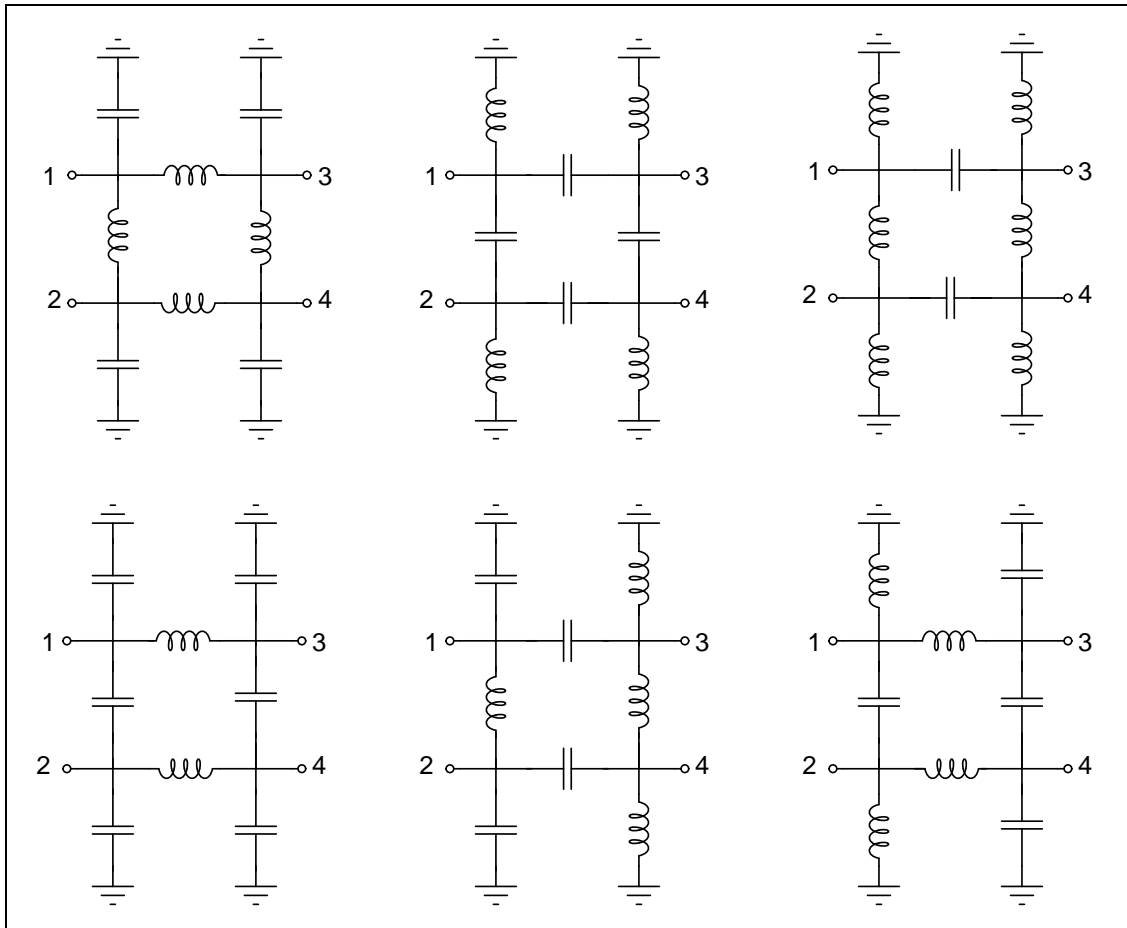
Figure 14: Different lumped equivalent models of two-branch distributed coupler

Using the same approach, [24] and [25] have proposed the lumped equivalent circuit of three-branch coupler (Fig.15).

As Eq.5 shows, the value of capacitors and inductors in a Π model are frequency dependent which means coupler designed using Π model for a certain frequency is a

narrowband circuit. On the other hand, the two-branch coupler is narrowband but itself. Thus one should use lumped model of the three-branch coupler whose bandwidth is not limited by the structure but by the lumped model of the transmission line. A more detailed analysis of the bandwidth in two-branch and three-branch couplers and their lumped model are provided in [26].
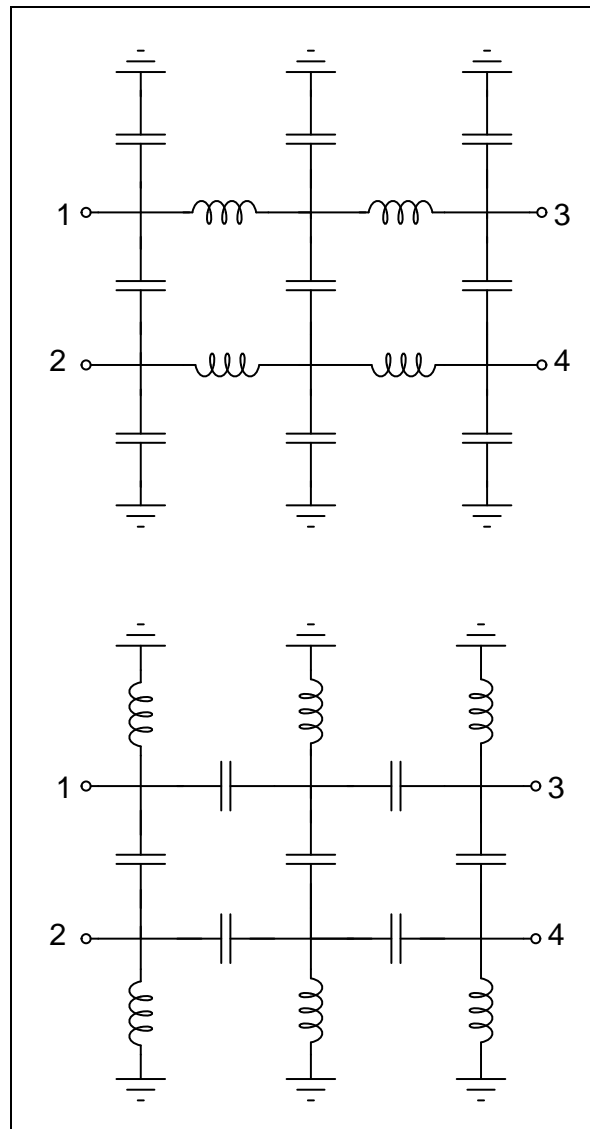
Figure 15: Lumped equivalent models of a three-branch distributed coupler

There are two available topologies for implementing lumped three-branch coupler (Fig.15), one with floating inductors, and the other one with grounded inductors. Considering the size of inductors for lumped implementation the coupler with floating inductors looks more reasonable.

2.3.3 – Active implementation of a 3 dB coupler

The lumped implementation of the coupler is promising for frequencies below 30 GHz, but at frequencies below 10 GHz the required inductors become large and impractical for circuits that have more than a few inductors. In the wideband approach, each phase shifter has at least four inductors. With an approximate area of 200 μm × 200 μm for each inductor and a separation of at least 300μm, the effective area of the inductors is about 1000μm×1000μm which is pretty large for on-chip applications.

On the other hand, active elements acting as an inductor (active inductors) are very compact and have been widely used for implementing filters [26]. Grounded active inductors are usually preferred because of stability problems for floating active inductors.

In order to overcome the problem of area consumption of passive inductors, one can replace passive inductors with active ones to implement lumped phase shifter. To do so, one of the two available architectures in Fig.15 should be selected. Although the first one has less number of inductors compared to second one, but the second one has only grounded inductors. As discussed before floating active inductors should be avoided

because of stability problems; therefore the second lumped model in Fig.15 (Fig.16) is the best choice to implement the lumped coupler with active inductors.

2.3.4 – Coupler design

The next step is to design the lumped coupler. The element values for the selected lumped architecture (Fig.16), the value of elements should be found. Based on equations in [27] and using a MATLAB program. This program takes center frequency and characteristic impedance of the system as inputs and generates the element value in Fig.16. The final values for center frequency of 4 GHz and characteristic impedance of 50 Ω are presented in Table 1.
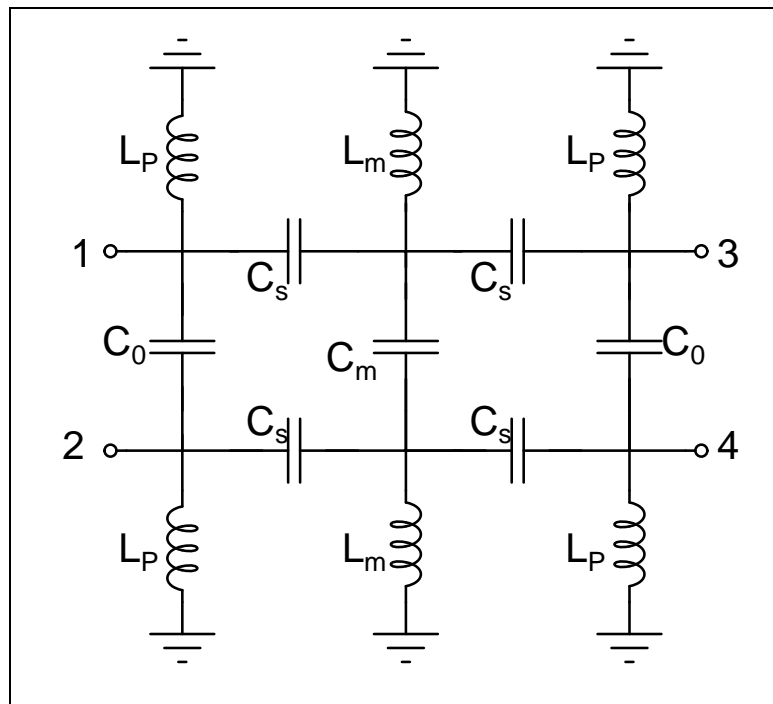
Figure 16: Lumped equivalent model of a three-branch distributed coupler

Table 1: Value of elements of Fig.16

Element	Value
L_p	1.025 nH
L_m	486 pH
C_s	1.14 pF
C_m	967 fF
C_o	398 fF

2.3.5 – Simulation result for the lumped coupler

Fig.17 shows the simulated S_{11} of the phase shifter using Cadence [28]. The magnitude of S_{11} shows an input matching of -20 dB at 4 GHz. Fig.18 shows the simulated S_{21} of the coupler. The magnitude of S_{21} shows the isolation between port 1 and port 2 is better than -20 dB at 4 GHz.
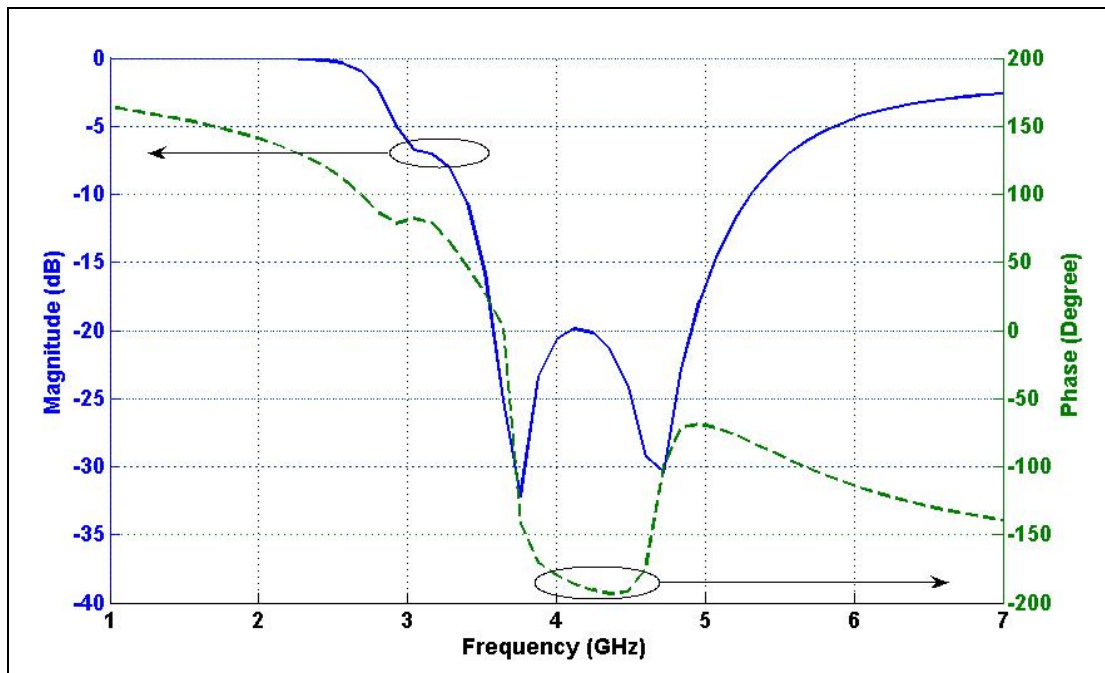
Figure 17: Simulated S_{11} of the lumped coupler
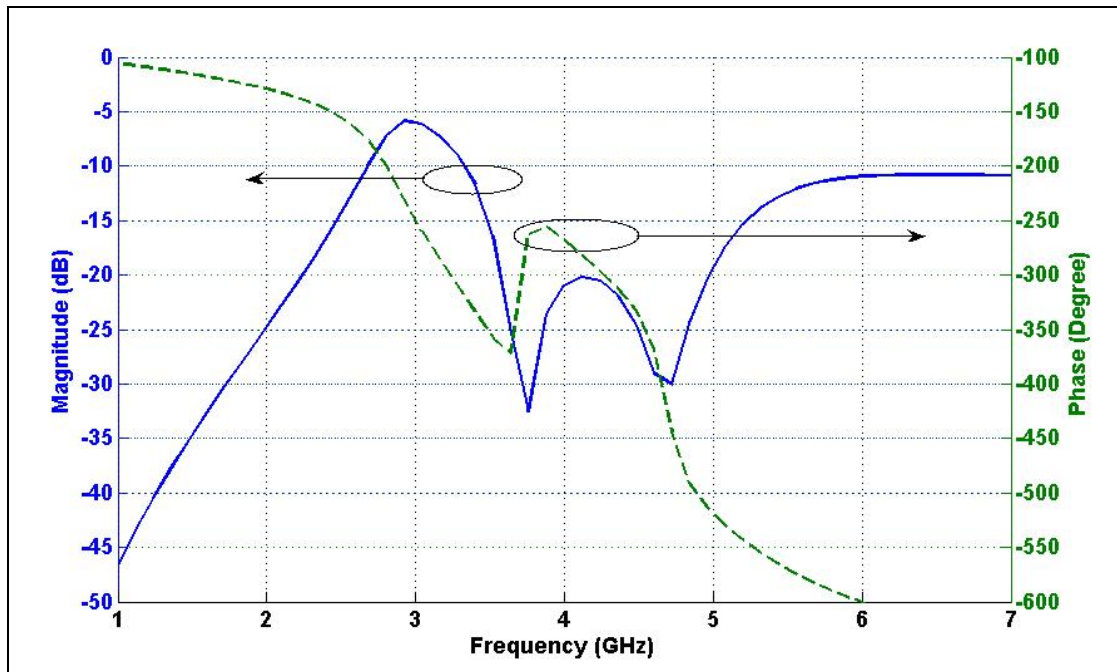
Figure 18: Simulated S$_{21}$ of the lumped coupler
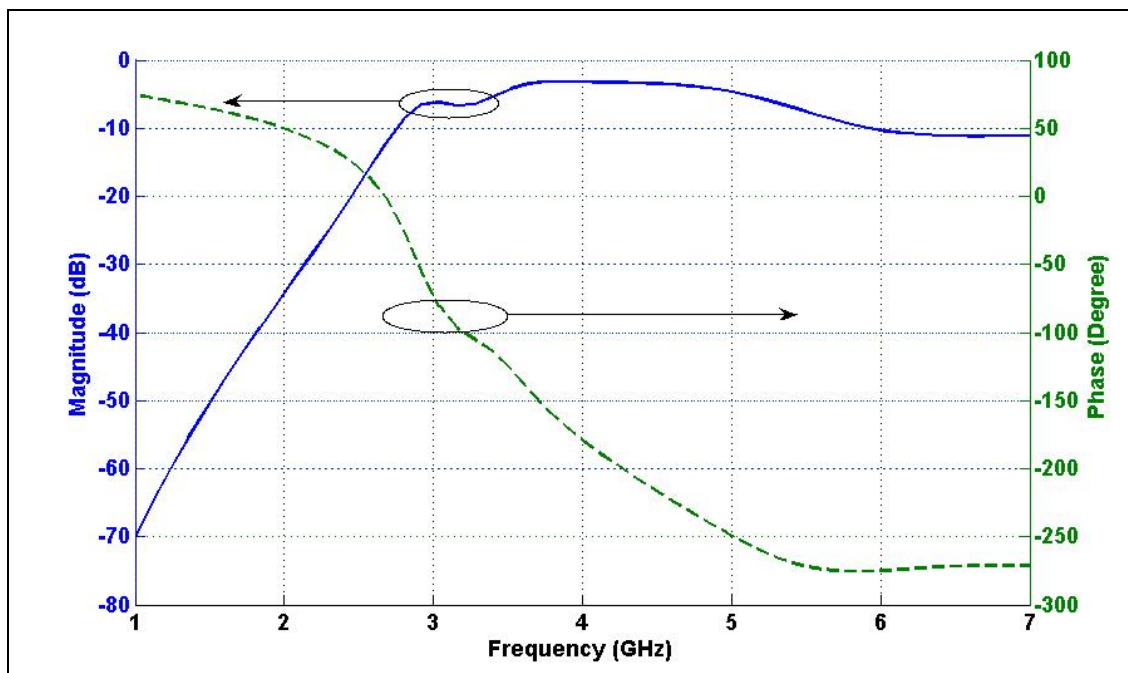
Figure 19: Simulated S$_{31}$ of the lumped coupler

Finally Fig.19 and Fig. 20 show S_{31} and S_{41} of the coupler respectively. As expected they both have amplitude around -3dB at 4GHz. The phase difference between port 4 and port 3 at 4 GHz is 270^0 (= -90^0) which perfectly matches with theory.
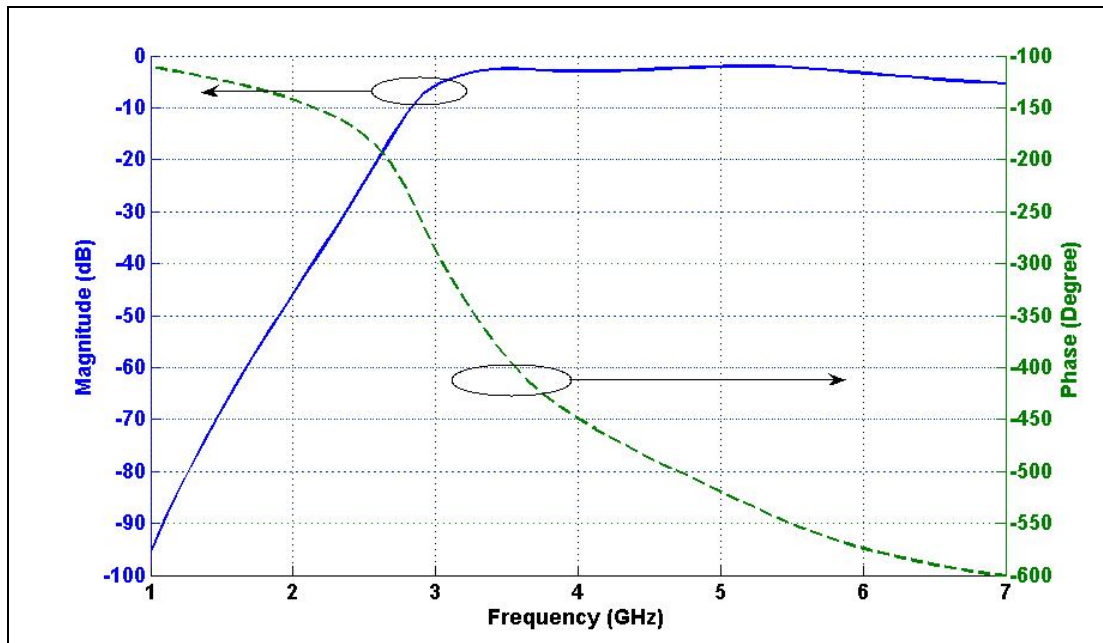
Figure 20: Simulated S_{41} of the lumped coupler

2.4 – Tunable reactive termination

According to Eq.4 the tunability of reactive element is essential in providing phase shift. This means the reactive network should be designed in such a way that it provides the highest possible phase tuning in Eq.4.

2.4.1 -90^0 phase shifter

For the phase shifter in Fig.10 if the termination is assumed infinite, the amount of phase difference would be -90^0. Taking this phase difference as a reference, the

required tuning in the reactive element for achieving a phase shift of 90^0 can be calculated using Eq.4 (see Eq.7).

Equation 7

$$90^0 = 2\left[\tan^{-1}\left(\frac{\infty}{Z_0}\right) - \tan^{-1}\left(\frac{X_1}{Z_0}\right)\right] \Rightarrow$$

$$45^0 = 90^0 - \tan^{-1}\left(\frac{X_1}{Z_0}\right) \Rightarrow$$

$$\tan^{-1}\left(\frac{X_1}{Z_0}\right) = 45^0 \Rightarrow$$

$$X_1 = Z_0$$

Equation means the final value of X for having a 90^0 phase shift should be equal to characteristic impedance of the system. By using an inductor as the variable impedance ($jL\omega = jX_1 = jZ_0$) the value of the required inductance and the required tuning range is shown in Eq.8.

Equation 8

$$\boxed{L_t = \left.\frac{Z_0}{\omega}\right|_{f=4GHz, Z_0=50\Omega} \approx 2nH \Rightarrow L_t\Big|_{2nH}^{\infty(open-circuit)}}$$

The termination inductors are in parallel with the L_P of the coupler, so one can implement the equivalent inductor as parallel combination of L_t and L_p (L_X). Considering the wide tuning range of L_t is not practical, the equivalent inductor, L_X, would be more practical (Eq.9). This variable inductor should be implemented using the

same active inductor used to implement the coupler. The active inductor should have a control mechanism for tuning the inductor to provide the required phase shift.

Equation 9

$$L_t \| L_P = L_X \Rightarrow L_X \Big|_{677\,pH}^{1.025\,nH}$$

2.4.2 – 180^0 and 360^0 phase shifter

With the same approach as in 2.4.1, other termination networks can be designed to implement 180^0 and 360^0 phase shifters.

For providing 180^0 phase shifter, one option is to use circuit in Fig.21. The series combination of the capacitor along with a tuning inductor is given in Eq.10 for the minimum and maximum value of tuning in the inductance. This shows when the inductor is minimum, the load is capacitive ($X_0 < 0$), but when the inductor is tuned to the maximum, the load is inductive ($X_1 > 0$).

Equation 10

$$jX_0 = jL_{min}\omega + \frac{1}{jC\omega} = \frac{1 + jL_{min}C\omega^2}{jC\omega}$$

$$jX_1 = jL_{max}\omega + \frac{1}{jC\omega} = \frac{1 + jL_{max}C\omega^2}{jC\omega}$$
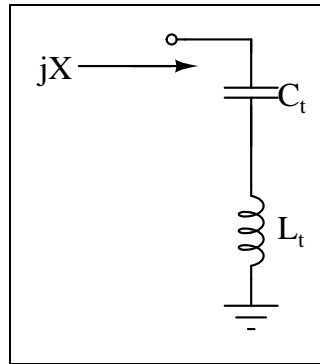
Figure 21: Proposed termination circuit for 180^0 phase shifter

To provide the required 180^0 phase shift, X_0 and X_1 should satisfy Eq.11. The minimum and maximum in the tuning range of inductors for two value of C (typical values in the on-chip application), in order to provide 180^0 phase shift, has been calculated using Eq.11 and the result is provided in table.2.

Equation 11

$$Eq.4 \Rightarrow 180^0 = 2 \times \left[\tan^{-1}\left(\frac{X_0}{Z_0}\right) - \tan^{-1}\left(\frac{X_1}{Z_0}\right) \right]$$

Table 2: Min and max tuning range of L for different C values for implementing a 180^0 phase shifter

Capacitance	Inductance	
	Min	Max
2pF	108pH	1.008nH
2.5pF	372pH	1.272nH

The termination impedance for 360^0 phase shifter should be able to satisfy Eq.12. Fig.22 shows the X/Z_0 as a function of $\tan^{-1}(X/Z_0)$. According to this figure, in order to satisfy Eq.12, the impedance of termination circuit (jX) should change such that it starts

from zero (short circuit) then becomes infinite (open circuit) and finally goes back to zero (short circuit) while tuning the inductor in the tuning range. This means that the termination circuit should provide have zero for both values of L_{min} and L_{max} while it should have a pole for an $L_{min} < L < L_{max}$.

Equation 12

$$X_0 = X \big| L_{min}$$

$$X_1 = X \big| L_{max}$$

$$Eq.4 \Rightarrow 360^0 = 2 \times \left[\tan^{-1}\left(\frac{X_0}{Z_0}\right) - \tan^{-1}\left(\frac{X_1}{Z_0}\right) \right]$$
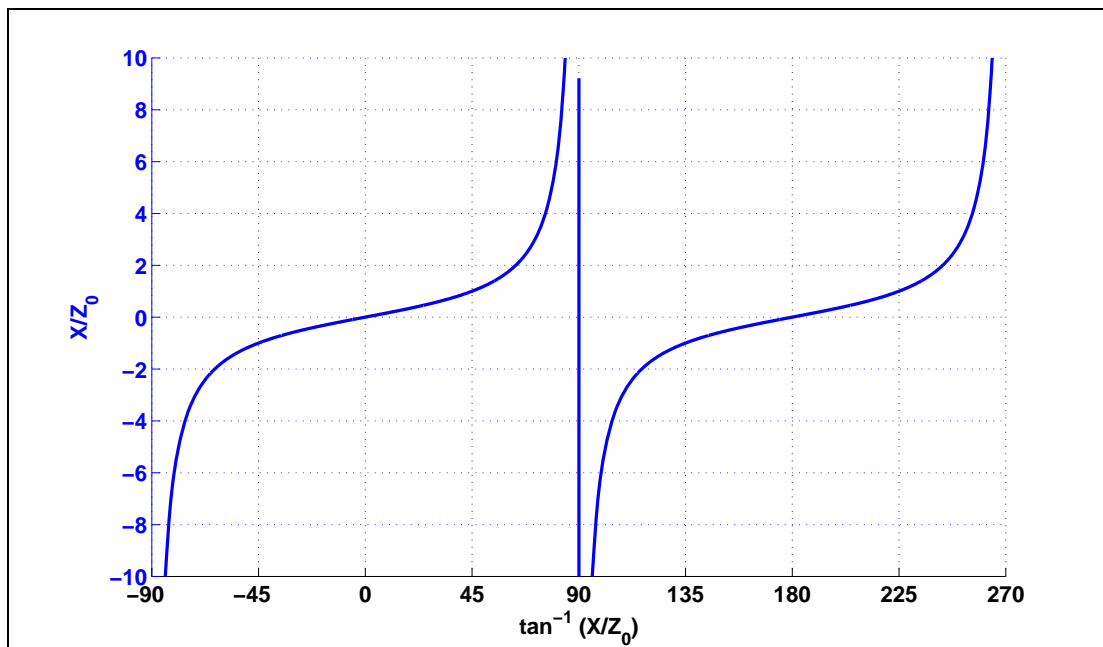
Figure 22: X/Z₀ as a function of tan-1(X/Z₀)

The circuit of Fig.23 is proposed to provide such tunability. Assuming that this tuning is provided by the variable inductor (L_t), the circuit to have two zeros one at the beginning of tuning range (L_{min}) and one at the end of the range (L_{max}). This means that

one of the LC branches in the circuit should resonate with L_{min} (Eq.13) and the other one should resonate with L_{max} (Eq.14). This will also guaranties a pole for the jX between L_{min} and L_{max} (Eq.15).
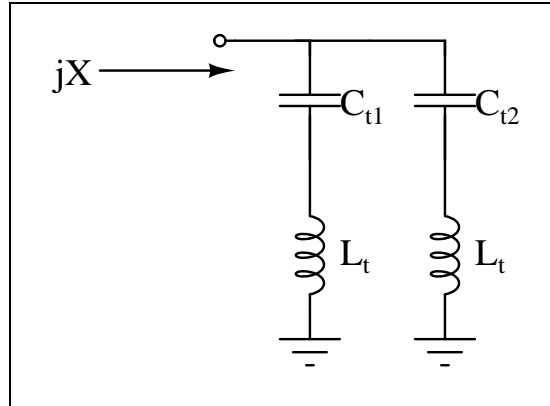
Figure 23: Proposed termination circuit for 360^0 phase shifter

Equation 13

$$\omega = \frac{1}{\sqrt{C_{t1} \times L_{min}}} \Rightarrow C_{t1} = \frac{1}{\omega^2 L_{min}}$$

Equation 14

$$\omega = \frac{1}{\sqrt{C_{t2} \times L_{max}}} \Rightarrow C_{t2} = \frac{1}{\omega^2 L_{max}}$$

Equation 15

$$L_t = \frac{L_{max} + L_{min}}{2} \Rightarrow jX \rightarrow \infty$$

E.g. if the tuning range of the inductors is between L_{min}=0.9nH and L_{max} =1.8nH, the required capacitors would be for center frequency of 4 GHz is given in Eq.16.

Equation 16

$$C_{t1} = 879\text{fF}$$
$$C_{t2} = 1.759\text{pF}$$

In this thesis the emphasize is implementing the 90^0 phase shifter, but implementing 180^0 and 360^0 ones uses the same approach but only different reactive networks as discussed.

2.5 – Simulation results for the lumped phase shifter

Using the coupler of section 2.3.4 and reactive network of section 2.4.1 the 90^0 phase shifter has been implemented (Fig.24). According to previous calculations, by tuning LX from 677 pH to 1.025 nH, the phase shift of 90^0 should be achieved for the circuit in Fig.24. Cadence simulation has been used to verify this circuit.
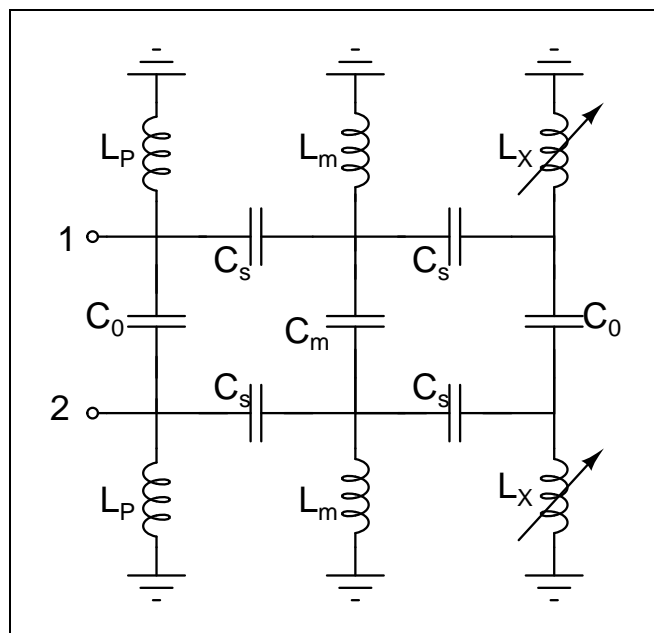
Figure 24: 90^0 phase shifter schematic

Fig.25 shows the simulated magnitude response of S_{11} of the circuit with different value of inductors in the mentioned range (677 pH to 1.025 nH). The simulation shows a matching better than 14 dB in the desired frequency range (3.7 GHz to 4.3 GHz). Since the structure is symmetric, S_{22} of is the same as S_{11}. Inductors are assumed lossless in this simulation.
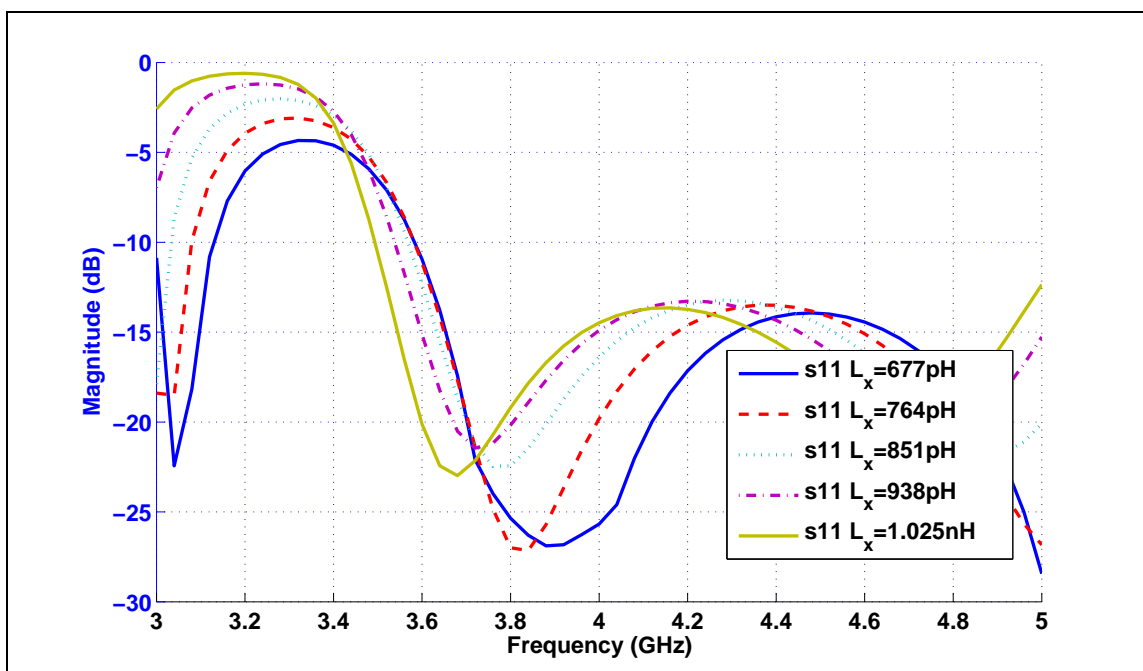
Figure 25: Magnitude of S_{11} vs. frequency for different inductance values

Fig.26 provides the magnitude of S_{21} for the phase shifter vs. frequency. This insertion loss is better than -0.2 dB at the frequency of interest (3.7 GHz to 4.3 GHz) and is very close to zero insertion loss.
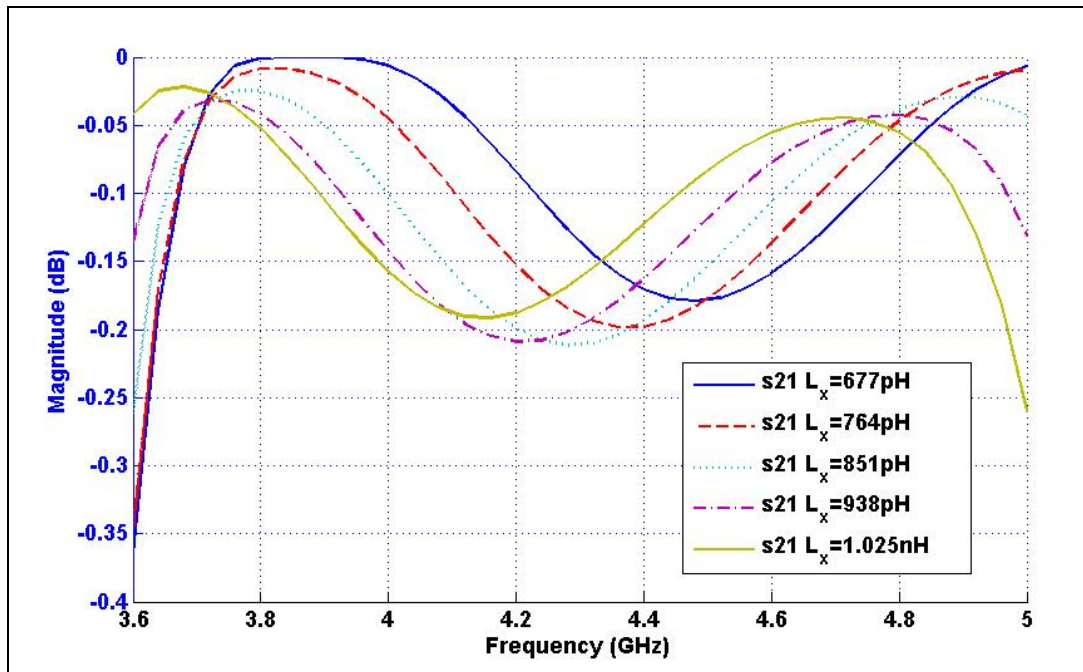
Figure 26: Magnitude of S_{21} vs. frequency for different inductance values

Fig.27 shows the phase behavior of S_{21} versus frequency for different inductance values. In a communication block the phase should be linear in the bandwidth of operation to keep the information on the phase of the signal. This makes the phase linearity an important issue for a wide band system. A typical parameter for estimating the phase linearity is the group delay of the system. A system with linear phase should have a constant group delay. Fig.28 shows this phase shifter has the group delay with variation less than 300 pS from 3.7 GHz to 4.3 GHz.
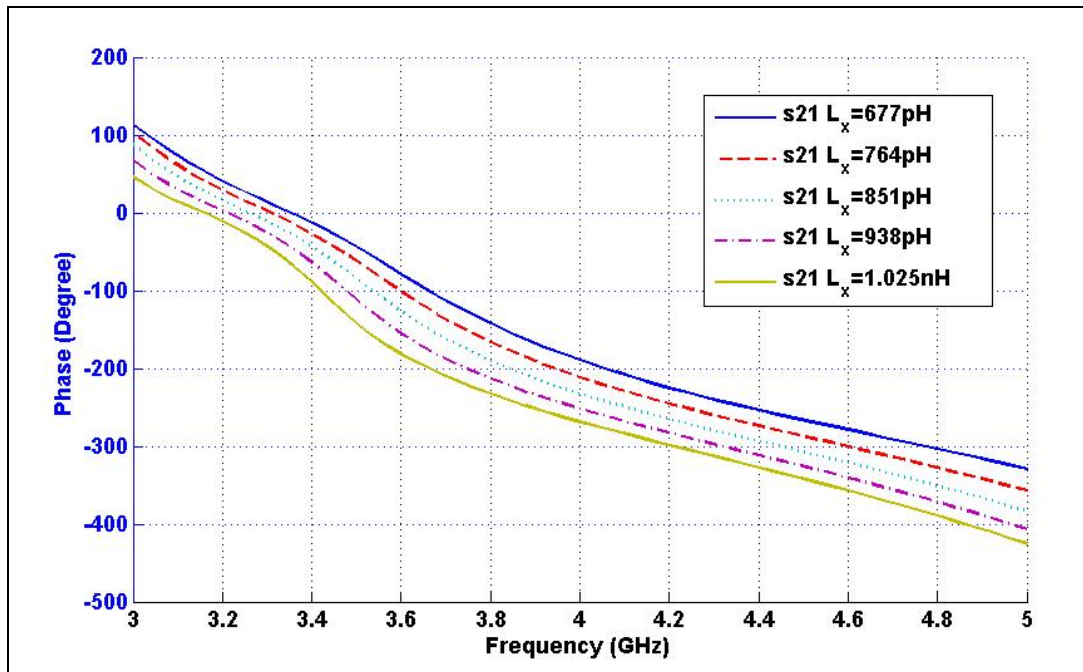
Figure 27: Phase of S$_{21}$ vs. frequency for different inductance values
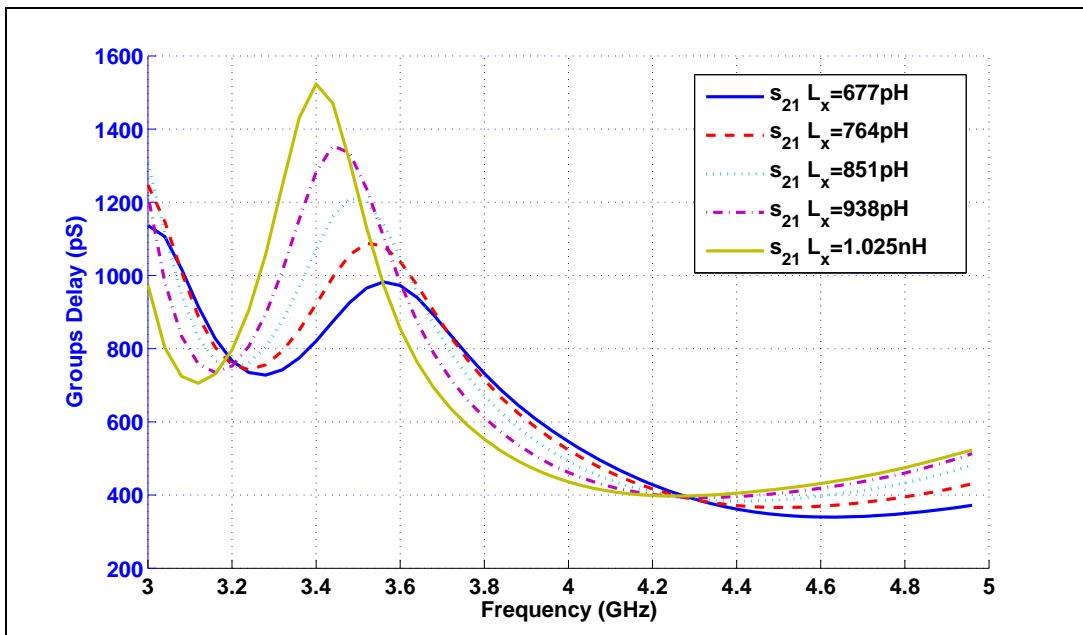
Figure 28: Simulated group delay of S$_{21}$ vs. frequency for different inductance values

Finally, the phase shift of the circuit versus the inductance value has been simulated (Fig.29). According to the plot, with tuning range of less than 677 pH to 1.1 nH the 90^0 phase shift range can be achieved.
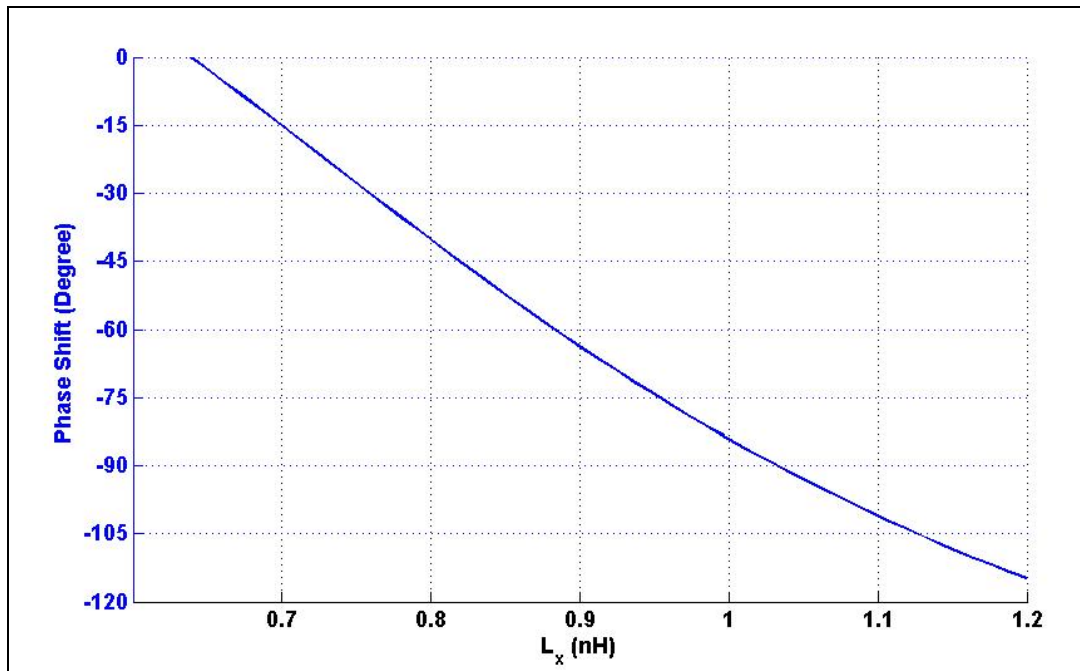
Figure 29: Phase shift vs. termination inductance

In this section we designed the lumped model of phase shifter and we simulated the lumped model with ideal elements. According to the simulation results, the proposed architecture works as a phase shifter. In the next section we design the appropriate active inductors and replace the ideal inductors of this design with their active counterparts.

3. ACTIVE INDUCTOR DESIGN

3.1 – Introduction

In the past, active inductors have been widely used for implementation of active RC filter [29], [30]. Since the bandwidth of the active inductors was limited, they were usually used in KHz range filters before the invention of the switched capacitor filters [31], [32].

Increased cut-off frequency and improvements in advanced semiconductor transistors provided the feasibility of using active inductors in microwave frequencies. Due to high cut-off frequency in GaAs FETs, these devices were used for implementing microwave active inductors [33]. But since GaAs process is not compatible with digital CMOS process, integrating the active inductor with the whole receiver system on a single chip is not possible.

With recent improvements in the short channel CMOS devices, the advanced CMOS process can compete with the GaAs process in terms of bandwidth of operation (f_t > 100 GHz [34]). As a result one can think of implementing active inductors in microwave frequencies using advanced CMOS technology.

3.2 – Different types of active inductors

Active inductors can be implemented as grounded or floating active inductors (Fig.30). A passive inductor is a floating inductor in general; this means floating active inductors can theoretically replace all kinds of inductors.

There has been several implementation of floating active inductors [35], [36], but the main issue of all implementations is stability at high frequencies. This high frequency stability problem is more severe in CMOS technology, because the value of gate-drain capacitor (C_{gd}) is in the order of gate-source capacitor (C_{gs}) which makes the device deviate from unilaterally stable region and increases the chance of instability at higher frequencies.
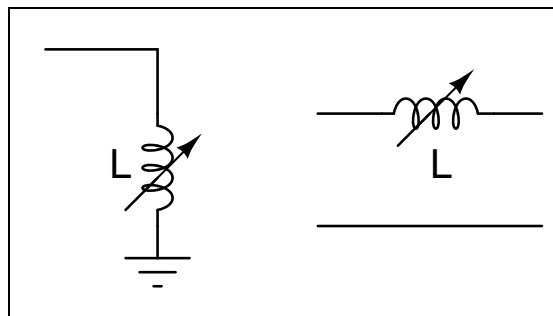
Figure 30: Grounded active inductor (left), floating active inductor (right).

Therefore, the phase shifter with grounded inductors (Fig.31) has been selected for active implementation, as it has only grounded inductors.
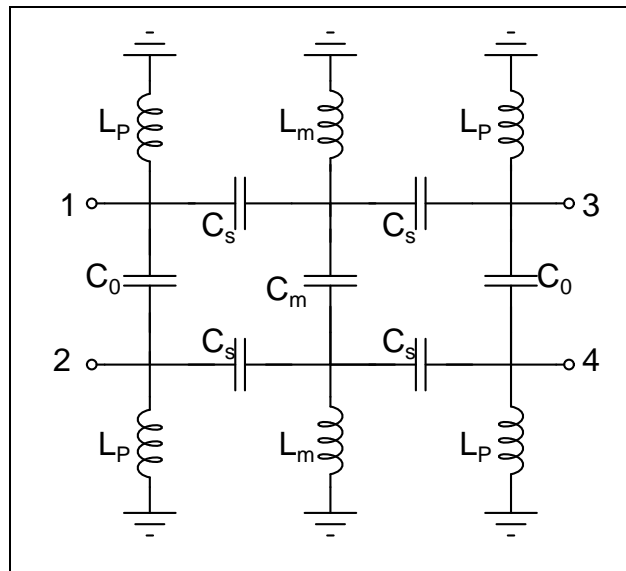
Figure 31: Lumped equivalent models of three-branch distributed coupler with grounded inductors

3.3 – Implementation of grounded active inductors

The first generation of active inductors has been implemented by employing a gyrator terminated with a capacitor so called gyrator-C active inductor [37], [38] (Fig.32). The value of this inductor is given by Eq.17.
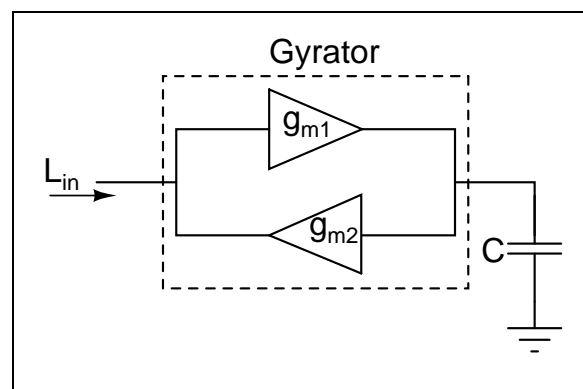
Figure 32: Gyrator-C active inductor

Equation 17

$$L_{in} = \frac{C}{g_{m1} \times g_{m2}}$$

According to Eq.17 if C is around 500 fF, to have inductance of 1 nH, gm should be around 25 mmho. Eq.18 shows the approximate formula of g_m as a function of (W/L) and I_C where (W/L) is the aspect ratio of the CMOS transistors used to implement the g_m section and I_C is the drain current of the same transistor. Considering the high cut-off frequency requirement of the transistor, the value of (W/L) can not be very high. This means for having such a high gm, I_C of the transistor should be very high (around 10 mA). Therefore the power consumption of this CMOS active inductor for practical purpose would be very high.

Equation 18

$$g_m \approx \sqrt{2\mu C_{OX} I_C (W/L)}$$

The other available approach to implement active inductors is using the output impedance of a source follower. From basic circuit theory we know that the output impedance of a simple source follower is inductive [39] (Fig.33 and Eq.19).
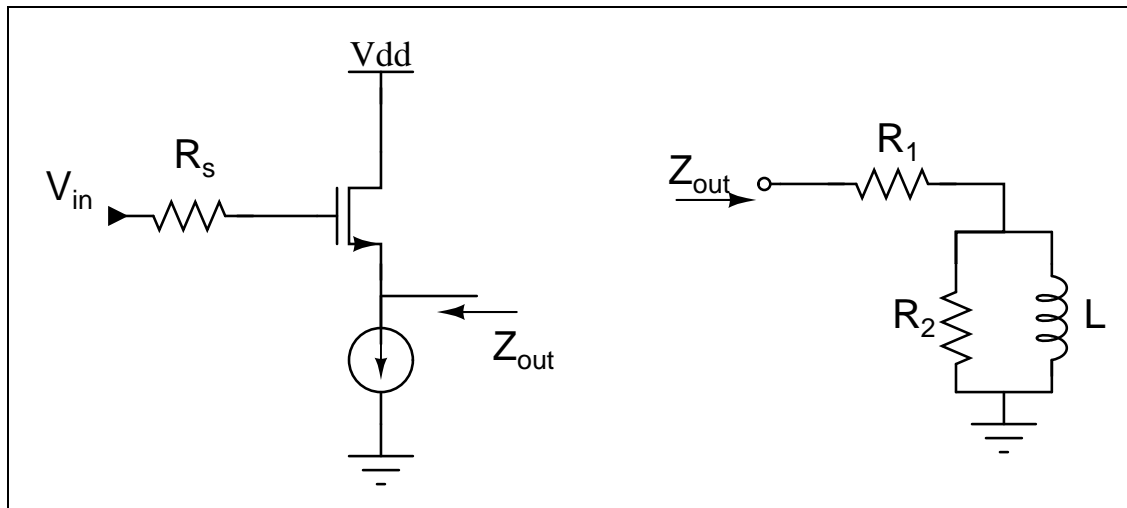
Figure 33: Output impedance of a source follower (left), source follower equivalent circuit for output impedance (right).

Equation 19

$$L = \frac{C_{GS}}{g_m}\left(R_S - \frac{1}{g_m}\right)$$

Equation 20

$$R_1 = \frac{1}{g_m}$$

Equation 21

$$R_2 = R_S - \frac{1}{g_m}$$

As Eq.19 shows, a reasonable value of inductance can be achieved with a reasonable value for g_m and Rs (e.g. g_m = 1 mmho and R_s = 1.1 KΩ while C_{GS} = 100 fF results in L = 1nH).

3.4 – Quality factor of active inductors

The quality factor (Q) specifies the amount of stored energy in the inductor over the dissipated energy (Eq.22). Therefore, a high Q inductor is desired for having a low loss phase shifter. The Q of inductor is usually determined by amount of parasitic resistance in the inductor.

Equation 22

$$Q = \omega \frac{E_{Stored}}{P_{Loss}}$$

3.4.1 –Quality factor of source follower inductor

For the active inductor of Fig.33, the Q is given by Eq.22. Using Eq.19, Eq.20 and Eq.21, Q can be calculated for the circuit in Fig.33 (Eq.23). Therefore with estimated values of g_m = 1 mmho and R_S = 1.1 KΩ, C_{GS} = 100 fF the value of Q at 4GHz would be around 2.5 which is very low even compared to passive inductors.

Equation 23

$$Q_L = \frac{L\omega}{R_1 \| R_2} = \frac{\dfrac{C_{GS}}{g_m}\left(R_S - \dfrac{1}{g_m}\right)}{\left(R_S - \dfrac{1}{g_m}\right)\left\|\left(\dfrac{1}{g_m}\right)\right.}\omega = R_S C_{GS}\omega$$

According to Eq.19, RS is tied to a certain value for the required inductance. Thus with this structure we can not increase the Q further.

3.4.2 – Active inductor with improved quality factor

Based on inductive effect of source follower output impedance, Hsiao [40] proposed an active inductor with improved quality factor (Fig.34, Eq.24, Eq.25, Eq.26 and Eq.27). In fact this active inductor is a cascaded source follower (M_1 and I_1) and amplifier (M_2, M_3 and I_2). The output of the source follower is fed back to the input of amplifier. This structure is known as super buffer because of its low output impedance.
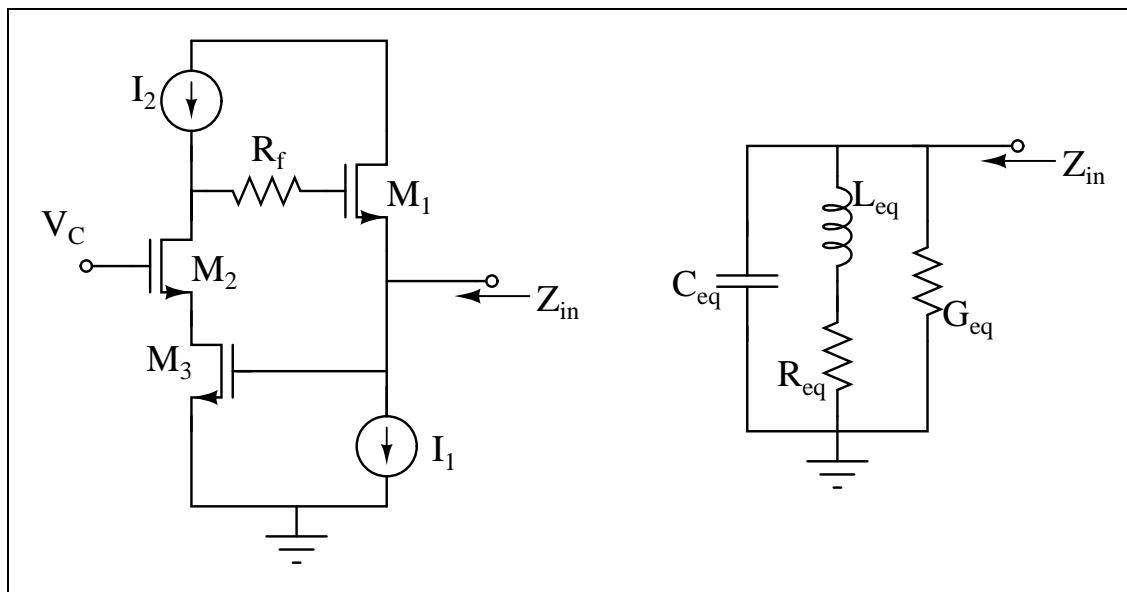
Figure 34: Proposed high-Q active inductor (left), equivalent circuit for the proposed active inductor (right).

Equation 24

$$C_{eq} = C_{gs3}$$

Equation 25

$$G_{eq} = \frac{2g_{ds2} + R_f g_{ds2}^{2}}{R_f g_{ds2} + 1}$$

Equation 26

$$R_{eq} = \frac{g_{m1}g_{ds2}g_{ds3} + \omega^2\left[g_{m2}C_{gs1}^2 - g_{m1}C_{gs1}C_{gs2}\left(R_f g_{ds2} + 1\right)\right]}{g_{m1}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}^2}$$

Equation 27

$$L_{eq} = \frac{g_{m1}g_{m2}C_{gs1} + \omega^2 C_{gs1}^2 C_{gs2}\left(R_f g_{ds2} + 1\right)}{g_{m1}^2 g_{m2}g_{m3} + \omega^2 g_{m2}g_{m3}C_{gs1}^2}$$

This low output impedance (higher equivalent trans-conductance of the circuit - G_m-) together with overall high series resistance in gate of M_1 (R_f in series with output impedance of M_2) results in a high-Q inductor, while keeping the value of inductor in a reasonable range (L < 10 nH). The simulation results for the active inductor using 0.18-µm CMOS technology are provided in Fig.35. It shows that the modified active inductor can achieve a high Q at frequencies below 2 GHz. Although the performance of this circuit is much more improved compared to the simple source follower, but for low loss application, higher Q values are needed at higher frequencies.
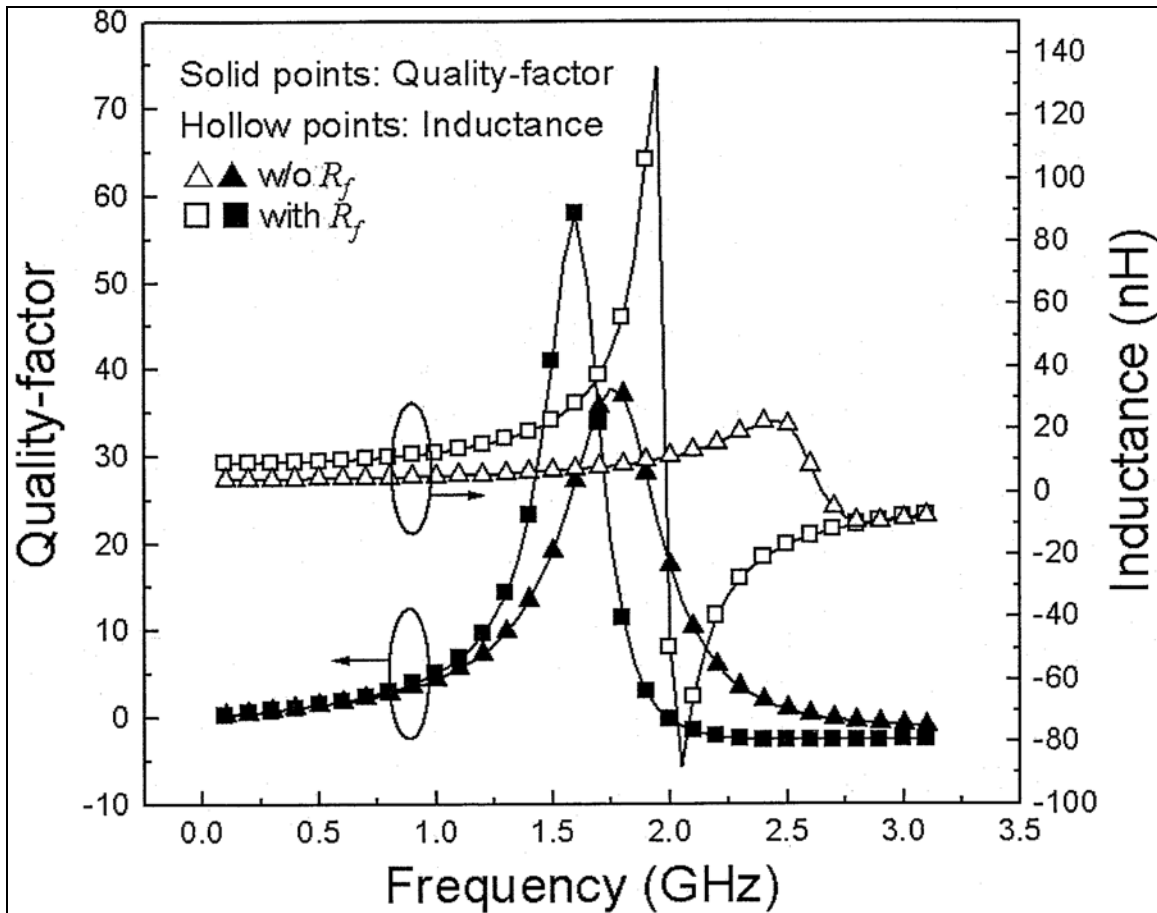
Figure 35: Simulation result of active inductor in [40]

3.5 – Proposed structure for active inductor

For our application the active inductor in [40] has been modified such that it provides higher Q in frequencies around the operating frequency of the phase shifter (4 GHz). The idea is to use impedance boosting technique to increase the gain of the amplifier (M_2, M_3 and I_2). As a result the overall G_m and overall series resistance in gate of M_1 both increase (Fig.36). The increase in G_m provides higher bandwidth of operation

while the high G_m along with high output impedance of the amplifier provides high quality factor.
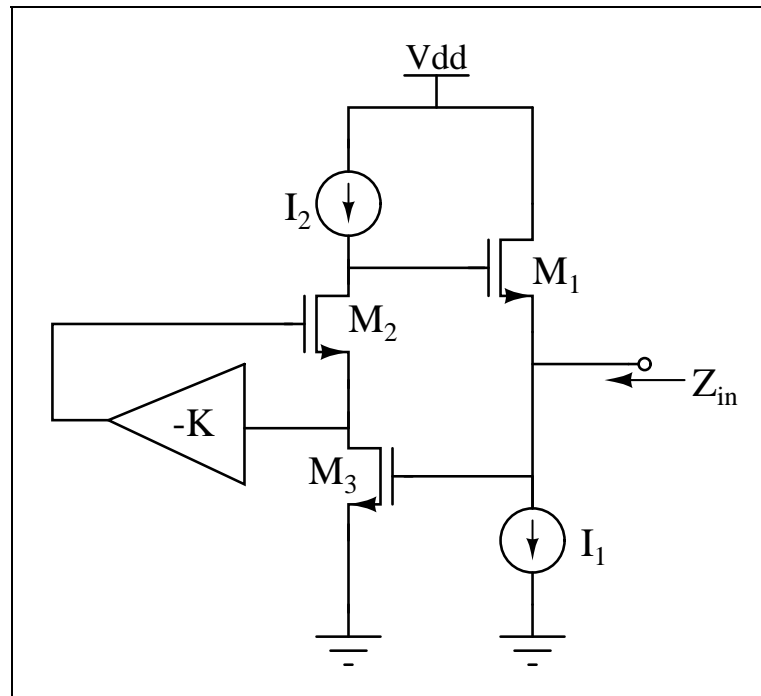
Figure 36: Proposed active inductor with impedance boosting

To provide impedance boosting a boosting amplifier is needed. This amplifier is realized using a common source amplifier with cascode load (Fig.37). The final schematic of the proposed active inductor including the bias circuit, boosting amplifier and current sources is provided in Fig.38. In this circuit, Z_{in} provides the inductor which can be tuned using the V_{tune} voltage which itself will tune I_1 (bias current of M_1).
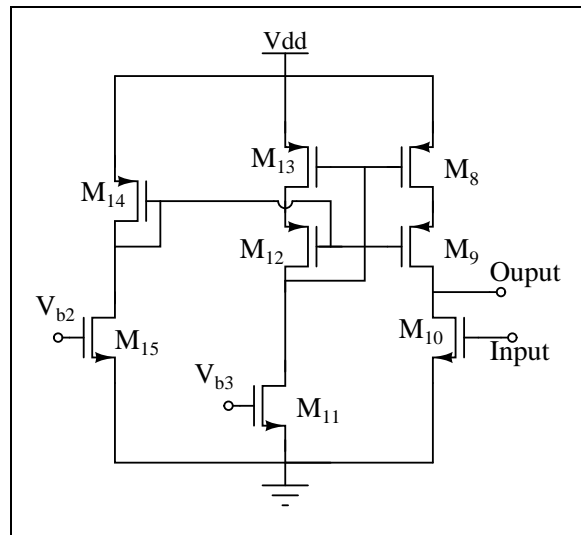
Figure 37: Proposed boosting amplifier
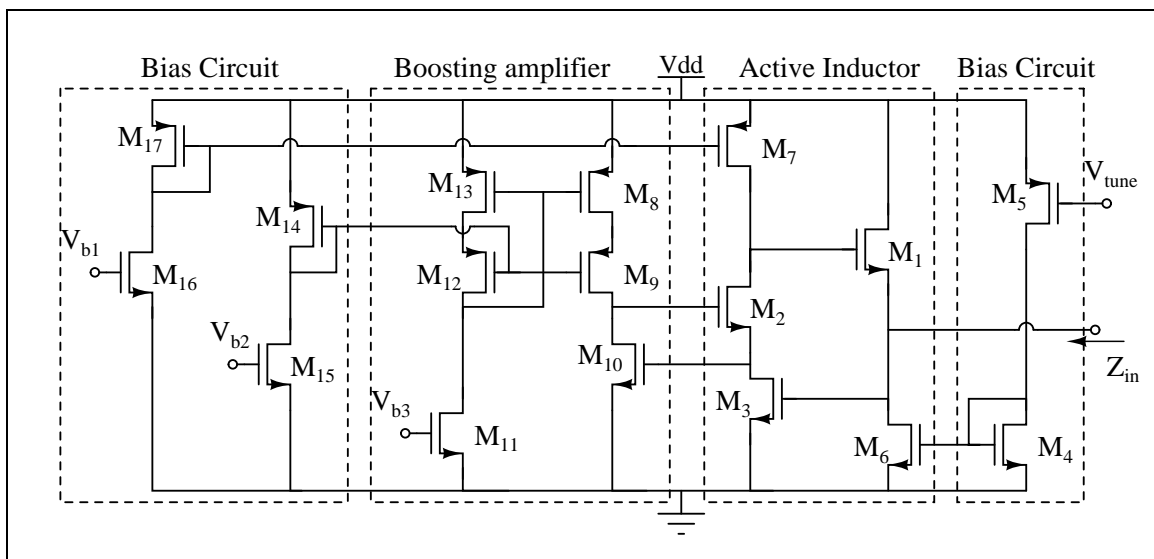
Figure 38: The proposed circuit for active inductor with impedance boosting

3.5.1 – Frequency analysis of the proposed active inductor

The parasitic capacitor of the inductor is set by C_{gs3} and therefore it is the limiting factor in bandwidth of the inductor. On the other hand since the circuit has two feedback loops (l_{p1} and l_{p2} in Fig.39), stability needs to be considered in the design.

All feedback loops in this circuit are around single stage amplifiers therefore each loop has only one low frequency pole. As a result stability could be provided by adding compensation capacitors to the nodes providing the low frequency poles (C_{c1} and C_{c2}). But since the circuit is working in very high frequency, the parasitic capacitors of those nodes provide the required compensation capacitor. In section.4, the stability of the phase shifter has been simulated to proof the stability of inductors in the structure.
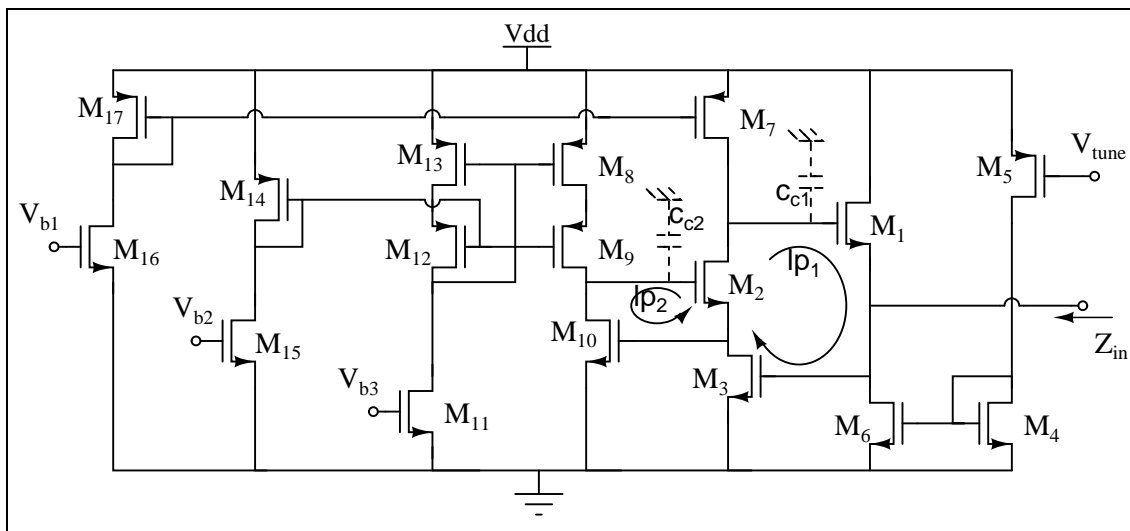
Figure 39: Model of the active inductor as an amplifier

3.5.2 – Noise analysis of the proposed active inductor

One of the main drawn backs of using active inductor is the noise contribution of the active elements in the system. In order to have an idea for how to improve the noise contribution of this circuit, the noise analysis of the inductor has been performed in this section.

If the gate of M_3 is disconnected from drain of M_6 (in Fig.38), the circuit would be an amplifier in which gate of M_3 is the input and drain of M_6 is the output (Fig.40). This amplifier has one boosted gain stage and a source follower afterward.
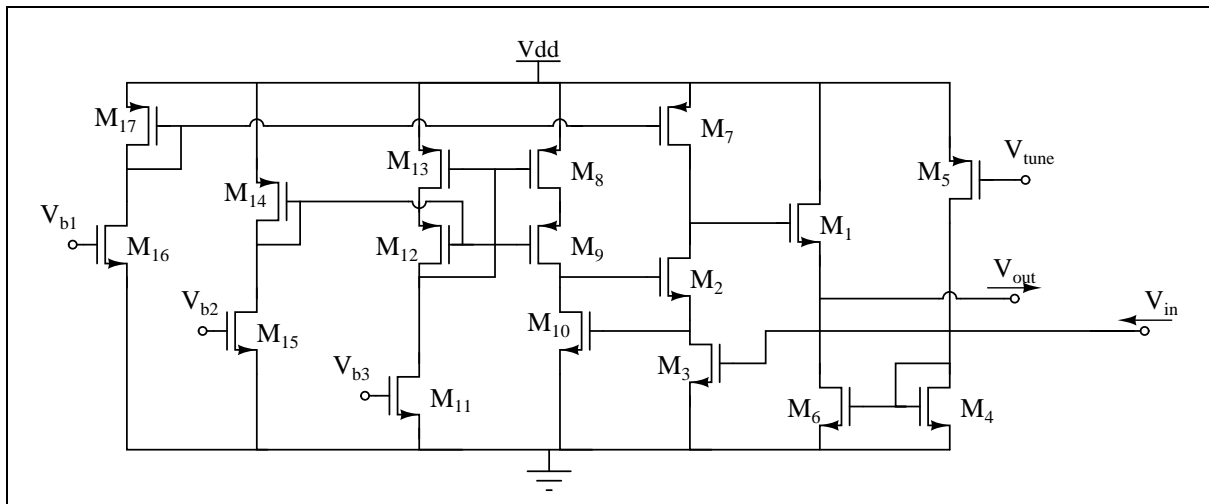
Figure 40: Active inductor as an amplifier

The first step to finding the noise contribution is to find the input referred noise of the amplifier at the gate of gate of M3. The input referred noise for a cascaded system in terms of input noise of each block ($v^2_{noise\_Ak}$) and gain of each block (A_{Vk}) is given by Eq.28. Since the first stage amplifier is a high gain amplifier, this noise is dominated by the noise of the first stage.

Equation 28

$$v_{noise\_input}^2 = v_{noise\_A_1}^2 + \frac{v_{noise\_A_2}^2}{Av_1^2} + \frac{v_{noise\_A_3}^2}{Av_1^2 \times Av_2^2} + \dots$$

In the first stage the noise of cascode transistor (M_2) is negligible and therefore the effective noise sources would be noise of M_3 (input transistor) and M_7 (active load transistor), hence the noise referred to the input of M_3 is given by Eq.29. Considering the input noise of a single transistor as Eq.30 [39], the input referred noise voltage would be given by Eq.31.

Equation 29

$$v^2_{n(input)} = v^2_{n(M3)} + \left(\frac{g_{m7}}{g_{m3}}\right)^2 v^2_{n(M7)}$$

Equation 30

$$v^2_{n(M)} = \frac{4kT\gamma}{g_m}$$

Equation 31

$$v^2_{n(input)} = \frac{4kT\gamma}{g_{m3}}\left(1+\left(\frac{g_{m7}}{g_{m3}}\right)\right)$$

It should be noticed that the inductor is the amplifier in unity gain structure. Thus the noise of the inductor is the noise of amplifier, referred to the output while having unity gain feedback. This means the equivalent noise at the output would be the same as the equivalent noise in the input (Fig.41).
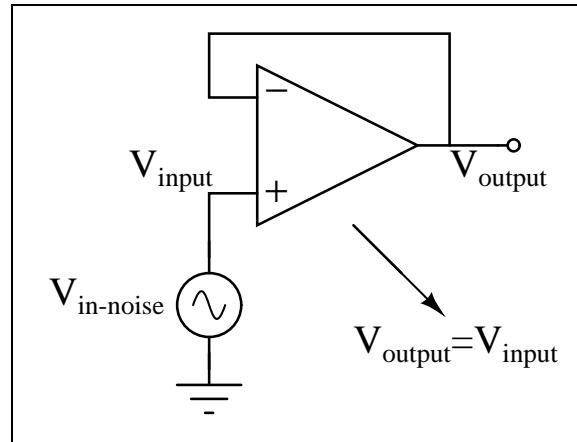
Figure 41: Noise of the unity gain amplifier

As a result the equivalent output noise of the active inductor is approximately given by eqation.32.

Equation 32

$$v^2{}_{nL} = \frac{4kT\gamma}{g_{m3}}\left(1+\left(\frac{g_{m7}}{g_{m3}}\right)\right)$$

As a result, to reduce the noise of inductor, one should design the circuit such that the g_{m3} be as high as possible while g_{m7} should be small. g_{m3} can be increased by increasing either the bias current or W/L of the M_3. Increasing W/L reduces the bandwidth of operation, therefore there is a trade-off between noise, bandwidth and power consumption in this circuit.

3.5.3 – Final design of proposed active inductor

The circuit of Fig.38 has been designed for inductance of 1.025 nH at 4 GHz. For noise consideration, the gm of M_3 should be high. M_2 should consumed small headroom

to provide a good voltage swing at the gate of M_1 which affects the linearity of the circuit. M_7 should have high output impedance, thus the length of this transistor is three times the minimum length. The main issues for determining the sizing of M_8, M_9 and M_{10} is the stability of the boosting amplifier and keeping the pole in internal nodes at high frequencies. M_6 should consume less headroom for increasing the output swing of the inductor (which directly affects the linearity of the inductor). Finally, M_1 is determined by value of required inductance, since its C_{gs} is transformed by the circuit to inductance. The mentioned considerations have been used for implementing the inductor with minimum power consumption. Table 3 provides the sizes of the CMOS transistors in Fig.38 in 0.18μm TSMC technology.

Table 3: Device sizing for active inductor with impedance boosting (Fig.38)

Transistor Number	Width (one finger)	Number of Fingers	Length
M1	1.5 μm	30	.18 μm
M2	1.8 μm	6	.18 μm
M3	1.8 μm	30	.18 μm
M4	1.8 μm	20	.18 μm
M5	.36 μm	7	.18 μm
M6	.36 μm	20	.18 μm
M7	1.8 μm	12	.54 μm
M8	1.8 μm	25	.18 μm
M9	1.8 μm	25	.18 μm
M10	1.8 μm	2	.18 μm
M11	.36 μm	7	.18 μm
M12	1.8 μm	25	.18 μm
M13	1.8 μm	25	.18 μm
M14	1.8 μm	4	.18 μm
M15	.36 μm	5	.18 μm
M16	.36 μm	15	.18 μm
M17	1.8 μm	12	.18 μm

3.5.4 – Simulation result of proposed active inductor

The proposed active inductor in Fig.38 is simulated using Cadence. The dimensions in Table 3 have been used to perform the simulations.

Fig.42 shows the simulated inductance and quality factor versus frequency. The inductance value around 4 GHz is 1.14 nH which is very close to what we want (1.025 nH). According to Fig.43 the quality factor of the inductor is better than 68 at 4 GHz which is high, comparing to passive inductors or the active inductor in [40] (at the same frequency).
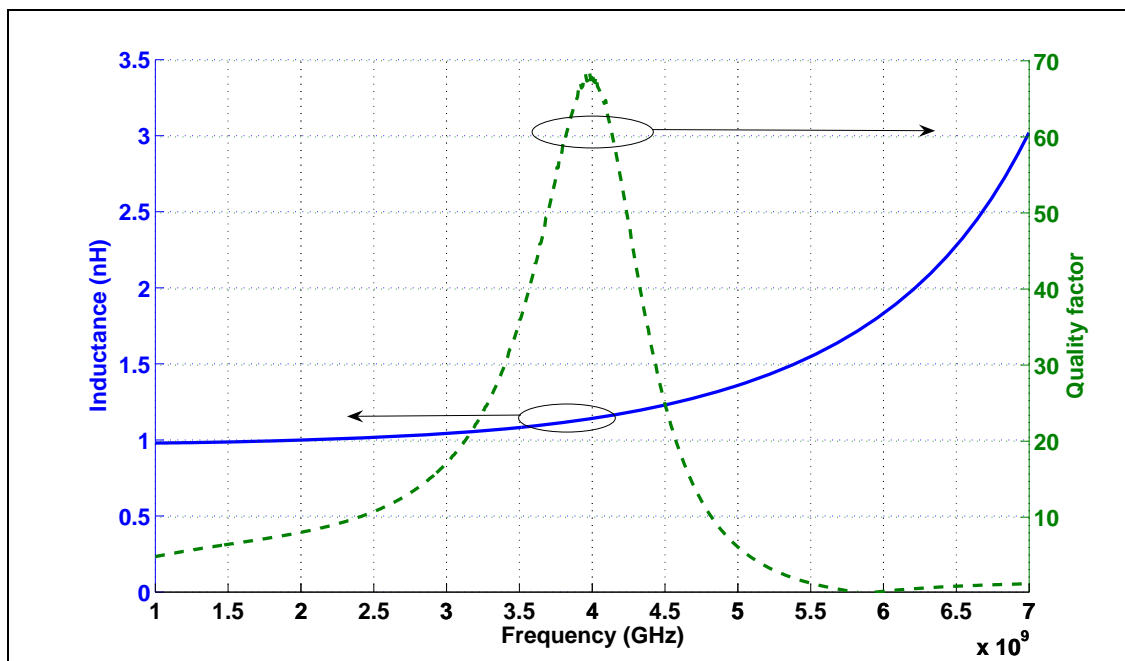
Figure 42: Inductance and quality factor versus frequency
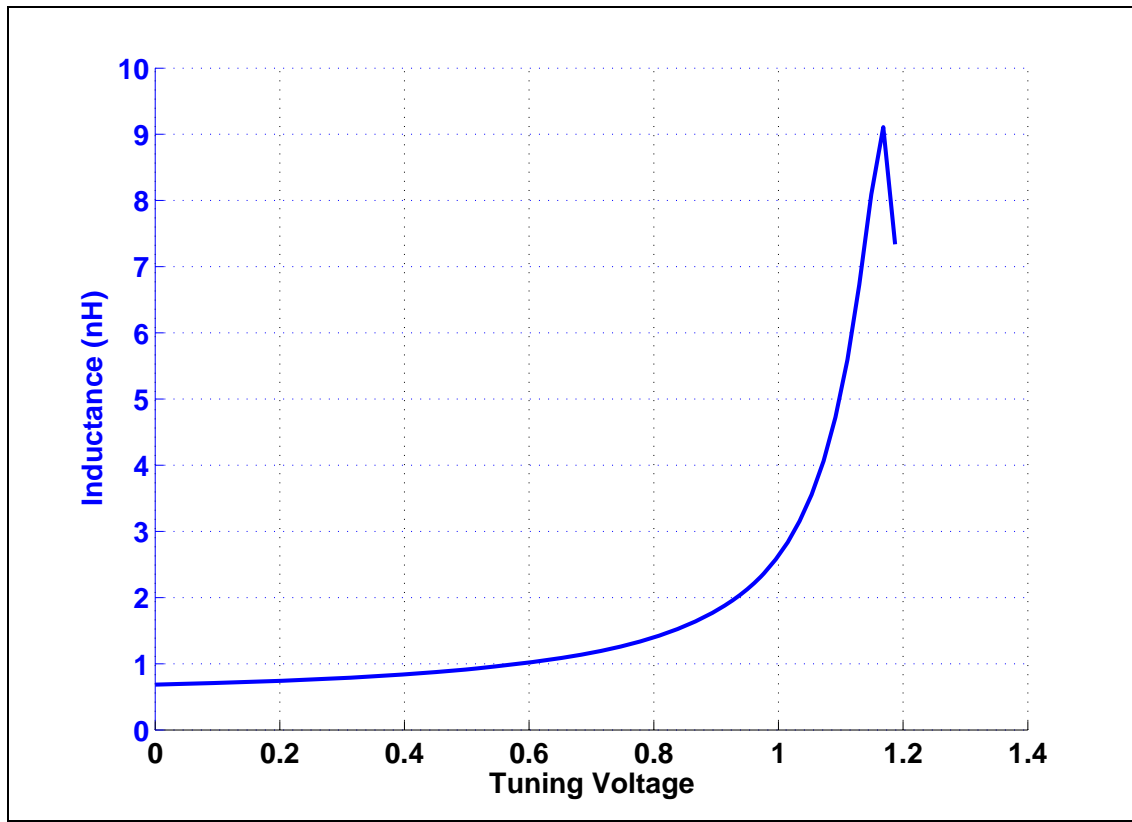
Figure 43: Inductance versus tuning voltage for the inductor
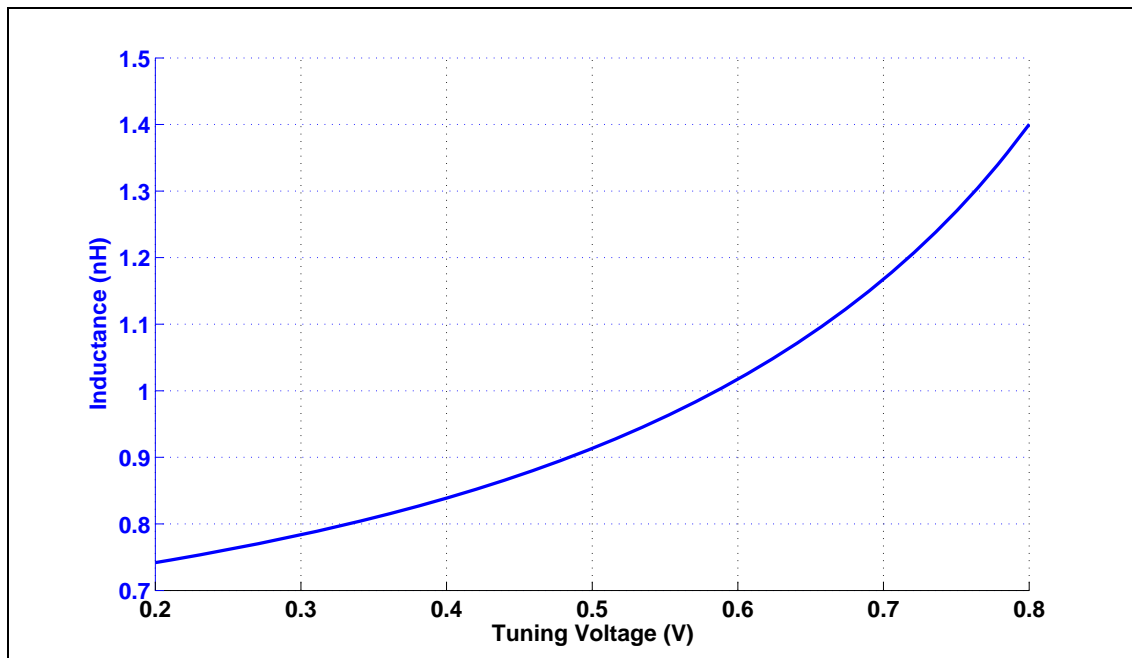
Figure 44: Inductance versus tuning voltage for between 0.2 – 0.8 volts

Fig.43 shows the inductance versus tuning voltage. This simulation shows that this inductor provides a high tuning range (.7 nH to 9 nH) with variation of tuning voltage. We are interested in more linear region. Fig.44 shows the tunability of the inductor for the tuning voltage between 0.2 - 0.8 volts where the inductor has more linear behavior. The inductor can be tuned from .7 nH to 1.4 nH (2:1 tuning ratio) tuning voltage between 0.2-0.8 volts.

Using noise analysis in cadence, output noise of the active inductor has been simulated (Fig.45). It shows an output noise voltage of 0.93 nV at 4 GHz. This is equivalent to the noise of a 52 Ω resistor.
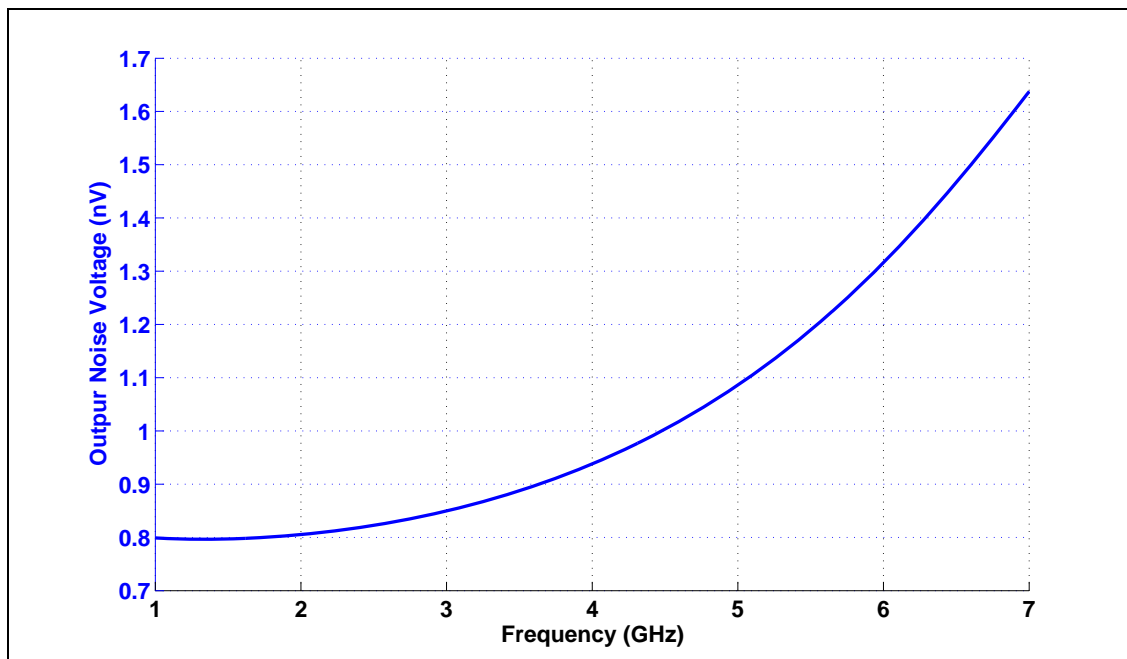
Figure 45: Output voltage noise of the inductor versus frequency

Simulation shows the total DC power consumption of the inductor is around 9mW. This value includes the power consumption for biasing network of the inductor.

In this section the required active inductor for the phase shifter is implemented and the design has been verified with simulation. Next section will present the final implementation of the reflective phase shifter using the proposed active inductor.

4. PHASE SHIFTER FINAL DESIGN AND SIMULATION RESULT

4.1 – Final design

By employing the active inductor (Fig.38), in the active phase shifter prototype (Fig.24), the final active phase shifter has been designed. Since the inductor in the middle (L_m) is around half the value of the inductors in both sides (L_p, L_X), it has been realized by two parallel active inductors (Fig.46). The inductors have been tuned to provide the required inductance. After achieving the desired inductance, only L_x will be used for tuning the phase shifter.
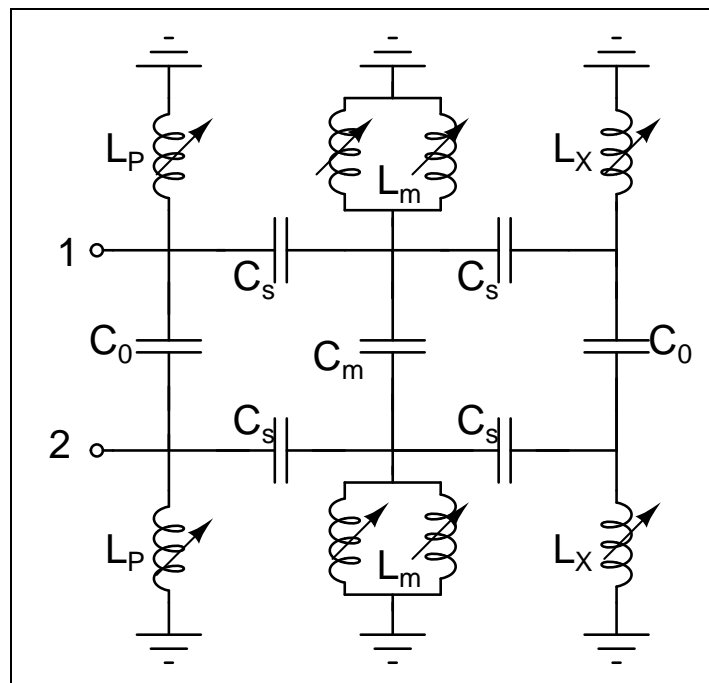
Figure 46: Lumped equivalent models of the reflection-type phase shifter

4.2 – Simulation result

For stability of a two port network, the two-port network should suffice properties of Eq.33 [41]. Fig.47 shows the simulation result of K_f and B1f in Cadence for this phase shifter. This shows the stability of phase shifter in bandwidth of operation.

Equation 33

$$K_f > 1$$

$$\beta > 0$$
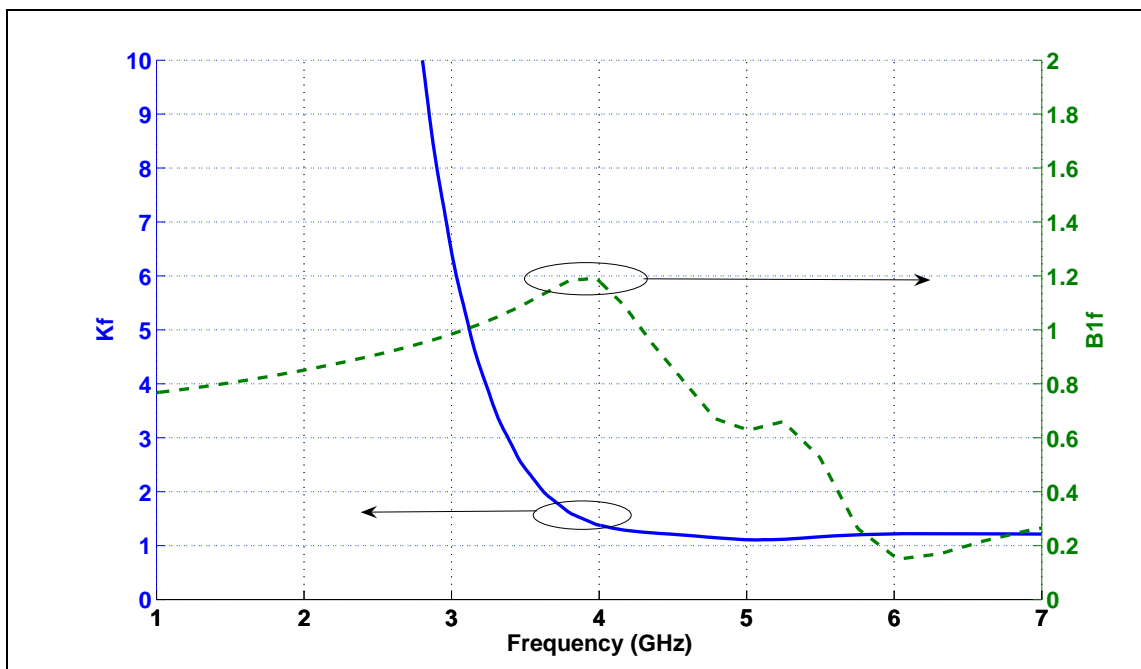
Figure 47: Simulation of K_f and β for stability of the phase shifter

Fig.48 shows the simulated phase shift of the phase shifter versus the tuning voltage (V_{tune}) for L_X. The tuning range is around 150^0. The $0-90^0$ is achieved within $0.7v - 1.3v$ voltage tuning range (Fig.49).
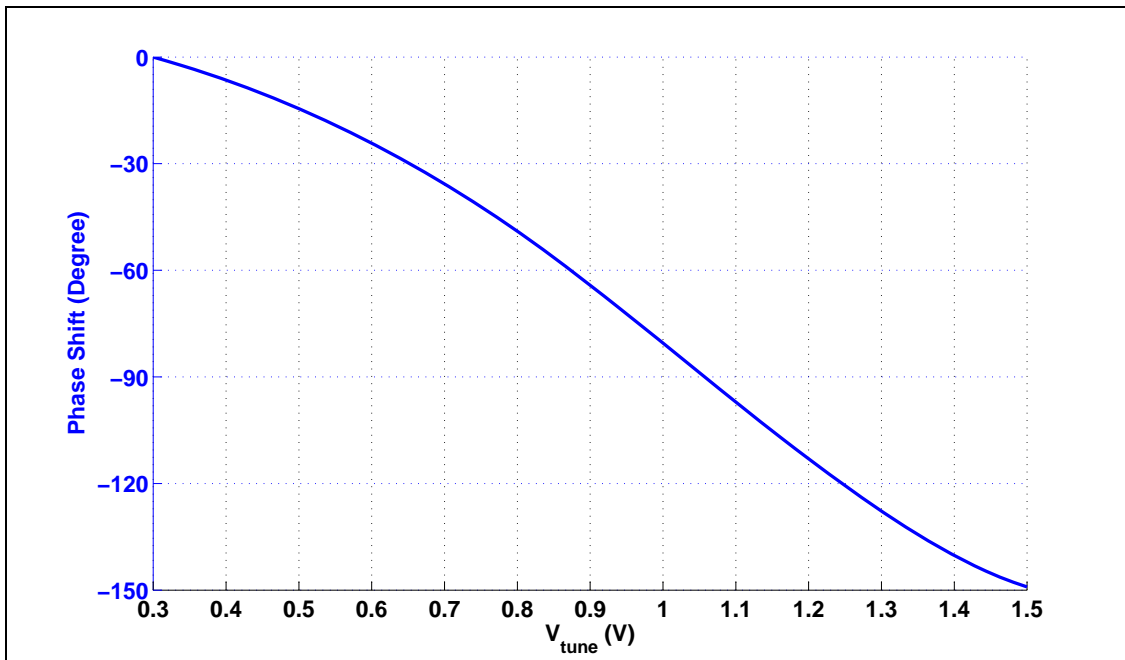
Figure 48: Relative phase shift versus tuning voltage
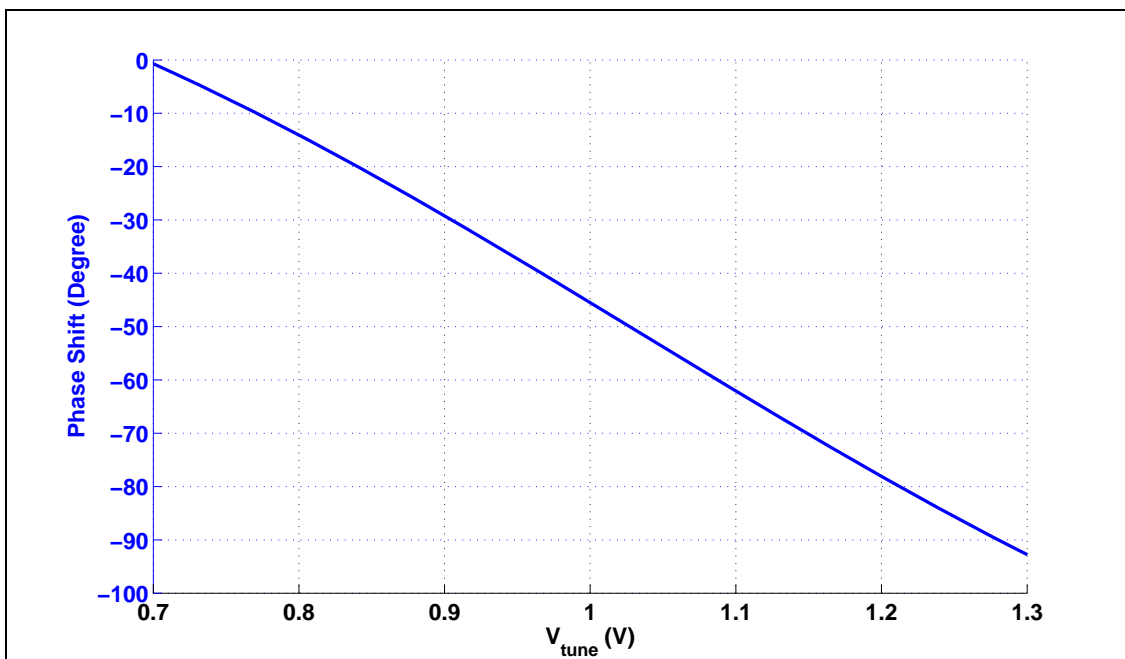
Figure 49: Relative 0-90^0 phase shift versus tuning voltage

The phase shifter needs to provide acceptable input and output matching within the bandwidth of operation (3.5 GHz to 4.5 GHz). The simulated S_{11} in Fig.50 shows the phase shifter has better than 12 dB input matching from 3.5 GHz to 4.5 GHz. As the phase shifter is a symmetric structure, S_{22} has the same response to S_{11}. The S_{11} response has been simulated for different value of tuning voltages and proves the structure has acceptable matching for the entire tuning range.
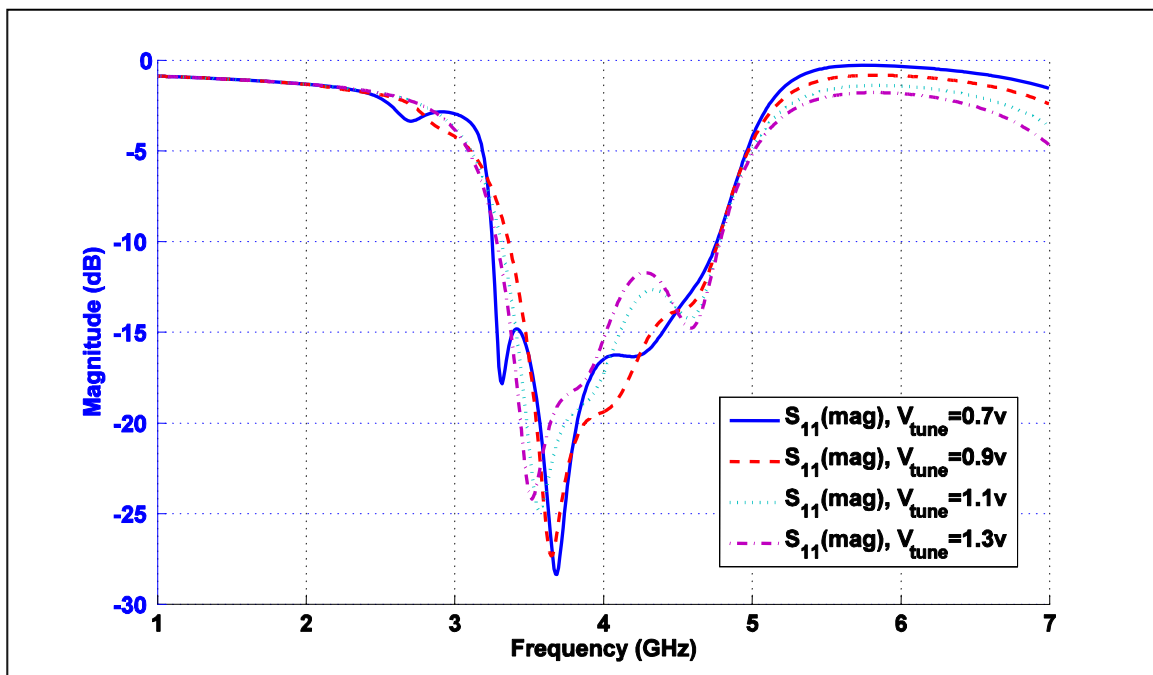
Figure 50: S_{11} (S_{22}) of the phase shifter for different value of tuning voltage

One of the most important properties of the phase shifter is the insertion loss of the phase shifter. Insertion loss shows the attenuation of the output signal with respect to the input signal. As shown in Fig.51, the phase shifter has an insertion loss better than 0.5 dB of S_{21} from 3.5 GHz to 4.5 GHz for different values of tuning voltage. The high value of active inductor's quality factor reduces the resistive loss of the circuit.

Simulated S_{11} and S_{22} results guaranty the performance of this phase shifter for the entire phase shift tuning range for 3.5 GHz to 4.5 GHz (better than 12 dB matching with less than 0.5 dB insertion loss in a bandwidth of 1 GHz).
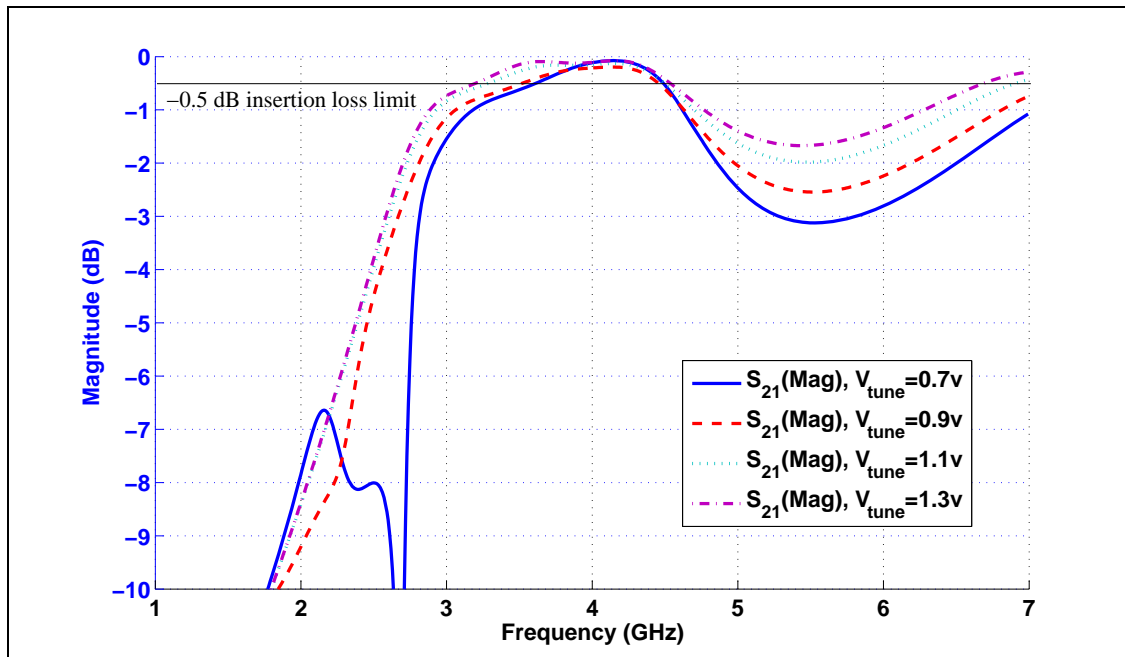
Figure 51: S_{21} of the phase shifter for different value of tuning voltage

The other important characteristic of a phase shifter is the phase linearity versus frequency. The slop of phase versus frequency is defined as group delay. By having a linear phase, the system has a constant group delay. Which means the time delay of the system for different frequencies is the same; for wideband receivers it is important that all thee frequency components of the modulated signal is delayed equally to present the distortion at the output of the demodulator. Fig.52 shows the phase response of the phase shifter for different tuning voltages. The phase response of the phase shifter is linear from 3.5 GHz to 4.5 GHz with different tuning voltages.
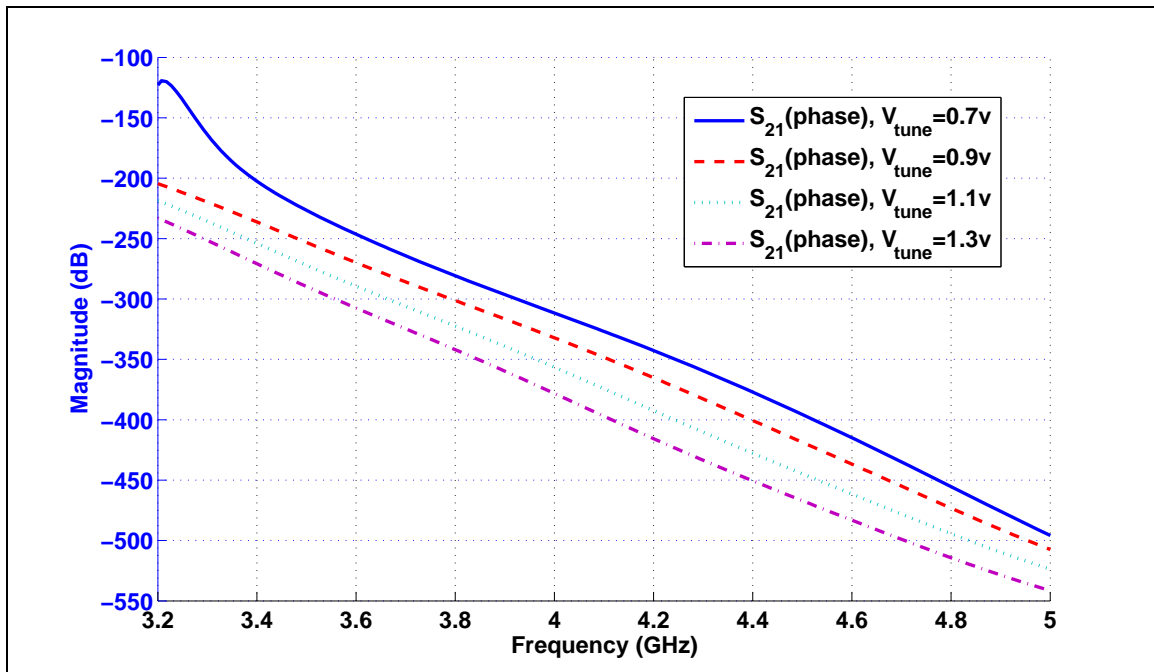
Figure 52: Phase response of the phase shifter for different value of tuning voltage

Unlike passive phase shifters, active phase shifters are noisy which means they contribute in the noise level of the circuit. Fig.45 shows the noise figure of the active phase shifter. According to Fig.53, the phase shifter has a noise figure of around 19 dB at 4 GHz. The noise figure is less or equal to this value in the 1 GHz bandwidth of operation (3.5 GHz - 4.5 GHz).

The other disadvantage of active phase shifters over passive ones is the linearity. Active devices have worse linearity compared to their passive counterparts. To investigate this effect, the output power is simulated vs. different values of input power. The simulation results in Fig.54 shows that the active phase shifter has a 1-dB compression point of -17dBm which is equivalent to IIP3 level of -7dBm.
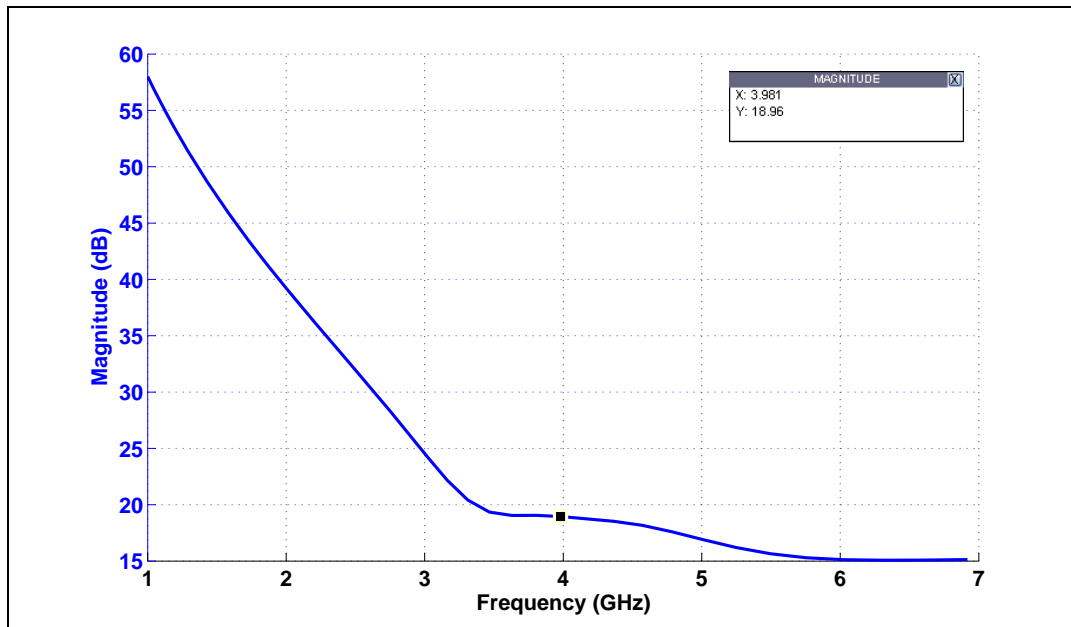
Figure 53: Noise figure simulation of the phase shifter
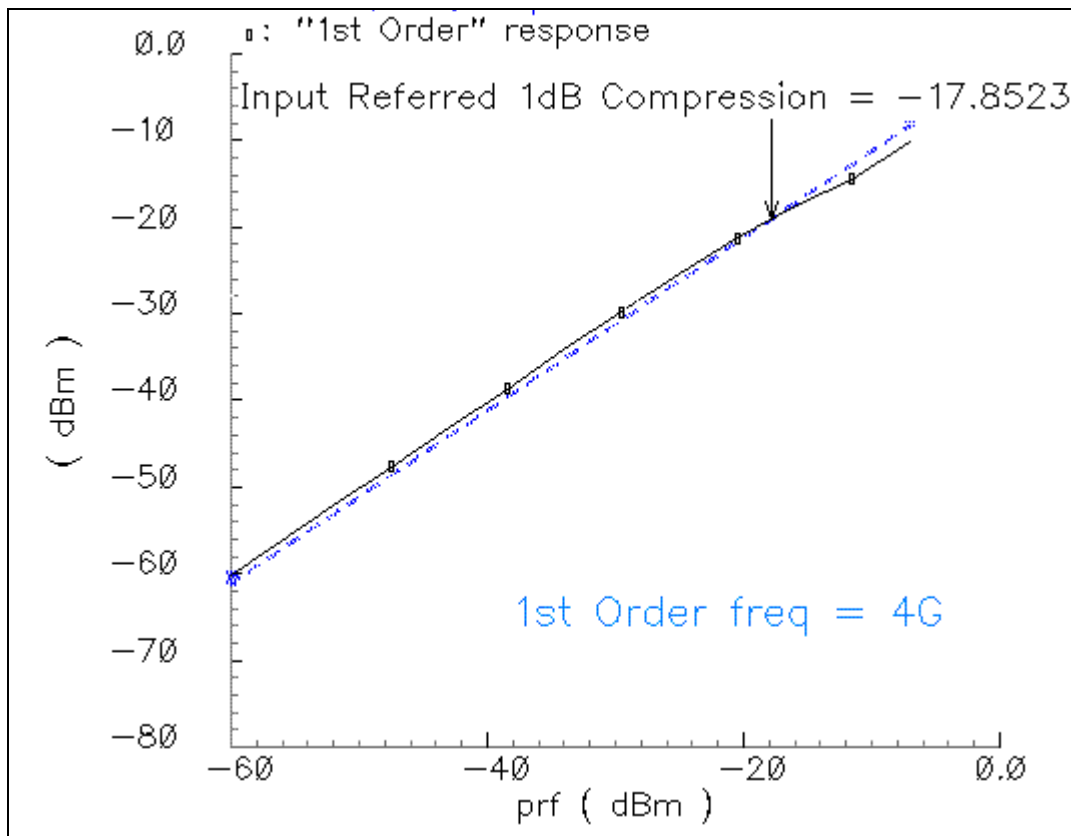
Figure 54: Simulated of 1-dB compression point for the active phase shifter

Finally, the power consumption has been evaluated for the simulated phase shifter. The phase shifter consumes 36 mW, I_{DC} = 20 mA. This is the price to pay for having a monolithic, integrated low loss CMOS phase shifter. The simulation results for the phase shifter are summarized in Table 4.

Table 4: Summery of simulation result for the active phase shifter

Parameter	Value
S11	< -12 dB
S21	> -.5 dB
tuning range	0-90^0
1-dB compression point	-17 dBm
NF	19 dB
power consumption	36 mW

4.3 –Comparison of active and passive phase shifter in a receiver chain

It looks like that the high noise figure of the active phase shifter would increase the overall noise figure of the receiver, but the overall noise figure not only depends on the noise of each building block but also depends on the gain/loss of other stages.

To perform a case study, the total noise figure of a cascaded phase shifter and a mixer is investigated (Fig.55). Since the phase shifter is located before the mixer the noise factor is given by Eq.34. In this equation, F_{PS} and F_{Mixer} are the noise factor of phase shifter and the mixer and L_{PS} is the insertion loss associated with the phase shifter.

Equation 34

$$F_{eq} = F_{PS} + L_{PS}\left(F_{Mixer} - 1\right)$$
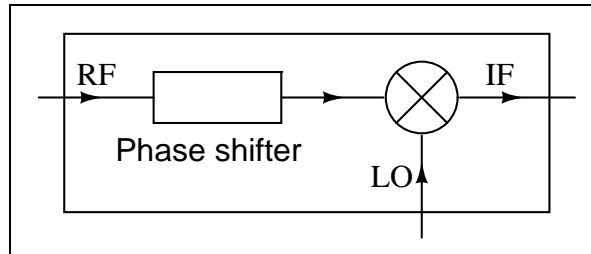
Figure 55: Cascaded structure of a phase shifter and a mixer

For comparison between noise behavior of passive and active phase shifter we can note that the quality factors of passive inductors around 4 GHz is in the order of 5.5 to 8.5. Thus for a fair comparison, one should consider the insertion loss of passive phase shifter due to low-Q passive inductors. Fig.56 displays the S_{21} of the passive phase shifter in Fig.16 with Q of 5.5, 7 and 8.5 for integrated inductors. It is obvious that the loss associated with the passive phase shifter (-7.5dB to -14dB for 3.5 GHz to 4.5 GHz bandwidth) is very high compared to the insertion loss of active one (-.5dB).

E.g. considering the passive phase shifter with Q = 7 and a 0.18μm passive RF CMOS mixer with noise figure of 15dB [43], the equivalent noise factor and noise figure is given by Eq.35.

Equation 35

$$F_{eq} = 307.22 \Rightarrow NF_{eq} = 24.87dB$$
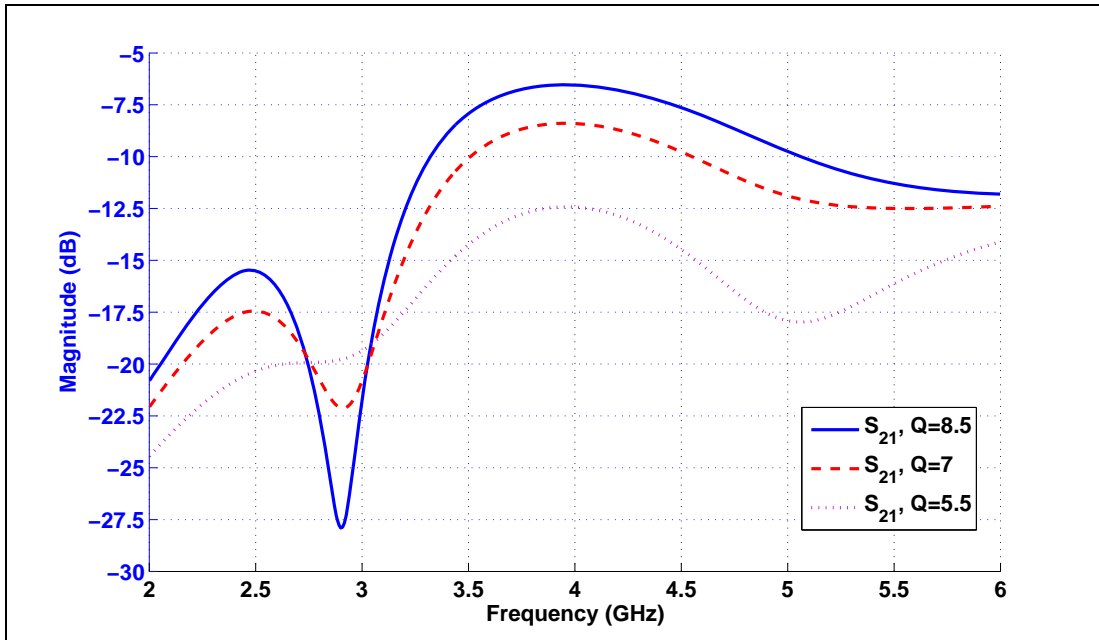
Figure 56: S_{21} of the passive phase shifter for different values of Q

Using the same mixer with the properties of designed active phase shifter, the noise figure and noise factor has been calculated in Eq.36.

Equation 36
$$F_{eq} = 113.79 \Rightarrow NF_{eq} = 20.56dB$$

As a result the noise figure of the active phase shifter + passive mixer has 4.3 dB improvement compared to the passive phase shifter + passive mixer combination.

In addition the assumed 15 dB noise figure for a mixer is based on [42] which is a passive CMOS mixer. In case an RF mixer is employed in the receiver chain [43], due to higher NF of active mixer compared to the passive one ($NF_{active\ mixer} \approx 20$ dB), the overall NF of the active phase shifter + active mixer has 7.2 dB improvement compared to NF of passive phase shifter + active mixer combination. (Eq.37)

Equation 37

$$NF_{eq\_passive} \approx 29.96dB$$

$$NF_{eq\_active} \approx 22.79dB$$

Regarding linearity, in the passive implementation of phase shifter-mixer chain, the dominant source of non-linearity is the mixer, while in the active implementation it is expected to have non-linearity effects due to phase shifter as well as the mixer. The IIP_3 of the mixer and phase shifter is expected to be the same ([43] and Fig.54). Thus one can conclude that the resulted IIP_3 of the chain containing the active phase shifter is worse than one with passive phase shifter. This is true only when the mixers for both cases have the same gain but in a real design the mixer after the passive phase shifter should provide additional gain to compensate the high loss resulted from the passive phase shifter. Since there is a trade-off between gain and linearity, the mixer, after the passive phase shifter, would have worse linearity compared to the other one. As a result, the overall linearity of passive and active implementations is not that different and depends on the design of the block which comes after them in the receiver chain.

The main advantage of passive phase shifter over active phase shifter is its zero power consumption.

4.4 –Conclusion

In this work an active phase shifter in 4 GHz has been designed using TSMC .18μm design kit. The integrated circuit performance has been simulated to support the idea (Table 4). Finally, the active implementation has been compared with passive implementation in the receiver chain. The main advantages of active implementation over the passive implementation are:

o Very compact size

o Lower loss

o Lower overall noise figure in the receiver chain

But it suffers from high power consumption.

5. INTRODUCTION TO 24 GHz VCO

5.1 – CMOS 24 GHz ISM band transceivers

With the increasing demand for high data rate communication systems and automotive radars millimeter-wave transceivers are becoming more attractive. Also increasing the frequency of operation shrinks the size of passive components and provides more integration for on-chip implementation. The available industrial, scientific and medical (ISM) bands at millimeter-wave are located at 24, 60, 122 and 245 GHz [44].

Millimeter-wave transceivers require semiconductor processes which could provide high performance in millimeter-wave frequencies. Traditionally expensive processes such as SiGe, GaAs, have been employed to impalement millimeter-wave integrated circuits. The high cost of these processes comparing to CMOS process reduced the tendency to invest on millimeter-wave transceivers for commercial application and limited their use in military applications.

With recent advances in the short-channel CMOS technology, the cut-off frequency (f_t) of CMOS transistors is becoming comparable with the advance processes (such as GaAs). This has been the main motivation for researches to implement millimeter-wave transceivers in CMOS technology. In addition to relatively low cost of fabrication, CMOS technology provides the potential for integrating the transceiver and digital baseband circuits on a single chip [34].

24 GHz ISM band is predicted to be used for short range and point-to-point communication. This band is becoming more attractive due to the fact that FCC has opened 22 to 29 GHz bands for automotive radar application recently [45].

5.2 – Frequency synthesizers

Frequency synthesizers are one of the most essential parts in a fully integrated transceiver system. This block is responsible for providing the required oscillation frequencies to the mixer/mixers in the circuit and sinks the channel frequency according to the incoming signal.

Fig.57 shows the block diagram of a typical frequency synthesizer. Frequency synthesizers are usually one of the most power hungry blocks in the transceivers. This power consumption increases dramatically with increase in the frequency of operation.
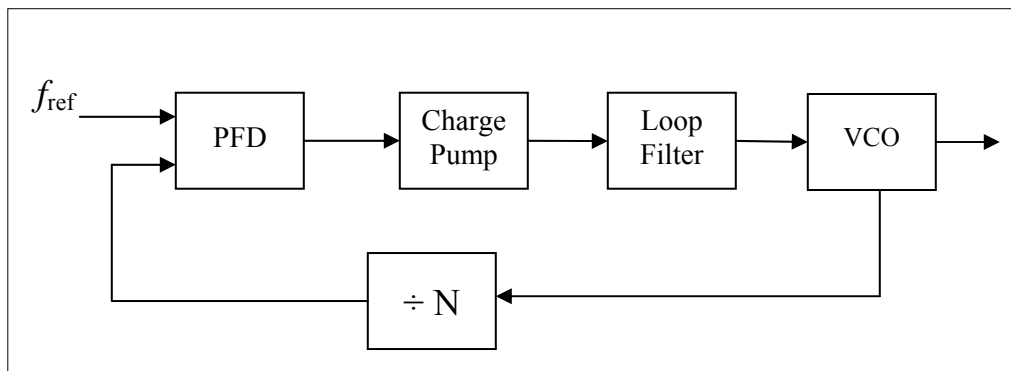
Figure 57: Typical direct frequency synthesizer

Voltage controlled oscillators are the main block in the frequency synthesizer, since it determines the final output frequency of the synthesizer. The main property of

the VCO is its phase noise which shows how selective it can provide a single tone at the output. Any other tone in the output signal of VCO will be directly interpreted to additional noise and distortion in the transceiver.

Eq.38 shows the simplified equation for phase noise of VCO [46]. In this equation, L{Δf} is the single sideband phase noise spectral power density in dBc/Hz, Q is the quality factor of the tank, F is the noise factor of the VCO, Psig is the signal power in Watts , f0 is the center frequency of oscillation in Hz, k is the Boltzmann's constant and T is the absolute temperature in degrees Kelvin.

Equation 38

$$L\{\Delta f\} = \frac{1}{8Q^2} \frac{FkT}{P_{sig}} \left(\frac{f_0}{\Delta f}\right)^2$$

The quality factor of inductor increases with frequency (Eq.39) while the Q of capacitors decreases with frequency (Eq.40). The quality factor of tank in terms of quality factor of inductor and capacitor is given by Eq.41. Since in lower frequency Q of capacitors are higher than Q of inductors, the value of Q in Eq.38 for low frequencies is dominated by the Q of inductors (f < 20GHz) but in higher frequency Q of inductors are higher than Q of capacitors, so for high frequencies (f > 20 GHz) this quality factor of the tank will be dominated by the Q of capacitor.

Equation 39

$$Q_L = \frac{2\pi f L}{R}$$

Equation 40

$$Q_C = \frac{1}{2\pi f R}$$

Equation 41

$$\frac{1}{Q_{\tan k}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

Considering the phase noise in Eq.38, the phase noise drops dramatically with increase in frequency. As discussed, the Q is not expected to increase with frequency when working in frequencies beyond 20 GHz (since it is dominated by Q of capacitor). This means with n times, multiplication of fundamental frequency, the phase noise degrades by n^2 times. The only option for reducing this phase noise is to increase the power (Psig). If the aim is to increase the fundamental frequency by n times but keeping the phase noise the same, the power should be increase by n^2 times.

5.3 – Indirect frequency synthesizers

In order to save power, indirect method of generating can be used [47]. Fig.58 shows the block diagram of a synthesizer based on indirect method of generating LO. In this figure, the loop is working in half of the frequency of interest. As a result the power consumption reduces dramatically in the VCO and frequency divider. Then a frequency doubler doubles the output frequency of VCO and brings it to the frequency of interest.

After that a buffer increases the output power of the structure to provide high output power to the system.
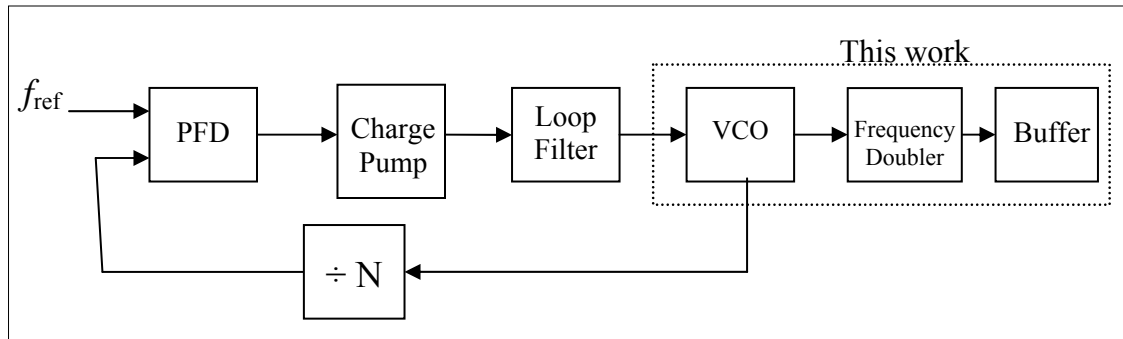
Figure 58: Typical indirect frequency synthesizer

5.4 – Overview

In this work, the VCO, doubler and buffer has been implemented using TSMC .18um CMOS process. The VCO generates a 12 GHz tone, the frequency doubler brings the signal to 24 GHz and finally the buffer provides the 24 GHz signal with high power to the output.

Followed by this section, section 6 investigates the design and characteristic of the VCO, doubler and buffer, section 7 provides simulation and measurement results for the fabricated VCO, doubler and buffer.

6. THEORY AND DESIGN OF THE VCO

In the last section, the advantages of using indirect method for generating the 24 GHz signal have been discussed. In this section the indirect VCO for 24 GHz is designed. The design consists of a 12 GHz LC-tank oscillator, frequency doubler and an output buffer.

6.1 – 12 GHz VCO

For indirect generation of 24 GHz signal, a 12 GHz VCO is needed. This VCO should have low phase noise and high tuning range while consuming less power comparing to the available 24 GHz VCOs.
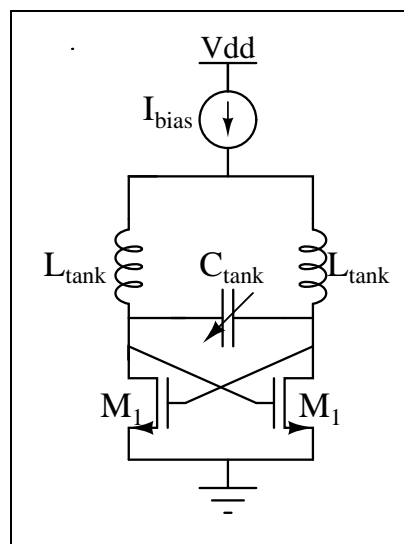
Figure 59: Typical LC-tank VCO

Equation 42

$$f_{osc} = \frac{1}{2\pi\sqrt{2L_{\tan k}C_{\tan k}}}$$

Fig.59 shows the typical structure for an LC tank VCO. In this figure, the cross coupled transistors of M_1 provide the $-G_m$ (large signal g_m) impedance for the oscillator. This negative impedance makes the circuit unstable as a result the oscillation starts, with the increase in the oscillation amplitude, the $-G_m$ drops until it gets equal to the parasitic resistors in the circuit which will limit the oscillation amplitude of the oscillator. It is important that the transistors have low input referred noise because this noise will be directly modulated to the output of the oscillator and increases the phase noise [48].

The L_{tank} and C_{tank} perform the filtering of other frequencies, and pass the desired frequency; therefore the oscillation happens only in the desired frequency. It is important that the LC tank has a high Q in order to provide good filtering of undesired signals. As a result, lower Q will be translated to higher phase noise. In order to tune the output frequency, C_{tank} is provided as a tunable capacitor, which by tuning that the oscillation frequency will be tuned accordingly (Eq.42).

Feeding the current through the source of transistors will cause the noise of the current source to be modulated and appear in the output signal; as a result the phase noise of the VCO will increase. In order to avoid this problem, the bias current is fed through the inductors on the top of the oscillator [48].

The circuit of Fig.60 is the VCO final circuit. The bias source has been implemented using PMOS transistor. The capacitors have one side grounded to cancel

out the parasitic capacitors to the ground. Three banks of capacitors have been used. C_1 has twice capacitance than C_2 and C_2 has twice capacitance than C_3. C_1 and C_2 are tuned digitally (0/1.8 v) for coarse tuning. C_3 is tuned with analog signal (0-1.8 v) for fine tuning the oscillation frequency. The tunable capacitors have been implemented with the available MOS-cap varactors in the process. The variable capacitors have been designed based on $L_m = 400$ pH.

Since the noise of M_1 is directly modulated to the output, it is important to optimize the noise on M_1. Based on power and noise trade-off M_1 has been designed to provide low noise while consuming low power (total current of circuit is designed to be 11 mA). M_{bias} is a PMOS transistor; PMOS transistors usually consume more headroom comparing to NMOS transistors. So the dimension of M_{bias} has been designed to consume minimum headroom. (Table 5)

Table 5: Device sizing for VCO in Fig.60

Transistor Number	Width (one finger)	Number of Fingers	Length
M_1	1.5 µm	24	.18 µm
M_{bias}	8 µm	64	.18 µm
M3	1.8 µm	30	.18 µm
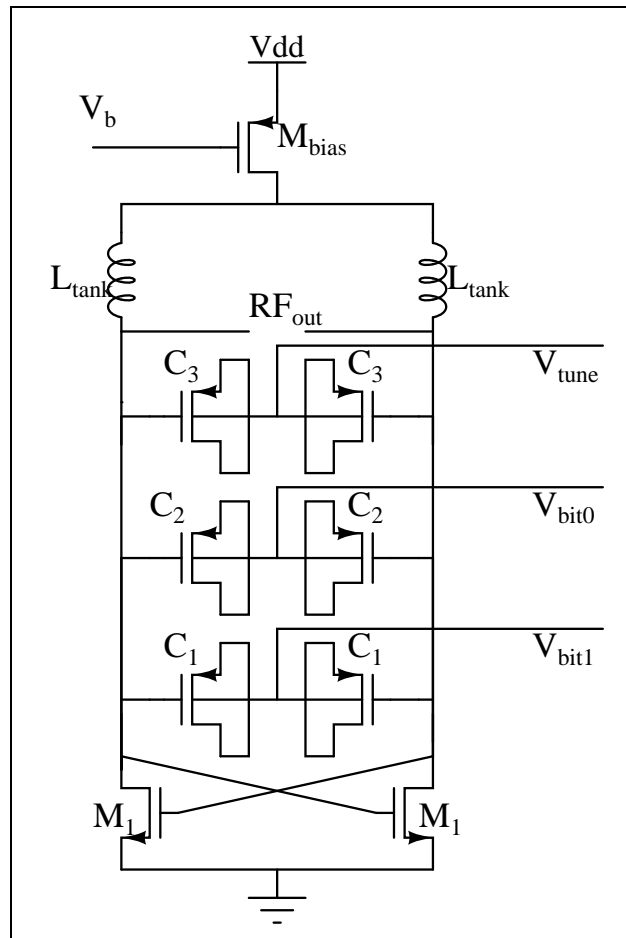
Figure 60: Implemented LC-tank VCO

6.2 – Frequency doubler

A typical mixer multiplies input signals (f_1 and f_2) which therefore generate both addition and difference of the input signal frequencies ($|f_1 + f_2| + (|f_1 - f_2|)$ (Fig.61). If both the input signals have the same frequency, the output will have two components, one is at DC and the other one is at twice the input frequency (2 f1) (Fig.62). If the DC signal is filtered out, then the output will have the $2f_1$ component. Both passive and

active mixers can be used for frequency doubler. A VCO with passive mixer as a frequency doubler is presented in [49]. The main disadvantage of passive mixer is the mixer loss and poor output signal.
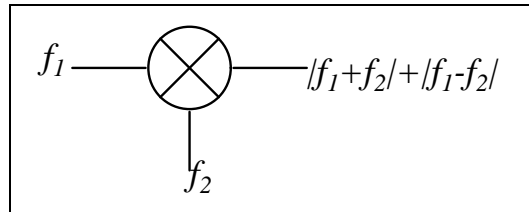
Figure 61: Mixer input and output frequencies
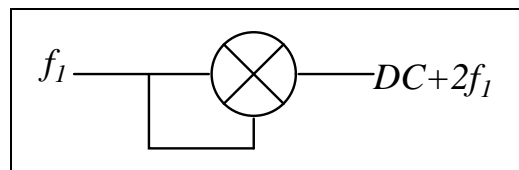
Figure 62: Mixer as a frequency doubler

In this design a double balanced Gilbert cell is used for the frequency doubler to provide higher output power for the VCO [50]. Fig.63 shows the final circuit implemented for the mixer. In this circuit both RF inputs are connected to the output of VCO. Since the output of VCO is 12 GHz, the output of the mixer has a 24 GHz signal. The LC-tank resonator (L_m and C_m) is provided as the load of the mixer to filter out-of-band signals (tones generated by mixer and the 12 GHz leakage tone) and provide a pure 24 GHz signal at the output of the mixer.

For the mixer the inductor value of 180 pH has been used. For this inductor the required value of capacitor is 49 fF which is realized with MIM capacitors. The transistor M_1 is at the RF input of the Mixer, as a result it should provide low input noise

based on power/noise trade-off. Transistor M_2 has been designed to provide good switching to reduce the noise of the mixer [50]. (Table 6)

Table 6: Device sizing for mixer in Fig.63

Transistor Number	Width (one finger)	Number of Fingers	Length
M_1	8 μm	4	.18 μm
M_2	8 μm	2	.18 μm
M_{bias}	8 μm	62	.2 μm
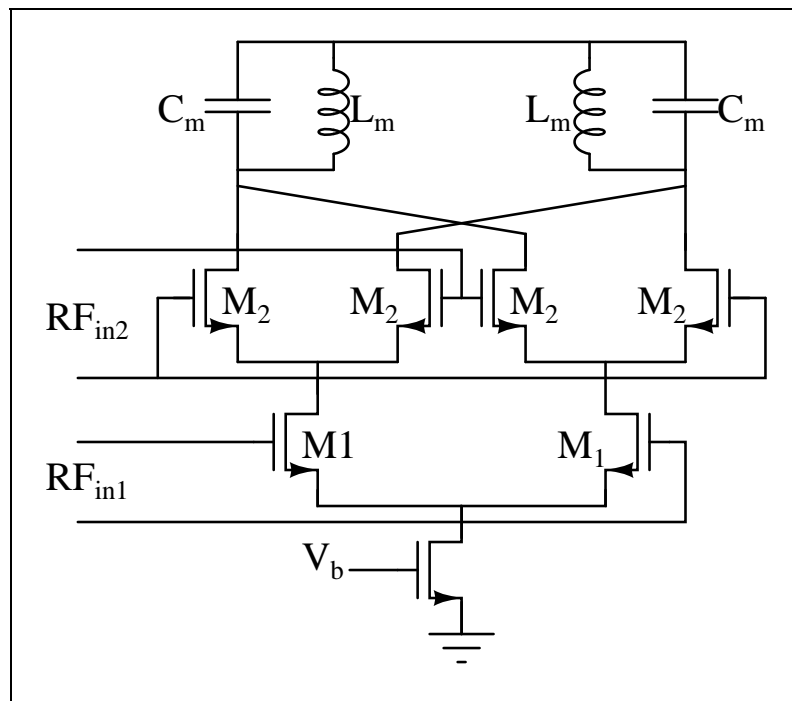
Figure 63: Double balance Gilbert cell mixer

6.3 – Output buffer

The final stage is an open drain differential buffer (fig.64). The output of the buffer will drive the input port of spectrum analyzer. Since the input impedance of the port is 50 Ω, the effective load of the buffer would be 50 Ω. M_1 has been designed to provide high gain at 24 GHz with a 50 Ω in the load while consuming around 1 mW. (Table 7)

Table 7: Device sizing for buffer in Fig.64

Transistor Number	Width (one finger)	Number of Fingers	Length
M_1	4 μm	5	.18 μm
M_{bias}	8 μm	64	.5 μm
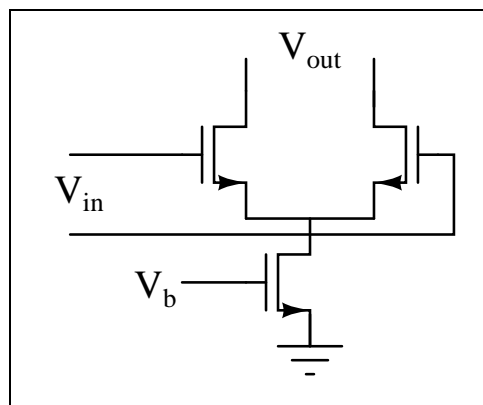
Figure 64: Output buffer

6.4 – LC-tank design

As mentioned before, the quality factor of the tank play an important role in the phase noise of the VCO. According to the TSMC manual, the Q of the MOS-capacitors (varactors) in the tank is around 20 and is fixed by process. As a result the Q of inductor should be increased in order to provide the highest possible quality factor for the LC-tank (Eq.43).

Equation 43

$$\frac{1}{Q_{\tan k}} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

The MOS capacitors have been realized using PMOS capacitors available in the process which is actually a PMOS transistor. One terminal is the Gate of the transistor and the other terminal is the Source, Drain and Bulk connected together. In order to reduce the parasitic capacitances to the ground, the gate terminal is connected to the drain of VCO transistor and the other terminal is connected to DC biasing voltage. (Fig.60)

The inductor for the VCO has been optimized using Sonnet full wave simulator [51]. Using the process variation data in the corners in the manual of the process, the value and quality factor of inductor has been simulated for typical (tt), fast (ff or ++) and slow (ss or --) corners.
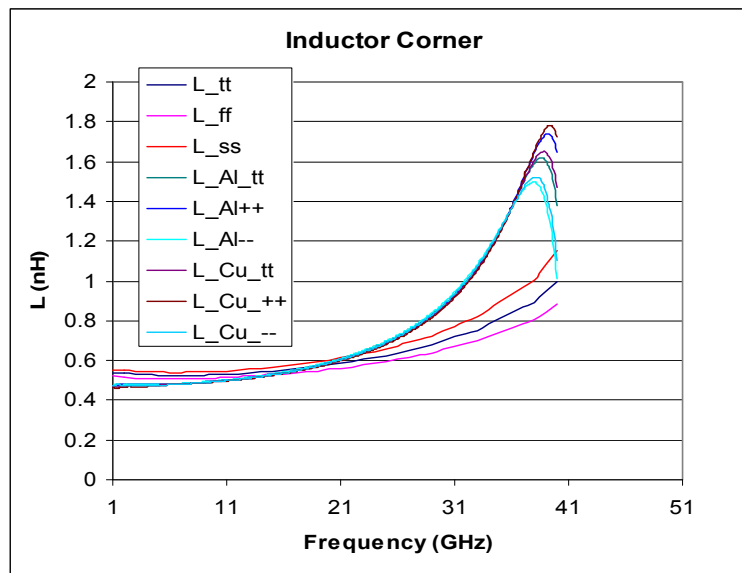
Figure 65: Simulation result of inductance versus frequency
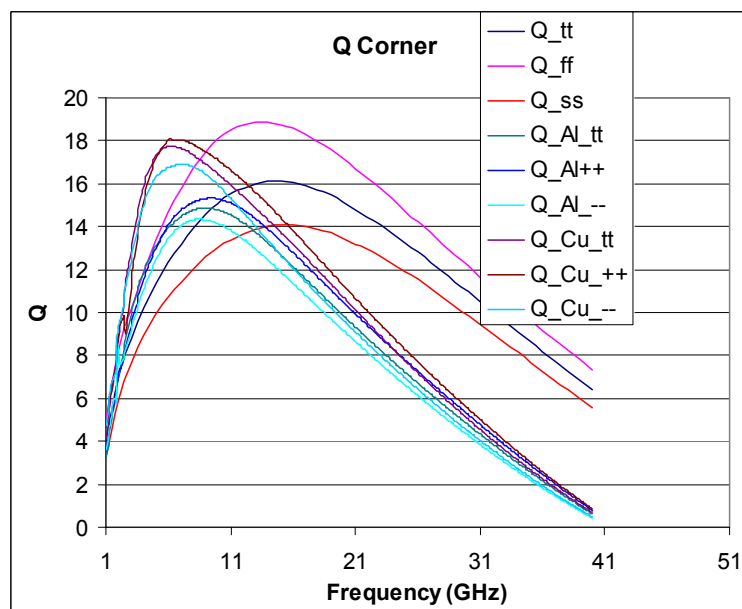
Figure 66: Simulation result of quality factor of inductors versus frequency

Also the inductor with Cu (M_1) or Al (M_2) ground plan for different corner has been simulated (Fig.65 and Fig.66). The simulation shows that for working at high frequencies, an inductor without ground plane underneath shows a better quality factor

than both available options of ground plan. The optimized inductor (without ground shielding) has been used for this circuit to improve the phase noise of the VCO.

6.5 – Final design

In order to provide independence DC biasing, VCO to mixer and mixer to buffer are connected with decoupling MIM capacitors.

This design has been implemented with 0.18 μm TSMC CMOS technology. The next section provides the simulation and measurement result of the VCO.

7. SIMULATION AND MEASUREMENT RESULT OF VCO

In the previous section, the design considerations for the VCO were discussed. In this section of the thesis, the VCO has been simulated and the simulation result has been compared to measurement.

7.1 – Simulation results

The time response of the 12 GHz VCO has been simulated using transient simulation using Cadence to show the settling time of the stand alone VCO. Fig.67 and Fig.68 show the simulation result of the transient simulation of the stand alone VCO for two tuning limits. For the output frequency of 13.49 GHz, the settling time is around 7 nS and the output frequency of 10.59 GHz, the settling time is around 11 nS. Therefore it is expected that the VCO to settles in the whole tuning range.

The phase noise has been simulated at the output of the 12 GHz VCO and the output of the mixer + buffer (Fig.69 and Fig.70). The simulation shows that at the output of 12 GHz VCO, the phase noise @1 MHz offset is around -106 dBc/Hz while the phase noise at the output of the buffer at the same offset frequency is around -102 dBc/Hz. This means the mixer degrades the phase noise by around 4 dB.

The output power of the buffer according to simulation is -8 dBm. Finally, the current consumption of the circuit is 11 mA @ 1.8 v supply (19.8 mW). The simulation result of the VCO is provided in Table 8.
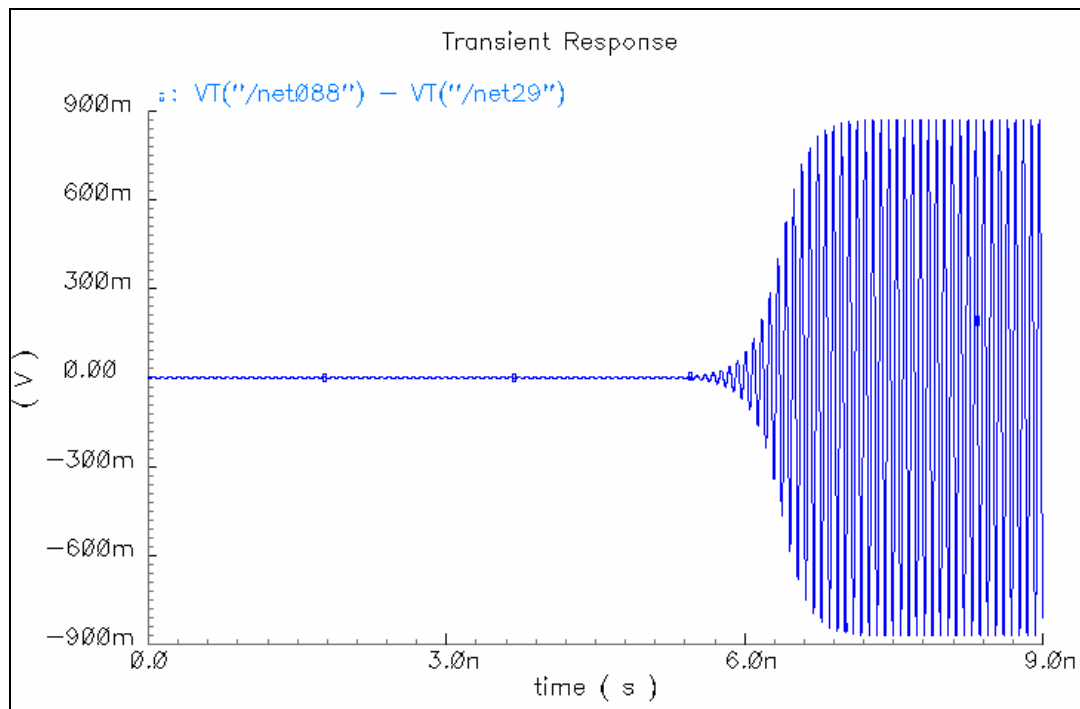
Figure 67: Transient analysis of stand-alone VCO (f$_0$ = 13. 49 GHz)
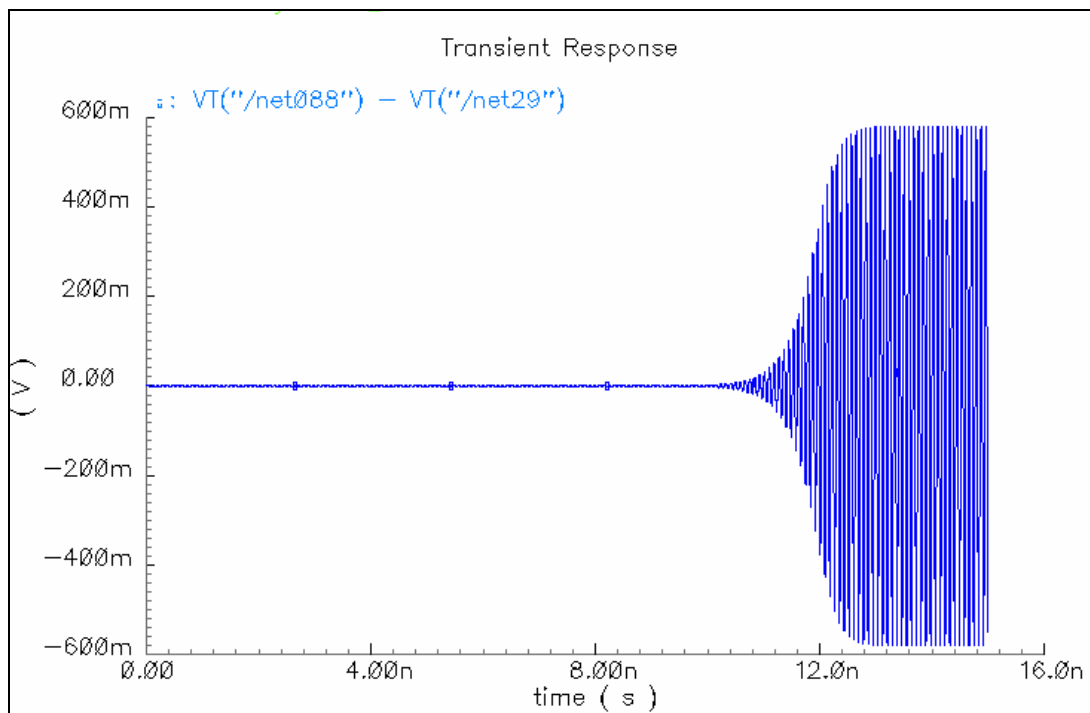
Figure 68: Transient analysis of stand-alone VCO (f$_0$ = 10.59 GHz)
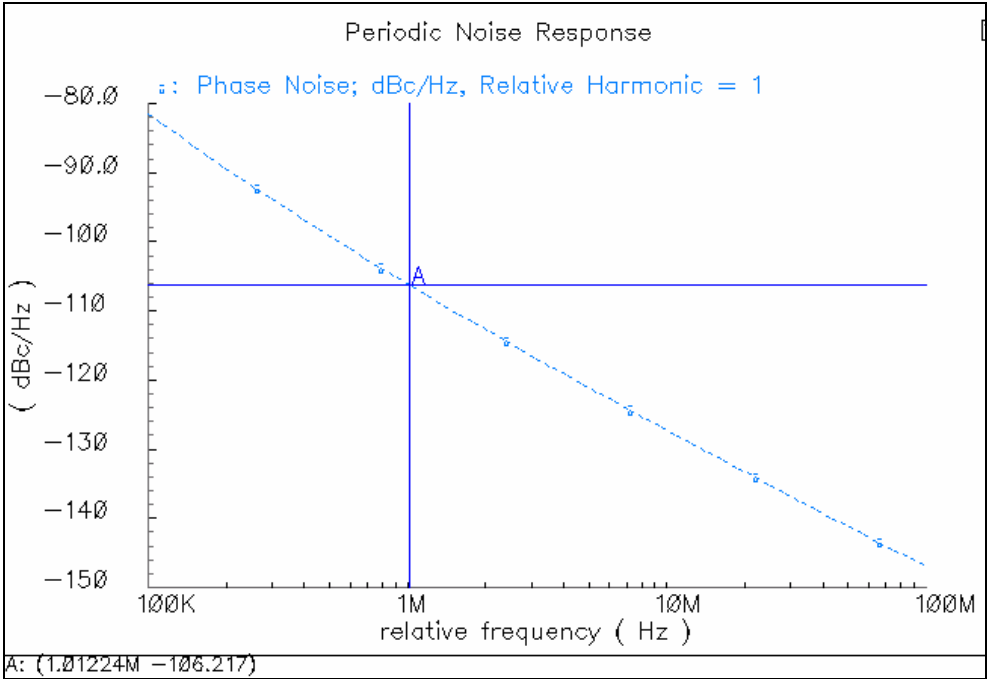
Figure 69: Simulated phase noise at the output of the 12 GHz VCO
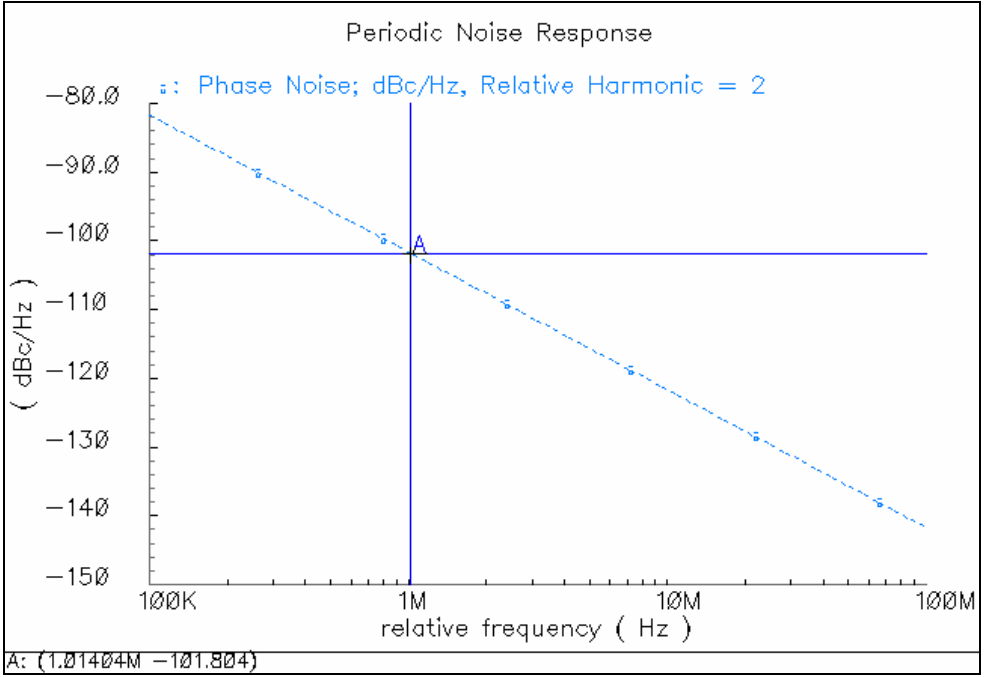
Figure 70: Simulated phase noise at the output of the buffer

Table 8: Simulation result of VCO

Parameter	12 GHz VCO	24 GHz VCO
Frequency (GHz)	12	24
Phase noise @1MHz offset (dBc/Hz)	-106	-102
Current Consumption (mA)	8	11

7.2 – Measurement

VCO has been fabricated with TSMC 0.18 μm CMOS technology (Fig.71).
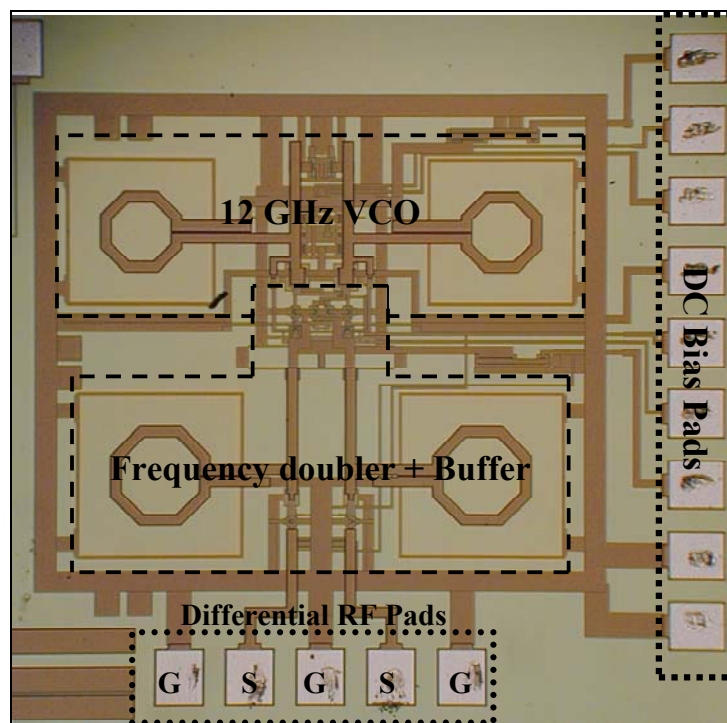
Figure 71: Fabricated VCO in TSMC 0.18 μm CMOS process

7.2.1 – Measurement setup

The measurements have been done using on-wafer technique. The DC bias has been provided by a DC probe. The output signal of the buffer is taken using GSGSG differential probe then each differential signal is passed through a Bias-Tee which provides the biasing for the differential open drain buffer. The outputs of Bias-Tees are fed to $0\text{-}180^0$ wideband coupler (6-26 GHz) with very low amplitude and phase imbalance which changes the differential signal to the single ended one to be able to send it to a single-ended 50 Ω spectrum analyzer. Finally the single ended output is measured with the "Agilent E4446A" spectrum analyzer. Since the maximum operating frequency of the cables used for this measurement is around 18 GHz, a high loss due to cables are expected to observe which needs to be calibrates out to find the real output power of the VCO.

7.2.2 – Measurement result

Fig.72 shows the output spectrum of the VCO. The output power is -31 dBm. The loss of the measurement setup is calculated to be around 19 dB, due to the lossy cables, hybrid coupler and Bias-Tees, the measured output power of the VCO is around -12 dBm.

The biasing circuit for this VCO has some leakage problems due to the poor layout; as a result the measured phase noise of the VCO (Fig.73) is lowered compared to the simulation result. The measurement shows the phase noise of around -94 dBm @ 1-MHz offset from the carrier.
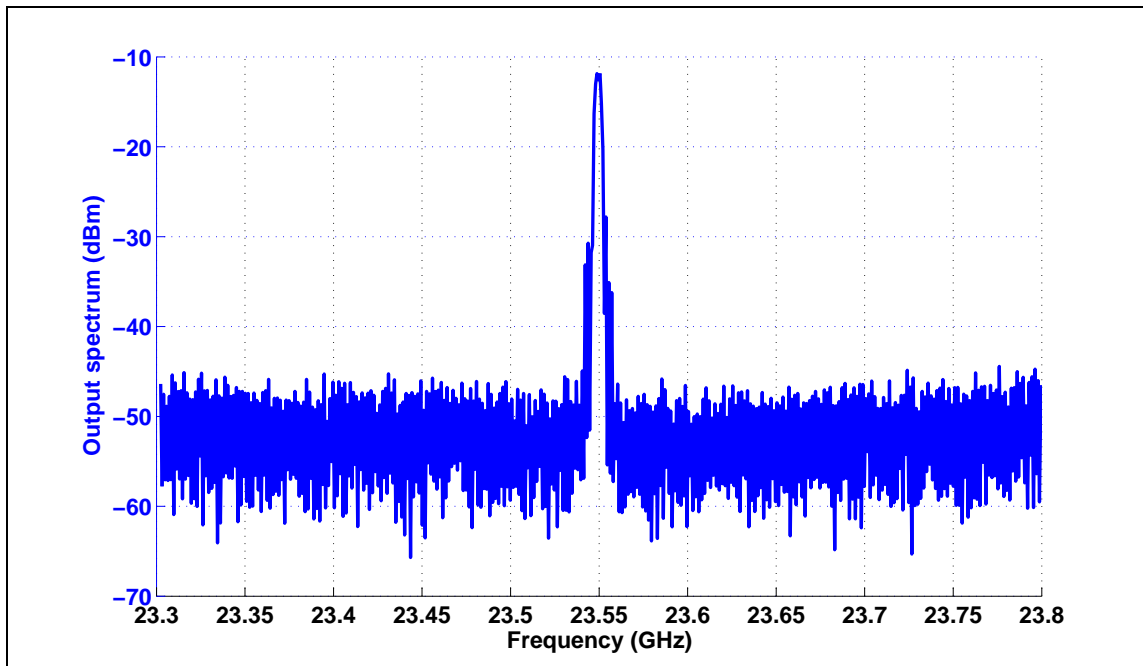
Figure 72: Output spectrum of the 24 GHz VCO
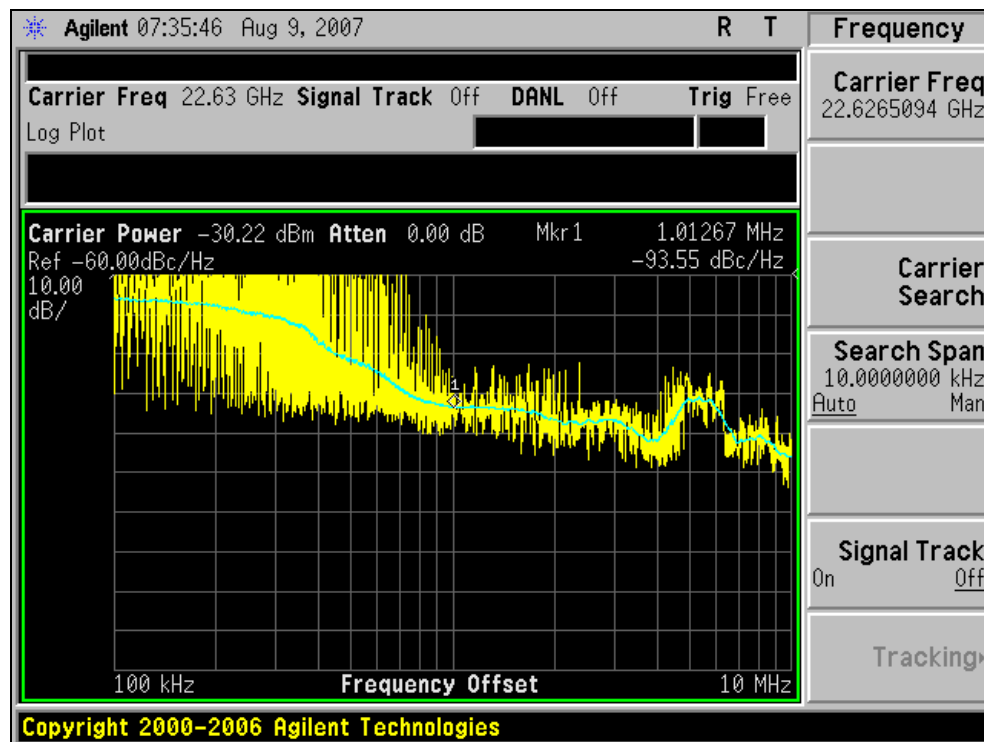
Figure 73: Phase noise of the 24 GHz VCO

The coarse tuning of the VCO provides four steps (00, 01, 10, and 11). The fine tuning of the VCO has been measured for all the coarse tuning modes by varying the tuning voltage in each mode and measuring the output frequency. This VCO provides tuning range from 21 GHz to 25.8 GHz (4.8 GHz tuning) which is equivalent to 20% tuning (Fig.74).
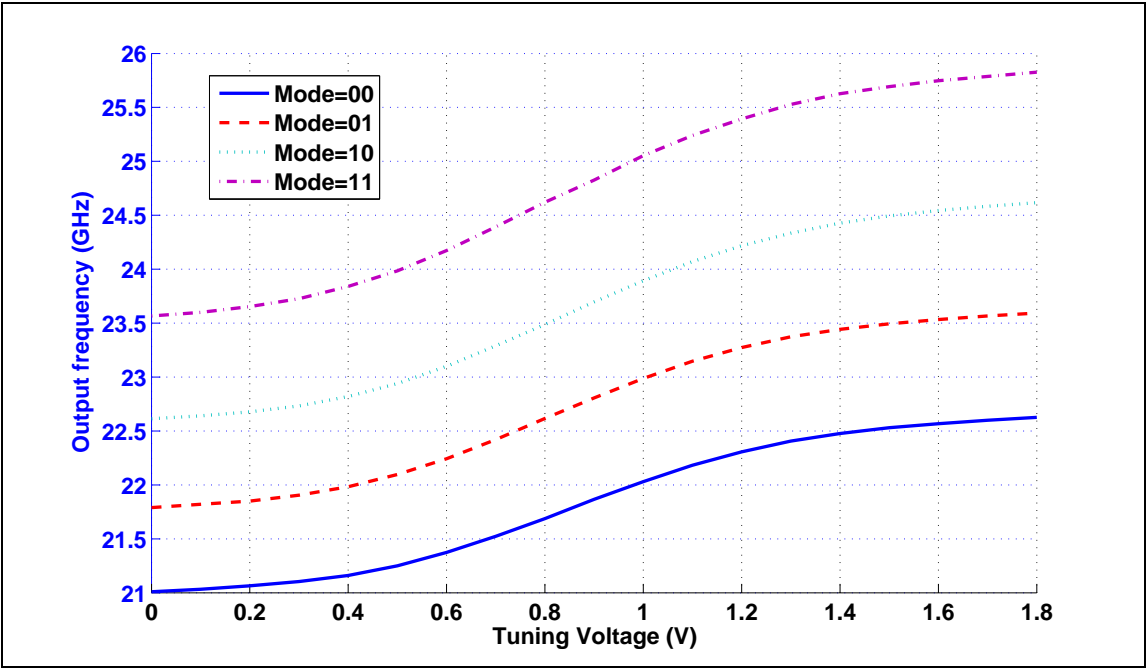
Figure 74: Tuning range of the VCO versus tuning voltage

Table 9: Measurement result of the 24 GHz VCO

Parameter	24 GHz VCO
Output power (dBm)	-12
Phase noise @1MHz offset (dBc/Hz)	-94
Current Consumption (mA)	10.94
Tuning range	21 – 25.8 GHz (%20)

Finally, the current consumption of the circuit is measured around 10.94mA @ 1.8 v supply (19.7 mW). From this current 9.14 mA is consumed by VCO + Mixer and 1.8mA is consumed by the buffer. Table 9 provides the measurement result of the VCO.

7.3 – Conclusion

A 12 GHz VCO and a doubler is implemented using TSMC 0.18μm CMOS process. The VCO and the doubler together provide the output frequency of 24 GHz. The resulted VCO would have a higher tunability compared to a stand-alone 24 GHz VCO which is another advantage over conventional VCO. This VCO provides less phase noise with less amount of current comparing to direct 24 GHz VCO. Using active mixer as a doubler provided higher output comparing to ones with passive mixer [50].

The phase noise of the VCO has been degraded due to noise effect coming from off-chip bias circuit with poor layout. The next step in this projects it to improve the off-chip biasing circuit and redo the measurements for the phase noise.

8. CONCLUSION

In the first four sections of this thesis, a fully integrated CMOS phase shifter has been designed for MIMO application at 4GHz. In the next three sections a fully integrated CMOS 4GHz integrated n the previous section, the design considerations for the VCO were discussed. In this section of the thesis, the VCO has been simulated and the simulation result has been compared to measurement.

In the first four sections an active phase shifter in 4 GHz has been designed using TSMC .18μm design kit. The integrated circuit performance has been simulated to support the idea. Finally, the active implementation has been compared with passive implementation in the receiver chain. The main advantages of active implementation over the passive implementation are:

o Very compact size

o Lower loss

o Lower overall noise figure in the receiver chain

But it suffers from high power consumption.

In the next three sections a 12 GHz VCO and a doubler is implemented using TSMC 0.18μm CMOS process. The VCO and the doubler together provide the output frequency of 24 GHz. The resulted VCO had a higher tunability compared to a stand-alone 24 GHz VCO which is another advantage over conventional VCO. This VCO provides less phase noise with less amount of current comparing to direct 24 GHz VCO.

Using active mixer as a doubler provided higher output comparing to ones with passive mixer.

The phase noise of the VCO has been degraded due to noise effect coming from off-chip bias circuit with poor layout. The next step in this projects it to improve the off-chip biasing circuit and redo the measurements for the phase noise.

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