Contributions to the efficiency and safety of stand-alone DC microgrids

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Abstract

Currently, the distributed generation based on renewable energy sources is mainly DC. Those DC systems are use diverse applications such as airplanes, automobiles, ships, spaceships, computers, servers, telecommunications stations, among others. This thesis considers an isolated DC microgrid architecture composed of a renewable source, an energy storage system, and a DC load. The thesis is aimed at identifying and solving efficiency and safety problems at the source, the DC bus, and the load. During the development of this Thesis six contributions to the state-of-the-art of DC microgrids were obtained. The first contribution is the mathematical model of a distributed maximum power point platform formed by multiple module-converter sets connected in series, which can be implemented in different programming languages and deployed on multiple platforms to evaluate optimization strategies. The second contribution is a vectorial MPPT algorithm for a distributed photovoltaic system, based in the perturb & observe algorithm. This algorithm provides a satisfactory trade-off between implementation cost and energy production since it uses a single I/V sensor. The third contribution is a reconfiguration algorithm that optimizes the electrical connections of a commercial photovoltaic array, which enables to maximize the energy extraction under arbitrary shading conditions. The fourth and fifth contributions are two control strategies, based on sliding-modes, designed for a charger/discharger DC/DC converter. Those solutions enable to regulate the voltage on the DC-bus of the microgrid to improve the microgrid safety. One of the strategies considers the current of the DC-bus into the sliding surface, which gives a better performance in terms of overshoot and settling time of the DC bus voltage. The final contribution concerns a control strategy, also based on sliding modes, to regulate a point-of-load DC/DC converter. Such a contribution enables to improve the conversion efficiency, and at the same time, to improve the load safety by reducing the current and voltage ripples delivered by the converter. Finally, those contributions improve the electrical efficiency and operational safety of DC microgrids based on renewable sources.
The results obtained in this thesis were published in five journals articles and three communications to conferences. From those, three articles were published in Q1 journals, one article was published in Q3 journal, and another one was published in a Colombian journal.

Keywords: DC-microgrid; sliding-mode; photovoltaic reconfigurator; distributed MPPT; vectorial MPPT; interleaving converter; POL; bus-DC regulation; bidirectional converter; charger/discharger; ripple; efficiency.

Contribuciones a la eficiencia y seguridad de operación en microrredes DC aisladas

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Resumen

Actualmente, la generación distribuida basada en fuentes de energía renovable es principalmente DC. Estos sistemas DC son utilizados en aviones, automóviles, barcos, naves espaciales, computadores, servidores, estaciones de telecomunicaciones, etc. Esta Tesis considera una arquitectura de microrred DC aislada compuesta por una fuente renovable, un sistema de almacenamiento de energía y una carga DC. La tesis tiene como objetivo identificar y solucionar problemas de eficiencia y seguridad de operación en la fuente, en el bus DC y en la carga. Durante el desarrollo de esta Tesis se obtuvieron seis aportes al estado del arte en microrredes DC. La primera contribución es el modelo matemático de una plataforma de seguimiento del punto de máxima potencia formada por múltiples conjuntos panel-convertidor conectados en serie, el cual se puede implementar en diferentes lenguajes de programación y desplegar en múltiples plataformas para evaluar estrategias de optimización. La segunda contribución es un algoritmo MPPT vectorial para un sistema fotovoltaico distribuido, basado en el algoritmo de perturbar y observar. Este algoritmo proporciona una compensación satisfactoria entre el costo de implementación y la producción de energía, ya que utiliza un solo sensor de I/V. La tercera contribución es un algoritmo de reconfiguración que optimiza las conexiones eléctrica de un arreglo de paneles fotovoltaicos comercial, el cual permite maximizar la extracción de energía bajo condiciones arbitrarias de sombreado. La cuarta y quinta contribución son dos estrategias de control, basadas en modos deslizantes, diseñadas para un convertidor DC/DC cargador/descargador. Estas soluciones permiten regular el voltaje del bus DC de la microrred para mejorar la seguridad de su operación. Una de las estrategias considera la corriente del bus DC en la superficie deslizante, lo cual da un mejor desempeño en cuanto al sobreimpulso y el tiempo de establecimiento del voltaje del bus DC. La contribución final es una estrategia de control, también basada en modos deslizantes, para regular un convertidor DC/DC point-of-load. Esta contribución permite mejorar la eficiencia de la conversión y al mismo tiempo mejorar la seguridad operativa de la carga reduciendo el rizado de voltaje y corriente entregado por el convertidor. Finalmente, estas contribuciones mejoran la eficiencia eléctrica y la seguridad operativa de microrredes DC basadas en fuentes de energía renovable.
Los resultados obtenidos en esta Tesis fueron publicados en cinco artículo de revista y tres ponencias en conferencias. De estos, tres artículos fueron publicados en revistas clasificadas en Q1, un artículo fue publicado en una revista con clasificación Q3 y otro en una revista colombiana.

Palabras clave: microrred DC; modos deslizantes; reconfiguradores fotovoltaicos; MPPT distribuido; MPPT vectorial; convertidores entrelazados; POL; regulación bus DC; convertidor bidireccional; cargador/descargador; rizado; eficiencia.

Preface

This thesis reports the results of my PhD studies at the Departamento de Ingeniería Eléctrica, Electrónica y Computación, Facultad de Ingeniería y Arquitectura, Universidad Nacional de Colombia. This work was carried out between Semester 2012-2 to Semester 2018-1, and it was supported by the Instituto Tecnológico Metropolitano. The developing of this thesis was supported by several research projects:

- Diseño, análisis y evaluación de estrategias de control para optimización de sistemas de generación basados en paneles fotovoltaicos (ITM code P10-102): Instituto Tecnológico Metropolitano and Universidad Nacional de Colombia.

- Maximización de extracción de energía en aerogeneradores para cogeneración urbana en el Valle de Aburrá (ITM code P10233): Instituto Tecnológico Metropolitano and Universidad Nacional de Colombia.

- Caracterización de convertidores conmutados DC/DC para aplicaciones industriales (ITM code P14215): Instituto Tecnológico Metropolitano and Universidad Nacional de Colombia.

- Desarrollo de un algoritmo MPPT con único sensor voltaje/corriente para maximización de potencia en la carga de sistemas fotovoltaico (ITM code P14220): Instituto Tecnológico Metropolitano and Universidad Nacional de Colombia.

- Diseño y control de microrredes basadas en fuentes renovables para el suministro de energía eléctrica a bajo costo en zonas no interconectadas de Colombia (Colciencias code 1118-669-46197): Universidad Nacional de Colombia, Universidad del Valle, Universidad Industrial de Santander and Instituto Tecnológico Metropolitano.

The results of this thesis were published in five articles and three conference papers (see appendix A). Four articles were published in international journals and another in a colombian journal. Two papers were published in international conferences and another in a colombian conference. This document was built thinking in making it easier for the reader to understand the overall work and to identify the improvements in the state of the art. Moreover, the eight publications significantly improve the diffusion of the thesis results.
The thesis follows common publishing guidelines given by international journals. Grayscale figures have been used to illustrate the simulation results. Color figures have been used only when strictly necessary, such as is the case of simultaneous plots of a high number of signals. Similarly, the bibliographical citations have been numbered in order of appearance, as have the equations, figures and tables. Both roman and italic fonts appear in the text, the latter being used to highlight important issues, differentiate nouns and mark non-English words.

Two experimental processes were developed in this thesis, one at the Universitat Rovira i Virgili - Spain, and another at Instituto Tecnológico Metropolitano - Medellín. In this last Institution also was developed the Hardware-In-the-Loop simulations. Likewise, simulations of the systems and power electronics circuits have been carried out by using Matlab/Simulink® and PSIM® software.
Finally, I want to thank the huge support of my Director, Professor Carlos Andrés Ramos Paja, who with his clarity on the topic was the best leader that I could have in the development of this thesis. Truly, I am very grateful to him.
Likewise, I want to thank to all the people who, in one way or another, helped me in this thesis, especially to Professor Daniel González and Master student Juan Pablo Villegas Ceballos.
This work was supported by the Universidad Nacional de Colombia and the Instituto Tecnológico Metropolitano under the project UNAL-ITM-39823/P17211.

Contents

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1. Introduction

The growth of the world economy has also increased the demand for electric power, which has led to the decrease of fossil fuel reserves and to increase CO_2 emissions. This situation has been addressed by governments, research centers, industry and energy supply companies by using renewable sources [1, 2, 3, 4, 5, 6, 7, 8]. However, the introduction of renewable energy sources presents major challenges in political, social and technology sectors. The political sector is mainly affected by the electricity prices and regulation of the electrical companies [9, 10, 11]. At the societal level, the renewable sources decrease the greenhouse gas emissions, improve the distribution system by increasing the population coverage, and provide service for both off-grid areas and stand-alone applications [10, 12, 13]. The technological level presents many challenges: on one hand, it is required to improve the conversion device, namely, more efficient and reliable the photovoltaic (PV) panels or fuel cells [14, 15, 16, 17]; on the other hand, it is required to improve the strategies for maximizing the energy production [18, 19, 20], improve the power quality [21, 22, 23] and fulfill some non-functional requirements such as reliability, scalability, size, cost, etc. [24, 25, 26, 27].

One of the economic sectors with bigger growth is the mobile telecommunication. Due to competition in the market, telecommunication companies need to provide better and cheaper services to the customers. That requires to install base stations in zones that have not access to electrical power infrastructure. Therefore, the typical solution to provide electric power to those systems is based on diesel power. However, due to the high costs and pollution produced by such a solution, recently the telecommunication companies have focused on renewable energies as the main power source for the base stations.

A common structure used for power systems based on renewable generators is presented in Figure **1-1**, which is based on a PV array, an energy storage device (ESD) and DC-loads. This stand-alone power system has been extensively used in energy supply systems for telecommunication equipment [28, 29, 30]; but also in other applications such as electric vehicles [25, 31, 32, 33, 34, 35, 36], irrigation systems [37, 38], heating systems [39], among others. The system considers an unidirectional DC/DC converter, whose purpose is to operate the renewable generator in its optimal conditions, according to an optimization strategy devoted to performing a maximum power point tracking (MPPT). In addition, a charger/discharger power converter interfaces the ESD with the DC-bus. Such a charger/discharger controls the power exchanged between the ESD and the DC-bus, and at the same time, it is in charge of regulating the DC-bus voltage. The main advantages of this topology are: the capability of storing the energy-in-excess produced by the generator; the capability of releasing the stored

energy when it is needed; and the impedance decoupling between the renewable source and the other elements, which enable to optimize the source operation. Finally, a unidirectional DC/DC power converter is connected to the DC-load, which is aimed at increasing the efficiency, and to ensure the DC power quality required by most modern loads such as data centers, computer equipment, modern televisions, standard home appliances, DC lighting systems, and telecommunication power systems.
In the remain of this Chapter, the issues of extracting the maximum power of the renewable source, the DC-bus voltage regulation, power flow control between the ESD and the DC-bus, and the regulation of the energy delivery to the DC-load with highly efficient and quality, are described.

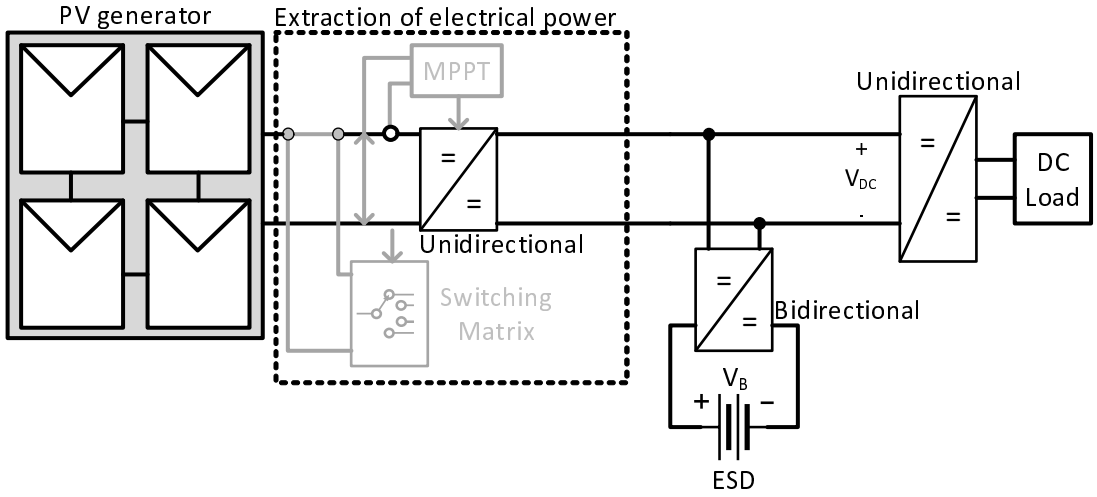


Figure 1-1.: Stand-alone power system based on renewable energy sources.

1.1. Power extraction of the PV generator

The PV generator of Figure **1-1** is formed, in general, by PV panels driven by a power converter connected to a DC-bus. Moreover, the PV panels are connected in a series-parallel (SP) configuration [40, 41, 42], which enables to reach the large DC voltage (or current) required by the power converter. A challenge in this type of PV arrays is to obtain the maximum power under any operating condition. Therefore, Chapter 2 proposes a solution to improve the power generation of the PV array in SP configuration. Despite the existence of other array configurations, such as total cross-tied (TCT), bridge-linked (BL) or honey-comb (HC) [43], the SP configuration is the most widely adopted due to its simplicity and reduced number of connections [44]. Hence, the SP configuration is considered to develop this Thesis. In uniform conditions, i.e. all the PV panels exhibiting the same parameters, temperature and solar irradiance, the electrical characteristics of the PV array are proportional to the

ones of any panel, just scaled in voltage by the number of panels in series and scaled in current by the number of strings in parallel. Thus, there exists a single optimal operating condition despite the connection between the PV panels [45, 46, 47]. However, if some (or all) PV panels exhibit different parameters, e.g. due to different irradiance caused by shades, as it is observed in Figure **1-2**, the PV array produces a different maximum power depending on the electrical connections between the panels. Moreover, in those mismatched conditions, the PV array exhibits multiple maximum power points (MPP) instead of a single one, as in uniform conditions [48, 49, 50]. Mismatched conditions commonly occur in PV installations due to shades generated by objects adjacent to the array, e.g. trees, buildings, posts, other PV arrays, etc. Furthermore, since the Sun moves along the day, a PV panel can be fully irradiated, partially shaded or completely shaded depending on the hour of the day.

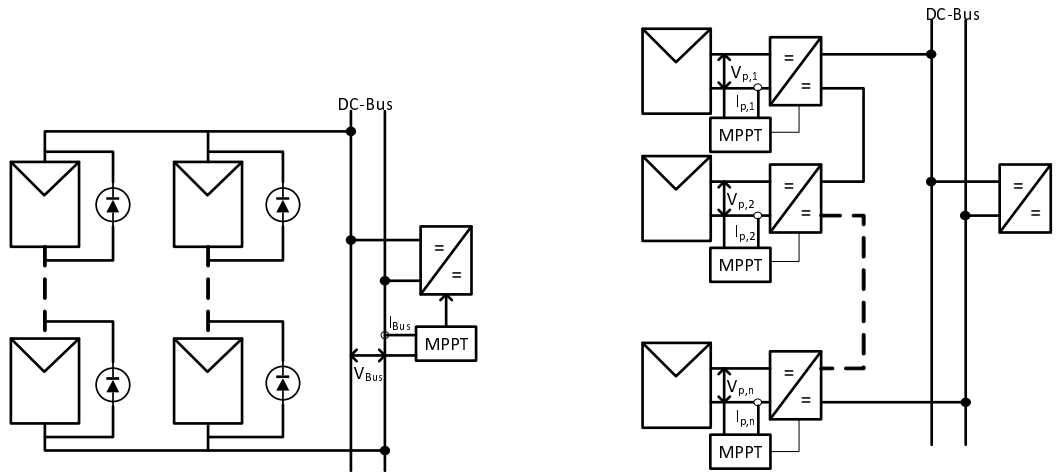
Figure 1-2.: Shading profiles affecting PV systems.

The effect of the shades must be carefully analyzed, otherwise, the power production of the PV array might be overestimated, leading to a subsequent non-viability of the system due to low profitability [51]. Hence, the effect of shading conditions should be reduced to increase the profitability and viability of a PV array subjected to those conditions, e.g. urban PV systems.

Under shading conditions, the current of an unprotected array is the lowest available PV current; as a result, the most productive PV modules suffer from an internal power dissipation as heat, which has a negative impact on the module lifetime. The traditional solution is to connect bypass diodes in anti-parallel to each PV module in the array. Those diodes short-circuit the PV module with lowest current production, thus protecting the whole array [52]. This solution generates multiple local maximum in the power-voltage curve of the array, which may confuse the power maximization algorithms that would lead those to be trapped in a local maximum, hence operating with non-optimal power production.

There exist some methods to improve the power extraction from PV arrays under shading conditions. One solution is to adjust the operating point on the I-V curve of the PV array, which is conducted with optimization algorithms that modify the input impedance of the DC/DC converter to maximize the power delivered to the load. Traditionally, a single algorithm that maximizes the power of the whole PV array is used to track the MPP; this scheme is known as a centralized system [53], e.g. Figure **1-3**a. Nevertheless, an dedicated MPPT algorithm and converter can be used for each PV module, as it is illustrated in Figure

1-3b; this begin called a distributed MPPT system or DMPPT [54, 55, 56].



(a) PV array with a centralized MPPT. (b) PV array with Distributed MPPT.

Figure 1-3.: Centralized and distributed control of a photovoltaic system.

Each solution presents advantages and disadvantages. The main benefit of the centralized method is the use of one MPPT controller and a single power converter (DC/DC or inverter), which reduces costs compared with the DMPPT [55]. However, the power converter used in the centralized system requires higher design complexity due to its multiple functions: boosting or reducing the voltage of the PV modules to the level required by the application, and performing the actions commanded by the MPPT algorithm [57].
Moreover, the centralized control architecture also introduces a disadvantage regarding implementation cost and complexity compared to typical MPPT algorithms. However, if such a high complexity always ensures the operation of the system at the maximum power point, then it might be acceptable. On the other hand, it is necessary to consider that a complex algorithm might not be viable due to processing hardware limitations [58, 59].
In contrast, the DMPPT solution guarantees the operation of each PV module at the corresponding MPP (maximum power point), therefore, it extracts the maximum available power from the array [60]. Nevertheless, this solution requires an elevated number of DC/DC converters (one per PV module), as well as a considerable amount of MPPT controllers and V/I sensors (one per each DC/DC converter) [61]. This characteristic introduces a high cost due to the large number of power conversion elements, sensors and processing platforms, as well as the complexity of the design, and the associated installation procedure. In any case, with the development of new technologies for data processing (DSPs, microcontrollers, FPGAs, processors, etc.) and multi-variable MPPT (MV-MPPT) algorithms, e.g. the one reported in Figure **1-4** [54, 62, 63, 64], some of the problems of this type of systems can be mitigated, thus finding a satisfactory balance between installation cost and power production.
Following the previous reasoning, the MV-MPPT algorithm depicted in Figure **1-4** aims to

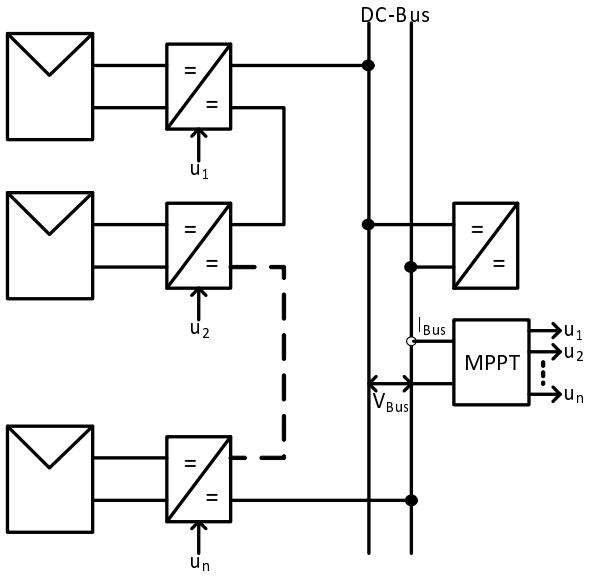


Figure 1-4.: PV array with multi-variable MPPT.

reduce both the hardware and system costs by using only one V/I sensor pair and a single processing device. To evaluate those type of algorithms it is necessary to have a general mathematical model for DMPPT systems, it including the electrical equations for each PV module and the dynamics imposed by the associated converters. Therefore, Section 2.1 introduces a model for DMPPT systems, while Section 2.2 proposes a MV-MPPT algorithm aimed at reducing the hardware requirements. Those are the first and second contributions of this Thesis.

Another approach to increase the power extraction of PV arrays is the adoption of switching matrices. Those devices change dynamically the electrical connections between the PV panels, which enable to reduce the adverse effects of operating under mismatching conditions [65, 66]. A large amount of solutions to this problem use analytical models to evaluate the best set of connections for a given shading profile [67, 68, 69, 70]. Nevertheless, such a solution requires full-size computers at high cost, which decreases the profitability in commercial applications.

Instead, Section 2.3 proposes a new solution for determining the best configuration of a PV array, connected in a series-parallel (SP) structure, without using complex mathematical models. Such a procedure uses the experimental voltage/current curves of the PV panels to construct the power/voltage curves of all of the possible configurations to identify the optimal one. The main advantage of this method is the low computational effort required to reconstruct the power/voltage curves of the array. This characteristic enables one to implement the reconfiguration solutions using inexpensive embedded devices, like FPGAs or DSPs, which are widely adopted in industrial applications.

1.2. DC bus regulation and storage management system

The use of renewable energy sources, or any other non-reversible source with limited bandwidth, requires the use of an additional Energy Storage Device (ESD) to store and release energy depending on the generator and load profiles: for example, slow sources (e.g., fuel cells) require ESD to support fast load transients [17]; non-predictable sources (e.g., photovoltaic panels) require ESD to support stand-alone loads during low irradiance conditions or during the nights [8].

In such a context, and due to the accelerated growth of the market for energy storage systems [71], this Thesis proposes a solution for the management of an energy storage system based on batteries. The solution considers both the bidirectional control of the energy flow to/from the battery and the voltage regulation of the DC-bus.

The common structure, based on renewable generators and ESD, used to supply electric power to the stand-alone telecommunications systems was already presented in Figure **1-1**. That system considers a charger/discharger power converter to interface the ESD with the DC-bus. Such a charger/discharger controls the power exchanged between the ESD and the DC-bus, and at the same time, it is in charge of regulating the DC-bus voltage.

Multiple solutions based on the topology presented in Figure **1-1** have been reported in the literature. For example, the work reported in [72] presents a power system based on a fuel cell and an ESD (supercapacitor and battery). That solution adopts a sliding-mode controller to regulate a bidirectional Buck-Boost converter with the aim of imposing the DC-bus voltage and the supercapacitor current. Moreover, the system includes a Boost converter to regulate the fuel cell, which is controlled by a PI structure to deliver a constant power flow without power peaks. However, this system does not include an optimization algorithm to improve the fuel cell operation, hence a fraction of the stored hydrogen could be wasted. Furthermore, the adopted sliding surface does not include the integration of the DC-bus voltage error, therefore it is difficult to guarantee a null steady-state error.

Similar topologies have been used in automotive engine/battery hybrid power systems. An example is presented in [73], which is based on a bidirectional DC/DC converter controlled with a variable current limiter. Similarly, the work presented in [74] proposes a three-level bidirectional converter for fuel-cell/battery hybrid power systems. In this case, the converter operates in both Buck and Boost modes controlled by a cascade of a voltage regulator and a current limiter.

In this kind of systems, one of the main challenges is to properly regulate the bidirectional power converter (charger/discharger) associated with the ESD, namely, the controller must operate with both positive and negative power flows with minimum disturbances, even at zero power. However, the non-linear system model changes with the direction of the current, but the DC-bus voltage must be regulated in the three conditions with minimum disturbances. Linear controllers (PI, PID or lead-lag) can be designed to mitigate such perturbations [75]. However, the main problems associated with these kinds of controllers are the reduction of

the closed-loop bandwidth, and the requirement to use a linearized model of the system that makes impossible to ensure the same performance, or even global stability, in all the operating conditions [76, 77, 78]. Therefore, other control techniques, mainly non-linear, are required to ensure stability in any operation condition, which is mandatory for a safe load operation. For example, sliding-mode control (SMC) has been widely investigated and has demonstrated to be a suitable solution for power converter regulation [79, 80, 81].

SMC requires the definition of a sliding surface with a desired equilibrium point, and towards to which the system must to converge: the objective is to force the system to operate within the surface at any given time [79, 82]. Most control systems based on sliding-mode include into the sliding surface the error between reference and one, or multiple, system states [83, 84, 85, 22, 86].

In the charger/discharger context, a solution based on SMC was reported in [83], in which it is proposed a cascade control of a DC/DC converter with a half-bridge bidirectional topology. In this case, the current control is designed with a fixed-frequency SMC to reduce electromagnetic interferences (EMI). In [85], a cascade control for a battery charger of an electric vehicle was proposed, but in this case, the converter is a unidirectional implementation. In that work, the inner inductor current control is designed with a discrete-time SMC, while the outer control loop calculates the current reference such that a power factor correction (PFC) stage regulates the DC-link voltage, and simultaneously, the current reference of a buck-type cells is determined depending on the state of charge (SOC) of the battery.

Similarly, the work reported in [86] is based on SMC and it is aimed at controlling a buck-boost charger/discharger converter with a cascade structure: an outer voltage loop based on a PI structure defines the reference of an inner current loop based on an SMC, in which the sliding surface is formed by the inductor current error. This solution is oriented to electric vehicles applications.

Other sliding-mode controllers adopt more complex sliding surfaces, e.g., the works reported in [87, 88], which will be reviewed in Chapter 3. Also, the work reported in [89] considers a sliding surface based on the output power error, hence it is a non-linear surface. This approach was used to provide constant power to the load and, at the same time, to reduce instability due to the negative impedance of the power converter. Similarly, the controller reported in [90] propose a sliding surface formed by the output voltage error and both the time integral and the derivative of that error, this to stabilize a Buck converter with constant power load. Since such a surface can be written as a second-order differential equation, the mathematical analyses required to guarantee stability are extensive despite the relative simplicity of the system model. Another SMC for controlling a bidirectional DC/DC converter, used to interface a parallel-connected hybrid energy storage system with a DC-bus, was proposed in [91]. That system is formed by a vanadium redox battery, a supercapacitor and a renewable power source. Moreover, in that work, the sliding-surface is similar to the one introduced in Chapter 3 of this Thesis, but without any adaptability to compensate for the duty cycle variation. Another complex surface is presented in [92], which is based on the

output voltage error and the square of the output capacitor current in a Buck converter. This surface is intended to improve the settling time and steady-state error of the output voltage regulation.
Chapter 3 of this Thesis proposes an adaptive sliding-mode controller for the ESD charger/discharger to regulate the load voltage in any power flow condition. The solution considers the topology presented in Figure **1-1** with a controller designed to fulfill both steady-state and dynamic performance criteria, which are defined in terms of the safe margins required for the correct load operation. This is the third contribution of the Thesis.

1.3. Efficient delivery of quality electric power to the load

The power quality must be a design criterion for any efficient and reliable micro-grid. Considering only DC micro-grids, low-quality power produces high losses due to undesirable oscillations on current and voltage signals [22]. Those losses also increase the cost of the energy, hence of the micro-grid. At the same time, the voltage and current oscillations also affect the reliability of the power converters.
The power supplies designed for telecommunication systems must provide sharp requirements: low voltage, high current, and low ripple at the load terminals. Such conditions are imposed to ensure a high performance of the processing devices of those types of equipment, namely, microprocessors, DSP, ASIC, or memory devices [93]. Likewise, the efficiency also can be increased guaranteeing DC-electrical-power-quality [94]. This issue is addressed in Chapter 4 of the Thesis, which proposes an active post-filter for a Buck converter aimed at reduce the ripple at the load terminals.
The fundamental elements that must be taken into account to ensure DC power quality are the inrush currents, fault currents, grounding and harmonic currents [94].
Inrush currents are associated to the turn-on of some equipment, mainly transformers and induction motors, which are AC loads. However, transients in the sources and loads of a micro-grid could introduce these inrush currents on the DC-bus as the one depicted in Figure **1-5**. Typically, this issue is faced with EMI filters placed between the DC-bus and ground, also by using an inrush current limiter (Surge Limiter), which is a special type of negative temperature coefficient (NTC) thermistor.
AC inrush current limiters are not the topic of this Thesis. However, they are widely known and there exist many works on this topic [95, 96, 97, 98, 99, 100, 101, 102, 103].
In the case of DC systems, the difference between the start output voltage and the regulated output voltage creates a high current demand. This, in turn, produces a large inrush current through the inductor of a DC/DC converter. The inrush current is a serious concern, since it can exceed the current derivative limitations of the source. To eliminate this undesired condition, some soft-start methods for DC/DC converters have been proposed [104, 105, 106, 107, 108, 109, 110]. Soft-start ensures that the maximum acceptable current is reached slowly, and not at once.

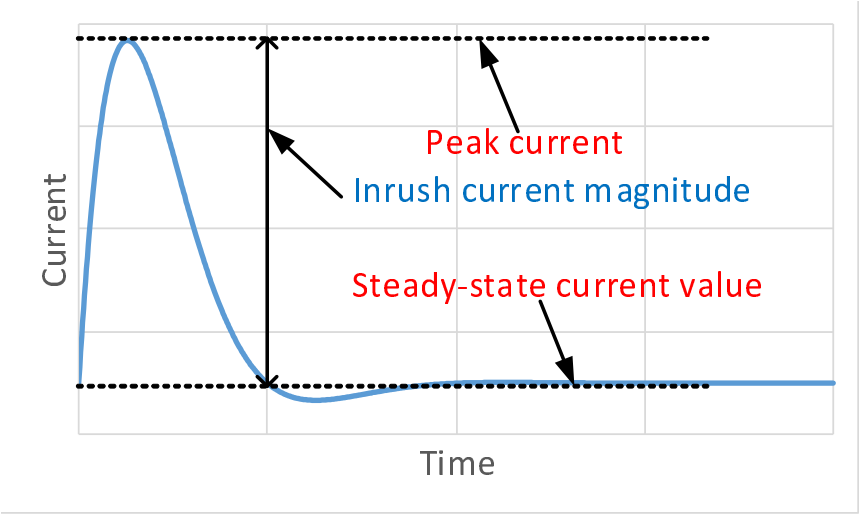


Figure 1-5.: Current waveform when the device is powered up.

In DC-systems, the fault current can be produced by a load, through a power converter, by a source or by the capacitance forming the DC bus. In any case, the fault current is limited by the power ratings of the converter, the source limitations or the charge stored in the distributed capacitance forming the DC-bus. Figure **1-6** shows both peak current and voltage droop of a Buck converter after a ground fault occurs, depicting also the subsequent activation of the protection. Those currents are generally detected by overcurrent relays. However, at higher voltage levels, the interruption of direct current by mechanical separation is an open research topic [111, 112].

On the other hand, an appropriate grounding configuration for a DC distribution system is very important for the power quality and safety of the system. The type of grounding used, e.g. TN-S, TT or IT grounding [113], determines the path of current for a ground fault, which impacts the level of fault current.

Finally, by definition, the DC-systems do not experience harmonic currents and voltages, since their fundamental frequency is $0Hz$. However, the presence of current and voltage oscillations generated by power converters, make possible to extend the harmonic term to a DC-system. Such DC-systems have converters at the Point-Of-Load (POL), at the source, at the storage device, and at the connection point with the AC-grid. Those converters non-linear effects create oscillations on the currents and voltages, which can produce damaging resonance currents and unacceptable EMI on equipment near the transmission lines, as well as overloading and physical damaging the transmission system itself [114, 115].

Considering that in telecommunication systems the loads operate at low voltage and high current, Buck converters are widely adopted for those applications. However, the quality of both current and voltage signals generated by a Buck converter is affected by the variations of the load, the source, or the parameters tolerance, which change the ripple magnitudes, among other problems [116, 117, 118].

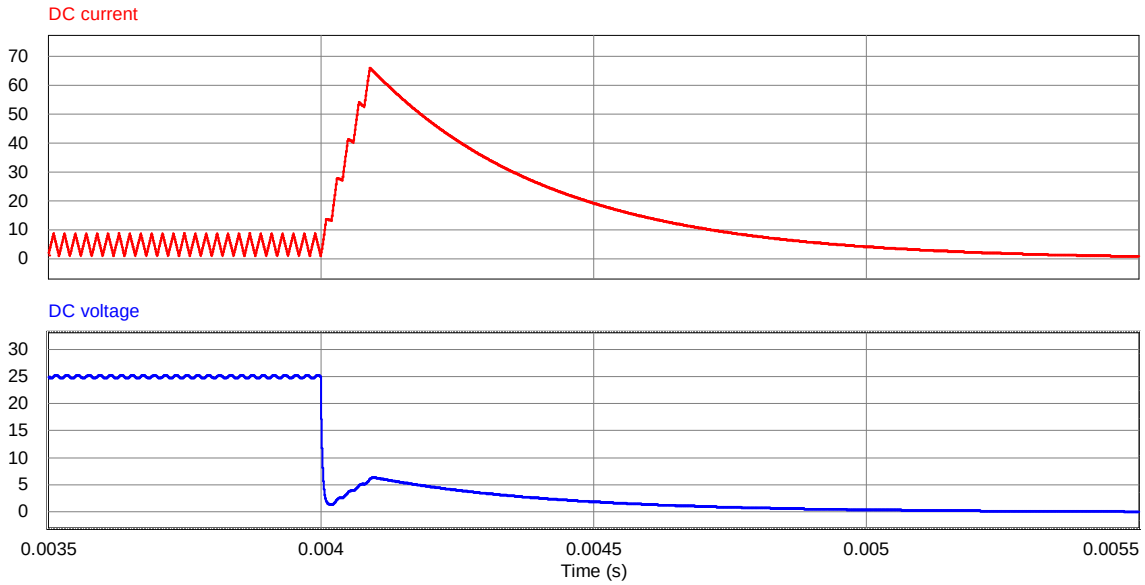


Figure 1-6.: Current and voltage characteristics during a DC short-circuit fault.

Several solutions have been proposed in the literature to improve the quality of the current and voltage generated by a Buck-based POL regulators. In [119], the ripple of a POL converter is reduced by means of a L-C output filter with two stages, which is classically regulated using a controller with two feedback points: the first point sensing the capacitor voltage of the first L-C stage and the second point sensing the capacitor voltage of the second L-C stage, that is, the load voltage. In such a solution, the authors demonstrate that a controller with a single feedback point could be used to stabilize the POL converter, but it requires adjusting one L-C filter to cancel out the zeros of the other L-C filter. In any case, the ripple magnitudes depend on the load impedance, which could change depending on the application conditions.

In [120] the performance of Buck-based POL with different current controllers is analyzed, taking into account the bandwidth of the voltage loop and the changes in the input voltage. But such a solution does not analyze the ripple behavior with load variations.

A different approach was presented in [121], where a digital controller is used to reduce the load current ripple in a non-isolated POL converter. Such a solution is based on peak current and average current controllers implemented in an FPGA. This controller scheme requires an Analog-to-Digital (A/D) converter, which increases the system cost in comparison with analog implementations. In the same way, [122] proposes a self-oscillating digital modulator to change instantaneously the duty cycle of the PWM signal driving the converter switch. Thus, it is possible to achieve the sampling frequency of the output voltage required in the control loop, which is higher than the switching frequency of the power converter. In this way, a short time response is achieved in the compensation of load variations. However, such

a solution does not introduce current or voltage ripples analyses.
In [123], a method to design the output filter of a low-voltage/high-current synchronous Buck converter, using performance boundary curves, is proposed. Such curves constrain the regions in the space of parameters to ensure an acceptable output voltage ripple. But, similar to the previous solutions, the load and source changes affecting the ripple magnitudes are not analyzed.
The previous solutions address the current and voltage ripple requirements by means of passive filters, which are impossible to be modified during operation time. Hence, those solutions are sensible to changes in the load impedance, source voltage, and tolerances of the electronic component parameters. Therefore, Chapter 4 of this Thesis proposes a POL solution based on a synchronous Buck converter operating in cascade with an active post-filter, which provides an almost ripple-free current to the load. The post-filter is formed by two parallel-connected Buck converters operating in complementary interleaving [124], and it is regulated using a sliding-mode controller to ensure its correct operation. The proposed POL compensates changes in the load impedance, source voltage, and electronic component parameters. Moreover, the proposed solution improves the electrical efficiency of the classical Buck-based POL. This correspond to the fourth contribution of the Thesis.
In conclusion, this Thesis will face three issues identified above for the architecture reported in Figure **1-1**. First, the improvement of generated power by the PV array (Chapter 2); second, the DC-bus regulation by controlling the storage management system (Chapter 3); finally, efficient power delivery to the load with high-quality electric power (Chapter 4). Those solutions introduce four state-of-art contributions, which have been reported in five (5) Journal papers: three Q1 (Scopus) papers and one Q3 (Scopus) paper. Those papers are also indexed by Publindex as three A1 papers and two A2 papers.

2. Improvements in the power extraction of photovoltaic source

This Chapter proposes two solutions to increase the power production of a PV array operating under mismatched conditions. The first solution is a distributed MPPT algorithm, while the second solution is a PV reconfigurator.

Design and simulation of distributed MPPT techniques require a model of the photovoltaic generation system. Therefore, this Chapter proposes a model considering the connection of a module-converter set in series with other sets, which can be sized depending on the particular application. The model is described by a series of equations that can be implemented on any mathematical software or programming language to solve them. Those equations include the static behavior of the photovoltaic module described in terms of the voltage-current relation. In addition, the model takes into account the dynamics of the boost converter, including losses in the inductor, to approximate the model behavior to a realistic situation. The simulations of the model, compared with the system implementation in a traditional circuital simulator, have an excellent fit.

The model was used in the design of a vectorial control with the aim of increasing the PV power transferred to the DC-link. This algorithm is a multivariable MPPT that perturbs the operating point of all the DC/DC converters at the same time. Simulation results confirm that the proposed technique performs better than other multivariable controllers presented in the literature.

Another method developed in this Chapter, aimed at increasing the maximum power of a PV array operating under mismatching conditions, is based on the dynamic electrical reconfiguration of the array connections. The proposed procedure determines the best configuration of a PV array connected in a series-parallel structure without using complex mathematical models. Instead, it is based on the experimental current vs. voltage curves of the PV panels, which are composed by multiple PV modules. Such curves are used to construct the power vs. voltage curves of all of the possible configurations, which is needed to identify the optimal one. The main advantage of this method is the low computational effort required to reconstruct the power vs. voltage curves of the array. This characteristic enables one to implement the proposed solution using inexpensive embedded devices, which are widely adopted in industrial applications. The proposed method and its embedded implementation were tested using a hardware-in-the-loop simulation of the PV system. Finally, the real-time operation and benefits of the proposed solution were illustrated using a practical example

based on commercial devices.
The methods developed in this Chapter were reported in [54, 125, 126, 127].

2.1. Mathematical model of distributed photovoltaic systems

DMPPT are the architectures, methods and algorithms dedicated to the maximization of the power produced by a PV array in presence of mismatching conditions [56]. In particular, according to this approach, each PV module has its own switching converter in charge of tracking the module MPP. The DMPPT can be implemented using micro-inverters or, as in the case described in [56], by means of DC/DC converters, each one of them working independently from the others. In this way, the maximum level of modularity is obtained, because each DC/DC converter tracks the best operating point of the PV module it is dedicated to, hence the power produced by the whole PV system is maximized.
The power delivered by a photovoltaic (PV) module is inherently DC, and it is generally at low voltage. However, in many applications it is necessary to connect the PV modules to a high voltage DC-bus or an AC grid. In both cases, the electric power generated by a PV module must be converted to high voltage levels with the highest efficiency possible. To raise the PV modules voltage it is necessary to connect them in series [128, 129, 130, 52], each one of them interfaced by its corresponding DC/DC converter.
Once the size of the PV array grows, validation process of this system design becomes very difficult, hence simulations are mandatory to predict power generation. Therefore DMPPT (Distributed MPPT) systems are traditionally evaluated using an electric simulator, e.g. PSPICE® or PSIM®.
Those constraints result in the need to develop a mathematical model to predict the behavior of a DMPPT system in a detailed and accurate way. Such a model must not be based on a particular simulation software, instead it should enable its implementation in any programming language, e.g. C or Matlab®. Some authors have developed this type of mathematical models for DMPPT systems that can be implemented in nonlinear systems of equations [128, 129, 131]. For example, the work reported in [131] propose the model for PV-converter set, where the converter is a four-switch buck-boost converter used for distributed maximum power point tracking (DMPPT) in series-connected PV system applications. Likewise, [129] presented a model of two module-boost converter sets used for non-linear control of DMPPT applications. Similarly, the study presented in [128] describes a DMPPT system modeling a PV array-inverter set as part of a DC micro-grid based on renewable energy. Nevertheless, those works do not present a general model for N module-power converter sets enabling easy implementation in any programming language.
Therefore, this section proposes a general mathematical model for DMPPT systems, which includes the electrical equations for each PV module and the dynamics imposed by the

associated converters. Such level of detail makes this model an ideal tool for evaluating safety levels and MPPT algorithms. The results of this work were reported in [54, 125].

2.1.1. Model description

The functional unit of a DMPPT system is composed by a PV module and a DC/DC converter [56]. The mathematical model of the PV module is reported in [75, 66] and it is described by (2-1), in which I_{PV} is the current of the module, I_{SC} is the short-circuit current, V_{PV} is the voltage of the module and A_0 and B_0 are parameters depending on the irradiance and temperature.

$$I_{PV} = I_{SC} - A_0 \left(e^{B_0 \cdot V_{PV}} - 1\right) \tag{2-1}$$

The mathematical representation of the converter depends on the topology. Other authors [56, 61] report different analyses to determine the recommended converter for this type of applications. Those works conclude that the boost converter exhibits the best efficiency and functionality features to increase the voltage delivered by each module and, at the same time, perform the MPPT process. As a result, this section is based on the boost converter presented in Figure **2-1**. The resistance R_L, includes the effect of the inductor resistance, MOSFET on-resistance and diode losses.

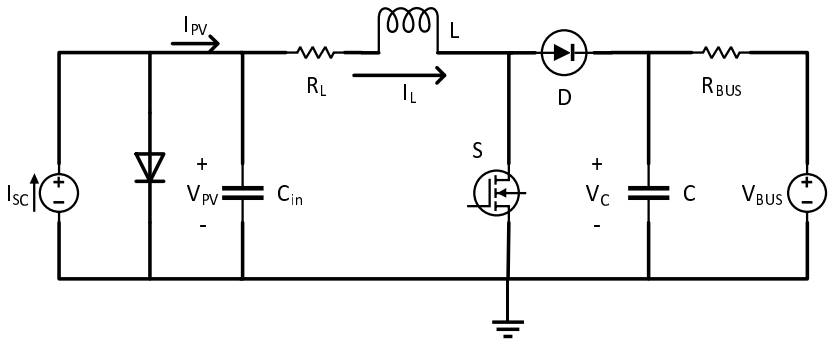


Figure 2-1.: Boost converter scheme.

2.1.1.1. Mathematical model of two modules in series

Figure **2-2** illustrates the connection in series of two PV-converter sets, which are coupled to a DC-bus. In commercial applications, the DC/AC converter (it could be a DC/DC converter for DC loads) regulates the voltage level of the DC-bus, which can be represented by its Thevenin equivalent [132, 133]. The parameters of this equivalent circuit are the voltage and the resistance of the bus, V_{BUS} and R_{BUS}, respectively. In Figure **2-2** both DC/DC converters have a control input (u_1 and u_2) to turn the MOSFETS on and off. Such an input corresponds

to a Pulse Width Modulated (PWM) signal with a D duty cycle generated by the MPPT controller. It is worth noting that the MPPT controller needs to know the instantaneous power of the system. Typically, each DC/DC converter has an associated MPPT controller, which means a significant number of processing units and, therefore, a high cost [56]. To mitigate this restriction, MPPT algorithms with multiple outputs have been proposed, e.g. the one depicted in Figure **2-2**. This type of MPPT algorithms record the power of the complete system to generate all the control signals, it requiring only a single pair of sensors and a single processing unit [56]. In any case, the model proposed in this section is suitable to evaluate both types of MPPT algorithms (single-output or multi-output).

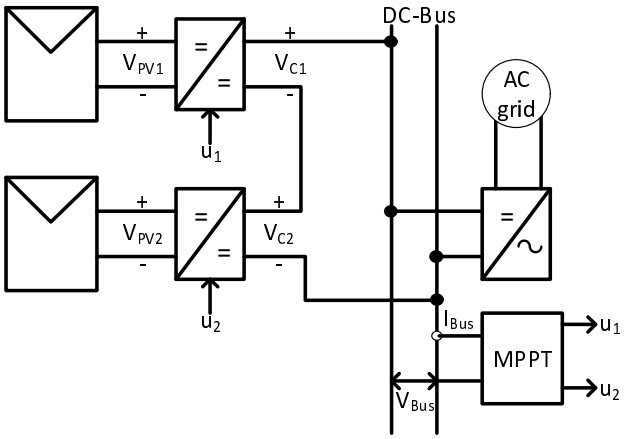


Figure 2-2.: Connection diagram of two modules in series with MPPT.

The equations representing the behavior of the system are presented in (2-2) to (2-7), where subscript 1 represents module 1 and subscript 2 refers to module 2. Those equations were obtained from the flux and charge balances in each inductor and capacitor, respectively [134]. For this mathematical model, a state variable is defined for each element storing energy. As a result, the system is composed by 6 state variables: voltages at the input (V_{pv1} and V_{pv2}) and output (V_{C1} and V_{C2}) capacitors, as well as the currents in the inductors (I_{L1} and I_{L2}). Equations (2-2) and (2-3) have an exponential component that corresponds to the model of the PV module in (2-1). Besides, (2-4) and (2-5) depend on the forward-voltage of the diode in each converter V_F. Finally, this mathematical representation corresponds to a nonlinear system with two binary control signals. In practice, such binary signals are replaced with continuous values of the duty cycles generated by the PWM signals.

Since the connection of the array is in series, it can be observed that in (2-6) and (2-7) the voltage in each output capacitor depends on the voltage of the next module. This is because $V_{BUS} = V_{C1} + V_{C2}$, where V_{BUS} is controlled by the DC/AC converter. As a result, a reduction in the output voltage of a converter produces an increase in the output voltage of the next converter. This means that the action on the control signal of a converter becomes a disturbance for another.

$$\dot{V_{pv1}} = \frac{I_{sc1}}{C_{in1}} - \frac{I_{L1}}{C_{in1}} - \frac{A_{01}}{C_{in1}}\left[e^{B_{01}V_{pv1}} - 1\right] \tag{2-2}$$

$$\dot{V_{pv2}} = \frac{I_{sc2}}{C_{in2}} - \frac{I_{L2}}{C_{in2}} - \frac{A_{02}}{C_{in2}}\left[e^{B_{02}V_{pv2}} - 1\right] \tag{2-3}$$

$$\dot{I_{L1}} = \frac{V_{pv1}}{L_1} - \frac{-\left(R_{L1} + R_{on1}u_1\right)}{L_1}I_{L1} - \frac{(1-u_1)}{L_1}V_{F1} - \frac{(1-u_1)}{L_1}V_{C1} \tag{2-4}$$

$$\dot{I_{L2}} = \frac{V_{pv2}}{L_2} - \frac{-\left(R_{L2} + R_{on2}u_2\right)}{L_2}I_{L2} - \frac{(1-u_2)}{L_2}V_{F2} - \frac{(1-u_2)}{L_2}V_{C2} \tag{2-5}$$

$$\dot{V_{C1}} = \frac{1-u_1}{C_1}I_{L1} - \frac{V_{C1}}{C_1R_{BUS}} - \frac{V_{C2}}{C_1R_{BUS}} + \frac{V_{BUS}}{C_1R_{BUS}} \tag{2-6}$$

$$\dot{V_{C2}} = \frac{1-u_2}{C_2}I_{L2} - \frac{V_{C1}}{C_2R_{BUS}} - \frac{V_{C2}}{C_2R_{BUS}} + \frac{V_{BUS}}{C_2R_{BUS}} \tag{2-7}$$

2.1.1.2. Model extension to $n > 2$ modules in series

This subsection describes an extension of the previous mathematical model to represent PV systems with $n > 2$ PV module-converter sets in series. An example of this type of systems was shown in Figure **1-4**. It is comprised by n modules and n converters, each one tagged with the subscript $1, 2, \ldots, n$. Moreover, each converter receives a control signal from the associated PWM, whose duty cycle is generated by the MPPT controller in charge of maximizing the power produced by the photovoltaic array.

Figure **2-3** shows the block diagram of the mathematical model of a PV array with n module-converter sets connected in series. The control signals are represented by vector $\vec{U}$ and the DC-bus voltage by the scalar value V_{BUS}. Similary, $(\vec{I_{SC}})$ is composed of the short-circuit currents of all the modules in the system. Those inputs are mathematically presented in (2-8). The output vectors are $(\vec{I_{PV}})$, $(\vec{V_{PV}})$, $(\vec{I_L})$ and $(\vec{V_C})$, which denote the currents of the modules, the voltage of the modules, the currents of the inductors of each converter and the output voltage of each module, respectively. Those outputs are described in (2-9).

$$\vec{I_{SC}} = \begin{bmatrix} I_{SC1} \\ I_{SC2} \\ \vdots \\ I_{SCn} \end{bmatrix} \quad ; \quad \vec{U} = \begin{bmatrix} u_1 \\ u_2 \\ \vdots \\ u_n \end{bmatrix} \tag{2-8}$$

$$\vec{I_{PV}} = \begin{bmatrix} I_{PV1} \\ I_{PV2} \\ \vdots \\ I_{PVn} \end{bmatrix} \quad ; \quad \vec{V_{PV}} = \begin{bmatrix} V_{PV1} \\ V_{PV2} \\ \vdots \\ V_{PVn} \end{bmatrix} \quad ; \quad \vec{I_L} = \begin{bmatrix} L_{L1} \\ L_{L2} \\ \vdots \\ L_{Ln} \end{bmatrix} \quad ; \quad \vec{V_C} = \begin{bmatrix} V_{C1} \\ V_{C2} \\ \vdots \\ V_{Cn} \end{bmatrix} \tag{2-9}$$

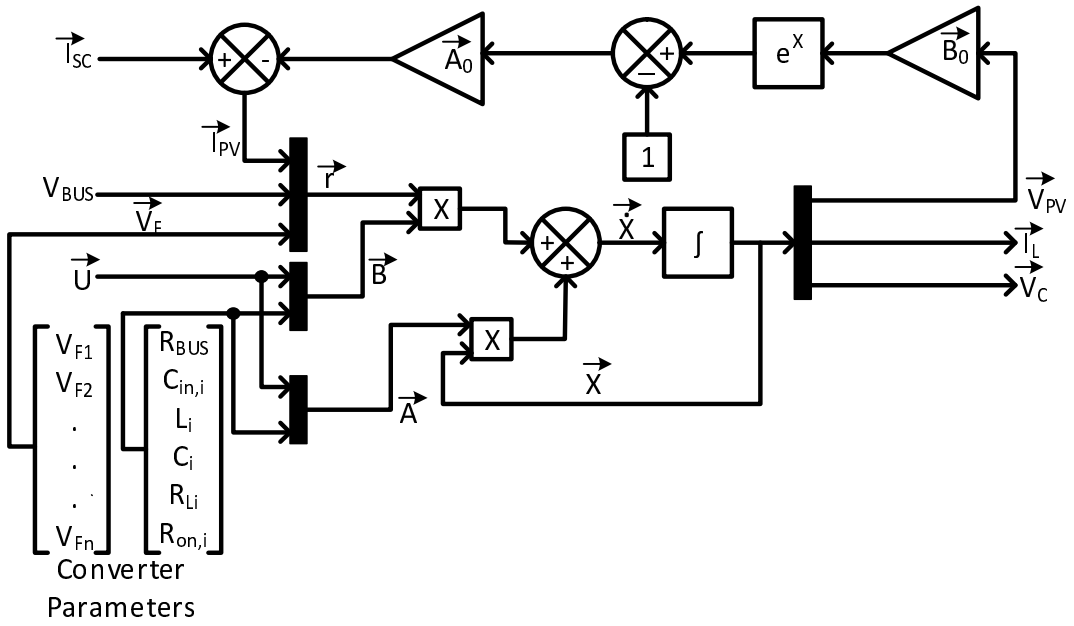


Figure 2-3.: Block diagram of the model of n modules in series.

Figure **2-3** also presents, on top, the equation of the current of the modules in a matrix, as shown in (2-11), which depends on the voltages ($\vec{V_{PV}}$) and matrices ($\vec{A_0}$) and ($\vec{B_0}$) defined in (2-10). Such matrices contain the parameters of each module in the order defined by (2-8).

$$\vec{A_0} = \begin{bmatrix} A_{01} & 0 & \dots & 0 \\ 0 & A_{02} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & A_{0n} \end{bmatrix} \quad ; \quad \vec{B_0} = \begin{bmatrix} B_{01} & 0 & \dots & 0 \\ 0 & B_{02} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & B_{0n} \end{bmatrix} \tag{2-10}$$

$$\vec{I_{PV}} = \vec{I_{SC}} - \vec{A_0} \left(e^{\vec{B_0} \cdot \vec{V_{PV}}} - \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \right) \tag{2-11}$$

The mathematical model of the array of n module-converter sets in series is based on the solution of the differential equation given in (2-13). In such a matrix equation, vector $\vec{X}$ contains the state variables of the system (2-12). It can be observed that the first 3 rows correspond to module 1, the next 3 rows to module 2, and so on until module n. Vector $\vec{r}$ is formed by the DC-bus voltage, the current of each module and the voltage of the diode in each converter (V_{Fn}), as described in (2-12). The current of the module and the voltage of the diode are different for each module-converter set, but the DC-bus voltage is the same.

By this reason, in the vector $\vec{r}$ every three positions there is a new module current and diode voltage, but the DC-bus voltage is only present in the first position.

$$\vec{X} = \begin{bmatrix} V_{PV1} \\ I_{L1} \\ V_{C1} \\ V_{PV2} \\ I_{L2} \\ V_{C2} \\ \vdots \\ V_{PVn} \\ I_{Ln} \\ V_{Cn} \end{bmatrix} \quad ; \quad \vec{r} = \begin{bmatrix} V_{BUS} \\ I_{PV1} \\ V_{F1} \\ 0 \\ I_{PV2} \\ V_{F2} \\ \vdots \\ 0 \\ I_{PVn} \\ V_{Fn} \end{bmatrix} \tag{2-12}$$

$$\dot{\vec{X}} = \vec{A}\vec{X} + \vec{B}\vec{r} \tag{2-13}$$

The solution of systems of non-linear differential equations with several variables, as the one given in (2-13), requires a numerical method, which may be Newton's method, the quasi-Newton method or finite difference method, among others.

Jacobian matrices $\vec{A}$ and $\vec{B}$, reported in (2-14) and (2-15), are obtained from the charge and flux balances, the parameters of the converters and vector $\vec{U}$. In matrix $\vec{A}$, the first column lists the parameters of the converter, which are multiplied by V_{PV1}; the second column corresponds to the parameters related to I_{L1}; and the third column contains the parameters to be multiplied by V_{C1}.

The subsequent columns follow the same order, but with respect to the other converters in the array. Around the main diagonal of matrix $\vec{A}$ are located the parameters of each converter. Every third column (which corresponds to the output voltage of the converters) lists the output capacitors of the rest of the converters, highlighted in gray, thus indicating the electrical coupling among all the converters in the array.

Matrix $\vec{B}$ contains the system parameters that are multiplied by the components of vector $\vec{r}$. The first column lists the terms that relate the output voltages with the DC-bus voltage, highlighted in gray. The second column includes parameters related to I_{PV1}, and the third column contains the terms multiplied by V_{F1}. The subsequent columns (in groups of three) correspond to converters 2 to n.

Due to the size of the Jacobian matrices, $\vec{A}$ and $\vec{B}$, it was necessary to split them with the aim that they fit within the margin of the page. The $\vec{A}$ matrix is split from the fifth column, while $\vec{B}$ matrix is split from the sixth column.

2.1.1.3. Model parameterization process

This subsection describes the process to implement the model of a distributed photovoltaic MPPT system composed of n module-converter sets connected in series:

$$\vec{A} = \begin{bmatrix} 0 & \frac{-1}{C_{in1}} & 0 & 0 & 0 \\ \frac{1}{L_1} & \frac{-(R_{L1}+R_{on1}u_1)}{L_1} & \frac{-(1-u_1)}{L_1} & 0 & 0 \\ 0 & \frac{1-u_1}{C_1} & \frac{-1}{R_{BUS}C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{-1}{C_{in2}} \\ 0 & 0 & 0 & \frac{1}{L_2} & \frac{-(R_{L2}+R_{on2}u_2)}{L_2} \\ 0 & 0 & \frac{-1}{R_{BUS}C_2} & 0 & \frac{1-u_2}{C_2} \\ \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{R_{BUS}C_n} & 0 & 0 \end{bmatrix}$$

$$\begin{bmatrix} 0 & 0 & \dots & 0 & 0 & 0 \\ 0 & 0 & \dots & 0 & 0 & 0 \\ \frac{-1}{R_{BUS}C_1} & 0 & \dots & 0 & 0 & \frac{-1}{R_{BUS}C_1} \\ 0 & 0 & \dots & 0 & 0 & 0 \\ \frac{-(1-u_2)}{L_2} & 0 & \dots & 0 & 0 & 0 \\ \frac{-1}{R_{BUS}C_2} & 0 & \dots & 0 & 0 & \frac{-1}{R_{BUS}C_2} \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 0 & \frac{-1}{C_{in,n}} & 0 \\ 0 & 0 & \dots & \frac{1}{L_n} & \frac{-(R_{Ln}+R_{on,n}u_n)}{L_n} & \frac{-(1-u_n)}{L_n} \\ \frac{-1}{R_{BUS}C_n} & 0 & \dots & 0 & \frac{1-u_n}{C_n} & \frac{-1}{R_{BUS}C_n} \end{bmatrix} \quad (2\text{-}14)$$

1. Obtain parameters A_0 and B_0 from each module, as reported in [130], and insert them into matrices $\vec{A_0}$ and $\vec{B_0}$.
2. Create vector $\vec{I_{SC}}$ from the irradiance of each module [130].
3. Implement the equation of system currents (2-11).

4. Obtain the parameters of each converter, i.e. C_{in}, L, R_L, R_{on}, V_F and C.

5. Create vectors $\vec{U}$, $\vec{r}$ and matrices $\vec{A}$ and $\vec{B}$ according to the sequence reported in (2-8), (2-12), (2-14) and (2-15), respectively.

6. Implement (2-13) and solve it using a numerical integration method. It is important to define the initial conditions of the state variables, avoiding negative values, because the system does not allow a change in the direction of the currents or the polarity of the voltages.

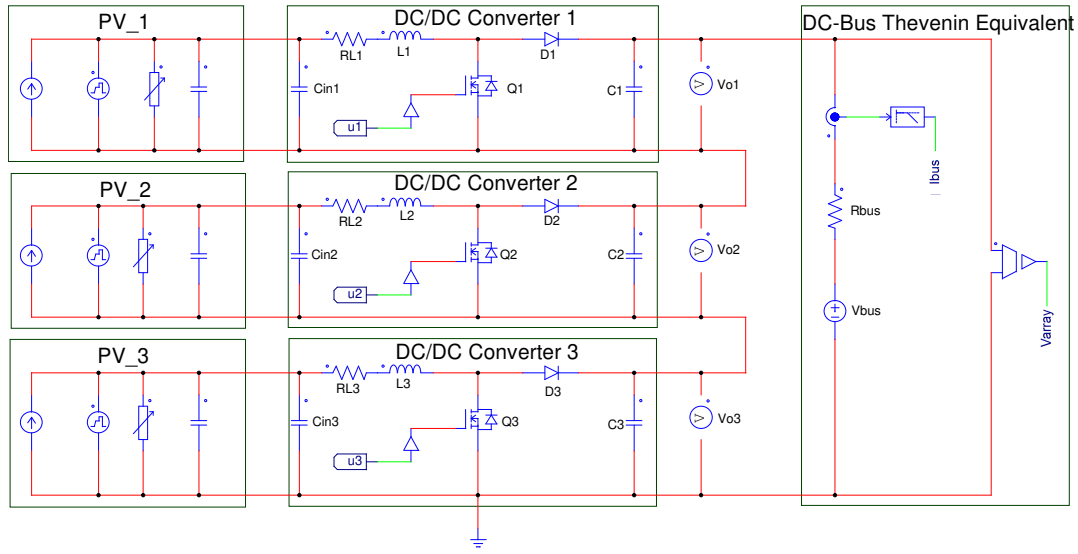
$$\vec{B} = \begin{bmatrix} 0 & \frac{1}{C_{in1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{-(1-u_1)}{L_1} & 0 & 0 & 0 \\ \frac{1}{R_{BUS}C_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{C_{in2}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{-(1-u_2)}{L_2} \\ \frac{1}{R_{BUS}C_2} & 0 & 0 & 0 & 0 & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{1}{R_{BUS}C_n} & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 0 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 0 & \dots & 0 & \frac{1}{C_{in,n}} & 0 \\ 0 & \dots & 0 & 0 & \frac{-(1-u_n)}{L_n} \\ 0 & \dots & 0 & 0 & 0 \end{bmatrix} \tag{2-15}$$

2.1.2. Model validation and application example

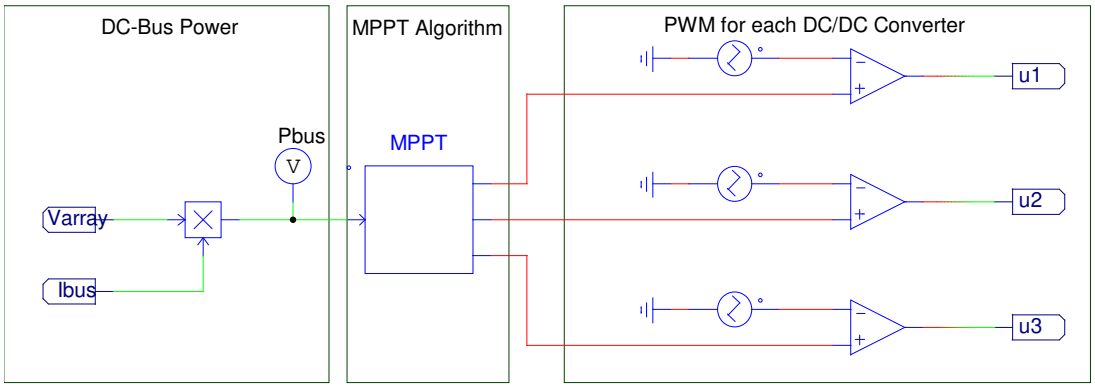
This section presents the validation of the proposed model, presenting also an example of the model use. First, the accuracy of the model is evaluated with respect to a detailed circuital simulation performed using the professional simulator PSIM® [135]. Second, an example of the application of the model is presented; it is used to evaluate the performance of a DMPPT algorithm controlling 10 PV-sets in series connection.

2.1.2.1. Validation of the mathematical model with three modules in series

In order to validate the proposed model, a circuit was designed based on Figure **1-4** considering three PV modules.The circuit was simulated in the electronic simulation software PSIM®. Moreover, the mathematical model was developed following the design procedure described in Subsection 2.1.1.3. The topology of the PV array implemented in PSIM® is presented in Figure **2-4**a: the array is composed of three module-converter units identified with subscripts 1, 2 and 3. Each panel is represented with a DC source and a nonlinear element, according to (2-1). To simulate the changes in irradiance, a variable current source is used in parallel with each panel. As previously mentioned, each DC/DC converter has a boost topology and the load of the array is the Thevenin equivalent of a DC-bus. Figure **2-4**b details the calculation of the DC-bus power; based on this information, the MPPT algorithm calculates the duty cycle of the PWM for each converter, as described below.
Both the model implemented in Matlab® and the PSIM® circuit consider the following parameters. BP-585 PV modules with STC parameters provided by the manufacturer: open circuit voltage of the module $V_{OC} = 22.1V$, short-circuit current $I_{SC} = 5A$, temperature coefficient for the voltage $-80\frac{mV}{^\circ C}$ and temperature coefficient for the current $0.065\frac{\%}{^\circ C}$. Those characteristics allow to evaluate the parameters $A_0 = 8.9412e^{-7}A$ and $B_0 = 0.7030V^{-1}$ by following the method proposed in [130]; which enable to simulate the behavior of the module for each irradiance value using (2-1), as illustrated in Figure **2-5**. That Figure shows the following MPPs under different irradiance conditions: for $600\frac{W}{m^2}$, it is at $49W$ power and $17.5V$ voltage; for $500\frac{W}{m^2}$, at $40W$ and $17.3V$; and at $32W$ and $17V$ for $400\frac{W}{m^2}$. The converter adopted for each PV module follows the design process presented in [75]: the input and output capacitors were calculated as $94\mu F$ and $55\mu F$, respectively, to meet a ripple voltage $\Delta V_C = 0.05V$. The inductor was selected as $28mH$ with an associated losses resistor R_L of $38m\Omega$ to meet a ripple current $\Delta I_L = 0.1A$ for a switching frequency of $100kHz$. Furthermore, to increase the model accuracy, the on resistance of the MOSFET $R_{ON} = 0.077\Omega$ was considered. Moreover, the system takes into account the voltage imposed by the DC/AC converter $V_{BUS} = 120V$ and a $R_{BUS} = 0.23\Omega$.
As previously mentioned, the validation of the model is carried out based on the scheme presented in Figure **1-4**, in which a centralized MPPT algorithm is used to generate the control actions for each converter (DMPPT action). The most widely used MPPT algorithm is based on the Perturb and Observe (P&O) method. It applies a constant increase or decrease



(a) The topology of three modules in series.



(b) PWM signals for each one of three modules in series.

Figure 2-4.: Simulation scheme in PSIM® of three modules in series.

to the voltage of the PV module and measures the resulting power in the module. If the power increases, the algorithm continues to change the voltage in the same direction; however, if power drops, voltage perturbation direction is changed [136, 58, 137]. In the adopted DMPPT system with n PV modules, the algorithm is designed to maximize power at the system output (i.e. at the input terminals of the DC/AC converter). This modification to the traditional algorithm enables to reduce the number of sensors in the output terminals of each module, thus reducing the implementation costs. This algorithm, named MOPOC (Multi-Output P&O Controller), has n outputs to define the duty cycle of the PWM associated with each one of the n DC/DC converters. The design of the algorithm is based on [56] with a modification that enables to reconfigure the parameters and automatically generate an algorithm for n PV modules. The flowchart in Figure **2-6** describes the algorithm.

The MOPOC algorithm starts by defining the operating parameters of the algorithm: n is

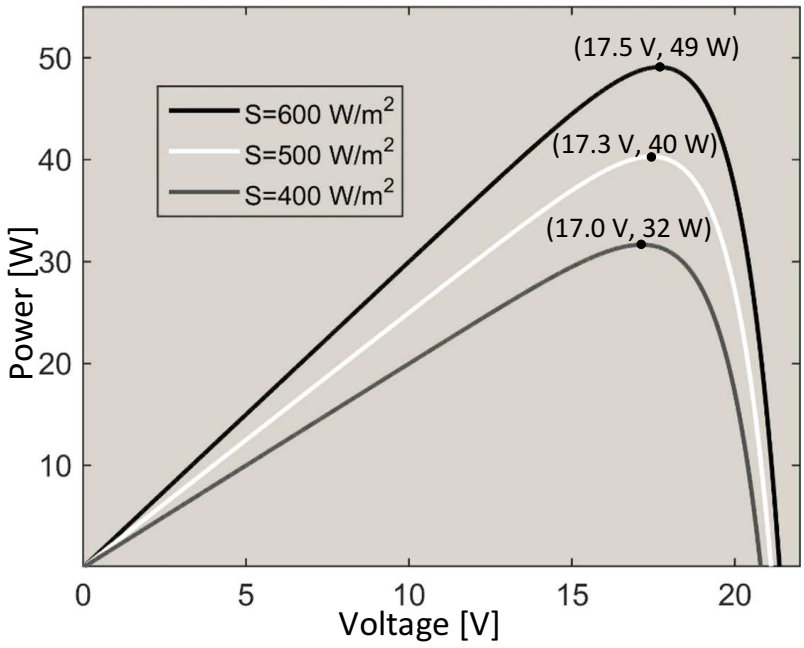


Figure 2-5.: Simulated power profile of the BP 585 module based on (2-1).

the number of modules, the magnitude of the perturbation in the duty cycle is Δd and the array power at the first instant is $P(k-1)$. Subsequently, the output power is measured and, if it is higher than the power measured in the previous instant and the duty cycle is within the valid range, the duty cycle is perturbed in the same direction. Otherwise, the disturbance changes sign and the duty cycle is perturbed in the opposite direction. The sequential tracking of the maximum power point of each PV module is thus ensured. Finally, for simulation purposes - on both the model and PSIM® - the DMPPT is considered with the parameters $\Delta d = 0.005$ and $t_s = 0.2ms$, obtained from the design process presented in [62].

Figure **2-7** presents the simulation of the system considering irradiance changes. The simulation compares the results of the mathematical model (white line) and the circuital simulation in PSIM® (black line). The simulation presents an irradiance change from $500\frac{W}{m^2}$ to $600\frac{W}{m^2}$ in PV_1 at $0.2s$; later, the irradiance drops to $400\frac{W}{m^2}$ at $0.8s$. Likewise, PV_2 exhibits an irradiance decrease at $0.6s$ from $600\frac{W}{m^2}$ to $500\frac{W}{m^2}$ and an increment to $700\frac{W}{m^2}$ after $1s$. Lastly, PV_3 presents an irradiance decrease from $500\frac{W}{m^2}$ to $400\frac{W}{m^2}$ at $0.4s$, while at $1.3s$ it is increased to $600\frac{W}{m^2}$. It should be noted that, for all the irradiance values, the power of each module is the maximum available power, as confirmed by Figure **2-5**. This demonstrates the accuracy of the adopted MPPT algorithm. Moreover, Figure **2-7** proves the model accuracy in the prediction of the circuital simulator data. An average of the point-to-point error was calculated during the complete simulation interval for both systems, with a resulting accuracy of 97 %. Such a value leads to the conclusion that the simulation based on the previously designed

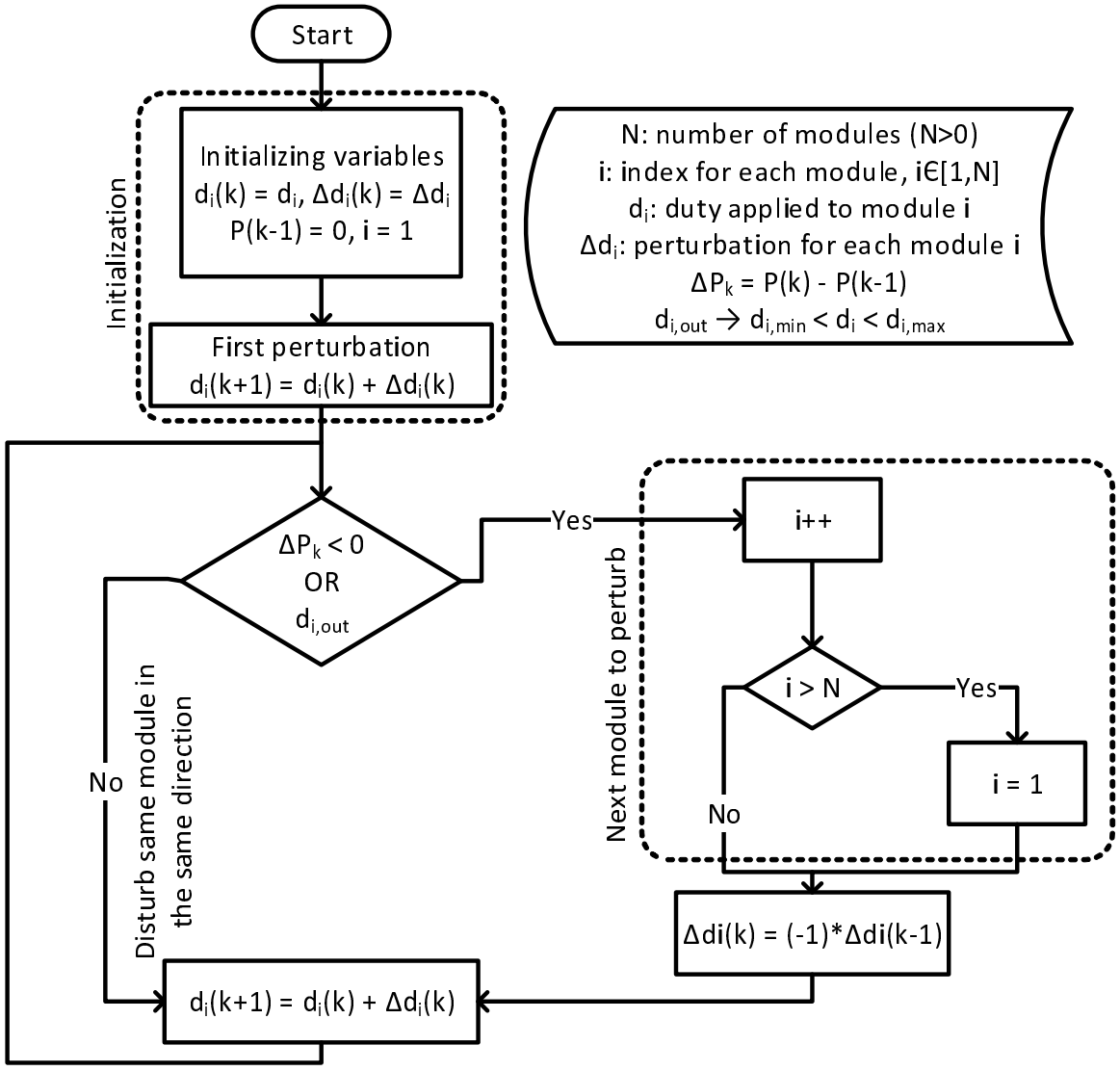


Figure 2-6.: Flowchart of the MPPT MOPOC algorithm.

model reproduces accurately the PV system behavior, thus avoiding the use of high-cost simulators or difficult-to-build simulation schemes which, eventually, delay the design of the application. Figure **2-8** presents the simulation of the current of each module, which again show a satisfactory behavior of the proposed model.

Similarly, Figure **2-9** presents the simulation of the voltage at the output capacitor of each converter in presence of constant irradiance changes. Such a simulation proves the effectiveness of the model in predicting the behavior of the system under variations at the input terminals of each converter. It should be noted that the sum of the voltages at each instant should equal the total voltage of the system imposed by the $120V$ DC/AC converter, e.g. at $t = 0.6s$, voltages $V_{C1} = 50V$, $V_{C2} = 40V$ and $V_{C3} = 30V$.

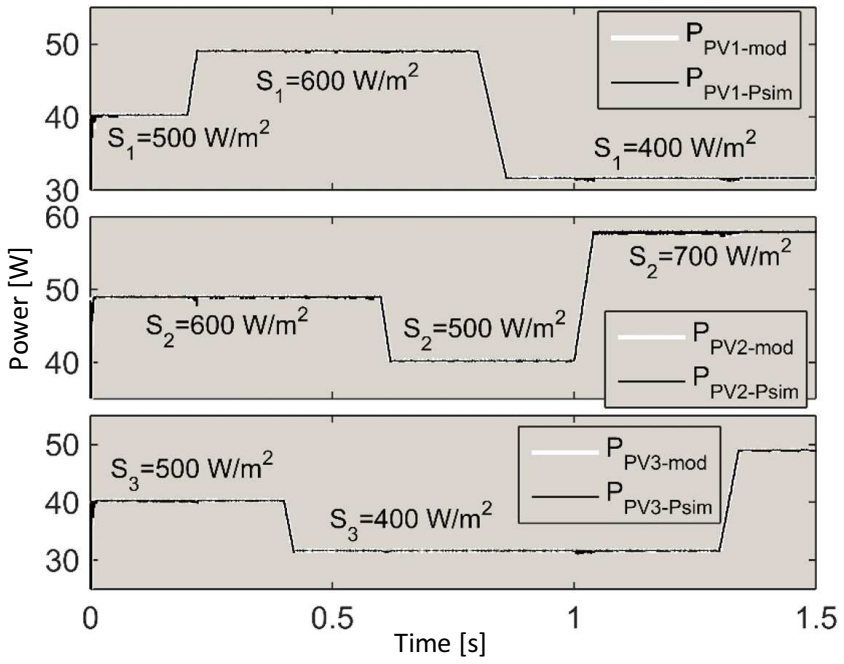


Figure 2-7.: Simulation of power generated by the system with three modules.

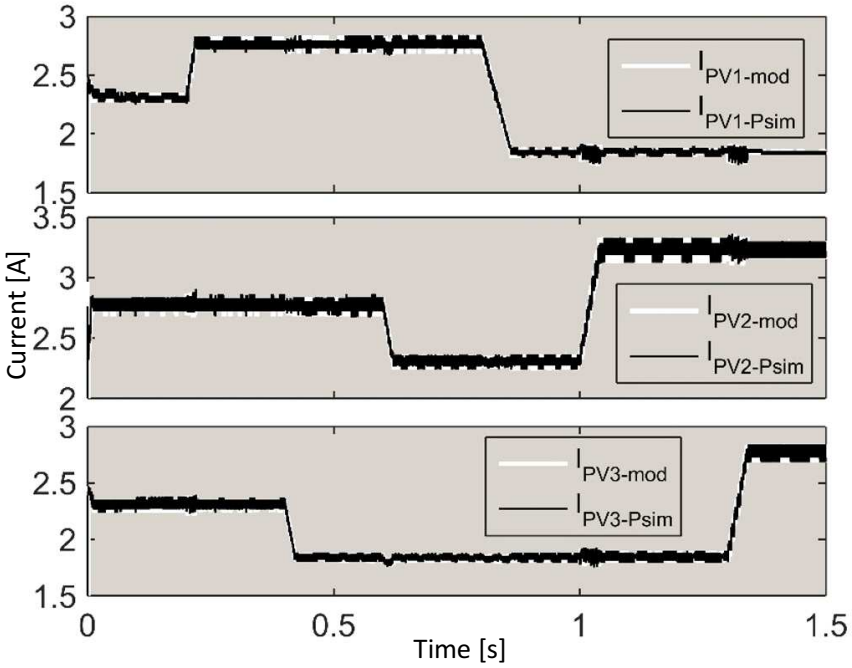


Figure 2-8.: Simulation of current generated by the system with three modules.

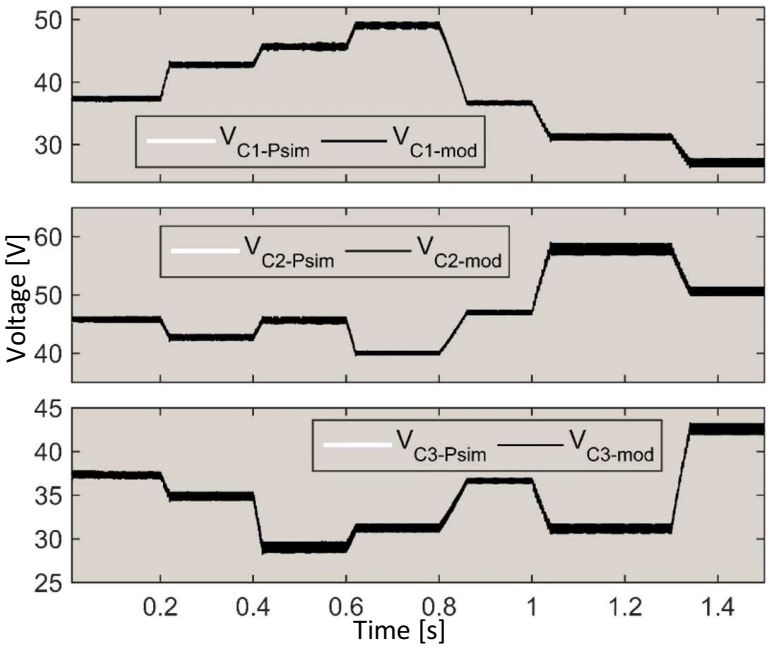


Figure 2-9.: Simulation of condenser voltage for the system with three modules.

2.1.2.2. Application example: simulation of a DMPPT system with 10 modules in series

In order to validate the capability of the model to carry out simulations of medium-sized photovoltaic arrays without using specialized simulation software, hence a 10-module system with the corresponding converters is proposed. The parameters are selected as in the previous simulations, except that the voltage imposed by the output DC/AC converter is adjusted to $V_{BUS} = 410V$ and $R_{BUS} = 0.78\Omega$. The proposed model is implemented with an expansion to 10 modules and it is evaluated under the same conditions stated before.

Figure **2-10** shows the power simulation of each module for different irradiance changes. In order to present the results appropriately, the 10 modules were classified into three groups with a specific irradiance. As a result, for modules PV_1-PV_4, the irradiance increased at $t = 0.2s$ and decreased at $t = 0.8s$. The next group is formed by modules PV_5-PV_7 with an irradiance drop at $t = 0.6s$ and a rise at $t = 1s$. The last group includes modules PV_8-PV_{10}, and it assumed an irradiance drop at $t = 0.4s$ and a rise at $t = 1.3s$. Similar to the simulation reported in Figure **2-7**, the modules present a maximum power equal to the one described in Figure **2-5**, which validates the effectiveness of the MPPT algorithm employed in this study.

Figure **2-11** presents the current of each group of modules, in which the changes due to irradiance disturbances can be noted. Contrary to the simulation presented in Figure **2-8**, slight current variations that occur with irradiance steps are observed. Such disturbances take place because the MPPT must be adjusted to send 10 independent control signals with a $t_s = 0,2ms$ delay between them, which affects the performance of the system.

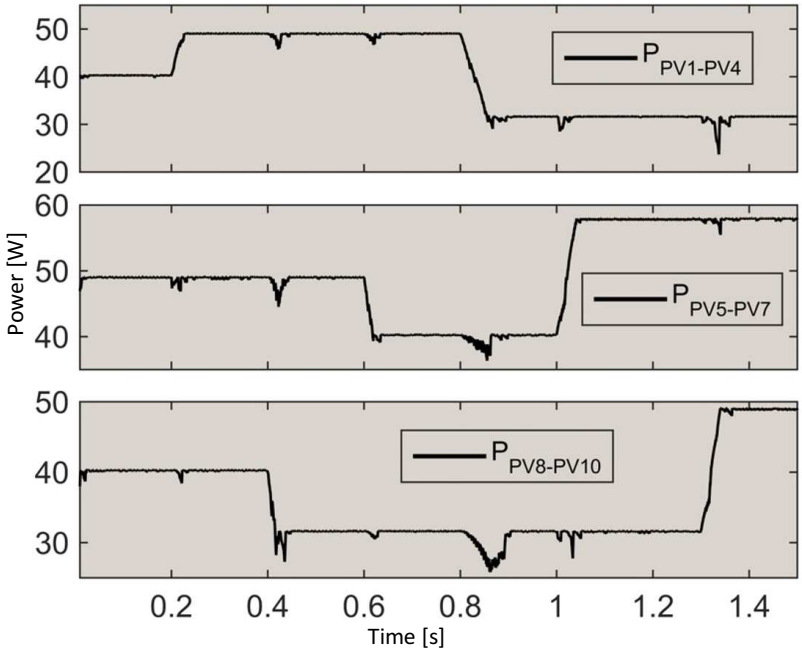


Figure 2-10.: Simulation of power generated by the system with 10 modules.

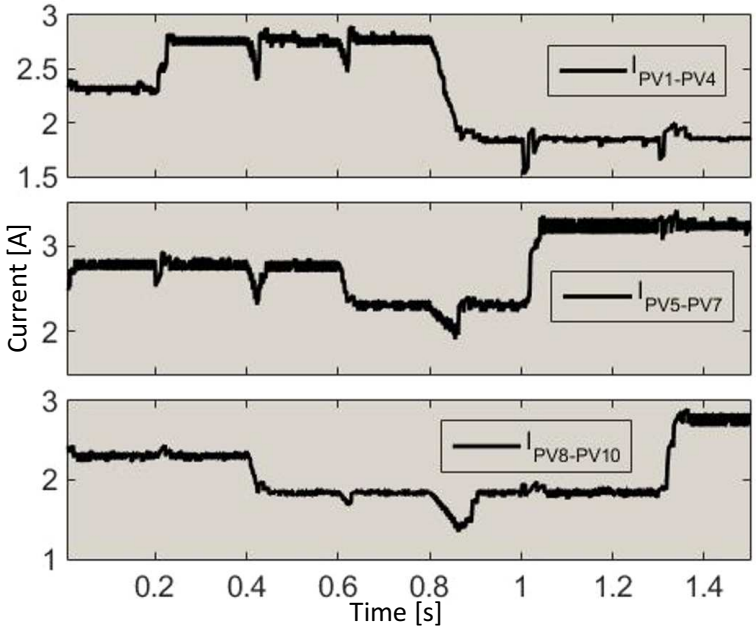


Figure 2-11.: Simulation of current generated by the system with 10 modules.

Finally, Figure **2-12** presents the simulation of the output voltage of each converter in the 10-module simulation. As in the simulations presented above, the voltages are associated with three measurement groups. The advantage of simulating the system and its behavior when irradiance changes occur is thus revealed, namely, to predict the behavior of voltages,

currents, and powers. Besides, the validity of the model is verified when the voltage restriction imposed by the DC/AC converter is respected, where the sum of the voltages at each instant is equal to $410V$, e.g. at $t = 0.6s$, the voltages $V_{C1-C4} = 50V$, $V_{C5-C7} = 40V$ and $V_{C8-C10} = 30V$. Those simulations validate the usefulness and accuracy of the model proposed for n series-connected PV sets.

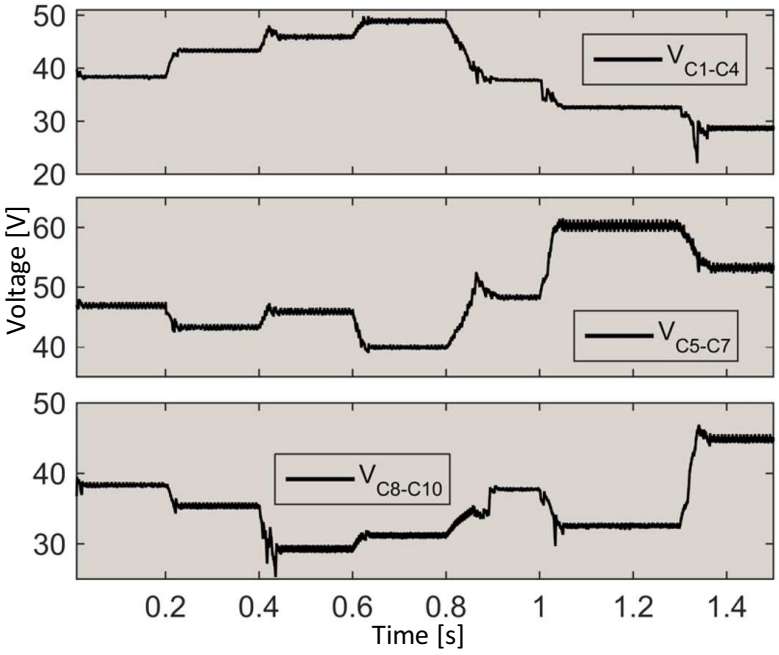


Figure 2-12.: Simulation of condenser voltage for the system with 10 modules.

Finally, this model is useful for predicting the complex dynamics exhibited by large DMPPT systems, which enable a correct design of DMPPT algorithms and protections.

2.2. Vectorial MPPT algorithm for distributed photovoltaic system

Traditional DMPPT solutions consider dedicated DC/DC converter each PV module, as it was discussed in the previous section. Unfortunately, this approach does not allow to obtain information about the mismatched conditions at which the PV modules work. Moreover, the number of current sensors becomes equal to the number of PV modules and the efficiency vs power curve of the DC/DC converters is not accounted for. In fact, in some operating conditions, the DC/DC conversion losses might counterbalance the benefits obtained with the DMPPT [138].
In recent literature some multi-variable MPPT (MV-MPPT) algorithms have been presented [62, 63, 64]. They require one pair of current/voltage sensors and one processing device only.

Therefore, MV-MPPT algorithms require less hardware and allow to reduce the system costs. Moreover, the multi-variable solutions maximize the total output power, therefore the DC/DC converters' operating points are also optimized.

In this section a novel MV-MPPT algorithm is introduced. The main difference with respect to other MV-MPPT solutions consist in the use of polar coordinates instead of cartesian coordinates: magnitudes and angles are used for describing the operating point instead of the PV voltages. Therefore, the perturbed variables are not the PV voltages as in [62, 64], but the magnitude and the angle of the vector that describes the operating point. This ensures a faster tracking of the MPP in comparison with other MV-MPPT algorithms, which perturb one PV voltage at the time, therefore in each perturbation instant there are $N-1$ frozen PV voltages, where N is the number of PV modules. Instead, the proposed vectorial MV-MPPT presented in this Section perturbs all the PV voltages at each perturbation instant, thus decreasing the MPP tracking time and providing more energy in transient conditions with respect to the solutions reported in [62, 64].

This section introduces the novel MV-MPPT algorithm operation, shows the steady-state profiles and demonstrates the improved tracking speed. Matlab® simulations confirm the advantages of the approach with respect to existing solutions. Finally, this work was reported in the conference paper [126].

2.2.1. PV system architecture for DMPPT

As it is usual in DMPPT architectures, in this section it is assumed that the output terminals of the DC/DC converters are connected in series as in Figure **2-13**. However, the solution proposed in this section is also applicable to parallel connected DC/DC converters. In both cases, the PV systems deliver the generated power to a DC-bus represented, without loss of generality, by a Thevenin model, which could be a battery or the input of a DC/AC stage.

The classical single-output (SOPO) [56] and multi-output control structures are depicted in Figure **2-14**. The multi-output solution observes the power delivered to the DC-bus in order to maximize it, and perturbs the DC/DC converters' voltage references, thus defining the PV voltages. Figure **2-13** also shows that the multi-output algorithms maximize the total power produced by the whole system, thus accounting for the DC/DC converters losses. This represents an advantage over classical SOPO solutions that are not able to account for the operating points of the DC/DC converters.

The proposed multi-variable MPPT algorithm (MVPOV) observes the DC-bus power to define the voltage of the PV modules. The operation mode and the features of the proposed algorithm are described in the next subsection.

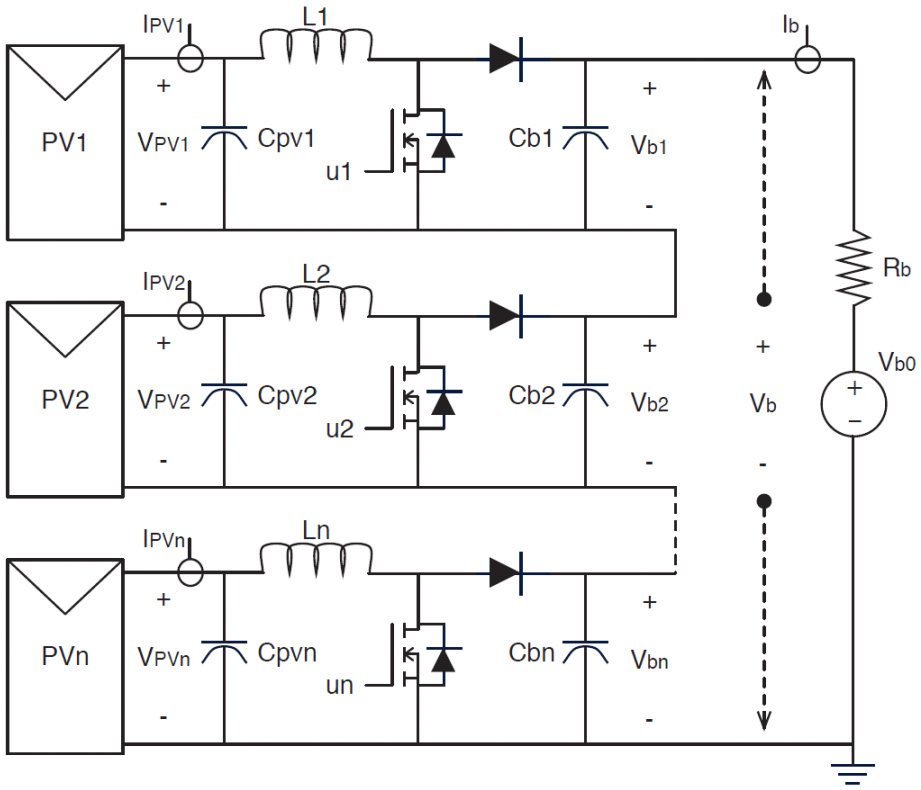
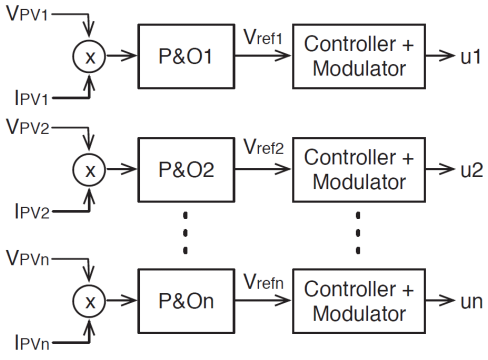
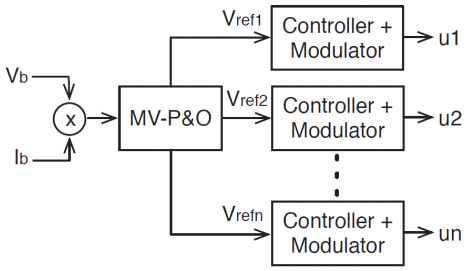


Figure 2-13.: Granular PV modules control architecture: power processing stages.



(a) Single output P&O.



(b) Multiple output P&O.

Figure 2-14.: Granular PV modules control architecture: control strategy.

2.2.2. The vectorial MPPT algorithm

The MVPOV algorithm is based on a vectorial representation of the system operating point by means of polar coordinates. Figure **2-15** shows both cartesian (MVPOC algorithm described in [62]) and MVPOV representations for a PV system composed by two modules. In such a system, MVPOC describes the MPP by means of PV voltages V_{PV1} and V_{PV2}, while MVPOV describes the MPP by means of the vector magnitude $|Vec|$ and angle θ. MVPOV

perturbs the system operating point so that a single variable is perturbed at any time, thus $|Vec|$ and θ are changed asynchronously. In MVPOC, the perturbation acts on a single PV voltage at a time, while in the proposed MVPOV the perturbation of $|Vec|$ or θ generates a simultaneous perturbation on both PV voltages as follows:

$$V_{pv1} = |Vec| \cos(\theta) \tag{2-16}$$

$$V_{pv2} = |Vec| \sin(\theta) \tag{2-17}$$

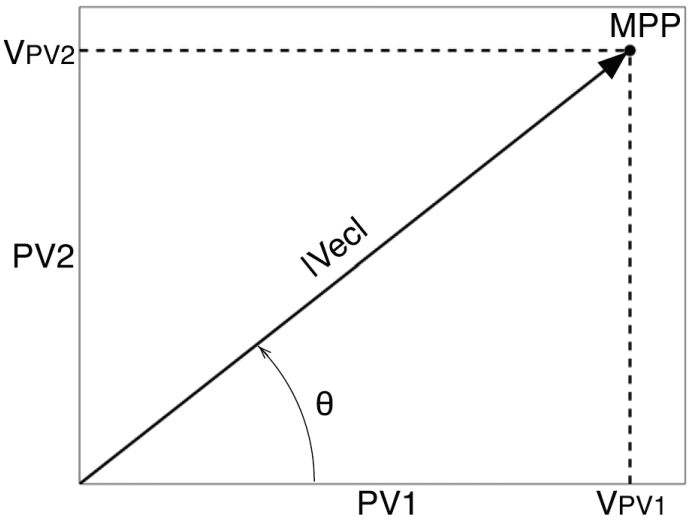


Figure 2-15.: Vectorial operating point description: two PV modules.

In general, for a PV system with N modules, the PV voltages $\{V_{PV1}, V_{PV2}, \ldots, V_{PVN}\}$ are described by spherical coordinates $\{|Vec|, \theta_1, \theta_2, \cdots, \theta_{N-1}\}$ [139].

For a number N of PV modules, the MVPOV algorithm perturbs each variable ($|Vec|$ and θ_i, $i = 1 \cdots N-1$) until the DC-bus power shows a decrease. In such a case, instead of changing the sign of the perturbation of the same variable, the latter is frozen and the perturbation affects the next variable in the totem, where the first element is $|Vec|$. Such perturbation is applied with a sign that is the opposite one of the last perturbation operated on the same variable (see Figure **2-16**). As explained in the sequel, such a strategy ensures that the whole system reaches a steady state that is a multi-dimensional extension of the typical P&O regime [62]: in MVPOV such profiles are on the vector variables, while in MVPOC they are on the PV voltages. The effect produced by the change of a spherical coordinate variable in the panels voltage is given in (2-18) [140].

$$
\begin{aligned}
V_{pv1} &= |Vec| \cos(\phi_1) \\
V_{pv2} &= |Vec| \sin(\phi_1) \cos(\phi_2) \\
V_{pv3} &= |Vec| \sin(\phi_1) \sin(\phi_2) \cos(\phi_3) \\
&\vdots \\
V_{pv_{n-1}} &= |Vec| \sin(\phi_1) \cdots \sin(\phi_{n-2}) \cos(\phi_{n-1}) \\
V_{pv_n} &= |Vec| \sin(\phi_1) \cdots \sin(\phi_{n-2}) \sin(\phi_{n-1})
\end{aligned}
\tag{2-18}
$$

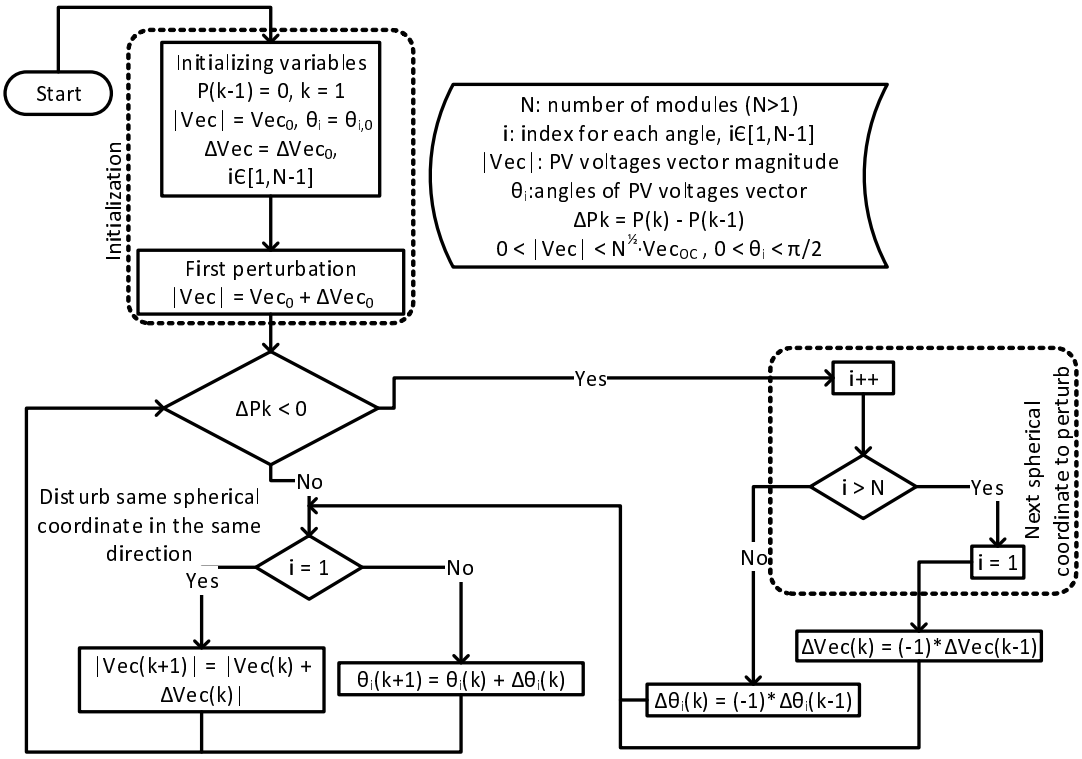
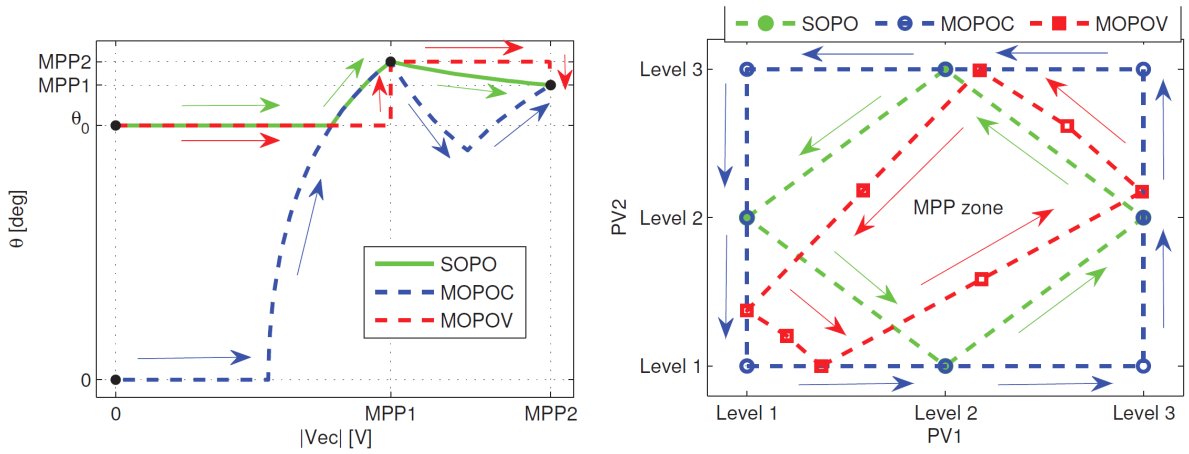


Figure 2-16.: Flowchart of the MPPT MOPOV algorithm.

To the aim of illustrating the MOPOV operation qualitatively, the case of two PV modules connected at the inputs of the same number of DC/DC converters, each one controlled by the SOPO, MOPOC and MOPOV algorithms, is considered (see Figure **2-17**). By using a fixed amplitude of the PV voltage perturbation steps, the SOPO algorithm exhibits the optimal trajectories to reach the MPPs for both PV units. Instead, MOPOC algorithm optimizes first V_{PV1} and then optimizes V_{PV2}, therefore the trajectories are far from the optimal ones. MOPOV offers a tradeoff between SOPO and MOPOC: it requires the same hardware needed for implementing the MOPOC algorithm, but its trajectory is close to the one exhibited by SOPO. MOPOV applies an initial angle of 45° so that it provides the same initial perturbation to both PV voltages. Figure **2-17**a shows the evolution of the PV system

operating point in a vectorial representation: it is evident that MOPOV perturbs a single vectorial variable at time, but it produces a MPP trajectory close to the optimal one followed by SOPO algorithm. It is also worth showing the steady-state behavior of the algorithms around the MPP. Figure **2-17**b shows the three-points behavior typical of the classical P&O approach for each PV module. Such a condition is clearly established by MOPOC: each PV voltage oscillates among three possible levels (1, 2 and 3), so that the sequence in steady-state is like 1-2-3-2. For a given number of variables (N) the number of states N_s is given in (2-19) [62].

$$N_s = N \cdot 4 \tag{2-19}$$



(a) Vectorial trajectory in a two PV system.

(b) Steady state voltage profiles in a two PV system.

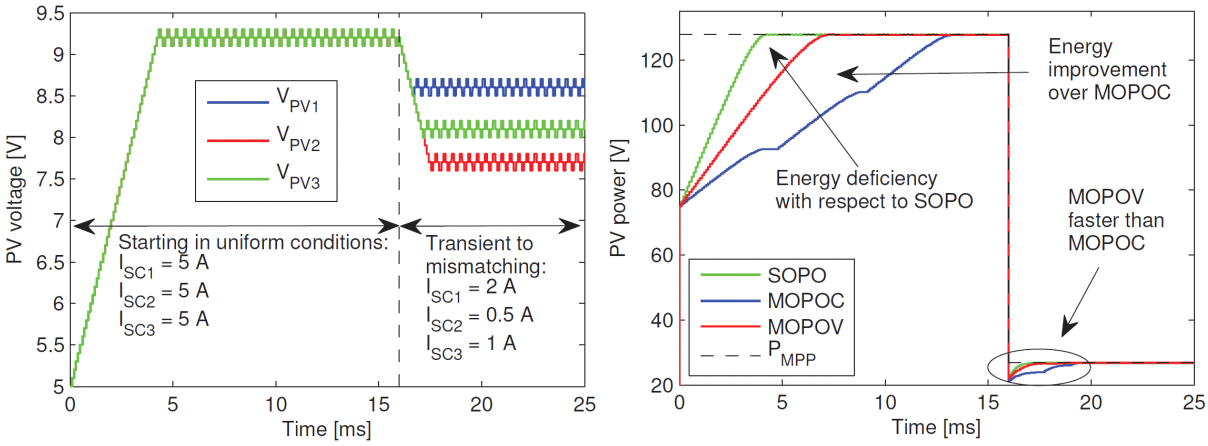
Figure 2-17.: MPPT trajectories and steady state profiles for single-output and multi-output algorithms.

The number of states defines the steady-state profile, hence it also defines the final oscillation of the output power around the MPP. Figure **2-17**b shows the states map for MOPOC: $N_s = 8$, so that a rectangle around the MPP is described. The lengths of its sides depend on the amplitudes of the applied PV voltages perturbation steps.
The steady state profile generated by SOPO algorithm is also shown in Figure **2-17**b: the PV modules voltages are perturbed at the same time, so that the three-point profiles on the PV voltages generate only four states, therefore a rhomboid trajectory is exhibited. The MOPOV algorithm describes a profile that is similar to that one given by MOPOC, but on the vector variables. Consequently, all the PV voltages are perturbed at the same time with a different step amplitude depending on the magnitude and angles relation. For example, in a system with two PV modules, V_{PV1} and V_{PV2} exhibit different voltages perturbation for the same $|Vec|$ and θ perturbations, it depending on the $|Vec|$ value: Figure **2-17**b shows

that larger $|Vec|$ produces larger V_{PV1} and V_{PV2} perturbations when θ changes. Therefore, MOPOV produces concave polygonal trajectories similar to rhomboids.
In conclusion, MOPOV algorithm provides a shorter MPP trajectory than MOPOC, and MOPOV steady-state profile also encloses the MPP as SOPO and MOPOC algorithms. It is evident that the perturbation amplitudes define the power losses caused by the MPPT oscillation, as in the classical P&O approach [137], and MOPOV parameters can be designed to achieve the desired PV voltages oscillations.

2.2.3. Simulation results

To evaluate MOPOV performance in contrast with SOPO and MOPOC, a PV system with three modules was simulated considering those MPPT algorithms. The simulation considers initial PV voltages equal to $5V$ with uniform irradiance, then at $16ms$ the PV systems enter on mismatched conditions with different irradiance for all the modules. Figures **2-18**a, **2-19**a and **2-19**c show the PV voltages for SOPO, MOPOC and MOPOV algorithms, respectively, where SOPO is the faster one tracking the MPP, MOPOV is the second one and MOPOC is the slower one, as predicted in section 2.2.2.

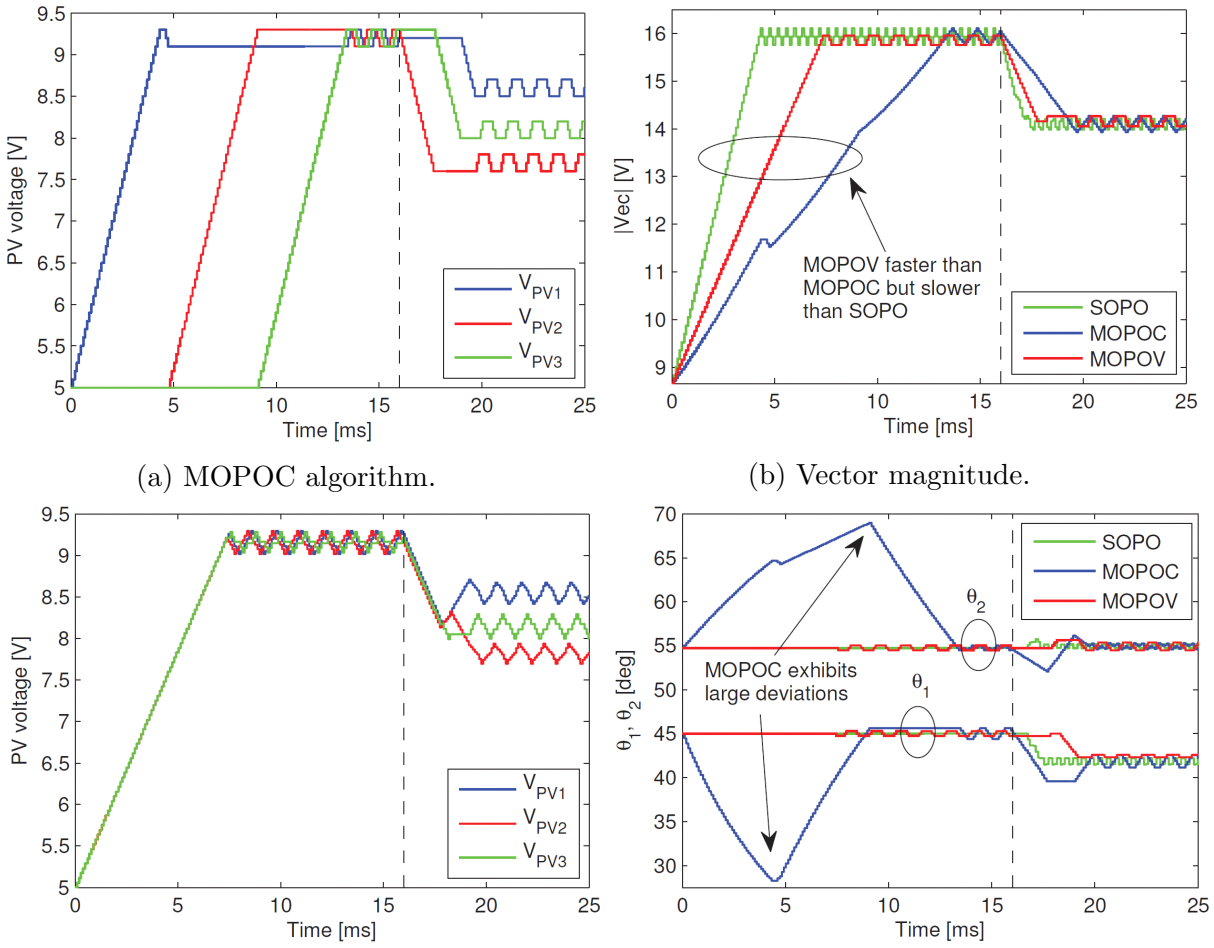


(a) SOPO algorithm.

(b) PV power profiles.

Figure 2-18.: Simulation of a 3 PV module system: SOPO algorithm and PV power profiles.

Such a behavior is confirmed by Figure **2-18**b, where the PV power profiles generated by the three MPPT algorithms are presented. The results show that SOPO solution is the one that provides more energy to the load, while MOPOC is the one that generates less energy. The proposed MOPOV algorithm produces 3.3 % less energy that SOPO algorithm, and 9.2 % more energy than MOPOC algorithm. Figure **2-18**b shows that SOPO, MOPOC and MOPOV produce the same steady-state power, which confirms that such MPPT algorithms track the MPP in both uniform and mismatched conditions.
Figure **2-19**b and **2-19**d confirm the results of the previous section: SOPO exhibits the best MPPT trajectory by optimizing the vectorial magnitude in a fast way, and tracking



(a) MOPOC algorithm.

(b) Vector magnitude.

(c) MOPOV algorithm.

(d) Vector angles.

Figure 2-19.: Simulation of a 3 PV module system.

the optimal angles. In this aspect, MOPOV was configured to start perturbing all the PV voltages in the same magnitude used for SOPO and MOPOC to provide a fair comparison. According to (2-20) [140], for any PV system where all initial PV voltages are equal, e.g. V_{pv0}, and the perturbations PV voltage are considered equal too, e.g. ΔV_{pv0}, the initial value of the vector magnitude and starting angles for the MOPOV algorithm are given in the Table **2-1**. The table reports the values up to six modules using (2-20). In the case of this simulation, $N = 3$, the starting angles are $\phi_1 = 54.74°$ and $\phi_2 = 45°$.

From Figures **2-19**b and **2-19**d it is observed that MOPOV is faster than MOPOC in the vector magnitude tracking. Similarly, the angles tracking speed provided by MOPOV is close to SOPO and much faster than MOPOC, which exhibits large deviations from the optimal values in transient conditions. Finally, MOPOV requires the same hardware than cartesian solutions, such as MOPOC, but produces more energy in transient conditions.

Therefore, the proposed MOPOV solution provides a satisfactory trade-off between imple-

mentation cost and energy production.

$$
\begin{aligned}
|Vec| &= \sqrt{V_{pvn}^2 + V_{pv(n-1)}^2 + \cdots + V_{pv2}^2 + V_{pv1}^2} \\
\phi_1 &= \arccos \frac{V_{pv1}}{\sqrt{V_{pvn}^2 + V_{pv(n-1)}^2 + \cdots + V_{pv1}^2}} \\
\phi_2 &= \arccos \frac{V_{pv2}}{\sqrt{V_{pvn}^2 + V_{pv(n-1)}^2 + \cdots + V_{pv2}^2}} \\
&\vdots \\
\phi_{n-2} &= \arccos \frac{V_{pv(n-2)}}{\sqrt{V_{pvn}^2 + V_{pv(n-1)}^2 + V_{pv(n-2)}^2}} \\
\phi_{n-1} &= \arccos \frac{V_{pv(n-1)}}{\sqrt{V_{pvn}^2 + V_{pv(n-1)}^2}}
\end{aligned}
\tag{2-20}
$$

Table 2-1.: Initial values for spherical coordinates in MOPOV algorithm.

Number of modules	$\boldsymbol{\lvert Vec_0 \rvert}$	$\boldsymbol{\phi_{1,0}}$	$\boldsymbol{\phi_{2,0}}$	$\boldsymbol{\phi_{3,0}}$	$\boldsymbol{\phi_{4,0}}$	$\boldsymbol{\phi_{5,0}}$
2	$\sqrt{2} * V_{pv0}$	45°	–	–	–	–
3	$\sqrt{3} * V_{pv0}$	54.74°	45°	–	–	–
4	$2 * V_{pv0}$	60°	54.74°	45°	–	–
5	$\sqrt{5} * V_{pv0}$	63.44°	60°	54.74°	45°	–
6	$\sqrt{6} * V_{pv0}$	65.91°	63.44°	60°	54.74°	45°

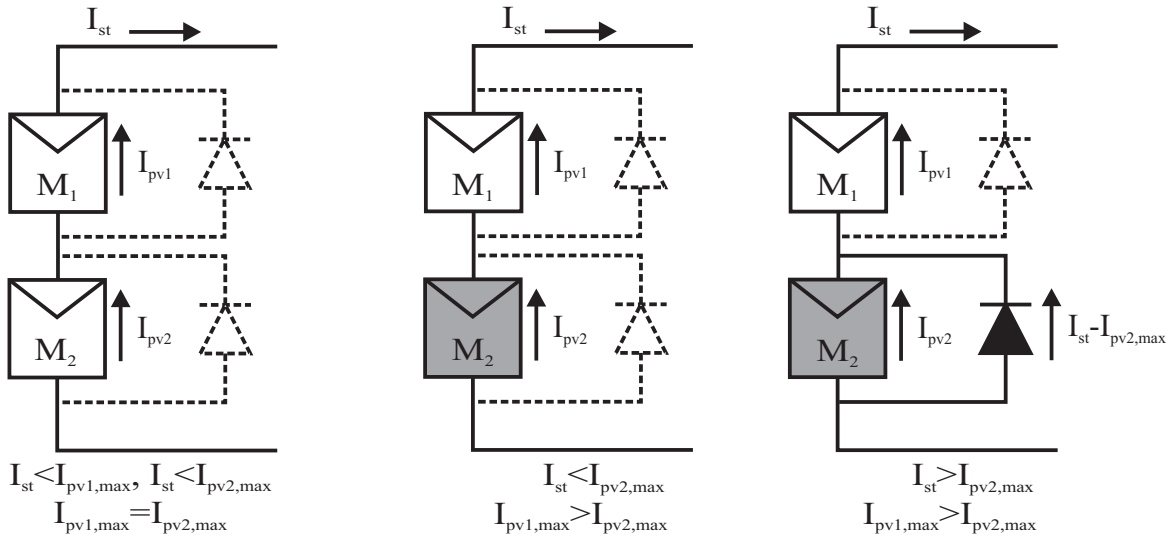
2.3. Photovoltaic array reconfiguration

This section presents another approach to mitigate the adverse effects of PV arrays operating under mismatching conditions: the dynamic electrical reconfiguration of the PV array. This section introduces a procedure to determine the best configuration of a PV array connected in a series-parallel (SP) structure without using complex mathematical models. Such a procedure uses the experimental current vs. voltage curves of the PV panels, which are composed by multiple PV modules, to construct the power vs. voltage curves of all the possible configurations to identify the optimal one. The main advantage of this method is the low computational effort required to reconstruct the power vs. voltage curves of the array. This characteristic enables one to implement the proposed solution using inexpensive embedded devices, which are widely adopted in industrial applications. The proposed method, and its embedded implementation, were tested using a hardware-in-the-loop simulation of the PV

system. Finally, the real-time operation and benefits of the proposed solution are illustrated using a practical example based on commercial devices. The results of this section were published in [127].

2.3.1. Reconfiguration of PV systems

In an SP array, multiple panels are connected in series to form strings, and the strings are connected in parallel to form the array. Considering that commercial panels are usually formed by two or more modules connected in series, a string is composed of a number of series-connected modules. Moreover, each module has a diode connected in antiparallel, named the bypass diode, which is used to protect the cells forming the module. The bypass diode provides an alternative path for the string current when a PV module is operating under mismatching conditions; thus, avoiding not only the dissipation of power in the cells of the mismatched PV module [141], but also the reduction of the current in the string [142]. Figure **2-20** illustrates the operation of the bypass diodes under uniform and mismatching conditions for a simple string of two PV modules. Under uniform conditions, the bypass diodes are reverse biased, and no current flows through them (see Figure **2-20**a). If the module M_2 is shaded, its maximum current ($I_{pv2,max}$) is lower than the maximum current of M_1 ($I_{pv2,max}$). Then, if the string current (I_{st}) is lower than $I_{pv2,max}$ (Figure **2-20**b), no current flows through the bypass diode of M_2; however, if $I_{st} > I_{pv2,max}$, the difference between I_{st} and $I_{pv2,max}$ flows through the bypass diode of M_2 to avoid the string current limitation and the power dissipation in the cells of M_2.



(a) Uniform conditions: $I_{pv1,max} = I_{pv2,max}$.

(b) Mismatching conditions: $I_{st} < I_{pv2,max}$.

(c) Mismatching conditions: $I_{st} > I_{pv2,max}$.

Figure 2-20.: Series-connected PV modules with bypass diodes under uniform and mismatching conditions.

The activation and deactivation of the bypass diodes produce multiple maximum power points in the power *vs.* voltage (P-V) curves of the PV arrays [142, 130, 49]. Therefore, if the panels in an SP PV array are organized in different ways (*i.e.*, different configurations), it is possible to obtain different P-V curves from the same PV panels involved. Moreover, one of those configurations will have a global MPP higher than the other configurations.
The classical reconfiguration of PV systems consist of modifying the electrical connections between the modules of the PV array. In SP arrays, such a procedure consists of moving, electrically, a module from one string to another one. To illustrate this concept, Figure **2-21** shows a PV array formed by two strings, St_1 and St_2, where each string is formed by two modules. Therefore, four modules (M_1–M_4) form the PV array. Such modules can be connected in three different configurations CF_1, CF_2 and CF_3, as described in Figure **2-21**. In this way, if the PV array originally operates in CF_1, the electrical connections between the modules can be modified to configure the array in CF_2 or CF_3. Such a procedure is performed using commercial controlled switches, e.g., relays or MOSFETs, which are organized in matrices to reduce the required space [143, 144].

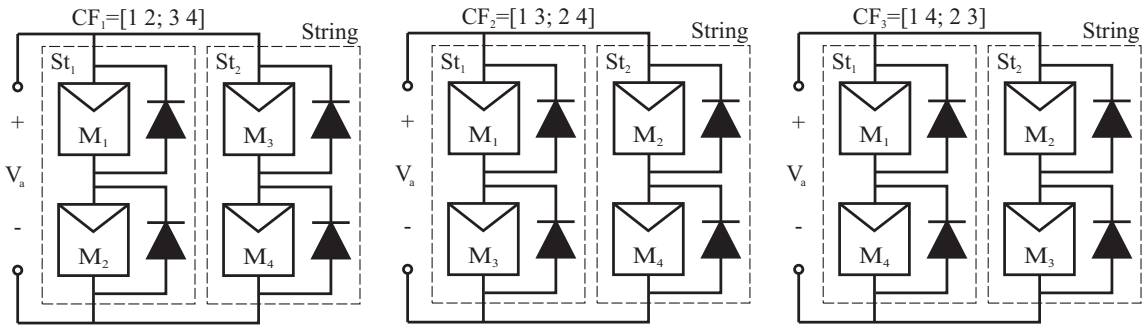


Figure 2-21.: Possible configurations of a series-parallel (SP) array with two strings of two modules each.

Figure **2-22** shows the experimental current-voltage (I-V) curves of one module from a BP 2150S PV panel [145] operating under different shading conditions. Four BP 2150S PV panels under different mismatched conditions were used to simulate the three configurations CF_1, CF_2 and CF_3, obtaining the power curves presented at Figure **2-22**: CF_1 and CF_3 produce almost the same maximum power (57.7 W at 21.84 V), while CF_2 produces 16.18 % more power (67 W at 21.47 V) just by connecting the four modules in a different way. This example puts into evidence the advantages of PV reconfiguration systems: provide higher power in comparison with static arrays; it requires simple switching elements with negligible power losses; and its cost is low in comparison with distributed maximum power point techniques that require one power converter for each PV panel (e.g., the Power optimizer from Solar Edge [146]).
A large amount of reconfiguration solutions proposed in literature, e.g. [147], are focused on structures similar to the one reported in Figure **2-21**, *i.e.*, reconfigure PV modules and

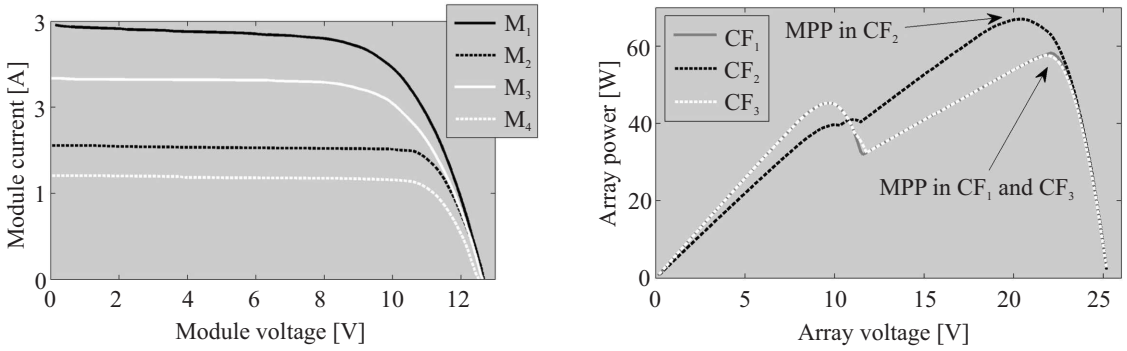


Figure 2-22.: (**a**): I-V curves of M_1, M_2, M_3 and M_4. (**b**): P-V curves of CF_1, CF_2 and CF_3.

not PV panels. However, commercial PV panels are commonly formed by two or more PV modules; hence, the reconfiguration of modules using commercial devices is not possible. Therefore, the following section proposes a procedure to reconfigure commercial PV panels based on experimental data.

2.3.2. Reconfiguration of panels based on experimental data

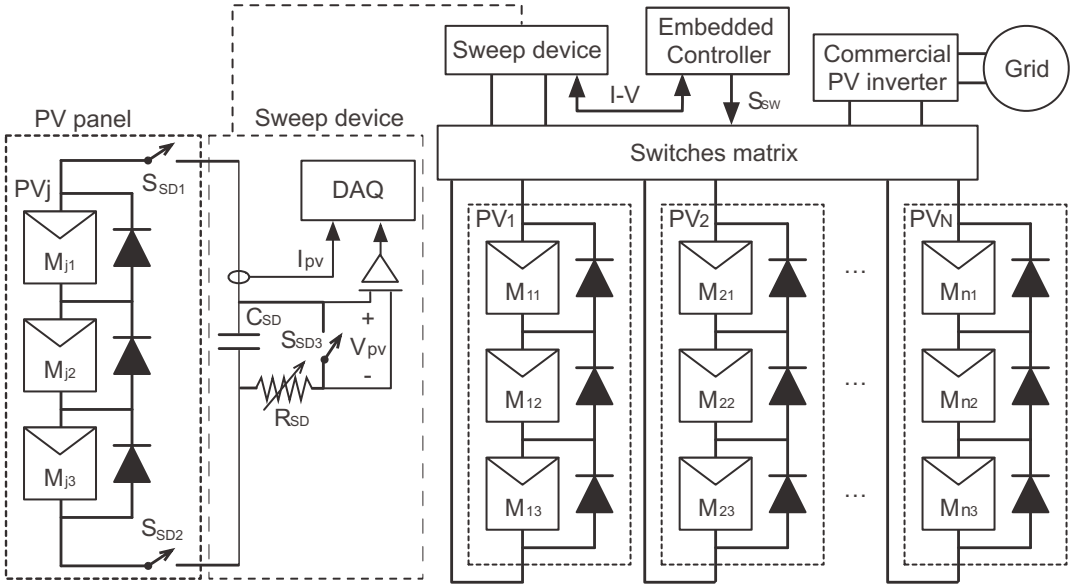
Several reconfiguration solutions are based on processing models to evaluate the array configuration that provides the highest power in the operating conditions to which the array is subjected to, e.g., [142, 148]. However, such an approach requires a large amount of calculations to estimate the maximum power of each configuration due to the complex non-linear systems required to model a PV array.

Instead, this thesis proposes to reconstruct the I-V curves of the PV array from the I-V curves of the PV panels to ensure the identification of the best configuration. Therefore, it is required to acquire the I-V curve of each panel in the array by performing a current/voltage sweep to measure both the voltage and current. This process can be done by using DC/DC converters, as reported in [149]; however, that device could be complex and costly; hence, this Section proposes a simpler solution.

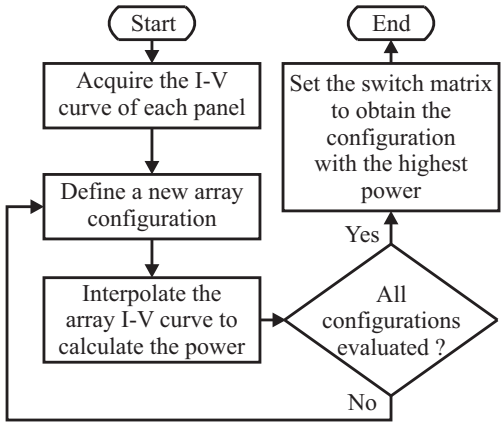
In a similar way, some commercially-available PV optimizers, designed for small PV installations (4, 8, 16 or 24 panels), acquire the I-V curve of each panel in the array for reconfiguration and monitoring purposes. This is the case of the ENDANA PV optimizer [150]. Moreover, the ENDANA device also enables disconnecting PV panels from the array for either maintenance purposes or to exclude shading panels from a PV string. Therefore, it is possible to assume that the inclusion of a device for tracing the I-V curve of each panel, and the inclusion of switches to dynamically change the array electrical connections, do not significantly degrade the economic viability of small PV installations.

2.3.2.1. Structure of the reconfiguration system

The structure of the proposed system is presented in Figure **2-23**a. It is composed of the PV panels, a switches' matrix, a sweep device, an embedded controller and a commercial PV inverter. The switches' matrix, the sweep device and the controller are described in the following paragraphs.



(a) General structure.



(b) Controller algorithm.

Figure 2-23.: Proposed reconfiguration system.

The PV panels are connected to the switches' matrix, which is implemented by a set of interconnected relays to obtain low power losses, as reported in [151, 142, 152, 150]. The switches' matrix has two main functions defined by the controller algorithm: connect each PV panel to some string of the array, and connect each PV panel to the sweep device.
The switches' matrix can be implemented in a centralized structure, as show in [151, 142],

or in a distributed structure, as proposed in [150]. In a centralized structure, each PV panel must be wired to the switches' matrix; therefore, it needs to be located close to the PV panels to avoid high ohmic losses and high installation costs caused by long cables. A distributed switches' matrix is composed of multiple units (remote units) located close to the PV panels. In this case, a set of PV panels (e.g., four PV panels in [150]) are connected to each remote unit, which is able to connect any PV panel to any string of the array or to an I-V tracing device located in a central unit as it is reported in [150]. Hence, a distributed switches' matrix reduces considerably the cabling requirements and, as a consequence, the ohmic losses and the installation costs in comparison with a centralized matrix. The design and implementation of different switches matrices are reported in [151, 142, 153, 152].
On the other hand, the circuit proposed to perform the voltage sweep (sweep device) in each panel only requires a capacitor, a set of switches, current/voltage sensors and an optional resistor to discharge the capacitor. Moreover, since the solution proposed in this section is designed to be implemented in commercial-friendly (and inexpensive) embedded controllers, the voltage/current data from each panel are acquired using analog-to-digital converters (ADC) available in most embedded devices, such as DSP or FPGA.
The structure of the sweep device is depicted in Figure **2-23**a: the capacitor C_{SD} is connected in parallel to the PV panel under test by means of the switches S_{SD1} and S_{SD2}. The capacitor C_{SD} starts discharging, since the switch S_{SD3} is closed at the beginning of the test. Then, switch S_{SD3} is set open, and the PV panel starts charging the capacitor from 0 V to the panel open-circuit voltage ($V_{OC,P}$), performing a sweep on the I-V curve. The control of the switches is performed by the embedded controller used to implement the reconfiguration algorithm. Moreover, the voltage and current data of the panel are acquired by means of ADCs available in that embedded controller. When the panel current is zero, switch S_{SD3} is closed to discharge the capacitor, so that a new test can be performed for another panel. The time required to perform a sweep of an I-V curve depends on the value of C_{SD} and on the panel current. Therefore, the longest sweep time is obtained at the lower irradiance condition. With the aim of providing an equation for the time required to perform the voltage sweep, the ideal single-diode model [154], given in (2-21), is used. Taking into account that the PV current charges the capacitor, which in turn defines the PV voltage, the differential equation given in (2-22) describes the evolution of the PV voltage.

$$i_{pv} = i_{SC} - A \cdot \exp\left(B \cdot v_{pv}\right) \tag{2-21}$$

$$\frac{d\, v_{pv}}{dt} = \frac{1}{C_{SD}} \cdot \left[i_{SC} - A \cdot \exp\left(B \cdot v_{pv}\right)\right] \tag{2-22}$$

Solving (2-22) requires numerical methods and the identification of the parameters of the PV model; therefore, an estimation of the capacitor charge time is obtained by considering a PV current equal to $I_{SC,min}$, which corresponds to the minimum short-circuit current to be tested. Under the light of such an assumption, the time required to perform a voltage sweep

T_{SD} is approximated by (2-23). It must be highlighted that (2-23) must be used for selecting the value of C_{SD} and to set the acquisition time of the ADCs in the embedded controller.

$$T_{SD} = \frac{C_{SD} \cdot V_{OC,P}}{I_{SC,min}} \tag{2-23}$$

The discharge of the capacitor C_{SD} can be done by means of an additional resistor R_{SD} when switch S_{SD3} is closed. The design of R_{SD} depends on the desired discharge time T_{dis} and minimum C_{SD} voltage δv_{pv} accepted to start a new test, as given in (2-24). A fast discharge can be imposed by reducing R_{SD} (even to a short-circuit) at the expense of increasing the stress in C_{SD}. However, C_{SD} can be implemented with a parallel array of multiple smaller capacitors to reduce the stress in each individual capacitor and, at the same time, to increase the reliability of the sweep device.

$$R_{SD} = -\frac{T_{dis}}{C_{SD} \cdot \ln\left(\delta v_{pv}/V_{OC,P}\right)} \tag{2-24}$$

Each panel of the PV array must be sequentially connected to the sweep device to obtain the I-V curve of all of the PV panels. Therefore, the time T_{sweep} required to acquire all of the I-V curves is given in (2-25), where M stands for the number of strings in the array and N stands for the number of panels in each string; hence, $N \cdot M$ represents the number of panels in the array. Moreover, T_{SW} represents the time required to open and close switches S_{SD1}, S_{SD2} and S_{SD3} in the following sequence: S_{SD1} and S_{SD2} are closed, and S_{SD3} is open at the same time of performing the voltage sweep, while S_{SD1} and S_{SD2} are open and S_{SD3} is closed at the same time to discharge the capacitor. Therefore, T_{SW} is equal to the time required to open and close a single switch. It must be clarified that S_{SD1} and S_{SD2} are part of the switches' matrix associated with each panel; hence, the connection to the sweep device is considered as an additional string in the switches' matrix.

$$T_{sweep} = (N \cdot M) \cdot (T_{SD} + T_{dis} + T_{SW}) \tag{2-25}$$

Finally, the embedded controller has two main functions: first, it processes the reconfiguration algorithm; and second, it coordinates the operation of the switches' matrix to set the new configuration and to trace the I-V curve of all of the panels using the sweep device. The controller algorithm is described in the flowchart of Figure **2-23**b. It starts acquiring the I-V curve of all of the PV panels, then it defines an array configuration and use interpolation to generate the array I-V curve to identify the global maximum power point (GMPP). Such a process is repeated for all of the possible configurations to identify the one that provides the highest GMPP (best configuration). Subsequently, the embedded controller defines the state of each switch (open/closed) in the switches' matrix to set the best configuration in the PV

array. This process is done using digital signals wired to the switches' control inputs. The vector S_{SW} represents those signals in Figure **2-23**a.
The following subsections describe in detail the process to trace the I-V curve of each configuration, illustrating it with an application example.

2.3.2.2. Evaluation of possible array configurations

To select the array configuration that produces the highest power, all of the possible options must be tested. Since, in general, every panel must be able to be connected to any string, the number of possible configurations (NCF) is given by the combination of all of the PV panels ($M \cdot N$) and the number of panels in each string (N), as shown in (2-26).

$$NCF = \frac{(M \cdot N)!}{N!(M \cdot N - N)!} \tag{2-26}$$

Such a number grows exponentially for increments in the number of panels. For example, a PV array formed by two strings of four panels ($N = 4$ and $M = 2$) has 35 possible configurations, while a PV array formed by two strings of twelve panels ($N = 12$ and $M = 2$) has 1,352,078 possible configurations. Since the common approach in the literature is to use models to evaluate the effectiveness of a given configuration, e.g., [155, 156, 157, 158], the evaluation of all of the possible configurations is a slow process. Hence, some algorithms have been proposed in the literature to search the best configuration without evaluating all of the possibilities, e.g., [159, 160]; however, it is not easy to find a solution that ensures, by means of an analytical proof, that it reaches the optimal configuration. Therefore, the solution proposed in this section is focused on a different approach: reduce, as much as possible, the time required to evaluate each configuration, which eventually reduces the time required to test all of the possible options. It is clear that testing all of the possibilities ensures the detection of the best configuration.
To speed-up the evaluation of each configuration, complex optimization algorithms and non-linear models must be avoided. Therefore, the proposed solution constructs the array I-V curve from the interpolation of the experimental data measured from the panels using few multiplications and additions, as illustrated in Figure **2-24**: the I-V curve of each string is obtained by adding the voltage generated by the corresponding panels for the same current. This process requires the interpolation of the panel voltage if the requested current does not correspond to a current value measured by the sweep device.
Similarly, the I-V curve of the array is obtained by adding the current of each string generated at the same voltage. In this case, the interpolation of the string current is required if the requested voltage does not correspond to a voltage value available in the string data. Since commercial PV inverters have limitations in terms of input voltage, *i.e.*, minimum and maximum array voltage, the array I-V curve is constructed only within that range, which reduces the amount of data required to evaluate.

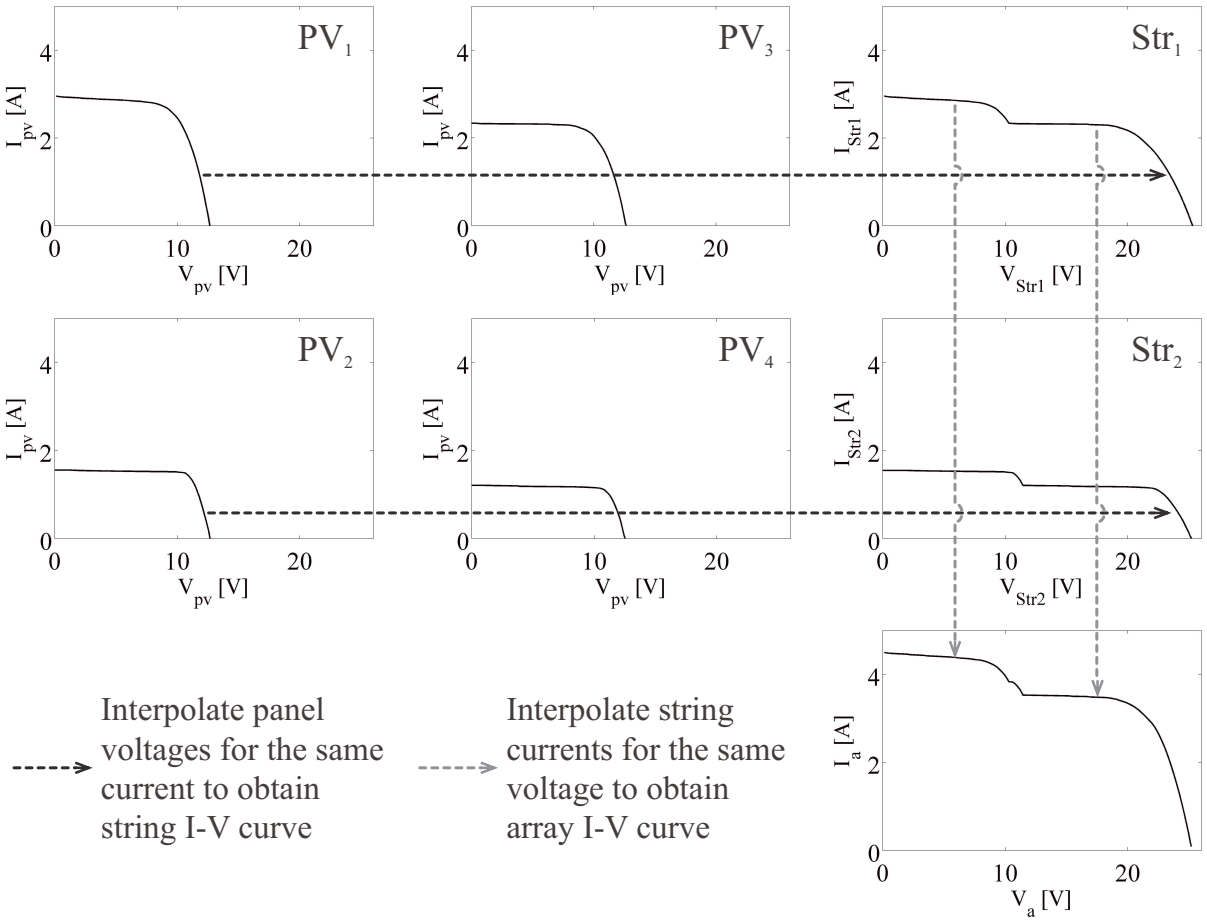


Figure 2-24.: Example of the interpolation procedures to construct the I-V curve of one configuration for an SP array with two strings of two modules each.

It is worth noting that the interpolation process is not required to evaluate all of the points of the string I-V curve, since some panels could exhibit the same current values for part of the curve. Similarly, if the voltages of the strings I-V curve match, no interpolation is required to construct the array I-V curve.

The interpolation of a single value requires four additions, one division and one multiplication as reported in (2-28). The division instruction is included in the instructions set architecture (ISA) of some high-level processors; however, other simpler processors require implementing the division using multiplication instructions. Hence, the six floating-point instructions described in (2-28) must be mapped to fixed-point and float-point instructions in the assembler, including data movement between registers and memory, additions, subtractions, data shift, logic operations, among others [161].

$$m = \frac{y_3 - y_1}{x_3 - x_1} \tag{2-27}$$

$$y_2 = m \cdot (x_2 - x_1) + y_1 \tag{2-28}$$

To estimate the processing time of the reconfiguration algorithm, it is necessary to take into account all of the data points in each I-V curve, the number of panels in each string, the number of strings in the array and the number of possible configurations of the array. Since the reconfiguration algorithm includes both fixed and float point instructions, the performance of the algorithm cannot be measured in instructions; instead, it must be measured in clock cycles. This is because the number of clock cycles required by one fixed-point instruction is, in general, different from the number of clock cycles required by one floating-point instruction.
Nevertheless, to accurately estimate the processing time of the reconfiguration algorithm, it would be necessary to take into account the number of clock cycles required by other sub-processes in the embedded system: function invocation, handle vectors, decision instructions, control flow, communications, among others. However, the number of clock cycles of those sub-processes depends on the technology used to implemented the algorithm, which makes difficult the construction of a closed mathematical expression for the processing time. Therefore, an accurate evaluation of the processing time required by the reconfiguration algorithm, in therms of clock cycles, should be performed experimentally. This procedure is illustrated in the example presented in Section 2.3.4.

2.3.2.3. Application example based on commercial devices

To illustrate the proposed reconfiguration solution, a PV installation based on the commercial PV inverter Sunny Boy 1200 [162] is assumed. Such an inverter has a nominal DC voltage $V_{DC\_nom} = 120$ V, maximum DC voltage and current values equal to 400 V and 12.6 A, respectively, and minimum DC voltage equal to 100 V. The installation uses the commercial PV panels BP-3155 from British Petroleum [163], which are formed by three modules. Each PV panel has nominal MPP voltage (V_{mpp}) and MPP current (I_{mpp}) equal to 34.9 V and 4.5 A, respectively. Hence, to match the nominal requirements of the PV inverter, the PV array must be constructed using two strings of four panels each (eight panels, 24 modules), resulting in operation voltage and current equal to 139.6 V and 9 A, respectively.
Figure **2-25** shows, at the top left, the I-V curves of the eight PV panels, which are based on the experimental I-V curves of BP 2150 PV panels [145] subjected to a solar irradiance equal to 625 W/m^2. The PV_1 panel is non-shaded; hence, its three modules exhibit the same electrical characteristics. The panel PV_8 is uniformly shaded; hence, its three modules also exhibit the same electrical characteristics. Instead, the modules PV_2–PV_7 are non-uniformly shaded; therefore, the I-V curves of such panels describe irregular electrical characteristics due to the activation of the bypass diodes of some modules.

Using samples of such I-V curves, the algorithm tests all possible configurations following the control algorithm given in Figure **2-23**b. Such a procedure detects the following configuration as the best (CFB): first string as $[PV_1\ PV_2\ PV_3\ PV_6]$ and second string $[PV_4\ PV_5\ PV_7\ PV_8]$. That configuration provides 370.1 W at an array voltage $V_a = 110$ V, which is within the operation range of the PV inverter. To illustrate the power increment achieved by the proposed solution, the worst configuration (CFW) for this PV installation is given by the strings $[PV_1\ PV_2\ PV_3\ PV_7]$ and $[PV_4\ PV_5\ PV_6\ PV_8]$, providing 313.2 W at an array voltage $V_a = 135$ V. It is worth noting that the difference between CFB and CFW is only in the permutation of PV_6 and PV_7, but such a modification generates a difference of $\Delta\eta = 18.14\,\%$ in the power production. Similarly, if the default configuration of the array is different from CFB, the proposed reconfiguration system will optimize the panels' connections to improve the power delivered to the inverter, which eventually reduces the return-of-the-investment time by increasing the energy produced.

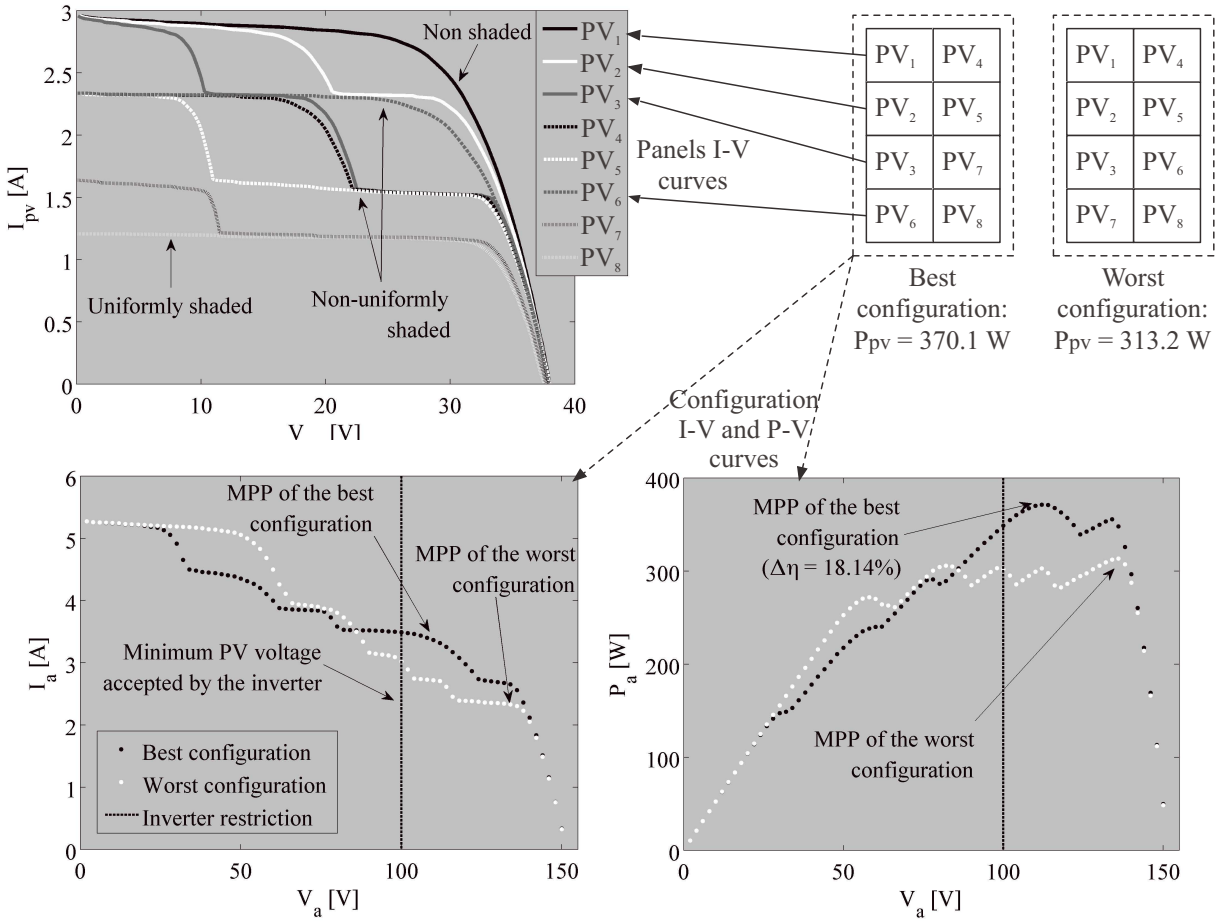


Figure 2-25.: Best and worst configurations for the application example.

2.3.3. Simulation platform implementation using commercial devices

With the aim of illustrating the performance of the PV array reconfiguration system, a hardware-in-the-loop (HIL) simulator was used to test the proposed solution implemented on a practical embedded device. HIL simulation was used because it ensures the same irradiance and shading conditions for multiple experiments [164], which is not possible using PV panels due to the variability of the solar irradiance. Moreover, the HIL simulator enables one to test the behavior of the proposed reconfiguration solution implemented on a real embedded device to reproduce the conditions of a real commercial deployment.

The proposed simulation platform is illustrated in Figure **2-26**. This platform is composed of two main blocks: the HIL simulator and the embedded device processing the reconfiguration solution. The first block (HIL) emulates the PV system, and it is implemented in Simulink Desktop Real-Time (SDRT) [165]. This HIL simulator processes the models of the PV array (composed of two strings of four PV panels each, *i.e.*, 4×2), the switches' matrix, a DC/DC boost converter to perform the maximum power point tracking (MPPT) and the load. The second block is the embedded controller implemented on a DSP TMS320F28335 from Texas Instruments, which processes both the proposed reconfiguration algorithm and the MPPT technique.

The PV array is implemented in the HIL using a Matlab® function based on a database of the I-V curves of the different configurations for each shading condition. The PV array function receives two parameters: the configuration defined by the switches' matrix and the operating voltage imposed by the power converter; moreover, it provides the array current according to the array I-V curve. Similarly, the switches' matrix is implemented using a Matlab® function that receives a vector with the state of all of the switches (S_{SW}) from the embedded controller, and it provides the configuration to the PV array function. The power converter is implemented using the ideal state-space average model on an S-function. Its input current is provided by the PV array function, while the duty cycle is provided by the embedded controller. Finally, the power converter imposes the voltage to the PV array, and it delivers the generated power to a resistive load.

The PV system emulator and the embedded controller exchange information using an RS-232C channel instead of discrete analog and digital signals. This structure enable one to reduce the wiring between the two devices without impacting the validity of the experiments, since the same information is transferred: the reconfiguration algorithm, on the embedded device, sends the optimal configuration of the array to the switches' matrix of the PV system; while the PV system sends the current and voltage of the PV array to the embedded system, which are used by the MPPT technique (implemented in the controller) to update the duty cycle of the Boost converter implemented in the HIL simulator. The adopted MPPT algorithm is the perturb and observe (P&O) [166]. It is worth noting that the P&O may be trapped in a local MPP or in the global MPP depending on the starting point (initial duty cycle) after a new configuration is set by the switches' matrix [151].

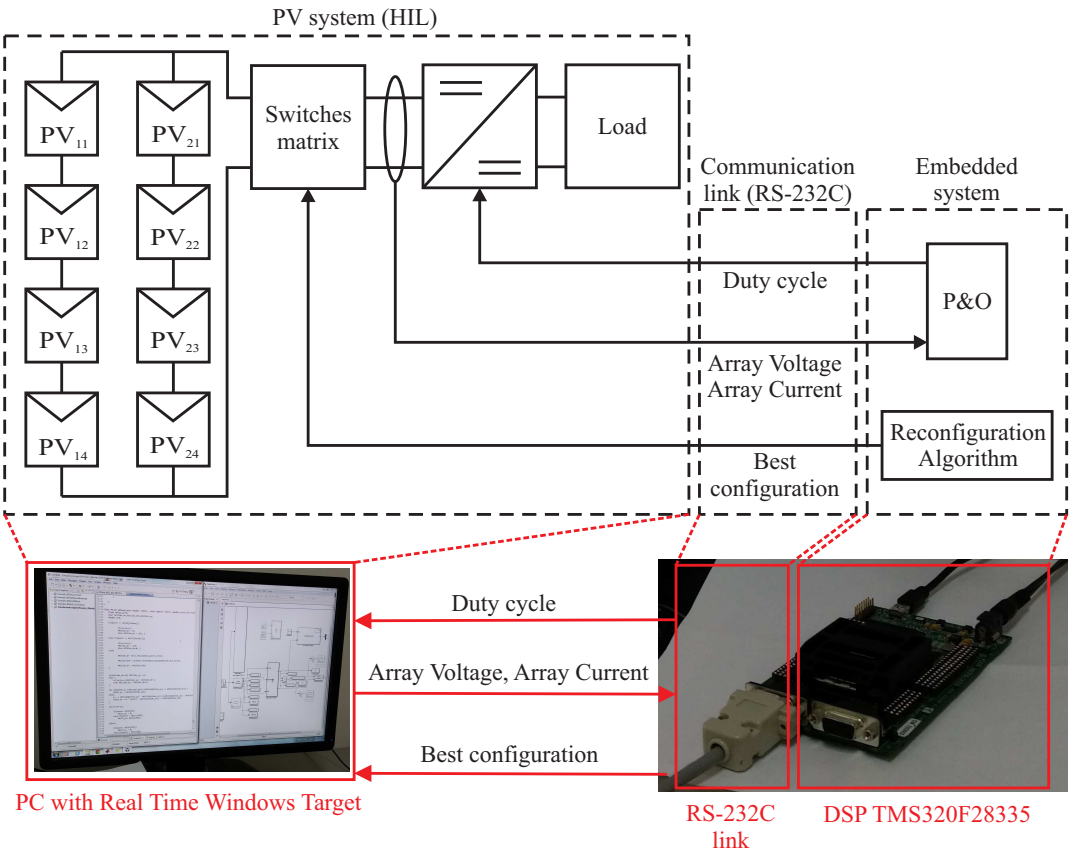


Figure 2-26.: Block diagram and hardware implementation of the proposed simulation platform.

The HIL system is processed in a Dell precision T7600 workstation with the following characteristics: processor Intel Xeon E5-2667 of 2.9 GHz, 32 GB of RAM memory, one COM Intel C600/X79 and a real-time operation imposed by the SDRT. The embedded device, TMS320F28335 DSP [167], used to implement both reconfiguration and MPPT algorithms has the following characteristics: CPU of 32 bits of 150 MHz, IEEE-754 single-precision floating-point unit (FPU) with 150 MIPS, 68 kB RAM memory, 512 kB Flash memory, 18 PWM channels with high resolution, 12-bit 12.5 MSPSADC and serial connectivity (three UART, one SPI, one I2C, one CANand one McBSP).

The sequence diagram in Figure **2-27** describes the run-time interaction between the PV system emulator and the embedded controller. The controller has four main software objects: *Timer*, *Reconfiguration*, *Linear Interpolation* and *P&O*; while the emulator has three main objects: *PV array*, *Switches Matrix* and *DC/DC Converter*.

The simulation starts with the *Reconfiguration* object sending the state of all the switches to the *Switches Matrix* object with the message *SetupCfg(0)* to set the initial configuration of the PV array. From such information, the *Switches Matrix* determines the array configuration to be set in the PV array by the message *PVarrayCfg(0)*. Then, an infinite loop (*loop*

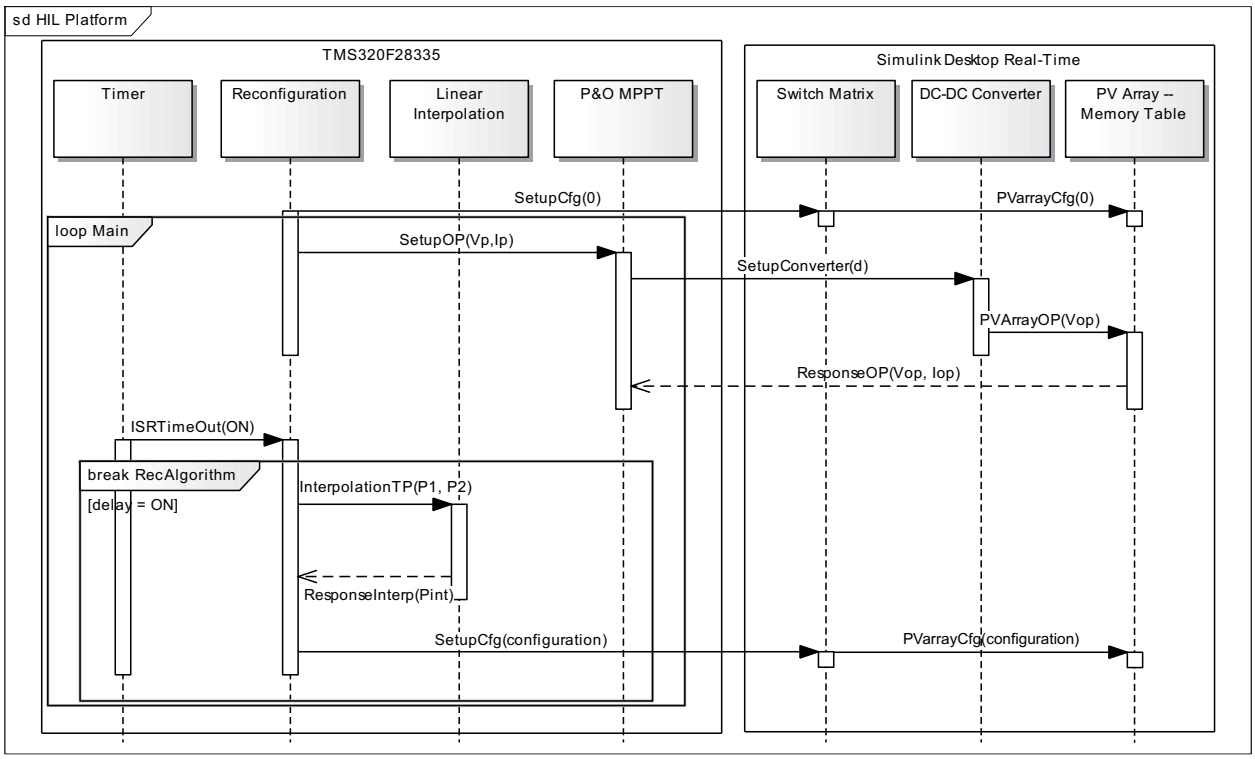


Figure 2-27.: Sequence diagram of the simulation platform.

Main) starts on the controller, where *Reconfiguration* calculates the optimal voltage (*Vp*) and current (*Ip*) for the actual configuration and operating condition. Later, *Reconfiguration* sends a message (*SetupOP(Vp,Ip)*) to *P&O* to set the starting point of the *P&O* algorithm close to the global MPP. This is why the proposed structure enables the classical *P&O* algorithm to overcome the multi-maximum problem present in mismatched PV arrays. This is a major advantage over classical PV systems with no updated information about the approximated position of the global MPP.

Once *Vp* is received by P&O, it calculates the duty cycle of the *DC/DC Converter* (*d*), required to set the PV array voltage (*Vop*). Then, that duty cycle is set to *DC/DC Converter* using message *SetupConverter(d)*. The *DC/DC Converter* sets the operating voltage (*Vop*) to the *PV Array* using *PVArrayOP(Vop)* message. The PV array function returns the operating voltage and current (*Vop,Iop*) to the P&O obtained with *d* using message *ResponseOP(Vop,Iop)*. Again, the P&O uses *Vop* and *Iop* to calculate a new duty cycle in order to track the closest MPP.

The *Timer* is configured to set the variable *delay* to *ON* every 90 s to start *break RecAlgorithm*, which executes the reconfiguration algorithm. When an interpolation is required within the reconfiguration algorithm, *Reconfiguration* sends the two points (*P1* and *P2*) to the *Linear Interpolation* using *InterpolationTP(P1,P2)*, which replies with the interpolated point (*Pint*) using *ResponseInterp(Pint)*. Once the optimal configuration (*configuration*) has

been determined, the reconfiguration algorithm ends by sending the state of all of the switches to the *Switches Matrix* using the *SetupCfg(configuration)* message. Finally, the *Switches Matrix* sets the best configuration to the PV array (*PVarrayCfg(configuration)*). It is worth noting that while the reconfiguration algorithm is running, the P&O algorithm does not run; therefore, the converter duty cycle remains constant for that period of time.
It must be highlighted that both reconfiguration and MPPT algorithms are processed by the TMS320F28335 DSP; hence, that embedded device could be used without modifications in a real application (commercial deployment). In that case, the HIL simulator will be replaced by the real PV panels, the switches' matrix and the power converter.

2.3.4. Simulation results based on experimental data

This section presents a practical example to illustrate the real-time operation of the proposed reconfiguration system running in the deployment-ready embedded device TMS320F28335 DSP.
The PV array considered for the simulations is composed of two strings of four panels each ($N = 4$ and $M = 2$), which has 35 possible configurations that should be evaluated to find the best one for a given shading condition. The time delay between two consecutive executions of the reconfiguration algorithm ($t_{reconfig}$) was set to 90 s, because one run of the reconfiguration algorithm takes around 36 s; moreover, in some cases, the PV power variability can be up to 60 % in 60 s, as reported in [168]. However, it is worth noting that the PV power variability also depends on the area occupied by the PV array, the geometry of that area, the velocity of the clouds, fast objects' movement around the array (animals, bird droppings), *etc.*

2.3.4.1. Simulated shading conditions

Four different shading conditions (SC) were simulated to illustrate the performance of the proposed reconfiguration system. Each SC is generated from different I-V curves of the eight PV panels that form the array; then, the I-V curve of the PV array is generated by using the interpolation process described in Section 2.3.2.2.
The description of each (SC) is given bellow, and the P-V curves of the eight PV panels for each condition are illustrated in Figure **2-28**.

- Condition No. 1 (SC_1: PV_1, PV_6 and PV_8 are uniformly shaded; hence, they have a single MPP. PV_2, PV_4, PV_5 and PV_7 have one shaded module (*i.e.*, two MPPs), while PV_3 has two partially-shaded modules (*i.e.*, three MPPs).

- Condition No. 2 (SC_2): PV_6 and PV_7 have, each, two shaded modules, while the others panels have one shaded module.

- Condition No. 3 (SC_3): PV_5 and PV_8 are uniformly shaded; moreover, PV_1, PV_2, PV_3 and PV_7 have one shaded module, while PV_4 and PV_6 have two shaded modules.
- Condition No. 4 (SC_4): PV_1, PV_5 and PV_7 are uniformly shaded. PV_2, PV_3, PV_4, PV_6 and PV_8 have one shaded module.

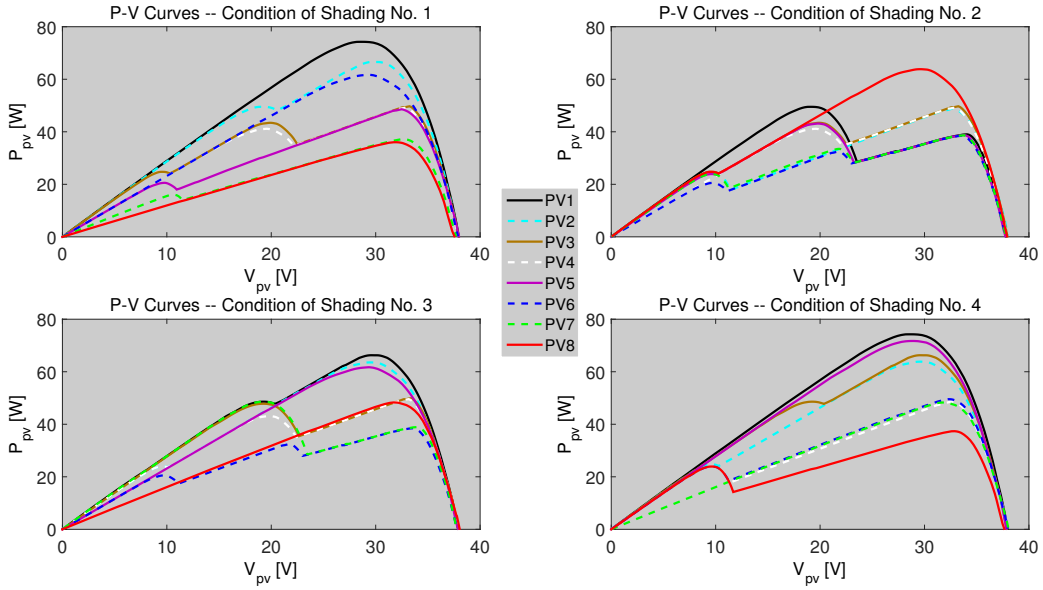


Figure 2-28.: P-V curves of the PV panels for the shading conditions.

The array P-V curves for the best and worst configurations for each SC are shown in Figure **2-29**. Note that each P-V curve has multiple local MPPs and one global MPP; however, the global MPP of the best configuration is significantly higher than the global MPP of the worst configuration.
The numerical values of the global MPPs of both the best and worst configurations for each SC are shown in Table **2-2**. That table also reports the increment in the power production with respect to the worst configuration. Finally, the electrical connections between the PV panels for the best and worst configurations are shown in Table **2-3**.
Table **2-3** also reports two additional configurations: *Initial with RA* (RA stands for, reconfiguration algorithm) (CF_0) and *Without RA* (CF_{18}). *Initial with RA* corresponds to the initial configuration set in the emulation system for the dynamic simulation of the reconfiguration system presented in Subsection 2.3.4.3. *Without RA* corresponds to the configuration set in the emulation system for the dynamic simulation of the classical (static) PV system presented in Subsection 2.3.4.5.

2.3.4.2. Sampling time and time delay of the sweep device and switches

The TMS320F28335 DSP has a fast 12-bit ADC capable of sampling an analog signal at

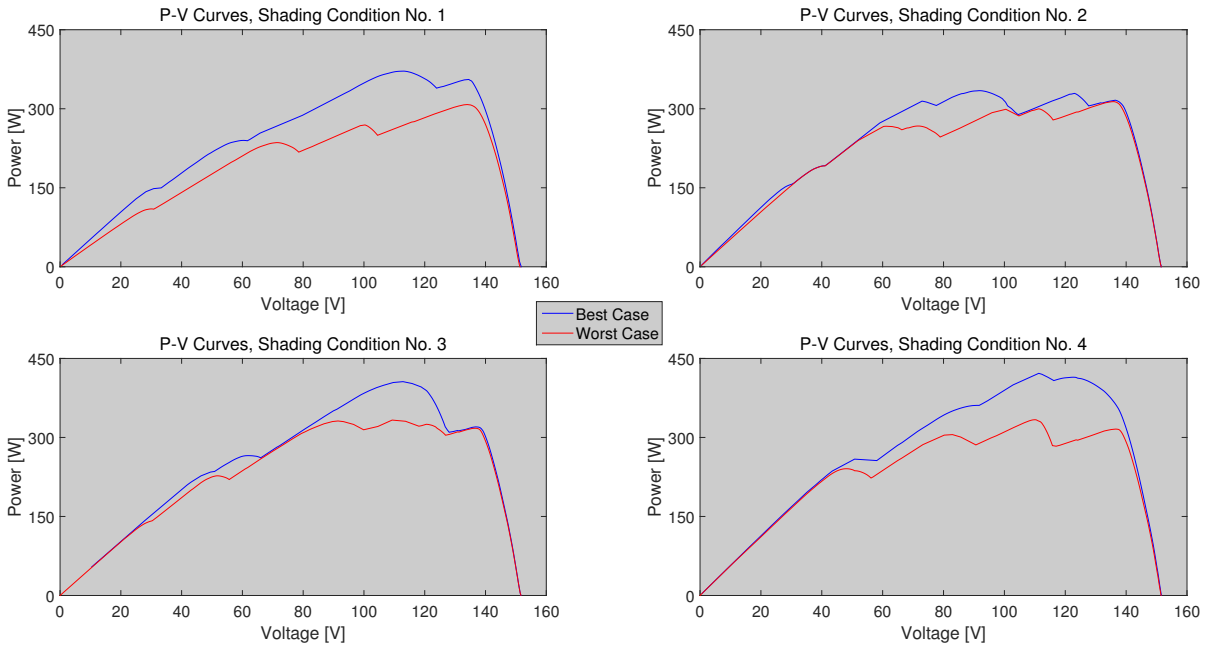


Figure 2-29.: Array P-V curves for best and worst configurations for each shading condition.

Table 2-2.: Information of the best and worst configuration of the PV array for each shading condition.

Shading condition	**Best configuration**		**Worst configuration**		**Power increment**	
	Number	**Power (W)**	**Number**	**Power (W)**	**(W)**	**(%)**
1	8	371.426	13	304.982	66.444	21.8
2	14	334.356	31	313.522	20.834	6.6
3	22	405.929	28	332.975	72.953	21.9
4	4	421.665	13	333.620	88.045	26.4

$12.5MHz$ ($80ns$ conversion time). However, since a single ADC is available to acquire two signals (PV voltage and current), those signals could be sampled at a maximum frequency of $6.25MHz$, which remains very fast.

To define the sampling frequency for tracing the I-V curves, the following conditions must be taken into account: first, the time required to trace the I-V curve depends on the sweep device capacitor C_{SD}, as given in (2-23); second, the number of samples per curve must enable an accurate reproduction of the I-V curve without overloading the DSP memory. Those conditions are addressed below.

Considering a minimum short-circuit current of $1A$ for this example (as depicted in Figure **2-25**) and a maximum open-circuit voltage equal to $38V$, the sweep device capacitor $C_{SD} = 39$ μF is calculated from (2-23) to ensure a maximum sweep time equal to 1.5 ms. Those

Table 2-3.: Configurations used in the simulations: RA, reconfiguration algorithm; SC, shading condition.

Configuration	Order of PV panels	Description
CF_0	$[PV_1\ PV_2\ PV_3\ PV_4; PV_5\ PV_6\ PV_7\ PV_8]$	Initial with RA
CF_4	$[PV_1\ PV_2\ PV_3\ PV_5; PV_4\ PV_6\ PV_7\ PV_8]$	Best for SC_4
CF_8	$[PV_1\ PV_2\ PV_3\ PV_6; PV_5\ PV_4\ PV_7\ PV_8]$	Best for SC_1
CF_{13}	$[PV_8\ PV_2\ PV_3\ PV_4; PV_5\ PV_6\ PV_7\ PV_1]$	Worst for SC_1 and SC_4
CF_{14}	$[PV_1\ PV_8\ PV_3\ PV_4; PV_5\ PV_6\ PV_7\ PV_2]$	Best for SC_2
CF_{18}	$[PV_1\ PV_5\ PV_6\ PV_4; PV_2\ PV_3\ PV_7\ PV_8]$	Without RA
CF_{22}	$[PV_1\ PV_2\ PV_5\ PV_7; PV_3\ PV_6\ PV_4\ PV_8]$	Best for SC_3
CF_{28}	$[PV_6\ PV_8\ PV_3\ PV_4; PV_5\ PV_1\ PV_7\ PV_2]$	Worst for SC_3
CF_{31}	$[PV_1\ PV_2\ PV_6\ PV_8; PV_5\ PV_3\ PV_7\ PV_4]$	Worst for SC_2

values provide an acceptable trade-off between capacitor size, cost and time delay. Other capacitors and sweep times can be adopted taking into account the following conditions: larger capacitors will require larger time delays, which in turn increases the reconfiguration time and capacitor cost; while smaller capacitors enable one to reduce the reconfiguration time; however, higher sampling frequencies and shorter processing times are required to acquire the I-V curve data.

The commercially available capacitor MKT1820639015 fulfills the requirements of capacitance and maximum voltage for this application (39 μF, 63 V). Another option is to implement C_{SD} using multiple capacitors in parallel to improve the system reliability. In that case, three capacitors MKT1820615015 (15 μF, 63 V) can be used in parallel to provide a much higher maximum current derivative, so that the capacitors stress is reduced. However, this last solution increases the cost of the sweep device. To discharge the capacitor C_{SD} without a significant stress, the additional resistor $R_{SD} = 8.25\ \Omega$ is calculated from (2-24) to ensure a maximum discharge time $T_{dis} = 1.5$ ms. Resistor R_{SD} must support a maximum instantaneous power $R_{SD} \times (I_{SC.max})^2 = 3$ W, where $I_{SC.max} = 5$ A is the maximum short-circuit current possible in the adopted PV panels. The commercially-available resistor 83F8R25 fulfills those conditions.

Taking into account that a PV curve must be acquired for each PV panel and a PV curve must be constructed for each string and the array, those PV curves are defined to have 160 samples each, so that the DSP memory is not overloaded. Since the PV curves are acquired in $1.5ms$, the sampling frequency of each channel of the ADC is set to $110kHz$.

Another time delay present in the hardware of the reconfiguration system concerns the switches' operation. To provide an inexpensive solution, general purpose electro-mechanical relays, such as the G5LE-1A4-DC24, can be adopted. Those types of relays have an average operation time of 15 ms. Based on the previous time delays of the sweep device and switches, the total time required to acquire all the PV panels I-V curves is calculated from (2-25)

as T_{sweep} = 264 ms. Moreover, each reconfiguration cycle requires opening and closing, simultaneously, some relays in the switches' matrix to set the new configuration; therefore, an additional 15 ms delay is imposed by the switching matrix. Finally, the time required by the hardware of the reconfiguration system is 279 ms for each reconfiguration cycle.

2.3.4.3. Dynamic simulation of the reconfiguration system

A dynamic simulation of the proposed reconfiguration system was carried out considering the PV array operating under the four different shading conditions described in Subsection 2.3.4.1. The simulation results are presented in Figure **2-30**a: the plots at the top and center correspond to the power and voltage of the PV array, respectively, while the plot at the bottom reports the shading condition (SC) and the time intervals in which the reconfiguration algorithm (RA) is running (Run) and stopped (Stop). Moreover, the black dashed lines illustrate the instants in which a run of the reconfiguration algorithm finishes, while the purple dashed lines report the instants in which the shadowing conditions change.

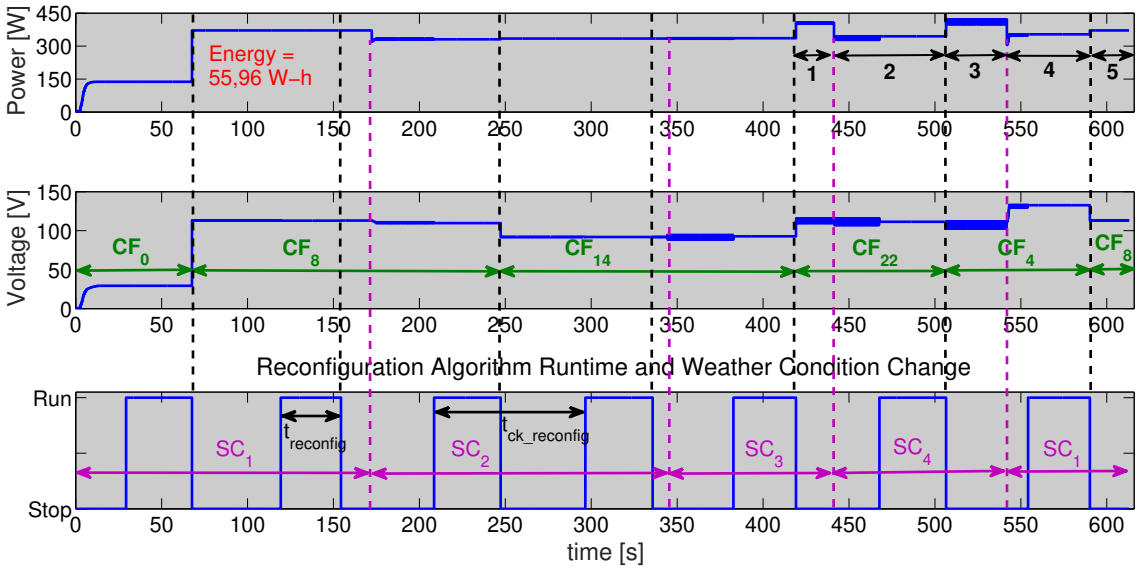
The simulation starts with the PV array in Configuration 0 (CF_0 in Table **2-3**) under the shading condition No. 1 (SC_1), where the P&O algorithm tracks an MPP around 40 V obtaining a power of 150 W. At 29.3 s, the RA starts, and it takes 33.4 s (*i.e.*, $t_{reconfig}$ = 33.4 s) to find the best configuration, which, in this case, is CF_8. Such a configuration is set by the switches' matrix at 67.88 s (including the 279-ms delay of the hardware) to produce a significant increment of 147 % in the PV array power (from 150 W to 371 W).

It is observed that each time the RA ends (black dashed lines), the PV power is increased or remains constant, depending on the existence of a change of the shading conditions. Moreover, each time the shading condition changes, there is a reduction in the PV array power, which means that the array configuration must be optimized again.

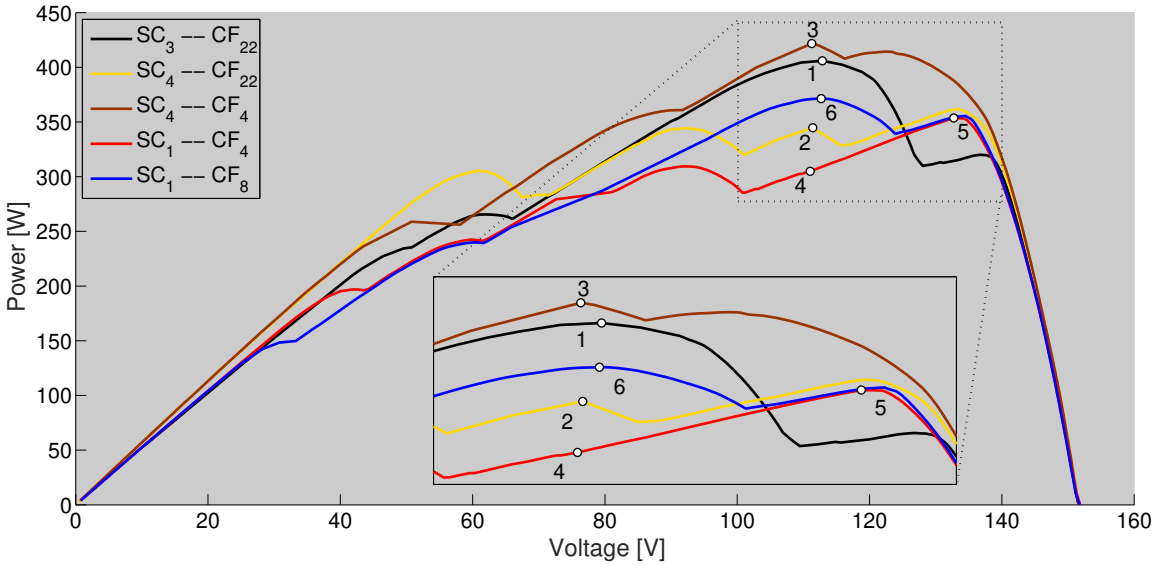
As explained at the beginning of Section 2.3.4, the time period selected to run the RA consecutively is 90.0 s (*i.e.*, $t_{ck\_reconfig}$ = 90.0 s); therefore, at 119.3 s, the RA starts again with $t_{reconfig}$ = 37.2 s. At that time, the shading conditions have not changed; hence, there is no change in the configuration of the PV array and, as consequence, no change in the PV array power and voltage occurs.

The first change in the shading conditions, from SC_1 to SC_2, is produced at 172.3 s, which leads to a reduction in the PV array power and voltage. Then, the RA starts at 208.5 s, with $t_{reconfig}$ = 36.2 s, obtaining that the best configuration for SC_2 is CF_{14} (see Table **2-3**). CF_{14} is set at 247.56 s, producing a small increase in the PV power (1 %) and a reduction in the PV voltage. Such a reduction shows that the voltage of the global MPP for CF_{14} under SC_2 is lower than the global MPP voltage for CF_8 under the same shading profile. The RA runs again between 296.6 s and 335.7 s ($t_{reconfig}$ = 38.4 s); however, the configuration does not change since the shading condition is the same (SC_2).

The shading condition changes again at 344.3 s, this time from SC_2 to SC_3. Therefore, after the subsequent run of the RA, the new optimal configuration CF_{22} is set at 419.38 s



(a) Dynamic behavior of PV array power, voltage and reconfiguration algorithm runtime.



(b) Operating points in the P-V curves from 430 s.

Figure 2-30.: Behavior of the PV array with the proposed reconfiguration algorithm.

($t_{reconfig}$ = 37.6 s + hardware delay of 279 ms). Once again, the change in the configuration produces an increment in the PV array power (21 %).

At 441.3 s, there is a new change in the shading profile from SC_3 to SC_4. The RA set the new optimal configuration is CF_4 at 506.78 s ($t_{reconfig}$ = 36.6 s + 279 ms). The configuration change produces a PV power increment of 22 %. The last change in the shading conditions, from SC_4 to SC_1, is produced at 541.9 s. As expected, the RA determines the new optimal

configuration CF_8, and the PV power and voltage are the same obtained after the first run of the RA. This time CF_8 is set at 588.08 s ($t_{reconfig}$ = 33.6 s + 279 ms).
To illustrate the behavior of both the reconfiguration system and P&O algorithm, Figure **2-30**b shows the trajectory of the operating point, on the array P-V curve, for the dynamic conditions between 430 s and 630 s of the previous simulation. The operating points are also illustrated in Figure **2-30**a in the plot at the top of the Figure. The sequence starts with the PV array at Point 1 (112.9 V, 405.9 W) that correspond to global MPP of CF_{22} under SC_3 (black line). The change from SC_3 to SC_4, at 441.3 s, changes the P-V curve to the yellow trace; therefore, the P&O tracks the local MPP closest to the last global MPP tracked (112.9 V), which is Point 2 (111.4 V, 344.7 W).
After the run of the RA (506.78 s), the P-V curve changes to the brown trace, which corresponds to CF_4, and the P&O algorithm tracks the new operating Point 3 (111.3 V, 421.7 W). With the change in the shading conditions from SC_4 to SC_1, at 541.9 s, the new operating point is 4 (111.0 V, 304.9 W); then, the P&O algorithm tracks the closest MPP: Point 5 (132.7 V, 353.6 W). Finally, the RA runs and determines that CF_8 is the best configuration for SC_1, and it sets the operating point to 6 (112.7 V, 371.4 W), which is the global MPP.

2.3.4.4. Calculation burden of the reconfiguration algorithm

The software objects implemented on the embedded controller (see Figure **2-27**) were programmed in the C language and compiled by using Code Composer Studio [161], which is an optimized compiler for the TMS320F28335 DSP. That compilation transforms each operation written in the C language (e.g., interpolation, communication with SDRT, *etc.*) into multiple fixed-point and floating-point instructions, including also control flow operations, which require different numbers of clock cycles. Moreover, the number of operations performed depends on the shading conditions; therefore, the performance of the RA is analyzed by using the number of clock cycles (ck_{cycles}) and the time required to find the best configuration $t_{reconfig}$.
For example, in the results presented in Section 2.3.4.3, the first execution of RA requires 5,050,855,766 clock cycles to evaluate the 35 possible configurations and to determine the best configuration (SC_1). In the TMS320F28335, such a number of clock cycles is translated into 33.672 s, because each cycle takes 6.67 ns (*i.e.*, clock of 150 MHz).
The calculation burden of the proposed RA is evaluated by using $t_{reconfig_i}$ and ck_{cycles_i} for each run of the RA in the simulation results presented in Figure **2-30**a. The sub-index i represents the number of the RA executions. The values of $t_{reconfig_i}$ and ck_{cycles_i} are shown in Table **2-4**, which also reports the deviation with respect to the average values (36.128 s and 5,416,534,590 clock cycles, respectively).
Table **2-4** shows that $t_{reconfig_i}$ and ck_{cycles_i} change depending on the shading conditions. However, those measurements also depend on other factors, like the communication delays, since even when the shading condition is the same, the simulation time is slightly different.

Table 2-4.: Reconfiguration algorithm performance.

Shading condition	i	$t_{reconfig_i}$ (s)	ck_{cycles_i}	Deviation from average
SC_1	1	33.409	5,008,845,577	−7.5 %
SC_1	2	37.180	5,574,212,894	2.9 %
SC_2	3	36.183	5,424,737,631	0.2 %
SC_2	4	38.388	5,755,322,339	6.3 %
SC_3	5	37.591	5,635,832,084	4.0 %
SC_4	6	36.589	5,485,607,196	1.3 %
SC_1	7	33.558	5,031,184,408	−7.1 %

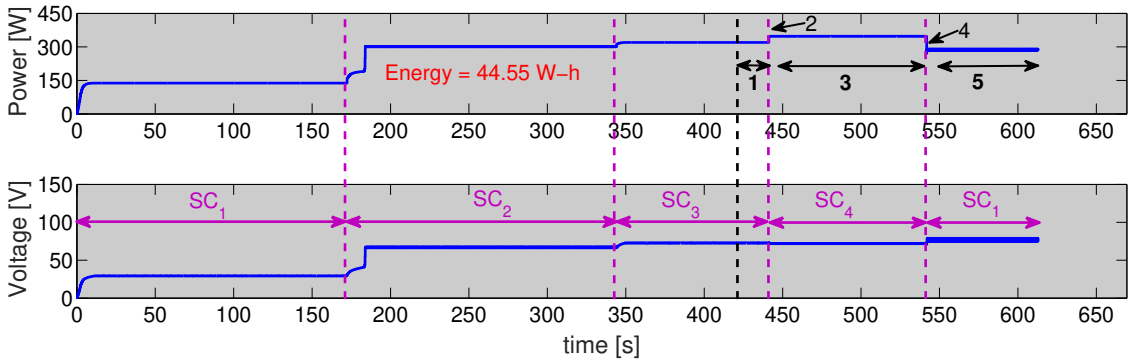
Finally, the longest processing time $t_{reconfig,MAX}$ must be shorter than the time period selected to run the RA consecutively. In this example, $t_{reconfig,MAX} = 38.388s < 90s$. It must be noted that the processing time will increase for a higher number of panels; therefore, an evaluation of the calculation burden must be performed for each case to ensure a correct selection of the embedded device and RA period.

2.3.4.5. Tests without accounting for array reconfiguration

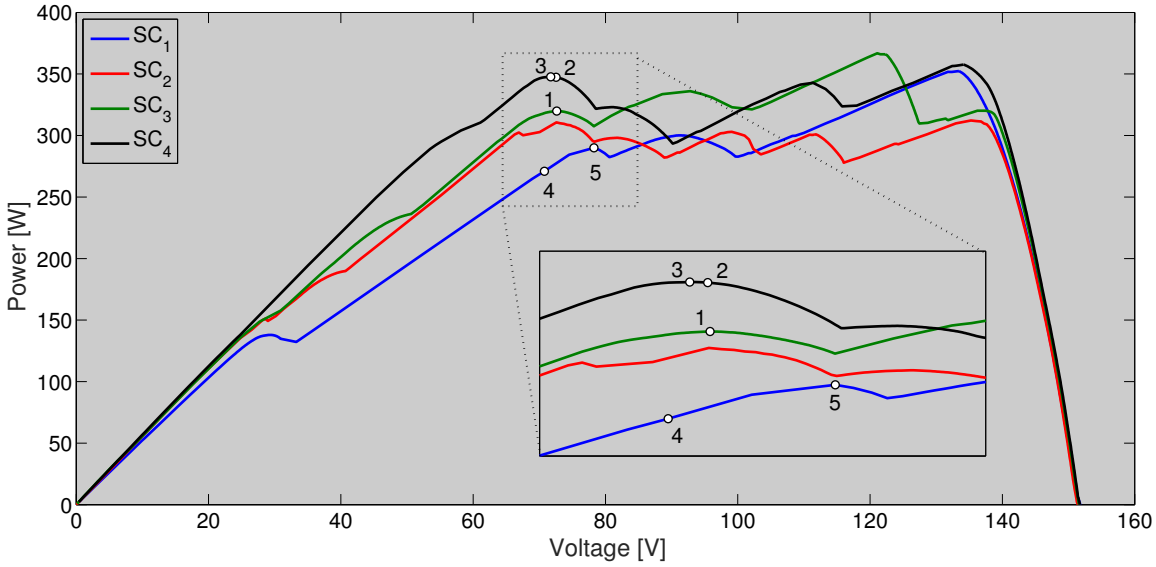
With the aim of illustrating the advantage of the proposed reconfiguration system over the classical static PV array, the simulation performed in Section 2.3.4.3 is repeated considering a PV array with a fixed configuration (CF_{18}). CF_{18} is selected because it is not the best or the worst in terms of power production. The test conditions are the same ones used to evaluate the PV system with reconfiguration, namely a duration close to 613 s and changes on the shading conditions at the same instants of time. The simulation results for this classical PV system are shown in Figure **2-31**a.

At the simulation start, the output power of the PV systems with and without reconfiguration is similar prior to the first run of the RA (29.91 s). Nonetheless, the output power of the PV system without reconfiguration is lower in comparison to the proposed solution after the first run of the RA. In the simulation, the shading condition sequence is: SC_1, SC_2, SC_3, SC_4 and SC_1. For such a sequence, the static PV system produces 230 W, 34 W, 85 W, 70 W and 80 W less power in comparison to the reconfiguration system. It is worth noting that the difference in the power wasted for SC_1 at the beginning and at the end of the simulation indicates that the MPPT tracks different local MPPs in both cases. This is due to the MPP detected by the P&O depends on the last operating point prior to the change in the shading profile as reported in Figure **2-31**b, which shows the evolution of the operating points in the simulation.

The reduced power production is translated into a significant reduction in the energy delivered to the load. The system with reconfiguration produced 55.96 Wh during the simulation, while the system without reconfiguration only produced 44.55 Wh. Therefore, the increment



(a) Dynamic behavior of PV array power and voltage.



(b) Operating points in the P-V curves.

Figure 2-31.: Behavior of the PV array with fixed configuration.

in the energy production with the proposed RA is 25.61 %.

The operating points of the static PV array during the simulation, starting from 430 s, have the following trajectory, as reported in Figure **2-31**band Figure **2-31**a. The sequence starts with the PV array at Point 1, which corresponds to a local maximum for CF_{18} under SC_3. After the change on the shading conditions, the operating point moves to 2 on the P-V curve of SC_4. Then, the MPPT moves the operating point to 3, which is the closest local MPP. For the next change of the shading profile, the operating point moves to 4 and then to 5. It should be noted that the operating point never reaches the global MPP, which explains why the power produced by this static solution is significantly lower in comparison with the PV reconfiguration system.

With the aim of illustrating the cost-benefit of the reconfiguration solution over the static

PV solution, the costs of both solutions are analyzed. The cost of the PV inverter is U.S. $680, and each PV panel has a cost of U.S. $85. The TMS320F28335 DSP has a cost of U.S. $35. The sweep device requires a capacitor with a costs equal to U.S. $10, a resistor with a cost equal to U.S. $2 and a relay to discharge the capacitor. Moreover, the switches' matrix must support four panels per strings and three strings (one string is used for the sweep device), which requires 82 relays according to [142]. In addition, the DSP, switches' matrix and sweep device must be placed in a PCB with a costs near U.S. $10. Taking into account that each relay has a cost of U.S. $1.3, the reconfiguration system (DSP, switches' matrix and sweep device) has a costs close to U.S. $165. Therefore, the complete PV installation with reconfiguration capabilities (including the inverter and eight panels) has a total cost of U.S. $1525. Taking into account that, in this example, the reconfiguration solution produces 25.61 % more energy, the static PV system will need, approximately, three or four additional PV panels (depending on the strings' configuration) to produce the same amount of energy provided by the reconfigurable PV system. This means that an equivalent static PV system (with three and four additional PV panels) will costs between U.S. $1615 and U.S. $1700, which is between 6 % and 11.5 % more expensive. In this case, the reconfiguration solution is the option with the lower cost per kWh.

Finally, the example presented in this section is a particular case of study to demonstrate the operation and benefits of the proposed reconfiguration system. However, depending on the shading profiles present in a particular PV installation, the dynamic behavior of the reconfiguration system (Subsection 2.3.4.3) could produce a negligible, or even null, power increment with respect to the static PV array. Therefore, it is required to analyze the economic viability of the reconfiguration system for the particular geographic location and shading patterns exhibited in a given application. This procedure can be done using simulations of the annual energy production and costs analyses for the PV installation with and without the reconfiguration system, so that the effective cost-benefit of this solution can be evaluated.

2.4. Conclusions

This chapter presented a model of photovoltaic generation systems based on a distributed MPPT structure. Such systems represent an alternative to mitigate the negative effects produced by partial shading of the modules and other mismatching conditions. The model considers the electrical behavior of the PV modules and the dynamics of the converter to generate a set of matrices that can be solved by any numerical method. As a result, classical electric simulators are not needed to evaluate the performance of distributed MPPT systems, which reduces the costs by avoiding the use of commercial software. Moreover, the design of simulation models is simplified because there is no need to construct all the discrete connections of each element using CAD applications, which is critical for systems formed by a large number of components. The proposed model can be easily implemented in any mathematical simulation software (e.g. Matlab® or Scilab®) or in any programming language

(e.g. C or Fortran) with the appropriate scientific libraries (e.g. GSL). Making the most of these libraries - some of which are free to use - increases computation speed and reduces implementation costs.

In Section 2.2 a novel multi-variable maximum power point tracking algorithm is introduced. The method is suitable for distributed photovoltaic applications with an architecture based on the adoption of a centralized controller for distributed DC/DC converters. Simulation results confirm that the proposed technique performs better than other multi-variable controls presented in recent literature, without requiring any additional hardware. Both model and MPPT technique corresponds to the first and second contributions of the Thesis.

A reconfiguration algorithm for PV arrays in a SP structure, based on the I-V curves of commercial PV panels, was proposed in Section 2.3. This algorithm starts measuring the I-V curves of the PV panels using a simple and inexpensive sweep device. Then, the P-V curves of all possible configurations are constructed from the I-V curves of the panels to determine the configuration that provides the highest global MPP. The proposed algorithm uses interpolation to minimize the arithmetic operations executed in the embedded system in order to reduce, as much as possible, the time required to evaluate each configuration. The reduction in the calculation time enables the evaluation of all of the possible configurations in a reasonable time using inexpensive embedded devices.

The proposed algorithm was implemented on the embedded system TMS320F28335 DSP. The PV system, *i.e.*, PV array, switches' matrix, DC/DC converter and load, was emulated using the Simulink Desktop Real-Time toolbox from Matlab®. This approach enables one to evaluate the performance of the proposed solution in a hardware-in-the-loop environment, with repetitive operating conditions to provide a fair comparison between different solutions.

The real-time operation and benefits of the reconfiguration solution were evaluated using a practical example based on commercial devices. Those HIL tests were performed considering a PV array formed by two strings of four panels each (4×2). The experiments consider four changes in the shading conditions to evaluate the reconfiguration speed, where the average time required to find the best configuration was 36.128 s plus 279 ms required to obtain the experimental I-V curves of all of the PV panels. Those results were compared with a classical static PV system and a typical MPPT technique. In this particular case, the reconfigurable PV system produces an increment of 25.61 % in the energy generated. To obtain the same energy with a fixed PV system, it would be necessary to add three or four panels to the array depending on the strings' configuration, which would be more expensive than the hardware required to perform the reconfiguration. However, it is important to note that the economical viability of the proposed reconfiguration system has to be evaluated for each particular application.

It is worth noting that the reconfiguration solution can be applied to small PV arrays (e.g., residential applications) in order to obtain a reasonable number of possible configurations and switches. Moreover, this solution can be improved in the following ways: the time between two consecutive runs of the algorithm could be optimized by introducing a circuit to

detect a change in the shading conditions, so that the reconfiguration only runs when it is required. Other possible improvement would be to reduce, even more, the calculation time by introducing a combinational optimization algorithm. In this case, the reconfiguration solution could be suitable for larger PV arrays. This reconfiguration solution corresponds to the third contribution of the Thesis.

3. DC-bus regulation

The goal of this Chapter is to provide a stable DC-bus voltage of the system presented in Figure **1-1** in any operating condition. Such a stand-alone power system is based on renewable energy sources, which also requires an Energy Storage Devices (ESD) interfaced with a charger/discharger based on a bidirectional DC/DC converter, and a DC bus.
The first work reported in this Chapter [88] proposes a single sliding-mode controller (SMC) for the charger/discharger DC/DC converter to provide a stable DC bus voltage in both charging or discharging conditions, or even without any power exchange between the ESD and the DC-bus. Due to the non-linear nature of the power converter, the SMC parameters are adapted online to ensure global stability in any operation condition. Such stability of the adaptive SMC is mathematically demonstrated using analytical expressions for the transversality, reachability and equivalent control conditions. Moreover, a design procedure for the adaptive SMC parameters is provided in order to ensure the dynamic response required for the correct operation of the load. Finally, simulations and experimental tests validate the proposed controller and design procedure. This solution corresponds to the fourth contribution of the Thesis.
The second part of this Chapter proposes a sliding-mode controller for the same charger/discharger DC/DC converter but with an improved disturbance rejection to provide a tight bus voltage regulation for safe operation [87]. The main novelty of this solution is the inclusion of the bus current into the sliding surface, which accelerates the controller response. Moreover, a formal proof of the system global stability is provided, and a detailed process is developed to calculate the controller and implementation parameters. Finally, the proposed solution is validated through simulations and experiments. This solution corresponds to the fifth contribution of the Thesis.
Finally, both solutions were published in [88, 87, 169].

3.1. Sliding-mode control of a charger/discharger DC/DC converter for DC-bus regulation in renewable power systems

The charger/discharger implementation circuit usually involves a bidirectional DC/DC converter. Moreover, the stand-alone power system depicted in Figure **1-1** exhibits a DC-bus

that is formed by the parallel connection of the DC/DC converters output. Finally, the bus must provide a regulated voltage depending on the load requirements.

Due to the low voltage operation commonly exhibited by renewable generators, such as PV systems, and the variability of the voltage required by several commercial loads, the unidirectional DC/DC converter interfacing the source is designed with the boost topology to provide both simplicity and high voltage conversion range [170, 171, 75]. In addition, the MPPT controller acting on the DC/DC converter is designed to optimize the operation of the renewable generator: for example, if a PV generator is used as the main source, the MPPT controller defines the duty cycle d of the DC/DC converter to increment the PV power p_g generated [170, 75]. Similarly, if a fuel cell is used as main generator, the MPPT controller regulates the DC/DC converter to decrement the generator current i_g, which is proportional to the hydrogen consumption [172, 173, 174]. Under the light of the previous analysis, and referring to Figure **3-1**, the output of the unidirectional DC/DC converter is not regulated, hence it provides a power profile p_s with a non-regulated current i_s. Therefore, the charger/discharger must be controlled to provide a stable voltage V_{DC} to the DC-bus in concordance with the load requirements.

In agreement with the previous requirement, the ESD and the charger/discharger with its associated controller form the DC-bus voltage regulator. This system provides or absorbes the power difference p_{DC} between the renewable generator and the load. This bus voltage regulator enables the system to supply energy when the main power source is not able to cover the load profile, *i.e.*, $p_o > p_s$. Furthermore, the bus voltage regulator stores the energy when the load is not consuming, or when a regenerative load recovers energy (negative p_o), e.g., regenerative breaking in electrical vehicles.

In conclusion, the bidirectional DC/DC converter behaves as a voltage source with a power profile p_{DC} equal to the positive or negative difference between the load and generator powers, *i.e.*, $p_{DC} = p_o - p_s$ with $i_{DC} = i_o - i_s$ since v_{DC} must be regulated (see Figure **3-1**).

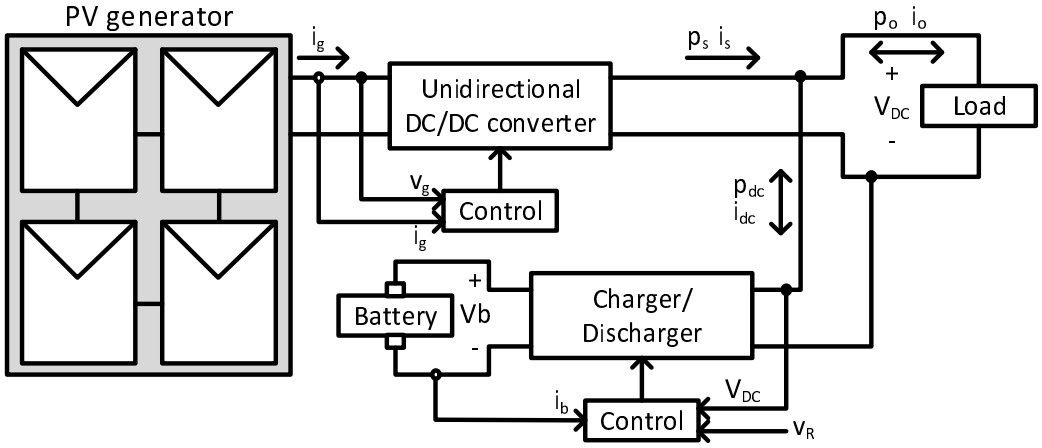


Figure 3-1.: Stand-alone power system with bus voltage regulation.

The classical solution to control a battery charger/discharger is based on an inner current loop and an outer voltage or power loop. The current loop has two main purposes: reduce the order of the system to simplify the controller design and reject fast current perturbations generated in the DC bus, for example, compensate changes in the power produced by the generator (e.g., sunlight increase/decrease in a PV system) or in the power requested by the load. The use of this structure is reported in the battery charger/discharger applications recently published in [175] and [176].

A widely used battery charger/discharger DC/DC converter is presented in Figure **3-2**, which is based on a bidirectional boost (buck) converter [177]. Moreover, this figure also illustrates a classical cascade current-voltage control structure, in which the current controller acts on the MOSFET signal u directly (e.g., sliding-mode, peak current, valley current controllers) or using a PWM (e.g., average current control). This structure is used to avoid the non-minimum phase condition exhibited by the transfer function between the DC bus voltage and the converter duty cycle. This is achieved by controlling the inductor current, i.e., the battery current, which exhibits a minimum phase transfer function with respect to the duty cycle. Then, the inductor is modeled as a current source to provide a minimum-phase first-order transfer function between the DC bus voltage and the current reference; hence, a linear controller can be used to regulate the bus voltage. However, this strategy requires a narrow bandwidth in the voltage loop to ensure the validity of the current source approximation. This is the main drawback of the cascade structure: the bandwidth of the voltage controller is between 5 and 10 times smaller than the current loop [178, 179, 180]. Hence, the controller speed is constrained, which reduces its ability to compensate fast perturbations.

The cascade structure has also been used to control the power flow between the battery and the DC-bus. This case was reported in [177], which uses an inner control loop to regulate the battery current and an outer control loop to regulate the DC bus energy. Note that the circuit presented in Figure **3-2** has an equivalent behavior: in a power system with a regulated DC-bus, similar to the one presented in Figure **1-1**, the difference between the load power and the power provided by the main generator is stored/supplied in the DC-bus capacitor. Therefore, the battery charger/discharger must be controlled to regulate the DC-bus voltage, which forces transferring that power difference from the DC-bus capacitor into the battery. In this case, if the DC-bus voltage is increased by a positive power difference between the generator and load power profiles, then the charger/discharger transfers that energy from the DC-bus to the battery; similarly, if the DC-bus voltage is decreased by a negative power difference between the generator and load power profiles, then the charger/discharger extracts that energy from the battery to supply the DC-bus.

This Section, whose results were published in [88, 87], adopts the bidirectional DC/DC converter circuit depicted in Figure **3-3** to enable both positive and negative current flows from/to the ESD. That switching structure is designed to interface low ESD voltages v_b with DC-buses exhibiting higher voltages v_{DC}, *i.e.*, $v_b < v_{DC}$. This is a common condition for systems that are based on low-voltage batteries or super-capacitors. In the electrical scheme

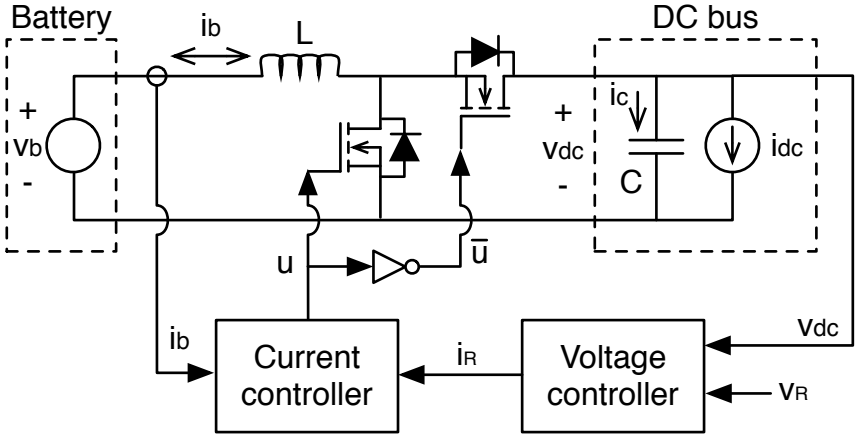


Figure 3-2.: Structure of a cascade control of the charger/discharger.

of Figure **3-3** the ESD is modeled as a voltage source with current i_b, while the DC-bus is modeled by a capacitor C and its associated current flow i_{DC}. The switched differential equations that describe the system dynamics are given in (3-1) and (3-2), where u represents the MOSFET activation signal ($u = 1$ for ON state and $u = 0$ for OFF state). Such a model accurately describes the charger/discharger dynamics.

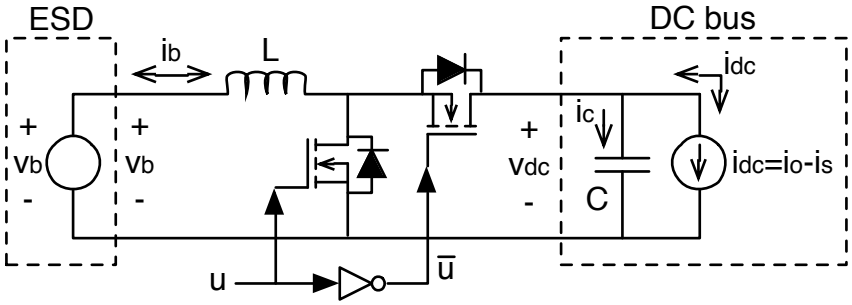


Figure 3-3.: Charger/discharger based on a bidirectional DC/DC converter.

$$\frac{d\, i_b}{dt} = \frac{v_b - v_{DC} \cdot (1-u)}{L} \tag{3-1}$$

$$\frac{d\, v_{DC}}{dt} = \frac{i_b \cdot (1-u) - i_{DC}}{C} \tag{3-2}$$

In conclusion, the main objective of the control system associated to this bus voltage regulator is to control the output voltage of the bidirectional DC/DC converter to guarantee stability. However, the non-linear nature of the bidirectional DC/DC converter makes impossible to fulfill that objective using classical lineal control techniques, e.g., PI, PID or lead-lag controllers. Moreover, the output voltage of the converter must be regulated in both charge and discharge operation conditions (positive and negative power flows), which is not a trivial

task for linear controllers. Under the light of the previous conditions, the charger/discharger must be regulated by a non-linear controller to guarantee the global stability of the DC-bus.

3.1.1. Sliding mode controller analysis

This Section proposes a sliding surface formed by the ESD current i_b, the DC voltage error and the integral of the DC voltage error. In this way, the controller is able to detect the direction of the power flow (charge or discharge), given by the sign of i_b, and the error in the DC voltage. The proposed switching function Ψ and sliding surface Φ are given in (3-3), where v_R represents the desired DC bus voltage (or reference) given by the load requirements, while k_p and k_i are parameters of the surface.
Figure **3-4** presents the block diagram of the sliding-mode control system, where the converter differential equations, in state-space representation, interact with the sliding-mode controller (SMC). The MOSFET activation signal u is generated by an inverted-comparator centered in zero evaluating the switching function Ψ.

$$\Psi = i_b + k_p \cdot (v_R - v_{DC}) + k_i \cdot \int (v_R - v_{DC})\, dt \quad \wedge \quad \Phi = \{\Psi = 0\} \tag{3-3}$$

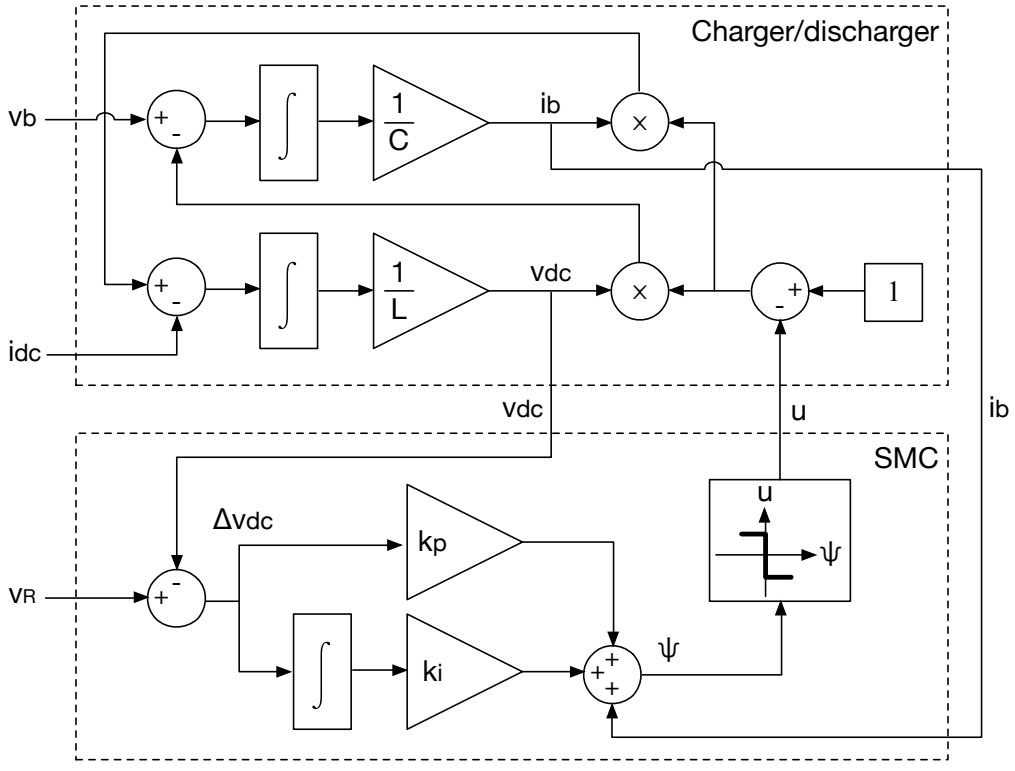


Figure 3-4.: Block diagram of the sliding-mode control.

The derivative of the switching function is given in (3-4), where Δv_{DC} represents the deviation of the DC voltage from the desired value. The reference v_R is a constant value defined by the load requirements. Substituting (3-1) and (3-2) into (3-4) leads to (3-5), which includes the binary control variable u.

$$\frac{d\,\Psi}{dt} = \frac{d\,i_b}{dt} - k_p \cdot \frac{dv_{DC}}{dt} + k_i \cdot \Delta v_{DC} \quad , \quad \Delta v_{DC} = v_R - v_{DC} \tag{3-4}$$

$$\frac{d\,\Psi}{dt} = \left[\frac{v_b - v_{DC} \cdot (1-u)}{L}\right] - k_p \cdot \left[\frac{i_b\,(1-u) - i_{DC}}{C}\right] + k_i \cdot \Delta v_{DC} \tag{3-5}$$

Inside the sliding-surface, *i.e.*, if the sliding-mode exists, the conditions in (3-6) are fulfilled [181, 80, 182, 82], which in steady-state stand for $v_{DC} = v_R$ and $i_b = -k_i \cdot \int \Delta v_{DC}\, dt$, hence a stable DC voltage equal to the desired value.

$$\Psi = 0 \quad \wedge \quad \frac{d\,\Psi}{dt} = 0 \tag{3-6}$$

To guarantee the existence of the sliding-mode, *i.e.*, guaranteeing (3-6), three conditions must be ensured [181, 80, 182]: transversality, reachability and equivalent control. The transversality condition analyses the system controllability, the reachability analyses the ability of reaching the surface, and the equivalent control analyses the local stability. Therefore, the transversality condition must be fulfilled to enable the sliding-mode controller to affect the system dynamics. The reachability condition must be fulfilled to enable the controller to drive the system towards the desired operation condition. Finally, the equivalent control condition must be fulfilled to enable the system to keep trapped inside the sliding-surface. In the following subsections those conditions are analyzed in detail.

3.1.1.1. Transversality condition

The transversality condition analyses the presence of the control variable into the derivative of the sliding-surface as given in (3-7) [183, 80]. In such a way, the fulfillment of (3-7) ensures the ability of the sliding-mode controller to modify the system behavior.

$$\frac{d}{du}\left(\frac{d\,\Psi}{dt}\right) \neq 0 \tag{3-7}$$

Deriving (3-5) with respect to u leads to the following equation:

$$\frac{d}{du}\left(\frac{d\,\Psi}{dt}\right) = \frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C} \neq 0 \tag{3-8}$$

From such an expression three possible conditions are indetified: $i_b = 0$, *i.e.*, null power exchange between the ESD and the bus; $i_b < 0$, *i.e.*, charging the ESD from the bus; $i_b > 0$, *i.e.*, discharging the ESD to supply the bus. From the first condition it is concluded that the transversality value is positive as in (3-9), which imposes the reachability conditions as described in [184, 80]. Therefore, the transversality must exhibit the same sign in all the conditions to provide an unified analysis that ensures the existence of the sliding-mode. Moreover, Section 3.1.1.4 will demonstrate that both k_p and k_i must be negative to guarantee a stable behavior of the system.

$$\frac{d}{d\,u}\left(\frac{d\,\Psi}{dt}\right) = \frac{v_{DC}}{L} > 0 \tag{3-9}$$

Then, also in the second condition $i_b < 0$ the transversality must be positive, which in (3-8) requires $k_p < 0$ since v_{DC}, L and C are positive quantities. Similarly, in the third condition $i_b > 0$ the transversality must be positive, which requires that condition in (3-10) be fulfilled. Then, such a restriction must be included in the design process of k_p.

$$-k_p < \frac{v_{DC}}{i_b} \cdot \frac{C}{L} \quad \text{for} \quad i_b > 0 \tag{3-10}$$

3.1.1.2. Reachability conditions

The reachability conditions analyze the ability of the system to reach the desired surface $\Phi = \{\Psi = 0\}$ [184, 80]. This concept is illustrated in Figure **3-5**: when the system operates under the surface, which means a negative value of the sliding function ($\Psi < 0$), the derivative of the sliding function must be positive to enable the system to reach the surface $\Psi = 0$. Similarly, when the system operates over the surface, which means a positive value of the sliding function ($\Psi > 0$), the derivative of the sliding function must be negative to enable the system to reach $\Psi = 0$. Then, the continuous switching between positive and negative derivatives of Ψ around $\Psi = 0$ creates the sliding mode [185].

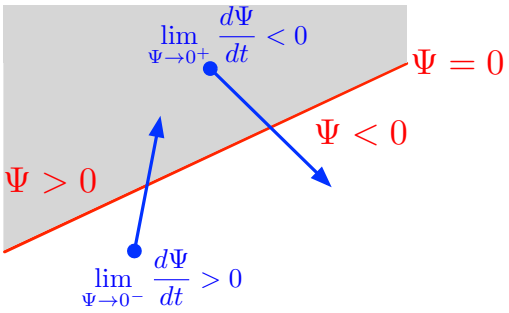


Figure 3-5.: Concept of reachability conditions.

The sign of the transversality defines the reachability conditions: since $\frac{d}{du}\left(\frac{d\,\Psi}{dt}\right) > 0$ then a positive derivative of the switching function is obtained for $u = 1$, while a negative derivative is obtained for $u = 0$. For a negative transversality the relation is inverse. Such conditions are mathematically described in (3-11) [80].

$$\lim_{\Psi\to 0^-} \left.\frac{d\,\Psi}{dt}\right|_{u=1} > 0 \quad \wedge \quad \lim_{\Psi\to 0^+} \left.\frac{d\,\Psi}{dt}\right|_{u=0} < 0 \tag{3-11}$$

Replacing (3-5) into (3-11) leads to the following conditions that must be guaranteed:

$$\frac{v_b}{L} + k_p \cdot \frac{i_{DC}}{C} + k_i \cdot \Delta v_{DC} > 0 \tag{3-12}$$

$$\left[\frac{v_b - v_{DC}}{L}\right] - k_p \cdot \left[\frac{i_b - i_{DC}}{C}\right] + k_i \cdot \Delta v_{DC} < 0 \tag{3-13}$$

To further analyze such expressions, the power balance equations of the DC/DC converter (disregarding losses) given in (3-14) must be used, in which d represents the converter duty cycle.

$$i_b \cdot v_b = i_{DC} \cdot v_{DC} \quad \wedge \quad v_b = (1-d) \cdot v_{DC} \quad \wedge \quad i_b \cdot (1-d) = i_{DC} \tag{3-14}$$

Using those relations, inequalities (3-12) and (3-13) become:

$$\left(\frac{v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] + k_i \cdot \Delta v_{DC} > 0 \tag{3-15}$$

$$-\left(\frac{v_{DC} - v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] + k_i \cdot \Delta v_{DC} < 0 \tag{3-16}$$

The term $\left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right]$ is positive since it corresponds to the transversality value, and $k_i < 0$ is required to guarantee a stable behavior of the system as it will be explained in Section 3.1.1.4. In addition, Δv_{DC} could be zero, positive or negative: $\Delta v_{DC} = 0$ stands for the desired v_{DC} condition; $\Delta v_{DC} > 0$ stands for an undershot $v_{DC} < v_R$, e.g., due to a fast increment in the bus current; while $\Delta v_{DC} < 0$ stands for an overshot $v_{DC} > v_R$, e.g., due to a fast decrement in the bus current. Then, both (3-15) and (3-16) must be analyzed for the three possible Δv_{DC} conditions.

- $\Delta v_{DC} = 0$: the following inequalities guarantee the reachability conditions (3-15) and (3-16).

$$\left(\frac{v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] > 0 \tag{3-17}$$

$$-\left(\frac{v_{DC} - v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] < 0 \tag{3-18}$$

- $\Delta v_{DC} > 0$: inequality given in (3-16) is guaranteed since $k_i < 0$. Instead, inequality (3-15) requires the following condition to be fulfilled:

$$-k_i < \left(\frac{1}{\Delta v_{DC}}\right) \cdot \left(\frac{v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] \quad \text{for} \quad \Delta v_{DC} > 0 \tag{3-19}$$

- $\Delta v_{DC} < 0$: inequality given in (3-15) is guaranteed since $k_i < 0$. Instead, inequality (3-16) requires the following condition to be fulfilled:

$$-k_i < -\left(\frac{1}{\Delta v_{DC}}\right) \cdot \left(\frac{v_{DC} - v_b}{v_{DC}}\right) \cdot \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] \quad \text{for} \quad \Delta v_{DC} < 0 \tag{3-20}$$

Then, both restrictions given in (3-19) and (3-20) must be fulfilled to guarantee the reachability conditions. Therefore, such restrictions must be included in the design process of k_i.

3.1.1.3. Equivalent control condition

The equivalent control condition analyzes the local stability of the system. In such a way, the conditions in (3-6) must be achieved in the normal operation of the DC/DC converter, *i.e.*, switching the MOSFET state (ON or OFF) using the control variable u. This means that u most not be permanently in ON or OFF state. Therefore, the analog equivalent value of u, denoted as u_{eq}, must be constrained within the values of u. Such a condition is mathematically expressed as follows [183, 185]:

$$\left.\frac{d\,\Psi}{dt}\right|_{u=u_{eq}} = 0 \;\rightarrow\; 0 < u_{eq} < 1 \tag{3-21}$$

Replacing u by u_{eq} in (3-5), and equating it to zero, leads to the following expression for the equivalent control:

$$u_{eq} = \frac{\left[\frac{v_{DC} - v_b}{L}\right] + k_p \cdot \left[\frac{i_b - i_{DC}}{C}\right] - k_i \cdot \Delta v_{DC}}{\left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right]} \tag{3-22}$$

Then, expressions for $u_{eq} > 0$ and $u_{eq} < 1$ are obtained in (3-23) and (3-24), respectively. Such expressions are equivalent to (3-12) and (3-13), hence fulfilling the reachability conditions also guarantee the equivalent control condition.

$$\left[\frac{v_{DC} - v_b}{L}\right] + k_p \cdot \left[\frac{i_b - i_{DC}}{C}\right] - k_i \cdot \Delta v_{DC} > 0 \tag{3-23}$$

$$\left[\frac{v_{DC} - v_b}{L}\right] + k_p \cdot \left[\frac{i_b - i_{DC}}{C}\right] - k_i \cdot \Delta v_{DC} < \left[\frac{v_{DC}}{L} + k_p \cdot \frac{i_b}{C}\right] \tag{3-24}$$

3.1.1.4. Sliding mode dynamics

The existence of the sliding-mode ensures the fulfillment of the conditions previously described in (3-6). In such a way, the sliding-mode dynamics are given by (3-25), in time domain, and by (3-26), in Laplace domain. Such expressions impose the closed-loop dynamics of the ESD current i_b.

$$i_b = -k_p \cdot \Delta v_{DC} - k_i \cdot \int \Delta v_{DC}\, dt \tag{3-25}$$

$$\frac{i_b(s)}{\Delta v_{DC}(s)} = -k_p - \frac{k_i}{s} \tag{3-26}$$

Then, the DC bus voltage dynamics, *i.e.*, (3-2), is imposed by (3-26). Moreover, since the sliding-mode controller drives the MOSFET signal u, the expression (3-2) must be modified to include the sliding-mode dynamics. To remove the switching condition from (3-2) it is required to average the binary control signal u over the switching period T, which is known as the averaged model approximation [186, 134]:

$$d = \frac{1}{T} \cdot \int_0^T u\, dt \tag{3-27}$$

Then, considering that $d' = 1 - d$, the closed-loop dynamic behavior of the DC voltage is given by (3-28).

$$\frac{d\, v_{DC}}{dt} = \frac{i_b \cdot d' - i_{DC}}{C} \tag{3-28}$$

Finally, by combining (3-26) and (3-28) in Laplace domain, the complete closed-loop dynamic behavior of the bus voltage is given by (3-29), which depends on the perturbations introduced by the bus current and the reference.

$$v_{DC}(s) = \frac{-s}{C \cdot s^2 - k_p \cdot d' \cdot s - k_i \cdot d'} \cdot i_{DC}(s) + \frac{(-k_p \cdot s - k_i) \cdot d'}{C \cdot s^2 - k_p \cdot d' \cdot s - k_i \cdot d'} \cdot v_r(s) \tag{3-29}$$

However, as pointed out before, the reference is a constant value imposed by the load characteristics, while the bus current depends on the operation conditions of the main generator and on the load power request. Therefore, the system given in (3-30) is used in the following section to design the parameters k_p and k_i of the sliding-mode controller.

$$\frac{v_{DC}(s)}{i_{DC}(s)} = \frac{-s}{C \cdot s^2 - k_p \cdot d' \cdot s - k_i \cdot d'} \tag{3-30}$$

Finally, (3-30) demonstrates that both k_p and k_i must be negative to guarantee stable sliding-mode dynamics, otherwise the equivalent dynamics will exhibit negative poles, *i.e.*, an unstable behavior.

3.1.2. Design of the sliding mode dynamic behavior

The closed-loop dynamics of the sliding-mode system, given in (3-30), show that any persisten change on the DC bus current i_{DC} will be compensated, *i.e.*, $\lim_{s\to 0} \frac{v_{DC}(s)}{i_{DC}(s)} = 0$. However, the dynamic behavior of the bus voltage must be controlled to avoid large voltage undershoots that could turn-off the load, or large voltage overshoots that could destroy the load. Therefore, the sliding-mode dynamic behavior is designed in terms of the following performance parameters and conditions:

1. The DC-bus could experiment fast current perturbations due to both load profile and renewable source characteristics. For example, PV generators could exhibit fast current decrements due to shades projected by mobile objects [187, 188]. On the other hand, the load could request fast current increments, as in the case of microprocessors [189], while fuel cells are unable to provide those fast step currents [190]. In the first case the DC-bus will be exposed to step-like current decrements, while in the second case the DC-bus will be exposed to step-like current increments. Therefore, the SMC design must consider step-like perturbations with magnitude Δi_{DC}.

2. The DC-bus voltage must be regulated at the desired value with deviations lower or equal to MO. This means that the maximum acceptable overshoot (or undershoot) magnitude is equal to MO.

3. During a transient, the load requires that the DC-bus voltage be recovered to an acceptable band $[-\delta_{safe}, \delta_{safe}]$, around the reference voltage, with a maximum stabilization time t_{safe}.

Then, the following information is required to design the dynamic behavior of the SMC: the expected maximum DC-bus current perturbation Δi_{DC}, the maximum voltage deviation MO accepted by the load, the safe band $[-\delta_{safe}, \delta_{safe}]$ and maximum stabilization time t_{safe} required for the correct operation of the load.
Since the previous design criteria are time-domain values, the time response of the DC-voltage, under the action of the sliding-mode controller, is calculated from the inverse Laplace transformation of (3-30). Then, two possibilities are considered: an underdamped response and a critically damped response. The main characteristics of those options are:

- Underdamped response: enable to reach faster the nominal voltage at the expense of oscillations around such a voltage. This dynamic response is suitable for loads very sensible to voltage drops but less sensible to voltage oscillations, e.g., microprocessors [189].

- Critically damped response: avoid oscillations around the nominal voltage at the expense of a longer delay to reach it. This dynamic response is suitable for loads very

sensible to voltage oscillations but with larger tolerance to voltage drops, e.g., variable speed drives for DC series motors [191].

This analysis does not consider an overdamped response since it does not provide any advantage over the critically damped response.

3.1.2.1. Underdamped response

The step response of (3-30), assuming values of k_p and k_i that leads to an underdamped time response, is given in (3-31), where the condition imposed by (3-32) must be fulfilled to guarantee the underdamped behavior. Such a response considers the largest current transient Δi_{DC} expected from the DC-bus.

$$y = \left(\frac{-\Delta i_{DC}}{C \cdot \sqrt{-\left(\frac{k_p \cdot d'}{2 \cdot C}\right)^2 - \frac{k_i \cdot d'}{C}}} \right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t\right) \cdot \sin\left(\sqrt{-\left(\frac{k_p \cdot d'}{2 \cdot C}\right)^2 - \frac{k_i \cdot d'}{C}} \cdot t\right) \quad (3\text{-}31)$$

$$-k_i > \frac{k_p^2 \cdot d'}{4 \cdot C} \quad (3\text{-}32)$$

The highest DC-bus voltage deviation caused by such a transient corresponds to the maximum overshoot MO. The MO occurs when the voltage derivative is equal to zero as it is analyzed in (3-33) and (3-34), which correspond to the time t_{MO} given in (3-35). Finally, the MO is calculated by evaluating (3-31) in (3-35), which leads to the expression given in (3-36).

$$\frac{d\,y}{dt} = \left(\frac{-\Delta i_{DC}}{C \cdot \Theta}\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t\right) \cdot \left[\left(\frac{k_p \cdot d'}{2 \cdot C}\right) \cdot \sin(\Theta \cdot t) + (\Theta) \cdot \cos(\Theta \cdot t)\right] = 0 \quad (3\text{-}33)$$

$$\Theta = \sqrt{-\left(\frac{k_p \cdot d'}{2 \cdot C}\right)^2 - \frac{k_i \cdot d'}{C}} \quad (3\text{-}34)$$

$$t_{MO} = \frac{1}{\Theta} \cdot \arctan\left(\frac{-2 \cdot C \cdot \Theta}{k_p \cdot d'}\right) \quad (3\text{-}35)$$

$$MO = \left(\frac{-\Delta i_{DC}}{C \cdot \Theta}\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t_{MO}\right) \cdot \sin(\Theta \cdot t_{MO}) \quad (3\text{-}36)$$

Expression (3-36) can be used to design k_p and k_i to ensure a maximum voltage deviation equal to MO. However, several loads require to restore the voltage within a safe range at a given time to avoid the turn-off of sensible circuits. That is the case of the Intel® Xeon® Processor W5590 configured to operate at 1.1V@100A, which after a current transient must operate at least at 0.99 V after a maximum delay of 25 ms [189]. Similarly, exposition to long

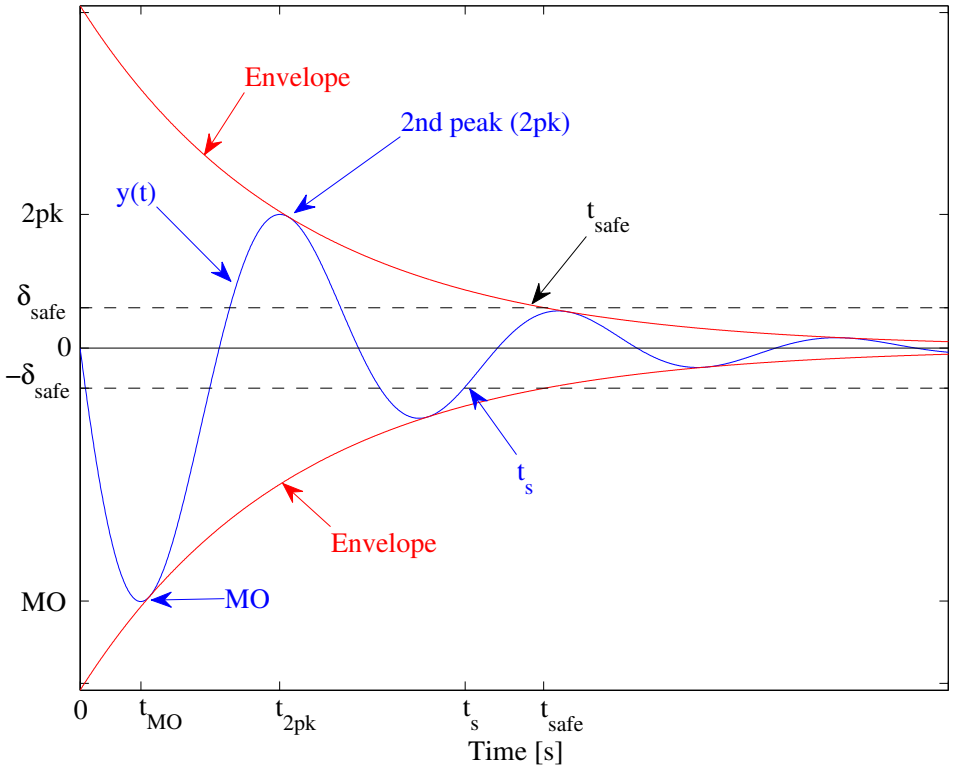


Figure 3-6.: Time response of an underdamped second-order system with a zero.

over-voltages could damage some loads such as the same Intel® Xeon® Processor W5590, in which overshoots cannot exceed 50 mV [189]. Therefore, in general, the bus voltage must be driven within the safe limits $-\delta_{safe}$ and δ_{safe} in, at maximum, the time interval t_{safe}. Such a condition is commonly addressed by using the settling-time t_s criterion, but the traditional expressions for t_s are, in general, inaccurate and they could lead to controllers that provide an effective settling time longer than the expected one as discussed in [192, 193, 194]. Moreover, the traditional t_s expressions provide inaccurate predictions for systems with a zero, e.g., (3-30), as discussed in [195]. Therefore, this Section proposes to design the sliding-mode controller using the envelope component of the system time response. To illustrate such an approach, Figure **3-6** presents the time response of (3-30), and its envelopes, for a positive step perturbation in the DC-bus current. In the figure it is observed the undershoot MO occurring at t_{MO}; while the system enters into the safe band $[-\delta_{safe}, \delta_{safe}]$ at the instant t_s. However, since t_s is difficult to predict due to the periodic oscillation, it is simpler (and safer) to predict the time t_{safe} in which the envelope enters the safe band since $t_s \leq t_{safe}$. Therefore, designing the controller on the basis of t_{safe} ensures that the systems enters the safe band in a time lower or equal than the required one t_s.

The expression describing the envelope waveform is obtained by removing the sinusoidal component from (3-31), leading to expression (3-37), which is parameterized in terms of

δ_{safe} and t_{safe}.

$$\delta_{safe} = \left(\frac{-\Delta i_{DC}}{C \cdot \Theta}\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t_{safe}\right) \tag{3-37}$$

Finally, expressions (3-36) and (3-37) form a simultaneous non-linear equation system that must be solved to calculate k_p and k_i, so that the DC-bus voltage exhibits a maximum deviation MO for a DC-bus current perturbation Δi_{DC}, entering into the load safe band $[-\delta_{safe}, \delta_{safe}]$ in the time t_{safe}. Moreover, k_p and k_i must fulfill the constraints given in (3-10), (3-19) and (3-20), which are required for the existence of the sliding-mode, and the constraint imposed in (3-32), which is required for an underdamped behavior.
Such a constrained and non-linear equations system can be solved using numerical methods like Trust-Region or Levenberg-Marquardt [196, 197], e.g., using Matlab® fsolve function.

3.1.2.2. Critically damped response

The main disadvantage of the underdamped design is observed in Figure **3-6**: in addition to the larger voltage deviation MO, the DC-bus voltage exhibits several additional oscillations. In fact, Figure **3-6** highlights the second peak (2pk) of the voltage, which in this case has an amplitude of 52.3 % of MO; therefore the load must support a voltage drop of MO and an over-voltage of $0.523 \cdot MO$. After that, a third peak with an amplitude of 27.3 % of MO occurs, causing an additional voltage drop; this cycle is repeated for several additional peaks. Some loads, like variable speed drives for DC series motors [191], are very sensitive to voltage oscillations, therefore for those cases it is desirable that the DC-bus voltage exhibits a low number of oscillations. It is impossible to avoid the voltage perturbation caused by the current transients, however it is possible to design k_p and k_i to impose a critically damped behavior, thus the bus voltage will exhibit only a single peak MO. It must be point out that an overdamped behavior will not exhibit any advantage since they also provide a single peak MO but with a longer safe time; therefore this Section deals only with the critically damped behavior.
The system given in (3-30) must fulfill the condition imposed in (3-38) to have two equal and real poles, *i.e.*, to produce a critically damped waveform. Then, the step response in such a condition to a current transient Δi_{DC} is given in (3-39).

$$k_i = -\frac{k_p^2 \cdot d'}{4 \cdot C} \tag{3-38}$$

$$y = \left(\frac{-\Delta i_{DC}}{C} \cdot t\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t\right) \tag{3-39}$$

The maximum voltage deviation MO occurs when the derivative of the time response is

equal to zero as given in (3-40). The time in which the MO occurs is given in (3-41)

$$\frac{d\,y}{dt} = \left(\frac{-\Delta i_{DC}}{C}\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t\right) \cdot \left[\frac{k_p \cdot d'}{2 \cdot C} \cdot t + 1\right] = 0 \tag{3-40}$$

$$t_{MO} = \frac{-2 \cdot C}{k_p \cdot d'} \tag{3-41}$$

The MO is calculated by evaluating (3-41) in (3-39) to obtain (3-42). In such a way, k_p and k_i are calculated from (3-42) and (3-38), respectively, to ensure a maximum deviation MO, but none condition regarding the safe band $[-\delta_{safe}, \delta_{safe}]$ and safe time t_{safe} are introduced.

$$MO = \frac{2 \cdot \Delta i_{DC}}{k_p \cdot d'} \cdot \exp(-1) \tag{3-42}$$

Therefore, it must be verified that the time t_{delta} required by this critically damped system to reach the safe band is lower, or at least equal, to the minimum time t_{safe} required for the normal operation of the load. Such a condition is calculated from (3-39) as follows:

$$t_{delta} \leq t_{safe} \quad , \quad \delta_{safe} = \left(\frac{-\Delta i_{DC}}{C} \cdot t_{delta}\right) \cdot \exp\left(\frac{k_p \cdot d'}{2 \cdot C} \cdot t_{delta}\right) \tag{3-43}$$

Finally, the values of k_p and k_i must fulfill the constraints imposed in (3-10), (3-19) and (3-20), which are required for the existence of the sliding-mode, and the constraint given in (3-43), which is required for the safe load operation.

3.1.3. Controller design and operation

The previous subsections provide equations to calculate and verify the SMC parameters k_p and k_i. However, those equations depend on the duty cycle d of the bidirectional DC/DC converter (charger/discharger), which changes depending on the values of the DC-bus and ESD voltages. Therefore, k_p and k_i must be continuously adapted to such changes on d, otherwise the conditions required for the existence of the sliding-mode could be not fulfilled, or the desired sliding-mode dynamics could not be achieved.

To address this problem, the equations to calculate and verify the SMC parameters must be normalized in terms of the duty cycle. Such a procedure was performed by defining the variables $x_p = k_p \cdot d'$ and $x_i = k_i \cdot d'$ to rewrite all the system equations, so that x_p and x_i are the unknown variables to be calculated instead of k_p and k_i.

In such a way, x_p and x_i are calculated off-line depending on the capacitance C, the maximum DC-bus current perturbation Δi_{DC}, the maximum voltage deviation MO imposed to the DC-bus, the safe band $[-\delta_{safe}, \delta_{safe}]$ and the maximum time t_{safe} imposed to reach that band. Then, the sliding-mode parameters are adapted on-line as described in Figure **3-7**: $k_p = x_p/d'$ and $k_i = x_i/d'$. Hence, this solution is an adaptive sliding-mode controller (Adaptive SMC in Figure **3-7**).

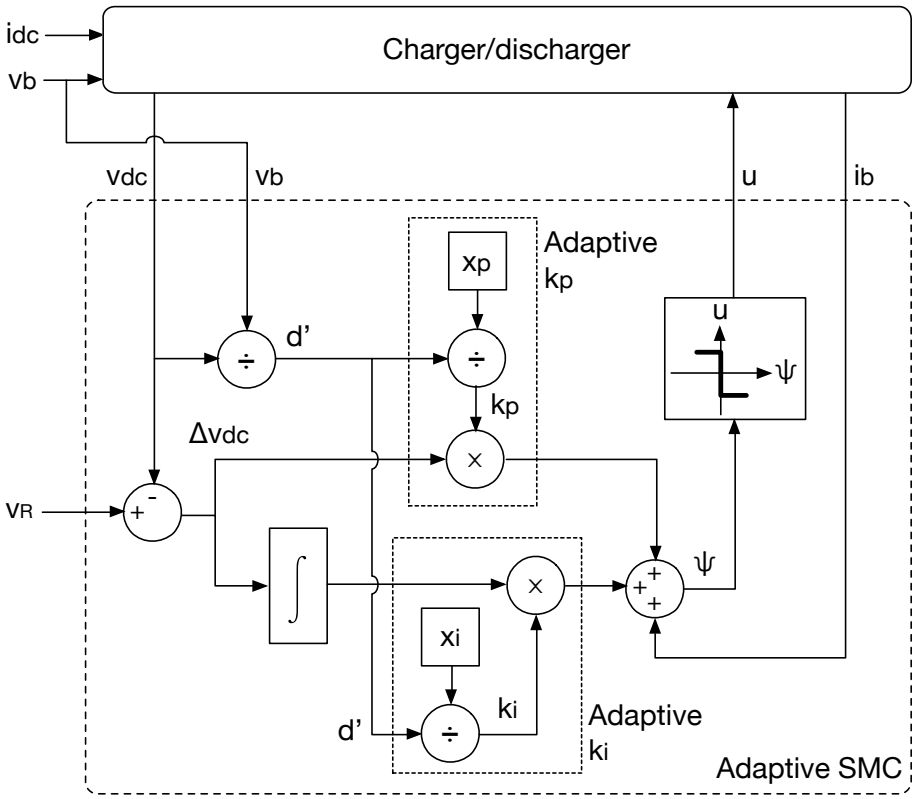


Figure 3-7.: Block diagram of the adaptive sliding-mode controller (Adaptive SMC).

3.1.3.1. Normalized equations for the sliding mode controller

The normalized equations for the sliding-mode constraints and parameters are obtained as follows.

3.1.3.1.1. Constraint equations Constraints (3-10), (3-19) and (3-20) must be fulfilled to guarantee the existence of the sliding-mode. Such restrictions, in terms of x_p and x_i are:

$$-x_p < \frac{v_b}{i_b} \cdot \frac{C}{L} \tag{3-44}$$

$$-x_i < \left(\frac{1}{\Delta v_{DC}}\right) \cdot \left(\frac{v_b}{v_{DC}}\right) \cdot \left[\frac{v_b}{L} + x_p \cdot \frac{i_b}{C}\right] \quad \text{for} \quad \Delta v_{DC} > 0 \tag{3-45}$$

$$-x_i < \left(\frac{-1}{\Delta v_{DC}}\right) \cdot \left(\frac{v_{DC} - v_b}{v_{DC}}\right) \cdot \left[\frac{v_b}{L} + x_p \cdot \frac{i_b}{C}\right] \quad \text{for} \quad \Delta v_{DC} < 0 \tag{3-46}$$

To guarantee that x_p and x_i fulfill such constraints, those expressions must be evaluated in the worst-case conditions for the DC-bus and ESD voltages and currents.

3.1.3.1.2. Underdamped behavior equations The equations for imposing an underdamped behavior to the DC-bus voltage are given in (3-34), (3-37). Such expressions, normalized in terms of the duty cycle, are:

$$\Theta = \sqrt{-\left(\frac{x_p}{2 \cdot C}\right)^2 - \frac{x_i}{C}} \tag{3-47}$$

$$t_{MO} = \frac{1}{\Theta} \cdot \arctan\left(\frac{-2 \cdot C \cdot \Theta}{x_p}\right) \tag{3-48}$$

$$MO = \left(\frac{-\Delta i_{DC}}{C \cdot \Theta}\right) \cdot \exp\left(\frac{x_p}{2 \cdot C} \cdot t_{MO}\right) \cdot \sin\left(\Theta \cdot t_{MO}\right) \tag{3-49}$$

$$\delta_{safe} = \left(\frac{-\Delta i_{DC}}{C \cdot \Theta}\right) \cdot \exp\left(\frac{x_p}{2 \cdot C} \cdot t_{safe}\right) \tag{3-50}$$

Then, expressions (3-49) and (3-50) form a simultaneous non-linear equations system that must be solved to calculate x_p and x_i in terms of C, Δi_{DC}, MO, δ_{safe} and t_{safe}.
An additional constraint, given in (3-32), must be fulfilled to guarantee the underdamped behavior. The normalized version, in terms of x_p and x_i, is given in (3-51).

$$-x_i > \frac{x_p^2}{4 \cdot C} \tag{3-51}$$

3.1.3.1.3. Critically damped behavior equations The equations for imposing a critically damped behavior to the DC-bus voltage are given in (3-42) and (3-38). Such expressions, normalized in terms of the duty cycle, are given in (3-52) and (3-53). Moreover, it must be verified that the time t_{delta} taken by the bus voltage for reaching the safe band is lower or equal to the time t_{safe} required for a normal operation of the load. Such a verification is described in (3-43), and its normalized version is reported in (3-54).

$$x_p = \frac{2 \cdot \Delta i_{DC}}{MO} \cdot \exp\left(-1\right) \tag{3-52}$$

$$x_i = -\frac{x_p^2}{4 \cdot C} \tag{3-53}$$

$$t_{delta} \leq t_{safe} \quad \text{with} \quad \delta_{safe} = \left(\frac{-\Delta i_{DC}}{C} \cdot t_{delta}\right) \cdot \exp\left(\frac{x_p}{2 \cdot C} \cdot t_{delta}\right) \tag{3-54}$$

3.1.3.2. Switching frequency

The zero-centered inverted-comparator used in the scheme of Figure **3-7**, which is in charge of generate the MOSFET signal u must be designed in terms of the switching frequency restrictions of the MOSFET used for the implementation. Therefore, sliding-mode controllers

for DC/DC converters are commonly implemented using hysteresis comparators to constraint the switching frequency according to the physical limitations [198, 199]. This Section adopts such a solution, in which the sliding function given in (3-3), *i.e.*, $\Psi = 0$, is modified as in (3-55), where H represents the width of the hysteresis band. The circuital implementation of (3-55) is presented in Figure **3-8**, which is constructed with a Flip-Flop S-R and two classical comparators to generate the control signal u. Moreover, the figure also presents the steady-state waveform of the switching function produced by the circuit.

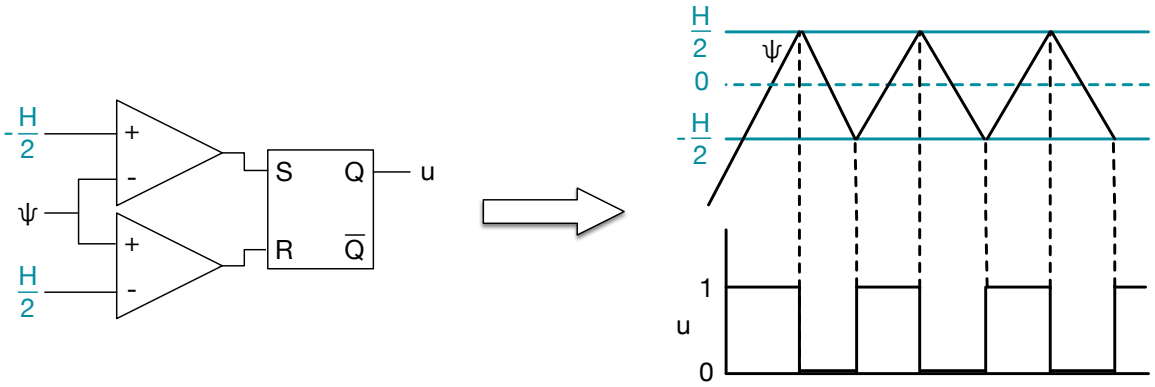


Figure 3-8.: Switching circuit.

$$|\Psi| < \frac{H}{2} \quad \Leftrightarrow \quad -\frac{H}{2} < \Psi < \frac{H}{2} \tag{3-55}$$

In steady-state $v_{DC} = v_R$, hence the switching function can be described as $\Psi = i_b + \delta v_{DC} + C_i$, where δv_{DC} represents the switching ripple of the DC-bus voltage and $C_i = k_i \cdot \int \Delta v_{DC}\, dt$ is a constant value. Therefore, the magnitude H of the variation of Ψ depends on δv_{DC} and on the magnitude of the variation of i_b, which in the scheme of Figure **3-3** corresponds to the switching ripple δi_b of the inductor current. From the analysis of i_b and v_{DC} derivatives, using (3-1) and (3-2), it is noted that the maximum value of the i_b ripple coincides with the minimum value of v_{DC} ripple. Therefore, the magnitude of the oscillation in Ψ is $H = |\delta i_b - \delta v_{DC}|$.

The magnitudes of the switching ripples, calculated from (3-1) and (3-2) as reported in [186, 134], are $\delta i_b = v_b \cdot d / (f_{sw} \cdot L)$ and $\delta v_{DC} = i_{DC} \cdot d / (f_{sw} \cdot C)$, where f_{sw} represents the switching frequency of the DC/DC converter. Then, H is calculated from (3-56) to limit the switching frequency to the value achievable by the MOSFET used in the implementation, it also depending on the inductance and capacitance of the charger/discharger, the maximum voltage supported by the ESD, the minimum voltage allowed to the DC-bus, and the maximum current injected from the DC-bus, *i.e.*, negative i_{DC}. The last condition is due to, for a constant H value, f_{sw} is higher for negative bus currents as concluded from (3-56).

$$H = \frac{1}{f_{sw}} \cdot \left(1 - \frac{v_b}{v_{DC}}\right) \cdot \left(\frac{v_b}{L} - \frac{i_{DC}}{C}\right) \tag{3-56}$$

3.1.3.3. Summary of the design procedure and operation

The design of the SMC is performed to fulfill both steady-state and dynamic conditions. The steady-state conditions are determined by the nominal DC-bus voltage and ESD voltage, which must be know. The dynamic conditions are: a maximum voltage deviation MO in the DC-bus, a safe band for normal operation $[-\delta_{safe}, \delta_{safe}]$, a maximum stabilization time t_{safe} to enter into the safe band after a perturbation, and a maximum bus current perturbation Δi_{DC}. In addition, the parameters of the DC/DC converter are needed, namely the capacitance C, inductance L and the maximum switching frequency f_{sw}.
The procedures to design and operate the SMC are described in the flowchart of Figure **3-9**. The design procedure is performed off-line, calculating first the hysteresis band H. Then, x_p and x_i are calculated for the type of dynamic response that is best for the particular application: underdamped or critically damped behavior. Such a procedure is performed using a restriction-based solver for non-linear equation systems, e.g., fsolve from Matlab®. It must be noted that, depending on the dynamic parameters MO, δ_{safe}, t_{safe} and Δi_{DC}, the system of non-linear equations could not have real solutions for x_p and x_i. This means that the SMC is not able to guarantee those simultaneous constraints. That condition could be addressed using two possible solutions: first, the dynamic parameters could be relaxed, e.g., increasing MO, δ_{safe} or t_{safe}; and second, the DC/DC converter could be modified, e.g., increasing C for reducing MO.
The operation procedure is performed on-line, calculating the complementary duty cycle d' to adapt k_p and k_i for the particular operation conditions. Such adaptive parameters are used to calculate the switching function Ψ, which is provided to the switching circuit to generate the MOSFET control signal u. This operation procedure cloud be performed with analog circuitry or in a digital processor.

3.1.4. Simulation Results

This section illustrates the design of the sliding-mode controller for the charger/discharger using the following parameters and conditions:

- Bidirectional DC/DC converter with the following parameters: $L = 50$ μH and $C = 120$ μF. Moreover, the DC/DC converter is designed to support maximum voltage and current levels equal to 50 V and 10 A, respectively. Therefore, the converter supports a maximum load power of 500 W.

- ESD nominal voltage $v_b = 12$ V and DC-bus nominal voltage $v_R = 48$ V.

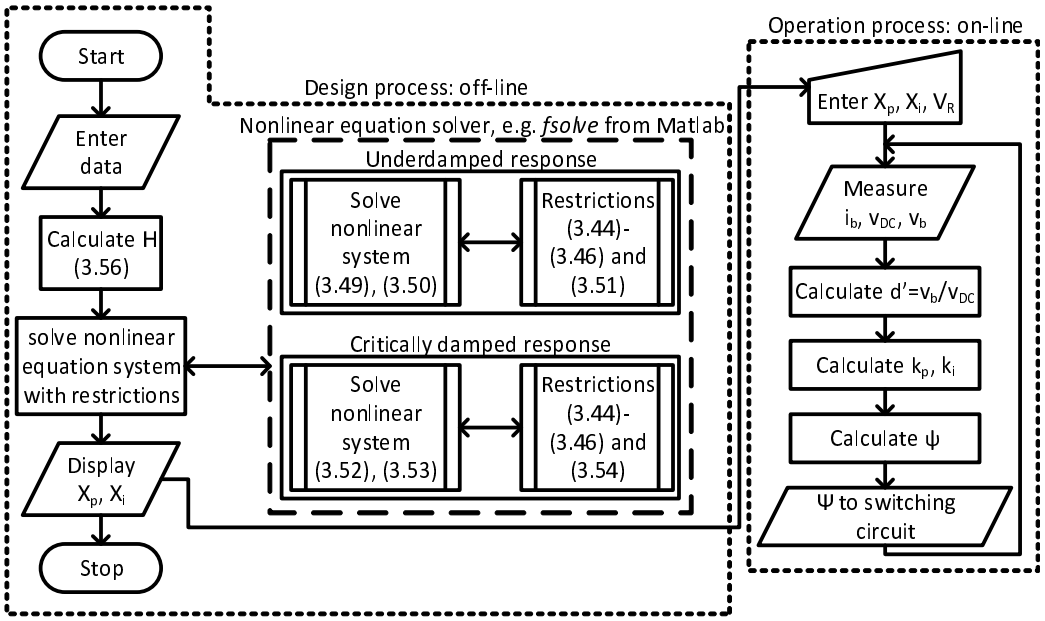


Figure 3-9.: Procedure to design and operate the SMC.

- Maximum DC-bus current transient: steps $\Delta i_{DC} = 1$ A.
- Maximum voltage overshoot (or undershoot) to prevent load or DC/DC converter destruction or turn-off: $MO = 2$ V $\rightarrow$ [46 V, 50 V].
- Safe band for normal load operation: $\delta = 0.3$ V $\rightarrow$ [47.7 V, 48.3 V].
- Maximum time to enter into the safe band after a transient: $t_{safe} = 3$ ms.
- Maximum switching frequency: $f_{sw} \leq 95$ kHz.

The previous values were used to parameterize the equations described in the flowchart of Figure **3-9**. To illustrate both underdamped and critically damped solutions, two sets of parameters were obtained using the non-linear solver fsolve from Matlab®: $[x_{p,u}, x_{i,u}]$ and $[x_{p,c}, x_{i,c}]$. The first set of parameters was obtained using the underdamped equations, while the second set was obtained using the critically damped equations.
For the underdamped solution $x_{p,u} = -0.1820$ and $x_{i,u} = -1.0464 \times 10^3$, where the general restrictions given in (3-44)–(3-46) are fulfilled: $-x_{p,u} < 6.9120$, $-x_{i,u} < 2.2519 \times 10^4$ and $-x_{i,u} < 8.0882 \times 10^4$. Moreover, restriction imposed by (3-51), which grants the underdamped behavior, is also fulfilled: $-x_{i,u} > 69.1627$.
Similarly, for the critically damped solution $x_{p,c} = -0.3679$ and $x_{i,c} = -281.9500 \times 10^3$, where the general restrictions in (3-44)–(3-46) are also fulfilled: $-x_{p,c} < 6.9120$, $-x_{i,c} < 2.0965 \times 10^4$ and $-x_{i,c} < 7.5301 \times 10^4$. Moreover, restriction in (3-54) is also granted: $t_{delta} = 2.85$ ms $< t_{safe} = 3.00$ ms.

Figure **3-10** presents the Matlab® simulation of the equivalent sliding-mode dynamics using both solutions. Those simulation results show the accurate limitation of the maximum voltage deviation to $MO = 2$ V for a current transient of $\Delta i_{DC} = 1$ A. Moreover, the fulfillment of $t_{safe} = 3$ ms is also verified. This simulation puts in evidence the difference between both solutions: the underdamped approach reaches faster the vicinity of the nominal DC-bus voltage, oscillating around such a value; instead the critically damped approach does not oscillates, hence it reaches the nominal voltage in a longer time. However, both solutions enter into the safe time almost at the same time, both respecting the design constraint $t_{delta} \leq t_{safe}$. Therefore, both solutions fulfill the design requirements, hence the selection of one of them depends on the specific load requirements as previously discussed in Subsection 3.1.2.

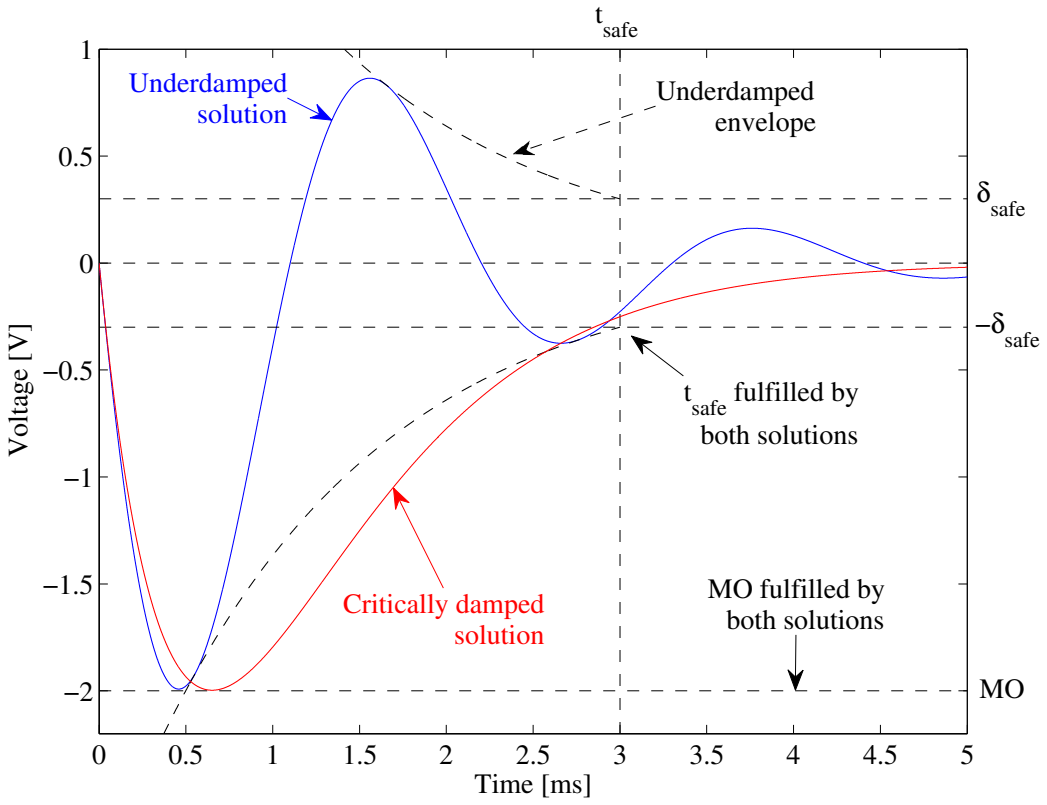


Figure 3-10.: Matlab® simulation of the sliding-mode dynamics.

The charger/discharger non-linear circuit was implemented in the power electronics simulator PSIM® following the scheme previously presented in Figure **3-3**, and the adaptive sliding-mode controller was implemented following the structure given in Figure **3-7**, which corresponds to the online process described in the flowchart of Figure **3-9**. That algorithm was implemented in C language into a C-block of PSIM®. Moreover, to simulate the processing of the SMC into a real digital device, the interaction of the C-block with the DC/DC converter and the hysteresis comparator was performed by means of Analog-to-Digital Con-

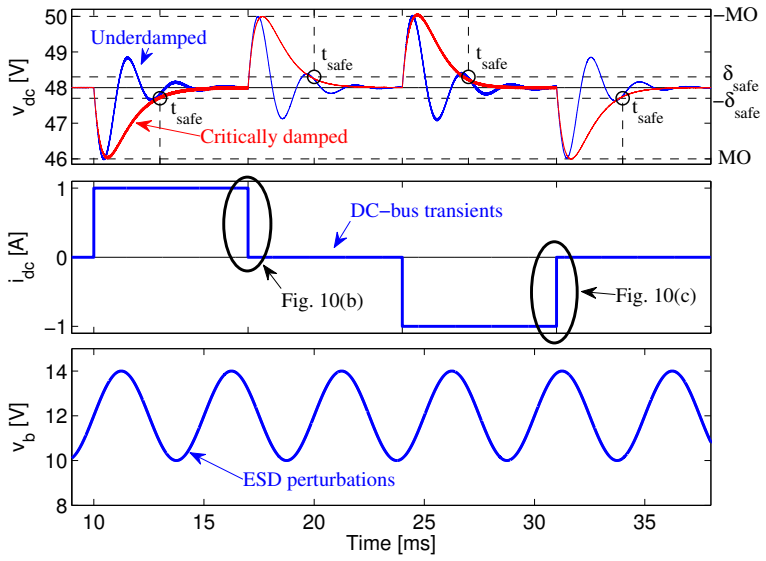
verters (ADC) and a Digital-to-Analog Converter (DAC), which were simulated using quantization blocks of 12 bits with a sampling frequency of 1 MHz. In addition, the hysteresis band was designed using (3-56) to ensure a switching frequency lower than 95 kHz, obtaining $H = 1.9605$. A slightly higher $H = 2$ was used to include a small safe margin.

The electrical scheme was simulated using the two sets of parameters calculated for the SMC, *i.e.*, the underdamped parameters and the critically damped parameters, to validate the sliding-mode dynamics predicted in Figure **3-10**. Those electrical simulations are presented in Figure **3-11**a, where step current transients in the DC-bus are considered for both discharge ($\Delta i_{DC} = 1$ A) and charge ($\Delta i_{DC} = -1$ A) conditions. Moreover, the simulations also consider a 33.33 % sinusoidal perturbation at the ESD voltage v_b (4 V oscillation around the nominal 12 V). It must be noted that such a perturbation is stronger in comparison with the variation of a battery voltage caused by normal operation of stand-alone power system based on renewable energy sources [72, 200] or more general applications [201], however this exigent perturbation is used to illustrate the robustness of both underdamped and critically damped sliding-mode controllers to variations in the ESD voltage.

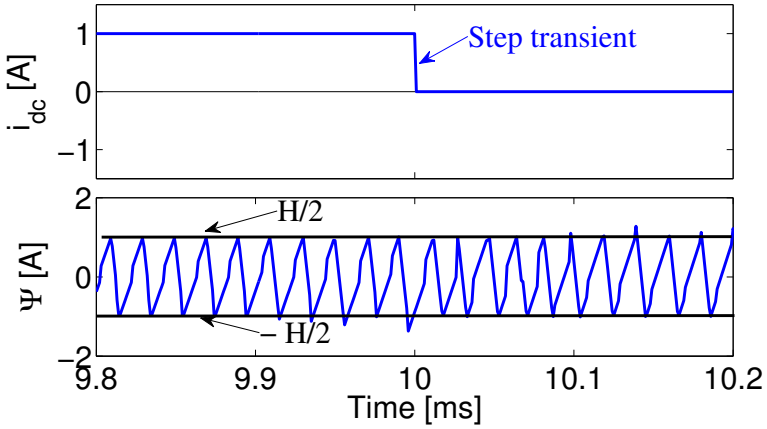
The simulations confirm that both controllers are able to constrain the maximum voltage deviation to $MO = 2$ V for current transients of 1 A. Similarly, both controllers guarantee that the DC-bus voltage enters the safe band within the imposed limit $t_{safe} = 3$ ms. Moreover, the theoretical switching frequencies calculated from (3-56) present errors below 1 % with respect to those circuital simulations for $i_{DC} = [-1$ A, 0 A, 1 A] with $f_{sw} = [86875$ Hz, 90000 Hz, 93125 Hz], respectively. Finally, Figure **3-11**a also shows the battery current i_b for both cases, where the charge and discharge conditions of the battery are observed.

Figures **3-11**b and **3-11**c present the waveforms of the switching function Ψ at both step-down and step-up transients, respectively, generated by the simulation of the critically damped SMC. Those simulation results put in evidence the correct behavior of the SMC even with perturbations in both DC-bus and ESD: the switching function fulfills (3-55), *i.e.*, $-\frac{H}{2} \leq \Psi \leq \frac{H}{2}$, which guarantee the existence of the sliding-mode. Therefore, since the sliding-mode exists, the SMC is able to track the voltage reference rejecting perturbations in both the DC-bus and the ESD as observed in Figure **3-11**a.

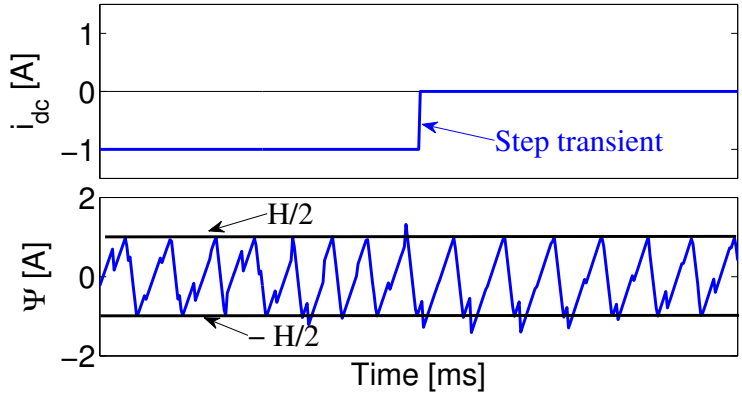
Moreover, the electrical scheme of the charger/discharger was also simulated in open-loop, *i.e.*, with a constant duty cycle $D_{OL} = 1 - \frac{v_b}{v_{DC}}$, to illustrate the magnitude of the DC-bus perturbations caused by both load and ESD transients, which enables to evaluate the effectiveness of the SMC. In this case the charger/discharger operates with a boosting factor $\frac{48\,V}{12\,V} = 4$. Figure **3-12**a shows the open-loop operation of the system for the i_{dc} perturbations considered in Figure **3-11**a: the simulation put in evidence the requirement of the SMC to ensure the desired bus performance imposed by the load (MO, t_{safe}, δ_{safe}). Similarly, Figure **3-12**b shows the open-loop operation of the system for the v_b perturbations considered in Figure **3-11**a. However, in this case a resistive load equal to 48 Ω is adopted to be in agreement with the constraints of the experimental devices used to validate this simulation. Moreover, the experimental device used to emulate the bus (BOP 72-14MG from Kepco®)



(a) Simulation of the charger/discharger with both underdamped and critically damped SMC.

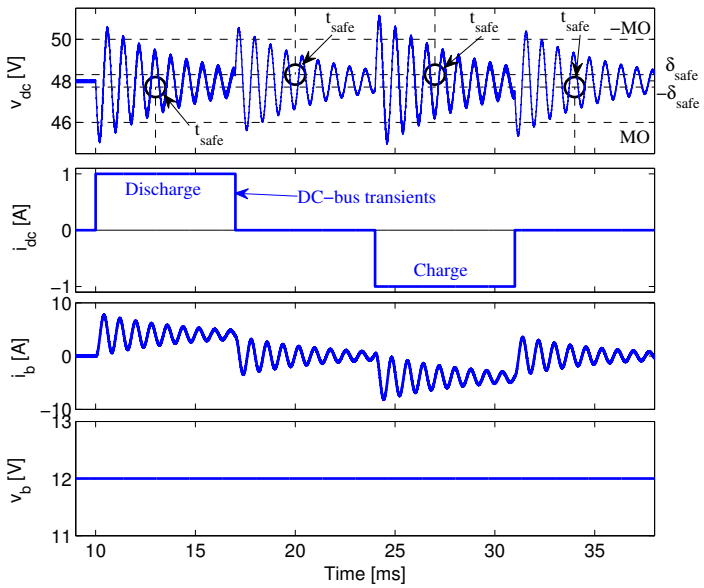


(b) Existence of the sliding-mode in step-down DC-bus perturbation.

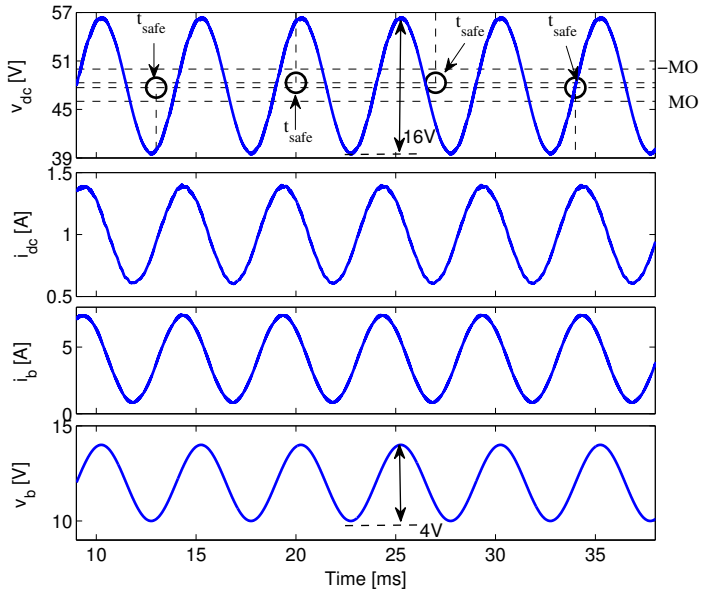


(c) Existence of the sliding-mode in step-up DC-bus perturbation.

Figure 3-11.: PSIM® simulations of the sliding-mode control system.



(a) Simulation under DC-bus current perturbations.



(b) Simulation under ESD perturbations.

Figure 3-12.: Open loop operation of the charger/discharger.

has a parasitic *RLC* network with 5.14 $m\Omega$, 104 μH and 33μF, respectively, which is also included in this simulation. Figure **3-12**b shows that the ESD oscillations are propagated to the DC-bus, generating a 16 V voltage oscillation out of the limits imposed by the desired bus performance. In conclusion, the open-loop operation of the charger/discharger could destroy the DC/DC converter since both perturbations produce voltages higher than the rated limit (50 V), or even a shutdown or over-voltage damage to the load. Hence, the comparison between the open-loop (Figure **3-12**) and closed-loop (Figure **3-11**) simulations

put in evidence the satisfactory rejection of perturbations provided by the proposed SMC. Finally, the previous electrical simulations verify the correctness and accuracy of the proposed design procedure and adaptive structure for the sliding-mode controller.

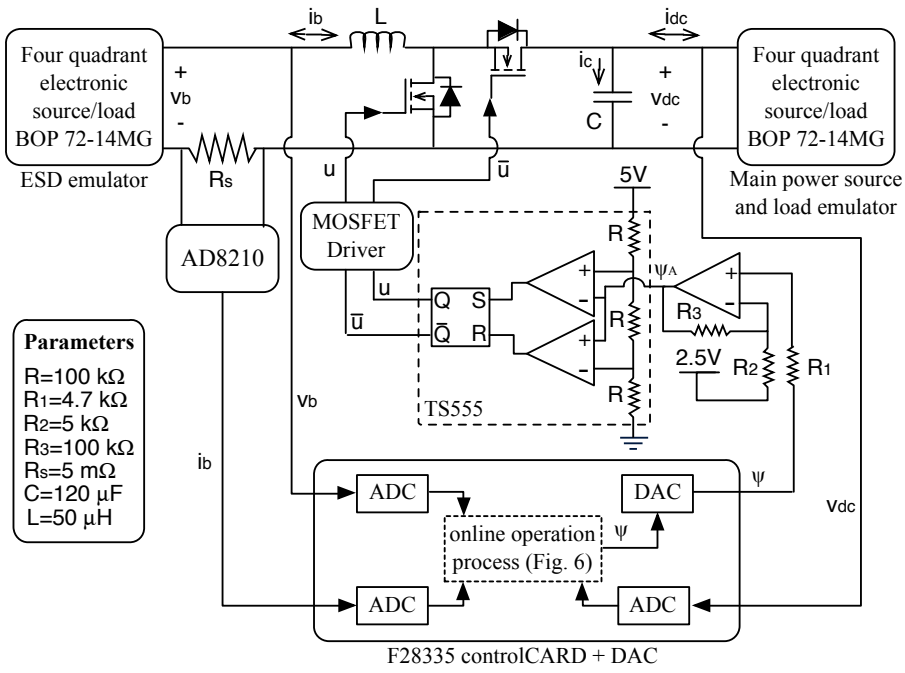
3.1.5. Experimental validation

To experimentally validate the proposed design procedure and adaptive structure for the SMC, a proof-of-concept prototype was developed with the same parameters described in the previous Subsection. Figure **3-13**a describes the prototype setup: the ESD was emulated using a four quadrant electronic source/load BOP 72-14MG from Kepco®, which is able to provide and absorb power. Such an equipment was used to have the possibility of injecting perturbations in the ESD. Similarly, the main power source and load were emulated using another four quadrant electronic source/load BOP 72-14MG, which enables to impose positive and negative power profiles in the DC-bus.

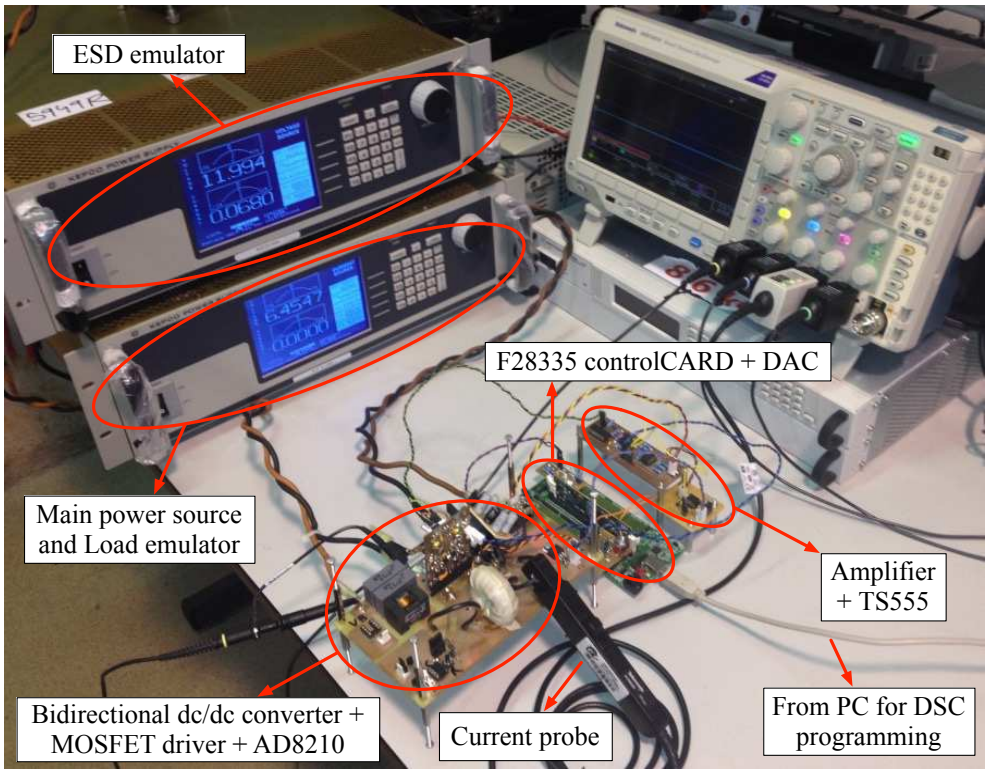
The online adaptive process of the SMC was executed in a F28335 controlCARD from Texas Instruments® programmed in C language, where Ψ is provided to the hysteresis comparator by means of the DAC MCP4822, which has a resolution of 12 bits and a sampling frequency of 20 MHz. The hysteresis comparator was implemented with the integrated circuit TS555, which provides the same circuital structure described in Figure **3-8**. However, the TS555 has the hysteresis centered in 2.5 V with band limits at 3.3 V and 1.6 V when the supply voltage is 5 V. Therefore, an additional amplification circuit was used to scale Ψ from 2 V to 1.7 V and to add an offset of 2.5 V, which corresponds to the scaled switching function Ψ_A provided to the TS555. Then, the output of the TS555, *i.e.*, the binary control signal u, and its complement $\overline{u}$, are provided to the driver HIP4081A, which drives both MOSFETS. The ESD current is measured using a shunt-resistor $R_s = 5\ m\Omega$ and the amplifier AD8210, which is designed to scale bidirectional current measurements. Then, the output of the AD8210, the ESD voltage and the DC-bus voltage are acquired by the controlCARD using the onboard ADCs, which have a resolution of 12 bits and a sampling frequency of 12.5 MHz. Figure **3-13**b presents the physical setup of the experimental system.

Two sets of experiments were carried out to test the performance of the SMC: a first one aimed at validating the SMC performance under step-like current transients in the DC-bus current, and a second one aimed at validating the SMC performance under perturbations in the ESD voltage.

The first experiment considers positive (discharge) and negative (charge) DC-bus currents with step-like transients. Therefore, this experiment has the same conditions considered in the simulations of the previous section. However, due to safety limitations of the BOP 72-14MG source/loads, it is preferable to avoid fast voltage oscillations in the DC-bus voltage, hence the experiment is only focused on evaluate the critically damped SMC. Figure **3-14** presents the waveforms recorded for this experiment, which verify the satisfactory performance of the proposed solution: the DC-bus voltage is constrained to [45.8 V, 50.2 V] for



(a) Electrical scheme.



(b) Physical setup.

Figure 3-13.: Experimental setup.

step current transients of 1.06 A (due to the accuracy provided by the BOP 72-14MG), which represents an error of 3.8 % with respect to the simulations presented in Figure **3-11**a. Such an error is mainly caused by the tolerances in the electronic elements, e.g., capacitor and inductor, hence introducing a safety margin in MO, e.g., reducing it by 4 %, will be enough to ensure the required operation conditions.

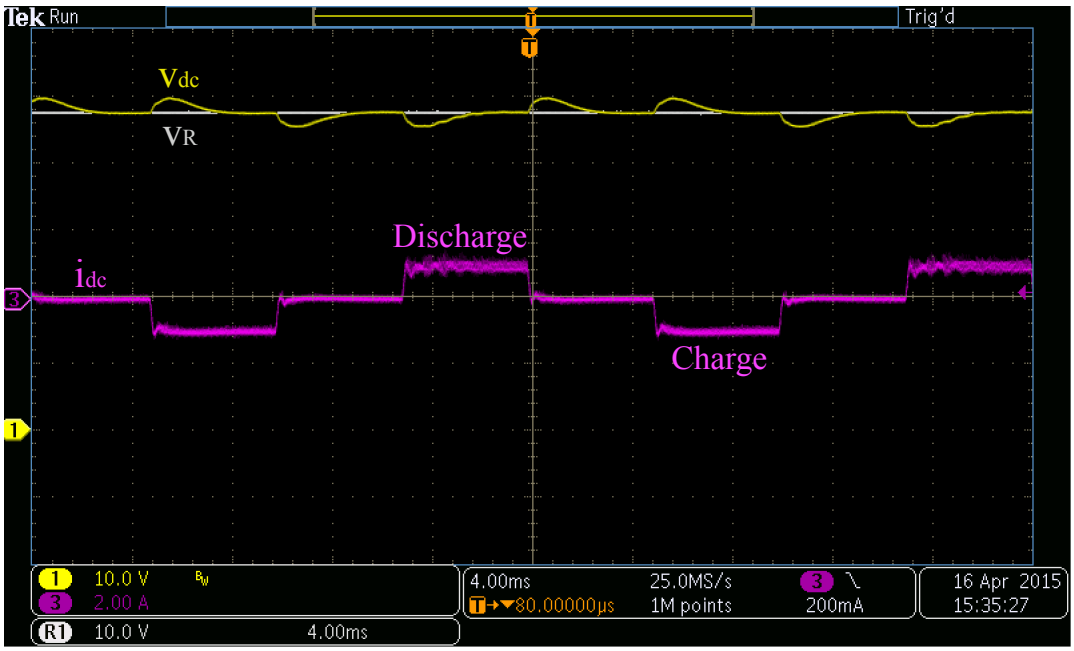
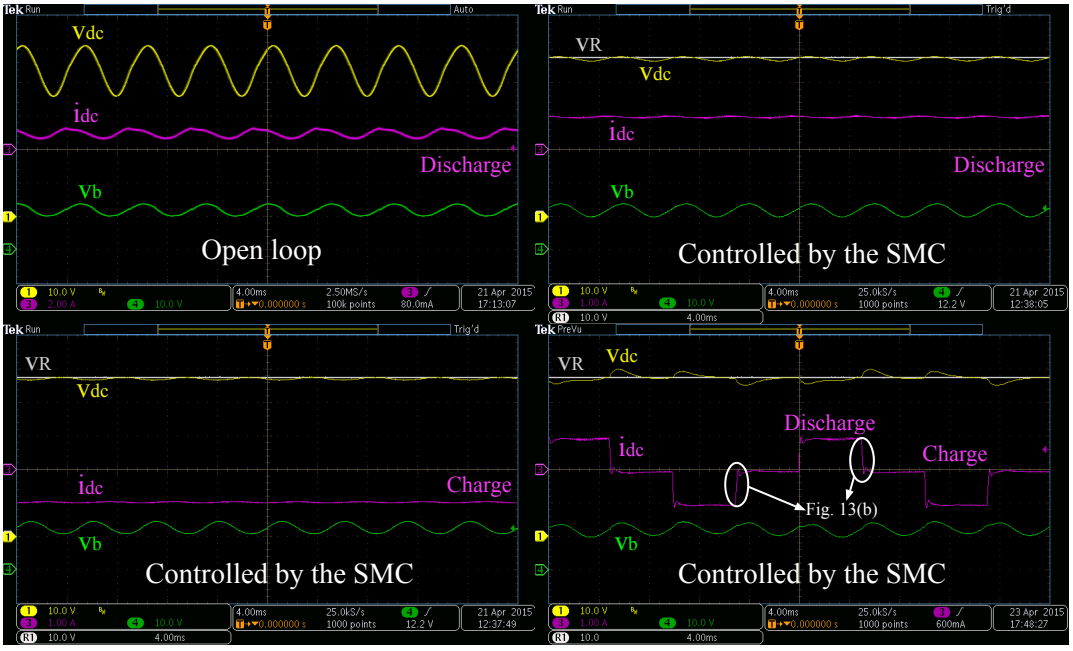


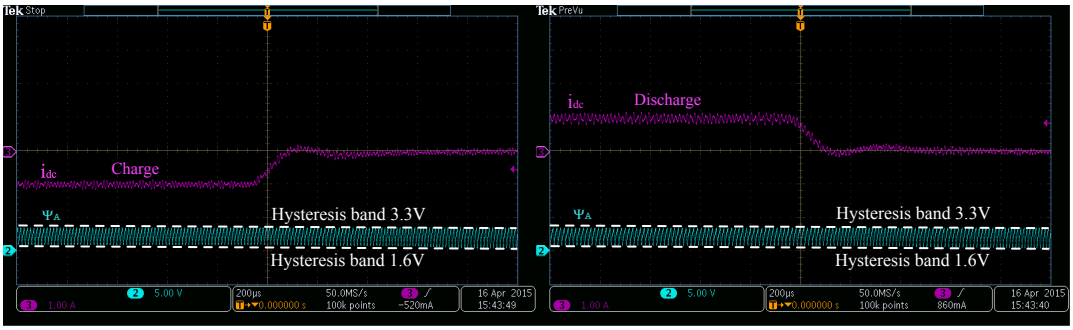
Figure 3-14.: Voltage regulation of the DC-bus for 1 A current steps.

The second experiment considers the same ESD voltage oscillation presented in Figure **3-12**b to validate both open-loop and closed-loop simulations. Figure **3-15**a, at the top-left plot, verifies the large DC-bus voltage oscillations propagated in open-loop operation, which corresponds to the simulation presented in Figure **3-12**b. Moreover, the top-right experiment of Figure **3-15**a shows the satisfactory mitigation of the ESD voltage oscillations provided by the SMC in discharge condition (mitigated to 8.8 % of the original amplitude). Similarly, the experiment at the bottom-left presents the SMC performance under the same ESD perturbation in charge condition (perturbation mitigated to 6.3 % of the original amplitude). The experiment at the bottom-right shows the SMC performance under perturbations in both ESD voltage and DC-bus current, where again the DC-bus voltage is successfully regulated. In addition, Figure **3-15**b presents the experimental scaled switching function for both step-up and step-down current transients. Such waveforms are in agreement with Figures **3-11**b and **3-11**c: the switching function is constrained within the hysteresis band, hence the sliding-mode exists and the SMC is able to guarantee the required DC-bus behavior. Moreover, the waveforms in Figure **3-15**b, and Figures **3-11**b and **3-11**c validate the circuit used to implement the switching control of Figure **3-8** since the same results are obtained.
Finally, the simulation results presented in Figure **3-11** validate the proposed design pro-

cedure and adaptive structure for the sliding-mode controller based on the surface given in (3-3). Moreover, the experiments reported in Figures **3-14** and **3-15** validate such simulations results since the same behavior is obtained. Finally, those simulations and experiments demonstrate the correctness of the controller design and implementation.



(a) Open-loop and closed-loop waveforms.



(b) Verification of the sliding-mode existence.

Figure 3-15.: Voltage regulation of the DC-bus under ESD voltage perturbations.

3.2. Control of a charger/discharger DC/DC converter with improved disturbance rejection for bus regulation

To avoid the bandwidth constraint imposed by the classical cascade structure reported in Figure **3-1**, the solution reported in Section 3.1 uses a unified sliding-mode controller for the charger/discharger, as illustrated in Figure **3-16**. Since this solution does not require any model approximation, the voltage control can be designed with the highest bandwidth possible, which provides a faster response compared with the cascade solution. Therefore, the unified controller has higher speed, which improves its ability to compensate perturbations. Moreover, since the SMC is designed using the non-linear model of the DC/DC converter, it ensures the system stability and desired performance in any operating conditions, which provides a safe operation in the entire operation range.

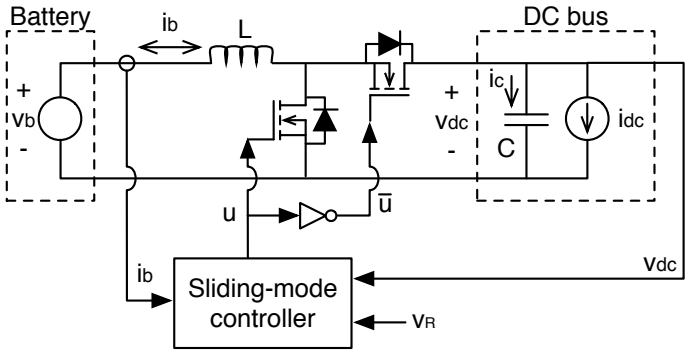


Figure 3-16.: Structure of the unified sliding-mode controller for the charger/discharger proposed in Section3.1

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The SMC designed in Section 3.1 [88] is based on the sliding function Ψ_{SM} and sliding surface Φ_{SM} presented in (3-3), which are recalled in this Section as (3-57) and (3-58), respectively. In those expressions, i_b represents the battery current, which is equal to the inductor current as observed in Figure **3-1** and Figure **3-16**; v_{dc} represents the DC bus voltage; and v_R represents the desired bus voltage, i.e., the reference value. Moreover, k_p and k_i are parameters designed to impose a desired dynamic response on the DC bus voltage.

$$\Psi_{SM} = i_b + k_p \cdot (v_R - v_{dc}) + k_i \cdot \int (v_R - v_{dc})\ dt \tag{3-57}$$

$$\Phi_{SM} = \{\Psi_{SM} = 0\} \tag{3-58}$$

However, both the cascade and unified control solutions have a main disadvantage: the controller is not able to instantaneously identify a perturbation in the bus current; therefore, the controller reacts to the perturbation in the bus voltage, which causes large voltage

disturbances. For example, in the cascade solution, the current controller acts on the battery current only when the voltage (or power) controller detects a perturbation in the bus voltage (or power); hence, the compensation provided by the current controller is delayed, which in turn delays the voltage (or power) compensation. The same behavior is observed in the results of the unified SMC reported in Section 3.1 [88].

Figure **3-17** presents the simulation of the unified SMC reported in Section 3.1, which was designed to provide a bus voltage equal to $48V$. The controller must provide a maximum voltage deviation of $2V$ for current transients in the bus up to $1A$. The simulation shows a correct behavior up to $20ms$, when a $3A$ current transient occurs in the DC bus, causing a voltage drop to almost $43V$, which is expected.

The magnified area of the simulation (from $19.8ms$ to $21.0ms$) also reveals the reason for the large voltage deviation caused by current transients: the change in the bus current must be compensated by the battery current, which due to power balance corresponds to a theoretical battery current of $i_{b,th} = i_{dc} \cdot v_{dc}/v_b$. However, as observed in the magnified region of the figure, the battery current imposed by the controller is considerably slower than the theoretical battery current; hence, the current difference must be provided by the bus capacitor, producing a voltage drop. This behavior is unavoidable in the structure of Figure **3-16** because, as observed in the magnified region of Figure **3-17**, the battery current is defined by the error between the bus voltage and the reference. Therefore, the battery current changes only when a deviation in the bus voltage occurs.

This undesired behavior can be removed by introducing the measurement of the bus current into the control scheme, which will enable the controller to impose a faster change in the battery current. This Section proposes a new sliding-mode controller based on such a concept.

3.2.1. Improved sliding mode controller

With the aim of improving the current disturbance rejection for the charger/discharger, the control structure proposed in Figure **3-18** considers the measurement of the bus current. Moreover, the controller must be designed to take advantage of this new information. In addition, since the charger/discharger must be controlled in both positive and negative power flows by the same controller, and because the bandwidth of the system must be set as high as possible, i.e., no linearization processes involved, the proposed controller is based on sliding-mode theory.

The proposed SMC is based on the sliding function Ψ and surface Φ presented in (3-59) and (3-60), respectively. This new surface includes the bus current i_{dc}, a new parameter k_b weighting the battery current i_b, the error between the bus voltage v_{dc} and the reference value v_R weighted by the parameter k_p, and the integral of the error between v_{dc} and v_R weighted by the parameter k_i. Then, the parameters k_b, k_p and k_i must be designed to impose

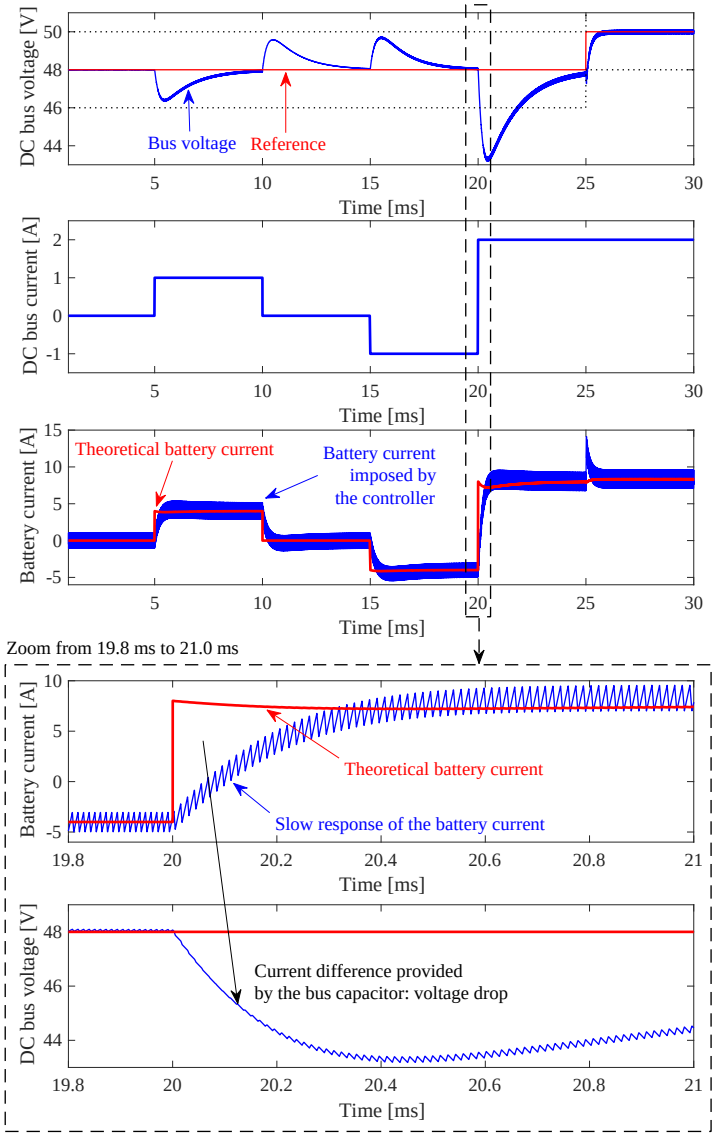


Figure 3-17.: Simulation of the controller presented in section 3.1.

a desired dynamic response on the bus voltage.

$$\Psi = (k_b \cdot i_b - i_{dc}) + k_p \cdot (v_R - v_{dc}) + k_i \cdot \int (v_R - v_{dc})\, dt \tag{3-59}$$

$$\Phi = \{\Psi = 0\} \tag{3-60}$$

The viability of implementing a SMC based on the surface Φ presented in (3-60) depends on three conditions [185]: transversality, reachability and equivalent control. These conditions are analyzed in the following subsections.

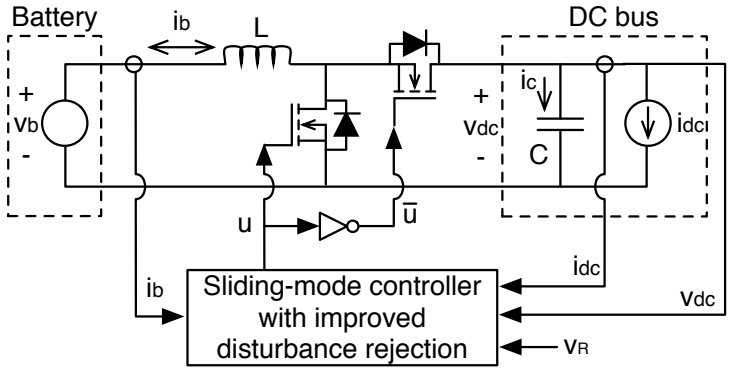


Figure 3-18.: Proposed structure of a sliding-mode controller with improved disturbance rejection for the charger/discharger.

3.2.1.1. Converter model and sliding function expressions

The first step in evaluating the viability of the sliding-mode controller is to provide an explicit expression for the sliding function derivative, which also requires a switched model for the DC/DC converter [186, 134] (see (3-1) and (3-2)).

From the charge and flux balances in the capacitor and inductor, respectively [134], the steady-state battery and bus voltages and currents are related by (3-14).

The derivative of the sliding function (3-59) is presented in (3-61), which considers the reference value to be constant, i.e., $\frac{dv_R}{dt} = 0$. This assumption is valid since a DC bus is commonly controlled to provide a constant voltage [202]. In fact, the objective of the proposed controller is to keep the bus voltage constant even under transients of the load current (or power). Finally, the explicit expression (3-62) for the sliding function derivative is obtained by substituting (3-1) and (3-2) into (3-61).

$$\frac{d\Psi}{dt} = k_b \cdot \frac{di_b}{dt} - \frac{di_{dc}}{dt} - k_p \cdot \frac{dv_{dc}}{dt} + k_i \cdot (v_R - v_{dc}) \tag{3-61}$$

$$\frac{d\Psi}{dt} = \frac{k_b}{L} \cdot [v_b - v_{dc} \cdot (1-u)] - \frac{di_{dc}}{dt} - \frac{k_p}{C} \cdot [i_b \cdot (1-u) - i_{dc}] + k_i \cdot (v_R - v_{dc}) \tag{3-62}$$

3.2.1.2. Transversality condition

The transversality condition analyzes the ability to act on the sliding function to reach the sliding surface. This conditions is formalized in (3-7), and it is rewritten in this subsection in (3-63), which ensures that the converter control signal u is present in the sliding function derivative [203]. If the transversality condition (3-63) is fulfilled, then the SMC is able to modify the sliding function trajectory by changing its derivative to reach the surface. Otherwise, the SMC output has no effect on the sliding function trajectory, and the bus voltage will not be controllable.

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) \neq 0 \tag{3-63}$$

By substituting (3-62) into (3-63), the transversality expression is obtained as presented in (3-64).This expression can be equal to zero since the battery current is negative in the charging stage. Therefore, such an expression must be analyzed to define the constraints that ensure the fulfillment of the transversality condition (3-63).

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = \frac{k_b \cdot v_{dc}}{L} + \frac{k_p \cdot i_b}{C} \tag{3-64}$$

Another important implication of the transversality value is the definition of the reachability conditions, which are imposed by the transversality sign [185], as will be discussed in the following subsection. In addition, these reachability conditions impose the control law of the MOSFETs. Therefore, to ensure a consistent implementation circuitry for the sliding-mode controller, the transversality must exhibit the same sign in any condition. This is addressed by forcing expression (3-64) to exhibit a positive sign in the charging ($i_b < 0$), stand-by ($i_b = 0$) and discharging ($i_b > 0$) stages. A positive sign is selected rather than a negative sign to simplify the implementation.
The constraints that ensure a positive sign for the transversality in the three possible stages of the charger/discharger are as follows:

- Stand-by stage ($i_b = 0$): since L and v_{dc} are positive quantities, the parameter k_b must be set as a positive quantity, as reported in (3-65).

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = \frac{k_b \cdot v_{dc}}{L} > 0 \quad , \quad \begin{cases} i_b = 0 \\ k_b > 0 \end{cases} \tag{3-65}$$

- Charging stage ($i_b < 0$): since L, C, v_{dc} and k_b are positive quantities, the parameter k_p must be set as a negative quantity, as reported in (3-66).

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = \frac{k_b \cdot v_{dc}}{L} + \frac{k_p \cdot i_b}{C} > 0 \quad , \quad \begin{cases} i_b < 0 \\ k_b > 0 \\ k_p < 0 \end{cases} \tag{3-66}$$

- Discharging stage ($i_b > 0$): since L, C, v_{dc} and k_b are positive quantities, the parameter k_p must fulfill the constraint presented in (3-67) to ensure the positive sign of the transversality.

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) > 0 \quad , \quad \begin{cases} i_b > 0 \\ k_b > 0 \\ k_p > -\frac{C}{L} \cdot \frac{v_b}{i_b} \end{cases} \tag{3-67}$$

In conclusion, the constraints reported in (3-68) must be fulfilled to ensure that the transversality condition (3-63) is satisfied and to simultaneously impose a positive sign of (3-64) for any operating conditions.

$$k_b > 0 \ \wedge \ -\frac{C}{L} \cdot \frac{v_b}{i_b} < k_p < 0 \quad \Rightarrow \quad \frac{d}{du}\left(\frac{d\Psi}{dt}\right) > 0 \tag{3-68}$$

3.2.1.3. Reachability conditions

As it was presented in the Subsection 3.1.1.2, the reachability condition must be satisfied with the aim of guarantee the global stability of SMC. Since a positive sign of the transversality was imposed, the conditions presented in (3-11) must be fulfilled, which are rewritten here in (3-69) and (3-70).

$$\lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \tag{3-69}$$

$$\lim_{\Psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \tag{3-70}$$

Substituting the expression of $\frac{d\Psi}{dt}$ presented in (3-62), evaluated for $u = 1$, into (3-69) leads to (3-71). This inequality enables establishing a restriction that must be fulfilled to ensure the surface reachability.

$$\lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} = \frac{k_b \cdot v_b}{L} - \frac{di_{dc}}{dt} + \frac{k_p \cdot i_{dc}}{C} + k_i \cdot (v_R - v_{dc}) > 0 \tag{3-71}$$

By using the charge and flux balance principles presented in (3-14), expression (3-71) is rewritten as constraint (3-72), which defines the relation between the maximum derivative of i_{dc} and the parameter k_i that ensures the existence of the sliding mode. In this expression, the terms $(1-d)$ and $\left[\frac{k_b \cdot v_{dc}}{L} + \frac{k_p \cdot i_b}{C}\right]$ are positive, where the latter one is the transversality (3-64). However, the term $(v_R - v_{dc})$ could be positive or negative; hence, the worst case (lower value) to be evaluated corresponds to the condition in which $(v_R - v_{dc})$ has an opposite sign to k_i.

$$\frac{di_{dc}}{dt} < (1-d) \cdot \left[\frac{k_b \cdot v_{dc}}{L} + \frac{k_p \cdot i_b}{C}\right] + k_i \cdot (v_R - v_{dc}) \tag{3-72}$$

A particular case for (3-72) occurs for a step perturbation in the DC bus current, which is the fastest (and strongest) perturbation possible: in this case, restriction (3-72) is not fulfilled in the very short time $t_{step} \approx 0$ in which the step occurs because $\frac{di_{dc}}{dt} \to \infty$, but after that short time, the current is almost constant, i.e., $\frac{di_{dc}}{dt} \approx 0$. Considering that Section 3.2.2 will demonstrate that k_i must be negative (3-86) for stability reasons, expression (3-72) is modified to define the maximum magnitude of k_i that ensures the reachability of the surface,

presented in (3-73), which corresponds to the most restrictive case: $(v_R - v_{dc})$ with opposite sign to k_i, i.e., $(v_R - v_{dc}) > 0 \Rightarrow v_{dc} < v_R$.

$$|k_i| < \frac{(1-d)\cdot\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right]}{(v_R - v_{dc})}\ ,\ v_{dc} < v_R \tag{3-73}$$

The another case $(v_R - v_{dc}) \leq 0 \Rightarrow v_{dc} \geq v_R$ produces the inequality provided in (3-74), which is always fulfilled.

$$|k_i|\cdot(v_{dc} - v_R) > -(1-d)\cdot\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right]\ ,\ v_{dc} \geq v_R \tag{3-74}$$

To summarize, constraint (3-73) provides the maximum magnitude of k_i to ensure reachability when the bus voltage is lower than the reference, i.e., $v_{dc} < v_R$.

The second reachability condition (3-70) is also analyzed by evaluating the expression of $\frac{d\Psi}{dt}$ provided in (3-62) for $u = 0$:

$$\lim_{\Psi\to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} = \frac{k_b}{L}\cdot[v_b - v_{dc}] - \frac{di_{dc}}{dt} - \frac{k_p}{C}\cdot[i_b - i_{dc}] + k_i\cdot(v_R - v_{dc}) < 0 \tag{3-75}$$

Using the charge and flux balance principles presented in (3-14), expression (3-75) is rewritten as constraint (3-76), which defines the relation between the minimum derivative of i_{dc} and the parameter k_i that ensures the existence of the sliding mode. In this expression, the term $(-d)$ is negative, and the term $\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right]$ is positive. However, the term $(v_R - v_{dc})$ could be positive or negative; hence, the worst case (higher value) to be evaluated corresponds to the condition in which $(v_R - v_{dc})$ has the same sign as k_i.

$$\frac{di_{dc}}{dt} > (-d)\cdot\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right] + k_i\cdot(v_R - v_{dc}) \tag{3-76}$$

In the particular case for (3-76) with a step perturbation in the bus current, the restriction is not fulfilled in the very short time $t_{step} \approx 0$ in which the step occurs because $\frac{di_{dc}}{dt} \to -\infty$, but after that short time, the current is almost constant, i.e., $\frac{di_{dc}}{dt} \approx 0$. Considering that k_i is negative, expression (3-76) is modified to define the maximum magnitude of k_i that ensures the reachability of the surface, presented in (3-77), which corresponds to the most restrictive case: $(v_R - v_{dc})$ with the same sign as k_i, i.e., $(v_R - v_{dc}) < 0 \Rightarrow v_{dc} > v_R$.

$$|k_i| < \frac{(-d)\cdot\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right]}{-(v_{dc} - v_R)}\ ,\ v_{dc} > v_R \tag{3-77}$$

The another case $(v_R - v_{dc}) \geq 0 \Rightarrow v_{dc} \leq v_R$ produces the inequality in (3-78), which is always fulfilled.

$$|k_i|\cdot(v_R - v_{dc}) > (-d)\cdot\left[\frac{k_b\cdot v_{dc}}{L} + \frac{k_p\cdot i_b}{C}\right]\ ,\ v_{dc} \leq v_R \tag{3-78}$$

To summarize, constraint (3-77) provides the maximum magnitude of k_i to ensure reachability when the bus voltage is higher than the reference, i.e., $v_{dc} > v_R$.

In conclusion, the system is able to reach the surface $\Psi = 0$ when the restrictions presented in (3-72)-(3-73) and (3-76)-(3-77) are fulfilled.

3.2.1.4. Equivalent control

According to Subsection 3.1.1.3, the equivalent control condition analyzes the saturation of the control signal to ensure that the system is always in a closed-loop state. The equivalent control corresponds to the average value u_{eq} of the binary control signal u within the switching period T_{sw}, which is reported in (3-79). Then, the equivalent control condition imposes that u_{eq} must be constrained within the possible values of u [203, 185], which in DC/DC converters are $u = 0$ and $u = 1$. The equivalent control condition is formalized in (3-80).

$$u_{eq} = \frac{1}{T_{sw}} \cdot \int_0^{T_{sw}} u \, dt \tag{3-79}$$

$$0 < u_{eq} < 1 \tag{3-80}$$

It is evident that the equivalent control (3-79) is equal to the converter duty cycle, i.e., $u_{eq} = d$. Therefore, fulfilling the equivalent control condition (3-80) prevents saturation of the duty cycle, which ensures that the controller is continuously acting on the system to compensate perturbations. Otherwise, if the duty cycle is saturated, then the converter will operate without any control.
The equivalent control condition assumes the existence of the sliding mode, which ensures that the sliding function is into the sliding surface and its trajectory is parallel to the surface [185]. These conditions are formalized in (3-6).
The expression for u_{eq} is obtained using the following procedure: first, the switched differential equations (3-1) and (3-2) are averaged within the switching period; then, the expression for $\frac{d\Psi}{dt}$ in (3-61) is recalculated based on these averaged expressions, changing u by the equivalent control u_{eq}. Finally, u_{eq} is obtained by evaluating (3-6) with the averaged version of $\frac{d\Psi}{dt}$. The expression of u_{eq} for the proposed SMC is presented in (3-81).

$$u_{eq} = \frac{1}{\frac{k_b \cdot v_{dc}}{L} + \frac{k_p \cdot i_b}{C}} \cdot \left[-\frac{k_b \cdot (v_b - v_{dc})}{L} + \frac{di_{dc}}{dt} + \frac{k_p \cdot (i_b - i_{dc})}{C} - k_i \cdot (v_R - v_{dc}) \right] \tag{3-81}$$

Finally, evaluating the equivalent control condition (3-80) considering the expression for u_{eq} presented in (3-81) leads to the same restrictions provided in (3-72)-(3-73) and (3-76)-(3-77). This result is expected since in [185] it was demonstrated that any SMC for DC/DC converters, which fulfills the reachability conditions, also fulfills the equivalent control condition. In any case, this subsection is devoted to demonstrating that the proposed sliding-mode controller avoids duty-cycle saturation.

3.2.1.5. Summary

The proposed sliding-mode controller based on the sliding function (3-59) and sliding surface (3-60) must fulfill the constraints reported in (3-68), (3-72)-(3-73) and (3-76)-(3-77) to ensure the sliding function controllability, surface reachability and non-saturation of the duty cycle. Moreover, the existence of the sliding mode guarantees operation of the system within the sliding surface and forces its trajectory to be parallel to the surface. These conditions ensure global stability of the system [79].

3.2.2. Design of the sliding mode dynamics

The sliding-mode dynamics are imposed with the parameters k_b, k_p and k_i. From the sliding function (3-59), it is observed that selecting parameter k_b equal to the complement of the converter duty cycle, as provided in (3-82), forces the term $k_b \cdot i_b - i_{dc}$ to become equal to the average current in the bus capacitor $i_{C,T_{sw}} = C \cdot \frac{dv_{dc}}{dt}$ (within the switching period T_{sw}), which only disregards the switching ripple. This value for k_b fulfills the restriction imposed in (3-68) and simultaneously enables combining both i_b and i_{dc} measurements into a single current value to simplify the mathematical analysis.

$$k_b = 1 - d = \frac{v_b}{v_{dc}} > 0 \tag{3-82}$$

The sliding-mode controller imposes the closed-loop dynamics given in (3-6), which are both linear for the selected sliding function. By using the k_b value presented in (3-82), the function (3-59) becomes the expression (3-83). Since this equation is also linear, the equivalent dynamics are expressed in the Laplace domain as reported in (3-84). Finally, the closed-loop transfer function $G_{dc}(s)$ between the DC bus voltage and the reference value is provided in (3-85).

$$C \cdot \frac{dv_{dc}}{dt} + k_p \cdot (v_R - v_{dc}) + k_i \cdot \int (v_R - v_{dc})\ dt = 0 \tag{3-83}$$

$$C \cdot s \cdot V_{dc}(s) + \left[k_p + \frac{k_i}{s}\right] \cdot [V_R(s) - V_{dc}(s)] = 0 \tag{3-84}$$

$$G_{dc}(s) = \frac{V_{dc}(s)}{V_R(s)} = \frac{-\frac{k_p}{C} \cdot s - \frac{k_i}{C}}{s^2 - \frac{k_p}{C} \cdot s - \frac{k_i}{C}} \tag{3-85}$$

Considering that k_p is negative (3-68), transfer function (3-85) indicates that a negative k_i value is required to ensure stable sliding-mode dynamics, i.e., negative closed-loop poles. This condition is formalized in (3-86).

$$k_i < 0 \tag{3-86}$$

The following subsections address the design of $G_{dc}(s)$ to obtain a desired dynamic response in the DC bus voltage.

3.2.2.1. Selection of the type of dynamic response

The two poles of the transfer function $G_{dc}(s)$ can be designed in three different ways depending on the damping ratio ρ: complex-conjugate ($\rho < 1$), real and equal ($\rho = 1$), or real and different ($\rho > 1$). To study the dynamic behavior of the closed-loop system depending on the type of damping ratio, $G_{dc}(s)$ is rewritten as shown in (3-87), where ω_n represents the natural frequency of the system. To exclusively analyze the effect of the damping ratio, the transfer function is normalized in terms of the natural frequency using the normalized Laplace variable $s_N = \frac{s}{\omega_n}$ as in (3-88).

$$G_{dc}(s) = \frac{2 \cdot \rho \cdot \omega_n \cdot s + {\omega_n}^2}{s^2 + 2 \cdot \rho \cdot \omega_n \cdot s + {\omega_n}^2} \tag{3-87}$$

$$G_{dc,N}(s) = \frac{2 \cdot \rho \cdot s_N + 1}{{s_N}^2 + 2 \cdot \rho \cdot s_N + 1} \tag{3-88}$$

Figure **3-19** shows the normalized dynamic response of $G_{dc}(s)$ to a step perturbation for different damping ratios: the higher the damping ratio is, the lower is the maximum overshoot. However, also note that $\rho = 1$ produces an overshoot equal to 13.5 %, and even $\rho = 1.5$ produces an overshoot equal to 7.6 %. Therefore, to ensure a low overshoot, it is necessary to design $G_{dc}(s)$ with $\rho > 1$, which requires the design of two real and different poles.

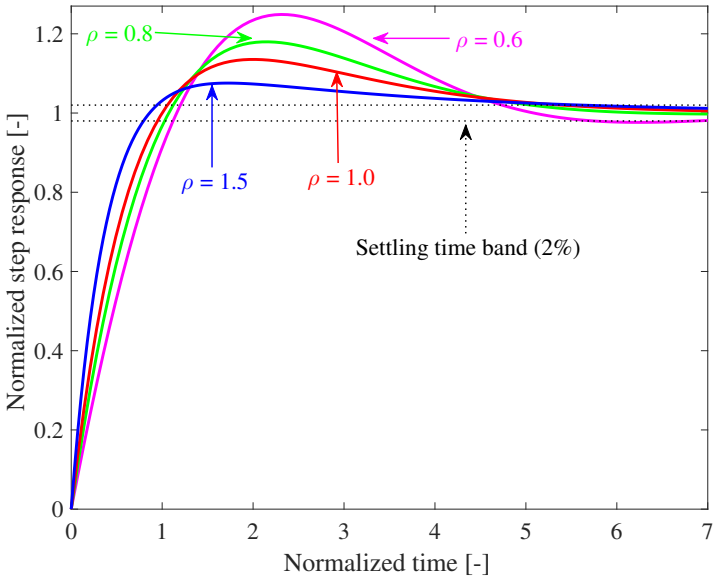


Figure 3-19.: Effect of damping ratio on the dynamic response of $G_{dc}(s)$.

The results presented in Figure **3-19** are valid for any natural frequency; hence, it is a general analysis. Finally, in the following subsections, the two real poles are designed to impose a given maximum overshoot and settling time, both defined by the load requirements.

3.2.2.2. Design of the maximum overshoot

It is important to limit the maximum (and minimum) DC bus voltage caused by perturbations in the bus current. These constraints depend on the voltage levels required by the load for normal operation. Therefore, a maximum overshoot must be imposed on $G_{dc}(s)$.
The overshoot is designed in terms of the poles of $G_{dc}(s)$ and considering a step perturbation, which is the strongest (and fastest) perturbation possible. For this analysis, $G_{dc}(s)$ is expressed in terms of the two real poles $s_1 = -P_1$ and $s_2 = -P_2$ of the characteristic equation presented in (3-89). The objective of this subsection is to find an expression for P_1 and P_2 that limits the overshoot Δv_{dc} under a given maximum value.

$$G_{dc}(s) = \frac{(P_1 + P_2) \cdot s + P_1 \cdot P_2}{s^2 + (P_1 + P_2) \cdot s + P_1 \cdot P_2} \tag{3-89}$$

The step response $Y(s)$ in the Laplace domain is calculated in (3-90), and the time response to a unitary step is presented in (3-91). This time-domain waveform will be used to design P_1 and P_2.

$$Y(s) = \frac{(P_1 + P_2) \cdot s + P_1 \cdot P_2}{s^2 + (P_1 + P_2) \cdot s + P_1 \cdot P_2} \cdot \frac{1}{s} \tag{3-90}$$

$$y(t) = 1 + \left(\frac{P_1}{P_2 - P_1}\right) \cdot e^{-P_1 \cdot t} - \left(\frac{P_2}{P_2 - P_1}\right) \cdot e^{-P_2 \cdot t} \tag{3-91}$$

To normalize the design of the maximum overshoot, the relation between the poles $-P_1$ and $-P_2$ is defined as the m value presented in (3-92). Then, the time response of the closed-loop system is rewritten as shown in (3-93).

$$m = \frac{P_2}{P_1} \tag{3-92}$$

$$y(t) = 1 + \left(\frac{1}{m - 1}\right) \cdot e^{-P_1 \cdot t} - \left(\frac{m}{m - 1}\right) \cdot e^{-m \cdot P_1 \cdot t} \tag{3-93}$$

The maximum overshoot occurs at $t = t_\Delta$ when the derivative of (3-93) is equal to zero:

$$\frac{dy(t)}{dt} = -\left(\frac{P_1}{m - 1}\right) \cdot e^{-P_1 \cdot t_\Delta} + \left(\frac{m^2 \cdot P_1}{m - 1}\right) \cdot e^{-m \cdot P_1 \cdot t_\Delta} = 0 \tag{3-94}$$

The solution of (3-94) is reported in (3-95). Then, the condition for imposing a given maximum overshoot Δv_{dc} is reported in (3-96): the value of the bus voltage described by (3-93) at $t = t_\Delta$ must be equal to $1 + \Delta v_{dc}$. Substituting (3-93) into (3-96) leads to (3-97), which is a non-linear equation that enables calculating the value of m required to impose the desired maximum overshoot Δv_{dc}. This equation must be solved using numerical methods, e.g., by using *fsolve* from Matlab®.

$$t_\Delta = \frac{2 \cdot \ln(m)}{P_1 \cdot (m-1)} \tag{3-95}$$

$$y(t_\Delta) = 1 + \Delta v_{dc} \tag{3-96}$$

$$\Delta v_{dc} = m^{\left(-\frac{m+1}{m-1}\right)} \tag{3-97}$$

Note that (3-97) does not depend on the specific value of P_1; rather, it depends on the relation m between P_2 and P_1. To illustrate this condition, several values of P_1 (and the associated values of P_2) were used to simulate the step response (3-93) for a specific value of m. The adopted value of $m = 0.0765$ was obtained by solving equation (3-97) for a maximum overshoot $\Delta v_{dc} = 5\,\%$. Then, four values for $P_1 = \{2000, 3000, 4000, 5000\}\ rad/s$ were tested, calculating the values of $P_2 = \{153.0, 229.5, 306.0, 382.5\}\ rad/s$ using equation (3-92). The simulation results are presented in Figure **3-20**, where it is verified that the time response of $G_{dc}(s)$ exhibits a maximum overshoot $\Delta v_{dc} = 5\,\%$ for all the P_1 conditions tested, which confirms the correctness of (3-97). Moreover, Figure **3-20** also shows that it is possible to design the settling time of $G_{dc}(s)$ using the value of P_1; the procedure is presented in the next subsection.

Expression (3-97) has two limits. The first limit $\Delta v_{dc} = 0\,\%$ occurs for $m \to 0$ and $m \to \infty$, which according to (3-92) corresponds to $G_{dc}(s)$ with a pole in infinity, i.e., a first-order transfer function. The second limit $\Delta v_{dc} = 13.5335\,\%$ occurs for $m \to 1$, which according to (3-92) corresponds to $G_{dc}(s)$ with two real and equal poles. Therefore, the system response can be designed to have a maximum overshoot within $0\,\% < \Delta v_{dc} < 13.5335\,\%$. Moreover, equation (3-97) always has two equivalent solutions, as reported in Figure **3-21**, where $\Delta v_{dc} = 5\,\%$ is obtained for $m = 0.0765$ and $m = 13.0719$. For example, considering $P_1 = 5000\ rad/s$ and $m = 0.0765$ results in $P_2 = 382.5\ rad/s$, while considering $P_1 = 382.5\ rad/s$ and $m = 13.0719$ results in $P_2 = 5000\ rad/s$. Therefore, solving (3-97) has two possible (and equivalent) domains for m: $0 < m < 1$ and $1 < m < \infty$.

Figure **3-21** also indicates that $\Delta v_{dc} < 5\,\%$ requires poles with a very large difference in magnitude, e.g., $\Delta v_{dc} = 3\,\%$ requires $P_2/P_1 = 25.6$, which could be difficult to implement.

3.2.2.3. Design of the settling time

The another performance criterion commonly used to specify the behavior of a DC bus corresponds to the settling t_s of the voltage after perturbations. The value of t_s is selected

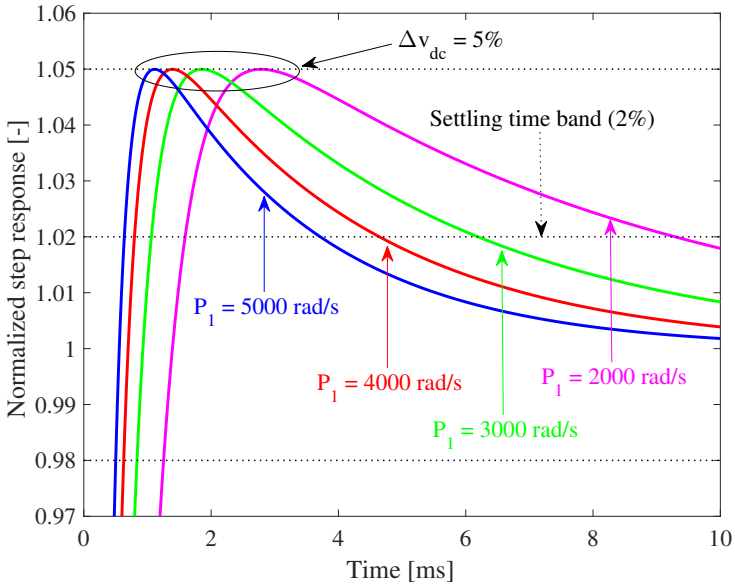


Figure 3-20.: Simulation of $G_{dc}(s)$ for $m = 0.0765$ to ensure that $\Delta v_{dc} = 5\,\%$.

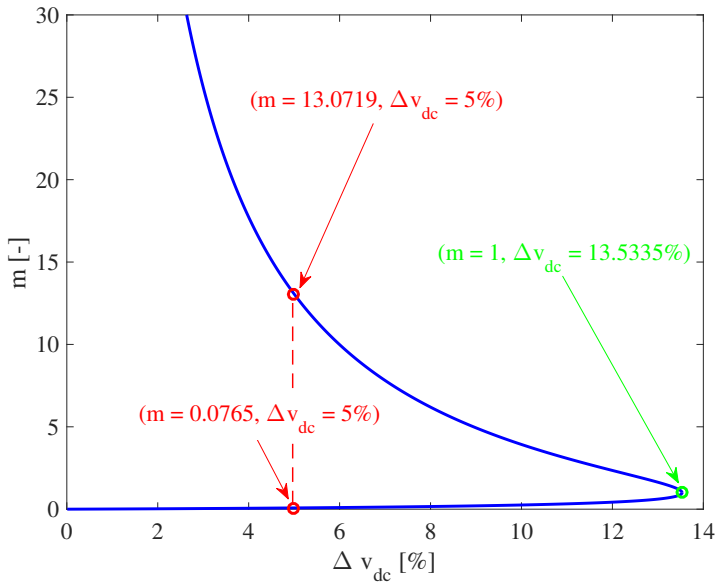


Figure 3-21.: Values of m to provide a desired Δv_{dc}.

from the time that the load is able to operate in a condition different from the nominal voltage.

In this Subsection, G_{dc} is designed to provide a desired settling t_s measured at a given settling time band ϵ, where the most classical band is $\epsilon = 2\,\% = 0.02$ [204]. Figure **3-20** shows that the settling time t_s occurs when the time response of the system (3-93) is $y(t_s) = 1 + \epsilon$. However, there are two crosses with $1 + \epsilon$: one before the maximum overshoot and another

one after the maximum overshoot. Therefore, the settling time fulfills $t_s > t_\Delta$, where t_Δ corresponds to the time (3-95) in which the maximum overshoot occurs.
On the basis of the previous analysis, the system response (3-93) is rewritten as shown in (3-98) to calculate the value of P_1 that provides the desired settling time t_s for the band ϵ, which includes the value of m calculated in the previous section to impose the maximum overshoot. This equation must be solved using numerical methods, e.g., by using *fsolve* from Matlab®.

$$\epsilon = \left(\frac{1}{m-1}\right) \cdot e^{-P_1 \cdot t_s} - \left(\frac{m}{m-1}\right) \cdot e^{-m \cdot P_1 \cdot t_s} \ , \ t_s > t_\Delta \tag{3-98}$$

To test the correctness of (3-98), four instances of $G_{dc}(s)$ were designed to guarantee a settling time of $t_s = 3\ ms$ for a band $\epsilon = 2\,\%$ considering different maximum overshoots. Figure **3-22** shows the simulation of these designs, which confirms that parameterizing the dynamic response using (3-98) ensures that the desired settling time is fulfilled for any feasible value of m. Table **3-1** presents the maximum overshoots, the values of m and the poles calculated using (3-92), (3-97) and (3-98) depicted in Figure **3-22**.

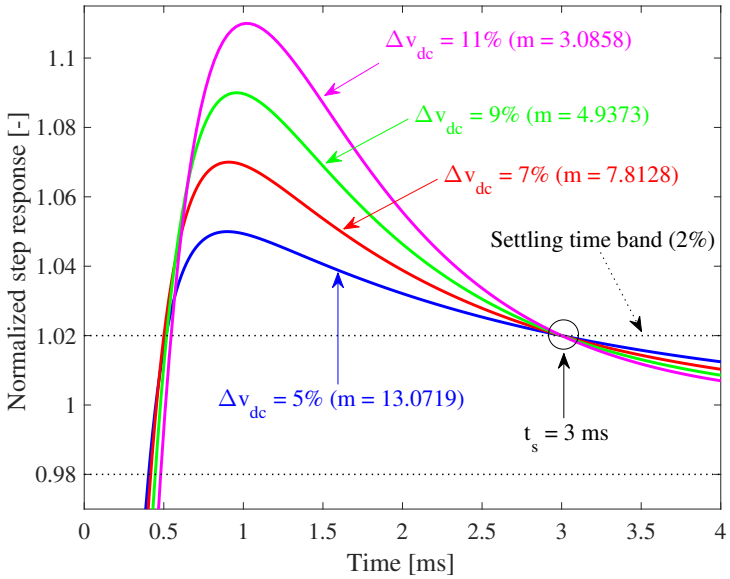


Figure 3-22.: Simulation of $G_{dc}(s)$ with values of P_1 to ensure that $t_s = 3\ ms$ for a settling time band $\epsilon = 2\,\%$.

3.2.2.4. Calculation of parameters k_p and k_i

The sliding function (3-59) and sliding surface are parameterized in terms of k_p and k_i. Therefore, the design of the sliding-mode dynamics in terms of the poles P_1 and P_2 must be translated to k_p and k_i values.

Table 3-1.: Poles for the simulation of $G_{dc}(s)$ presented in Figure **3-22**.

Δv_{dc}	m	P_1	P_2
5 %	13.0719	473.7 rad/s	6192.2 rad/s
7 %	7.8128	664.4 rad/s	5190.8 rad/s
9 %	4.9373	847.1 rad/s	4182.4 rad/s
11 %	3.0858	1057.6 rad/s	3263.5 rad/s

Contrasting the coefficients of $G_{dc}(s)$ in both (3-85) and (3-89) leads to the following expressions for k_p and k_i:

$$k_p = -C \cdot (P_1 + P_2) \tag{3-99}$$

$$k_i = -C \cdot (P_1 \cdot P_2) \tag{3-100}$$

Those values of k_p and k_i must fulfill the constraints reported in (3-68), (3-72)-(3-73) and (3-76)-(3-77) to ensure the global stability of the sliding-mode controller.

3.2.2.5. Summary

The design of the sliding-mode dynamics must be performed using the following steps:

1. Based on the load voltage requirements, define the maximum overshoot Δv_{dc} and settling time t_s (also specify the settling time band ϵ).

2. The parameter k_b must be adapted continuously based on (3-82).

3. Calculate the parameter m by solving (3-97) to limit the maximum overshoot to Δv_{dc}, which occurs at $t = t_\Delta$ presented in (3-95).

4. Calculate the pole P_1 by solving (3-98) to provide the desired settling time t_s for the band ϵ.

5. Calculate the pole P_2 from m and P_1 values by using (3-92).

6. Calculate k_p and k_i using (3-99) and (3-100), respectively.

7. Evaluate the constraints reported in (3-68), (3-72)-(3-73) and (3-76)-(3-77). If some of these constraints are not fulfilled, then change the design requirements (Δv_{dc}, t_s, ϵ) and/or the converter capacitor C and repeat from Step 3.

3.2.3. Implementation and operation analysis

The implementation of the sliding-mode controller involves two main parts: the switching circuit implementing the control law and the circuit to synthesize the sliding function (3-59). The following subsections discuss these circuits.
Moreover, this section also analyzes the response of the closed-loop charger/discharger to step perturbations in the DC bus current, which enables identifying the dynamic restrictions imposed by the passive elements of the DC/DC converter in the compensation of fast current transients.

3.2.3.1. Control law and switching circuit

The implementation of the sliding-mode controller requires a hysteresis band to limit the switching frequency [79, 205]. The insertion of a hysteresis band $[-H, +H]$ changes the control law imposed by the reachability conditions (3-69) and (3-70) as follows:

$$\begin{cases} \text{if } \Psi \leq -H & \Rightarrow & \text{SET } u = 1 \text{ (MOSFET ON)} \\ \text{if } \Psi \geq +H & \Rightarrow & \text{SET } u = 0 \text{ (MOSFET OFF)} \end{cases} \tag{3-101}$$

The implementation of the control law in (3-101) is performed using two comparators and a flip-flop S-R, as presented in Figure **3-23**, in which the signal u defines the MOSFET state.

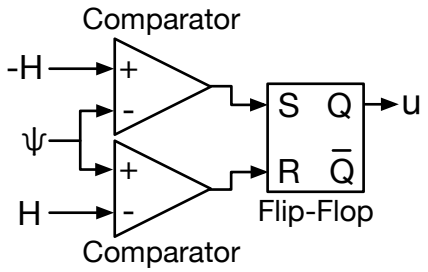


Figure 3-23.: Switching circuit implementing the control law in (3-101).

The value H of the hysteresis band can be set in the previous circuit using operational amplifiers, Zener diodes or independent voltage sources. Moreover, the circuit in Figure **3-23** can be implemented using integrated circuits such as the TS555 from STMicroelectronics [206].
The calculation of H depends on the desired steady-state switching frequency F_{sw} and on the passive elements of the converter. Under steady-state conditions, the average value of the bus voltage is equal to the reference, i.e., $\langle v_{dc} \rangle = v_R$, and the average value of the battery current $\langle i_b \rangle$ is equal to $\frac{i_{dc}}{d'}$, as reported in (3-14), where $d' = 1 - d$. Moreover, the steady-state battery current waveform $i_{b,SS}$ has two components: an average value $\langle i_b \rangle$ and a triangular current ripple $\delta i_b(t)$, as reported in (3-102). Similarly, the steady-state bus voltage waveform

$v_{dc,SS}$ has two components: an average value $\langle v_{dc} \rangle$ and a triangular current ripple $\delta v_{dc}(t)$, as reported in (3-103). Finally, the parameter k_b was previously designed as $k_b = 1 - d = d'$ in (3-82).

$$i_{b,SS} = \langle i_b \rangle + \delta i_b(t) \tag{3-102}$$

$$v_{dc,SS} = \langle v_{dc} \rangle + \delta v_{dc}(t) \tag{3-103}$$

Therefore, under steady-state conditions, the sliding surface (3-60) becomes the function $\Psi_{SS} = 0$ reported in (3-104). Replacing the steady-state values $\langle v_{dc} \rangle$ and $\langle i_b \rangle$ in (3-104), and considering that the integral of the voltage ripple is equal to zero due to the charge balance principle [134], the ripples of the battery current and bus voltage are related by (3-105).

$$\begin{aligned} \Psi_{SS} = [d' \cdot (\langle i_b \rangle + \delta i_b(t)) - i_{dc}] + k_p \cdot [v_R - (\langle v_{dc} \rangle + \delta v_{dc}(t))] \\ + k_i \cdot \int [v_R - (\langle v_{dc} \rangle + \delta v_{dc}(t))] \; dt = 0 \end{aligned} \tag{3-104}$$

$$d' \cdot \delta i_b(t) - k_p \cdot \delta v_{dc}(t) = 0 \tag{3-105}$$

The hysteresis band $[-H, +H]$ of the control law (3-101) implements (3-105), as given in (3-106); hence, the maximum value of (3-106) is equal to H.

$$-H \leq d' \cdot \delta i_b(t) - k_p \cdot \delta v_{dc}(t) \leq +H \tag{3-106}$$

The maximum value $\delta i_{b,pk}$ of the battery current ripple δi_b is obtained from (3-1), as given in (3-107), and the minimum value is symmetrical. Similarly, the maximum value $\delta v_{dc,pk}$ of the bus voltage ripple δv_{dc} is obtained from (3-2), as given in (3-108), and the minimum value is also symmetrical.

$$\delta i_{b,pk} = \frac{v_b \cdot d}{2 \cdot L \cdot F_{sw}} \tag{3-107}$$

$$\delta v_{dc,pk} = \frac{i_{dc} \cdot d}{2 \cdot C \cdot F_{sw}} \tag{3-108}$$

Moreover, from (3-1) and (3-2), note that the battery current and bus voltage waveforms have opposite derivatives. This means that the maximum value of the battery current ripple $max\,(\delta i_b(t)) = \delta i_{b,pk}$ occurs when the bus voltage ripple is minimum, i.e., $min\,(\delta v_{dc}(t)) = -\delta v_{dc,pk}$. In addition, since k_p is a negative quantity (3-68), it is represented as $k_p = -\,|k_p|$, where $|k_p|$ is the parameter magnitude. Based on the previous analyses, expression (3-106) is rewritten as follows:

$$d' \cdot \delta i_{b,pk} - |k_p| \cdot \delta v_{dc,pk} = H \tag{3-109}$$

Finally, the value of H in (3-110) is obtained by replacing the values of $\delta i_{b,pk}$ and $\delta v_{dc,pk}$, given in (3-107) and (3-108), into expression (3-109).

$$H = \left(\frac{d}{2 \cdot F_{sw}}\right) \cdot \left(\frac{v_b \cdot d'}{L} - \frac{|k_p| \cdot i_{dc}}{C}\right) \tag{3-110}$$

Expression (3-110) enables designing the value of H to impose the desired switching frequency F_{sw} to the switching circuit and MOSFETs. It is important to design H for the worst case, i.e., the higher frequency condition. For a fixed value of H, the value of F_{sw} in (3-110) increases when the bus current decreases; hence, the maximum switching frequency occurs when the battery is being charged with the maximum current (most negative current). This means that H must be designed in that condition to ensure a lower switching frequency in other operating conditions.

3.2.3.2. Synthesis of the sliding function

The calculation of the sliding function Ψ (3-59) requires the measurement of the DC bus voltage, DC bus current, battery voltage and battery current. Using the battery and DC bus voltages, the controller calculates the complementary duty cycle to parameterize $k_b = d'$ (3-82). Similarly, the DC bus voltage and the reference value are used to calculate the voltage error $E_{v_{dc}} = v_R - v_{dc}$, which is simultaneously multiplied by k_p and integrated and multiplied by k_i, and these two terms are added to $d' \cdot i_b - i_{dc}$. Figure **3-24** presents the block diagram of both the charger/discharger and the sliding-mode controller implementing Ψ. This figure also shows the hysteresis comparator with band $[-H, +H]$.
Finally, the controller block diagram presented in Figure **3-24** can be implemented with analog circuitry using operational amplifiers and an analog multiplier, using a digital microprocessor with analog-to-digital converters (ADCs), or with a mixed analog/digital circuit, as it will be described in Section 3.2.5.

3.2.3.3. Speed limitation under perturbations

The proposed controller was designed to detect the current changes in the DC bus to improve the rejection of perturbations. However, note that changes in the battery current are limited by the maximum slope achievable by the inductor current, which depends on the inductor L and battery voltage. This limitation constrains the speed of the controller.
To illustrate this speed limitation, Figure **3-25** shows the simulation of the proposed controller with a step perturbation in the DC bus current. It is observed that the theoretical battery current $i_{b,th} = i_{dc} \cdot v_{dc}/v_b$ needed to compensate the perturbation has a step waveform

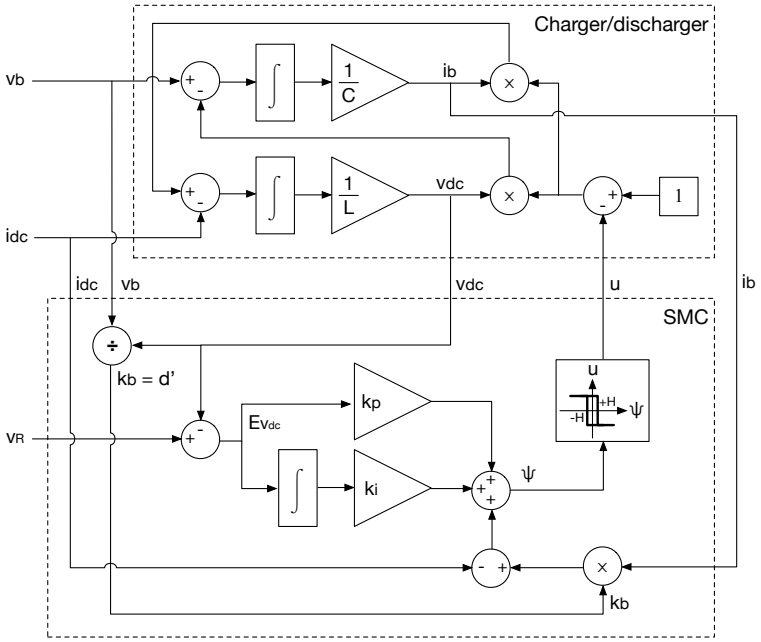


Figure 3-24.: Block diagram of the charger/discharger and the sliding-mode controller (SMC).

with an infinite slope. However, from (3-1), it is observed that the maximum slope achievable by the battery (inductor) current is v_b/L; hence, the battery current takes some time to reach the required theoretical value $i_{b,th}$. Moreover, the controller must set the signal $u = 1$ to increase the battery current, which disconnects the inductor from the DC bus. Therefore, during the time in which the battery current is increased, the bus current must be extracted from the bus capacitor, producing an unavoidable voltage drop.
The time τ required by the battery current to reach the theoretical value $i_{b,th}$ is calculated from (3-1), considering $u = 1$, as given in (3-111). This expression considers a bus current perturbation with magnitude Δi_{dc}.

$$\tau = \frac{\Delta i_{dc} \cdot L}{v_b \cdot d'} \tag{3-111}$$

Note that (3-111) depends on the duty cycle; therefore, it is difficult to provide a precise value of the voltage drop since v_{dc} and d depend on each other simultaneously. However, the voltage drop v_{drop} can be approximated by integrating the bus current perturbation during the time τ in which $u = 1$:

$$v_{drop} \approx \frac{{\Delta i_{dc}}^2 \cdot L}{v_b \cdot d' \cdot C} \tag{3-112}$$

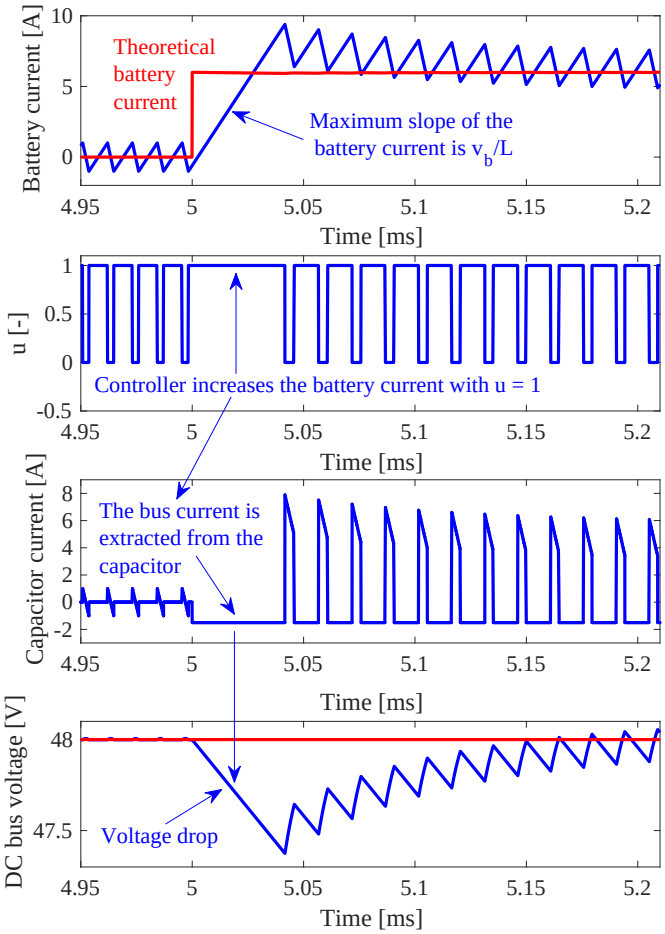


Figure 3-25.: Simulation of the proposed controller with a step perturbation in the DC bus current.

Expression (3-112) is useful for designing L and C such that a maximum voltage drop is ensured for the maximum current perturbation expected Δi_{dc}.
Note that the speed limitation described in this subsection is inherent to the DC/DC converter construction; hence, it does not depend on the controller performance. In fact, expressions (3-111) and (3-112) depend on the size of the passive elements L and C and not on the controller parameters. Moreover, the proposed sliding-mode controller forces the change in the battery current with the highest derivative possible, i.e., providing the fastest response possible. Therefore, the voltage drop in (3-112) is the smallest one achievable with any controller.

3.2.4. Design example and simulation results

This Subsection presents a design example of the proposed controller for the charger/discharger circuit illustrated in Figure **3-18**. The DC/DC converter has the following passive elements: $L = 50\ \mu H$ and $C = 100\ \mu F$. Moreover, the battery has a nominal voltage $v_b = 12\ V$, and

the DC bus voltage v_{dc} must be regulated to $v_R = 48\ V$. The controller design is performed by following the steps summarized in subsection 3.2.2.5.

This example considers a desired settling time $t_s = 3\ ms$ for a band $\epsilon = 1\,\%$ and a maximum overshoot $\Delta v_{dc} = 5\,\%$. Moreover, the parameter k_b is adapted continuously based on (3-82), as reported in Figure **3-24**, dividing v_b by v_{dc}. Then, $m = 13.0719$ is calculated from (3-97), and the pole $P_1 = 704.7945\ rad/s$ is calculated from (3-98). The pole $P_2 = 9213\ rad/s$ is calculated by using (3-92), and $k_p = -0.9918\ A/V$ and $k_i = -649.3272\ A/(V \cdot s)$ are calculated using (3-99) and (3-100), respectively.

Considering a maximum supported battery current of $i_{b,max} = 20\ A$ and evaluating constraint (3-68) results in $-1.2 < k_p = -0.9918 < 0$, which fulfills the transversality condition. Moreover, evaluating (3-73) reveals that $|k_i| = 649.3272$ fulfills the reachability conditions for $v_{dc} - v_R < 16.0336\ V$; hence, $v_{dc} < 64.0336\ V$. Similarly, evaluating (3-77) indicates that such a k_i value fulfills the reachability conditions for $v_{dc} - v_R > -47.9721\ V$; hence, $v_{dc} > 0.0279\ V$. Therefore, the calculated values for k_p and k_i ensure global stability for the bus voltage $v_{dc} = 48\ V$.

The hysteresis band parameter $H = 1/4\ A$ was designed using (3-110) to provide a steady-state switching frequency $F_{sw} = 90\ kHz$ in stand-by mode ($i_{dc} = 0\ A$). This value of H imposes steady-state switching frequencies equal to $104.88\ kHz$ and $75.12\ kHz$ for DC bus currents of $-1\ A$ (charge stage with $i_b = -4\ A$) and $1\ A$ (discharge stage with $i_b = 4\ A$), respectively.

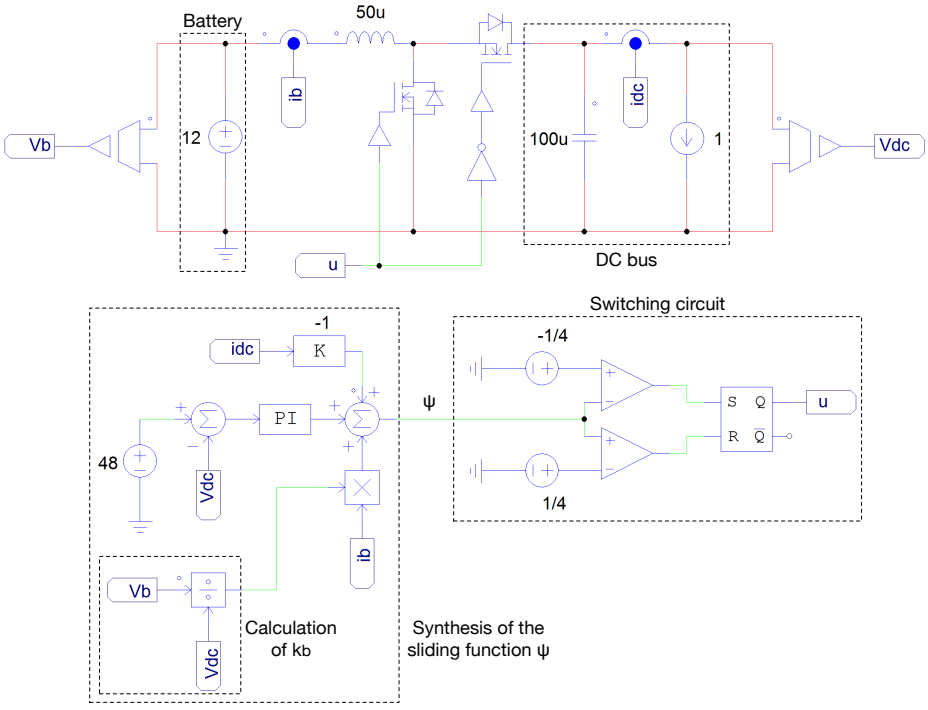


Figure 3-26.: Circuit implemented in PSIM® electrical simulator.

Figure **3-26** presents the circuit scheme implemented in the electrical simulator PSIM®, in which the switching circuit and the synthesis of the sliding function are observed. This scheme uses a PI block and an adder from PSIM® to implement the terms $k_p \cdot (v_R - v_{dc}) + k_i \cdot \int (v_R - v_{dc})\ dt$ of Ψ; the transfer function of the PI block from PSIM® is presented in (3-113), where the PI block parameters $k_{psim} = -0.9918$ and $T_{psim} = 0.0015\ s$ were calculated using the expressions presented in (3-114).

$$G_{PI} = k_{psim} \cdot \frac{1 + s \cdot T_{psim}}{s \cdot T_{psim}} \tag{3-113}$$

$$k_{psim} = k_p \quad \wedge \quad T_{psim} = \frac{k_p}{k_i} \tag{3-114}$$

Figure **3-27** shows the simulation of the proposed sliding-mode controller with a step change of 1 V in the reference value. This simulation shows that the controller forces a fast change in the battery current to accelerate the bus voltage response. However, as described in subsection 3.2.3.3, this action requires $u = 1$ during the time in which the battery current is increased, forcing the bus capacitor to provide the bus current, which produces a small voltage drop $v_{drop} = 0.25\ V$. Therefore, the effective reference change faced by the controller is $1.25\ V$; this means that the maximum overshoot must be $\Delta v_{dc} = 0.05 \cdot 1.25\ V = 62.5\ mV$, and the band $\epsilon = 1\,\%$ corresponds to $0.01 \cdot 1.25\ V = 12.5\ mV$. The magnified plots at the bottom of Figure **3-27** confirm the correct behavior of the controller, where the maximum overshoot and settling time are measured with the average signal of v_{dc} to remove the switching ripple. The simulation also shows that the fast change in the reference value forces the sliding function to leave the surface during a very short time, but the fulfillment of the reachability conditions drives the system to return to the surface. This behavior demonstrates the global stability provided by the proposed solution. In conclusion, the controller performance presented in Figure **3-27** verifies the correctness and accuracy of the analyses and design process proposed in the previous Subsections.

Figure **3-28** presents the simulation of the proposed SMC with perturbations in the DC bus current for all the operating conditions: stand-by stage ($i_{dc} = 0\ A$), charge stage ($i_{dc} < 0\ A$) and discharge stage ($i_{dc} > 0\ A$). The simulation considers step perturbations in the bus current with a magnitude equal to 2 A, which is 100 % higher than the magnitude of the perturbations used to test the controller reported in Section 3.1 [88]. The simulation results demonstrate the satisfactory performance of the controller in compensating the bus current perturbations. Similarly, the simulation shows a fast and accurate tracking of the sliding surface in all the operating conditions. Note that the perturbations produce different deviations in the bus voltage: in the discharge stage, the battery current i_b increases with the slope v_b/L ($u = 1$) and decreases with the slope $(v_b - v_{dc})/L$ ($u = 0$), which has a higher magnitude. Therefore, the transition from stand by to discharge is slower than the transition from discharge to stand by; hence, a larger voltage deviation occurs in the former transition. This comparison is presented in the magnified region at the bottom of Figure **3-28**.

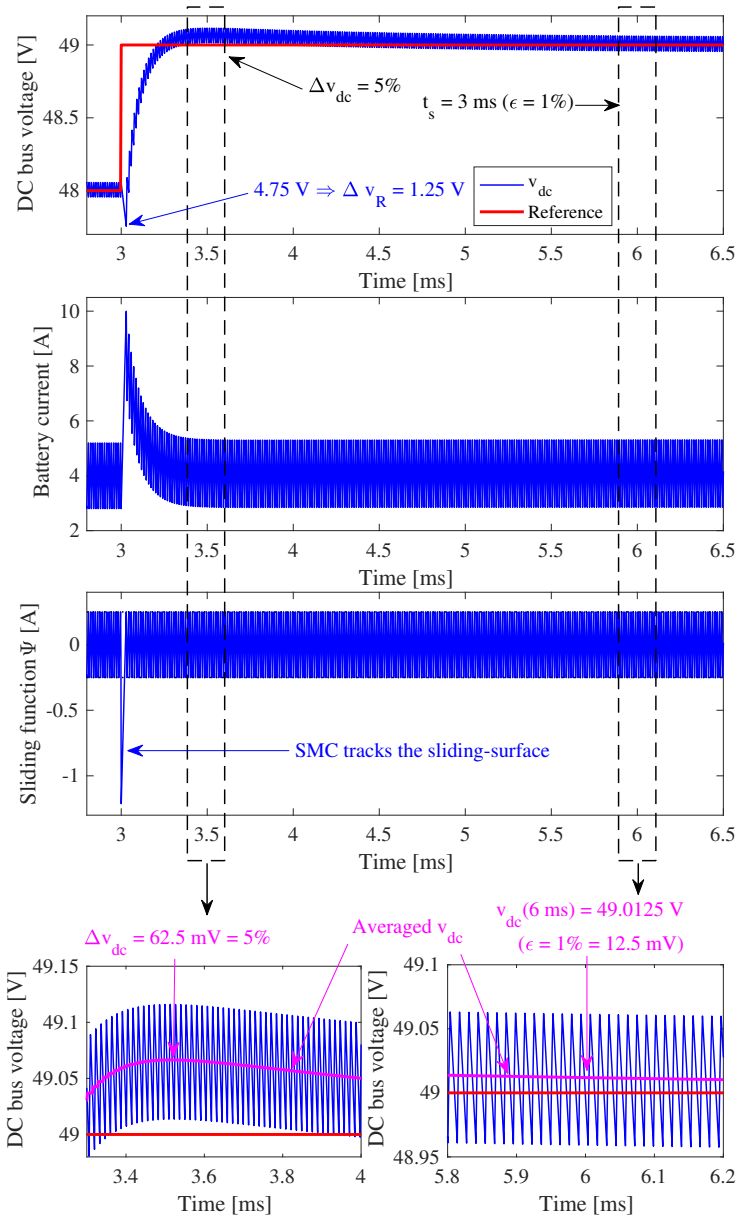


Figure 3-27.: Simulation of the proposed SMC with changes in the reference.

In contrast, the transition from stand by to charge occurs with the slope $(v_b - v_{dc})/L$ $(u = 0)$; hence, it produces a lower voltage deviation compared with the transition from stand by to discharge. Finally, the transition from charge to stand by occurs with the slope v_b/L $(u = 1)$, but due to the small voltage ripple in the stand-by condition, the voltage deviation is negligible.

Figure **3-29** presents an additional simulation that contrasts the performances of the proposed controller and the SMC without measuring i_{dc} reported in Section 3.1 [88]. The results demonstrate the improved disturbance rejection provided by the solution proposed in this

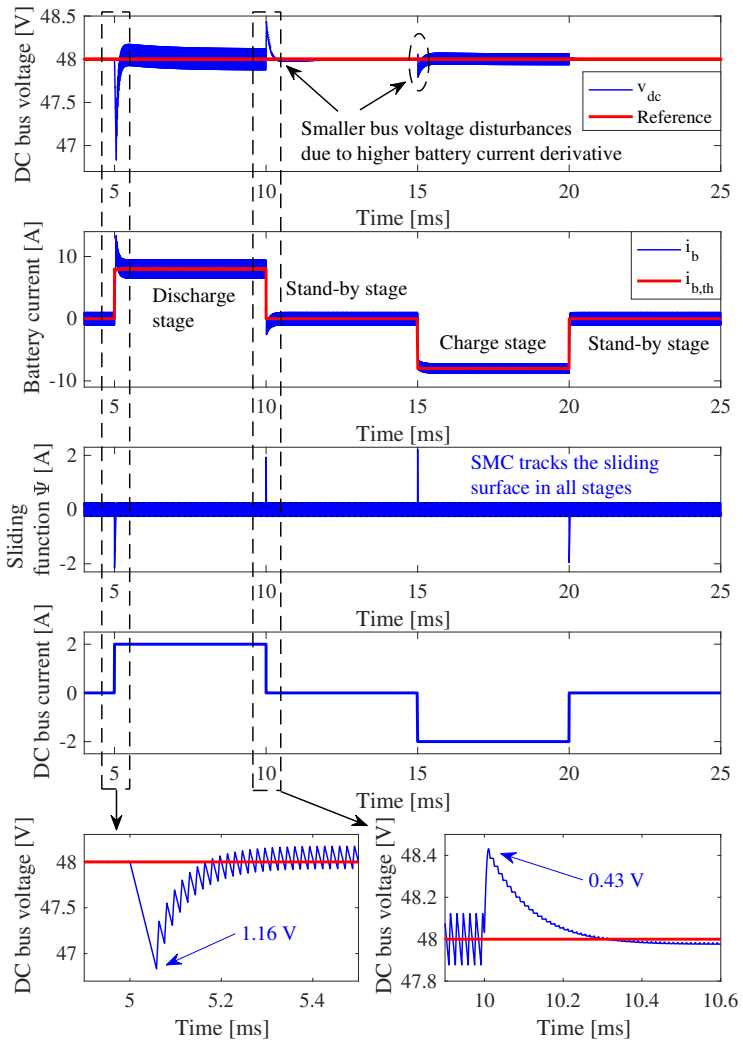


Figure 3-28.: Simulation of the proposed SMC with perturbations in the bus current.

Section:

- Bus current step from 0 A to 1 A (5 ms): the bus voltage deviation produced under the control of the new solution is only 16 % of the deviation produced under the control of the solution in Section 3.1 [88].

- Bus current step from 1 A to 0 A (10 ms): the bus voltage deviation produced under the control of the new solution is only 6 % of the deviation produced under the control of the solution in Section 3.1 [88].

- Bus current step from 0 A to -1 A (15 ms): the bus voltage deviation produced under the control of the new solution is only 5 % of the deviation produced under the control of the solution in Section 3.1 [88].

- Bus current step from $-1\ A$ to $2\ A$ ($20\ ms$): the bus voltage deviation produced under the control of the new solution is only 33 % of the deviation produced under the control of the solution in Section 3.1 [88].

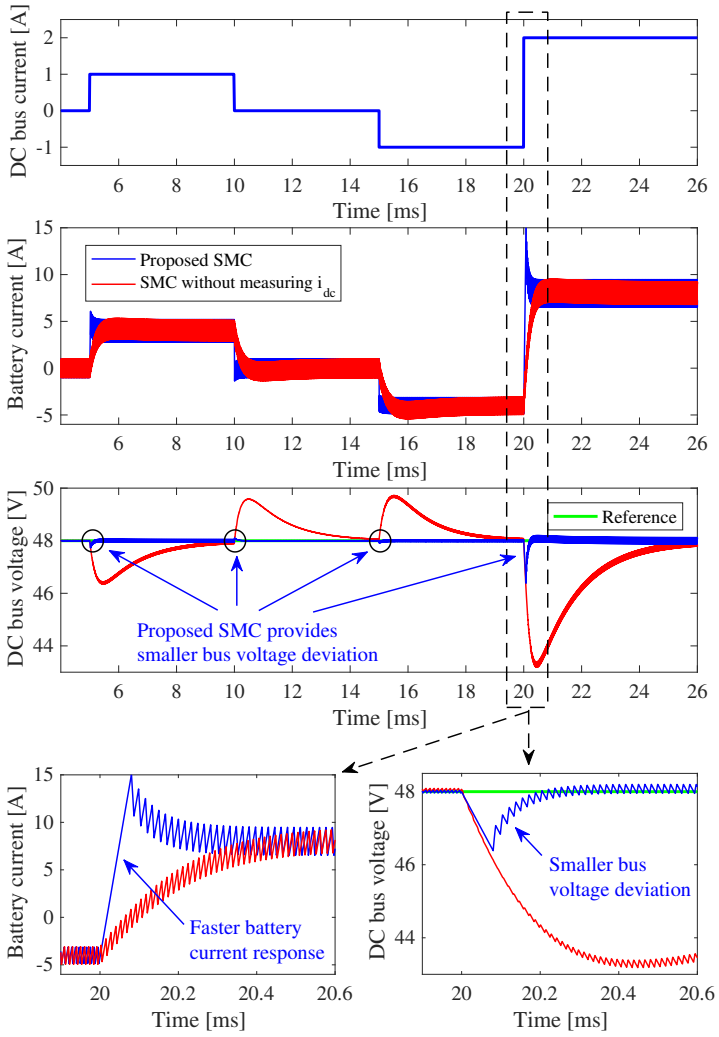


Figure 3-29.: Simulation of both the proposed SMC and the SMC without measuring i_{dc} presented in Section 3.1.

This improved disturbance rejection is due to the faster battery current response provided by the SMC proposed in this Section. Such a condition is observed in the magnified region at the bottom of Figure **3-29**, where the battery current imposed by the new SMC increases faster to compensate the bus current in a shorter time. This behavior results in a lower current extraction from the bus capacitor to provide a lower voltage deviation of the bus voltage.

It must be noted that step-like current perturbations, similar to ones considered in the previous analyses and simulations, could be triggered by sudden connections and disconnections

of loads and generators to/from the DC bus. However, some real loads require a charge produce, e.g. electrical machines, which produces a relaxed waveform with a limited frequency content. Therefore, since the control system developed in this Section considers the worst-case scenario (step-like perturbations), this solution will provide shorter settling times and overshoots in presence of relaxed waveforms. Figure **3-30** shows the performance of the proposed SMC for both step-like and relaxed current perturbations in the DC bus: assuming a current transient with frequencies limited to $14kHz$ (relaxed waveform), the maximum voltage overshoot is reduced 5 times and the settling time is reduced to the half, both in comparison with a step-like current transient (step waveform). Therefore, the solution proposed in this Section guarantees voltage overshoots and settling times smaller or equal to the limits defined in the design process.

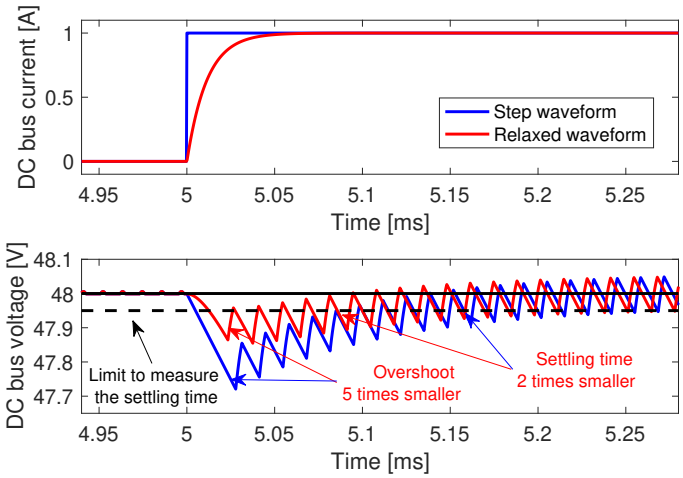


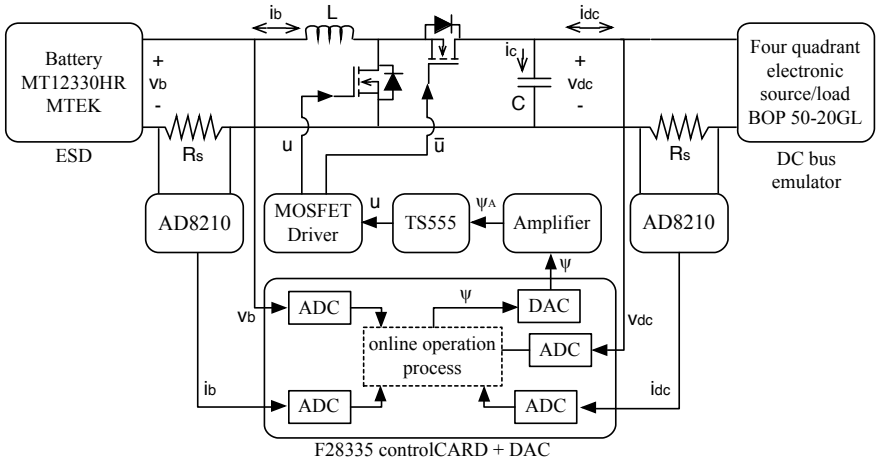
Figure 3-30.: Behavior of the proposed SMC for both step and relaxed current perturbations.

3.2.5. Experimental validation

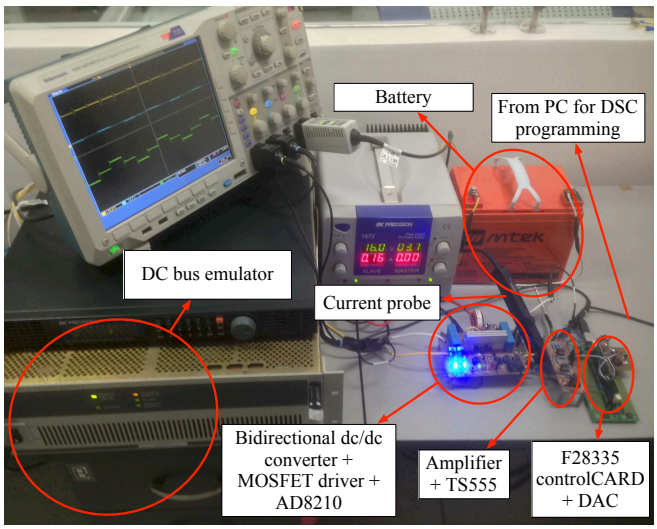
To provide an experimental proof-of-concept, the battery charger/discharger and the proposed SMC were implemented as reported in Figure **3-31**. In particular, Figure **3-31**a shows the schematic diagram of the experimental platform. The prototype consists of a MT12330HR sealed lead-acid battery from MTEK [207], a BOP 50-20GL four-quadrant source/load from Kepco [208] to emulate the DC bus, the bidirectional power converter reported in Figure **3-18**, and digital and analog circuits implementing the sliding-mode controller.

The implementation of the sliding surface includes two current-sensing circuits based on the AD8210 [209]: one of them measuring the DC bus current and the other measuring the battery current. Moreover, the DC bus voltage and battery voltage are scaled with voltage dividers. With this information, the adaptive surface of the SMC is calculated in a

TMS320F28335 Delfino Microcontroller from Texas Instruments® [210].
The hysteresis comparator was implemented with the timer TS555 [206] according to Figure **3-23**, whose reference voltage is imposed by the TMS320F28335 through a MCP4822 digital-to-analog converter (DAC) [211], and according to Section 3.2.4, the hysteresis band was established as $0.25\,A$. However, this value was eventually scaled to a reference voltage within $2.50\,V \pm 0.83\,V$ since the TS555 has a fixed $H = 0.83\,V$. The TS555 output, i.e., the control signal u, is delivered to the HIP4081A MOSFET driver [212], which sets the states of both MOSFETs. The experimental setup is depicted in Figure **3-31**b.



(a) Schematic diagram of the experimental platform.



(b) Experimental devices.

Figure 3-31.: Experimental platform.

With the aim of providing a comparative analysis between the solution proposed in this Section and the SMC introduced in Section 3.1, both SMCs were experimentally tested under

the same conditions. Due to the physical limitations of the BOP 50-20GL four-quadrant source/load, the experiments consider relaxed current perturbations similar to the ones reported in Figure **3-30**. Moreover, some parameters of this experimental evaluation are different from the parameters used in the simulation examples presented in the previous section: the experimental DC/DC power converter has a $44\mu F$ capacitor and a $22\mu H$ inductor. Finally, the DC bus voltage is regulated at $36V$ to have a safe margin from the maximum voltage supported by the BOP 50-20GL ($50V$).

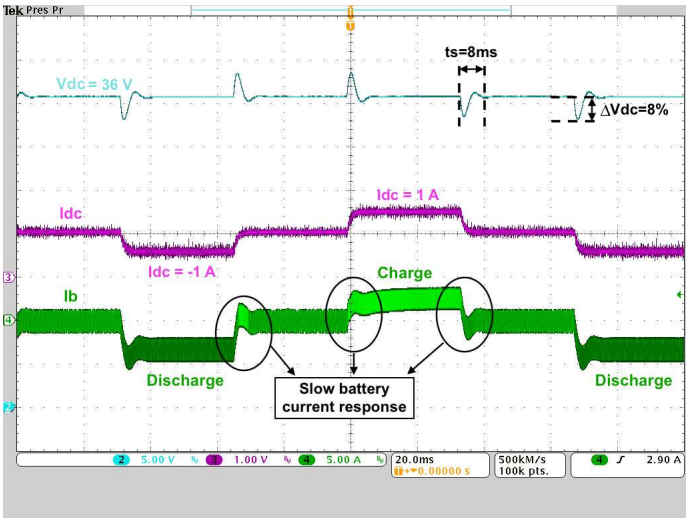
For the experimental tests, the dynamic response of the system was defined with a maximum overshoot of 5 %, which requires, according to Table **3-1**, establishing the poles P_1 and P_2 at 704.76 rad/s and 9213.42 rad/s, respectively, with $m = 13.0719$. Moreover, the settling time was set to 3 ms for $\epsilon = 1\,\%$. Then, using equations (3-99) and (3-100), the parameters $k_p = -0.4364\ A/V$ and $k_i = -285.7040\ A/(V \cdot s)$ were calculated. Those values ensure the global stability of the system by fulfilling the transversality and reachability conditions reported in Section 3.2.4.

Figure **3-32**a presents the waveforms obtained with the SMC reported in Section 3.1. The upper waveform shows the DC bus voltage, the middle one is the DC bus current, and the waveform at the bottom is the battery current. Similarly, Figure **3-32**b shows, in the waveforms at the top, the comparison of the DC bus voltages generated by both the new SMC and the SMC introduced in Section 3.1. Moreover, the waveform in the middle is the same DC bus current, and the waveform at the bottom is the battery current generated by the new SMC.

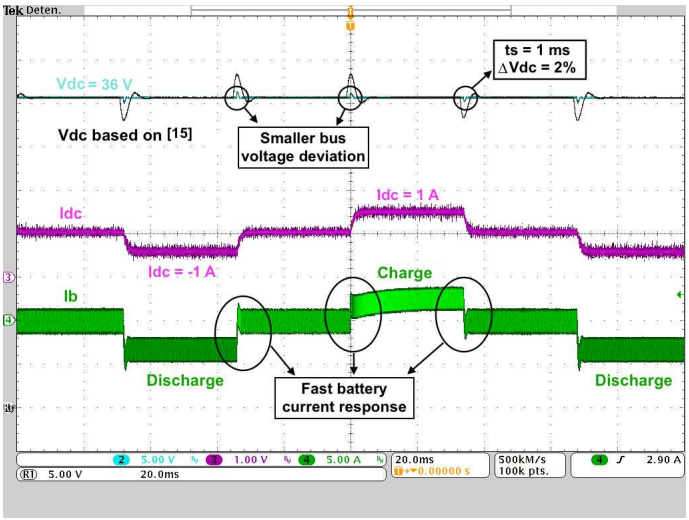
To reproduce the simulations reported in Figure **3-29**, the experimental perturbations in the DC bus current have a magnitude of $1A$ in the three operating conditions: charge, discharge and stand by. Figure **3-32**a shows the slow change in the battery current imposed by the SMC introduced in Section 3.1; in contrast, Figure **3-32**b shows the fast change in the battery current imposed by the SMC proposed in this Section. Such a behavior enables the new SMC to provide a tighter voltage regulation. Moreover, the experiments consider a relaxed current waveform, hence the voltage overshoot and settling time must be smaller than the maximum limits imposed for the design process: 5 % and $3ms$, respectively. In fact, the experimental voltage waveform reported in Figure **3-32**b exhibits an overshoot near to 2 % and a settling time near to $1ms$. Finally, both Figure **3-32**a and Figure **3-32**b validate the analysis and simulations presented in the previous Section and, simultaneously, demonstrate the correctness and implementation viability of the proposed solution.

3.3. Conclusions

This Chapter has presented control strategies, based on the sliding-mode theory, to regulate a bidirectional DC/DC converter interfacing an ESD and a DC bus in a renewable power system. The control strategies provide a regulated DC bus voltage, ensuring global stability in any operation condition, despite of the non-linear nature of the system and the bidirectional



(a) DC bus voltage regulation with the SMC reported in Section 3.1.



(b) DC bus voltage regulation with the proposed SMC.

Figure 3-32.: Experimental results for 1 A steps in the bus current.

power flows. The first controller is based on a sliding surface formed by the ESD current and both the DC voltage error and its integral, which enables to design the dynamic response of the DC bus voltage in agreement with the load requirements, where underdamped and critically damped responses are achievable.

The Chapter also provides detailed analyses of the sliding-mode conditions and proposes an easy-to-follow design process based on the load and DC bus operative restrictions, which are: maximum acceptable deviation of the DC bus voltage, the safe band for normal load operation, the maximum time acceptable to enter into the safe band after a perturbation, the maximum bus current perturbation and both the DC bus and ESD nominal voltages. However, the design equations and sliding-mode existing conditions depend on the converter

duty cycle, hence they must be recalculated in each operation condition. To face this problem, those equations where normalized in terms of the duty cycle, providing new adaptive equations valid for the complete operation range. Hence, that first solution is an adaptive sliding-mode controller.

The performance of such a solution was evaluated by means of simulations made in both Matlab® and PSIM®, and with experimental data obtained in a proof-of-concept prototype. Both simulation and experimental results demonstrate the correctness of the adaptive sliding-mode controller, its mathematical analyses and the design process, which are the fourth contribution of the Thesis.

This Chapter has also presented a second sliding-mode controller to regulate the bidirectional DC/DC converter interfacing a battery and a DC bus. The controller provides a satisfactory regulation of the DC bus voltage, improving the compensation of bus perturbations with respect to the SMC proposed in the first part of the Chapter. This tight bus regulation provides safe operating conditions to both the load and sources. The main feature of this solution is the inclusion of the bus current into the sliding surface, which enables the controller to improve the compensation of bus perturbations. Moreover, a new design process ensures global stability in any operating condition, but at the price of the on-line calculation of one of the surface parameters, i.e., k_b, which requires a fast microprocessor and ADC for the implementation. This second SMC, and the associated design process, are the fifth contribution of the Thesis.

The second SMC was tested under different operation conditions, achieving always the desired performance: the DC bus voltage exhibits limited voltage overshoots and settling times. In this way, the simulations reports a satisfactory match with the imposed criteria under the most extreme condition, i.e., step current perturbations. Moreover, the simulations also report smaller overshoots and settling times when the perturbations describe relaxed waveforms instead of ideal steps. Those results were confirmed by experimental measurements in a proof-of-concept platform, which ensures a safe operation of the DC bus under real conditions. Finally, both simulations and experiments were used to demonstrate the improved regulation with respect to the first solution.

An implementation challenge is to avoid the current sensors, which are costly devices with high failure rates. For this topic, the mathematical analyses presented in this Chapter can be used to design an observer for the battery current. Moreover, replacing the classical boost (buck) charger/discharger with an interleaved structure will reduce the current ripple injected into the battery, which in turn will improve the battery health.

However, the proposed analyses consider one major simplification: both the converter equations and adaptive laws do not take into account parasitic losses. Without such a simplification the system and SMC equations are very complex and difficult to analyze, however a future work could be dedicated to that particular topic to provide an improved design process.

4. Point-of-load converter with reduced current ripple and increased efficiency

The goal of this Chapter is to provide with high-efficiency a quality power to the load. Hence, this Chapter proposes an active post-filter to reduce the ripple of the voltage delivered to the load of the system presented in Figure **1-1**. The post-filter is based on two Buck converters, connected in parallel, operating in complementary interleaving. In such a configuration the ripple in the load current could be virtually eliminated to improve the power quality in comparison with classical Point-Of-Load (POL) regulators based on a single Buck converter. The post-filter is designed to isolate the load from the main Buck regulator, leading to the proposed three-converter structure named BuckPS. The correct operation of the post-filter is ensured by means of a sliding-mode controller. Finally, the proposed solution significantly reduces the current harmonics injected into the load, and at the same time, it improves the overall electrical efficiency. Such characteristics are demonstrated by means of analytical results and illustrated using circuital simulations. The results of this Chapter were published in [22], which corresponds to the sixth contribution of the Thesis.

4.1. POL regulator based on a post-filter

The proposed step-down POL regulator is based on the classical Buck topology, named BuckS, shown in Figure **4-1**. In such a topology the output voltage ripple occurs in the output capacitance, which is typically implemented using a large capacitor [213]. Using the classical approach given in [134], the output voltage ripple ΔV_o in the Buck converter is given in (4-1), which depends on the inductor peak current ripple ΔI_L. In (4-1), T represents the switching period, C the output capacitance, R_{Loss} the aggregated parasitic resistances of the inductor L and the MOSFETs [23], D is the converter duty cycle, while I_o and V_o represent the steady state load current and voltage, respectively. Since the POL converters must provide reduced voltage ripples to the load [214, 215, 216], ΔV_o can be reduced by increasing C and L or by reducing T (increasing the switching frequency F_{sw}) and the parasitic losses R_{Loss}. Instead, this thesis proposes to use a DC/DC converter to reduce the effective ΔI_L magnitude that reaches the capacitor C to achieve the required small ΔV_o condition.

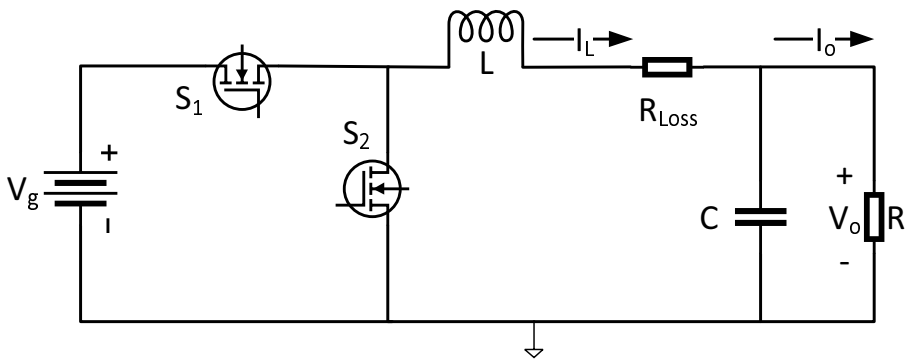


Figure 4-1.: Typical structure of a Buck converter (BuckS).

$$\Delta V_o = \frac{\Delta I_L \cdot T}{8 \cdot C} \quad \wedge \quad \Delta I_L = \frac{(V_o + R_{Loss} \cdot I_o) \cdot D' \cdot T}{2 \cdot L} \tag{4-1}$$

Moreover, from the small ripple approximation, volt-second and change balances [134], the steady-state induction current I_L, which is equal to the steady-state load current I_o, and the voltage conversion ratio are given in (4-2). In such equations R represents the load impedance at the desired operation condition and V_g represents the power source voltage.

$$I_L = \frac{V_o}{R} \quad \wedge \quad \frac{V_o}{V_g} = \frac{D}{1 + \frac{R_{Loss}}{R}} \tag{4-2}$$

Finally, the efficiency η of the BuckS POL regulator is given in (4-3). Such efficiency is reduced when the load current increases since the impedance R is reduced. Therefore, the solution proposed in this Thesis is also intended to improve the overall electrical efficiency.

$$\eta = \frac{1}{1 + \frac{R_{Loss}}{R}} \tag{4-3}$$

In the following subsections the proposed post-filter and POL regulator are introduced, contrasting the achieved performance with the classical BuckS solution.

4.1.1. Post-filter based on parallel buck converters

Figure **4-2** presents the proposed post-filter consisting of two Buck converters, operating in complementary interleaving, where the output capacitor is common for both Buck branches. The post-filter main MOSFETs (S_{1U} and S_{1L}) are complementarily activated to generate complementary inductor current waveforms on L_1 and L_2. Such a condition produces the

cancelation of the inductor current ripples to provide an almost ripple-free current to the output capacitor C, and based on (4-1), a small voltage ripple is imposed on the load. It must be pointed out that the secondary MOSFETs (S_{2U} and S_{2L}) are also complementarily activated with respect to the main MOSFET of each branch.

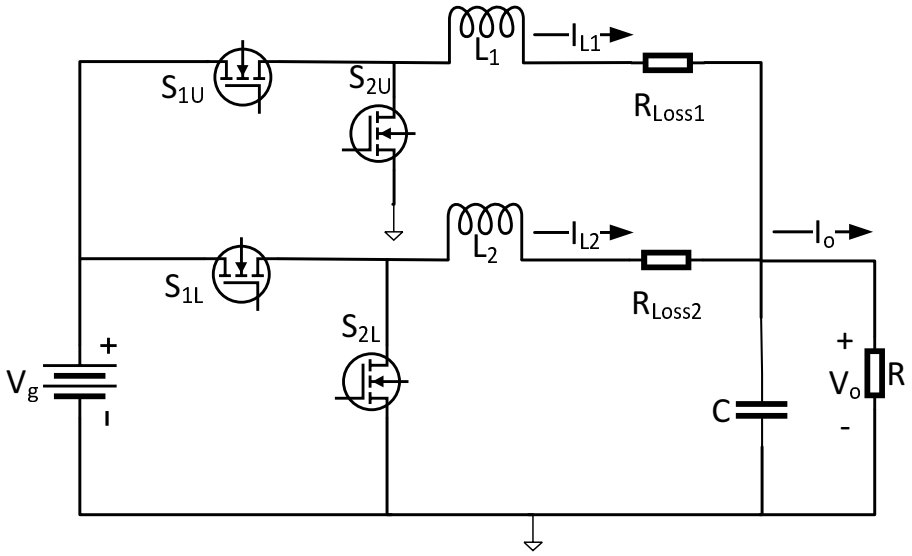


Figure 4-2.: Buck converter in interleaved topology.

To ensure the cancellation of the inductor current ripples, both Buck branches must operate in continuous conduction mode (CCM); otherwise, if a branch current is zero (in discontinuous conduction mode – DCM), the other branch ripple is propagated to the output capacitor. From (4-1), and considering the scheme of Figure **4-2**, where R_{Loss1} and R_{Loss2} represent the parasitic resistances in each branch, the CCM on both branches is achieved when the condition given in (4-4) is fulfilled. Such an expression takes into account the complementary activation of S_{1U} and S_{1L}; therefore the first branch has a duty cycle D while the second branch has a complementary duty cycle $D^{'} = 1 - D$.

$$\frac{V_o}{V_g} = \frac{D}{1 + \dfrac{R_{Loss1}}{R}} = \frac{D^{'}}{1 + \dfrac{R_{Loss2}}{R}} \tag{4-4}$$

Solving (4-4) for D leads to relation (4-5):

$$D = \frac{R + R_{Loss1}}{R_{Loss1} + 2 \cdot R + R_{Loss2}} \tag{4-5}$$

Therefore, the symmetrical interleaved Buck converter must be operated at the duty cycle D given in (4-5) to achieve the desired reduction of the output voltage ripple. Moreover, such a duty cycle imposes the voltage conversion ratio given in (4-6).

$$\frac{V_o}{V_g} = \frac{D \cdot R_{Loss2} + R_{Loss1} \cdot (1 - D)}{R_{Loss2} + (R_{Loss1} \cdot \frac{R_{Loss2}}{R})} \tag{4-6}$$

In a practical implementation the inductors L_1 and L_2 and the MOSFETs could be selected to have similar values and construction characteristics: $L_1 = L_2 = L_f$ and $R_{Loss1} = R_{Loss2} = R_{Lf}$. Such a condition is useful to simplify the post-filter design and control since both branches must process the same power. On the basis of such a practical consideration, the required duty cycle given in (4-5) becomes $D = 0.5$, while the voltage conversion ratio provided by the post-filter is given in (4-7).

$$\frac{V_o}{V_g} = \frac{1}{2 + \frac{R_{Lf}}{R}} \tag{4-7}$$

Moreover, the steady-state currents in each inductor are equal, as given in (4-8), while the steady-state load current is the sum of both currents, that is, the double of a branch current.

$$I_{L1} = I_{L2} = \frac{V_g}{2(2 \cdot R + R_{Lf})} \tag{4-8}$$

In addition, the current ripples of both braches have the same magnitude, while the current ripple injected into the load is near to zero since the post-filter branches operate in complementary mode, which generates opposite slopes for both inductors current as illustrated in Figure **4-3**, in which ΔI_{L1} and ΔI_{L2} represent the ripple magnitudes for each branch. Therefore, since the current ripple reaching the post-filter output capacitor (C in Figure **4-2**) is near to zero, the output voltage ripple is also near to zero.

To ensure a correct ripple cancellation in the post-filter it is required that both branches exhibit the same average current with opposite instantaneous slopes, and at the same time, it is required that both branches operate in CCM. Such conditions must be ensured despite the load current magnitude or the aging of the components. But, from (4-5) and (4-7), it is noted that in all cases the duty cycle and voltage conversion ratio are fixed. Therefore, classical control paradigms based on fixed-frequency drivers, such as the PWM, are not suitable to regulate the post-filter: classical controllers, such as PI, PID, or lead-lag, change the duty cycle (using a PWM [134, 77]) to compensate the system perturbations, but because the post-filter requires a fixed duty cycle, it is not possible to regulate it using such type of controllers. For this reason, it is necessary to adopt another control paradigm that provides an additional freedom degree. In such a way, this Thesis proposes to regulate the post-filter using the sliding-mode technique to dynamically change the switching frequency, which according to (4-1) is given by (4-9).

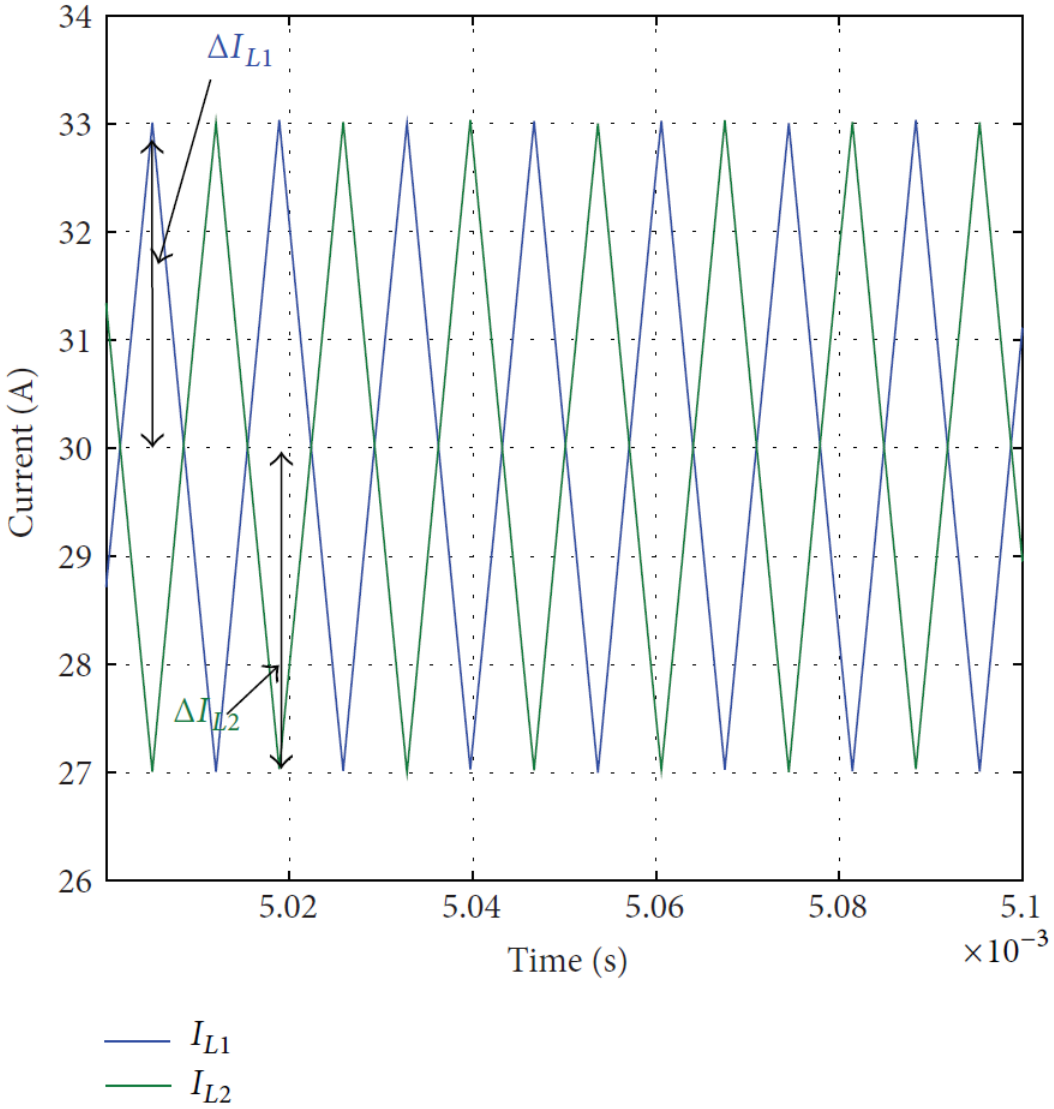


Figure 4-3.: Inductors currents waveform.

$$F_{sw} = \frac{(V_o + R_{Lf} \cdot I_o) \cdot D'}{2 \cdot L \cdot \Delta I_L} \tag{4-9}$$

Therefore, the SMC must be designed to ensure that both branches operate with a fixed maximum difference between their currents, which ensures that both branches exhibit the same duty cycle, average current, and ripple magnitude for any system condition. Finally, since the post-filter was designed using synchronous Buck converters, the CCM operation is granted.

4.1.2. POL converter

The main drawback of the post-filter is evident from (4-5), (4-6), and (4-7): the voltage conversion ratio is constant. Therefore, an additional Buck converter is used to regulate the load voltage. Figure **4-4** presents the proposed POL topology, named BuckPS, obtained from the cascade connection of a Buck converter (interacting with the source) with the post-filter (interacting with the load), where the Buck converter must be independently controlled to regulate the load voltage. Hence, such a Buck converter can be controller using classical approaches based on PWM drivers and PI or PID controllers, or any other approach.

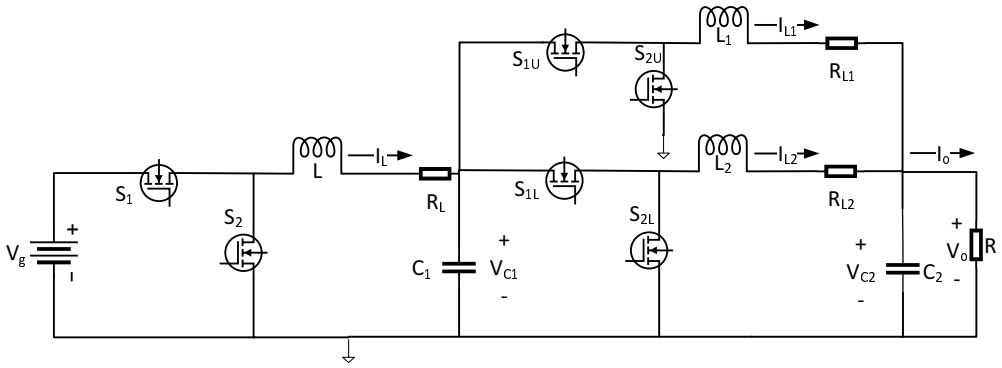


Figure 4-4.: Synchronized Buck converter with post-filter in interleaved operation (BuckPS).

To provide a design criterion, which also ensures a fair comparison with the classical POL based on a Buck converter (BuckS), the inductors of both the post-filter and the Buck converter are considered to be equal; thus $L = L_1 = L_2 = L_{Lf}$ and $R_L = R_{L1} = R_{L2} = R_{Lf}$.Then, the voltage conversion ratio of the BuckPS is given in (4-10), where D_{PS} represents the duty cycle of the Buck converter. Such an equation puts in evidence that the Buck converter could be independently controlled using a classical PWM-based technique.

$$\frac{V_o}{V_g} = \frac{2 \cdot D_{PS} \cdot R}{4 \cdot R + 3 \cdot R_L} \tag{4-10}$$

Moreover, the inductor current of the BuckPS first stage, that is, the Buck converter, and the output current are given in (4-11). Contrasting such results with the BuckS characteristics given in (4-2), it is recognized that the BuckPS requires three inductors instead of one, but such devices must support the half of the current imposed to the BuckS inductor.

$$I_L = \frac{D_{PS} \cdot V_g}{4 \cdot R + 3 \cdot R_L} \quad \wedge \quad I_o = \frac{2 \cdot D_{PS} \cdot V_g}{4 \cdot R + 3 \cdot R_L} \tag{4-11}$$

An additional condition of the BuckPS solution is extracted from (4-10): the voltage conversion ratio is always lower than 0.5. This condition is illustrated in Figure **4-5** considering four

cases for $\frac{R_L}{R} = \{0\,\%, 10\,\%, 25\,\%, 35\,\%\}$. In such an example, for $\frac{R_L}{R} = 10\,\%$, a $\frac{V_o}{V_g} = 0.25$ is obtained by operating the BuckPS at $D_{PS} = 0.5375$, while in a BuckS $D_S = 0.275$ is required to achieve the same voltage conversion ratio. In general, from (4-2) and (4-10) it is concluded that the BuckPS always provides lower output voltage than the BuckS for a given duty cycle. Such a condition is verified in Figure **4-5**. Hence, lower POL voltages can be achieved with the BuckPS by avoiding duty cycle saturations imposed by turn-ON and turn-OFF times of the MOSFETs, which limit the minimum operative duty cycle of the classical BuckS.

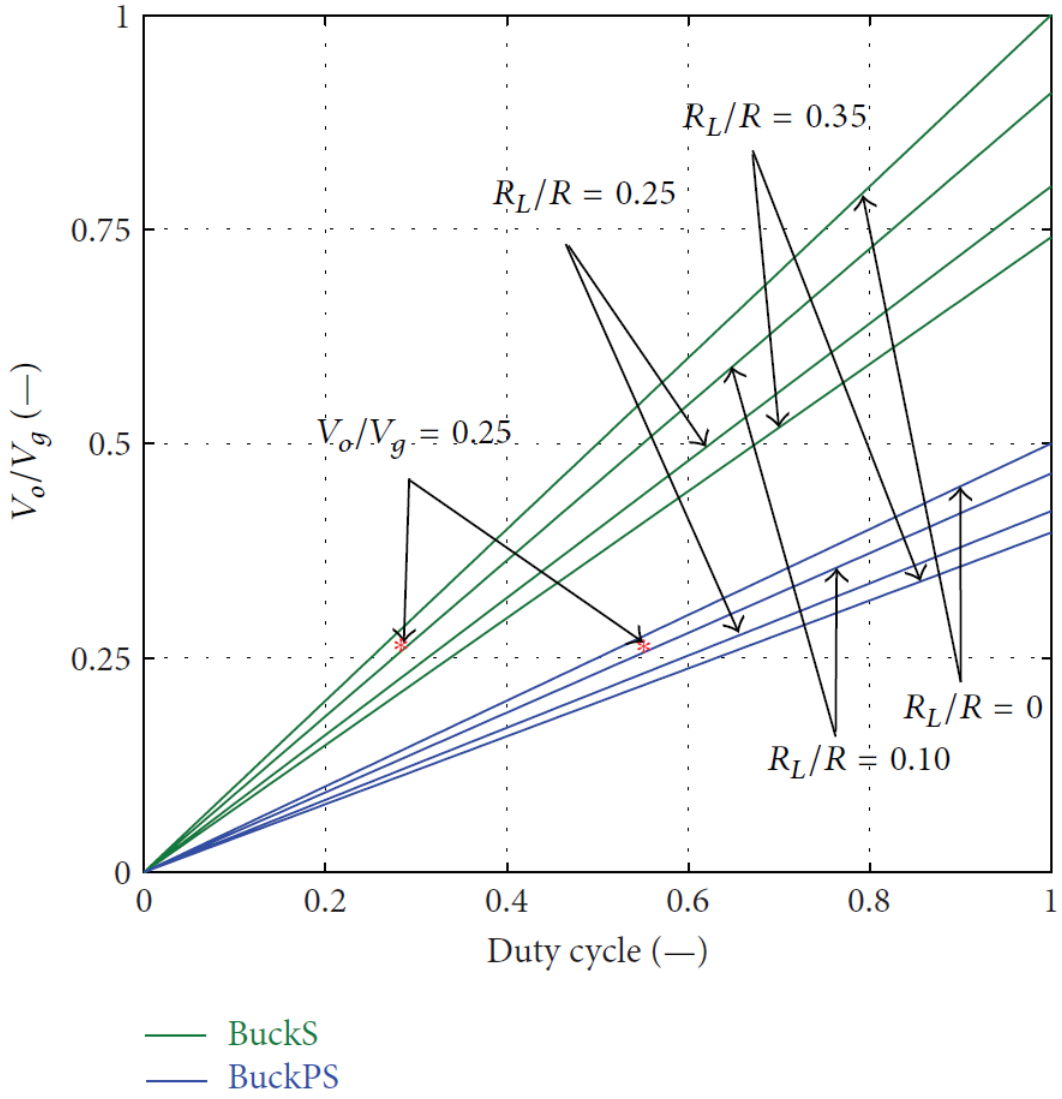


Figure 4-5.: Conversion ratio of BuckPS and BuckS.

Then, the efficiency of the BuckPS, given in (4-12), which is obtained from (4-10) and (4-11):

$$\eta_{BuckPS} = \frac{1}{1 + \frac{3}{4} \cdot \frac{R_L}{R}} \tag{4-12}$$

Such an expression shows an efficiency improvement over the BuckS (4-3). This improvement is achieved because the BuckPS generates currents in each of the three inductors equal to half of the inductor current in the BuckS. Therefore, since the power losses depend on the square of the current, the losses in the BuckPS are lower. To illustrate such an aspect, the resistance relation k_r, given in (4-13), and the efficiency factor α, given in (4-14), have been defined. In particular, $\alpha > 1$ implies an improved efficiency of BuckPS over BuckS, while $\alpha < 1$ implies a reduced efficiency of BuckPS in comparison with BuckS.

$$k_r = \frac{R_L}{R} \tag{4-13}$$

$$\alpha = \frac{\eta_{BuckPS}}{\eta_{BuckS}} = \frac{4 + 4 \cdot k_r}{4 + 3 \cdot k_r} \tag{4-14}$$

Since $k_r > 0$ for real values of R and R_L, $\alpha > 1$ is always granted in (4-14), which demonstrates that the proposed BuckPS solution is more efficient than the classical BuckS implementation. Figure **4-6** presents the efficiency improvement factor $\alpha - 1$, which quantifies the relative efficiency improvement of BuckPS over BuckS, for different values of the resistance relation k_r. Such numerical results illustrate the improved efficiency provided by the BuckPS solution.

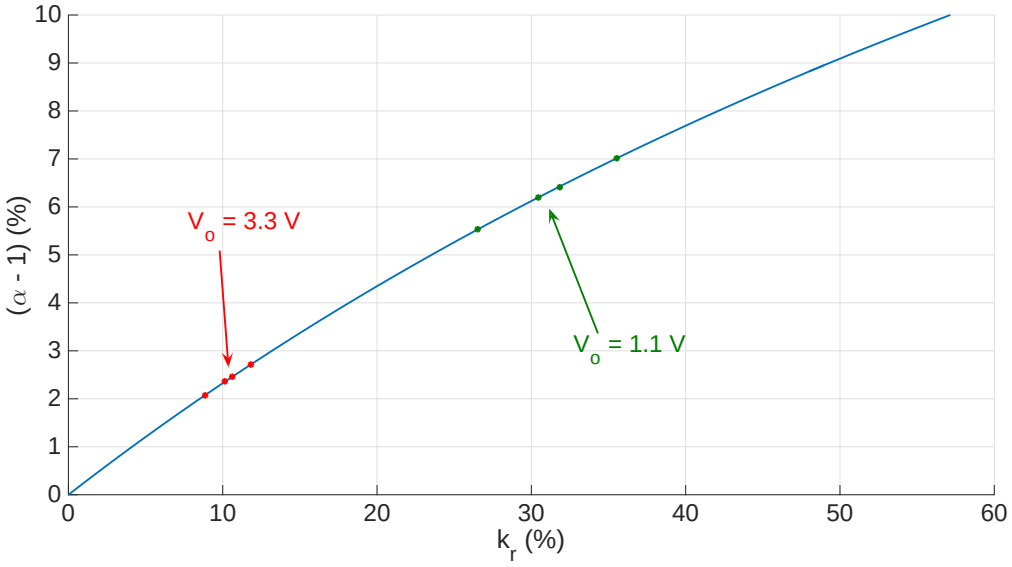


Figure 4-6.: Improvement efficiency factor.

Table **4-1** shows values of the efficiency improvement factor considering commercial elements [217]. The calculations were made for load currents (I_o) equal to $5A$, $20A$, $40A$, and $60A$, with a current ripple of 10 %. Moreover, R_L is calculated by adding the inductor resistance and the ON-resistance of the MOSFETs.Then, k_r and $\alpha-1$ have two values: the left value corresponds to a load voltage $V_o = 3.3V$, while the right value corresponds to $V_o = 1.1V$. In the first case, the efficiency improvement is near to 2.4 %, while in the second case the efficiency improvement is between 5.5 % and 7.0 %. Therefore, for modern microprocessors requiring low operation voltages, the proposed BuckPS could provide a significant improvement in the electrical efficiency.

Table 4-1.: Resistance relation and improvement efficiency factor with commercial elements.

Load (A)	$R_L(m\Omega)$	$k_r(\%)$		$\alpha-1(\%)$	
5	18.0 + 49.0	10.15	30.45	2.36	6.20
20	8.0 + 9.5	10.61	31.82	2.46	6.42
40	5.0 + 2.3	8.85	26.55	2.07	5.53
60	3.5 + 3.0	11.82	35.52	2.71	7.01

4.2. Sliding mode current control

The sliding-mode control technique has been extensively used in the literature to regulate power converters due to its robustness and speed [218]. Moreover, sliding-mode controllers have been also used to regulate active filters to improve power quality in AC environments [219]. In the same way, this chapter proposes to design a sliding-mode controller to regulate the post-filter, this with aim of ensuring the correct behavior of the system in any operation condition.

The controller design requires a state-space model of the POL converter. Therefore, the state-space system that describes the BuckPS dynamic behavior, depending on u_B (driving signal of the first Buck converter) and u_{1U} (driving signal of the post-filter), is given in (4-15). Such a system considers the states vector $x = [i_L \quad i_{L1} \quad i_{L2} \quad v_{C1} \quad v_{C2}]^T$ and follows the nomenclature defined in Figure **4-4**.

In (4-15) $u_{1U}^- = 1-u$, where $u_{1U} = 1$ means that MOSFET S_{1U} is turned ON and MOSFET S_{1L} is turned OFF, while $u_{1U} = 0$ means that MOSFET S_{1U} is turned OFF and MOSFET S_{1L} is turned ON.

Following the same approach proposed in [220], a sliding-mode controller was designed to regulate both post-filter inductor currents.The adopted sliding surface, given in (4-16), is intended to impose the same current to both post-filter branches.

$$\begin{aligned}
\dot{i_L} &= -\frac{R_L \cdot i_L}{L} - \frac{v_{C1}}{L} + \frac{V_g \cdot u_B}{L} \\
\dot{i_{L1}} &= -\frac{R_{L1} \cdot i_{L1}}{L_1} + \frac{v_{C1} \cdot u_{1U}}{L_1} - \frac{v_{C2}}{L_1} \\
\dot{i_{L2}} &= -\frac{R_{L2} \cdot i_{L2}}{L_2} + \frac{v_{C1} \cdot \bar{u_{1U}}}{L_2} - \frac{v_{C2}}{L_2} \\
\dot{v_{C1}} &= \frac{i_L}{C_1} - \frac{i_{L1} \cdot u_{1U}}{C_1} - \frac{i_{L2} \cdot \bar{u_{1U}}}{C_1} \\
\dot{v_{C2}} &= \frac{i_{L1}}{C_2} + \frac{i_{L2}}{C_2} - \frac{v_{C2}}{R \cdot C_2}
\end{aligned} \tag{4-15}$$

$$S(x) = i_{L1} - i_{L2} = 0 \tag{4-16}$$

But, to design a practical realization, the surface must be constrained into a hysteretic band $\pm H$, where the MOSFET commutation is determined by (4-17): when the difference between the inductor currents is smaller than the lower boundary of the hysteretic band $-H$, u_{1U} must be turned ON (set to 1); if the difference between the inductor currents is larger than the upper boundary of the hysteretic band $+H$, u_{1U} must be turned OFF (set to 0). Therefore, H defines the steady-state value of the currents ripple. Moreover, such surface $S(x) = 0$ imposes the same average value to both currents, which guarantee the correct operation of the post-filter. Figure **4-7** presents the logic scheme for both the sliding surface and the hysteretic comparator.

$$i_{L1} - i_{L2} < -H, \quad u_{1U} \quad set \quad to \quad 1 \quad \wedge \quad i_{L1} - i_{L2} > +H, \quad u_{1U} \quad set \quad to \quad 0 \tag{4-17}$$

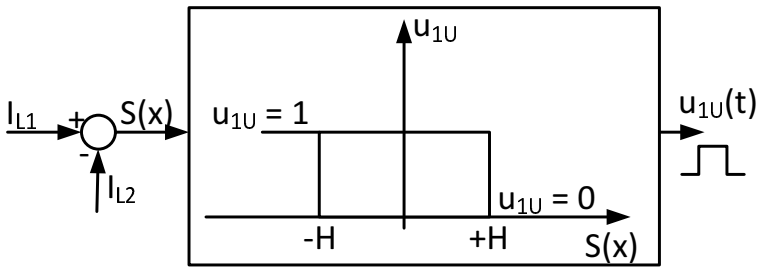


Figure 4-7.: Logic scheme of sliding-mode controller.

With aim of guarantee the global stability of the system, it is necessary to demonstrate the transversality, reachability and equivalent control conditions (see Subsections 3.1.1.1, 3.1.1.2 and 3.1.1.3) of the Buck converter with post-filter.

The ability to act on the system is guaranteed by fulfilling the transversality condition given in (4-18).

$$\frac{d}{du}\left(\frac{d\,S}{dt}\right) \neq 0 \tag{4-18}$$

Considering the sliding surface given in (4-16) and the state-space model of the Buck converter with post-filter given in (4-15) expression (4-19) is obtained.

$$\frac{d}{du}\left(\frac{d\,S}{dt}\right) = \frac{V_{C1} - V_{C2}}{L_f} \neq 0 \tag{4-19}$$

In such an expression L_f is the inductance of the inductors L_1 and L_2. Since the parasitic resistances on both branches are equal to R_L, and the load R and conversion voltage relation of the post-filter are given in (4-7), the condition that guarantee the system transversality is demostrated in (4-20): given that V_{C2}, R_{Lf}, R and L_f are values different to zero, the condition established in (4-20) is always fulfilled.

$$\frac{V_{C2} \cdot \frac{R_{Lf}}{R}}{L_f} \neq 0 \tag{4-20}$$

The necessary and sufficient conditions for surface reachability were discussed in Chapter 3 and defined in (4-21) for this case.

$$\lim_{S\to 0^-} \frac{dS(x)}{dt} > 0, \quad u_{1U} = 1 \quad \wedge \quad \lim_{S\to 0^+} \frac{dS(x)}{dt} < 0, \quad u_{1U} = 0 \tag{4-21}$$

The time derivative of the sliding surface given in (4-22) is obtained from (4-16). Then, by introducing the relation (4-16) into (4-21), and replacing also the second and third rows of (4-15) into (4-21), the expressions for surface reachability given in (4-23) are obtained.

$$\frac{dS(x)}{dt} = \frac{di_{L1}}{dt} - \frac{di_{L2}}{dt} \tag{4-22}$$

$$\begin{aligned}
\lim_{S\to 0^-} \frac{dS(x)}{dt} &= v_{C2} \cdot \left(\frac{1}{L_2} - \frac{1}{L_1}\right) + \left(\frac{R_{L2}}{L_2} \cdot i_{L2} - \frac{R_{L1}}{L_1} \cdot i_{L1}\right) + \frac{v_{C1}}{L_1} > 0 \\
\lim_{S\to 0^+} \frac{dS(x)}{dt} &= v_{C2} \cdot \left(\frac{1}{L_2} - \frac{1}{L_1}\right) + \left(\frac{R_{L2}}{L_2} \cdot i_{L2} - \frac{R_{L1}}{L_1} \cdot i_{L1}\right) + \frac{v_{C1}}{L_1} < 0
\end{aligned} \tag{4-23}$$

Since, for a practical implementation the post-filter inductors are selected equal ($L_f = L_1 = L_2$ and $R_{Lf} = R_{L1} = R_{L2}$), relation (4-23) is simplified as in (4-24). In such an expression it is evident that both inequalities are fulfilled, this is because inductors are always positive ($L_f > 0$) and Buck converters provide output voltages with the same polarity of the input voltage ($v_{C1} > 0$). Therefore, the surface reachability of the post-filter controller is always guaranteed.

$$\lim_{S\to 0^-} \frac{dS(x)}{dt} = \frac{v_{C1}}{L_f} > 0 \quad \wedge \quad \lim_{S\to 0^+} \frac{dS(x)}{dt} = -\frac{v_{C1}}{L_f} < 0 \tag{4-24}$$

The another important aspect in terms of control concerns the local stability, which is verified by using the equivalent control condition given in (4-25) [220], where u_{eq} represents an equivalent continuous control input that constrains the system evolution into the sliding surface.

$$\frac{dS(x)}{dt} = 0, \quad 0 < u_{eq} < 1 \tag{4-25}$$

From (4-22) and the second and third rows of (4-15), in which the control input u_{1U} has been replaced by the equivalent continuous variable u_{eq}, the condition given in (4-25) can be rewritten as in (4-26):

$$0 < u_{eq} = \frac{R_{L1} \cdot L_2 \cdot i_{L1} - R_{L2} \cdot L_1 \cdot i_{L2} + (L_2 - L_1) \cdot v_{C2} + L_1 \cdot v_{C1}}{(L_1 + L_2) \cdot v_{C1}} < 1 \tag{4-26}$$

Taking into account that the inductors are selected equal, then (4-26) becomes (4-27):

$$0 < R_{Lf} \cdot L_f \cdot (i_{L1} - i_{L2}) + L_f \cdot v_{C1} < 2 \cdot L_f \cdot v_{C1} \tag{4-27}$$

Therefore, the difference between the inductor currents must satisfy (4-28) to guarantee local stability.

$$-\frac{v_{C1}}{R_{Lf}} < i_{L1} - i_{L2} < \frac{v_{C1}}{R_{Lf}} \Rightarrow \mid i_{L1} - i_{L2} \mid < \frac{v_{C1}}{R_{Lf}} \tag{4-28}$$

To ensure that relation (4-28) is fulfilled in any condition, the maximum magnitude of the inductors current difference must be constrained as in (4-29).

$$max \mid i_{L1} - i_{L2} \mid = \Delta_{max} < \frac{v_{C1}}{R_{Lf}} \tag{4-29}$$

From the second and third rows of (4-15), with $u_{1U} = 1$ and $\bar{u}_{1U} = 0$, the ripple magnitudes of both post-filter currents, defined in Figure **4-3**, are given in (4-30). It is noted that the maximum difference between the inductor currents is constrained by the sum of such ripple magnitudes as in (4-31).

$$\Delta I_{L1} = \frac{T}{4 \cdot L_f}(-R_{Lf} \cdot i_{L1} + v_{C1} - v_{C2}) \quad \wedge \quad \Delta I_{L2} = -\frac{T}{4 \cdot L_f}(-R_{Lf} \cdot i_{L2} - v_{C2}) \tag{4-30}$$

$$\Delta_{max} = \Delta I_{L1} + \Delta I_{L2} \quad \wedge \quad \Delta_{max} = \frac{T}{4 \cdot L_f}(-R_{Lf} \cdot (i_{L1} - i_{L2}) + v_{C1}) \tag{4-31}$$

Since the maximum difference between the inductor currents is $\mid i_{L1} - i_{L2} \mid = \Delta_{max}$, expression (4-31) must consider $i_{L1} - i_{L2} = \Delta_{max}$.Therefore, the maximum difference between the inductor currents is given in (4-32).

$$\Delta_{max} = \frac{v_{C1}}{(4 \cdot \frac{L_f}{T}) + R_{Lf}} \tag{4-32}$$

Then, equivalent control condition of the sliding-mode controller given in (4-29) is rewritten as in (4-33).

$$\frac{v_{C1}}{(4 \cdot \frac{L_f}{T}) + R_{Lf}} < \frac{v_{C1}}{R_{Lf}} \tag{4-33}$$

Such an inequality leads to the condition given in (4-34), which is fulfilled for any operating condition since both the inductance and switching period are positive quantities. Hence, relation (4-34) confirms the equivalent control condition of the proposed sliding-mode controller.

$$\frac{4 \cdot L_f}{T} > 0 \tag{4-34}$$

Therefore, since surface reachability is guaranteed by (4-24) and the equivalent control condition is guaranteed by (4-34), the proposed sliding-mode controller always drives the post-filter, from any initial condition, to operate within the space $\mid i_{L1} - i_{L2} \mid < H$, which ensures the same average current for both branches and a maximum current difference constrained to H. Such characteristics ensure a correct operation of the post-filter.

4.3. Application example

A realistic application was considered to illustrate the operation and advantages of the proposed POL structure by means of circuital simulations. The example considers a POL regulator designed to supply an Intel Core 2 Duo processor [221, 222], which requires a regulated $1.1V$ with 1 % voltage ripple and $60A$. Then, the POL converter was designed to provide a maximum voltage ripple equal to $11mV$ with a constant current ripple in the load equal to 10 % of the maximum load current ($6A$). Moreover, the switching frequency was selected equal to $100kHz$ for the single Buck converters and near to $100kHz$ for the post-filter. Therefore, the inductors were calculated equal to $1.5\mu H$. Similarly, the capacitors were calculated to fulfill the desired voltage ripple, hence all the capacitors were selected equal to $280\mu F$. Moreover, the parasitic resistance for the single Buck converter and each post-filter branches is extracted from the last row of Table **4-1**, which for all the inductors and MOSFETs are equal to $6.5m\Omega$. Finally, the application considers a $12V$ DC bus.
Figure **4-8** shows the practical implementation of the proposed POL regulator to supply the Core 2 Duo processor. Such a scheme shows the two control systems required: the sliding-mode controller to regulate the post-filter, named SMC, and a PID controller acting on the Buck converter to regulate the load voltage.

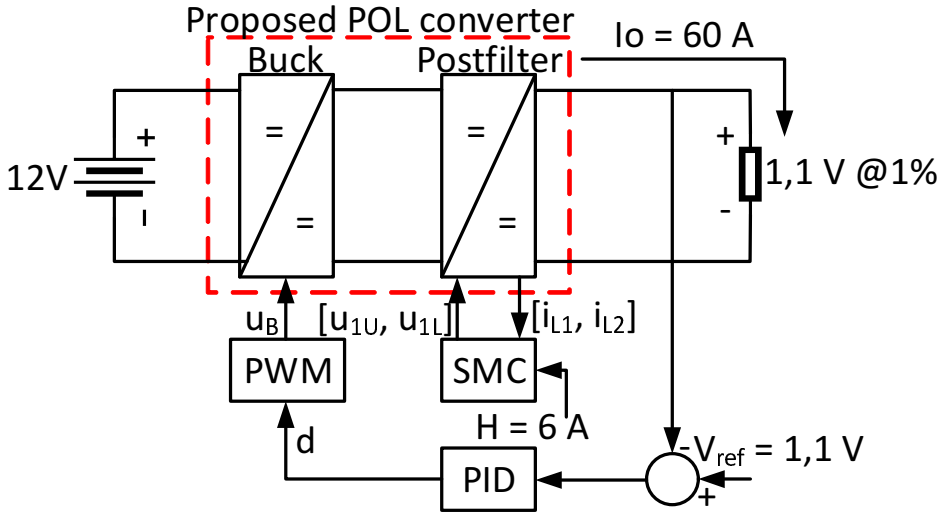


Figure 4-8.: Practical implementation of the proposed Core 2 Duo POL regulator.

Figure **4-9** shows the post-filter operation in two conditions: start-up and load transient. The former one considers the start-up of the POL converter, where the voltage and currents of all the capacitors and inductors are zero. The time simulation of the post-filter (top-left) shows the satisfactory current ripple cancellation, where the output current I_o is almost ripple free. It must be pointed out that in such a figure I_o is presented divided by 2 to be in the same scale of the post-filter inductor currents. In addition, the figure also presents, in

black traces, the maximum limits of the inductors current difference, which is in agreement with the current ripple condition imposed by the application ($6A$). From such a behavior it is noted that, in the start-up condition, the sliding-mode controller successfully guarantees the correct post-filter operation: both inductor currents have the same average current and the same current ripple, which produces a fixed duty cycle equal to 0.5 to ensure the ripple cancellation.

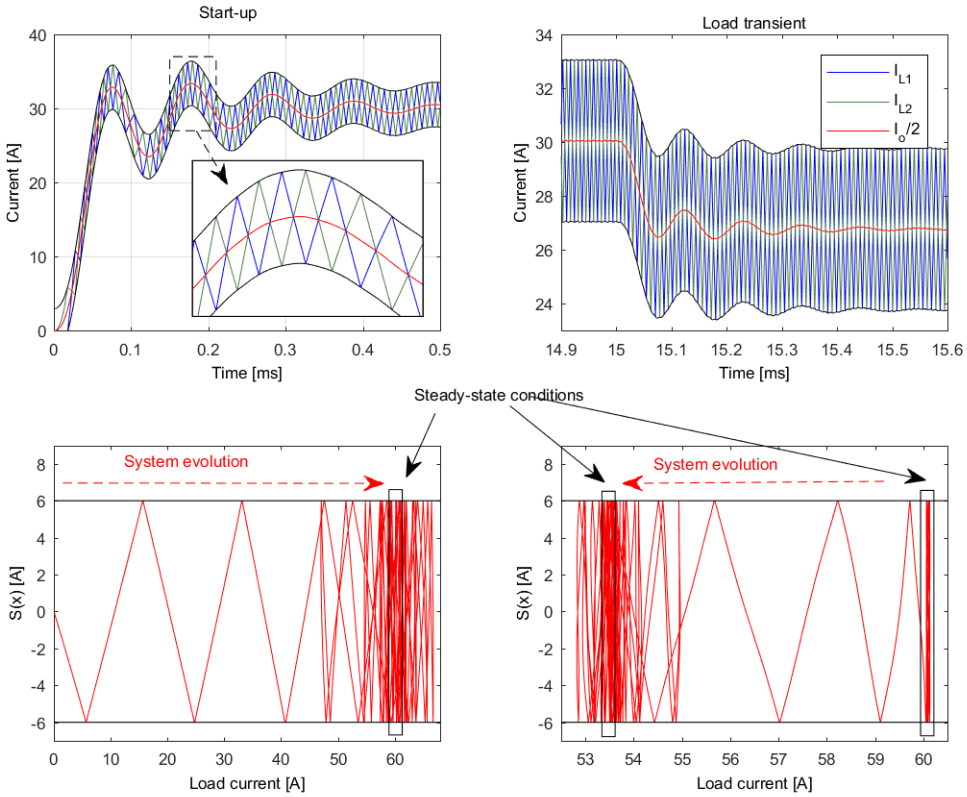


Figure 4-9.: Post-filter simulation: start-up and load transient conditions.

The post-filter phase plane for the start-up operation is also presented at the bottom-left figure, where it is confirmed that the system operates into the sliding surface for any steady-state or transient condition.

The same behavior is achieved for a step-down load transient, which is presented in the figure at top-right, where a 10 % load perturbation was introduced. Similar to the start-up case, in this transient condition the post-filter provides an almost ripple-free load current, while the system is always operating within the sliding surface (depicted at the bottom-right). Therefore, the simulation in Figure **4-9** confirms both the correct operation of the post-filter and the stability of the sliding-mode controller predicted in (4-24) and (4-34) for any operation condition.

Another component to design in the proposed POL solution concerns the load voltage regulator, named PID in Figure **4-8**. To design such a controller, the post-filter is modeled including the closed loop with the sliding-mode controller, where both inductor currents are equal and the duty cycle of the post-filter is 0.5. Therefore, the state-space (4-15) is simplified as given in (4-35), where the single control variable is u_B.

$$\begin{aligned} \dot{i_L} &= -\frac{R_L \cdot i_L}{L} - \frac{v_{C1}}{L} + \frac{V_g \cdot u_B}{L} \\ \dot{i_{Lf}} &= -\frac{R_{Lf} \cdot i_{Lf}}{L_f} + \frac{v_{C1}}{2 \cdot L_f} - \frac{v_{C2}}{L_f} \\ \dot{v_{C1}} &= \frac{i_L}{C_1} - \frac{i_{Lf}}{C_1} \\ \dot{v_{C2}} &= \frac{2 \cdot i_{Lf}}{C_2} - \frac{v_{C2}}{R \cdot C_2} \end{aligned} \tag{4-35}$$

Then, using the PWM-based averaging technique described in [223, 134], the state-space system in (4-35) is linearized by replacing u_B with the duty cycle of the Buck converter. Such a system is used to design the PID controller. In this example, the PID controller was designed in agreement with the following criteria: closed loop bandwidth equal to $6kHz$, phase margin higher than $60°$, and gain margin higher than $6dB$. The design of the controller was performed in SISOTOOL from Matlab®, obtaining the expression given in (4-36).

$$PID(s) = 1200 \cdot \frac{1 + 3.1 \times 10^{-5} \cdot s}{s} \tag{4-36}$$

To illustrate the improvement of the proposed POL, a BuckS POL was also designed and simulated. Figure **4-10** compares the BuckS and BuckPS output voltage ripples, obtaining magnitudes of 3.1 % and 0.032 %, respectively. Such results put in evidence the large reduction in the voltage ripple provided by the proposed solution, which avoids the requirement of electrolytic capacitances. Similarly, Figure **4-11** shows the power spectral density (PSD) of the output voltage harmonics for both the BuckS and BuckPS, where a large harmonic component at $100kHz$ produced by the BuckS is observed, while the BuckPS exhibits a much attenuated component due to the complementary inductor currents of the post-filter. The simulation also shows that the BuckPS produces a different PSD due to the contribution of both inductor currents, which results in a new harmonic component at $143kHz$. In any case, those results confirm the improvement in the power quality provided to the load by means of the proposed solution.

To show the overall system performance, Figure **4-12** shows the dynamic behavior of the BuckPS under a load transient. In such a case, the PID controller must regulate the load voltage while the sliding-mode controller regulates the post-filter. The simulation considers a load current perturbation equal to 10 % of the steady-state value (from $60A$ to $66A$). The

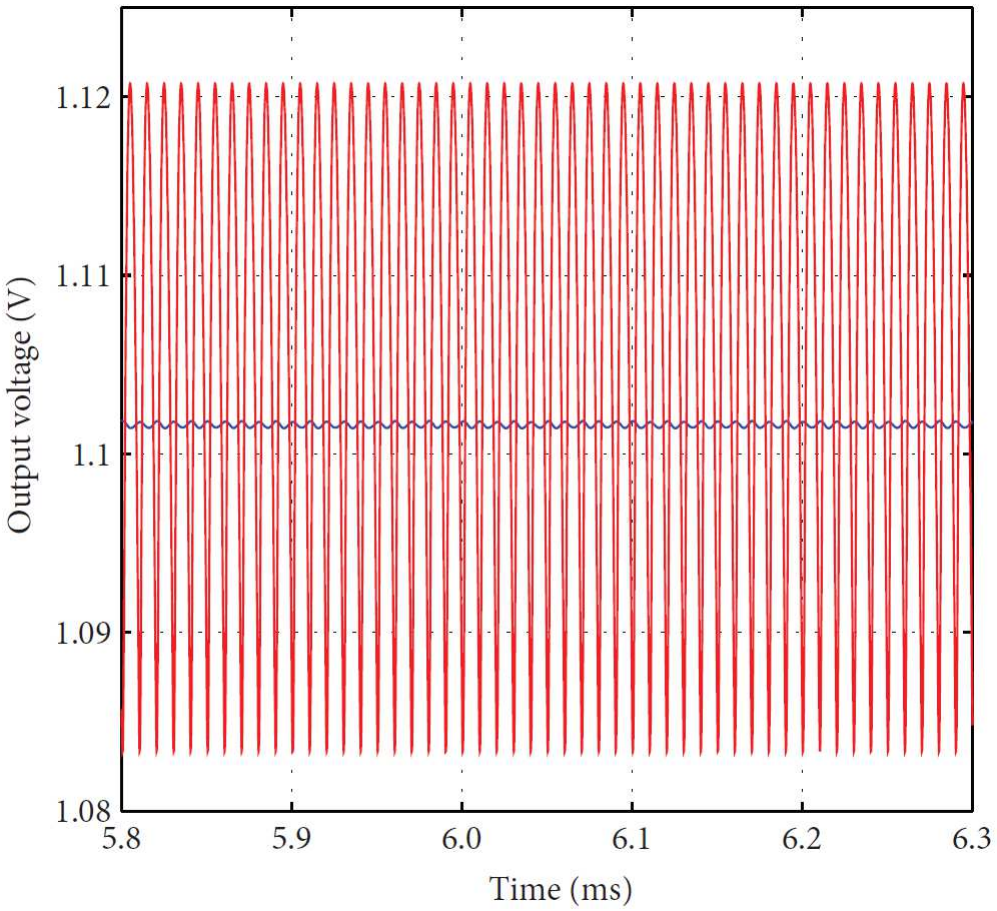


Figure 4-10.: Output voltage ripple comparison between BuckS and BuckPS.

results show the satisfactory compensation of the load voltage provided by the PID controller given in (4-36). Similarly, Figure **4-12** also shows the satisfactory regulation of the post-filter inductor currents. Such a correct operation of the sliding-mode controller is also evident from the system evolution reported in the bottom figure, where the system operation is always constrained within the sliding surface $S(x)$ for any condition.
It must be point out that a more complex controller for the Buck converter, such as a high-order lead-lag structure, could be used to improve the output voltage dynamics.

4.4. Conclusions

This chapter has presented a POL converter based on the cascade connection of an interleaved post-filter with a Buck converter. This solution, named BuckPS, has the aim of improving the quality of the power provided to the load, which is achieved by reducing the output voltage ripple. Moreover, the BuckPS provides an improved efficiency (between 2.5 % and 7.5 %) over a classical POL based on a single Buck converter, named BuckS. Similarly, since the BuckPS

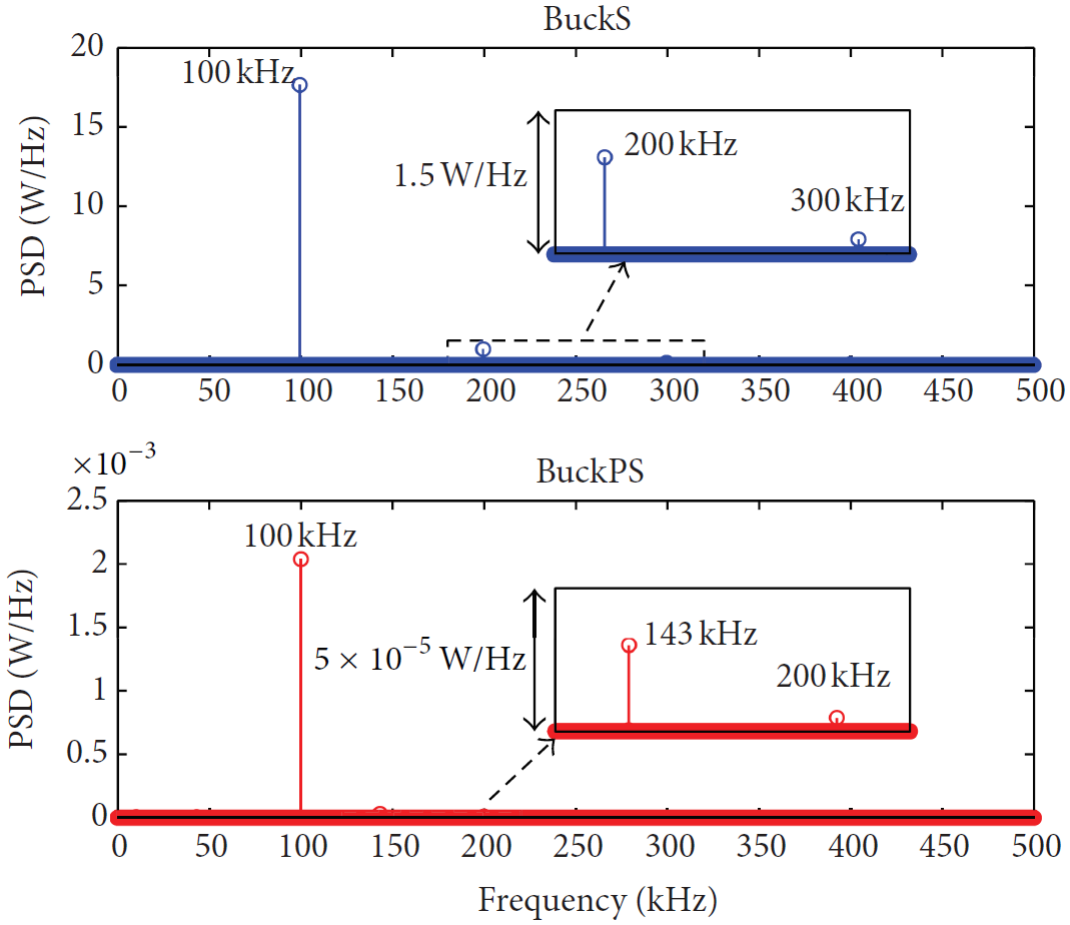


Figure 4-11.: Power spectral density of BuckS and BuckPS.

strongly reduces the output current ripple, its output capacitor could be significantly smaller in comparison with the classical BuckS implementation. This characteristic allows designing the BuckPS without using electrolytic capacitances, which improves the system reliability [224].

Despite the advantages of the BuckPS structure, it requires more elements and its regulation strategy is more complex in comparison with the BuckS, which could lead to a more costly device. In any case, the elements required by the BuckPS have lower ratings, therefore lower cost, which is especially important for the output capacitor: in BuckS structures a large electrolytic capacitor is required, which increases the system size and cost. Therefore, a comparison between the cost and size of BuckS and BuckPS solutions depends on the specific application conditions. This new BuckPS POL solution corresponds to the sixth contribution of the Thesis.

To illustrate the benefits of the proposed solution, a practical application based on real load requirements was analyzed and simulated. The simulation results of such an example confirm the correctness of the POL converter and the stability of the sliding-mode controller. In the

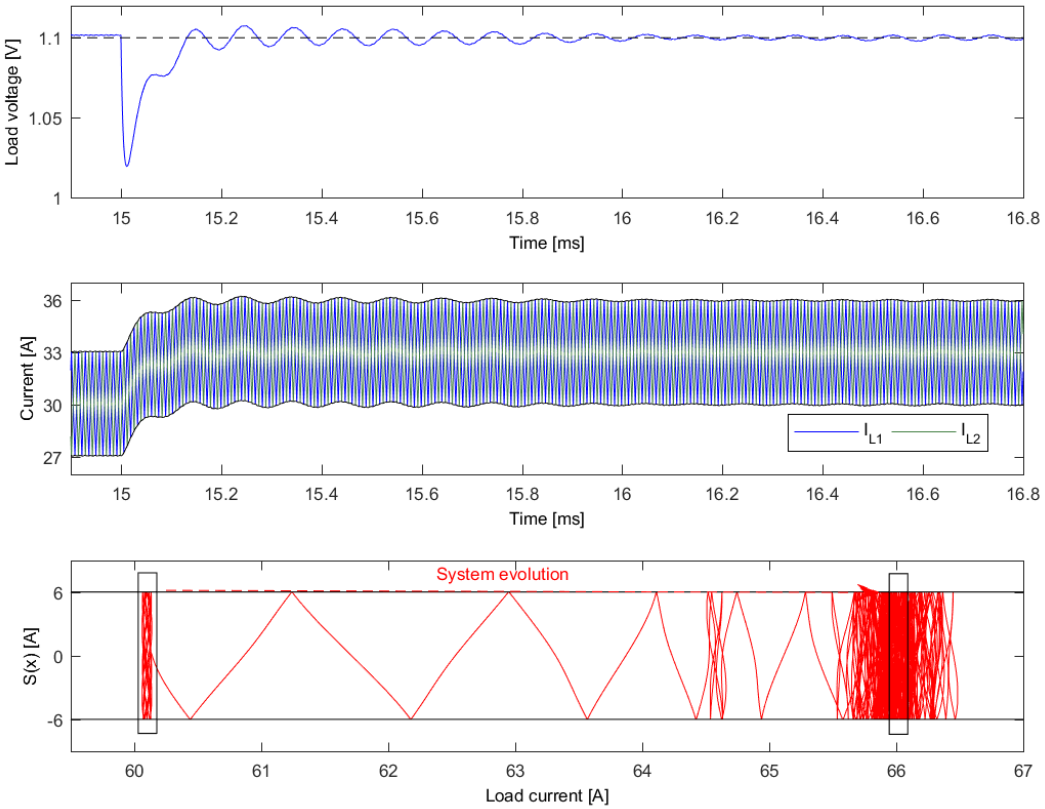


Figure 4-12.: Dynamic behavior of the BuckPS output voltage.

same way, the simulation also puts in evidence the improvement of the proposed BuckPS regulator over a classical BuckS solution.

Finally, this chapter describes an analog implementation of the POL controllers. Therefore, a future research may be focused on the digital implementation of the POL control system to provide a more flexible and industrial oriented solution. In such a further work, one of the open problems concerns the fast acquisition of the post-filter currents since the sampling circuit could filter such high-frequency signals. Similarly, the time-delay effect generated by the acquisition and processing circuits could introduce errors in the sliding-mode comparator, degrading the controller accuracy and stability.

A final improvement concerns the design of a different voltage controller aimed at reducing the settling-time of the load voltage after a transient occurs.

5. Conclusions

This Thesis has proposed solutions to some issues present in a stand-alone DC power system, which are related with the source, the DC-bus and the DC-load. The power system is based in the architecture described in Figure **1-1**, which consist of a photovoltaic power source, a charger/discharger system for batteries and an DC-load. This power system is used in energy supply systems for telecommunication equipment, electric vehicles, irrigation systems, heating systems, and so on. The following issues were identified at the power system: maximizing the power extraction of the photovoltaic source, the DC-bus voltage regulation and the improvement of the efficiency and quality of the power delivered to DC-load.
For the building of this Thesis it was developed an exhaustive review of the state-of-the-art concerning the issues previously described. Such a review includes more than two hundred works published in both international journal and conferences.
Moreover, this Thesis provide six contributions to the state-of-the-art:

1. A model of photovoltaic generation systems based on a distributed MPPT structure.

2. A vectorial MPPT algorithm for distributed photovoltaic system.

3. A reconfiguration algorithm for PV arrays in a SP structure, based on the I-V curves of commercial PV panels.

4. An adaptive sliding-mode (SMC) controller that provides a regulated DC-bus voltage in any operation condition.

5. A second SMC to regulate the bidirectional DC/DC converter interfacing a battery and a DC bus, which provides a satisfactory regulation of the DC bus voltage, improving the compensation of bus perturbations with respect to the SMC previously proposed.

6. A DC/DC converter based on Buck topology and a post-filter for improving both the quality and efficiency of the power provided to the load, in comparison with the classical Buck converter.

The first, the second and the third contributions aim to extract the maximum power of a renewable power source based on a PV array. The fourth and fifth contributions aim to regulate the DC-bus voltage using a SMC on the charger/discharger DC/DC converter. The mainly difference between those two contributions is that the fifth contribution improves

the compensation of bus perturbations by taking into account and additional measurement. Finally, the sixth contribution minimize the voltage ripple produced by switching of the DC/DC power converter interacting with the load. This is achieved with a modification of the classical Buck converter topology used for POL applications, adding a post-filter formed by two interleaved Buck converters. This post-filter minimizes the current ripple by canceling the ripple of both branches. Likewise, splitting the load current between both branches decrease the ohmic losses, which improves the efficiency of system.

The maximization of the power extraction in renewable power sources based on photovoltaic panels was faced in three ways (see Chapter 2). First it was considered several PV-converter set connected in series, with the first PV-converter set connected to the positive DC-bus voltage and the last PV-converter set connected to negative DC-bus voltage. For this distributed photovoltaic system composed by N PV-converter sets in series, it was developed a mathematical model, which can easily be implemented in a high-level language, like C, to run on an electronic simulation software, on a DSP or on an industrial computer for simulation or hardware-In-the-Loop (HIL) purposes.

This software module has the following advantages: it could run on free software platforms, e.g. it can be implemented in programming languages like C or Python™; it could be implemented on low-cost hardware platform, like DSP, FPGA, SBC (single board computer) or microcontroller, as long as their speed allow a real-time emulation of the system. Similarly, the module also could be implemented on circuits or systems professional simulators like PSIM®, Matlab® or Scilab™,using embedded C-Block on PSIM®, S-function on Simulink® or called by a function in Scilab™. The module may be also deployed on high-performance industrial computers, like Speedgoat®, CompactRIO® or PXI system, which are very common in the industry. However, the main advantage of this mathematical model of a distributed photovoltaic system is the simplicity to define the system, since only the number of modules and the electrical parameters need to be defined, while the differential equations system is built automatically. Instead, in simulators like in PSIM® or Matlab®, it is necesarry draw the schematic or to write the differential equations system, which is a non-trivial task if the renewable source is compose by many PV-converters sets. Using this mathematical model it is possible to evaluate any MPPT, either scalar or vectorial. However, the mathematical model is only for PV-converters sets in series, others topologies are not considered.

The second contribution is a multi-output perturb & observe vectorial (MOPOV) algorithm. The MOPOV algorithm is based on a vectorial representation of the operating point of the system using spherical coordinates. MOPOV perturbs a variable, $|Vec|$ or θ_i, generating a simultaneous perturbation on all PV voltages. In this way, the MOPOV algorithm provides a shorter MPP trajectory than the multi-output P&O Cartesian, reducing the power loss. Although the single-output P&O (SOPO) algorithm extracts more power, the MOPOV algorithm provides a satisfactory trade-off between implementation cost and energy production, since it uses a single I/V sensor.

The third contribution was a reconfiguration algorithm. This technique allows to dynamically change the PV-array topology in agreement with the shading conditions of the photovoltaic panels to set a different maximum power point condition. The algorithm is deterministic, hence it always gives the same result under the same conditions, since it evaluates all possibilities and and select the one that produces the higher power. This algorithm exhibits run-times of tens of seconds, according to the number of PV-converters sets, which is useful for small PV-arrays. Due all possible configurations are evaluated, large PV arrays will require a high-performance computer system in order to obtain the results within a practical time interval.

The fourth and fifth contributions aim to regulate the DC-bus voltage under any operating condition (see Chapter 3): ESD (energy storage devices) charge, ESD discharge or even without any power exchange between the ESD and the DC-bus. The DC-bus voltage regulation strategy is based in an adaptive sliding-mode controller, where the sliding surface is a PI function of the DC-bus voltage error plus the ESD current for the third contribution; while the fourth contribution includes also the DC-bus current. The constants of the sliding-surfaces of both contributions depend of the duty-cycle, which requires an on-line calculation of surface parameters.

The sliding-surface defined in the fourth contribution improves the general performance of the system, since the overshoot and the settling time are reduced in comparison with the sliding surface defined in the third contribution. However, such as improvement in the performance requires the measurement of DC-bus current, which increases the complexity of the system.

Furthermore, those contributions define a design process of the controller to select the desired transient response. This design process also guarantees the system globally stability, since the conditions of transversality, reachability and equivalent control are always fulfilled.

The last contribution is related with the power delivery to the load (see Chapter 4). This is a issue that must be faced according to the load type. In this Thesis was considered a DC-load of high-current and low-voltage, known as Point-of-Load (POL), which is typical in electronic devices used in computing, communications, electrical vehicles, among others. The POL are highly sensible to voltage oscillations, which are quite common in switched converters. For this reason, the main goal of this solution was to reduce the current ripple delivered to the load. This solution was achieved with the design of an interleaved post-filter with two branches and a classical Buck converter. Splitting by two the current of the classical Buck allows to cancel the current ripple using complementary commutation of the interleaved post-filter.

This was achieved by defining a sliding-surface equal to the subtraction between the currents of each branch of the post-filter. However, the small difference between the parameters of the electrical components of each branch makes difficult a total cancellation of the ripple. In any case, this control strategy provides a voltage ripple below 1 % of the nominal voltage, which is usually into the specifications of devices powered by a POL.

Moreover, the ohmic losses depend of the square of the current, hence the overall efficiency is increased. Therefore, this solution improves both the quality and efficiency of the power delivered to the load.

Finally, the topics addressed in this Thesis are only a part of all the issues related to DC-microgrid. In this way, this Thesis was aimed to solve some of the issues present in three fundamental elements of a DC-microgrid: the PV source, the DC-bus and the load. Other important topics that must be addressed are, for example, to consider solutions to maximize the power extraction in other renewable sources like wind-power, fuel cells, among others. Likewise, in the solutions for the battery charger/discharger not have been considered neither the state-of-charge or state-of-health estimation. Moreover, solutions that improve the transient response of the POL converter must be developed.

Finally, the management algorithms of the sources and the loads must be improved to provide higher efficiency and safety. This is a very important issue currently, approached, mainly, using intelligent control, but formal controllers ensuring global stability could be developed.

A. Appendix: Publications

The main results of this PhD thesis have been or are intended to be published in journal papers and conference proceedings. The papers below are published or accepted for publication in journals or conference proceedings, and they contribute to the divulgation of the research results.

A.1. Journal articles

1. S. Serna-Garcés, D. Gonzalez Montoya, and C. Ramos-Paja, "Control of a Charger/Discharger DC/DC Converter with Improved Disturbance Rejection for Bus Regulation", *Energies*, vol. 11, p. 594, mar 2018. Scimago-JR (Scopus) 2018 (Q1), Publindex 2018 (A1).

2. S. Serna-Garcés, D. González Montoya, and C. Ramos-Paja. "Sliding-Mode Control of a Charger/Discharger DC/DC Converter for DC-Bus Regulation in Renewable Power Systems", *Energies*, vol. 9, p. 245, mar 2016. Scimago-JR (Scopus) 2016 (Q1), Publindex 2016 (A1).

3. E. E. Henao-Bravo, D. A. Márquez-Viloria, J. P. Villegas-Ceballos, S. I. Serna-Garcés, C. A. Ramos-Paja, and D. González-Montoya. "Modelo matemático de sistemas fotovoltaicos para búsqueda distribuida del punto de máxima potencia", *Tecno Lógicas*, vol. 19, pp. 107-124, 07 2016. Scimago-JR (Scopus) 2016 (Non-indexed), Publindex 2016 (A2).

4. S. Serna-Garcés, J. Bastidas-Rodríguez, and C. Ramos-Paja. "Reconfiguration of Urban Photovoltaic Arrays Using Commercial Devices", *Energies*, vol. 9, p. 2, dec 2015. Scimago-JR (Scopus) 2015 (Q1), Publindex 2015 (A1).

5. S. I. Serna-Garcés, R. E. Jiménez, and C. A. Ramos-Paja. "Sliding-Mode Control of a Dc/Dc Postfilter for Ripple Reduction and Efficiency Improvement in POL Applications", *Journal of Applied Mathematics*, vol. 2013, pp. 1-10, 2013. Scimago-JR (Scopus) 2013 (Q3), Publindex 2013 (A2).

A.2. Conference papers

1. C. A. Ramos-Paja, D. Gonzalez Montoya, and S. I. Serna-Garcés. "Hybrid linear/non-linear adaptive controller for battery charger/discharger in renewable power systems", in *VIII Simposio Internacional sobre Calidad de la Energía Eléctrica - SICEL 2015*, (Valparaiso, Chile), pp. 127-132, Universidad Técnica Federico Santamaría, nov 2015.

2. J. P. Villegas-Ceballos, D. Márquez-Viloria, E. Henao-Bravo, and S. I. Serna-Garcés. "Rastreo del punto de máxima potencia multivariable para un arreglo de paneles fotovoltaicos", in *Simposio de Investigación USTAMED*, (Medellín, Colombia), pp. 340-352, Universidad Santo Tomás - sede Medellín, nov 2015.

3. C. A. Ramos-Paja, G. Spagnuolo, G. Petrone, S. I. Serna-Garcés, and A. Trejos. "A vectorial MPPT algorithm for distributed photovoltaic applications", in *2013 International Conference on Clean Electrical Power (ICCEP)*, (Alghero, Italy), pp. 48-51, IEEE Industrial Electronics Society, jun 2013.

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