HIGH PERFORMANCE CMOS INTEGRATED CIRCUITS FOR OPTICAL RECEIVERS

A Dissertation

by

MOHAMMADREZA SAMADIBOROUJENI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2006

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Aydin Karsilayan
Committee Members,	Jose Silva-Martinez
	Reza Langari
	Prasad Enjeti
Head of Department,	Costas Georghiades

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ABSTRACT

High Performance CMOS Integrated Circuits for Optical Receivers.

(December 2006)

MohammadReza SamadiBoroujeni, B.S., Isfahan University of Technology;

M.S., University of Tehran

Chair of Advisory Committee: Dr. Aydin Karsilayan

Optical communications is expanding into new applications such as infrared wireless communications; therefore, designing high performance circuits has gained considerable importance. In this dissertation a wide dynamic-range variable-gain transimpedance amplifier (TIA) is introduced. It adopts a regulated cascode (RGC) amplifier and an operational transconductance amplifier (OTA) as the feed forward gain element to control gain and improve the overload of the optical receiver. A fully-differential variable-gain TIA in a 0.35μm CMOS technology is realized. It provides a bit error rate (BER) less than 10^{-12} for an input current from 6μA-3mA at 3.3V power supply. For the transimpedance gain variation, from 0.1kΩ to 3kΩ, -3dB bandwidth is higher than 1.7GHz for a 0.6pF photodiode capacitance. The power dissipations for the highest and the lowest gains are 8.2mW and 24.9mW respectively.

A new technique for designing uniform multistage amplifiers (MA) for high frequency applications is introduced. The proposed method uses the multi-peak bandwidth enhancement technique while it employs identical, simple and inductorless stages. It has several advantages, such as tunability of bandwidth and decreased sensitivity of amplifier stages, to process variations. While all stages of the proposed MA topology are identical, the gain-bandwidth product can be extended several times. Two six-stage amplifiers in a TSMC 0.35μm CMOS process were designed using the proposed topology. Measurements show that the gain can be

varied for the first one between 16dB and 44dB within the 0.7-3.2GHz bandwidth and for the second one between 13dB and 44dB within a 1.9-3.7GHz bandwidth with less than 5.2nV/√Hz noise. Although the second amplifier has a higher gain bandwidth product, it consumes more power and occupies a wider area.

A technique for capacitance multiplication is utilized to design a tunable loop filter. Current and voltage mode techniques are combined to increase the multiplication factor (M). At a high input dynamic range, M is adjustable and the capacitance multiplier performs linearly at high frequencies. Drain-source voltages of paired transistors are equalized to improve matching in the current mirrors. Measurement of a prototype loop filter IC in a 0.5μm CMOS technology shows 50μA current consumption for M=50. Where 80pF capacitance is employed, the capacitance multiplier realizes an effective capacitance varying from 1.22nF up to 8.5nF.

To my wife, Homayra

ACKNOWLEDGEMENTS

I would like to acknowledge the many individuals who have contributed to the completion of my research. First, I would like to thank my advisor, Dr. Aydin Karsilayan, for his guidance, encouragement, and support. He has been extremely generous in his time and resources and has provided valuable assistance in every single step of my research and writing. I am also grateful to my committee members, Dr. Jose Silva-Martinez who has kept me focused and provided me with insight from his own experiences, Dr. Reza Langari who has been a real mentor to me and has generously spent time on guiding me, and Dr. Prasad Enjeti who agreed to be on my committee at a very short notice. I would also like to thank Dr. Mercer who was originally on my committee, but who retired before my defense. I thank you all for your dedication toward helping me attain this goal. Furthermore, I would like to extend my appreciation to Dr. Edgar Sanchez-Sinencio who, in the first place, provided the opportunity for me to come to Texas A&M and continued supporting and guiding me throughout my studies.

In the University's Department of Engineering Technology and Industrial Distribution Dr. Rainer Fink and Dr. Ben Zoghi have helped me in countless ways. They have always had encouraging words, bright smiles, helping hands and positive outlooks. While pursuing my studies, I was fortunate to work as a graduate assistant to them.

I wish also to express my sincere appreciation and gratitude to Advanced Micro Devices (AMD) in South Austin for generously letting me use their lab equipment and instruments to carry out my tests for my dissertation. I give special thanks to my supervisors and colleagues in the Physical Design Group who have been extremely understanding, patient and cooperative during the time I have been working on my dissertation.

Next, I want to express my deepest gratitude to my wife without whose love, patience, encouragement and support, I would have been unable to survive in this doctoral process. Truly I cannot find the words to express my appreciation of her and what she has done for me.

Finally I would like to thank my parents for giving me the value of life. They have always encouraged me to be persistent and fight for what I believe in.

Completing this dissertation was a journey that I did not have to take alone due to the patience and unwavering support provided by all those mentioned.

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NOMENCLATURE

AM	Amplitude Modulation
BER	Bit Error Rate
BOM	Burst Mode Optical Receivers
CG	Common Gate
CD	Chromatic Dispersion
CDR	Clock and Data Recovery
CMA	Chained Multistage Amplifier
CMOS	Complementary Metal Oxide Silicon
DEMUX	Demultiplexer
GBP	Gain Bandwidth Product
GBP_1	Gain Bandwidth Product of one stage
GBP_T	Total Gain Bandwidth Product
HBT	Hetero junction-Bipolar Transistor
ILD	Injection-Laser Diode
ISI	Inter symbol interference
LA	Limiting Amplifier
LD	Laser Driver
LED	Light-Emitting Diode
MA	Multistage Amplifier
MUX	Multiplexer
OC	Optical Communications
OLT	Optical line Terminal
PD	Photo Detector
PDA	Personal Digital Assistants
PM	Phase Modulation
PMD	Polarization Mode Dispersion
PON	Passive Optical Network
RGC	Regulated Cascode
SDH	Synchronous Digital network

SERDES	serialization and deserialization
SNR	Signal to noise Ratio
SONET	Synchronous Optical Network
TIA	Transimpedance Amplifier
VCO	Voltage Controlled Oscillator
XAUI	Extent Attachment Unit Interface

CHAPTER I

INTRODUCTION

A Introduction and Motivation

The increasing demand for transferring higher volumes of data at higher speeds leads to the adoption of high speed wideband systems. High speed data cannot travel through copper (Cu) or over radio waves at fiber optic speeds [1]; besides, for wideband communications, signal-to-noise ratio (SNR) on copper (Cu) medium is insufficient, especially for large distances. Moreover, as speed increases the attenuation over Cu traces sharply increases, which causes signal loss and intersymbol interference (ISI) [2]. Fiber optical links can provide low attenuation at high speed and wideband communications for long-haul and short-haul systems without the electromagnetic interference from which coaxial and twisted pair cables suffer. Optical interconnections designed for low power consumption at high bit rates, offer an excellent means of overcoming data rate limitations imposed by conventional wiring between chips [1], [3]. Although networks of fiber-optic links have become a main stream for long-haul high speed communications, recent advances in laser diode output power combined with the global deployment of communications satellites and the need for more efficient communications have made free-space optics (or fiberless optics) very attractive.

Free-space optic links help fiber optic links in high traffic of data in short distance interconnections (<100m) such as cabinet level (1–100m), backplane level between boards (10cm–1m), chip to chip on a board (<10cm) and on-chip (<2cm) communications [3]. Demonstrations of high-bandwidth, long-range systems under realistic operating conditions further validate free-space optical communications, showing that it can provide high bandwidth,

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This dissertation follows the style of *IEEE Transactions on Circuits and Systems I.*

and secure inexpensive communications for a variety of applications [4]. Using infrared beams [5], free-space optical interconnections find applications in laptop computers, cellular phones, digital cameras, computer peripherals, personal digital assistants (PDAs), and many other consumer electronics equipment [4].

Further demand for fiber and free-space optical communications and generation of high-speed networks, such as gigabit Ethernet, has led to the need for more flexible, low-cost and high performance circuits. Although using GaAs or Si-bipolar technologies for very high bandwidth designs is dominant, cost-effective optical link consumer products require low-power dissipation and small silicon area CMOS receivers. Furthermore, high performance wideband circuits can be designed on baseline CMOS processes with heterojunction-bipolar-transistors (HBTs) [6]. Designs based on standard ("generic") CMOS process technology are the main incentive in the consumer applications market [7].

CMOS technologies have already been used for the standard receivers, especially for portable systems and consumer devices because of their low-cost, small size, low-power and highly integrated analog and digital circuits, still though, further designs are needed for less power consumption and area occupancy.

B Optical Communications Systems

An optical communications system is similar to the copper wire communications system in which fiber or free space replaces wire. Fig. 1-1 shows an optical communications system. At one end of the system there is a transmitter, where the digital data in different lines are combined by a multiplexer (MUX) in a single line. The digital signal is converted to electronic pulses to drive light-emitting diode (LED) or an injection-laser diode (ILD) to generate the light pulses. The light pulses are grouped into the fiber (or air), where they transmit themselves down the line [8]. The light bounces back and forth as it travels down the core in the fiber.

The attenuation of the light in fiber depends on several parameters, such as distance and wavelength of the light [8]. As the distance increases, the delivered power reduces. Several factors result in dispersion in transferring light waves in fiber links such as polarization mode dispersion (PMD) and chromatic dispersion (CD), which lead to intersymbol interference (ISI). In most free-space applications, the optical signal must be transmitted over long distances at high speed, and its signal level varies over a wide range due to fluctuations of attenuation in the atmosphere in different weather conditions [9]-[10] caused by fog, rain or snow.

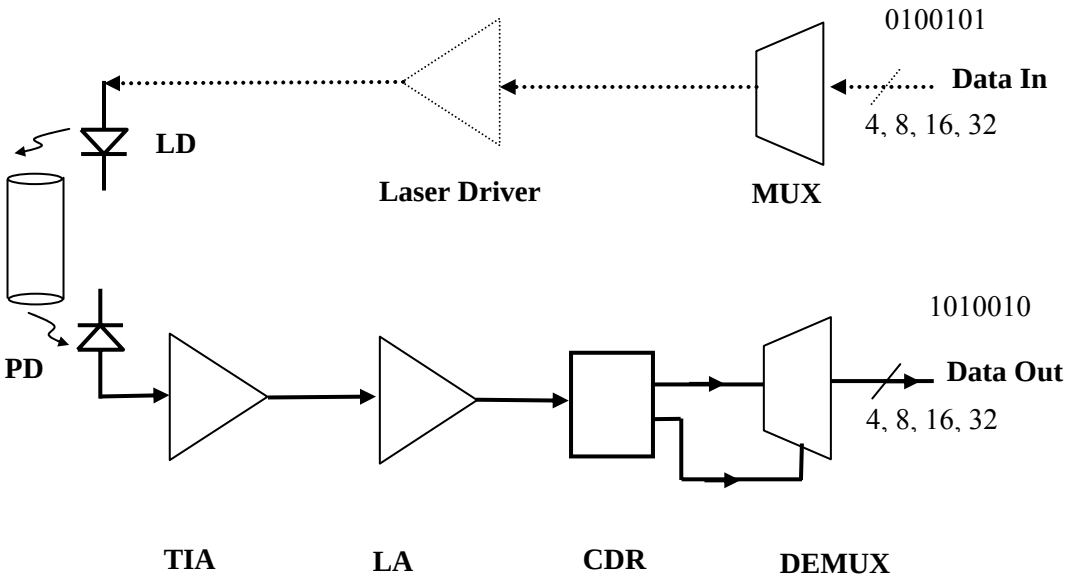


Fig. 1-1 An optical communications system

In Fig. 1-1 when the light leaves the fiber, a photo detector (PD) in a receiver converts the light into an electrical signal for processing. The power of the electrical signal depends on several parameters such as distance, power of transmitter and parameters of transferring light (fiber or air), and also the power reduction in the photo detector [11]. The electrical signal is further amplified by two amplifiers: TransImpedance Amplifier (TIA) or preamplifier and Limiting Amplifier (LA) or main amplifier. Then from the amplified signal, clock and data

recovery (CDR) circuit retimes data and extracts the clock [12]. Finally, demultiplexed digital data and clock in different lines (see Fig. 1-1) are sent to signal processing systems. Fiberless optic links work in the same way. For example, low-power infrared beams transmit digital data through the air. Transmission is done between transceivers that are mounted on rooftops or behind windows.

There are a couple of well-known standards for transmission of digital data in optical communications systems. One of them is Synchronous Optical Network (SONET) specified in ANSI T1.105 [13]. A similar standard, Synchronous Digital Hierarchy (SDH), has been also established in Europe by UTI-T. SONET and SDH are technically consistent standards. Besides using SONET for short distance optical communications, the standards of serialization/deserialization (SERDES) for range DC bit rate up to 3.7Gbits/S [14] and XAUI (an 8/10 bits 3.1247Gbits/S, an IEEE 802.3ae interface for chip to chip) [15] are very popular.

In the Burst-Mode Optical Receivers (BOM) (the IEEE 802.3ah PX10 and PX20 standards [16]), on point-to-multipoint optical network configuration with no active elements in the interconnection, a single fiber can be shared among multiple users [17]. The power of the injected light of each subscriber's transmitters is different. Thus, at the optical line terminal (OLT) of a passive optical network (PON), the time-division multiplexed optical signal from the users is a sequence of burst data packets with varying powers [18]-[19]. Therefore, in addition to high sensitivity [e.g. -28dBm], high overload [e.g. 0dBm] must be handled to support these variable power burst packets in a wide input dynamic range of the OLT receivers [18], [20]-[21].

C Optical Receiver

To clarify the operation of an optical receiver, a brief description of receiver components is presented here.

1. Transimpedance Amplifier (TIA) and Limiting Amplifier (LA)

As mentioned before, TIA's output voltage must be further amplified by a LA to reach the proper voltage swing necessary to drive the clock and data recovery (CDR) circuits. TIA must be sensitive enough to detect the weakest wideband signal (when receiver is far from transmitter). In other words, noise of TIA must be so low that the signal with a weak power can be amplified. Furthermore, when the power of the received signal is very high, the receiver must not be saturated and overloaded. So, the most challenging problem in TIA is to increase input dynamic range and extend bandwidth to reduce the jitter and distortion of the amplified signal [11].

The LA is a multistage amplifier with a high gain and a wide bandwidth with frequency response from DC range to several GHz. It provides the following decision circuit with uniform output level regardless of input swing level. Also, low phase shift deviation and small crossing point fluctuations must be insured over a wide input dynamic range to avoid degrading the sensitivity of the receiver system including the decision system [11]. The major challenges for the design of LA are to remove the DC offset (CMOS based circuits) with the minimum number of external components, to increase bandwidth and input voltage dynamic range.

To have a receiver with the capability to work at different bit rates and input powers, adjustable circuits are needed. This dissertation is proposing adjustable structures for TIA and LA and offers solutions to the challenges, mentioned in the previous paragraphs, that lead to performance enhancement of TIA and LA. Furthermore, an on chip circuit for DC offset cancellation circuit which employs a new capacitance multiplier is introduced.

2. Clock Data Recovery (CDR) Circuits

To extract data from the received distorted signals and synchronize them, a clock and data recovery (CDR) circuit is used. The CDR circuit has two main functions. First, it recovers the clock of data. Second, it transfers the synchronized data and the recovered clock to multiplexers

(see Fig. 1-1). CDR circuits have been implemented employing one or two loops. Each loop of a CDR circuit consists of a frequency and phase detector, a charge pump, a loop filter and a voltage controlled oscillator (VCO). A Two-loop CDR structure with external clock is shown in Fig. 1-2. One loop does phase-locking (loop I) and the other one does frequency-locking (loop II) [23].

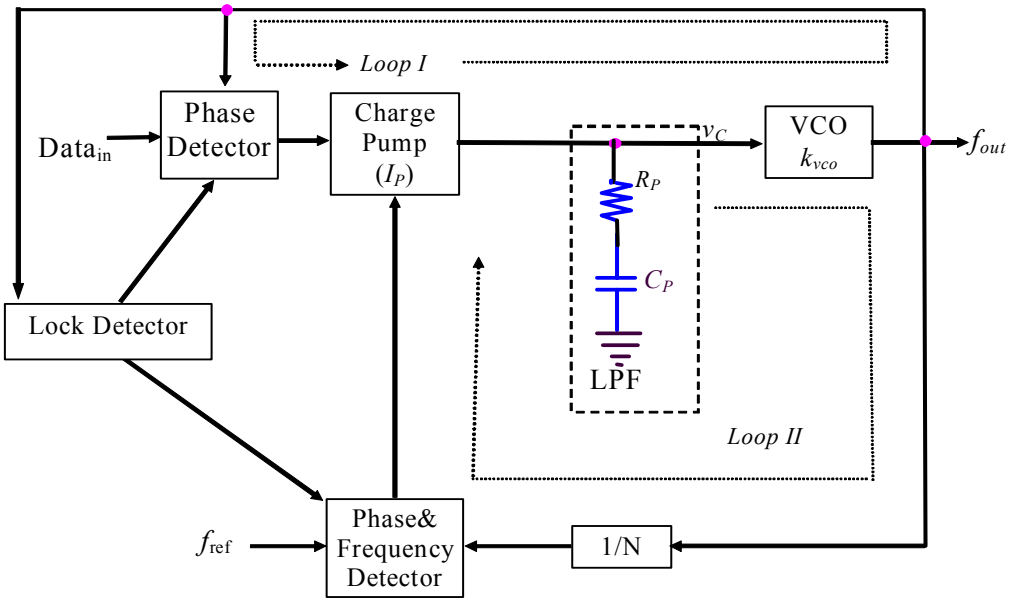


Fig. 1-2 A two-loop CDR architecture

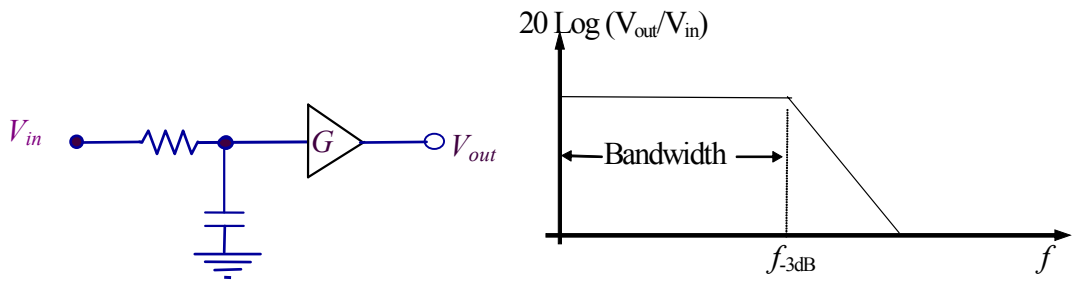
The lock detector monitors the difference between f_{out} and Nf_{ref} in the circuit in Fig. 1-2. It enables loop II and locks the oscillator to Nf_{ref}. When frequency error (the difference between f_{out} and Nf_{ref}) is small, it disables loop II and enables loop I. Since each loop has a different bandwidth and damping factor, low pass filter needs different values of capacitances and resistors (this will be described more in chapter V). It means the capacitors and resistors must be switched or tuned. This dissertation proposes to use a tunable loop filter in CDR circuits.

D General Concepts

To provide a better understanding of the goal of this dissertation, the following concepts are clarified:

1. Bandwidth

A wideband amplifier usually behaves as a low pass filter with some passband gain. The input signal is limited by amplifier's bandwidth as shown in Fig. 1-3. The frequency at which the voltage gain drops by -3dB in a wideband amplifier is referred to as bandwidth.



(a) (b)

Fig. 1-3 (a) The model of a wideband amplifier (b) Magnitude of the gain transfer function of a wideband amplifier

An amplifier with limited bandwidth prevents a high frequency signal from reaching the maximum amplitude and it does not let the voltage drop to its lowest level in a short time. This is shown in simulation results illustrated in Fig. 1-4. This figure shows an input voltage and the output voltage of a wide bandwidth amplifier. As seen, there is a delay time between the input voltage and the output voltage. Depending on the sequence of "0"s and "1"s, the delay time is different; furthermore, the output voltage swings between different peaks. For example, during 1.5746uSec to 1.5764uSec (see Fig. 1-4(b)) the output voltage could not reach the 300mV and -

300mV. This is because of the amplifier is slow and the time needed for the output voltage to reach the maximum and the minimum voltage is more than unity interval time (bit time).

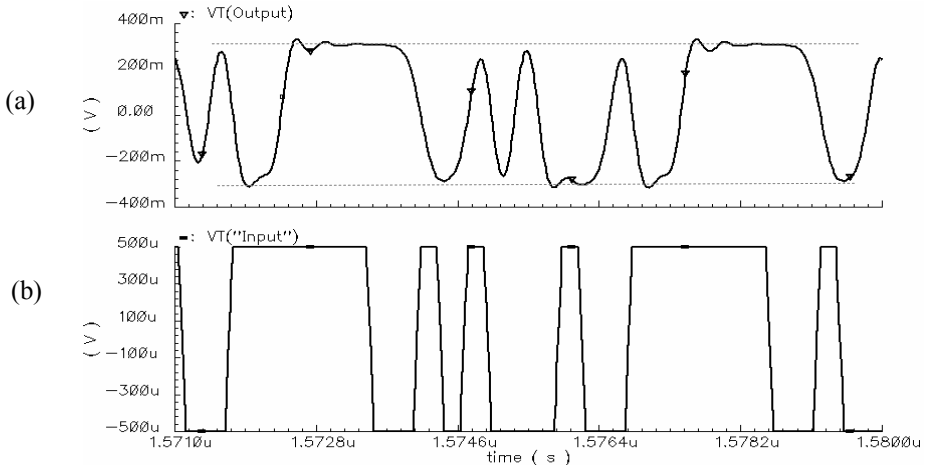


Fig 1-4 Amplifying a signal by an amplifier with a limited bandwidth (a) Output (b) Input

2. Eye Diagram

The performance of a high bit rate link can be measured from the eye diagram of the system [23]. The eye-pattern measurement is a time-domain measurement which is based on measuring signals in unity time interval (the bit time). An eye diagram simulation result is shown in Fig. 1-5. As explained for a limited bandwidth, signals cannot reach the peaks in the bit time. Furthermore, the transition times (rise and fall times) are slow and depending on the sequence of bits delay times are different. As a result the bits are overlapped and eye diagram of data would be closed. In CDR circuits, the horizontal opening gives a better sampling time interval for the received signal without error from intersymbol interference (ISI). Typically CDR circuit can tolerate higher than 50% horizontal closing [23]. The vertical height of eye opening is a measurement of the amplitude distortion of the signal. As the bandwidth is reduced, the vertical height of the eye's opening decreases and the eye closes [24]. In the digital gates of CDR

circuits, the vertical closing converts to horizontal closing and it increases the jitter in CDR circuits.

In characterization of the wideband amplifiers, small signal model behaviors are employed. But using AC response, obtained from small signal analysis, cannot be very accurate in the characterization of amplifiers with high swing signals; while, time domain measurements such as eye diagram measurements do not suffer from this shortcoming.

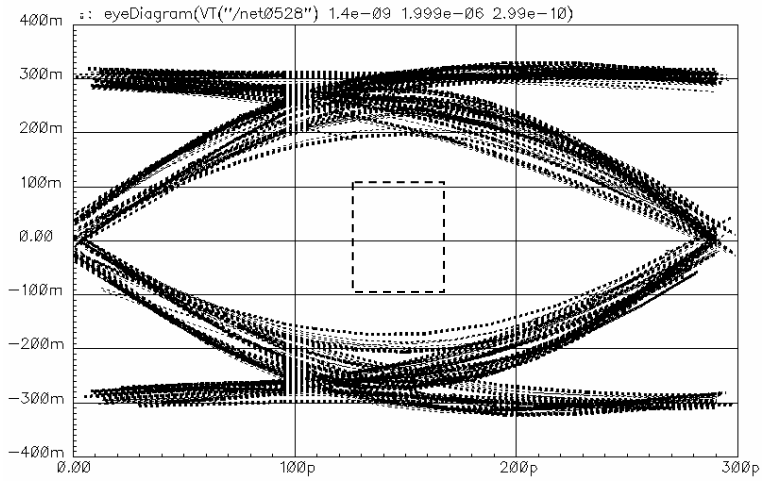


Fig. 1-5 Eye diagram

E Organization of Dissertation

Chapter I introduces briefly the optical communication systems with emphasis on receiver blocks. The concept and necessities of designing a TIA, and a new variable gain differential TIA are described in Chapter II. Chapter III discusses a simple design-oriented method used to design a multistage amplifier (MA) as a wideband amplifier. An introduction for the design of an LA will be presented. Also the concept of a new amplifier for LA, called chain multistage amplifier (CMA), is introduced. Design description and measurement results will be described further in

chapter IV. The design principles of the new capacitance multiplier and its usage in tunable loop filters of CDR circuits and the DC offset cancellation circuit in the main amplifier will be presented in chapter V. Measurement results of the capacitance multiplier will be discussed in the same chapter. Finally, summary of the results and suggestions for further studies and research are given.

CHAPTER II

TRANSIMPEDANCE AMPLIFIER

A Introduction

In a typical optical receiver, the combination of a photo detector and transimpedance amplifier is called "Front End of Optical Receiver". The overall performance of an optical receiver crucially depends on the transimpedance amplifiers (TIA) performance. For example, the receiver sensitivity is a strong function of the noise and the bandwidth of TIA. In addition to the wide bandwidth, the transimpedance amplifier requires high transimpedance gain in conjunction with low input referred noise for reliable operation at low photodiode input currents. High overload current imposes more jitter in a high transimpedance gain and requires higher power consumption. Therefore, design of high-sensitive, low-jitter, low-power, wide-band and wide input dynamic range TIAs forms a group of conflicting performance requirements that sets the TIA for a challenging CMOS design problem.

In recent years various CMOS transimpedance amplifier architectures have been reported that essentially explore various input stages for isolating the large input capacitance of the photodiode from bandwidth determination, such as common-source (CS) [25]-[26], common-gate (CG) [27], or common-drain (CD) [28] stage. Further bandwidth extension techniques in TIA, such as capacitive, inductive or transformer [29]-[30] peaking techniques [7], capacitive feedback [26] and using positive feedback to emulate a negative capacitance [31] have been adopted. A commonly used topology is the Regulated Cascode Transimpedance Amplifier (RGC TIA). Its relatively low input impedance, wide bandwidth and high stability have made it very attractive for wideband communications applications; however, low overload current is the most important drawback of this amplifier.

As discussed, a wide range of input current is possible especially for wireless and burst-mode optical receivers [16] in order to accommodate variable link distances. The combination of varying link lengths and channel losses (due to propagation through fiber or free space) requires wide input dynamic range of the preamplifier. However, finding a balance between dynamic range and power consumption requirements can be a challenge, since keeping bias currents small degrades the preamplifier's ability to handle large signals. To overcome overloading and nonlinearity, some designers have used transistor switching to adjust the feedback impedance [31]-[32]. Nonetheless, a flexible variable gain with a large gain dynamic range could not be easily implemented utilizing switching transistors in high frequency applications.

This chapter introduces a new architecture for a variable gain CMOS TIA. The proposed topology uses a modified regulated cascode (RGC) TIA stage to obtain an efficient, high-speed variable-gain TIA. The principle by way of gain, bandwidth, and input-referred noise analysis is developed in detail for this TIA. In addition, a fabricated prototype chip implementation of the proposed TIA using the low-cost TMSC 0.35μm CMOS process technology is reported.

B Circuit Design and Analysis

1. Parameters of TIA

The sensitivity of a TIA is the minimum input current which can be converted to voltage when the bit error rate (BER) is acceptable. The maximum tolerated noise can be calculated via the desirable BER of the application. The BER is given [23] by

$$BER = \frac{1}{2} erfc\left(\frac{Q}{\sqrt{2}}\right) = \frac{1}{Q\sqrt{2\pi}} \exp\left(\frac{Q^2}{\sqrt{2}}\right) \tag{2-1}$$

where

$$Q = \frac{I_{\min}}{I_{n,rms}} \tag{2-2}$$

I_{min} is the minimum input current and $I_{n,rms}$ is the *rms* (root of mean-square) of the input referred current noise ($\overline{i_{n,in}^{2}}$ is the spectral density of the input referred current noise) of TIA. The maximum noise of transimpedance amplifier can be obtained from BER and I_{min}. To have a specific bit error rate, noise must be less than what is calculated from equations 2-1 and 2-2 for the minimum current.

As the bandwidth is reduced, intersymbol interference increases, however, using a higher bandwidth collects more noise. Fig. 2-1 depicts sensitivity (detectable current) as a function of bandwidth.

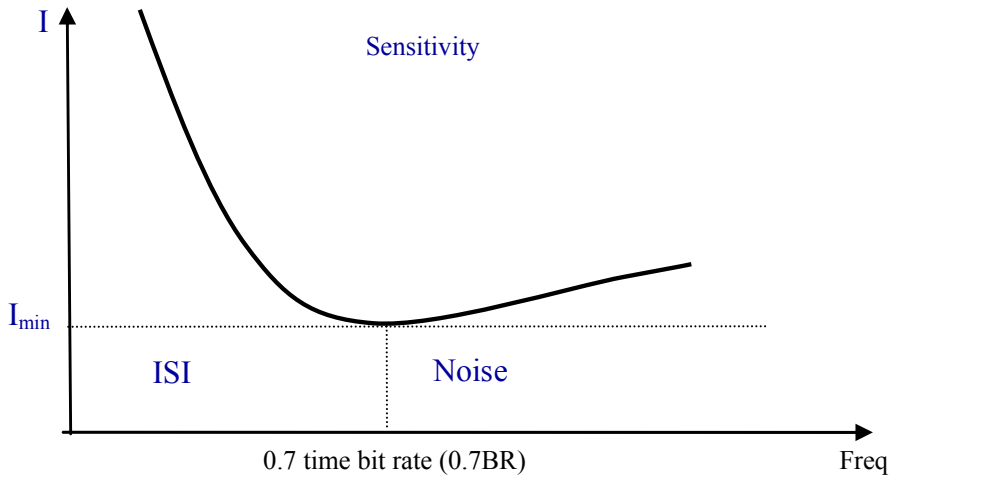


Fig. 2-1 Sensitivity of transimpedance amplifier, sensed current via bandwidth of transimpedance

In addition to TIA's noise, the shot noise of photo detector, which can be considerably big, depending on technology and implementation of the detector increases the minimum required light power in a receiver [24]. To reduce the total integrated noise, the bandwidth must be minimized. As explained, reducing the bandwidth introduces the intersymbol interference in random data and it closes the eye diagram both vertically and horizontally. There is a rule of thumb used for intuitively estimating the required bandwidth for a special bit rate. This is

obtained via modeling TIA as a first order transfer function with a slight amount of ISI while performance of TIA is still acceptable in practical applications. Based on this rule for an amplifier, the bandwidth must be approximately 0.7 times bit rate [23]. For example, for SONET OC-48 a bandwidth of 1.75GHz is recommended for TIA.

The third important parameter of a TIA is offering a high current to voltage conversion. Increasing transimpedance gain increases the chance of amplifying a weaker signal to a level detectable by the main amplifier; however, at a high photodiode input current a low gain is required. In SERDES (serialization and deserialization) [14] implementations, such an amplifier (TIA) has to work in a wide input current dynamic range from 100uA to 4mA [22], [33], and for OC-48 applications a 5uA to 0.5mA input current must be amplified.

C TIA's Circuit Design Principles

The received optical pulse signal is converted by a reverse-biased p-i-n photodiode (or other types of photodiodes such as *pn* and Avalanche [23] diode etc.) into an input electron–hole drift current (i_{in}) driving the input node of TIA. A typical lumped circuit model for a real p-i-n photodiode [30], [34]-[38] is illustrated in Fig. 2-2. In this dissertation for simulation, a simplified model consisting of a capacitance (C_{PD}=500*fF*) and current source (i_{PD}) is used and the other parasitic elements of photodiode are ignored.

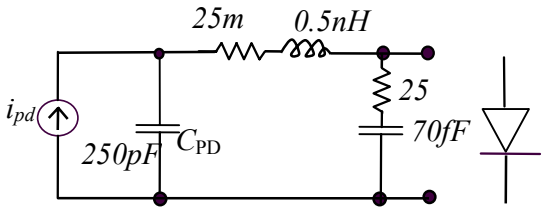


Fig. 2-2 Small signal model of photo detector

1. Common Gate TIA (CG TIA) with g_m-boosting Amplifier

The topology of the common gate (CG) transimpedance amplifier with g_m-boosting amplifier is shown in Fig. 2-3 (a). This type of TIA is also called regulated cascode (RGC) TIA. RGC TIAs were previously reported in [33]–[38]. The input node of CG TIA is the source node of the CG nMOS device (M_L). The -3dB bandwidth of the overall amplifier is determined by the low input impedance of the CG TIA and the high photodiode input capacitance (and hence, its poor intrinsic bandwidth). The energy of light converted to current i_{in} passes through transistor M_L and develops a voltage drop on resistor R_L. In Fig. 2-3 (b), a cascode amplifier is used as the boosting amplifier.

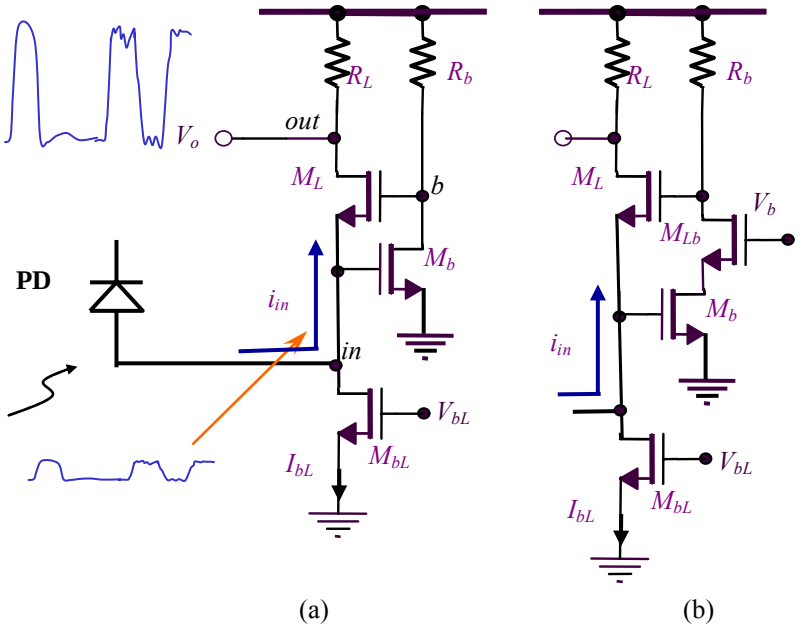


Fig. 2-3 Common gate (CG) transimpedance amplifier with g_m-boosting amplifier (a) simple amplifier (b) cascode amplifier

2. Bandwidth and Transimpedance Gain

Figure 2-4 illustrates a small signal model of CG TIA with g_m-boosting amplifier (illustrated in Fig. 2-3(a)). The equations for the current in nodes *in*, *out* and *b* can be written as

$$v_i = \left(\frac{1}{g_{dsbL} + sC_{in}}\right)\left\{i_{pd} + (v_b - v_i)\left[g_{mL} + s\left(C_{gsL} + C_{gdb}\right)\right]\right\} \tag{2-3}$$

$$v_O = \left(\frac{1}{g_L + sC_o}\right)\left[(-v_b + v_i)g_{mL} + (v_b - v_o)sC_{gdL}\right] \tag{2-4}$$

$$g_b v_b + v_i g_{mb} = (-v_b + v_i)s\left(C_{gsL} + C_{gdb}\right) + (-v_b + v_o)sC_{gdL} \tag{2-5}$$

The transimpedance can be approximated as

$$z_T(s) \approx \frac{g_{mL}\left(g_{mb}R_b + 1\right)}{\left[g_L + s\left(C_o + C_{gdL}\right)\right]\left\{\begin{array}{l}\left[g_{dsbL} + g_{mL} + s\left(C_{in} + C_{gsL} + C_{gdb}\right)\right]\left[1 + sR_b\left(C_{gdL} + C_{gsL} + C_{gdb}\right)\right] \\ + \left[g_{mL} + s\left(C_{gsL} + C_{gdb}\right)\right]\left[R_b g_{mb} - sR_b\left(C_{gsL} + C_{gdb}\right)\right]\end{array}\right\}} \tag{2-6}$$

Equation 2-6 can be simplified as

$$z_T(s) \approx \frac{g_{mL}\left(1 + g_{mb}R_b\right)}{\left[g_L + s\left(C_o + C_{gdL}\right)\right]\left\{g_{dsbL} + g_{mL}\left(1 + g_{mb}R_b\right) + s\left[C_{in} + \left(1 + g_{mL}R_b\right)\left(C_{gsL} + C_{gdb}\right)\right]\right\}} \tag{2-7}$$

where g_{mL} and g_{mb}, are transconductance of M_L and M_b; C_{gdb} and C_{gdL} are gate-to-drain capacitances of M_L and M_b, respectively. Also C_{gsL} is the gate-source capacitance of M_L and $g_L=1/R_L$. C_{in} is contributed from photodiode capacitance, capacitances of gate-source of M_b, source-substrate junction of M_L and drain-substrate junction of M_{bL} (If the photo detector is an external chip component, the pad and ESD protection capacitance would be added to C_{in}.). The low frequency transimpedance gain (called midband gain) of the amplifier is

$$z_T(s)\big|_{s=0} \approx R_L \tag{2-8}$$

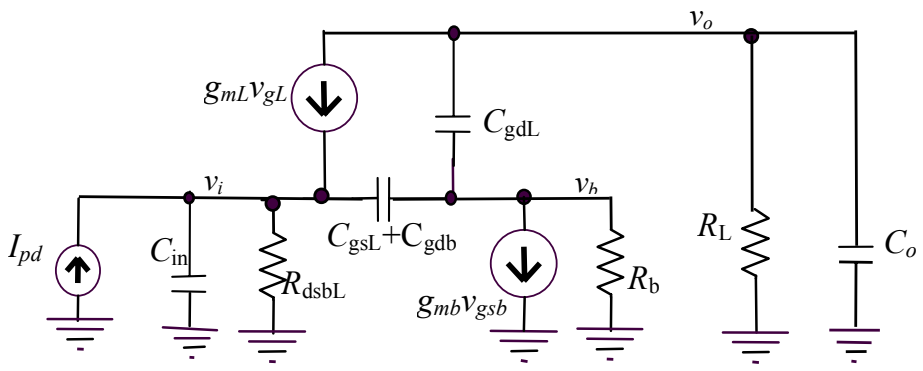


Fig. 2-4 Small signal model of common gate (CG) transimpedance amplifier

The dominant pole of the transimpedance gain can be given as

$$p_1 \approx \frac{g_{mL}\left(1+g_{mb}R_b\right)}{C_{in}+\left(1+g_{mL}R_b\right)\left(C_{gsL}+C_{gdb}\right)} \tag{2-9}$$

For a practical case, the second term of the denominator of Eq. (2-6) can be ignored. Then the dominant pole can be approximated as

$$p_1 \approx \frac{g_{mL}\left(1+g_{mb}R_b\right)}{C_{in}} \tag{2-10}$$

The dominant pole of CG TIA is $p_d = g_{mL}/sC_{in}$. That means using g_m-boosting amplifier can expand the bandwidth $\left(1+g_{mb}R_b\right)$ times that of the regular CG TIA. Equation 2-10 shows that using booster expands the bandwidth, when C_{in} (the equivalent of the capacitance in input of TIA) is comparable or bigger than $\left(1+g_{mL}R_b\right)\left(C_{gsL}+C_{gdb}\right)$. The DC input impedance can be calculated from

$$z_{in}\big|_{s=0} \approx \frac{1}{g_{mL}\left(1+g_{mb}R_b\right)} \tag{2-11}$$

To match the input impedance with low resistivity impedance (like 50 Ohms transmission lines), the gain of boosting amplifier can be adjusted. Increasing the current of bias of the transistor M_L

and using a bigger transistor (M_L) would somewhat help to reduce input impedance. Also using cascode amplifier as shown Fig. 2-3 (b) would help to reduce input capacitance and to increase boosting gain that helps to lower input impedances.

To have a higher transimpedance gain, a bigger R_L must be used. This shifts the pole (in equation 2-7) related to output node to lower frequencies and even makes it closer to the dominant pole. Therefore, it degrades the phase of the transimpedance gain in frequencies around corner frequency. For a limited power supply, to keep transistor M_L in saturation region when using a big R_L, bias current of M_L (I_L) must be reduced. On the other hand, decreasing I_L reduces g_{mL} and shifts the dominant pole to lower frequencies. Thus, that mandates a tradeoff between transimpedance gain and bandwidth.

3. Noise

The theoretical analysis of the input current referred noise spectral density of the transimpedance amplifier is discussed next. As it was explained, the minimum detectable signal depends on the noise produced by TIA and photo detector. Since, the low frequency signals are filtered after TIA, flicker noise can be ignored in the noise characterization. Thermal noise is the most important noise determines the sensitivity of TIA. Fig. 2-6 depicts a circuitry for modeling the noise in CG TIA with g_m-boosting amplifier

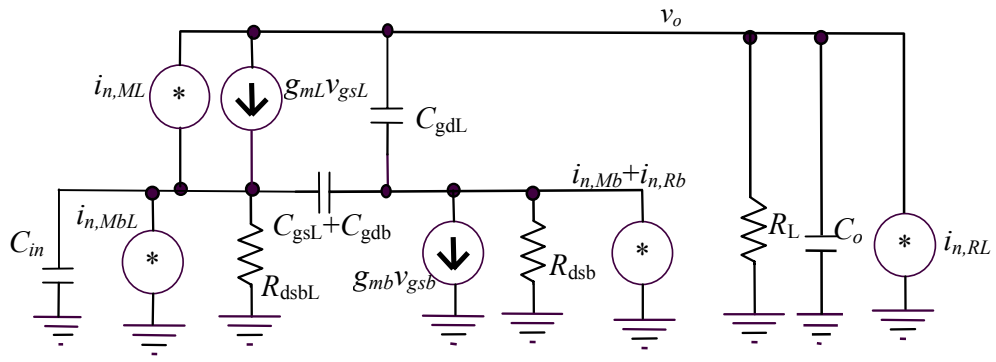


Fig. 2-5 A scheme for modeling the noise model of CG TIA with g_m-boosting amplifier

The spectral density of the equivalent input current referred noise of CG TIA with g_m-boosting amplifier can be calculated [36]-[37] as

$$\overline{i_{n,in}^{\,2}} = \overline{i_{n,R_L}^{\,2}} + \overline{i_{n,M_{bL}}^{\,2}} + \left(\overline{i_{n,M_L}^{\,2}} + \overline{i_{n,R_L}^{\,2}}\right)\omega^2\left[\frac{C_{in}+\left(C_{gsL}+C_{gdb}\right)\left(1+g_{mL}R_b\right)}{g_{mL}\left(g_{mb}R_b+1\right)}\right]^2 + \left(\overline{i_{n,R_b}^{\,2}} + \overline{i_{n,M_b}^{\,2}}\right)\omega^2\left(\frac{R_bC_{in}}{g_{mb}R_b+1}\right)^2 \tag{2-12}$$

where $\overline{i_{n,R_L}}$ and $\overline{i_{n,R_b}}$ are the thermal noise of R_L and R_b and $\overline{i_{n,M_L}}$, $\overline{i_{n,M_{bL}}}$ and $\overline{i_{n,M_b}}$ are the channel thermal noise of M_L, M_{bL} and M_b, respectively. The thermal noise of the gate poly resistance and the bulk resistance are negligible in typical applications since they are not considered. Assuming transistors M_L, M_b and M_{bL} are in strong inversion. The equation 2-12 can be approximated as

$$\overline{i_{n,in}^{\,2}} = \frac{4kT}{R_L} + 4kT\gamma g_{mbL} + 4kT\omega^2\left(\gamma g_{mL}+\frac{1}{R_L}\right)\left[\frac{C_{in}+\left(C_{gsL}+C_{gdb}\right)\left(1+g_{mL}R_b\right)}{g_{mL}\left(g_{mb}R_b+1\right)}\right]^2 + 4kT\left(\gamma g_{mb}+\frac{1}{R_b}\right)\left[\omega^2\left(\frac{C_{in}R_b}{g_{mb}R_b+1}\right)^2\right] \tag{2-13}$$

where K is the Boltzman's constant, T is the absolute temperature, and γ is the body effect factor [39]-[40]. If the integrated noise is calculated from equation 2-13 in whole bandwidth of TIA, the contribution of the noises of the thermal noise of R_{L} and of the channel thermal noise of M_{L} are more significant than the other terms. The noise of g_m-boosting amplifier (see Eq. (2-13)) gets bigger at higher frequencies.

A bigger R_L contributes less thermal noise but it increases the voltage drop across R_L and reduces the overdrive voltage required for the stage after TIA. Furthermore, it limits the maximum input current and I_L, which is the bias current of M_{L} in Fig. 2-3 (a). I_L must be set such that for the lowest peak and the highest peak of the photo detector's current passing through the M_L it stays in saturation region. Pushing the M_L to triode and sub threshold region degrades speed, increases jitter and closes the eye diagram of data pattern [23]. The width of the input device M_{L} is optimized considering the mutually conflicting requirements of low input referred noise current and low input impedance [7], [41]. A minimum bias current and the smallest size of transistor for M_{bL} must be employed to reduce g_{mbL}, as a result, it reduces noise.

To meet the standard requirements, the sensitivity of TIA must be increased. So, I_L must be reduced and R_L must be enlarged. On the other hand, the requirements for overload protection of the TIA due to a high current produced in photo detector enforce us to use a bigger I_L. There is a conflict between requirements of these two parameters of TIA; the smallest detectable signal and the biggest detectable signal.

D The Proposed TIA

1. Differential Ended CG TIA

To protect TIA from substrate noise and power supply noise, differential structures are employed that give differential outputs. Depending on the application and the type of photo detector (e.g. a laser detector such as avalanche photo detector, or Infrared detector [17], [37]), the differential

TIA can be used in two configurations. First, one side of the photo detector is connected to a bias voltage and the other side is connected to TIA. In this case TIA has an input current as shown in Fig. 2-6. The g_m-boosting amplifier is the differential amplifier expands the bandwidth. The second configuration is to use fully differential TIA in which the two ends of the photo diode will be connected to TIA.

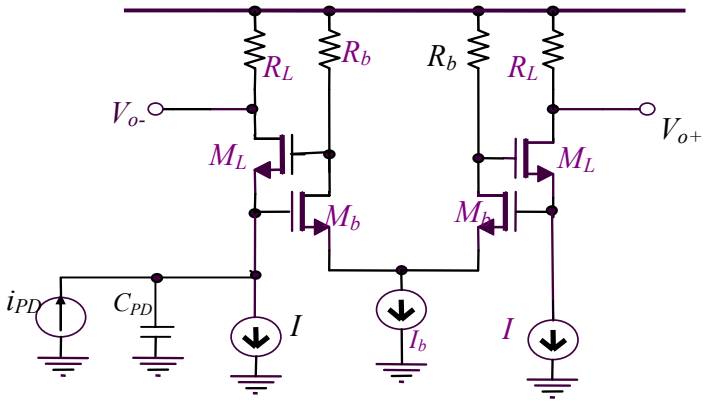


Fig. 2-6 Single input differential ended CG TIA

The transimpedance gain of the proposed TIA in Fig. 2-6 can be approximated as

$$z_T(s) \approx \frac{g_{mL}\left\{\left(\frac{g_{mb}}{2}R_b+1\right)g_b+\frac{g_{mb}}{2}+s\left(\frac{g_{mb}}{2}R_b+1\right)\left(C_{gdL}+2C_{gsL}+2C_{gdb}\right)\right\}}{\left[g_L+s\left(C_o+C_{gdL}\right)\right]\left\{\left(2\frac{g_{mb}}{2}+g_b\right)\left[g_{mL}+s\left(C_{gsL}+C_{gdb}\right)\right]+sC_{in}\left(\frac{g_{mb}}{2}+g_b\right)\right\}} \tag{2-14}$$

The low frequency transimpedance gain can be calculated as

$$z_T(s)\big|_{s=0} \approx R_L \tag{2-15}$$

The dominant pole and zero can be given as

$$p_1 \approx \frac{\left(2\frac{g_{mb}}{2}+g_b\right)g_{mL}}{\left(2\frac{g_{mb}}{2}+g_b\right)\left(C_{gsL}+C_{gdb}\right)+C_{in}\left(\frac{g_{mb}}{2}+g_b\right)} \tag{2-16}$$

$$z_1 \approx \frac{2\frac{g_{mb}}{2} + g_b}{\left(\frac{g_{mb}}{2} R_b + 1\right)\left(C_{gdL} + 2C_{gsL} + 2C_{gdb}\right)} \tag{2-17}$$

Although p_1 in equation 2-16 is less than two times the value of the dominant pole of CG TIA and it can be lower than the value of the dominant pole of the regular RGC TIA (calculated in Equation 2-9), p_1 can be compensated by z_1 when

$$g_{mL} R_b \geq \frac{2\left(C_{gsL} + C_{gdb}\right) + C_{in}}{\left(C_{gdL} + 2C_{gsL} + 2C_{gdb}\right)} \tag{2-18}$$

$g_{mL}R_b$ can be set as

$$g_{mL} R_b \approx 1 + \frac{C_{in}}{2\left(C_{gsL} + C_{gdb}\right)} \tag{2-19}$$

In this case the transimpedance gain can be approximated as:

$$z_T(s) \approx \frac{1}{g_L + s\left(C_o + C_{gdL}\right)} \tag{2-20}$$

An advantage of the circuit in Fig. 2-6 (as equation 2-20 depicts) is that the transimpedance gain can be independent of photodiode capacitance and the input capacitance of TIA. Furthermore, I_L does not affect the bandwidth directly as it does in a regular RGC TIA. For this TIA, the input resistance is higher than that of RGC TIA. The DC input impedance can be calculated from

$$z_{in}\big|_{s=0} > \frac{1}{2g_{mL}} \tag{2-21}$$

The input referred noise can be approximated as

$$\overline{i_{n,in}^2} \approx 2\overline{i_{n,R_L}^2} + 2\overline{i_{n,M_{bL}}^2} + \left(\overline{i_{n,M_L}^2} + \overline{i_{n,R_L}^2}\right)\omega^2\left(\frac{C_{in}}{2g_{mL}}\right)^2 + \left(\overline{i_{n,R_b}^2} + \overline{i_{n,M_b}^2}\right)\omega^2\left(\frac{R_b C_{in}}{2}\right)^2 \tag{2-22}$$

Noise is worse than that of the regular RGC TIA but it can have a wider bandwidth and it has differential outputs.

The differential ended TIA in Fig. 2-6 was designed and simulated in a CMOS 0.35μm technology for a power supply 3.3V while C_{PD}=0.5pF. TIA was connected to a buffer to drive 50Ω and 2pF capacitances. For R_L=1$k\Omega$ and I_L=1mA a midband gain of 60dB and the bandwidth of more than 2.6GHz were obtained. Figure 2-7 illustrates the magnitude of transimpedance gain. A random pattern from 16000 bits was used for eye diagram measurement while i_{in}(peak-to-peak)=200μA and bit rate was 4Gbits/s. The eye diagram is depicted in Fig. 2-8. In this simulation when i_{in}(peak-to-peak) is increased to 1mA, TIA converts i_{in} to a suitable voltage without intersymbol interference as shown in Figure 2-9 (a) for 2.5 Gbits/S. As i_{in}(peak-to-peak) is increased to 2.5mA, eye diagram is closed completely. The integrated input referred noise is 487nA. Figure 2-9 (b) illustrates the eye diagram.

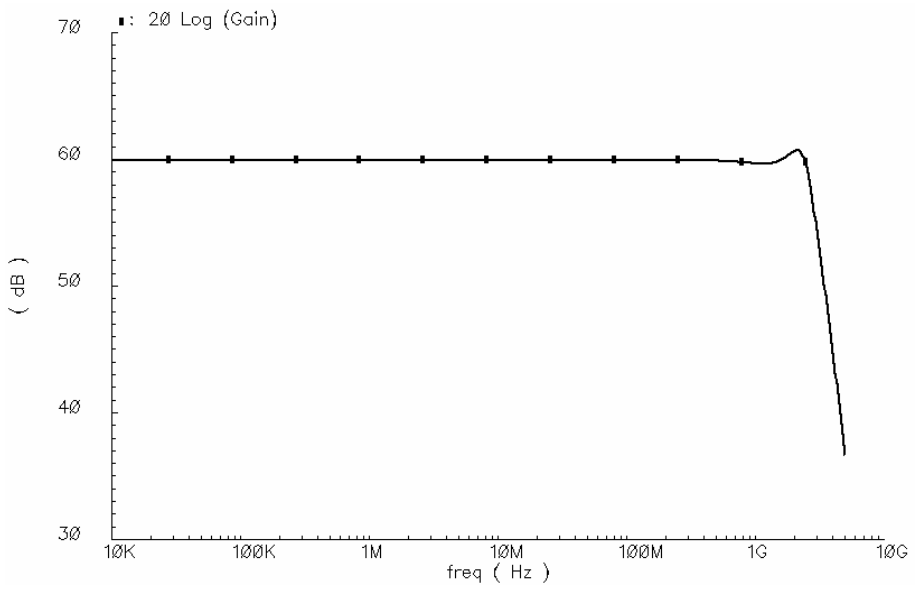


Fig. 2-7 Magnitude of transimpedance gain of single input differential ended RGC TIA.

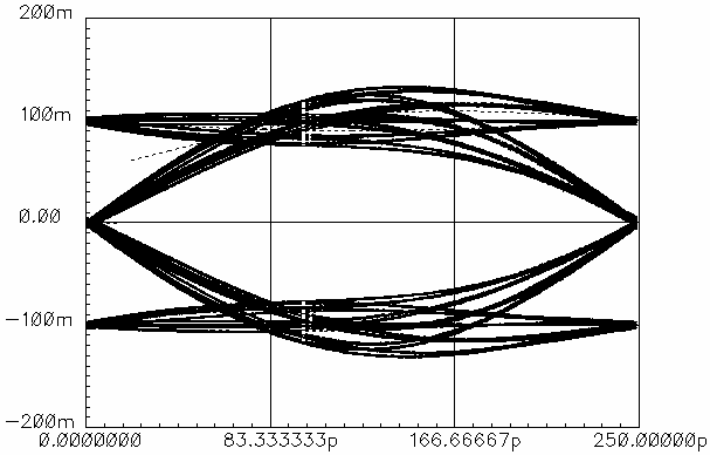
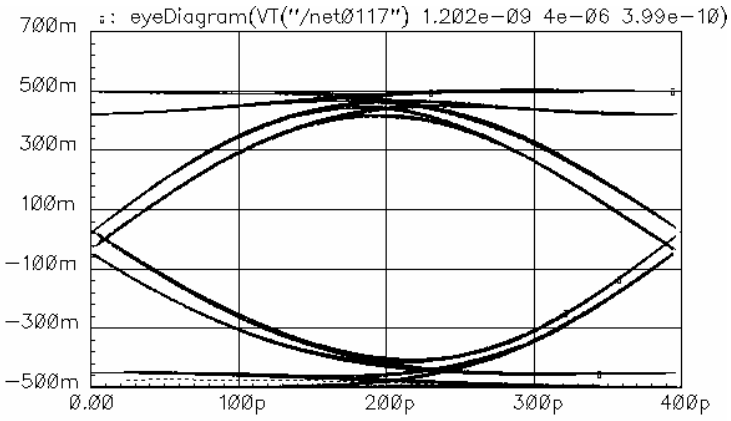


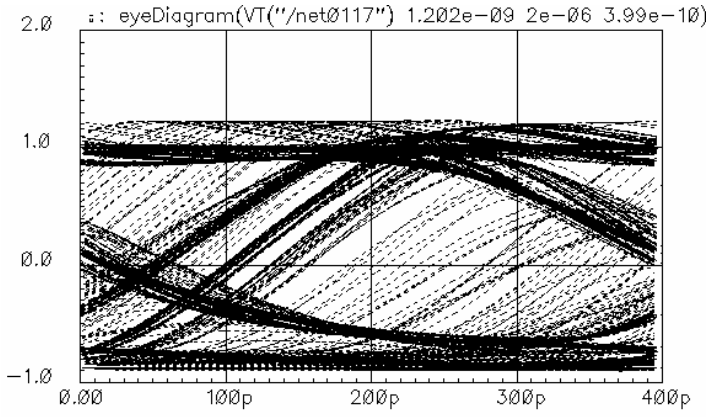
Fig. 2-8 Eye diagram at 200uA and 4Gbits/s for 16000 random bits of single input differential ended RGC TIA for a C_{PD}=0.5pF

The fully differential RGC TIA can be used as illustrated in Fig. 2-10. The differential input current is converted to differential output voltage. The transimpedance gain can be approximated to twice the value of $z_T(s)$ in equation 2-7. The photo detector's capacitance, which is placed between two input nodes, doubles the equivalent capacitance seen of each input of TIA.

As shown before, TIA with high input current is overloaded (that limits the usage of this TIA in the application with high power light). To avoid the overloading, the gain must be reduced; furthermore, the bias current of M_L must be increased to have a linear TIA.



(a)



(b)

Fig. 2-9 Eye diagram for 2.5Gbits/s (for 10000 random bits) of single input differential ended RGC TIA (a) at 0.5mA (b) at 2.5mA.

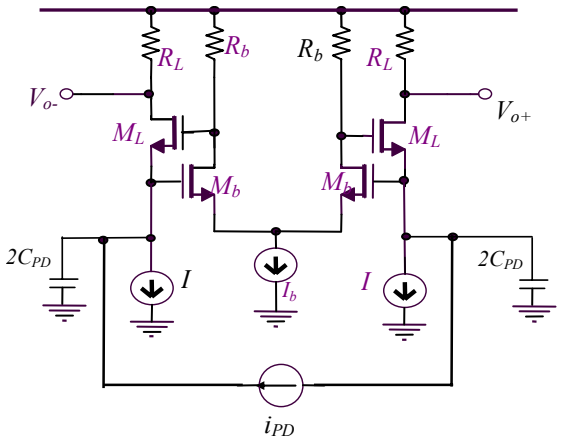


Fig. 2-10 Fully differential RGC TIA

E The Proposed Variable Gain TIA

Fig. 2-11 (a) depicts the CG TIA's operation at a low input current. The input transistor (see M_L in Fig. 2-3) is operating in saturation region and the output swing is small; therefore, TIA is operating linearly. But in Fig. 2-11 (b) due to a high input swing current, the output voltage swing (v_O) is so high that it presses the voltage drop on the nodes of drain and source of the input transistor so it is pushed to triode region or subthreshold. As a result, the performance of the circuit is degraded. The proposed operating scheme of the TIA is illustrated in Fig. 2-11 (c). To avoid high swing voltage at output node, a feed forward current produced by a current controlled current source (CCCS) drops the current from i_{in} to i_{in}–i_v so a small output swing voltage is obtained. In other words, linearity operation of the main transistor is performed and the TIA is protected from overloading.

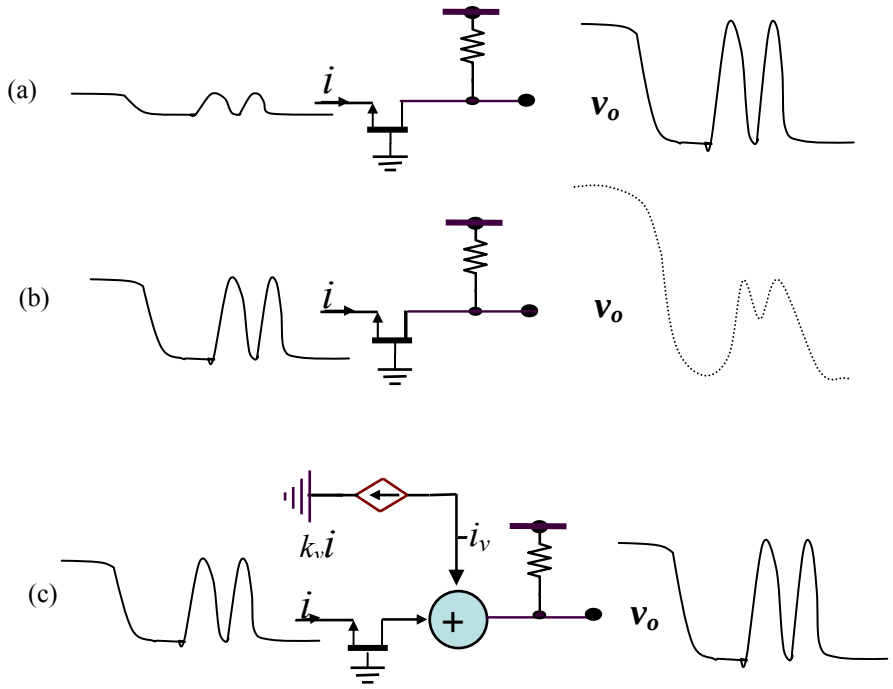


Fig. 2-11 Scheme of CG TIA (a) the conventional CG TIA when the input current is low (b) the conventional CG TIA when the input current is high (c) the proposed TIA when the input current is high and low

In Fig. 2-11(c) $i_v=k_v i_{in}$ and $v_o=R_L(1-k_v)i_{in}$; thus, the transimpedance gain is reduced from R_L to $R_L(1-k_v)$. Changing k_v varies the transimpedance gain.

1. The Variable Gain TIA Circuit

The topology of the proposed variable gain TIA is shown in Fig. 2-12. It incorporates three main stages: (1) a RGC TIA stage, (2) a variable gain controller, consisting of an operational transconductance amplifier (OTA) to control transimpedance gain and (3) a loop to control the gain of OTA. The gain controlling loop is comprised of a peak detector, a comparator and an integrator. The input current of the RGC TIA stage passes through the transistor M_L and it is combined with a negative feed forward current (i_v). The OTA generates the negative current by

sensing v_b. In the gain controlling loop, the comparator compares the peak of the output signal with a reference (V_{ref}) and leads the integrator to define the bias of OTA. If the peak of the signal is higher than the reference, I_V must be increased; otherwise, it must be reduced.

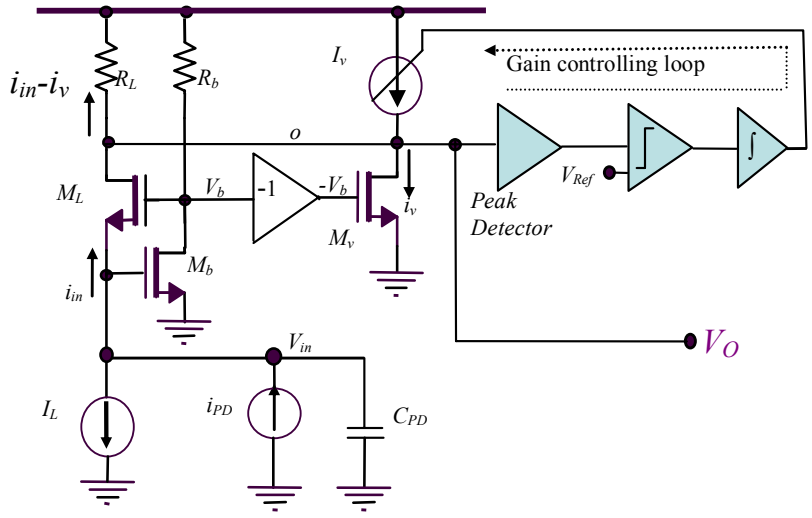


Fig. 2-12 Variable gain RGC TIA with gain controlling loop

The integrator keeps increasing and reducing I_V for the possible maximum number of sequential low ("0") bits. Fig. 2-12 depicts that $-v_b$ is converted to a current (i_v) by the OTA. If the input current increases slightly, voltage of input node (v_{in}) will pull up; consequently, v_b (at phase shift) will drop down and i_v increases and a lower voltage swing at the output node is produced.

2. Fully Differential Variable Gain RGC TIA Circuit

The variable gain RGC TIA can be implemented as a fully differential variable-gain TIA as illustrated in Fig. 2-13.

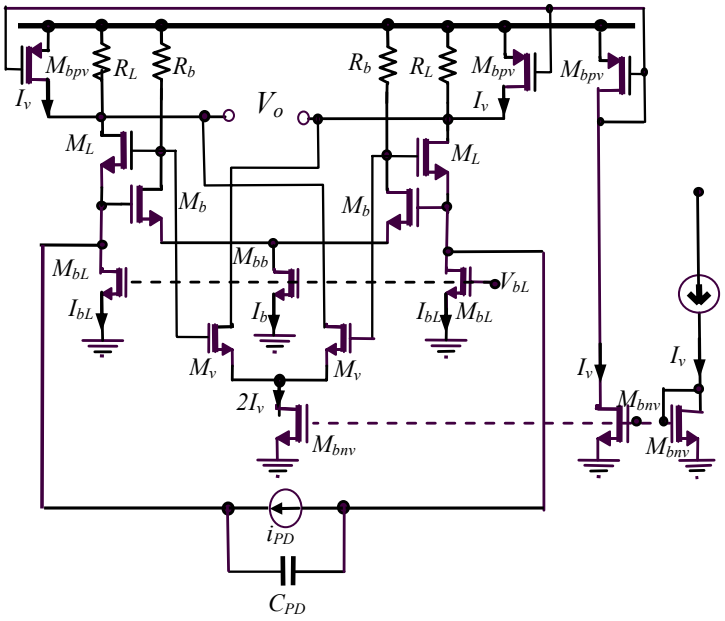


Fig. 2-13 Circuit of the fully differential variable gain RGC TIA

In Fig. 2-13 paired transistors M_v, M_{bpv} and M_{bnv} compose the OTA. Although the Miller effect of C_{pd} (photodiode capacitance) in fully differential TIA degrades the bandwidth further, it can be compensated for by using capacitance neutralization [23]. Fig. 2-14 shows the small signal model of the fully differential variable gain RGC TIA. This circuit can be used to describe the transimpedance gain of the variable gain RGC TIA.

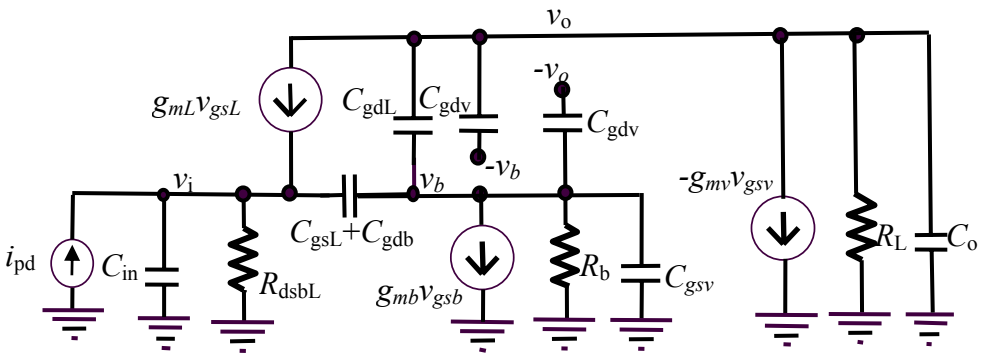


Fig. 2-14 A small signal model of the fully variable gain RGC TIA

The transimpedance gain of TIA in Fig. 2-13 can be given as

$$z_T(s) = \frac{A(s)}{B(s)} \tag{2-23}$$

where

$$A(s) = 2g_{mL}\left[g_{mb}R_b + 1 + s\left(C_{gdL} + C_{gdv} + C_{gsv}\right)R_b\right] - 2g_{mv}\left[g_{mb}R_b - s\left(C_{gsL} + C_{gdb}\right)R_b\right] \text{ , } \tag{2-24}$$

and

$$\begin{aligned} B(s) = {} & \left[g_L + s\left(C_o + C_{gdL} + C_{gdv}\right)\right]\times \\ & \left\{\begin{array}{l}\left[g_{dsbL} + g_{mL} + s\left(C_{in} + C_{gsL} + C_{gdb}\right)\right]\left[1 + s\left(C_{gsL} + C_{gdb} + C_{gdL} + C_{gdv} + C_{gsv}\right)R_b\right] \\ + \left[g_{mL} + s\left(C_{gsL} + C_{gdb}\right)\right]\left[g_{mb}R_b - s\left(C_{gsL} + C_{gdb}\right)R_b\right]\end{array}\right\} \end{aligned} \tag{2-25}$$

In equations (2-24) and (2-25) g_{mv} is the transconductance and C_{gdv} and C_{gsv} are the gate-drain and the gain-source capacitances of M_v, respectively. The zero frequency can be written as:

$$z_1 \approx \frac{g_{mb}\left(g_{mL} - g_{mv}\right) + g_b g_{mL}}{g_{mL}\left(C_{gdL} + C_{gdv} + C_{gsv}\right) + g_{mv}\left(C_{gsL} + C_{gdb}\right)} \tag{2-26}$$

As g_{mv} is increased, the denominator in equation (2-26) is also increased and the numerator is reduced. This shifts z_1 to lower frequencies and expands the bandwidth. The dominant pole frequency can be approximated as:

$$p_1 \approx \frac{g_{dsbL} + g_{mL} + g_{mb}R_b g_{mL}}{\left(C_{gdL} + C_{gdv} + C_{gsv}\right)g_{mL}R_b + \left(C_{gsL} + C_{gdb}\right)\left(g_{mL}R_b + 1\right) + C_{in}} \tag{2-27}$$

Although, as expected, the additional components shift the dominant pole and the second pole (which is corresponding to parasitic components at the output node) to lower frequencies, the zero frequency can expand the bandwidth significantly, especially when g_{mv} is increased. In general, the dominant pole for g_{mv}=0 is approximately equal to that of the regular RGC TIA. The input impedance of each input node is

$$z_{in}(s)=\left[g_L+s\left(C_o+C_{gdL}+C_{gdv}\right)\right]\frac{1+s\left(C_{gsL}+C_{gdb}+C_{gdL}+C_{gdv}+C_{gsv}\right)R_b}{B(s)} \tag{2-28}$$

The input impedance of the variable gain RGC TIA similar to that of the regular RGC TIA is decreased by $(1/(1+g_{mb}R_b))$. For each input node it is about the input impedance of the single ended RGC TIA.

The input referred current noise spectrum density of the fully differential variable gain TIA can be approximated as

$$\begin{aligned}\overline{i_{n,in}^{\,2}} &= 2\overline{i_{n,R_L}^{\,2}}+2\overline{i_{n,M_{bL}}^{\,2}}+2\left(\overline{i_{n,M_L}^{\,2}}+\overline{i_{n,R_L}^{\,2}}+\overline{i_{n,M_v}^{\,2}}\right)\omega^2\left[\frac{C_{in}+\left(C_{gsL}+C_{gdb}\right)\left(1+g_{mL}R_b\right)}{g_{mL}\left(g_{mb}R_b+1\right)}\right]^2 \\ &+2\overline{i_{n,M_v}^{\,2}}+2\left(\overline{i_{n,R_b}^{\,2}}+\overline{i_{n,M_b}^{\,2}}\right)\omega^2\left(\frac{C_{in}R_b}{g_{mb}R_b+1}\right)^2\end{aligned} \tag{2-29}$$

where $\overline{i_{n,M_v}}$ is the channel thermal noise of M_v. For I_v=0, the input referred current noise is twice that of a regular RGC TIA, that is a drawback of the topology of the proposed TIA. This is not just specific to this TIA. Fully differential TIA always adds twice as much noise to the input current compared to the single input TIA. Since a variable gain is available, a bigger R_L can be employed. Adopting a bigger R_L gives a chance to lower I_L and reduces the noise further; however, a bigger R_L shifts the second pole to lower frequencies. The low frequency transimpedance gain of the fully differential RGC TIA can be calculated from

$$z_T\left(s=0\right)\approx 2R_L\left[1-\frac{g_{mv}\left(g_{mb}R_b\right)}{g_{mL}\left(1+g_{mb}R_b\right)}\right] \tag{2-30}$$

When g_{mv} is zero, the DC gain is $2R_L$, which is twice that of a regular RGC TIA. Increasing g_{mv} in equation (2-30) reduces the transimpedance gain of TIA. So it is easy to change the bias current of transistor M_v to adjust the transimpedance gain of the TIA.

Assuming that the lengths of transistors M_v and M_L are the same, the low frequency transimpedance gain can be calculated from equation (2-31) as

$$z_T(s)\big|_{s=0} = 2R_L\left(1-\frac{b}{1+b}\sqrt{\frac{W_v}{W_L}\frac{I_v}{I_L}}\right) \tag{2-31}$$

where b is DC gain of the g_m-boosting amplifier ($b=g_mR_b$), and W_v and W_L are the widths of transistors M_v and M_L, respectively. Changing the ratio of two currents I_v and I_L varies the transimpedance gain.

F Implemented Circuit

The implemented circuit of the fully differential variable gain RGC TIA illustrated in Fig. 2-15 in a CMOS 0.35μm technology (f_T≈14GHz) for a power supply 3.3V was implemented. Where C_{PD}=0.5pF, it was connected to a buffer to drive the paralleled 50Ω resistances and 2pF capacitances. The bias current of M_L (I_L) is increased in such a way that for a high input current swing the bias current ($I_L=I_{bL}+0.5I_v$) would be enough to keep M_L in the saturation region. In the implemented circuit the lengths of transistors M_v and M_L are the same; therefore, the midband transimpedance gain can be calculated from

$$z_T(s)\big|_{s=0} = 2R_L\left(1-\frac{g_{mb}R_b}{1+g_{mb}R_b}\sqrt{\frac{0.5W_v}{W_L\left(\frac{I_{bL}}{I_v}+0.5\right)}}\right) \tag{2-32}$$

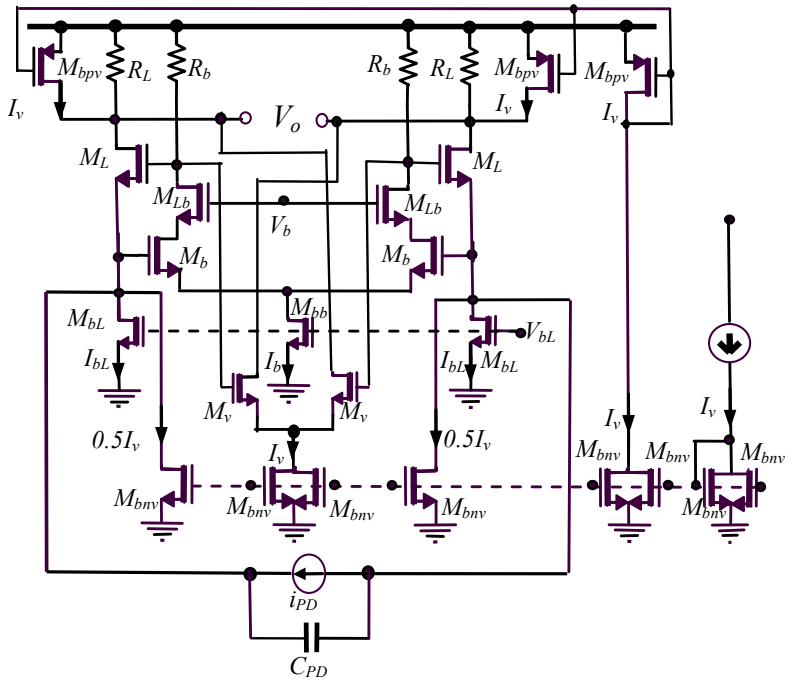


Fig. 2-15 Implemented fully differential variable gain RGC TIA

where W_v and W_L are the widths of the transistors M_v and M_L, respectively. For W_v =2W_L, R_L=1.5kΩ and I_{bL}=0.5mA, the results of the midband transimpedance gain simulation are shown in Fig. 2-16 and the simulation results of the input impedance of each input node are illustrated in Fig. 2-17 where I_v was swept from 0 to 1mA.

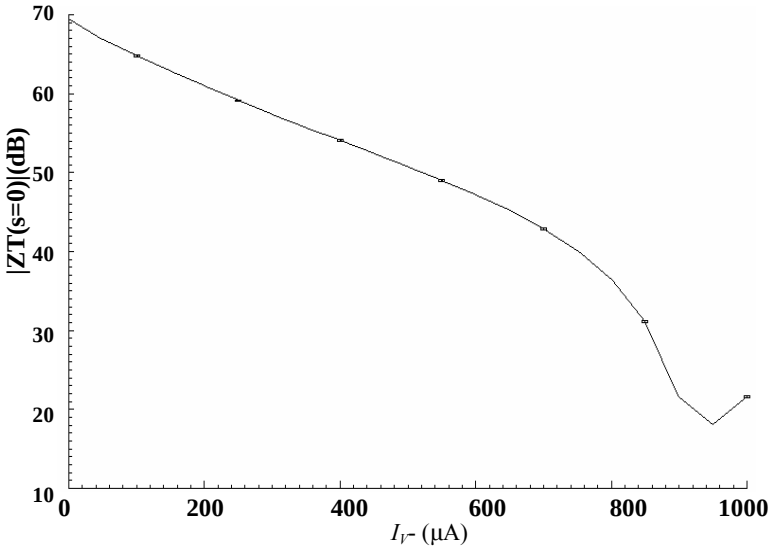


Fig. 2-16 Simulation results of the midband gain of the fully differential variable gain RGC TIA

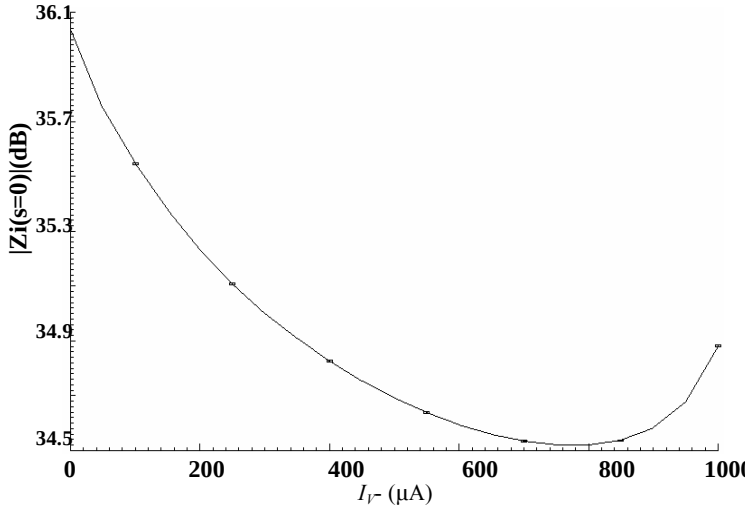


Fig. 2-17 Simulation results of the input impedance of the fully differential variable gain RGC TIA

To increase the sensitivity of the TIA, I_v is minimized so that the input referred noise of the current source ($\overline{i_{n,M_{bL}}}$) is reduced. As a result, the power dissipation will also be reduced.

However, it must be taken into consideration that using a small I_L shifts the dominant pole to lower frequencies. When the input current signal is weak, the gain must be increased (and a lower g_{mv} must be used); thus, the input referred current noise for g_{mv}=0 and the desirable BER can be used for estimating the sensitivity. g_m-boosting amplifier is a cascode differential amplifier whose low input capacitance expands the bandwidth further. The input referred current noise is less than 6.96pA/√Hz at 1GHz. Fig. 2-18 illustrates the input referred current noise spectral density of TIA. The input referred noise current spectral density is less than 14 pA/√Hz within the amplifier's output noise bandwidth. At the highest gain, the average output voltage noise spectral density is 90nV/√Hz.

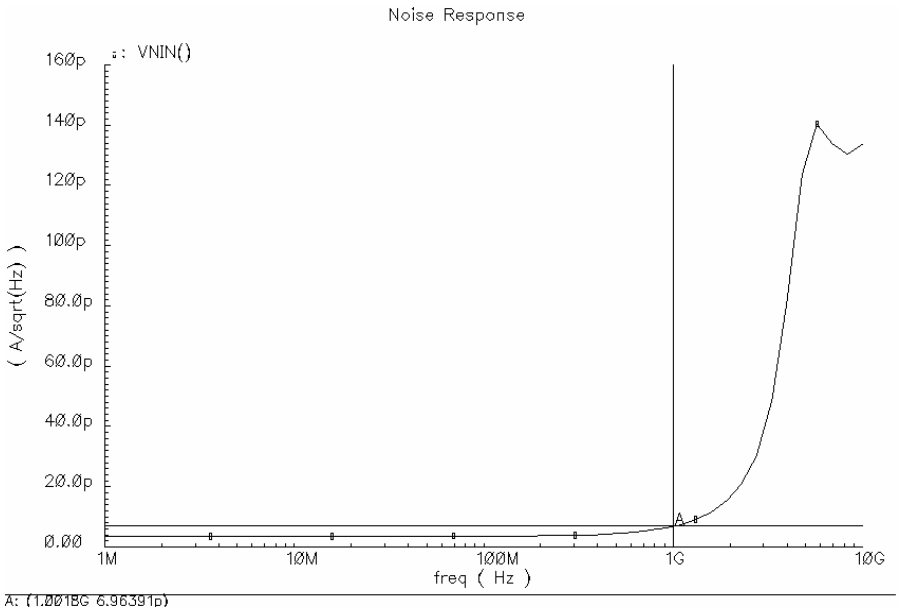


Fig. 2-18 Simulation results of the input referred current noise of the fully differential variable gain RGC TIA

1. Measurement Results

The TIA in Fig. 2-15 and a f_T doubler buffer were fabricated, where an external voltage-to-current converter source generates the TIA's input current. The capacitance connected to each input is greater than $0.6pF$. For I_v=0, a 70dB gain and a bandwidth more than 1.7GHz were obtained. For I_v=2.5mA, the DC gain of 40dB and an approximately 3GHz bandwidth were obtained. Fig. 2-19 illustrates the measurement results of the magnitude of the transimpedance gains. Because of low performance of the buffer in calibration circuit, the AC response measurement results in low frequencies (less than 80MHz) and high frequencies (higher than 3GHz) have less accuracy. This can be clarified by examining eye diagram results. Fig. 2-20 depicts the eye diagram measurement results for the highest gain at the minimum detectable current when for an input test pattern of 2^{31}-1 pseudo-random bits stream (PRBS) BER=10^{-12}. The overall jitter seen in this figure is a combination of several jitters such as jitter of balance to unbalance (Balun) transformers in the test circuit that is created in low-rate bits, jitter of transmitter (source) and the generated jitter by transimpedance amplifier. However, as Fig. 2-20 shows the ripple of the magnitude of transimpedance gain must be less than 3 dB inband. Otherwise, the eye could be vertically closed more than 40%. Fig. 2-21 (a) illustrates the eye diagram measurement results when there is a high gain and a high input current. In this case eye diagram is completely closed. When I_v is increased and the gain is reduced, the eye diagram is opened (see Fig. 2-22 (b)). Table 2-1 compares the performance of the proposed TIA with the existing reports. In terms of overloading, area, noise, and gain dynamic range, this work is better and the overall gain bandwidth is comparable to or better than other reports. The die size of TIA is 100μm×200μm as shown in Fig. 2-23.

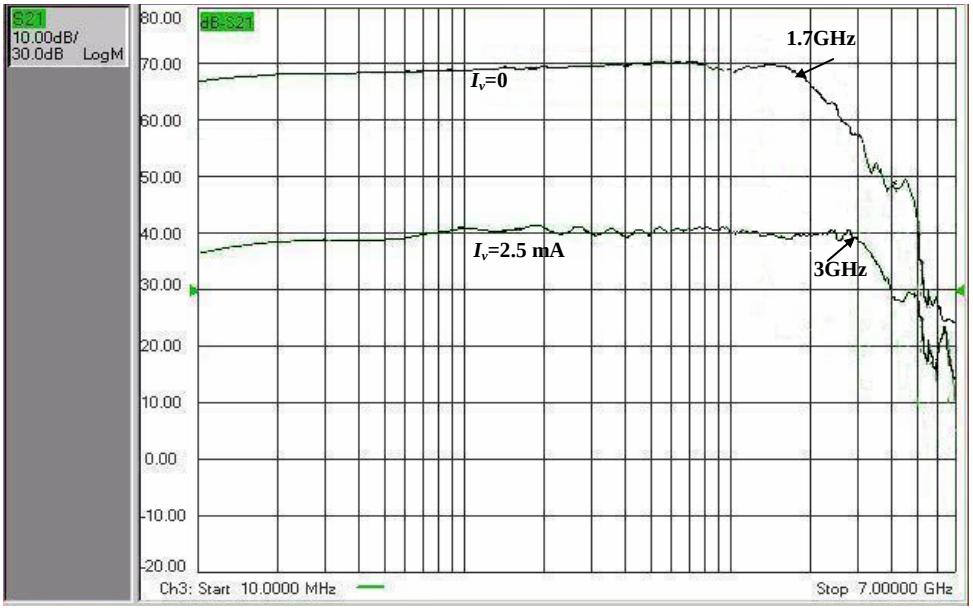


Fig. 2-19 Measurement results of the magnitude of TIA for I_v=0. I_v=2.5mA when I_{bL}=0.5mA

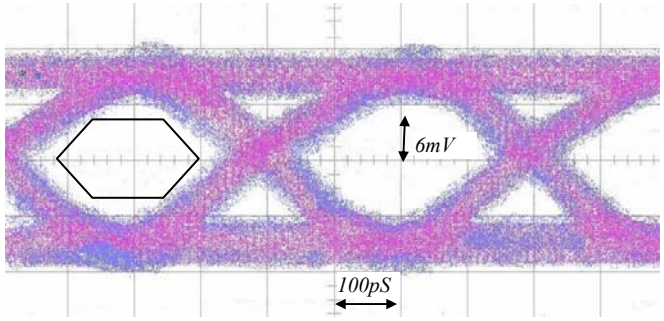


Fig. 2-20 Eye diagram measurement results for I_v=0 and $i_{p\text{-}p}$=6uA when I_{bL}=0.5mA at BER=10^{-12} for an input test pattern of 2^{31}-1 pseudo-random bits stream (PRBS)

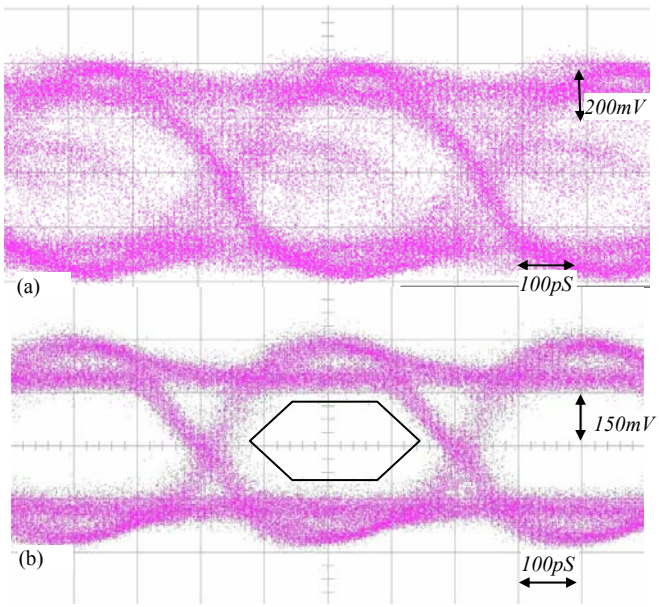


Fig. 2-21 Eye diagram measurement results for $i_{p\text{-}p}$=3mA (a) when I_{bL}=0.5mA and I_v=0 eye is closed (b) when I_{bL}=0.5mA and I_v=2.5mA it is open and BER=10^{-12} for a test pattern of 2^{31}-1 pseudo-random bit stream (PRBS)

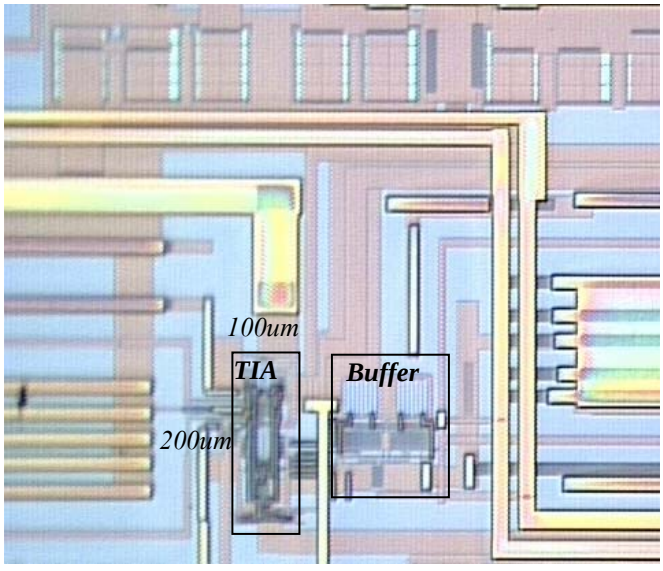


Fig. 2-22 TIA die microphotograph

Table 2-1: Comparison of measurement results with existing reports

parameter	This work	Ref[32]	Ref[17]	Ref[43]	Ref[44]	Ref[45]	Ref[30]
DC Gain (dB)	40-70	60-84.6	57-66	54.5	63.5	54	64
*-3dB frequency (*GHz*)*	1.7-3		2.1	2.7	1.25	2.2	2
Bite Rate (Gbps)	2.5	1.25	2.5	2.5	1.25	2.5	2
Power dissipation (mW)	8.2-24.9	7	38	22.5	40	210	110
Sensitivity (μA)	6	2	7.5	16	5.6		
Input referred noise (nA)	510		540	<800	>560		>600
Overload (μA)	3000	500	200		500		1000
Peak-to-peak jitter (pS)	<120	<140	28	<200	300		>70
Power Supply	3.3	3	1.8	3	3.3	5	5
Input Capacitance (pA)	>0.6	0.8	0.7	0.5	0.7	0.5	0.6
Technology (CMOS)	0.35	0.35	0.18	0.35	0.35	0.6	0.5
Area(mm^2)	0.02	0.04	0.25				0.6

2. Simulation of the Differential Variable Gain TIA in CMOS 0.35μm Technology

TIA in Figure 2-23 was designed and simulated in a CMOS 0.35μm technology for a power supply of 3.3V where C_{PD}=0.5pF. TIA was connected to a buffer to drive paralleled 50Ω resistance and 2pF capacitance loads. When R_L=1$k\Omega$ and I_L=0.5mA, for I_v=0 a midband gain of 60dB and a bandwidth more than 1.8 GHz were obtained. When I_v=1.5mA a midband gain of 40dB and a bandwidth of more than 3.6 GHz were gained. Figure 2-24 illustrates the magnitude of transimpedance gains.

For eye diagram measurement, a random pattern (10000 bits) was used when i_{in}(peak-to-peak)=1uA and bit rate is 2.5Gbits/s. The eye diagram is depicted in Figure 2-25 (a). In this simulation when i_{in}(peak-to-peak) is increased to 4mA, TIA can convert it to proper voltage with the minimum intersymbol interference as shown in Figure 2-25 (b). Since the magnitude of the gain in frequencies higher than 500MHz is more than 40.5 dB, the eye is slightly vertically closed.

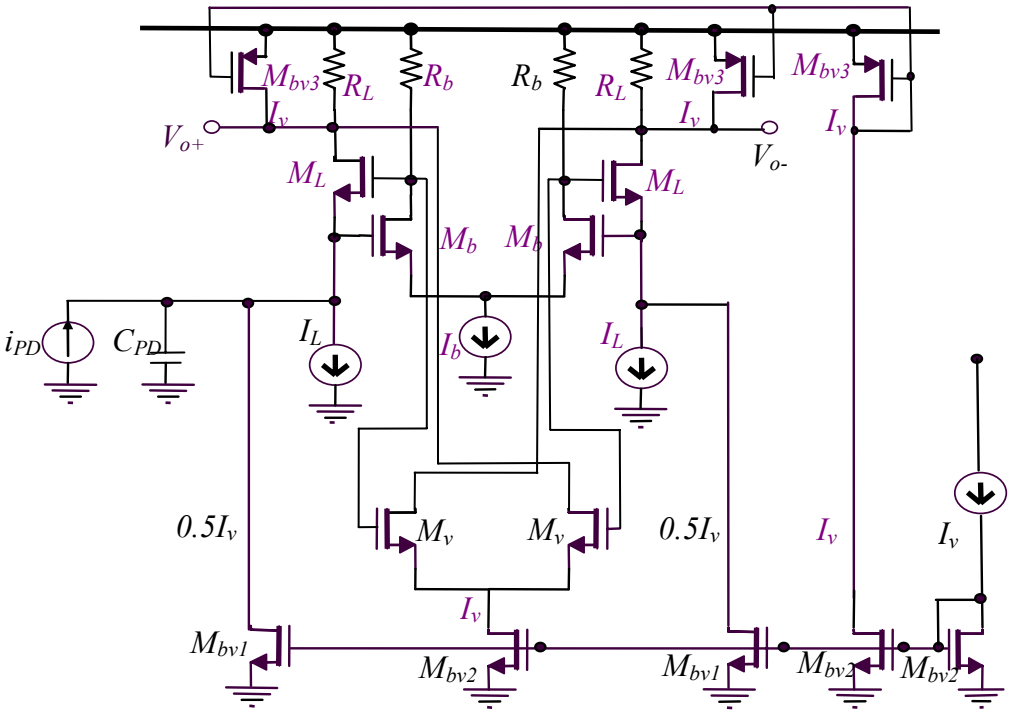


Fig. 2-23 Differential variable gain RGC TIA

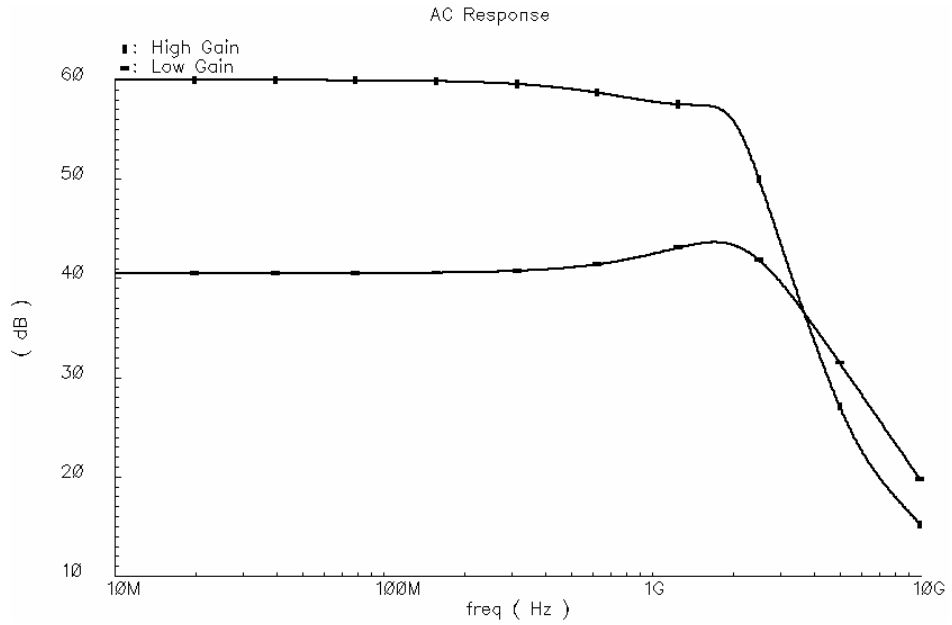
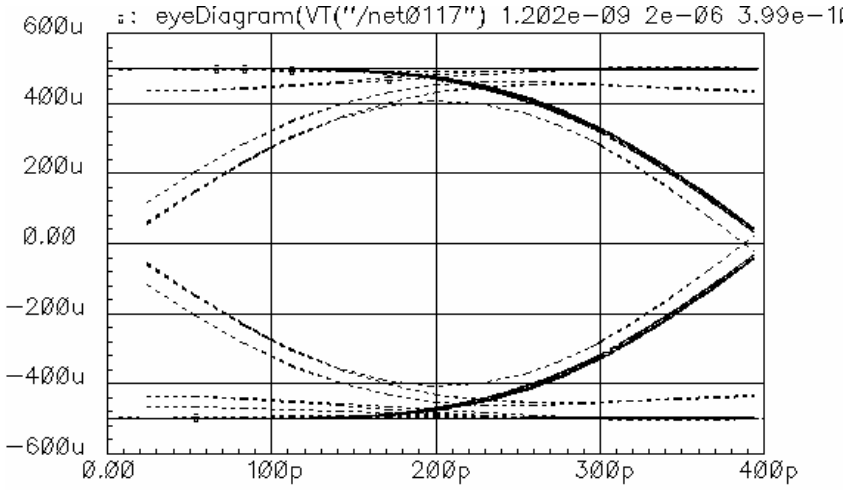
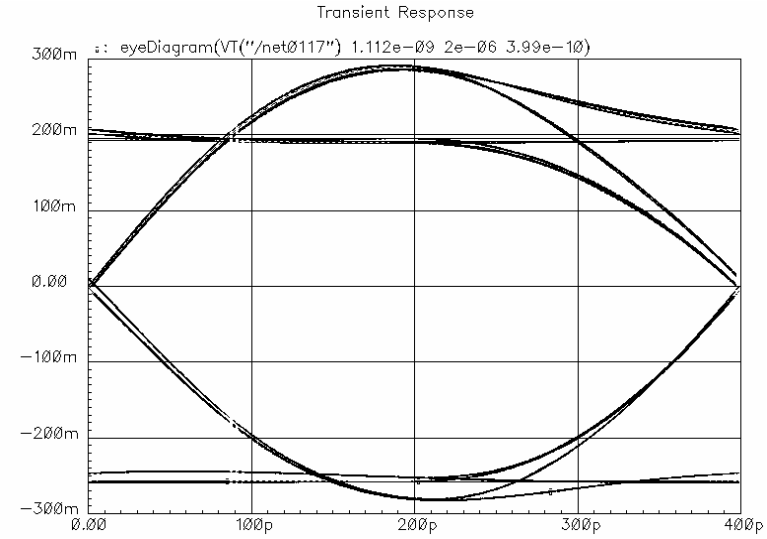


Fig. 2-24 Magnitude simulation results of the differential variable gain RGC TIA



(a)



(b)

Fig. 2-25 Eye diagram for 2.5Gbits/s for 10000 random bits of the differential variable gain RGC TIA. (a) at 1uA (b) at 4mA

CHAPTER III

LIMITING AMPLIFIER

In this chapter designing a limiting amplifier (LA) through designing a multistage amplifier (MA) is described. Usage of a LA in a receiver is demonstrated in Fig. 1-1. The output amplitude of the LA must be independent of the input amplitude over a wide input voltage dynamic range. Since the limiting amplifier directly acts on each single bit, the limiting amplifier can suppress both fast and slow amplitude variations. In order to design a wideband multistage amplifier, the following items must be considered:

-Bandwidth of the multistage amplifier must be wide enough to pass the maximum data rate.

-Gain must be high enough that its output voltage drives the input gates of CDR circuits.

-DC offset must be reduced and a DC offset cancellation circuit must be employed. This will be discussed in chapter V.

-As explained the MA must have a low phase shift deviation and a crossing point fluctuation over a wide input dynamic range to avoid degrading the sensitivity and phase margin of CDR [11].

-Noise and power dissipation must be minimized.

-Design of the MA must be easy for a lower supply voltage.

-The gain and bandwidth must be programmable and adjustable, so that the performance degradation due to any process variation can be compensated for and adjusted. Programmability and adjustability can also help to optimize LA for different applications.

In order to evaluate the performance of a wideband MA topology, the bandwidth, total gain bandwidth product (GBP_T), gain bandwidth of technology, gain bandwidth product of one stage, noise, power consumption and sensitivity of amplifier parameters are calculated.

A Multistage Amplifier

Cascading amplifiers is an approach to achieve a high gain and a wide band amplifier. Cascaded stages directly contribute to define the bandwidth of amplifier. A typical multistage amplifier (MA) can be designed by cascading simple gain stages. Fig. 3-1 illustrates a 3-stage MA consisting of three forward amplifiers with gains of g_1, g_2 and g_3, where the overall gain is $g_1g_2g_3$.

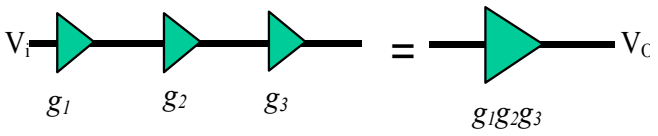


Fig. 3-1 3-stage conventional multistage amplifier (MA)

B Conventional Multistage Amplifier

The amplifier blocks in Fig. 3-1 have traditionally been implemented using three different approaches; two of them are illustrated in Fig. (a)-(b). In Fig. 3-2(a), all stages of the *n*-stage conventional MA have the same transfer function with the same single dominant pole ($\omega_{p1}=\omega_{p2}=...=\omega_{pn}=\omega_p$) [47]-[48] and the same DC gain of G as:

$$g_j(s)=\frac{\omega_p G}{s+\omega_p} \tag{3-1}$$

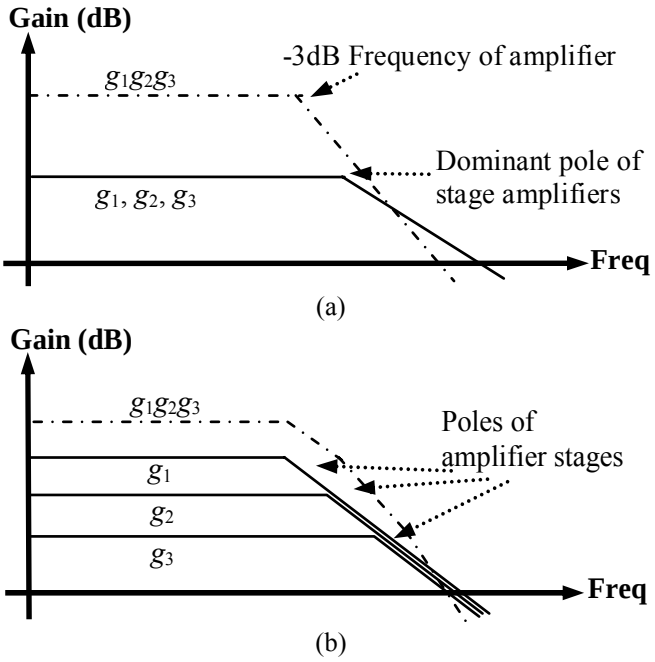


Fig. 3-2 Implementation of amplifier stages in Fig. 3-1 (a) all stages are identical (b) gains as well as dominant poles are different

Then, the overall DC gain and the bandwidth of an *n*-stage MA are obtained by

$$G_T = G^n \tag{3-2}$$

$$\omega_{bw} \approx \omega_p \sqrt{2^{1/n} - 1} \tag{3-3}$$

In Fig. 3-2(b) amplifier stages have different transfer functions, i.e., they do not have the same single dominant pole and DC gain.

Each stage of a conventional multistage amplifier can be realized as a simple circuit in Fig. 3-3. Depending on bias current [49] and employed technology, gain bandwidth of this stage can be approximated. The NMOS transistors M_1 are main amplifying transistors. Resistor R_L is used as amplifier load to get wide-band and low-noise operation.

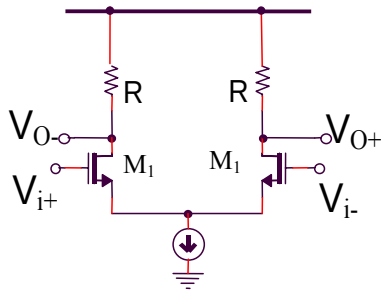


Fig. 3-3 A simple stage for an *n*-stage conventional MA

For analysis of the multistage amplifier, in Fig. 3-2(a) and (b), a simple model for each stage can be considered. Fig. 3-4 illustrates a cascode connection of an *n*-stage amplifier, where each stage is modeled with a current source, resistor and capacitors.

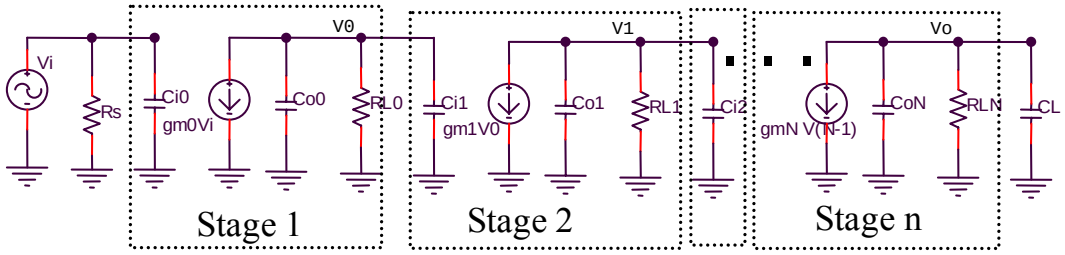


Fig. 3-4 A small signal model for *n*-stage amplifier, each stage modeled by the current source, load resistor and two capacitors (output capacitor of the stage and input capacitor of the next stage)

Each *j*th stage has the dominant pole ω_{pj}.

$$\omega_{pj} = \frac{1}{C_j R_{oj}} \tag{3-4}$$

where C_{oj} and C_{ij} are output and input capacitances and R_{Lj} and R_{ij} are load resistance and input resistance of the *j*th stage; respectively. $C_j = C_{i(j+1)} + C_{oj}$ and $R_{oj} = R_{Lj} // R_{i(j+1)}$ The input-output transfer function of the amplifier can be obtained directly from

$$H(s) = \prod_j g_j(s) = \frac{\prod_j G_j}{\prod_j \left(1 + \frac{s}{\omega_{pj}}\right)} \tag{3-5}$$

Assume equation (3-5) can be approximated as a first order transfer function with a dominant pole of ω_{bw} and the total gain G_T. In this case

$$H(s) \approx \frac{G_T}{1 + s(1/\omega_{bw})} \tag{3-6}$$

The transient time of output voltage is

$$t_r \approx \frac{2.2}{\omega_{bw}} \tag{3-7}$$

If the slowest transient time for a system is defined as $t_{r\text{-}max}$, the amplifier must have a pole of

$$\omega_{bw} > \frac{2.2}{t_{r-\max}} \tag{3-8}$$

For example, for a transient time of 200pS the bandwidth must be higher than 1.75GHz. In industry, the bit rate is usually considered as the bandwidth of the main amplifier. For instance, the bit rate of OC-48 is 2.5Gbits/S; a bandwidth about 2.5 GHz [23] for the main amplifier is expected.

The input voltage referred noise spectral density can be modeled as a voltage source in series with the input of a multistage amplifier. Assuming that all stages are identical and their transfer functions are as described in Fig. 3-2(a) and the stages are like Fig. 3-3, the noise can be given as

$$\overline{v_n^2} = \frac{16}{3} kT \frac{1}{g_m}\left(1 + \frac{1}{G}\right) + \frac{\overline{v_{n,2}^2}}{G^2} \tag{3-9}$$

in which, g_m is the transconductance gain of input transistors, $G=g_mR$ is the DC gain of the first stage and $v_{n,2}$ is the input voltage referred noise of the amplifier after the first stage. Equation 3-9 also shows that in order to reduce the input referred noise, transconductance gain (g_m) and also the DC voltage gain (G) must be increased.

The bandwidth of a MA made of stages illustrated in Fig. 3-3 is not adjustable easily, although changing the bias current of stages can be used (as not a flexible way) to vary the DC gain.

*C Gain Bandwidth Product (*GBP*)*

A definition used to describe an amplifier is total GBP (GBP_T) e.g. for Fig. 3-2(a), for an *n*-stage conventional MA (when all stages are designed as in Eq. (3-1)) can be written

$$GBP_T = G^n \omega_p \sqrt{2^{1/n} - 1} \tag{3-10}$$

A meaningful definition for performance of an *n*-stage MA is the gain-bandwidth product of a single stage [49] (GBP_1), which can be written as:

$$GBP_1 = \left(Overall\ Gain\right)^{1/n} \times (3 - dB\ bandwidth) \tag{3-11}$$

GBP_1 shows how much gain bandwidth of one stage is used. For example, for a multi stage amplifier with magnitude as shown in Fig. 3-2 (a) (for an *n*-stage conventional MA), GBP_1 is obtained from

$$GBP_1 = G\omega_p \sqrt{2^{1/n} - 1} \tag{3-12}$$

As Equation (3-12) shows, only $(2^{1/n}\text{-}1)^{0.5}$ times the gain bandwidth of each stage ($G\omega_p$) is used. In other words, to have a total gain of G^n, bandwidth of ω_{3dB} and a desirable power

consumption, a technology with a stage's gain bandwidth product of $(2^{1/n}-1)^{-0.5}G\omega_{3dB}$ must be used. Equation 3-12 shows if the number of stages (n) is increased, GBP_1 is decreased.

D Conventional Multistage Amplifier with Passive Feedback

Consider an n-stage conventional MA with passive negative feedback within each stage as illustrated in Fig. 3-5. Assume each stage has a feedback gain of F (frequency independent) and each forward gain stage can be modeled as a 1st-order transfer function where the bandwidth of each stage is $k\omega_p$ (assuming k>1). Assuming DC loop gain $L=GF$, using feedback, the dominant pole of each stage is ideally shifted to $(1+L)k\omega_p$. Ideally the overall bandwidth of an n-stage MA with passive feedback can be written as

$$\omega_{bw} \approx k\omega_p(1+L)\sqrt{2^{1/n}-1} \tag{3-13}$$

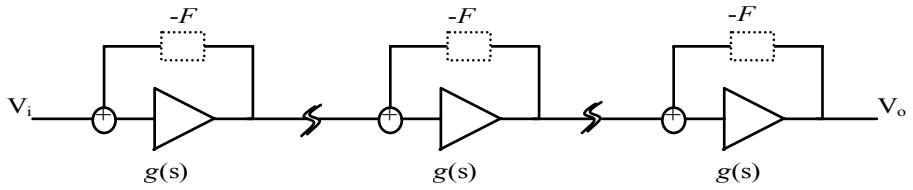


Fig. 3-5 N-stage conventional MA with passive local feedback [63]

But in practice, using feedback devices adds extra parasitic and reduces the bandwidth of each stage from $k\omega_p$ to ω_p and the dominant pole of each stage is shifted to $(1+L)\omega_p$. The overall bandwidth of an n-stage MA with passive feedback can be approximated as

$$\omega_{bw} \approx \omega_p(1+L)\sqrt{2^{1/n}-1} \tag{3-14}$$

The GBP_1 of Fig. 3-5 is also obtained by Equation (3-12) and GBP_T can be written as

$$GBP_T = \frac{G^n}{(1+L)^{n-1}} \omega_p \sqrt{2^{1/n} - 1} \tag{3-15}$$

Equations (3-14) and (3-15) show that increasing feedback for having a ((1+L)/k times) wider bandwidth, decreases GBP_T proportional to $1/k(1+L)^{n-1}$.

E Expanding the Bandwidth

As it was discussed, the performance of digital-signal and pulse-based systems and instrument is usually affected by bandwidth of amplifiers. Designing MAs with a bandwidth that is as large as the bit rate of the signal [23] (e.g. 10 GHz for SONET OC-192), using standard CMOS technology is still a challenging issue. Employing bandwidth enhancement techniques such as capacitance neutralization [23], capacitive-peaking [51], bootstrapping [52] and shunt-peaking [30] expands the bandwidth of gain stages, thus broadens the overall bandwidth ω_{bw} [53]. Expanding ω_p, is the method used to broaden the overall bandwidth of an MA [30], [51]-[54].

For example, the bandwidth of the amplifier is further enhanced by the use of inductive loads in every gain stage. This famous technique, called shunt peaking, moves the pole of each stage to a higher frequency by partly tuning out its capacitive load. It can extend the bandwidth by about 70% [48] without introducing undesirable peaking in the frequency response. Figure 3-6 shows a stage of a limiting amplifier using this approach to enhance bandwidth [10], [30], [48]-[50].

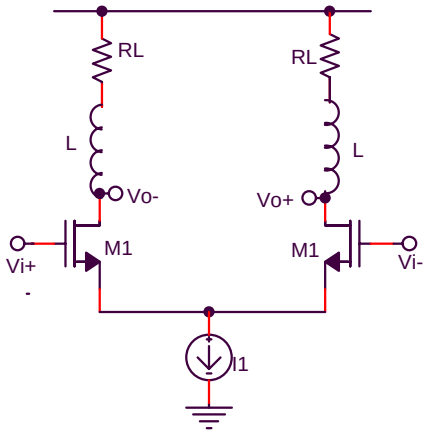


Fig. 3-6 An enhanced stage of limiting amplifier

It is difficult to use a 0.35μm CMOS technology (a cheap technology, even 0.25μm CMOS technology) to design spiral inductors with high inductance (e.g. 10 nH) and keep the self-resonance well outside (>> 2.7GHz). Moreover, ten spiral inductors consume a large area. Another answer to this problem is using the circuit shown in Fig. 3-7(a). V_g biases the gate of transistors M_Ls. Model of transistor M_L, resistor serried with gate (R_g) and bias voltage is shown in Fig. 3-7(b). In this case since R_g is much bigger than inverse g_{mL}, transistor M_L and resistor serried with its gate can even be modeled as Fig. 3-7(c)

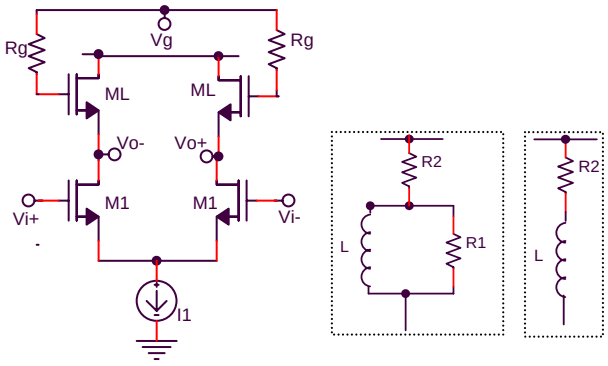


Fig. 3-7 (a) An enhanced stage of limiting amplifier with active load (b) a model for active load (c) the simplified model of the active load

In Fig. 3-7 (b)

$$R_1 = (R_g - \frac{1}{g_{mL}}) \approx R_g \tag{3-16}$$

$$R_2 = \frac{1}{g_{mL}} \tag{3-17}$$

$$L = (R_g - \frac{1}{g_{mL}}) \frac{C_{gsL}}{g_{mL}} \approx R_g \frac{C_{gsL}}{g_{mL}} \tag{3-18}$$

where g_{mL} and C_{gsL} are transconductance gain and gate-source capacitance of M_L; respectively. The gain of the stage with active inductors is determined by the geometrical ratio of two NMOS transistors M_1 and M_L as

$$A_j = \frac{g_{m1j}}{g_{mLj}} = \sqrt{\frac{W_1}{W_L}} \tag{3-19}$$

The input voltage referred noise spectral density can be given as

$$\overline{v_n^2} = \frac{16}{3} kT \frac{1}{g_m} + \frac{16}{3} kT \left(\frac{1}{g_m} \right)^2 g_{mL} + \frac{\overline{v_{n,2}^2}}{G^2} \tag{3-20}$$

Obtained noise from Equations 3-20 and 3-9 show the circuit with active loads produces more noise. As seen, DC gain and the bandwidth of the circuit in Fig. 3-6 like that of circuit in Fig. 3-3 can be adjusted (not in a flexible way). If the circuit in Fig. 3-7 (a) is employed, the MA can be slightly tunable. However changing the gain is still far from easy.

1. Conventional Peaking Technique

Widening the bandwidth of individual stages is usually not sufficient for bandwidth enhancement, where the overall bandwidth is typically smaller than individual poles [23], [48]. However, increasing ω_p is not enough for bandwidth enhancement since the combination of the poles of all stages degrades the overall bandwidth, ω_{bw}. For example, for a conventional MA, ω_{bw} is always less than ω_p when n>1.

Two approaches traditionally used for implementation of a multistage amplifier (like n-stage conventional MA in Fig. 3-1) were shown in Fig. 3-2 (a) and (b). The third approach is using peaking techniques. Peaking techniques enhance ω_p by introducing a peak in a transfer function at high frequencies.

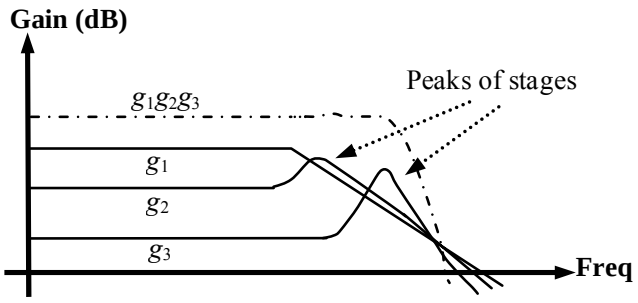


Fig. 3-8 Implementation of amplifier stages in Fig. 3-2 peaking is used within amplifiers

In Fig. 3-8 the conventional peaking technique is used for bandwidth enhancement. Some of the stages have transfer functions with complex poles, which introduce peaks [55]-[56].

The amplifier topologies in Fig. 3-2(b) and 3-8 are not uniform and their amplitude sensitivity with respect to each stage's component is different. Conventional multi-peak enhancement techniques use stages with different gains and poles in order to create peaks at different frequencies. An early roll-off due to a low frequency pole in one stage can be compensated with peaking in the next stage [55]-[56]. Although the conventional peaking technique gives a wider bandwidth, it has three drawbacks. First, the design of amplifier stages is not uniform and each stage needs to be designed separately. Second, amplifier stages with high quality factors are required, thus process variations may result in an undesirable peaking [57]. In other words, sensitivity of stages with high quality factors limits the usage of these circuits in typical applications. Third, the widest bandwidth is obtained when inductors are used, which increases the chip area [55]-[56].

F Proposed LA

The proposed TIA, LA and DC Offset Cancellation Circuit are shown in Fig. 3-9. This dissertation introduces a new topology *entitled* the chained multistage amplifier (CMA), which uses the peaking technique to expand the bandwidth while the topology can be implemented uniformly. Due to active feedback, amplifier sections can be designed with low quality factors and with no inductors. In addition, CMA exploits the intrinsic capacitance within the transistors to push output pole of each stage to a higher frequency. The topology of CMA offers several advantages such as improved performance and gain-bandwidth product and high flexibility to vary gain and bandwidth that make the proposed structure suitable for multi standard optical communications. To demonstrate the proposed topology, two tunable six-stage amplifiers in 0.35μm CMOS process were designed and fabricated. In the following sections, the proposed structure of CMA is described in detail. The design procedure and realization details of two amplifiers, post-layout simulations and measurement results are presented in chapter IV.

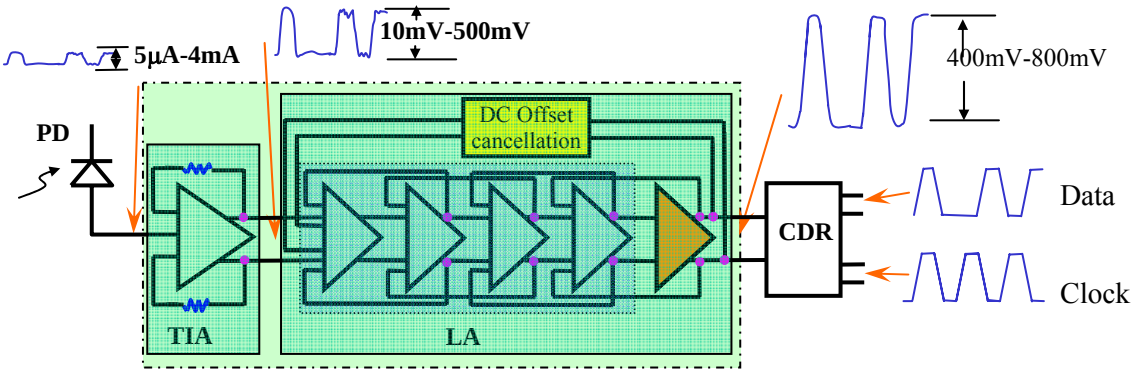


Fig. 3-9 Proposed TIA, LA and DC offset cancellation circuit

G Chained Multistage Amplifier

Fig. 3-10 shows the general topology of the proposed *n*-stage CMA. The overall structure is composed of *n* amplifier stages $g_1(s)$,…, $g_n(s)$ with active feedback gains $f_1(s)$,…, $f_n(s)$. The outputs of forward gain stages, $g_j(s)$, and feedback stages, $-f_j(s)$, are added together. The input-output transfer function of the *n*-stage CMA can be obtained from

$$H(s)=\frac{\prod_{i=1}^{n} g_i(s)}{1+\sum_{i=1}^{n-1} L_i(s)+\sum_{i=1}^{n-3}\sum_{j=i+2}^{n-1} L_i(s)L_j(s)+\sum_{i=1}^{n-5}\sum_{j=i+2}^{n-3}\sum_{k=j+2}^{n-1} L_i(s)L_j(s)L_k(s)+\ldots} \tag{3-21}$$

where $L_m(s)=g_m(s)\,f_{m-1}(s)$ is the loop gain of $(m\text{-}1)th$ loop while m=1,2,… n-1.

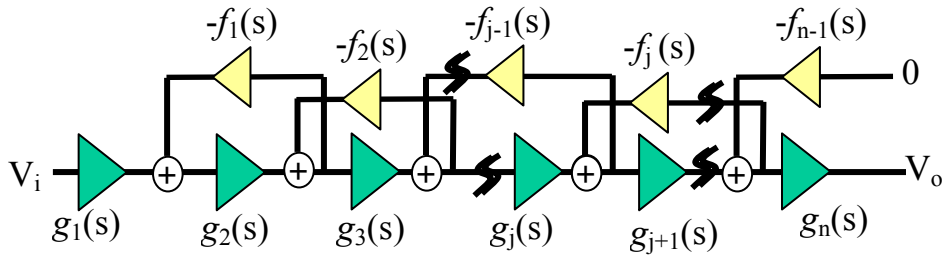


Fig. 3-10 General form of CMA topology

The general equation of the transfer function can also be shown as

$$H(s)=\frac{\prod_{i=1}^{n} g_i(s)}{1+\sum_{i=1}^{n-1} L_i(s)+\sum_{js\ without\ overlap}\prod L_j(s)} \tag{3-22}$$

H Uniform Chained Multistage Amplifier (CMA)

Topology of the proposed amplifier is illustrated in Fig. 3-11. The overall structure consists of identical forward amplifiers (g(s)) with identical active feedbacks ($-f$(s)). The input-output transfer function of the uniform n-stage CMA can be obtained as

$$H(s)=\frac{[g(s)]^n}{1+(n-1)L(s)+\left[(n-2)\frac{(n-3)}{2}L^2(s)\right]_{n>3}+\left[\sum_{i=2}^{n-4}(n-i-3)\frac{(n-i-2)}{2}L^3(s)\right]_{n>5}+..} \tag{3-23}$$

where L(s)=g(s) f(s) is the loop gain.

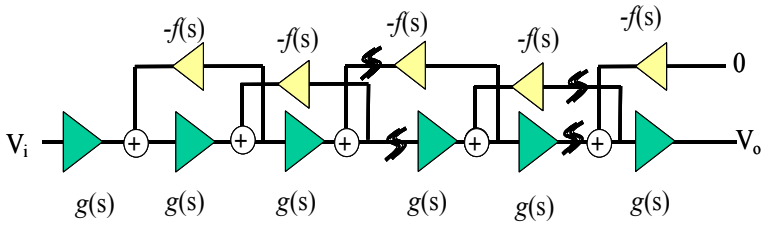


Fig. 3-11 Topology of the proposed MA (the uniform n-stage CMA)

Assume $g(s)$ and $f(s)$ have a single pole and no zeros; however, the effect of additional poles will be discussed for stability. Therefore, Eq. (3-2) represents the transfer function of $g(s)$, where $f(s)$ can be given as

$$f(s)=\frac{\omega_p F}{s+\omega_p} \tag{3-24}$$

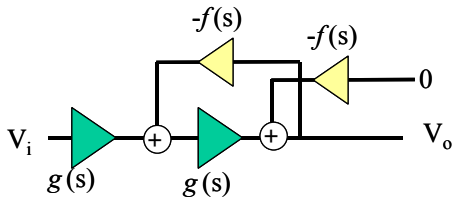


Fig. 3-12 Topology of a uniform 2-stage CMA

A uniform 2-stage CMA is illustrated in Fig. 3-12. Its input-output transfer function is a 2nd-order function as

$$\frac{G_T \omega_n^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \tag{3-25}$$

where ω_n is the natural frequency and Q is the quality factor given by

$$\omega_n = \omega_p \sqrt{1+L} \tag{3-26}$$

$$Q = 0.5\sqrt{1+L} \tag{3-27}$$

Equations (3-25), (3-26) and (3-27) show that 2-stage CMA has always complex poles for L>0. For L>1, where the response is under-damped, the 3-dB bandwidth can be given as

$$\omega_{bw} = \omega_p \left[L - 1 + \sqrt{2\left(L^2 + 1\right)} \right]^{0.5} \tag{3-28}$$

In this case, the amplitude of the normalized gain has a peak given by

$$M_p = 0.5(L+1)/\sqrt{L} \tag{3-29}$$

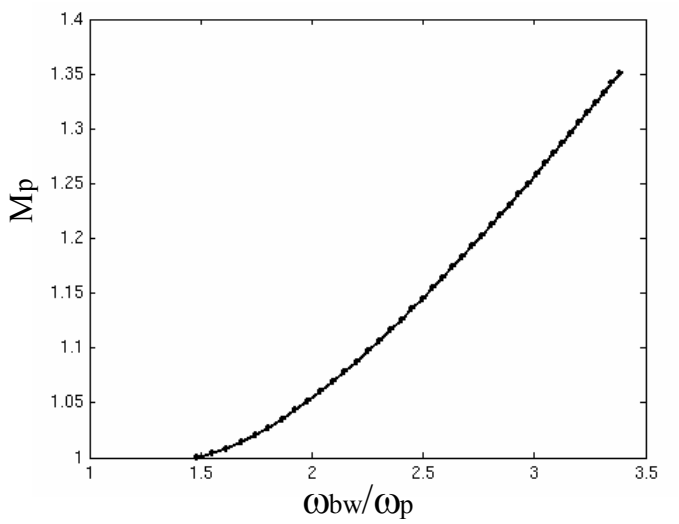


Fig. 3-13 M_p vs. ω_{bw}/ω_p of the 2-stage CMA

Fig. 3-13 illustrates M_p as a function of ω_{bw}/ω_p for a 2-stage CMA. For the case of no peaking in the frequency response (M_p=1, L=1), the bandwidth can be enhanced to $1.41\omega_p$. Further improvement up to $2.70\omega_p$ can be obtained if the loop gain is increased to 3.3, which also increases the peak to 1.19 (or 1.5 dB). DC gain (G_T) is calculated by

$$G_T = \frac{G^2}{(1+L)} \tag{3-30}$$

As expected in feedback amplifiers, G_T reduces as L increases when G is kept constant. If the gain and the bandwidth are given in Equations (3-28) and (3-30), respectively, are realized by a conventional 2-stage amplifier (as shown in Fig. 3-2(a)), then the gain-bandwidth product required for a single stage can be found as

$$1.55G\omega_p\left[\left(L-1+\sqrt{2\left(L^2+1\right)}\right)/(1+L)\right]^{0.5} \tag{3-31}$$

Assuming that the stages of MA are used as the forward amplifiers of CMA and the feedback amplifiers are combined with them to create the amplifier stages, the parasitic of the feedback

amplifier has reduced the bandwidth of the forward amplifier from $k\omega_p$ to ω_p, when k depends on the circuit implementation of the amplifier stages and technology (k>1). Consequently, the required gain-bandwidth product of the amplifier stages must be greater than $1.55G\omega_p/k$ for the conventional topology (MA), whereas CMA requires a gain-bandwidth product of $G\omega_p$, where L>l. For example, for k=1.2 the required gain-bandwidth product for MA is more than $1.3G\omega_p$.

The 4-stage CMA's transfer function (which is 4th order) can be expressed as a product of two 2nd-order transfer functions with natural frequencies ω_{n1}, ω_{n2} and quality factors Q_1, Q_2 given as

$$\omega_{n1} = \omega_p\sqrt{1+2.62L} \tag{3-32}$$

$$\omega_{n2} = \omega_p\sqrt{1+0.38L} \tag{3-33}$$

$$Q_1 = 0.5\sqrt{1+2.62L} \tag{3-34}$$

$$Q_2 = 0.5\sqrt{1+0.38L} \tag{3-35}$$

For 0.38<L<2.62, one of the 2nd order functions has a peak, whereas for 2.62<L each function has a peak at frequencies ω_{peak1} and ω_{peak2}

$$\omega_{peak2} \approx \omega_p\sqrt{0.38L-1} \tag{3-36}$$

$$\omega_{peak1} \approx \omega_p\sqrt{2.62L-1} \tag{3-37}$$

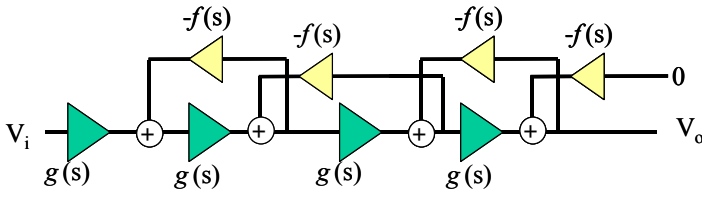


Fig. 3-14 Topology of the uniform 4-stage CMA

The overall bandwidth of 4-stage amplifier can be improved up to about $2.9\omega_p$ with a peak smaller than 1.5dB in the transfer function.

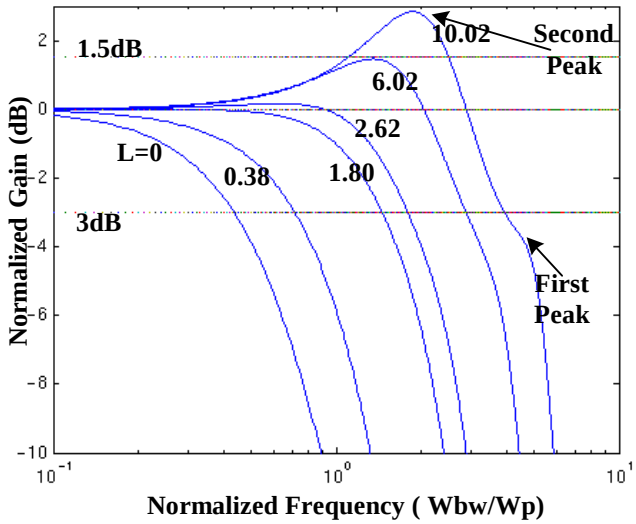


Fig. 3-15 A Matlab plot of the normalized gain of a 4-stage CMA for L=0, 0.38, 1.80, 2.62, 6.02 and 10.02

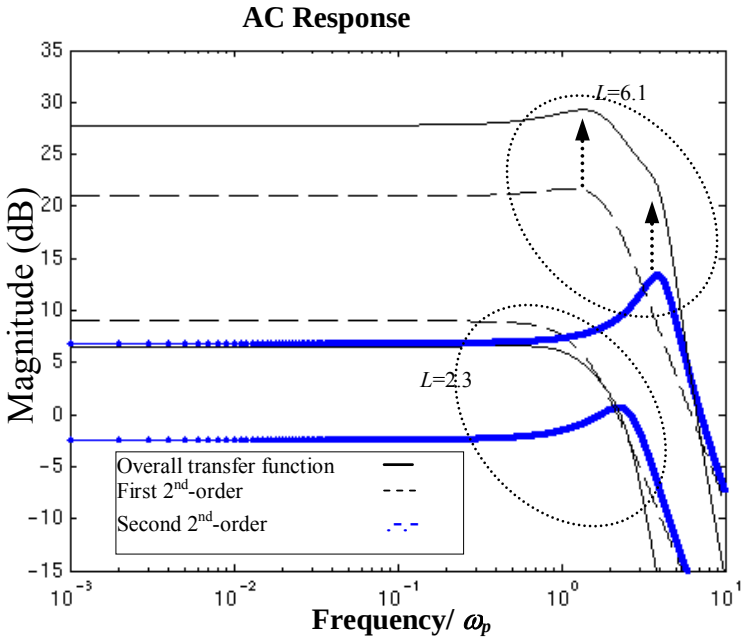


Fig. 3-16 A Matlab plot of magnitude of two 2nd-order transfer functions and the overall function of 4-stage CMA

Fig. 3-15 illustrates a Matlab plot of the normalized gain of the 4-stage amplifier for different values of L. For $L \leq 1.8$, the CMA's transfer function's amplitude does not have a peak and the bandwidth is less than or equal to $1.47\omega_p$. As L is increased beyond 2.62, the second 2nd-order transfer function introduces the second peak. Further increase in L separates the frequencies of the two peaks. Fig. 3-15 shows that increasing L increases the peak of the gain, which expands the bandwidth. A Matlab simulation of the transfer function of 4-stage CMA and two 2nd-order functions (at F=1) for Ls of 2.3 and 6.1, respectively, are illustrated in Figure 3-16. The peak of one of the 2nd-order functions is placed, where the other 2nd-order function is decreasing. For small Ls, the $-3dB$ frequency of CMA is determined by the $-3dB$ frequency of the first 2nd-order function. Increasing DC gain of forward stages (G) increases the ripple of the overall function and pushes the $-3dB$ frequency to higher frequencies and extends the

bandwidth. Increasing DC loop gain widens the bandwidth up to the point, where the first 2nd-order function produces a peak of more than 1.5dB.

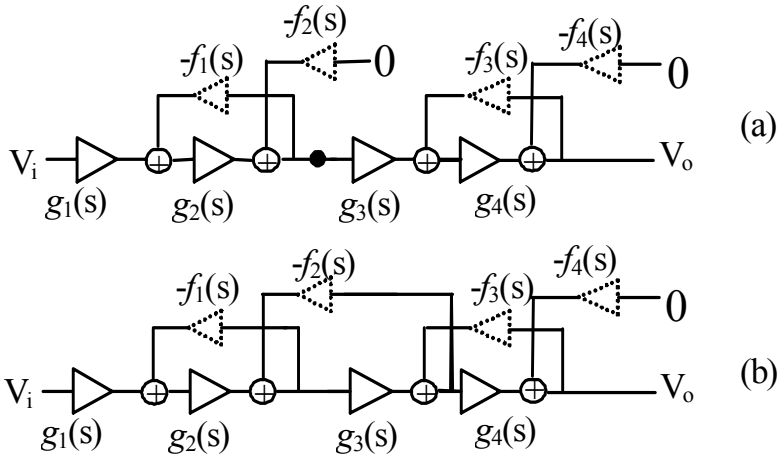


Fig. 3-17 The schemes of (a) cascaded two 2-stage CMAs, (b) 4-stage CMA

To clarify how much the feedback between stages improves the bandwidth of a 4-stage CMA, consider two 2-stage CMAs in cascade form (see Fig. 3-17 (a)). It can be intuitively seen that cascade combination of two 2-stage CMAs (see Fig. 3-17 (a)) has a bandwidth less than the single 2-stage CMA. Also Fig. 3-18 shows the Matlab plots of the magnitude of transfer functions of a 4-stage CMA and two cascaded 2-stage CMAs for different Ls and F=1. Indeed, a 4-stage CMA has one extra feedback path from the output of the third stage to the second stage. For G>2.3 in two cascaded 2-stage CMAs, there is a peak (>1.5 dB). The maximum bandwidth in two cascaded 2-stage CMAs is $1.96\omega_p$ that is about 71% of the bandwidth of one 2-stage CMA. Not only the maximum achievable bandwidth of 4-stage CMA did not decrease, but also it can reach up to $2.9\omega_p$ without incurring a significant peak in transfer function. In this case the maximum bandwidth can be 6.7 times of the bandwidth of a 4-stage conventional MA ($k\approx1$). If a

conventional MA is going to be used instead, the technology, which must be employed, has to have a gain bandwidth of stage more than $2.41G\omega_p/k$.

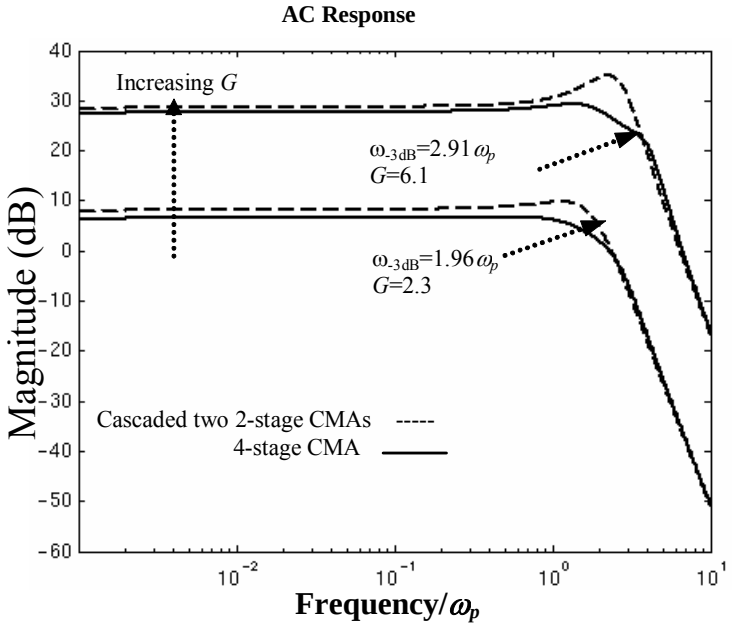


Fig. 3-18 A Matlab plot of magnitude of transfer functions of schemes in Figure 3-17 for different *G*s and *F*=1

1. Peaking in 6-stage and 8-stage CMA

The transfer function of the CMA for *n*=6 and 8 can also be written as a product of 2nd-order transfer functions. Peaking frequencies for a simple 6-stage CMA can be approximated as

$$\omega_{peak1} \approx \omega_p\sqrt{L/5.05} \tag{3-38}$$

$$\omega_{peak2} \approx \omega_p\sqrt{L/0.64-1} \tag{3-39}$$

$$\omega_{peak3} \approx \omega_p\sqrt{L/0.31-1} \tag{3-40}$$

Peaking frequencies for a simple 8-stage CMA are

$$\omega_{peak1} \approx \omega_p \sqrt{L/8.29} \tag{3-41}$$

$$\omega_{peak2} \approx \omega_p \sqrt{L-1} \tag{3-42}$$

$$\omega_{peak3} \approx \omega_p \sqrt{L/0.43-1} \tag{3-43}$$

$$\omega_{peak3} \approx \omega_p \sqrt{L/0.28-1} \tag{3-44}$$

As seen for both 6-stage and 8-stage CMA peak frequencies are placed in different frequencies. Similarly, the transfer function for an *n*-stage CMA can be arranged so that the bandwidth is improved with the desired level of peaking.

Detailed analysis of the key parameters of the CMA will be presented in the following subsections.

2. Gain and Bandwidth

The overall DC gain (G_T) for different values of *n* has different equations. For instance, G_T for *n*=2 was shown in equation (3-30) while for *n*=4, 6, and 8, it can be respectively calculated as

$$G_T = \frac{(mL)^2}{1+3L+L^2} \tag{3-45}$$

$$G_T = \frac{(mL)^3}{L^3+6L^2+5L+1} \tag{3-46}$$

$$G_T = \frac{(mL)^4}{L^4+10L^3+15L^2+7L+1} \tag{3-47}$$

where $m=G/F$. When *G* is kept constant, increasing feedbacks increases bandwidth and reduces gain; in other words, increasing *m* increases G_T. In general, the more feedback is reduced, the more the CMA matches the conventional MA.

The exact equation for the bandwidth (ω_{bw}) as a function of *n* can be calculated from Eq. (3-23). To reduce the calculation overhead, the following approximation will be used for $4 \le n \le 18$

$$\omega_{bw} \approx (1+L)\omega_p \sqrt{2^{1/n}-1} \quad \text{for} \quad n=4,5\ldots,18 \tag{3-48}$$

Assuming that the bandwidth of each forward amplifier of MA is $k\omega_p$, using a CMA, a bandwidth of $(1+L)/k$ times the bandwidth of MA can be achieved.

Fig. 3-19 shows the bandwidth of n-stage CMA extracted from the magnitude response simulation result for different DC loop gains (L) for n=2, 4, 6, and 8. The n-stage CMA for odd ns has a real pole (at ω_p) which limits the expansion of bandwidth to some extent. Fig. 3-19 shows that the CMA has two advantages. First, its bandwidth can be several times of ω_p (the bandwidth of one stage); whereas for n-stage conventional MA, ω_{bw} is always less than ω_p. Second, CMA can have more bandwidth as n increases. As shown above, 4-stage CMA has more bandwidth than 2-stage CMA. On the contrary, 4-stage conventional MA has less bandwidth than 2-stage conventional MA. The maximum bandwidth that can be obtained for n=8 is $4.51\omega_p$. As F decreases, a higher G is needed to have the same bandwidth. Although as n increases CMA can have more bandwidth, it also needs more L. Fig. 3-19 shows that if L is constant, a smaller n gives more bandwidth.

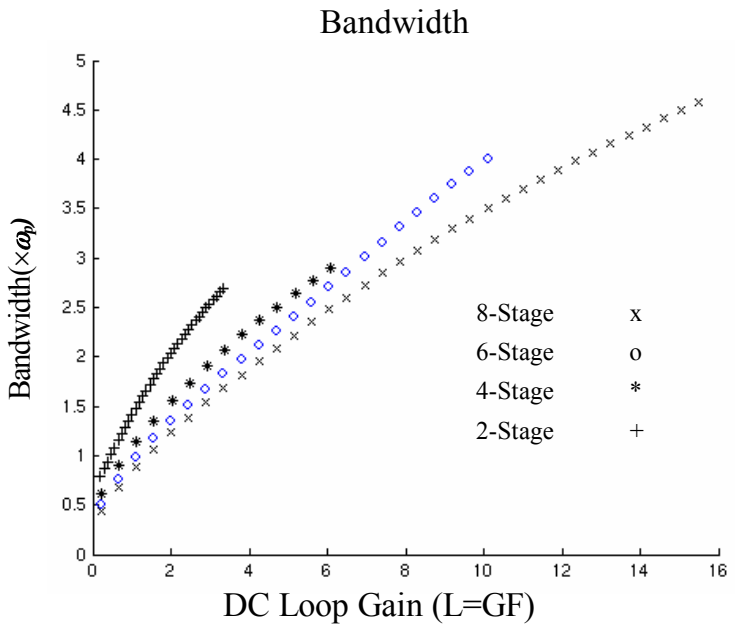


Fig. 3-19 A Matlab plot of the bandwidth of 2, 4, 6 and 8-stage CMA in ω_p for different DC loop gains (L)

For the same number of stages and the same L, both structures of CMA and MA shown in Fig. 3-5 have the same bandwidth (assuming the stages have the same bandwidth of ω_p). In contrast to CMA, the topology in Fig. 3-5 cannot have high loop gains due to passive feedback, which limits the expansion of the bandwidth.

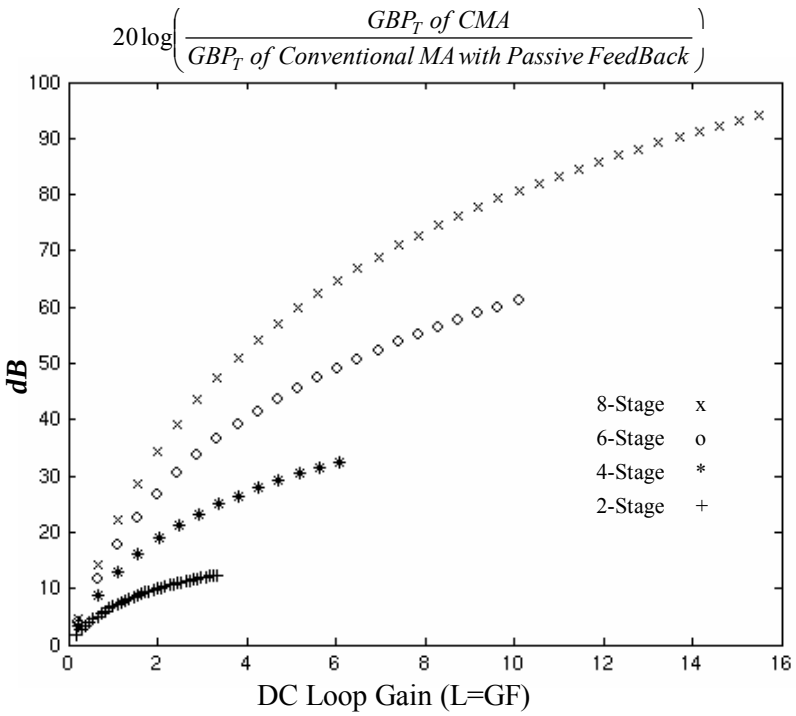


Fig. 3-20 A Matlab plot of the ratio of GBP_T of n-stage CMA and conventional MA with passive feedback illustrated in Fig. 3-5 for n=2, 4, 6 and 8

The ratio of GBP_T of CMA and conventional MA shows how much GBP_T is decreased. The general equation of the total Gain bandwidth product of an n-stage CMA, like the simple uniform CMA, can be calculated as

$$GBP_T \approx \frac{\left(G^n(1+L)\omega_p\sqrt{2^{1/n}-1}\right)}{1+(n-1)L+\left[(n-2)\frac{(n-3)}{2}L^2\right]_{n>3}+\left[\sum_{i=2}^{n-4}(n-i-3)\frac{(n-i-2)}{2}L^3\right]_{n>5}+\ldots} \tag{3-49}$$

Unfortunately, GBP_T of CMA in comparison with that of the conventional MA is smaller (as n and DC loop gain are increased this ratio decreases further). However, GBP_T of CMA in comparison with that of other structures (such as Figure 3-5) is much better. A simulation of the ratio of GBP_T of an n-stage CMA and an n-stage conventional MA with passive feedback for

n=2, 4, 6 and 8 for different DC gain loops is shown in Figure 3-20. As it shows, increasing DC loop gain increases CMA's GBP_T. As n is increased, this ratio also increases.

GBP_1 of an amplifier, which is used to show the performance of a multistage amplifier, was described before. The general equation of the gain bandwidth product of a single stage for an n-stage CMA, like the uniform CMA, can be calculated as

$$GBP_1 \approx \frac{G(1+L)\omega_p\sqrt{2^{1/n}-1}}{\left\{1+(n-1)L+\left[(n-2)\frac{(n-3)}{2}L^2\right]_{n>3}+\left[\sum_{i=2}^{n-4}(n-i-3)\frac{(n-i-2)}{2}L^3\right]_{n>5}+\ldots\right\}^{1/n}} \quad (3\text{-}50)$$

Another parameter is the ratio of GBP_1 of CMA to that of a similar conventional MA (when the MA's forward amplifier has the bandwidth of $k\omega_p$ and DC gain of G) that shows how much the GBP_1 is improved. This ratio is simulated in Fig. 3-21. It shows that GBP_1 of an n-stage CMA can be several times GBP_1 of an n-stage conventional MA shown in Fig. 3-1. As explained previously, if an n-stage MA topology is used to implement the same specifications of a CMA, the required gain bandwidth product for the stages will be much higher than that of CMA and it can be extracted from the ratio of their GBP_1s, when they have the same overall gain. The required gain bandwidth product for the stages of a MA ($GBP_{R,MA}$) can be calculated as

$$GBP_{R,MA} \approx \frac{G(1+L)\omega_p/k}{\left\{1+(n-1)L+\left[(n-2)\frac{(n-3)}{2}L^2\right]_{n>3}+\left[\sum_{i=2}^{n-4}(n-i-3)\frac{(n-i-2)}{2}L^3\right]_{n>5}+\ldots\right\}^{1/n}} \quad (3\text{-}51)$$

Thus the stages must be enhanced as $GBP_{R,MA}/G\omega_p$.

$$\frac{GBP_{R,MA}}{G\omega_p} \approx \frac{(1+L)/k}{\left\{1+(n-1)L+\left[(n-2)\frac{(n-3)}{2}L^2\right]_{n>3}+\left[\sum_{i=2}^{n-4}(n-i-3)\frac{(n-i-2)}{2}L^3\right]_{n>5}+\ldots\right\}^{1/n}} \quad (3\text{-}52)$$

Fig. 3-21 shows k times this ratio for n=2, 4, 6, and 8–stage

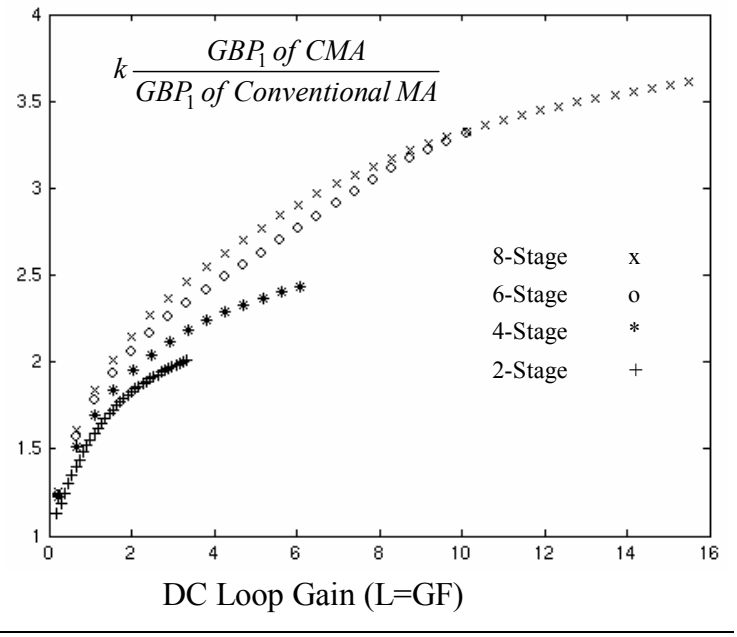
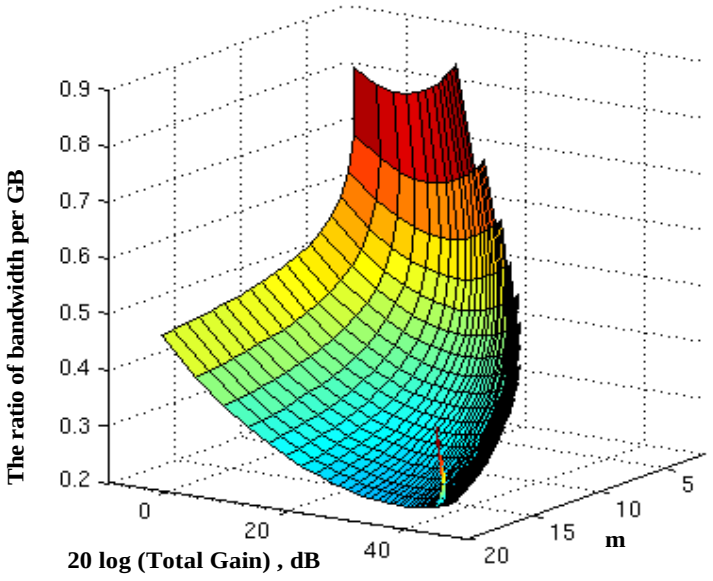


Fig. 3-21 A Matlab plot of the ratio of GBP_1 of 2, 4, 6 and 8-stage CMA and conventional MA for different Ls

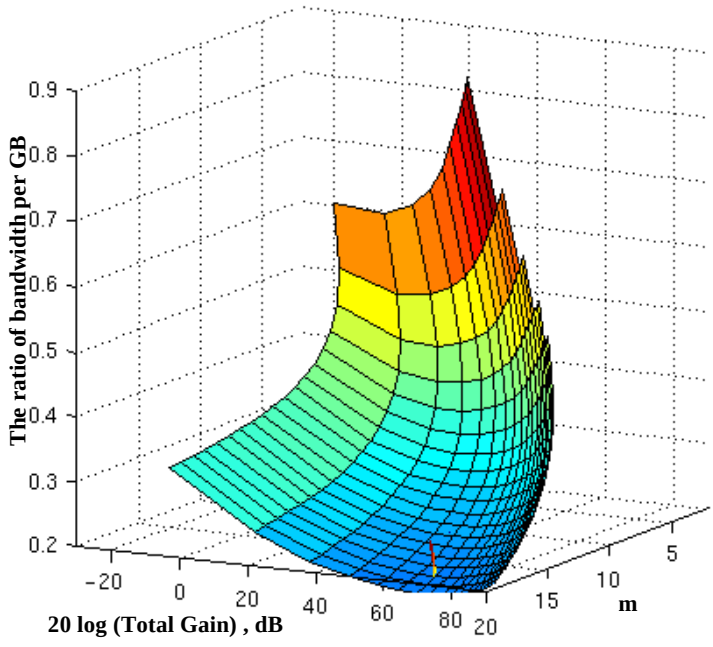
For a given technology and power dissipation, assume that the gain-bandwidth product of each amplifier stage is constant and equal to GB [23], [47]. For the CMA it can be approximated as $GB=(G+F)\omega_p$. The ratio of the acquired ω_{bw} and GB can be approximated as

$$\frac{\omega_{bw}}{GB} \approx \frac{(1+L)\sqrt{2^{1/n}-1}}{\sqrt{mL}+\sqrt{L/m}} \tag{3-53}$$

Figures 3-22 (a)-(b) show two Matlab 3D-plots of ω_{bw}/GB vs. G_T while m is swept from 2 to 20 and $1<G<10$ for the 4 and 8-stage CMA without sustaining an undesired peak (assuming >1.5dB creates a (>19%) vertical closing which is not tolerable in CDR).



(a)



(b)

Fig. 3-22 Matlab 3d-plots of the ratio of the acquired ω_{bw} and *GB* vs. total gain while *m* is changed from 2 to 20 (a) 4-stage (b) 8-stage

It can be seen that ω_{bw}/GB can be higher than 0.2 with a G_T>100, which is always less than 0.18 for a conventional MA [22]. Increasing m increases G_T and reduces the bandwidth. Fig. 3-22 (a)-(b) also show that the 8-stage CMA can give a higher gain with a lower bandwidth in comparison with that of the 4-stage CMA, when m is kept constant.

A comparison of the required L for the maximum bandwidth with no peak and 1.5dB peak for 4-, 6- and 8-stage amplifiers is presented in Table 3-1. Consequently, for a 1.5dB peak and at the expense of larger values of L and n, one can improve the bandwidth more than 4 times the bandwidth of a simple stage.

Table 3-1: A comparison of the maximum achievable bandwidth for the simple uniform 4, 6 and 8-stage CMA

	M_P=0dB		M_P=1.5dB	
	L	ω_{bw_max}/ω_p	L	ω_{bw_max}/ω_p
4-stage	1.80	1.47	6.02	2.9
6-stage	2.62	1.62	8.60	4.0
8-stage	3.80	1.83	15.50	4.6

3. Group Delay

Group delay is usually used to describe the linearity of phase response of the small signal behavior of a wideband amplifier. It is calculated from [60]

$$\tau(\omega) = -\frac{d\theta}{d\omega} \tag{3-54}$$

where θ is the phase of the gain transfer function of a wideband amplifier. As it was explained the gain transfer function of the uniform CMA can be written as multiplication of the 2nd-order transfer functions. Assuming that each 2nd-order transfer function can be written as

$$H_2(s) = \frac{G^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{3-55}$$

where ω_n and Q can be written as equations 3-26 and 3-27, respectively. From equation 3-26 and 3-27 the fol1owing equation can be obtained

$$\frac{\omega_n}{Q} = 2\omega_p \tag{3-56}$$

where ω_p is the dominant pole of each stage of the CMA. The group delay of the 2nd-order low-pass transfer function can be calculated as

$$\tau_2(\omega) = \frac{\omega_n}{Q} \frac{\left(\omega_n^2 + \omega^2\right)}{\left(\omega_n^2 - \omega^2\right)^2 + \left(\frac{\omega_n}{Q}\right)^2 \omega^2} \tag{3-57}$$

which can be written as

$$\tau_2(\omega) = 2\omega_p \frac{\left(\omega_n^2 + \omega^2\right)}{\left(\omega_n^2 - \omega^2\right)^2 + \left(2\omega_p\right)^2 \omega^2} \tag{3-58}$$

Equation (3-56) shows that the group delay is constant for $\omega << \omega_n$, approaches zero for $\omega >> \omega_n$, and reaches its maximum around $\omega = \omega_n$. Fig. 3-23(a) illustrates the Matlab plot of the group delay for the 2-stage CMA, where increasing L increases the group delay variation. This limits the usage of the entire bandwidth in wideband applications.

As explained previously, input-output transfer function of an n-stage CMA can be written as products of 2nd-order transfer functions. Therefore, the overall group delay can be written as the sum of group delays of 2nd-order sections ($\tau_i(\omega)$) as,

$$\tau(\omega) = \tau_1(\omega) + \tau_2(\omega) + \ldots + \tau_{n/2}(\omega) \tag{3-59}$$

If n is odd, delay of a 1st-order transfer function will be added to equation (3-59). Matlab plot for

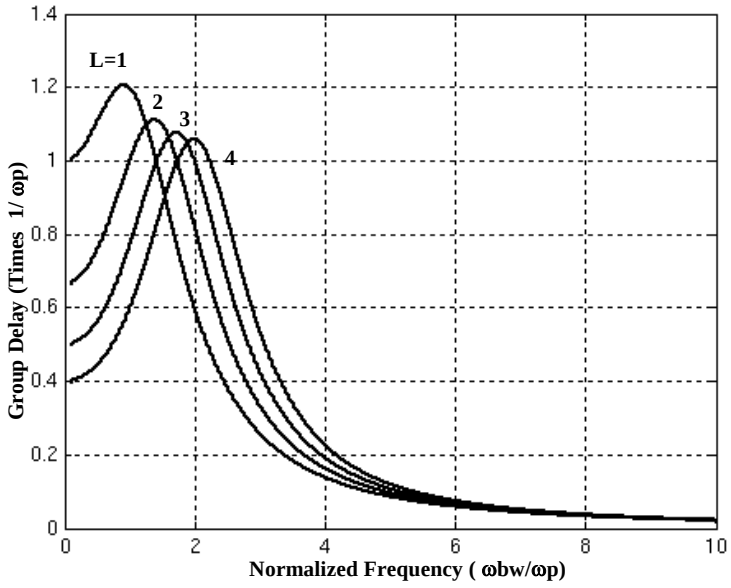
the group delay of the 8-stage CMA is shown in Fig. 3-23(b). The 8-stage CMA's input-output transfer function is the product of four 2nd-order transfer functions with group delay peaks at different frequencies. As *L* is increased, the natural frequencies of the 2nd-order transfer functions are placed far from each other, which increase the group delay variation. This problem also exists for the conventional multi-peak transfer function.

A wideband amplifier with a higher group delay variation produces more jitter. Practically a group delay variation of less than 15% can be tolerated in wideband application with a low swing signal. As it was explained in chapter I, using group delay characterization in low swing voltage is more useful because in a low swing signal the amplifier can work linearly. But in a high amplitude signal the amplifier (used in optical communication circuits) is not working linearly and analyzing group delay characterization is not that critical.

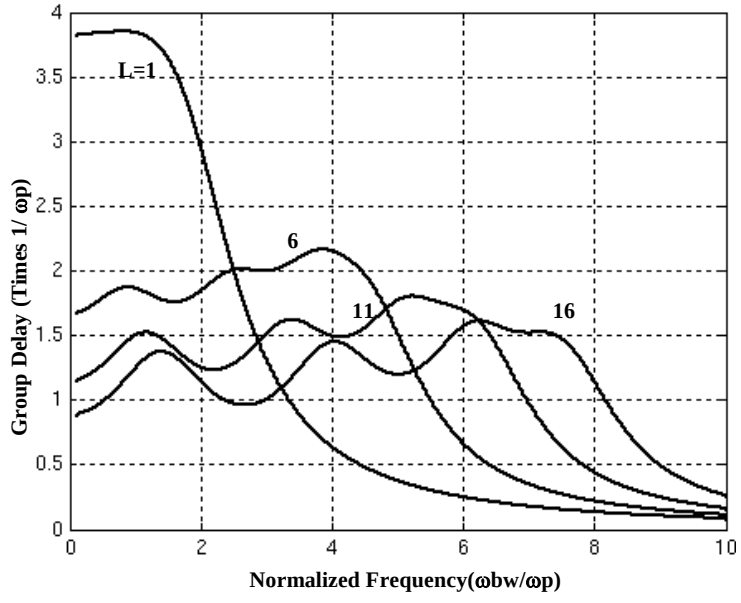
4. Sensitivity

Inaccuracy of the nominal values and the variation of the parasitic capacitances, resistors and inductors of a MA degrade performance. Imprecision due to process variation is always expected, which can cause the gain stage to malfunction [57]. Sensitivity of the overall transfer function with respect to each gain stage for the amplifier in Fig. 3-1 can be approximated as

$$S_{g_i}^{g_1 g_2 g_3}\Big|_{i=1,2,3} \approx 1 \tag{3-60}$$



(a)



(b)

Fig. 3-23 Matlab plots of group delay for (a) 2-stage topology for *L*=1, 2, 3 and 4 (b) 8-stage topology for *L*=1, 6, 11 and 16

Equation (3-60) means the variation of each stage will directly appear in the overall transfer function. For a 4-stage CMA, the amplitude's sensitivity with respect to the first forward amplifier is 1, with respect to the second and fourth forward amplifier is $(1+2L)/(1+3L+L^2)$, and with respect to the third amplifier is $L/(1+3L+L^2)$, which are smaller than 1. If the amplitude's sensitivity with respect to the feedback amplifiers is considered, all of them are between -1 and 0. Therefore, the imprecision of amplitude due to malfunction of forward amplifiers (except the first forward amplifier) is reduced.

Variation of the gain stage's parasitic capacitances, inductors and resistors of an MA shifts natural frequency and corner frequency of gain stages, thus it degrades the overall amplitude, while this variation has lesser effect on CMA's. For instance, a simple uniform 2-stage CMA has two pairs of forward amplifier and feedback amplifier. Assume each pair has different corner frequency and the CMA's transfer function can be written as:

$$H(s)=\frac{G^2\dfrac{\omega_{p2}}{\omega_{p1}}}{s^2+(1+\dfrac{\omega_{p2}}{\omega_{p1}})s+(L+1)\dfrac{\omega_{p2}}{\omega_{p1}}} \tag{3-61}$$

Sensitivity with respect to each corner frequency can be obtained from

$$S_{\omega_p}^{|H_{CMA2}(\omega)|}=\frac{\omega^2\left(\omega^2+1-L\right)}{\left(\omega^2-1-L\right)^2+4\omega^2} \tag{3-62}$$

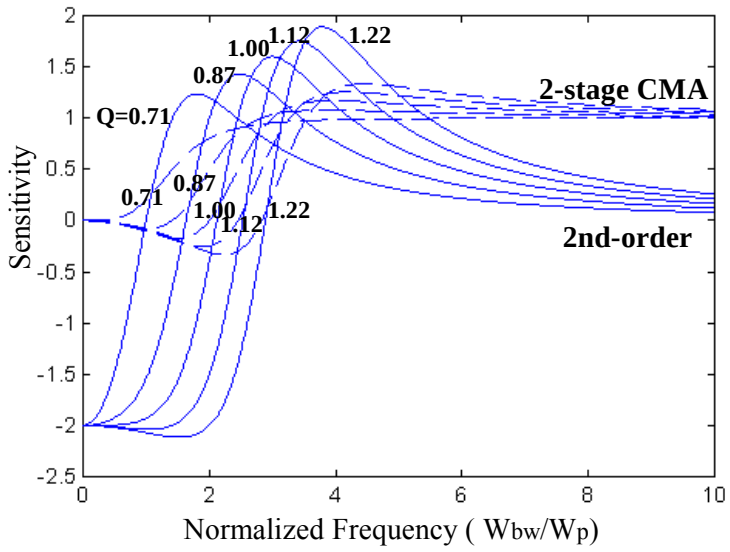


Fig. 3-24 A Matlab plot of the sensitivity of a 2-stage CMA with respect to the variation of corner frequency of one of its stages and sensitivity of a stage with 2nd-order transfer function to the variation of the natural frequency. Q= 0.707, 0.866, 1, 1.118 and 1.225

Value of equation (3-62) is smaller than the sensitivity of the gain of the 2-stage MA, $S_{\omega_{pi}}^{|g_1 g_2|}$ for the dominant pole of each stage (g_i) in Fig. 3-8, where ω_{pi} is the dominant pole frequency of stage g_i. To clarify this let us compare a 2-stage CMA with a 2nd-order low pass transfer function in which the quality factor is greater than 0.707. Consider a 2nd-order transfer function of

$$H_2(s) = \frac{\omega_n^2}{s^2 + \frac{\omega_n}{Q}s + \omega_n^2} \tag{3-63}$$

The amplitude sensitivity of the 2nd-order transfer function $H_2(s)$ can be shown as $S_{\omega_n}^{|H_2|}$. The natural frequency of the stage with a high Q depends on parasitic capacitances, resistors and inductances whose correct values are confined in accuracy of process parameters. The sensitivity of the magnitude response to the pole magnitude is

$$S_{\omega_n}^{|H_2(\omega)|} = 2 - \frac{2\left(1-\frac{\omega^2}{\omega_n^2}\right)+2\frac{\omega^2}{Q^2\omega_n^2}}{\left(1-\frac{\omega^2}{\omega_n^2}\right)^2+\frac{\omega^2}{Q^2\omega_n^2}} \tag{3-64}$$

$S_{\omega_n}^{|H_2|}$ is maximized when the frequency approaches the peak frequency of $H_2(s)$. $S_{\omega_n}^{|H_2|}$, for a high Q, depends on 2Q [57]. So having a higher quality factor increases the amplitude sensitivity of the transfer function. Fig. 3-24 shows a comparison of $S_{\omega_n}^{|H_2|}$ and equation (3-62) at different frequencies and quality factors. The figure shows that as the quality factors are increased both sensitivities increase but an amplifier with the 2nd-order low pass transfer function has more sensitivity than the 2-stage CMA's gain with respect to the local parasitic variation.

Considering a CMA's transfer function can be a product of 2nd-order transfer functions. Assuming that each 2nd-order transfer function can be written as

$$H_2(s) = \frac{G^2\omega_p^2}{s^2+\frac{\omega_n}{Q}s+\omega_n^2} \tag{3-65}$$

Equations (3-26)-(3-27) as well as equations (3-32)-(3-35) can be generalized as

$$\omega^2{}_n = (\beta+\alpha FG)\omega^2{}_p \tag{3-66}$$

$$Q^2 = 0.25(\beta+\alpha FG) \tag{3-67}$$

where α equals to 0.38 and 2.62 and β=1 for a 4-stage CMA and α=1 and β=8.29, 1, 0.426 and 0.283 for an 8-stage CMA. Assume variations of ω_p, G and F change $|H_2(\omega)|$; therefore, it can be written that

$$\frac{\partial|H_2(\omega)|}{|H_2(\omega)|} = S_{\omega_p}^{|H_2|}\frac{\partial\omega_p}{\omega_p} + S_G^{|H_2|}\frac{\partial G}{G} + S_F^{|H_2|}\frac{\partial F}{F} \tag{3-68}$$

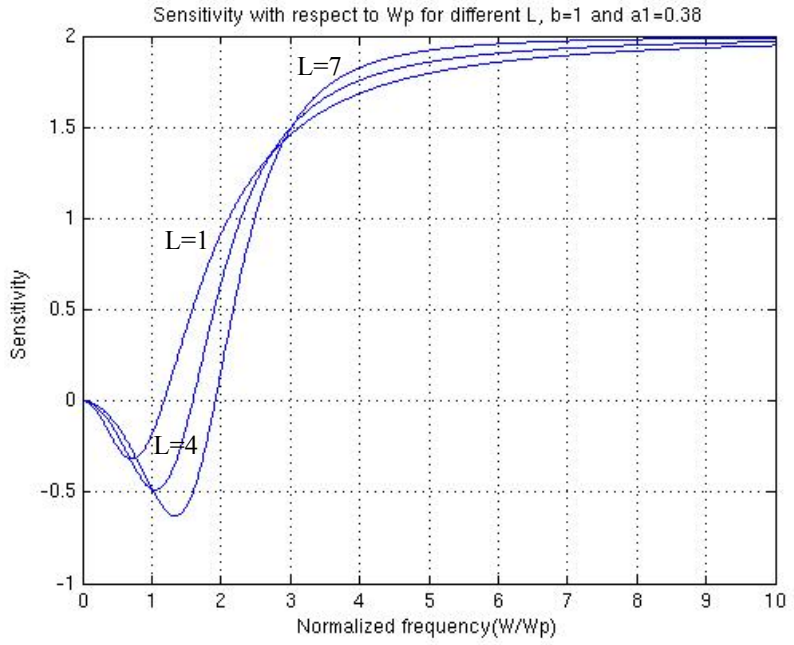
where sensitivities $S_{\omega_p}^{|H_2|}$, $S_G^{|H_2|}$ and $S_F^{|H_2|}$ can be calculated as

$$S_{\omega_p}^{|H_2(\omega)|} = 2 - \frac{2\left(1 - \frac{\omega^2}{(\beta+\alpha L)\omega_p^2}\right) + 2\frac{\omega^2}{0.25(\beta+\alpha L)^2\omega_p^2}}{\left(1 - \frac{\omega^2}{(\beta+\alpha L)\omega_p^2}\right)^2 + \frac{\omega^2}{0.25(\beta+\alpha L)^2\omega_p^2}} \tag{3-69}$$

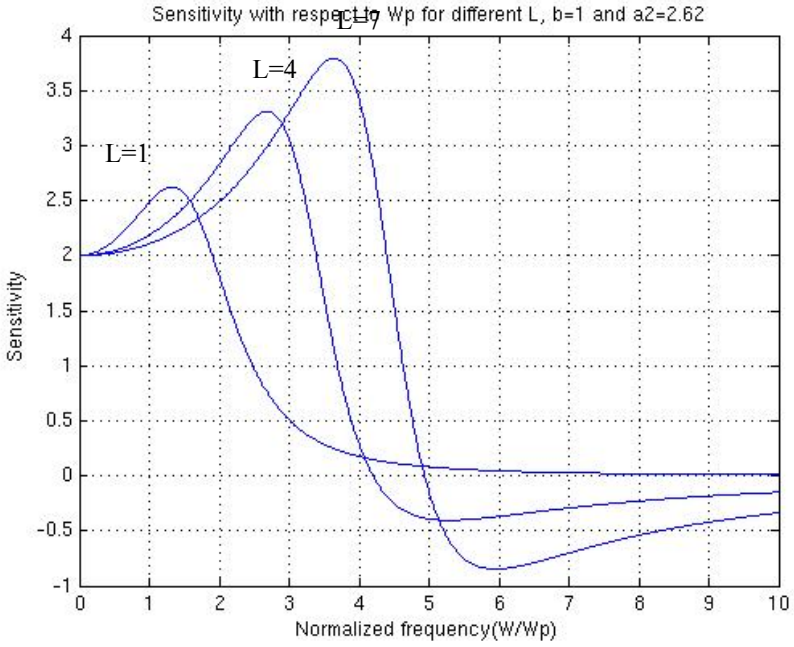
$$S_G^{|H_2(\omega)|} = 2 - \frac{\frac{\alpha L}{(\beta+\alpha L)}\left[-\frac{\omega^2}{(\beta+\alpha L)\omega_p^2}+1\right]}{\left[-\frac{\omega^2}{(\beta+\alpha L)\omega_p^2}+1\right]^2 + 4\frac{\omega^2}{(\beta+\alpha L)^2\omega_p^2}} \tag{3-70}$$

$$S_F^{|H_2(\omega)|} = -\frac{\frac{\alpha L\omega_p^2}{(\beta+\alpha L)\omega_p^2}\left[-\frac{\omega^2}{(\beta+\alpha L)\omega_p^2}+1\right]}{\left[-\frac{\omega^2}{(\beta+\alpha L)\omega_p^2}+1\right]^2 + 4\frac{\omega^2}{(\beta+\alpha L)^2\omega_p^2}} \tag{3-71}$$

respectively. In practice, the global process variations change the parasitic and parameters of amplifiers thus it change the gain of the CMA amplifier. A simulation of $S_{\omega_p}^{|H_2|}$ for two 2nd-order transfer functions of the gain of a 4-stage CMA when L=1, 4, 7 is shown in Fig. 3-25 (a)-(b).



(a)



(b)

Fig. 3-25 Sensitivity of the 2nd-order transfer functions of the gain of a 4-stage CMA with respect to ω_p when L=1, 4, 7

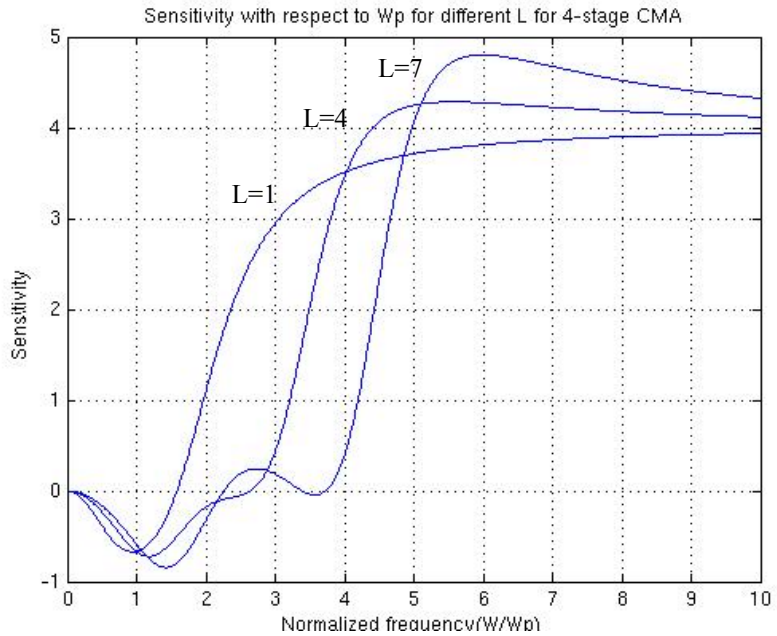
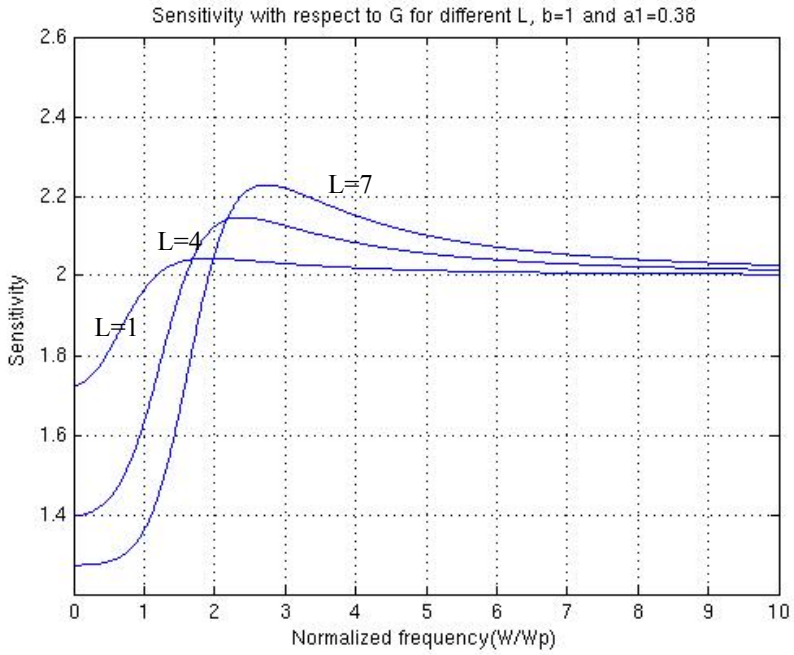
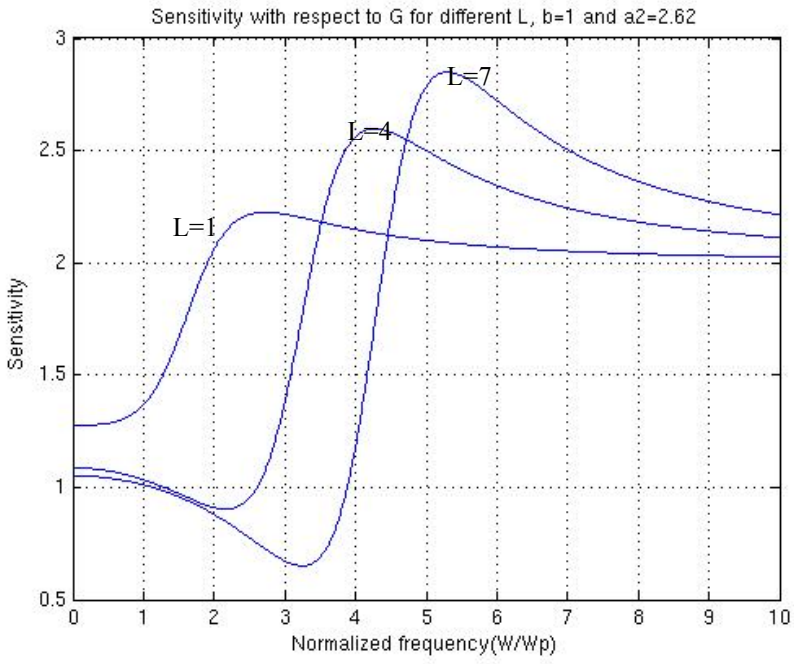


Fig. 3-26 Sensitivity of the gain transfer function of a 4-stage CMA with respect to ω_p when L=1, 4, 7

The sensitivity of the amplifier's gain with respect to ω_p is illustrated in Fig. 3-26. The sensitivity out of band is almost constant (with a variation <25%). As L increases variation in band also increases. Fig. 3-27 (a)-(b) illustrate $S_G^{|H_2|}$ for two 2nd-order transfer functions of a 4-stage CMA's gain when L=1, 4, 7. The sensitivity of the amplifier's gain with respect to G is shown in Fig. 3-28. Variation of G has less effect in the magnitude of total gain in frequencies less than corner frequency. Increasing L creates more variation in sensitivity in frequencies higher than amplifier's corner frequency. The sensitivity with respect to F, $S_F^{|H_2|}$ for is depicted in Fig. 3-29 (a)-(b) for two 2nd-order transfer functions of a 4-stage CMA's gain when L=1, 4, 7. Fig. 3-30 shows the simulation results of the amplifier's gain with respect to F. As it shows the amplifier's gain has less sensitivity to process variation in die area of feedback amplifiers.



(a)



(b)

Fig. 3-27 Sensitivity of the 2nd- order transfer functions of a 4-stage CMA's gain with respect to *G* when *L*=1, 4, 7

Assuming that forward amplifiers and feedback amplifiers are matched and variations of *G* and *F* are equal; Fig. 3-31 illustrates the sensitivity of the amplifier's gain with respect to changes F and G together. The sensitivity in Fig. 3-31, in comparison with Fig. 3-28 is reduced.

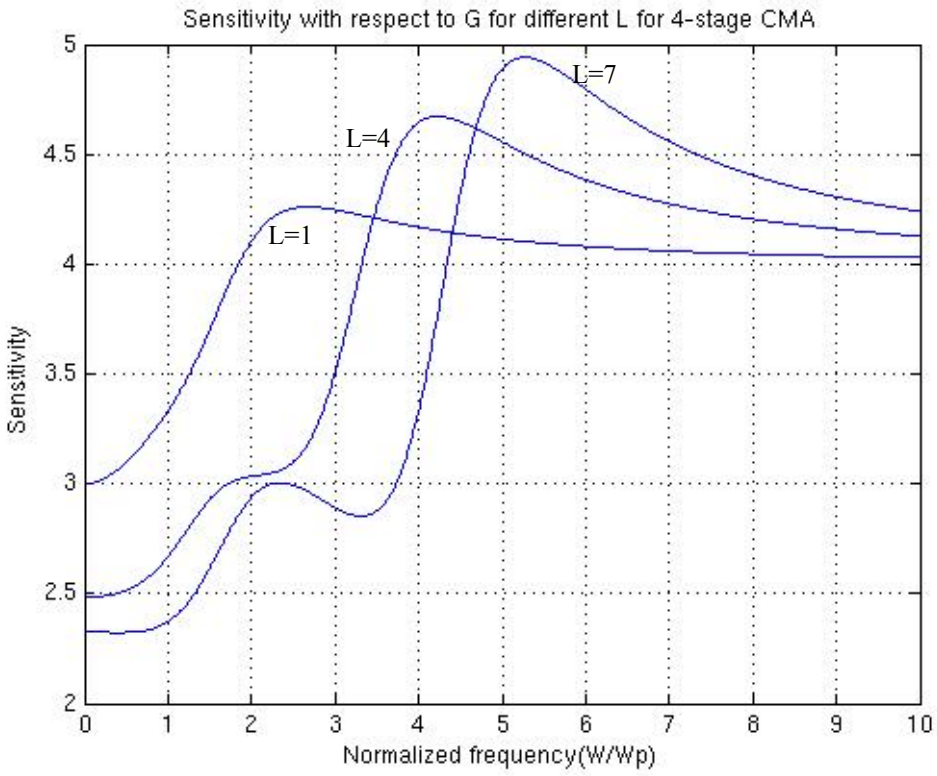
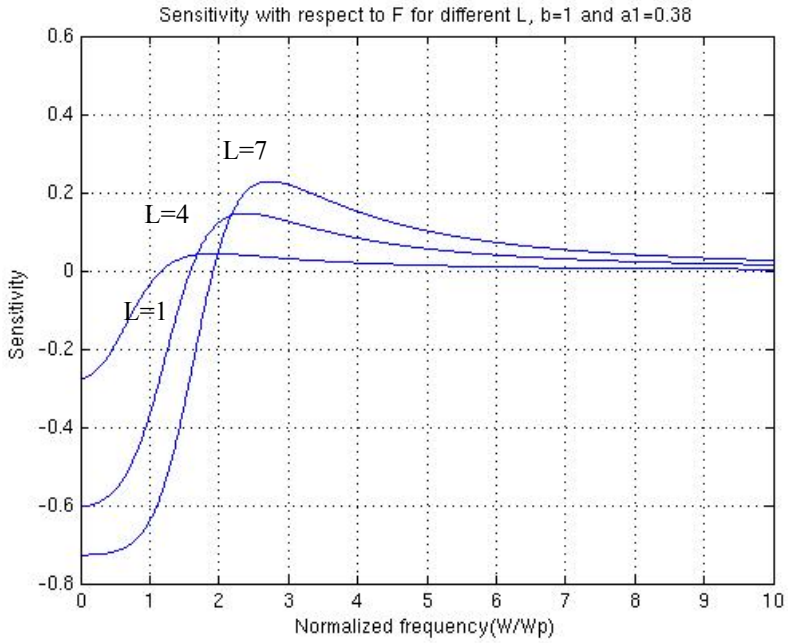


Fig. 3-28 Sensitivity of the gain of a 4-stage CMA with respect to *G* when *L*=1, 4, 7



(a)

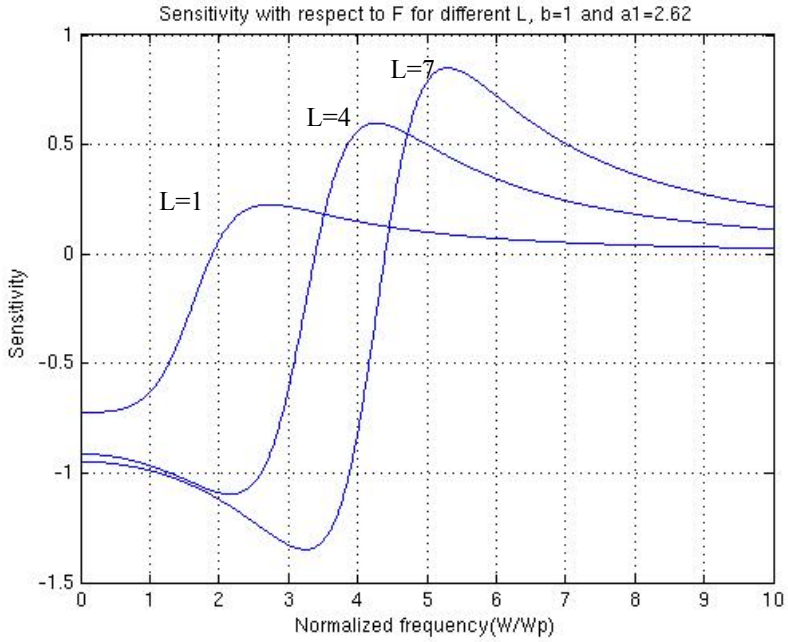


Fig. 3-29 Sensitivity of the 2nd- order transfer functions of a 4-stage CMA's gain with respect to *F* when *L*=1, 4, 7

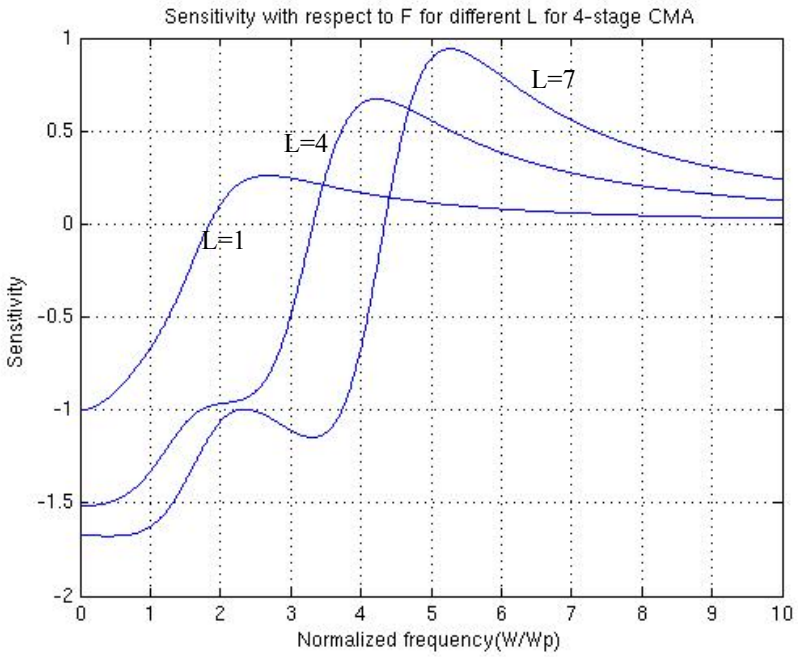


Fig. 3-30 Sensitivity of the transfer function of a 4-stage CMA's gain with respect to *F* when *L*=1, 4, 7

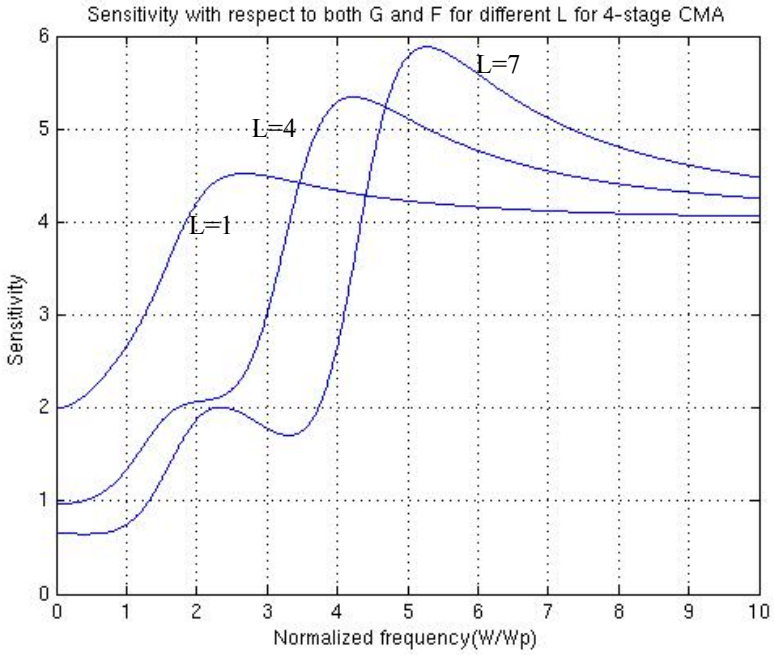


Fig. 3-31 Sensitivity of the transfer function of a 4-stage CMA's gain with respect to *F* and G (when they have the same variation) when *L*=1, 4, 7

5. Stability

Stability of the CMA was analyzed at the macro-model level using several criteria. First, the Routh-Hurwitz criterion shows that for $L>0$, the denominator polynomial do not have poles with a negative real part that insures stability for the entire frequency range [58]. Second, the step response of the input-output transfer function for $L>0$, while peaking is kept below 1.5dB, shows that the CMA is stable. Third, the phase responses of all opened loops for $L>0$ have a minimum phase margin of 45^{o}. To investigate the effect of the second pole of $g(s)$ and $f(s)$ on stability, the second pole (real pole) is shifted from $3\omega_p$ to $10\omega_p$. With the peaking kept below 1.5dB, the Routh-Hurwitz criterion, step response and phase margin of loops are checked again. For different values of n, only the phase margin test puts some limitations on the second pole, depending on the value of L. Furthermore, the local and global variations of L and ω_p by more than 25% didn't produce any instability when $L>0$. To test stability of the transistor-level circuit implementation of the topology, a 3Gbit/Sec random signal is amplified by the CMA for different values of L. To measure the stability of amplifier when the global and local processes variations are occurred, the transistor level circuits of CMA are further simulated. In chapter IV the obtained results are discussed.

6. Noise

Adding active components to an amplifier produce more noise; hence, using CMA's topology is expected to increase the noise spectrum density. The value of input referred noise fictitiously sets the minimum amplitude of signal, which can be amplified by a multistage amplifier. All stages contribute in this value. Nonetheless, the equivalent of noise of the first stages is more effective in the overall input referred noise. In CMA the noise of the first stage is scaled down (with $1/g^2(j\omega)$). The other stages' noise is further scaled down. For instance, the input referred noise of a 4-stage CMA is

$$\overline{n_{in,r,n=4}^2} = \frac{\left(\overline{n_g^2} + \overline{n_f^2}\right)}{\left(g(j\omega)\right)^2}\left[1 + \frac{1}{\left(g(j\omega)\right)^2} + \frac{\left(1+L(j\omega)\right)^2}{\left(g(j\omega)\right)^4}\right] + \frac{\left(1+2L(j\omega)\right)^2}{\left(g(j\omega)\right)^8}\overline{n_g^2} \tag{3-72}$$

assuming that each stage produces a noise spectral density of $\overline{n_g^2} + \overline{n_f^2}$ where $\overline{n_g^2}$ and $\overline{n_f^2}$ are the noise spectral density of the forward amplifier and the feedback amplifier, respectively. Only the last stage has a noise of $\overline{n_g^2}$.

In a comparison with the noise of a four stage of MA, it can be written that

$$\frac{\overline{n_{in,r,n=4}^2}\Big|_{CMA}}{\overline{n_{in,r,n=4}^2}\Big|_{MA}} = \frac{\frac{\left(\overline{n_g^2} + \overline{n_f^2}\right)}{\overline{n_g^2}}\left[1 + \frac{1}{\left(g(j\omega)\right)^2} + \frac{\left(1+L(j\omega)\right)^2}{\left(g(j\omega)\right)^4}\right] + \frac{\left(1+2L(j\omega)\right)^2}{\left(g(j\omega)\right)^6}}{1 + \frac{1}{\left(g(j\omega)\right)^2} + \frac{1}{\left(g(j\omega)\right)^4} + \frac{1}{\left(g(j\omega)\right)^6}} \tag{3-73}$$

Equation 3-73 can be further approximated as

$$\frac{\overline{n_{in,r,n=4}^2}\Big|_{CMA}}{\overline{n_{in,r,n=4}^2}\Big|_{MA}} \approx 1 + \frac{\overline{n_f^2}}{\overline{n_g^2}} \tag{3-74}$$

Consider the case where thermal noise is superior to the other noise sources, such as flicker noise, shot noise, thus $\overline{n_g^2} / \overline{n_f^2} < m$. In the worst case $\overline{n_g^2} / \overline{n_f^2} \approx m$, therefore the input referred noise is increased by 1/*m* times that of the MA's. Since *m* is practically higher than 5, using active feedback doesn't increase the noise by more than 20%. In the next chapter a circuit simulation is reported where the obtained noise is much less than 20%.

CHAPTER IV

IMPLEMENTATION OF CMA TOPOLOGY

A Designing an n-*stage CMA*

To design an *n*-stage CMA, assume that *F, G* and $\omega_{p,}$ are defined based on the parameters of the small signal models of stages' circuits (that will be explained later), and their limitations such as, the maximum available DC forward gain and DC feedback gain (depending on the technology) are specified.

The wideband amplifier is designed for a given set of specifications such as bandwidth, overall gain, technology, and power dissipation. Depending on technology and application of amplifier, the tolerable peak in transfer function and the tolerable ripple of the group delay are specified. The procedure of the design is carried out according to the following steps:

1. For the specified technology and power (or current) consumption, the achievable gain bandwidth product of amplifier stages (*GB*) is approximated.
2. Amplifier circuit for a stage of CMA is chosen.
3. The ratio of ω_{bw} to *GB* is calculated.
4. Initially, it is assumed that a 2-stage CMA can satisfy the required specifications.
5. For the number of stages (*n*), the ratio of ω_{bw}/GB vs. G_T is extracted (from Matlab simulation or macro model simulation) while all limitations of parameters are considered.
6. If ω_{bw} and G_T cannot be achieved step 7, otherwise step 8 will be followed.
7. The number of stages (*n*) is increased and step 5 is repeated. If the number of the required stages is not reasonable or power consumption is not desirable, changing the type of stages is suggested and the steps from step 4 must be followed.
8. From the number of stages (*n*) and the minimum *G* (from step 6), the DC gain of feedback

amplifier and the transistors' dimensions can be calculated.

These eight steps are illustrated in the flow chart in Fig. 4-1.

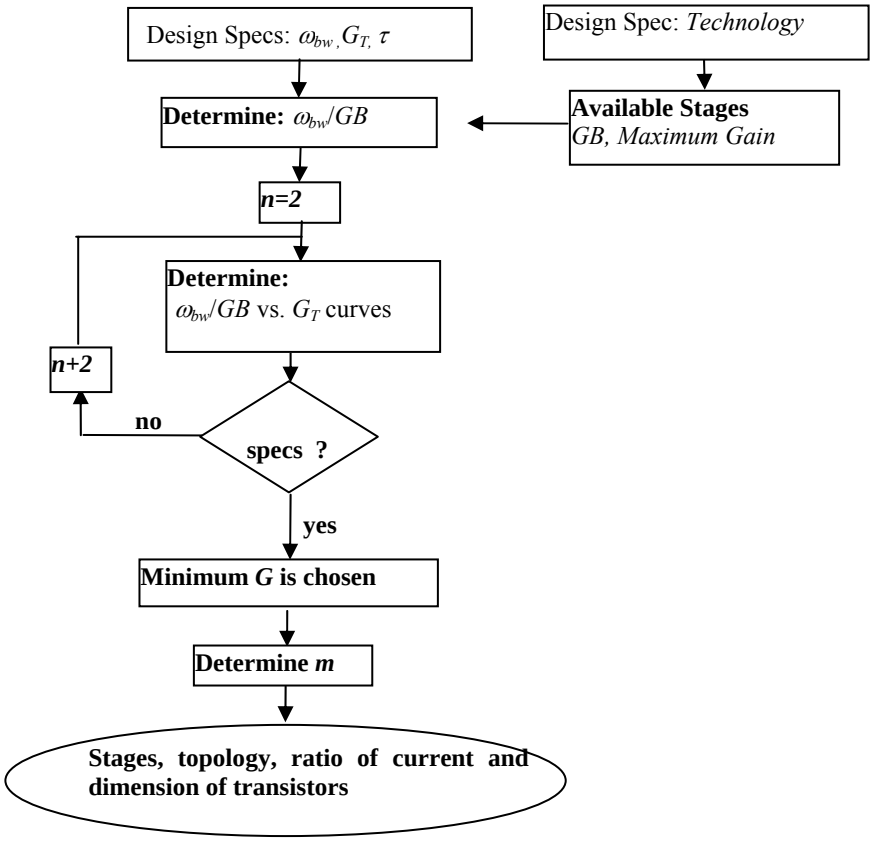


Fig. 4-1 Design flow chart of the CMA

B Realization of the Uniform CMA

1. Amplifier Stages

The amplifier stage of the CMA is composed of two operational transconductance amplifiers (OTAs) g_{mg} and g_{mf} and load resistors R_Ls, as illustrated in Fig. 4-2. The output voltage of the stage is calculated from

$$V_o = g_{mg} R_L V_g - g_{mf} R_L V_f \tag{4-1}$$

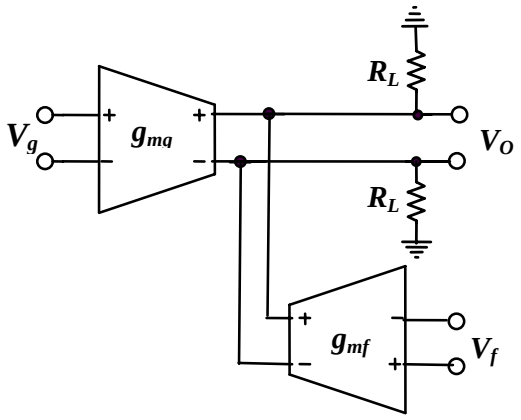


Fig. 4-2 CMA's single stage implementation

For wideband applications, amplifier stages must be fast with minimum area. Implementation of stages as differential amplifiers gives more immunity for external noise and suppresses common DC level [59]. Two possible candidates for such amplifiers are illustrated in Fig. 4-3. Paired transistor M_g forms the forward amplifier input stage, whereas M_f pair is used for feedback amplifier inputs. The minimum size of the transistors must be used to reduce parasitic capacitance. DC gains of forward amplifier and feedback amplifier are calculated from $G=g_{mg}R_O$ and $F=g_{mg}R_O$, respectively, while g_{mg} is the transconductance of M_g, g_{mf} is the transconductance of M_f, and R_O is the output impedance of the stage. If $I_f \ll I_g$ in Fig. 4-3(b), current I_f can be used to control F so that the change of the DC voltage level at the output nodes can be neglected.

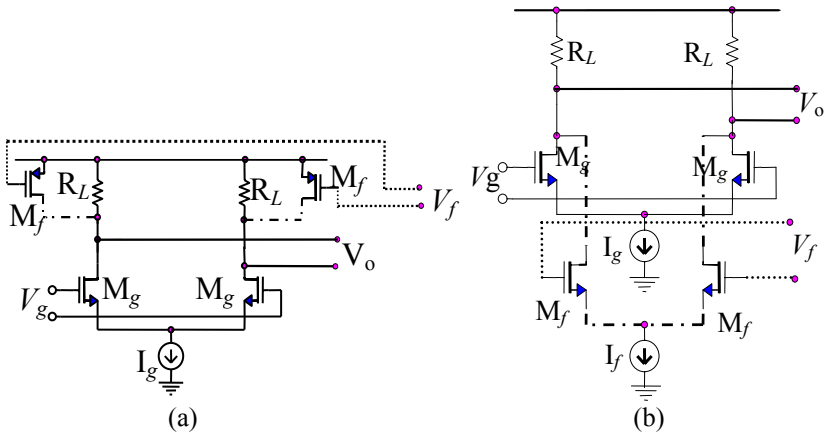


Fig. 4-3 Examples for circuits of stages of a simple *n*-stage CMA (a) with non-controllable feedback amplifier (b) with controllable feedback amplifier

Fig. 4-4 illustrates the connection of stages of the CMA.

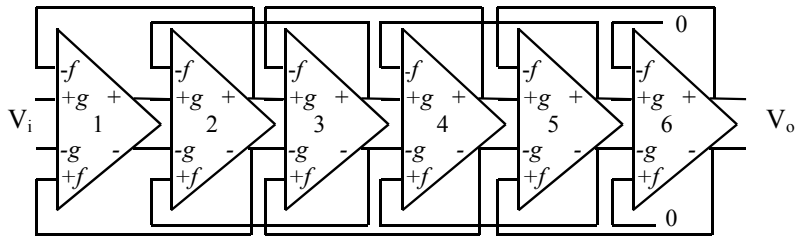


Fig. 4-4 Circuitry of a 6-stage CMA

The output signals of each stage drive the inputs of the forward amplifiers of the next stage and inputs of the feedback amplifiers of the previous stage. The feedback amplifier of the last stage has zero inputs. Fig. 4-5 depicts the small signal model for an *n*-stage CMA, where R_O and C_{eq} are resistance and equivalent capacitance, respectively, of the output node of the amplifier stage. For this case, $F=g_{mf}R_O$, $G=g_{mg}R_O$ and $\omega_p=1/R_OC_{eq}$. The ratio of DC forward gain and DC feedback gain of each stage can be calculated as $m=G/F$ or $m=g_{mg}/g_{mf}$. For instance, in Fig. 4-3(b) if $(W/L)_g=(W/L)_f=(W/L)$, DC loop gain (L) and m can be obtained from

$$L = FG = 2\mu C_{ox} \frac{W}{L} \sqrt{I_g I_f} R_O{}^2 \tag{4-2}$$

$$m = \sqrt{I_g / I_f} \tag{4-3}$$

So one can employ I_f to control L and m; the two main parameters of the design of the CMA.

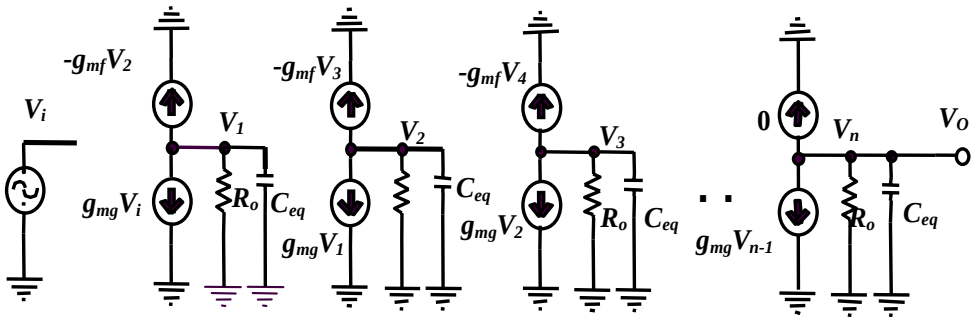


Fig. 4-5 Small signal circuit of a simple uniform n-stage CMA with $G=g_{mg}R_o$ and $F=g_{mf}R_o$

2. Reducing the Miller Effect of Gate-Drain Capacitance of Transistors

In cascaded circuits, the dominant poles are usually placed at the output nodes of individual amplifier stages. Fig. 4-6(a) shows two stages of a conventional MA, where $(1+g_mR_L)C_{gd}$ (the Miller effect of gate-drain capacitance of Mg) will be paralleled with the output capacitance of the first stage at the nodes x and y. Increasing the gain increases the Miller effect of C_{gd} thus degrades the bandwidth of the stage; therefore it reduces the overall bandwidth of MA. Reducing this capacitance enhances the bandwidth. To use this amplifier for a wider bandwidth, DC gain must be reduced.

Employing the feedback amplifier adds extra parasitic capacitances to each output node of stage amplifier. However, the feedbacks in the CMA topology somewhat reduce the parasitic capacitance of output nodes. Consider the 2-stage CMA in Fig. 4-6(b), which is implemented in transistor level as shown in Fig. 4-6(c). The feedback loop formed by M_{g21}, M_{g22}, M_{f11} and M_{f12}

is separately shown in Fig. 4-6(d). The output voltage at the node o_1 can be given as

$$V_{o1} \approx -\left(G_T\right)^{1/n} V_x \tag{4-4}$$

Thus a capacitance of $(1+(G_T)^{1/n})\ C_{gdg21}$ will appear at the node x. Similarly, V_{o2} can be obtained as

$$V_{o2} \approx \left(G_T\right)^{1/n} V_x \tag{4-5}$$

which causes an additional capacitance of $(1-(G_T)^{1/n})\ C_{gdf12}$ to appear at node x. This capacitance is a negative capacitance and it reduces the Miller effect of C_{gdg21}. Due to symmetry, similar capacitance values can be found for node y.

To remove the Miller effect of C_{gdg21}, W/L ratio of M_{f12} must be as large as that of M_{g21}. To have a high G, W/L of M_{g21} and M_{g22} is enlarged. To reduce the capacitance at nodes x and y, sizes of M_{f11} and M_{f12} must also be increased. However, using large transistors increase drain-bulk junction and gate-source capacitances; therefore, they are avoided at the input stage of forward and feedback amplifiers.

One problem with the amplifier in Fig. 4-3(b) is that the two transistors M_f and M_g cannot work at the maximum speed; since their drain currents are not equal (one of them can work in high f_T). Although the CMA structure reduces the capacitance at the output nodes, the effect of extra parasitic can only be removed partially. Besides, C_{eq} of the last stage is larger than those of other stages because the last stage does not have a negative capacitance at the output node and is loaded by a buffer capacitance, which degrades the overall bandwidth [46]. To increase the accuracy of the design procedure, the dominant pole of the last stage can be modeled as a fraction of ω_p.

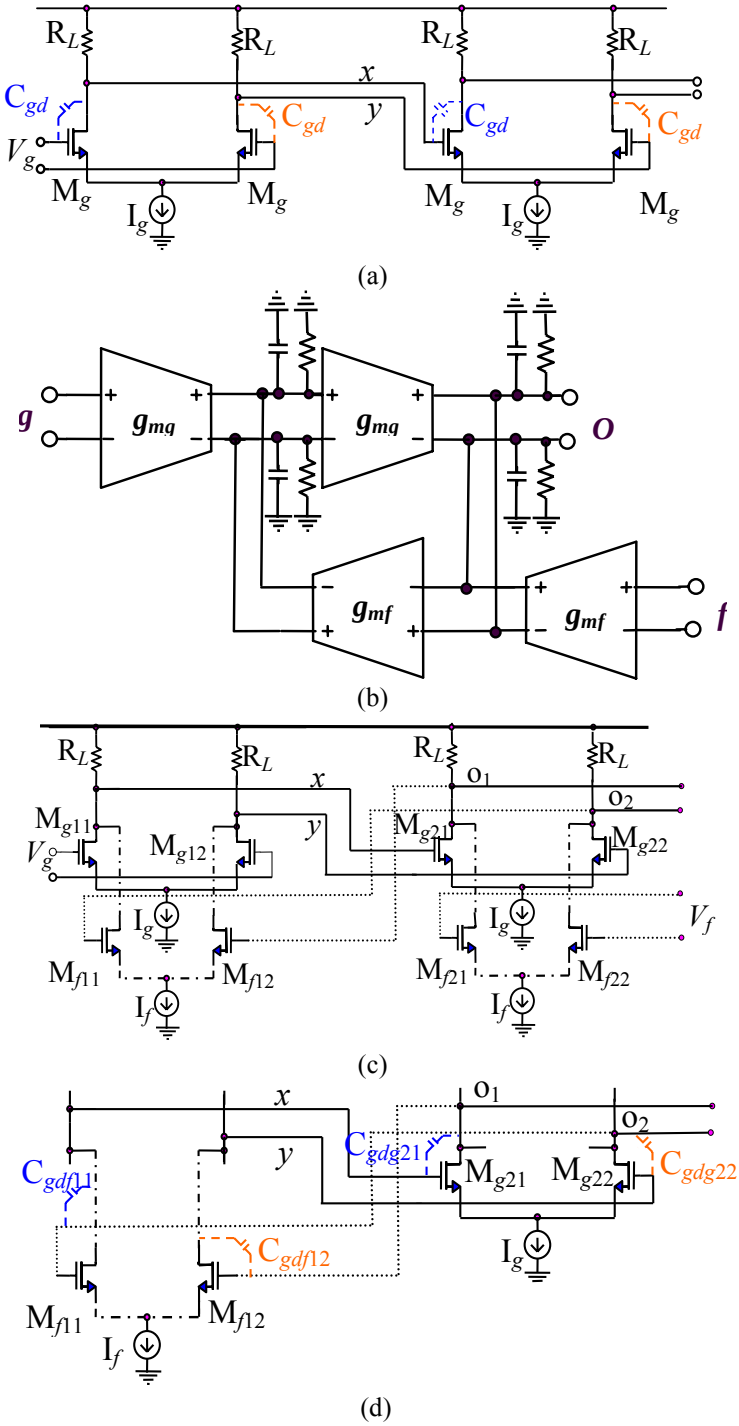
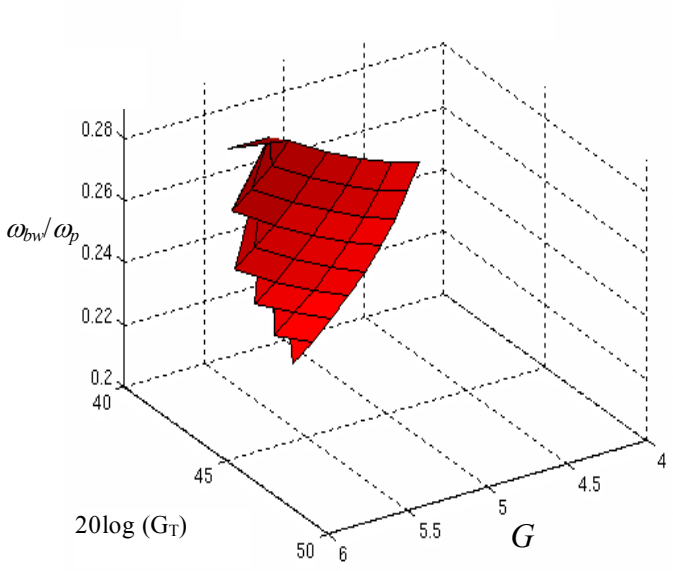


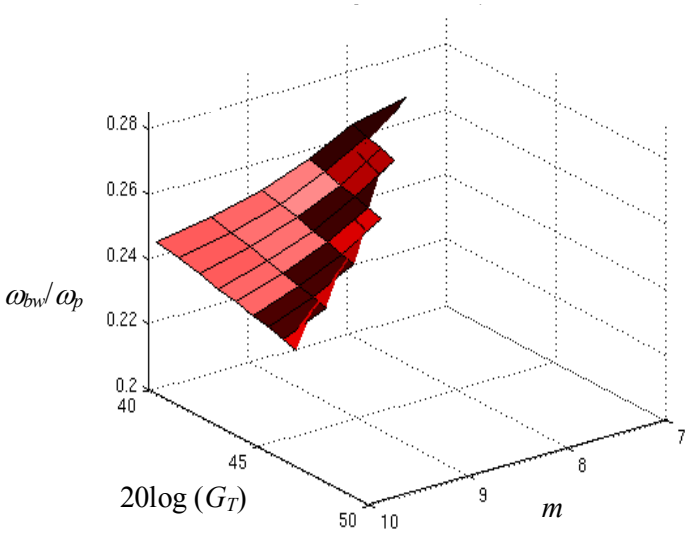
Fig. 4-6 Miller capacitances of gate-drain in an MA and a CMA (a) two stage of an MA (b) two stage of a CMA with output node capacitance of stages (c) a circuit implementation of two stages of CMA (d) a loop of circuit in (c)

3. Design and Implementation of the First 6-stage Uniform CMA

Let us design a CMA with a gain more than 100 and a bandwidth more than 1.4GHz while the



(a)



(b)

Fig. 4-7 A Matlab plot of ω_{bw}/GB vs. G_T for the 6-stage CMA while group delay's ripple is less than 8% for (a) varying G (b) varying m

ripple of the in-band group delay is less than 8%. The amplifier circuit in Fig. 4-3(b) will be used for the stages. Assume that the extra parasitic capacitances of the feedback amplifier and those of the last stage reduce *GB* to about $f_t/2$. The design steps can be listed as follows: (I) Define the limitations: $\omega_{bw}/GB>0.2$, $1<G<10$, $G_T>100$ and $m>2$, (II) Initialize $n=2$, (III) Calculate *L* from the available range of *G* and *m*, and obtain G_T from equation (3-5). Extract ω_{bw}/GB from equation (3-48) and extract the group delay from equations (3-52) and (3-53). Compute the percentage of the group delay variation from

$$\gamma = 2\frac{\tau_{\max}(\omega)-\tau_{\min}(\omega)}{\tau_{\max}(\omega)+\tau_{\min}(\omega)} \tag{4-6}$$

(IV) Increment *n* and repeat step (III) if there is no overlapping area for the required parameters. For $n=6$, all specifications are achieved and a region as in Fig. 4-7 (a) and (b) is the answer. For $4.2<G<5.7$ and $7.5<m<10$, the 6-stage CMA can give a gain more than 100 and a bandwidth more than 1.4GHz. (V) Obtain the maximum f_T for 0.35μm CMOS technology resulting in V_{GS}-V_{th}=0.5V.

The designed circuit was combined with a buffer to drive a 50Ω load in parallel with a 1pF capacitor at 3.3V single power supply. The parameters in Table 4-1 were used for the 6-stage CMA. The amplifier was fabricated using TSMC 0.35μm CMOS technology. Fig. 4-8 shows the simulated and measured gain of the amplifier. Group delay simulation and measurement is illustrated in Fig. 4-9. Group delay reaches its peak at a frequency higher than 2GHz in simulation, and at 1.5GHz in measurement. The simulation and the measurement results of the chip are summarized in Table 4-2. Poor performance of the buffer and effects of parasitic components degrade the bandwidth of the amplifier, also lowering the accuracy of the measurement at frequencies higher than 3GHz.

During the simulations and measurements, the value of I_g was kept constant around

2mA, and I_f was swept from 5μA to 500μA (see Fig. 4-3(b)). When I_f is increased, the drain-source resistor (r_{dsf}) of M_f is reduced, which decreases the output resistance of the amplifier stage and degrades G. At the same time, ω_p is also decreased due to increased parasitic capacitances. Fig. 4-10 illustrates the simulated and measured results of G_T and f_{-3dB} as a function of $\sqrt{I_f}$. The magnitude of the gain for different I_f=0, 45μA and 246μA are illustrated in Fig. 4-11. The chip microphotograph is shown in Fig. 4-12.

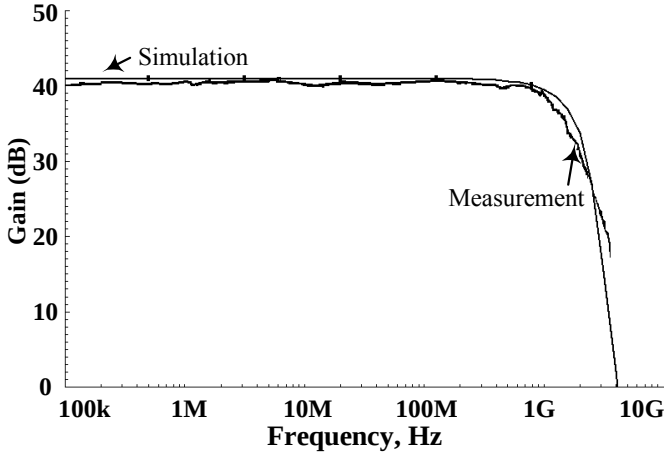


Fig. 4-8 Gain of the 6-stage CMA using the amplifier in Fig. 4-3(b) in 0.35μm CMOS

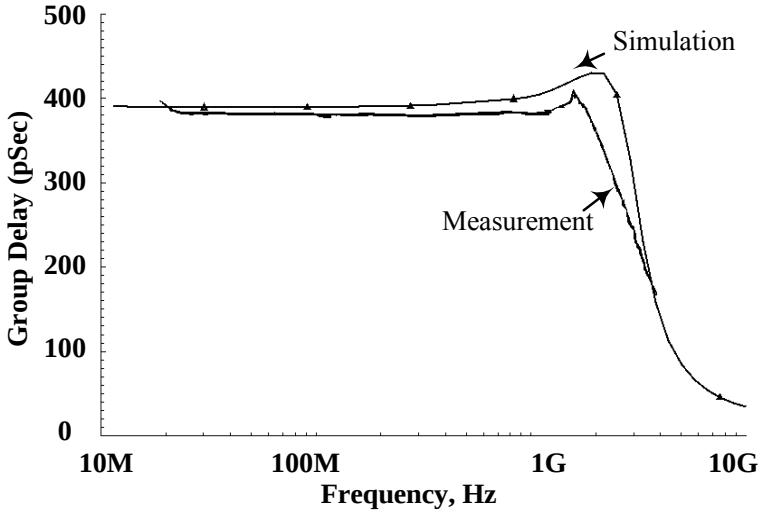


Fig. 4-9 Group delay of the 6-stage CMA using the amplifier in Fig. 4-3(b) in 0.35μm CMOS

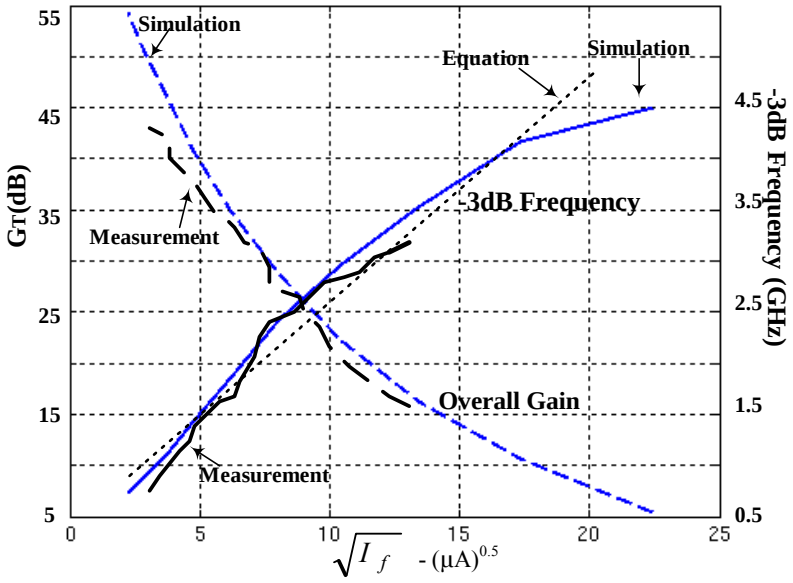


Fig. 4-10 Transistor level simulation of the overall gain and the bandwidth of the 6-stage CMA using the circuit in Fig. 4-3(b) as the amplifier stage, I_f is swept from 5uA to 500uA while I_g=2mA and G=4

Table 4-1: Parameters of the 6-stage CMA (stages are shown in Fig. 4-3 (b))

Parameters	Values
M_g	W/L=60
M_f	W/L=60
R_L	1.25KOhms
Load Transistor	2(W/L=300)

Table 4-2: The designed results of the 6-stage CMA (stages are shown in Fig. 4-3(b))

Parameters	Simulation	Measurement
f_{-3dB}	1.4GHz	1.3GHz
Group Delay Ripple in Band	22pS	20pS
Gain	40.8 dB	40dB
I_f	24μA	34μA
Power Consumption	39.6mW	38.3mW

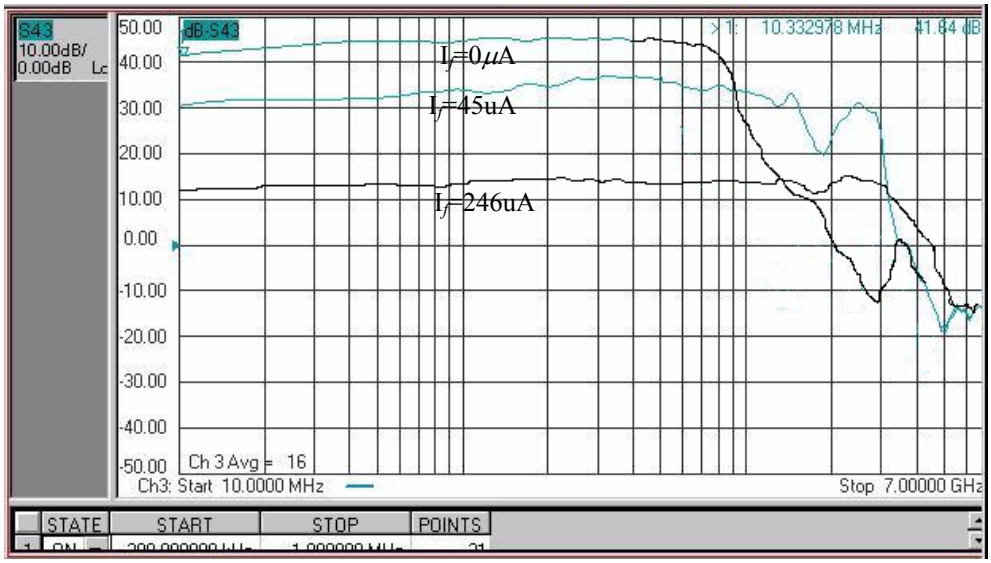


Fig. 4-11 The magnitude measurement for I_g=2mA while I_f is changed

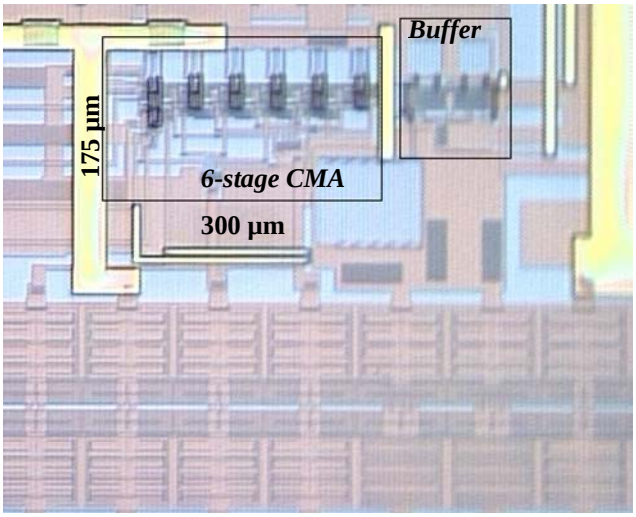


Fig. 4-12 The first 6-stage CMA's die microphotograph

The eye diagram measurement results of pseudo-random data (2^{31}-1 pseudo-random data) for the minimum and the maximum input swing voltage (10mV and 1V; respectively), when I_g=3mA, are shown in Fig. 4-13 (a) and (b). To reduce the jitter, when there is a high swing voltage, I_f is increased and gain is adjusted. This is shown in Fig. 4-13(c). To have a BER lower than 10^{-12} the bandwidth must be enough. BER cannot be reached in a low voltage and the lowest voltage is 10mV.

Using the proposed amplifier topology with I_g≈3mA, 38dB overall gain and 2.3 GHz bandwidth could be achieved, while the peak–to–peak jitter for 2.5Gb/Sec (2^{31}-1 pseudo-random) bits is less than 150pS at 10mV input voltage and 200pS at 1V peak-to-peak input voltage. In terms of jitter, power consumption, and occupied chip area, the CMA topology is considerably better than a recent paper which reports a non-uniform peaking technique in 0.35µm CMOS process [44], and it is comparable with a report presenting a uniform MA in 0.18µm CMOS [60].

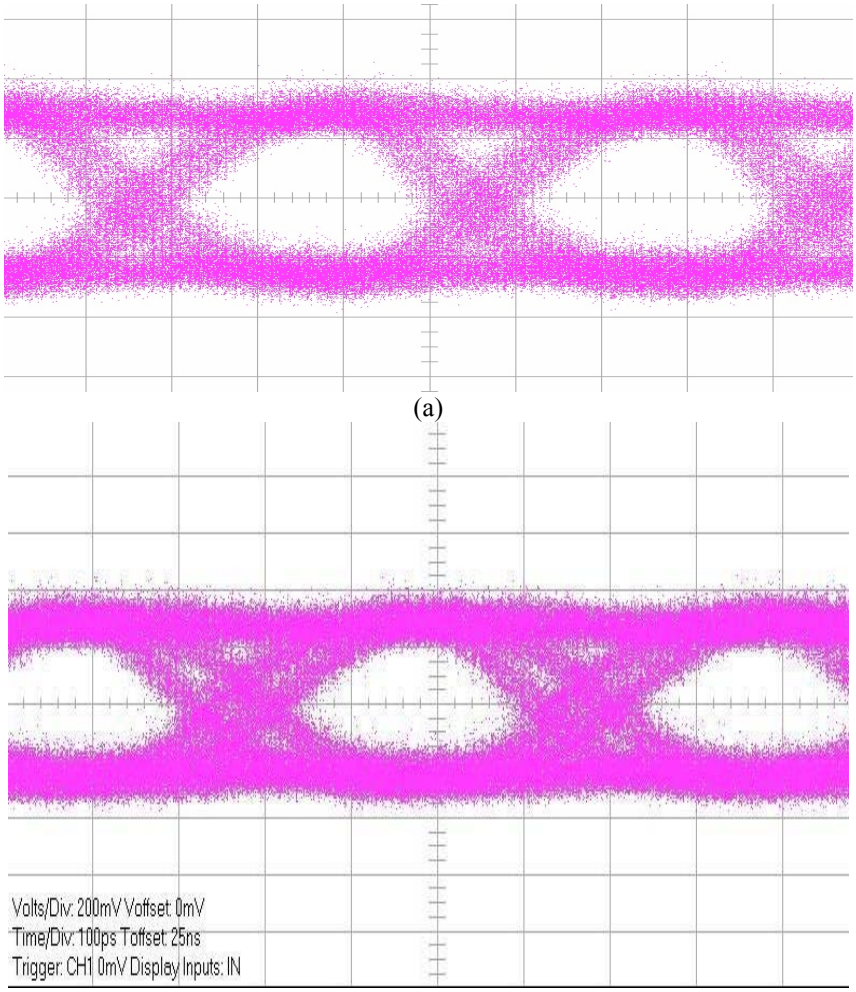


Fig. 4-13 Eye diagram measurement results of the 6-stage CMA for I_g=3mA and (a) 10mV peak-to-peak input voltage (b) 1V peak-to-peak input voltage.

4. Sensitivity Simulation

To investigate the sensitivity of CMA to mismatch and process variations, two sets of simulations were performed. The first set covers the local variations and mismatches for R_L, M_g and M_f components in Fig. 4-3(b). The mismatch produced in each stage causes offset, degrades the gain and high frequency performance of the amplifier. However, due to feedback used in the CMA topology, the offsets are reduced. The offset generated in the last stage has minimum

effect on the overall performance; therefore, R_L, M_g and M_f of the first five stages of the 6-stage CMA were varied within ±5%. The performance of the amplifier is not degraded by mismatching M_f transistors when I_f is very low. However, mismatches in M_gs and R_Ls especially in the first stages degrade the performance of the CMA, as also expected in MA.

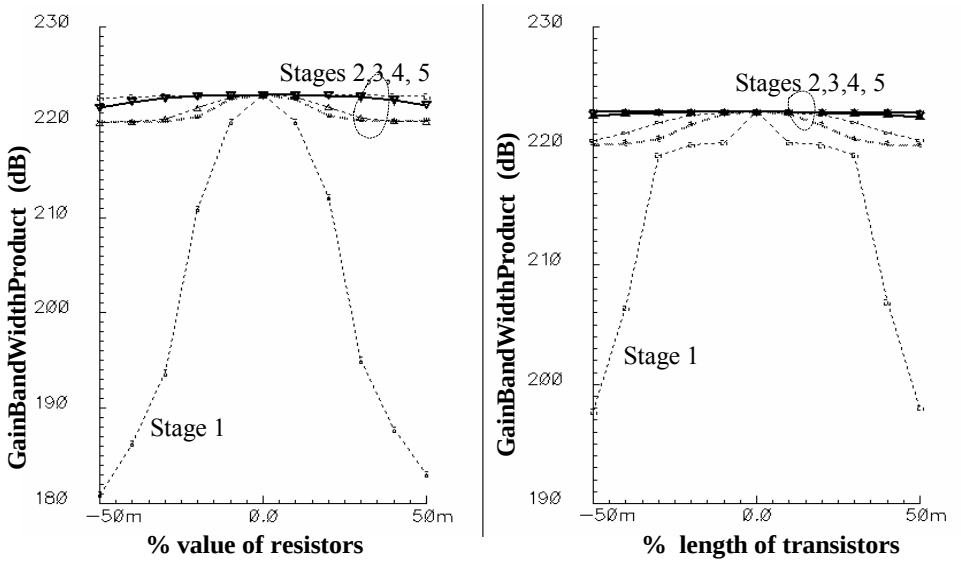


Fig. 4-14 Transistor level simulation results of the gain bandwidth product of the 6-stage CMA using the circuit in Fig. 4-3(b) as the amplifier stage, I_f =24μA, I_g=2mA and G=4 while a mismatching of between pair load resistors and length of paired transistors from stage 1, 2, ..,5, were swept from-5% to 5%. Mismatching in (a) resistors (b) transistors

Fig. 4-14 illustrates the gain bandwidth product of the amplifier where a mismatch is introduced to different stages. The second set covers larger variations in the die, which affect matching among different stages. As expected, matching M_g (and also M_f) across different stages does not affect the performance of the amplifier as long as they are matched within one stage. On

the other hand, mismatch of R_L resistors between amplifier stages causes the common-level voltage of each stage to be different, which degrades the performance. Fig. 4-15 (a) and (b) show the simulation results of gain bandwidth product of the amplifier while the value of load resistors (R_L) and length of transistors (M_g) are varied. Increasing R_L of the first stage shifts its dominant pole to a lower frequency, which directly affects the performance of the amplifier, as also expected for a conventional MA.

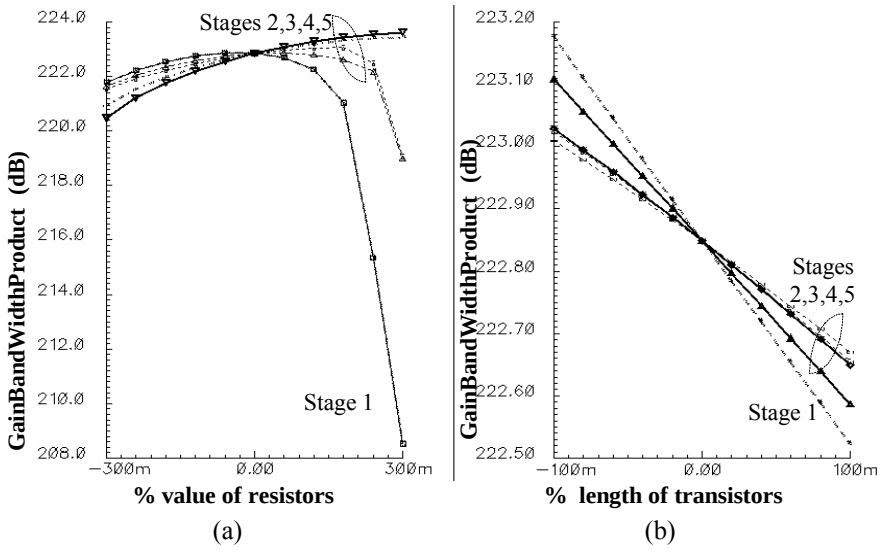


Fig. 4-15 Transistor level simulation results of the gain bandwidth product of the 6-stage CMA using the circuit in Fig. 4-3(b) as the amplifier stage, I_f=24μA, I_g=2mA and G=4 while the varying between load resistors and length of transistors from stage 1, 2, ..., 5 were swept from-30% to 30% and -10% to 10%. Variation in (a) resistors (b) size of transistors

5. Noise Simulation

To investigate the noise produced by CMA amplifier, I_f of an 8-stage CMA amplifier was swept from 0 to 560uA and the input voltage referred noise was measured. Figure 4-16 shows the

results of the spectral density of the input voltage referred noise. In this simulation *m* was changed from infinite to 7.4 and the measured noise is changed from 1.47 V/(Hz)$^{0.5}$ to 1.62 V/(Hz)$^{0.5}$. The added noise is less than $1/m^{0.5}$ (per (Hz)$^{0.5}$) which is about 10% additional noise.

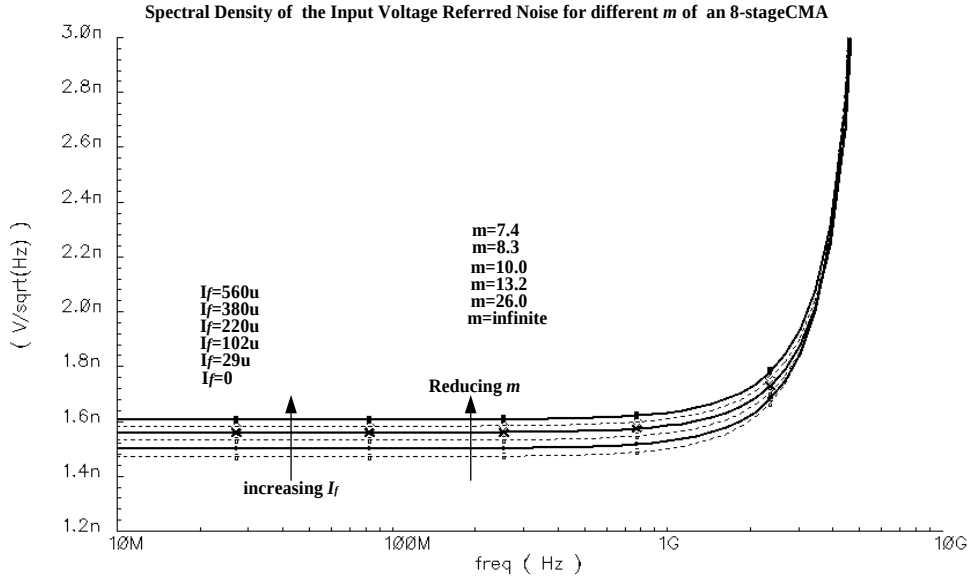


Fig. 4-16 Transistor level simulation of the input voltage referred noise of an 8-stage CMA while *m* is reduced from infinite to 26.0, 13.2,10.0,8.3 and 7.4 when I_g=2mA and G=4.3

C Second Uniform Implementation of an n-*stage CMA*

Using the circuit in Fig. 4-17 decreases the input capacitance of individual stages effectively and increases the forward gains. Gain boosting shifts the pole of the M_g's drain node to higher frequencies while it adds new parasitic capacitances and new poles. The forward amplifier transfer function for this stage can be given as:

$$g(s) \approx G \frac{A(s/z_1 + 1)}{\left(s^2 + Bs + A\right)\left(s/p_3 + 1\right)} \tag{4-7}$$

and the feedback amplifier transfer function can be written as

$$f(s) = \frac{F}{(s/p_3 + 1)} \tag{4-8}$$

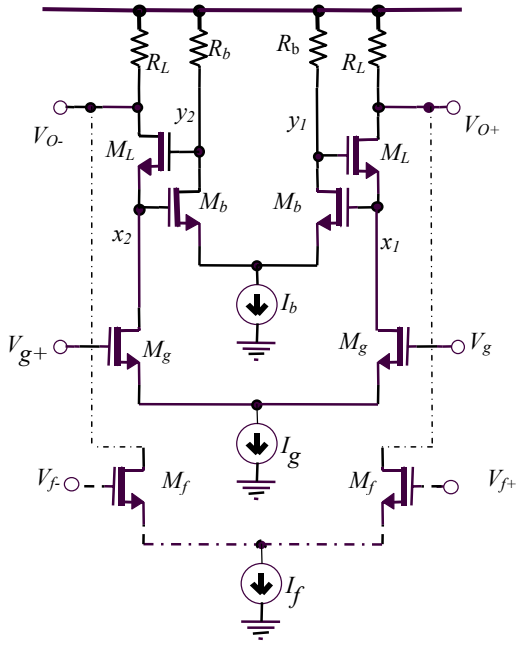


Fig. 4-17 A stage for the uniform implementation of CMA with minimum input capacitance

In this circuit the capacitance in the output node is a summation of a drain-bulk capacitance, the input capacitance of the next stage (which is small) and the Miller effect of C_{gdf} (which is a negative capacitance). Since the positive capacitances are small, a small capacitance as a negative capacitance is needed to decrease the overall capacitance in each node. Where R_O is output resistance of a stage and g_{mf} is the transconductance of M_f. $G=g_{mg}R_O$ and A, B and z_1 can be obtained from

$$A = \frac{g_{mL}(1 + g_{mb}R_b)}{R_b\left((C_y + C_{xy})C_x + C_yC_{xy}\right)} \tag{4-9}$$

$$B = \frac{\left|g_{mL}(C_y + C_x) + G_b(C_x + C_{xy}) + g_{mb}C_{xy}\right|}{\left((C_y + C_{xy})C_x + C_yC_{xy}\right)} \tag{4-10}$$

$$z_1 = \left(1 + g_{mb} R_b\right) / C_y R_b \tag{4-11}$$

where g_{mb} and g_{mL} are transconductances of transistors M_b and M_L. C_y and C_x are the parasitic capacitances in nodes y_1 (and y_2) and in nodes x_1 (and x_2), respectively. C_{xy} is the parasitic capacitance between nodes x_1 and y_1 (or between nodes x_2 and y_2). To reduce the effect of parasitic capacitances in nodes x_1 and x_2, the gain of boosting amplifier must not be too big.

1. Simulation Results

The CMAs and the MAs without feedback for n=2, 4, 6 and 8 in 0.35μm CMOS were designed and optimized with different W_f (width of the transistor M_f) and R_L to have the minimum ripple (<1.5dB) in their transfer function, where the forward DC gain (G) was kept constant for all stages. The MAs' stages are similar to the circuit in Fig. 4-17 except that they do not have M_f and the current source I_f). The circuits were combined with a buffer to drive the 50Ω loads in series with 1pF capacitors at 3.3V single power supply. Fig. 4-18 illustrates the simulation of AC responses (at F≈1). The CMA has a wider bandwidth and the simple cascade structure without feedback gives a larger gain. 8-stage CMA has a bandwidth of about 2.9 GHz and a DC gain of about 60dB, while the 8-stage MA has a bandwidth of about 0.43 GHz and a DC gain of 91dB.

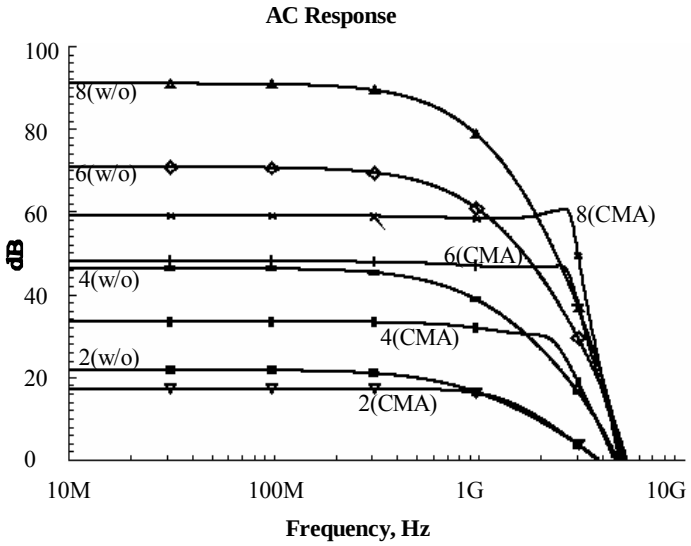


Fig. 4-18 AC response simulation of the gain of the CMAs and the conventional MAs (without) for n=2, 4, 6 and 8

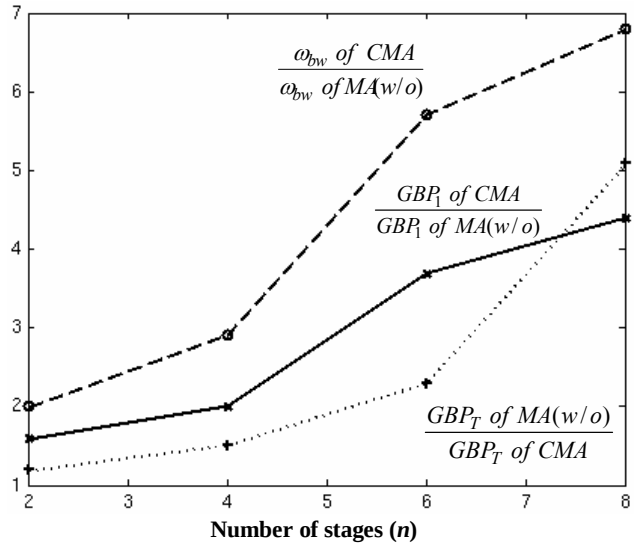


Fig. 4-19 Ratio of bandwidth and GBP_1 of n–stage CMA and n-stage conventional MA (without) and the ratio of total gain bandwidth product (GBP_T) of n-stage conventional MA (without) and an n-stage CMA

To compare the CMAs and the MAs for n=2, 4, 6 and 8, their GBP_1s and the overall GBPs (GBP_T) of circuit simulation results were extracted. GBP_1 of CMA for n=2, 4, 6 and 8 are 3.70GHz, 4.21GHz, 6.88GHz and 7.38GHz respectively. The ratio of GBP_1s and the bandwidths for two structures of CMA and MA is illustrated in Fig. 4-19. The CMA's GBP_1 is higher and increasing n gives a bigger GBP_1 for CMA. This is exactly the opposite of what is seen in the conventional MA. As Fig. 4-19 shows that bandwidth of CMA is more than 6.7 times of that of MA. The sole stage, whose dominant pole is different from others, is the last stage. Having more stages makes more peaks and compensates for rolling-off of transfer function affected by the dominant pole of the last stage. Fig. 4-19 also illustrates the ratio of the overall gain bandwidth product (GBP_T) of MA and CMA. As it shows, this ratio is increasing as n increases. Compared to bandwidth ratio, it is lower.

As discussed before group delay, which is somewhat related to the bandwidth, is a parameter to explain about linearity of phase in a wideband amplifier. Fig. 4-20 illustrates group delays of CMAs and MAs. Unfortunately, the group delay of CMA has a peak around corner frequency. This variation is increasing as n increases (this is exactly the same with conventional MA). This can be predicted because having more poles (specially separated poles in a region) makes more variation in group delay.

For n=8 the power consumption of each stage is less than 9mW. Input referred noise of CMA is $2(nV/(Hz)^{0.5})$-$3(nV/(Hz)^{0.5})$ which is small enough for optical communications applications. Noise for MA is $1(nV/(Hz)^{0.5})$-$2(nV/(Hz)^{0.5})$.

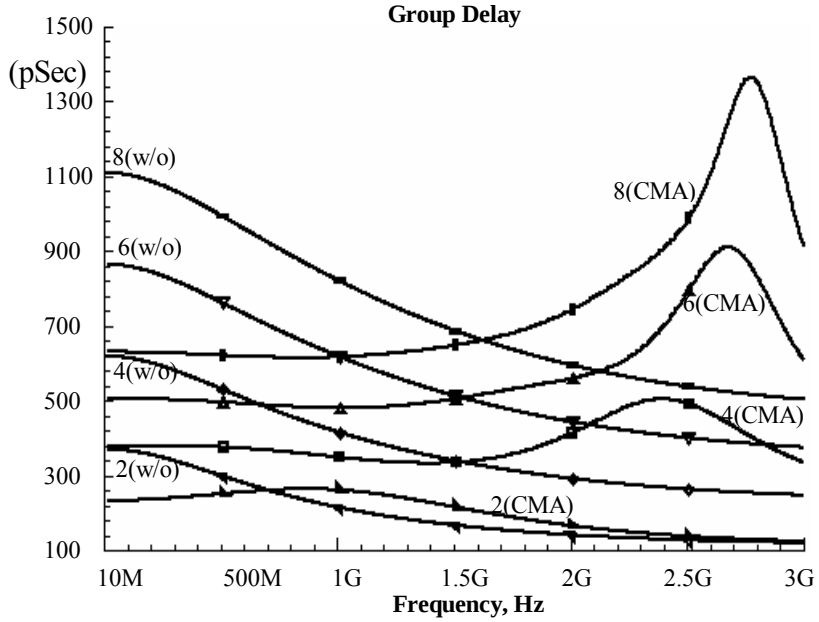


Fig. 4-20 Group delay simulation result of an *n*–stage conventional MA (without) and an *n*-stage CMA for *n*=2, 4, 6 and 8

2. Design of the Second Uniform 6-stage CMA

The design example of section IV-B-3, the amplifier shown in Fig. 4-4 were implemented using the inductor less differential cascode structure with gain boosting illustrated in Fig. 4-17. As it was explained using a cascode structure decreases the effective input capacitance of individual stages and increases the forward gains. Gain boosting shifts the pole of the M_g's drain node to higher frequencies. Parameters of transistors and resistors which are used for simulations and measurement are shown in Table 4-3. Simulation results of the chip are summarized in Table 4-4. Fig. 4-21 shows an AC response simulation of the amplifier. Group delay simulation is illustrated in Fig. 4-22. Group delay reaches its peak at a frequency higher than 2GHz in simulation. As Table 4-4 shows the percentage of the variation in band of group delay is less than 5% while the overall gain bandwidth product is 5.1 times that of the 6-stage CMA with

structure of Fig. 4-3(b). This improvement consumes more power (about 50%).

Table 4-3: Parameters of the *n*-stage CMA (stages are shown in Fig. 4-17)

Parameters	Values
M_g	W/L=60
M_f	W/L=10
M_b	W/L=60
M_L	W/L=30
R_L	0.85KOhms
R_b	0.85KOhms
Load Transistor	2(W/L=300)

Table 4-4: The simulation results of the 6-stage CMA with stage in Fig. 4-17 simulated in 0.35um CMOS Technology

Parameters	Values
f_{-3dB}	1.5GHz
Group Delay Ripple in Band	27pS
Gain	54.4 dB
Power Consumption	59.4mW

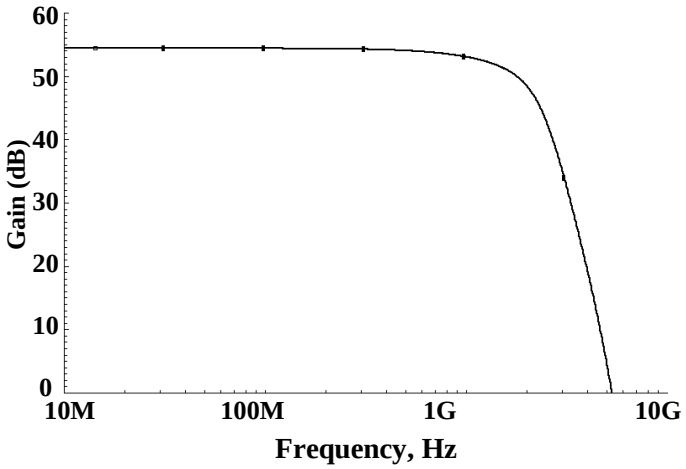


Fig. 4-21 Gain of the 6-stage CMA in 0.35um CMOS technology is made from Fig. 4-17

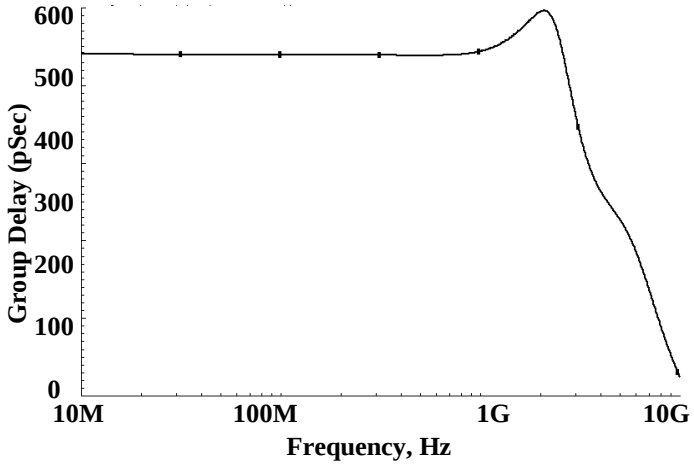


Fig. 4-22 Group delay of the 6-stage CMA in 0.35um CMOS technology is made from Fig. 4-17

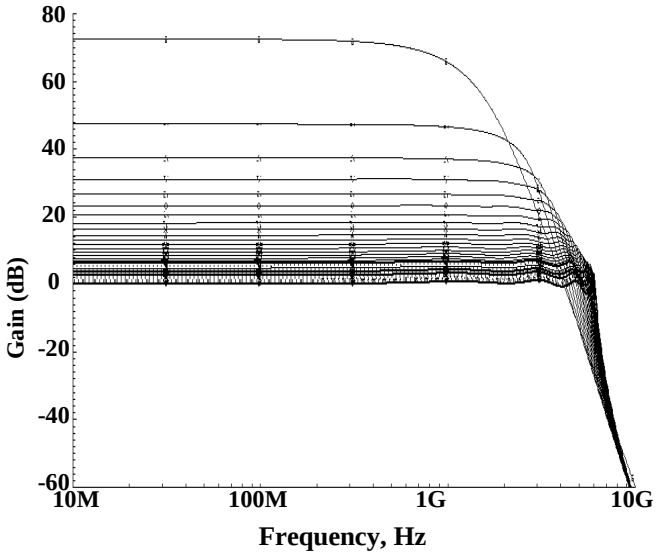


Fig. 4-23 The magnitude of AC response simulation of the second 8-stage CMA using circuit in Fig. 4-17 as stage amplifier, I_f is swept from 5uA to 875uA, while I_g=2mA and G=4

A simulation results of amplitude a 6-stage amplifier when I_f is swept from 5uA to 875uA, where I_g=2mA is illustrated in Fig. 4-23. As it shows in high I_f the ripple in the amplitude has a higher swing. A transistor level simulation of the overall gain of the two implemented 6-stage CMA amplifiers is illustrated in Fig. 4-24. For reaching the same bandwidth, the second CMA circuit gives much higher bandwidth while the group delays variation, specially when there is a higher bandwidth, is worse. A comparison between GBP_1 of four 8-stage amplifiers is illustrated in Fig. 4-25. Stages are circuits in Fig. 4-3(b) and in Fig. 4-17 for CMA1 and CMA2 respectively, and for MA1 and MA2 are the same circuits while the feedback paths and the feedback transistors are removed from circuits. The input transistors, load resistors, I_g and buffers are the identical for all amplifiers. The speed of the input transistors depends on their drain-source voltage. Although using boosting amplifiers in MA2 creates more parasitic capacitances, employing a lower drain-source voltage for input transistors increases the speed of stage amplifiers. Fig. 4-25 shows the GBP_1 of MA2 is about 1.5 times that of MA1. Increasing I_f expands bandwidth more and increases the performance of the amplifiers of CMA1 and CMA2.

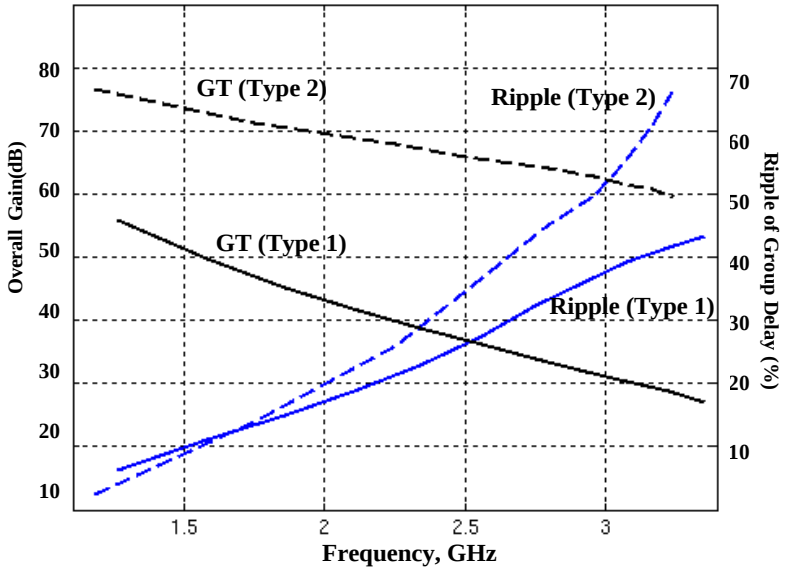


Fig. 4-24 Transistor level simulation of the overall gain of two 6-stage CMA, stages are circuit in Fig. 4-3(b) and in Fig. 4-18, the overall gain and the percentage of the ripple of the group delay vs. the bandwidth

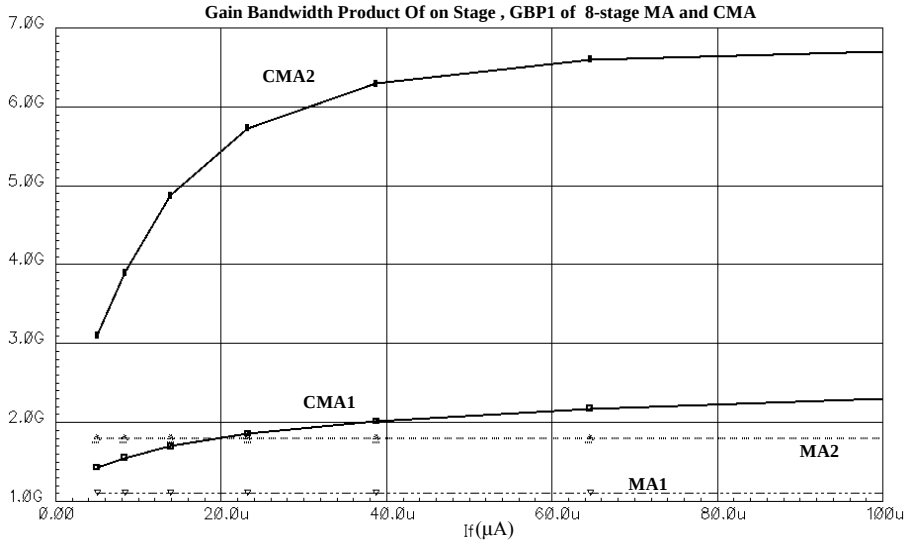


Fig. 4-25 The simulation results of the gain bandwidth product of one stage of 8-stage amplifiers of MA and CMA, stages are circuit in Fig. 4-3(b) and in Fig. 4-18 when I_g=2mA.

3. Measurement Results

The fabricated 6-stage CMA in a test circuit on printed circuit board (PCB), where it was buffered to drive 50Ohms at 3.3V power supply, was measured. The measured results of magnitude of the transfer function are shown in Fig. 4-26 when I_g=2mA, I_b=1mA for I_f=0,45uA and 390uA. The malfunction of buffer in high frequency produces some dumping peaks in the transfer function especially it adds peaks in high DC loop gain (L). It can be seen when for I_f=390uA it makes a worse situation. There is some inaccuracy in measurements of transfer functions in frequencies less than 80MHz and higher than 3-GHz which is produced from balance to unbalance circuits, DC coupling and calibration circuits. But still the enhancement of circuits so significant that the results are comparable or better than that reported recently in wideband amplifiers. The die photomicrograph is shown in Fig. 4-27. The eye diagram for the minimum swing voltage 2mV and the maximum swing voltage 2V are shown in Figure 4-28.

Using the proposed amplifier topology with I_g=3mA and I_b=1.19mA, 43dB overall gain and 2.91 GHz bandwidth could be achieved, while the peak–to–peak jitter for 2.5Gb/S (2^{31}-1 pseudo-random) bits is less than 120pS for 2mV peak-to-peak input voltage and 200pS for 2V input voltage. This amplifier also in terms of jitter, power consumption, and occupied chip area, the CMA topology is considerably better than a recent paper which reports a non-uniform peaking technique in 0.35μm CMOS process [45], and it is comparable with a report presenting a uniform MA in 0.18μm CMOS [60]. Table 4-5 illustrates a comparison of measurement results with some reports have been recently published.

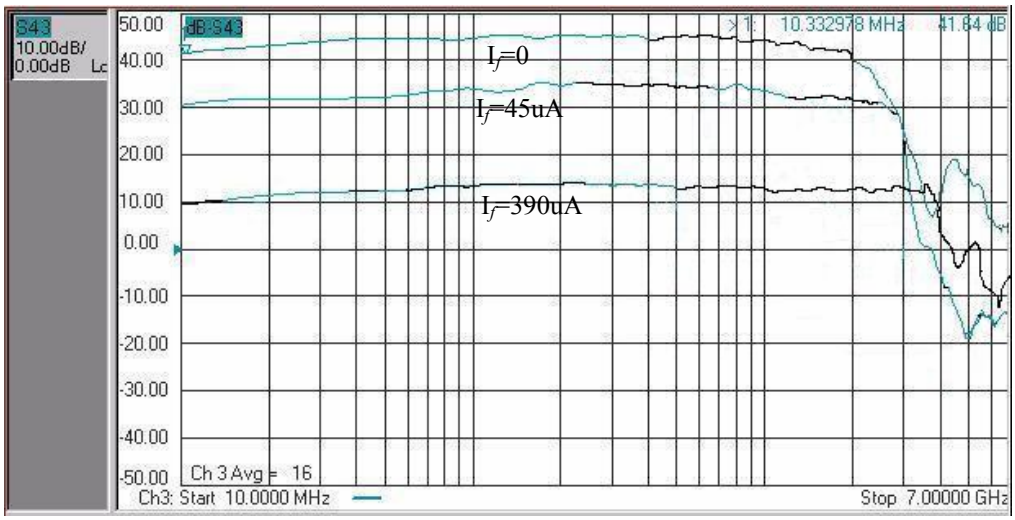


Fig. 4-26 The amplitude measurement results of the 6-stage CMA in 0.35um CMOS technology is made from circuit shown Fig. 4-17 when I_b=1mA and I_g=2mA

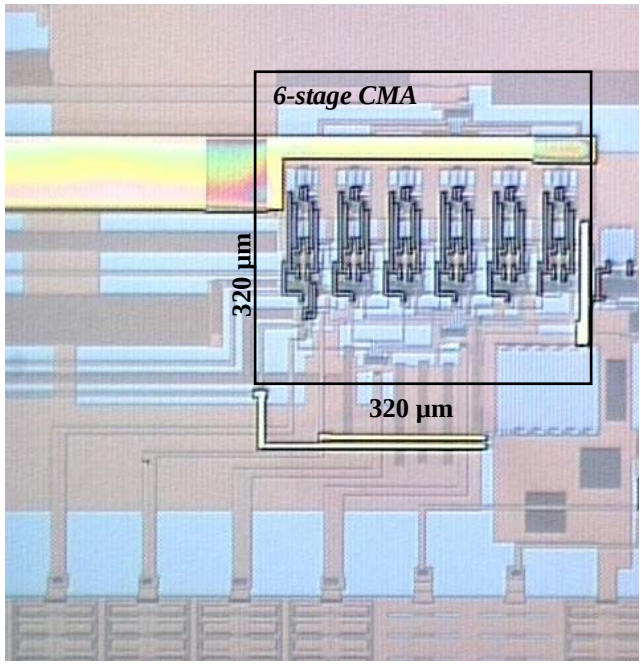


Fig. 4-27 Die microphotograph of the second 6-stage CMA

Table 4-5: A comparison of measurement results with some recent reports

parameter	This work	Ref[43]	Ref[42]	Ref[61]	Ref[59]	Ref[52]
DC Gain (dB)	43	42	30	40	32	42
*-3dB frequency (*GHz*)*	2.91	2.3	3		3	3
Bite Rate (Gbps)	2.5	2.5	3.2	2.5	2.5	3.1
Power dissipation (mW)	83	277.5	135	225	53	225
*Sensitivity (*m*V)*	2	6	3 (10^{-9})	5	2	
Input referred noise (μV)	100				165	
Overload (V)	2		1	0.5	1	
Peak-to-peak jitter (*pS)*	<120	<200			~80	~70
Output Swing-v	0.8	0.3	0.3-0.4	0.4	0.4	
Power Supply	3.3	3	5	5	2.5	2.5
Technology (CMOS)	0.35	0.35	0.25 BICMOS	0.35	0.25	0.18
Area(mm^2)	0.01	0.19		1.1	0.03	

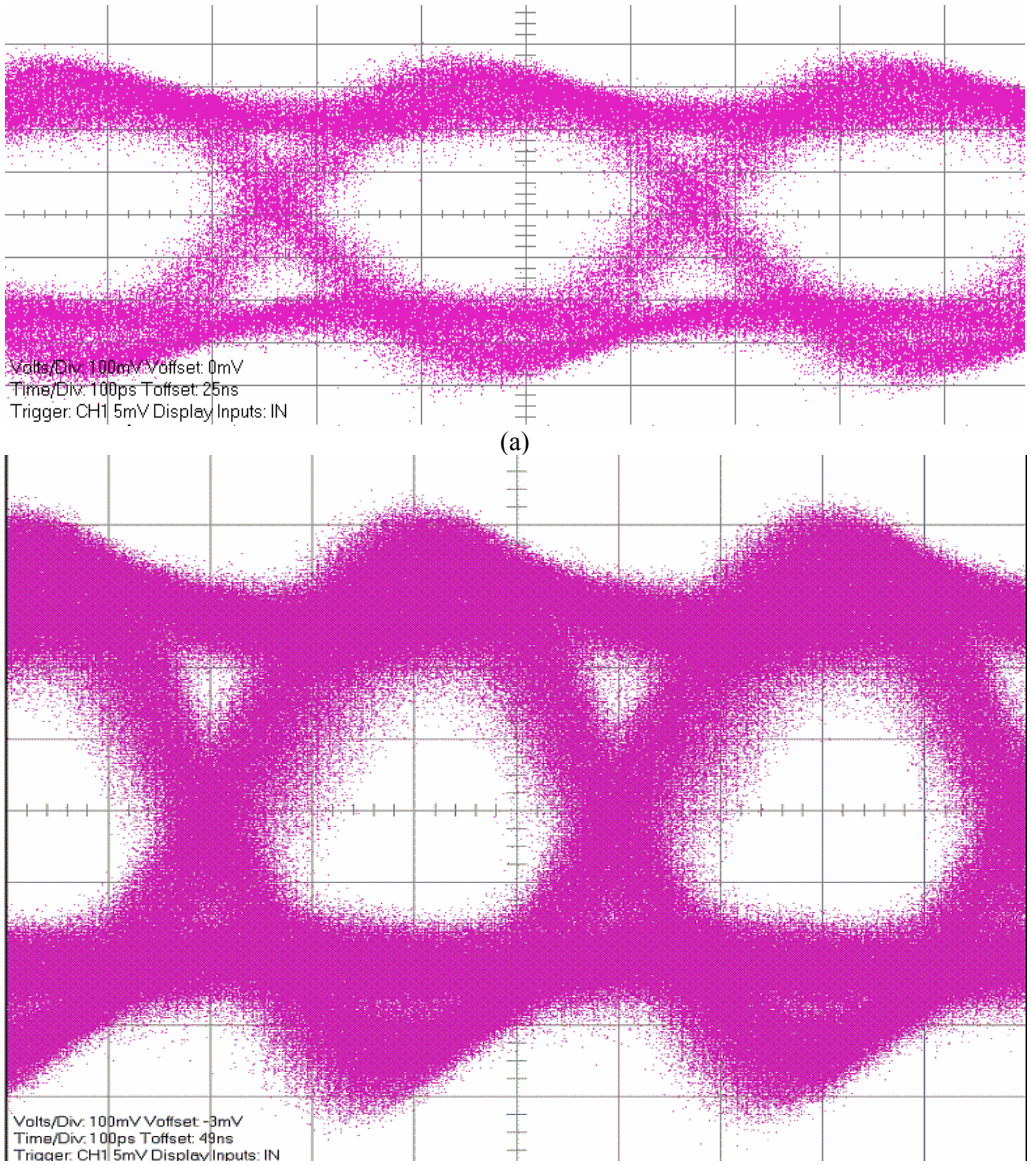


Fig. 4-28 Eye diagram measurement results when I_g=2.47mA, I_b =1.53mA for input voltage (a) Vi=2mV, I_f=0 (b) Vi=2V, I_f=263uA (Div X=100pSec and Div Y=100mV)

CHAPTER V

A CAPACITANCE MULTIPLICATION TECHNIQUE COMBINING VOLTAGE AND CURRENT MODE

A Introduction

Low cost and high-level integration of CMOS technologies create a strong incentive to build high performance filter circuits in silicon. Fig. 5-1 demonstrates that in clock and data recovery loops a low pass filter is employed. As discussed in chapter I, since each loop has a different bandwidth and damping factors, changing loop filter specification is necessary [23]. To change the loop filter specification, a capacitance multiplier with variable multiplication factor is proposed. Furthermore, to remove the DC offset in the main amplifier a low pass filter in a DC negative feedback is used. To implement such a low pass filter in optical communications usually external capacitances have to be employed [23]. To avoid using such external capacitances, an on-chip capacitance multiplier can be used.

1. Tuning Loop Filter

f_{out} in loop II in Fig. 5-1 equals to Nf_{ref} , where the phase transfer function is a second order function with damping factor [23] of

$$\xi = \frac{R_p}{2}\sqrt{\frac{I_p C_p K_{vco}}{2\pi N}} \tag{5-1}$$

Increasing N reduces ξ, which in turn degrades the loop stability. Although increasing R_P improves stability, due to process variation, implementation of an accurate variable R_P on chip is not practical[1]. Furthermore, it has been shown that R_P cannot be increased arbitrarily without introducing instability [23]. In practical low power implementations, changing I_P by the same

[1] The bank of resistors is used to switch the values of R_P that needs trimming to return the accuracy of R_P.

order of the desired variation in N is not an option. A variable C_p can be suitable to adjust the damping factor. To further reduce the jitter of the loop, the bandwidth of the loop filter needs to be reduced. This usually requires using a relatively large external capacitor (C_p is several nF). The demand for integration of such large capacitance on chip provides the motivation to use capacitance multiplication techniques. Using an on-chip tunable capacitance multiplier, the desired damping factor can easily be realized.

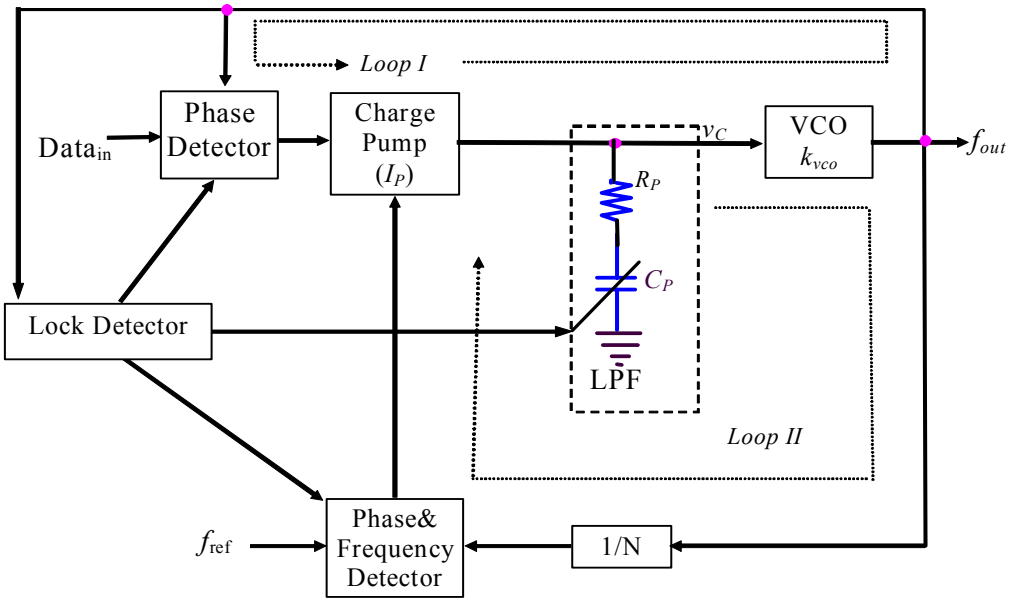


Fig. 5-1 Proposed CDR architecture with an external reference

2. DC Offset Cancellation

One of the challenges for the design of the main amplifier is to remove the DC offset [56].The DC offset cancellation circuit is used to remove the possible offset introduced by mismatching paired transistors and load resistors. The mismatch, produced by non-uniformity of the process variation in die, creates an offset for each stage of multistage amplifier. The offset in the first stage is amplified by next stages which in turn degrades the performance of the later stages. The

DC offset of the input transistors of the first stage (in CMOS technology) can be in the order of millivolt [39]-[41] that is comparable to the weak signal which must be amplified by the first stage. DC offset must be minimized in the first stage to increase sensitivity of the main amplifier (see Fig. 5-2).

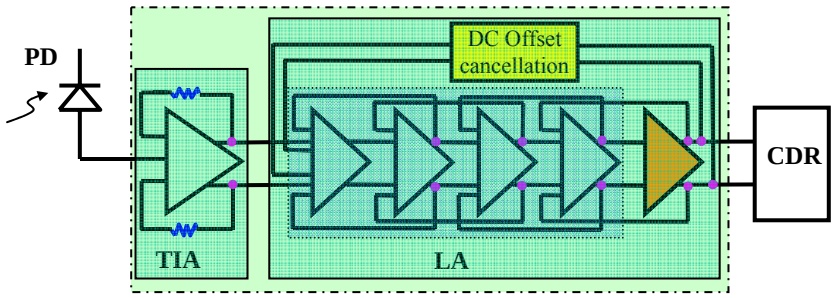


Fig. 5-2 Proposed TIA, LA and DC offset cancellation circuit

The DC offset cancellation circuit can be designed as a simple RC circuit. The DC offset at the output nodes is used to adjust the DC voltage levels of the first stage's output nodes in a way that the overall DC offset is minimized. Unfortunately, DC offset cancellation circuit also degrades the low frequency performance of the amplifier (LA). The output voltage of the amplifier drops down (it is called "droop" [23]); as a result, it creates a vertical distortion in eye diagram (see Fig 1-4 and Fig. 2-1) when there is a constant pattern of the consecutive identical bits [23]. Depending on the maximum number of possible sequenced "1"s (or "0"s) and possible vertical distortion, the constant time (RC) of low pass filter can be calculated.

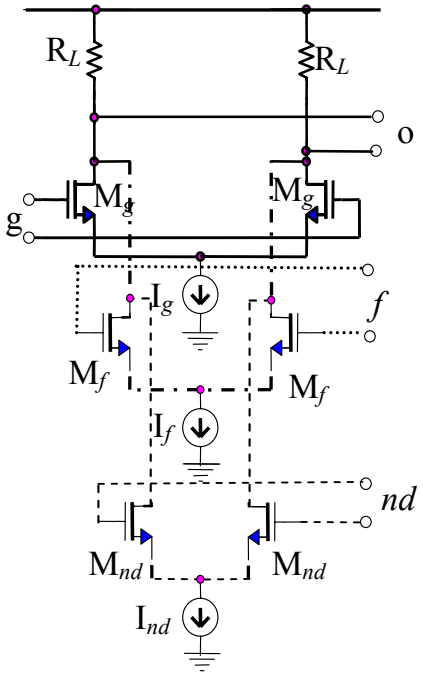


Fig. 5-3 The first stage of the CMA (see section IV-B-3)

The first stage of a CMA is shown in Fig. 5-3. The DC negative feedback employs an OTA structure consisting of the paired transistor M_{nd} to adjust the current of the pair resistor of the first stage. M_{nd}s and the RC circuit are shown in Fig. 5-4. Assume the DC gain of amplifier is A_{M} and g_{mg} is the transconductance of the first paired transistors (in Fig. 5-3) and g_{mnd} is the transconductance of the paired transistors M_{nd} which produce a negative current to compensate for the offset.

Assuming the transfer function of the DC negative feedback circuit can be modeled as a first order function with the dominant pole frequency of $f_{\text{-3dB,fiter}}$, the low frequency pole of the overall transfer function of LA (with DC offset cancellation circuit) can be written as

$$\omega_{-3dB,DC} = 2\pi f_{-3dB,filter}(1 + DC\,loop\,gain) \qquad (5\text{-}2)$$

For example, for a 2.5 Gbits/S optical link the low cutting frequency is a few tens of kilohertz. The overall transfer function of amplifier has a DC gain of g_{mg}/g_{mnd}, a low frequency zero (z_1), and a low frequency pole (p_1). z_1 and p_1 can be calculated as

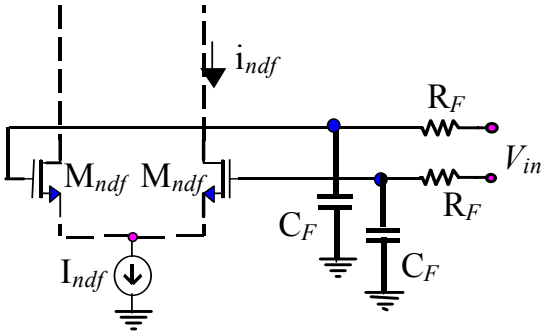


Fig. 5-4 The DC negative feedback scheme

$$z_1 = \frac{1}{R_F C_F} \tag{5-3}$$

$$p_1 = \frac{1 + A_M g_{mndf} / g_{mg}}{R_F C_F} \tag{5-4}$$

Fig. 5-5 shows a magnitude simulation of the transfer function of an 8-stage CMA with a DC negative feedback.

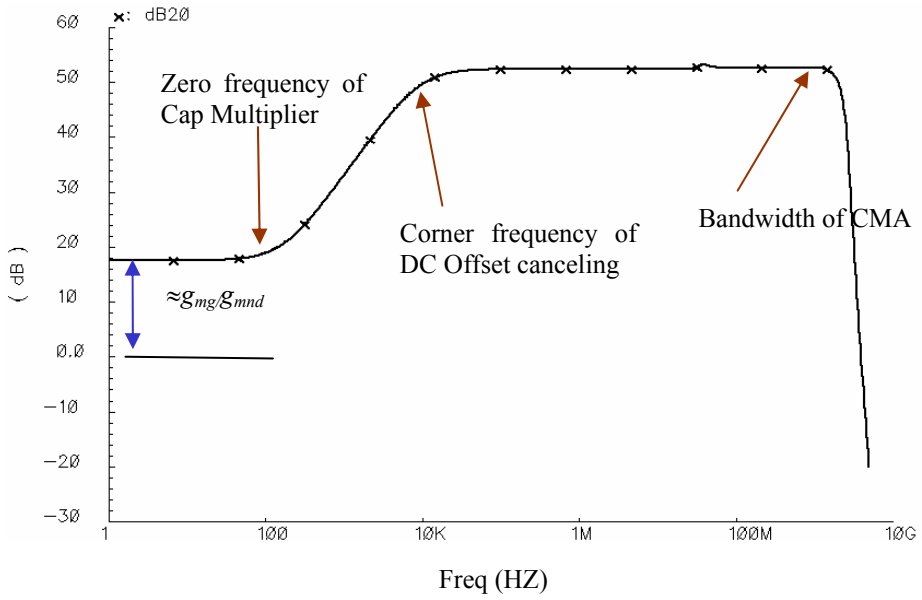


Fig. 5-5 Magnitude simulation results of the transfer function of a CMA while a DC negative feedback is used

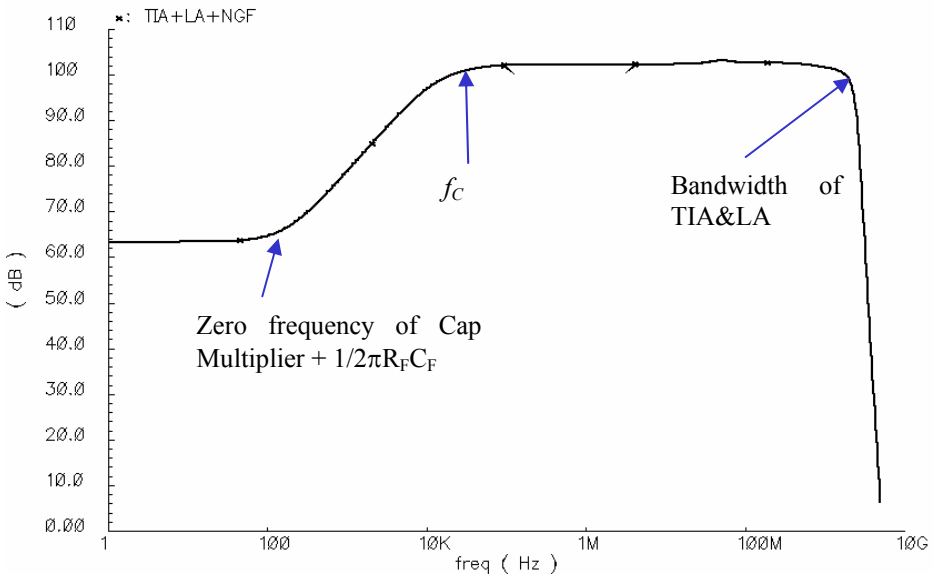


Fig. 5-6 The magnitude of the transfer function of a front end amplifier of optical communication, a TIA and an LA when the LA employs a DC negative feedback in input stage

Magnitude simulation results of the amplitude of the overall current-to-voltage conversion gain of the cascaded of a TIA and an LA with a DC negative feedback is illustrated in Fig. 5-6.

3. Capacitance Multiplier

Active capacitance multipliers have been developed during the past decade, employing current and voltage mode techniques [62]. Solutions using current mode techniques, as depicted in Fig. 5-7, provide high swing and high frequency performance, but they suffer from reduced multiplication factor, poor tunability [62]-[63], low input resistance, and DC leakage current [61]-[64]. DC leakage current introduces spurs in VCO and frequency dependent low input resistance increases the nonlinearity behavior of VCO.

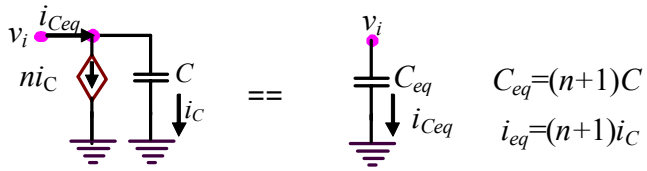


Fig. 5-7 Current mode capacitance multiplication technique

Voltage-mode techniques, as shown in Figure 5-8, can provide high multiplication factors utilizing voltage amplifiers to multiply the Miller capacitance [65]-[66]. There are four main drawbacks in typical Miller compensation methods. First, high multiplication factors are obtained only at low frequencies because high gain amplifiers have relatively low frequency poles. Second, large capacitors are needed for stability purposes (later it is explained more),

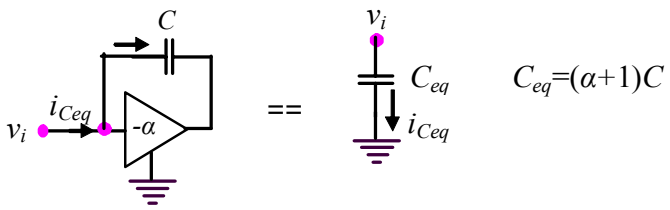


Fig. 5-8 Voltage mode capacitance multiplication techniques

which occupy substantial chip area [65]-[68]. Third, high gain amplifiers easily go to saturation, thus the input of the capacitance multiplier is limited to smaller signals. Forth, a proper DC bias voltage is needed to keep the input transistors of the amplifier in saturation.

In this chapter, a capacitance multiplication technique is introduced. The proposed method uses a combination of voltage and current mode techniques to realize high multiplication factors with improved frequency response and voltage swing. The capacitance multiplier is used in a first order low pass filter. To demonstrate the proposed topology, the capacitance multiplier was designed and fabricated in a 0.5μm CMOS process.

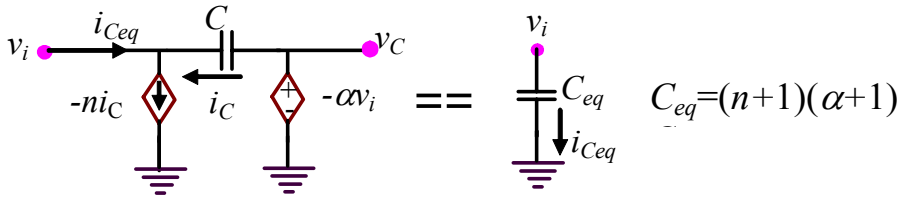


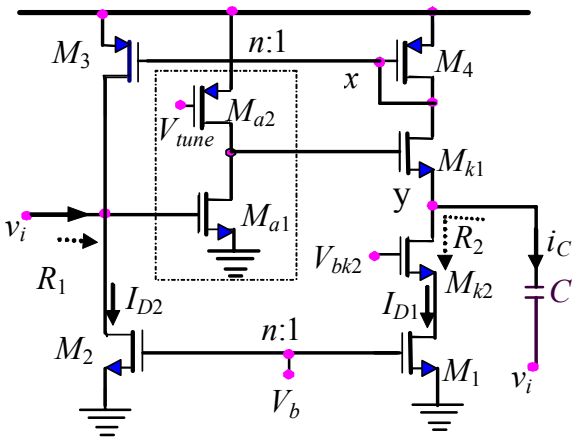
Fig. 5-9 The proposed capacitance multiplication technique

B Proposed Capacitance Multiplication Technique

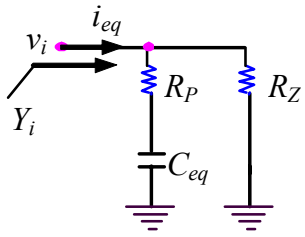
The basic principle of the proposed multiplication technique is illustrated in Figure 5-9. The current moving through the capacitor (i_C) is amplified by a current mirror to provide $i_{Ceq}=-(n+1)i_C$ whereas v_i is amplified to set the capacitor voltage to $v_C=-(\alpha+1)v_i$. The equivalent

capacitance (C_{eq}) seen at the input can be calculated as $C_{eq}=MC$, where $M=(n+1)(\alpha+1)$. The equivalent capacitance is negative for $\alpha<-1$, whereas positive multiplication can be obtained for $\alpha>-1$. n is usually fixed and not easily controlled, since α can be varied to have a variable multiplication factor M.

Fig. 5-10 (a) shows a circuit implementation of the proposed multiplication scheme. The voltage amplifier is composed of transistors M_{a1} and M_{a2}, where the current mirror is constructed using M_3-M_4. Gain of the amplifier (α) is varied by means of V_{tune}.



(a)



(b)

Fig. 5-10 Simplified circuit of the proposed capacitance multiplication, (a) circuit (b) equivalent model

Assume that the parasitic capacitances of M_3-M_4 in Fig. 5-10(a) are much smaller than C, (C_x<<C) and the amplifier (M_{a1}-M_{a2}) has poles at relatively higher frequencies. A simplified equivalent circuit of Figure 5-10(a) can be shown as in Fig. 5-10(b), where R_P and R_z can be obtained as

$$R_P \approx \frac{1/g_{mk1}}{M} \tag{5-5}$$

$$R_Z \approx R_1 // \frac{R_2}{M} \tag{5-6}$$

where g_{mk1} is the small-signal transconductance of M_{k1}. Since the intention here is to have a pure capacitance (C_{eq}), it is desirable to increase R_Z and to decrease R_P. Although increasing M reduces R_P, it also decreases R_Z. Alternatively, g_{mk1} can be increased to reduce R_P, where R_1 and R_2 can be increased to enhance R_Z. The input resistance R_1 in Figure 5-10(a) is equal to the parallel drain-to-source resistances of M_2 and M_3. It is inversely proportional to I_{D2} and n. Increasing n reduces R_1. Thus, there is a trade-off between increasing R_Z and increasing n. Although due to the cascode configuration R_2 is much larger than r_{ds2}, R_2/M can still be comparable to r_{ds2} when M>50.

1. Admittance

The input admittance Y_i of Figure 5-8(a) can be calculated as

$$\frac{i_{Ceq}}{v_i} \approx (\alpha+1)(n+1)C\frac{s+z_1}{s/p_1+1}\left(\frac{s/z_2+1}{s/z_2+1}\right) \tag{5-7}$$

$$p_1 = (g_{mk1} + g_2 + g_{dsk1})/C \tag{5-8}$$

$$p_2 = g_{m4}/C_x \tag{5-9}$$

$$z_1 = \left(n\alpha g_2 + g_1\right)/\left(\alpha + 1\right)\left(n+1\right)C \tag{5-10}$$

$$z_2 = g_{m4}\left(n+1\right)/\,C_x \tag{5-11}$$

where $z_1 \approx 1/MR_ZC$ and $p_1 \approx 1/MR_PC$. The p_2 depends on parasitic capacitance at node x and the transconductance of transistor M_4. The z_2 is at higher frequencies. It is desirable to remove the first zero (or shift it to lower frequencies), increase g_{mk1} (or increase p_1) and reduce C_x (which depends directly on n) so that $Y_i(s) \approx MCs$. Increasing C shifts z_1 to lower frequencies; however, p_1 also shifts in the same direction. At low frequencies, the equivalent admittance Y_i is approximated to $1/R_Z$. As frequency is increased, it gets equal to $C_{eq}s$. As the frequency further increases, Y_i approaches $1/R_P$. At higher frequencies p_2 and z_2 become more dominant.

Based on the admittance transfer functions, the proposed technique has two advantages compared to the current mode technique. First, p_1 of the proposed method depends on the transconductance of transistor M_{k1} (that can be increased using a boosting amplifier), while in the current mode technique it depends on the transconductance of M_4 (that can not be increased arbitrarily since it also increases the leakage) [68]. z_1 in the current mode technique depends on the overall conductance of the input node (that could be at higher frequencies) while the proposed technique's zero depends on the overall conductance looking into the node y, which is independent of the circuit connected to the capacitance multiplier [68]. The second pole is the same for the two techniques, but the parasitic poles of extra amplifiers in the proposed method could degrade performance of the capacitance multiplier at higher frequencies. In practice, such a capacitance multiplier is not expected to be used at very high frequencies because high frequency filters inherently use smaller capacitances, and a capacitance multiplier would not be necessary.

There are two points to consider in using the circuit illustrated in Fig. 5-10(a). First, the stability of the circuit, which is composed of loops, should be guaranteed. Second, to keep the transistor M_{mk1}in active region, a proper gate-source voltage should be employed. This will be further discussed later.

2. Complete Scheme

The complete schematic of the proposed capacitance multiplication circuit is shown in Fig. 5-11. Matching the paired transistors (M_3-M_4) is guaranteed by using error amplifier A_3 with a gain of κ, which equalizes the source-drain voltage (V_{SD}) of M_3 with that of the transistor M_4. A_3 controls the gate voltage of M_6, and as a result, it controls the drain voltage of transistor M_3. A_3 also increases R_1; meanwhile R_1 is also increased by employing the cascode transistor M_5, thus, enhancing R_Z. Amplifier A_2 with a gain of β boosts g_{mk1}, which reduces R_P by a factor of β. A_1 is a variable amplifier with the gain of $-\alpha$, where α can have a positive or a negative value. For a positive α, a minimum M of n+1 is guaranteed by this scheme.

One of the advantages of the proposed structure in comparison with the typical current mode technique is the high input resistance of the capacitance multiplier, which reduces the leakage current[2].

[2] The leakage current in loop filter increases ripple of control voltage of VCO; thus introducing the spurs of VCO.

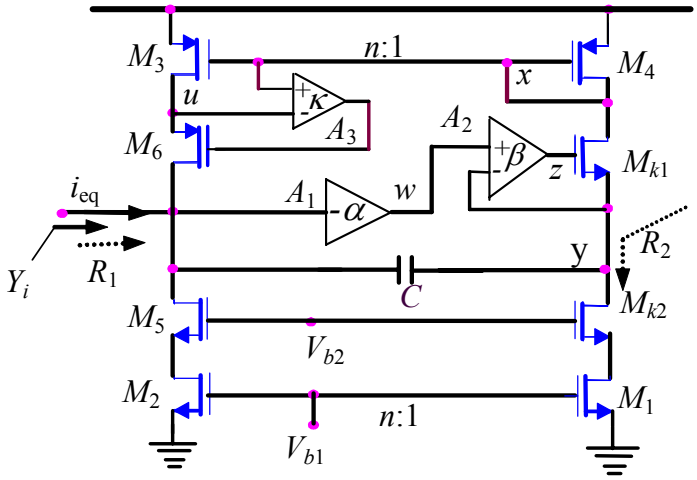


Fig. 5-11 Complete schematic of the capacitance multiplication circuit

3. Stability

As Figure 5-11 shows, two loops are employed by the capacitance multiplication circuit. The first loop, which is shown in Fig. 5-12, consists of A_1, A_2, M_{k1}, M_4, M_3 and M_6, and it can be potentially unstable. Its loop gain can be approximated as

$$Loop\ \ Gain \approx -\alpha n \frac{s/z_1 + 1}{(s/p_d + 1)(s/p_1 + 1)(s/p_2 + 1)} \frac{g_2}{g_1} \tag{5-13}$$

$$p_d = \frac{g_1}{[(1+\alpha)C + C_1]} \tag{5-14}$$

C_1 is parasitic capacitance (output capacitance of the circuit connected to capacitance multiplier). g_1 is the overall conductance at the input node. C is chosen such that p_d is smaller than p_1 and p_2. Fig. 5-13 shows the amplitude response of the loop gain. The two poles p_1 and p_2 are relatively close to each other. This increases the possibility of instability. To have enough phase margin, first p_2 can be shifted to higher frequencies (by minimizing the dimension of transistors M_3 and M_4). Second, as Fig. 5-13 shows for α>-1 since C and C_1 are positive the n is the upper limit of the amplitude of the loop gain. Reducing n pushes the unity gain bandwidth to low frequencies

and it helps to shift p_2 to higher frequencies. Third, p_d can be shifted to lower frequencies far from p_1 to avoid sharp phase variations.

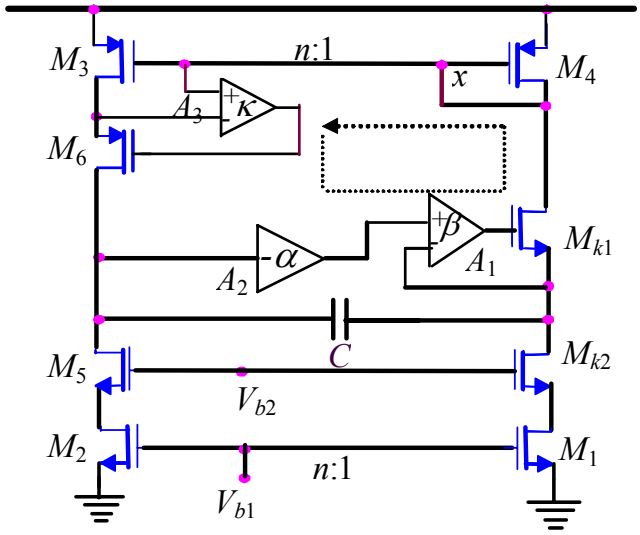


Fig. 5-12 Main loop of cap multiplier

The second loop consists of A_1, A_2, M_{k1} and C that also can potentially be unstable. Its loop gain is similar to the plot in Fig. 5-13, with the exceptions that the dominant pole is $[(1/g_1+R_2)C]^{-1}$ and the maximum loop gain is $\sim\alpha$. To reduce the possibility of instability, α can be decreased. The voltage mode technique has a higher maximum for the loop gain; thus, increasing C is needed to reduce the possibility of instability.

Amplifiers A_1 and A_2 have poles that degrade the phase margin of loop gains. So they must be fast enough and their poles have to be much higher than the unity gain bandwidth frequency of loops. On the other hand, to have a large M, α (the gain of A_1) must be increased. This can be done by using multistage or cascode amplifiers; however, they consume more power and add new poles. As a result, the phase margin of the closed loop of two loops is degraded, thus to reduce the possibility of instability, C must be increased.

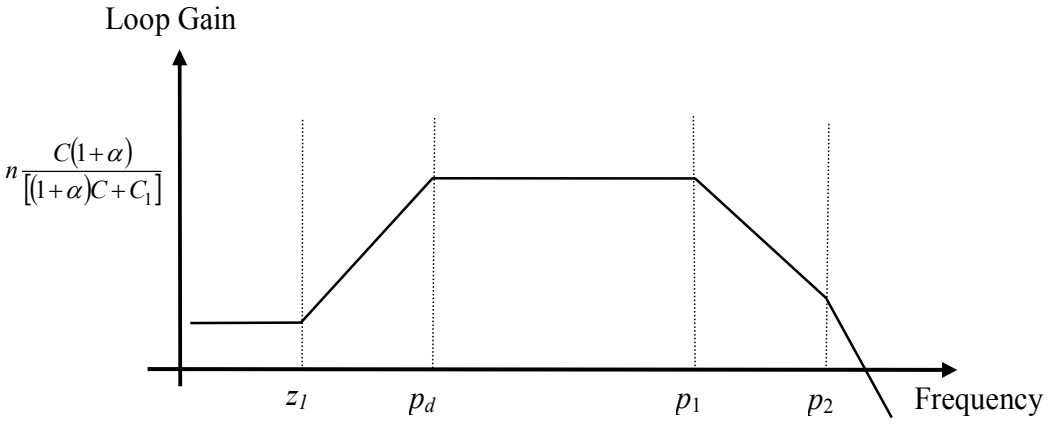


Fig. 5-13 Amplitude of the main loop gain

4. Swing

With a low power supply, the voltage swing at the output of amplifiers A_1 and A_2 is limited. The cascode structure of transistors M_1, M_{k2}, M_{k1} and M_4 puts more limitation on the linearity of the capacitance multiplier. The maximum voltage swing in the node y is between $VDD\text{-}V_{SG4}\text{-}V_{ov,n}$ and $2V_{ov,n}$. The output swing of A_1 and A_2 is limited by requirements of the voltage swing in y. The minimum voltage in the node w cannot be less than $V_{GSk1}+2V_{ov,n}$ and the maximum voltage on the node z is $VDD\text{-}V_{SG4}\text{-}V_{ov,n}$. The input voltage swing of the capacitance multiplier must be small enough to keep all transistors in saturation region.

To compare the linearity of the current mode, voltage mode and the proposed multiplier techniques, let us assume multiplication factors are n+1, α+1 and (n+1)(α+1), respectively. The current mode technique can have an input voltage swing of $VDD\text{-}2V_{ov,p}$ to $V_{SG,n}$. The proposed technique can have approximately the same swing when α is small ($\approx$1). Therefore, for

$M \approx 2(n+1)$ we have the same voltage swing at the input node[3]. Thus, for almost the same voltage swing, the proposed technique gives a bigger multiplication factor. The voltage swing of voltage mode technique is the same as that of the proposed technique while the proposed technique's multiplication factor is $(n+1)$ times that of voltage mode technique. In general, for the same voltage swing a higher multiplication factor can be achieved in the proposed technique comparison with that of other techniques.

5. Noise

The phase noise of the phase locked-loop is specified by the application. The loop filter's noise must be minimized to guarantee the phase noise specs. The noises of R_P and Cp in the circuit in Fig. 5-1 yield jitter in the VCO. R_P is lowered to reduce the jitter bandwidth [23] and C_P is enlarged to decrease the peak value in the jitter transfer function [23]. Utilizing an active capacitance as C_P in a loop filter (shown in Figure 5-1) inevitably produces noise. The thermal and flicker noise of transistors in a capacitance multiplier are dominant. There are two sources of noise in the proposed technique. First is the contributed noise of the current mirrors. The flicker noise of transistors M_1 and M_2 are reduced by transistors M_3 and M_4. The flicker noise of transistors M_5, M_6 and M_{k2} are negligible while that of transistors M_3 and M_4 is dominant. Although PMOS transistors have less noise, it can be reduced even more if bigger transistors are used. Normally the contributed thermal noise of all these transistors is low; however, in higher frequencies it can be the dominant noise. The second noise is due to amplifiers that can be reduced by using PMOS transistors in the input of amplifier A_1 and by shrinking the size of transistor M_{k1}. The main drawback of the proposed technique is higher noise compared to that of the current and voltage mode techniques.

[3] It is assumed the A_1 and A_2 swing do not saturate the cascode structure.

C Measurement Results

The prototype chip of capacitance multiplier was fabricated in AMI's 0.5μm CMOS technology with two poly and three metal layers. The final circuit of the capacitance multiplier is shown in Fig. 5-14 when C=80pF, n=10, and α could vary from 0.39 to 8.7 with 3.3V power supply.

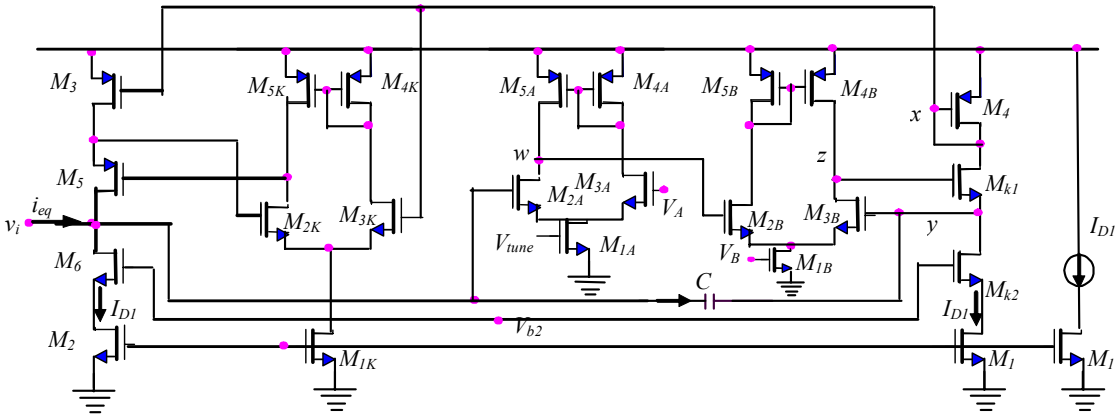


Fig. 5-14 The capacitance multiplier circuit

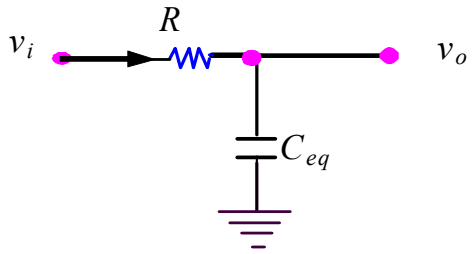


Fig. 5-15 The first order low pass filter used to measure capacitance multiplier

V_{tune} is used to change the gain of amplifier A_1 (transistors M_{1A}, M_{2A}, M_{3A}, M_{4A} and M_{5A}). I_{D1}=3.3μA was used and the overall current is less than 72μA. The capacitance multiplier was employed to realize a first order LPF shown in Figure 5-15. For R=26KΩ Fig. 5-16 shows the amplitude response of the transfer function. The C_{Min} is measured when α is zero (very small) and the C_{Max} is achieved by the maximum gain of α. The f_{-3dB} frequency is 720Hz for C_{Max} and

more than 5KHz for C_{Min}. The phase of the transfer function is shown in Fig. 5-17. The equivalent capacitance changed from 1.22nF to 8.5nF, while leakage current was varied from 1μA to 3μA.

For a high voltage swing, a 400mV peak-to-peak source was used and the amplitude and phase of the transfer function were measured. The transfer function is linear when the amplitude is decreased more than 20dB (up to 10 KHz, its behavior is not that of a first order filter). As it was explained a high swing voltage changes the linear behavior of the cap multiplier.

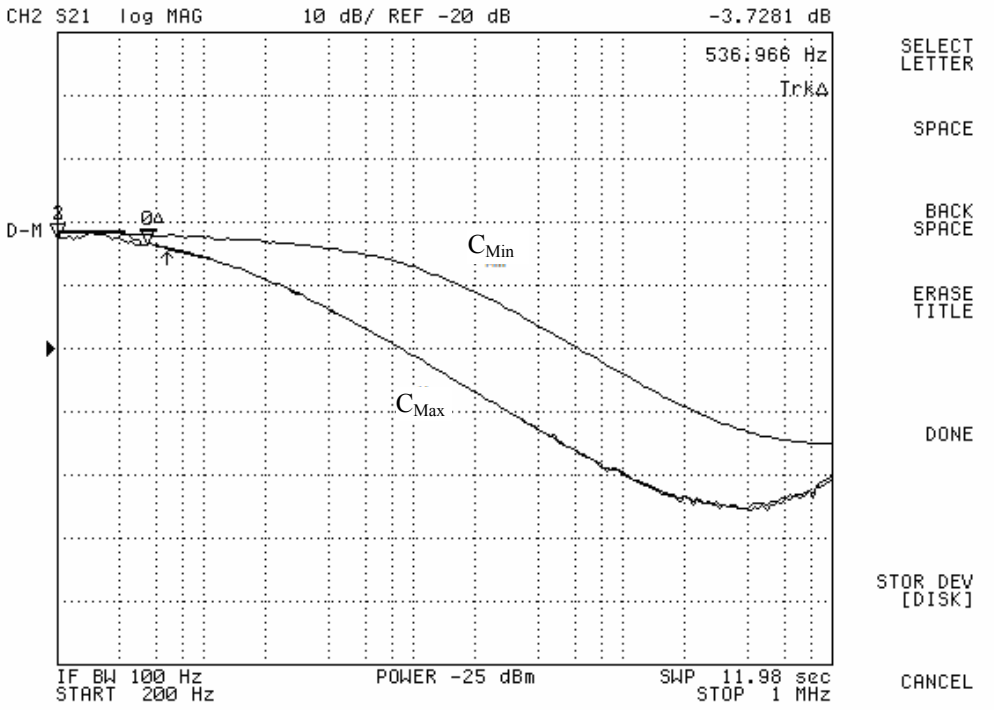


Fig. 5-16 The amplitude of transfer function $v_o(f)/v_i(f)$ of Fig 5-13, C_{Min} : α`~0.39, n=10 and M=11, $C_{Max}$: $\alpha$`~8.7, n=10 and M=106.3

Fig. 5-18 illustrates the magnitude of transfer function in low frequencies and where the

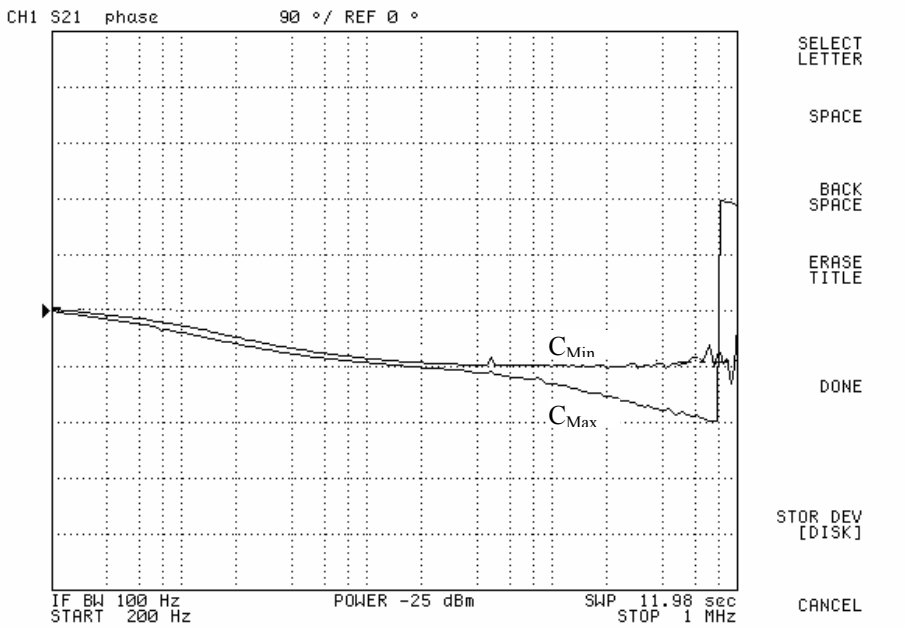


Fig. 5-17 The amplitude of transfer function $v_o(f)/v_i(f)$ of Fig. 5-13, C_{Min} : α`~0.39, n=10 and M=11, $C_{Max}$: $\alpha$`~8.7, n=10 and M=106.3

amplitude is low enough it works as linear element. In this case the phase depicts in Fig. 5-19. At lower frequencies the transfer function magnitude must be 0dB, but the biasing and accuracy of the instrument probe comes to be -1.5dB. Fig. 5-20 shows for an input voltage of 30KHz signal with 800mVp-p, the output is reduced to 13.5mV when α=5. Fig. 5-21 shows for an input of 1.78Vp-p at 60Hz frequency, the output voltage is 1.41Vp-p. As it shows the low frequency can be passed while there is a high voltage swing.

To prove the stability of the main loop, the phase and amplitude of the loop gain of the first loop are simulated (in a post layout simulation) and illustrated in Fig. 5-22 and phase margin is depicted in Fig. 5-23. As they illustrate, the loop is stable for C_u=80pF while V_{tune} is swept from 1.3V to 2.3V that creates a wide dynamic range in the gain of the amplifier.

To measure the sensitivity of cap multiplier with respect to the process variation, the

length of transistor of M_4 was changed from -10% to +10%. The magnitude of the low pass filter's transfer function is illustrated in Fig. 5-24. As it shows 10% mismatching in transistors M_4 and M_3 reduces 117% of the equivalent capacitance of cap multiplier. This is a drawback of employing the current mode capacitance multiplication.

The voltage level of node *w* changes the level voltage of node *z* in the gate of transistor M_{mk1}. Mismatching the current and size of transistors $M_{4A}$and M_{5A} changes the level voltage of node *w*; furthermore, it degrades the gain of amplifier. To simulate the sensitivity of cap multiplier when a mismatching is produced in the amplifier, the length of transistor M_{5A} was varied from -10% to 10%. The simulation results are illustrated in Fig. 5-25. It depicts for such variation the equivalent capacitance is changed by 38%. The voltage biases V_A and V_B can be used to adjust the voltage level of node *w*, though this further increases the complexity of the circuit.

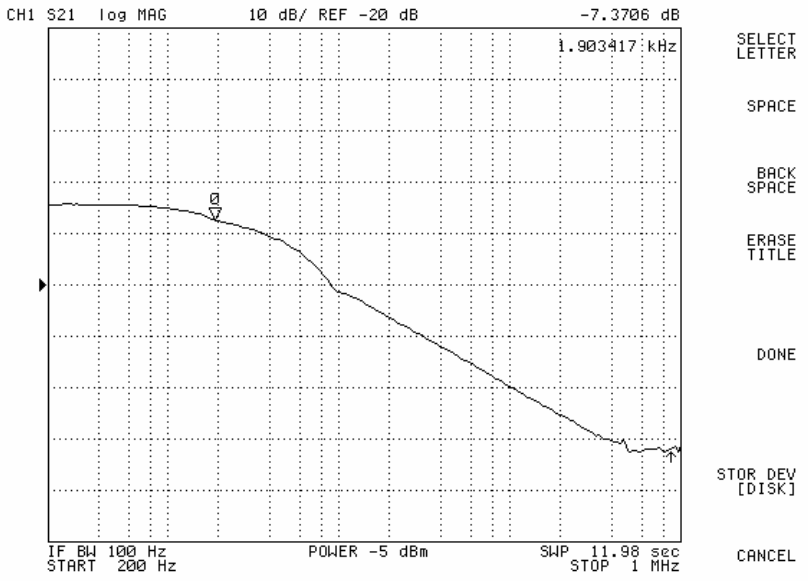


Fig. 5-18 The amplitude of transfer function $v_o(f)/v_i(f)$ of Fig. 5-13, α`~3, *n*=10 and *M*=44 and swing is 400mV peak-to-peak.

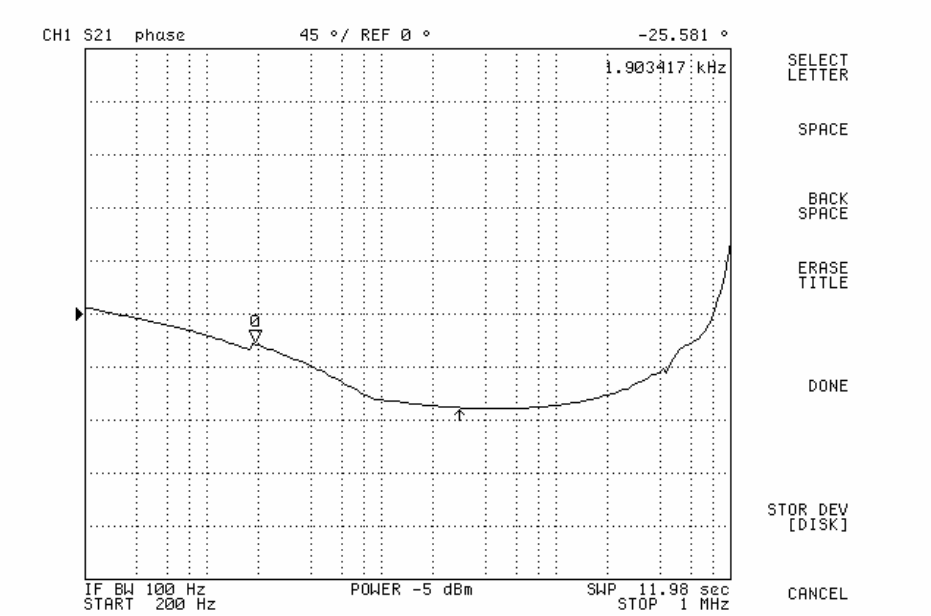


Fig. 5-19 The phase of transfer function $v_o(f)/v_i(f)$ of Fig. 5-13, α~3, n=10 and M=44 and swing is 400mV peak-to-peak.

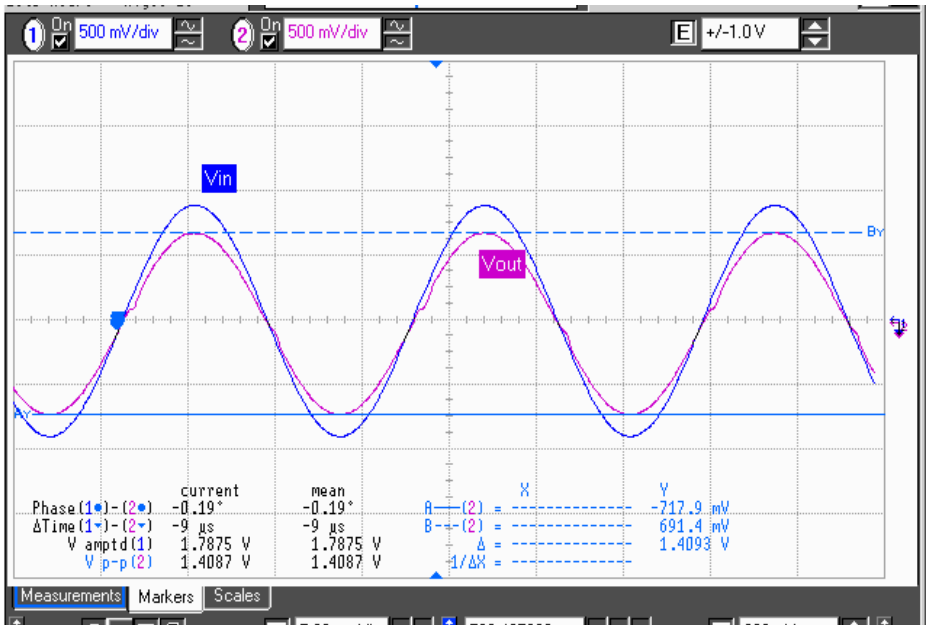


Fig. 5-20 The signals of $v_o(t)$ and $v_i(t)$ of Fig. 10, α~17, n=10 and M=200 and swing is 990mV peak-to-peak and frequency is 30KHz.

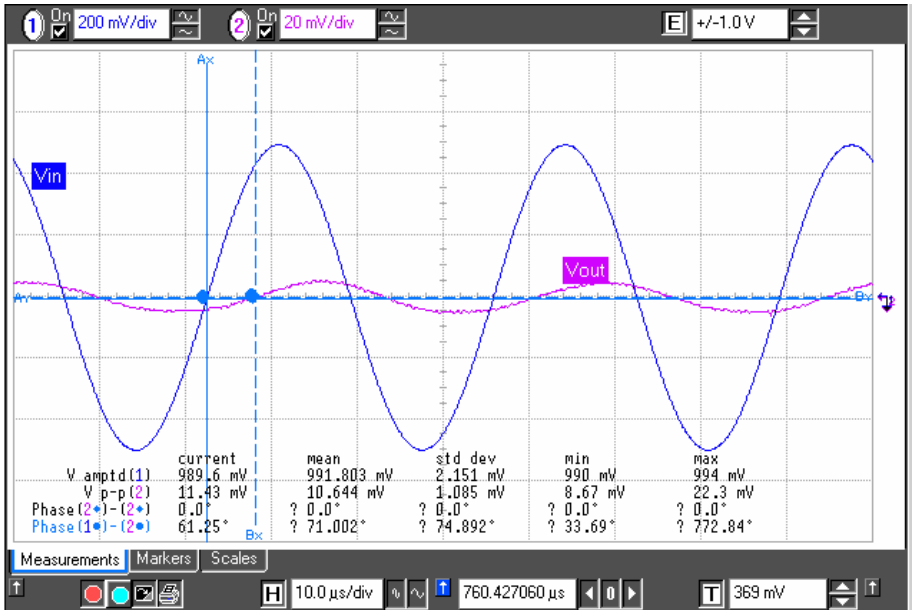


Fig. 5-21 The signals of $v_o(t)$ and $v_i(t)$ of Fig. 10, α~5, n=10 and M=66 and swing is 1785mV peak-to-peak at 60Hz

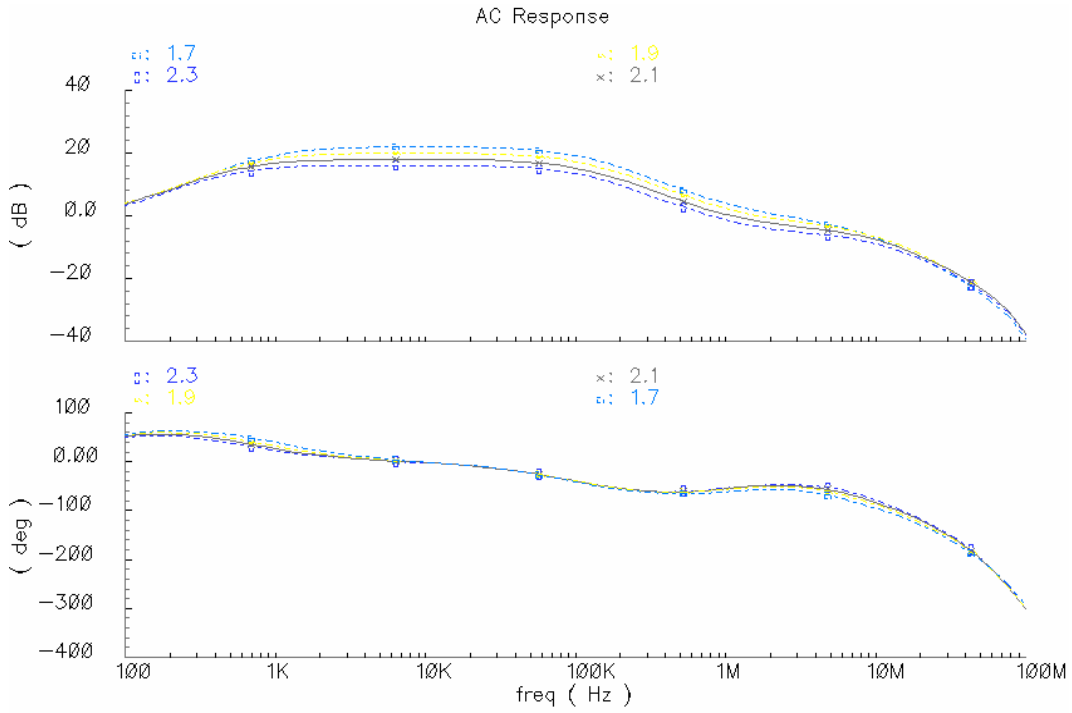


Fig. 5-22 Magnitude and phase of the loop I for different V_{tune} (1.7-2.3) when C=80pF and n=10

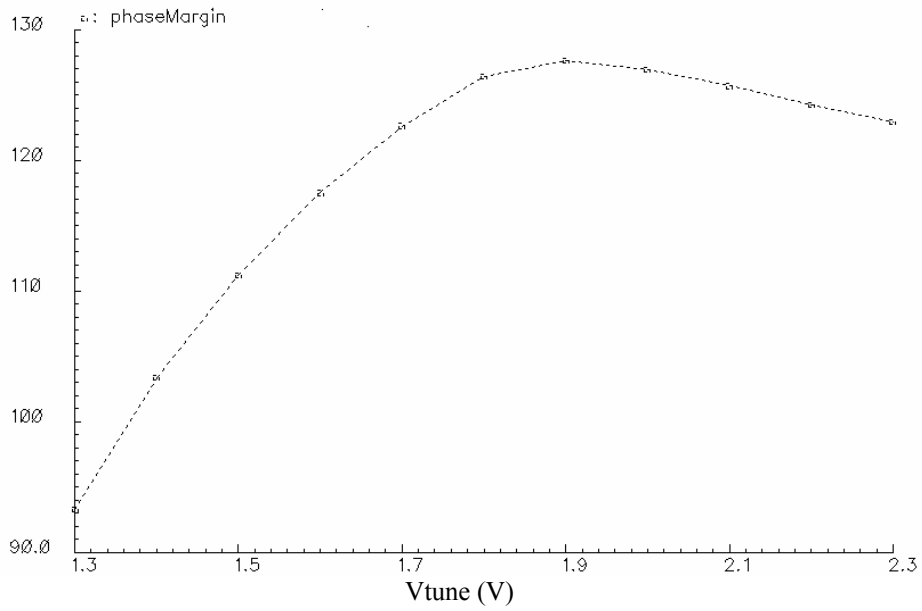


Fig. 5-23 Phase margin of the loop I for different V_{tune} (1.3-2.3) when C=80pF and *n*=10

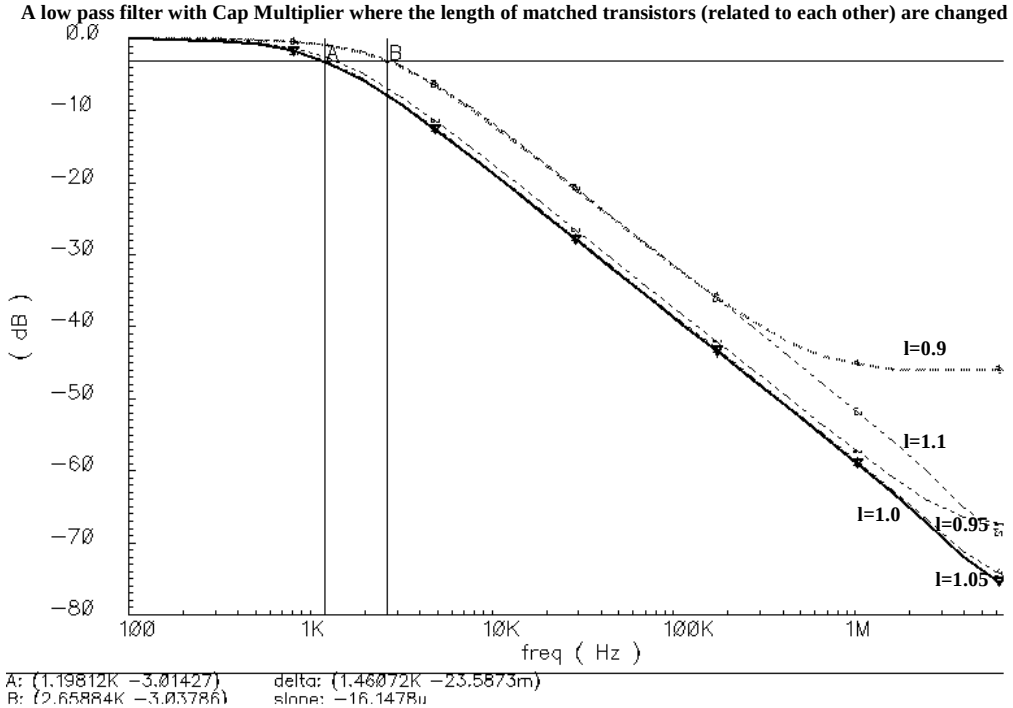


Fig. 5-24 Magnitude of the low pass filter's transfer function when the length of transistor M_4 is varied from -10% to 10%

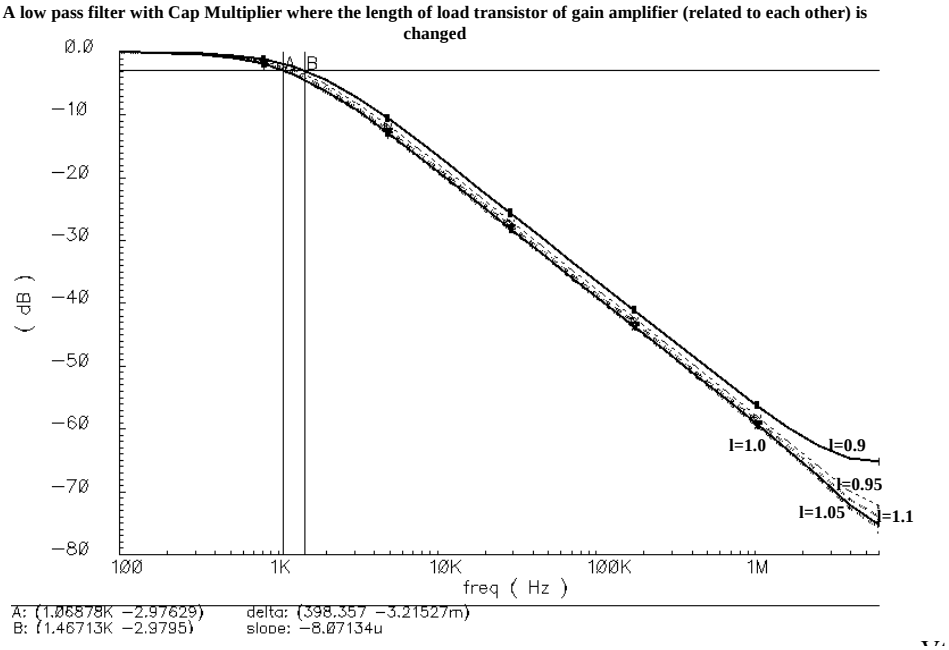


Fig. 5-25 Magnitude of the low pass filter's transfer function when the length of transistor M_{5A} is varied from -10% to 10%

CHAPTER VI

CONCLUSION

A Conclusion

This dissertation presented a brief explanation about concepts of designing a TIA. A new differential RGC TIA was introduced and its features were detailed. Furthermore, a new high sensitive, wide dynamic range variable-gain TIA was presented. It employed a RGC amplifier and an OTA as the feed forward gain element. To achieve wide bandwidth design goals, a boosting amplifier was utilized. Due to peak monitoring and gain reduction, the linearity is guaranteed and overloading capability is increased. Biasing current level is reduced to lower noise and power dissipation. The variable-gain TIA in a 0.35μm CMOS technology is realized. It provides a BER less than 10^{-12} for a current from 6μA-3mA at 3.3V power supply. For more than ten times variations of the transimpedance gain, from 0.1kΩ to 3kΩ, -3dB bandwidth is higher than 1.7GHz for a 0.6pF photodiode capacitance. The power dissipations for the highest and the lowest gains are 8.2mW and 24.9mW; respectively, and when the equivalent input noise current spectral density is found to be less than 14pA/√Hz inband for the highest gain. In addition, the transimpedance amplifier has high noise immunity, wide input dynamic range and low power dissipation, and hence, compares favorably to other recently reported transimpedance amplifiers developed for optical transceiver applications. A prototype implementation of the proposed transimpedance amplifier has also been reported.

A novel procedure for designing uniform multistage amplifiers for high frequency applications was proposed. The method uses multi-pole enhancement while it employs identical, inductor-less and simple stages. It has several advantages such as bandwidth increase with increasing number of stages and tunability of bandwidth. The sensitivity of CMA's performance

to process variations of stages in comparison with that of MA to process variations of stages, when it uses the conventional peaking technique, is reduced. The intrinsic capacitances within transistors are used by the active negative feedbacks to expand the bandwidth. While all stages of the proposed MA topology are identical, the bandwidth can be several times more than that of a single stage amplifier, and the gain-bandwidth product can be extended several times. The design procedure is presented and exemplified by designing a tunable 6-stage CMA in a 0.35μm CMOS process. Measurement results show that the gain of the amplifier can be varied between 16 dB and 44 dB within 0.7-3.2GHz bandwidth with less than 5.2nV/√Hz noise. The die area of the amplifier is 175μm×300μm.

To increase the speed of input transistor of the forward amplifiers, the drain-source drop voltage is reduced by employing boosting amplifier. For 2mV to 2V input swing voltage, a 600mVoutput swing voltage would be available. A 43dB overall gain and 2.91GHz bandwidth could be achieved, while the peak–to–peak jitter for 2.5Gb/S (2^{31}-1 pseudo-random) bits is less than 150pS for 2mV input swing voltage. The die area of the amplifier is 320μm×320μm.

A tunable design technique for capacitance multiplication was presented. The proposed method combines current and voltage mode techniques to enlarge the multiplication factor. To improve matching in current mirrors, drain-source voltages of paired transistors were equalized by means of error amplifiers. For the same swing as that of the current mode technique previously reported, the proposed technique provides a wider bandwidth and twice the multiplication factor. For the same swing as that of the voltage mode technique, the proposed technique provides much wider bandwidth and (n+1) times the multiplication factor. The prototype IC implementation in a 0.5μm CMOS technology of the capacitance multiplier can be tuned to have a multiplication factor of 106.3. While 80pF capacitance is used, the effective capacitance varies from 1.22nF up to 8.5nF. At low frequencies and the frequencies more than

two or three times the corner frequency the capacitance multiplier is linear. Measurement of a loop filter shows 50μA current consumption for M=50. The input resistance is more than 1MΩ and the noise of the circuit is less than-103dBm/Hz at 100KHz.

B Suggestions for Further Studies

The gain control loop in the variable gain (fully) differential TIA can be fully exploited if it is used as a fast automatic gain control loop to optimize the performance of TIA in different rates and input powers. Three most important parameters which can be optimized are jitter, noise and power dissipation.

The uniform CMA could have a wide bandwidth while the gain is changeable. Moreover, for a special gain the bandwidth can be varied. Thus, in a procedure of optimization the bandwidth and the gain of CMA can be adjusted in a way that power dissipation and jitter are reduced. A loop can be employed to adjust the current of feedback and forward amplifiers online. Such optimization can be done for different rates and input swing voltage.

Furthermore, the jitter can be measured and used to update the DC cancellation circuit specs in a way that while the rate and power of input signal are changed the DC negative feedback loop (the DC cancellation circuit) can be adjusted. It must guarantee the low frequencies data in different power can be amplified when the DC frequencies are eliminated.

Using the non-uniform CMA can give greater chance to reduce group delay variation and jitter. Furthermore, a practical way to design different stages can be arrived at while the group delay variation and produced jitter are minimized. Moreover, to produce different delay CMA can be employed. This feature can be used in equalizers to compensate the deformation of digital data received in high speed lines. Expanding characterization and analysis in non-uniform CMA structure is necessary.

The CMA can be implemented in higher frequencies where using inductors are more

affordable. Employing two peaking techniques can improve the performance such amplifier.

REFERENCES

[1] P. Kapur, and K. C. Saraswat, "Comparisons between electrical and optical interconnects for on-chip signaling," in *Proc. of IEEE International Interconnect Technology Conf.*, June 2002, pp. 89–91.

[2] H. Cho, P. Kapur, and K. C Saraswat. "Power comparison between high-speed electrical and optical interconnects for interchip communication," *Journal of Lightwave Technology.,* vol. 22, pp. 2021–2033, Sept. 2004.

[3] Li, E. Towe, and M.W. Haney, "Special issue on optical interconnections for digital systems," in *Proc. of the IEEE*, vol. 88, June 2000, pp. 723–727.

[4] R. Y. Chen , T. Hung, and C. Hung, "A CMOS infrared wireless optical receiver front-end with a variable-gain fully-differential transimpedance amplifier," *IEEE Trans. on Consumer Electronics*, vol. 51, pp. 424-429, May 2005.

[5] Infrared Data Association. IrDA-Standard-Physical Layer, Version 1.3, March 2001. Available: http://www.irda.org.

[6] A.J. Joseph, D.L. Harame, B. Jagannathan, D. Coolbaugh, D. Ahlgren, *et al*., "Status and direction of communication technologies-SiGe BiCMOS and RFCMOS," in *Proc. of the IEEE,* vol. 93, Sept. 2005, pp. 1539-1558.

[7] S. M. R. Hasan, "Design of a low-power 3.5–GHz broad-band CMOS transimpedance amplifier for optical transceivers," *IEEE Trans. on Circuits Sys. I*, vol. 52, pp. 1061-1072, June 2005.

[8] W. Goraski, *Optical Networking and WDM*. Berkeley, CA: McGraw-Hill, 2001.

[9] I. A. Prokes, and V. Zeman, "Optical receiver performance analysis," in *Proc. of IST2001*, Tehran, Iran, 2001, pp. 135–138.

[10] F. M. Chik and L. He, "Design and analysis of a broad band transimpedance amplifier," in *Proc. of ICMMT 4th International Conference on Microwave and Millimeter Wave Technology*, August 2004, pp. 296-299.

[11] B. Kwark, D. S. Ma, H. Seo; K. Ham, and M. S. Park, "Low-cost AlGaAs/GaAs HBT multi-gigabit limiting amplifier packaged with a new plastic air tight cavity encapsulation process," *IEEE Trans. on Components, Hybrids, and Manufacturing Technology*, vol. 21, pp. 309 –313, August 1998.

[12] B. Razavi, "Design of high-speed circuits for optical communication systems," in *Proc. of the IEEE Custom Integrated Circuits Conference (CICC)*, May, 2001, pp. 315–322.

[13] Standard Manual of ANSI TI.105.06-1996. Available: www.ansi.org/

[14] *SERDES Handbook*, Lattice Semi. Co. April 2003. Available: www.latticesemi.com/account/_download.cfm?AMID=5280

[15] XAUI (Extent attachment unit interface) in *10Gbs USER Conf.* 2002. Available: www.10gea.org .

[16] "Media access control parameters, physical layers and management parameters for subscriber access network,'' *Standard Draft IEEE PX02.3ah*, Oct. 2002. Available: www.ieee802.org/3/efm/public/comments/d3_1/D3_1_proposed_responses.pdf .

[17] W. Chen, and R. Gan, "1.8V, Variable gain transimpedance amplifiers with constant damping factor for burst-mode optical receiver," in *Digest of Papers*, *IEEE Radio Frequency integrated Circuits (RFIC) Symposium,* June 2005*,* pp. 691-694.

[18] K. Okada, and N. Miki, "Fiber-optic subscriber systems for point-to multipoint transmission architecture," in *Proc. ECOC'92*, Berlin, Germany, 1992, pp. 102-105.

[19] C. Chen , C.-M. Tsai, D. Li, and L. Huang, "A 1.25Gbps burst-mode receiver IC with extended dynamic range," in *Digest of Papers*, *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium,* June 2005, pp. 625-628.

[20] M. Nakamura, N. Ishihara, Y. Akazawa, and H. Kimura, "An instantaneous response CMOS optical receiver IC with wide dynamic range and extremely high sensitivity using feed-forward auto-bias adjustment," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 991-997, Sept.1995.

[21] Y. Ota, and R.G. Swartz, "Burst mode compatible optical receiver with a large dynamic range," *Journal of Light Wave Technology,* vol. 8, no. 12, pp. 1897-1903, 1990.

[22] C. Kromer, G. Sialm, T. Morf, M. L. Schmatz, F. Ellinger, *et al.*, "A low-power 20-GHz 52-dB transimpedance amplifier in 80-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 885-894, Oct. 2004.

[23] B. Razavi, *Design of Integrated Circuits for Optical Communications*, Boston, MA: McGraw-Hill College, 2002.

[24] J. Powers, *An Introduction to Fiber Optic Systems*, Boston, MA: McGraw-Hill College, 1997.

[25] C. Q. Wu, E. A. Sovero, and B. Massey, "40 GHz transimpedance amplifier with differential outputs using InP/InGaAs heterojunction bipolar transistors," in *Digest of Papers of IEEE GaAs IC Technology Symposium,* Monterey, CA, Nov. 2002, pp. 63–66.

[26] N. Haralabidis, S. Katsafouros, and G. Halkias, "A 1 GHz CMOS transimpedance amplifier for chip-to-chip optical interconnects," in *Proc IEEE Int. Symp. Circuits Systems*, vol. 5, May 2000, pp. 421–424.

[27] B. Razavi, "A 622 Mb/s 4.5 pA (Hz)-0.5 CMOS transimpedance amplifier," in *Dig. Tech. Papers, IEEE Int. Solid-State Circuits Conf.*, Feb. 2000, pp. 162–163.

[28] C. Toumazou, and S. M. Park, "Wideband low noise CMOS transimpedance amplifier for gigahertz operation," *Electron. Lett.,* vol. 32, no. 13, pp. 1194–1196, Jun. 1996.

[29] T. Yoon and B. Jalali, "1 Gbit/s fiber channel CMOS transimpedance amplifier," *Electron. Lett.* , vol. 33, no. 7, pp. 588–589, Mar. 1997.

[30] S. S. Mohan, M. M. Hershenson, S. P. Boyd and T. H. Lee, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, Mar. 2000.

[31] C. Tsai, "20mW 1.25 Gbit/s CMOS transimpedance amplifier with 30 dB dynamic range," *Electron. Lett.*, vol. 41, no. 3, Feb. 2005.

[32] S. Chandrasekhar, A.H. Gnauck, W. T. Tsang, F. S. Choa, and G.J. Qua, "A monolithic 5Gb/s p-i-n/HBT integrated photoreceiver circuit realized from chemical beam epitaxial material," *IEEE Photonics Technology Letters* , vol. 3, pp. 823 –825, Sept. 1991.

[33] H. Tran, F. Pera, D. S. McPherson, D. Viorel, and S. P. Voinigescu, "6k Ohms 43-Gb/s Differential Transimpedance-Limiting Amplifier With Auto-Zero Feedback and High Dynamic Range," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1680-1689, Oct. 2004.

[34] S. M. Park, and C. Toumazou, "A packaged low-noise high-speed regulated cascode transimpedance amplifier using 0.6μm N-Well CMOS technology," in *Proc. of the 26th European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2000, pp. 432-435.

[35] T. Vanisri, and C. Toumazou, "Integrated high-frequency low-noise current-mode optical transimpedance amplifiers: theory and practice," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 6, pp. 677–685, Jun. 1995.

[36] S. M. Park, and H. J. Yoo, "1.25-Gb/s regulated cascode CMOS transimpedance amplifier for gigabit Ethernet applications," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, Jan. 2004.

[37] J. Leeb, J. Knorr, and H. Zimmermann, "Sensitivity-enhanced OEIC with capacitance multiplier for reduced lower-cutoff frequency," in *Proc. of the 2004 International Symposium on Circuits and Systems (ISCAS)*, May, 2004, pp. 829-832.

[38] J. Martínez-Castillol, A. Díaz-Sánchez, R. S. Murphy, and J. L. Finol, "Linearity in two optical receiver structures for high-frequency applications," in *Proc. 5th IEEE International Caracas Conference on Devices, Circuits and Syst*., Nov., 2004, pp. 126-129.

[39] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, New York, NY: 4th ed., Oxford University Press, 1998.

[40] D. A. Johns and K. W. Martin, *Analog Integrated Circuit Design*, New York, NY: John Wiley & Sons: 1997.

[41] Z. Chang, and W. M. C. Sansen, "Low-noise, low-distortion CMOS AM wide-band amplifiers matching a capacitive source," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 3, pp. 833–840, Mar. 1990.

[42] W. L. Wolfe, *Introduction to Infrared System Design*, The International Society for Optical Engineering (SPIE) Press, vol. TT24, 1996.

[43] W. Chen, and C. Lu, "A 2.5 Gbps CMOS optical receiver analog front-end," in *Proc. of IEEE Custom Integrated Circuits Conference (CICC),* pp.359- 362, May 2002.

[44] K. Schrödinger, J. Stimma and M. Mauthe, "A fully integrated CMOS receiver front-end for optic gigabit Ethernet," *IEEE Journal of Solid-State Circuits,* vol. 37, pp. 874–880, July 2002.

[45] C. Lu, and W. Chen, "Bandwidth enhancement techniques for transimpedance amplifier in CMOS technologies," in *Proc. 27th European Solid-State Circuits Conference* (*ESSCIRC),* Sept. 2001, pp. 174 – 177.

[46] R. P. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS," *IEEE Journal of Solid-State Circuits*, vol. SC-22, pp. 512–521, Aug. 1987.

[47] D. L. Feucht, *Handbook of analog circuit design*, San Diego, CA: Academic Press, c1990.

[48] E. Sackinger, and W. C. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receivers," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1884–1888, Dec. 2000.

[49] E. Abou-Allam, T. Manku, M. Ting, and M.S. Obrecht, "Impact of technology scaling on CMOS RF devices and circuits," in *Proc. of IEEE Custom Integrated Circuits Conference (CICC)*, May 2000, pp. 361-364.

[50] E. Cherry, "Impedance mismatching in wide-band transistor amplifier design," *IEEE Trans. Circuits and Syst.,* vol. 17, pp. 131 –132, Feb. 1970.

[51] F. Chien, and Y. Chan "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design," *IEEE Journal of Solid-State Circuits*, vol. 34, pp.1167–1170, Aug. 1999.

[52] F. Centurelli, R. Luzzi, M. Olivieri, and A. Trifiletti, "A bootstrap technique for wideband amplifiers," *IEEE Trans. Circuits and Syst-I*: vol. 49, pp. 1474 –1480, Oct. 2002.

[53] M. Vadipour, "Capacitive feedback technique for wide-band amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 90 - 92, Jan. 1993.

[54] Y. Yoon, and B. Jalali, "Front-end CMOS chipset for fiber-based gigabit Ethernet," in *Dig. Tech. Papers of VLSI Circuits Symp.*, June 1998*,* pp. 188–191.

[55] B. Analui, and A. Hajimiri, "A multipole bandwidth enhancement technique for transimpedance amplifiers," in *Proc. of IEEE European Solid-State Circuits Conference (ESSCIRC)*, Sept. 2002, pp. 301 –308.

[56] S. Galal, and B. Razavi, "10G/b limiting amplifier and laser/modulator driver in 0.18um CMOS technology," in *Dig. Technical Papers of the IEEE International Solid-State Circuits Conference (ISSCC)*, Sept. 2003, pp. 315 –322.

[57] R. Schaumann, M.S. Ghausi, and R. L. Kenneth, *Design of Analog Filters: Passive, Active RC and Switched Capacitor,* Englewood Cliffs, NJ: Prentice-Hall, 1990.

[58] B. C. Kuo, *Automatic Control Systems,* Englewood Cliffs, NJ: Prentice-Hall, 1991.

[59] B. Razavi, *Design of Analog CMOS Integrated Circuits,* Boston, MA: McGraw-Hill, 2001.

[60] E.A. Crain, and M.H. Perrott, "A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1/spl mu/s offset compensation," *IEEE Journal of Solid-State Circuits*, vol. 41, pp. 443-451, Feb. 2006.

[61] R. Tao, Z. Wang, T. Xie, H. T. Chen, Y. Dong, *et al.*, "CMOS limiting amplifier for SDH STM-16 optical receiver," *Electronics Lett.*, vol. 37, pp. 236 –237, Feb. 2001.

[62] J. Silva-Martinez, and A. Vazquez-Gonzalez, "Impedance scalers for IC active filters," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS),* vol. 1, May 1998, pp. 151-154.

[63] G.A. Rincon-Mora, and P.E. Allen, "A low-voltage, low quiescent current, low drop-out regulator solid-state circuits," *IEEE Journal of Solid-State Circuits*, vol. 33, pp. 36 –44, Jan. 1998.

[64] G. A. Rincon-Mora, **"**Active capacitor multiplier in miller-compensated circuits," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 26-32, Jan. 2000.

[65] S. Pennisi, "High accuracy CMOS capacitance multiplier," in *Proc. 9th IEEE International Conference on Electronics, Circuits and Systems (IECS)*, vol. 1, Sept. 2002, pp. 389-392.

[66] K. Shu, E. Sanchez-Sinencio, J. Silva-Martinez, and S. Embabi, "A 2.4-GHz monolithic fractional-N frequency synthesizer with robust phase-switching prescaler and loop capacitance multiplier," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 866-874, Jan. 2003.

[67] G. D. Cremoux, Y. Christoforou, and I**.** v. Loo, "A new method for multiplying the Miller capacitance using active components," in *Proc. IEEE Custom Integrated Circuits Conference (CICC)*, May 2003, pp. 697 – 700.

[68] G. D. Cataldo, G. Ferri, and S. Pennisi, "Active capacitance multipliers using current conveyor," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS '98)* vol. 2, 1998, pp. 343-346.

VITA

Name: MohammadReza SamadiBoroujeni

Mailing address: M/S 625, Advanced Micro Devices, 5900 East Ben White Blvd.,

Austin, TX, 78741

Education:

- Ph.D. Electrical Engineering
  Texas A&M University 2000-2006
- M.S. in Electrical Engineering – Electronics
  University of Tehran, *Tehran, Iran* 1993-1996
- B.S. in Electrical Engineering – Electronics
  Isfahan University of Technology, *Isfahan, Iran* 1988-1992

Previously published materials:

- R. Samadi., A. Karsilayan, "Uniform design of multi-peak bandwidth enhancement technique for multistage amplifiers," (Accepted) *IEEE, TCAS I*, 2006
- R. Samadi., A. Karsilayan, "Multi-peak bandwidth enhancement technique for multistage amplifiers," *GLAVLSI*, April 2004
- M. R. Samadi, A. Karsilayan, "Bandwidth enhancement of multistage amplifiers using active feedback," *Proc. IEEE ISCAS*, May 2004
- M. R. Samadi., A. Karsilayan, "Degradation of commercially available DAC ICs in mixed-radiation environment," *Proc. IEEE NSREC*, 2003
- M. R. Samadi, A. Karsilayan, "Design of transimpedance and limiting amplifiers for 10 Gb/s optical communications," *Proc. IEEE MWSCAS*, 2002
- M. R. Samady, *et al.*, "Implementation of serial port interconnections for integrated circuits," *ICM Conference*, Kuwait, 1999