Chapter

Effect of Surface Variations on Resistive Switching

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Abstract

In this chapter, we study factors that dominate the interfacial resistive switching (RS) in memristive devices. We have also given the basic understanding of different type of RS devices which are predominantly interfacial in nature. In case of resistive random access memory (RRAM), the effect of surface properties on the bulk cannot be neglected as thickness of the film is generally below 100 nm. Surface properties are effected by redox reactions, interfacial layer formation, and presence of tunneling barrier. Surface morphology affects the band structure in the vicinity of interface, which in turn effects the movements of charge carriers. The effect of grain boundaries (GBs) and grain surfaces (GSs) on RS have also been discussed. The concentration of vacancies (O_v)/traps/defects is comparatively higher at GBs which leads to leakage current flow through the GBs predominantly. Such huge presence of charge carriers causes current flow through grain boundaries.

Keywords: resistive switching, interface, grain boundary, oxygen vacancy, surface morphologies

1. Introduction

In this chapter, the fundamentals of nanoionic redox based resistive switching materials are described including different modes of switching. The primary parameters have also been discussed which essentially affect the resistive switching behavior. In addition, this chapter encompasses the various physical as well as chemical phenomena occurring at nano level during resistive switching of devices and other related trending technological areas are also included. An introduction to three distinct kinds of redox based resistive switching materials is given followed by their short history and promising applications into device fabrication field. Further, a brief discussion related to requirement and optimization of device performance parameters has been incorporated along with future prospects, challenges and important industrial applications such as memory, logic circuits and so on. The elements that observe resistive switching are driven by a reversible phenomenon taking place between two terminals. This behavior depicts primarily two different resistance values of nonvolatile nature depending on the external electrical bias conditions [1]. However, such a reversible behavior obtained under continuous applied external stimuli can also be achieved within more than two resistance levels commonly called as multilevel resistive switching. The term 'nonvolatile' suggests the retention or preservation of change in resistance level after removal of the external stimuli. Such memristive materials are capable of memorizing these resistance values under the influence of stimuli [2]. Similar to phenomenon of resistive switching, there can be different

possible switching scenarios such as magnetoresistive phenomenon i.e. spin-transfer torque, electrical effects like the leakage current *via* gate oxide layer containing trapped defects, change in structure/phase among amorphous and crystalline phases, and nanoionic redox phenomenon [1]. So, this chapter deals with the phenomenon of nanoionic redox realized due to ion movement within the two terminal based device structure elements and results into different resistance values of the material. In this chapter, a few terminology such as redox-based resistive switching random access memory (RRAM), resistive switching and/or memristive etc. is to be used frequently. Such terms have been essentially included to explain the fundamental physical characteristics of materials showing potential in multilevel switching or analog properties.

2. Resistive system and type of physical mechanism

Following the systematic and consistent study of RRAM devices, it has been realized that the resistive switching material (I) embedded between two metal electrodes (M) plays a key role in switching phenomenon in the metal–insulator–metal (MIM) stratified device structures. In general, MIM devices are referred to sandwiched stacks/layers of metals and insulator. In a simplistic way, the resistive switching effect can be identified phenomenology as the different switching occurring within stratified MIM layered structure. For such device structures, it is comprehensible to understand the different locations of switching while moving vertically from one metal electrode to other. Therefore, there can be following possible switching locations (**Figure 1**):

i. switching taking place in close proximity to interface of either metal electrode

ii. switching at or near middle of the electrode interfaces

iii. switching occurring over or along the whole path formed among interfaces of metal electrodes.

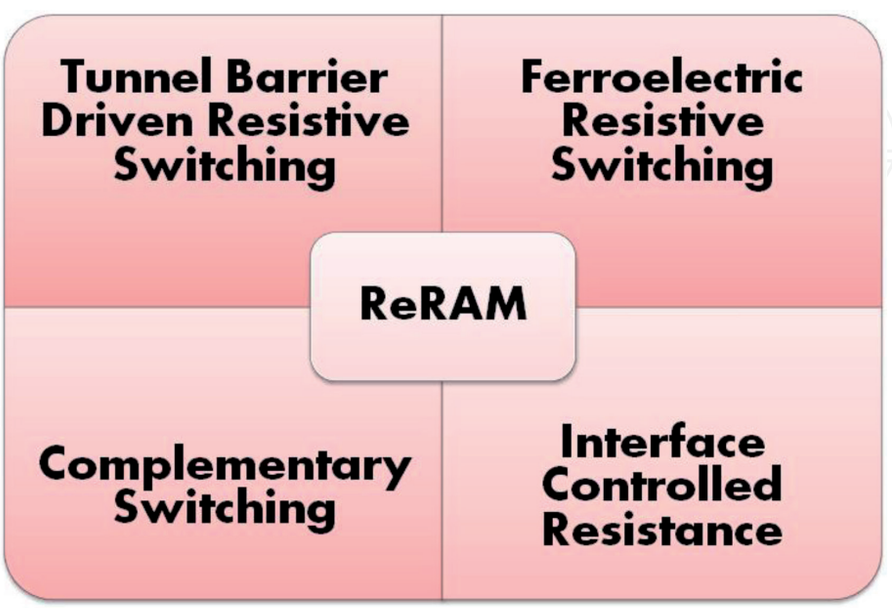

Figure 1.
Different types of resistive switching in which the formation of an interfacial layer between metal electrode and oxide plays a key role in device performance.

On the other hand, switching locations are also possible along perpendicular direction i.e. in the plane of device cross section (lateral direction). Due to this, following switching types are induced:

i. switching based on the formation and rupture of conducting filament (CF) called as filamentary switching.

ii. switching dependent upon contact area. In this case, the switching phenomenon participates to whole device cross section. This results into the scaling of current with the area of cross section. Usually, such a switching behavior is also termed as interface type switching due to the process taking place near the metal electrode.

3. Interface-type switching

The interface type switching is usually of uniform nature and shows area scalable characteristics. ReRAMs devices utilizing metal oxides (initially semiconductor or conductor) are frequently governed by interface type switching phenomena. Such a resistive switching behavior is primarily observed at the metal oxide and electrode interface. In this context, Baikalov *et al*. [1] investigate the resistance behavior of theperovskite oxide based memory devices. It has been demonstrated that an applied electric field significantly modifies the value of contact resistance measured among perovskite oxide and metal electrode. In order to understand the interface type resistive switching, many groups of researchers have given effort to establish different models for switching mechanism. These models are framed using ionic point defects (oxygen vacancies) and their drifted movement or electromigration within the metal oxide materials [1–5]. Some of the models are based on the formation of charge carrier i.e. electrons and/or holes trapping at defect sites [6] and observation of Mott transitions taking place at the interfaces [7, 8]. In the case of ReRAMs, low resistance value (in the range of kΩ) as well as the extended retention behavior (in the range of years) are realized in terms of models based on the modification of atomic or ionic configurations. Therefore, ionic and electronic mechanisms are used to examine the resistive switching characteristics and its origin at microscopic level. For ReRAMs, the interface type resistive switching is primarily predicted to dominant if the resistance of device scales with area. Therefore, Nb-doped $SrTiO_3$ is governed by interface type switching whereas filament based resistive switching prevails in NiO based memory cells [9, 10].

In case of valence change memory (VCM) devices, the resistive-switching phenomenon is understood by the chemical reactions and events taking place near or at the interface of metal electrode and oxide. While characterizing such VCM devices through spectroscopic techniques, the interface related switching behavior is investigated after averaging the area which essentially eliminates the need of any optical arrangements for focusing and/or magnification. The predefined interface dependent switching helps to designate the localized resistive switching phenomenon ascribed to CFs. Due to such interface i.e. thin oxide layer developed between insulator oxide and reactive metal electrode, the external stimuli driven electrochemical modification of interface considerably affects the performance of device. It is known that devices fabricated with reactive electrodes and insulating oxide materials show redox type reactions inducing movement of oxygen towards metal electrode (**Table 1**).

Switching Device Fabrication Technique of Switching layer	Retention (sec)	Endurance (cycle)	Switching Voltage	Type of Switching	Ref
Au/$LaMnO_3$/C-AFM Pulsed injection metal–organic chemical vapor deposition (PI-MOCVD)	—	—	V_{SET} = 4 V, V_{RESET} = −6 V,	Oxygen displacement, Mn oxidation state(+3.6 to +3.1), Work function decreases by 0.28 eV.	[11]
Ag/$Pr_{0.6}Ca_{0.4}MnO_3$/Al Pulsed laser deposition (PLD)	$3.6x10^5$	$12x10^3$	—	Formation and modulation of a rectifying interfacial AlO_x layer	[12]
Pt/$PbTiO_3$/ Nb:$SrTiO_3$(100) Hydrothermal method	$3x10^3$	$5x10^2$	V_{SET} = 4 V, V_{RESET} = −4, −6 V	Trap controlled spacecharge-Limited, M odulation of the Pt/ $PbTiO_3$Schottky-like junction	[13]
Pt/Nb:STO/Pt PLD	10^6	10^7	—	Pt/single crystal Nb:$SrTiO_3$ Schottky junction	[10]
Ti/PCMO/$SrRuO_3$ PLD	—	—	V_{SET} = 6.8 V, V_{RESET} = −6.8 V	Cacomposition, dependence on the RS characteristics, formation of amorphous TiO_ylayers at the interfaces	[14]

Table 1.
Comparison of different parameters for interfacial type RS devices.

3.1 Formation of a blocking layer on conducting oxides

The formation of an interface between oxide layer and an active electrode shows significant impact onto the different phenomena such as nonlinear transport of the charge carriers and affects performance of VCM type devices. In particular, the nonstoichiometric metal oxide layer demonstrates reversible oxidation and reduction at or near the interface which makes device functional. It is known that the interface type switching is mainly observed in conducting oxides like doped manganites utilizing metal electrodes e.g. Al, Ti and Ta etc. Such electrode metals exhibit relatively high oxygen affinity facilitating interface driven switching [9, 15, 16]. In case of $Pr_{0.7}Ca_{0.3}MnO_3$ (PCMO), it has been established that the growing Al metal electrode is oxidized whereas deposited PCMO thin film layer depicts the reduction process during deposition process as evidenced by thorough *in-situ* photoemission studies. Therefore, in interface type resistive switching process, the prominent electronic transport across interface is highly dependent upon the developed interfacial oxide thin layer. Such insulating oxide layers at interface are important in deciding the resistivity behavior during switching of the fabricated devices [17]. In TiN/SiO_2/Fe stacked structure, Feng *et al.* reported RS behavior induced because of thin FeO_x transition layer at SiO_2/Fe interface formed

during processing of plasma-enhanced tetraethyl orthosilicate. However, after incorporating Pt into Fe electrode ($TiN/SiO_2/Fe_{0.73}Pt_{0.27}$) reduces the concentration of Fe in thin FeO_x layer which eventually improved the data dispersion of switching parameters [18]. In another report, the annealing of $TiN/SiO_2/FeO_x$/FePt stratified structure dramatically modifies RS properties. Under optimized annealing conditions, excellent improvements have been observed including distinct reduction in RS parameters such asforming voltage, set/reset voltages, and their dispersions along with higher resistance i.e. ON/OFF ratio [19, 20].

3.2 Electrically induced redox reactions at the Interface

The conducting oxide e.g. manganites or cobaltites based memristive devices that employ reactive metal electrodes practically show uniform electrical conduction throughout the active area of device [9, 21]. It is known that the electrical resistance in case of the fabricated devices is low and increases primarily as a function of the applied bias. Such positive bias is applied onto the top electrode of the fabricated device. A careful analysis employing the cross-sectional TEM along with EELS and HAXPES measurements revealed that the actual thickness of oxide layer formed at or near the interface enhances noticeably due to the electroforming treatment [14, 17]. In $TiN/SiO_2/FeO_x$/Fe device, Chang *et al.* demonstrated multilevel RS characteristics containing thin FeO_x transition layer which essentially assist in achieving controlled current compliance in SET process and stopped voltage during RESET process. Interestingly, the controlled external electric conditions facilitate tunable resistive states. The distinct mechanism for multilevel RS behavior has been realized by distinguishing the electrical behaviors, statistically which indicated the mobile-ion-assisted electrochemical redox governed RESET process [22].

3.3 Schottky-like metal/conducting oxide interfaces

Prior to explaining the resistive switching effects, the realization about the fundamental of the electronic properties related to conducting oxides is very important. Also, the current and voltage (*I-V*) behavior of interface formed at conducting oxide and metal electrode plays a key role in device performance. However, the contact resistance of such interfaces are largely modified by two major effects. One of the two effects is the existence of unwanted chemical reaction of metal electrode with conducting oxide. Secondly, the distinct Fermi level of conducting oxide and metal electrode leads to generation of space charge layer. The high contact resistance of interface is predominantly due to the Schottky barrier. This forms space charge region where essentially the majority charge carriers are depleted. In many cases of memory devices, the different electrode metals not only induce considerable modification in the resistive switching properties but also the contact resistance is affected significantly [6, 15, 23]. In case of stratified $M/Pr_{0.7}Ca_{0.3}MnO_3/SrRuO_3$ (M/PCMO/SRO) and $M/SrTi_{0.99}Nb_{0.01}O_3$/Ag (M/Nb:STO/Ag) where M is top electrode metal, the change in *I-V* characteristics has been discussed utilizing different electrode materials. The authors have used Ti and Au with work functions as ~4.3 and 5.1 eV, respectively whereas SRO possesses the highest value of work functions as 5.3 eV [15]. In present case, PCMO and Nb:STO exhibit only Ohmic contacts with SRO and Ag acting as the bottom metal electrode. It is known that while PCMO semiconducting oxide is dominated by *p*-type behavior, Nb:STO depicts *n*-type conduction. One can realize that the contact resistance between M and *p*-type dominated PCMO oxide is the largest for M with the least work function. Therefore, for PCMO based memory cells, Ti having the lowest work function demonstrates rectifying I-V behavior i.e. hysteretic characteristics distinctive to

resistive switching properties. However, the contact resistance between M and *n*-type Nb:STO increases as the work function of M enhances. This indicates that Nb:STO based memory cells utilizing Au as the top electrode display hysteretic characteristics during *I-V* measurements. These observations are in good agreement with the fact that the rectifying behavior of *I-V* characteristics is governed by Schottky type barrier height formed at the interfaces. Therefore, an important and critical role of Schottky type barrier can be easily perceive in driving the resistive swathing effect in the fabricated memory cells. Considering the highly reactive nature of Ti top electrode material, it is also necessary to take the accounts of different chemical reactions occurring at the interface. For example, Ti being a more reactive metal can chemically react to the semiconducting oxide through the extraction of oxygen ions during film deposition and subsequent annealing procedure. Such events take place when the oxygen vacancies are injected *via* areas in close proximity to the interfaces. These oxygen vacancies are primarily of donor type and hence, capable of modifying the initial donor concentration of *n*-type Nb:STO semiconducting oxide. The considerable enhancement in the amount of donors ensures improved Ohmic contact conductance behavior. On the other hand, *p*-type PCMO oxide experiences the diminished conductivity which eventually results into an insulating type region of PCMO close to the interface. Such a phenomenon is similar to space charge effects which adds up to oxidize Ti metal. Thus, it evokes resistance at interface since the oxidation of Ti forming non-stoichiometric TiO_x has low conductivity.

I-V as well as *C-V* behavior demonstrate a hysteretic type characteristics if the resistance switching is area scalable. This is well explained on the basis of Schottky depletion model through the mechanism of electronic trapping or detrapping [24]. In practice, different contributions from the metal electrode work function, electron affinity of the *n*-type Nb:STO semiconducting oxide and interface trap sates residing within low-*k* interfacial layer are taken into consideration while estimating the accurate Schottky barrier height [25]. Interestingly, a noticeable sign related to electronic trapping or detrapping of bandgap states can be perceived within the depletion region for memory cells where resistive switching characteristics are area scalable. Also, due to small read out currents, a shorter retention time (in the range of 10^2–10^3 s) is measured for such cells which endorses the retention time and current variations obtained for only electronic switching. A voltage-induced unidirectional threshold resistive switching has been reported for Au/NiO/Nb:$SrTiO_3$ devices fabricated by pulsed laser deposition. Interestingly, only positive voltage values demonstrate the forming process controlled threshold resistive switching behavior [26].

Further, Schottky barrier at the interface is altered not only *via* the impact ionization but also depend onto the movement of oxygen vacancies driven applied electric field [15]. In another report, for single crystals of self-doped $SrTiO_3$ (STO), the authors have discussed the effect of electrode engineering with variable work function, device geometry and measurement configurations upon the resistive switching. Additionally, the various metal electrode combinations such as Ti and Pt has been exploited to analyze and manipulate the electrical transport i.e. Ohmic or Schottky type across junctions. It has been concluded that the observed resistive switching behavior is greatly influenced by changing the amount of oxygen vacancies only at or near the interface under an effective applied electrical bias [27]. For most of the switching binary or complex transition metal oxides (i.e. solid electrolytes), it is well known that current transport is the collective manifestation of electronic charge carriers as well as the mobile ions and related ionic defects. There exists cationic interstitials, delocalized electrons and oxygen vacancies in hypo-stoichiometric oxides whereas oxygen interstitials, delocalized holes and cationic vacancies are the major charge carriers in hyper-stoichiometric oxides.

In general, both the electron affinity of metal oxide materials and metal electrode work function define the Schottky barrier height. This implies the fact that the metal work function is believed to be directly related to the Schottky barrier. Nevertheless, in practice, the Schottky barrier height is considerably affected by the formation of metal electrode/oxide interfacial layer providing an additional capacitor i.e. insulator type thin slab. In this context, Cowley and Sze revealed that formation of such capacitive layers evoke a definite and noteworthy drop in voltage which ultimately alters the ideal height of Schottky barrier.

Moreover, the formation of interface between metal electrode and oxide layer is also described in terms of the Helmholtz plane and diffuse double layers [28]. It has been thoroughly discussed that there exists an intrinsic electrochemical potential difference at the interface of metal electrode and oxide which induces the transfer of electrons among oxide layer and metal. Such an event produces dipole layer at the interface due to the movement of electrons ensuing space charge effect. Under applied electrical bias, electronic charge carriers, ions and related ionic defects take part in screening the electric field via the diffuse double layer in the oxide region. However, there is a little screening of electric field at the metal electrode side because of sufficiently high enough concentration of electrons. It is evident that the screening length is extended much deeper inside the oxide layer than that of metal electrode owing to large difference in the concentration of charge carriers and electrons. While the first screening of electric field is caused by the ions residing over the Helmholtz plane, the second screening is primarily due to the electronic charge carriers, ions and related ionic defects present in the diffuse double layer [28].

For the most frequently employed metal oxides such as Ta_2O_5, HfO_2, and SiO_2 based memristive devices with compatible metal electrodes like Ta, Hf, and Ti have been extensively studied. For example, HfO_x/AlO_y-based homeothermic devices depict low-power and homogeneous RS behavior useful synaptic applications [29]. In vanadium-based devices, Lin *et al.* demonstrate excellent RS characteristics through interface where localized transition occurs [30]. Hsieh *et al.* discussed mitigation of critical issue of short-term relaxation in HfO_x/CeO_x derived RRAM devices [31]. In case of bilayer structure devices employing $Ni/SiN_x/HfO_2/p^{++}$-Si stacks, a self-rectifying has been shown to improve the sneak-path current emerging in the crossbar arrays fabrication process. Such bilayered devices provided enhanced rectification ratio usually $>10^4$. It has been revealed that during negative bias, the formation of large Schottky barrier of HfO_2 facilitate the reduction in current [32]. The progressive and consistent investigations have shown that interfacial layer exists inherently between the metal electrode and oxide. However, the oxygen affinity of metal as well as chemical and thermodynamic strength of the oxide layer determines the degree of oxidation of metal electrodes. Thus, the performance of fabricated device is highly dependent onto the extent of interfacial layer altering the initial crystal structure of oxide layer [33].

4. Tunnel barrier driven resistive switching

The tunnel ReRAM based on oxides is peculiarly known as the nonvolatile memory that demonstrate area dependent resistive switching properties. Unity Semiconductor Company first introduced the tunnel ReRAM and then Rambus Labs followed the work. ReRAM employs thin insulator type oxide layer to control the current through quantum-mechanical tunneling as magnetic RAM. In contrast to other oxide based RRAM system showing movement of oxygen ions, the quantum-mechanical tunneling effect within the insulator or barrier provides a more regulated current values in different processes such as SET, RESET and

Read-out which facilitate improved device performance. The mobile oxygen ion traveling across the insulator or barrier tunnel shows considerable impact onto the tunnel properties. Also, an appropriate change in thickness of tunnel barrier or oxide effectively helps into regulate the device current levels. Moreover, such a control over *I-V* characteristics for SET and RESET states offers transistor or diode-like selector less fabrication of passive cross-point configuration (1R) based working memory devices. This type of operation memory devices exhibit self-select feature. A precise and optimized tunnel device geometry with regulated current conduction serves high device yeild due to small variability in cell-to-cell and wafer-to-wafer operation. Further, the multibit storage can also be realized even in a single memory cell owing to an analog transition of the SET and RESET processes. The area dependent switching properties also enables smaller technology nodes in near future. Since tunnel ReRAM is still in development stage, it suffers from a few critical issues like ease of processing, integration and optimum retention time [34].

The tunnel ReRAM is also a stratified structure containing a very thin tunnel oxide layer (in the range of 2–3 nm only) placed between conducting oxide and metal electrode. The conducting meal oxide is usually a metallic type perovskite oxides including (Pr, Ca)MnO_3 or highly conducting La or Nb doped $SrTiO_3$. The stable electrical insulators possessing high-*k* oxides such as ZrO_2 or HfO_2 are employed generally as the tunnel oxide barrier layer [35]. The noble metals like Pt are utilized as electrodes for electrical biasing. The use of noble electrode metal is of utmost since they do not

Switching Device Fabrication Technique of Switching layer	**Retention (sec)**	**Endurance (cycle)**	**Switching Voltage**	**Type of Switching**	**Ref**
$Ni/Si_3N_4/SiO_2/p+$ -Si low-pressure chemical vapor deposition (LPCVD)	—	—	V_{SET} = 4 V, V_{RESET} = −2 V,	Si_3N_4 (5 nm) as a resistive switching layer and SiO_2 (2.5 nm) tunnel Barrier	[36]
$Pt/Ti/HfO_2/TiOx/Pt$ Atomic layer deposition (ALD)	10^4	$3x10^2$	—	HfO_2 (4 nm) as a resistive switching layer and TiO_x (6 nm) tunnel barrier	[37]
$Pt/Ta_2O_5/TaO_x/TiO_2/Pt$ Atomic layer deposition (ALD)	10^{10}	10^4	—	TiO_2 (4 nm) as a resistive switching layer and Ta_2O_5(6 nm) tunnel barrier	[38]
$Ti/HfO_2/Al_2O_3/TiN$ Atomic layer deposition (ALD)	—	—	—	HfO_2 (10 nm) as a resistive switching layer and Al_2O_3 (1 nm) tunnel barrier	[39]

Table 2.
Comparison for of switching parameters for tunnel barrier type RS devices.

react chemically with oxygen ions inducing formation of unwanted interfacial layer. The mechanism of tunnel ReRAM is radically different to interface based switching devices discussed above. In order to obtain good conductivity, both the conducing metal oxides e.g. (Pr, Ca)MnO_3 and tunnel oxide layer are processed at high temperature to ensure optimum crystallinity of the deposited films (**Table 2**) [34].

5. Ferroelectric resistive switching

In the late year *1970*, the first experimental work by Esaki reported the resistive switching behavior utilizing reversal of polarization in ferroelectric material [40]. This report followed many other ferroelectric based resistive switching materials such as the perovskitetitanates including $PbTiO_3$ [41], $BaTiO_3$ [42], and multiferroic system e.g. $BiFeO_3$ [43]. With consistent investigations, researchers have explained the resistive switching in ferroelectrics [40–43]. Usually, there exists two different types of ferroelectric based resistive switching memory. Considering the conduction mechanism, first is the ferroelectric tunneling junction and other is known as ferroelectric diode type memory. An ultrathin tunneling ferroelectric barrier is the primary component of the ferroelectric tunneling junctions. For such junctions, one can observe significant modification in tunnel oxide barrier height because of polarization reversal occurring in the ferroelectric materials. The ferroelectric tunnel barrier exhibits potential distribution of asymmetric type which evokes change in the height of barrier when reversal of polarization takes place. For memory cells, when both the metal electrodes are different that impose distinct screening lengths, the asymmetric potential distribution is achieved [44, 45]. The asymmetric behavior of potential has also been examined after placing a non-ferroelectric ultrathin layer onto the ferroelectric oxide layer [46]. The presence of dielectric ultrathin layer acts as a separation wall which essentially divides polarization charge in ferroelectric oxide layer and screening charge in metal electrode. Therefore, the non-ferroelectric i.e. dielectric layer possesses a certain distribution of the potential. In case of ferroelectric diode, the interface between metal electrode and ferroelectric layer observes the formation of Schottky type barrier. Upon the reversal of polarization in ferroelectric layer, the height of Schottky type barrier correspondingly changes (**Table 3**) [41].

Switching Device Fabrication Technique of Switching layer	Retention (sec)	Endurance (cycle)	Switching Voltage	Ref
Cu/$Pb(Zr_{0.2}Ti_{0.8})O_3$/ $La_{0.7}Sr_{0.3}MnO_3$/$SrTiO_3$	—	—	V_{SET} = 0.8 V, V_{RESET} = −2.1 V,	[45]
2-nm C-AFM Tip/BTO/30-nm LSMO ($La_{2/3}Sr_{1/3}MnO_3$)	—	—	V_{SET} = 3.5 V, V_{RESET} = −3.5 V	[42]
Ag/$BiFeO_3$/Ag	—	—	V_{Pulse} = 150 V, −150 V	[43]

Table 3.
Comparison of switching voltages for ferroelectric type RS devices.

6. Complementary switching

The complementary resistive switching (CRS) is the switching mode in which two distinct locations of switching are found. CRS devices contain variable concentration of defects within the switching layer. In particular, SET process occurs if the oxygen vacancies accumulate at either of metal electrodes. This takes place on

account of the reduced oxygen vacancy concentration at the other end [47]. It states that both the interfaces cannot switch simultaneously. One needs to switch OFF when the other is ON. The mechanism of CRS is explained in terms of the distribution of defect within the insulating i.e. switching layer. After the applied electrical bias (positive or negative), the movement of defects towards certain electrode is observed. Depending upon the accumulation of defects at one or opposite interface, the SET and RESET states occur giving current levels under +ve and/or -ve bias conditions. With the help of either current compliance condition or sudden stop of bias at current peaks, only the SET state is obtained and one can limit the RESET state to takes place giving rise to bipolar switching [48]. Compared to other resistive switching devices, CRS provides slow and steady SET operation at one interface rather than an abrupt transition in current level. At the same time, RESET operation occurring at other interface eliminates the need of positive feedback [49]. It is known that an individual VCM device can exhibit CRS operation. For VCM devices with symmetric stack and similar top and bottom metal electrodes shows CRS phenomenon (**Table 4**).

Switching Device	Retention (sec)	Endurance (cycle)	Switching Voltage	Reason for Switching	Ref
$HfO_2/Al_2O_3/TiO_x$(HAT)	10^4	10^3	V_{SET} = −3.8 V, V_{RESET} = −3.5 V,	Anionic redistribution in HfO_2 and TiO_x layers, leaving Al_2O_3 as tunnel barrier	[50]
TiN/HfOx/Pt	10^4	10^3	V_{SET} = −0.86 V, V_{RESET} = 1.08 V,	BRS of device transforms to CRS after transitional processes through controlling compliance current	[51]
Pd/ Ta_2O_{5-x}/TaO_y/ Pd	~3.5x10^3	2x10^3	V_{SET} = −0.9 V, V_{RESET} = 1.1 V	Different oxygen compositions of Ta_2O_{5-x} and TaO_y layers, oxygen vacancies (V_O) can be exchanged between two layers.	[52]
Ta/ZnSnO/ TiN	10^4	2x10^3	V_{SET} = −2 V, V_{RESET} = 1.5 V	TaO and TiON interface layers are formed at the top Ta/ZnSnO and bottom ZnSnO/TiN interfaces	[53]

Table 4.
Comparison for complementary type RS devices.

7. Interface controlled resistance (ICR)

The redox reaction driven resistive switching is dominated by the mechanism in which the charged defects or impurities rearrange at the metal electrode and oxide interface. Such a rearrangement of mobile defects reduce the contact resistance due to large interface charge concentration which ultimately decreases the contact barrier height as well as width. This process is examined through the Mott–Schottky theory dealing with the contact formed among metal and non-metal elements. For nanoionic devices, the resistance switching mechanism based on the formation of an interfacial layer has been investigated in a wide variety of metal oxides including TiO_2 [54], HfO_2 [55, 56], ZrO_2 [57, 58] Ta_2O_5 etc. It is well known that the metal oxides are more prone to oxygen ion i.e. ease of defect formation and hence, largely show nonstoichiometric nature. Therefore, the inherent nonstoichiometric nature of metal oxides produce several lattice point defects or impurities like vacancies and/or interstitials of metal and oxygen ions. Such defects present in metal oxides can be similar to acceptors or donors and are capable of modifying the electronic properties and the switching characteristics of device. Owing to sufficient concentration of charge carriers i.e. defects, such metal oxides can act equivalent to extrinsic semiconductor and thus, the classical semiconductor model governs the electronic conduction.

In order to highlight three main differences between nonstoichiometric metal oxide and classical semiconductor, researchers categorized them into a particular group known as mixed ionic–electronic conductors or chemiconductors [59, 60]. Followings are the distinctions used for classification:

i. the variation in oxide composition i.e. nonstoichiometric feature induces defect ions producing donors and acceptors i.e. *dopants* in chemiconductors,

ii. under applied electrical bias, while the defect ions are able mobile within the lattice, dopants in semiconductors are fixed at certain positions in lattice, and.

iii. however, the dopants are non-uniformly distributed at the interface, in particular.

Apart from the above differences, the classical semiconductor acts similar to chemiconductors possessing sufficient nonstoichiometric feature. Therefore, their electrical characteristics are described in the framework of the Mott–Schottky model producing Schottky barriers at the interface (**Table 5**).

Switching Device	Retention (sec)	Endurance (cycle)	Switching Voltage	Reason for Switching	Ref
Al/MoO_x/Pt	—	$5x10^2$	V_{SET} = −3 V, V_{RESET} = −2 V,	Self-rectifying and interface-controlled	[61]
TiN/ZrO_2/Pt	120	—	—	oxygen vacancy conducting filamentary paths	[57]
s-In/ NSTO/o-In	10^4	$3.5x10^3$	—	Schottky interface	[62]

Table 5.
Comparison for interface controlled resistance RS devices.

8. Effect of grain surface area and grain boundary

Interfacial type resistive switching (RS) in memristive device is dominated by the surface morphology and properties. Under the application of an external voltage bias, the density distribution of defects/vacancies can vary along the film thickness, which affects the bandgap of material and produces unpredictable behavior in resistive switching response. These uncertain changes at the interface, barrier bandgap leads to a change in the sample's resistance in an interfacial RS which is extremely sensitive to interfacial properties.

Generally, interface is defined between two different materials systems but sometimes interface can also be defined at the regions which have the same composition and crystal structure but different crystal orientations (even inside the same solid such as grain boundaries (GBs)-including tilt and twist boundaries-twin boundaries and stacking faults) [34]. Moreover, an interface is affected by the several external environment conditions such as air, vacuum, moisture and some other material properties such as the crystallinity of solids at the interface. However, the defect chemistry is comparatively different in the proximity of a charged interface (GB) from the bulk situation (single crystal). Basically, charged interface induces the redistribution of the mobile charge carriers in the space-charge layer region while in bulk, the electroneutrality has been played an important role (at equilibrium) between differently charged point defects. In this section, the effect of grain boundaries (GBs) and grain surfaces (GSs) on RS have discussed.

Oxygen vacancies and defects are considered responsible for resistive switching phenomena in oxides materials. For nanoscaled materials, GBs conductivity is directly proportional to grain size, and it may modulate according to the direction of current flow (perpendicular and parallel direction of GBs) [63]. However, the position of the GBs is dependent on the shape and size of the grain J. Maier [63] has reported that in case of yttria-doped zirconia if the grain size decreases at particular dimension (~ 50 nm in diameter) then most of the current passes perpendicular to the GB axis and the conductivity parallel to GB becomes negligible. Further, the formation of GBs when two adjacent and equally oriented grains are rotated to each other and twisted GB occurs when the rotation axis is perpendicular to the boundary. On the other hand, if the rotation axis is lied in the boundary plane, a tilted boundary is resulted [34]. Moreover, the degree of rotation also affects the coherence of the final grain boundary. GB with minimum rotation angle can be treated as an group of edge dislocations and aggregation of screw dislocations [34]. The concentration of oxygen vacancies (O_v) is comparatively higher at GBs which leads to leakage current flow through the GBs predominantly [64]. Any variation in O_v will be closely related to grain boundary and grain surface area. In some polycrystalline oxide thin film, structural defects, grain boundaries and local nonstoichiometric regions are responsible for high leakage current. Further, high electrical stress due to applied electrical potential, induces traps/cracks along the GBs. Induced traps/cracks also increases the leakage current and size of the conduction region at the GBs as compared to the grain regions [65]. In recent years, the ab initio calculations and conductive atomic force microscopy (CAFM) have demonstrated to study the charge transport through grain boundaries in polycrystalline HfO_2 [66].

The space-charge conduction model for acceptor-doped zirconia suggests that the lower ionic conductivity in zirconia occurs due to the depletion of oxygen vacancies and excess the positive charge laying in the GB core [67, 68]. However, dislocations appeared in YSZ single crystal due to plastic deformation does not improve the material's electrical transport significantly [69]. Further, the resistive switching in WO_3 thin film is dominated by the grain surface region, not by the GB [70].

In case of polycrystalline oxide films, GBs contain a high density of defects, which will accumulate the more traps inside the grain regions. A traps present inside the grain may cause a percolation path under a high electric field [65]. In filamentary type conduction, oxygen vacancies/ions would form a filaments throughout the oxide layer (highly conductive path) via GB [71]. Another interpretation of conductive filament's formation is connected with the motion of the O^{2-} ions which usually appears near the crystal defects such as oxygen vacancies and GBs [56, 72, 73]. A filament forming behavior in switching oxide film can be controlled by controlling the grain size underneath the top electrode and smaller grain size indicate the large number of GBs. These types of correlation can be identified by varying the electrode size and the number of GB underneath. However, these correlation becomes are not impactful if electrode size less than the individual grain size [74]. In addition, Das *et al*. have discussed the effect of GBs, GSs, and surface morphology such as (hillocks, lattice mismatch) on the statistical variation of RS parameters (forming voltage, set-reset voltage) in yttria-based resistive switching device (**Figure 2**) [64]. Successive RS operations depend on the inhomogeneous changes in defect structure, and as a result, the switching parameters also vary persistently. During RS process, there are several type of sources in different oxides which provoke variability in device parameters. However, the formation and recombination of oxygen vacancies is highly stochastic in nature and play dominant role in deciding degree of variability. After analyzing the experimental data, Monte Carlo simulation has established a potential stochastic model that relates subsequent RS behavior to the initial states of contact in resistive memory cells [75].

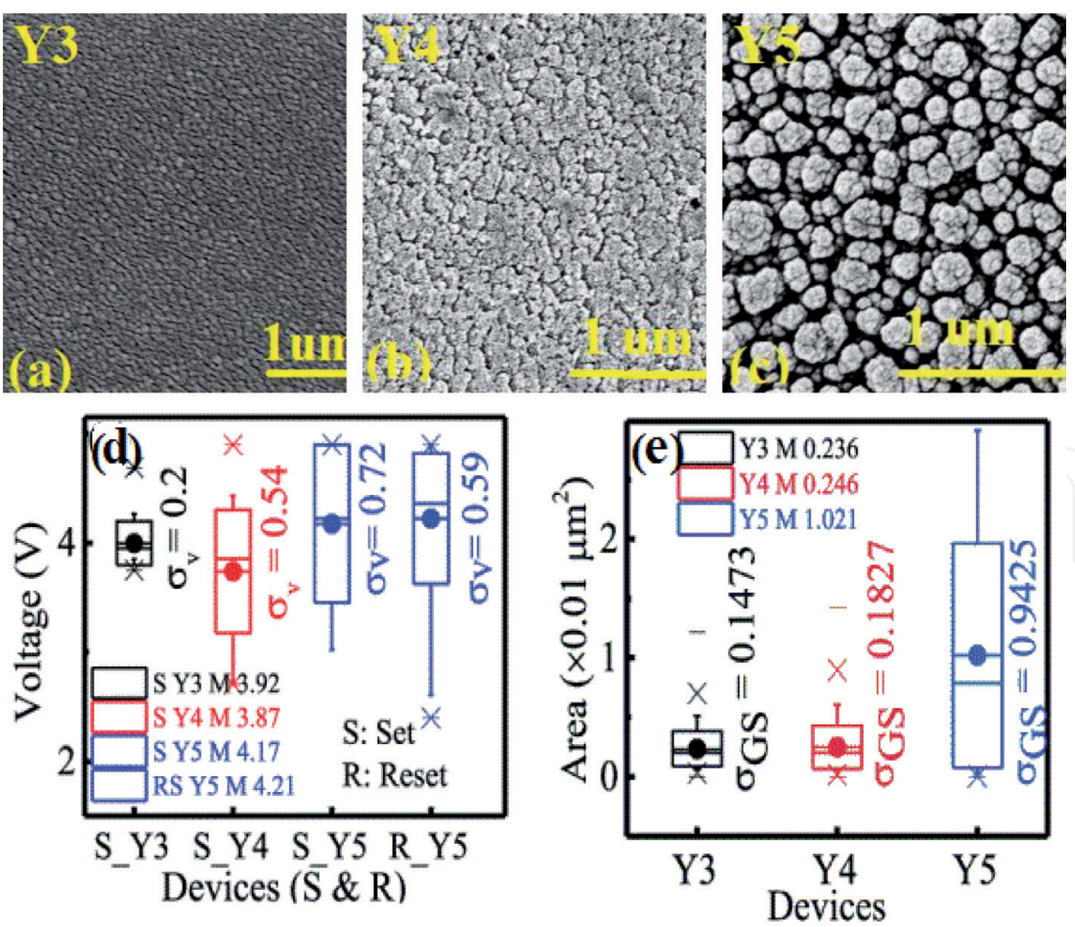

Figure 2.
Yttria layer (~80 nm) is deposited at different substrate temperatures of 300 (Y3), 400 (Y4), and 500°C (Y5) by dual ion beam sputtering system. Scanning electron microscope (FESEM) images of (a) Y3 (b) Y4 (c) Y5. (d) Mean (M) and standard deviation (σ) of the set and reset voltages. (e) Mean (M) and standard deviation (σ) of the grain surface area (figure d and e. reprinted with permission: Ref. [64]).

9. Conclusions

This chapter dealt with different types of resistive switching where the role of interface formation modifying the switching properties was thoroughly discussed. The surface properties of thin films demonstrated significant dependence onto the predominant factors e.g. redox reactions, interface formation along with tunnel barrier thereby affected the device performance. The morphological characteristics of surface across the interface containing GBs and GSs regulated the charge carrier transport due to modified band structure. Owing to relatively high defect concentration at the interface, GBs controlled the leakage current behavior of device.

Conflict of interest

This book chapter is written through contributions of all authors. All authors have given approval to the final version of the manuscript. Mangal Das and Sandeep Kumar is the main author and co-author, respectively. The authors declare no competing financial interest.

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