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Dispersive readout of reconfigurable ambipolar quantum dots in a silicon-on-insulator nanowire Ⓕ

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ABSTRACT

We report on ambipolar gate-defined quantum dots in silicon on insulator nanowires fabricated using a customized complementary metal–oxide–semiconductor process. The ambipolarity was achieved by extending a gate over an intrinsic silicon channel to both highly doped n-type and p-type terminals. We utilize the ability to supply ambipolar carrier reservoirs to the silicon channel to demonstrate an ability to reconfigurably define, with the same electrodes, double quantum dots with either holes or electrons. We use gate-based reflectometry to sense the inter-dot charge transition (IDT) of both electron and hole double quantum dots, achieving a minimum integration time of 160 (100) μs for electrons (holes). Our results present the opportunity to combine, in a single device, the long coherence times of electron spins with the electrically controllable hole spins in silicon.

The spin degree of freedom of single electrons bound to quantum dots in silicon is considered one of the most scalable candidates to host quantum information.[1] By isotopic purification of the material, the Hahn-echo coherence time has been extended up to 28 ms,[2] enabling magnetically driven single and two-qubit control fidelities of over 99.9%[3] and 98%,[4] respectively. All-electrical control of spin qubits via the spin–orbit interaction can be used to achieve faster and more scalable control; however, the intrinsic spin–orbit coupling of electron spins is too weak to induce high-fidelity coherent rotations.[5] In contrast, hole spins are subject to stronger spin–orbit fields, enabling fast two-axis control of the qubit albeit with the drawback of sub-microsecond coherence times.[6–10]

Electron and hole spin qubits have typically been achieved using different host materials and/or gate stacks. Ambipolar devices, able to operate in both electron and hole regimes, are interesting platforms to attempt to combine the best features of both and to explore their performance within the same crystalline environment.[11,12] Ambipolar transport has been previously demonstrated in group IV materials

such as graphene,[13] carbon nanotubes,[14–16] and germanium.[17] In silicon MOS devices, ambipolar quantum dots have been achieved by integrating both n-type and p-type reservoirs in a single device[11,12,18–20] or by tuning the reservoir Fermi energy using NiSi source/drain electrodes.[21] Such ambipolar quantum dots have been studied via direct electrical transport, and recently, ambipolar charge sensing via single-electron and single-hole charge sensors has been demonstrated.[22] However, readout via gate-based sensors[23] or direct dispersive readout via spin projection in double quantum dots[24–26] offers more compact and scalable measurement methodologies with comparable measurement sensitivity and shorter integration time.

In this Letter, we present a silicon nanowire (SiNW) multiple quantum dot device, fabricated with a double poly-silicon gate layer technology, together with ambipolar carrier reservoirs for the supply of either electrons or holes. We demonstrate reconfigurable single and double quantum dots in both n-type and p-type regimes via gate-based dispersive readout.[27] We also discuss the signal-to-noise ratio (SNR) in the detection of inter-dot electron and hole charge

transitions, finding minimum integration times, for SNR = 1, of 160 and 100 μs, respectively.

Figures 1(a)–1(d) show false-colored scanning electron microscopy images and schematic cross sections of the two types of devices studied here, hereinafter named device I and device II. The devices were fabricated on 150 mm silicon-on-insulator (SOI) wafers with a customized CMOS process in VTT's Micronova cleanroom facilities. The process consisted of 8 UV and 3 e-beam lithography layers. The SOI layer was thinned down to 35 nm by thermal oxidation and oxide stripping and patterned to form the nanowires. A 20 nm thermal SiO$_2$ was grown to provide the insulator between the SiNWs and first gate layer. This step reduced the Si layer to its final thickness of 24 nm. The first and second polycrystalline silicon (polysilicon) gate layers, respectively, Poly-1 and Poly-2, have thicknesses 50 nm and 80 nm and were degenerately doped with low energy phosphorous ion implantation. The 35 nm thick SiO$_2$ dielectric layer between the polysilicon gate layers was grown by low-pressure chemical vapor deposition (LPCVD). From van der Pauw structures, we measured the room temperature resistivities of Poly-1 and Poly-2 films to be $\rho_1 = 1.14 \times 10^{-2} \, \Omega \, cm$ and $\rho_2 = 1.9 \times 10^{-3} \, \Omega \, cm$, respectively. Openings through the deposited dielectrics were etched on the source/drain regions of the SOI and phosphorous (n-type) or boron (p-type) implantation was used to dope these regions. A 250 nm thick SiO$_2$ was

deposited with LPCVD, and the wafers were heated to 950 °C to activate the dopants and anneal the dielectrics. Contact holes for all three layers were etched with subsequent dry and wet etching processes. Finally, a metalization layer consisting of 25 nm TiW and 250 nm AlSi was deposited and patterned, and the wafers were treated with a forming gas anneal passivation.
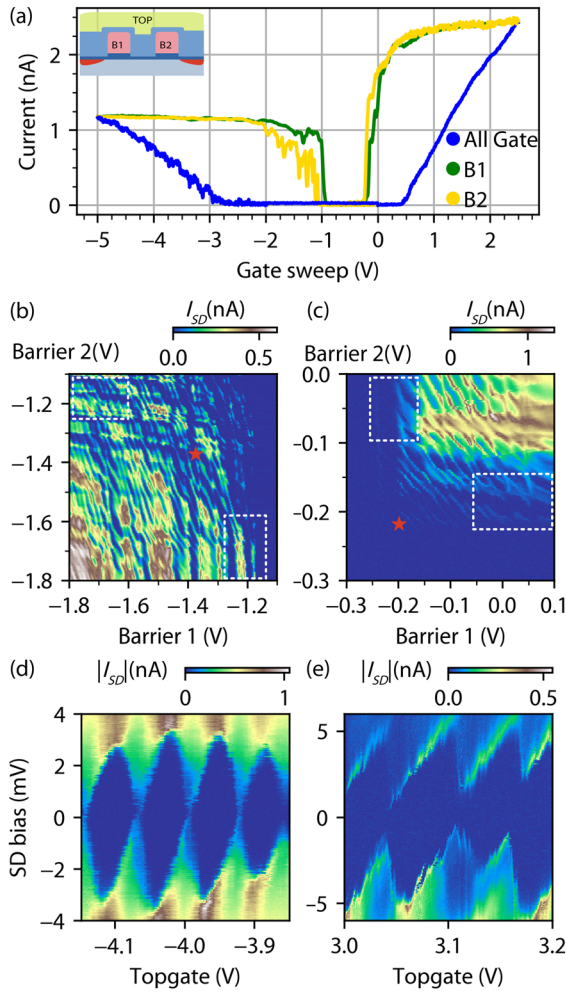
The two devices measured here have an effective SiNW cross section of 24 nm × 24 nm. Device I consists of three polysilicon gates: two in Poly-1, with a gate length of 50 nm and a pitch of 100 nm, and one Poly-2 that covers the SOI area from source to drain. Device II consists of seven gates for the operation of the ambipolar quantum dots. Extension gates 1 and 7 are used to accumulate carriers in the intrinsic silicon connecting the quantum dot "channel" area to the reservoirs. By applying a positive voltage above some threshold $V_{e,th}$, we induce a two-dimensional electron gas (2DEG) in the channel, supplied by the n-type reservoir contact. Conversely, by applying a negative bias below $V_{h,th}$, we induce a two-dimensional hole gas (2DHG) from the p-type reservoir contact, as illustrated in Fig. 1(e). In contrast to the single topgate found in device I, the distinct gates 1 and 7 present in device 2 allow for independent control of the left and right reservoir polarities. Gates 2–6 are used to confine quantum dots and tune tunnel coupling between the dots and the reservoirs. Gates 2, 4, and 6 (Poly-1) wraparound the SiNW and have a gate length of 110 nm. Gates 3 and 5 (Poly-2) have a gate length of 120 nm and nominally overlap the Poly-1 gates by 10 nm.

We use gate-based dispersive readout to sense the charge state of single and double quantum dots in these ambipolar devices. Gate 5 is connected to an LC resonant circuit, consisting of a planar spiral NbTiN superconducting inductor on silicon for high sensitivity reflectometry readout.[27,28] The choice of gate here is motivated by the much lower resistivity for the Poly-2 vs Poly-1 gates, leading to better high-frequency performance, despite the expected lever arm from this gate on the quantum dots being lower. Together with the parasitic capacitance in the circuit, we obtain a resonance at 489.8 MHz with a resonant bandwidth of 1.64 MHz and a loaded quality factor $Q = 300$ and a coupling coefficient $\beta = 0.33$. The NbTiN thin film thickness is 45 nm, and we estimate the total kinetic and geometric inductance of the spiral inductor to be 132 nH.[29] The parasitic capacitance is around 0.8 pF, and a surface-mount capacitor of 0.05 pF was used to decouple the resonator from the line.[27] All measurements were conducted at the dilution refrigerator base temperature of 10 mK.

We first study the quantum dot formation in the SOI channel by measuring the source–drain current of device I, as illustrated in Fig. 2(a). Both n-type and p-type transport currents are measured with a source–drain bias voltage $V_{SD} = 2$ mV applied across the source and drain contacts. Topgate threshold voltages for n-type and p-type conductions are measured to be $V_{e,th} = 0.40$ V and $V_{h,th} = -2.72$ V, respectively. The asymmetry in threshold voltages can be explained by the work function of the n-type doped polysilicon gates. The barrier gates B1 and B2 have much lower threshold voltages $V_{e,th} \simeq -0.2$ V and $V_{h,th} \simeq -1$ V over the SOI channel because of the comparatively thinner gate oxide. From the linear regions of the electrical transport curve in Fig. 2(a), we extract mobilities of $\mu_e = 608.4 \pm 3.4$ cm^2/V s and $\mu_h = 259.8 \pm 1.9$ cm^2/V s at 10 mK showing a similar ratio of μ_e/μ_h to that seen in planar ambipolar devices.[12] We investigate the effect of the individual barrier gates on the electrical transport in Figs. 2(b) and 2(c), including their use to form a quantum dot in the silicon channel. Current peaks with a diagonal slope (see red stars) are
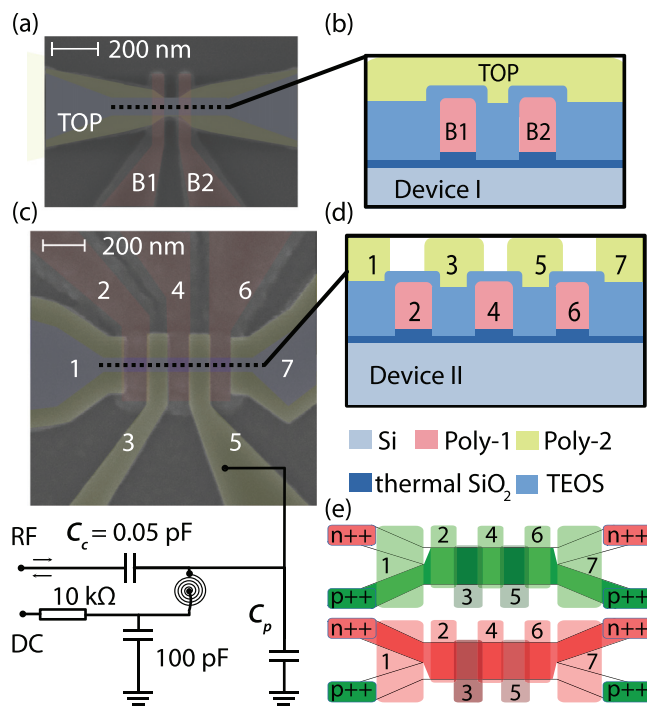
FIG. 1. (a) and (c) False colored scanning electron microscope image of devices nominally identical to device I and device II. Gate 5 of device II is attached to an LC circuit for dispersive readout. (b) and (d) Cartoon cross sections of the stacked silicon channel, oxide and poly-silicon gates along the dashed line in (a) and (c); and (e) schematic of the ambipolar device operation mode, with accumulation of electrons or holes depending on the applied voltage on all the seven gates. Gates 1 and 7 extend from the implanted regions to the channel, while gates 2–6 define the quantum dots which confine single electron or holes.

TABLE I. Electrostatic properties of the ambipolar quantum dots.

Device	QD	E_c (meV)	C_g (aF)	C_s (aF)	C_d (aF)	α
I (Topgate)	Electron	5.4	2.2	25	3	0.074
	Hole	3.2	2.4	30	18	0.048
II (Gate 5)	Electron	17.4	1.7	4.0	3.5	0.18
	Hole	10.6	2.6	12	0.4	0.17

simplification, with total area $50 \times 24 \times 3$ nm^2 (considering three sides of the nanowire) and stated oxide parameters—this suggests that these highly occupied quantum dots are distributed across most of the SiNW cross-sectional area, as opposed to being localized within the SiNW corners.

Device II was similarly measured in transport and using gate reflectometry. Each gate was confirmed to pinch-off the channel [see Figs. 3(a) and 3(b)], while the Coulomb diamonds shown in Figs. 3(c) and 3(d) indicate the formation of electron (hole) quantum dots under gate 5, having been measured with all other gates biased well above (below) the threshold voltage of 3 V (−4.5 V). The measured lever arms and gate capacitances for this ambipolar quantum dot under gate 5 are presented in Table I. These Coulomb diamonds are

FIG. 2. Quantum dot formation in device I: (a) transport characteristics of device I, sweep of all gate kept at the same voltage (blue), sweep of barrier gate (B1,B2), while other gates kept at well above threshold voltage(2.5V for n-type and −5 V for p-type), the inset shows the schematic of double barrier gated nanowire (device I). (b) p-type transport current as a function of each barrier gate B1, B2 at $V_{Top} = -4.5V$. (c) n-type transport current as a function of each barrier gate B1, B2 at $V_{Top} = 3V$. (d) transport measurement of p-type channel taken at B1 = −1.38 V, B2 = −1.38 V [⋆ in (b)], (d) transport measurement of n-type channel taken at B1 = −0.20 V, B2 = −0.22 V [⋆ in (c)].
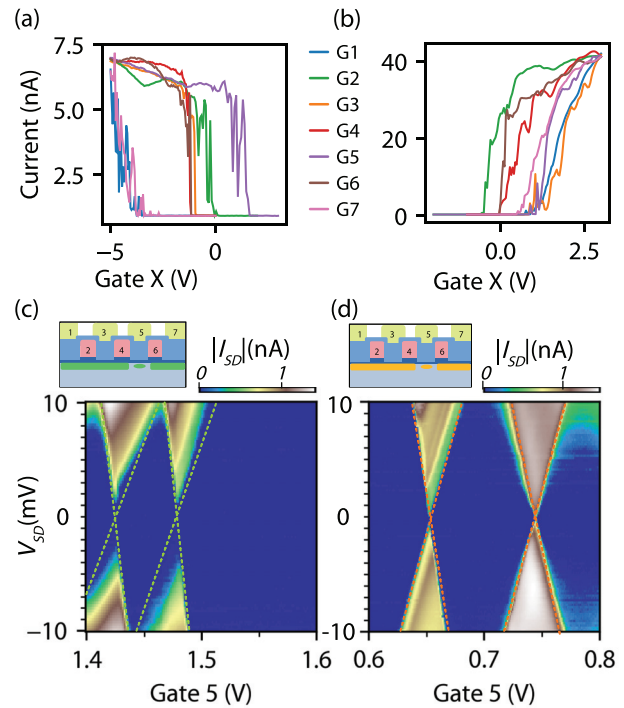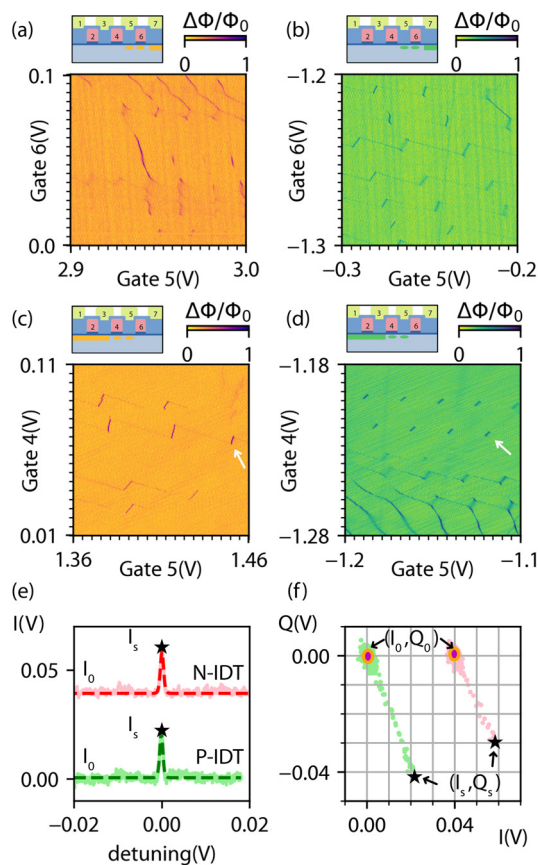
attributed to a quantum dot formed between two barrier gates, coupled similarly to B1 and B2. Quantum dots can also form under the B1 and B2 gates themselves, thanks to the natural confinement from the silicon nanowire, as can be seen in the vertical and horizontal current peaks (white boxes). From charge stability measurement at fixed barrier voltages shown in Figs. 2(d) and 2(e), we observe regular Coulomb diamonds corresponding to the central quantum dot in both electron and hole regimes, with respective charging energies $E_{C,e} \simeq 5.4$ meV and $E_{C,h} \simeq 3.2$ meV. From these measurements, we can extract capacitance values and gate lever arms for electron and holes, as summarized in Table I. The gate capacitance values are consistent with a nominal estimate of 2.5 aF based on a parallel-plate capacitor

FIG. 3. Ambipolar transport Device II: (a) p-type transport measurement ($V_{SD} = 2$ mV) as a function of each gate where all other gates were biased at −4.5 V. (b) n-type transport measurement ($V_{SD} = 2$ mV) as a function of each gate where all other gates were biased at 3 V. (c) p-type source to drain current I_{SD} as a function of Gate 5 and V_{SD} when other gates were biased at −4.5 V. (d) n-type source to drain current I_{SD} as a function of Gate 5 and V_{SD} when other gates were biased at 3 V.

measured in the few-carrier regime, and correspondingly, the dot-lead capacitance values are much smaller than for the highly occupied quantum dots studied in device I. As a result, the gate capacitance dominates and the gate lever arms α are larger. Given the nominal 110 nm gate length in device II, the measured gate capacitances indicate a smaller effective area of the quantum dot, suggesting that these few-carrier dots are now localized in the top corners of the SiNW cross section. Similar measurements (shown in supplementary material Fig. S1) using gate 4—which is located in the Poly-1 layer, with much thinner oxide—yield a larger lever arm of $\alpha_e = 0.50$.

Finally, we demonstrate reconfigurable ambipolar double quantum dots and measure them dispersively. In Figs. 4(a)–4(d), we present multiple ambipolar double quantum dot scenarios: Double electron or hole quantum dots located either under gates 5 and 6 (with the source reservoir off), or under gates 4 and 5 (with the drain reservoir off).

The stability diagram for each scenario is measured by monitoring the normalized phase difference, $\Delta\Phi/\Phi_0$, between the incoming and outgoing radio frequency signals from the resonator, where Φ_0 is the maximum phase difference. The IDTs within the pair of quantum dots are visible in all four different configurations. No IDTs were observed between dots formed under non-adjacent gates—the tunnel barriers formed under gates 2, 4, or 6 were evidently too opaque due to their length. The magnitude of the dispersive response at the IDT is important for spin readout based on the Pauli spin blockade since it determines the maximum signal.[24–26] In Fig. 4(e), we take two line traces of the IDT reflectometry signal from both electron double quantum dots and hole double quantum dots, illustrated by the arrows in Figs. 4(c) and 4(d), and filter the demodulated quadrature and in-phase signals with a notch-filter at 16 kHz to suppress a noise peak attributed to the audio component of the pulse tube of the dilution refrigerator.[30] We show the scatterplot of these detuning-dependent traces in (I, Q) space in Fig. 4(f), the dispersive peak at (I_s, Q_s) can be identified in the complex plane, facilitating the extraction of the SNR.[24,31] We calculate the SNR as

$$\frac{(I_s - I_0)^2 + (Q_s - Q_0)^2}{2\sigma_S^2},$$

where I_0 and Q_0 are, respectively, the in-phase and quadrature component mean of the signal background and σ_s is the average 2D standard deviation of the background noise, which can be seen as the radius of the dot around the noise background in the inset of Fig. 4(f). We obtain $\mathrm{SNR_{e,IDT}} = 49.8$ and $\mathrm{SNR_{h,IDT}} = 52.9$, indicating that our measurement configuration should provide a minimum integration time, for SNR = 1, of $\tau_e = 160\,\mu s$ and $\tau_h = 100\,\mu s$ for electrons and holes, respectively. The introduction of a tunable tunnel coupling in the ambipolar double dot could be used to develop a more generalized comparison of the dispersive readout SNR for electron and hole IDTs. This sensitivity could be further enhanced by performing reflectometry using a gate in the Poly-1 layer: the larger lever arms of such gates should give an improvement factor of $\left(\frac{\alpha_{e,Poly-1}}{\alpha_{e,Poly-2}}\right)^2 \simeq 9$. Operating at a higher reflectometry frequency (e.g., 1.8 GHz) should yield a $\sim 5\times$ SNR improvement due to reduced parasitic capacitance,[31] while further improvements using a Josephson parametric amplifier[28] and critically coupled resonator could bring the integration time down to $\tau = 100$ ns, which is close to the state-of-art dispersive charge readout 10 ns.[31,32]

In conclusion, we have fabricated and experimentally demonstrated reconfigurable ambipolar quantum dots in an SOI multi-gate nanowire transistor. There is a good evidence suggesting observation of the last hole/electron in the quantum dot, but a more robust confirmation requires magneto spectroscopy to examine shelling filling or spin filling experiments. This work demonstrates several core ingredients, which could be used to benchmark electron and hole spin qubits in the same silicon device, including RF readout of the IDT, which is the basis of Pauli-blockade based spin measurement. Furthermore, the availability of gate-based reflectometry opens up the possibility of new types of studies in such ambipolar silicon devices. In silicon, ambipolar p–n double quantum dot formation is challenging to measure through direct transport current due to the large silicon bandgap—RF readout of the dot-lead charge transition can enable neighboring quantum dots to be sensed as in the capacitive shift of sensor transition, at zero source–drain bias.[33] Furthermore, the same

FIG. 4. Ambipolar double dots: (a)–(d) different ambipolar double dot configurations and its corresponding charge stability diagrams (a) electron double dots under gates 5 and 6, (b) hole double dots under gates 5 and 6, (c) electron double dots under gates 4 and 5, (d) hole double dots under gates 4 and 5; see supplementary material Fig. S2 for full page view (a)–(d). (e) line trace and fit of homodyne quadrature signal I across IDT in n-type double dot (red, offset by 0.04 V) and p-type(green) measured with input power $P_c = -92$ dBm. (f) Scatter plot of line trace from both quadrature signals in I-Q plane, signal peak (I_s, Q_s) of the line-fit($\star$), 2D standard deviation of background I-Q signal. We used a 10 kHz low-pass filter to filter the homodyne quadrature signal IQ and took the average over 300 traces to obtain a sufficient SNR.

dot-lead charge transition detected by RF reflectometry can provide an accurate measure of the reservoir temperature,[34] enabling comparative studies of the electron and hole interactions with phonons within the same nanostructure.

See the supplementary material for the lever arm for the Poly-1, Poly-2 gate of multi-dot device.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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